Deep Level Assessment of n-Type Si/SiO_2 Metal-Oxide-Semiconductor Capacitors with Embedded Ge Quantum Dots

M. Aouassa,[1] H. Vrielinck,[2] and E. Simoen[2,3,*,z]

[1] *LMON, Faculté des Sciences, Monastir 5019, Tunisia*
[2] *Department of Solid State Sciences, Ghent University, B-9000 Ghent, Belgium*
[3] *Imec, B-3001 Leuven, Belgium*

This paper reports on a Deep-Level Transient Spectroscopy (DLTS) study of n-type silicon Metal-Oxide-Semiconductor capacitors with Ge Quantum Dots (QDs) embedded in a SiO_2 gate dielectric. For a zero-dot reference and in capacitors fabricated with a 1, 2 or 3 nm amorphous Ge layer similar spectra have been obtained. They are characterized by a peak at or above room temperature for a bias pulse in depletion and by an electron trap around 200 K, which is shown to be associated with dangling bond acceptor states at the Si/SiO_2 interface. The maximum density of states increases with average Ge QD size, while the average activation energy, corresponding with the peak maximum position shifts to lower values. Although no direct evidence of electron tunneling to the Ge QDs has been found so far, there is a marked impact of their presence on the Capacitance-Voltage characteristics, resulting in an increase in the accumulation capacitance with QD size, a shift of the flatband voltage toward more positive gate bias and a counterclockwise hysteresis, associated with the charging and discharging of QD levels and related Ge traps in the SiO_2.
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Device structures with silicon or germanium Quantum Dots (QDs) embedded in an oxide matrix may find application in the field of Non-Volatile Memories (NVMs)[1,2] or photonics.[3–5] In the former case, the QDs can become charged by tunneling of electrons or holes from the silicon substrate through a tunnel oxide. Successful operation requires that the charge does not leak away by the assistance of traps or defects in the material stack or by thermally-assisted tunneling to the substrate.[6,7] In fact, QDs embedded in a semiconductor or oxide matrix behave in many aspects like giant traps, so that their defect levels can be studied by capacitance-voltage (C-V) measurements at different frequency (f) and temperature (T),[8–12] also called admittance spectroscopy[13,14] and by capacitance transient-based techniques,[15–32] like Deep-Level Transient Spectroscopy (DLTS).[14,33] This enables the assessment of hole and electron emission from the levels associated with QDs, revealing their energy position and capture cross section for thermally stimulated carrier processes. The contribution of field-assisted tunneling to carrier release from the QDs can be studied by changing the reverse bias over the junction, containing the nanodots.

In the present work, we report on a systematic investigation of Metal-Oxide-Semiconductor (MOS) capacitors fabricated on n-type Czochralski silicon substrates and containing Ge QDs with different size. In order to distinguish deep level centers in the silicon depletion region from the ones at the silicon/SiO_2 interface,[14] DLT-spectra have been recorded for different bias pulses from a reverse bias V_R to a pulse bias V_P, accounting for the shift in the flatband voltage (V_{FB}) of the capacitors. The latter defines the onset of electron accumulation at the interface. It is shown that both in the zero-dot reference sample and in the Ge QD capacitors, two prominent features are present: a peak in the 150–200 K range which is most likely related to so-called dangling bond P_b centers and a peak at or above room temperature, which could be related to the so-called minority carrier generation in a MOS capacitor.[34,35] The main impact of the presence of the Ge QDs is the change in the V_{FB} toward more positive values with increasing QD size and indicating the introduction of negative charge and, secondly, the increase in the counterclockwise hysteresis in the C-V curves between a forward and a reverse bias sweep, which is a fingerprint of more pronounced charge trapping.

Experimental

An amorphous Ge layer with well-controlled thickness of 1, 2 or 3 nm was deposited by Molecular Beam Epitaxy (MBE) at low temperature (<100°C) on a 5 nm tunnel oxide, thermally grown on an n-type Czochralski silicon wafer. The Ge QDs on the SiO_2 thermal layer were obtained using an in situ dewetting process at solid state by Ultra-High Vacuum (UHV) heating at a temperature of 730°C for 30 min. An Atomic Force Microscopy (AFM) picture is given in Fig. 1, showing a high density ($>10^{11}$ cm^{-2}) of Ge QDs. Their average size increases with the thickness of the deposited amorphous Ge layer. Next, 50 nm of SiO_2 was deposited. A reference without QDs was also made. MOS capacitors were obtained by thermal evaporation of 2 mm diameter Al gate contacts on the SiO_2, while InGa eutectic+In foil ohmic contacts were made on the silicon substrate side. The device structure is schematically shown in Fig. 2.

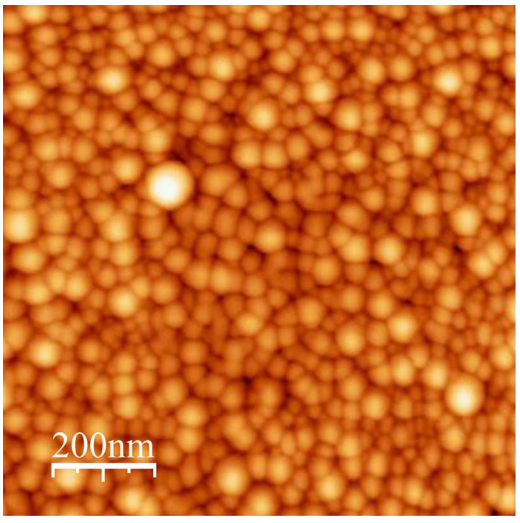

Figure 1. Atomic Force Microscopy picture of a 3 nm Ge layer QD sample deposited by MBE on a 5 nm SiO_2 tunnel oxide, after 730°C annealing under UHV for 30 min.

*Electrochemical Society Fellow.
[z]E-mail: eddy.simoen@imec.be

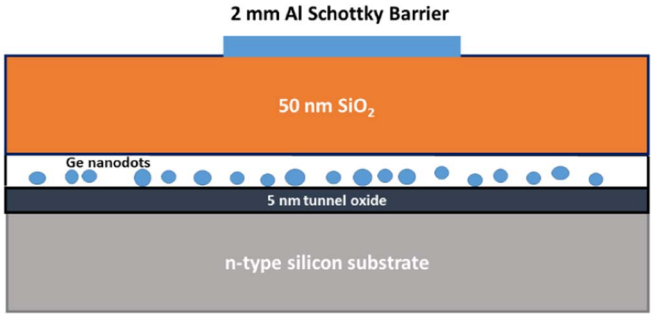

Figure 2. Schematic cross section of the studied MOS capacitors with embedded Ge QD.

Capacitance-Voltage (C-V) characterization was performed at a fixed frequency f = 1 MHz, using both a forward and reverse gate voltage sweep. The gate leakage current is negligible both in forward (from depletion to accumulation) and reverse bias direction. The C-V graph for the zero-dot reference capacitor is represented in Fig. 3. From the deep depletion part, the doping density N_D has been derived, based on the slope of a dC^{-2}/dV_R versus V_R plot. Typical uniform values in the range between 2 and 8×10^{15} cm^{-3} were derived for the studied samples. The accumulation capacitance C_{ox} corresponds to $\varepsilon_{ox}\varepsilon_0 A/t_{ox}$ and should reach about 1500 pF for a $t_{ox} = 55$ nm, which is in good agreement with the results in Fig. 3. A is the gate area (= 3.14 mm^2), ε_{ox} is the dielectric constant of SiO_2 and ε_0 is the permittivity of vacuum.

DLTS was performed using a Fast-Fourier Transform (FFT) based system,[36] with the samples mounted in a liquid-nitrogen cryostat, where the temperature was varied between 75 K and 320 K. In addition, isothermal scans at room temperature (RT) were also carried out, where the sampling period t_w was varied between 1 ms and 1 s. Measurements were performed employing different bias pulses from V_R to V_P in order to scan different parts of the MOS structure.[37–39] For a bias pulse in depletion, mainly deep levels in the silicon depletion region, with a possible contribution from interface states, are probed. Pulsing to V_{FB} or beyond (more positive bias) emphasizes the contribution of the interface states in the upper half of the bandgap and possibly also populates so-called border traps in the SiO_2.[2,14,40–43] In

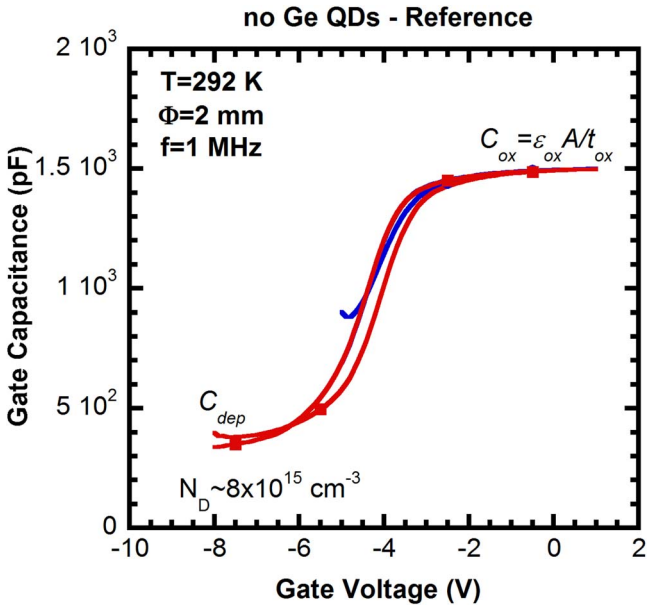

Figure 3. Capacitance-Voltage (C-V) plot at a frequency of 1 MHz and room temperature for the zero-dot reference sample.

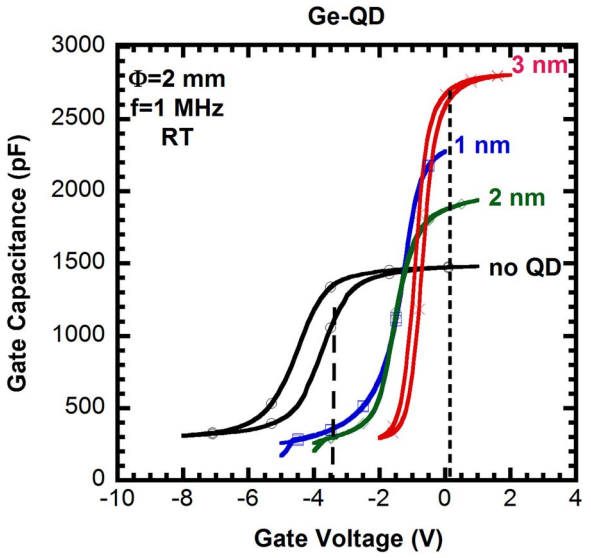

Figure 4. Capacitance-Voltage (C-V) plot at a frequency of 1 MHz for the zero-dot reference and the three samples with embedded nanodots fabricated with an a-Ge layer thickness of 1, 2 and 3 nm.

the latter case, carrier capture is expected to proceed through inelastic tunneling, according to the logarithm of the pulse time t_p. This corresponds with the progression of the tunneling front with time deeper into the oxide.[40–44]

Results and Discussion

Comparing the C-V plots in Fig. 4 for the different Ge QD sizes, a few trends become clear. First, the C_{ox} value increases from around 1500 pF for the zero-dot reference to about double this value for 3 nm dots. This could be related to the presence of a 3 nm Ge-like layer with a dielectric constant of 16 in 55 nm SiO_2. However, the capacitance for a 3 nm Ge layer is about 100 times higher than for 55 nm SiO_2, so that it has a negligible effect on the total series capacitance. Since A and t_{ox} should be the same in all cases, the presence of the Ge dots must have an impact on the permittivity of the overall gate stack. Next, the V_{FB} of the capacitors becomes more positive for capacitors with larger Ge QDs. This suggests the presence of negative charge, stored in the Ge dots or in traps in the SiO_2. Based on a V_{FB} increase (ΔV_{FB}) of 4.0 V for the 3 nm capacitor, a rough estimate of the negative charge density of $\Delta V_{FB} \times C_{ox}/q \sim 7 \times 10^{10}$ cm^{-2} can be derived, which is comparable with the density of nanodots of $\sim 10^{11}$ cm^{-2}. Finally, the hysteresis also tends to increase with nanodot size, although, unexpectedly, the reference samples appears to have the strongest hysteresis. The origin of this is not clear for the moment but could be linked to the absence of a forming gas annealing (FGA) after deposition, which leaves a high density of dangling bond states not passivated.

Figure 5 represents the T-scan spectra for the reference sample, corresponding with different bias pulses. For the spectrum in deep depletion from −8 V to −4 V, a peak at 300 K is found, while an electron trap shifting from about 250 K to 200 K is observed when pulsing into accumulation. The latter trap(s) should be more representative for deep levels at the Si/SiO_2 interface or possibly border traps in the gate dielectric. As the samples have not been passivated by a FGA, the most likely candidates for the observed electron trap(s) are the silicon dangling bond acceptors ($P_b^{0/-}$) in the upper half of the bandgap.[38,39,45–49] Oxide traps in the lower quality 50 nm deposited SiO_2 correspond with rather large tunneling times, if they are deeper than 5 nm from the interface, practically excluding this explanation.

The 1-nm Ge nanodot sample exhibits qualitatively the same behavior as the reference capacitor (Fig. 6). It shows that in deep depletion, there is a broad peak between 150–250 K which could stem from

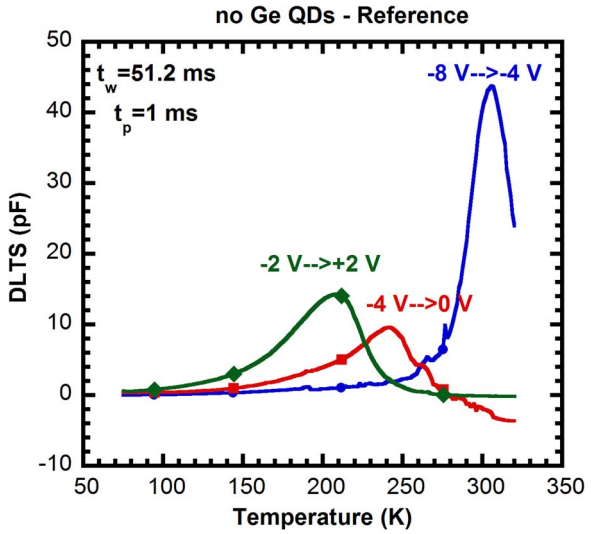

Figure 5. DLT-spectra for a reference capacitor without Ge QDs, corresponding with different bias pulses on the gate. This enables to separate bulk silicon from interface traps.

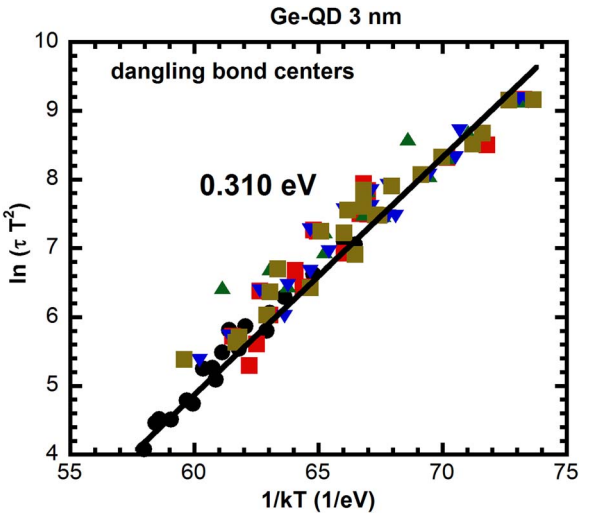

Figure 7. Arrhenius plot for the 3 nm Ge QD sample, corresponding with the most prominent interface peak and for a pulse from −1 V to +1 V and different pulse durations: 1 ms and $t_w = 51.2$ ms) (●); 10 μs and $t_w = 512$ ms (▼); 100 μs and $t_w = 521$ ms (brown squares); 1 ms and $t_w = 512$ ms (red squares); 10 ms and $t_w = 512$ ms (▲).

the response of filled interface traps. The increase found at and above room temperature may originate from minority carrier generation in the depletion region.[2,14,34,35] The latter response differs from a true electron emission spectrum and is typical for a MOS capacitor, biased in deep depletion. It originates from the minority carrier generation either by thermal Shockley-Read-Hall (SRH) carrier generation by deep levels in the depletion region or by the diffusion of minority carriers (holes) from the neutral region toward the negatively biased gate. Holes will be collected at the Si/SiO_2 interface to build up an inversion layer, so that the depletion capacitance will increase until C_{ox} after a sufficiently long relaxation time. This leads thus to an increasing capacitance transient, which is similar to the one which corresponds with the thermal emission of captured electrons by an electron trap in the depletion region, although the basic mechanism is different. At room temperature and for a good quality substrate, this process should take several minutes if not more and will accelerate exponentially at higher temperatures, with an expected activation energy of $E_G/2$ (SRH dominated) or E_G (diffusion dominated) (E_G the silicon bandgap).[34,35]

The potential DLTS amplitude can be very large, since the transient amplitude may reach up to C_{ox}-C_{dep} and will depend on the applied emission time constant window, i.e., on the sampling period t_w. The minority carrier response will be more pronounced for longer t_w. The fact that a pronounced minority carrier generation peak is observed for the reference samples indicates a rather strong SRH generation and a rather poor quality of the Si/SiO_2 interface.

The Arrhenius plot in Fig. 7, corresponding with 3 nm Ge dots reveals an activation energy of 0.31 eV with respect to the conduction band. This is close to what is expected for the dangling bond ($P_b^{0/-}$) acceptor level.[45–49] It is clear, however, from a comparison of the spectra in Fig. 8 that the energy position changes with the size of the quantum dots. The maximum temperature is the lowest for the 3 nm dots (∼180 K), while it is around 200 K or higher for the zero-dot reference or the 1 and 2 nm case. The Arrhenius plots of Fig. 9 confirm the shift of the activation energy from about 0.44 eV for the no QD reference sample to 0.31 eV for the 3 nm counterpart. This

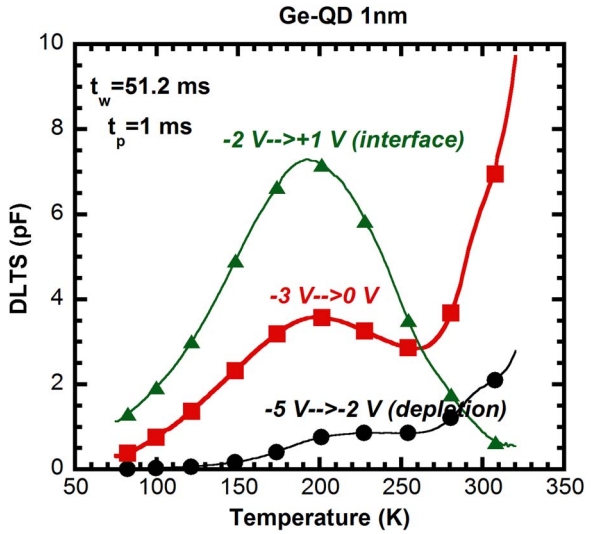

Figure 6. DLT-spectra for a 1 nm Ge QD capacitor corresponding with different bias pulses on the gate. This enables to separate the bulk silicon response from that of interface traps.

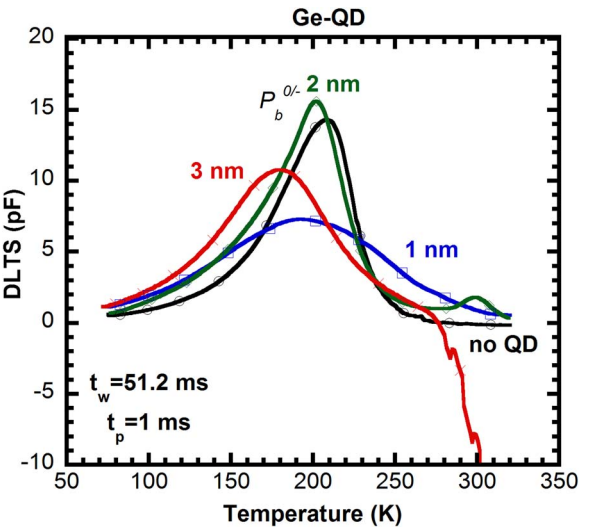

Figure 8. DLT-spectra for all cases studied and corresponding with a bias pulse near accumulation, i.e., probing the interface. The spectra correspond with a no QD reference (black); 1 nm (blue); 2 nm (green) and 3 nm (red).

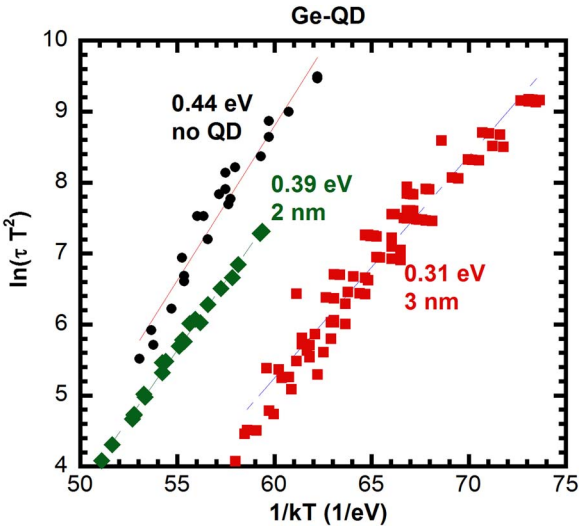

Figure 9. Arrhenius plot corresponding with the electron traps at the Si/SiO_2 interface, for the no QD, the 2 nm and the 3 nm Ge QD sample.

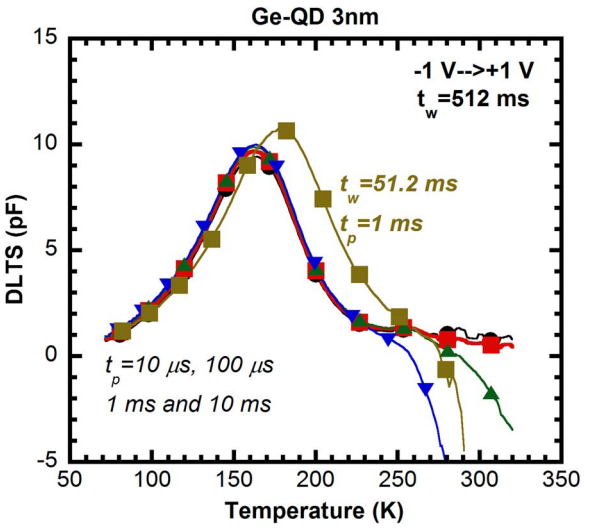

Figure 10. DLTS spectra for a 3 nm Ge QD capacitor from −1 V to +1 V, using a sampling period $t_w = 512$ ms and pulse durations from 10 μs to 10 ms. A reference spectrum, corresponding with $t_w = 51.2$ ms and $t_p = 1$ ms is also included.

suggests some impact of the presence of Ge on the energy position of the supposed Si/SiO_2 interface states.

At the same time, the width of the peak increases for increasing QD size. Broad DLTS peaks are usually associated with a number of overlapping independent deep levels or with a distribution of energy levels associated for example with an extended defect.[14] One way to figure out which of these possibilities is the most relevant one, measurements as a function of pulse duration are helpful. As will be seen below, the evidence points to a point-defect origin of the spectra in Fig. 8, so that the width of the peaks suggest an overlap of different types of point defects. One possibility is that the presence of an increasing amount of Ge with QD size at the Si/SiO_2 interface creates different types of dangling bond centers, whereby one or more Ge atoms replace the silicon back-bond atoms in the P_b centers.[50]

The density of interface states (D_{it}) can be derived from the DLTS amplitude according to:[14,38,44]

$$D_{it} = (\varepsilon_0 \varepsilon_{Si} A C_{ox} N_D \Delta C)/(\beta k_B T C_R{}^3) \quad [1]$$

with ε_{Si} the dielectric constant of silicon, k_B Boltzmann's constant and C_R the depletion capacitance, corresponding with a reverse bias V_R. The factor β is derived from the Full Width at Half Maximum of a typical FFT DLTS peak and defines the energy resolution; it is on the order of 2.5.[44] The maximum densities derived from Fig. 8 are estimated in the range of 6×10^{11} $cm^{-2}eV^{-1}$ for the 3 nm QD sample. This is at least one decade higher than for a well-passivated $Si-SiO_2$ interface, where mid gap interface state densities on the order of 10^{10} $cm^{-2}eV^{-1}$ can be achieved.

A final observation is the fact that the DLTS amplitude of the interface state peak is constant for a pulse duration in the range of 10 μs to 10 ms (Fig. 10), when applying a bias pulse into accumulation. This indicates that the electron traps are completely filled for a pulse of 10 μs, imposing a lower limit for the electron capture cross section of about 5×10^{-17} cm^2. Similar behavior was found for the other types of samples studied. From this, it can be concluded that the electron traps behave like point defects, supporting their identification as centers at the Si/SiO_2 interface and not border trap in the oxide or extended defects in the silicon substrate.

Summarizing, DLTS of n-type silicon MOS capacitors, with Ge nanodots embedded in the SiO_2 gate dielectric mainly reveal electron traps associated with interface states around 200 K in the spectra and a minority carrier generation peak at or above room temperature, dominating the spectrum for a bias pulse in depletion. The impact of the Ge dots on the spectra is not so clear: there is no evidence for the occurrence of tunneling to and from the QDs in the oxide, which should lead to signals whose amplitude increases according to a tunneling process, i.e., with $\ln(t_p)$.[40–44] Such tunneling processes have been found in the past for Ge dots embedded in SiO_2 by low-frequency noise spectroscopy,[51] where the QDs where placed at about 2 nm from the interface. The fact that the distance here is 5 nm, resulting in longer time constants probably explains the absence of such features in the present study. At the same time, it has been shown that the presence of Ge-related traps and QDs in the gate oxide affects the flatband voltage, the oxide capacitance and the counterclockwise hysteresis of the C-V curves at 1 MHz. The effects generally become more pronounced for increasing average QD size.

A final comment should be made with respect to the negative feature around room temperature in the spectra for the 3 nm Ge QD sample (Figs. 8 and 11). Measuring the DLTS amplitude as a function of the pulse duration reveals an unusual pronounced negative peak for $t_p > 1$ ms. Negative DLTS bands are normally associated with minority carrier peaks (hole traps in n-type silicon). The occurrence of hole emission at room temperature after a sufficiently long bias pulse appears to be rather unlikely. Alternatively, a negative peak

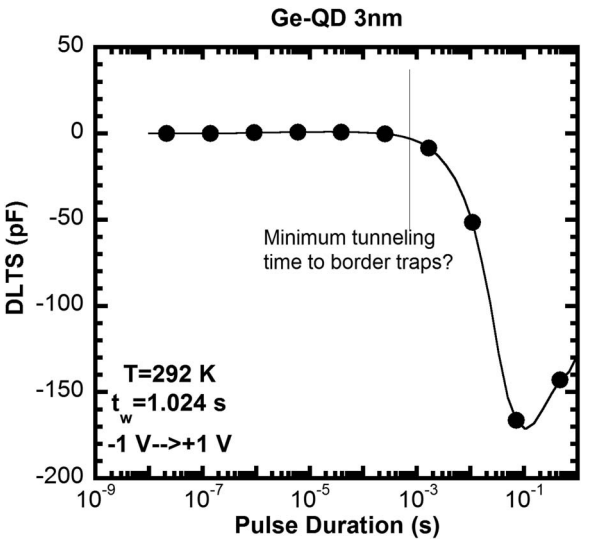

Figure 11. DLTS amplitude as a function of the pulse duration at 292 K and for a pulse from −1 V to +1 V for a 3 nm Ge QD MOS capacitor.

could result from net electron capture, with capture times in the range of 1 ms to 1 s. Such a range of capture times could result from tunneling of electrons toward traps in the oxide. Considering a tunneling time given by:[43]

$$\tau = \tau_0 \exp(\alpha z) \quad [2]$$

with τ_0 the SRH recombination lifetime at the Si-SiO_2 interface and α the decay parameter of the electron wave function in SiO_2 yields depths z in the range of 1 nm to 2 nm, if we assume $\tau_0 = 10^{-10}$ s and $\alpha = 10^8$ cm^{-1}. This suggests the presence of Ge-related electron traps in the 3 nm Ge QD sample within 1 to 2 nm from the interface. These are not necessarily connected with QD states, which are expected at a higher distance from the interface, but they can degrade the charge retention of memories and should, therefore, be further studied in more detail. In fact, it is well-documented that Ge segregates to the Si/SiO_2 interface after a high-temperature annealing step, thus creating a high density of interface states.[52–54] Another question is in how far FGA can passivate these Ge-related DB states and border traps in order to improve the MOS capacitor characteristics.

Conclusions

DLTS of n-type silicon MOS capacitors with Ge QDs embedded in the SiO_2 gate dielectric reveal the presence of a high density of interface states, associated with unpassivated dangling bonds. The electrical parameters of these electron traps change with the size of the QDs, indicating the presence of Ge atoms at the interface. These interface states can serve as intermediate stepping stones for the elastic tunneling of charge out of the QDs, followed by fast thermal emission to the conduction band and should, therefore be controlled, for example by a forming gas anneal. The main impact of the Ge QDs on this peak is a shift of its maximum position from around 200 K to 180 K, suggesting some chemical effect on the electron traps at the interface. In addition, a feature related to the minority carrier response is found for a bias pulse in depletion. At the same time, the presence of germanium QDs and related traps in the oxide markedly affects the C-V characteristics at 1 MHz: both the flatband voltage, the hysteresis and the accumulation capacitance change with the average QD size, revealing the negative charging of the corresponding levels.

References

1. S. Tiwari, H. Hanafi, A. Hartstein, E. F. Crabbe, and K. Chan, *Appl. Phys. Lett.*, **68**, 1377 (1996).
2. R. Beyer, J. von Borany, and H. Burghardt, *Microelectron. Eng.*, **86**, 1859 (2009).
3. J. von Borany, R. Grötzschel, K. H. Heinig, A. Markwitz, W. Matz, B. Schmidt, and W. Skorupa, *Appl. Phys. Lett.*, **71**, 3215 (1997).
4. D. A. Grachev, A. V. Ershov, A. V. Belolipetsky, L. V. Krasilnikova, A. N. Yablonskiy, B. A. Andreev, and O. B. Gusev, *Phys. Status Solidi A*, **213**, 2867 (2016).
5. S. Siontas, P. Liu, A. Zaslavsky, and D. Pacifici, *Appl. Phys. Lett.*, **109**, 053508 (2016).
6. M. Geller, C. Kapteyn, L. Müller-Kirsch, R. Heitz, and D. Bimberg, *Appl. Phys. Lett.*, **82**, 2706 (2003).
7. L. Bonato, E. M. Sala, G. Stracke, T. Nowozin, A. Strittmatter, M. N. Ajour, K. Daqrouq, and D. Bimberg, *Appl. Phys. Lett.*, **106**, 042102 (2015).
8. G. Medeiros-Ribeiro, D. Leonard, and P. M. Petroff, *Appl. Phys. Lett.*, **66**, 1767 (1995).
9. G. Medeiros-Ribeiro, J. M. Garcia, and P. M. Petroff, *Phys. Rev. B*, **56**, 3609 (1997).
10. P. N. Brunkov, A. R. Kovsh, V. M. Ustinov, Yu. G. Musikhin, N. N. Ledentsov, S. G. Konnikov, A. Polimeni, A. Patanè, P. C. Main, L. Eaves, and C. M. A. Kapteyn, *J. Electron Mater.*, **28**, 486 (1999).
11. R. Wetzler, A. Wacker, E. Schöll, C. M. A. Kapteyn, R. Heitz, and D. Bimberg, *Appl. Phys. Lett.*, **77**, 1671 (2000).
12. A. J. Chiquito, Yu. A. Pusep, S. Mergulhão, J. C. Galzerani, and N. T. Moshegov, *Phys. Rev. B*, **61**, 5499 (2000).
13. D. L. Losee, *J. Appl. Phys.*, **46**, 2204 (1975).
14. E. Simoen, J. Lauwaert, and H. Vrielinck, *Semiconductors and Semimetals*, Eds. L. Romano, V. Privitera, and C. Jagadish, 91, pp. 205, Elsevier 2015.
15. M. M. Sobolev, A. R. Kovsh, V. M. Ustinov, A. Yu. Egorov, A. E. Zhukov, M. V. Maksimov, and N. N. Ledentsov, *Semicond.*, **31**, 1074 (1997).
16. C. M. A. Kapteyn, F. Heinrichsdorff, O. Stier, R. Heitz, M. Grundmann, N. D. Zakharov, D. Bimberg, and P. Werner, *Phys. Rev. B*, **60**, 14265 (1999).
17. Z. -Q. Fang, Q. H. Xie, D. C. Look, J. Ehret, and J. E. Van Nostrand, *J. Electron. Mater.*, **28**, L13 (1999).
18. R. Magno, B. R. Bennett, and E. R. Glaser, *J. Appl. Phys.*, **88**, 5843 (2000).
19. H. Pettersson, C. Pryor, L. Landin, M. -E. Pistol, N. Carlsson, W. Seifert, and L. Samuelson, *Phys. Rev. B*, **61**, 4795 (2000).
20. C. M. A. Kapteyn, M. Lion, R. Heitz, D. Bimberg, C. Miesner, T. Asperger, K. Brunner, and G. Abstreiter, *Appl. Phys. Lett.*, **77**, 4169 (2000).
21. H. L. Wang, D. Ning, H. J. Zhu, F. Chen, H. Wang, X. D. Wang, and S. L. Feng, *J. Cryst. Growth*, **208**, 107 (2000).
22. W. -H. Chang, W. Y. Chen, C. Y. Lai, T. M. Hsu, N. -T. Yeh, and J. -I. Chyi, *Phys. Rev. B*, **64**, 125315 (2001).
23. V. V. Ilchenko, S. D. Lin, C. P. Lee, and O. V. Tretyak, *J. Appl. Phys.*, **89**, 1172 (2001).
24. E. Gombia, R. Mosca, P. Frigeri, S. Franchi, S. Amighetti, and C. Ghezzi, *Mater. Sci. Engin. B*, **91**, 393 (2002).
25. O. Engström, M. Malmkvist, Y. Fu, H. Ö. Olafsson, and E. Ö. Sveinbjörnsson, *Appl. Phys. Lett.*, **83**, 3578 (2003).
26. S. Schulz, S. Schnüll, Ch. Heyn, and W. Hansen, *Phys. Rev. B*, **69**, 195317 (2004).
27. S. W. Lin, C. Balocco, M. Missous, A. R. Peaker, and A. M. Song, *Phys. Rev. B*, **72**, 165302 (2005).
28. S. Schulz, A. Schramm, Ch. Heyn, and W. Hansen, *Phys. Rev. B*, **74**, 033311 (2006).
29. M. Kaniewska, O. Engström, A. Barcz, and M. Pacholak-Cybulska, *Mater. Sci. Engin. C*, **26**, 871 (2006).
30. J. S. Kim, E. K. Kim, J. O. Kim, S. J. Lee, and S. K. Noh, *Superlatt. and Microstruct.*, **46**, 312 (2009).
31. T. Asano, Z. Fang, and A. Madhukar, *J. Appl. Phys.*, **107**, 073111 (2010).
32. V. -T. Rangel-Kuoppa, A. Tonkikh, P. Werner, and W. Jantsch, *Appl. Phys. Lett.*, **102**, 232106 (2013).
33. D. V. Lang, *J. Appl. Phys.*, **45**, 3023 (1974).
34. N. O. Pearce, B. Hamilton, A. R. Peaker, and R. A. Craven, *J. Appl. Phys.*, **62**, 576 (1987).
35. S. N. Volkos, E. S. Efthymiou, S. Bernardini, I. D. Hawkins, A. R. Peaker, and G. Petkos, *J. Appl. Phys.*, **100**, 124103 (2006).
36. S. Weiss and R. Kassing, *Solid-State Electron*, **31**, 1733 (1988).
37. C. Gong, E. Simoen, N. Posthuma, E. Van Kerschaever, J. Poortmans, and R. Mertens, *Appl. Phys. Lett.*, **96**, 103507 (2010).
38. E. Simoen, C. Gong, N. E. Posthuma, E. Van Kerschaver, J. Poortmans, and R. Mertens, *J. Electrochem. Soc.*, **158**, H612 (2011).
39. E. Simoen, A. Rothschild, B. Vermang, J. Poortmans, and R. Mertens, *Electrochem. and Solid-St. Lett.*, **14**, H362 (2011).
40. P. Van Staa, H. Rombach, and R. Kassing, *J. Appl. Phys.*, **54**, 4014 (1983).
41. D. Vuillaume, J. C. Bourgoin, and M. Lannoo, *Phys. Rev. B*, **34**, 1171 (1986).
42. H. Lakhdari, D. Vuillaume, and J. C. Bourgoin, *Phys. Rev. B*, **38**, 13124 (1988).
43. E. Simoen, H. -C. Lin, A. Alian, G. Brammertz, C. Merckling, J. Mitard, and C. Claeys, *IEEE Trans. Device and Mater. Reliab.*, **13**, 444 (2013).
44. E. Simoen, V. Ferro, and B. J. O'Sullivan, *J. Appl. Phys.*, **116**, 234501 (2014).
45. E. H. Poindexter, G. J. Gerardi, M. -E. Rueckel, P. J. Caplan, N. M. Johnson, and D. K. Biegelsen, *J. Appl. Phys.*, **56**, 2844 (1984).
46. D. Vuillaume and J. -C. Bourgoin, *J. Appl. Phys.*, **58**, 2077 (1985).
47. H. G. Grimmeiss, W. R. Buchwald, E. H. Poindexter, P. J. Caplan, M. Harmatz, G. J. Gerardi, D. J. Keeble, and N. M. Johnson, *Phys. Rev. B*, **39**, 5175 (1989).
48. D. Vuillaume, D. Goguenheim, and G. Vincent, *Appl. Phys. Lett.*, **57**, 1206 (1990).
49. R. Beyer, H. Burgardt, I. Thurzo, D. R. T. Zahn, and T. Geßner, *Solid-State Electron*, **44**, 1463 (2000).
50. A. Stesmans, T. Nguyen Hoang, and V. V. Afanas'ev, *J. Appl. Phys.*, **116**, 044501 (2014).
51. S. Ferraton, J. Zimmermann, L. Montès, G. Ghibaudo, J. Brini, J. Gurgul, and J. A. Chroboczek, *Proc. Noise in Devices and Circuits II*, Eds. F. Danneville, F. Bonani, M. J. Deen, and E. Levinshtein, SPIE Vol. 5470, p. 560 (2004).
52. F. K. Le Goues, R. Rosenberg, T. Nguyen, F. Himpsel, and B. S. Meyerson, *J. Appl. Phys.*, **65**, 1724 (1989).
53. J. von Borany, R. Grötzschel, K. H. Heinig, W. Matz, B. Schmidt, and W. Skorupa, *Appl. Phys. Lett.*, **71**, 3215 (1997).
54. E. S. Marstein, A. E. Gunnæs, A. Olsen, T. G. Finstad, R. Turan, and U. Serincan, *J. Appl. Phys.*, **96**, 4308 (2004).