STUDY OF ELECTRICALLY ACTIVE DEFECTS IN EPITAXIAL LAYERS ON SILICON

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ABSTRACT

Electrically active defects in silicon-based epitaxial layers on silicon substrates have been studied by Deep-Level Transient Spectroscopy (DLTS). Several aspects have been investigated, like, the impact of the pre-epi cleaning conditions and the effect of a post-deposition anneal on the deep-level properties. It is shown that the pre-cleaning thermal budget has a strong influence on the defects at the substrate/epi layer interface. At the same time, a post-deposition Forming Gas Anneal can passivate to a large extent the active defect states. Finally, it is shown that application of a post-deposition anneal increases the out-diffusion of carbon from a Si:C stressor layer into the p-type CZ substrate.

INTRODUCTION

A crucial step in silicon epitaxy is the preparation of a clean silicon surface prior to the deposition [1]. The removal of oxygen and carbon contamination is essential for a defect-free growth of good quality layers. However, besides the structural integrity of the epi layer, one should also be concerned with the presence of grown-in point defects, which may affect their electrical properties (resistivity, carrier lifetime,...). Previous Deep-Level Transient Spectroscopy (DLTS) studies have revealed several types of defects, which are usually ascribed to impurities present at the interface between the substrate and the epi layer [2]-[4]. Here, DLTS will be applied to address point-defect-related issues in silicon-based epi layers on silicon substrates.

EXPERIMENTAL DETAILS

Three sets of Chemical Vapor Deposition (CVD) epitaxial layers will be discussed, focusing on different aspects. In a first case study, the impact of the pre-epi clean procedure (*ex situ* HF dip in combination with *in situ* bake) will be explored, as there is a tendency to reduce the overall thermal budget during CVD. Here, the impact of the pre-epi bake temperature in the range of 750 °C-850 °C will be discussed. The effect of a post-deposition Forming Gas Anneal (FGA) on the deep-level spectra is studied in a second case, where a standard 850 °C pre-epi bake of p-Si is followed by a 500 °C deposition from SiH_4. FGA is performed at 500 °C for 5 min. A third set of samples focuses on blanket Si:C stressor layers on p-Si substrates, in order to investigate the presence of interstitial carbon (C_i) related deep levels in the underlying p-type Czochralski (CZ) Si substrate. As will be shown, the concentration of a C_i-related peak at 0.4 eV above the valence band edge E_V increases significantly after an 800 °C anneal, indicating that substitutional carbon is lost from the stressed Si:C layer by transforming into C_i and related complexes, followed by diffusion into the CZ silicon substrate.

Processing details can be found, respectively in Refs. [4], [5] and [6]. Different device structures have been utilized to enable DLTS: either a p-n junction [4], a Metal-Oxide-Semiconductor (MOS) capacitor, based on Al_2O_3 gate dielectric or an Al Schottky barrier, evaporated on the Si:C epi layer.

RESULTS AND DISCUSSION

In order to evaluate the impact of different types of pre-epi cleaning on the epitaxial quality, 400 nm 1×10^{17} cm^{-3} B-doped Si layers have been deposited on n-type CZ Si substrates [4]. An *ex situ* HF clean was followed by a High Temperature Bake (HTB) in H_2 for a temperature in the range 750 to 850 °C. For one wafer, no pre-epi bake has been performed. As shown in Fig. 1, a broad distribution of electron traps can be observed at the interface/junction with the n-type substrate; their density-of-states is highest for the HF dip only (no bake) junction, based on the corresponding broader and higher peak. The origin is thought associated with residual impurities at the epitaxial interface, which become less effectively removed by the lower bake temperature [2]-[4]. At the same time, the corresponding junction leakage current increases significantly, for lower bake temperature, as demonstrated by Fig. 2. It indicates that an

increasing density of generation centers occurs in the depletion region and at the epitaxial interface.

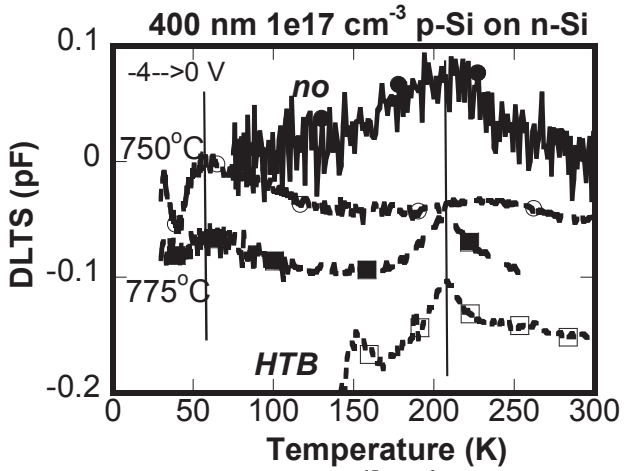

Figure 1: DLT-spectra of 1×10^{17} cm^{-3} B doped Si epi layers on n-type silicon substrates, corresponding with different pre-epi bake temperatures. HTB: high-temperature bake at 1000 °C. A bias pulse from -4 V to 0 V has been applied. The spectra have been shifted in vertical direction for clarity.

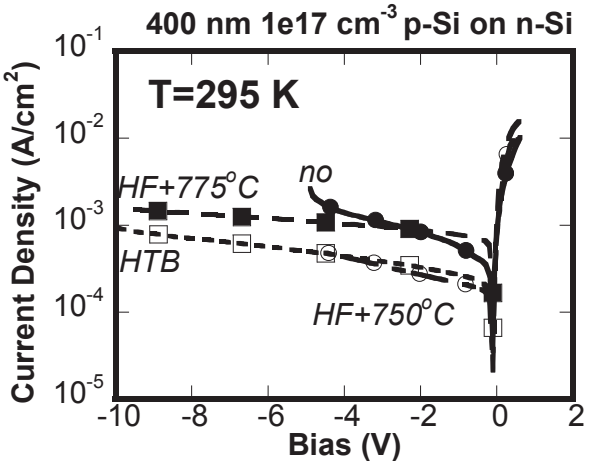

Figure 2: Current-Voltage characteristics at room temperature of p^+-n junctions fabricated by CVD deposition, using an ex situ HF clean, followed by a pre-epi bake at different temperatures.

It is clear that using a high-temperature pre-bake, gives rise to good-quality silicon epi layers. This is confirmed by the results of Figs 3 and 4, corresponding with 30 nm of silicon CVD at 500 °C. The resulting epi layers, with p-type behavior based on the polarity of the MOS capacitor C-V measurements, exhibit a low density of deep levels. According to the frequency scan of Fig. 3, a broad distribution of hole traps, present in the depletion region of the MOS capacitor, has been detected. The bias pulse conditions in Figs 3 and 4 are such that the DLT-spectra are dominated by hole traps in the depletion layer in the p-type silicon substrate + epi layer, suppressing the contribution from traps at the Si-SiO_2 interface. After a FGA at 500 °C, most of the deep level defects present in the substrate/epi-layer have been passivated. This is confirmed by the flat temperature-scan spectrum in Fig. 4, corresponding with a bias pulse in depletion from 3 V-->2 V.

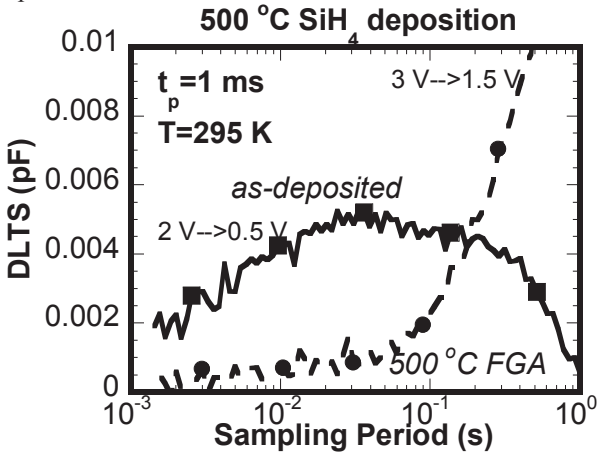

Figure 3: DLT-spectra at room temperature of low-temperature CVD p-type silicon on a p-Si substrate before and after a 500 °C FGA for 5 min. A filling bias pulse of 1 ms has been applied.

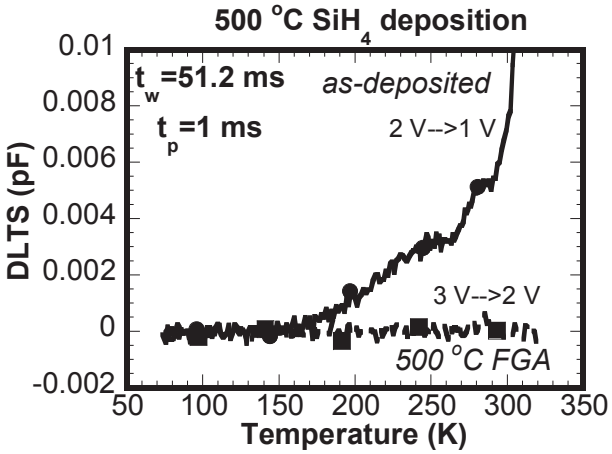

Figure 4: T-scan spectra of low-temperature CVD p-type silicon on a p-Si substrate before and after a 500 °C FGA for 5 min. A pulse period t_w=51.2 ms and a filling pulse time t_p=1 ms has been employed. The reverse bias of the measurements reflects the shift in flat band voltage of the capacitors upon annealing at 500 °C.

DLTS is also useful to investigate defects associated with the deposition of stressor layers, like, e.g., Si:C, which is useful for imparting tensile strain in n-channel Si bulk FinFETs [7]-[10]. In the case of undoped Si:C epi layers, the reverse bias pulse in DLTS probes mainly the p-type Si substrate for the presence of C_i-related species, diffused in from the 97 nm epi layer with a targeted

substitutional C content of 1.6%. Measurements have been performed after deposition and following annealing at 800 ^{o}C for 15 min under N_2. Al Schottky barriers have been evaporated, enabling DLTS evaluation. For the as-grown material, a single hole trap with activation energy of 0.4 eV above the valence band edge is detected in Fig. 5, which most likely corresponds to the C_iO_i peak in CZ Si [11],[12]. The trap concentration increases roughly by a factor of 10 after 800 ^{o}C RTA in Fig. 6, indicating that more interstitial carbon species diffuse into the substrate. At the same time, it will be shown that larger C-related clusters give rise to a deeper band of hole traps closer to the epitaxial interface. This can partly explain the observed loss in strain of the stressor layer after annealing [6],[13].

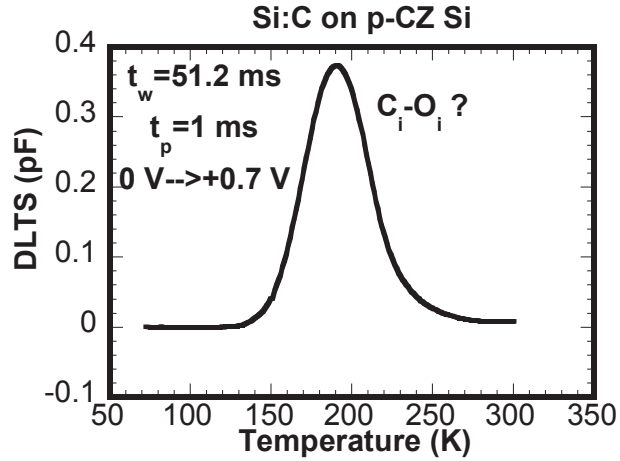

Figure 5: T-scan DLTS of an as-deposited Si:C epilayer on a p-type Si substrate at a bias pulse from 0 V to +0.7 V.

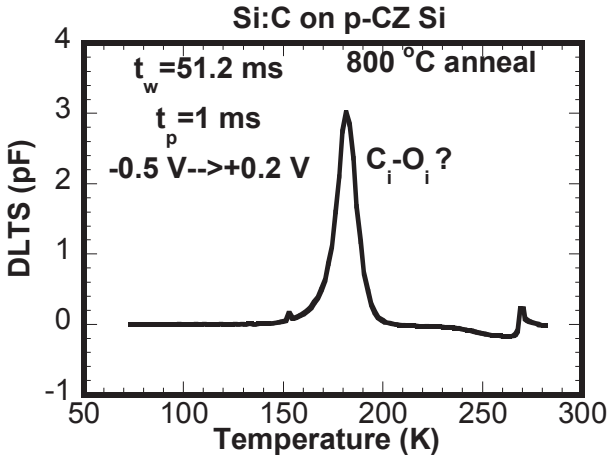

Figure 6: T-scan DLTS of an 800 ^{o}C annealed Si:C epi layer on a p-type Si substrate at a bias pulse from -0.5 V to +0.2 V.

CONCLUSIONS

In summary, it is clear that DLTS is useful in the study of electrically active point (and extended) defects in silicon epitaxial layers. A basic prerequisite, however, is the fabrication of proper device structures for addressing either the epi layer and/or the interface with the substrate.

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