Universitá di Pisa

Facoltá di Ingegneria

Corso di Laurea Specialistica in Ingegneria Elettronica

Tesi di Laurea

Analysis and Architecture Design of DSPACE, a Digital Signal Processor for space applications

Candidato
Alessandro Vincenzi

Relatore
Prof. Luca Fanucci

Relatore
Prof. Sergio Saponara

Anno Accademico 2010–2011

In ricordo di Eleonora

ABSTRACT

The request of digital signal processing performed on satellites or spacecraft is greatly increased in past years, however the European Space Agency (ESA) has not got a suitable device for these applications made in Europe area. ESA is currently forced to address to United States (US) made alternatives but the exportation of those devices is restricted by the International Traffic in Arms Regulations (ITAR) and this places ESA in a dependent position.

The DSPACE project aim to solve this lack providing a new Digital Signal Processor (DSP), as an intellectual property, and a software tool-chain to exploit its features.

The first part of this thesis work regarded an analysis of the state-of-the-art and the practical solutions in order to identify a target technology and a reference architecture.

The second part of this work concerned a detailed definitions of the DSPACE core architecture and features. Moreover a complete decode & dispatch VHDL model, with a formal functional verification, was realized.

The third part of this work regarded two caches modelling, the instruction and the data cache, that are two essential components of the DSPACE core.

This thesis work was concluded with the first functional simulations coming from the DSPACE model and considerations about the resource occupation of the core.

CONTENTS

LIST OF FIGURES

LIST OF TABLES