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High-Voltage Integrated Circuits design and validation for automotive applications

Thesis

Giuseppe Pasetti

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Tutors:	Prof. Luca Fanucci
	Prof. Roberto Saletti
	Ing. Riccardo Serventi
Candidate:	Giuseppe Pasetti

Abstract

Electronic Integrated Circuits (ICs) are an important pillar of the automotive market, especially since legal and safety requirements have been introduced to manage vehicles emissions and behaviors. Furthermore, the harsh environment and the tight safety requirements, summed with the market that is pushing to reduce the development lead time and to increase the system complexity, require to develop dedicated ICs for the automotive applications.

This thesis presents some peculiar high-power and high-voltage ICs for automotive applications that have been studied, designed and developed taking into account all the requirements that automotive grade ICs have to respect, with emphasis on performance, quality and safety aspects. Particularly the thesis reports the design and validation of power management blocks and output drivers for inductive loads, showing how to fulfill in an effective way the performance, quality and safety targets according to the guidelines and the constraints of the latest automotive standards, like ISO26262 and AEC-Q100.

All the designed ICs has been simulated and manufactured, including layout drawings, in a 0.35 μm HV-CMOS technology from AMS. The effectiveness and robustness of the proposed circuits has been validated on silicon and corresponded measurement results has been reported.

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1 Introduction

Since the last fifty years, the importance of electronics in automotive environment is constantly increasing, driven by the continuous requests to develop new safety and infotainment devices. This has led to a constant increase of the number of electronic devices and control units (ECUs) in the modern cars and today several hundreds of different ECUs can be found in a car, each one specialized to do a different task[1, 2, 3]. This has led to the need to develop automotive specific integrated circuits (ICs), that have to operate in that harsh environment[4]. Indeed, compared with standard consumer ICs, automotive grade integrated circuits have very different environment requirements. The first simple mind environment difference is the ambient temperature[5]. Just think that cell phones have to work at maximum 60°C, when they are operating in the Sahara desert, while all the engine related electronics have to work normally with a temperature above 100°C. The operating temperature and many other environment differences can cause standard consumer ICs to fail when trying to operate in the automotive field. Table1.1 shows the main differences between those two environments.

Table 1.1: Consumer vs Automotive semiconductor requirements

Parameter	Consumer	Automotive
Temperature	0 to 40°C	−40 to 150°C
Maximum Voltages	3.3 to 5V	> 70V
Power	< 5W	up to 10W
Operation time	1-3 years	up to 25 years
Humidity	Low	0% to 100%
Tolerated Field Failure Rate	< 1000 ppm	target: zero defect
ESD	4-8kV	4-8kV IC level

Indeed, since electronics are used to control also the safety parts of the ve-

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hicle, like braking and steering systems, it is very important to guarantee the highest quality level and a "zero defect" rate during all the lifetime of those safety related systems.

On the other hand, the market is constantly pushing to implement new features increasing the complexity of the electronics in the vehicle. This has led to an increased number of electronic systems and stringent requirements for those systems.

For these reasons, the designer of automotive ICs has to take care of a huge number of different requirements, making its work very difficult. In fact, during the development phase of automotive ICs, the designers not only have to guarantee the functionality over the operative range of supply voltages and temperature, but have to take care of the absolute voltage and temperature ratings and consider the very stringent requirements about the IC and system level Electrostatic Discharge (ESD) protection performances and about the Electromagnetic Immunity (EMI) and Compatibility (EMC) of the IC and of the whole system.

Indeed, especially in the high voltage periphery part of automotive ICs, the absolute maximum rating can be very different from the operative. Spikes and surges events, which can appear in automotive environment, can seriously damage the Integrated Circuit if they are not correctly managed and filtered. Furthermore, automotive ICs have to avoid damages and manage correctly the permanent reverse battery condition, condition in which the supply voltage can stay below ground without time limitation, and the loss of ground event, when the ground connection is lost. In this case the ICs must detect it and signal it to the driver.

Moreover, as many different devices are close in the car, it is very important that every device don't disturb and don't be disturbed by the others. Indeed in the automotive environment, the devices are close together and shares the same supply and this can led the arise of issues when they operates concurrently.

To avoid or limit these kinds of issues, the designer has to take care of the stringent requirements of EMI and EMC. Those aspects are very difficult to predict and simulate, as they mainly deal from parasitic components at IC and

PCB level and must be solved as high-frequency wave transmission simulator instead of circuit simulator.

Furthermore the designer has to check the operative region of every device to guarantee the target lifetime of the IC, recognizing possible weak devices and doing all the necessary modifications in order to increase the whole IC lifetime. Last but not least, like every battery powered system, the designer has to implement power saving techniques. Those techniques are necessary to reduce the total power consumption, increasing the discharge time of the battery when the engine is turned off and reducing the fuel consumption and CO₂ emissions when the engine is running.

As said before, since the importance of electronics is constantly increasing in modern car, the main car makers and semiconductor suppliers have established the international Automotive Electronics Council (AEC) with the task of establishing common part-qualification and quality-system standards. The AEC has defined the international AEC-Q100 standard, covering the quality requirements for automotive integrated circuits.

Actually, every electronic system that is sold for automotive application needs to fulfill all the requirements defined in the AEC-Q100 standard, and then those requirements must be well considered in the development phase of automotive ICs.

At the end, during the development of automotive integrated circuits, there are many different forces that drive the design phase, that can be divided into three main sectors: the *performances*, the *quality* and the *safety*.

The rule of the designer is to balance those forces, finding the best solution for the target application and with the given requirements.

Indeed, there is not only one solution for every problem, but it can change depending on the system requirements. The good designer must be able to find the best approach for a given problem, modifying the system architecture and defining the needed performances for the single blocks that compose it.

1.1 Design for Performances

Designing for performances means to increase the overall performances of the IC. It can be done in several ways, like reducing the power consumption or implementing new functions.

Indeed in the automotive environment, the market, which is constantly pushing for innovative and cost-effective electronic systems, demands always more complex Integrated Circuits while at the same time requires to reduce the power consumption.

One important performance parameter is the power consumption. In fact, the car makers, to reduce the fuel consumption, need to reduce the total power consumption of the electronics in the car and one of the most important parameter for them to choose an electronic system is the power dissipation.

Another important parameter is the system cost. One way to reduce it is to integrate on the same die different functions, reducing the number of electronic ICs. This requires large design effort, because, when many systems are integrated on the same die, the interferences and the noise between them can reduce the overall system performances.

1.2 Design for Quality

Designing for the quality means to take all the necessary actions to ensure that the electronic part is working correctly and doing the one for which it was designed.

Those countermeasures permit to identify and discard the faulty devices, that are not working correctly at test, and the possible weak devices, that are functional at test but can reveal a latent fault during the device lifetime.

In order to reach the "zero defect" target, a combination of design, test and qualification must be mixed together, identifying all the possibles weaknesses

from the early stage of the system design and implementing all the needed countermeasures to solve that. For this, many standardized design methodologies have been implemented and they have been widely analyzed in literature[6, 7, 8, 9]:

- Design for Test (DFT)
- Design for Manufacturability (DFM)
- Statistical Analysis
- High Temperature Operating Life (HTOL)
- Burn-in / High Voltage Stressing

Design for Test

Testing ICs permits to locate and screen failing devices and having a complete coverage at test is necessary to reach the "zero defect" rate. The DFT is in charge to increase the observability and controllability coverage at test, adding special structures like the SCAN chain or testing analog multiplexer to have the possibility to read-out the voltage on internal nodes.

Design for Manufacturability

The DFM is based on the data of previous products from silicon foundry and permits to increase the production yield, implementing basic countermeasures on possible production related failures. For instance, they can cover metal sizing and spacing to limits the short and open failures related to the metal.

Statistical Analysis

The applying of statistical analysis during the test of the devices permits to recognize weak devices that have all parameters inside the specifications. For instance, PAT (Part Average Testing) method calculates the tester limits based on the statical distribution of the previous devices. In this way is possible to screen the devices that have some parameters far away from the other devices.

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This can lead to a shorter lifetime, so screening those devices permits to increase the lifetime of device.

High Temperature Operating Life

The HTOL test is a reliability test and permits to estimate the lifetime of the device. That test requires the application of high temperature and voltage stress on the semiconductor devices over long periods for a small sample size, accelerating the aging of the devices and highlighting lifetime issues. This permits to evaluate the lifetime and failure rate of the larger population[10]. In fact, that test is very important to calculate the FIT (Failure In Time) and MTTF (Mean Time To Failure), which can estimate the lifetime of the semiconductor devices.

Burn-in / High Voltage Stressing

Those techniques permits to identify the latent defects, accelerating their manifestation, while operating at high temperature, during Burn-in, or at high voltage, in case of High Voltage Stressing.

1.3 Design for Safety

Designing for the safety means to take all the necessary actions that prevent harms and injuries to the users of the electronic system, when a fault condition occurs.

In this case, it is investigated the effect of a single or multiple faults on the system behavior and are minimized all the possible causes of injuries for the users.

Recently, a new automotive standard for functional safety, mainly focused on electrical/electronic systems mounted on series of passenger cars, has been developed: the *ISO26262 Road vehicles – Functional safety* standard[11].

That standard derives from the Industry Functional Safety standard IEC61508[12],

but has been adapted for the automotive Electric and Electronic industry. Like the IEC61508[13], the ISO26262 rely on the following assessments on the risk:

- Zero risk can never be reached
- Safety aspects must be considered from the beginning
- Non-tolerable risks must be reduced

Furthermore, compared with the IEC61508, the ISO26262 introduces the idea of controllability, which can be synthesized in the ability to avoid hazardous events by the action of the driver[14, 15].

In fact, the ISO26262 provides an automotive specific lifecycle and defines the necessary activities to do for each stage of the lifecycle, requiring to keep record of all the safety-related activities during the entire lifetime of automotive electronic systems, from the early design to the out-of-production phases.

The ISO26262 standard defines an automotive-specific risk-based approach for determining risk classes (Automotive Safety Integrity Levels, ASILs) and divides the ASILs into four different levels: from the ASIL-A level, which corresponds to fails that can cause no safety issues and has the lowest safety requirements, to ASIL-D, related to fails that can hazard the driver in case of failure and requiring the highest safety requirements, passing through ASIL-B and ASIL-C with intermediate safety requirements.

Each ASIL level specifies the necessary safety requirements, has its own process and defines the different steps for item development to achieve an acceptable residual risk, the residual probability of fault after that all ISO26262 actions has been taken.

The ASIL level depends on the combination of assessments[16] of:

- Severity
- Exposure
- Controllability

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The **Severity** indicates the grade of possible injuries that the fault can generate and is divided into four grades: from **S0**, which relies on non safety-related failures, to **S3**, which coincides on faults that can generate life-threatening or fatal injuries.

The **Exposure** indicates the probability that the fault can occur. In the ISO standard, five different grades are defined: from **E0**, which means situations that occur less then once in the vehicle lifetime, to **E4**, which means situations that occurs during almost every drive on average.

The **Controllability** indicates the needed driver skills to avoid harm when the fault occurs. It is divided in four grades: from **C0** to **C3**, while **C0** means that all driver or other traffic participants can avoid a specific harm and **C3** means that less than 90% or more of all driver or other traffic participants are usually able to avoid a specific harm.

Driven by the car makers requirements, in short time, this ISO standard is becoming the new reference for all the new developed electronic systems.

The ISO26262 requirements, that are related to the whole electronic system, can be easily reported to the requirements for the ICs that builds the system. In this case, the standard FMEDA approach can be successful[17, 18, 19].

1.4 Scope and organization of the thesis

The scope of this thesis work is to present the design and validation phases of innovative high voltage CMOS integrated circuits for automotive applications. During this thesis, all the aspects of the automotive design flow will be faced, focusing on the main difficulties that the IC designers will have to face to reach a working device and highlighting the chosen system architecture and the designed circuitry. All those are shown taking a look to the needed actions to satisfy the new ISO26262 requirements.

More in detail, in chapter 2 is shown the development of an automotive DC-DC buck voltage regulator with integrated power switch and very low current

consumption.

Chapter 3 describes the development and validation phases of two drivers for inductive loads. The first driver is designed to drive relays or solenoid valves, while the second is especially designed to drive the excitation of the rotor in automotive alternators.

Chapter 4 shows the development and validation phases of an high-power Intelligent Power Switch (IPS) that can be used as LED driver in automotive applications. The IPS has been integrated as driver for the alternator warning lamp indicator.

Chapter 5 shows an innovative way to develop an alternator voltage regulator, indicating the major difficulties that designers meet and highlighting an innovative way to overcome them.

The research leading to the results described in section 3.2, chapter 4 and chapter 5 has received founding from the European Community's Seventh Framework Programme under grant agreement n°216436 (project ATHENIS).

2 HV IC design for automotive switching regulators

In this chapter the development phase of a buck DC-DC switching regulator for automotive applications is presented.

More in detail, Section 2.1 analyzes the voltage regulators, highlighting its application; section 2.2 shows the development of a switching voltage regulator and, finally, section 2.3 highlights the validation phase of the regulator, with simulation data and measurements on silicon.

2.1 Switching voltage regulators

Each electronic device needs to be supplied by a stable supply voltage to operate correctly. The devices that generate that supply voltage are called voltage regulators. Indeed, those devices generate a constant DC voltage, that can be used to supply other electronic devices, starting from an unstable and unregulated supply voltage.

Each voltage regulator can be divided into three main blocks: the power processor, the controller and the voltage reference, as shown in Fig. 2.1.

The power processor is the block that regulates the power flow from the input port to the output port. The voltage reference is the block that generates a temperature stabilized reference voltage, for instance a bandgap voltage generator. The controller is the block that generates the control signal for the power processor comparing the output voltage with the reference, in order to minimize the difference between them.

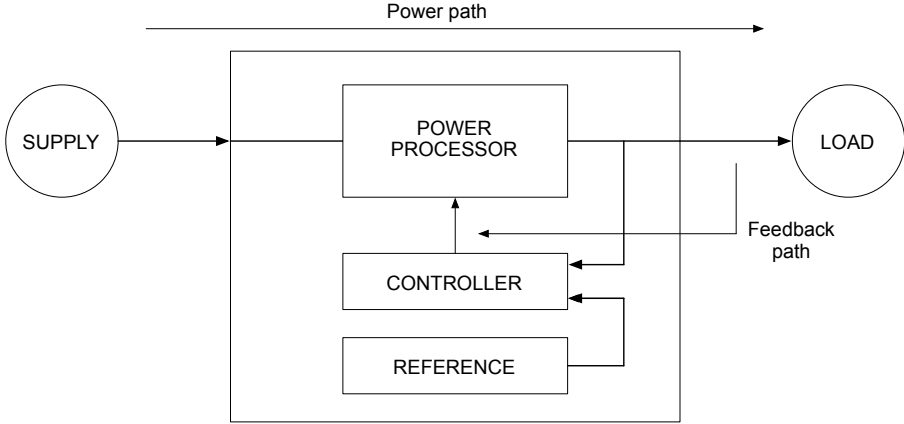


Figure 2.1: *Electronic Voltage Regulator block diagram*

In the Fig. 2.1 two different paths can be found: the power path and the feedback path.

The power path is the main path and permits the power flow from the input port to the output port. The power, flowing from the input to the output, has to pass through the power processor, which regulates that flow.

The feedback path has the task to adjust the power flow, controlling the power processor.

Hereafter three important parameters will be defined. They are useful to evaluate and compare the performances of the different regulators.

The first is the efficiency, defined in equation (2.1), and explain the ability to transfer power from the input to the output.

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out}I_{out}}{V_{in}I_{in}} \quad (2.1)$$

The second and third parameters are the line and load regulation, defined in the equations (2.2) and (2.3) respectively. Those parameters explain the ability of the regulator to handle the variation of the input voltage (line regulation) and the load (load regulation).

$$LineReg = \frac{\delta V_{out}}{\delta V_{in}} \quad (2.2)$$

$$LineReg = \frac{\delta V_{out}}{\delta I_{out}} \quad (2.3)$$

The voltage regulators can be divided into two main groups, depending on the operating region of the power processor:

Linear Where the power processor acts as a variable linear device (a variable resistor), permitting a constant power flow.

Switching Where the power processor acts as a switch, permitting the power flowing only for a fixed time.

2.1.1 Linear voltage regulators

The linear voltage regulators[20] are the simplest regulators that can be found to supply electronic devices. The Fig. 2.2 shows its block diagram, highlighting the power path and the feedback path.

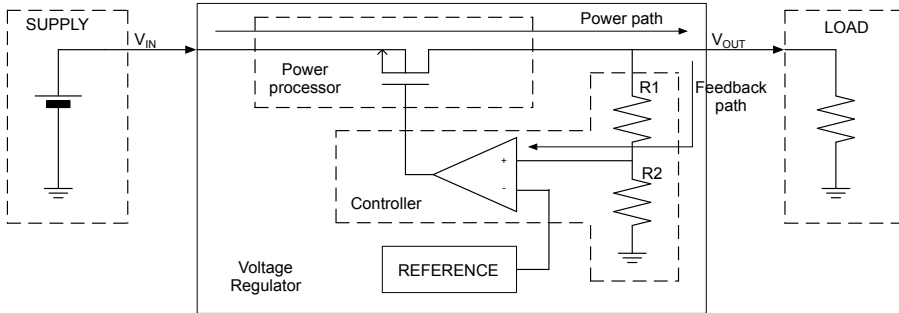


Figure 2.2: *Linear Voltage Regulator block diagram*

In that kind of regulators, the power device (BJT or MOSFET) acts as a variable resistor, adjusting its resistance according with the voltage that comes up from the controller block. The controller generates the inputs of the operational MOS minimizing the error between the two inputs of the operational

amplifier. So the output voltage can be calculated easily from the equation (2.4), where V_{out} is the output DC voltage and V_{ref} is the reference voltage.

$$V_{out} = V_{ref} \frac{R_1 + R_2}{R_2} \quad (2.4)$$

The linear voltage regulators are widely used in all the electronic systems, because they can generate a very stable and noiseless output voltage, rather than switching voltage regulators.

On the other hand, since the power device acts as a resistor, they are very inefficient, limiting their application only when low output power is needed. Indeed, as the I_{in} is equal to I_{out} , the efficiency of linear regulators can be explained as the equation (2.5).

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out}I_{out}}{V_{in}I_{out}} = \frac{V_{out}}{V_{in}} \quad (2.5)$$

2.1.2 Switching voltage regulators

The switching voltage regulators are a bit more complicated than linear one and typically require more electronic components. Their working principle is based on storing an amount of energy in an inductor during the first switching phase and releasing it to the load during the second phase.

Those regulators can be divided into three main groups, depending on the relationship between the input and output voltage: the **buck converter** in which the output voltage is always below the input voltage, the **boost converter** in which the output voltage is always above or equal to the input voltage and the **buck-boost converter** in which the output voltage can be lower or higher than the input voltage.

Fig. 2.3 shows the circuit topology of the buck converter. In this case the efficiency, ideally equal to 100%, is very high and depends mainly on the R_{ON} of the PMOS and on the forward voltage of the diode. Using standard commercial buck regulators, a typical efficiency of about 80–90%

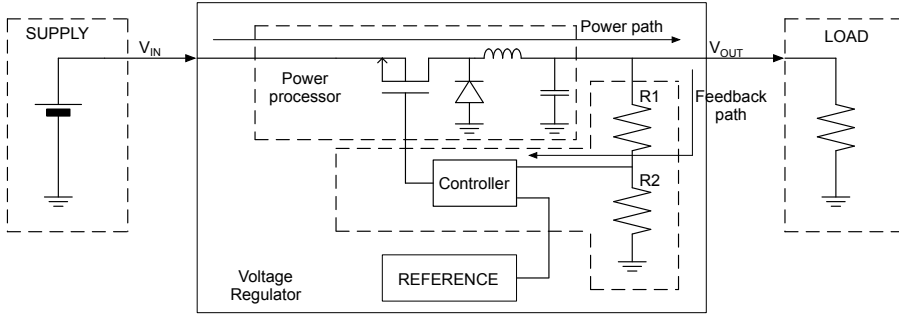


Figure 2.3: *Switching Voltage Regulator block diagram*

can be easily achieved.

Switching regulators are widely used in all those applications where a very high efficiency is needed, due to their very high efficiency, and where is needed a voltage higher than the supply.

2.1.3 Control techniques

The linear regulators, having a linear behavior, are easy to control. In fact it is possible to apply the standard linear control techniques, like linearization around the operating point and Bode diagram, and the controller can be the well known proportional (P) or proportional-integrative (PI) controller.

The switching regulators, instead, have a very non linear behavior, so the linear control techniques cannot be applied. Indeed, new control techniques must be adopted[21]. In literature, it is possible to find two main control techniques developed for switching regulators: voltage feedback control and current feedback control. Those control techniques can be adopted with a fixed switching frequency, called *Pulse Width Modulation* (PWM) or with a variable frequency, in this case is called *Pulse Frequency Modulation* (PFM).

The voltage feedback control, which is shown in Fig. 2.4, uses only the output voltage as feedback signal. It amplifies the error between the output voltage

and the reference (done by the *Error Amplifier*) and the compares it with a sawtooth waveform, to generate the PWM or PFM signal that controls the switch.

This kind of control permits to achieve better performance in term of load regulation, output ripple and better EMI filtering. Furthermore this control technique simplifies the stabilization of the control loop, because no compensation networks are needed to guarantee the stability of the loop.

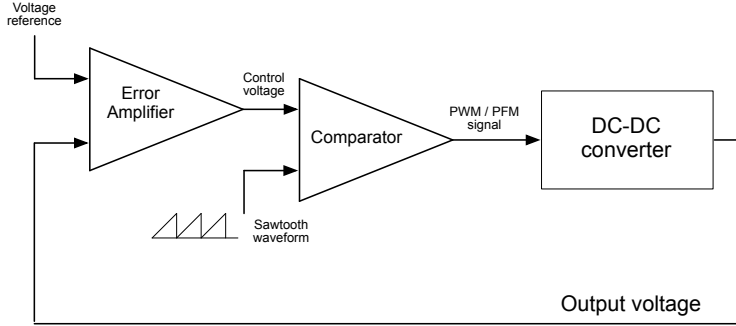


Figure 2.4: *Voltage control scheme*

The current feedback control, shown in Fig. 2.5, uses both the information on the voltage and on the current to regulate the output voltage[22, 23]. Like the voltage controller, it amplifies the difference between the output voltage and the reference voltage, even done by the *Error Amplifier*, but then compares it with the information on the current that is flowing through the inductor to generate the switch control signal.

This kind of control, applied with a variable frequency signal, permits to achieve a better efficiency with low output current and to generate a *feed-forward* path that speeds up the regulator in the response to supply and load variations. Furthermore, controlling and limiting the current in the switch permits to size it and the inductor better, because that current doesn't depend on the external components like in the voltage feedback control. In addition, the control of the current permits to connect more devices in parallel without any issue. In fact, when multiple regulators are connected together, having a current control permits to balance equally the current in the various regulators.

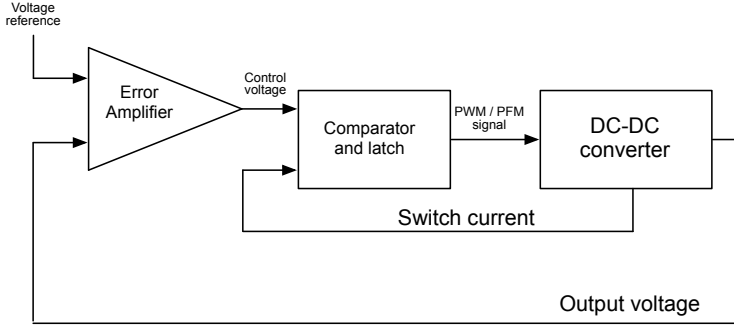


Figure 2.5: *Current control scheme*

2.2 Designing a switching voltage regulator

The target application for the switching regulator is to use it as high efficiency voltage regulator to supply other low voltage devices directly from the car battery, with an output current in the range of 100 – 500mA.

The DC-DC buck regulator[24] has been designed considering all the stringent requirements for automotive grade devices. More in detail, the operative input voltage can vary from 5V to 50V, while the absolute input voltage is 55V; the operative ambient temperature range is $-40 - 125^{\circ}\text{C}$, while the junction temperature range is $-40 - 150^{\circ}\text{C}$.

Furthermore the regulator must be able to supply an output current up to 700mA and has a very low current consumption in standby mode and maximizes the efficiency, specially with very low output current.

Moreover, the regulator has two digital logic input pins that can be driven from any logical family supplied from 3.3V up to 50V, called SHDNN and ILIMIT in Fig. 2.6. When the SHDNN signal is low, the system goes into standby mode, characterized by a very low current consumption, otherwise it operates normally. When the ILIMIT signal is low, the maximum output current is limited to only 350mA, reducing the output ripple, otherwise the maximum output current is 700mA.

Table 2.1 summarizes the main characteristics of the regulator.

Table 2.1: Regulator requirements

Parameter	Min	Max	Unit
Operative Input Voltage	5	50	V
Operative Output Voltage	1.25	V_{in}	V
Peak Input current		2	A
Output Current		0.7	A
Operating temperature range	-40	125	°C
Junction temperature		150	°C

2.2.1 Block diagram

The DC-DC regulator has been designed in High Voltage 0.35 μ m technology from AustriaMicroSystems.

It integrates on the same die the controller, the reference generator and the power switch, in this case a PMOS, and needs only few external components to operate correctly: the diode, the inductor and the filtering capacitors on the input and output. The controller has been chosen considering the target application of the regulator and the choice fell on a current control with a PFM technique. In fact, with this kind of controller, it's possible to minimize the current consumption because no oscillator is needed, at the cost of worst performances in terms of output ripple voltage.

Fig. 2.6 shows a simplified block diagram of the regulator. The system can be divided into 4 main blocks:

Power Management Unit The PMU includes a linear regulator, to generate the internal supply voltage for the other blocks, and a band-gap, to generate the reference voltage. Furthermore it includes a temperature protection circuit to avoid silicon damages if the die temperature rises too much.

Controller The controller is implemented using a SR-latch: setting it when the voltage goes below the threshold and resetting it when the maximum current is reached[25].

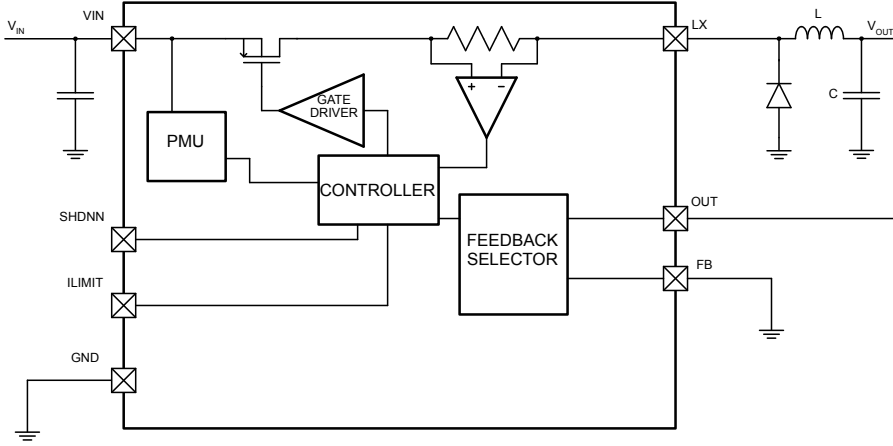


Figure 2.6: *Regulator block diagram*

Feedback In the feedback path checks the presence of an external divider and, if connected, uses it to regulate the output voltage. If it is disconnected, it uses the internal divider, regulating the output voltage to about 5V.

Power Stage The Power Stage includes the PMOS, with very low R_{ON} (about 200m Ω), and the gate-driver, which has to charge and discharge the gate of the PMOS in few nanoseconds, to guarantee the right functionalities of the regulator and to reduce the power consumption during the transitions.

A more detailed description of the here described DC-DC converter can be found in [24]

2.2.2 Layout

Fig. 2.7 shows the layout of the entire chip, resulting in a 6.5mm^2 die. The right side is completely filled by the Power-PMOS while the left side contains all other blocks. To avoid substrate injection and disturbances to sensitive blocks, like the bandgap reference generator, a large *n-well* as isolation has been placed between the PMOS and the other blocks.

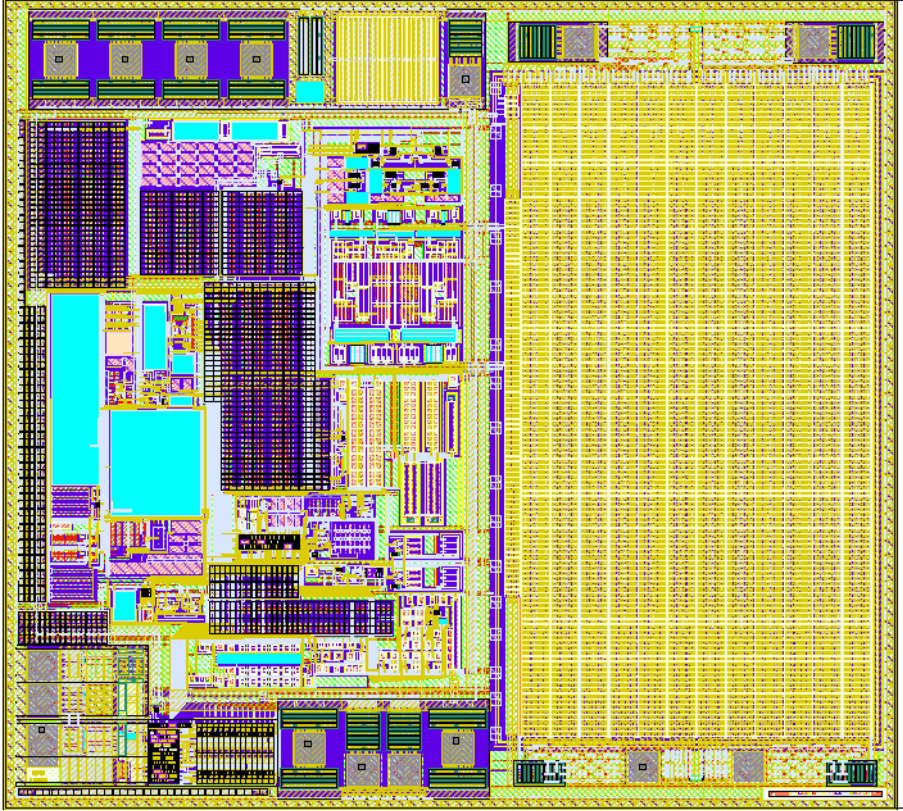


Figure 2.7: *Regulator layout*

The layout placement has been done also considering the possibility to integrate it as module in a more complex IC. In this way, all the parts that can be shared when the system is used as a module, like the PMU, are placed on the periphery and the layout effort to integrate it is very low.

2.3 Validation: simulations and measurements

The entire system was first simulated and then measured to complete validate its design, checking the right functionality and evaluate the achieved performances.

As first parameter, the standby current has been checked.

The simulations reported that the current consumption in shutdown is only $1\mu\text{A}$ in typical conditions and only $1.8\mu\text{A}$ at worst case, while in no load condition is only $15\mu\text{A}$ typical and $25\mu\text{A}$ maximum.

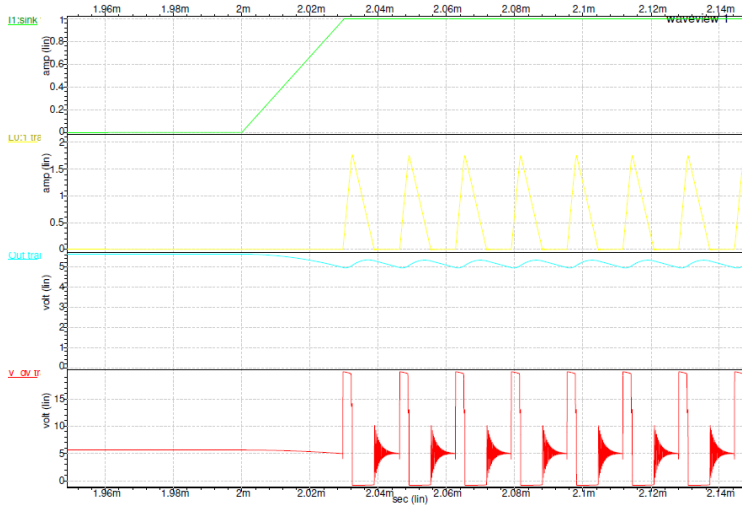


Figure 2.8: *Normal mode waveform*

Fig. 2.8 shows regulator waveforms in normal operation when the output current changes from 0 to 1A. The first row is the output current, the second is the current flowing in the inductor, the third is the output voltage (V_{OUT} in Fig. 2.6) and the forth is the LX voltage (see Fig. 2.6).

As far as simulated performance is concerned, Fig. 2.9 and 2.10 show the simulations of the variation of the output voltage versus the input voltage (in the range 5 – 50V with different inductors ($10\mu\text{H}$ and $39\mu\text{H}$) and for different

output currents (100mA and 500mA).

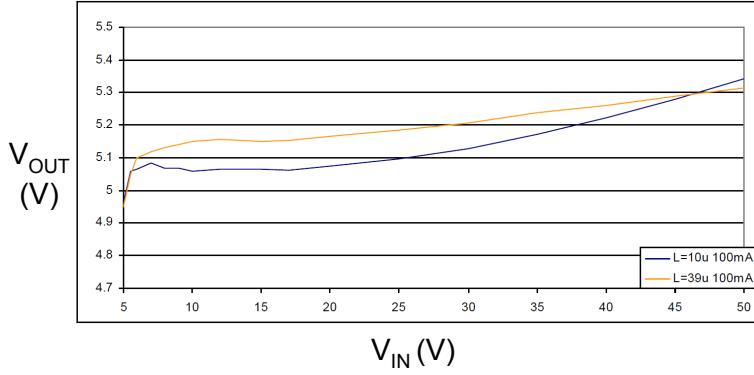


Figure 2.9: V_{OUT} vs V_{IN} with 100mA output current

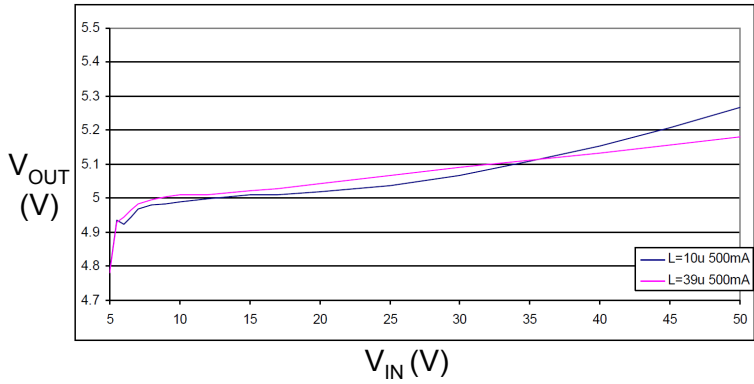


Figure 2.10: V_{OUT} vs V_{IN} with 500mA output current

Fig. 2.11 and 2.12 show the simulations of the load regulation of the regulator. More in detail, in Fig. 2.11 the supply voltage is 5V and the regulator goes in dropout mode, keeping the PMOS always on, while in Fig. 2.12 the supply voltage is 12V, like in typical condition.

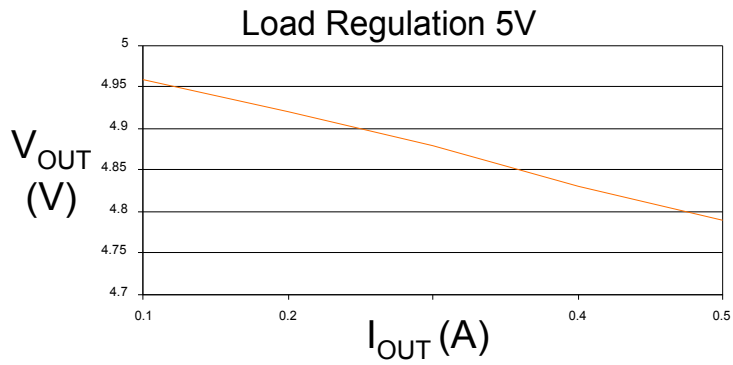


Figure 2.11: Load Regulation with 5V supply voltage

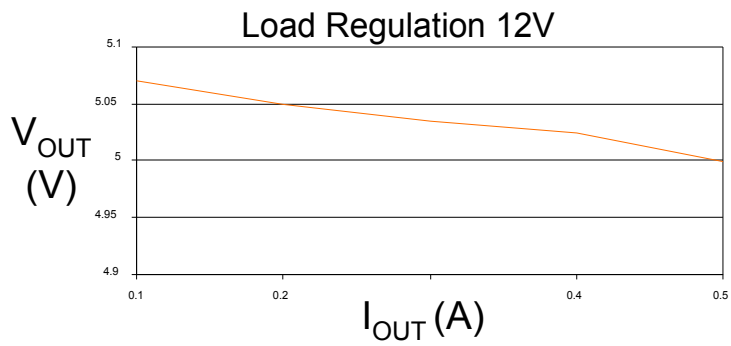


Figure 2.12: Load Regulation with 12V supply voltage

3 Drivers for inductive loads

Especially in the automotive environment, the use of electromagnetic actuators, like injectors, relays and solenoid electro-valve, is constantly increasing, driven by the continuous replacement of mechanical parts with electronics actuators.

This exchange on one hand permits to control electronically the engine and the other mechanical parts of the car, reducing the fuel consumption and the CO2 emissions, but on the other hand requires electronic driver for such kind of loads, having an inductive behavior. Indeed, compared with classical drivers for resistive and capacitive loads, the design of drivers for inductive loads, requires overcoming more issues because the management of the current, and then the energy stored in the inductor, must be well considered[26, 27, 28, 29]. In fact, when inductive loads are driven, it's very important controlling the freewheeling phase. As shown in [30], there are 4 main freewheeling strategies proposed in literature that can be used, explained in Fig. 3.1. Table 3.1 shows both the advantages and disadvantages of all those different freewheeling strategies.

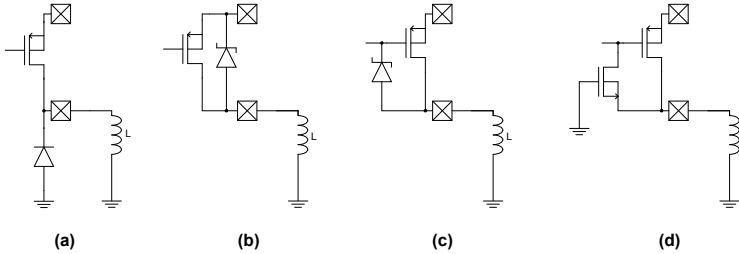


Figure 3.1: *Principles of typical solutions to handle inductive freewheeling*

Actually those drivers should be part of distributed systems interconnected by digital controllers with different busses.

This kind of approach leads the IC manufactures to integrate on the same die the power devices with the interface to the digital control host through standard local communication protocols, like Serial Peripheral Interface (SPI) or Inter-Integrated Circuit (I2C), and/or through vehicle networks, like FlexRay, CAN or LIN busses.

At the same time, to guarantee the latest functional safety standards that can be found in automotive grade devices, like ISO26262, it's necessary to integrate on the same die also diagnostic circuits that monitor constantly the status of the driver and signal to the digital part when a fail condition occurs.

Table 3.1: Advantages/Disadvantages of typical solutions in Fig. 3.1

Fig. 3.1	Advantages	Disadvantages
(a)	Very simple, No zener diode	Long turn-off time Requires high power diode
(b)	Short turn-off time	Requires an integrated high power zener diode
(c)	Short turn-off time	Requires an integrated zener diode
(d)	Very simple, No zener diode	Long turn-off time

The first freewheeling strategy, shown in Fig. 3.1(a), is normally used when a constant current flow is needed, like in a buck DC-DC converter and in a Lundell alternator as excitation driver[31]. Indeed, this configuration has a very long turn-off time and, acting the MOSFET with a PWM like signal, permits to maintain a constant current flow in the inductor.

The second and third freewheeling strategies, shown in Fig. 3.1(b) and (c), are normally used when the current must be zero at the end of the operation, like acting a relay or a solenoid valve. In fact, in this case, is very important to discharge the energy stored in the inductor as short as possible, to minimize the turn-off time, ensuring a good system behavior.

The last freewheeling strategy, shown in 3.1(d), has the same behavior of 3.1(a), but can be used only with low currents, because of the higher power dissipation in the freewheeling phase.

In the following sections, two examples of the design of inductive loads driver

will be exploited.

Section 3.1 shows the development of an inductive load driver, highlighting the design and validation phases, especially suited to drive relays and solenoid valves with integrated capability of self-monitoring and fault diagnostic. It has been designed to overcome the limitations of the circuits on Fig. 3.1 (c) and (d), combining the main advantages of the two structures and avoiding the integration of power diodes or power zeners as in the solution (a) and (d) in Table 3.1 and Fig. 3.1. The designed smart driver can be easily integrated as hard macro-cell in more complex automotive grade ICs and can be directly interfaced to a host digital ECU since it integrates both the High-Voltage (HV) MOS power circuitry and the low-voltage circuitry for control and digital interfacing.

Section 3.2 presents the design and validation phases of a single-chip integrated Rotor Coil Driver that can be used in automotive alternators. It integrates the power switch with the control circuitry and the diagnostics. It follows the freewheeling strategy shown in 3.1(a), with new functionalities, like full reverse polarity protection and programmable output slope control against in-rush currents and current spike transients. This rotor coil driver has been implemented in a 0.35 μ m HV-CMOS technology and has been embedded in a mechatronic brush-holder regulator system-on-chip for an automotive alternator.

3.1 Solenoid Valve Driver

The inductive load driver, implemented in 0.35 μ m HV-CMOS IC technology from Austriamicrosystems, fulfills all the requirements that can be found in automotive grade devices. The smart driver has been designed to be integrated as hard IP in automotive UCs and it communicates with the digital part into the IC, receiving the command signal and sending back the status flags.

3.1.1 Design

The scheme of the driver, shown in Fig. 3.2, can be divided into 4 different blocks: the power MOS driver, the gate-driver, the zener-like circuit, detailed in Fig. 3.3, and the diagnostic circuit, detailed in Fig. 3.4.

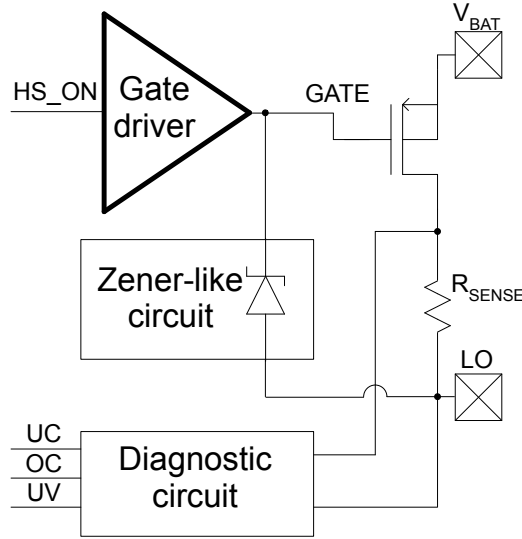


Figure 3.2: Inductive driver block diagram

The driver is an integrated high-power high-side PMOS with low ON resistance. The gate-driver block drives the gate of the PMOS power switch to turn it ON and OFF depending on the status of the HS_ON digital signal in Fig. 3.2. The zener-like circuit is the active circuit that turns ON the PMOS during the freewheeling phase. The scheme diagram of this block is shown in Fig. 3.3.

With respect to state of art solutions in Fig. 3.1 and Table 3.1, this different approach (configuration of Fig. 3.2 with a zener-like circuit as in Fig. 3.3) avoids the use of power diodes, occupying a large part of the chip area, as is in Fig. 3.1(a) or (b) and avoids the use of integrated zener diodes as in Fig. 3.1(b) or (c).

Integrated zener diodes are absent in the considered 0.35 μ m HV-CMOS tech-

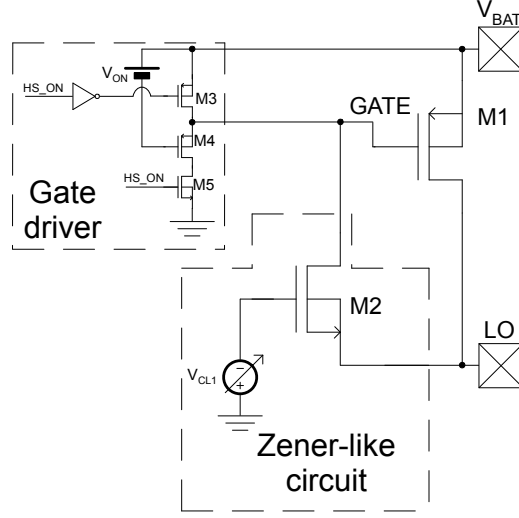


Figure 3.3: Gate-driver and Zener-like circuits

nology and in other typical HV-CMOS technologies.

Some BCD technology exists, offering the integration of zener diodes, but as process option at an increased technology and integration cost vs. basic HV-MOS technologies.

The gate-driver is the block that drives the gate of the PMOS power switch to turn it ON and OFF depending on the status of the HS_ON digital signal in Figs. 3.2 and 3.3[32]. The PMOS $M4$ and the V_{ON} bandgap stabilized voltage reference, generated according Equation (3.1) while $V_{GS MAX(M1)}$ is the maximum V_{GS} for $M1$ and $VT_{p(M4)}$ is the threshold voltage of the PMOS $M4$, limit the V_{GS} of the PMOS $M1$ below the maximum allowed for that device.

$$V_{ON} = |V_{GS MAX(M1)}| + |VT_{p(M4)}| \quad (3.1)$$

The main part of the zener-like circuit is the NMOS $M2$ that is turned ON when the voltage on the output is below ground. In this condition the PMOS $M1$ works in saturation region and the V_{GS} must follow the Equation (3.2) where I_L is the output load current while VT_p and β_p are the parameters of

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the PMOS transistor.

$$|V_{GSON}| = |VT_p| + \sqrt{\frac{2I_L}{\beta_p}} \quad (3.2)$$

$$V_{CL} = |V_{CL1}| + VT_{n(M2)} \quad (3.3)$$

Absolute values are used for V_{GSON} and VT_p in Equations (3.2) and (3.3) since for a PMOS these values are negative. Similarly V_{CL} is negative; Equation (3.3) gives the absolute value of V_{CL} below ground.

The diagnostic circuit, shown in Fig. 3.4, is composed by an under-voltage (UV) comparator on the output, by a current limitation circuit and by an overcurrent (OC) and undercurrent (UC) comparators.

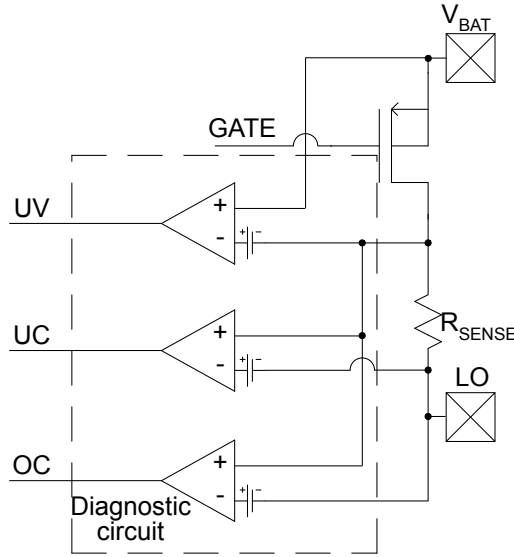


Figure 3.4: *Diagnostic circuit*

The under-voltage comparator senses the difference between the battery pin and the output pin. If this difference is higher than a fixed threshold (about 2V), it sets the UV flag.

The current limitation circuit, on the other hand, senses the current flowing in the power PMOS using a very small sensing resistor(R_{SENSE}) and uses this information to limit the current flowing in the driver. Moreover it uses the information coming from the sensing resistor to compare the PMOS current with two fixed thresholds and then to generate an undercurrent (UC) and an overcurrent (OC) flags.

All those thresholds (under-voltage, undercurrent and overcurrent) are generated by a bandgap stabilized voltage reference circuit placed far away from the power devices, to limit the thermal interferences between the two circuits.

The UC flag permits to detect a disconnection of the load while the OC flag permits to detect a short circuit condition on the load. The OC flag, after a confirmation time of 1ms, forces the turn-off of the driver to avoid damage to the driver itself. This solution can be not sufficient if a short circuit condition with a very low ohmic path is present. In this case the current flowing in the driver is limited only by the sensing resistor and the inductor series resistor and it can reach several amperes, damaging metal routing of the driver. To avoid this condition, the circuit uses the information on the current, sensed through R_{SENSE} in Fig. 3.4, as feedback to limit the maximum current flowing in the driver. To be noted that the current limitation circuit and the OC flag circuit share the same current sensing device and the same threshold generation unit. This solution ensures that the OC flag is always set when the current is limited, also in worst-case condition.

As said before, the driver, although is designed to drive inductive loads, implements also a linear current limitation circuit, permitting to drive also resistive and capacitive loads. In fact, the main issue, when a capacitive load is driven, is the very high in-rush current that charges the load capacitor. This very high current can destroy the driver if a current limitation circuit is not present.

Implementing in the same smart driver both the zener-like integrated circuit and the current limitation circuit permits to connect inductive, resistive and capacitive loads using the same driver.

Moreover to protect the circuit, an integrated temperature sensor and an over-temperature protection have been implemented. When the die temperature reaches the over-temperature threshold, the driver is automatically turned-off and kept in this state until the die temperature fall below the recovery threshold.

3.1.2 Layout

To check the design of the inductive load, a *testchip* has been realized, integrating on the same die eight drivers with different maximum operating current together with a power management block and with CAN and LIN transceivers for interfacing versus an off-chip network or control host.

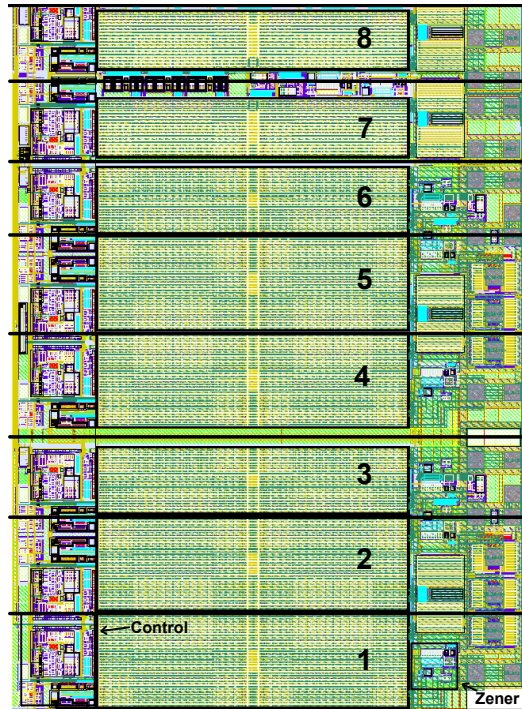


Figure 3.5: *Layout of 8 different inductive drivers*

In Fig. 3.5 the layout of the drivers is shown. The drivers 1, 2, 4 and 5

are of Type1, with 600mA as maximum DC current, the drivers 3 and 6 are of Type2, with 400mA as maximum DC current and the drivers 7 and 8 are of Type3, with only 200mA as maximum DC current.

The drivers 1, 2, 4 and 5, sustaining higher currents are those occupying a larger area rather than drivers of Types 2 and 3.

Besides, Fig. 3.5 highlights the layout of control logic and of the zener-like circuits for the first driver.

Table 3.2 summarizes the operating temperature, voltage and current ranges of the driver. Moreover, Table 3.2 shows the typical ON resistance of the three different drivers, the value of the diagnostic thresholds and the maximum driving current in DC conditions and AC pulsed ones.

Table 3.2: Operating and environmental ratings

Operating temperature	-40 – 150	°C
Operating battery voltage (V_{BAT})	5 – 40	V
DC current Type1	Up to 0.6	A
Pulsed current Type1	Up to 1.1	A
DC current Type2	Up to 0.4	A
Pulsed current Type2	Up to 0.75	A
DC current Type3	Up to 0.2	A
Pulsed current Type3	Up to 0.58	A
PMOS ON resistance (Type1)	330	mΩ
PMOS ON resistance (Type2)	470	mΩ
PMOS ON resistance (Type3)	625	mΩ
UV flag detector	2	V
UC flag detector	20	mA
OC flag detector (Type1)	830	mA
OC flag detector (Type2)	580	mA
OC flag detector (Type3)	435	mA
Zener activation voltage (referred to ground)	-15	V

3.1.3 Quality and safety aspects

As said in the introduction (Chapter 1), to achieve the stringent requirements of the ISO26262 standard, many diagnostic features must be integrated

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on the same die, in order to detect a failure condition and, when it is possible, to take countermeasures to isolate the fault, avoiding hazard conditions. In fact, ISO26262 requires to monitor continuously the devices, signaling to the driver when something is not working correctly.

In this case, the diagnostic block is in charge to detect the status of the driver and the digital part, using the control and status flags (HS_ON, UV, UC and OC), can detect failure conditions, like the disconnection of the load or the short to ground of the driver. Moreover, the digital part can also detect a variation of the parameters of the driver, like the ON resistance, and can implement all necessary measures to avoid hazard conditions.

3.1.4 Validation

To validate the design of the inductive load driver, the driver has been first simulated and then measured. Hereafter the simulation and measure results will be discussed.

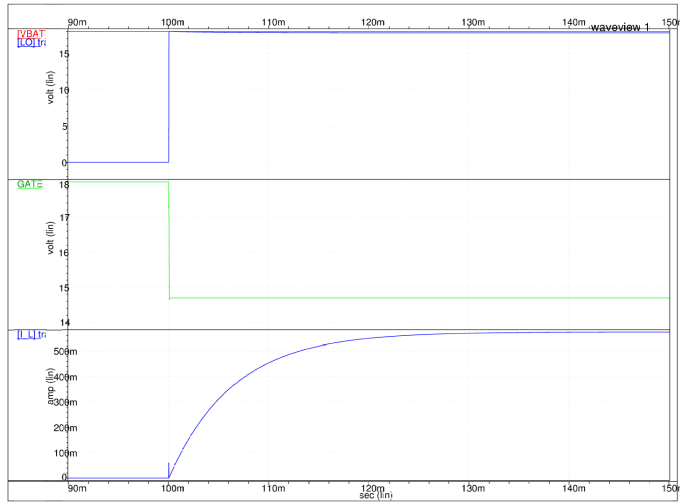
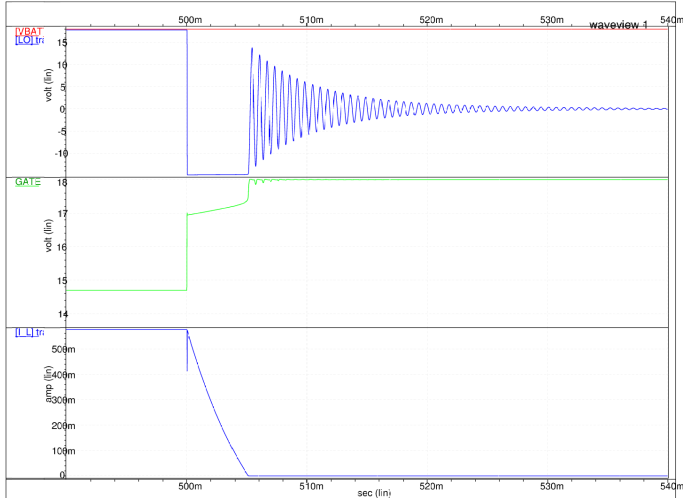


Figure 3.6: *Simulated turn-on transient*

Figs. 3.6 and 3.7 show respectively the simulated turn-on and turn-off tran-

Figure 3.7: *Simulated turn-off transient*

sients of the driver in the example case of three inductive loads of 600mH each, connected in parallel between the pin LO and ground.

The waveform at the top of each figure highlights the battery (red line) and the LO (blue line) voltage signals.

The waveform in the middle shows the voltage on the gate of the driver PMOS. The waveform at the bottom shows the current I_L flowing in the inductor.

Figs. 3.8, 3.9 and 3.10 shows respectively the results of the Montecarlo simulation of the under-voltage (UV), undercurrent (UC) and overcurrent (OC) flags. Those Montecarlo simulations are done considering both process and mismatch variations.

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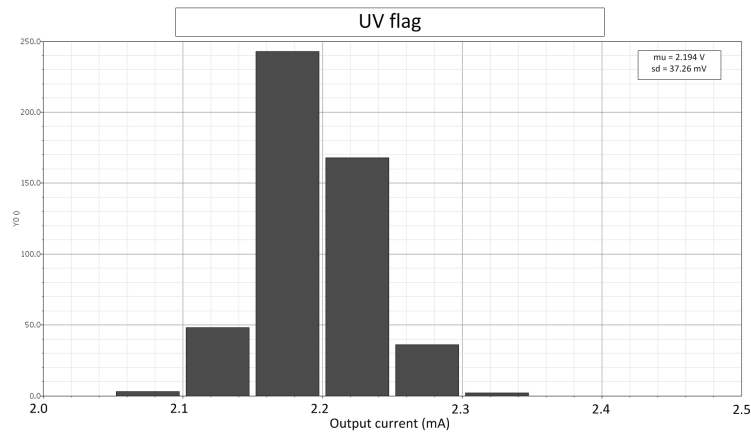


Figure 3.8: *UV flag Montecarlo simulation*

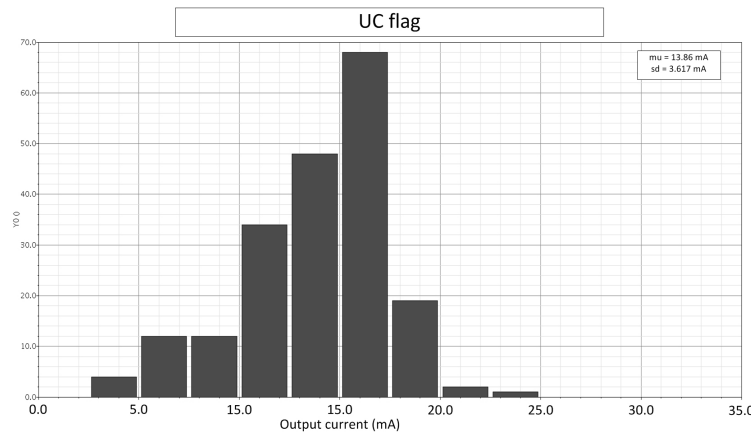


Figure 3.9: *UC flag Montecarlo simulation*

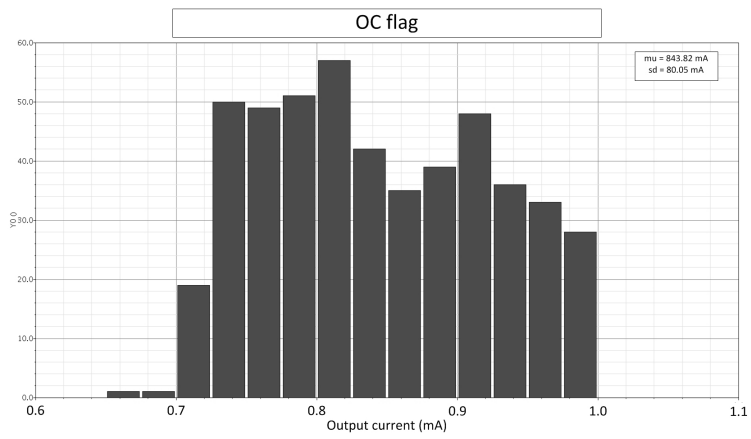


Figure 3.10: *OC flag Monte Carlo simulation*

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Figs. 3.11 and 3.12 shows respectively the oscilloscope waveforms of the turn-on and turn-off transients with the same load condition of Figs. 3.6 and 3.7.

In this case the yellow waveform is the battery voltage, the red is the LO voltage and the green is the current flowing in the load.

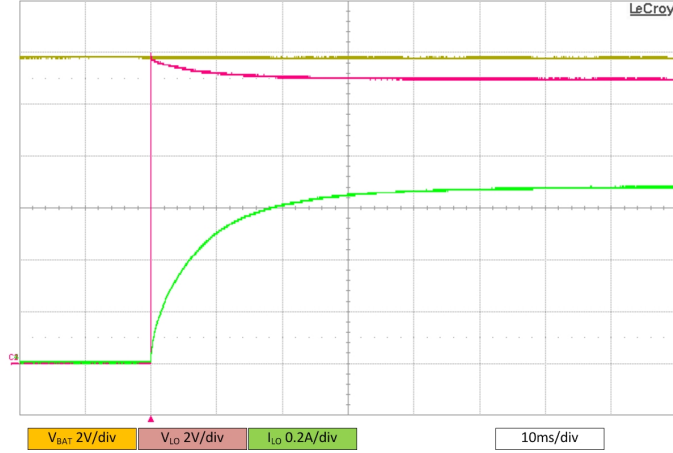


Figure 3.11: *Measured turn-on transient*

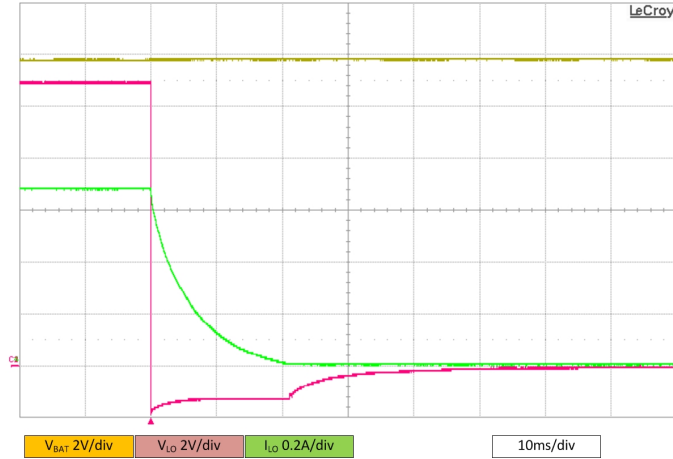


Figure 3.12: *Measured turn-off transient*

In the Fig. 3.12, it is possible to note that the negative clamping voltage is only 1.5V below ground, instead 15V as designed. This behavior has been analyzed and the root cause was found in a parasitic BJT not included in the models supplied by the foundry. In fact, a parasitic npn bipolar transistor (shown in Fig. 3.13), generated by two HV-MOS devices in the V_{CL1} generator in the Fig. 3.2, reduces the clamping voltages to the measured value.

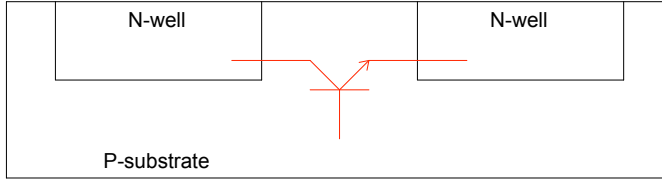


Figure 3.13: *npn BJT parasitic device*

To solve this issue, a new silicon fab run is necessary to increase the distance between the n-wells and increase the immunity of the V_{CL1} clamp generator to this kind of parasitic devices.

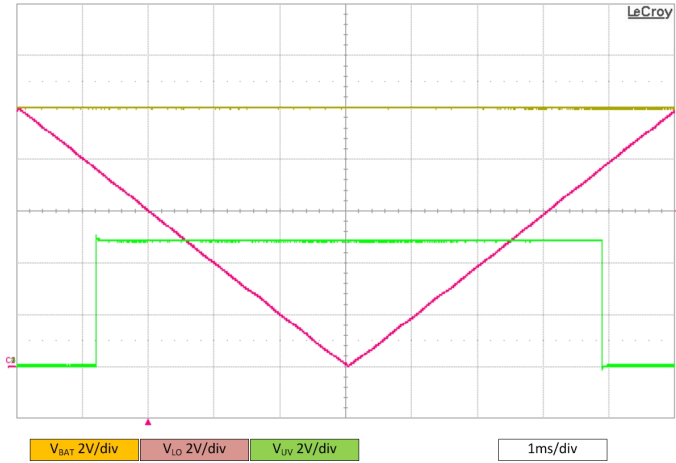


Figure 3.14: *Measured UV flag*

Figure 3.14 shows the UV flag waveform. In this case, the battery voltage (the yellow line) is kept to 10V, while the LO pin (the red line) is swept from

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10V to ground and vice-versa.

To avoid a very high current flow through the driver, it has been kept off during the measurement.

The green line is the resulting diagnostic flag: it is set when the difference is higher than 2.2V, and is cleared when it becomes lower.

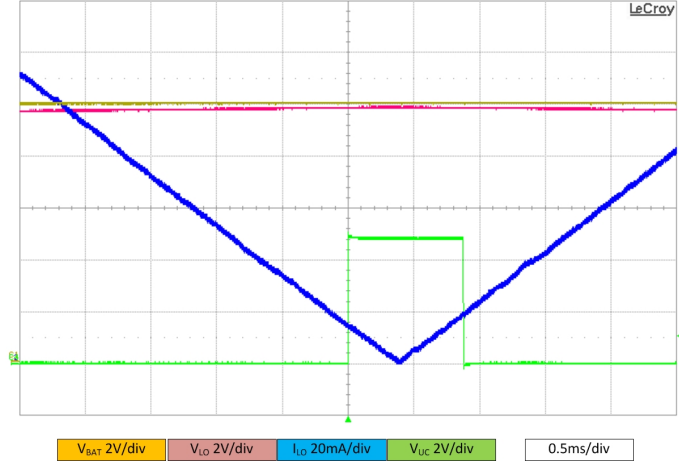


Figure 3.15: *Measured UC flag*

Figure 3.15 shows the UC flag waveform. In this case, the battery voltage (the yellow line) is kept to 10V, while from the LO pin (the red line) is sunk a variable current (the blue line) from 120mA to 0mA and vice-versa.

In this case, to ensure the right behavior, the driver is kept on during the test. The green line is the resulting diagnostic flag: it is set when the current is below 20mA, and is cleared when it becomes higher.

3.2 Rotor Coil Driver

The Rotor Coil Driver (RCD), implemented in Austriamicrosystems HV-CMOS 0.35 μ m ASIC technology, has been designed to completely fulfill the requirements that can be found in automotive grade devices. Particularly the RCD can operate with battery voltage between 6V and 50V, covering both cold cranking and load dump events. Furthermore it can sustain permanent reverse polarity on battery down to -3.2V, which is the maximum forward voltage across the series of two diodes in the stator rectifier bridge, and unexpected battery voltage surges up to 55V.

The RCD has been designed to operate correctly up to the max absolute junction temperature of 180°C before reaching an “over-temperature protection threshold”, indeed above 180°C the integrated temperature protection circuit switches off the driver to avoid silicon damage.

This RCD, respect to other solutions [33, 34], implements a current slope control on the high-side, avoiding voltage spikes due to parasitic inductance of the alternator-battery cable.

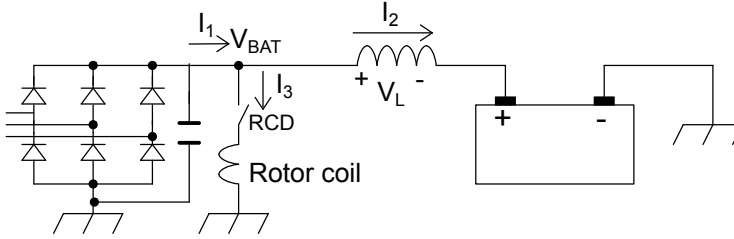


Figure 3.16: Connection of alternator output, battery and rotor coil with its driver

In fact, in Fig. 3.16 the current that flows from the rectifier bridge (I_1) is almost constant and depends on the magnetic field on the stator coils and hence on the rotor coil current. During the turn-on phase, if the current I_3 increases very rapidly, according to Eq. (3.4) the current I_2 will decrease rapidly as consequence. According to Eq. 3.5, due to the parasitic inductance of the wire L_W , there will be a fast negative voltage spike on V_{BAT} . During the turn-off

phase a dual condition happens: if the current I_3 decreases rapidly, I_2 will increase rapidly as consequence and a fast positive voltage spike on VBAT can be observed. Those spikes are not acceptable because they can generate EMI problems to other electronic devices.

$$\Delta I_1 = \Delta I_2 + \Delta I_3 \text{ since } \Delta I_1 \simeq 0 \rightarrow \Delta I_2 \simeq \Delta I_3 \quad (3.4)$$

$$V_L = L_W \frac{\partial I_2}{\partial t} = -L_W \frac{\partial I_3}{\partial t} \quad (3.5)$$

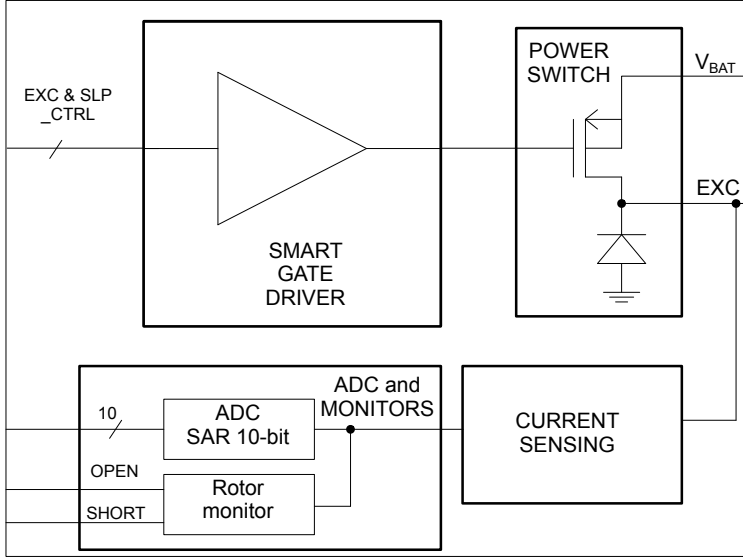
3.2.1 Design

The coil driver scheme, shown in Fig. 3.17, can be divided into 4 different blocks: the smart gate driver, the power switch, the current sensing and the ADC and monitors.

The interface towards the processing core of the voltage regulator system is composed by the following output signal: two flags, OPEN and SHORT, signaling if the current in the rotor coil is under or over programmable current thresholds and a 10-bit signal providing a measure of the rotor coil current. The digital core sends to the smart gate driver in Fig. 3.17 the order to increase or decrease the rotor coil current changing the duty cycle of the *EXC_CTRL* control signal.

The gate of the high side switch is driven by a PWM signal with a fixed frequency f_{PWM} in a range of some hundreds of Hz typically. Rotor current is modulated changing the duty cycle of the PWM signal from minimum, typically set to 5%, to 100%(maximum field).

Fast transients in the current sunk from the battery can generate undesired overshoots, oscillations and ringing on the battery voltage. To avoid them, for EMC compliance, the current through the high-side has a slope controlled transient during the switching on and off transitions. The digital core, through the *SLP_CTRL* signal, can select the desired current slope.

Figure 3.17: *Alternator coil driver schematic*

Power Switch

One of the most important blocks is the high-side power switch, which is a p-type HV lateral diffused (LD) MOS with 3.3V thin gate oxide, included in the HV-CMOS technology from Austriamicrosystems (H35). The main operating and absolute parameters of the HV-PMOS power switch are shown in Table 3.3, which also shows a comparison with the lateral diffused HV-NMOS of the same technology.

Both PMOS and NMOS HV devices fulfill the operating battery range, but the choice of PMOS is due to two main factors: reverse polarity protection and charge pump avoidance. Using the PMOS is possible, driving the bulk terminal properly, to avoid current flow in parasitic devices when the battery voltage is below zero, as shown in Fig. 3.18. Using the NMOS as in [33, 34] that behavior cannot be achieved using a standard HV-CMOS technology, but a more expensive technology must be used to avoid the diode between drain and substrate.

Another advantage using PMOS instead of NMOS is that a charge pump is

Table 3.3: HV-PMOS and HV-NMOS operating and absolute ratings

	HV-PMOS	HV-NMOS
Operating Junction Temperature	-40°C to 150°C	-40°C to 150°C
Absolute Junction Temperature	-40°C to 180°C	-40°C to 180°C
Maximum Drain-Source Voltage (operating / absolute)	-50V / -55V	50V / 55V
Maximum Drain-Source Breakdown Voltage	-70V	70V
Maximum Gate-Source Voltage (operating / absolute)	-3.6V / -5V	3.6V / 5V
ON Resistance	$1.3R_n$	R_n

not needed. Indeed, the gate capacitance of the switch is in the order of some nF and is almost the same when a PMOS or an NMOS is used, so the charge pump for gate driving requires big integrated capacitors. In fact, considering that in the alternator system additional pins for external bypass capacitors are not provided, integrated capacitors must be used. If a rise time of about 10 μ s is considered, they have to be in the range of 100pF, requiring a lot of silicon area. Considering also that in the chosen HV-CMOS technology the R_{DSon} of the HV-PMOS is not much higher than the NMOS one, as shown in Table 3.3, the use of NMOS with big capacitors for the charge pump could have an higher die size and silicon cost than the use of PMOS. Avoiding charge pump circuitry permits also to reduce the EMC conducted emissions and simplify the driving circuitry, because no advanced techniques, like spread spectrum, are necessary to reduce EMI in charge pump design. Basing on the previous considerations, in the considered HV-CMOS technology, the use of PMOS instead of NMOS permits to reduce the total area occupation and then the silicon cost, permits to achieve full reverse polarity protection and also permits to have better performances in terms of EMC radiated and conducted noise.

As far as EMC is concerned, in addition to current slope control and the avoidance of charge pump circuitry, EMC decoupling capacitors have been implemented on the supply of clocked blocks in the RCD (e.g. the SAR ADC).

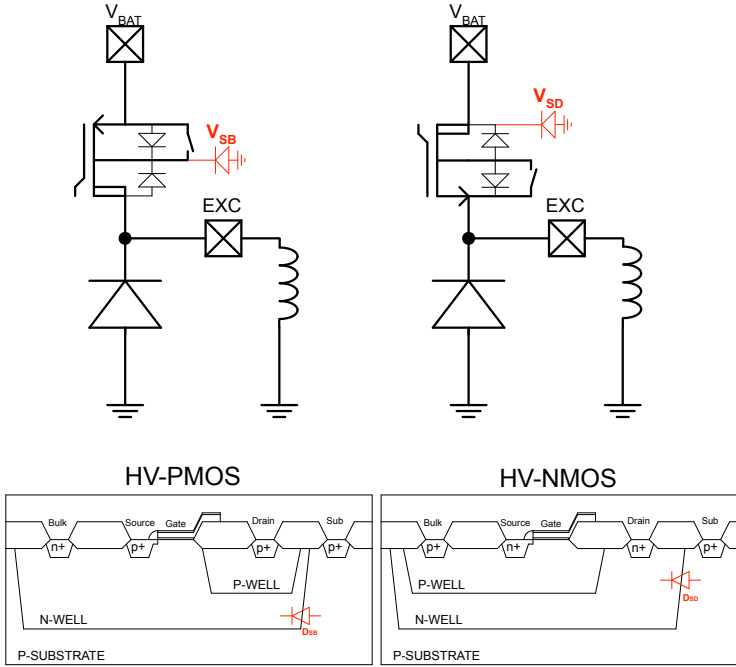


Figure 3.18: *PMOS vs. NMOS comparison during reverse battery condition*

To avoid crosstalk between different blocks due to shared supply lines, a layout design strategy with dedicated metal routing for supply and ground has been implemented.

Smart Gate-Driver

The smart gate driver is the block that drives the gate of the PMOS power switch in Figs. 3.17 and 3.19 to obtain the rotor coil current control. Fig. 3.19 highlights this block (the power MOS is the device M1) which operates in two different modes, one during the turn-on and turn-off transients (switch S1 in Fig. 3.19 in position 3), and one during the on and off steady states (switch S1 in Fig. 3.19 in positions 2 and 1, respectively). When the turn-on command is received through the *EXC_CTRL* control signal, the gate driver unit starts driving the gate of M1 in order to have a slope-controlled current flowing in the

PMOS. The switch S1 is closed in position 3, connecting together the gates of the two PMOS (M1 and M2). The digital controlled current ramp generator in Fig. 3.19 starts generating a current ramp on the OUT pin. Because M1 and M2 act as a current mirror, a current ramp on M2 forces a current ramp also in M1. The current that flows in M1 is obtained by scaling the current that flows in M2 by the dimensional factor ratio of the two PMOS devices, K_{M1M2} , which amounts to about 1600. The slope can be changed in two different ways: setting high the *SLP_CTRL* signal doubles the slope and adjusting the bias current in the gate driver permits a finest selection of the output current slope. In this coil driver both of those strategies are implemented: for the bias current both temperature coefficient and absolute value can be trimmed; trough the *SLP_CTRL* signal the slope can be set to the trimmed value or to the double.

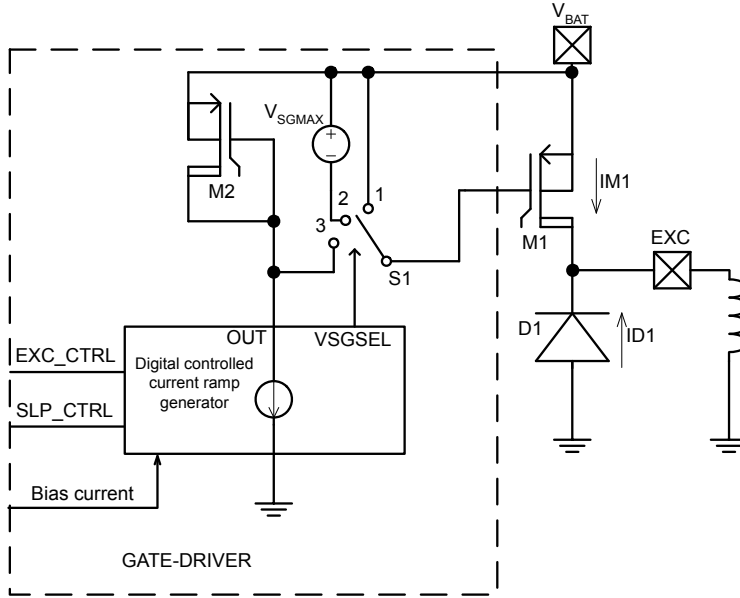


Figure 3.19: *Gate-Driver block diagram*

As consequence, as reported in Eq. (3.6), by controlling during turn-on and turn-off transients the shape and slope of the I_{out} signal, which is limited at a maximum at few mA, it is possible controlling the shape and slope of the rotor

coil current I_{M1} , which is in the order of several Amperes. Since I_{M1} in Fig. 3.19 is the rotor coil current, the control of the slope of that current realized by the proposed gate driver allows avoiding overvoltage phenomena and spike generation due to too fast current slope.

$$I_{M1} = K_{M1M2} * I_{M2} = K_{M1M2} * I_{OUT} \quad (3.6)$$

On the other hand the slope of the current I_{M1} cannot be too slow. This is because during the turn-on and turn-off transients, when the rotor current is flowing in D1 and M1, like shown in Fig. 3.20, the PMOS works in saturation region and large t_{ON}/t_{OFF} values would lead to high energy dissipation. During transients the output voltage and current of the PMOS M1 are both different from 0: the current I_{M1} can be modeled as a ramp going from 0 to I_{MAX} (when turning-on, the opposite when turning-off), while the M1 output voltage is almost constant, clamped at $V_{SD} = V_{BAT} - V_{EXC} = V_{BAT} + V_{DIODE}$ since D1 is on. As consequence the energy dissipated at each switching transient can be modeled as in Eq. (3.7). The average power dissipation P_{DAVG} , with a PWM switching frequency f_{PWM} , can be modeled as in Eq. (3.8).

$$E_{DON} = t_{ON} * \frac{(V_{SD} * I_{MAX})}{2}, \quad E_{DOFF} = t_{OFF} * \frac{(V_{SD} * I_{MAX})}{2} \quad (3.7)$$

$$P_{DAVG} = f_{PWM} * (E_{DON} + E_{DOFF}) \quad (3.8)$$

For typical values of $V_{BAT} = 14V$, $V_{DIODE} = 1V$, $I_{MAX} = 5A$, $f_{PWM} = 250Hz$, and a current slope controlled at $200mA/\mu s$ (slow control set of the RCD), t_{ON} and t_{OFF} amount to $25\mu s$. Therefore E_{DON} and E_{DOFF} are always less than $1mJ$ and P_{DAVG} is less than $0.5W$. In the worst case scenario of $I_{MAX} = 8A$ and $V_{BAT} = 50V$ then P_{DAVG} is about $4W$, which can be reduced to $2W$ using a faster slope control at $400mA/\mu s$ (fast control set of the RCD). The P_{DAVG} contribution should be added to the power dissipation when the PMOS is on, due to non null R_{DSon} resistance: $P_{DON} = D * R_{DSon} * I_{MAX}^2$ being D the duty cycle of the PWM driving command. For typical values of

3 Drivers for inductive loads

$I_{MAX} = 5\text{A}$ and $R_{DSon} = 60\text{m}\Omega$ and worst case values of $I_{MAX} = 8\text{A}$ and $R_{DSon} = 100\text{m}\Omega$ then P_{DON} is up to 1.5W and 6.4W respectively. The RCD power stage has been designed so that such power dissipation values can be sustained.

From the above case example is clear that, by proper controlling the current slope in the range of hundreds of $\text{mA}/\mu\text{s}$, the main contribution to power dissipation is due to P_{DON} . On the contrary, if the current slope is not controlled, and is in the range of tens of $\text{mA}/\mu\text{s}$, then the above P_{DAVG} power dissipation becomes the dominating contribution reaching critical values for the HV-PMOS.

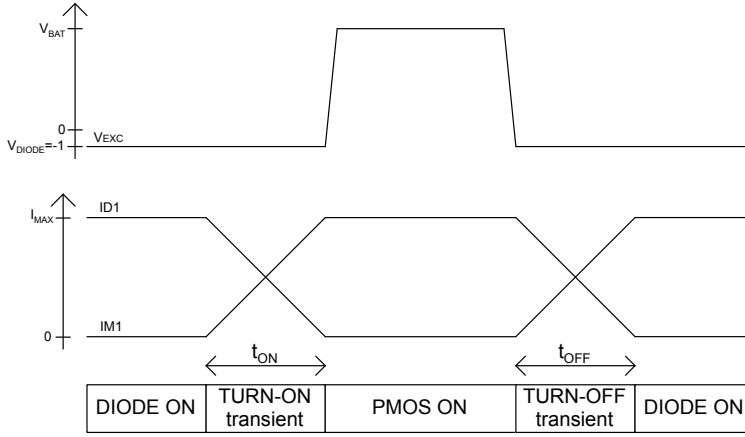


Figure 3.20: *Gate-Driver transients*

After analyzing the behavior of the smart gate driver during transients, hereafter its configuration during on and off steady states is discussed. During the on steady state to lower the R_{DSon} and minimize the power dissipation, the switch S1 in Fig. 3.19 is closed in position 2, connecting the output of the gate driver to V_{SGMAX} and forcing the maximum allowed V_{SG} to lower the R_{DSon} resistance of the PMOS. To be noted that the gate driver is supplied between V_{BAT} and ground, but its output is limited between V_{BAT} and $V_{BAT} - V_{SGMAX}$, which is generated subtracting a band-gap stabilized voltage reference of about

3.5V from V_{BAT} . Since V_{SGMAX} has been generated using a bandgap circuit its value is stable in a wide temperature range and is always within the maximum operating value of 3.6V reported in Table 3.3. During the off steady state the switch S1 in Fig. 3.19 is closed in position 1 and the output of the gate driver is V_{BAT} forcing the HV-PMOS off ($V_{SG} = V_{SGMIN} = 0$).

Current Sensing and Monitors

The current sensing block in Fig. 3.21 is in charge to read back the current flowing in the switch and to send this information to the digital part[35]. Moreover it informs the digital part if a fail status is reached. It sends to the digital part two diagnostic flags: the OPEN flag is set when the coil current is below a fixed threshold (about 20mA) to inform that the rotor coil is disconnected and the SHORT flag is set when the current is higher than the maximum allowed current (programmable between 8.5 to 12A) to detect fast current spikes, e.g. due to a short on the rotor coil windings. The used ADC is a 10-bit successive approximation converter (SAR) with a main clock of 704kHz and a sample rate of 64kHz. Such frequencies allow for fine time resolution of the alternator regulator as foreseen in recent works [33, 34]. A complete block diagram of this block is shown in Fig. 3.21.

The V_{TH1} and V_{TH2} thresholds are calculated following the Eqs. (3.9) and (3.10).

$$V_{TH1} = R_f * I_{TH1}; I_{TH1} = 0.02\text{mA} \quad (3.9)$$

$$V_{TH2} = R_f * I_{TH2}; 8.5\text{A} < I_{TH1} < 12\text{A} \quad (3.10)$$

An integrated temperature sensor is also present forcing in off state the power switch when the measured temperature value is beyond a programmable threshold.

Moreover the reference current used in the ADC is temperature stabilized since it is generated as the sum of a PTAT (proportional to absolute temperature) current and of a CTAT (complementary to absolute temperature) current. A

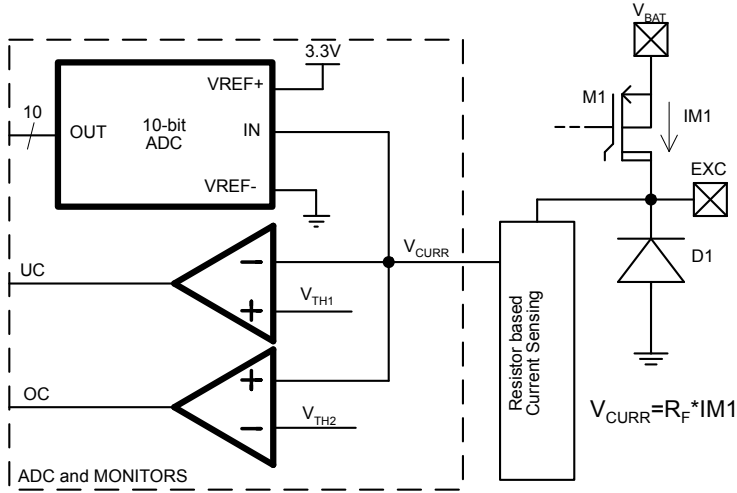


Figure 3.21: ADC and monitors block diagram

trimming structure on the overcurrent detector and a software calibration on the output of the ADC have been also implemented. Particularly, during the calibration phase, a fixed current is imposed on the rotor coil and the same current is acquired through the ADC. Doing the calibration with two different current values is possible to compensate the offset and gain error of the ADC.

3.2.2 Layout

The Rotor Coil Driver has been realized in 0.35 μm HV-CMOS technology and integrated in an alternator voltage regulator.

Fig. 3.22 shows the layout of the complete voltage regulator IC (see Chapter 5) and highlights the PMOS, diode and control logic placing. Table 3.4 highlights the area contribution of the RCD, 29% of the total regulator area. The main contribution is due to the HV-PMOS and diode, see Fig. 3.22, which are 16% and 10% of the total regulator while the low-voltage control logic occupation is limited to about 3%.

Table 3.5 shows the electrical and environmental operating and absolute ranges of the RCD, determined by design choices and verified by experimental

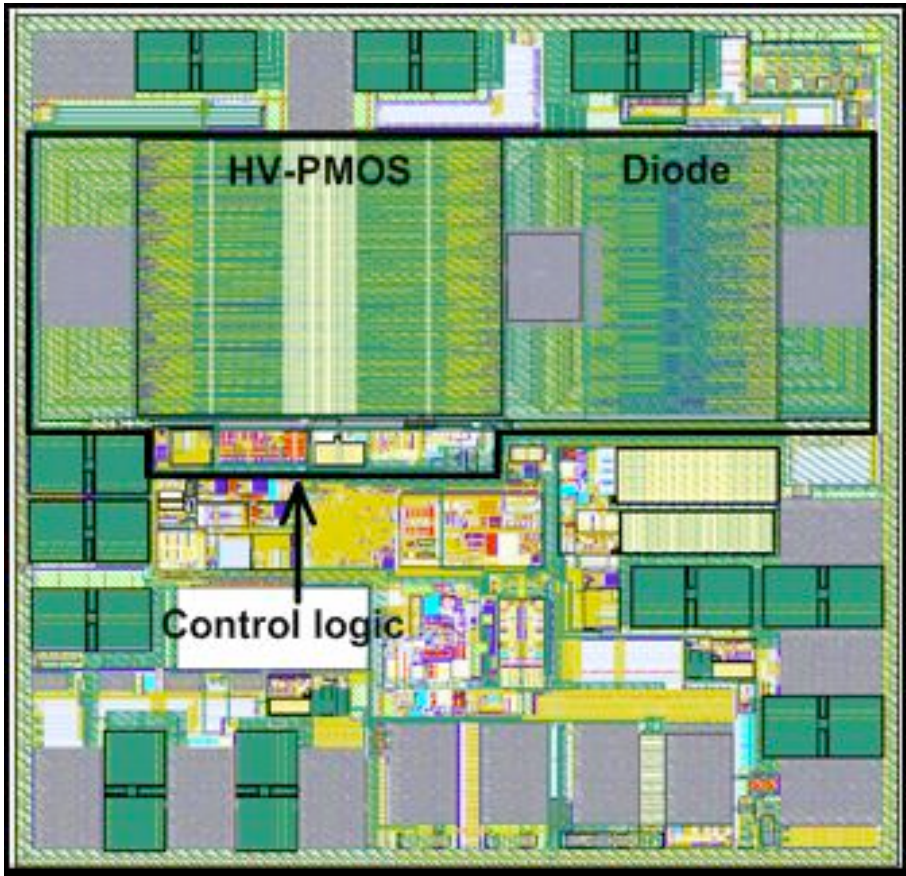


Figure 3.22: Alternator Voltage Regulator IC with the designed rotor coil driver

measurements on realized IC samples.

3.2.3 Quality and safety aspects

It is worth nothing that to meet "zero defect" automotive requirements in the design phase it has been verified that every device in the RCD is working in the safe operating area with the lifetime acceleration factor close to 1 in order to increase the Mean Time To Failure (MTF). As already discussed before, ESD, EMC and on-chip diagnostic and protection issues have been addressed and

Table 3.4: Rotor Coil Driver area occupation

Block	Rotor Coil Driver	HV-PMOS	Diode	control logic
Area, %	29%	16%	10%	~ 3%

Table 3.5: HV-PMOS and HV-NMOS operating and absolute ratings

	Min	Typ	Max
Operating Junction Temperature ($^{\circ}\text{C}$)	-40		150
Absolute Junction Temperature ($^{\circ}\text{C}$)	-40		180
Operating Battery Voltage (V)	6	14.4	55
Absolute Battery Voltage (V)	-3.2		55
PMOS R_{DSon} (m Ω)	43	62	96
Trimmable overcurrent detection (A)	8.5		12
Current slope slow (mA/ μs)	150	200	250
Current slope fast (mA/ μs)	300	400	500
ESD-HBM (kV)	-8		8

a “design for testability” (DFT) flow has been followed to achieve full analog coverage.

Moreover High Temperature Operating Life (HTOL) qualification tests have been implemented and, to recognize weak devices at test, PAT (Part Average Testing) and Statistical Bin Analysis (SBA) techniques have been addressed. To be noted that during RCD testing and validation it has been verified that the device can temporary work above 150°C and 180°C but lifetime validation tests, such as the HTOL qualification test, have been done at 150°C . A detailed description of the followed ASIC design flow with the $0.35\mu\text{m}$ HV-CMOS AMS technology is reported in [36].

The reliability of the RCD has been proven forcing the driver to switch permanently at maximum duty cycle and at maximum ambient temperature in order to reach junction temperature around 150°C without performance degradation.

3.2.4 Validation

Hereafter the validation phase of the RCD will be explained.

The RCD turn-on and turn-off behavior has been first simulated and then measured.

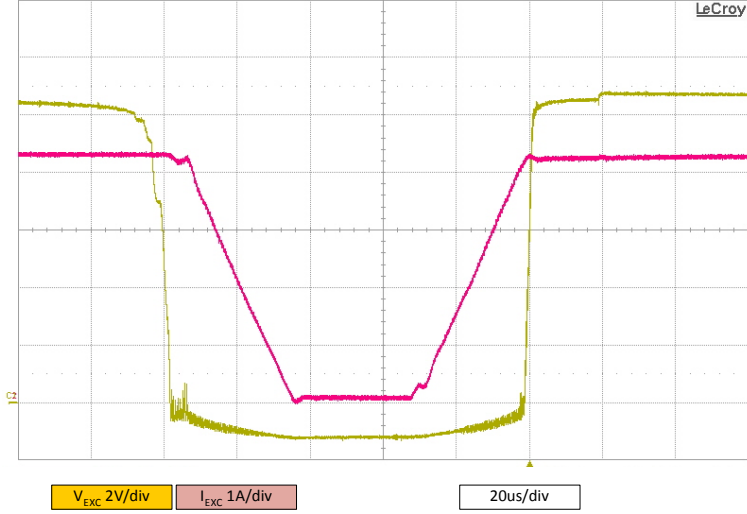


Figure 3.23: *Voltage and current in the rotor coil*

Fig. 3.23 shows the typical behavior of voltage and current in the rotor coil. The rotor excitation voltage (EXC), in yellow, goes from the battery voltage to about -1V, while the current, in red, goes from 0A to 4A. Details of the turn-on and turn-off phases changing the slope control bit are visible in Figs. 3.24 and 3.25.

In Fig. 3.24 the measurements are done setting the *SLP_CTRL* bit cleared (slow current slope: 200mA/μs), and the measured value is about 197mA/μs, while in Fig.3.25 the *SLP_CTRL* bit is set (fast current slope: 400mA/μs) and the measured current slope is about 383mA/μs.

3 Drivers for inductive loads

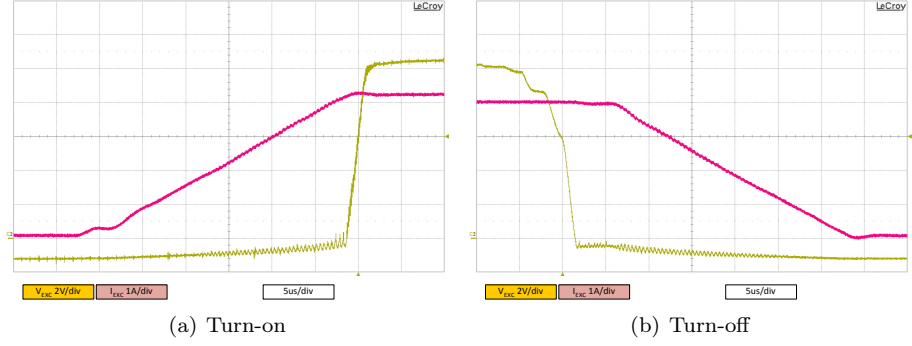


Figure 3.24: *Slow current slope*

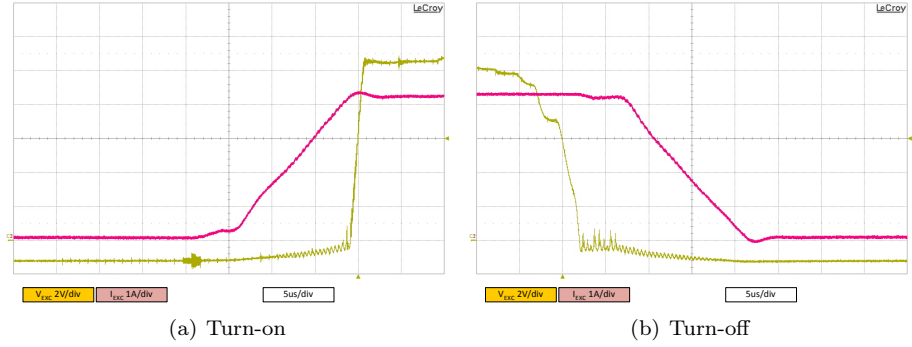


Figure 3.25: *Fast current slope*

The RCD has been thermally characterized in the range -40°C to 180°C using the Thermostream TP04300A system. Hereafter some measurement results are shown.

As example Fig. 3.26 shows the measured variation over the temperature of the R_{DSon} of the PMOS, which is always quite below the $100\text{m}\Omega$ target in the operating range from -40°C to 150°C (tests have been done with currents from 0.1A to 2A obtaining similar results).

As another example of thermal characterization in the extender range -40°C to 180°C , Fig. 3.27 shows the measured variation versus the temperature of the voltage drop of the diode D1 in Fig. 3.19 when is in forward condition

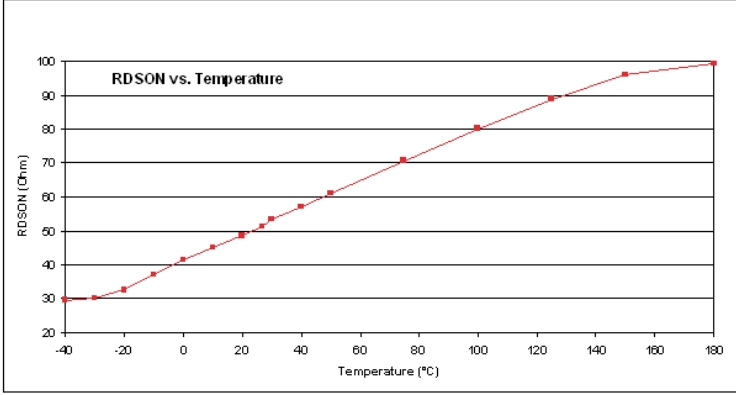


Figure 3.26: $R_{DS(on)}$ of the HV-PMOS vs. Temperature

(V_{diode} in Fig. 3.27) and of the V_{SG} of the HV-PMOS when the transistor is in on-state ($V_{SG} = V_{SGMAX}$). Fig. 3.27 demonstrate the good stability versus the temperature of the designed driver.

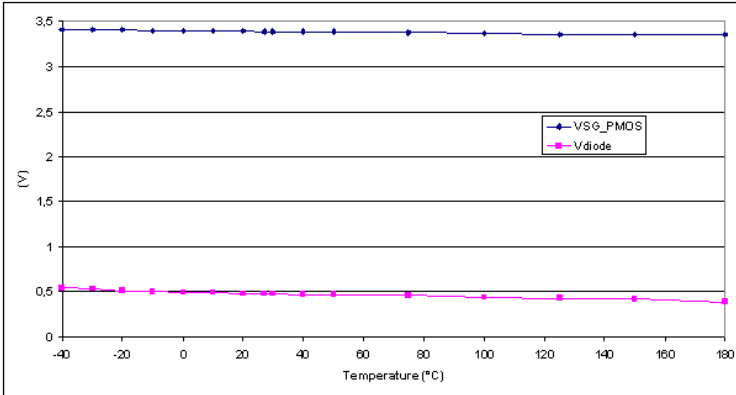


Figure 3.27: V_{SG} of the HV-PMOS and V_{diode} vs. Temperature

4 LED Driver IC design for automotive lighting

In the last years, the LED technology is experiencing a very fast and important growth, superseding the bulb technology as lighting source in home and automotive lighting applications[37]. In fact, to achieve the harsh environment requirements as CO₂ emissions and reduce the fuel consumption, the car makers needs to reduce the total power consumption of the vehicles, and the adoption of LEDs must be seen in this way, because they dissipate 5 times less power at equal output lighting intensity.

As the LED technology is constantly growing, the LEDs have reached the the needed quality and reliability factor that permits their use in automotive applications and their cost is constantly decreasing.

However, compared with bulbs, the LEDs are more difficult to drive and therefore LED-drivers requires more control functions than bulb-drivers.

Furthermore, automotive applications require compact and low-cost solutions, that must be interfaced to digital ECUs and to cope different wiring configurations and relevant parasitics[38].

Automotive lighting systems should be also robust respect to EMI and over-temperature, over-current and over-voltage phenomena, such those due to ringing effects generated by resonance of wiring inductance and connector capacitance. Usually in automotive environment, few meter long cable are used, generating dumped oscillations that can reduce the LEDs lifetime and lighting efficiency, in addition to system issues if those phenomenas are not well considered[39].

Indeed, to limit or avoid this phenomena, the LEDs cannot be driven by

mechanical relay, but a smart driver is required to control the slope of the LED current during transients, keeping it below the characteristic frequency of the wire.

The main difficulties in the design of an universal LED-driver, flexible enough to be applied to different wiring configurations, are the ringing and EMI issues. These problems depend on environmental and parasitic components that are difficult to predict and simulate. While bulbs are easily modeled as linear PTC (Positive Temperature Coefficient) resistors and are less sensitive to parasitic components, a LED is a special diode and follow the Shockley exponential V-I law. A very small fluctuation on the voltage across the LED can generate a very high variation on its current affecting, as shown in [39], both efficiency and lifetime and creating lighting disturbs. This behavior can generate ringing and high current spikes if the LED is not properly driven. By the same token, a bulb-designed driver, as shown in [40, 41], cannot be directly used to drive efficiently LEDs. This is particularly true when the LED and the driver are separated by a few meter cable as in automotive connections. In this case the wiring parasitics can generate ringing and EMI.

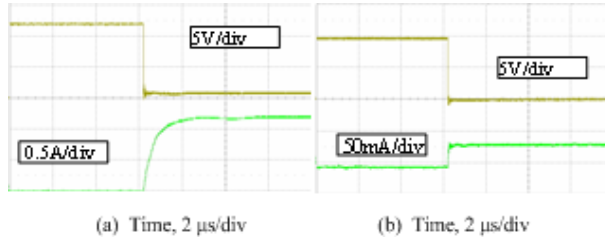


Figure 4.1: *Bulb (a) and LED (b) behavior with 10cm long connection cable*

Figs. 4.1 and 4.2 shows a comparison, based on experimental results, between the turn-on transient of a 2W bulb lamp and a 0.1W LED with different cables. Respectively, Fig. 4.1 highlights the behavior with a very short wire, about 10cm long, and Fig. 4.2 shows the behavior with a long wire, about 3m long. In those pictures, a simple relay is used as switch to highlight the different behavior of those loads and they show the necessity of using a well-designed

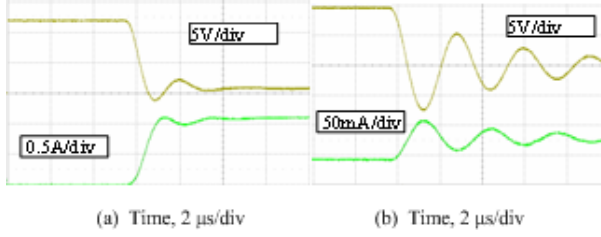


Figure 4.2: Bulb (a) and LED (b) behavior with 3m long connection cable

driver for LEDs, to avoid unwanted effects due to wiring parasitics. Indeed, the behavior of the current in the bulb does not change significantly with the cable length (shown in Figs. 4.1(a) and 4.2(a)), while the current in the LED shows significant differences (highlighted in Fig. 4.1(b) and 4.2(b)).

4.1 Flexible LED driver IC

Respect to bulb driver shown in [42, 41], the smart LED driver needs to fulfill the same harsh automotive environment constrain, but the driving of LEDs has required the implementation of specific techniques to limit the undesired effects of wiring parasitics, such as ringing and consequent overshoots and undershoots.

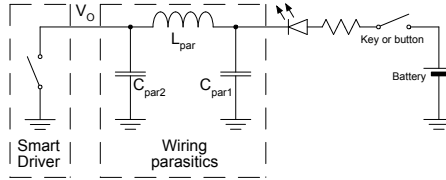


Figure 4.3: Highlight of wiring parasitic

In Fig. 4.3 the scheme of the wiring parasitic and of a possible connection between the driver and the load is shown: the output pin of the driver, which is represented by a switch to ground, is connected to a LED, in series with the car battery and a mechanical switch, that is controlled by the user through a button or a ignition key.

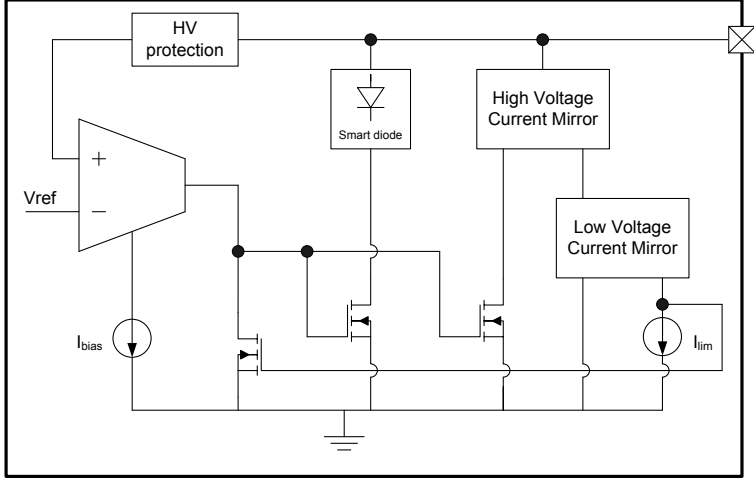


Figure 4.4: Architecture of the LED driver

The basic scheme of the flexible LED driver is shown in Fig. 4.4: the architecture is based on two nested control loops. The inner loop limits the output current to 1A, while the outer loop regulates the output voltage to a reference voltage (V_{ref}). The *Smart Diode* in series to the power switch (an HV-LDNMOS) is a complex structure that acts as an HV-Diode with a very low forward voltage and provides the reverse polarity capability to the device. The inner loop, which limits the output current, protect the driver in case of short circuit and permits the use of this driver also as bulb-driver.

The outer loop, regulating the output voltage to an intermediate value, permits to detect the status of the switch on the battery with a simple comparator, independently from the status of the driver. Indeed, when the driver is turned ON, the output voltage is independent from the current that flow inside and a simple comparator can detect the status of the switch.

A more detailed description of the functional behavior of this LED driver can be found in [40, 43].

Finally, the LED driver has been integrated as hard macrocell in a complex

automotive control unit that regulates the alternator output voltage, implemented in Austriamicrosystems 0.35 μ m HV-ASIC technology.

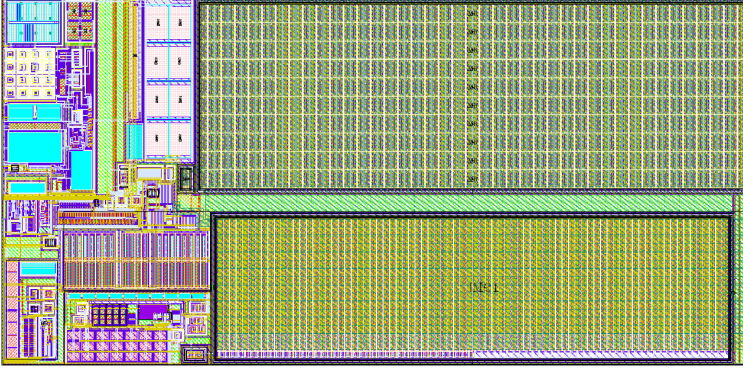


Figure 4.5: *Layout of the LED driver*

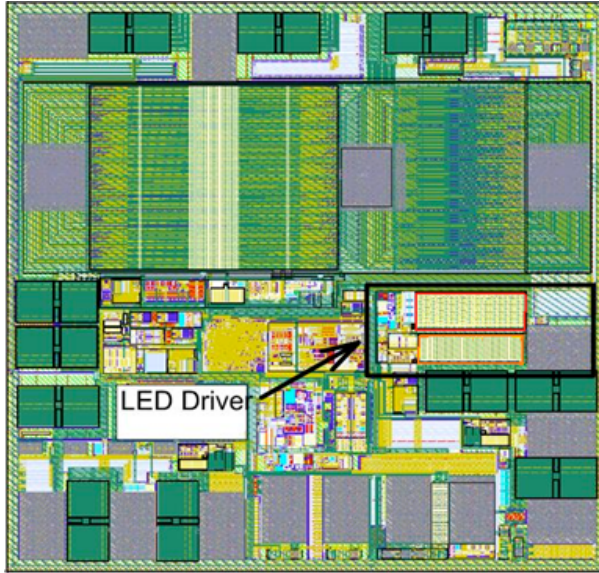


Figure 4.6: *Layout of the automotive IC with the LED driver*

Fig. 4.5 shows the layout of the LED driver, while Fig. 4.6 shows the complete alternator voltage regulator, highlighting the LED driver placement.

4.2 Validation

The behavior of the LED driver has been validated and some experimental results are shown.

For the measurements, real automotive cables are measured and then the extracted parasitic components, see Table 4.1, are used for the following measurements.

Table 4.1: Wiring parasitic measurements

	L_{par} (μH)	C_{par1} (nF)	C_{par2} (nF)
Range	3 – 5	10 – 50	50 – 200

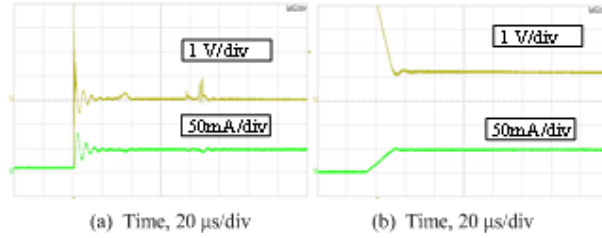


Figure 4.7: Output voltage and current during the turn-on transient

Fig. 4.7 compares the results achieved with the current slope control disabled (a) and enabled (b), when the load is the series of three 0.1W LEDs with only 50mA forward current.

In this case, when the current slope control is disabled, ringing phenomena can occur. The ringing phenomena disappear if the slope control is enabled, as shown in Fig. 4.7(b).

To evaluate the LED driver with an higher DC current, the same measurements of Fig. 4.7 has been repeated changing the load with the parallel connection of five 0.1W LEDs, each one forward biased with 20mA. So, the total current that is flowing in the LED driver is 100mA, twice the value of the previous measurement. Fig. 4.8 shows the results achieved without the current slope control (a) and with the current slope control (b).

Also in this case, when the current slope control is enabled, the ringing phe-

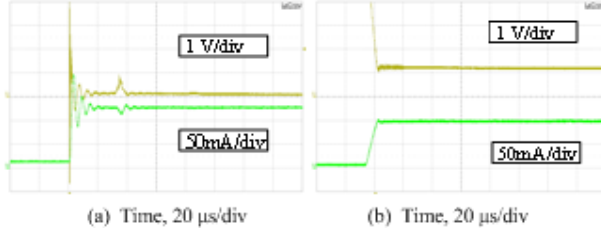


Figure 4.8: *Output voltage and current during the turn-on transient*

nomena disappear.

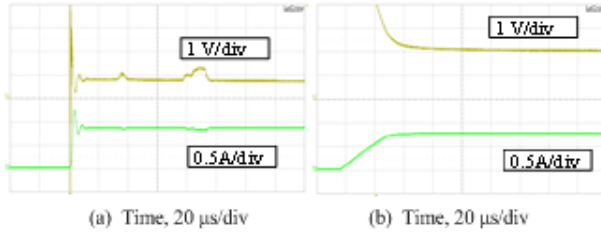


Figure 4.9: *Output voltage and current during the turn-on transient*

In the last measurement, a real high power stand-alone LED, SST-90 from Luminous Inc. [44], is used with 900mA forward biased. Also in this case a comparison between the current slope disabled (a) and enabled (b) is shown in Fig. 4.9.

5 Voltage regulators for automotive alternators

The automotive alternators transform the mechanical power, picked up on the engine, in electrical power to be delivered to the battery and to the electrical loads of the car.

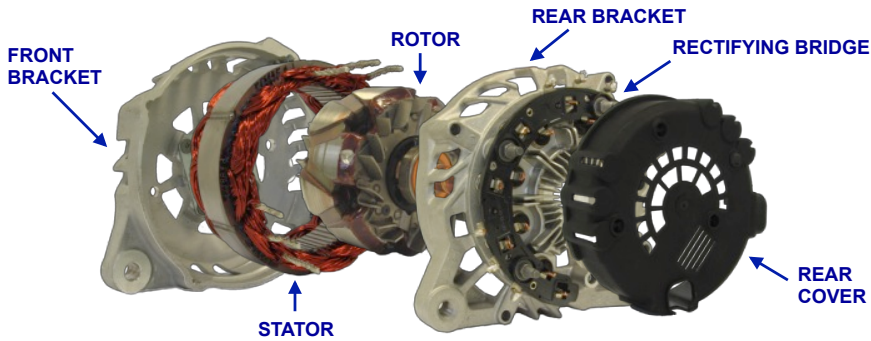


Figure 5.1: *Exploded view of an alternator*

The power machine (Fig. 5.1) consists of the rotor and stator coils, that generates an alternating voltage, and the rectifier diode bridge, whose output is the DC voltage for battery and loads. The rotor coil, belt driven by the pulley and rotating with the engine, generates a magnetic field that is induced in the single or double three phases stator. Amplitude of the alternating voltages on the phases of the stator, and then the direct output voltage, depends on the amplitude of the biasing current of the rotor coil and on its rotational speed. The biasing current is supplied to the rotor through a pair of brushes, which realize the electrical contact between static and rotating parts. This contact

Two phases from the stator outputs are connected to the ASIC die in order to monitor the speed and the level of phase signals. The regulator communicates with the ECU through a dedicated connection and, in case of malfunction, alters the driver switching on a lamp on the dashboard. Fig. 5.2 shows physical blocks of a regulated alternator and electrical connections on the vehicle.

The mechatronic brush holder, shown in Fig. 5.3, includes on one hand the bare ASIC die silver glued directly on a heat sink and wire bonded on a lead-frame, and on the second hand the brushes and the connectors to the power machine of the alternator and to the vehicle engine control unit.

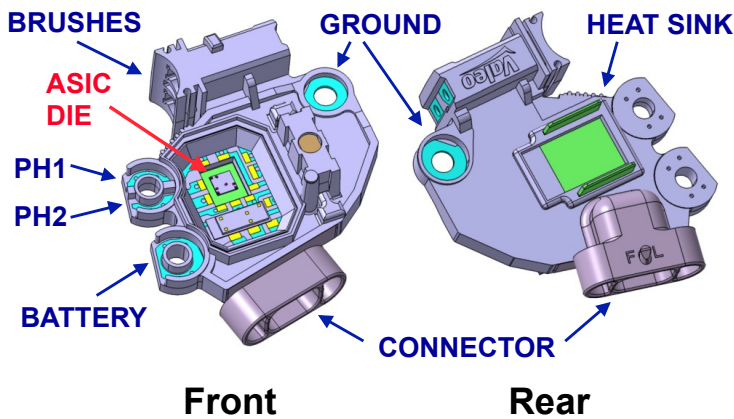


Figure 5.3: *Mechatronic top and bottom view*

The regulation principle is based on a closed loop, as depicted in Fig. 5.4[45].

The direct chain of the loop includes a proportional or proportional-integral error corrector, which acts on the amplitude of the excitation field generated by the rotor coil[46, 47]. The amplitude is controlled by the excitation duty cycle managed by the power stage. The excitation field induces a stator voltage that delivers current to the battery through the bridge rectifier. The feedback chain of the loop picks up the voltage amplitude signal on the battery, through the sense connection, and, after a proper and anti-aliasing filtering, converts it to the digital domain for comparison with the reference. Note that some regulator loop are fully analog. The result of the comparison is applied to the

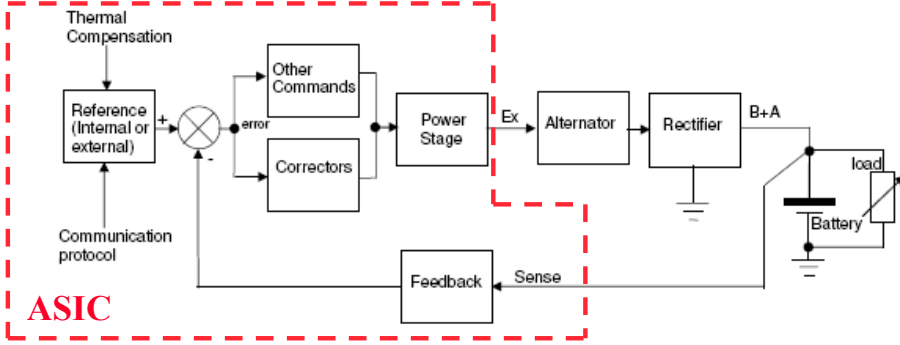


Figure 5.4: Regulation loop principle

direct chain. The reference voltage is set by the internal or external reference. The feedback chain and the error corrector are integrated in the ASIC die, which power stage includes the rotor coil driving circuit. As Fig.5.5 shows, the rotor excitation coil is driven by an high side driver switch and a low side freewheeling diode.

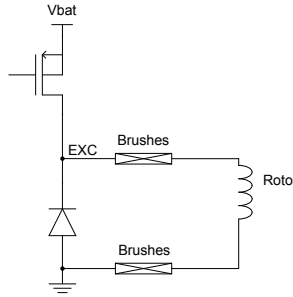


Figure 5.5: Rotor excitation driver

The gate of the high side switch is driven by a square wave fixed frequency signal in a range of 60Hz to 400Hz depending on a trade-off behavior stability versus power losses. Some regulators used free excitation frequency with a fixed duty cycle. Rotor current is modulated changing the duty cycle of the square wave signal from minimum DC (0% to 5%) to 100% (maximum field). Those differences are directly linked to customer specifications that have to be implemented in their dedicated product.

Alternator regulators are among the most demanding automotive SoC application with respect to the combination of harshest reliability requirements, such as temperature, voltage and current. The complete alternators are mounted in the engine compartment, where the under roof ambient temperature requirement (-40°C to 125°C) leads to a maximum operating junction temperature which is currently 150°C and up to 180°C - 200°C for future applications. The rotor coil that generates the excitation field of the alternator requires very high currents (up to 4A) with a well controlled duty cycle to guarantee the regulation accuracy, but during cold and cranking condition the rotor current can even go up to 8A. In case of rotor short circuit, fast current spikes up to 15A are observed. At present, the maximum voltage requirement for the alternator supply is 65V, which is the battery voltage overshoot limit due to alternator zener diode rectifying maximum voltage in case of unexpected harness surges. To be noted that all regulator pins shall be protected against sudden surges such as ESD and others sparkling pulses due to harness coupling.

Considering that actually the swap of the battery pins can be one of the main causes of failure in alternators, the battery pin of the regulator has to withstand -3.2V, which is the maximum voltage across the series of two power diodes of the rectifier bridge of the alternator in forward biasing conditions. All the other HV pins shall withstand a reverse polarity voltage of -15V without damage in case of error during maintenance. Furthermore a ground shift can appear between the ground of the alternator and the negative terminal of the battery because of the high currents delivered by the alternator to the battery or sunk from the battery by the starter during cranking.

The alternator is one of the most power demanding part of the vehicle, transforming mechanical power to electrical power, and, due to car maker fuel reduction programs, improving the efficiency of the alternator is mandatory.

The efficiency of that machine can be improved in three ways: electrical engineering design of the machine[48], rectifying losses[46, 49] and regulator behavior[47].

5.1 New alternator development

In order to improve the development lead time, the functions can be developed in two steps. The first step is related to the electronics for interfaces, which realize the signal adaptation and conversion ones is standard or easily adapted to the alternator specifications. These interface functions are usually analog and the most difficult to design because the system has to fulfill the automotive requirements and, in particular, the Electro-Magnetic Compatibility (EMC) and the Electro-Static Discharge (ESD) constraints[50]. Furthermore very harsh requirements in terms of temperature, voltage and current, lead to use high cost technologies for dice manufacturing. The digital part, that does the regulating algorithms, have less environmental constraints, but needs to be changed and adapted between different alternators.

The implemented new type of intelligent and flexible alternator regulator[45] with programmable functionalities is based on two different electronic parts: an **IC** (electronics for interfaces) and a **FPGA** (electronics for algorithms). The IC is used to manage the interfaces between the alternator, the power train signals and the FPGA and includes the power stage that supplies the current to the rotor. The FPGA, assembled on a mezzanine board, is the programmable brain of the regulator and communicates with IC through a 3-wire serial protocol. Both are located inside a standard brush-holder, making possible the test of the alternator directly inside a current car in a real environment (Fig. 5.6).

The target is to use this demonstrator system to develop a new generation of regulators, with improved performances and higher flexibility, where the electronics for algorithms already validated in the demonstrator is transferred to the digital part of the IC. This approach reduces the risks and the costs of design changes and increases the possibility to adapt the product to the new requirements.

Fig. 5.7 shows the proposed system architecture and the interconnections between the blocks.

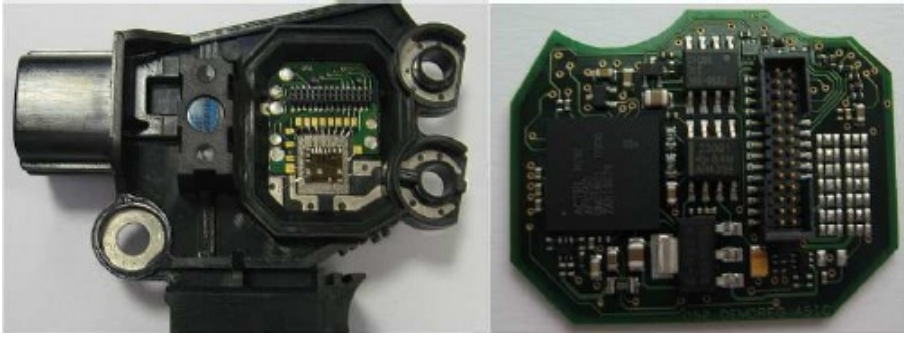


Figure 5.6: Assembled brush holder with the IC (left) and mezzanine board with the FPGA (right)

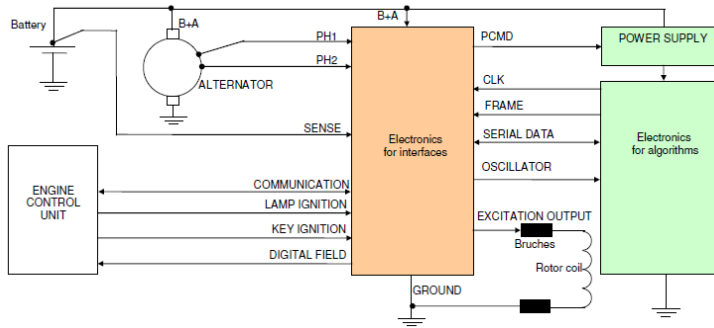


Figure 5.7: Electronic system block definition

Electronics for interfaces The electronics for interfaces is in charge of signal adaptation and conversion and is connected directly to the alternator and to the ECU. It converts the sensed battery voltage to the digital domain (ADC) and sends, via the serial communication channel, the feedback data of the regulation loop to the electronics for algorithms. It also sends the information regarding the status of the alternator in the car, like key insertion, engine rpm and data received from communication with ECU. This part receives from the FPGA the information to manage the regulation function and the data to send to the ECU. The electronics for interfaces includes all the power stages: the power MOS for field excitation, the free wheeling diode and the power transistor for the lamp stage.

Electronics for algorithms The flexibility of the FPGA, which is fully programmable in a very short time, allows the possibility to test on the system various algorithms as, for instance, different control loop solutions. The electronics for algorithms implements the regulation control loop making use of the data received from the electronics for interfaces (feedback voltage converted to digital) and generating the signals to drive it (duty cycle of the rotor excitation driver). Since this algorithm is programmable, the proposed mixed signal architecture solves many stability issues that arise during regulator development or when the designed regulated alternator is transferred from one vehicle platform to another with varied equipments and a different electrical power network.

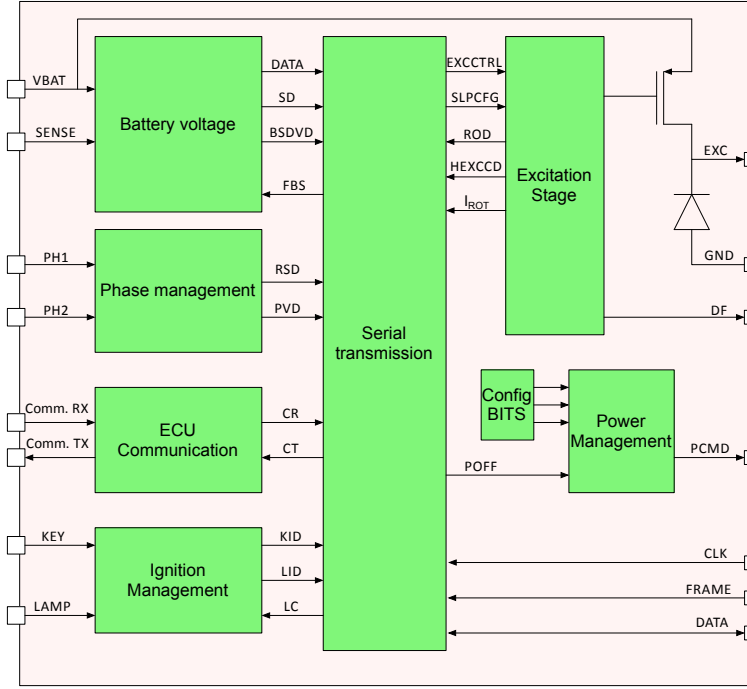
The FPGA controls the functionalities of the entire alternator. Furthermore it manages the communication with ECU, coding and decoding the information, decides the state of the alarm lamp, turning it on when something goes wrong, and sends the power off signal when the engine is stopped.

5.2 IC design

The IC was developed using the H35 technology from Austriamicrosystems. It is an high performance low cost HV-CMOS technology able to integrate on the same die low voltage and high voltage devices. The design has taken into account the required maximum junction temperature (at least 150°C), the maximum absolute voltage (at least 65V) and the reverse polarity requirements on pins. To guarantee the lifetime of the battery charge when car is long time stopped it has been necessary to introduce a standby condition with reduced current consumption of the IC.

The implemented IC can be divided into 7 main blocks. A simplified block diagram of the IC is shown in Fig. 5.8:

Battery Voltage Block The main task of this block is to generate a digital value from the voltage sensed on the positive battery contact, which is the feedback of the regulation loop. A 10bit ADC is used. The voltage drop on

Figure 5.8: *Simplified block diagram*

power cables caused by the large flowing currents is not included in the ADC conversion because a sense pin on battery contact (SENSE) is used. Depending on the car maker charge strategy and on diagnostic, the FPGA can select if the loop has to use the sense path or directly the supply path on the battery pin (VBAT) of the IC. Furthermore this block monitors the sense path and generates two digital signals (SD , $BSDVD$) that indicate if a failure on this path occurs. The SD signal informs the FPGA when the sense cable is connected or disconnected. This information can be used to control the close loop on the battery pin (VBAT) instead on the sensed output of the rectifier bridge. The $BSDVD$ checks the voltage difference between the sense and the battery pins of the IC and it is used to indicate when an abnormal voltage is present between VBAT and SENSE. For instance a resistive path on sense can give a battery voltage sensing to the regulation loop lower than expected and

the alternator voltage can increase. Consequently and for safety, the algorithm forces the control of the close loop to the battery voltage pin of the IC, avoiding electrical damages and overloaded battery.

Phase Management Block This block measures the amplitude and the frequency on two of the three stator phases. The frequency on phases is measured as soon as possible when the alternator is in motion in order to manage the lamp status signal and the transition between pre-excitation mode (without regulation, a small current is supplied to the rotor, used to increase the magnetic field amplitude) and normal mode (with regulation). As soon as the amplitude voltage on phases is sufficient, the block starts to generate digital signals for FPGA with information about the rotational speed frequency of the engine (*RSD* signal) and the amplitude of the magnetic field (*PVD* signal). Particularly these signals indicate to the electronics for algorithms when the amplitude on the phases is enough to wakeup from standby mode because alternator is rotating without ignition, and when the frequency to start the regulation mode is achieved. Furthermore the information on the rotational speed can be used by the algorithm to improve the performance of the system and sometime used for the driver speedometer.

ECU Communication Block The ECU Communication block is composed by a receiver, a transmitter and an activity detector. The receiver and the transmitter operate as level shifter, translating from ECU levels to FPGA levels and vice versa. The activity detector is used in order to wakeup the IC when the ECU transmits some data.

Excitation Stage Block The excitation stage is in charge to manage the current flow inside the rotor and includes the high side switch and the low side free-wheeling diode. The FPGA sends to this block the order to increase or decrease the rotor current changing the duty cycle of the *EXC_CTRL* signal, the PMOS gate control. The excitation stage turns ON or OFF the Power-PMOS according to the received order.

The development phase of the excitation stage block is well described in section

3.2.

Power Management Block The power management block has the task of wake-up or shutdown the IC and the FPGA. In stand-by mode the current consumption of the IC is reduced below $200\mu\text{A}$ and the FPGA is switched off. When the key is turned on, activity from ECU is detected or the engine starts rotation, this block sends the wakeup signal to the IC and the FPGA. In order to improve the IC wakeup strategy, it is also possible to decide, via a configuration bonding wire on the IC, which signal can not wakeup it. Only the key ignition signal can not be left out. When the electronics for algorithms detects no activity on the signals, after a certain delay, it sends an order to the power management block, turning off the power supply. Figure 5.9 shows how it works.

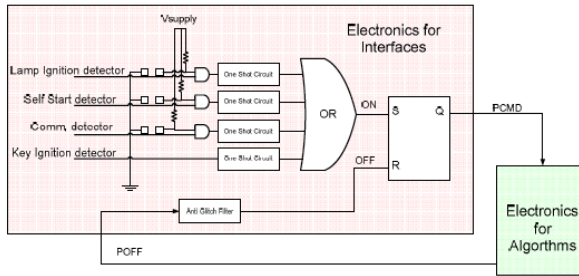


Figure 5.9: Power up strategies

Ignition Management Block The ignition management block is in charge of detection when an ignition condition happens. It monitors the state of the key using two ways. The first monitors directly the key status indicating to the FPGA when the key is plugged and engaged, activating the *KID* signal. The second monitors the key with an alert lamp in series. In this way, is possible to monitor when the key is engaged (*LID* signal) and to drive an alert lamp that indicates to driver when something is abnormal, through the *LC* signal.

Serial Interface Block The serial interface is in charge to manage the communications between IC and FPGA. It uses a 3-wire serial protocol with a clock frequency of 2.816MHz. Two wires are used to receive the system clock and the communication direction (called frame) from FPGA to IC and the third wire is used for data exchange. The frame exchanged between IC and FPGA is composed by 43 bit (36 from IC to FPGA and 7 from FPGA to IC). Clock frequency has been chosen considering the number of bits inside a frame (Nbit) and both the quantization error on the duty-cycle of the excitation signal and the sample-rate of the sensing ADC. For a good regulation the system needs a minimum sample rate of about 64kHz and a resolution of about 1 by 256 on the excitation field duty-cycle. Considering the equation (5.1), equation (5.2) was used to calculate the system clock frequency.

$$F_{exc} = 250\text{Hz} , N_{bit=44} , N_{frame} = 256 \quad (5.1)$$

$$F_{clk} = F_{exc}N_{frame}N_{bit} = 250 * 256 * 44 = 2.816\text{MHz} \quad (5.2)$$

5.3 Quality and safety aspects

The alternator must be able to detect when a fault condition occurs, and signal it to the driver.

To cover the possible faults on wiring connection, many diagnostic signals monitor constantly the connection of the alternator to the car. The SD and BSDVD signals monitors the connection on the SENSE and VBAT wiring. The combination of PVD and RSD signal can detect when one of the phases connection (PH1 or PH2) is disconnected. The diagnostic block on the Rotor Coil Driver, well described in section 3.2, permits to detect the disconnection or the short condition on the rotor.

Moreover, an overvoltage detector on VBAT and a rotational speed detection on the phases permits to increase the fault detection coverage and an overtemperature protection avoid silicon failure due to high power dissipation.

The bulb/LED driver, implemented on the alternator voltage regulator IC, turns ON the lamp on the dashboard to signal to the driver that a fault condition has occurred.

Finally, to prove the reliability of the voltage regulator, it has been kept switching at maximum ambient temperature and with the maximum excitation current, in order to reach the maximum power dissipation and the maximum junction temperature, without silicon failure.

5.4 Validation: simulations and measurement results

Finally the IC has been manufactured and assembled on the brush-holder together with the FPGA and has been measured.

Fig. 5.6 shows the brush holder with the mounted IC and the mezzanine board with the FPGA, while Fig. 5.10 shows the microphotograph of the designed IC.

The validation phase of the excitation stage is described in section 3.2.4, while this section explain the validation phase of the remaining part of the IC and, finally, of the whole alternator system.

Measurements verified the correct functionality of the entire system, as well as the standby current, the communication, the slope control and the reverse voltage protection.

First of all, the communication between the IC and the FPGA has been checked, ensuring that the data sent is correctly understood by the receiver. This is done by activating a single IC function from the FPGA and checking the right behavior and checking the answer frame that comes out from the IC at the FPGA.

The alternator system, being always connected to the battery, has to reduce its current consumption when the car engine is halted, in order to not discharge

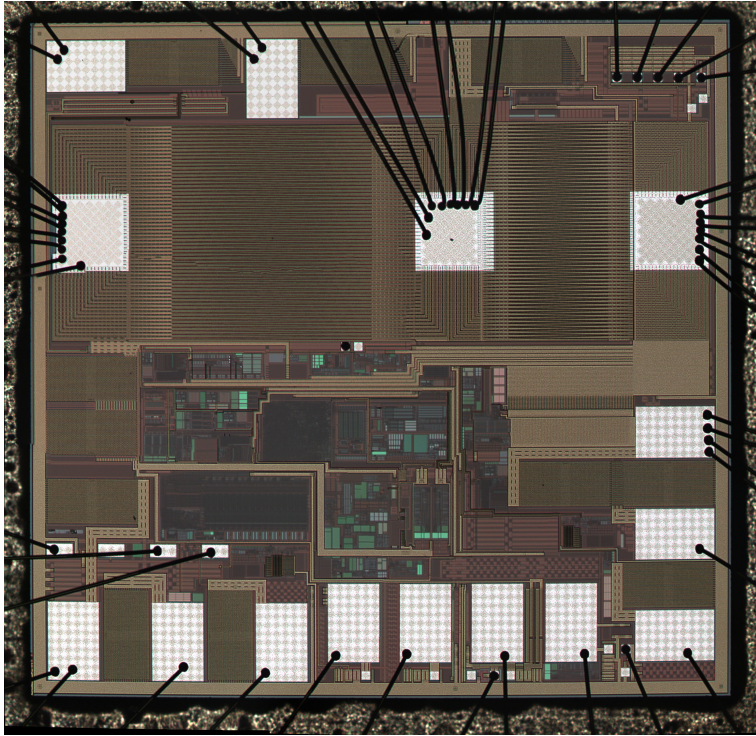


Figure 5.10: *IC microphotograph*

the battery. To do this, when the alternator recognize that the engine is not rotating checking the rotor rotational speed, it goes in a standby mode with a very low current consumption from the battery.

In the designed alternator voltage regulator the measured standby current is only $158\mu\text{A}$, and this very low value permits to increase the battery discharging time when the car is parked.

As required, the IC can withstand a reverse battery voltage of -3.2V and a reverse voltage on the external pins of -15V without any damage for itself. In Table 5.1 the current absorbed in case of reverse bias is shown for each significant pin. The high current value for the COMM.RX, KEY and LAMP pins is due to internal pull-up or pull-down resistor, which carry the reverse current

during the test.

Table 5.1: Reverse voltage protection

Pin	Voltage (V)	Simulated current (mA)	Measured current (mA)
VBAT	-3.2	12	14
PHASE1	-15	220	226
PHASE2	-15	220	226
COMM. RX	-15	4292	4346
COMM. TX	-15	14	14
DF	-15	14	14
SENSE	-15	59.3	61
KEY	-15	3000	3054
LAMP	-15	3815	3968

Finally, Fig. 5.11 shows the measurement bench with the complete brush-holder and the rotor, power supply and oscilloscope on the background.

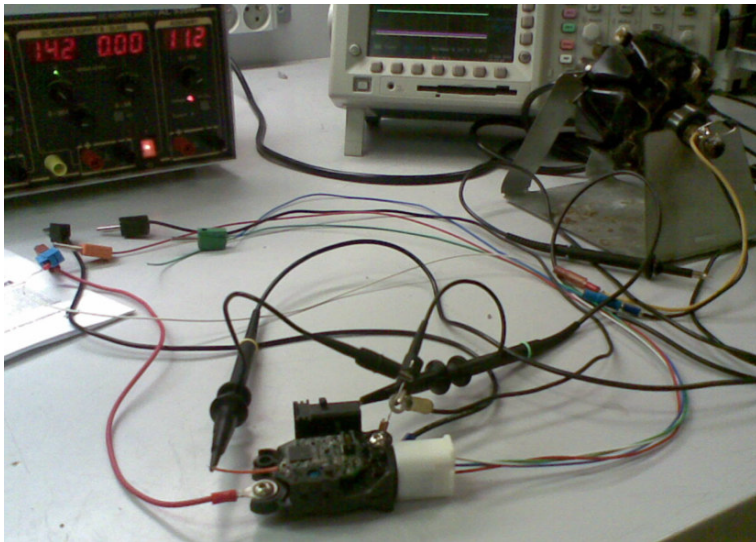


Figure 5.11: *Measuring setup*

Conclusions and Outlook

The purpose of this thesis work was to show the development and validation of innovative Integrated Circuits for automotive applications, focusing on the analog high-power part, like output drivers and power management blocks. All the here proposed circuits were developed, simulated and then realized in Austriamicrosystems HV-CMOS 0.35 μm ASIC technology (H35).

The key research contribution made during the doctoral are summarized below:

- An high-voltage power DC-DC buck converter with very low current consumption was designed and tested experimentally. It can achieve a very high efficiency with low output current and has a very low current consumption both in standby (only 1.8 μA in worst case) and in no load condition (only 25 μA in worst case). Furthermore it can manage a very wide input voltage (from 4.5V up to 50V) and provides a fixed 5V output voltage or an adjustable one.
- A single-chip Smart Driver for inductive, and also capacitive and resistive, loads with very low turn-off time was designed and tested experimentally. The used topology doesn't need the integration of power or zener diodes and can be controlled through high speed automotive CAN or LIN busses or by a micro-controller through SPI protocol. Furthermore it integrates self-monitoring/diagnostic capability to achieve the harsh requirements of the ISO26262 standard.
- An innovative Rotor Coil Driver for automotive alternators with control of the current slope and reverse polarity capability has been developed and validated. It has been designed to carry DC current up to 8A with

very low on resistance, $62\text{m}\Omega$ typical and lower than $100\text{m}\Omega$ in worst case condition. Furthermore it can manage ESD events up to 8kV and permanent over-voltages up to 55V without silicon damaging.

- A smart LED-driver, particularly for automotive lighting applications, has been developed and validated. It implements Soft Start and Current Slope Control techniques and this permits to avoid ringing and overshoot phenomena in presence of wiring parasitics. This will led to reduce EMI and spikes on supply voltages. Furthermore overcurrent and overtemperature protections avoid possible silicon damages. Experimental results with different power levels prove the effectiveness of the control against the wiring parasitics.
- An innovative and effective approach to design and test voltage regulators for automotive alternators with programmable functionalities has been developed. The realized prototype can be used to develop a new type of intelligent and flexible automotive alternators, allowing to check and debug the alternator control loop stability and other functionalities during the alternator development phase, before releasing a final version of the regulator silicon.

Outlook

This research work has provided the basis for enabling the development of very complex automotive Integrated Circuits, that integrates on the same die the high power part with the high speed digital part. Future research direction will focus on always more complex ICs, that continuously integrates on the same die more functions with more high power devices. Furthermore the automotive market is pushing to increase the voltage domain from 12V to 48V . This have led IC foundries to develop automotive high voltage devices[51, 52] with higher breakdown voltages (about 120V actually), keeping as lower as possible the silicon cost, and the automotive IC designers to implement more functionalities with more complex technologies.

Publications

The research leading this results has been submitted to the international scientific community and has been already published or accepted for publication in 2 ISI peer-reviewed international journal and in 5 peer-reviewed international conferences.

One paper has been published on the IEEE Transaction on Power Electronics:

1. S. Saponara, G. Pasetti, N. Costantino, F. Tinfena, P. D'Abramo, and L. Fanucci, "A flexible led driver for automotive lighting applications: IC design and experimental characterization," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1071–1075, 2012.
doi: 10.1109/TPEL.2011.2174653

Another paper has been selected for future publication on the IEEE Transaction on Industrial Electronics:

2. G. Pasetti, L. Fanucci, S. Saponara, F. Tinfena and P. D'Abramo, "HV-CMOS design and characterization of a smart rotor coil driver for automotive alternators", *IEEE Trans. Ind. Electron.*, 2012.
doi: 10.1109/TIE.2012.2192898

The list of the papers that are already published or accepted for publication on international peer-reviewed conference proceedings is:

3. G. Pasetti, L. Fanucci, and R. Serventi, "A high-voltage low-power dc-dc buck regulator for automotive applications," in *Proc. Design, Automation & Test in Europe Conf. & Exhibition (DATE)*, 2010, pp. 937–940.
4. L. Fanucci, G. Pasetti, P. D'Abramo, R. Serventi, F. Tinfena, P. Chassard, L. Labiste, and P. Tisserand, "An high voltage cmos voltage regulator for automotive alternators with programmable functionalities and

- full reverse polarity capability,” in Proc. Design, Automation & Test in Europe Conf. & Exhibition (DATE), 2010, pp. 526–531.
5. G. Pasetti, N. Costantino, F. Tinfena, R. Serventi, P. D’Abramo, S. Saponara, and L. Fanucci, “Characterization of an intelligent power switch for led driving with control of wiring parasitics effects,” in Proc. Design, Automation & Test in Europe Conf. & Exhibition (DATE), 2011, pp. 1–2.
 6. G. Pasetti, S. Saponara, F. Tinfena, R. Serventi, P. D’Abramo and L. Fanucci, "An integrated smart driver for inductive loads with self-monitoring/diagnostic capability", will be presented at International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM), 2012, Sorrento, Italy, JUNE 2012.
 7. E. Biagi, L. Fanucci, G. Pasetti, F. Tinfena and R. Serventi, "A high voltage high power high frequency boost/flyback DC-DC converter for automotive applications", will be presented at International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM), 2012, Sorrento, Italy, JUNE 2012.

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