# Nanomechanical switches based on metal-insulator-metal capacitors from a standard complementary-metal-oxide semiconductor technology

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# Nanomechanical switches based on metal-insulator-metal capacitors from a standard complementary-metal-oxide semiconductor technology

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We report experimental demonstrations of contact-mode nano-electromechanical switches obtained using a capacitor module based on metal-insulator-metal configuration of a standard commercial complementary metal oxide semiconductor technology. The developed 2 terminals Titanium Nitride switches operate at low voltages (~10 V) thanks to its small gap (27 nm), showing an excellent $I_{ON}/I_{OFF}$ ratio ($10^4$) and abrupt behavior (5 mV/decade, one decade of current change is achieved with a 5 mV voltage variation). A switch configuration is also presented where using two electrodes three different contact mode states can be obtained, adding functionalities to mechanical switches configurations. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4882918]

Micro-electromechanical switches have emerged as a technological solution to decrease the static power consumption of scaled down complementary metal oxide semiconductor (CMOS) transistors. When these devices are operating in the OFF state ($V_{GS} < V_{TH}$), the drain to source current, $I_{DS}$, is mainly produced by the diffusion of carriers (drift component is almost negligible). This transport mechanism follows a Boltzmann distribution and therefore the current follows and exponential dependence with gate to source voltage, $I_{DS} \propto e^{V_{GS}-V_{TH}/U_T}$ (being $U_T$ the thermal voltage, $U_T = k_B T/q$).[1] As the transistor dimensions are reduced its electrostatic field is scaled too, reducing the values of $V_{DD}$ and $V_{TH}$. Due to the small values of $V_{TH}$, when the polarization voltage takes values $V_{GS} < V_{TH}$, the $I_{DS}$ current reaches non negligible values, making the static power consumption considerable, even reaching the same value as the active power in small nodes (45 nm).[2] Moreover, its abrupt behavior is limited by its nature, having its sub-threshold slope or sub-threshold swing, $S = (d(\log I_{DS})/dV_G)^{-1} = (k_B T/q)\ln(10)$, a limit of 60 mV at ambient temperature.[3]

Numerous solutions have been proposed in order to reduce the $I_{OFF}$ current based on optics, biological, or plastic devices.[2] However, these solutions cannot take advantage of the superior manufacturing infrastructure that the semiconductor industry can offer. In this direction, alternative transistor designs with steeper sub-threshold swing have been proposed as double-gate tunnel field-effect transistor (FET) or ferroelectric FET.[2] However, they still present nonzero $I_{OFF}$. As an alternative to these limitations, mechanical switches devices are envisioned.[2,3] Additionally, mechanical switches are integrable with CMOS as their fabrication process is based on surface micromachining processes. The use of mechanical element for computing is not a novel idea: they have been used from the abacus to complex mechanical devices used in the second world war to codex information.[4] Nowadays, thanks to the progress on the semiconductor industry field, elements with small dimensions can be defined, making possible to reach high integration level and low operating voltages close to the MOS transistors voltage biasing.[3,5]

Micro/Nano-electromechanical systems (M/NEMS) switches are composed by a mobile structure that is deflected using electrostatic forces until it reaches contact with an electrode, forming a path for the current to flow and changing the state of the device. So we have two different states: no contact (OFF state) or contact (ON state). In the OFF state, the current is limited to vacuum tunneling and Brownian motion displacement currents that appear in the physical gap that separates the mobile structure and the electrode. These currents have low values, reducing the problem of passive power consumption that CMOS transistors present as they are scaled to the submicron regime.

In order to deflect the active element until it comes in contact with the opposing electrode, a voltage difference between them is applied. As a consequence, an attractive electrostatic force will appear ($F_{ELEC}$). This force has to be big enough to overcome the elastic restoring forces ($F_{ELAS}$) due to the structure bending. This is achieved at a voltage, pull-in voltage ($V_{pull-in}$), in which a non-equilibrium point is reached and the structure collapses. At this point, an abrupt current between the two terminals will appear due to its voltage difference. Its value will be fixed by the contact resistance ($R_{CO}$). Once the structure is collapsed, adhesive contact forces will emerge (Van der Waals forces $F_{VDW}$, mainly). While the structure is stuck $F_{VDW} + F_{ELEC} > F_{ELAS}$. In order to release the structure, the voltage difference is reduced until a voltage is reached (pull-out voltage, $V_{pull-out}$) in which this condition is not satisfied anymore. At this point, the elastic recovery forces are bigger than the electrostatic and contact adhesive forces reopening the switch, breaking the contact between the conductors and reducing the current to $I_{OFF}$. On the other hand, there are devices whose elastic restoring forces are not bigger enough to overcome the adhesive forces although the electrical voltage bias is fully removed. These devices operate in a non-volatile way in contrast with the previously exposed (volatile devices). In both cases, the I-V response shows hysteresis behavior which makes them suitable for logic or memory applications.

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Due to its abrupt behavior, promising good density capability,[6] and operability in harsh environments, numerous M/NEMS switches devices have been reported in the last decade using top-down and bottom-up approaches.[5] The main advantage of bottom-up devices is their intrinsic small dimensions that allow them to reach low operating voltages and high performance but an expense of difficult, non reproducible fabrication processes and non compatible with CMOS technologies. It is at this point where top-down devices have its strength as they are defined using lithography steps, commonly used in the semiconductors industry. Using this approach, numerous solutions have appeared[3,7–9] showing good reliability ($10^9$ cycles), abrupt behavior (0.1 mV/decade), and high $I_{ON}/I_{OFF}$ ratio ($10^{11}$).[8] Although much progress has been made in the performance offered by top-down mechanical switches, it has been obtained at an expense of large dimensions designs. As the dimensions are reduced, the reliability is lower ($10^5$ cycles[10]) as the elastic restoring forces are weaker in order to overcome the contact forces and smaller contact area are defined (higher density currents need to be supported). Furthermore, small dimensions are needed to get low operating values (0.4 V pull-in voltages have been obtained defining 4 nm gap[11]) and these are more difficult to reach as the gaps are fixed by lithography steps and the fabrication of thin layers entails more complex fabrication process. In order to reduce the snap-in values without reducing the gap, numerous switches configurations have appeared that try to maximize the coupling area in order to decrease the operating voltages: U-shaped,[12] curved shape,[9] seesaw,[7] or 3D-torsionals.[13] All these configurations require a complex dedicated process.

This work presents a simple fabrication process based on a standard CMOS technology (AMS 0.35 $\mu$m) that allows obtaining low pull-in voltage without any additional technological complex process. It is important to highlight that the NEMS switches are monolithically integrated with CMOS, taking advantages of its robust fabrication process and allowing its integration with additional circuitry without any additional effort. A two terminal (2-T) switch based on a torsional configuration will also be presented, where three different states are available, adding functionalities to 2-T switches.

Previously, MEMS switches were fabricated using the back-end metal layers of AMS 0.35 $\mu$m CMOS technology.[14] However, its large gaps translated into high pull-in voltages. With the aim of getting small gaps the Metal-Insulator-Metal (MIM) module, available in analog CMOS technologies, has been used to define the mechanical structures. A schematic view of the MIM module is presented in Figure 1. It is formed by a metal insulator metal sandwich whose insulator layer (based on nitride) presents a small thickness (27 nm). Thanks to this feature big capacitances can be fabricated using small areas and make it attractive to define out of plane mechanical switches. Once we have defined a structure using the METCAP layer, it will be released using a wet etching process based on a buffered HF solution previously reported.[15] Metal 2 layer will act as the bottom excitation electrode and METCAP (Titanium Nitride with a Young Modulus, E = 600 GPa (Ref. 10)) will be the mobile structure. The main problem in order to use this

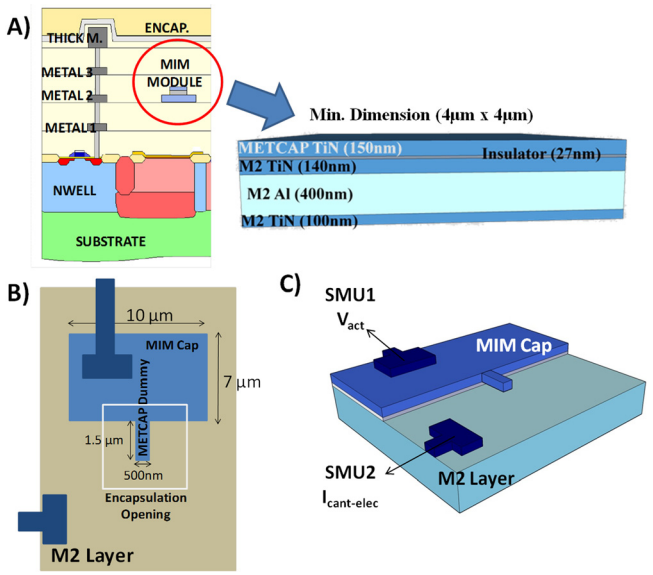


FIG. 1. (a) MIM module schematic view. (b) METCAP dummy element for implement NEMS cantilever. It can be observed how to release just the cantilever an opening in the encapsulation is defined above it (white square), preventing the releasing of the anchor. (c) Electrical characterization SET-UP of the cantilever switch. SMU1&2 are the two Source-Measurement-Units corresponding to B1500A semiconductor analyzer used for the electrical characterization.

approach is that MIM module design rules fix the minimum dimensions to 4 $\mu$m × 4 $\mu$m area. In order to make the releasing process easier, dummies structures with a minimum dimension of 500 nm (Figure 1(b)) will be used as the mechanical structure. A METCAP dummy structure is placed besides a regular MIM capacitance that will act as the anchor of the cantilever movable switch, Figure 1(c).

Using this approach two terminals (2-T) out of plane switches have been developed, using two different structures: cantilever beams (Figure 2(a)) and semi-paddle structures (Figure 2(b)). It can be seen in Figure 2(c), how the 27 nm gap has been obtained without any complex fabrication process, just taking advantage of the high performance that commercial CMOS technologies offer.

The semi-paddle structure has been designed in order to have three different states. The first one is the equilibrium position (state A in Figure 2(b)) when no voltage is applied and an air gap separates the structure and the electrode. In the second state (state B in Figure 2(b)), the tip of the switch makes contact as a consequence of the torsional movement produced in the paddle anchors. In the third state (state C in Figure 2(b)), the snap of the whole paddle structure is produced. In order to have these three states, it is important to have special careful on the paddle anchors design (in our particular case simple beams with $l_a$, $w_a$, and $t_a$ dimensions). See supplementary material[20] for a detailed design process in order to have three state switches.

Once the chips were post-processed to release the structures, we carefully characterized the devices and measure the two-terminal switching behavior using a semiconductor Devices Analyzer (Agilent B1500A).

Cantilever beams with different lengths (2.5 $\mu$m, 2.0 $\mu$m, and 1.5 $\mu$m) and the same width, 580 nm, were characterized,

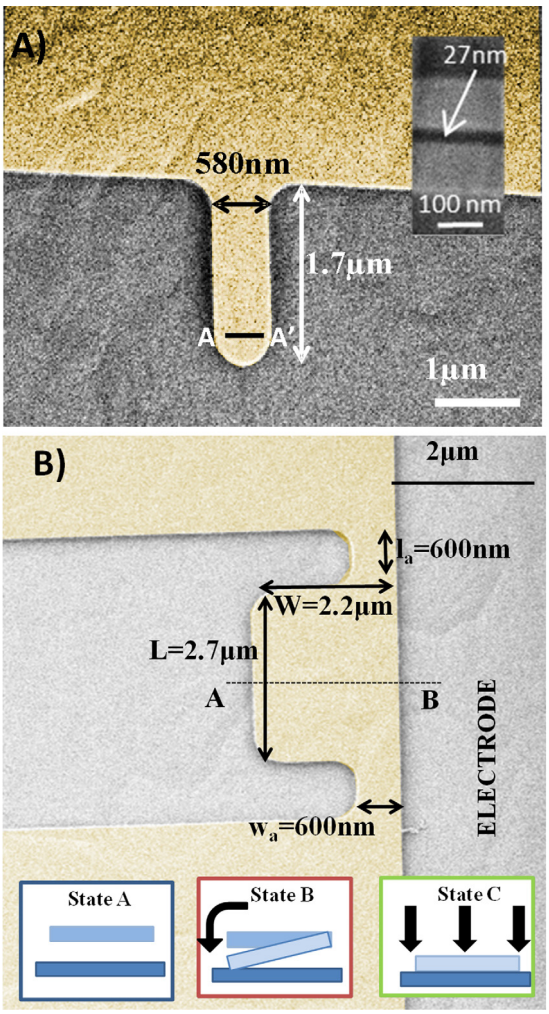


FIG. 2. (a) SEM Image of a cantilever switch (METCAP layer has been colored for easy recognition). (Nominal thickness, t = 150 nm, designed length l = 2 $\mu$m, and width w = 500 nm.) In the inset, a zoom in of A-A' FIB cross sections shown to show he 27 nm actuation gap between METCAP cantilever and MET2 electrode. (b) SEM image of a semi-paddle switch and a schematic of its operation modes at the cross section A-B defined in the SEM image. State A: without actuation voltage, state B: pull-in due to the torsional movement of the paddle anchors, state C: pull-in due to the flexural movement of the paddle anchors.

presenting the responses showed in Figure 3. The pull-in events take places at 11.6 V, 16.7 V, and 19 V (respectively) and the pull-out at 2 V, 4 V, and 18 V, approximately. Pull-in voltages increase as the beam length is reduced since the beam spring constant is higher. Thanks to this spring constant increase, higher pull-out values are obtained, since the elastic restoring forces are bigger and attractive forces like Van der Waals forces can be more easily overcame (note that in the 2.5 $\mu$m length beam the pull-out is not abrupt, probably because the elastic restoring forces are not strong enough to completely restore the beam to its original position). Its hysteresis behavior makes these devices suitable for memory applications.

In order to improve the reliability of the MIM switch an atomic layer deposition (ALD) was done[10] depositing 8 nm $Al_2O_3$ oxide. Figure 4 shows its electrical characterization showing a lower pull-in voltage (compared with the same device without ALD). Moreover, a good $I_{ON}/I_{OFF}$ ratio ($10^4$)

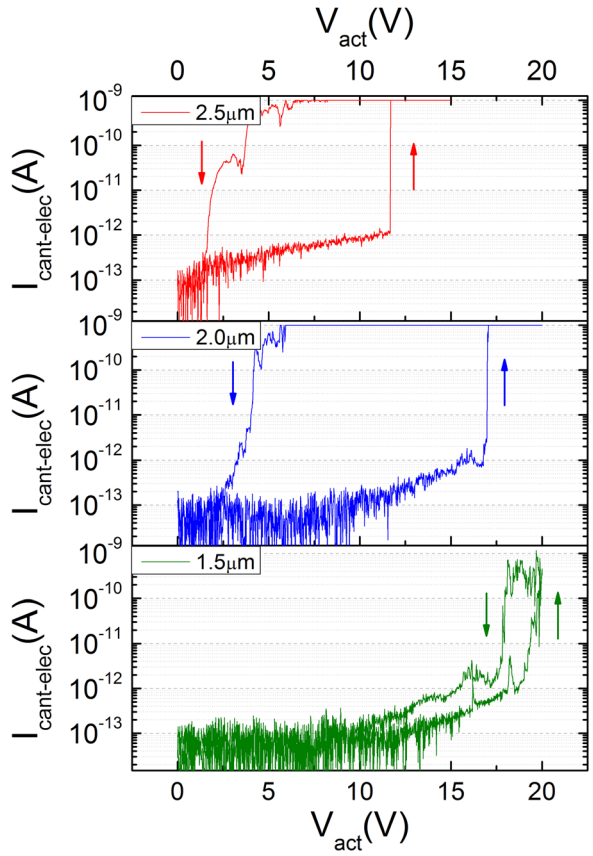


FIG. 3. Electrical measurement for different cantilever lengths (width = 580 nm, thickness 120 nm).

was obtained, where the $I_{OFF}$ value is given by the experimental set-up and $I_{ON}$ value is fixed by the semiconductor analyzer compliance and an additional resistance of 500 MΩ to avoid abrupt current peaks. Abrupt behavior (at least 5 mV/decade) during switch-on transition can be observed (see Figure 4, inset). It was found that the reliability was improved, making the switch works for ten cycles, remaining then stuck (Figure 4). It can also be appreciated, how the pull-in voltages are reduced as the number of operating cycles is increased. This effect could be explained by an accumulation of charges in the dielectric deposited by ALD.[16,17] Charges can be stored in these layers, adding an electrostatic force that could reduce the initial gap, as it was

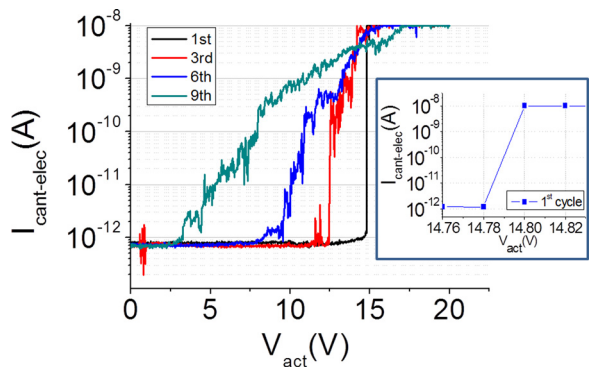


FIG. 4. Electrical measurement after ALD (1.5 $\mu$m length and 580 nm width). (Just the sweep-up cycles are represented.)

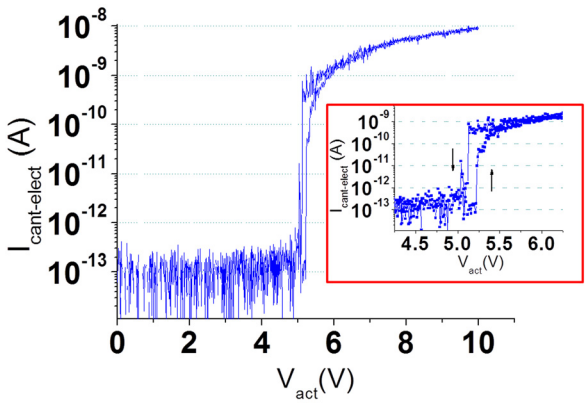


FIG. 5. Cantilever switch (1.5 $\mu$m length and 580 nm width) electrical characterization after ALD process (8 nm $AL_2O_3$ oxide). The variation in the pull-in and pull-out voltages respect other measured designs is attributed to charge accumulation on the dielectric.

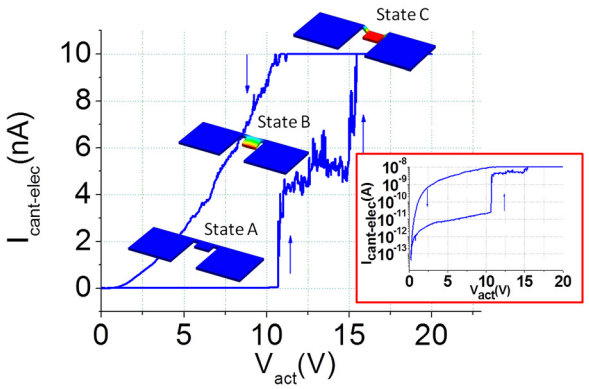


FIG. 6. Semi-paddle switch electrical characterization where two different pull-in events can be observed. For each state (defined in Figure 2), finite element simulation is shown.

observed in some devices (Figure 5) that presented lower pull-in values (5 V was the minimum value observed).

In Table I, a summary of the main attributes of the designed MIM switches is presented and compared with the state of the art of minimum dimensions top down switches. It can be observed how using a fabrication process based on a commercial CMOS technology similar features have been obtained in terms of abrupt behavior (5 mV/decade), $I_{ON}/I_{OFF}$ ratio ($10^4$), and low pull-in voltages (5 V) making our approach comparable to the state of the art switches.

Semi-Paddle switches electrical characterization with the two different pull-in events is presented in Figure 6. The first pull-in corresponding to the torsional mode occurs at 10.7 V, while the flexural pull-in takes place at 15 V. Both experimental voltages slightly differ from the theoretical values found (8.66 V the first snap-in event and the second at 17.58 V; see supplementary material[20] for the calculation details).

The semi-paddle 2-T switch presents three different states, making this device appropriate for three-state logic in digital circuits as registers, bus drivers, and flip-flops. It shows a high impedance state when it is not making contact with the electrode and two different states (torsional or flexural) depending on the voltage applied between the structure and driver. Therefore, using this switch the number of bits could be reduced in memory and logic applications, as 3 different states are obtained just applying one voltage difference (actuation voltage), in contrast to common memories where two different bits (voltages) are necessary in order to obtain 3 different states (00, 01, 10).

In summary, we have developed mechanical switches based on MIM module in a standard commercial CMOS technology. The small dimensions of the structures (length 1.5 $\mu$m, 580 nm width, and 27 nm gap) ensure a high integration density and consequently a cost reduction. Although lower pull-in voltages have been reported using top-down approaches (Table I) they are not totally CMOS fabricated as our approach, which requires only one additional post-processing step to release the structures. Moreover, the switches present abrupt behavior and a good $I_{ON}/I_{OFF}$ ratio. Further efforts are need in order to improve the reliability. In addition, we have presented a 2-terminal 3 states switch with promising applications in memory and logic applications.

TABLE I. Top down switches state of the art (special attention has been taken to those works that try to minimize switches area and co-integrate them with CMOS).

| Material and dimensions (length (l) and gap (s)) | Vpull-in $I_{ON}/I_{OFF}$; mV/decade | CMOS |
|---|---|---|
| Silicon carbide[18] | 1–8 V | |
| l = 6–20 $\mu$m, s = 27–90 nm | $10^3$; … | NO |
| TiW/W[11] | 0.4 V | Suited for NEM-CMOS |
| l = 1.5 $\mu$m, s = 4 nm | $10^6$; 10 | |
| Pt[19] | 4.3 V | NEMS on CMOS |
| l = 3.5 $\mu$m, s = 100 nm | $10^4$; 0.8 | |
| TiN[10] | 14 V | CMOS compatible |
| l = 0.3 $\mu$m, s = 15 nm | $10^5$; 3 | |
| TiN [this work] | 5 V | Monolithically integrated |
| l = 2.5–1.5 $\mu$m, s = 27 nm | $10^4$; 5 | |

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[20]See supplementary material http://dx.doi.org/10.1063/1.4882918 for a detailed design process in order to have three state switches and for the calculation details.