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Control of Static Converters for Grid-Side and Machine-Side Applications

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Dedicated to my family

Dedicata alla mia famiglia

Abstract

The research activities summarized in this Ph.D. thesis are mainly referred to the power electronics field, with some extensions related to electric machines and electrical drives. The first chapter focuses on the analysis and control of an unconventional static converter able to extend a common 1-phase mains feeder into a standard 3-phase power supply featuring either a 3-wires or a 4-wires output, the latter including neutral. Such converter exhibits a complete power reversibility and permits to achieve a good power quality level both at the input and the output side. It is proposed as an attractive alternative to conventional solutions possibly available in the market, such as converters for drives supplied by 1-phase mains yet using 3-phase motors, thanks to the following benefits: greater simplicity, lower cost, inherent active-filter-like operation at supply side, low harmonic distortion at load side. Such converter might be then successfully applied in any application requiring a 3-phase standard supply when a 1-phase mains feeder is available. A theoretical analysis of the converter is presented as well as a semi-ideal simulation model implemented referring to different control strategies. Several simulation results are finally reported and commented, confirming the effectiveness of the proposed solution. The second chapter focuses on the real-time control of 3-phase single-dc-bus shunt active filters employed for the parallel compensation of harmonics, reactive components and unbalancing in the currents drawn by a power supply when generic 3-phase non-linear, non-resistive and unbalanced loads are connected. In particular, the specific issues related to applications featuring a high fundamental frequency, such as in aerospace ambit, were addressed, investigating an innovative improved dead beat digital control algorithm. Such solution was proposed and get ready mainly aiming to achieve a rather high bandwidth of the current control loop and a good reference tracking even when the number of commutations per fundamental period that can be used is rather low. In order to probe the performances of the proposed control strategy, a simulation model was first developed and a prototype system was finally get ready. The results obtained from several virtual and experimental tests are reported and commented referring both to standard industrial and much more demanding aerospace oper-

ative conditions, thus proving the validity of the proposed solution. The third chapter focuses on the real-time control of 3-phase multilevel shunt active filters employing a multilevel cascaded H-bridges structure, again mainly referring to applications featuring a high fundamental frequency such as in aerospace ambit. In fact, such power structures may permit to improve the equivalent converter performances while keeping at relatively low values the actual switching frequency of the power devices. In particular, the combined application of an innovative modulation technique and of a dead-beat strategy analogous to the one described in the previous chapter was investigated. A theoretical analysis of the proposed control strategy is reported, as well as several experimental results obtained from a prototype system purposely get ready and tested at both industrial and aerospace frequency, highlighting the potential of the proposed solution especially for the latter applications. The experimental activities related to chapters 2 and 3 were developed during a study period spent at the University of Nottingham, UK. The fourth chapter deals with the modeling and control of an innovative rotary-linear brushless machine. In particular, after its ideal analytical modeling and operation principle, its basic control strategy inspired to sinusoidal brushless machines is presented, reporting some simulation results. A more detailed simulation model based on the equivalent magnetic circuit approach is then presented, permitting to approximately take into account several secondary aspects neglected by the simpler basic sinusoidal model while remaining not much computationally intensive as a finite element model would be. Simulation results obtained by such model are reported and commented, highlighting its potential usefulness for both preliminary machine design purposes and for analyzing the operation of a complete drive. Finally, the fifth chapter presents the application of the same intermediate-level modeling approach described in chapter 4 to a consequent-pole brushless machine featuring an unconventional magnet-pole angular width ratio. After some considerations on the specific arrangement examined, which was conceived to achieve a better exploitation of the active materials, a simulation model of the machine is presented and numerical results are reported and commented, highlighting the usefulness of the proposed intermediate-level modeling approach.

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Introduction

Power electronics deals with the study, modeling, analysis and design of static converters, i.e. apparatuses able to regulate electric quantities such as voltages and currents without employing moving parts and ideally not requiring any energy loss to implement their operation principle. In fact, a static converter basically consists in an electric circuit that may consist of 2 classes of components: reactive elements, i.e. inductors and capacitors, and switching cells, i.e devices whose operation ideally resembles a switch that may assume only the open and closed states according to a command signal and/or to the operative conditions. Such discipline combines then several engineering areas related to electrical circuits, electronics, applied informatics, control systems and electrical machines when drive applications are considered. Actually, since about 4 decades power electronics may be considered one of the most dynamic fields in electrical engineering, permitting to drastically extend the opportunities to control electric apparatuses and grid quantities. In fact, although the first implementations of static conversion apparatuses based on large thermionic valves date back a few decades earlier, only the development of more and more effective semiconductor power devices led to the actual spreading of power electronics as a revolutionary means to control large electric voltages and currents with levels of efficiency and flexibility otherwise impossible. From the early diode, whose name directly comes from the valves era, the devices based on bipolar technology, i.e. BJT and SCR, were first introduced and then further developed leading to Triac and GTO. Successively, the metal-oxide technology was introduced leading to the development of MOSFET and then of the hybrid IGBT device, which presently represents the most successful and diffused power semiconductor component available on the market. Further improvements, at least under specific points of view, are expected by other innovative devices still under development, such as SIT and MCT. The availability of new devices, approaching more and more effectively the "controllable switc" behaviour constituting the basic element of static converters over a more and more wide size range, permitted to gradually increase the complexity, capability and performances of static converters while even reducing their costs thanks to the improvement of manufacturing pro-

cesses. In fact, novel converter topologies and advanced modulation techniques were proposed, as well as sophisticated control strategies permitting to achieve better and better performances in both motor drives and grid applications. As example, for machines control vector or field-oriented control, direct torque and flux control (DTC), sliding mode or variable structure control, optimal and sensorless control technioques were developed. Consequently, power electronics permitted to further extend the application potential of electrical drives and devices, ultimately playing a central role in several industrial, civil and transportation applications ranging from low-power personal and domestic devices to high-power processes and propulsion systems. As example, present applications involving static converters include dc and ac regulated power supplies, uninterruptible power supply (UPS) systems, static VAR compensators as SVC and STATCOM, active filters for compensation of harmonics, reactive power and phase unbalancing, high voltage converters for HVDC systems, interface converters for photovoltaic and fuel cell generation systems, motor drives employing conventional and innovative machines.

In this scenario, the research activities summarized in this Ph.D. thesis mainly focus on the control of static converters for different grid-side applications, i.e. an active 1-phase to 3-phase mains extender, a 3-phase standard active filter and a multilevel 3-phase active filter featuring a cascaded structure. Finally, some modeling aspects of electric machines useful for the analysis of electrical drives, particularly referring to the design of the control strategy, are addressed.

In the first chapter, the control of an unconventional converter able to effectively convert a standard 1-phase feeder into a standard 3-phase supply is addressed. The usefulness of such mains extender mainly relates to the fact that, for practical reasons, most of utilities offer only a 1-phase standard feeder for relatively low power supply levels, despite the grid features historically a 3-phase structure and 3-phase loads could actually exhibit better characteristics. Such solution may be even applied to larger loads and medium voltage feeders in rural areas and developing countries. In fact, although nowadays the use of d.c. distribution systems would be quite feasible just thanks to static converters and is already applied successfully in small scale industrial plants, for what concerns the utility grid such transition may be only envisaged at the moment, due to the high related costs. The proposed converter features a few interesting characteristics: greater structural simplicity vs. potentially available solutions, such as conversion systems for drives using 3-phase motors, thanks to the use of the available mains voltage as one of the outputs; low distortion of generated output voltages; high power quality at input side, due to an inherent active-filter-like behavior;

full reversibility. The 3-wires and 4-wires variants of the proposed converter are presented and analyzed under a theoretical point of view, also describing suited simulation models. Different possible control strategies are then presented, reporting and commenting simulation results confirming the good performances achieved also under unfavorable conditions.

The second chapter investigates the application of an improved dead-beat digital control strategy to a standard 3-phase shunt active filter featuring the usual single-dc-bus structure, typically employed to compensate harmonics, reactive components and unbalancing in the currents drawn by non-linear, non-resistive, non-balanced loads. The proposed control strategy is described in detail particularly referring to the possible application to aircraft power systems, which turns out particularly demanding for both the power and control sections due to the high value of reference frequency (400 Hz). Such strategy employs also a simple method for predicting the values of the relevant variables, as necessary to compensate the inherent delay due to the elaboration time required by the digital control system. A simulation model of the converter is also presented, as well as a prototype purposely realized for testing at the University of Nottingham during a study period spent there. Significant simulation and experimental results are then reported and commented mainly referring to a typical nonlinear load constituted by a 3-phase-diodes-bridge-fed apparatus, highlighting the validity of the proposed solution.

In the third chapter, the same digital control strategy previously illustrated is applied to a 3-phase multilevel active filter featuring a Y-connected cascaded structure employing 2 H-bridge units with isolated d.c. capacitors banks per each inverter phase. The use of such more complicated structure was also firstly motivated by the aerospace application target, since a multilevel arrangement may permit to increase the equivalent switching frequency of the converter while keeping relatively low the actual switching frequency of each power device. In fact, this is a key aspect to achieve a a sufficiently high bandwidth of the current control loops despite the high fundamental frequency, thus still permitting to compensate at least the most significant low-order harmonics of load currents. After a short overview of multi-level inverters, the considered structure is examined in detail, analyzing the possible alternatives for the definition of the modulation technique and highlighting the inherent limits in the capability to compensate unbalanced loads, which derive from the impossibility to transfer power between different phases. A simulation model is then presented, as well as a prototype of the system purposely get ready at the University of Nottingham. Significant simulation and experimental results are finally reported and discussed mainly referring again to a

nonlinear load constituted by a 3-phase-diodes-bridge-fed apparatus, highlighting the effectiveness of the proposed solution also at the high fundamental frequency typical of aerospace applications.

In the fourth chapter, an innovative rotary-linear brushless machine is first described, highlighting its potential applicative interest mainly related to the possible manufacturing using standard parts commonly available on the market. The ideal control strategy of the machine derived from a model inspired to the classical sinusoidal approximation is then presented, reporting and commenting some related simulation results. A more detailed analytical mid-complexity model of the machine based on the equivalent magnetic circuit approach is then presented, aimed to permit a first estimation of the effects of the main non ideal aspects neglected by the sinusoidal model, such as actual winding distribution, slots openings etc. Such type of model turns out particularly useful to provide a better insight both of the machine characteristics, during its preliminary design phase, and of its operation in a complete drive system, as required in the context of system-level simulations typically used to get ready the related control system. In fact, the much higher computational burden related to an actually detailed FEM electromagnetic analysis makes this approach usually unwise for such purposes, even when all of the existing symmetries are exploited to reduce the size of the actually modeled region. Simulation results obtained by the implementation of the mid-level model introduced are reported and commented, highlighting the effects of different variants in the machine design.

Finally, chapter five deals with consequent pole brushless machines featuring an unconventional non-even pole-magnet width ratio, showing that such arrangement may permit to improve the exploitation of magnetic materials and thus ultimately to achieve higher specific performances. A mid-complexity model of this machine based on the equivalent magnetic circuit approach is then presented, reporting and commenting several simulation results highlighting its potential to provide a fairly accurate estimation of both the main and the most important secondary phenomena. This confirms that the proposed approach may represent a wise compromise between accuracy and computational burden for the modeling of electric machines aimed to preliminary design and drive-level simulation analysis.

Chapter 1

Control of a 1-Phase to 3-Phase Mains Supply Extender

1.1 Introduction

When available, in technical terms a standard 3-phase a.c. supply is preferable with respect to a 1-phase feeder. In fact, at steady state a 3-phase feeder may provide an instantaneous power that is actually constant rather than pulsating. This indirectly turns into better performances of load apparatuses. For example, 3-phase induction motors, which are still widely used in direct supply mode for low-cost grossly-constant speed applications, result more compact and efficient than 1-phase motors, also providing less torque ripple. Analogously, 3-phase diode rectifiers may provide a lower output ripple, with related benefits for the connected loads. Moreover, the size of reactive elements used as energy buffers inside converters may be reduced. Nevertheless, due to historical, economical and practical reasons a standard 3-phase supply is usually not available from utilities for power levels below 10 kVA or even more. On the other hand, the power quality issues are gaining more and more importance, especially in terms of harmonic current injection and reactive power drawing from the mains: in fact, such phenomena determine underutilization of distribution lines and voltage disturbances across the whole grid. Consequently, more and more strict power quality limits are enforced by means of penalties, thus increasing the request of active filters and advanced grid interfaces. Therefore, an interface converter able to provide a standard 3-phase supply from an available standard 1-phase feeder may result interesting under an applicative point of view, especially when it is able to provide an adequate power quality level at both input and output sides and to feature a reasonably simple and effective structure permitting to limit its costs. Power flow reversibility would also represent a plus, permitting to manage conditions such as

regenerative braking from drives etc.

After a brief overview of the general purpose and specific solutions available in the literature for such type of application, highlighting that the considered niche problem was not much investigated, a purposely conceived converter is presented. The power structure and main features of such converter in comparison to the available solutions are commented, highlighting its reduced complexity, its potential capability to provide a good power quality at both input and output sides and its full reversibility. Two different variants of the converter are described and compared. The main theoretical and simulation results achieved are also presented, as well as the control strategies examined including current and voltage control using hysteresis controllers, PI controllers with PWM modulator etc. The opportunity to also effectively adopt a vector control approach, although not obvious at a first view due to the unusual structure of the converter, is then highlighted and examined, illustrating the first application considered. Significant results coming from a simulation model purposely developed, concerning the steady-state and dynamic performances of the proposed control methods, are finally presented and commented, highlighting the good results achieved in most cases and the issues singled out.

1.2 Short Overview of the available solutions

1.2.1 General purpose converters

Several well established solutions are available for variable frequency electric drives using 3-phase motors and supplied by 1-phase mains. Such solutions, providing a fully adjustable 3-phase output, would be obviously useable also for the considered less-demanding application scenario. In most of such solutions, a VSI inverter is employed as output stage supplied by an internal d.c. bus supported by capacitors, whereas the most common configuration for the input stage includes a simple diodes rectifier eventually complemented by a passive line filter to attenuate the inherent power quality issues of such topology. Improved variants of the input stage are equipped with either a mono-directional PFC-like module or an inverter-based active front-end, aiming to improve the line-side power quality and to eventually permit power flow reversibility. The opportunity to reduce the number of switching components is also examined in a few papers. For example in fig. 1.1 [1, 2, 3], a dual-spit d.c. bus is proposed and investigated, whose center tap is connected to both one of the feeder terminals and one of the load terminals. Two VSI inverter legs are then used to provide the further 2 terminals required to complete a 3

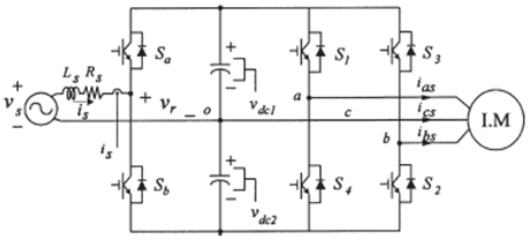


Figure 1.1: 3-legs 1- to 3-phase converter for induction drives

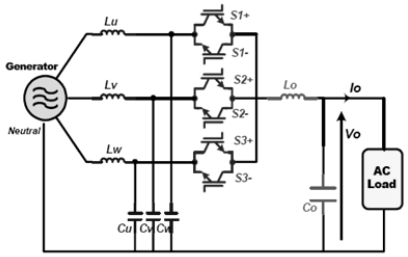


Figure 1.2: Matrix converter for 3- to 1-phase conversion

wires output by generating 2 line-to-line load voltages, whereas a third leg is used as half-bridge inverter to provide an active bidirectional mains interface through a line inductor. Different configurations were also proposed for partly analogous applications. For example, in [4] the use of a cycloconverter was considered; anyway, it determines relevant issues under the power quality point of view at both input and output sides. In [5] the use of matrix converters was investigated for 3-phase to 1-phase power conversion in railway applications (fig. 1.2), which could be indeed reversed aiming to the considered problem. Anyway, despite the potential benefits coming from the elimination of d.c. bus and related capacitors, matrix converters still represent a relatively expensive and not consolidated solution.

1.2.2 Purposely designed converter

Although potentially applicable also in the considered scenario, the general purpose solutions above described result more complex and expensive than strictly required. In fact, as long as a standard 3-phase supply is required, presumably it may be assumed that the frequency, amplitude and waveform of the voltage available via the 1-phase feeder should be fine, and thus directly useable, as one of either the phase or the line-to-line output voltages. This permits then to minimize the converter complexity by directly forwarding the feeder voltage to the load. For instance, in the basic topology introduced in [6] for low-cost limited induction motor regulation the feeder voltage is used both as a line-to-line output voltage (fig. 1.3) and to supply a dual d.c. capacitors bank via a simple 2-diodes half-wave rectifier and a filtering inductor. Such bus supplies in turn a half-bridge VSI inverter which provides the third terminal of the 3-wires output. Anyway, such topology only permits reverse power flow via the direct connection; moreover, it exhibits an inherent poor behavior in terms of power quality at both input side, due to the rectifier operation, and at output side, due to the lack of any filtering between inverter and load. Four topologies still exploiting the same basic

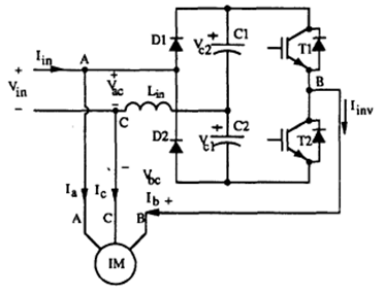


Figure 1.3: 1- to 3-phase converter with split bus and 1 VSI leg

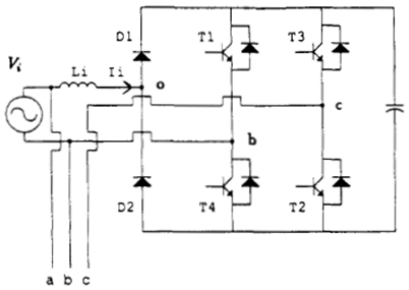


Figure 1.4: 1- to 3-phase converter with diodes and 2 VSI legs

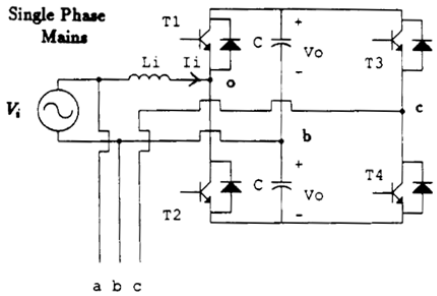


Figure 1.5: 1- to 3-phase converter with split DC bus and 2 VSI legs

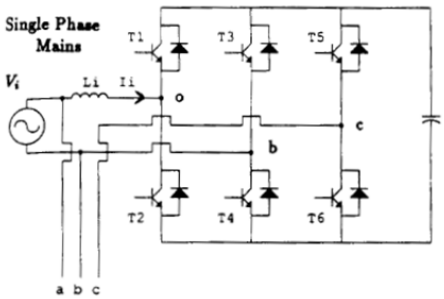


Figure 1.6: 1- to 3-phase converter employing 3 VSI legs

concept are analyzed in [7]. In the first one (fig. 1.4), the input stage is enhanced by including a second VSI inverter leg permitting to use a simpler non-split d.c. capacitors bank bus voltage and to improve the input-side behavior, although at the price of some interference between the control loops of input current and output voltage. In the second analogous variant, a split d.c. bus is again considered and the 2 standard inverter legs are replaced with corresponding NPC legs. In a third variant, a split d.c. bus is still used whereas the diode rectifier leg in [8] is replaced by an inverter leg (fig. 1.5), thus permitting both to separately control the input current and output voltage and to achieve full power flow reversibility. In a fourth variant (fig. 1.6), the diodes rectifier leg in the scheme depicted in fig. 1.4 is replaced with a third VSI inverter leg, thus permitting to employ a standard 3-legs arrangement, to improve the decoupled control of input and output operation and to achieve full power flow reversibility.

1.3 Proposed Converter Variants

Hereafter a pair of topologies tailored to the considered problem are proposed and analyzed, respectively referring to 3-wires (no neutral) and 4-wires (with neutral)

output variants. The first proposed converter variant, whose scheme is depicted in fig. 1.7, may be considered as an improved variant of the basic topology in fig. 1.5: in fact, it also applies the basic concept of using a dual-split d.c. bus supported by capacitors, which is connected to the mains feeder by means of a L-C-L filter and a standard 2-cells leg operating as a VSI half-bridge inverter. The voltage across the above filter capacitor, whose low-frequency components are assumed to strictly resemble the main voltage as the size of the line inductor is supposed to be wisely small, is directly forwarded to the 3-phase load as one of the line-to-line voltages. The second line-to-line voltage required to complete the 3-wires output is generated by a second VSI 2-cells inverter leg via a L-C filter, again with respect to the center tap of the d.c. bus that also constitutes an output terminal. Thanks to the presence of the L-C filters connected at the output of both inverter legs, a fine dynamic control of the current drawn from the mains and of the generated output voltage waveform is possible, thus permitting to provide a better power quality than the simpler structure sketched in fig. 1.5 yet without requiring a larger number of semiconductor components as in fig. 1.1 or in standard configurations. The presence of the line-side inductor permits to further reduce the high-frequency component in the current drawn from the feeder, also preventing excessive current peaks at switch-on and the propagation of eventual impulsive disturbances from the mains to the load. In fig. 1.7 are also shown 2 varistors connected in parallel to the d.c. capacitors aiming to prevent possibly dangerous excessive overvoltage conditions, especially during fast and partly uncontrolled transients such as at startup. The second proposed converter variant, whose scheme is reported in

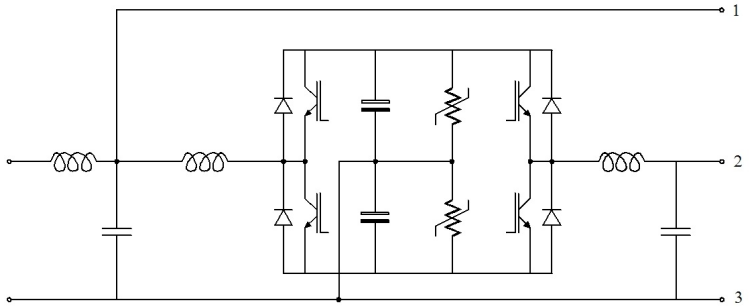


Figure 1.7: Ideal scheme of first converter variant: 2-legs, 3-wires, no neutral

fig. 1.8, may be considered as an extension of the previous one tailored to 4-wires output applications, where the input feeder voltage is considered as adequate to become a phase voltage for the load rather than a line-to-line output voltage. In fact, basically this variant features the same structure as above with the addition of a third 2-cells VSI inverter and related L-C output filter. Therefore, in this case

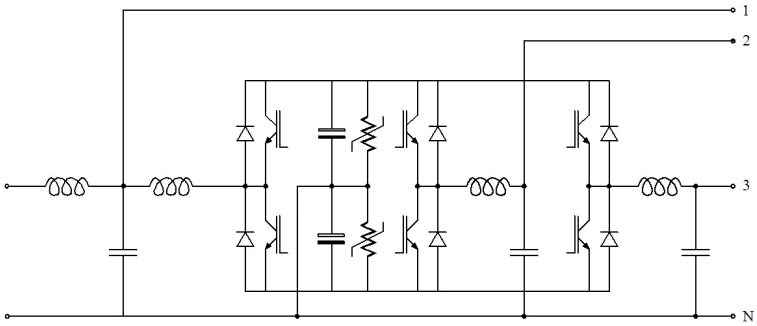


Figure 1.8: Ideal scheme of second converter variant: 3-legs, 4-wires, with neutral

the first inverter leg operates to manage the grid interface, whereas the other 2 legs provide the 2 missing phase voltages required to complete the 4-wires output, whose neutral point is connected to the center tap of the d.c. bus. Actually, in both variants the input stage of the converter operates simultaneously as an active filter in respect to the unconverted load current I_1 and as an active front end with respect to the converter core. On the other hand, the converter topology makes it basically unable to actively adjust the output voltage directly derived from the mains feeder, e.g. to compensate voltage drops, sags or waveform distortion. Anyway, in comparison with fully adjustable converters used for variable speed drives, the proposed topologies permit to save 1 inverter leg over 3 or 4 respectively for the 3-wires or 4-wires output variants, while providing a better output voltage quality thanks to the filtering elements.

1.4 Theoretical Analysis

A theoretical analysis of the proposed converter [9] may be undertaken by considering its equivalent circuital model: as usual, an ideal behavior may be assumed as a first approximation for both the reactive elements and the switching cells composing the inverter legs. Accordingly, the equivalent circuits reported respectively in fig. 1.9, 1.10 may be considered for the first and second variant of the converter. In both circuits, each of the inverter legs is replaced by 3 controlled generators: a voltage generator U_k connected to the related output inductor L_k and a couple of current generators I_{Pk}, I_{Nk} properly connected to the d.c. bus bars. Introducing a tern of switching signals

$$\sigma_k(t) = \pm 1 \qquad k = 1, 2, (3) \tag{1.1}$$

to represent the instantaneous state of each VSI leg by associating the $+1$ value to the positive-side-connection condition and the -1 value to the complementary

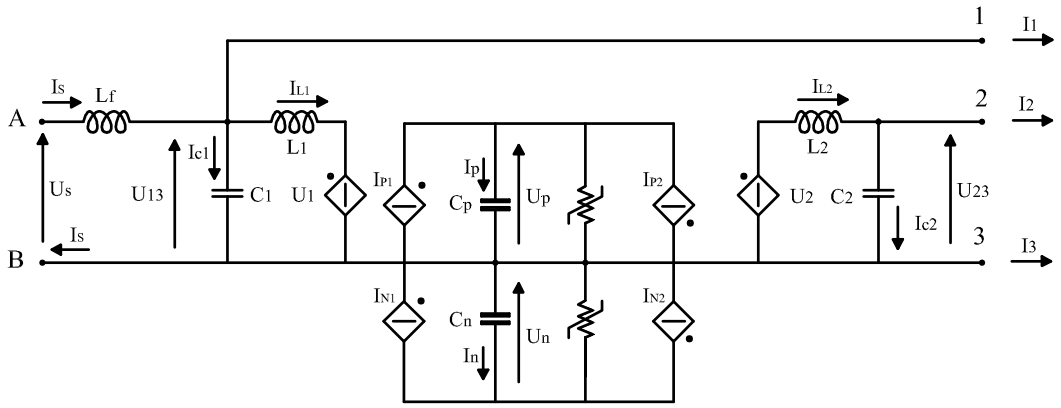


Figure 1.9: Idealized equivalent circuit for the first proposed variant

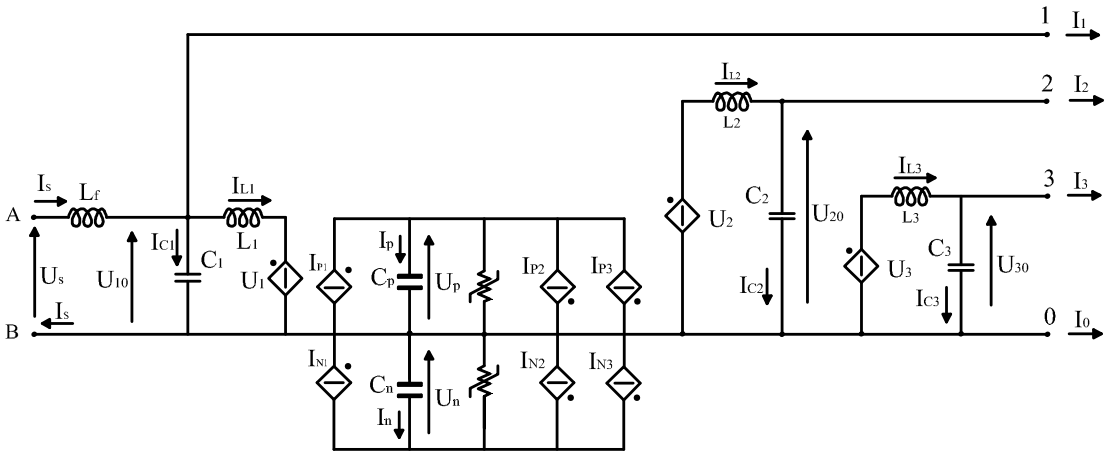


Figure 1.10: Idealized equivalent circuit for the second proposed variant

state, the associated output voltages result expressed as

$$u_k(t) = \sigma_k(t) \cdot [u_P(t) + u_N(t)]/2 + [u_P(t) - u_N(t)]/2 \tag{1.2}$$

while the currents provided by the related generators are

$$i_{Pk}(t) = i_{Lk}(t) \cdot [\sigma_k(t) + 1]/2 \tag{1.3}$$

$$i_{Nk}(t) = i_{Lk}(t) \cdot [\sigma_k(t) - 1]/2 \tag{1.4}$$

Therefore, neglecting the currents flowing in the two varistors connected in parallel to the d.c. capacitors, the current flowing in the positive and negative d.c. bus capacitors C_P, C_N are expressed as

$$i_P(t) = C_P \cdot \frac{d}{dt} v_P(t) = i_{P1}(t) - i_{P2}(t) - i_{P3}(t) \tag{1.5}$$

$$i_N(t) = C_N \cdot \frac{d}{dt} v_N(t) = i_{N1}(t) - i_{N2}(t) - i_{N3}(t) \tag{1.6}$$

where the last term is omitted in the first variant. The currents in the other capacitors are instead given by

$$i_{C1}(t) = C_1 \cdot \frac{d}{dt} v_{1q}(t) = i_S(t) - i_1(t) - i_{L1}(t) \tag{1.7}$$

$$i_{Ck}(t) = C_k \cdot \frac{d}{dt} v_{kq}(t) = i_{Lk}(t) - i_k(t) \tag{1.8}$$

while the voltages across the inductors are given by

$$L_f \frac{d}{dt} i_S(t) = v_S(t) - v_{1q}(t) \tag{1.9}$$

$$L_1 \frac{d}{dt} i_{L1}(t) = v_{1q}(t) - u_1(t) \tag{1.10}$$

$$L_k \frac{d}{dt} i_{Lk}(t) = u_k(t) - u_{kq}(t) \tag{1.11}$$

where in all of the expressions $k = 2$ and $q = 3$ for the first variant, $k = 2, 3$ and $q = 0$ for the second variant. Such models may be used to carry out pseudo-linear dynamic analysis basing on the time-averaged values approach. Anyway, due to the converter purpose its normal operation would be typically referred to quasi-sinusoidal conditions. It is then worth analyzing such steady-state scenario considering the rms phasors representing the fundamental components of a.c. quantities. Assuming as ideal the converter operation, i.e. neglecting the internal losses and the voltage drop on inductor L_f , for a direct sequence of output voltages one has

$$\widetilde{V}_{13} = \widetilde{U}_S = U_S \cdot e^{j0} \qquad \widetilde{U}_{23} = \widetilde{V}_{13} \cdot e^{-j\pi/3} = U_S \cdot e^{-j\pi/3} \tag{1.12}$$

$$\widetilde{I}_1 = I_1 \cdot e^{j(\pi/6-\varphi_1)} \qquad \widetilde{I}_2 = I_2 \cdot e^{j(-\pi/2-\varphi_2)} \qquad \widetilde{I}_3 = I_3 \cdot e^{j(5\pi/6-\varphi_3)} \tag{1.13}$$

in the 3-wires variant, while in the 4-wires variant one has

$$\widetilde{U}_{1N} = \widetilde{U}_S = U_S \cdot e^{j0} \qquad \widetilde{U}_{2N} = U_S \cdot e^{-j2\pi/3} \qquad \widetilde{U}_{3N} = U_S \cdot e^{j2\pi/3} \tag{1.14}$$

$$\widetilde{I}_1 = I_1 \cdot e^{-j\varphi_1} \qquad \widetilde{I}_2 = I_2 \cdot e^{j(-2\pi/3-\varphi_2)} \qquad \widetilde{I}_3 = I_3 \cdot e^{j(2\pi/3-\varphi_3)} \tag{1.15}$$

Assuming that the fundamental component of the current flowing in capacitor C_1 is negligible and that a unity power factor at input side is actually achieved, keeping in mind 1.12 and 1.13 from the active power balance one obtains

$$\widetilde{I}_S = I_S = P/U_S = \Re\left[\widetilde{U}_{13} \cdot \widetilde{I}_1^* + \widetilde{U}_{23} \cdot \widetilde{I}_2^*\right]/U_S = I_1 \cdot \cos(\varphi_1 - \pi/6) + I_2 \cdot \cos(\varphi_2 + \pi/6) \tag{1.16}$$

$$\widetilde{I}_{L1} = \widetilde{I}_S - \widetilde{I}_1 = I_2 \cdot \cos(\varphi_2 + \pi/6) + j \cdot I_1 \cdot \sin(\varphi_1 - \pi/6) \tag{1.17}$$

for the 3-wires variant, whereas for the 4-wires variant one has

$$\widetilde{I}_S = I_S = P/U_S = \Re\left[\widetilde{U}_{1N}\cdot\widetilde{I}_1^* + \widetilde{U}_{2N}\cdot\widetilde{I}_2^* + \widetilde{U}_{3N}\cdot\widetilde{I}_3^*\right]/U_S = \\ I_1\cdot\cos(\varphi_1) + I_2\cdot\cos(\varphi_2) + I_3\cdot\cos(\varphi_3) \quad (1.18)$$

$$\widetilde{I}_{L1} = \widetilde{I}_S - \widetilde{I}_1 = I_2\cdot\cos(\varphi_2) + I_3\cdot\cos(\varphi_3) - j\cdot I_1\cdot\cos(\varphi_1) \quad (1.19)$$

When balanced load currents are considered as in the phasor diagram in fig. 1.11 i.e.

$$I_1 = I_2 = I_3 = I \qquad \varphi_1 = \varphi_2 = \varphi_3 = \varphi \quad (1.20)$$

the amplitude ratio between the input leg current and the load current (also corresponding to the current flowing in the other inverter legs when the currents in the output capacitors may be neglected) may be derived from eq. 1.16 for the 3-wires variant

$$I_{L1}/I = \left|\widetilde{I}_{L1}\right|/I = \sqrt{1-\sqrt{3}\cdot\sin(\varphi)\cdot\cos(\varphi)} \quad (1.21)$$

whereas for the 4-wires variants one obtains from eq. 1.18

$$I_{L1}/I = \left|\widetilde{I}_{L1}\right|/I = \sqrt{1+3\cdot\cos^2(\varphi)} \quad (1.22)$$

Such expressions depend on the load phase as shown in the graph depicted in fig. 1.12, which highlights that in most cases the input leg results more stressed in the 4-wires variant than in the 3-wires one. Actually, in the 4 wires variant the input leg must be oversized up to a factor 2 with respect to the output legs, as required in the worst case represented by resistive load. A uniform sizing of the legs with same rated current as the load would instead suffice for the 3-wires variant to cope with any common ohmic-inductive passive load, since the worst case is represented by

$$\varphi = -\pi/4, 3\pi/4 \quad \rightarrow \quad I_{L1}/I = \sqrt{1+\sqrt{3}/2} = 1.37 \quad (1.23)$$

It is interesting to note that under balanced loads the value of the current flowing in the input leg results invariant with respect to the chosen cyclic sequence of output phases for the 4-wires variant, whereas for the assumed terminals labeling a direct sequence results favorable for the 3-wires variant as far as the load features and inductive-type nature. On the other hand, the active power actually flowing inside the converter results

$$P_C = \Re\left[\widetilde{U}_{13}\cdot\widetilde{I}_{L1}^*\right] = U_S\cdot I_2\cdot\cos(\varphi_2+\pi/6) \quad (1.24)$$

for the 3-wires variant, whereas for the 4-wires variant

$$P_C = \Re\left[\widetilde{U}_{1N} \cdot \widetilde{I}^*_{L1}\right] = U_S \cdot \left[I_2 \cdot \cos\left(\varphi_2\right) + I_3 \cdot \cos\left(\varphi_3\right)\right] \tag{1.25}$$

In case of balanced load, this implies that the ratio of converted power vs. load active power results

$$P_C/P = \cos\left(\varphi + \pi/6\right) / \left[\sqrt{3} \cdot \cos\left(\varphi\right)\right] = \left[1 - \tan\left(\varphi\right)/\sqrt{3}\right]/2 \tag{1.26}$$

for the 3-wires variant, thus depending on the load phase, whereas for the 4-wires variant such ratio results constant:

$$P_C/P = 2/3 \tag{1.27}$$

When considering balanced loads with power factor close to 1 as customary nowadays, the quote of output power actually converted amounts then to about 50% and 67% respectively in 3- and 4-wires variants, resulting appreciably lower than in popular full-conversion topologies: this may permit to save on size and cost of reactive elements while lowering conversion losses, thus also improving efficiency.

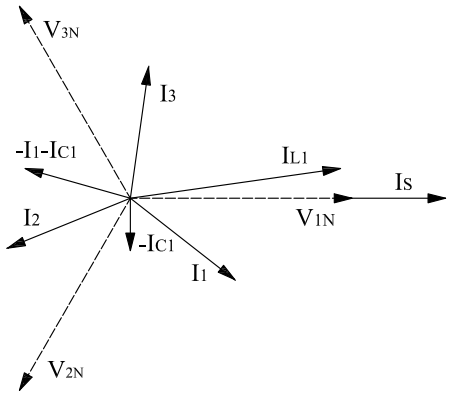


Figure 1.11: Qualitative phasor diagram for steady-state sinusoidal condition

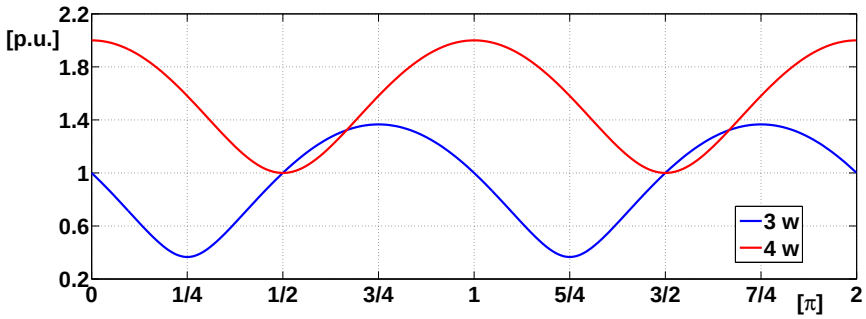


Figure 1.12: Balanced load: input leg current / load current ratio vs. load phase

1.5 Modeling and Simulation of 3-Wires Variant

At first the analysis and the control scheme has been developed for the converter topology without neutral referring to the semi-ideal scheme sketched in fig. 1.13. In particular the first proposed control strategy has been organized as below described. Each inverter leg is equipped with a current control loop to virtually convert the voltage source character of the VSI leg into current source by means of the corresponding filter inductor. Each loop is governed by a 2-levels hysteresis controller that directly provides the driving signal for the related inverter leg. Aiming to prevent possible damaging of the inverter, the above control logic may be temporarily overridden by a safety mode simply tending to reduce the output current of the leg, which operates under the control of an hysteretic relay monitoring the current amplitude. The reference signal for the current loop of the input

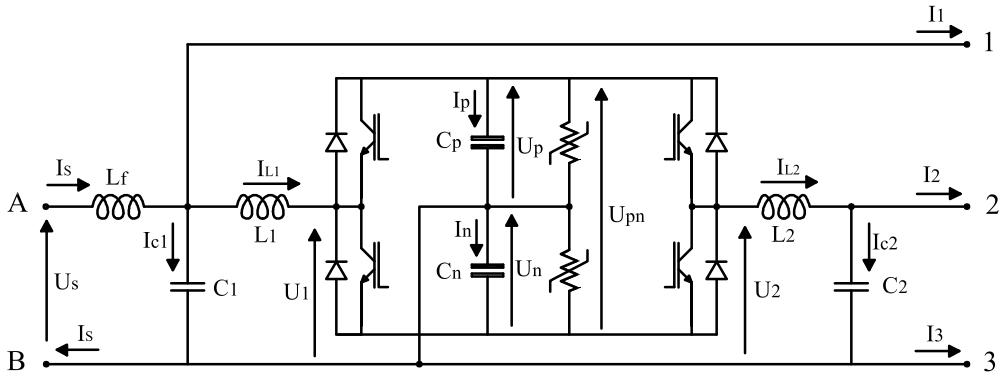


Figure 1.13: Semi-ideal scheme for the first converter variant

leg is obtained as $I_{L1ref} = I_{Sref} - I_1 - I_{C1fund}$ i.e. as the difference between the desired supply current and the sum of the current drawn by the load phase 1 plus the estimated fundamental component of the current drawn by the filter capacitor C_1; the latter is derived in turn by elaborating the fundamental component of the voltage across the capacitor C_1 , which is obtained by filtering the measured value of V_{13}. The desired value for the supply current I_{Sref} is obtained, as in a PFC active rectifier, by multiplying a copy of the fundamental component of the voltage V_{13} by the output of a PI saturated controller that monitors the average value of the total d.c. bus voltage U_{pn} aiming to keep it at about the design value independently on the load. The reference signal for the current loop of the output leg is obtained as $I_{L2ref} = I_2 + I_{C2ref}$ i.e. as the sum of the current drawn by load phase 2 plus the desired current to be drawn from capacitor C_2 which in turn is calculated as the product of a basic signal, obtained the fundamental component of the voltage V_{13} delayed (phase shifted) by $T/6$, i.e. one sixth of period, and multiplied by a factor determined by a controller aimed to ensure that the actual

amplitude of the generated voltage V_{23} equals the amplitude of the fundamental component of V_{13}; such solution permits to pursue the assumed goal to provide the load with a symmetrical voltage tern in terms of fundamental components, independently on the value of the output capacitance C_2 thus making the system insensitive to the possible variation of such parameter. Aiming to ensure a null d.c. component in the generated output voltage, a further controller was also included monitoring the average value of V_{23} and providing a limited unidirectional additional component to the reference value for I_{L2}. The control system above described performed rather well under steady-state conditions and was also able to manage fairly well load transients. Anyway, some aspects of possible improvement were singled out:

- the voltage balance between the 2 sections of the d.c. bus, since the inherent self-adjustment capability operates too slowly to ensure avoiding possibly dangerous large deviations that might emerge under unfavorable conditions, e.g. due to the combined effect of nonlinear or unbalanced loads and of the control loop monitoring the total d.c. bus voltage;

- the power quality level at steady state on both input and output sides especially under non-linear and unbalanced loads;

- the sensitivity to load transients especially for what concerns the output voltages;

- the sensitivity to the variation of the values of the parameters of the reactive elements used, which may differ from the rated values due to manufacturing tolerances, materials ageing etc.

Several different possible variants of the control structure were considered and probed; the variations that resulted most interesting are below described. To cope with the most important weak point previously highlighted, a control loop was included aimed to actively balance the average voltages across the 2 sides of the d.c. bus. Such loop, equipped with a suitable continuous controller, provides an additional unidirectional component that is summed to the main part of the reference current I_{1ref} of the input inverter leg. In particular, it was found out that a linear proportional regulator performs rather well in this task when the load draws a sinusoidal or distorted current, yet with small or negligible average value. It was also considered the replacement of the hysteretic regulators used for current loops with combinations of a continuous regulator and a generalized PWM-like modulator featuring fixed switching frequency and variable carrier vertexes according to the actual current values of the voltages of the 2 sections of the

d.c. bus. In particular, in the control of the input leg 1 this solution performed rather well using a suitable regulator featuring 1 zero and 2 poles, including 1 null. Rather good performances were also obtained by applying the above solution to the inner control loop of the output leg 2. Anyway, a bit better results were obtained by replacing the whole control subsystem of the output leg 2 with a voltage controller which monitors the generated voltage V_{23} versus the reference sinusoid that is still obtained from V_{13} by filtering and phase shifting as previously described. Such controller directly drives a generalized PWM-like modulator again featuring fixed switching frequency and variable carrier vertexes based on the actual voltages of the 2 sections of the d.c. bus. In particular, such solution provided very good performances when a suitable first order lead-leg compensator was used. The design of the controllers above cited was carried out by means of the usual heuristic procedure involving analytical calculations and predictions followed by numerical check, validation and fine tuning using a simulation model described in section 1.5.1. The theoretical analysis was carried out referring to the average-value idealized model, thus neglecting several secondary aspects such as high frequency oscillations due to the inverter, mutual interferences between input and output regulation subsystems etc.

1.5.1 Simulation Modeling

Aiming to investigate more in detail the behavior of the proposed converter under different operating conditions and using different versions of the control strategy above described, a suited semi-ideal model was developed for the converter using the Matlab-Simulink® simulation environment. The model is suitably organized in hierarchical way and takes into account the more relevant phenomena, neglecting secondary aspects such as switching time and voltage drop across switches, saturation and core losses in inductors etc. In particular in fig. 1.14 one of the schemes realized for the control of leg 1 is shown, implementing the sinusoidal input current strategy previously described. The various analog filters used may be noted, as well as the PI saturated regulator of the d.c. bus voltage control loop providing the reference supply current waveform, the derivation of the reference signal for the input current i_{L1} by subtraction of i_1 and estimated i_{C1} , the modified PI controller used for control of i_{L1} and the safety trip logic overriding such control when an active limitation of i_{L1} is necessary. Figures 1.15 and 1.16 show instead the simulation schemes relative to the control subsystems implemented according to the structures previously described for the output leg, reporting the variants including and not including the inner current loop.

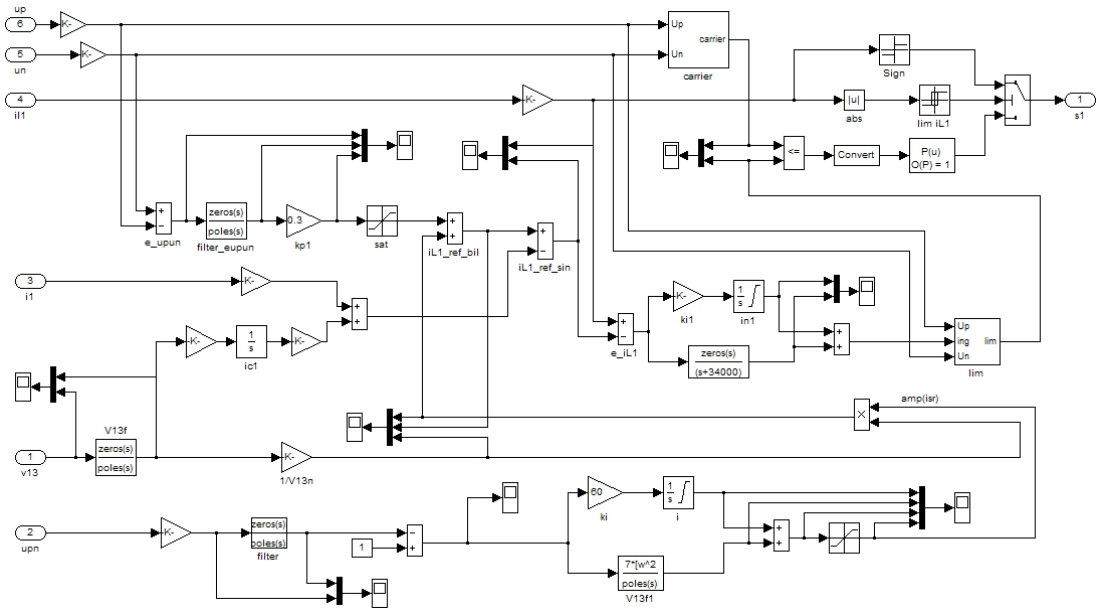


Figure 1.14: Implemented scheme for input leg control subsystem

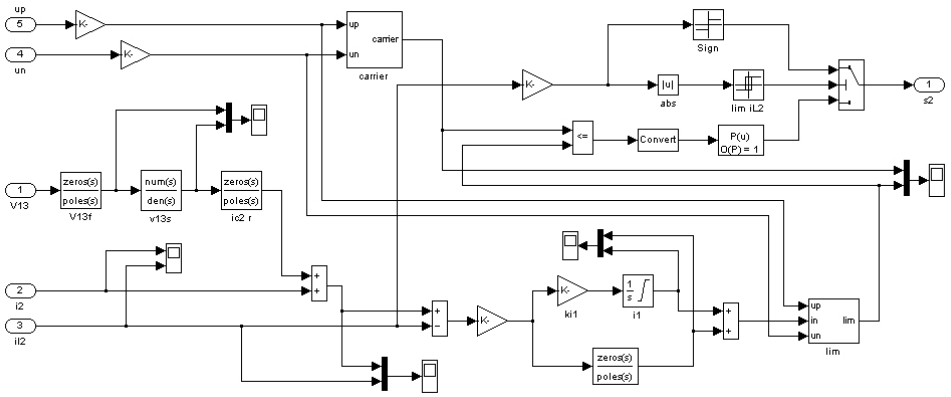


Figure 1.15: Implemented scheme for output leg control with current loop

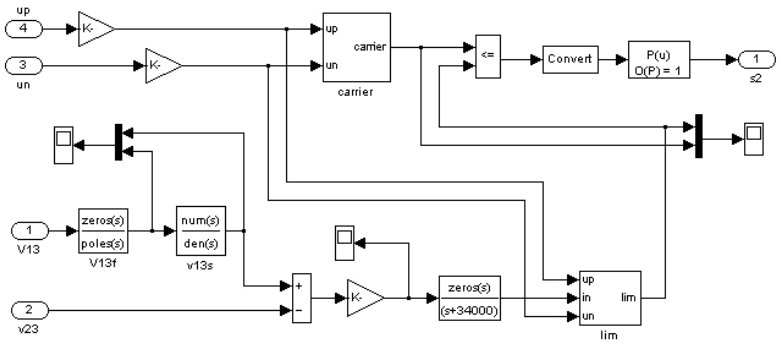


Figure 1.16: Output leg control scheme without current loop

1.5.2 Simulation Results

Hereafter are reported several diagrams illustrating the performances of the different control subsystems designed under various significant operating conditions, assuming that the main design parameters of the the converter are as follows:

- rated input (terminal 1): 230 Vrms , 15 Arms, 50 Hz
- rated output (terminal 2): 10 Arms
- d.c. bus: 2×400 V design, $2 \times 1200\ \mu F$
- input filter: $L_f = 400\ \mu H\ C_1 = 4.7\ \mu F\ L_1 = 2.2\ mH$
- output filter: $L_2 = 2.2\ mH\ C_2 = 6.8\ \mu F$
- carrier frequency for PWM: 15 kHz
- fixed hysteresis band: 5% rated current

At first a steady-state operating condition under *sinusoidal supply and balanced almost-resistive load* $cos\varphi = 0.99$ has been analyzed referring to both hysteresis (fig. 1.18, 1.20) and PWM (fig. 1.17, 1.19, 1.21) control of the input leg. The typical harmonic groups due to PWM modulators may be noticed both in the generated output voltage and in the input current, anyway they exhibit well acceptable values thanks to the employed filters. Also the low frequency harmonics at both sides result well acceptable, being smaller than 1% for both the control algorithms as shown in the detail spectrum in fig. 1.20 - 1.21. In fig. 1.22 - 1.27 a sequence of 2 transients is described under sinusoidal supply, namely a partial switch-off at $t = 0.3s$ followed by recovery of load to the initial condition at $t = 0.6s$. The impact of such transients on the output voltages appears negligible (fig. 1.24), as confirmed by the results of Park transformation carried out using a synchronous frame (fig. 1.25). The transient in the d.c. bus is also fairly limited, confirming the validity of the d.c. voltages control loops (fig. 1.27). The associated transient in the supply current appears also fairly fast and limited as shown in fig. 1.26. In fig. 1.28 - 1.34 a steady-state behavior is illustrated under sinusoidal supply from the feeder and unbalanced non-linear ohmic-inductive load. The load consists in particular in twin non-linear inductors between terminals $1-3$ and $2-3$ plus linear resistor between $2-3$. Despite the relevant distortion of load currents highlighted by the currents waveforms (fig. 1.28) and by one of the related spectrum (fig. 1.29), the load voltages remain fine although the typical commutation harmonics are detectable (fig. 1.30, 1.31). The spectrum of the input current also results fine both using a PWM modulator (fig. 1.33) and

using an hysteretic controller (fig. 1.34). Finally, in fig. 1.35 - 1.40 the operation with balanced almost resistive load under highly distorted mains supply with harmonics $3^{rd} = 10\%$, $5^{th} = 2.5\%$, $7^{th} = 1\%$ is illustrated. The quality, amplitude and phase of the line-to-line voltage generated appear quite satisfying as it may be noticed in fig. 1.35 and 1.36 despite the not negligible distortion of currents (fig. 1.37 and 1.38) and feeder voltages. The quality of the supply current appears also quite acceptable considering the unfavorable conditions (fig. 1.39 and 1.40).

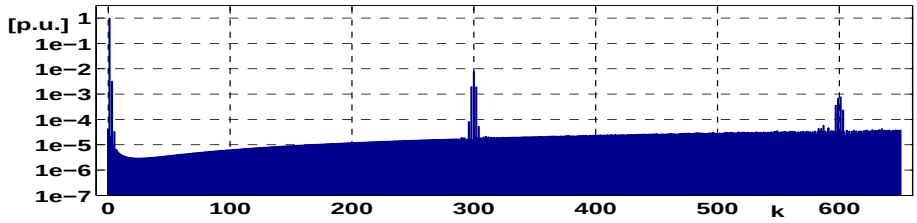


Figure 1.17: PWM control: spectrum of V_{23} [p.u.]

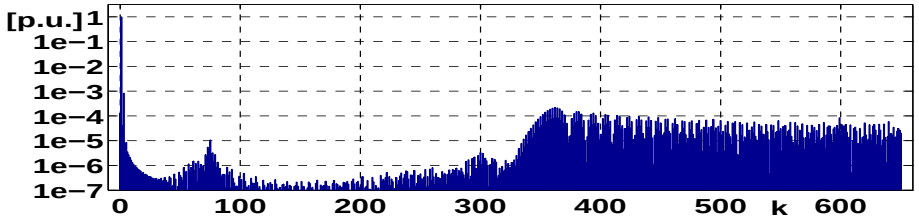


Figure 1.18: hysteresis control: spectrum of I_S [p.u.]

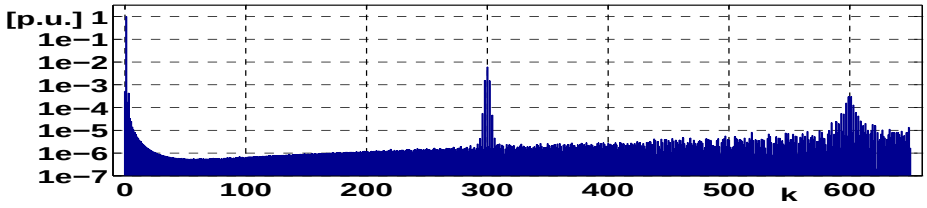


Figure 1.19: PWM control: spectrum of I_S [p.u.]

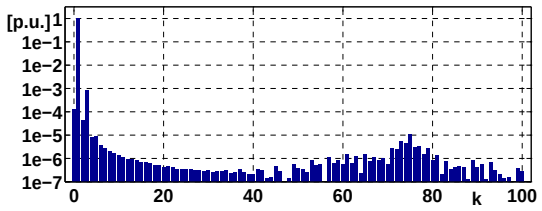


Figure 1.20: Detail of spectrum of I_S

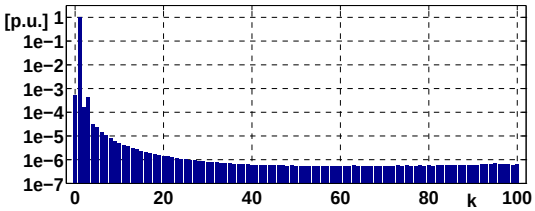


Figure 1.21: Detail of spectrum of I_S

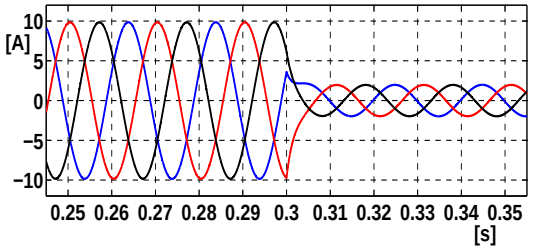


Figure 1.22: Load currents detail [A]

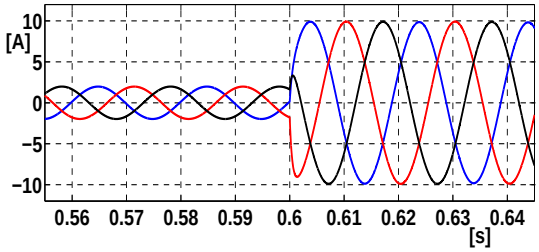


Figure 1.23: Load currents detail [A]

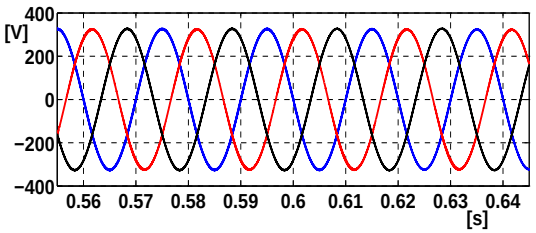


Figure 1.24: Output voltages [V]

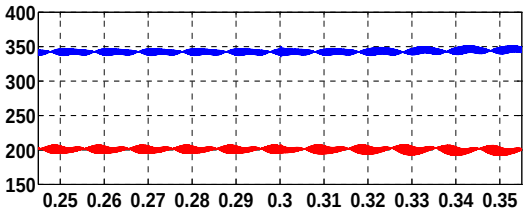


Figure 1.25: Output Park components [V]

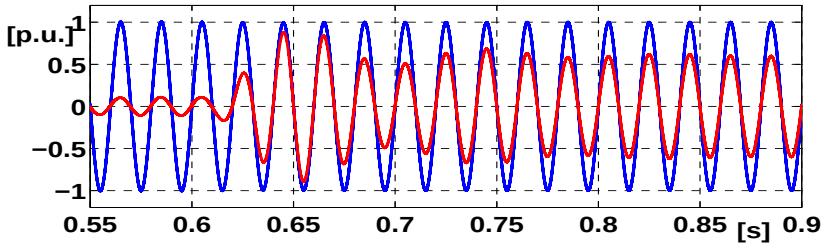


Figure 1.26: Supply voltage and current

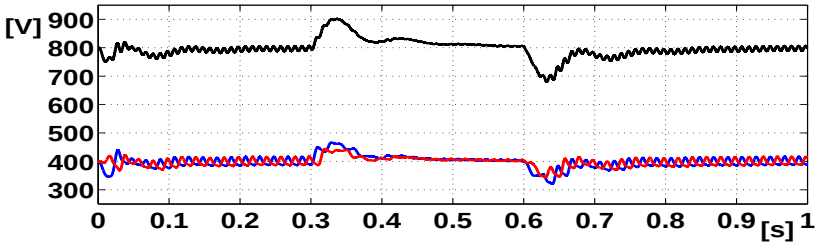


Figure 1.27: D.C. bus voltages [V]

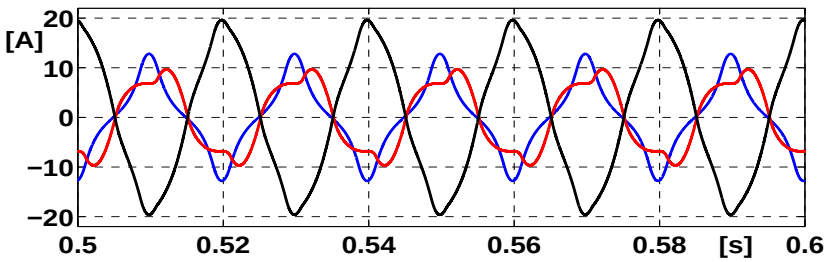


Figure 1.28: Non-linear load currents [A]

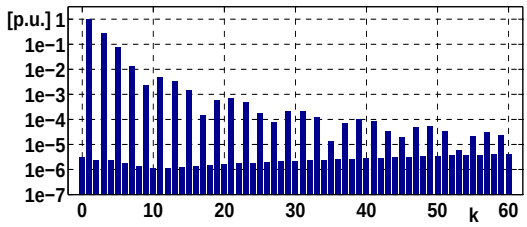


Figure 1.29: Spectrum of I_1 [p.u.]

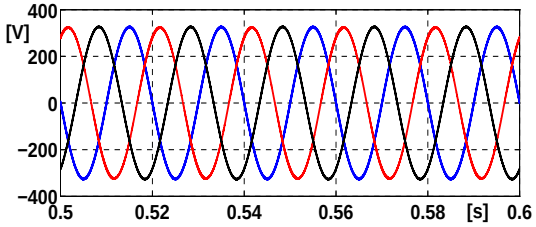


Figure 1.30: Load voltages [V]

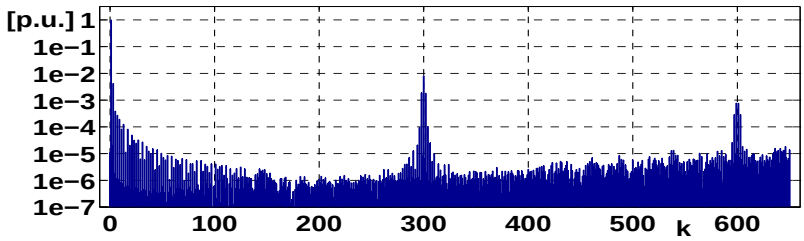


Figure 1.31: Spectrum of V_{23} [p.u.]

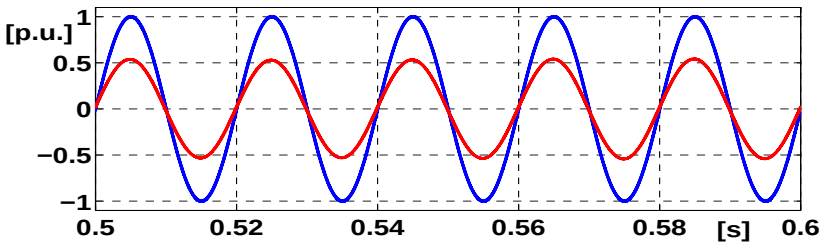


Figure 1.32: Supply voltage and current

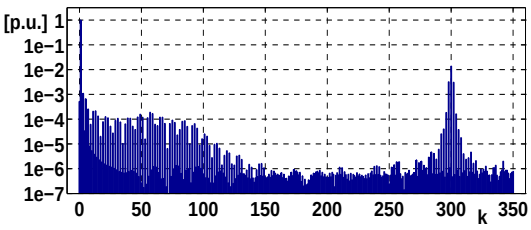


Figure 1.33: Spectrum of I_S [p.u.]

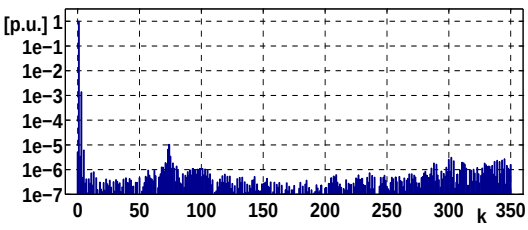


Figure 1.34: Spectrum of I_S [p.u.]

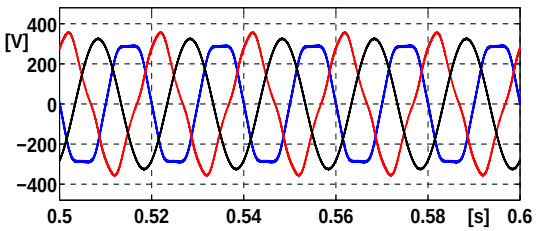


Figure 1.35: Output voltages [V]

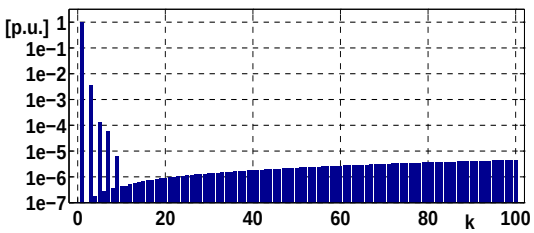


Figure 1.36: Spectrum of V_{23} [p.u.]

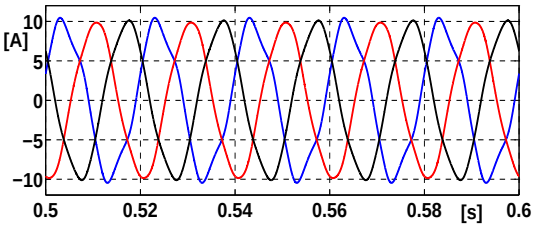


Figure 1.37: Load currents [A]

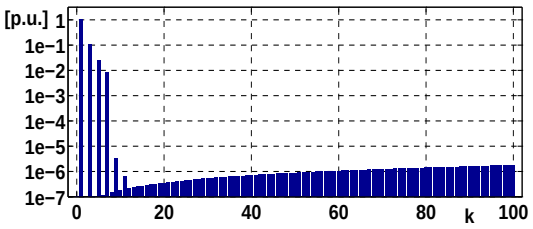


Figure 1.38: Spectrum of I_1 [p.u.]

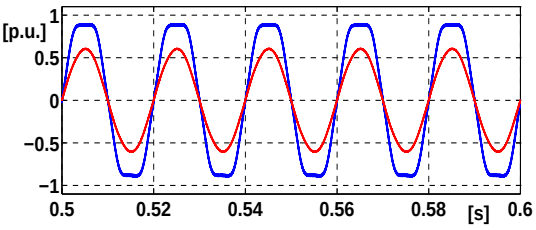


Figure 1.39: Supply voltage and current

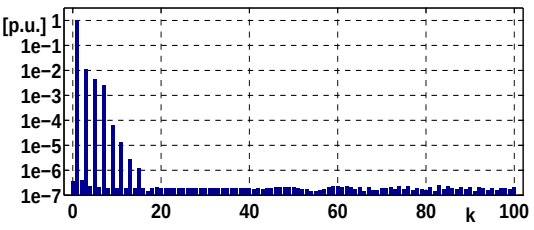


Figure 1.40: Spectrum of I_S [p.u.]

1.6 Modeling and Simulation of 4-Wires Variant

The second proposed converter variant, able to provide a 4-wires output, features the power structure shown in fig. 1.41. Basically, it may be derived from the 3-wires topology above described by assuming that the output terminal connected to the center tap of the d.c. capacitors bank becomes the neutral point and that a third VSI inverter leg, equipped with output filtering elements $L_3 - C_3$, is added to the circuit. Therefore, in this variant the first inverter leg still operates as active bidirectional controlled grid interface by means of the ballast inductor L_1, whereas the first output phase voltage V_{1N} is now derived from the feeder via the $L_F - C_1$ filtering pair. The further 2 output phase voltages V_{2N} , V_{3N} are provided by the other 2 inverter legs via their respective $L - C$ filtering groups. Thanks to their similarity, analogous control strategies may be adopted for both of the proposed converter variants. Moreover, basically the low-level control of

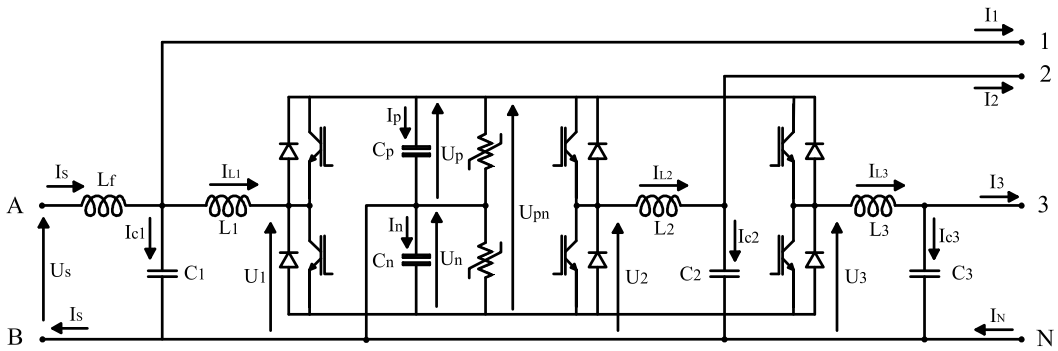


Figure 1.41: Semi-ideal scheme for the first converter variant

the various inverter legs may be treated independently thanks to the decoupling function carried out by the d.c. bus capacitors. For what concerns the first inverter leg, its role basically consists in regulating the current I_{L1} by means of the controlled voltage U_1 , in such a way to determine an appropriate waveform for the mains supply current I_S. Two different approaches were considered to generate the reference current waveform: it was obtained as a suitably scaled copy either of the actual feeder voltage waveform, or of its fundamental component. In the first case a pseudo-resistive PFC-like operation is achieved, which minimizes the rms value of the current drawn from the mains yet introducing current harmonics in case of distorted mains voltage. In the second case, ideally no current harmonics are generated, although this determines a potentially non-linear behavior of the converter in case of distorted mains voltage. In both cases, the control of current I_{L1} may be implemented either using a regulator driving a PWM modulator, or directly employing a simple hysteretic modulator-controller, anyway keeping into account the currents drawn from capacitor I_{C1} and from the first phase of load I_1 . In any case, the reference supply current is determined by an external slower control loop in such a way that the voltages U_P, U_N of the dual-split d.c. bus are kept around the design value. This may be achieved by modulating the amplitude of the supply current I_S depending on the error in the total d.c. bus voltage and by adding a limited offset when required to recover any unbalancement that might arise between the 2 bus sections. For what concerns the output inverter legs, each one is appointed to regulate a line-to-neutral voltage in such a way that the load is supplied with a symmetrical 3-phase system, at least for what concerns the fundamental component. Different control strategies were again examined, separately controlling each leg by exploiting the direct relationship between output voltage an related filter capacitor charge. A hierarchic scheme was tested first, including an inner control loop acting on the leg voltage U_k to determine an appropriate ballast inductor current I_{Lk} following the reference signal generated by an external slower loop controlling the output voltage V_{kN}. Such outer loop keeps into account the load current I_k to ensure that the capacitor current I_{Ck} evolves as required to generate the desired output voltage. Also in this case, both hysteretic and regulator-modulator variants were tested for the internal loop. Each current control loop was also equipped with a simple current-limitation emergency override logic aimed to increase the converter safety against overloads at almost no cost. As alternative, the opportunity to directly control each output voltage V_{kN} by using a single loop acting on the relevant leg voltage U_k and equipped with an appropriate regulator and PWM modulator was also investigated, treating the related load current I_k as a disturbance.

1.6.1 Simulation Results

In order to evaluate the performances of the 4-wires structure different simulation tests have been carried out exactly as for the 3-wires structure above presented. Several operative conditions, including quasi-sinusoidal steady-state, distorted steady-state and transients, were analyzed via simulation referring to different control strategies. As an example, hereafter are reported some results related to 3 significant conditions, referring to a converter featuring the following characteristics:

- input inductor: $L_f = 0.4$ mH
- filter inductors: $L_1 = L_2 = L_3 = 2.2$ mH
- capacitors: $C_1 = 4.7\ \mu F$, $C_2 = C_3 = 6.8\ \mu F$ and $C_P = C_N = 1200\ \mu F$
- rated input - phase output voltage: 230 V , 50 Hz
- current control loops including PWM modulators $f_c = 15$ kHz

In fig. 1.42 - 1.47 are reported significant results concerning a transient test under sinusoidal mains voltage, including three events (startup under linear balanced ohmic-inductive load, load step-down at $t = 0.3$ s, load step-up at $t = 0.6$ s) separated by short settling intervals. A polar plot of Clark vector of output phase voltages is shown in fig. 1.42, whereas the trends of synchronous Park components and the waveforms of the d.c. bus voltages are reported in fig. 1.43, 1.44 respectively. Detail plots of load phase voltages and currents and of mains voltage and current around the more demanding step-up transient instant are reported respectively in fig. 1.45, 1.46, 1.47. It may be noticed that the startup settling results rather fast without excessive voltage overshoot and that the perturbation of output voltage due to the load transient appears negligible thanks to a wise management of the transient variations of d.c. bus voltages, which anyway remain well balanced. The settling of supply current occurring after load transients result also rather quick and smooth.

In fig. 1.48 - 1.52 significant results are reported concerning a steady-state test under sinusoidal mains supply with heavily unbalanced and partly distorted load, including resistors and non-linear inductors. Despite the harsh conditions highlighted by the current waveforms reported in fig. 1.48, the quality of output voltages results rather fine as shown by the waveforms and relative spectrum reported in fig. 1.49-1.50, determining a $THD[V_{3N}] < 0.9\%$. The current drawn from the mains results also quasi sinusoidal and almost in phase with voltage, as shown by the p.u. waveforms reported in fig. 1.51 and confirmed by the spectrum

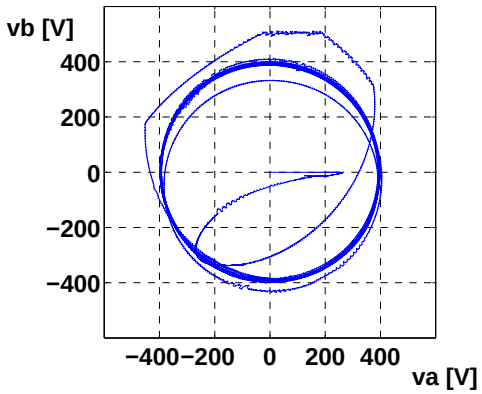


Figure 1.42: Clark polar vector diagram of output voltages

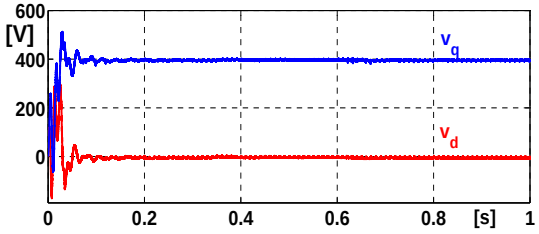


Figure 1.43: Output Park components [V]

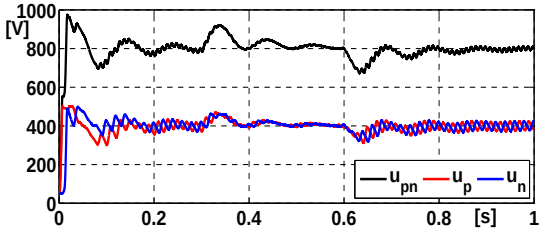


Figure 1.44: DC bus voltages [V]

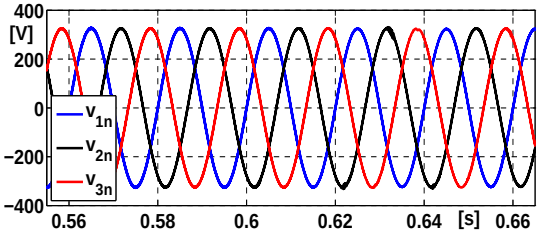


Figure 1.45: Output phase voltages [V]

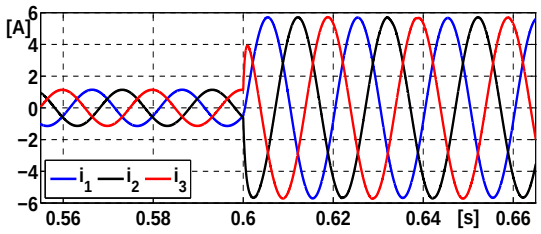


Figure 1.46: Load currents detail [A]

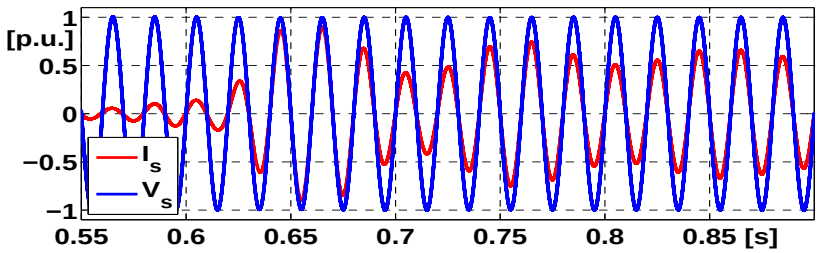


Figure 1.47: Transient test: supply voltage and current after load step-up

reported in fig. 1.52 determining a $THD[I_S] < 1.1\%$. Keeping in mind the waveform of the non-converted load current I_1 , the ability of the converter to operate also as an active filter results well highlighted.

Finally, in fig. 1.53 - 1.56 are reported significant results concerning a steady-state test under heavily distorted mains voltage (harmonics vs. fundamental amplitude: $A_3 = 10\%$ $A_5 = 2.5\%$ $A_7 = 1\%$, $THD[U_S] > 10\%$) with linear ohmic-inductive load, referring to a control strategy using the fundamental com-

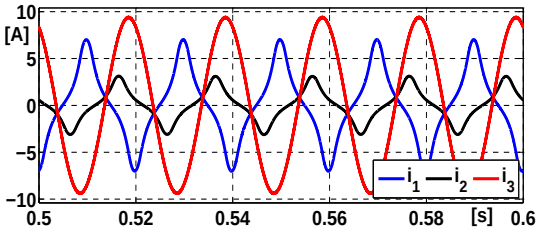


Figure 1.48: Non-linear load currents [A]

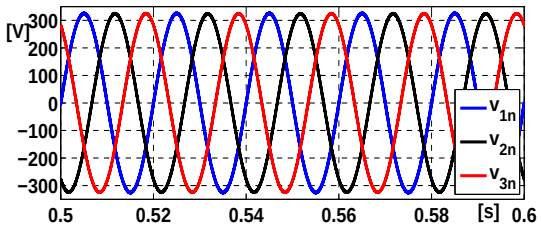


Figure 1.49: Output phase voltages [V]

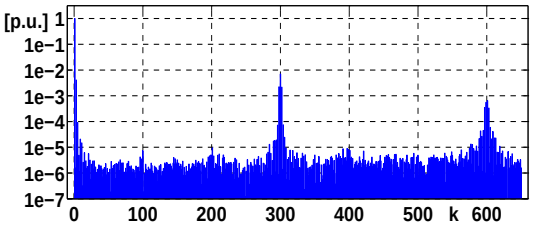


Figure 1.50: Spectrum of V_{3n}

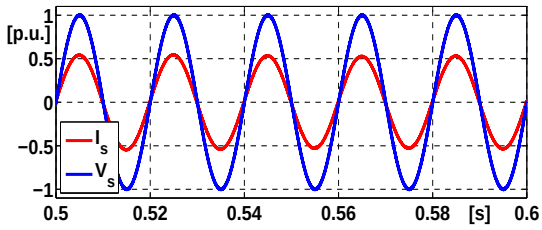


Figure 1.51: Supply voltage and current

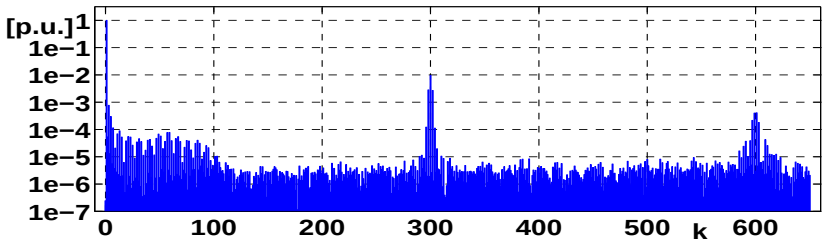


Figure 1.52: Steady-state test with distorted load: spectrum of mains current I_S

ponent of the mains voltage as reference waveform for the input current loop. The p.u. graphs of input voltage and current are depicted in fig. 1.53; highlighting the effective operation of the current shaping loop that is also confirmed by the relative spectrum of the mains current reported in fig.1.55, which determines a $THD[I_S] < 1.5\%$. The waveforms of output phase voltages are reported in fig. 1.54, highlighting the quality of the 2 phase voltages generated by the converter in comparison to the mains voltage, as also confirmed by the relative spectrum reported in fig. 1.56 which determines a $THD[V_{3N}] < 0.5\%$. In synthesis, the simulation results obtained for the 4-wires variant result promising and qualitatively similar to those achieved by the 3-wires variant already reported. Only minor differences are observed, basically related to the more demanding operation due to the larger percentage of load power actually converted in the 4-wires variant; it is expected that the performances might be further improved by increasing the size of d.c. bus capacitors to provide a more stable supply to the inverter legs, thus permitting to reduce the residual mutual disturbance between their control loops.

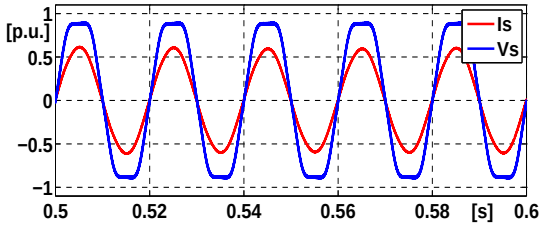


Figure 1.53: Supply voltage and current

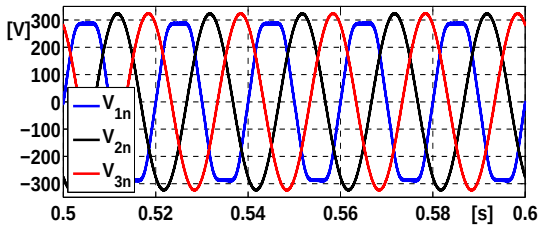


Figure 1.54: Output phase voltages [V]

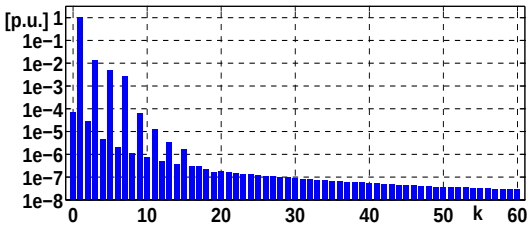


Figure 1.55: Spectrum of I_S

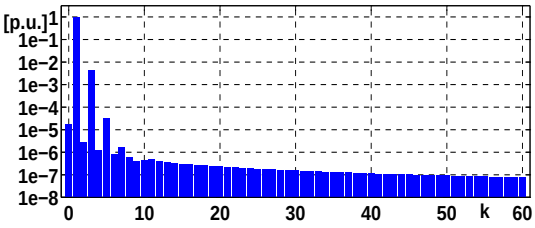


Figure 1.56: Spectrum of V_{3N}

1.6.2 Multi-Dimensional Vector Control

Besides the standard approach above recalled, considering actual variables, an alternative opportunity for controlling the proposed converter consist in adopting a multi-dimensional vector approach, eventually coupled to suited variables transformations able to further simplify the analysis of the system and the operation of controllers. In fact, such approach is already proposed for controlling active filters (e.g. [10]), representing a analogous yet not equivalent application. The opportunity of applying a vector control approach results rather evident for the 4-wires variant of the proposed converter, whose core consists in a standard 3-legs VSI bridge inverter with central tap: adopting such viewpoint means then considering the inverter as a whole instead than as a set of independently controlled legs. Keeping in mind the converter structure, it results rather evident that in most operating conditions the set of voltages U_k that the inverter should ideally generate should result not much different from a sinusoidal symmetric tern at fixed grid frequency. Therefore, by employing a vector control approach based on the Park "synchronous" transformation (i.e. with transformation parameter varying linearly with time according to the pulsation of grid voltage), the control loops should generate reference voltage vectors resulting grossly constant and featuring predominant d-q components. It may be then expected that simple controllers, such as PI, may be employed more easily with respect to control approaches operating on quantities basically varying in sinusoidal way. On the other hand, such approach results inherently less suited to implement control strategies acting in significantly different ways in the 3 phases; in particular, a suited compromise has

to be reached between the somewhat different requirements concerning the input leg and the output legs. Moreover, the problem should be approached at its full 3-D extent: in fact, despite the z (usually named homopolar) component is expected to be relatively small at steady state, it must be actively controlled since there is no reason permitting to neglect its contribution especially in dynamic terms. This conclusion is also supported by the connection to the center tap of d.c. bus, which may permit the sum of 3 the output currents flowing away from the inverter legs to be non-zero. In particular, the control system examined adopts the following strategy:

- the reference current for the input leg is calculated as previously described for the sinusoidal input variant, i.e. by multiplying a signal proportional to the fundamental component of the mains voltage, extracted through selective filtering, by a scaling factor determined by the d.c. bus voltage controller and by adding a suitably small rebalancing offset when necessary;

- the reference current for each output leg is also calculated as previously described, i.e. by determining first the desired load voltage waveform to be generated, by estimating then the current that should flow in the related capacitor and by finally adding the current drawn by the load;

- the errors of the actual currents I_{Lk} with respect to the above references are calculated, transformed using Park synchronous transformation and forwarded to 3 independent PI controllers, which provide the reference values for the d-q-z components of the inverter output voltage;

- such reference components are then forwarded to a complete SVM modulator that employs a 4-states basic pattern to achieve the equivalence of average values between reference and output for both the d-q and the z components, keeping into account the actual values of the d.c. bus voltages.

1.6.3 Simulation Results using Vector Control

A suitably adapted version of the Matlab-Simulink® model above recalled was get ready to permit investigating the behavior of the proposed converter using the vector control above described. The most interesting waveforms obtained for steady state conditions were also post-processed to determine their spectral contents. Hereafter are reported the most interesting results obtained this way, referring to the following mid-low power hypothetical application scenario:

- rated mains voltage and phase load voltage: 230 Vrms, 50 Hz

- design DC bus voltage: 2×400 V

- inductors: $L_f = 0.4\ mH$, $L_1 = L_2 = L_3 = 2.2\ mH$

- capacitors: $C_1 = C_2 = C_3 = 6.8\ \mu F$, $C_P = C_N = 1200\ \mu F$

Assuming as reference operation steady-state conditions under rated sinusoidal mains supply and linear equilibrated almost ohmic inductive load with fundamental power factor $cos\varphi_1 = 0.99$, in fig. 1.57 are reported the waveforms of the output phase voltages, whose fine trend may be noticed. In fig.1.58 are reported in p.u. the waveforms of feeder voltage and current, highlighting the good power quality achieved also at input side. In fig. 1.59 an interpolated spatial representation for the trend of the 3 output voltages U_k provided by the inverter in a short time interval is also reported, exhibiting small oscillations around the vertexes of the ideal cube due to the ripple in the d.c. bus voltages. In fig. 1.60 the transient trend of the d.c. bus voltages is reported following a switch-on under the same load: it may be noticed that its duration is rather limited with a short overshoot capped by varistors, after which the voltages are quickly led to their reference values exhibiting the inherent complementary ripple due to power balance inside a mains period. In fig. 1.61 the projection on Clark plane of the interpolated plot of the output voltages provided by the inverter is depicted from switch-on to steady state, highlighting the effect of the variable d.c. bus voltages in the Clark reference frame.

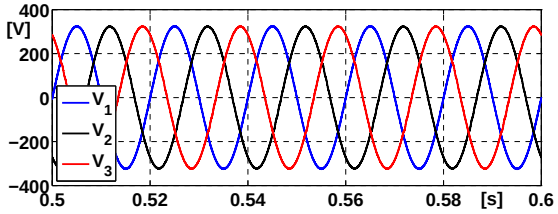


Figure 1.57: Output phase voltages [V]

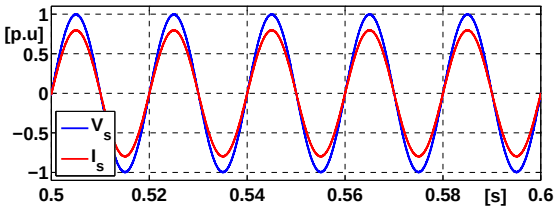


Figure 1.58: Supply voltage and current

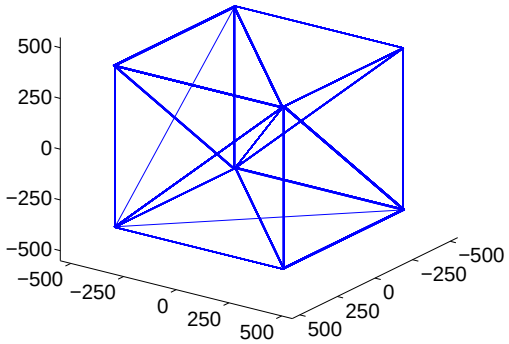


Figure 1.59: Interpolated inverter voltages at steady-state.
Three-dimensional reference system having as axes the three legs output voltages U_1, U_2 and U_3

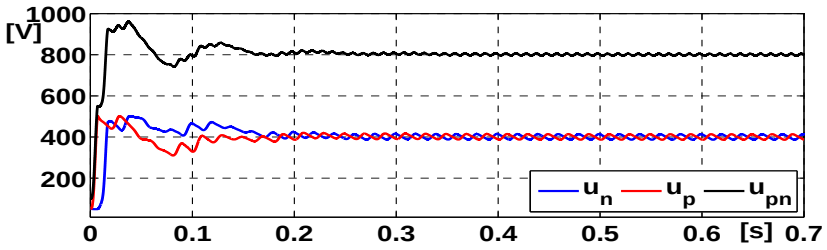


Figure 1.60: DC bus total and partial voltages: startup transient and settling

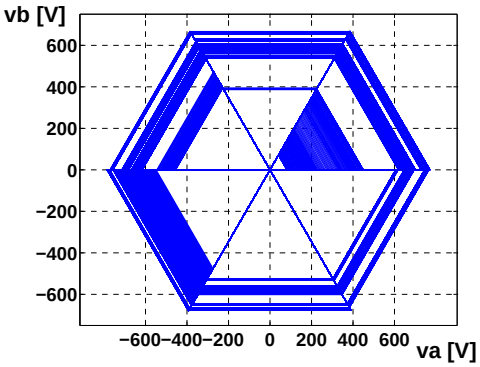


Figure 1.61: Interpolated inverter voltage d-q components during the d.c link charging transient

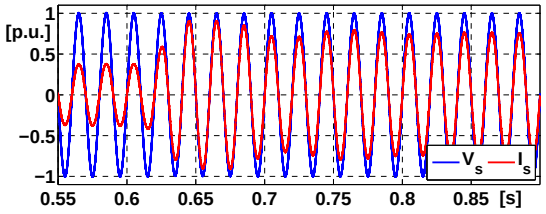


Figure 1.62: Mains current and voltage

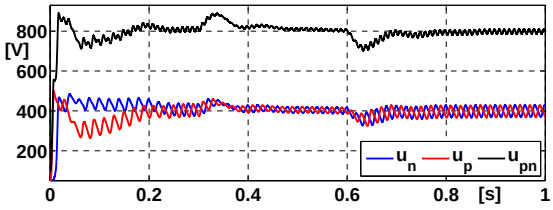


Figure 1.63: DC bus voltages [V]

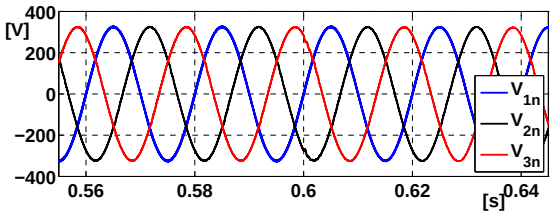


Figure 1.64: Output phase voltages [V]

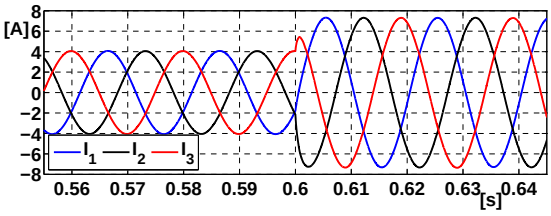


Figure 1.65: Load currents detail [A]

As an example of dynamically perturbed conditions a transient is examined consisting in a rapid sequence of complementary step variations of amplitude and fundamental power factor of a linear balanced quasi-ohmic load similar to the one considered in the standard operation case, still assuming rated sinusoidal mains supply. Namely, after startup the load is reduced at $t_1 = 300$ ms and it is then reverted to its initial level at $t_2 = 600$ ms. The resulting current waveforms around the second more demanding transient are reported in fig. 1.65, whereas the corresponding voltages are reported in fig. 1.64 highlighting the good load

rejection capability of the system as the perturbation effects in the 2 generated voltages result barely noticeable. In fig. 1.63 the full trend of the d.c. bus voltages is reported, highlighting the 2 opposite transients taking place due to load step-down and step-up. Finally, the corresponding trend of the current drawn from the mains around the second transient is reported in fig. 1.62, highlighting a rather fast settling capability with a limited overshoot. For the sake of brevity not additional results are reported hereafter related to other unfavorable conditions. Anyway the good results above illustrated confirm the good behaviour obtained even using a space vector control strategy.

1.7 Conclusions

Although 3-phase loads are usually technically preferable with respect to their 1-phase counterparts, only 1-phase feeders are often available for low power levels electric utilities. Therefore, extending a standard 1-phase feeder into a 3-phase supply represents a problem having some practical interest. Several solutions might be considered for such purpose, including any of the popular converter topologies used for 3-phase drives supplied by 1-phase mains which might well provide the desired fixed output. Nevertheless, more wise solutions may be singled out keeping into account the peculiarities of the problem. In fact, in the considered context the available 1-phase supply may be used to directly provide one of the phase or line-to-line load voltages. Moreover, a bidirectional power flow capability is appreciable to properly manage regenerative braking of motors etc. Finally, a good input and output power quality should be assumed as a goal, due to the known issues related to harmonic pollution, voltage distortion and reactive power flow. Keeping in mind the above considerations, 2 versions of a dedicated converter were proposed respectively referring to 3-wires and 4-wires output. Their schemes and operation principle have been explained, highlighting the dual function of output-side generator and input-side active front-end and filter performed by the core of the converter, consisting in a 2-legs or 3-legs VSI inverter supported by a split d.c. bus. Such structures, exploiting the opportunity to directly use the mains voltage as one of the output voltages, permits to achieve high power quality at both sides and full reversibility using simpler and less expensive topologies than solutions derivable from common variable-speed AC drives. Different control options were investigated and explained, as well as the analytical and simulation models developed. A phasor-based steady-state analysis was reported, as well as design considerations highlighting some differences between the 2 variants. The control strategies monitoring separately input and output in-

verter legs, have been explained. The opportunity to also consider vector control has been then highlighted, illustrating its potential benefits and a first application to the 3-legs 4-wires variant. A semi-ideal simulation model purposely developed in the Matlab-Simulink® environment to permit analyzing the actual behavior of the proposed system has been then recalled. Finally, simulation results concerning several different operating conditions, including both sinusoidal and distorted supply and both linear and non-linear loads, have been reported and commented. Such results basically confirm the applicability of the vector control approach to the proposed converter.

Chapter 2

Real-Time Control of a Single-Bus Active Filter

2.1 Introduction

In recent years, due to the intensive use of power converters, power quality issues have become more and more important. Non sinusoidal currents drawn by non-linear loads in fact cause several undesirable effects such as supply voltage distortions, increased communication and protection equipment failures, increased losses, overheating and overloading problems that have to be taken into account. In order to limit these problems in most countries electrical supply industry has established strict regulations limiting the magnitude of harmonic distortion that can be drawn by each user. This is leading to a growing interest in active mains interface and active filters witch are both effective and convenient solutions to mitigate harmonic pollution problems. A possibility may consist in using a shunt active filter (SAF) connected to the mains. In its classical configuration, a SAF basically consists in a VSI inverter whose dc side is connected to a capacitors bank whereas its ac side is connected to the mains by means of a suited filter, including at least series inductors (e.g. fig. 2.1 referred to the most common 3-wires configuration without neutral). Thanks to such configuration, ideally the SAF is able to operate as a controllable current generator, injecting in the mains any set of null-sum current waveforms. Obviously, since under steady-state conditions the voltage of the dc bus is intended to remain nearly constant at the design level to permit an indefinitely long operation, the currents injected in the mains must determine a small net average power flow towards the apparatus, exactly balancing its internal losses. Therefore, a SAF is ideally able to provide the unbalanced, reactive and harmonic components of the currents drawn by any load, in such a way that the global equivalent load, as seen from the grid, resembles a resistive

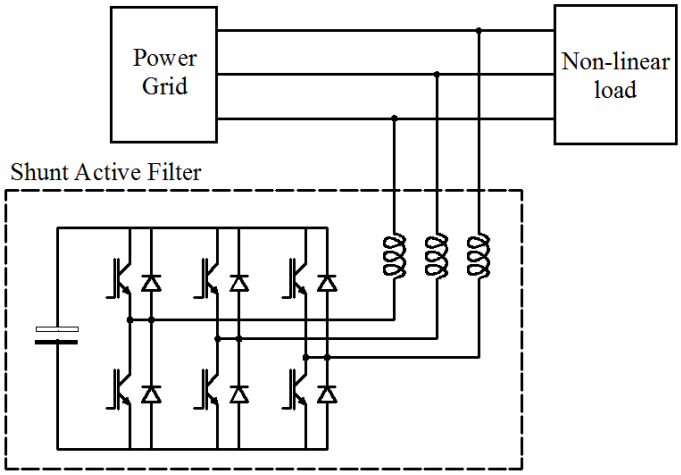


Figure 2.1: Typical structure of 3-wires Shunt Active Filter

balanced load drawing about the same active power. After a brief overview of the classical control strategies used for active shunt filter control in standard industrial applications hereafter several specific solutions for aerospace applications are recalled. The main issues related to the high frequency involved are discussed highlighting as the overall system may result particularly demanding for both power and control devices. A modified dead beat control able to work both in standard industrial applications and aerospace ambit is then proposed. Significant results obtained by experimental tests are finally reported and commented, referring to a prototype system purposely implemented.

2.2 Classical Control Strategies for SAFs

The accurate management of active filters is a demanding control challenge, as high bandwidth regulation is required with a relatively low switching frequency even in the presence of supply disturbances. The current reference consists of the harmonic components at frequencies much higher than the fundamental which need to be identified. The identification algorithm employed could itself have an influence on the dynamic behavior of the system. The current controller should minimize the phase and amplitude errors for a wide range of reference trajectories, provide fast dynamic response, have robustness to model and parameter uncertainties, and also be able to reject noise. From a theoretical point of view, several different well established strategies are available in the technical literature for effective compensation of current harmonics and reactive power using SAFs. Classical control compensators such as proportional plus integral (PI), or PI plus Lead, fail to meet these requirements, mainly because the sampling delays in-

curred through using a digital control with pulse width modulators (PWM) limit the maximum bandwidth realistically achievable. Moreover, if reference signals are sinusoidal quantities, this kind of control is not able to eliminate the steady state error and to achieve satisfactory reference tracking performances. Therefore often a control strategy consisting in multiple reference frames is adopted [11] increasing the accuracy but reducing at the same time the implementation simplicity; the interactions among different frames and the presence of band-pass filter stages make the design and the tuning of the controllers a rather difficult task. Alternatively a proportional plus resonant controller may be used [12] in order to avoid the frame transformation and reduce the related computational burden. The possibility of reducing the number of measurements is also investigated in several paper [13], using a state feedback control and a suitable designed observer. Other types of control structure have been considered, including neural networks, sliding mode and hysteresis controllers. Finally among other techniques, also predictive current control [14], [15], [16] was considered in several papers. In fact even if, as a model based control, its performances depend on the knowledge of system parameters, it offers the advantage of precise current tracking over a wide frequency range. Basically the task of this control strategy is to predict the future behavior of the plant according to the model. The prediction techniques published so far can be divided into two main categories according to the processing power required. A less computationally intensive approach incorporates prediction methods concerning the next few sampling periods [17], [18], [19]. Alternatively, a prediction up to a specified finite horizon, including on-line optimization, demands intensive processor time, which can be a major restriction in applications such as ASFs which have high frequency reference trajectories [20], [21], [22]. Here a method for predicting variables one and two sample instants in advance able to work in the presence of microprocessor and actuation based delays is proposed. The stability with respect to the model parameter uncertainties is analyzed, and system robustness to parameter mismatch is demonstrated. An additional consideration is that high bandwidth controllers usually have high sensitivity to the different types of noise that can appear on experimental systems (e.g. quantization, electromagnetic interference from other power electronic devices and systems), and therefore practical implementation can be very difficult in an environment where the noise cannot be easily reduced. The sensitivity of the proposed control solution to measurement noise is analytically quantified and experimentally verified with respect to the conventional deadbeat controller. This work discusses issues connected with ASF current reference prediction when a polynomial-type extrapolation predictor is employed and proposes an alternative more robust solution.

2.3 Specific Solutions for Aircraft Applications

Recently an interesting field in witch the application of active shunt filter has been studied and developed is the aerospace/avionic ambit. The "more electric aircraft" paradigm, consisting in the replacement of most of hydraulic/pneumatic actuators with electronically controlled electromechanical devices, gained a growing interest in the aerospace industry. In fact, it is expected to provide significant benefits in terms of actuation accuracy, employ flexibility, system dependability, energy efficiency and overall lifecycle cost thanks to the reduced maintenance requirements [23]. A simplified example of typical generic constant-frequency aircraft power system is sketched in fig. 2.2, where only one aircraft engine is shown for simplicity. It basically consists in an AC variable-speed fixed-frequency AC bus, typically operated at 115 V - 400 Hz, which is used to supply different loads and may be fed either from on-board generators or from an external power source when the aircraft is parked. The power system also includes two DC buses, respectively operated at 540 V and 28 V: the first one is connected to the AC bus through an active rectifier and to the second one via a bidirectional dc-dc converter between them. Although the presence of electrically powered equipment is desirable for the several reasons above outlined, the growing employ of apparatuses operating as non-linear loads, especially when fed through converters, makes more and more difficult keeping a good power quality level in the aircraft grid. In fact, the size of aircraft electric power systems is relatively small with a rough balance of rated power of loads and generators, exacerbating the typical issues due to harmonic pollution. This is leading to a growing interest in active mains interfaces and active filters suited to operate in aerospace ambit. In fact, shunt active filters (SAFs) are generally used to turn unbalanced, non-resistive and distorted loads into equivalent quasi- balanced resistive linear loads. Anyway, their application in the avionic ambit presents specific issues mainly related to the higher rated frequency (presently 400 Hz), which deserve further investigation. Despite the increasing power quality issues on board of aircrafts, the use of SAFs in such applications has been investigated rather rarely in the literature. For example, in [23] a complete model for an aircraft electric power system was developed using a perfect harmonic cancellation method. Actually, the aerospace ambit poses specific challenges for both the power and control parts of SAFs due to the much higher frequency (400 Hz in spite of 50/60 Hz as used in standard applications). Such aspect will be exacerbated in the future, when the AC bus will be operated at variable voltage and frequency, possibly up to 800 Hz, to permit eliminating the mechanical coupling apparatuses that presently permits to keep almost constant the generators speed when the driving engines operate at variable speed. In

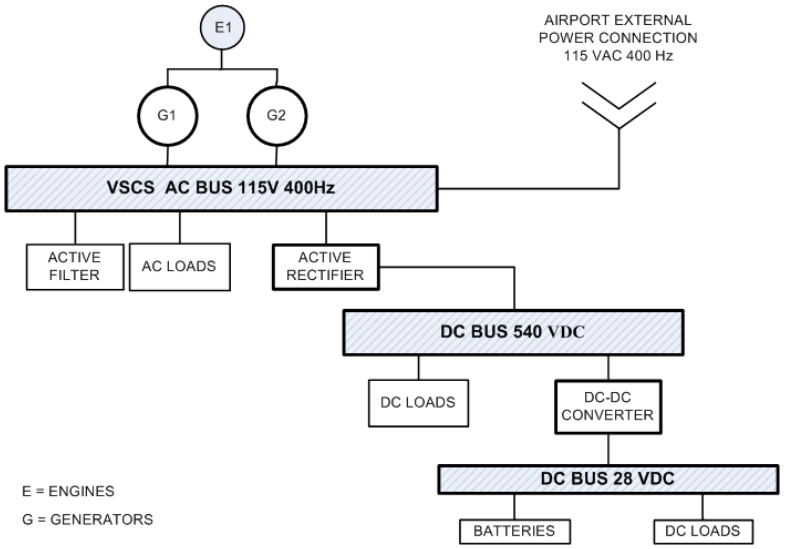


Figure 2.2: Simplified example of electric aircraft power network

fact, good compensation performances require a suitably large bandwidth of control loops in comparison to the base frequency, which may be difficult to achieve considering the present limits of power semiconductor devices and of microcontrollers/DSP in terms respectively of switching frequency and elaboration speed.

2.4 System modeling

The proposed control is a model-based control method and therefore an appropriate model of the system is an essential part for the controller design. The operation of the active filter is determined not only by the active filter itself but also by the system, i.e., by the ac source impedance and the load characteristics. According

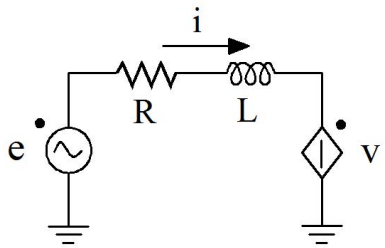


Figure 2.3: Equivalent circuital model of each SAF phase

to [24], [25], [26], a theoretical pseudo-linear dynamic analysis of the considered SAF, based on the time-averaged value approach, may be undertaken referring to the semi-ideal model based on the equivalent single-phase circuit sketched in fig. 2.3. In such model, aimed to investigate the operation at ac side separately per

each SAF phase, all of the relevant elements are represented in idealized terms:

- the mains phase voltage at PCC is schematized as a purely time-dependent generator $e(t)$, thus neglecting the equivalent impedance of the grid; the set of phase voltages at PCC is assumed having a direct sequence, i.e. including only a direct symmetrical component;

- the average value of the inverter leg voltage during a sampling period is schematized as a controlled generator $v(t)$ whose value depends on the modulator output and on the DC bus voltage, thus neglecting the conduction voltage drop in the switching devices;

- the 3 filter inductors are modeled as linear $R-L$ series bipoles featuring the same parameter values.

Since a 3-wires connection without neutral is assumed between SAF and grid (fig. 2.1), the sum of the currents drawn by the inverter has to be null: this implies that the tern of voltage drops across the line inductors must exhibit a null zero sequence component. Therefore, both of the generators in fig. 2.3 actually represent the balanced components of the relevant phase voltages of grid and inverter. The equation governing such simple circuit results:

$$\frac{\mathrm{d}i\,(t)}{\mathrm{d}t} + \frac{R}{L} i\,(t) = \frac{e\,(t) - v\,(t)}{L} \tag{2.1}$$

where $i\,(t)$ is then the relevant phase current drawn by the SAF. Assuming that both mains and inverter voltages may be considered almost constant during a sampling period T_s of the digital controller the above equation provides:

$$i\,(t+T_s) \cong i\,(t) \cdot e^{-\frac{R}{L}\cdot T_s} - \frac{e\,(t) - v\,(t)}{R}\left(1 - e^{-\frac{R}{L}\cdot T_s}\right) \tag{2.2}$$

Introducing the a and b parameters

$$a = e^{-\frac{R}{L}\cdot T_s} \cong 1 - \frac{R}{L} \quad T_s \qquad , \qquad b = \frac{1 - e^{-\frac{R}{L}\cdot T_s}}{R} \cong \frac{T_s}{L} \tag{2.3}$$

and the sequential step notation used in discrete-time systems, the equation describing the SAF behavior may be then rewritten in an approximated form as:

$$I(k+1) = I(k) \cdot a + [E(k) - V(k)] \cdot b \tag{2.4}$$

where $E(k)$, $V(k)$, $I(k)$ denote the values of the corresponding time domain quantities $i(t)$, $v(t)$, $e(t)$ at time instant $t_k = kT_s$

2.5 Proposed Control System

The strategy proposed for controlling the system is based on considering the load and the SAF as a whole aggregate consuming power and featuring some electric energy storage capability, primarily due to the capacitors bank connected to the d.c bus. Keeping in mind the power balance of the whole aggregate, obviously at steady state the average power drawn from the mains must equal the average power drawn by the load plus the small internal losses inside the SAF apparatus. In such condition, the average energy stored in the SAF capacitors, and thus the d.c. bus voltage, must then remain constant in average terms across a period. Therefore, the control system of the SAF may generate reference waveforms for the line currents globally drawn from the aggregate as a 3-phase set of sinusoids exhibiting only a direct symmetrical component and the same phase as the PCC voltages, in such a way to emulate an ideal sinusoidal load with null fundamental reactive power. The amplitude of such reference currents has to be suitably regulated by a dedicated control loop, in such a way that in average terms the d.c. bus voltage remains constant across a period, assuming a value close to the rated one. Therefore, the reference waveforms for the currents to be drawn by the SAF are obtained by subtracting the actual distorted load currents from the global currents reference waveforms generated as above outlined. The SAF currents are then forced to closely track such reference signals by means of dedicated inner control loop, which ultimately determine the inverter operation eventually by means of a modulation block, such as a space vector modulator (SVM). Therefore, the SAF control system basically features a dual-loop nested hierarchical scheme, with rather different response times as the dynamics of the DC bus voltage is expected to be rather slow in comparison to the dynamics of load and filter currents. For the controller used to keep the average voltage of SAF d.c. bus voltage at its design value, a simple PI saturated regulator was adopted, as it results adequate and rather simple to implement. The output of such controller provides the amplitude id^* of the Park vector representing the desired set of sinusoidal symmetrical 3-phase direct-sequence mains currents that would ensure the power balance of the aggregate with null fundamental reactive power. The response time of this control loop is purposely adjusted to be suitably longer than the response time of the current control loop described thereafter. The actual waveforms of the aggregate reference currents are obtained from the reference vector above cited by applying the inverse synchronous Park transformation, using as transformation parameter the value provided in real time by a PLL (phase-locked loop). The reference signals I^* for currents drawn from the SAF are then obtained by subtracting from the above global waveforms the actual currents drawn from the load. For

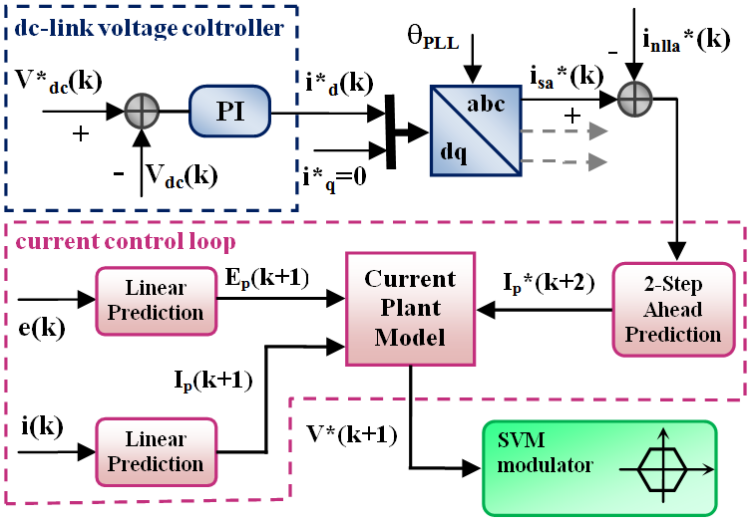


Figure 2.4: Block diagram of the overall control scheme

such purpose only 2 current sensors are used, while the third current is simply calculated as the opposite of the sum of the former two, due to the null sum constraint determined by the 3-wires configuration. When the values of $E(k)$ and $I(k)$ are available by sensing, at a first look equation 2.4 might seem permitting to provide at each step the best value of the inverter voltage $V(k)$ based on the desired current trend $I(k+1)$, which could be obtained as described in the previous section. Nevertheless, in practice such calculations require some elaboration time, meaning that they cannot be completed according to the timing scenario that led to eqn. 2.2: this implies that eqn. 2.4 cannot provide a dynamic response involving a simple 1-cycle delay. Assuming that the above calculations can be completed within one sampling period of the system, moving equation 2.4 one step forward

$$I(k+2) = I(k+1) \cdot a + [E(k+1) - V(k+1)] \cdot b \tag{2.5}$$

and introducing the current error signal ΔI between reference current I^* and actual current I

$$\Delta I(k+2) = I^*(k+2) - I(k+2) \tag{2.6}$$

one obtains

$$V(k+1) = E(k+1) - \frac{[I^*(k+2) - \Delta I(k+2) - I(k+1) \cdot a]}{b} \tag{2.7}$$

Equation 2.7 might be used to determine, by calculations carried out within sampling period k , the desired voltage value to be applied during step $k+1$ aiming to make the inductor current achieve its reference value at the end of the following sampling period, i.e. this would permit then to achieve a 2-steps dynamic delay. The block diagram of the overall control structure considering

both the voltage and current control loop is depicted in fig. 2.4. The meaning of the prediction blocks will be explained hereafter. Unfortunately, the values of $I(k+1)$ and $E(k+1)$ appearing in eqn. 2.7 are not available at time t_k , as well as the desired value $I^*(k+2)$: the use of corresponding predicted quantities E_p, I_p , I_p^* is then necessary. Equation 2.7 can be rewritten as:

$$V^*(k+1) = E_p(k+1) - \frac{\left[I_p^*(k+2) - I_p(k+1)\cdot a - I(k+1)\cdot a\right]}{b} \tag{2.8}$$

Keeping in mind that the PCC voltage is expected to exhibit a rather sinusoidal waveform, for its prediction a simple linear extrapolation algorithm was used according to

$$E_p(k+1) \cong 2\cdot E(k) - E(k-1) \tag{2.9}$$

Regarding the SAF current, an approach not involving the use of a system model was preferred to make the prediction less sensitive to parameters variations and noise. Therefore, only the available values of actual current I and of reference current I^* were used as well as the predicted value of reference current I_p^*, finally obtaining

$$I_p(k+1) = I_p^*(k+1) + \frac{[I(k) - I^*(k)]}{2} \tag{2.10}$$

Determining the 1-step and 2-steps ahead predictions of the current reference signal required in the above expressions results indeed more challenging. In fact, since $i^*(t)$ may be affected by significant harmonics, a linear extrapolation may not result sufficiently accurate. When the sampling frequency is fixed, using an higher order polynomial extrapolation may appear an interesting solution. For example, using the generic n^{th} order Lagrange extrapolation formula as in [25], the generic predicted value is given by a linear combination of the values assumed in n previous sampling instants as:

$$I_p^*(k+1) = \sum_{h=0}^{n} (-1)^{n-h} \frac{(n+1)!}{h!(n-1-h)!} \cdot I^*(k+h-n) \tag{2.11}$$

Such expression may be then applied 2 times to obtain sequentially the predictions $I_p^*(k+1)$ and $I_p^*(k+2)$. Nevertheless, the frequency response of such predictor using different extrapolation orders was checked to highlight possible issues when used in the digital control system. Assuming for example a reasonable sampling frequency (10 kHz), the related amplitude and phase Bode diagrams for the significant frequency range resulted as depicted in fig. 2.5, 2.7 for the lowest 5 orders. The amplitude diagram highlights a marked band-pass effect centered at half the sampling frequency, which is notably enhanced by the extrapolation order.
On the other hand, at low frequency the best amplitude response is provided by

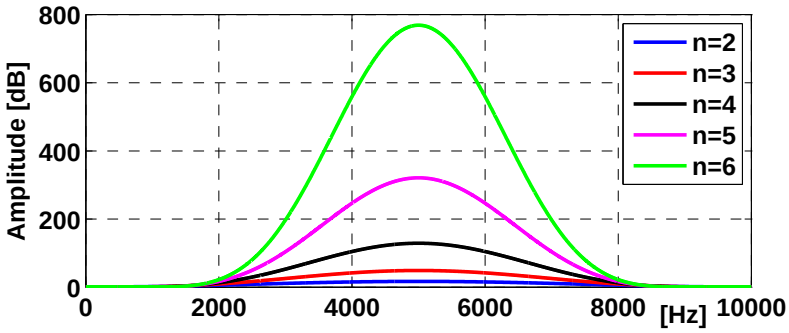


Figure 2.5: Amplitude Bode diagram of different orders Lagrange predictors

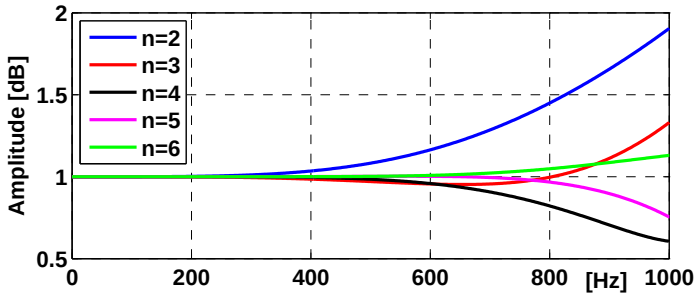


Figure 2.6: Low-frequency range detail of Bode diagram depicted in fig. 2.5

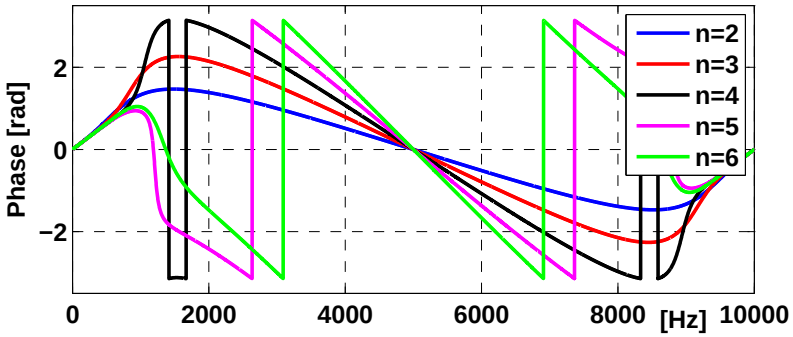


Figure 2.7: Phase Bode diagram of different orders Lagrange predictors

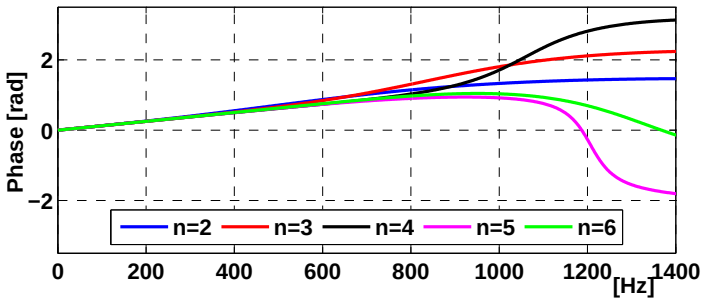


Figure 2.8: Low-frequency range detail of Bode diagram depicted in fig. 2.7

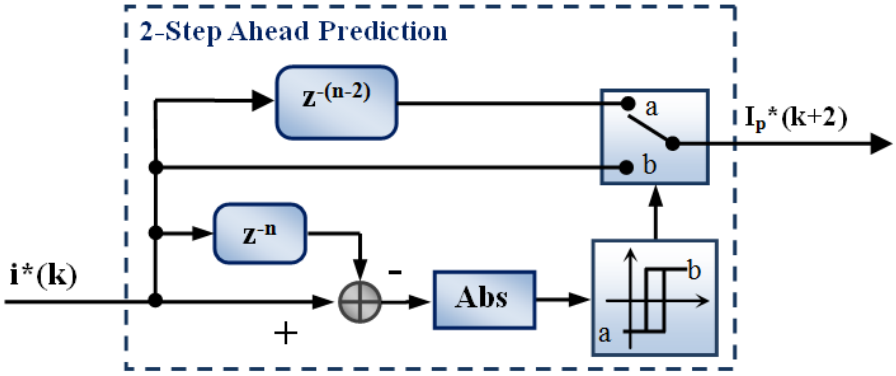


Figure 2.9: Block diagram of the 2-Step Ahead Prediction

the highest order extrapolator, as highlighted by the detail shown in fig. 2.6, 2.8. A satisfying compromise, enabling to filter-out high order harmonics while preserving low order ones, which are expected to be accurately compensated, may then result rather difficult to achieve, especially when considering a rather high fundamental frequency as 400 Hz.

To overcome such problem, a "*history based*" prediction is adopted here, leveraging on the fact that at steady-state the signals are ideally periodic, meaning that in practice they should exhibit at least a rather close repetitive behavior. In fact, this allows to predict the value of any quantity at a given instant t by simply checking the value of that variable exactly 1 period before (T), i.e. at the time instant $t - T$. Nevertheless, when applied systematically such kind of prediction would introduce an unacceptable 1-period delay during fast transients: under such conditions, even a very simple guess, such as assuming for the predicted quantity the last known value, may then produce better results. Therefore, an hysteretic-type operative mode identification logic was added based on the absolute difference between the values assumed by the considered quantity at the current step and exactly 1 period before. When such difference falls below a first suited threshold, steady-state condition is detected and the history-based prediction is activated; when instead it rises above a second greater threshold, transient condition is detected and such prediction is replaced by the present value of the signal that is known at time t_k. This way, in steady-state mode the predictor actually compensates the phase error introduced by the computation delay, whereas in transient mode it operates introducing a 2-sampling-steps response delay. In this paper, such approach was used in particular to obtain the required prediction of the current reference signal I^*. A block diagram of the prediction algorithm actually implemented is shown in fig. 2.9, where n indicates the number of samples in a fundamental period. The inverter leg voltages reference values obtained from 2.8 as above described are finally forwarded to a Space Vector Modulator (SVM) op-

erating in asymmetric mode, thus permitting to employ a sampling frequency that is twice the inverter switching frequency.

2.6 Prototype System

The actual performance of the proposed control strategy was probed by experimental testing referring to a prototype system, which was purposely built in the University of Nottingham laboratory. According to the scheme depicted in fig. 2.1, the SAF experimental prototype used includes a standard 3-legs IGBT based VSI inverter whose leg rated current is 15 A whereas the designed d.c. bus voltage is 500 V. The d.c. terminals of the inverter are connected to a capacitors bank featuring a 4400 μF capacity, whereas the a.c. terminals are connected to the mains PCC via three filtering inductors: featuring equivalent series parameters $L = 3$ mH, $R = 0.037\ \Omega$. The control system is composed of a main board featuring a digital signal processor (DSP) and an auxiliary board equipped with a field programmable gate array (FPGA). Such boards may be noticed on top in the picture of fig. 2.10, showing the prototype SAF except the a.c. side inductors. The DSP board, equipped with a $TMS320C6713$ device clocked at 225 MHz, is used to handle all high-level computational-intensive and not strictly time-sensitive tasks:

- real-time calculations required by the implemented loop control algorithms;
- determination of the required inverter state sequence (legs state and related time duration) based on the implemented modulation technique;
- management of communication with a host PC permitting to directly download software and to provide the operator with full acquired data concerning both internal variables and signals digitalized by means of A/D converters.

The FPGA board, equipped with a $ProASIC\ 3\ A3P400$ device clocked at 50 MHz, carries out the most time-sensitive low-level tasks:

- generation of proper gate drive signals for the 6 IGBTs including dead time management, basing on the leg-state commands provided by the DSP,
- management of safe switch-off procedures in case of overcurrent or overvoltage alarms or failures;
- management of the Analog to Digital converters (ADC) cycle, forwarding the acquired data to the DSP.

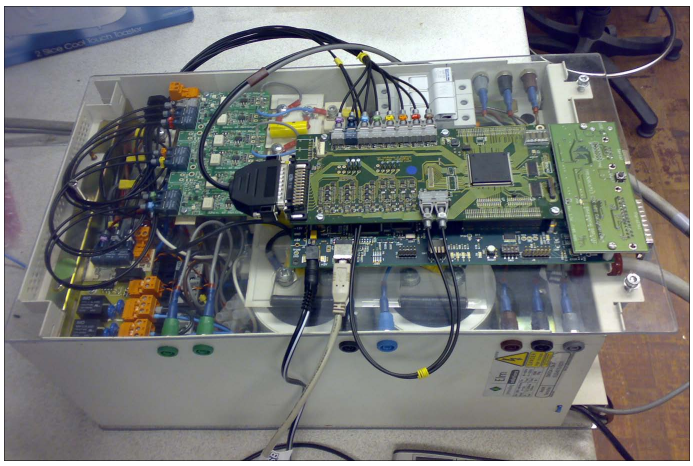


Figure 2.10: Top view of the experimental SAF prototype

2.7 Validation of the Control Method in Standard Industrial Applications

The efficacy of the proposed new controller is demonstrated by employing the active filter to compensate the harmonic currents drawn by an uncontrolled diode rectifier load as shown in fig. 2.11. At first the experimental tests were carried out in order to verify the behaviour of the overall control algorithm for standard industrial applications. In particular for the purpose of experimental validation reduced scale experimental tests were performed under the following operating conditions:

- fixed fundamental frequency: 50 Hz
- line to neutral voltage: 100 Vrms
- d.c. link voltage: 300 V
- non linear load: 3-phase diodes rectifier bridge supplying a 15 Ω and equipped with an input filter constituted by 3 series inductors featuring $L = 1$ mH
- sampling frequency 20 kHz switching frequency 10 kHz
- modulation technique: asymmetric SVM

The supply voltage was provided by a 12 kVA dedicated controlled static generator (*Chroma* 61705) exhibiting high stability and a very low equivalent output impedance. The implemented control algorithm operates at fixed sampling frequency $fs = 20$ kHz while the switching frequency of the inverter is $fsw = 10$ kHz in asymmetric SVM mode. This results in a number of samples per fundamental

period $n = 20kHz/50Hz = 400$. The phase voltage and current, the ASF current and the load current were recorded on an oscilloscope and related supply and load current harmonics were calculated by a post processing analysis performed using Matlab. The upper trace of fig. 2.11 shows that the supply current is significantly less distorted than the load current and in phase with the supply voltage. The results of the Fast Fourier Transform (FFT) analysis for the load and supply currents prove a significant reduction of the most dominant low order harmonics as shown in fig. 2.12. The Total Harmonic Distortion (THD) of the load current was 27% while the supply currents THD was only 3.7% when the proposed ASF was employed. To demonstrate the current loop reference tracking performance of the proposed ASF, the comparison between the ASF current and its reference is shown in fig. 2.13 confirming excellent results.

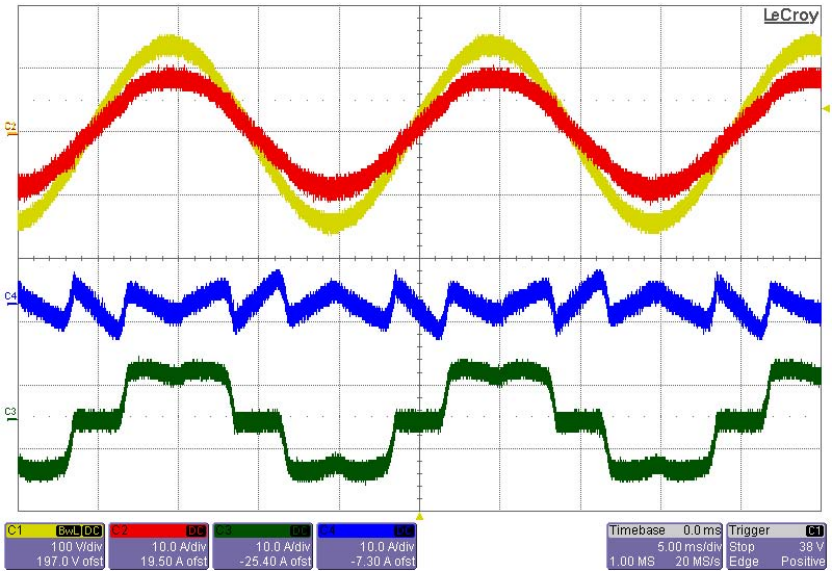


Figure 2.11: Measured steady-state data for a system phase: mains current (red) and voltage (yellow), SAF current (blue) and non-linear load current (green)

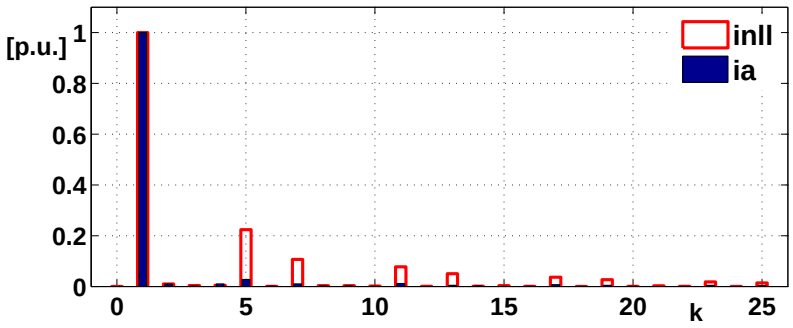


Figure 2.12: Harmonic spectrum: non-linear load (red) vs. mains (blue) current

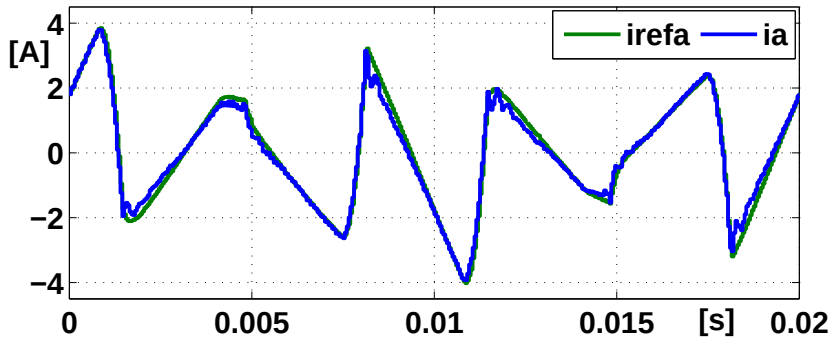


Figure 2.13: ASF actual and reference currents

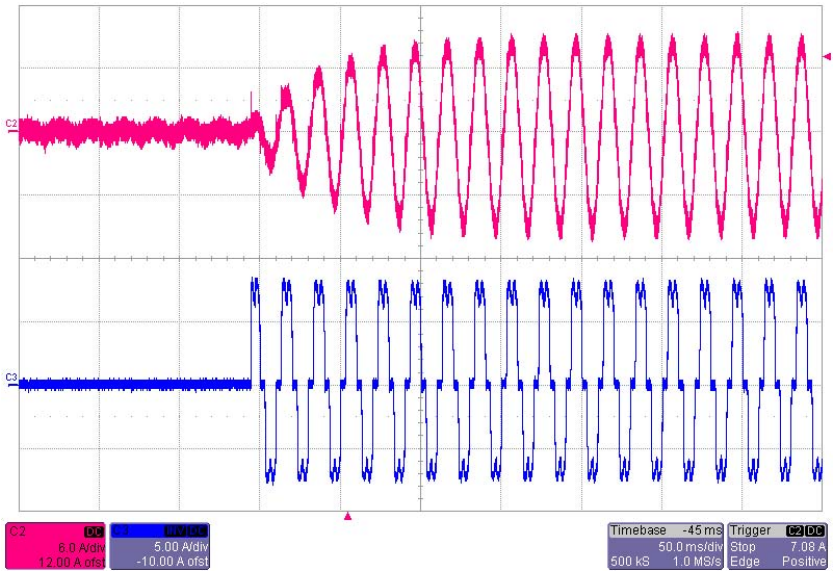


Figure 2.14: Experimental results for load turn-on; supply and non linear load current

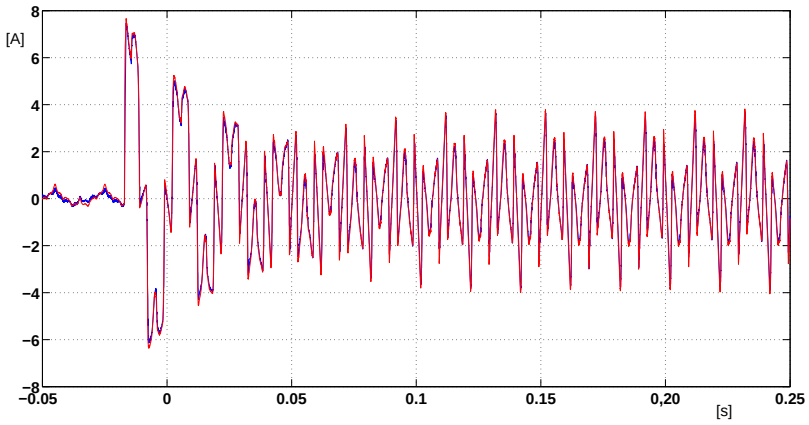


Figure 2.15: Comparison between the actual and the reference shunt active filter current during a load turn-on

To verify the transient behaviour of the proposed method, a turn-on transient of the uncontrolled rectifier load was tested. As shown in fig. 2.14 the transient takes around 5 line periods which is dominated by the PI dc-link voltage controller. However, an excellent transient behaviour of the proposed current control method is shown in fig. 2.15. To further validate the proposed method the conventional deadbeat current controller was implemented on the same ASF and the results are shown in fig. 2.16, 2.17. The results were compared with the ones obtained by means of the proposed predictive current control (fig. 2.18, 2.19) for the same experimental setup as above but in this case no input inductance was connected at the input of the diode-rectifier. The THD of the supply current was 15% when the conventional current controller was employed reducing to only 4% when the proposed controller was employed instead. The THD of the load current was 30% for this test.

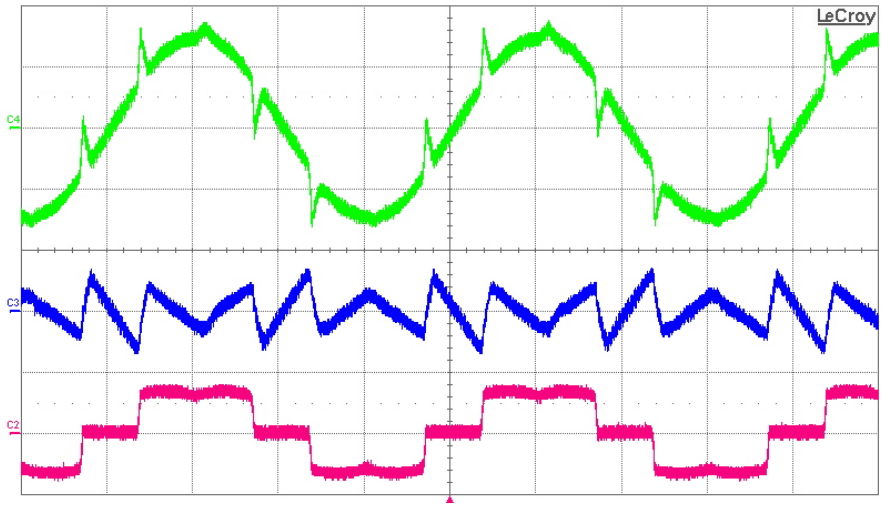


Figure 2.16: Deadbeat Control: measured steady-state data for a system phase

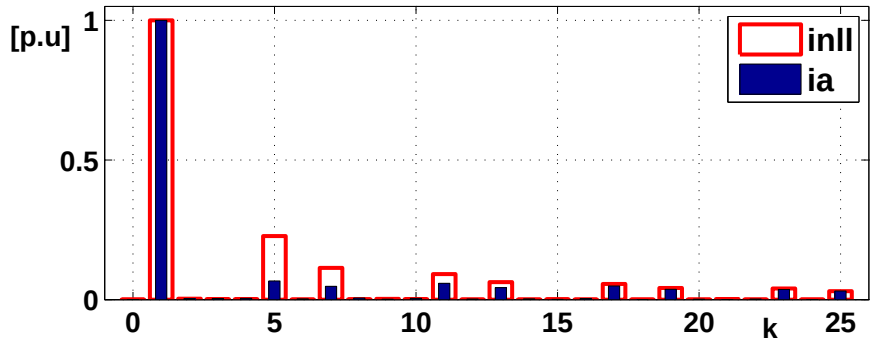


Figure 2.17: Harmonic spectrum: non-linear load (red) vs. mains (blue) current

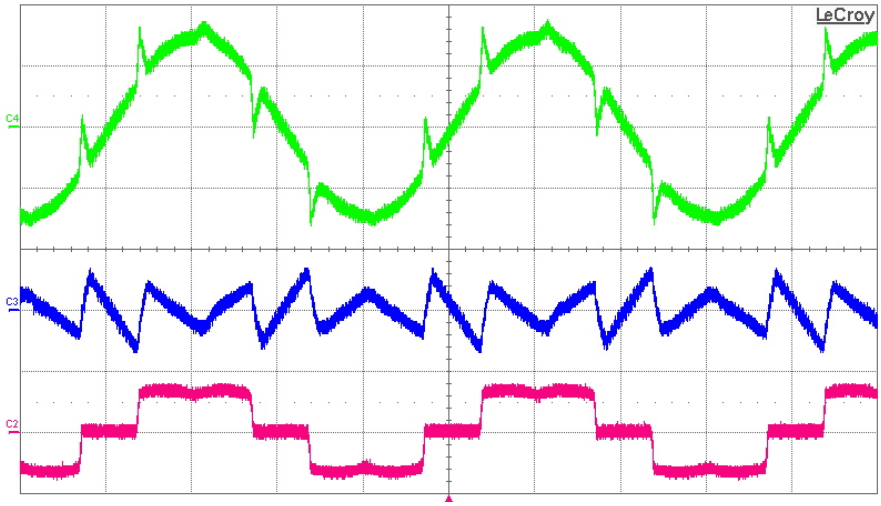


Figure 2.18: Predictive Control: measured steady-state data for a system phase

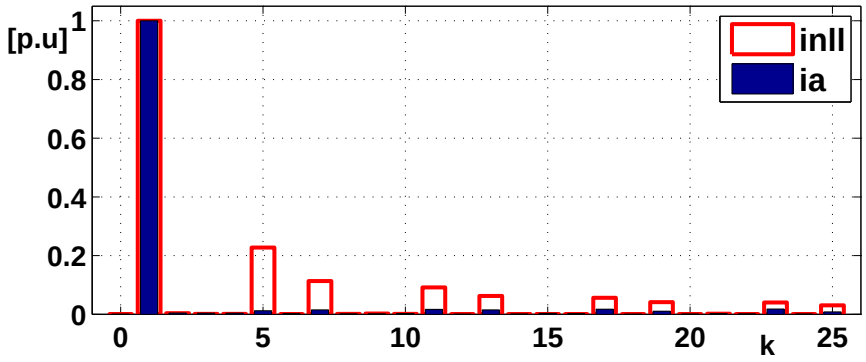


Figure 2.19: Harmonic spectrum: non-linear load (red) vs. mains (blue) current

2.8 Validation of the Control Method in Aerospace Applications

In order to verify the behaviour of the overall control scheme applied to standard aerospace applications hereafter several simulation results obtained using a purposely developed simulation model and experimental tests are reported and commented referring to the following operating conditions:

- fixed fundamental frequency: 400 Hz
- line to neutral voltage: 115 Vrms
- d.c. link voltage: 500 V
- non linear load: 3-phase diodes rectifier bridge supplying a 15 Ω and equipped with an input filter constituted by 3 series inductors featuring $L = 1$ mH

- sampling frequency 26 kHz switching frequency 13 kHz

- modulation technique: asymmetric SVM

2.8.1 Simulation Analysis

Aiming to achieve a preliminarily estimation of the actual performances that may be expected from the designed SAF using the control strategy previously described in standard aerospace applications, a simulation model was first purposely developed in the Matlab-Simulink® environment describing the core of the system, i.e. the power parts and the current control loop. In fact, the compensation performances of the SAF, which are significantly evaluated at steady-state, depend mainly on inner current loops when the d.c. bus capacitors feature a sufficiently large capacitance. Therefore, the voltage control loop was not modeled, assuming that the voltage of the SAF d.c. bus remains constantly equal to its design value. To permit a more realistic evaluation permitting a close correlation with the planned experimental tests described in section 2.8.2, the developed model was conceived to receive as external inputs the actual waveforms of the PCC voltages and of the currents drawn by the non-linear load. The above voltage and current signals were acquired and recorded by means of a digital scope (500 MHz LeCroy 6050) during actual operation of the experimental rig. In the considered operative conditions, as expected the currents drawn by the non-linear load result rather distorted: this is highlighted by the waveform depicted in fig. 2.20 and confirmed by the related p.u. spectrum reported in fig. 2.21, where large 5,7,11,13 harmonics may be noticed determining a high total harmonic distortion $THD > 18\%$. The significant improvement achieved by means of the SAF in terms of waveform distortion is highlighted in fig. 2.22, where the load and mains currents are compared (e.g. respectively red and blue waveforms referred to the same phase). Such result is confirmed also in terms of harmonic content by comparing fig. 2.21 with the spectrum of the mains current reported in fig. 2.23: for example, thanks to the SAF the amplitude of 5^{th} harmonic is reduced from 16.2% to 0.9% vs. the fundamental component, whereas a much lower distortion $THD < 3\%$ is globally achieved. Moreover, fig. 2.22 shows that the fundamental component of the mains current waveform is phase-shifted ahead with respect to the corresponding load current component. As highlighted in fig. 2.24, the mains currents result indeed almost in phase with the corresponding PCC voltages, thus proving that most of reactive fundamental component of load currents is also compensated by the SAF, as expected.

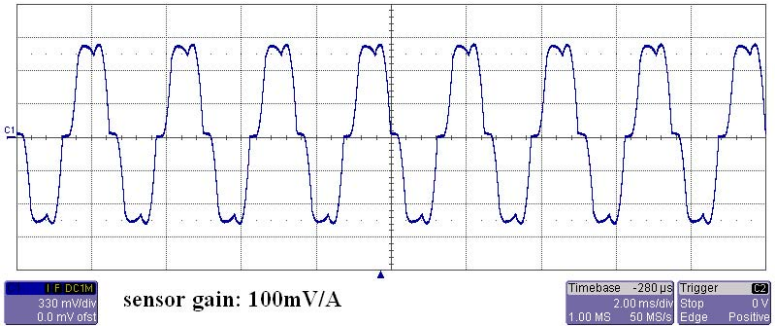


Figure 2.20: Measured waveform of non-linear load current

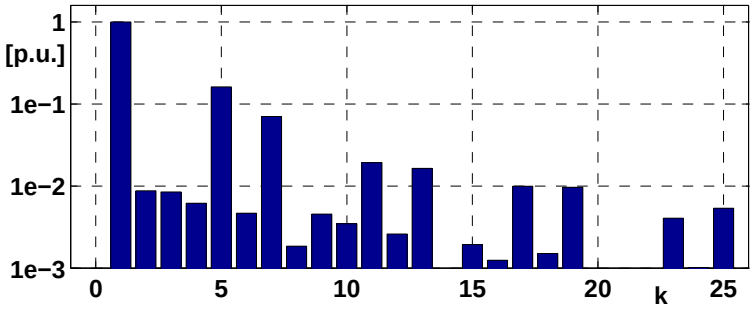


Figure 2.21: Spectrum of measured non-linear load current

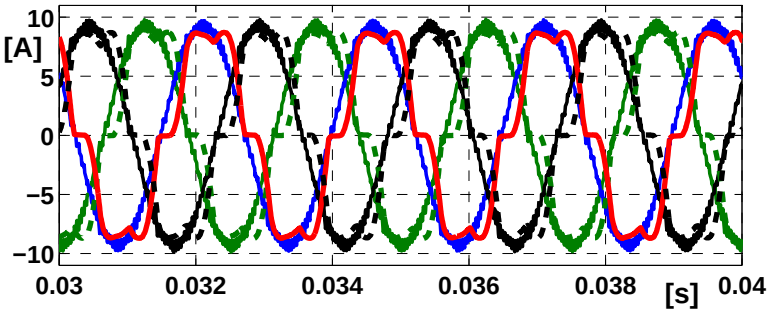


Figure 2.22: Simulated mains currents vs. measured load currents (dashed)

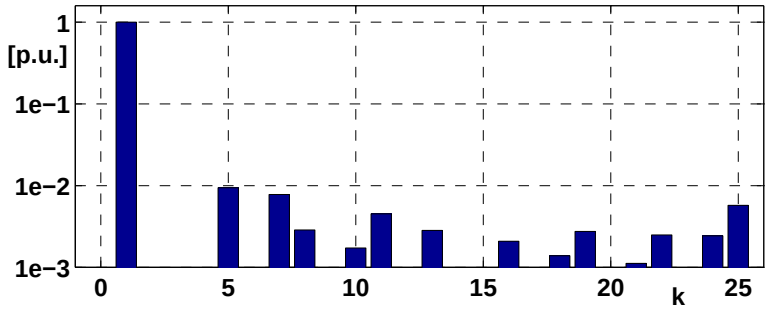


Figure 2.23: Simulated mains currents spectrum

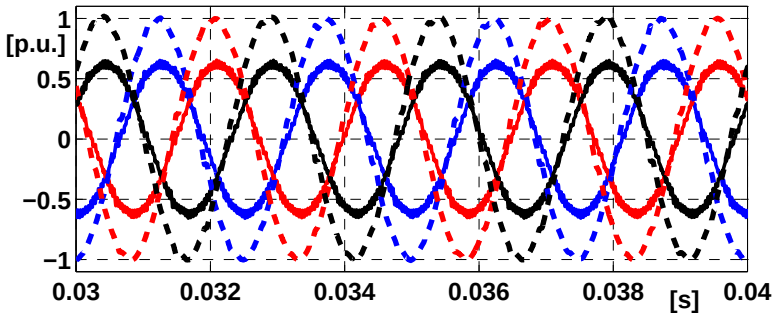


Figure 2.24: Simulated mains currents vs. measured mains voltages (dashed)

2.8.2 Experimental Tests

Several experimental tests were carried out using the SAF prototype and the non-linear load previously described under the recalled standard supply conditions ensured by the dedicated supply system above mentioned. The waveforms of several electric quantities were acquired by means of a high quality digital scope during actual operation of the system, whereas spectral data were obtained by numerical post-elaboration. Further significant info was also recorded by means of an acquisition system embedded in the DSP board, which directly transfers data to a connected host PC. Such data concern both internal signals of the control system and physical quantities sensed from the SAF sensors and acquired by means of A/D converters operating synchronously with elaboration tasks at frequency f_s. As expected, significant improvements were actually achieved in terms of harmonic pollution thanks to the SAF. For example, when the load draws the distorted current reported in fig. 2.20 the mains currents waveform shown in fig. 2.25 was obtained, resulting quasi sinusoidal with a fairly limited superimposed high-frequency ripple mainly due to inverter commutation. The achieved benefits were also confirmed in spectral terms by comparing the mains current spectrum reported in fig. 2.26 and the load current spectrum shown in fig. 2.21, whose lower portions are superimposed for convenience in fig. 2.27; in fact, the smaller amplitude of major low-order harmonics permits to achieve a $THD < 6\%$. The overall behavior of the tested system in the considered conditions is summarized in fig. 2.28, where the waveforms of non-linear load current, SAF current, supply current and mains voltage are reported for one of the phases. The superimposed plot of mains voltage and current highlights the almost null phase displacement that was actually achieved between them. In fig. 2.30 the trend of the reference current signal and of the related two-steps-ahead prediction are compared, highlighting the good performances of the adopted prediction algorithm previously described. A comparison between the reference and actual waveforms

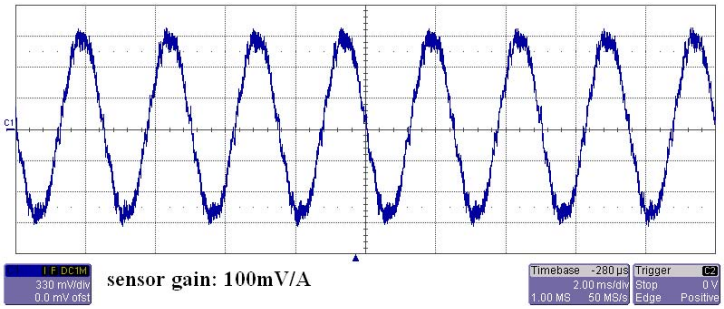


Figure 2.25: Measured waveform of mains current

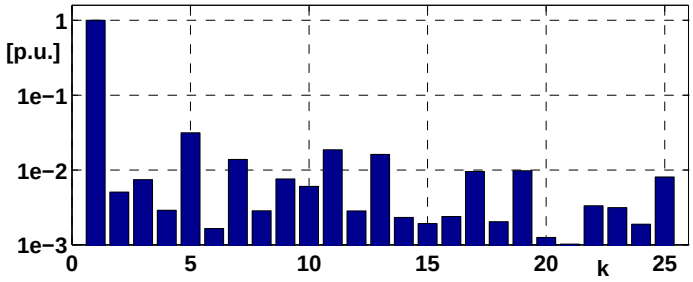


Figure 2.26: Spectrum of measured mains current

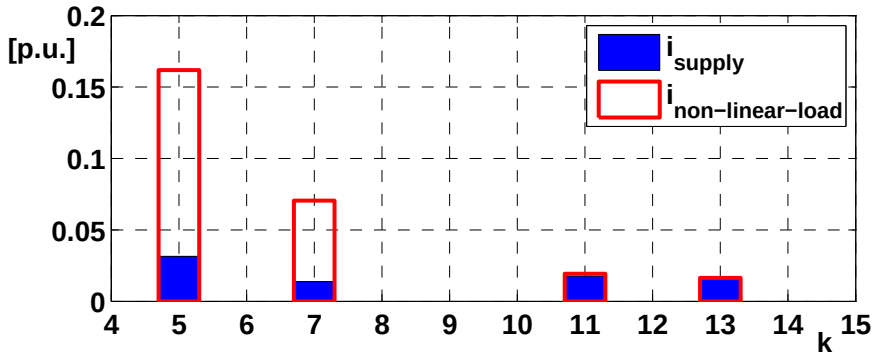


Figure 2.27: Harmonic spectrum of the measured non-linear load current (red) and mains current (blue)

of one of the currents drawn by the SAF is finally reported in fig. 2.31, highlighting a rather good overall current tracking capability although small mismatches may be noticed due to the strong distortion of the load current waveform to be compensated. The transient behavior of the proposed control system was also checked: for example, a step-down change of the rectifier load was achieved by increasing the resistance up to 150% of the rated value. The waveforms of mains voltage, mains current and load current measured for one of the phases during such transient are reported in fig. 2.32: it may be noticed that the SAF takes about 7 fundamental periods to settle after the transient, as dictated by the dynamics of

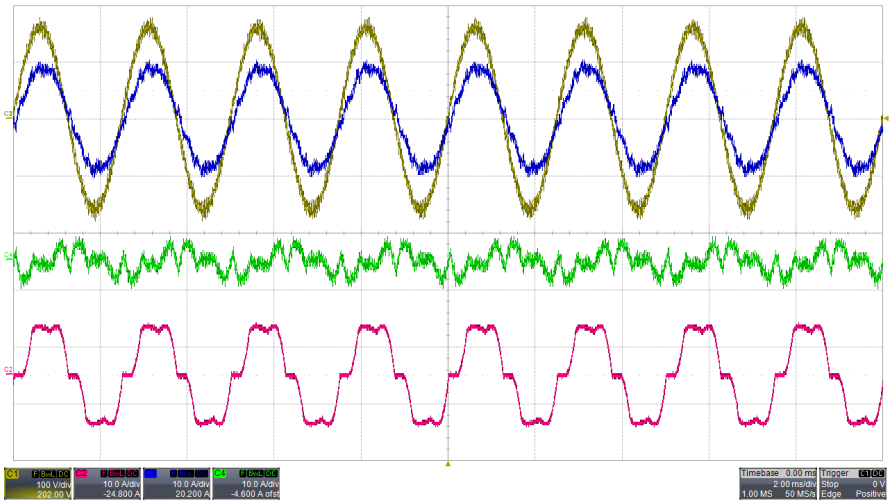


Figure 2.28: Measured steady-state data for a system phase: mains current (blue) and voltage (yellow), SAF current (green) and non-linear load current (red)

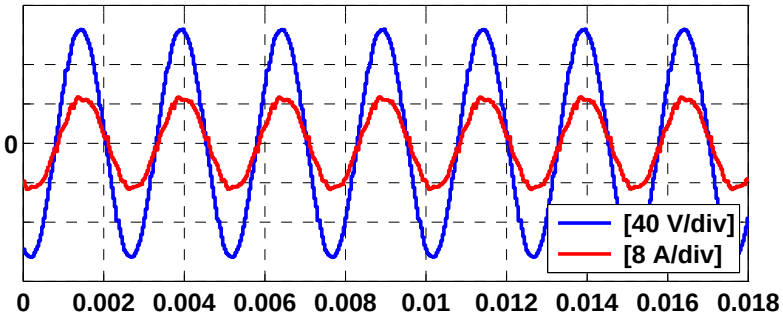


Figure 2.29: Acquired data: phase current (red) vs. mains phase voltage (blue)

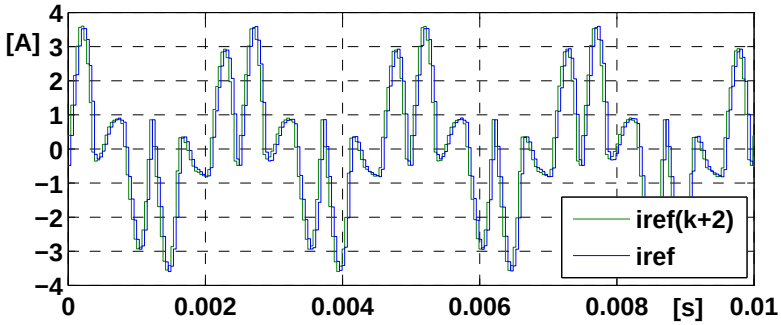


Figure 2.30: Acquired data: reference current vs. related prediction

the DC bus voltage control. The reference and actual current waveforms referred to a SAF phase across the load step instant are reported in fig. 2.33, as obtained by the embedded data acquisition system. It may be noticed that also in this case the system exhibits a rather good tracking capability, although discrepancies may be noticed especially during the first fundamental period after the load step.

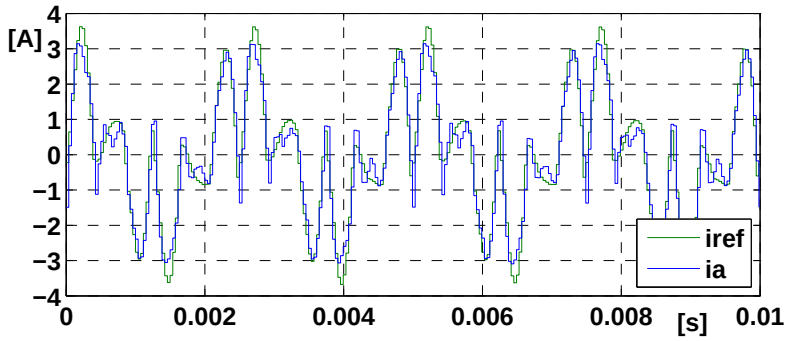


Figure 2.31: Acquired data: reference vs. actual inverter leg current

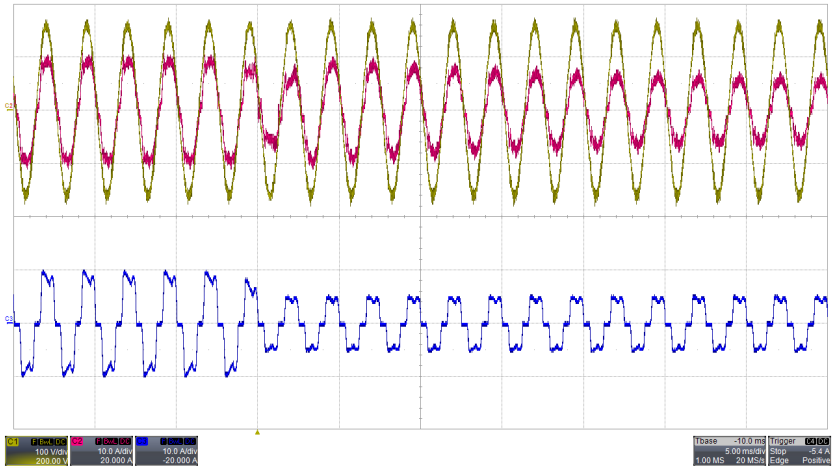


Figure 2.32: Measured transient data for a system phase: mains current (red), mains voltage (yellow) and non-linear load current (blue)

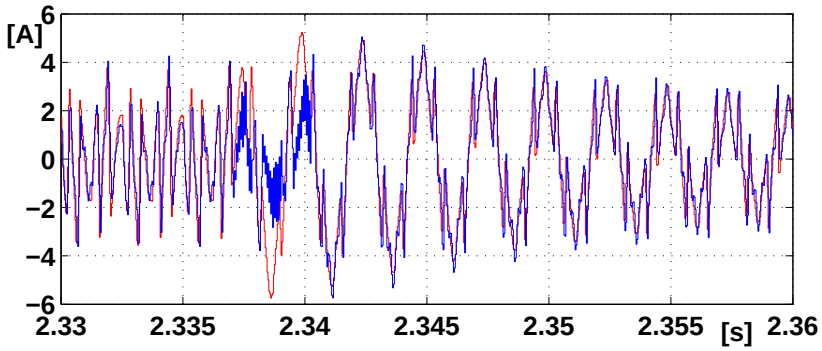


Figure 2.33: Acquired data: phase current (red) vs. mains phase voltage (blue)

Considering the unfavorable conditions due to the high fundamental frequency, forcing to use a rather low number of commutations per period, in overall terms the power quality improvement achieved by means of the examined SAF results rather good, basically confirming the theoretical expectations and the validity of the proposed solution.

2.9 Conclusions

In this chapter one-sample-period-ahead predictive current control algorithm designed specifically for active power filter applications was investigated. In particular the control algorithm was proposed as able to compensate for load harmonics on both industrial and aerospace applications where accurate current tracking at high frequencies is required. The growing use of power loads supplied by means of converters in fact poses more and more serious power quality issues on board of modern aircrafts, as the limited size of the on-board mains makes it prone to harmonic pollution problems. After a short overview of different solutions available in the literature, an improved dead-beat control strategy suitable for digital implementation was proposed, employing different predictors to anticipate the values expected for various quantities. In particular, the use of a repetitive predictor leveraging on the periodicity of signals at steady-state was proposed, adopting an hysteretic logic to detect the insurgency of transients to switch to a faster response mode aiming to avoid the inherent 1-period delay. A first SAF prototype implementing the proposed solution was then described, finally reporting and commenting several results coming both from simulations and from experimental tests concerning both steady-state and transient conditions. In overall terms, such promising results confirmed the theoretical expectations and validate the proposed solution.

Chapter 3

Real-Time Control of a Multilevel Active Filter

3.1 Introduction

Thanks to their better performances, multilevel voltage source converters represent a promising evolution of standard topologies and are becoming more and more popular especially for large-power applications. The general idea behind multilevel converters consists in approximating a generic voltage waveform using a number of voltage levels larger than usual, obtained by means of several distinct voltage sources typically constituted by capacitors. Despite the more complex structure compared to conventional converter topologies, they may provide the following benefits: higher voltage capability, lower voltage rating of power devices, improved harmonic spectrum and better EMI performances. They were initially considered in the technical literature to overcome the issues related to the voltage limits of semiconductor devices; thanks to their features, they were then successfully proposed and applied in both grid-side and machine-side medium voltage applications. The main multilevel topologies may be classified into the following categories: *diode clamped*, *capacitor clamped or flying capacitors*, *cascaded multi-cell structure*; other hybrid variants were also proposed basing on the previous topologies. For example, flying capacitor and neutral point diode clamped (NPC) converters were proposed as alternative to conventional converters for high voltage direct current applications in [27] and [28]. On the other hand, in [29] several multi level topologies were considered for industrial medium-voltage drives. Finally, the solution of multilevel converters was also considered even for compensation of load harmonics in power distribution systems. For example, in order to produce multilevel pulsewidth modulated waveforms and achieve then higher power quality levels, a neutral point diode clamped converter was used in [30] as

active power filter. Hereafter at first, in order to highlight the main advantages of each structure, a brief overview of the main topologies is provided especially focusing on the *multilevel cascaded converter* that was further investigated in this work. The main modulation techniques available in the technical literature for multilevel converters are then shortly recalled and described. The application of a modified deadbeat control to a cascaded H-bridge multilevel structure used as active filter for compensation of harmonics in aircraft power systems is finally considered, evaluating the possibility to apply a modified modulation algorithm purposely developed. Several experimental results obtained by means of a prototype system purposely developed are reported and commented. In particular, the possibility to obtain a good power quality level using a rather low ratio between switching frequency and fundamental frequency was investigated, especially referring to aerospace applications where the high mains frequency (typically ≥ 400 Hz) may constitute a serious challenge for conventional methods.

3.2 Diode Clamped Converter

Among the multilevel topologies, one of the most popular and diffused solutions consists in the diode-clamped converter. In this configuration, the converter is typically supplied by an even number n of string-connected voltage sources, usually constituted by capacitors intended to be operated at about constant equal voltage. Each inverter leg is composed of a set of $2 \cdot n$ string-connected switching cells (each one constituted in turn of a switching device, e.g. IGBT, and an anti-parallel free-wheeling diode). The terminal taps of the string are connected to the terminal taps of the sources string. A string of n clamping diodes is also connected in anti-parallel across each of the $n-1$ sub-strings composed of n intermediate switching cells. Using the number k of cells located below each sub-string to identify the latter, the intermediate k^{th} tap of the related clamping diodes string, also counted from the bottom, is connected to the corresponding k^{th} intermediate tap of the sources string. Finally, the middle tap of the cells string constitutes the output terminal of the leg. The number of cells N_C and clamping diodes N_D required per each leg results then

$$\begin{cases} N_C = 2 \cdot n \\ N_D = n \cdot (n-1) \end{cases} \tag{3.1}$$

In such a converter, the permitted states of each leg consist in any of the $n+1$ combinations such that a set of n consecutive cells is closed whereas the other ones are open. The output terminal may be then connected either to the upper or lower terminals of the voltage sources string, or to any of its intermediate nodes,

thus permitting to obtain a number of distinct output voltage values equal to $n+1$ which are usually evenly spaced. In any of such conditions, a wise design permits to limit the voltage stress in each device to the individual rated voltage of the sources, whereas the current stress equal the output leg current. The simplest implementation of such structure consists in the well known *3-levels neutral point clamped* (NPC) whose electrical scheme is shown in fig. 3.1 for 1 leg, while a more complex example of five levels diode clamped converter is reported in fig. 3.2 also showing only 1 leg.

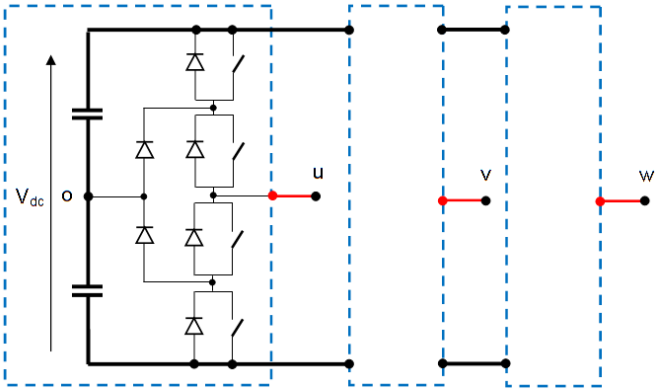


Figure 3.1: Neutral point clamped converter

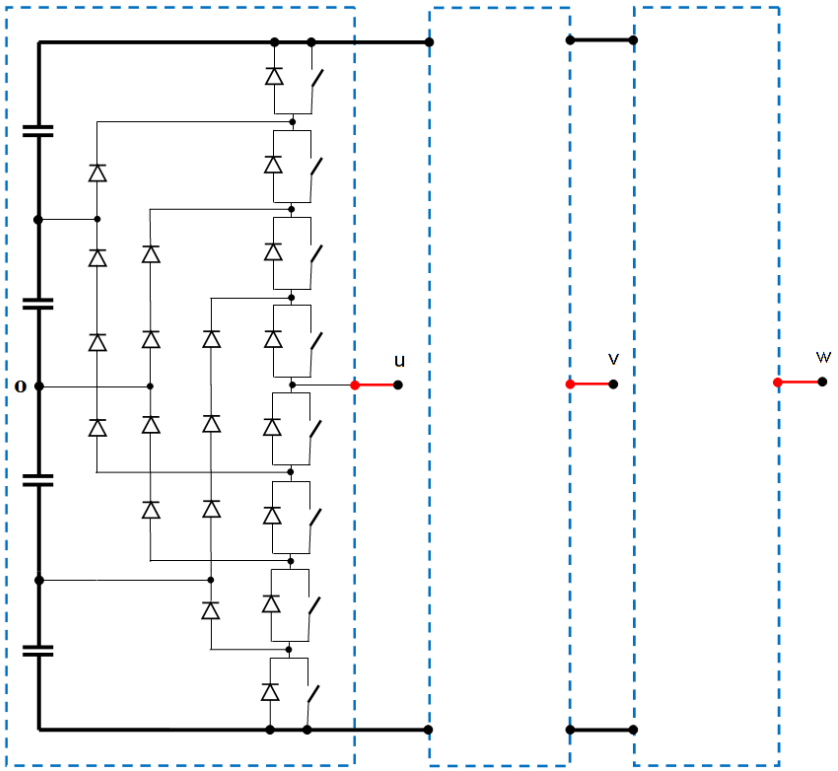


Figure 3.2: Five level diode clamped and flying capacitors structure

As in this converter no insulated d.c. sources are required, it can be applied more easily with respect to other configurations. On the other hand, when capacitors are used to provide the intermediate voltage levels under an actually simple bipolar d.c. supply, or when the latter is actually absent as in active filters, a major challenge posed by this converter topology consists in keeping balanced the capacitors voltages: in fact, this may require complicated algorithms especially for rather large numbers of levels. In practice, it is clear that the implementation of diode clamped structure becomes fairly complex when the number of levels increases making this solution feasible only for limited number of output voltage levels. A theoretical analysis of the converter may be undertaken assuming an ideal behavior for the switching cells and diodes composing the inverter legs, obviously taking into account that only the mentioned states are allowed. To represent the instantaneous state of each switching cell, a simple numbering beginning from 1 at the bottom of the leg may be introduced to single out them and a corresponding *switching state function* S_k may be then introduced:

$$S_k = 1, 0 \qquad k = 1, 2, ..., 2 \cdot n. \tag{3.2}$$

By associating the +1 value to the close-switch-status condition and the 0 value to the complementary state, the $n + 1$ different permissible conditions lead to an equal number of possible values of the output voltage V_{uo} referred to the center tap of the voltage sources string, without any redundancy. For instance, indicating with V_{dc} the total voltage of the dc sources, the possible switching configurations and the related output voltages are reported in tab. 3.1 and 3.2 for the cases $n = 2, 4$ respectively. In general terms, for a converter featuring n equal sources the following different output voltages referred to the central tap of the d.c. link are obtained:

$$V_{uo} = \pm j \cdot \frac{V_{dc}}{n} \qquad j = 0...n/2. \tag{3.3}$$

For a 3-phase structure the number of permitted converter states results then $N_{states} = (n + 1)^3$, thus introducing a wider control flexibility compared to a common single-source inverter that may be used to study and consider different modulation techniques.

Table 3.1: Relationships between switches state and output voltage - three levels

S_1	S_2	S_3	S_4	V_{uo}
1	1	0	0	$V_{dc}/2$
0	1	1	0	0
0	0	1	1	$-V_{dc}/2$

Table 3.2: Relationships between switches state and output voltage - five levels

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	V_{uo}
1	1	1	1	0	0	0	0	$V_{dc}/2$
0	1	1	1	1	0	0	0	$V_{dc}/4$
0	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	$-V_{dc}/4$
0	0	0	0	1	1	1	1	$-V_{dc}/2$

3.3 Flying Capacitor Multilevel Converter

The *flying capacitors* topology, also named *capacitor clamped*, resembles the diode clamped structure above described, where the clamping diodes strings are replaced by capacitors performing a somewhat analogous function yet without any connection to the main voltage source, which may then typically keep a simple bipolar structure. For the sake of brevity, only a 3-levels structure is reported here as example in fig. 3.3 ; nevertheless, as in the previous case it is easy to generalize the scheme to a n-level topology. In this case, performing an analogous analysis

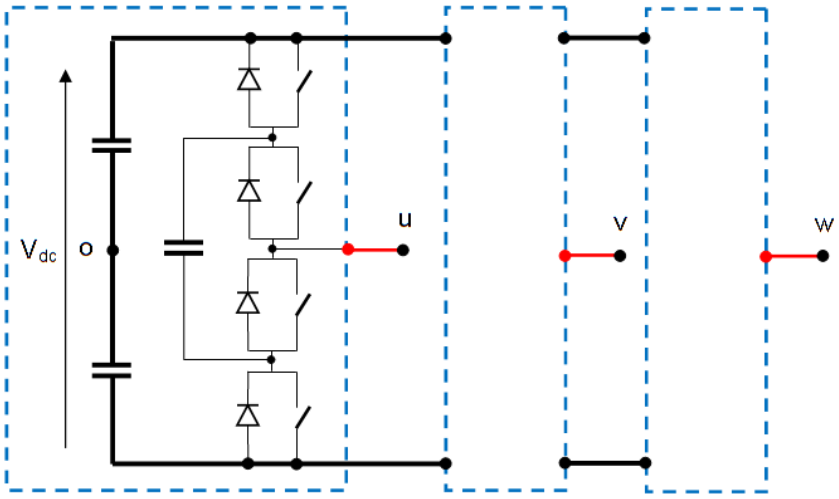


Figure 3.3: Three levels flying capacitor structure

as before, it may be noticed that there are more permissible switching configurations than output levels. In fact, this topology presents intra-phase switching redundancy, which can be ultimately exploited to keep the voltages of the flying capacitors at their reference values. For example, in the structure reported in fig. 3.3 the reference voltage of the 3 capacitors is typically the same, and under such condition a null output voltage with respect to the center tap of d.c. bus may be generated in 2 ways, i.e. by closing either the first and third cell from

the top, or the second and fourth ones. Anyway, the load current will flow in opposite directions in the flying capacitor in the 2 above cases, thus charging or discharging it respectively. Unfortunately, both the power structure and the control scheme become more and more complex when the number of voltage levels increases, making this solution rather difficult to design and prototype. In practice, even if this structure was extensively studied in the technical literature, it achieved a very limited practical diffusion mostly due to the large number of bulky clamping capacitors and complex pre-charge circuit required, not mentioning the control difficulties also due to the typical large dispersion and variability of the characteristics of capacitors. to the large number of bulky clamping capacitors and complex pre-charge circuit required.

3.4 Multilevel Cascaded Converter

In the multilevel cascaded topology, each phase of the converter is composed of a set of H-bridge VSI inverters (fig. 3.4), whose a.c. sides are connected in series whereas the d.c. sides are connected to independent voltage sources, often consisting in insulated capacitors. Typically, 3 of such phases are then connected in Y configuration to constitute a complete 3-phase converter: for example, in fig. 3.5 the scheme of a topology involving 2 H-bridges per phase is reported. Such solution features several advantages with respect to the other topologies above described especially in terms of modularity, simplicity and number of switching devices vs. number of achievable output voltage levels. In fact, per each phase the output voltage is simply generated as the sum of the output voltages of each related H-bridge. When the d.c. sources feature the same voltage, as usual, this means that to generate any odd number n of output voltage levels the following number of H-bridges (N_{HB}) and switching devices (N_{SW}) are required:

$$\begin{cases} N_{HB} = (n-1)/2 \\ N_{SW} = 2 \cdot (n-1) \end{cases} \tag{3.4}$$

Comparing these relations with the ones obtained for diode clamped converter (eq. 3.1) the reduction of the number of required switching devices appears evident, especially when the number of levels increases. As an example, for $n = 5$ the series of two H-bridges and eight switching devices need to be used, as shown in the scheme depicted in fig. 3.5.

A theoretical analysis of the converter may be undertaken by considering for simplicity a single H-bridge module as reported in fig. 3.4. As usual, an ideal behaviour may be assumed as a first approximation for the switching cells composing

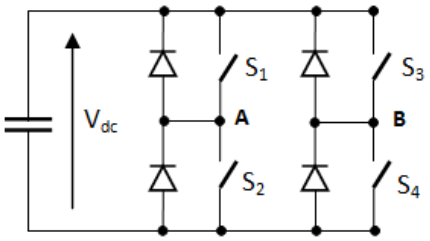


Figure 3.4: Single H-bridge module

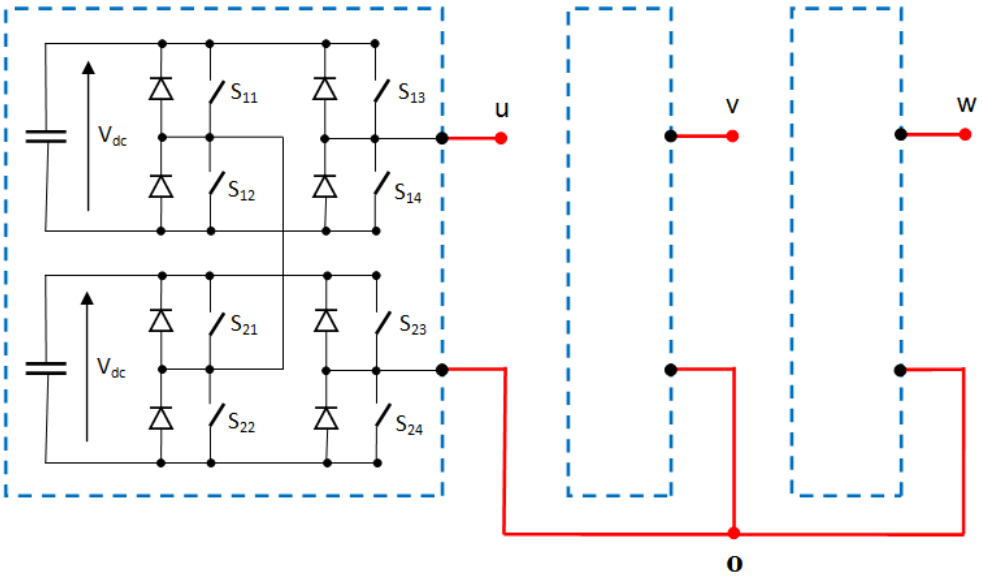


Figure 3.5: Five levels inverter

the converter legs. Introducing the *switching state function* S_k to represent the instantaneous state of each H-bridge switch

$$S_k = 1, 0 \qquad k = 1, 2, 3, 4 \tag{3.5}$$

by associating the $+1$ value to the closed-switch-status condition and the 0 value to the complementary open state, the associated possible output voltages V_{AB} result: V_{dc}, $-V_{dc}$ and 0 as reported in tab. 3.3. In particular there are two different switching configurations leading to a null output voltage determining, as in

Table 3.3: Relationships between switches state and output voltages

S_1	S_2	S_3	S_4	V_{AB}
0	1	1	0	$-V_{dc}$
1	0	1	0	0
0	1	0	1	0
1	0	0	1	V_{dc}

the flying capacitor structure, an intra-phase redundancy which can be properly exploited in the control strategy, e.g. for evenly distributing switching losses. By connecting in series two such H-bridge units it becomes possible to generate two further voltage levels, namely $2V_{dc}$, $-2V_{dc}$ as explained in tab. 3.4. Moreover, some

Table 3.4: Relationships between switches state and output voltages

S_{11}	S_{12}	S_{13}	S_{14}	S_{21}	S_{22}	S_{23}	S_{24}	V_{uo}
0	1	1	0	0	1	1	0	0
1	0	1	0	1	0	1	0	0
0	1	0	1	0	1	0	1	0
1	0	0	1	1	0	0	1	0
0	1	1	0	1	0	1	0	V_{dc}
0	1	1	0	0	1	0	1	V_{dc}
1	0	1	0	1	0	0	1	V_{dc}
0	1	0	1	1	0	0	1	V_{dc}
1	0	0	1	1	0	1	0	$-V_{dc}$
1	0	0	1	0	1	0	1	$-V_{dc}$
1	0	1	0	0	1	1	0	$-V_{dc}$
0	1	0	1	0	1	1	0	$-V_{dc}$
0	1	1	0	1	0	0	1	$2V_{dc}$
1	0	0	1	0	1	1	0	$-2V_{dc}$

further intra-phase redundancy is achieved for what concerns the generation of the intermediate voltage levels, which may be exploited to properly divide the power to be delivered to the load among the d.c. sources, e.g. to keep balanced their voltages when only isolated capacitors are used, as in active filters. Analogously, connecting in series further H-bridge units permits to generate 2 additional voltage levels per each unit included. Therefore, by employing a generic number N_{HB} of H-bridges featuring the same d.c. supply voltage a number $2N_{HB}+1$ of evenly distributed voltage values may be generated by the equivalent converter leg:

$$V_{uo} = \pm j \cdot V_{dc} \qquad j = 0...(n-1)/2. \tag{3.6}$$

The phase-shifted pulse width modulation is commonly used to control a multilevel cascaded converter topology, as it may provide an optimized harmonic spectrum for the output voltage by using suitably phase-shifted carrier signals for the different H-bridge units in one phase. For example, if in a 5-level topology as shown in fig. 3.5, the carriers of the 2 H-bridges are phase shifted exactly by one quarter of a switching period, then an additional harmonic cancelation effect may be achieved.

3.5 Modulation Strategy

Several different modulation techniques for multilevel converters have been studied and analysed in the technical literature. In fact, the possibility to approximate a reference waveform using several different voltage levels may lead to interesting improvements by paving the way of modulation strategies based on innovative solutions. Anyway it is worth notice that all the modulation strategies used for standard 2-level converters can be easily adapted even to multilevel structures. Actually the most used modulation methods for multilevel converters may be classified as *low switching frequency* or *high switching frequency* techniques.

The first family of modulation techniques operates a spectral approximation of the reference waveform adopting a "*global*" approach; i.e. using a relatively limited number of commutations of switching devices per fundamental period: it includes methods such as *selective harmonic elimination* and *space vector control* (SVC). As an example of selective harmonic elimination method fig. 3.6 represents a possible output staircase waveform referring in particular to a 7-levels waveform. Once

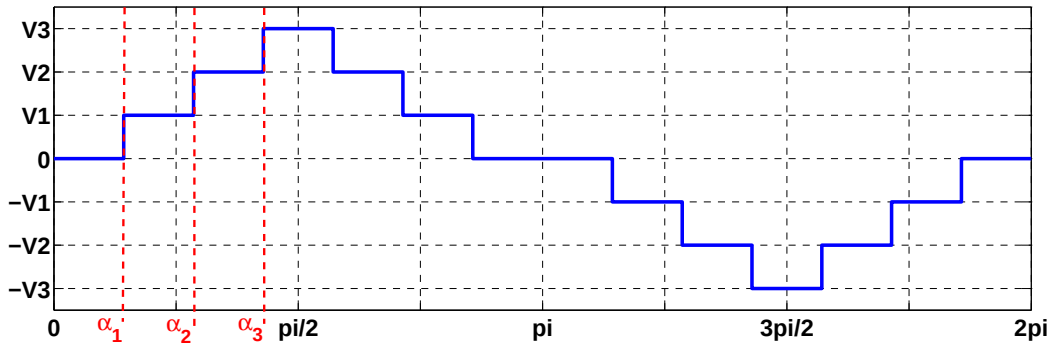


Figure 3.6: Output waveform of a 7-levels selective harmonic elimination

the shape of the staircase waveform is chosen, for example assuming alternativity and odd-symmetry about the origin, for a generic n levels converter the Fourier coefficients result expressed as:

$$V_m = \frac{4}{\pi \cdot m} \sum_{k=1}^{N} V_k \cos\left(m \cdot \alpha_k\right) \tag{3.7}$$

where V_k is the k^{th} level of dc voltage, m is an odd harmonic order, N is the number of switching angles, and α_k is the k^{th} switching angle in the first quarter of period $\left[0 \quad \pi/2\right]$. Therefore, the switching angles may be purposely calculated in order to achieve the elimination of selected harmonics or the minimization of a related quality index by means of an optimization procedure, while also usually controlling the amplitude of the fundamental component.

The high switching frequency methods operate applying a "*local*" spectral approximation approach and thus using a relatively high number of commutations per fundamental period. In fact, in most cases they are conceptually meant to produce, inside small consecutive fixed time intervals Δt, an average output voltage that is proportional to a given reference signal, typically provided by some external control loop. For poly-phase converters, especially 3-phase, they may be further classified as *space vector modulation* methods (SVM) or *pulse width modulation* methods (PWM) depending as usual on the fact if the 3-phase converter is considered as a whole or if each phase is controlled as an independent entity. The most popular SVM methodology, referred to 3-phase inverters, consists in generating a sequence of converter states such that the average value of the d-q components of the output voltages, calculated according to Park transformation, approximately equals the corresponding values of the related reference signals inside consecutive time intervals featuring a duration Δt smaller enough with respect to the the fundamental period. The most common implementation of such approach consists then in the following operations:

- in the Clark plane, identification of the 3 adjacent vectors corresponding to permissible converter states that result closest to the reference vector V^*, whose tips actually constitute the vertexes of a triangle that encloses the tip of the reference vector, as shown in fig. 3.7;

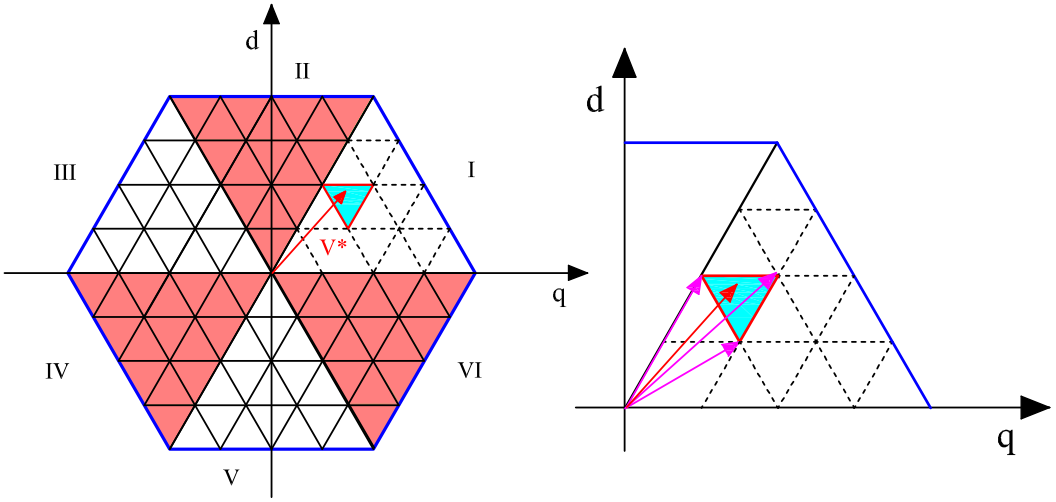


Figure 3.7: Voltage vectors of 5-levels converters in the d, q synchronous reference frame.

- calculation of the duty cycle of application of each chosen vector, corresponding to the quote of the approximation interval during which the corresponding converter state will be kept, in order to achieve the same local average

value as the reference voltage vector V^*; it may be demonstrated that such procedure is always applicable and provides a well defined result, since by arbitrarily varying such duty cycles under the constraint that their sum fills the reference interval, any point lying in the delimited triangle is reached exactly 1 time;

- identification of the actual temporal sequence to be used for the vectors composing the selected pattern, in order to minimize for example the number of commutations per period.

Among the PWM techniques the most commonly applied are the *level shifted pulse width modulation* (LSPWM) for the diode clamped multilevel converter and the *phase shifted pulse width modulation* (PSPWM) for the cascaded multilevel H-bridge.

The LSPWM involves more carriers featuring the same amplitude and frequency, which occupy contiguous bands between the extreme values of the phase output voltage $+V_{dc}/2$ and $-V_{dc}/2$ as depicted in fig. 3.8 for a 5-level converter. Depending on the relative phase of the different carriers, a further classification may be introduced:

- *in-phase* LSPWM when all the carriers are in phase;

- *phase-opposition* LSPWM when the carriers associated to negative levels of voltage are in opposition of phase with respect to the ones associated to positive levels;

- *alternative-phase-opposition* LSPWM when adjacent carriers are in opposition one respect to the other.

In general then the number of carriers needed to generate the driving signals for a n-level converter is $n-1$. As an example the resulting output waveform obtained with the first of the three methods for a five levels converter is shown on the bottom of fig. 3.8. Whichever of the previous variants is considered, in the PWM methods the state of the cells composing a leg is properly switched according to the comparison of the carriers and reference signal as usual, eventually implementing wise optimization criteria exploit the internal redundancies. Accordingly, the actual switching frequency of each device is usually lower than the global equivalent switching frequency of the converter leg. For example, in case of cascaded H-bridge structure controlled in bipolar mode, each unit is usually driven according to the comparison between the reference signal and a specific carrier, thus incurring in switching only when the reference crosses the band occupied by the relevant carrier.

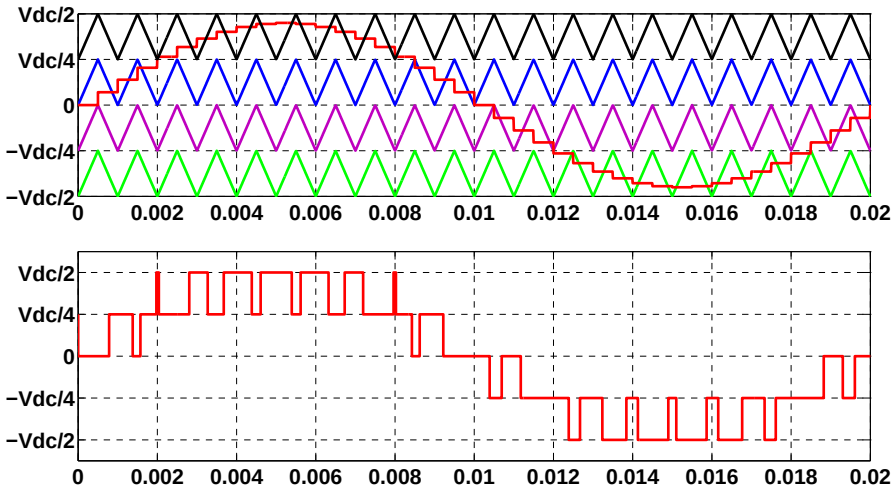


Figure 3.8: Phase disposition level shifted PWM for a 5-level converter

In the PSPWM, for a n-levels converter a set of n-1 carriers featuring the same amplitude and frequency is again used: nevertheless, differently from LSPWM, such carriers spread across the whole output voltage range and are suitably phase-shifted. The output voltage is conceptually obtained by summing the results of the comparison of the carriers with the unique reference signal. For example, in a cascaded H-bridge converter each unit can be driven according to the comparison of the reference signal with one of the carriers: the phase shifting among the carriers permits then to better approximate the reference waveform by generating a smoother signal featuring a larger number of steps with a smaller amplitude than a single larger H-bridge could generate, thus also minimizing the harmonic content. Actually, the best behavior in terms of harmonic distortion is obtained when the carriers are evenly spaced inside a carrier period, i.e. when the following phase shift (P_{shift}) is used:

$$P_{shift} = \frac{T_s}{n-1} \tag{3.8}$$

where n is the number of levels and T_s is the carriers period.

As an example for a 5-levels converter the modulation signal, the four required phase shifted carriers and the resulting output voltage waveform are depicted in fig. 3.9. As a consequence of the phase shift between the carriers the resulting switching frequency of the output voltage waveform is higher than the switching frequency of a single device. In particular, for a generic n level an effective output voltage switching frequency of $(n-1)\cdot$ times the single device switching frequency may be obtained. Different variants of PSPWM may involve different modulation signals but in this context they are not described for the sake of brevity. Some additional details will be reported in section 3.9 where a modified PSPWM will be proposed as modulation technique for cascaded multilevel converters.

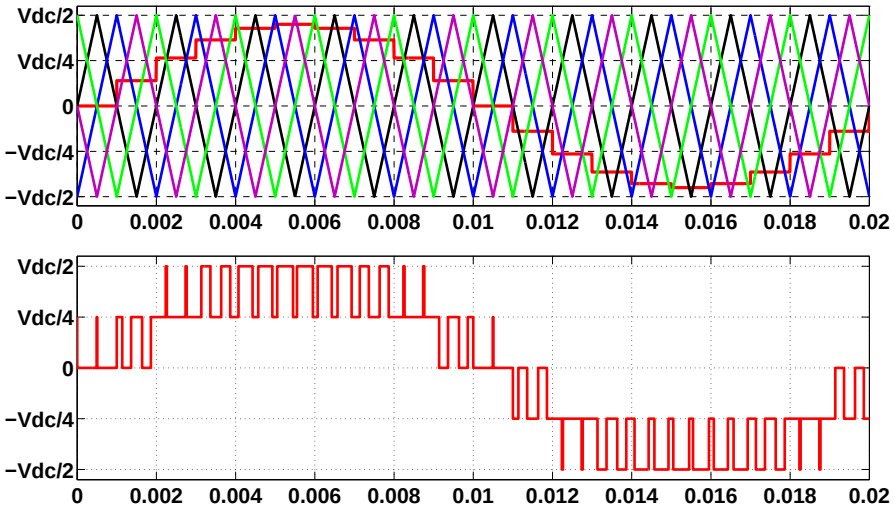


Figure 3.9: Phase shifted PWM for a 5-level converter

3.6 Cascaded H-bridge Multilevel Active Filter

Considering the favorable characteristics above highlighted, it is worth to investigate the use of multilevel converters in particular for such applications requiring high performances that are not easily obtained by means of standard VSI inverters. In fact, despite the much complicated structure, the improvements achieved in terms of performances may justify the higher costs. Aiming to evaluate the improvements achieved with respect to a standard VSI inverter, a multilevel cascaded H-bridge has been analysed considering its use as active power filter for aerospace applications. When the fundamental frequency involved is very high as in such applications (typically 400 Hz) the main issue is to obtain very high bandwidth of the control loops which may be difficult to achieve considering the present limits of power semiconductor devices and of microcontrollers/dsp in terms, respectively, of switching frequency and elaboration speed. Such problems are expected to be exacerbated in the future when the planned variable-frequency-and-voltage operation will be adopted which could lead to fundamental operating frequency as high as 800 Hz. In this scenario the possibility to obtain a good reference tracking with a relatively limited switching frequency by means of a multilevel structure results very attractive. The power structure of the active filter considered hereafter corresponds to the scheme depicted in fig. 3.10, including a 3-phase Y-connected cascaded multilevel inverter whose legs are composed of 2 series-connected H-bridge units each one in turn connected to independent d.c. capacitors; the a.c. inverter terminals are instead connected to the mains point of common coupling (PCC) by means of 3 equal magnetically decoupled interfacing series inductors. The shunt active filter (SAF) is assumed to be controlled by a digital system operating at

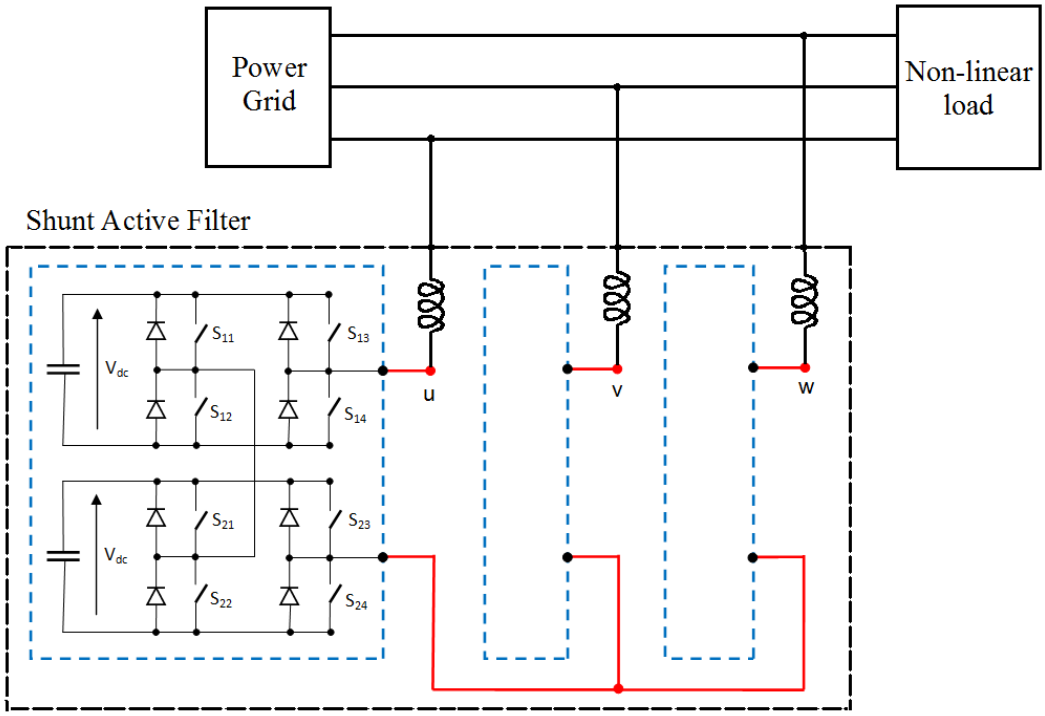


Figure 3.10: Electrical scheme for a 3-wires 5-levels cascaded H-bridge active filter

constant sampling frequency. The target of such controller consists in achieving a good power quality level in the currents drawn from the mains, especially for what concerns low-order harmonics compensation, while ensuring a constant average voltage on the dc bus capacitors. In particular a suitable control logic able to balance the different capacitor voltages has to be included avoiding possible dangerous large deviations that might emerge under unfavorable conditions, e.g. due to the presence of nonlinear or unbalanced loads.

3.7 Proposed Control System

Aiming to compare the performances of the multilevel SAF above illustrated with the standard two-level structure proposed in chapter 2, the same modified predictive control algorithm was employed. At first, it could be assumed that the 3 phases of the SAF may be considered independent, as it would be the case when a four wires configuration would be actually considered including a direct connection between the center tap of the multilevel converter and the neutral point of the supply grid. In such case, the same equivalent scheme already reported in fig. 2.3 could be used to model also the ac-side operation of each phase of the multilevel SAF. Therefore, basically the same mathematical model could be used for both converter types, where the two generators $e(t)$ and $v(t)$ schematized in

the circuit represent respectively the mains phase voltage at PCC and the average resulting value of the inverter leg voltage. When instead the neutral connection is not present, as in most of cases including the considered one, the same model may still be used provided that the 2 generators reported in the scheme above cited are intended to be cleared out of the homopolar component of the mains and SAF voltages, just as clarified in the analysis already presented in detail in section 2.5. Avoiding to duplicate here the above analysis for the sake of brevity, only the final resulting relation is recalled as obtained by solving the related continuous time equation in a discrete time domain and taking into account the delay introduced by the digital control system:

$$V(k+1) = E(k+1) - \frac{[I^*(k+2) - \Delta I(k+2) - I(k+1) \cdot a]}{b} \tag{3.9}$$

The equation may be implemented independently for each phase and allows to determine the desired voltage value to be applied during step $k+1$ aiming to make the inductor current achieve its reference value at the end of the following sampling period. A 2-steps dynamic delay is achieved.

The block diagram of the overall control structure of the three-phase five-levels SAF is illustrated in fig. 3.11 and closely resembles the one already realized for the standard single-bus 2-levels active filter. Keeping in mind the overall power balance, the currents globally drawn from the aggregate have to exactly compensate for the dissipated power when the internal energy is invariant, i.e. when the voltage of the SAF d.c. buses is kept constant at least in average terms across a period. Therefore the reference for each phase current drawn from the mains may be obtained as a sinusoidal waveform in-phase with the corresponding fundamental component of the phase voltage at PCC, whose amplitude is provided by a controller monitoring the SAF d.c. buses voltage of the same phase. The reference signal for each phase current to be drawn by the SAF may be then obtained by subtracting the phase current actually drawn by the load from the global current reference waveform previously generated. Such reference signals are then tracked by the control algorithm that regulates the SAF inverter. The controller used for keeping the two SAF d.c. buses voltage for each phase at their design value is constituted by a simple PI saturated controller, whose output provides the amplitude I^* of the phase mains current reference that would ensure the power balance with null fundamental reactive power drawing. The time constant of this control loop is chosen to provide a fairly slower time response than the current control loop, thus realizing a classical dual-nested loop hierarchical control scheme with separated dynamics. An additional control loop was also included to ensure an active balancing of the average voltages across the 2 d.c. buses in each inverter phase.

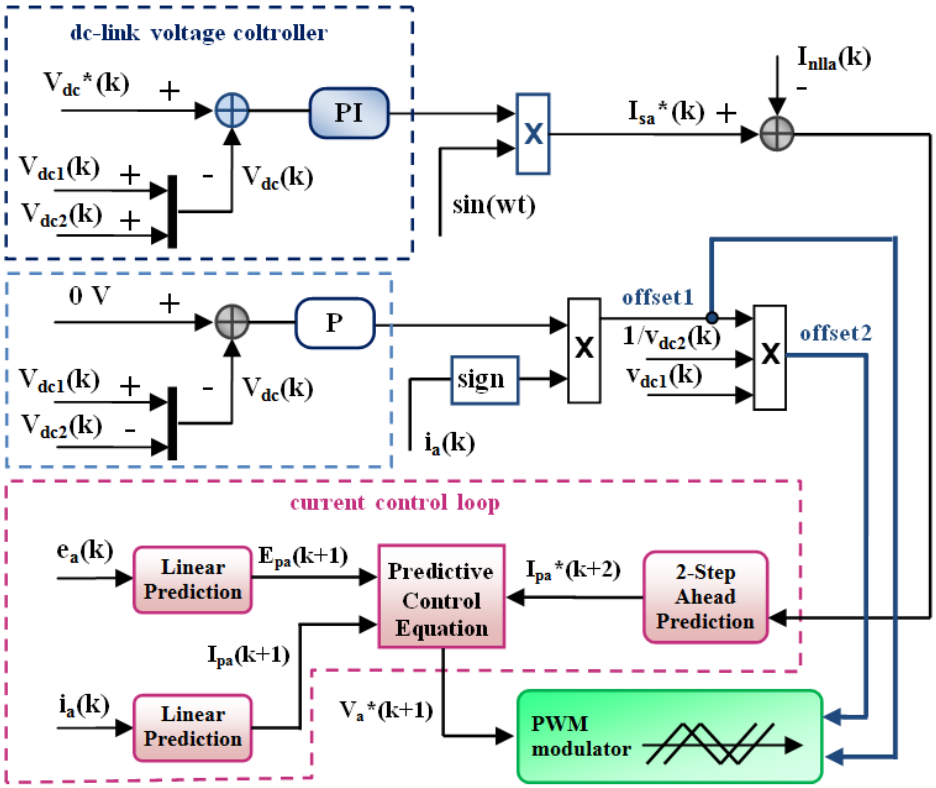


Figure 3.11: Single-phase representation of the overall control structure of the three-phase five-level SAF

Such loop, equipped with a suitable continuous controller, provides an additional unidirectional component that is summed to the modulation signal $V^*(k+1)$ in order to balance the two capacitor voltages. In fact, although the basic modulation strategy adopted would not inherently tend to introduce any voltage unbalancing between the 2 d.c. bus in each phase, such problem might still arise in practice due to several unideal issues, such as different losses in the power components or values of d.c. capacitance etc. In particular, it was found out that a linear proportional regulator performs rather well in this task, even when the load draws distorted currents. As described in more detail in section 3.9, the modulation strategy applied for the considered multilevel converter is based on PSPWM , yet with a wise modification aimed to achieve improved current reference tracking performance.

3.8 Theoretical Analysis

A theoretical analysis of the proposed converter may be undertaken by considering its equivalent circuital model: as usual, an ideal behavior may be assumed as a first approximation for both the reactive elements and the switching cells composing

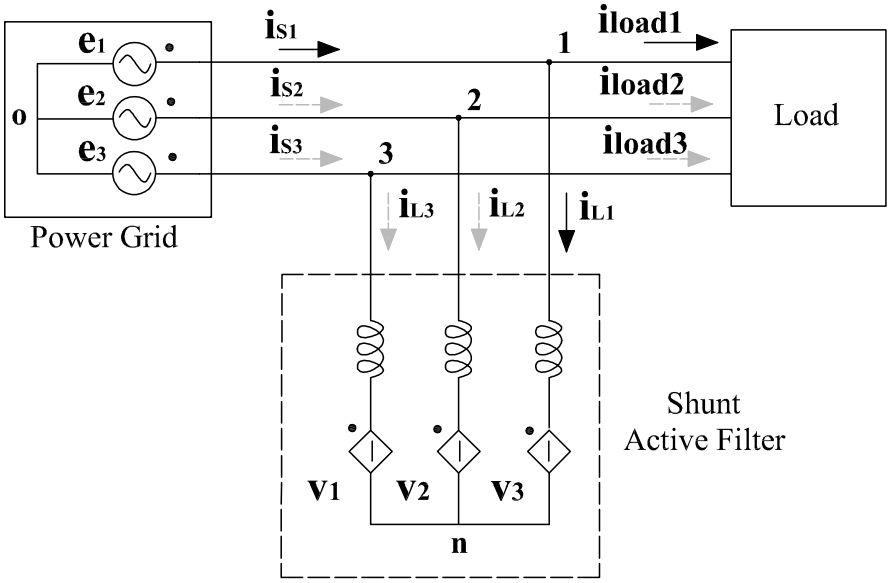


Figure 3.12: Shunt active filter three phase equivalent circuit

the inverter legs. The equivalent circuit reported in fig. 3.12 may be considered. In the circuit, each couple of H-bridges in one phase is replaced by a controlled generator whereas the mains is assumed to be ideally represented by a three phase symmetrical voltage generators neglecting the equivalent impedance of the grid. Such model may be used to carry out pseudo-linear dynamic analysis basing on the time-averaged values approach. Anyway, considering at first the active filter used for load balancing and reactive compensation, its operation would be typically referred to quasi-sinusoidal conditions. It is then worth analyzing the steady-state operation considering the rms phasors representing the fundamental components of a.c. quantities: in fact, this permits to highlight some inherent operative limits of SAFs featuring the considered multilevel structure. Keeping in mind the overall power balance, as already explained, at steady state the average power drawn from the mains must equal the average power drawn by the load plus the small internal losses of the active filter. Therefore, when it is assumed that the SAF performs its task and that the mains voltages constitute an ideal symmetrical tern, the following conditions should be obtained:

- a balanced set of currents should be drawn from the mains, each one resulting exactly in phase with the corresponding phase voltage;
- the dc buses voltages should remain nearly constant and equal to their design level;
- the currents injected in the mains by the SAF should determine a small net average power flow towards it, exactly balancing its internal losses.

Since the internal SAF losses should actually result very small, in this context they are neglected, meaning that under steady state conditions the net average power flow towards SAF should result

$$P_p = \sum_{k=0}^{3} P_{pk} \cong 0; \tag{3.10}$$

where P_{pk} is the actual power drawn by a generic phase k defined as:

$$P_{pk} = \frac{1}{T} \int_0^T V_{kn} i_{Lk}\, dt \tag{3.11}$$

Moreover, since each d.c. capacitors bank is completely insulated from the others, there is no chance to exchange power between different phases. Such peculiarity of the considered multilevel inverter, which is obviously not observed in a common single-bus SAF, implies that the following conditions must separately stand:

$$\begin{cases} P_{p1} = \dfrac{1}{T} \displaystyle\int_0^T V_{1n} i_{L1}\, dt \cong 0 \\ P_{p2} = \dfrac{1}{T} \displaystyle\int_0^T V_{2n} i_{L2}\, dt \cong 0 \\ P_{p3} = \dfrac{1}{T} \displaystyle\int_0^T V_{3n} i_{L3}\, dt \cong 0 \end{cases} \tag{3.12}$$

Under sinusoidal steady-state conditions, the previous relations imply that per each SAF phase the phasor identifying the related voltage $\widetilde{V}_{kn}$ must result orthogonal to the corresponding current phasor $\widetilde{I}_{Lk}$.

Let consider at first the hypothesis that the power structure actually includes a direct connection between the neutral point of the grid and the center tap n of the SAF. In such case, the possibility to satisfy the relations 3.12 while completely performing the SAF tasks depends significantly on the load. In particular, as long as the load is balanced the conditions 3.12 may be ideally verified even when the compensation of reactive currents is necessary. In fact, as shown in the phasor diagram depicted in fig. 3.13, in such scenario the multilevel inverter may operate correctly since the phase voltages $\widetilde{V}_{kn}$ are just equal to the mains phase voltages $\widetilde{E}_k$ and thus inherently orthogonal to the reactive currents that the SAF is expected to generate. On the other hand, when the load is unbalanced there is no way to guarantee the accomplishment of the previous constraints.

In fact, let consider for instance an unbalanced load simply consisting in a resistor connected between the line terminals 1 and 3. As it results evident from the phasor diagram shown in fig. 3.14, in this case the currents that the SAF should generate to compensate the load are not orthogonal at all with respect

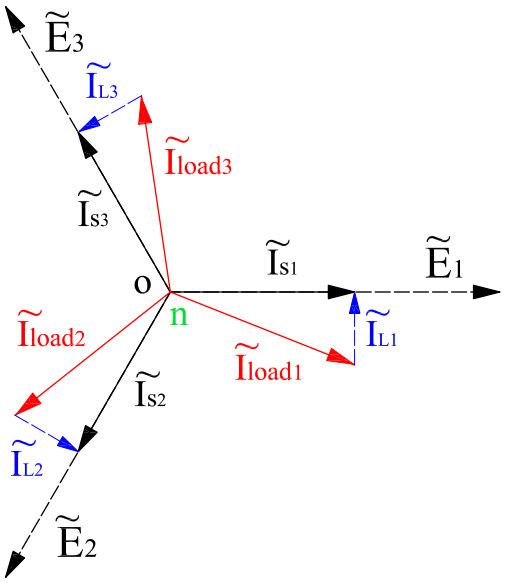


Figure 3.13: Example 1: liner balanced load drawing a reactive current component

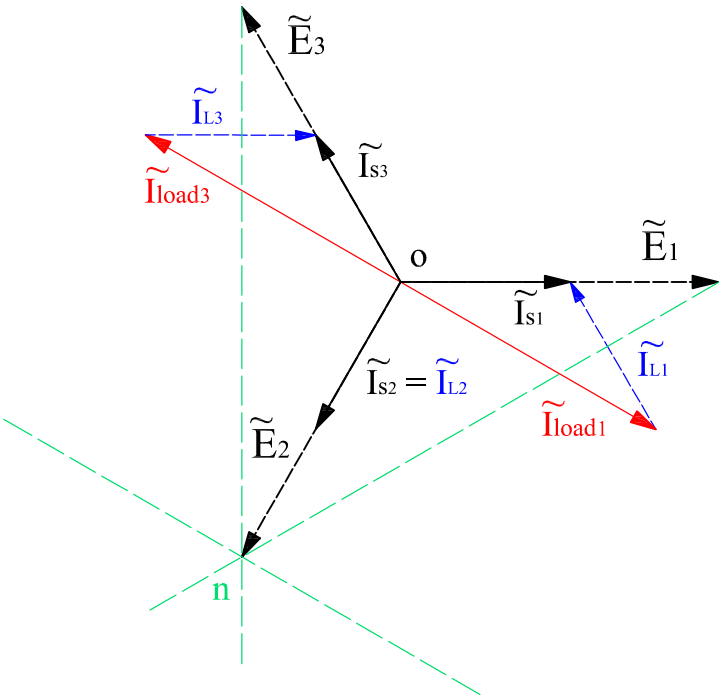


Figure 3.14: Example 2: single phase resistive load

to the corresponding mains phase voltages, turning out even in-phase for phase 2. A greater capability to compensate unbalanced loads is achieved when the SAF center tap is not connected to the grid neutral, as the voltage $\widetilde{V}_{on}$ may then become not null thus permitting the SAF phase voltages to be different from the grid phase voltages. In fact, referring for example to the same condition above depicted in fig. 3.14, the conditions of orthogonality 3.12 may be realized when

the SAF is controlled in such a way to generate the following set of phase voltages:

$$\widetilde{V}_{1n} = \widetilde{V}_{12} \qquad \widetilde{V}_{2n} = 0 \qquad \widetilde{V}_{3n} = \widetilde{V}_{32} \tag{3.13}$$

Thanks to the additional degree of freedom constituted by the voltage $\widetilde{V}_{on}$, at a first analysis the considered multilevel SAF seems able to properly operate even in case of strongly unbalanced loads, such as for example the case shown in fig. 3.15. Nevertheless, a more accurate analysis highlights that an entire family of possible load cases exists which makes impossible to verify the constraint 3.12.

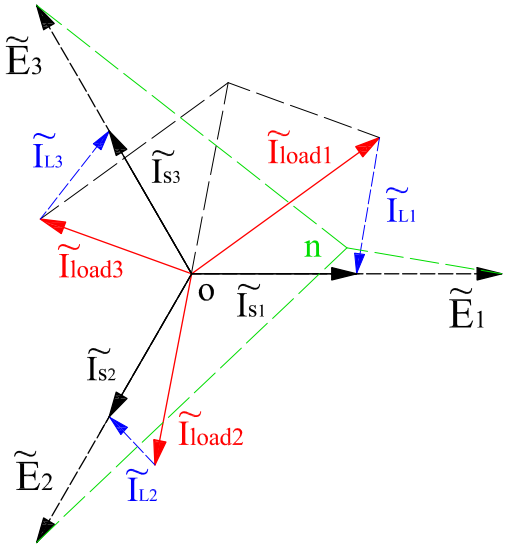


Figure 3.15: Example 3: generic unbalanced load

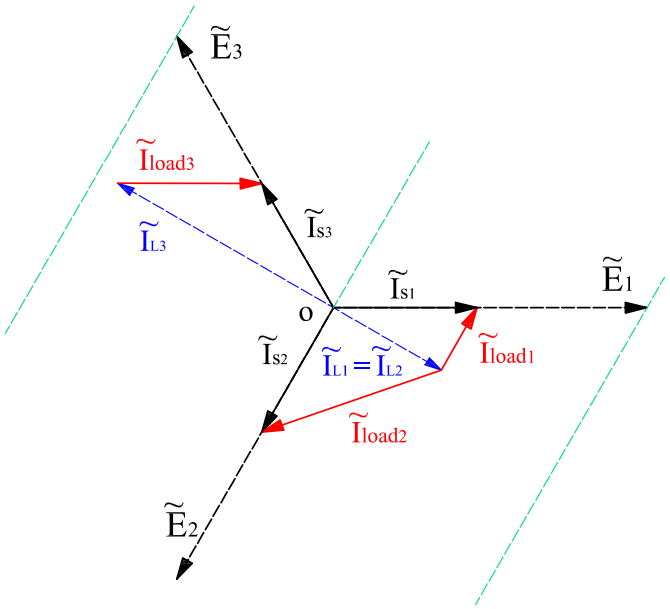


Figure 3.16: Example 4: limit condition for a 3-wires power structure

In fact, when the compensation of the load would require the SAF to generate a null-sum set of currents that are actually in phase or in opposition each other, the orthogonality conditions 3.12 cannot be simultaneously verified, since evidently this would require the phase voltages generated by the SAF to be also in phase or in opposition each other along the direction orthogonal to currents. Nevertheless, such condition would imply that the amplitudes of SAF voltages $\widetilde{V}_{kn}$ tend to infinity, as shown for example in the phasor diagram depicted in fig. 3.16, since their differences are anyway constrained to equal the line-to-line voltages imposed by the grid at PCC, which are obviously not in-phase. In analytical terms, such family of critical cases can be analyzed assuming that the currents to be ideally generated by the SAF assume the following generic expression:

$$\overrightarrow{I_f} = \widetilde{k} \begin{bmatrix} \alpha_1 & \alpha_2 & \alpha_3 \end{bmatrix} = \widetilde{k}\overrightarrow{\alpha} \tag{3.14}$$

where $\widetilde{k} = \beta e^{-j\vartheta}$ is a generic complex number and α_1, α_2, α_3 are three null-sum real numbers. Assuming then that the grid phase voltages constitute a direct sequence balanced set expressed as

$$\overrightarrow{V_s} = V \begin{bmatrix} 1 & e^{-j\cdot\frac{2}{3}\pi} & e^{-j\cdot\frac{2}{3}\pi} \end{bmatrix} \tag{3.15}$$

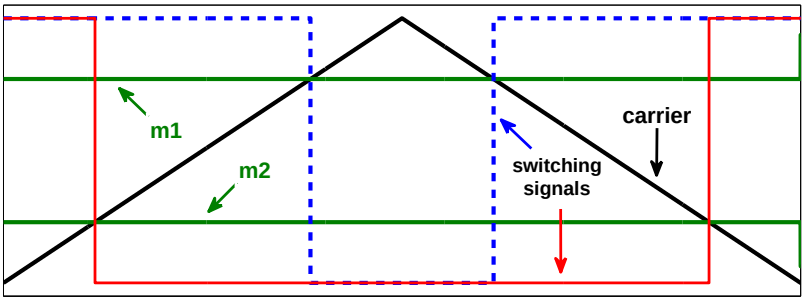
when the value of $\widetilde{k}$ is given by the following expression

$$\widetilde{k} = j \cdot \beta \overrightarrow{\alpha}^T \overrightarrow{V_s} \tag{3.16}$$

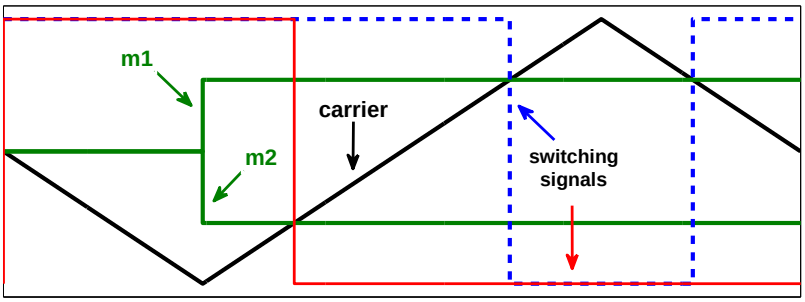
it may be easily demonstrated that the total active power drawn by the SAF, which is obtained as the dot product of the voltage and current vectors $\overrightarrow{V_s}$, $\overrightarrow{I_f}$, results actually null. Nevertheless, such null global value is obtained with not-null values of the average power flowing in each SAF phase, meaning that the compensation of such kind of load may be actually achieved only when some way to exchange power among the phases of the SAF is actually implemented, thus inherently excluding the multilevel structure here examined. In practice, this implies that any SAF featuring the structure depicted in fig. 3.10 is prone to exhibit an anomalous behaviour, such as unbalancing problems among the d.c. capacitors and practical impossibility to control the currents, when facing a load condition falling in the class above singled out. Moreover, similar problems may be expected even when the load approaches too much closely the conditions previously singled out, when the phase voltages that would be ideally compatible with all of the constraints actually exceed the SAF voltage capability.

3.9 Modified phase shifted PWM

According to the classical PSPWM technique the switching signals related to each leg of the two series connected H-bridges are obtained by comparing the modulation signal against two carriers shifted one respect to the other by one quarter of period. One of the carriers is then used to generate the switching signals for the upper H-bridge, whereas the other one is employed for the lower H-bridge, as shown in fig. 3.17, 3.18. Basically two possible modulations techniques may be realized. In the first one, named symmetrical PWM modulation, the modulation signals are kept constant during a whole period of the carrier, leading to the switching patterns shown in fig. 3.17 where the green lines refer to the opposite modulation signals used for the 2 legs of each H-bridge while the blue and red lines represent the related switching signals. This way, the equivalent switching frequency of the inverter leg results equal to 4 times the switching frequency of a single power device.



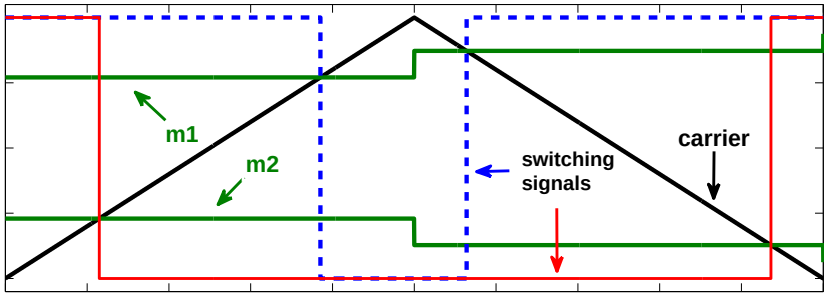
a) switching signals for the upper H-bridge



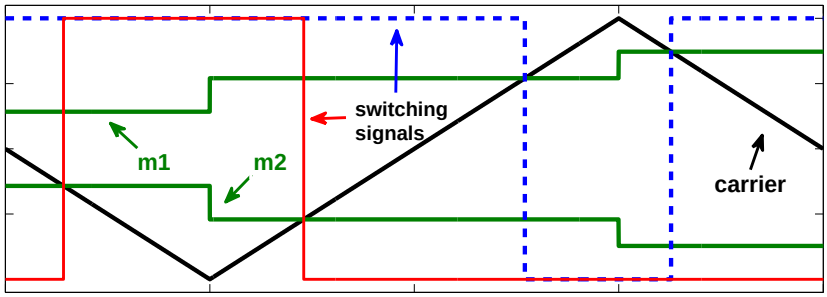
b) switching signals for the lower H-bridge

Figure 3.17: Symmetrical pulse shifted PWM pulse generation

In the second modulation technique, known as asymmetrical PWM, the modulation signal is updated at each notch of the carrier signal as shown in fig. 3.18, still determining a resulting equivalent switching frequency of the inverter leg equal to 4 times the switching frequency of a single device. Anyway, in this case it is possible to update at double frequency the reference signal, although obviously



a) switching signals for the upper H-bridge



b) switching signals for the lower H-bridge

Figure 3.18: Asymmetrical pulse shifted PWM PWM pulse generation

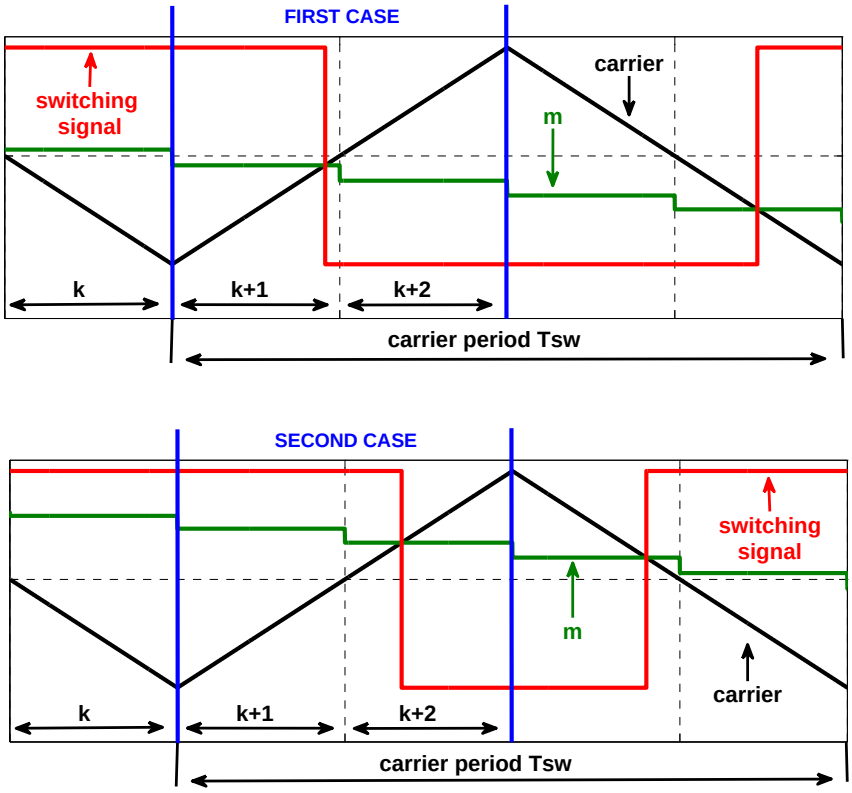


Figure 3.19: Modified asymmetrical PWM

this requires to double the sampling of the relevant quantities and the control algorithm has to be run 4 times per carrier period instead of 2.

In order to take advantage of all of such sampled values, the standard asymmetrical regular sampled PWM was modified as follows: instead of updating the modulation signals only at the beginning and at the middle of each carrier period, the proposed novel approach enables updating at each quarter of period. According to the new modulation the falling edge of a switching signal may be calculated as below described, referring to the 2 types of cases shown in fig. 3.19. At first the control algorithm calculates during the sampling period k the modulation signal m to be used during the sample period $k+1$; according to the calculated value of m two possible cases may occur:

- first case: if, according to the calculated value of m, the switching will happen during the sampling period $k+1$ the resulting calculated modulation signal is valid and will be employed.

- second case: if, according to the value of m the switching will take place during the sampling period $k+2$ the control algorithm will be repeated within the next sampling period $k+2$ in order to get a more accurate value for the modulation signal.

A similar approach may be used to determine the rising edges of switching signals.

3.10 Prototype System

Aiming to probe the actual performances of the proposed control strategy and compare the results to the ones obtained by means of the two level active filter a prototype system was purposely built in the University of Nottingham laboratory. According to the scheme depicted in fig. 3.10, the SAF experimental prototype used includes 6 H-bridges and 24 IGBTs whose rated current is 25 A with associated gate drive circuits whereas the designed d.c. bus voltage is 250 V. The d.c. terminals of each H-bridge are connected to a capacitors bank featuring a 1000 μF capacity, whereas the a.c. terminals are connected to the mains PCC via three filtering inductors: featuring equivalent series parameters $L = 3$ mH, $R = 0.037\ \Omega$. The control system is composed of a main board featuring a digital signal processor (DSP) and an auxiliary board equipped with a field programmable gate array (FPGA). Such boards may be noticed on the right in the picture of fig. 3.20, showing the prototype SAF except the a.c. side inductors. The DSP board, equipped with a $TMS320C6713$ device clocked at 225 MHz, is used to handle all high-level computational-intensive and not strictly time-sensitive tasks:

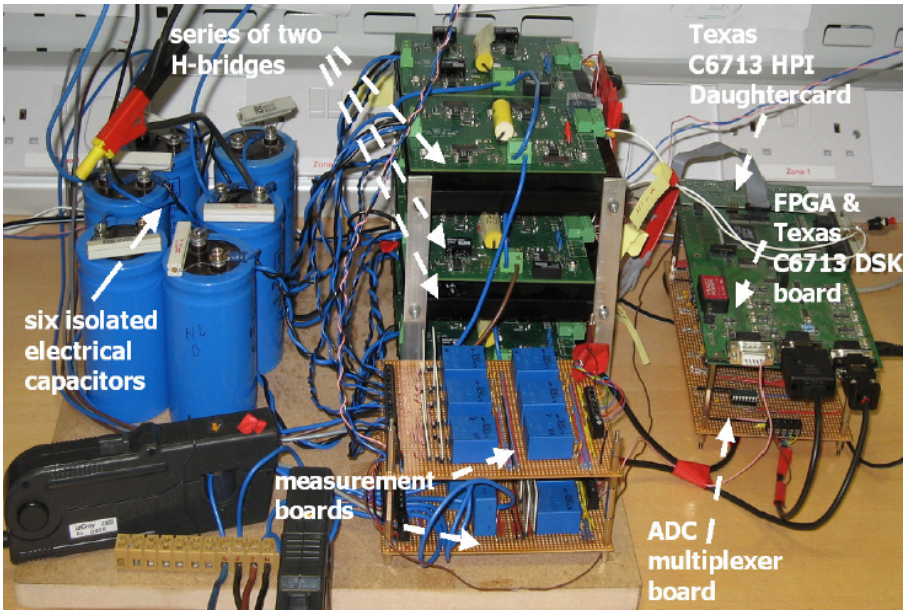


Figure 3.20: Top view of the experimental multilevel SAF prototype

- real-time calculations required by the implemented loop control algorithms;
- determination of the required inverter state sequence (legs state and related time duration) based on the implemented modulation technique;
- management of communication with a host PC permitting to directly download software and to provide the operator with full acquired data concerning both internal variables and signals digitalized by means of A/D converters.

The FPGA board, equipped with a $ProASIC\ 3\ A3P400$ device clocked at 50 MHz, carries out the most time-sensitive low-level tasks:

- generation of proper gate drive signals for the 24 IGBTs including dead time management, basing on the leg-state commands provided by the DSP,
- management of safe switch-off procedures in case of overcurrent or overvoltage alarms or failures;
- management of the Analog to Digital converters (ADC) cycle, forwarding the acquired data to the DSP.

3.11 Experimental Tests

Several experimental tests were carried out using the SAF prototype previously described, under the following operating conditions:

- fixed fundamental frequency: 400 Hz;
- line to neutral voltage: 115 Vrms;
- d.c. link voltage: 250 V for each capacitor bank;
- non linear load: 3-phase diodes rectifier bridge supplying a 15 Ω resistive load and equipped with an input filter constituted by 3 series inductors featuring $L = 1$ mH;
- sampling and switching frequency: 26 kHz and 6.5 kHz;

Aiming to compare the results with the ones already obtained for the single bus active filter similar tests have been performed evaluating at the same time the improvements achieved using the new proposed modified phase shifted PWM. The waveforms of the electric quantities were acquired by means of a high quality digital scope (500 MHz LeCroy 6050) during actual operation of the system, whereas spectral data were obtained by numerical post-elaboration. Further significant data were also recorded by means of an acquisition system embedded in the DSP board, which directly transfers data to a connected host PC exactly as explained in the previous chapter. Such data concern both internal signals of the control system and physical quantities sensed from the SAF sensors and acquired by means of A/D converters operating synchronously with elaboration tasks at frequency f_s. At first several experimental results are reported referring to the multilevel active filter working under the above reported operating conditions and using a standard asymmetrical phase shifted PWM modulation technique. The overall behavior of the tested system is summarized in fig. 3.21 where the main waveforms are shown. The blu curve identifies the non linear load current that, as it may be noticed, results strongly distorted with high low order harmonic content. The improvements achieved by means of the SAF are clearly highlighted by the mains current waveform (yellow curve). The current results, as expected, almost sinusoidal and in phase with the corresponding mains voltage (red curve) with a fairly limited superimposed high-frequency ripple mainly due to inverter commutation. In order to appreciate the improvements achieved in terms of harmonic content the mains and non linear load current spectra have been compared in fig. 3.22 for what concern the low order harmonics. The total harmonic distortion (THD) calculated results greater than the 18% for the non linear load current whereas reduced to the 8% for the supply current. In practice only the 5^{th} harmonic is significantly reduced. Exactly the same tests have been then carried out using the active filter under the same specified operating conditions but employing the proposed modified PWM modulation. The detail of the waveforms is shown in

fig. 3.23. The current drawn by the non linear load (blu curve) features exactly the same waveform as in the previous case with the same low order harmonic content leading to a THD grater than the 18%. On the other hand the supply current (yellow curve) results almost sinusoidal and in phase with the voltage (red curve). In such case, thanks to the new modulation, the resulting THD may be further reduced to the 3.8%. Despite the rather low involved switching frequency (6.5 kHz) when compared to the fundamental, both the 5^{th} and the 7^{th} harmonics result widely reduced as highlighted by the spectrum comparison reported in fig. 3.24. Therefore the improvements achieved using the modified modulation

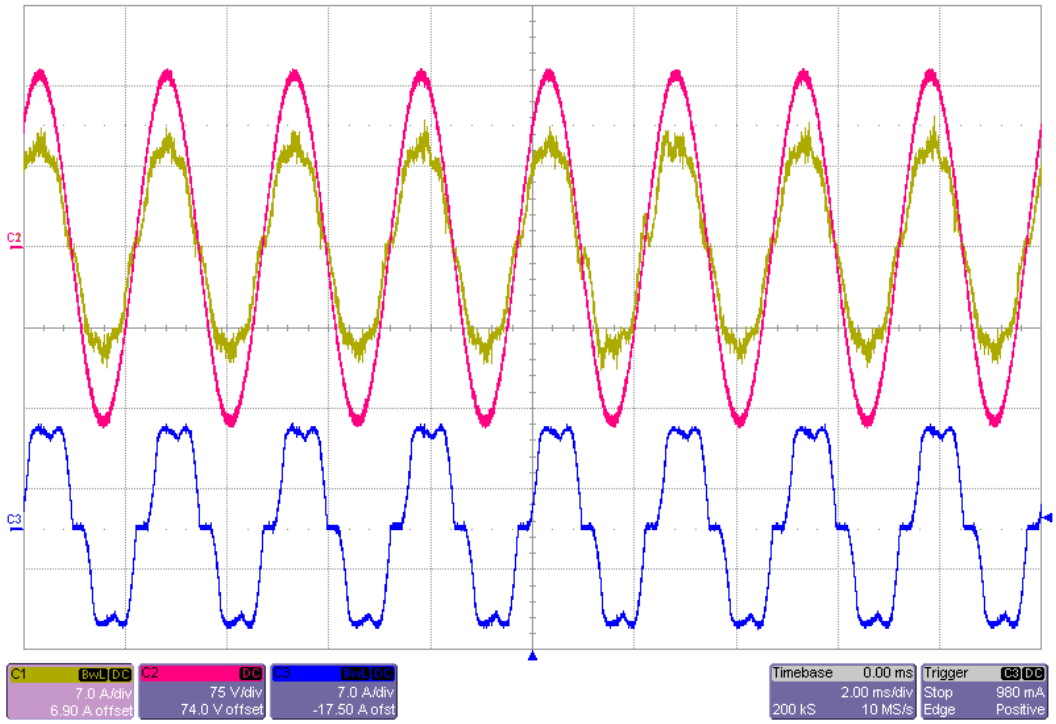


Figure 3.21: Measured steady-state data for a system phase: mains current (yellow), mains voltage (red) and non-linear load current (blue)

algorithm in terms of harmonic content are significant confirming the validity of the proposed solution. Considering the promising results obtained using the new modulation it is interesting to evaluate more in detail both the steady state and the transient behavior of the overall control strategy. In fig. 3.25 the trend of the reference current signal and of the related two-steps-ahead prediction are compared, highlighting the good performances of the adopted prediction algorithm. A comparison between the reference and actual waveforms of one of the currents drawn by the SAF is finally reported in fig. 3.26, highlighting a rather good overall current tracking capability although small mismatches may be noticed due to the strong distortion of the load current waveform to be compensated and the high

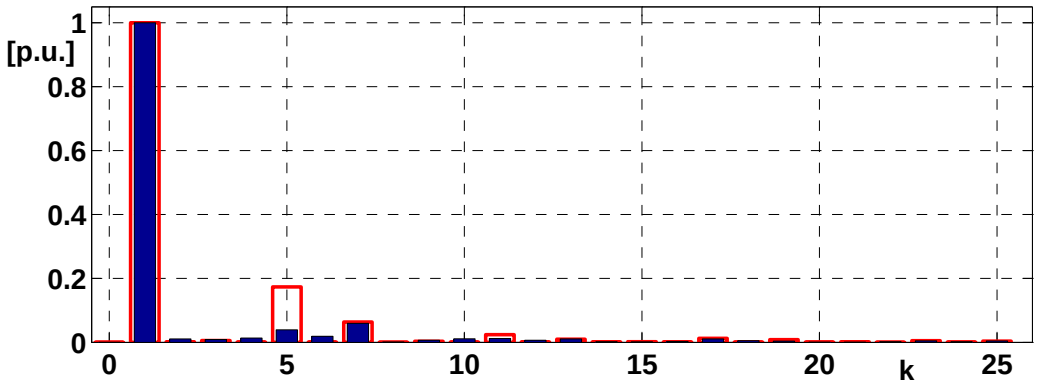


Figure 3.22: Harmonic spectrum of the measured non-linear load current (red) and mains current (blue)

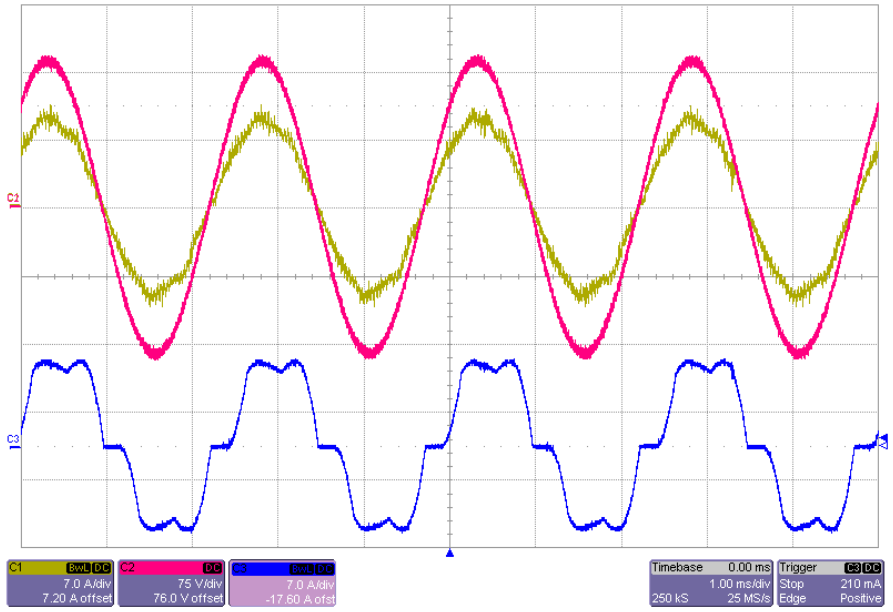


Figure 3.23: Measured steady-state data for a system phase: mains current (yellow), mains voltage (red) and non-linear load current (blue)

fundamental frequency involved. The transient behaviour of the proposed control system was also checked: exactly the same transient as for the single bus active filter has been tested i.e. a step-down change of the rectifier load achieved by increasing the resistance up to 150% of the rated value. The waveforms of mains voltage, mains current and load current measured for one of the phases during such transient are reported in fig. 3.27: it may be noticed that the SAF takes about 8 fundamental periods to settle after the transient, as dictated by the dynamics of the d.c. bus voltage control. The reference and actual current waveforms referred to a SAF phase across the load step instant are reported in fig. 3.28, as obtained by the embedded data acquisition system. It may be noticed that also in this

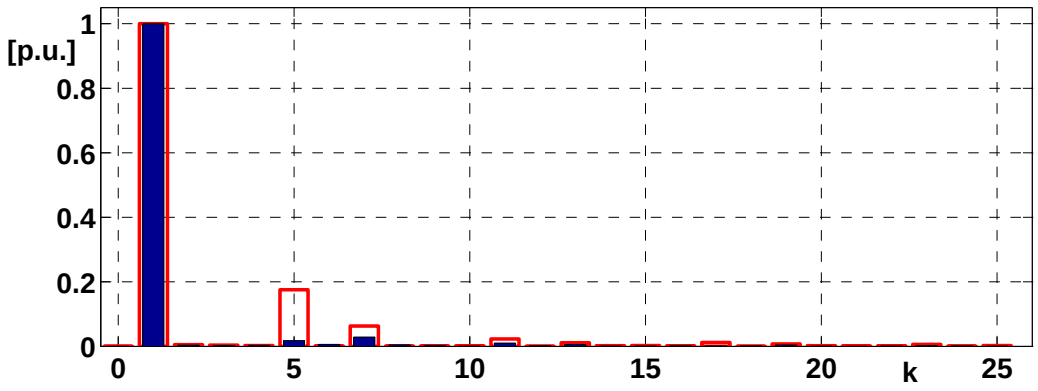


Figure 3.24: Harmonic spectrum of the measured non-linear load current (red) and mains current (blue)

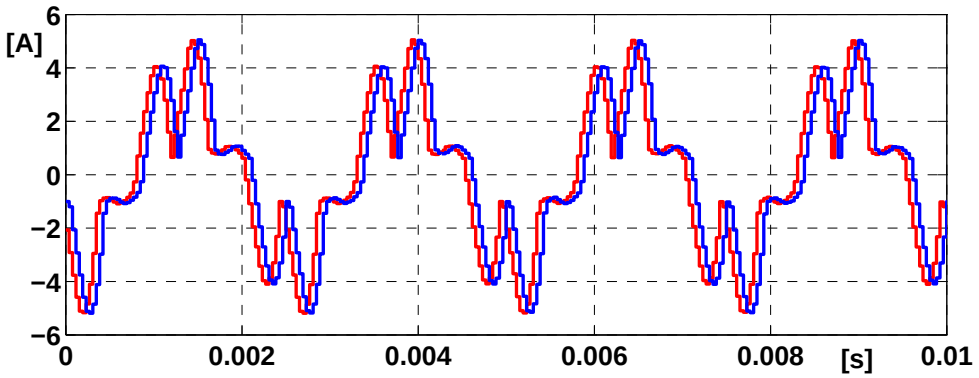


Figure 3.25: Acquired data: reference current vs. related prediction

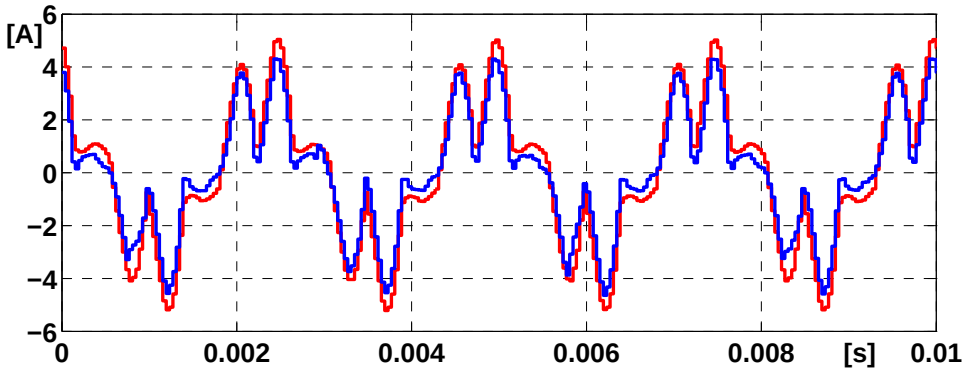


Figure 3.26: Acquired data: reference vs. actual inverter leg current

case the system exhibits a rather good tracking capability. The behaviour of the control logic able to exclude the reference current prediction during the transients may be appreciated in fig. 3.29. According to what explained in section 2.5 in fact an hysteretic-type operative mode identification logic has been implemented. The logic is based on the calculation of the absolute difference between the actual

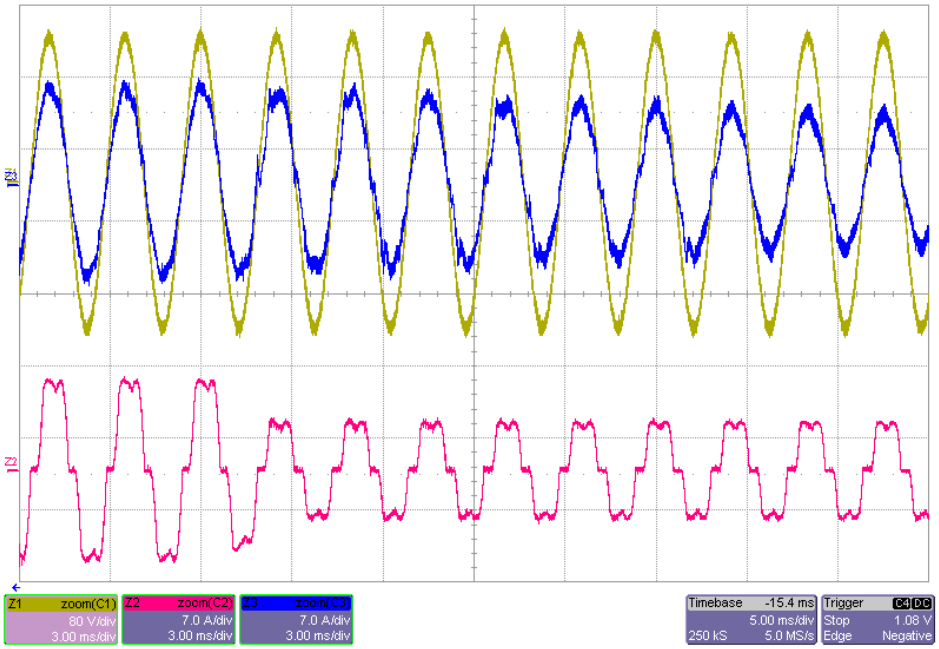


Figure 3.27: Measured transient data for a system phase: mains current (blue), mains voltage (yellow) and non-linear load current (red)

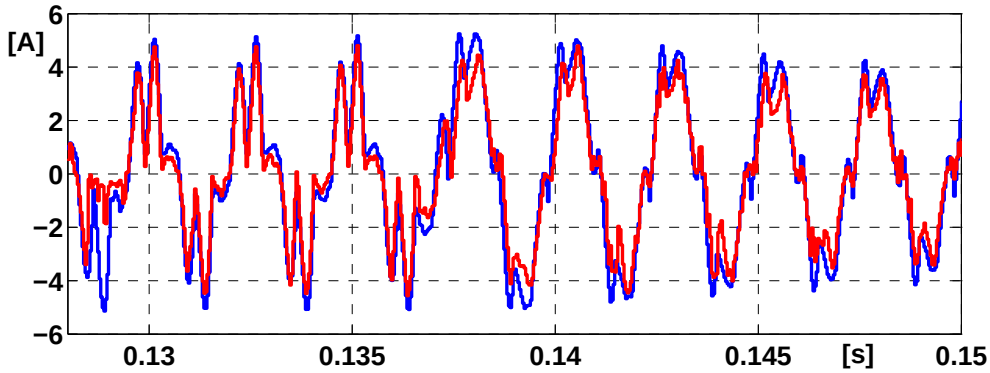


Figure 3.28: Acquired data during transient: reference vs. actual inverter leg current

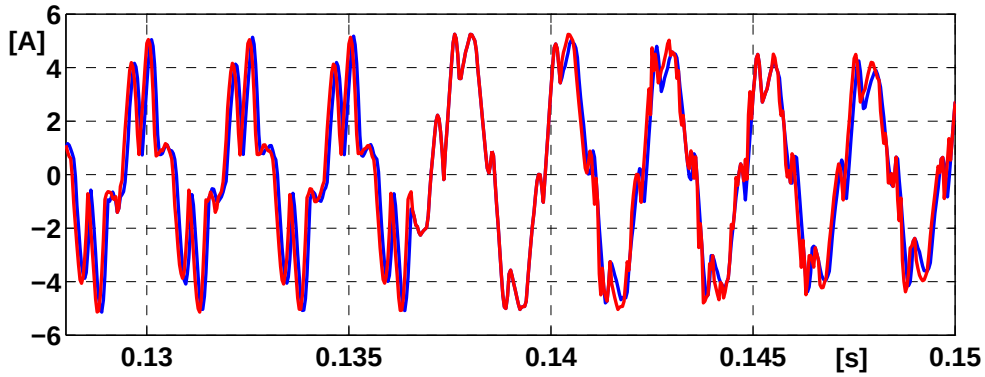


Figure 3.29: Acquired data during transient: reference current vs. related prediction

value assumed by the reference current at the present step and the value assumed exactly 1 fundamental period before. When this difference falls below a first suited threshold, steady-state condition is detected and the prediction is activated; when instead it rises above a second greater threshold, transient condition is detected and the prediction is replaced by the present value of the signal. According to the chosen threshold values the prediction is excluded at least for the first two fundamental periods after the transient (fig. 3.29). Only after these two periods the prediction of the reference current is included again making possible the compensation of the phase error introduced by the computation delay.

3.12 Conclusions

The predictive current control introduced and explained in detail in the previous chapter was considered able to provide high performances especially when high tracking capability at high frequency are required. Therefore, it was considered interesting to further investigate the performances of the control algorithm when applied to a different power structure. In particular, a multilevel SAF structure featuring 2 cascaded H-bridges per each inverter phase was considered and proposed especially referring to the compensation of load current harmonics in aircraft power systems. A purposely developed prototype was get ready at the University of Nottingham in order to perform several experimental tests and compare the results with the ones already obtained using the 2-levels active filter. A suitably modified modulation technique was also proposed and tested for this purpose. In comparison with the performances exhibited by the single-bus SAF and described in the previous chapter, the results obtained with the examined structure seem promising especially when the new modified modulation technique is employed. In fact, using exactly the same sampling frequency as before ($f_s = 26$ kHz), it is possible to get similar or better results while halving the switching frequency of power devices, thanks to the different power structure and modulation technique.

Chapter 4

Modeling and Analysis of a Rotary-Linear Brushless Machine

4.1 Introduction

Rotary-linear motors, able to provide both force and torque along the same axis, represent an interesting solution for managing combined linear and rotary motions along the same direction, as alternative to the usual employ of 2 separated normal motors. In several applications, including tooling machines, robotics and various industrial apparatuses for pick&place assembly, packaging, mixing, shaking etc, the combination of rotary and linear motion along the same axis is often used, for example for drilling, threading, machining, operating robot arms and end-effectors etc. Rotary-linear motors, able to effectively generate torque and axial force in a suitably controllable way, constitute then one of the most interesting typologies of multi-degree-of freedom machines (e.g. [31]). A further applicative area that is presently opening to such machines is the vehicular ambit, for example as servo-actuators for gearboxes (e.g. [32]) or for the integrated actuation of pairs of basic motions in active wheels on board of electric and hybrid vehicles (e.g. [33]), in the context of x-by-wire technology. Several rotary-linear machine typologies were proposed in the literature or patented (e.g. [34]). The simplest solutions consist in mechanically coupling a rotary and a linear motor not sharing any active part (e.g. [32]). More integrated machine configurations were also proposed. Anyway, some types exhibit a rather complicated behavior making difficult achieving an effective decoupled control of force and torque (e.g. [35], [36]). Due to the unconventional layout of magnetic core and/or windings, other types (e.g. [37], [38]) require peculiar and presently expensive manufacturing processes: in fact, for example magnetic core parts facing variable flux conditions with non-planar field maps cannot be properly realized using laminations, thus requiring

different solutions such as iron powder materials. Anyway, such technology has not yet gained a sufficient industrial diffusion and maturity, making presently not much attractive even potentially interesting machines such as [39], featuring a simple effective modular structure and a linear decoupled control of force and torque. Aiming to overcome the issues above recalled, recently a novel type of rotary-linear permanent magnets synchronous machine was purposely designed at the University of Pisa to permit manufacturing using common parts and diffused affordable technologies readily available on the market, while featuring a good ideal controllability.

4.2 Basic Structure

The structure and theoretical analysis of the basic variant of such machine, which was first proposed in [40], is described in detail in [41]. As shown in the qualitative axial section sketched and in the three-dimensional view in fig.4.1, in the basic variant of the proposed machine the stator part is actually constituted by 2 identical modules featuring an almost hollow-cylindrical shape and aligned side-by-side along their shared axis. A mover having quasi cylindrical shape is located inside them, aligned with the same axis. The stator modules are enclosed in an appropriate mechanical frame also supporting the mover by means of suitable rotary linear bearings, which permit it to rotate and translate along the machine axis yet suitably bounding the useful stroke. Each of the stator modules is composed of a separate winding and a macroscopically isotropic ferromagnetic core. Such core, which may feature semi-open slots facing the inner side as usual, may be manufactured by axially stacking silicon iron laminations, as usual. Each winding section, eventually hosted inside the core slots, features a standard 3-phase symmetrical structure with any number p of pole pairs. The width of the distance l_D between stator cores is intended to be as small as possible, having to host the end turn portions of windings protruding from the cores.

The active parts of the mover include a ferromagnetic core and a number $2 \cdot p$ of permanent magnets equal to the number of poles of stator windings. Such magnets feature identical sector-hollow-cylindrical shape with basically radial magnetization pattern having uniform intensity along their axial length; the radial orientation is inward for half of the magnets and outward for the others. The magnets are attached (e.g. by gluing) in symmetrically centered position around the external surface of the mover core, which features a basically cylindrical shape. The length of magnets, which are disposed in a belt-like sequence of alternated inward and outward poles, is ideally just equal to the sum of the axial length of

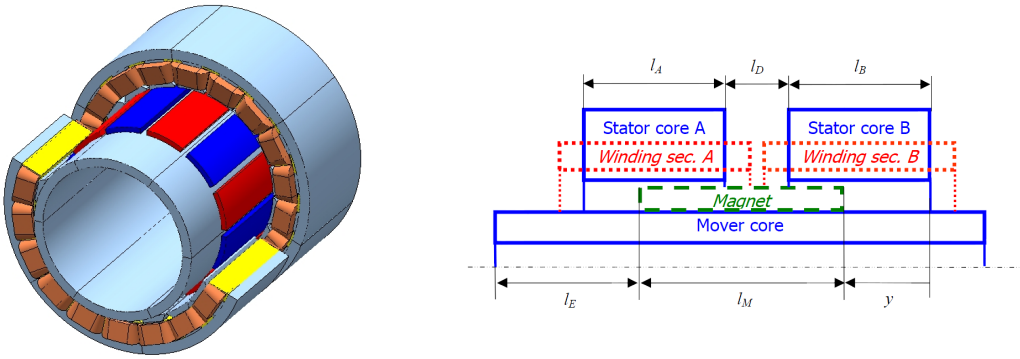


Figure 4.1: Qualitative axial section and three-dimensional view of the basic variant of proposed machine

a stator core $l_A = l_B = l$ plus the distance between stator cores, i.e. $l_M = l + l_D$. The ideal useful stroke, which is identified by the conditions of alignment of the magnet borders to the external sides of the 2 stator cores, corresponds then to the range of mover position $y \in (0, l)$. In practice, the length of magnets may be slightly increased to avoid the probable loss of potential performances in proximity of the stroke boundaries, thus reducing correspondingly the useful stroke length. The mover core may be manufactured either by stacking hollow circular laminations fitted on the mechanical shaft of the machine, or in massive form by properly shaping the shaft itself, which must be built-up of ferromagnetic material in this case. Anyway, the length of the active parts of the mover core protruding at both sides of the magnets corresponds at least to the stroke length, i.e. ideally $l_E = l$: this way, at any permitted position the whole main surface of each stator core faces active parts of mover, as required.

4.3 Ideal Operation of Basic Variant

A theoretical analysis of the proposed machine is illustrated resembling the popular basic treatment used for common rotary isotropic brushless motors. In fact, the material of the cores is considered as ideal linear with high permeability, while the difference between the permeability values of air and magnets is neglected as well as the effects of slots openings and the phenomena taking place close to end turns of windings. The classic sinusoidal approximation is finally used for the descriptive functions of windings and magnets. Under the above assumptions, it was highlighted that the resulting 6-phase 2-degrees-of-freedom electromechanical device may be conveniently analyzed using a global variables transformation actually consisting in 2 related Park transformations separately applied to each machine

module. This ultimately permits to derive the equivalent electric model of the machine in terms of corresponding pairs of complex Park vectors $\widehat{x} = x_d + j \cdot x_q$, each one referred to a stator section. Referring to the normalized axial position $y' = y/l \in (0, 1)$ the fluxes result so given by

$$\hat{\Psi}_A(t) = \Psi'_0 \cdot y'(t) + L_T \cdot \hat{i}_A(t) \tag{4.1}$$

$$\hat{\Psi}_B(t) = \Psi'_0 \cdot (1 - y'(t)) + L_T \cdot \hat{i}_B(t) \tag{4.2}$$

where L_T and Ψ'_0 are the transformed values of inductance and null-currents flux. Introducing the normalized axial speed $v'(t) = \frac{\mathrm{d}y'(t)}{\mathrm{d}t}$ and the electric speed $\omega(t) = p\Omega(t)$, whwre Ω is the actual speed of the mover the transformed Park voltages result as

$$\hat{v}_A(t) = r \cdot \hat{i}_A(t) + L_T \cdot \frac{d\hat{i}_A(t)}{dt} + j \cdot \omega(t) \cdot \hat{\Psi}_A(t) + \Psi'_0 \cdot v'(t) \tag{4.3}$$

$$\hat{v}_B(t) = r \cdot \hat{i}_B(t) + L_T \cdot \frac{d\hat{i}_B(t)}{dt} + j \cdot \omega(t) \cdot \hat{\Psi}_B(t) + \Psi'_0 \cdot v'(t) \tag{4.4}$$

where r is the common value of phase resistance. The above expressions closely resemble the classic model of isotropic brushless rotary machines, yet with an additional term proportional to axial speed while the fluxes result dependent on the axial position as in 4.1, 4.2. The same analysis permits to determine the total wrench acting on the mover, i.e. the global values of force and torque, which result given by

$$\begin{bmatrix} F\left(\vec{i}'\right) \\ C\left(y, \vec{i}'\right) \end{bmatrix} = \frac{\Psi'_0}{l} \cdot \begin{bmatrix} (i_{Ad} - i_{Bd}) \\ p \cdot (y \cdot i_{Aq} + (l - y) \cdot i_{Bq}) \end{bmatrix} \tag{4.5}$$

The electromagnetic force F results then proportional to the difference between the d current components, independently on the mover position. Analogously, the torque C results indeed proportional to a linear combination of the q current components, yet with coefficients depending on the mover axial position in complementary linear way. The expressions above recalled highlight that each wrench component depends on 2 transformed current components, meaning that some regulation criteria is required to map a generic reference wrench vector into a set of reference currents. Different criteria may be then considered also keeping into account the typical constraints due to max resistive losses, max voltage etc. In fact, the combination of such constraints and adopted regulation criteria determines the machine wrench capability. Hereafter, for the sake of brevity only the regulation criterion aimed to minimize the global resistive losses will be addressed. When the max resistive losses constraint results dominant in limiting the machine performances, i.e. typically at low speed since in this condition iron

losses are usually rather low being related to frequency, an interesting regulation criterion may consist in minimizing the total value of Joule losses per any given wrench. Introducing the rated current I_R as the limit rms current value allowed in each stator section and defining the corresponding rated values of force and torque F_R , C_R representing separately the max capability limit of the machine when the other wrench component is null, the normalized values of the currents obtained by applying the above regulation criterion result

$$\begin{bmatrix} i_{Ad}" & i_{Bd}" \end{bmatrix} (F") = \begin{bmatrix} 1 & -1 \end{bmatrix} \cdot F" \qquad \forall y' \tag{4.6}$$

$$\begin{bmatrix} i_{Aq}" & i_{Bq}" \end{bmatrix} (y', C") = \frac{\begin{bmatrix} y' & 1-y' \end{bmatrix}}{2 \cdot y'^2 - 2y' + 1} \cdot C" = \begin{bmatrix} f_A(y') & f_B(y') \end{bmatrix} \cdot C" \tag{4.7}$$

where $F"$, $C"$ are the p.u. force and torque values referred to rated values and the torque functions f_A , f_B depend on the axial position according to the trends shown in fig. 4.2.

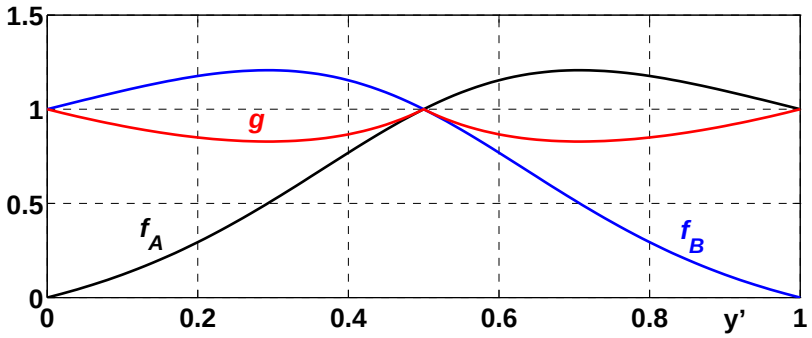


Figure 4.2: Trend of capability related functions f_A, f_B, g

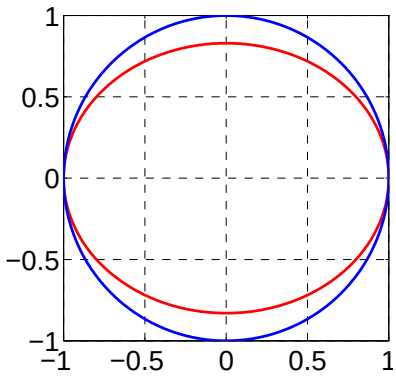


Figure 4.3: Capability min/max curves

When normal cooling solutions are adopted, the 2 stator modules may be prudentially considered as independent from the thermal point of view. Accordingly, when it is required that the resistive losses in each winding section are limited to the rated value produced by I_R , as shown in fig. 4.3 the p.u. capability region of the machine results a centered ellipse featuring constant maximum force whereas the maximum torque value varies with the mover axial position, ranging about in the interval $[0.83, 1]$ according to a function g whose trend is also reported in fig. 4.2.

4.4 Drive Control Using Sinusoidal Model

Aiming to permit checking different control solutions and to adjust the parameters of regulators by probing the overall performances, a first parametric simulation model of a complete drive using the proposed machine was get ready within the Matlab-Simulink© simulation environment. Such model included semi-ideal models for both the machine (implementing the sinusoidal model above recalled), the supply and regulation converter (assuming instantaneous commutations and ideal on and off conditions of commutation cells) and of the control system (represented by continuous-time blocks and ideal modulators). In particular, as case study a drive was modeled assuming that the supply converter consists in a pair of common 3-legs 1-supply-level VSI inverters directly feeding the 2 machine sections, whereas the control system consists in modified PI regulator. The scheme of the external level of the resulting simulation model is depicted in fig. 4.4. Referring to the minimum global Joule losses regulation criterion above described, an application scenario requiring the control of angular speed and axial position was first considered for the selected case study, assuming that the mechanical load features a passive nature exerting a force and a torque equal to a constant quote plus a variable quote depending on speed.

The considered solution was tested by checking its response to various operative conditions. As example of the results provided by the model, hereafter some data are reported referring to a sequence of 4 transients consisting in a reference angular speed step at $t_1 = 0.5s$, a load torque step at $t_2 = 1.5s$, a reference axial position step at $t_3 = 2.5s$ and finally a load force step at $t_4 = 4s$. It may be noticed that in overall terms the behavior of the drive may be considered as fairly good, confirming the substantial validity of the proposed solution. Nevertheless, as expected the position control task results more challenging than the angular speed control, leading in this example to a more oscillating operation.

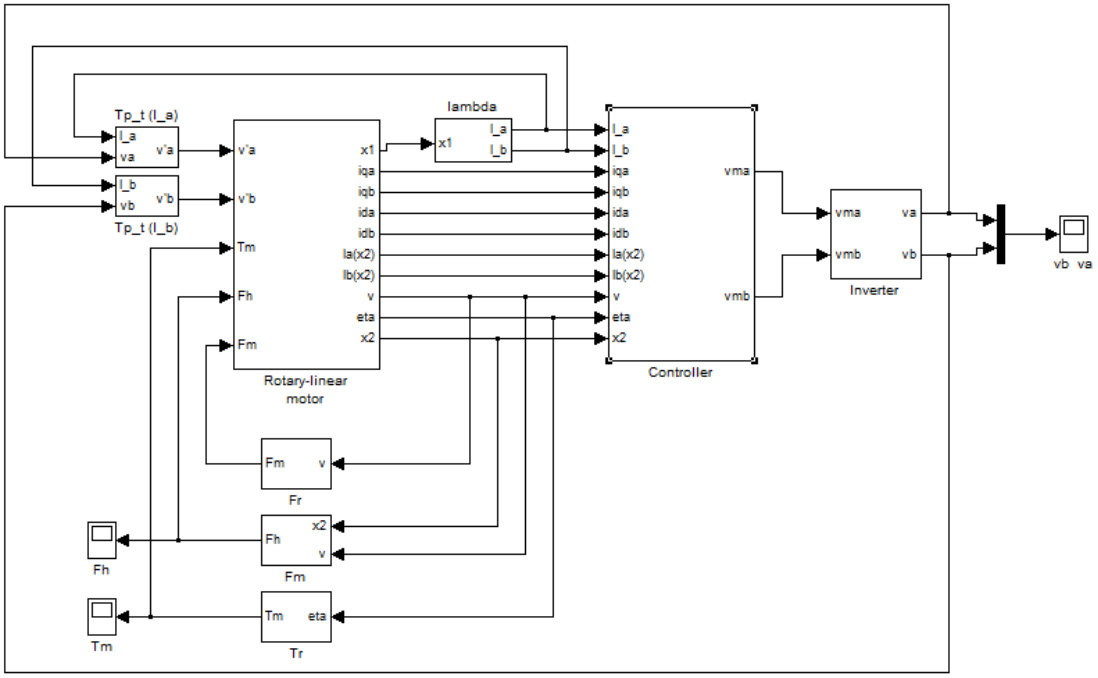


Figure 4.4: Main level of the Simulink model of the rotary-linear drive

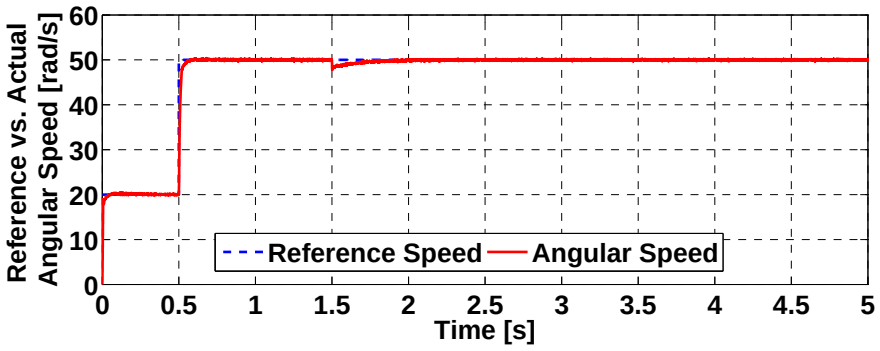


Figure 4.5: Reference vs. actual angular speed

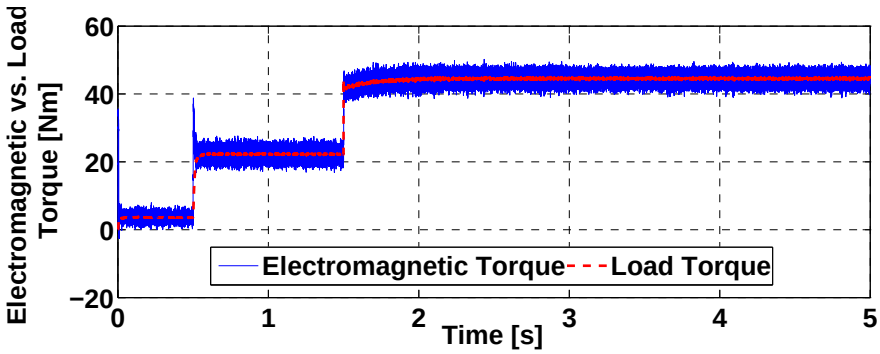


Figure 4.6: Electromagnetic torque vs. load torque

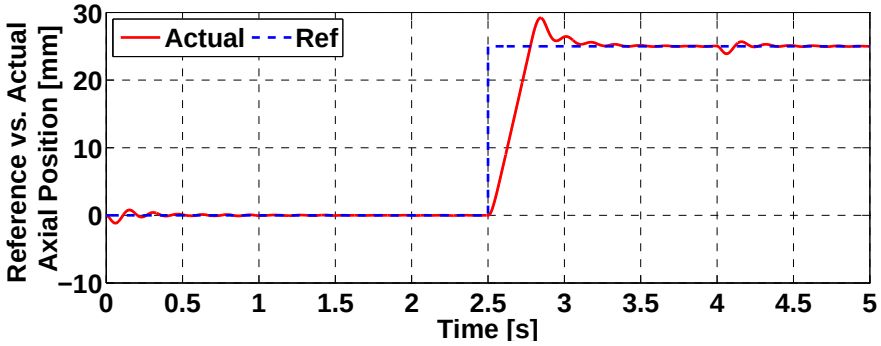


Figure 4.7: Reference vs. actual axial position

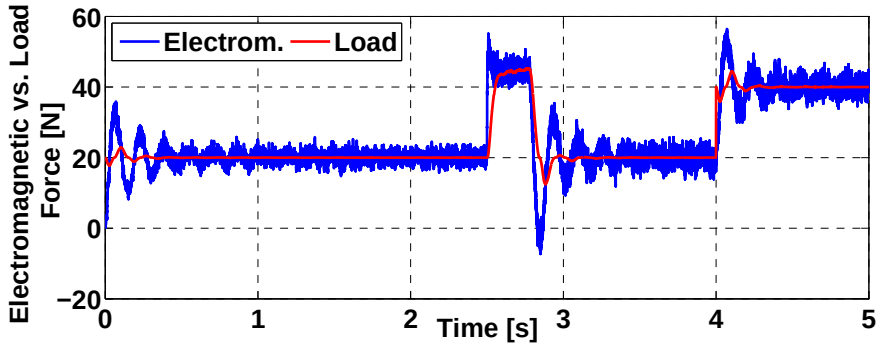


Figure 4.8: Electromagnetic force vs. load force

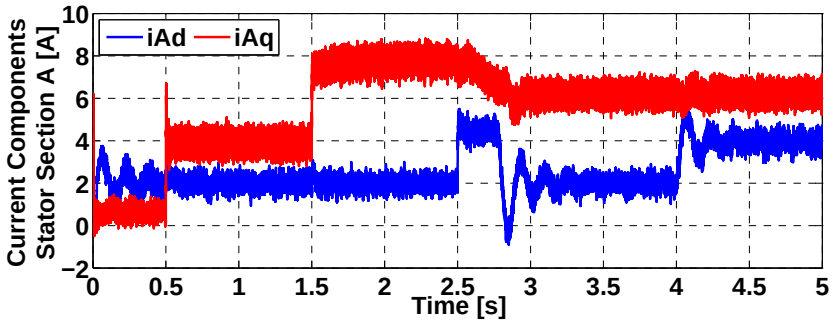


Figure 4.9: Park current components in winding section A

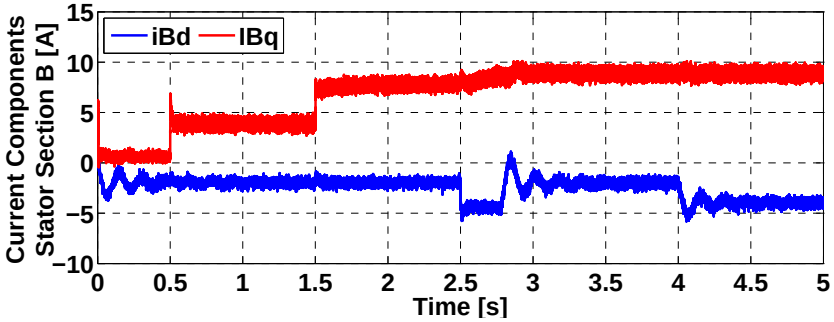


Figure 4.10: Park current components in winding section B

4.5 Equivalent Magnetic Circuit Model

The idealized sinusoidal model previously recalled permits to analyze with fair accuracy the main aspects affecting the machine behaviour, thus permitting to single out suitable general criteria for its regulation. Nevertheless, a more accurate approach is required when at least the most significant secondary effects neglected by the sinusoidal model are going to be taken into account to check the actual behavior of the machine more in detail. The most accurate approach available for electromagnetic simulations consists in using a 3-D FEM model; its development for the considered machine is described in [42]. Nevertheless, even when all of the existing symmetries are exploited to reduce the size of the actually modeled region, such approach results far too much computationally intensive for a system-level analysis aimed to check the behavior of a complete drive. An intermediate level of accuracy may be obtained with a much lower computational burden by using the equivalent magnetic circuit modeling approach. In such type of model, the geometry of the main flux tubes is preliminarily determined by a qualitative examination of the machine structure. Each significant portion of flux tube featuring sufficiently homogeneous properties is then modeled as a permeance depending on the mover position and eventually featuring a non-linear magnetic tension vs. flux curve when it is composed of ferromagnetic materials and saturation is kept into account. Moreover, equivalent m.m.f. generators are included in each branch representing a portion of magnets, to keep into account their coercivity. The equivalent circuit model may be limited to the main flux tubes when the reluctance of ferromagnetic parts is neglected, as in such case the effects of secondary fluxes may be kept separately into account by means of a dedicated inductance matrix to be added externally. Otherwise, branches keeping into account the leakage flux tubes must be also included in the circuit. Finally, a set of equivalent m.m.f. generators is used to keep into account the winding currents: although partly arbitrary, their location in the circuit must ensure that for any mesh in the circuit the resulting m.m.f. equals the total current actually linked with the corresponding physical loop. In the model of the proposed machine, at first saturation is neglected and the permeability of the ferromagnetic material composing the cores is assumed to be much higher than air, whereas the magnets are assumed featuring a uniform thickness and radial magnetization pattern. This permits to consider the shape of the main field lines as approximately straight and radial inside the main airgap, thus neglecting the local curvature due to slots openings, magnets borders etc. Moreover, the same hypotheses permits to approximately neglect the m.m.f. drops inside the core parts, since no critical situation exist consisting in closed paths completely passing inside ferromagnetic materials and linking a non-zero

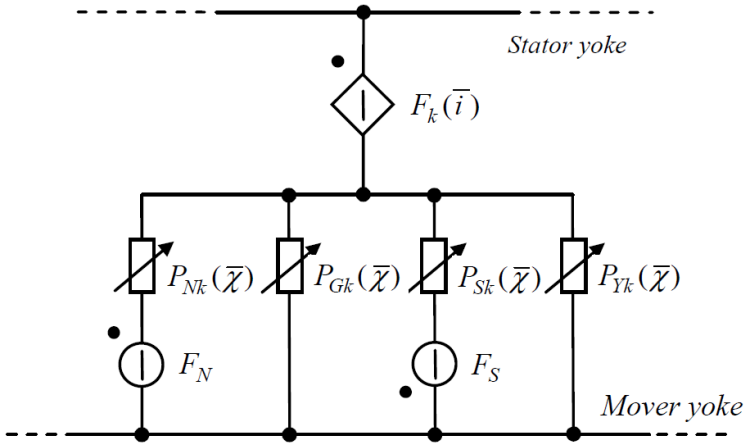


Figure 4.11: Typical structure of 3-wires Shunt Active Filter

resulting current. In such scenario, at most 4 types of main flux tubes leave the main face of any dent to cross respectively outward (north) polarized magnets, inward (south) polarized magnets, the eventual gaps existing between magnets and the area of mover yoke adjacent to the previous ones along the axial direction and not covered by magnets. Therefore, under the assumed hypotheses the equivalent magnetic circuit of the machine may be arranged in modular way focusing on the above 4 types of flux tubes per each stator tooth, as sketched in fig. 4.11. In fact, per each module a set of such blocks equal to the total number of the teeth is considered; the 2 sets share the lower bar of the circuit, representing the mover yoke, whereas 2 distinct upper bars have to be considered as the 2 stator yokes are not magnetically separated. For any tooth k in a stator module, the 4 equivalent permeances $P_{Nk}(\overline{\chi})$, $P_{Sk}(\overline{\chi})$, $P_{Gk}(\overline{\chi})$, $P_{Yk}(\overline{\chi})$ related to the above 4 types of flux tubes depend on the mover position, as it determines their cross section. In fact, under the assumed hypotheses all of such permeances result linearly dependent on the axial position, resulting piecewise constant or linearly variable with angular position. The polarization of magnets is kept into account by means of equivalent m.m.f. generators F_N , F_S included in the related branches, whose values are determined as the products of the corresponding coercive field by the magnets thickness. Assuming that stator teeth are numbered sequentially along a given tangential direction, the value of the m.m.f. generator associated to each of them $F_k(\bar{i})$ is calculated, for example, as the total current flowing in the slots located along the considered direction between tooth 1 and the considered tooth k; thus posing $F_1 = 0$ in any case. The above model may be used to determine the main linked fluxes when the mover position and the phase currents are assigned, thus permitting to investigate various combinations of winding distribution, magnets size etc. It may be also used to determine derived quantities, such as inductances

and motional coefficients, which are required to analyze a generic operative condition. In particular, under the assumption of linear magnetic behavior the inductances may be determined by conceptually solving the equivalent circuit applying the superimposition method, in such a way to separately calculate the flux quotes due to permanent magnets and currents. The latter permit then to calculate the inductance matrix, whereas the motional coefficients may be obtained in any case by numerically approximating the analytical derivative of fluxes vs. positions at constant currents with the corresponding incremental ratio, separately considering the null-currents and incremental quotes. When slots openings are not modeled, or gaps between magnets are not present and an integer number of slots per pole is used, it may be concluded that at null currents the variation of internal energy vs. position is negligible, just as for the theoretical model. Therefore, in such hypotheses the null-currents wrench results null just as in the sinusoidal model, conceptually permitting to calculate the wrench developed in generic conditions by integrating the motional coefficients function vs. currents from zero. Such integration may be carried out either analytical or numerical approximated form. When instead both stator and mover feature local anisotropy, i.e. slots openings are considered and magnets width is smaller than 1 pole pitch, a not negligible wrench at null currents may arise, which may be estimated by approximating the coenergy derivative vs. positions at fixed currents with the related incremental ratio. A fully parametric model of the considered machine typology based on the above equivalent magnetic circuit was implemented as a script function in the Matlab® simulation environment. The top-view of the graphical interface realized is shown in fig.4.12. Once introduced the main geometrical parameters such model permits to estimate with a fair level of accuracy the effects of some machine characteristics that are neglected in the theoretical sinusoidal model, such as the width of slots openings and of the eventual tangential gaps between magnets, the permeability of the latter and the deployment of winding inside different slots. This permits then to quickly check the effects of different design options for both the machine and the control system. As it may be noticed on the graphical interface right section several machine parameters may be modified, updated and the resulting machine structure shown directly in the 2-dimensional view reported on the left. Only one pole pair is shown for simplicity. Right below the figure it is then possible to choose among a concentrated or distributed winding configuration. Finally on the bottom it is possible to select from the popup menu the desired function to be calculated (permeances, fluxes, inductances, motional coefficients and coenergy).

The above model may be first used to estimate the machine characteristics. As a qualitative example, hereafter some numerical data are reported referring to

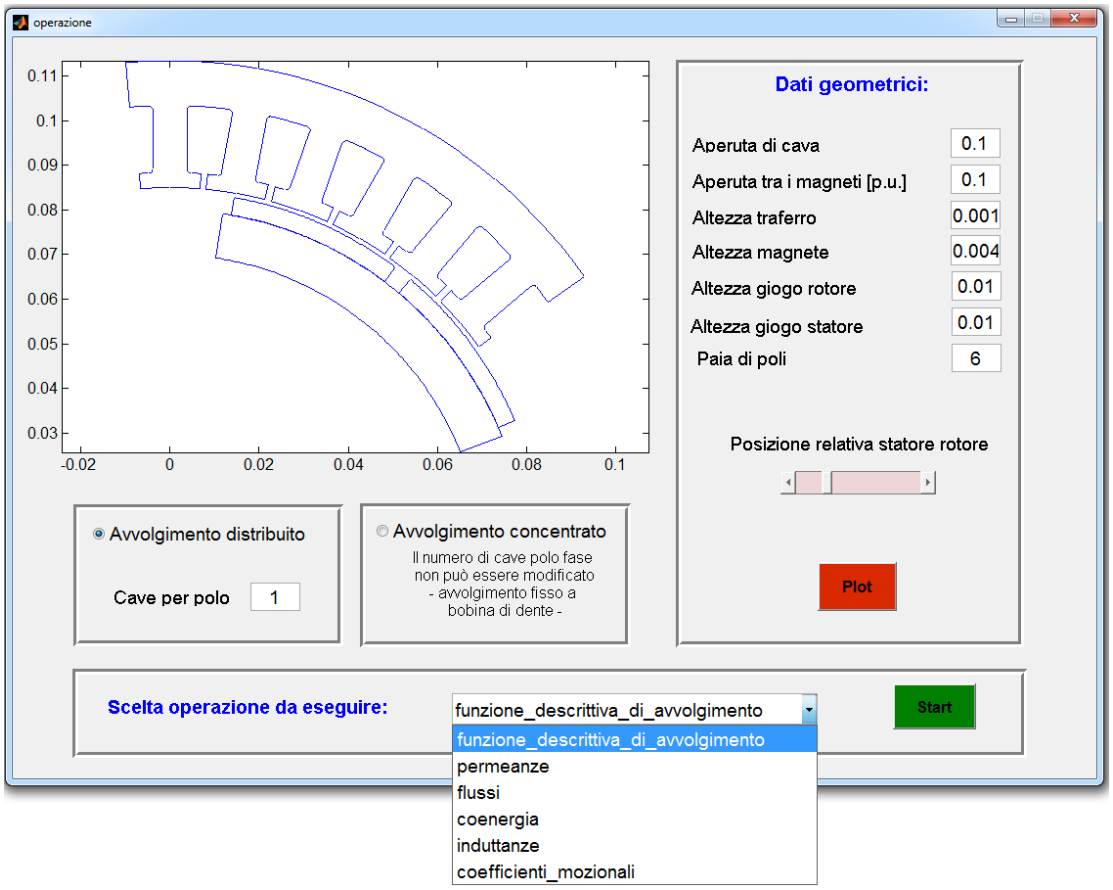
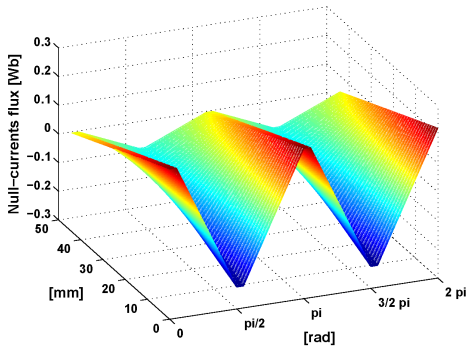


Figure 4.12: Top-view of the graphical interface

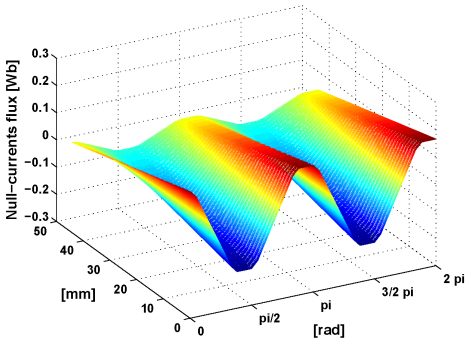
a machine featuring 2 pole pairs with a gap between magnets equal to 10% of the pole pitch and the following different configurations of teeth and winding:

- case 1: negligible slots openings (i.e. almost closed slots), 1 coil per phase per pole pair with full pole pitch;
- case 2: negligible slots openings, 1 coil per phase per pole pair with 2/3 pole pitch (coils wound around the teeth as nowadays usual in torque motors);
- case 3: negligible slots openings, 3 coils per phase per pole pair with full pole pitch;
- case 4: slots openings equal to 10% of slot pitch, 1 coil per phase per pole pair with full pole pitch.

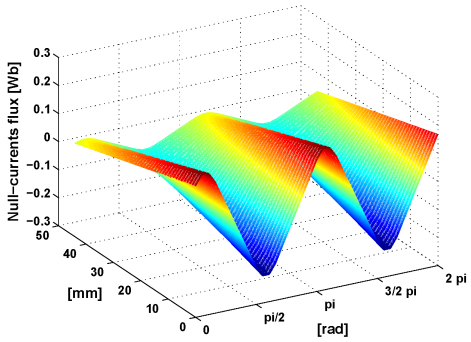
The trend of the null-currents flux linked with one of the phases of module B is reported in fig. 4.13 as a function of the angular and axial positions of the mover. The lower peak flux value achieved in case 2 due to the reduced pitch may be noticed, as well as the smoother trend vs. angular position obtained in case



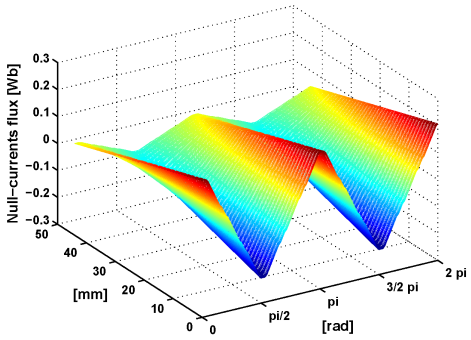
a. 1 coil, full pitch, closed slots



b. 1-coil, 2/3 pitch, closed slots

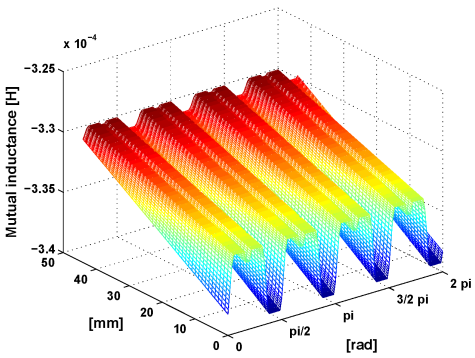


c. 3-coils, full pitch, closed slots

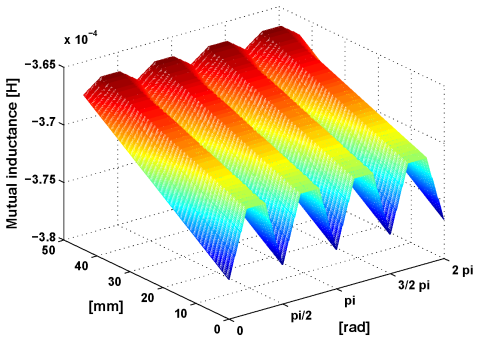


d. 1-coil, full pitch, 10% open slots

Figure 4.13: Null-currents flux [Wb] vs. positions [mm], [rad]

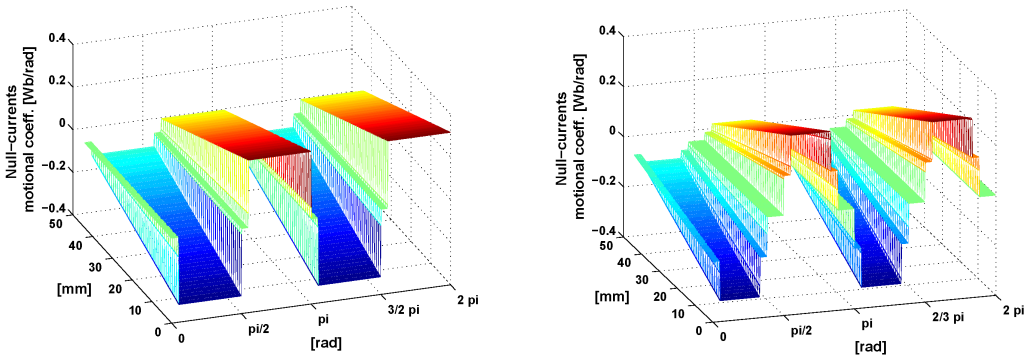


a. 1-coil, full pitch, 10% open slots



b. 3-coils, full pitch, closed slots

Figure 4.14: Mutual inductances vs. position [H] vs. positions [mm], [rad]



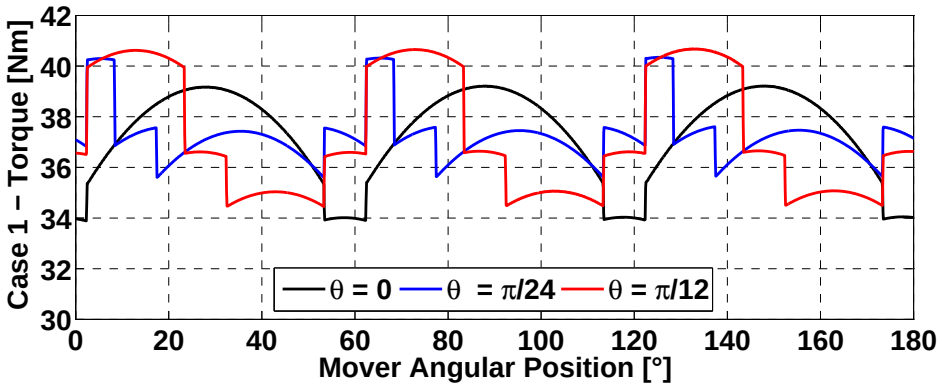
a. 1 coil, full pitch, closed slots

b. 1-coil, 2/3 pitch, closed slots

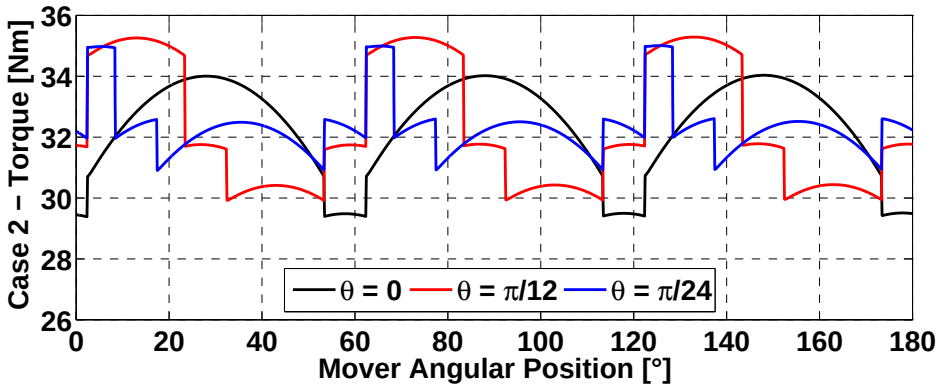
Figure 4.15: Null-currents motional coeff. [Wb/rad] vs. positions [mm], [rad]

3 thanks to the multiple coils per pole pair adopted; the effects of slots openings may be appreciated by comparing case 1 and case 4. For cases 1 and 2, the trend of a null-currents rotational motional coefficient vs. positions is reported in fig. 4.15 for a phase in module B: the null values due to the gaps between magnets may be noticed, as well as the lower values in case 2. Finally, the trend of mutual inductances between 2 phases in section B is reported in fig. 4.14 for cases 3-4, showing the effect of slots openings. The implemented model may be also used to estimate the actual force and torque generated under different supply conditions. In fact, referring for example to the minimal total resistive losses strategy previously recalled, at fixed axial position and constant angular speed the reference current waveforms result sinusoidal for any given wrench. Nevertheless, in practice supplying the machine with such waveforms may still give rise to torque and force profiles affected by some ripple due to the various non-ideal aspects such as winding structure, slots openings etc. The ripple in the total wrench acting on the mover is also affected by the relative angular position of the 2 stator modules, which may be then used as a further design parameter to minimize this disturbance, yet the effectiveness of this remedy depends on the mover axial position and on the supply strategy adopted. By means of the above type of analysis, the equivalent magnetic circuit model developed permits also to single out specific current-position mapping functions aimed to reduce the resulting ripple by applying suitable shaping adjustments to the ideal sinusoidal currents waveforms. As qualitative examples, some results referred to the minimum Joule losses strategy with mover located in central position are reported hereafter for the first 3 machine configurations above considered.

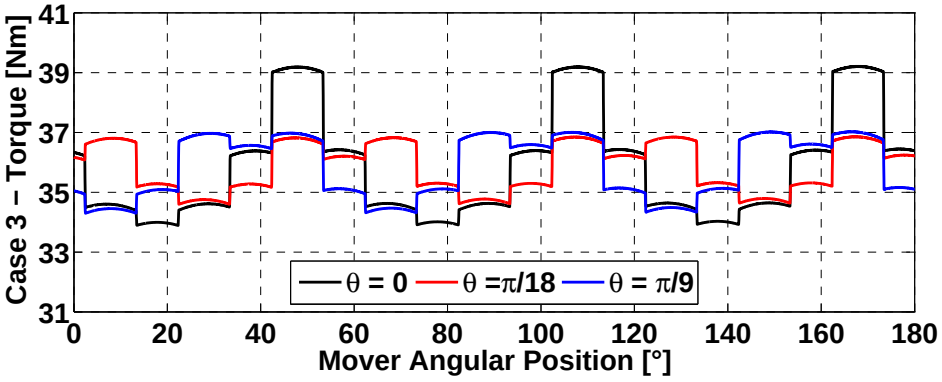
In particular, in fig. 4.16 the trend of torque waveforms generated under null reference force is reported for 3 different values of angular shift between stator



a. 1-coil per phase per pole pair with full pole pitch

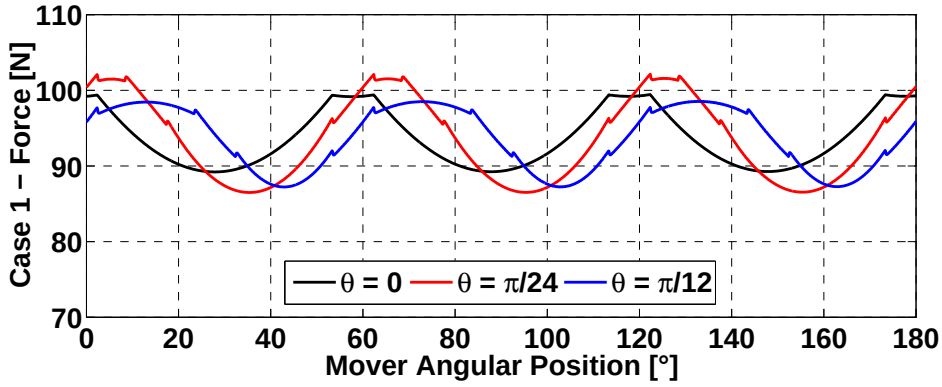


b. 1-coil per phase per pole pair with 2/3 pole pitch

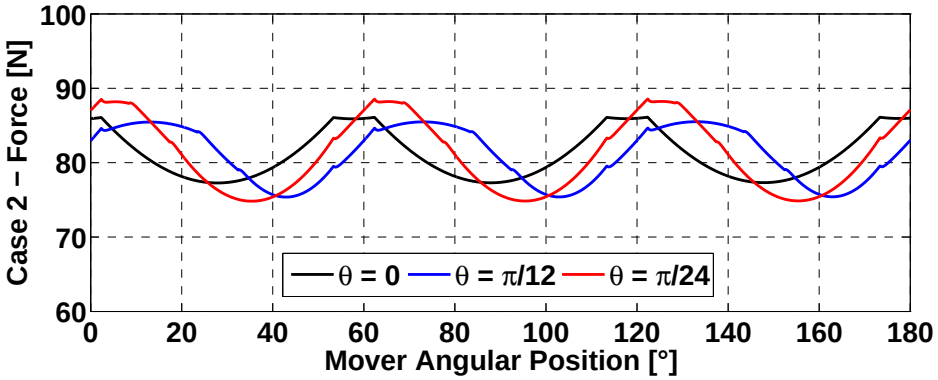


c. 3-coils per phase per pole pair with full pole pitch

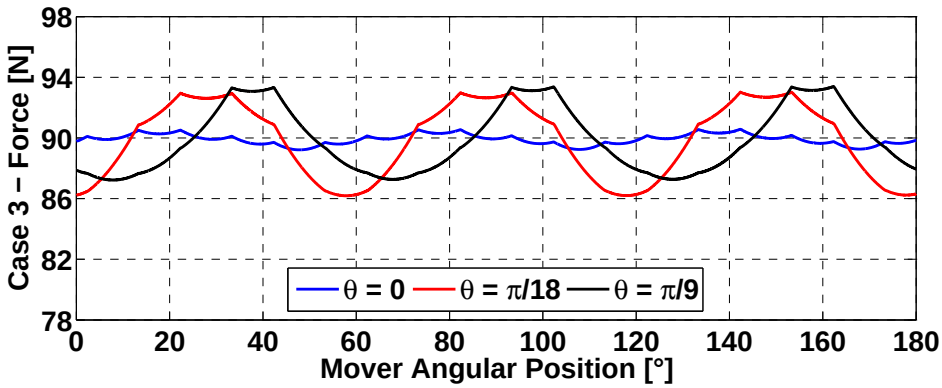
Figure 4.16: Torque vs. angular position at null force for 3 angular shifts



a. 1-coil per phase per pole pair with full pole pitch



b. 1-coil per phase per pole pair with 2/3 pole pitch



c. 3-coils per phase per pole pair with full pole pitch

Figure 4.17: Force trend vs. angular position at null force for 3 angular shifts

modules. As expected, the average torque achieved in case 2 (tooth-wound coils) results lower, whereas case 3 provides the smallest ripple with a lower performance loss thanks to the use of 3 coils per pole pair. It may be also noticed that in all configurations the torque ripple is significantly affected by the shift angle, as expected. Analogously, in fig. 4.17 the trend of force vs. angular position generated under null reference torque is reported for 3 different values of angular shift between stator modules. The small ripple achieved in case 3 with aligned stators may be noticed, as well as the lower convenience of phase shifting in the considered cases for what concern force ripple reduction.

4.6 Conclusions

Despite their potential interest in several applications, rotary-linear electric machines are not yet diffused because either requiring unconventional and expensive manufacturing processes, or resulting difficult to control effectively. A novel machine structure was recently proposed as purposely designed to use common processes while ideally achieving a linear controllability. The machine description, as well its theoretical analysis, and its FEM modeling, are presented in detail in [40], [41], [42]. In this chapter, after recalling the machine characteristics and its main regulation criteria, a simulation model based on the theoretical sinusoidal analysis of the machine was described referring to its implementation in the Matlab-Simulink® environment. Simulation results referred to a potential application requiring the control of angular speed and axial position were then reported and commented. Such results confirmed the conceptual possibility to get ready effective rotary-linear drives using the proposed machine. A more accurate model of the proposed machine, based on the equivalent magnetic circuit approach, was then presented referring to wise simplifying hypotheses. The implementation of such model in the Matlab environment as a fully parametric script function was then described. Finally, numerical results provided by such model were presented concerning both the equivalent circuital parameters of machines featuring different configurations and the ripple actually affecting the wrench profiles under ideal supply conditions. Such results highlighted the influence of several design parameters on the actual performances of the machine, confirming the usefulness of an intermediate level model permitting to quickly estimate the main effects of design choices before undertaking a more detailed FEM analysis requiring a much higher computational effort. The possibility to use such model to wisely amend the ideal current supply profiles aiming to reduce ripple was finally highlighted.

Chapter 5

Modeling and Analysis of a Consequent-Pole Brushless Machine

5.1 Introduction

Brushless permanent magnet synchronous machines probably constitute nowadays the leading typology in electric machinery, being more and more employed in a mess of applications ranging from industrial drives to electric propulsion and wind turbines. To better address the widely different goals and requirements of such applications, many variants of such machines were proposed, mostly concerning specific features of the rotor structure. Under such point of view, 4 main typologies of brushless machines may be found in the literature, as below recalled.

In the simplest typology, i.e. the *surface magnets machine* (SM), the magnets feature an about sector-hollow-cylindrical shape and are attached on the external surface of the cylindrical ferromagnetic yoke, which is supported by the mechanical shaft (e.g. [43], fig. 5.1). They directly face the main airgap, featuring a basically radial magnetization pattern. For low to mid speed applications, the magnets may be simply glued onto the yoke; when they also feature constant thickness and uniform magnetization, the rotor results then very simple and inexpensive to manufacture. Nevertheless, when the usual inner-rotor layout is used and the centrifugal forces become significant, the employ of a sleeve, bandage or set of metallic rings becomes necessary to keep in place the magnets (e.g. [44]). Moreover, even when modern rare-earth magnets are employed, the average flux density in the airgap results rather low with respect to the capability of commonly used silicon-iron laminations. This implies that the volumetric specific performances may result not much high and that the stator teeth often result either oversized

or relatively narrow, leaving rather large slots that may turn out less effective in permitting to achieve a good filling factor thus ultimately resulting oversized.

In the second machine typology, *permanent magnets* are suitably *buried* within the rotor core (BM machines). Usually, the magnets feature a simple brick shape with uniform magnetization pattern parallel to the smallest edge to minimize costs. Depending on the arrangement of the magnets, 3 main variants of this typology may be identified: polygonal, radial or star layout (e.g. [45], see fig. 5.3). The magnetization directions are alternated inward-outward for adjacent magnets in the polygonal variant and for adjacent couples of magnets in the star variant, while they are alternated clock- and counterclock-wise for adjacent magnets in the radial variant. The star layout may be then considered as derived from any of the other 2 variants by splitting in 2 each of the magnets. In any case, the magnets are surmounted by suitably shaped ferromagnetic poles that keep them in place while facing the main airgap. When suitably designed, BM machines may feature both an anisotropy torque component and a rather high airgap flux density due to the flux concentration effect, besides offering a better protection and retention of magnets. Nevertheless, the pole expansions must be connected to the shaft: for convenience and space reasons, this is often achieved by means of relatively narrow links to the yoke made up of the same material, leading to local magnetic saturation and to a not much robust structure. In any case, BM machines result more complex and sophisticated to design, manufacture and control, thus turning out usually more costly.

The third rotor typology features the *inset magnets layout* (IM machines), which may be derived from the SM type by using magnets whose tangential width is smaller than 1 pole pitch, thus leaving gaps between them that are occupied by pole expansions protruding from the yoke (e.g. [46], fig. 5.2). Usually, both magnets and poles feature the same external cylindrical shape, thus leading to a smooth rotor surface, while the magnets thickness is constant as well as the radial magnetization strength. Such structure features then a robust and still relatively simple rotor core. Moreover, it provides a better mechanical protection and retaining of magnets even in case of simple gluing, as glues react much better to the shear stress arising on the lateral surfaces of magnets than to the tensile stress arising on the back. Finally, the rotor core provides a preferential path for main field lines via the poles interposed between magnets: referring to the popular approximated sinusoidal model, the machine features then a quadrature inductance larger than the direct inductance. This fact facilitates the use of such machines for applications requiring a wide field-weakening operation range.

A fourth rotor structure, which is described more in detail in the following

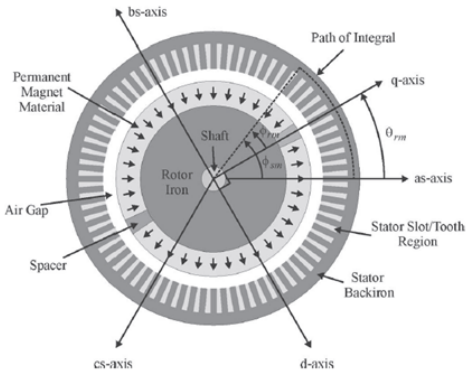


Figure 5.1: Surface magnets type

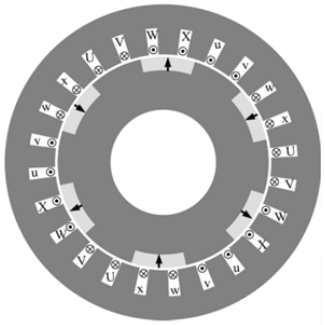
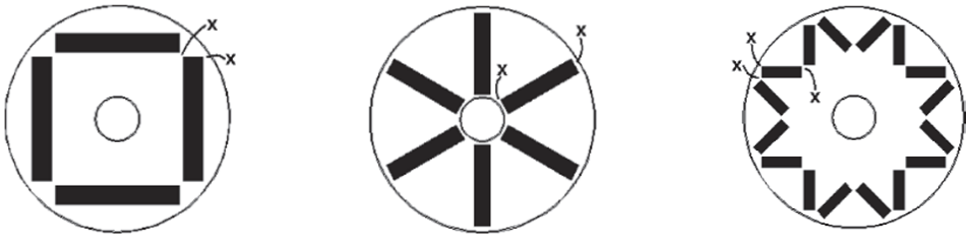


Figure 5.2: Inset magnets type



(a) (b) (c)

Figure 5.3: Buried magnets types: a) polygonal, b) radial, c) star

section, consists in the *consequent-poles type of IM typology*. Such machine was not much investigated till now in the literature, keeping substantially unaltered the basic characteristics of the initial concept while mainly focusing on a few advanced additional features such as field regulation [47] or magnetic bearingless suspension [48, 49, 50, 51], both achieved by means of additional elements, respectively a dual rotor layout and auxiliary stator coils. Hereafter the opportunity to adjust the basic design layout of consequent pole machines aiming to reduce volume and weight by better exploiting the magnetic potential of silicon-iron laminations used for the cores is investigated. The mid-complexity machine model based on the reluctance network analysis, already presented in the previous chapter, is used in order to investigate the main aspects of the machine design.

5.2 Inset Consequent Pole Machines

The consequent-pole permanent magnets synchronous machine (CP) is characterized by a rotor structure that may be considered as a modified IM type where all of the magnets feature the same magnetization pattern, e.g. radial outward, while the poles separating them feature a rather large tangential width, typically just the same as the magnets (e.g. [48], fig. 5.4). This way, the usual alternated

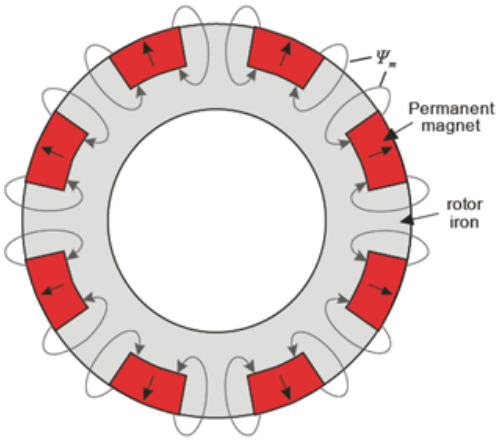


Figure 5.4: Rotor structure for a consequent pole machine

sequence of magnetic poles facing the main airgap in the basic SM typology is achieved again as a consequence of the rotor structure. In fact, at null currents each main flux line crosses twice the main airgap, leaving a magnet towards the stator and entering back the rotor via one of the adjacent poles. In this machine, the number of magnets, as well as the number of rotor poles, equals then the number of pole pairs, instead of the number of poles as usual. Moreover, since modern magnets feature a differential permeability close to air, it turns out that the rotor core exhibits a clear anisotropy yet with a spatial period equal to 2 pole pitches instead of 1. With respect to IM structure, CP machines feature then analogous or even better levels of rotor robustness and manufacturing simplicity when the shape of magnets is kept sector-hollow-cylindrical: in fact, the number of magnets and rotor poles is halved for any given number of pole pairs. Anyway, at least another aspect of potential interest may be singled out, which was not much investigated till now. In SM machines, the level of flux density that may be achieved in the airgap portions facing the magnets is relatively limited with respect to BM machines. In fact, even the best NdFeB magnets available nowadays exhibit a remanence (about 1.45 T at 20°C) somewhat smaller than the flux density permitted by normal silicon iron laminations. In practice, flux density values as low as 0.5 T may be then achieved with utilization levels of the magnets quite compatible with their properties, whereas values usually ranging in the interval $0.8 - 1.5$ T are commonly adopted for the peak airgap flux density in other machines featuring isotropic stator core; even higher values are used in doubly-salient variable reluctance machines. As a result, SM machines result inherently more suited for designs featuring relatively large diameter and rather narrow and short teeth with comparatively wide slots, thus possibly leading to a poor uti-

lization of the occupied volume and eventually to larger, heavier and ultimately more expensive active parts. When the basic criterion till now mainly considered in the literature is applied, CP machines are designed keeping basically equal the angular widths of magnets and poles as typical of SM machines, i.e. $\beta_M = \beta_P$. In such case, at null currents the average airgap flux density results basically the same both in front of the magnets and above the rotor poles, thus incurring in the same issues previously highlighted. Nevertheless, since in CP machines half of the magnets are removed with respect to SM machines, the flux density above the expansion poles replacing them may be increased to better exploit the potential of the ferromagnetic parts. This may be achieved by adopting an uneven width ratio, i.e. using rotor poles having a smaller angular width than the magnets, which in turn span then over more than 1 pole pitch. Consequently, it may be argued that for any given tangential size of the magnets the total circumferential size of the rotor, and thus its diameter, may be reduced with respect to the related basic SM design, ultimately permitting to increase the specific performances provided that the whole machine design is properly revised. Alternatively, it may be possible to redesign the machine achieving higher performances while keeping the same rotor diameter.

Referring to the usual idealized approximated scenario, and considering at first the null-currents condition, the same value of main flux Φ crossing any magnet also crosses any expansion pole: therefore, one has

$$B_M \cdot \beta_M \cdot r \cdot l = \Phi \cong B_P \cdot \beta_P \cdot r \cdot l \tag{5.1}$$

where l is the machine axial length, β_M, β_P are the angular widths of magnets and expansion poles and B_M, B_P are the average flux density values in their mean sections, which are assumed having cylindrical shape with equal radius r. Introducing the magnet vs. pole expansion width ratio ξ, which from 5.1 results also equal to

$$\xi = \frac{\beta_M}{\beta_P} = \frac{B_P}{B_M} \tag{5.2}$$

for a machine featuring p pole pairs one obtains then

$$\beta_P = \frac{2}{1+\xi} \cdot \frac{\pi}{p} \qquad\qquad \beta_P = \frac{2 \cdot \xi}{1+\xi} \cdot \frac{\pi}{p} \tag{5.3}$$

With respect to any given SM machine reference design featuring the same magnet tangential size τ_M, a first raw estimation of the possible size shrinking benefit may be then realized by considering the ratio of the rotor radiuses in the 2 cases, which in turn is approximately given by

$$\rho_R = \frac{r_{R_C P}}{r_{R_S M}} \approx \frac{p \cdot (\tau_M + \beta_P \cdot \tau_M / \beta_M)}{2 \cdot p \cdot \tau_M} = \frac{1+\xi}{2 \cdot \xi} \tag{5.4}$$

Under the point of view above considered, a reasonable intermediate value of the width ratio and the resulting rotor diameter shrinking factor may be estimated as

$$B_M \approx 0.65 \quad T \qquad B_P \approx 1.3 \quad T \quad \Rightarrow \quad \xi \approx 2, \quad \rho_R \approx 0.75 \tag{5.5}$$

therefore, in such scenario an appreciable size reduction of about 25% may be roughly estimated for the rotor, and thus possibly also for the whole machine. In any case, the reduction of the rotor diameter and mass leads inherently to a lower inertia, which may be appreciated in motors for high-dynamics applications. A qualitative sketch of the layout of such a machine is shown in fig. 5.5.

5.3 Considerations

Obviously, when deriving a CP machine with uneven magnet/pole width ratio from a given SM machine, several other design aspects must be also kept in mind. In particular, the possibility to shrink in equally effective way also the stator structure depends on the filling factor of slots in the SM design. In fact, when the cross section of stator teeth have to be enlarged to keep pace with the increased peak airgap flux density, the width of slots should be reduced. When this cannot be done without making them deeper to still permit hosting the winding, the external diameter of the stator core will not be reduced the same way as the internal diameter, thus possibly mitigating the actual benefits in terms of overall machine size shrinking. Moreover, the magnets sizing is also affected. In fact, at null currents the application of Ampere and Gauss laws, neglecting m.m.f. drops inside the cores and assuming thin airgap and magnets layers, provides for a SM machine the following approximated relationships

$$H_M \cdot \varepsilon_{MSM} + H_G \cdot \varepsilon_G \cong 0 \qquad B_G \cong B_M \tag{5.6}$$

correlating the average values of field strength H_M, H_G and flux density B_M, B_G respectively in the magnets and airgap. Assuming that the magnets feature a linear magnetic behavior with remanence B_R and differential permeability approximately equal to airgap μ_0, i.e.

$$B_G = \mu_0 \cdot H_G \qquad B_M \cong B_R + \mu_0 H_M \tag{5.7}$$

one obtains that achieving a given value of flux density in the magnets of such machine (or approximately in the airgap above them) requires a magnets thickness resulting

$$\varepsilon_{MSM} \cong \frac{\varepsilon_G}{B_R/B_M - 1} \tag{5.8}$$

In a CP machine with given width ratio ξ, at null currents the approximated expressions analogous to 5.6 become

$$H_M \cdot \varepsilon_{MCP} + H_{GM} \cdot \varepsilon_G + H_{GP} \cdot \varepsilon_G \cong 0 \tag{5.9}$$

$$B_M \cdot \beta_M \simeq B_{GM} \cdot \beta_M \simeq B_{GP} \cdot \beta_{GP} \tag{5.10}$$

where different values of field strength H_{GM}, H_{GP} and flux density B_{GM}, B_{GP} are considered in the airgap layers facing the magnet and the expansion pole. Assuming the same material properties 5.7, the magnet thickness required to achieve a given flux density results then given by

$$\varepsilon_{MCP} \cong \varepsilon_G \cdot \frac{B_P + B_M}{B_R - B_M} = \varepsilon_G \cdot \frac{(1+\xi)}{(B_R/B_M - 1)} \tag{5.11}$$

Therefore, when the airgap thickness and the remanence and circumferential width of magnets are kept about the same, achieving the same magnets flux density in a CP machine with uneven width ratio requires a total volume of magnets resulting larger than in the basic SM machine by a factor

$$\gamma_M \cong \frac{p \cdot \tau_M \cdot \varepsilon_{MCP}}{2 \cdot p \cdot \tau_M \cdot \varepsilon_{MSM}} \cong \frac{1+\xi}{2} = \xi \cdot \rho_R \tag{5.12}$$

For example, in the condition 5.5 one has then $\gamma_M \approx 1.5$. Anyway, nowadays the good performances of rare-earth materials often lead to use in SM machines rather thin yet large magnets, possibly incurring in mechanical issues. Therefore, using half the number of magnets all featuring the same characteristics (including magnetization direction) and a wider thickness may turn out not much more expensive or even desirable, although the total weight is higher. On the other hand, the electromagnetic voltage waveforms are also modified. For example, referring to the condition 5.5 one cycle of the ideal waveforms of the voltages (V_1', V_1") induced at null currents and constant speed in a couple of conductors displaced by 1 pole pitch is shown in fig. 5.6, resulting not alternative (yet with null average value) due to the flux concentration effect determined by the rotor poles. The voltage V_1 for the coil composed by such conductors is also shown, as well as the corresponding waveforms V_2, V_3 induced in 2 coils displaced by $2\pi/3p$: the set may then constitute an elementary symmetrical 3-phase winding. It may be noticed that during each of the 6 intervals highlighted inside a period, 2 of the phases generate constant and opposite motional voltages, whereas the third voltage is null. Therefore, the above simple machine structure, featuring only 1 full-pitched coil per pole pair per phase, appears well suited to operate in a DC-brushless like mode, i.e. ideally using currents whose waveforms replicate the respective phase voltages. In fact, in such condition the torque provided by the machine would

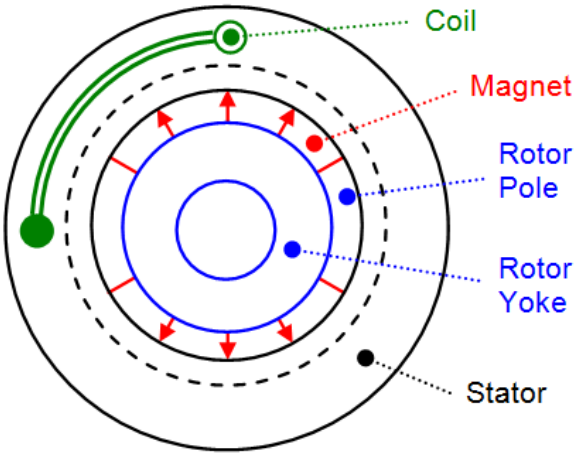


Figure 5.5: Qualitative layout of uneven CP machine with $p = 2$, $\xi = 2$

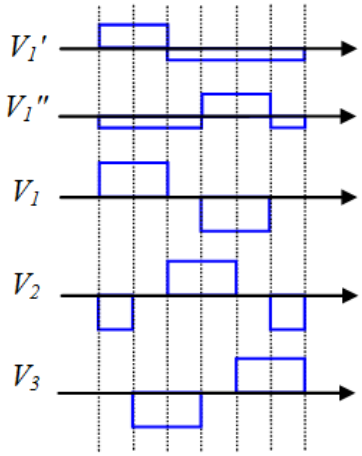


Figure 5.6: Ideal voltage waveforms in full-pitch coils for machine in fig. 5.5

be ideally constant, although in practice the reluctance effects due to the rotor poles would somewhat affect such basic behavior introducing a torque ripple and a voltage perturbation that shall be taken into account when actually designing the machine.

5.4 Machine Modeling and Analysis

An approximated analytical model of the CP machine with uneven width ratio was deduced basing on the equivalent magnetic circuit approach. Wise simplifying hypotheses were assumed as usual: in particular, m.m.f. drops inside the cores and leakage flux tubes were neglected, focusing on the main flux. Such tubes are assumed crossing the airgap with a radial trend, thus also neglecting the portions of rotor facing slots openings. Such magnetically linear model was then imple-

mented in a spreadsheet permitting to quickly analyse different configurations of the machine by estimating the main significant quantities, such as flux density values, voltages, torque etc. Such tool was then used to get ready a wise preliminary design for a given case study, referring to a mid-speed mid-size motor; the main characteristics of such machine are reported in tab. 5.1, giving rise to the geometrical layout shown in fig. 5.7. For the sake of brevity, the above model and the design criteria adopted are not described. Basing on the analytical model

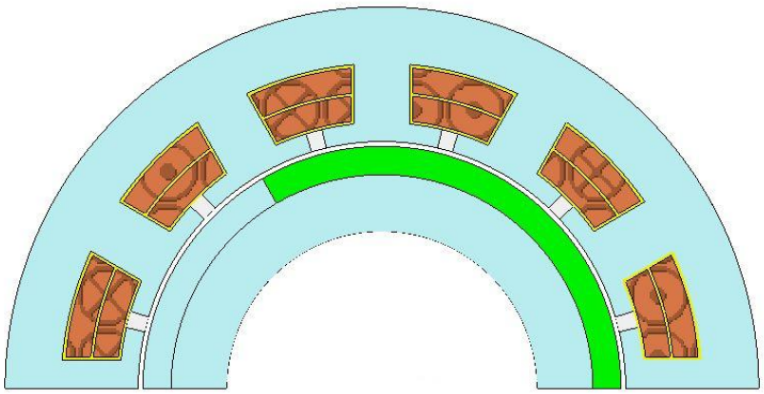


Figure 5.7: Geometrical model for the examined CP machine

Table 5.1: Main characteristics of the machine assumed as a case study

Rated power	10 kW	Rated speed	5 krpm
Rated pk voltage	200 V	Rated pk current	25 A
Pole pairs	2	Phases	3
Slots and Coils	12	Coils pitch	full
Turns per coil	12	Slot depth	12.5 mm
Slots opening	3.3 mm	Tooth head width	24 mm
External diameter	161 mm	Core length	145 mm
Rotor diameter	102 mm	Airgap thickness	1 mm
Mag./exp. w. ratio	2	Magnet remanence	0.62 T
Magnet rel. perm.	1.23	Magnet remanence	0.62 T

above recalled, a semi-ideal simulation model of the proposed machine typology was also get ready in the general purpose Matlab-Simulink® software environment, aiming to permit a more detailed dynamic analysis of the machine and to check different control strategies. The model was implemented in mixed form, using both a blocks part for high-level interactions and a core script to efficiently manage the solution of the equivalent magnetic circuit while achieving an effective parametrization permitting to easily adjust the machine data.

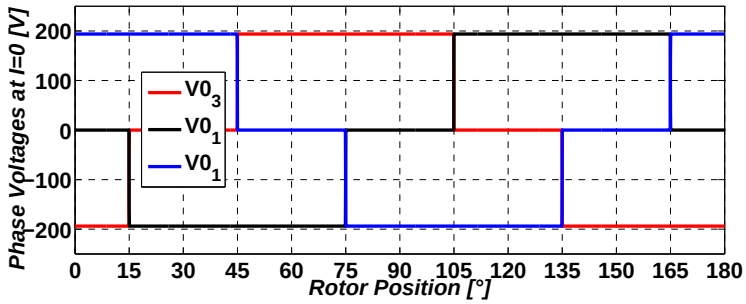


Figure 5.8: Phase voltages at null currents neglecting slots openings

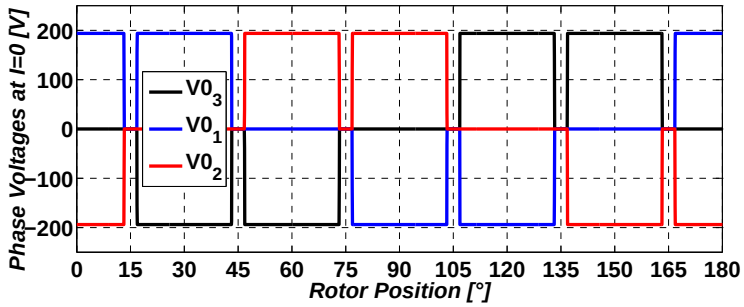


Figure 5.9: Phase voltages at null currents considering slots openings

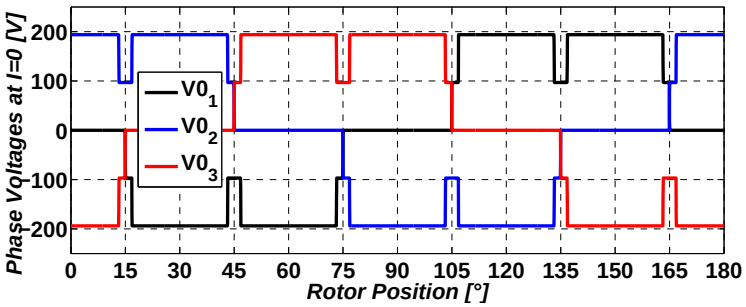


Figure 5.10: Average trends of phase voltages at null currents

Referring to the case study recalled in tab. 5.1, several simulations were carried out to investigate the machine behaviour. Since the actual machine operation is expected to be also affected by the main flux tubes originating from the portions of rotor facing slots openings, which are not accounted for by the model, 2 sets of simulations were first completed, respectively neglecting and considering the slots openings. The average of the results obtained in the 2 cases was then calculated, aiming to provide a more accurate estimation as the real behaviour of the modelled phenomena is expected to stay between the 2 results. In fig. 5.8, 5.9, 5.10 a period is reported of the waveforms of the phase voltages at null currents and rated speed, which are proportional to the null-currents motional coefficients: the 6-steps trend obtained neglecting slots may be noted, as well as the full dips introduced by the latter and the more realistic intermediate dips obtained by averaging.

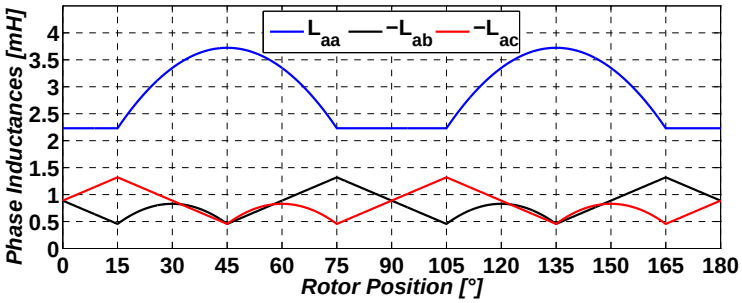


Figure 5.11: Self and mutual inductances trend neglecting slots openings

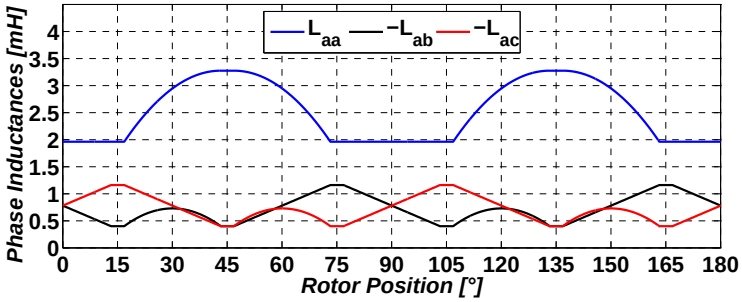


Figure 5.12: Self and mutual inductances trend considering slots openings

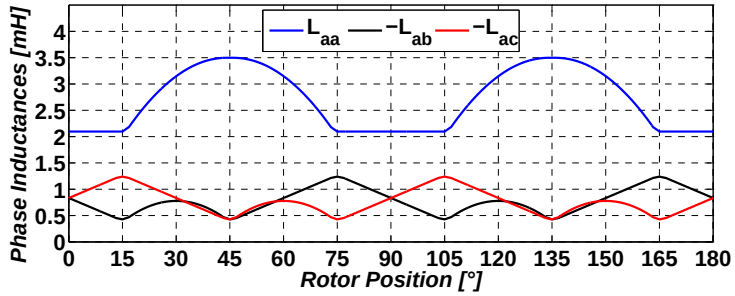


Figure 5.13: Average trend of self and mutual inductances

The trend of a phase self inductance and of the 2 complementary mutual inductances is reported in fig. 5.11, 5.12, 5.13, reversing the sign of the latter for better clarity. The ideal effects of slots openings may be noticed, determining both lower absolute values of inductances and a constant trend just in the intervals where the motional coefficients are null. The average quantities obviously exhibit intermediate trends. The electromagnetic torque was calculated according to the theoretical approach in [52], i.e. by summing 3 terms: the null-currents term, arising only when the slots openings are considered making anisotropic the stator core; the term related to null-currents fluxes, which depends linearly on currents; the term related to inductances variability, which depends on currents in quadratic way. Under ideal DC-brushless like 6-steps rated supply, i.e. constant current in each phase in the rotor position intervals where the related ideal motional

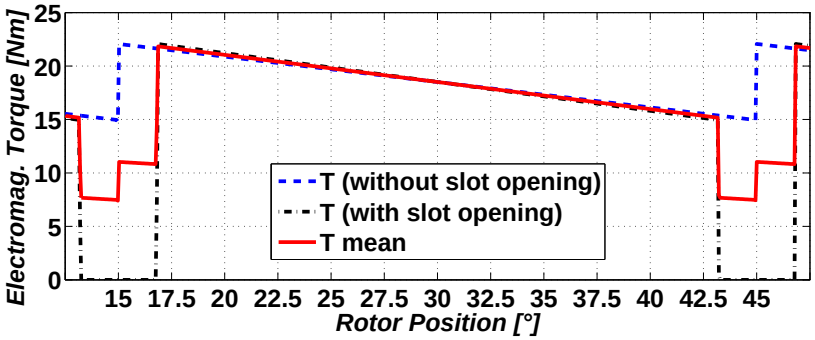


Figure 5.14: Torque profiles at rated currents: no slots, with slots, average

coefficient is not null, the trends of torque for the 2 analyzed cases and the related average trend result as shown in fig. 5.14. Within each of such basic intervals, an almost linear dependence of torque on rotor position may be noticed, with step variations at the boundaries of each sector due to reluctance effects.

5.5 Conclusions

The inset magnets typology of permanent magnets brushless synchronous machines presents some benefits in comparison to surface-mounted and buried magnets typologies. In the consequent poles arrangement, about the same magnetic flux flows both in any magnet and in any rotor pole expansion. As the average flux density inside magnets is usually rather lower than the max value acceptable from iron laminations, the opportunity to reduce the machine size by using an uneven angular width ratio between magnet and pole expansion was investigated. After some considerations about the advantages and disadvantages of such concept, a simplified analytical model based on the magnetic circuit approach was recalled as well as its implementation as a spreadsheet for design purposes and as a parametric model for simulation. Referring to a case study, simulation results were reported under different analysis hypotheses about slots openings.

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