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DESIGN OF SMART SENSORS FOR DETECTION OF PHYSICAL QUANTITIES

Autore:

Michele Dei

Relatori:

Prof. Paolo Bruschi

Ing. Massimo Piotto

Prof. Andrea Nannini

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ABSTRACT

Microsystems and integrated smart sensors represent a flourishing business thanks to the manifold benefits of these devices with respect to their respective macroscopic counterparts. Miniaturization to micrometric scale is a turning point to obtain high sensitive and reliable devices with enhanced spatial and temporal resolution. Power consumption compatible with battery operated systems, and reduced cost per device are also pivotal for their success. All these characteristics make investigation on this filed very active nowadays.

This thesis work is focused on two main themes: (i) design and development of a single chip *smart flow-meter*; (ii) design and development of *readout interfaces* for capacitive micro-electro-mechanical-systems (MEMS) based on capacitance to pulse width modulation conversion.

High sensitivity integrated smart sensors for detecting very small flow rates of both gases and liquids aiming to fulfil emerging demands for this kind of devices in the industrial to environmental and medical applications. On the other hand, the prototyping of such sensor is a multidisciplinary activity involving the study of thermal and fluid dynamic phenomenon that have to be considered to obtain a correct design. Design, assisted by finite elements CAD tools, and fabrication of the sensing structures using features of a standard CMOS process is discussed in the first chapter. The packaging of fluidic sensors issue is also illustrated as it has a great importance on the overall sensor performances. The package is charged to allow optimal interaction between fluids and the sensors and protecting the latter from the external environment. As miniaturized structures allows a great spatial resolution, it is extremely challenging to fabricate low cost packages for multiple flow rate measurements on the same chip. As a final point, a compact anemometer prototype, usable for wireless sensor network nodes, is described.

The design of the full custom circuitry for signal extraction and conditioning is coped in the second chapter, where insights into the design methods are given for analog basic building blocks such as amplifiers, transconductors, filters, multipliers, current drivers. A big effort has been put to find reusable design guidelines and trade-offs applicable to different design cases. This kind of rational design enabled the implementation of complex and flexible functionalities making the interface circuits able to interact both with on chip sensors and external sensors.

In the third chapter, the chip floor-plan designed in the STMicroelectronics BCD6s process of the entire smart flow sensor formed by the sensing structures and the readout electronics is presented. Some preliminary tests are also covered here.

Finally design and implementation of very low power interfaces for typical MEMS capacitive sensors (accelerometers, gyroscopes, pressure sensors, angular displacement and chemical species sensors) is discussed. Very original circuital topologies, based on chopper modulation technique, will be illustrated. A prototype, designed within a joint research activity is presented. Measured performances spurred the investigation of new techniques to enhance precision and accuracy capabilities of the interface.

A brief introduction to the design of *active pixel sensors* interface for hybrid CMOS imagers is sketched in the appendix as a preliminary study done during an internship in the CNM-IMB institute of Barcelona.

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1. DESING AND DEVELOPMENT OF INTEGRATED THERMAL SENSORS FOR GAS AND LIQUID FLOW SENSING

1.1 MEMS and integration technology

Since Feynman's challenge in the famous lecture in 1959 [1], a great effort has been put in technology research to master micrometer scale and nanometer scale physics in order build sophisticated devices. Micro-electro mechanical systems (MEMS) belong to that class of devices, and, nowadays MEMS market represents a profitable and prominent field in electronic industry, with a projection of increasing leverage in the following years [2].
Their remarkable economical impact, commented in Fig.1.1 have been achieved, so far, thanks to consumer electronics products, such as game controllers, digital cameras, camcorders, MP3 players, personal navigation devices etc. At the same time the word “MEMS” begins to be part of common spoken language thanks to frequent articles in daily newspapers regarding MEMS tailored to more and more specialized applications (flying micro-robots, smart dust, wearable computers and silicon micro-surgery).
MEMS technology initially developed from the well consolidate IC technology, using the same technological procedures such as: deposition, epitaxy, thermal oxidation, implantation, sputtering, casting, etching where layers are patterned using photo-lithography, inheriting one of the most important aspects of economical success: the possibility of batch fabrication techniques similar to those used for integrated circuits. Furthermore possibility to integrate these electromechanical elements together with electronics allows the implementation of a system able to

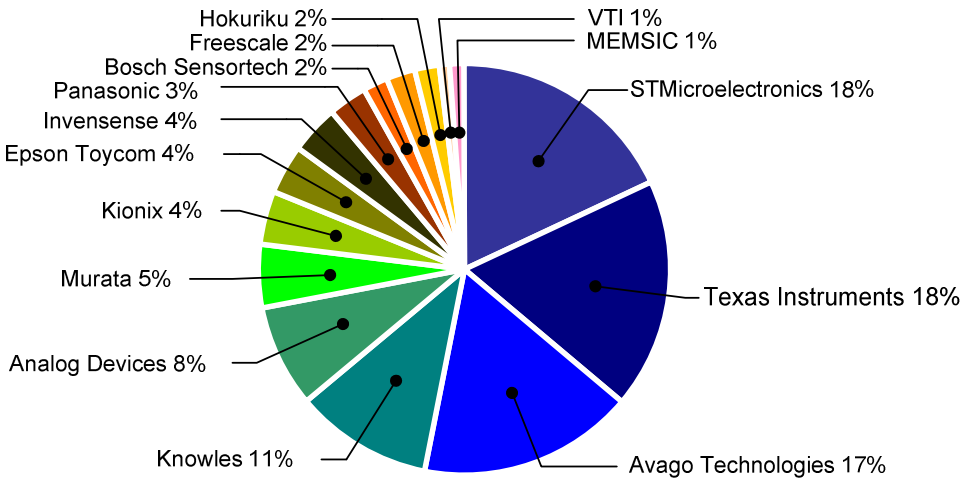


Fig. 1.1 – Ranking of companies in the global consumer/mobile MEMS market in 2008. Data are taken from [2]. The market forecast society iSuppli predicts that MEMS market will increase to 2.4 billion dollars in 2012, up from scarcely 1 billion dollars in 2006.

accomplish complex functionalities, usually referred to as system-on-a-chip.
Anyway it should be also pointed out that MEMS technology is not solely about making things out of silicon; nowadays MEMS technology evolves and includes also non-standard techniques in IC processing such as anodization, or Silicon-Germanium deposition in order to strive for new applications and/or better performances. The term micromachining is referred, in this respect, to all the techniques used to fabricate MEMS.
On the other hand, the term MEMS, in a strict sense, depicts a micron scale transducer device that links mechanical and electrical quantities. Anyway, it has become common to indicate with MEMS all sort of micron scale devices which are able to detect or to perturb same kind of physical quantity (mechanical, thermal, biological, chemical, optical, and magnetic phenomena) producing an electrical signal or controlled by an electrical signal. These two functions can be accomplished by MEMS sensors or MEMS actuators, respectively.

1.2 Integrated flow-meters

Dealing with a flow of fluid can be misleading unless the issue of physical quantities is not clarified: a fluid flow can be either a gas flow or a liquid flow. Among others quantities, a fluid flow can be measured in terms of amount of moved mass (weight per unit time), moved distance (meters per unit time), moved volume (volume per unit time). Anyway in this work we will consider preferably two principal units of measurement: the standard cube centimer per minute (sccm), when dealing with gasses, and the milliliter per minute (ml/min) when dealing with liquids.
A variety of conventional macroscopic flow sensors exist, but they are often of little use in the micro domain. Limited sensitivity, large size and high dead volume restrict their use for some specific applications, especially in the very low flow regimes. On the other hand, microfabricated devices offer the benefits of high spatial resolution, fast time response, integrated signal processing, and potentially low costs. A crucial issue is power consumption especially when aiming to battery-powered systems: in this respect, micro-scale flow meters typically outperform the macroscopic counterpart. They have recently matured from the research stage to commercial applications (see for example: Sensirion AG, Honeywell, Bosch, SLS Micro Technology) and are now real competitors for conventional sensors.
The automotive industry has been, and is still one of the major driving forces for MEMS-based sensors. In the last years the number of sensors in engine control applications, is constantly increasing [3]. Micro flow-meters are essential in the electronic fuel injection systems where it is needed to know the mass flow rate of air sucked into the cylinders to meter the correct amount of fuel [3–5].
Other areas of application are in pneumatics, bioanalysis [6], metrology (wind velocity and direction [7, 8]), civil engineering (wind forces on building), the transport and process industry (fluidic transport of media, combustion, and vehicle performance), environmental sciences (dispersion of pollution), medical technology (respiration and blood flow, surgical tools [9]), indoor climate control (ventilation and air conditioning [10]), and home appliances (vacuum cleaners, air dryers, fan heaters). Due to their very small pay-load, integrated flow sensors represent a optimal alternative also in space applications: they have been yet used as within

measuring instruments for space scientific experiments and control the mass of propellant expulsed by thrusters.
The first micromachined flow sensors were presented by van Putten et al. [11] and van Riet et al. [12] in 1974. They used the thermal domain as the measurement principle. In principle, a large variety of physical principles other then thermal can be used to detect fluid flows, but most of them are not suitable for integration. In this respect, thermal flow-meters are to be preferred for their mechanical simplicity, absence of moving parts, high sensitivity and relative robustness.
In the next sessions we will briefly review some mechanical flow sensors and than we will illustrate the more popular thermal flow sensors. More sophisticated (and complicated) revealing methods, such as Coriolis force sensors, fluid imaging and optical flow sensing are not covered here and are beyond the aim of this thesis. The interested reader can find more on these topics in references [13, 14].

1.2.1. Mechanical flow sensors

Sensing of a flow rate can be achieved through electro-mechanical transduction of the forces of the fluid applied to a solid element. Although a lot of different and sophisticated methods of interaction between the fluid and a solid body can be exploited, in principle, to the sensing purpose, some of them are impracticable for integration at the micron range scales. Here, we resume some of the most popular types of mechanical flow sensors: (i) pressure difference sensors, (ii) drag force sensors and (iii) lift force sensors.
Pressure difference sensors rely on the measurement of the differential pressure P in a flowing fluid. Pressure sensors can be used to measure flow by sampling the pressure drop along a flow channel with known fluidic resistance, R_f, and calculating the flow Q from the fluidic equivalent to Ohm's law: $Q = \Delta p/R_f$. It is comparable to measuring the current (Q) in an electric circuit by sensing the voltage drop (Δp) over a fixed resistance (R_f).

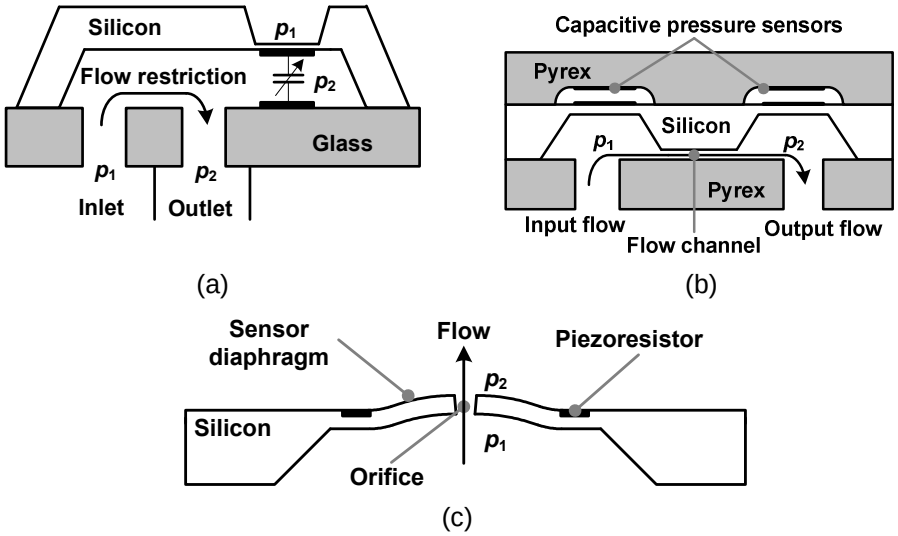


Fig. 1.2 – Pressure Difference sensors for flow measurements. Pressure difference $\Delta p = p_2 - p_1$ is transformed into electrical signal using: (a) deflecting membrane capacitive technique, (b) differential capacitive technique, (c) piezoresistive stress sensors.

Figure 1.2 shows three possible implementations of this technique. More details on capacitive sensors will be given in chapter 4 of this thesis. It is important to point out that all this kind of sensors needs to create a flow restriction in order to make R_f high enough and to produce a measurable pressure drop Δp across the channel. This represents an important flaw in many applications, such as anemometry for example, where little insertion pressure lost is desired.
On the other hand, drag and lift force flow sensor consists of a cantilever beam, or paddle, with an integrated strain gauge resistor. When the cantilever is immersed in a flowing fluid, a drag force is exerted resulting in a deflection of the cantilever, which can be detected by the piezoresistive elements incorporated in the beam. Figure 1.3(a,b,c) shows schematics of devices using this measurement principle.
A general disadvantage of the drag force flow sensors is the possible damage through high-speed particles, which can destroy the petit paddle suspension, or low-speed particles, which clog the fluid pathway and block the paddle in case of in-plane sensor arrangement. There is a trade-off between robustness and

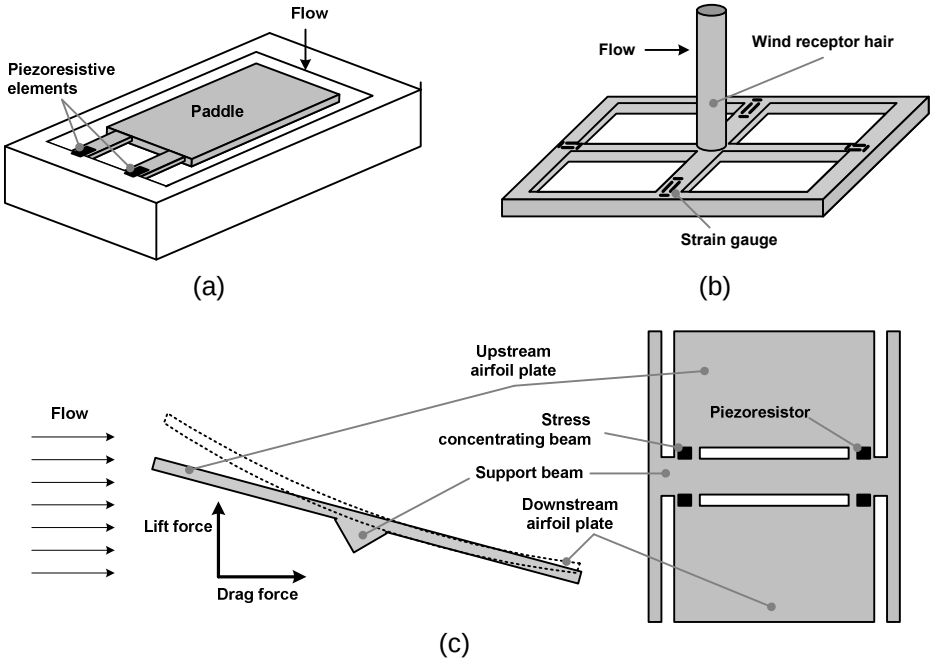


Fig. 1.3 – Examples of force driven flow sensors: (a) in-plane drag force flow sensor, (b) out-of-plane drag force flow sensor, (c) lift force sensor.

sensitivity of the sensor. However, the chip size is generally smaller than the pressure difference flow sensors. These sensors, like the pressure difference sensor of the preceding section, do not induce heat to the fluid, which could represent an advantage in some applications.

1.2.2. Thermal flow sensors

Integrated thermal flow sensors fabricated through micromachining technology present, respect to the mechanical counterpart, structural and electronic simplicity. Furthermore it has been largely demonstrated that it is possible to get high

performance sensor starting from standard CMOS IC process and adding some post-CMOS micromachining and/or some deposition technique [15]. For this reason, the overwhelming majority of micro flow sensors work in the thermal domain. In this respect we have to point out some requirements of CMOS solid-state sensors:

i. Use the materials provided by the CMOS IC process.
ii. Exploit the thermal (and coupling) effects inherent in the CMOS materials.
iii. Design structures that bring out the transducer effects, but within the limits of the CMOS and post-CMOS fabrication rules (which are broader than the conventional CMOS IC design rules).

CMOS materials include bulk silicon, polysilicon (possibly both n- and p-doped), dielectrics (silicon oxide, silicon nitride, passivation), and metal (alloy with mainly aluminium). All these materials can serve as thermal mass. Silicon and metal conduct heat efficiently. The dielectric layers provide only moderate thermal isolation in view of their small thicknesses. That is why removal of material by micromachining is required for efficient thermal isolation.
The thermoresistive effect (Joule heating) makes it possible to use electrically conducting materials, such as polysilicon, for resistive heating which is the base for every thermal flow-meter. The temperature coefficient of resistivity is exploited for resistive thermometers: RTD and thermistors. The difference in Seebeck coefficients between different conducting CMOS materials (including differently doped silicon areas) is the basis of integrated thermocouples and thermopiles that will be illustrated at the end of this section. Finally, the different thermal expansion coefficients of different CMOS materials produce the bimorph effect, which can be exploited for the thermo-mechanical actuation of micromechanical structures.
All these thermal properties depend on doping and structure (mono- or polycrystalline) and as a consequence they heavily depend on the process. For example, the temperature coefficient of the resistivity of polysilicon can be positive or negative, depending on doping. Besides, sheet resistance, resistive temperature coefficients, major carrier density (*n* or *p* for semiconducting materials), Seebeck coefficients, temperature conductivity and specific heat represent the basis for thermal MEMS design. All of these properties are temperature dependent. Thermal flow sensors can be classified into three basic categories, schematically sketched in Fig. 1.4:

(a) **Hot wire/hot film anemometers**: they are thermal mass flow sensors which measure the effect of the flowing fluid on a hot body.
(b) **Calorimetric flow sensors**: they are thermal mass flow sensors which measure the asymmetry of temperature profile around the heater which is modulated by the fluid flow.
(c) **Time of flight sensors**: they are thermal mass flow sensors which measure the passage of time of heat pulse over a known distance.

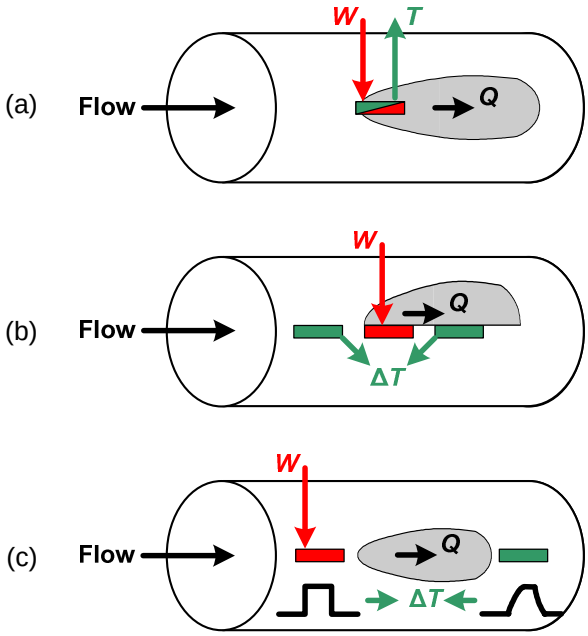


Fig. 1.4 – Schematic of the working principles of thermal flow sensors: (a) anemometer (heat loss), (b) calorimetric flow sensors (thermotransfer), and (c) time of flight sensors.

Hot wire/hot film anemometers exploit the effects of thermal conductance variation due to the fluid in motion. An ideal anemometer, i.e. with no heat losses on supports, obeys to the King's law:

$$G_T(v) = G_T(0)\sqrt{1+\beta v} \qquad (1.1)$$

Where $G_T(v)$ is the total thermal conductance seen by the wire/film as function of the flow velocity v, while β is a coefficient dependent by the fluid characteristics and the geometries of the sensor, usually empirically determined.
A micromachined anemometer is often formed by a suspended dielectric cantilever (hot wire) or membrane (hot film), while usually the sensing element is a patterned layer of platinum. Other materials can be used such as gold, polysilicon, and amorphous germanium; anyway platinum is the best choice in terms of chemical stability with temperature. The wire/film is driven to a temperature higher than the fluid temperature, justifying the name hot wire/film. The motion of the fluid forces a heat loss of the sensor as the total thermal conductance changes with eq. (1.1).
On the other hand, a temperature change influences the electrical conductivity of the wire/film offering the possibility to detect the fluid velocity through the relative electrical resistance variation. This technique can exploit the so called RTD (resistive temperature detector) devices.
The calorimetric principle illustrated in Fig. 1.4(b). For such arrangement, the heat source and the temperature probes are distinct and can be bipolar transistors, field

effect transistors or even diodes: all this devices offers a relevant sensitivity to temperature changes. Differently when used as pure electronic devices, high temperature sensitivity represents a good advantage here. Anyway, in order to obtain effective temperature isolation from the silicon substrate, large area of the chip has to be suspended and considerable technological difficulties arise.
The sensors presented in this thesis are based on a different thermal to electrical conversion principle, known as Seebeck effect, which is a reversible thermo-electrical phenomenon occurring when two jointed electrical conducting materials (metals or semiconductors) are submitted under a thermal gradient. In Fig. 1.5 a schematic representation is given, where the conductors A and B are jointed in two points each of them at a fixed temperature forming a so called thermocouple. The circuit has broken by the insertion of an ideal voltmeter which reveals a voltage difference ΔV.
The differential Seebeck coefficient (also called thermopower) is defined by:

$$\alpha_{AB} = \lim_{\Delta T \to 0}\left(\frac{\Delta V}{\Delta T}\right). \tag{1.2}$$

The coefficient α_{AB} is a function with the absolute temperature and is determined by the chosen couple of conductors A and B. It can be expressed by two distinct coefficients, α_A and α_B, called absolute thermopower of A and B, respectively:

$$\alpha_{AB} = \alpha_A - \alpha_B . \tag{1.3}$$

Seebeck coefficients of materials available in standard CMOS processes do not come through the few microvolt per centigrade. Typically thermocouples are electrically connected series in order to form a thermopile. A thermopile formed by N equal thermocouples, with all hot junctions well thermally coupled and all the cold junctions thermally coupled, present a global Seebeck coefficient equal to:

$$\alpha_{THERMOPILE} = N \cdot \alpha_{THERMOCOUPLE} . \tag{1.4}$$

In the next section we will illustrate more deeply the sensors used in this work that are based on the Bipolar-CMOS-DMOS version 6 (BCD6) process of STMicroelectronics.

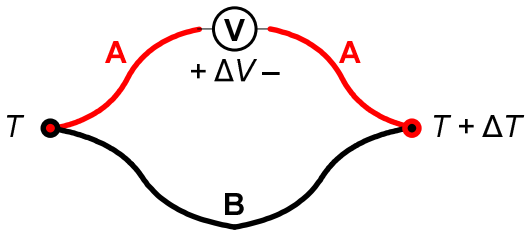


Fig. 1.5 – Schematic representation of a thermocouple. A and B are two conducting materials, V is an ideal voltmeter. Junctions are subjected to two different temperatures: the junction at $T + \Delta T$ is called hot junction, while the junction at T is called cold junction.

1.3 Design of an integrated calorimetric flow meter

Sensing principles described in Fig. 1.4 apply also for macroscopic thermal flow sensors. When dealing with micron scale silicon structures the problem of thermal insulation has to be coped, as all thermal sensing principles are based on the presence of some on temperature difference. Unfortunately, the high thermal conductivity of bulk silicon prevents the chip from large temperature gradients. Typically, a micromachining technological step is needed to obtain the suspension of hot elements in order to realize a physical separation of the latter with respect to the bulk. Once solved this technological problem, the integrated structures takes a substantial advantage with respect to the macroscopic thermal flow sensors in terms of:

(i) **Speed,** as it increase with the second power of typical geometrical features of the sensor; this can be qualitatively demonstrated considering, under small Biot number hypothesis, the thermal time constant RC is given by $R = L/(k \cdot A)$, $C = C_P \cdot L \cdot A$, where L is the length along heat exchange direction, A is the respective cross section, while k and C_P are the thermal conductivity and the specific heat at constant pressure of the material.

(ii) **Power consumption**, as very small thermal masses have to be heated.

(iii) **Miniaturization**, obviously. It is worth noting that miniaturization has a potential impact on sensor sensitivity, because the sensor can be introduced in very small cross section channels, allowing very low mass flows to be measured.

In a typical standard CMOS process the usable materials for the temperature sensing structures are: aluminium metal layers, polysilicon (*n* and *p*), unsiliced and silicided polysilicon. With these layers, it is possible to implement both thermisors and thermopiles. Until now an analytical comparison in presence of other constraints, such as dissipated power and area occupation, has not been done to the author knowing, anyway generally integrated thermistors are considered to be more sensitive with respect to integrated thermopiles. For example typical values for a n+polysilicon/p+polysilicon thermocouple are about 400 μV/K, while for for a n+polysilicon/aluminium thermocouple, values are stated below 100 μV/K; the temperature coefficient of resistance (TCR ≡ $\Delta R/R \cdot 1/T$) of a polysilicon strip can reach up to 0.5 %/K.

On the other hand, thermopiles are offset-free temperature sensors, as for $\Delta T = 0$ their output voltage is intrinsically zero, while thermistors have to be connected in a Wheatstone bridge configuration which inevitably results unbalanced due to device mismatching, and an accurate and reiterated in time calibration/trimming is needed. Furthermore offset may result temperature dependent, and, as the operative temperature vary with the applied flow, heavy limitation of measure accuracy has to be expected. For this reasons, the work presented in this thesis is focused on thermopile based calorimetric sensors.

1.3.1. Differential calorimetric flow sensor in the BCD6 process of STMicroelectronics

The sensing structure shown in Fig. 1.6 represents a classical differential calorimetric flow-meter made up of a heater placed between an upstream and a downstream temperature probe placed symmetrically with respect to the heater. The actual sensor made out on the STMicroelectronics BCD6 process counts with a 1 kΩ polysilicon resistor, constituting the heater, positioned over a dielectric membrane suspended by means of four 45 degrees arms. The temperature probes are two thermopiles including 7 p+-poly/n+-poly thermocouples with the hot contacts at the edge of a dielectric cantilever beam and the cold contacts on bulk silicon. Thermal insulation of the dielectric membranes from the substrate has been obtained by means of a post-processing procedure described later on.
In the zero-flow regime the temperature distribution should be symmetrically around the heater, so that the two probes sense the same temperature and $V_{T1} = V_{T2}$. When the fluid begins to flow, the temperature profile displaces towards the flow direction. Now the two temperature probes sense a different temperature, and at their output a different Seebeck voltage is present: $V_{T2} > V_{T1}$.
Thermopiles are electrically connected in order to provide an output differential voltage:

$$V_{sens} = V_{T2} - V_{T1}, \tag{1.5}$$

which is function of the flow rate.
Openings in the dielectric layers, through which the bare silicon substrate becomes accessible for the etching, must be provided in order to suspend the heater and the hot junctions of the thermopiles. In some commercial CMOS processes, like the BCD3s of STMicroelectronics, openings can be fabricated by the silicon foundry if a proper stacking of active area, contact, via and pad-opening layers is provided during the chip design. In this case, the post-processing is limited to the silicon

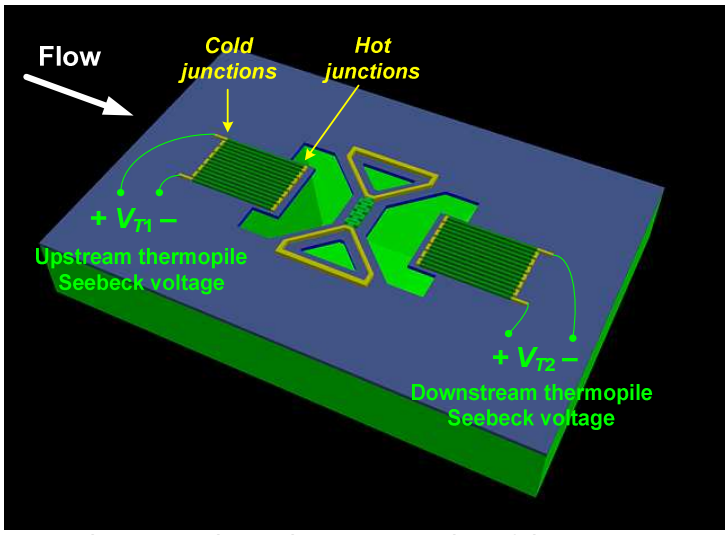


Fig.1.6 – Schematic representation of the BCD6 differential calorimetric flow-meter.

etching. Differently, in the BCD6 process, the silicided active areas and tungsten plugs used to fill contacts and vias prevent a direct access to the bare silicon substrate. Since silicide and metal plug removal requires processes and equipments not easily available in a research laboratory, it is more convenient to perform both the dielectric openings and the silicon etching in the post-processing phase.

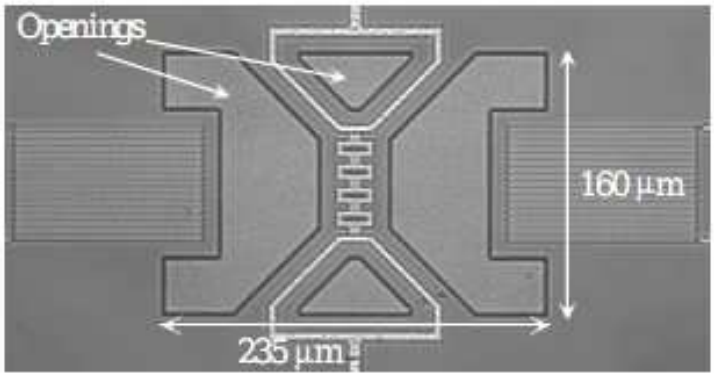


Fig. 1.7 – Photograph of the BCD6 single heater structure before post-processing.

The passivation openings have been performed by the silicon foundry while the residual dielectric layers have been removed in the post-processing. In Fig. 1.7 a photograph of the sensing structure before the post-processing is shown: the passivation openings are indicated. The residual dielectric layers were removed by means a 1 µm resolution photolithography and a buffered HF (BHF) solution as SiO_2 etchant. An etching time of 30 minutes at room temperature was necessary to reach the bare silicon substrate. After that, silicon was anisotropically removed by means of a solution of 100 g of 5 wt% TMAH with 2 g of silicic acid and 0.6 g of ammonium persulfate. This modified TMAH solution has a good selectivity toward dielectric layers and aluminium allowing silicon etches to be performed without any additional mask. Moreover, TMAH is less toxic than EDP solutions and is IC-compatible [16]. Nevertheless, the modified TMAH solutions are prone to a fast "aging-effect" with a noticeable decrease of the etch rate and increase of the etched surface roughness. A frequent solution refresh is thus necessary for long etch times [17]. In our case a 70 µm deep cavity has been obtained with only two etch steps, 40 minutes each, performed at 90 °C. Figure 1.8 schematically resumes (with some simplifications) all the post-processing steps.
A SEM (scanning electron microscope) micrograph of a sensing structure after the post-processing procedure is shown in Fig. 1.9, where the heater and thermopile conducting layers are not visible due to the upper dielectric layers.
In the next three sections, typical issues in designing and realizing of a flow meter will be presented; more specifically: section 1.3.2 deals with packaging methods, section 1.3.3 and 1.3.4 deals with the problems of sensor structural offset and power consumption, explored with the aids of finite element simulations, and finally in section 1.3.5, the problem of pressure sensitivity at low pressure will be introduced.

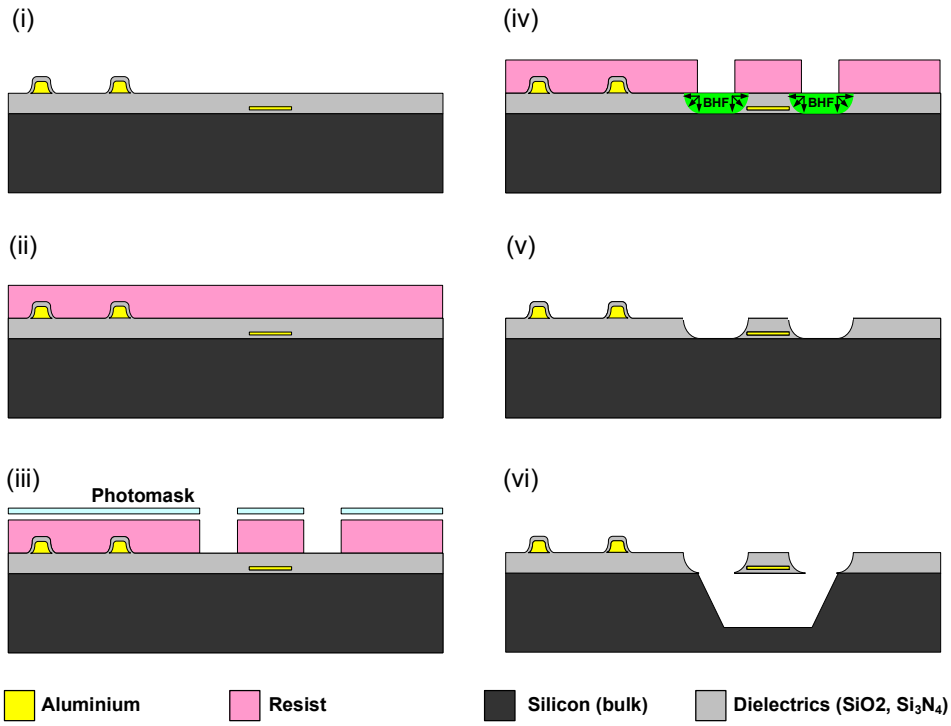


Fig. 1.8 – Schematic representation of post processing steps needed to obtain dielectric membranes over bulk silicon.

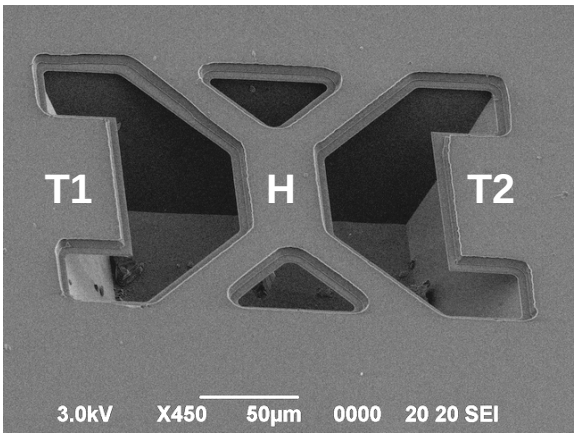


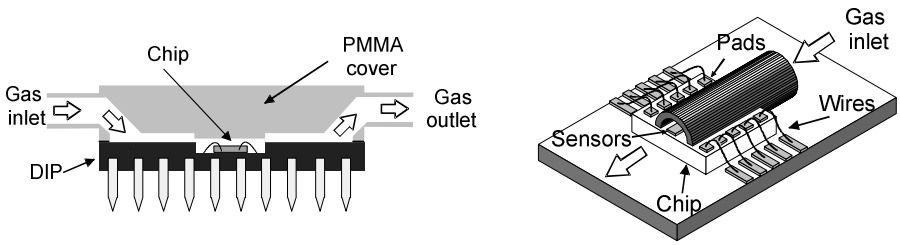
Fig. 1.9 – Scanning electron micrograph of a sensing structure after the post-processing procedure. T1, T2 and H indicate the thermopile and heater membranes, respectively.

1.3.2. Packaging methods for integrated thermal flow sensors

Packaging is a fundamental research area of the MEMS field. In the integrated circuit technology, package must provide reliable electrical interconnections and heat dissipation, as well as protect the chip from the external environment. By contrast, MEMS packaging has to take account of a more complex scenario. It must protect the fragile micromachined structures and, at the same time, allow the access to or the interaction with the physical quantity to be measured. In consequence, standards for MEMS packaging do not exist and the design of the package becomes important as the design of the MEMS itself because it affects the functionality and the performances of the device [18].

As far as gas flow sensors are concerned, several strategies have been proposed in literature. The simplest solution is that of placing the whole chip, including bonding wires, inside a channel where the fluid is made to flow [19]. In this case, the channel cross-section can not be reduced below several mm^2. It should be noted that thermal flowmeters are actually velocity sensors and it is often requested that the gas flow is accelerated in proximity of the sensing structure in order to detect very low flow rates. In addition, flow disturbance caused by the bonding wires and the chip borders must be taken into account and, eventually, minimized. Flow disturbance is avoided by separating the chip and the flow by means of a thermally conductive membrane [20]. Unfortunately, since the whole chip or large portions of the membrane should be heated for correct operation of this kind of sensors, an important degradation of the sensor speed and power consumption should be expected. Furthermore, this solution is clearly not optimized for device sensitivity so that it is usually employed in anemometric applications. Better sensitivity is achieved with sensors based on micro-channels etched either on the same silicon substrate as the sensing structures or on a silicon/glass cover, bonded to the main chip [21]. Nevertheless, this approach is applicable only to real microfluidic applications, since only very reduced channel cross-sections can be obtained. Various packaging methods have been explored during this thesis work. A first solution is schematically shown in Fig. 1.10(a), where the whole the chip is inside the channel (CIC).

In CIC solution, a plastic cover has been glued to the top of the DIP case by means of epoxy resin. The cover includes two channels, used as inlet and outlet for the gas stream, which convey the gas into the small chamber that hosts the chip.



(a) (b)

Fig. 1.10 – Two different packaging solutions: (a) the whole chip inside the channel (CIC); (b) a metal pipe adapted (MPA) to the chip.

Upstream and downstream horizontal sections, each 1 cm long, have been included to make the gas flow parallel to the chip surface. A channel with a cross section of about 8 mm^2 was obtained around the sensing structure.
Unless this solution is very simple to implement it is affected by important problems that may strongly reduce its practical use. All chip pads are exposed to the fluid which could result in a short circuit in case of conducting liquids. Besides, the fragile bonding wires are exposed too, making the device prone to failures.
Figure 1.10(b) shows a second packaging strategy using a metal pipe adapted (MPA) to the chip itself, which allows to flow to be conveyed on a selected area of chip avoiding lateral pads. The metal pipe has an external diameter of 2.4 mm. It was milled in order to obtain a groove where the chip was positioned. In this configuration, the chip is connected directly to the pipe and a very small channel, with a section of about 0.8 mm^2, was obtained over the sensing structure.
The pipe was carefully aligned to the chip using a x-y-z micrometer stage assuring that the sidewalls of the pipe fell between the pads. It should be pointed out that some pads perpendicular to the pipe axis become unusable because they are enclosed by the pipe itself. For this reason, in the chip layout all the pads of the sensing structures of interest must be placed along the chip borders parallel to the pipe axis. After the alignment, the pipe was glued and sealed to the chip and DIL case with an epoxy resin. In Fig. 1.11 a photograph of the final device in this configuration is shown.

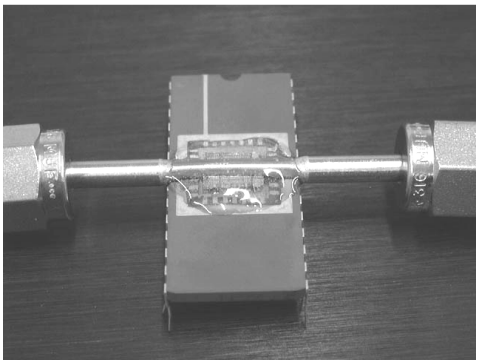


Fig. 1.11 – Photograph of the device with the MPA package.

After the silicon etch, the die was glued to a standard IC package by means of epoxy resin; wedge bonding was used to connect selected chip pads to the case pins.
The reduced pipe section over the sensor allowed a local increase of flow velocity at constant mass flow rate. Consequently, a sensitivity increase with respect to that obtained with a CIC solution is achieved. Anyway some issues were still open:

(i) In order to apply the MPA technique the chip should be designed following some important restrictions, for example some pads in the chip pad-ring must be sacrificed to permit the application of the pipe.

(ii) The contact perimeter between the opening in the pipe and the chip is quite complex and consequently is not easy to guarantee an adequate sealing.

Due to previously commented problems, we developed another packaging procedure based on a plastic adapter. Figure 1.12 together with the chip layout, consisting in a solid piece with an optically flat face slightly smaller than the chip area free from bonding pads.

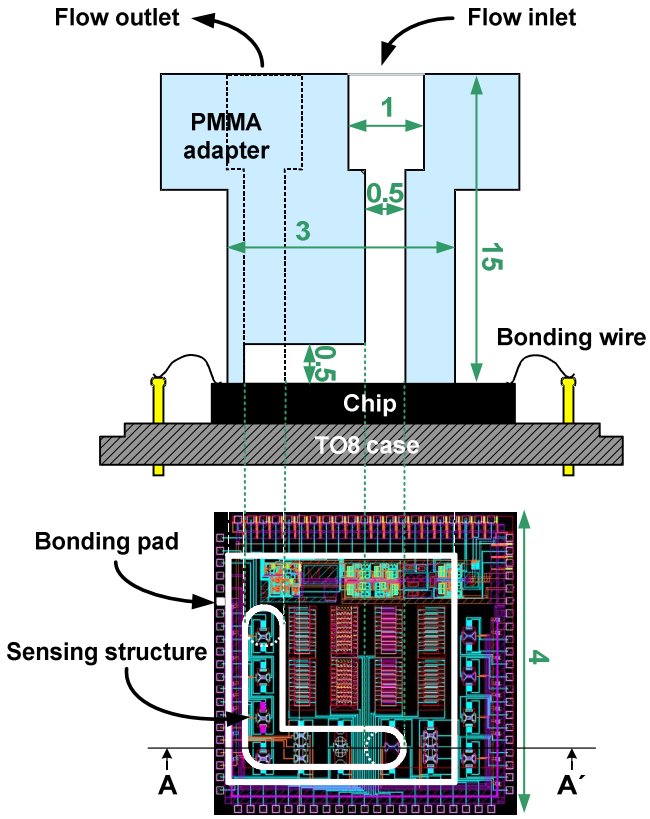
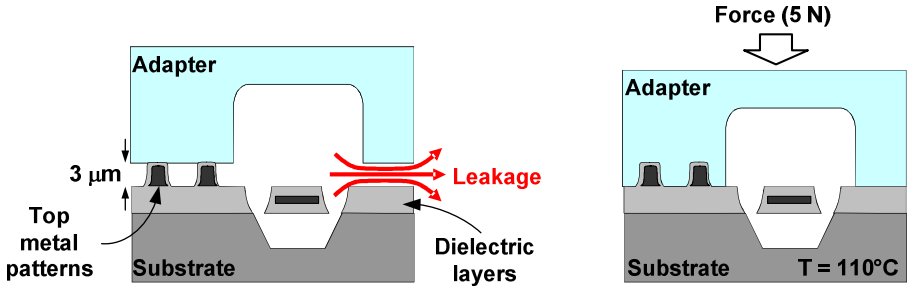


Fig. 1.12 – Structure of the adapter with main dimensions (in mm) (not to scale).

A L-shaped trench has been cut into the adapter face by means of a precision milling machine (VHF CAM 100) controlled by a computer. The latter was aligned to the chip front side in order to include the sensing element into the trench and, at the same time, avoid contact with the bonding pads. Two holes connect the two extremes of the trench to the inlet and outlet fittings. The upper part of the adapter is enlarged with respect to the section joined to the chip in order to allow an easier connection to the gas line.
Alignment of the adapter to the chip is obtained by means of a micrometric displacement stage, equipped with a low magnification microscope. With the aim to make an easier alignment, a special holder was built that made the adapter free to

rotate along two axes parallel to the chip surface. In this way even a small angular mismatch is self-recovered applying a light pressure between the two pieces (chip and adapter). During this phase, the adapter is kept separated from the chip by a small air gap (about 0.1 mm); then the adapter is placed in contact to the chip front side. Unfortunately, this does not guarantee a leak free adhesion of the two surfaces; owing to the roughness of the chip front face mainly due to the thick upper interconnect layers (metals). In fact, those metal patterns are covered by a non planarized dielectric passivation layer, resulting in protrusions acting as spacers for the two surfaces. Measurements performed by means of a stylus profilometer showed that, for the process adopted, steps up to 3 μm were present on the chip surface.
To overcome this problem a thermal/mechanical procedure was adopted. We were able to soften the adapter surface by heating the chip to a proper temperature, i.e. the glass transition temperature of the plastic material used for the adapter. In our case, sealing of the flow channels was then obtained maintaining the chip at the



(a) (b)

Fig. 1.13 – Schematic representation of (a) leakage due to roughness of the passivation layer; (b) thermal/mechanical procedure for channel sealing.

PMMA glass transition temperature (110°C) for 5 min utes while applying a force of about 5 N between the chip itself and the adapter. The sealing procedure is schematically represented in Fig. 1.13.
Heating of the chip during the application of the package was controlled by a power mosfet and a temperature sensor integrated on the same die as the sensing structures. In fact, a ΔV_{BE} substrate temperature sensor and a series of power DMOS transistors present on the chip were used to maintain a constant temperature for the duration of the whole sealing procedure. The schematic diagram of the circuit used to control the chip temperature is shown in Fig. 1.14, where the on-chip components are included in the shaded box, while the other components are placed on an external printed circuit board (PCB).

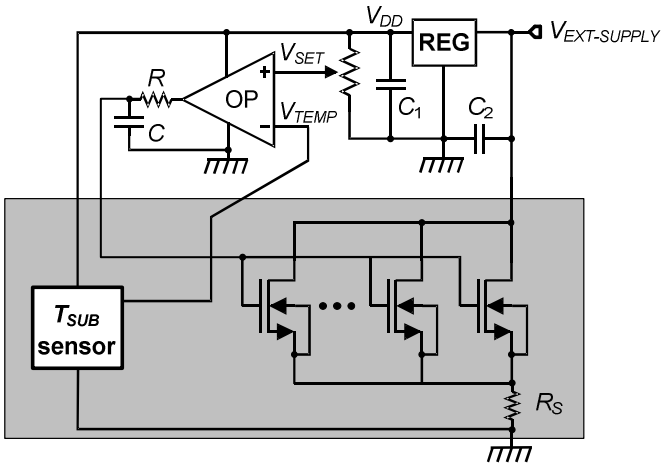


Fig. 1.14 – Structure Circuit used to control the chip temperature. The elements into the shaded box are integrated on the test chip.

The power mosfet is formed by 20 n-DMOS connected in parallel and distributed along the chip perimeter. The power supply voltage is $V_{EXT\text{-}SUPPLY}$ = 5 V. This constitutes the drain voltage of the power mosfet. A regulator (REG) is used to provide the 3.3 V power supply required by the chip. The T_{SUB} sensor produces a voltage V_{TEMP} proportional to the absolute temperature of the silicon substrate with a sensitivity of 3 mV/K. An external operational amplifier (OP) with rail-to-rail input and output ranges, compares the voltage V_{TEMP} with the set point voltage V_{SET} and drives the power mosfet gate. The RC filter cuts high frequency components (greater than 10 kHz) in order to avoid unwanted oscillations due to parasitic capacitive coupling.
In order to obtain the desired result, the choice of the material for the adapter is fundamental. The requisites are:

(i) transparency, to facilitate the alignment of the sensing structure into the trench;
(ii) acceptable surface hardness, to avoid unintentional scratches of the surface during alignment;
(iii) low enough glass transition temperature.

We compared three commonly available, transparent plastic materials: PMMA, Polycarbonate and Polystyrene. The hardness and glass transition temperature are reported in table 1.I for the three materials, where it is evident that PMMA represents the optimal choice.
Due to the poor adhesion of PMMA on silicon and silicon dioxide, the structure obtained in this way, though being leak proof, is rather fragile. A robust structure is obtained by carefully pouring epoxy resin inside the package chip chamber through holes in the guide. It is worth observing that, without the thermal sealing procedure, the resin slipped between the chip and the adapter, partially filling the trenches.
The compact resulting structure is shown in Fig. 1.15.

Material	*Hardness (Rockwell M)*	*Glass transition temperature (°C)*
PMMA (Polymethylmethacrylate)	90	100
Polycarbonate	70	150
Polystyrene	72	90

Table1.I – Properties of investigated transparent polymers.

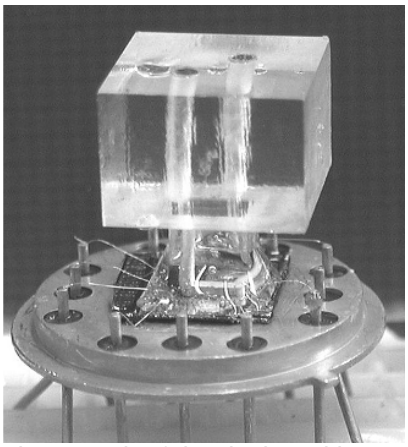


Fig. 1.15 – Photograph of the device with PMMA adapter.

1.3.3. Design of thermal flow meter by means of FEM simulations

A new test chip in the BCD6s (shrinked version of BCD6) process of STMicroelectronics has been realized. To this aim, a thermo-fluid dynamic model in the COMSOL Multiphysics™ environment has been developed. Beside, experiences from experiments with sensors fabricated from the BCD6 and BCD3s processes have been recollected in order to revise and optimize the design of the new sensing structures. The implemented model follows the same strategy illustrated in [22], which will be now briefly resumed. A correct finite element modelling of miniaturized flow-meter should include both the fluid dynamic and the thermal domain equations. In a steady-state incompressible newtonian fluid those equations can formalized in the following system [23]:

$$\rho\mathbf{u}\cdot\nabla\mathbf{u} = \nabla\cdot\left[p\mathbf{I} + \eta\left(\nabla\mathbf{u} + (\nabla\mathbf{u})^T\right)\right] + \mathbf{F}\,. \tag{1.6a}$$

$$\nabla\cdot\mathbf{u} = 0 \tag{1.6b}$$

$$\nabla\cdot\left(-k\nabla T\right) + \rho C_P\mathbf{u}\cdot\nabla T = \mathbf{q} \tag{1.6c}$$

Equations (1.6a) and (1.6b) are known as Navier-Stokes system of equations, while eq. (1.6c) is known as thermal equation. More specifically, eq. (1.6a) derives from the second Newton's law of motion stated for a fluid medium, while eq. (1.6b) expresses the principle of mass conservation. In those equations **u** indicates the

three-dimensional vector of fluid velocity, $\mathbf{u} = (u\ v\ w)^T$, where u, v, and w are the x-y-z velocity components, respectively. The scalar quantity p indicating the local pressure gets multiplied by the 3×3 identity matrix $\mathbf{I}$ in order to be correctly included in the formal of the equation. Vector $\mathbf{F} = (F_x\ F_y\ F_z)^T$ represent eventual body forces per unit volume, while parameter ρ and η are the volumetric mass density and the dynamic viscosity, respectively. Also equation (1.5c) is intrinsically a system of three equations, where T indicates the temperature field, $\mathbf{q} = (q_x\ q_y\ q_z)^T$ represent the heat flux per unit volume, and finally the parameter k and C_P are the medium thermal conductivity and the specific heat at constant pressure.

Resolving the system of equations (1.6a-c) means to find the distribution in the considered domain of the dependent quantities u, v, w, p, T at every given point (x, y, z) of the given domain, i.e. it means to find the velocity, pressure and temperature fields. In a more general formulation of the system those solutions depend also on the time variable, which here is not considered as we focus only on steady-state solutions. Beside the well known intrinsic non linearity of fluid dynamic equations, equations are strongly interacting: in fact, the velocity field solution **u** appears in the thermal equation, while the temperature field is implicitly carried in the physical parameters (ρ and η) of the former equation.

It should be clear to the reader that any attempt to solve the above equation analytically is strongly discouraged, unless the problem cannot be reduced to very simple geometry in a one-dimensional schematization. Unfortunately this is not the case for complex structure such of that illustrated in section 1.3.1.

In principle, this limitation can be surmounted by using a numerical approach offered by the finite element method (FEM). In this case, solutions are as close to physical reality as how closely the sensor geometry is represented. A three-dimensional model would be strongly desirable. However, convergence problems tied to the complexity of the fluid dynamics equations allow practical use of three-dimensional simulations again only for very regular flow channel geometry (absence of steps and cavities) and/or simplified sensor structure. Furthermore, very small geometries included in much more bigger domains make numerical convergence even more difficult.

On the other hand, two-dimensional simulations present less convergence problems and, in principle, can be used to simulate more realistic and irregular flow channel profiles. Typically, 2D simulations are applied to cross-sections defined by one direction parallel to the flow channel length and the other perpendicular to the substrate surface. Application is limited to sensor structure where gradients along the third axis (perpendicular to the simulated cross-section) can be considered negligible.

Unfortunately, suspending elements, i.e. the heater supports, have dominant heat exchange paths that cannot be included in a single 2D cross-section. Neglecting these heat flows result in a large overestimation of the temperature reached by the heater. This problem has been addressed using the methodology illustrated in [22], where specific heat exchange terms have been added in the above equations to obtain a well manageable two-dimensional model.

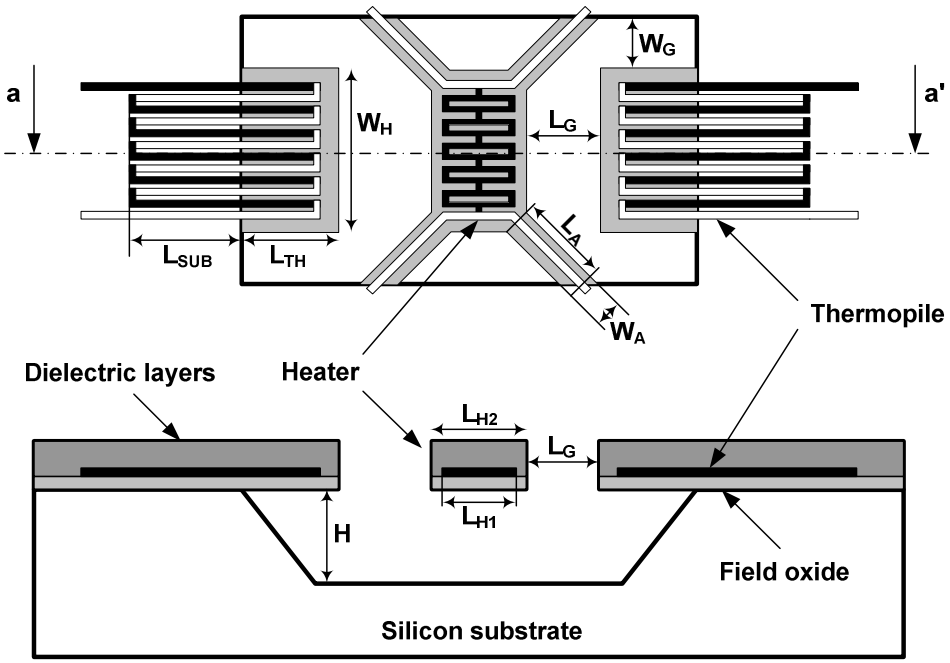


Fig. 1.16 – Schematic top view (upper) and cross-section (lower) of the simulated flow meter (not to scale).

W_G	34	W_H	89.3
L_G	60	L_{H1}	22
W_A	25.6	L_{H2}	42
L_A	61	L_{TH}	34
H	58.4	L_{SUB}	91

Table 1.II – Values of sensor geometries of Fig. 1.16, all values are expressed in μm.

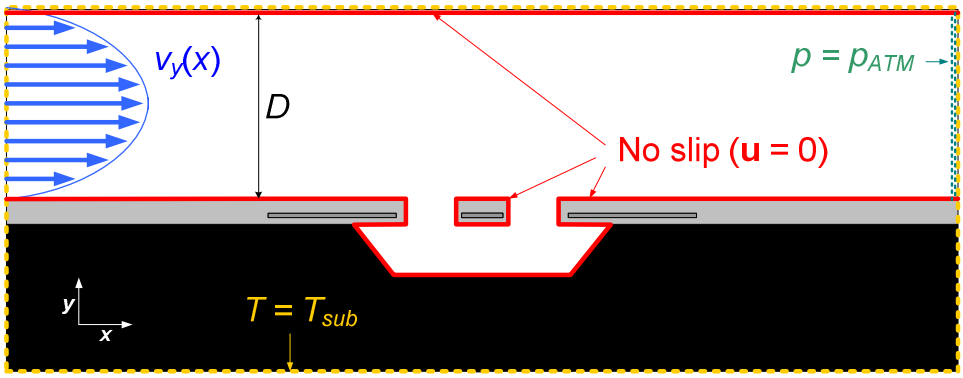


Fig. 1.17 – The sensor is placed inside a duct formed by chip top surface (bottom wall) and the PMMA surface (top wall), D = 500 μm. A parabolic velocity distribution of the flow was imposed to one end, while atmospheric pressure was applied ad the opposite end, all other fluid/solid interfaces have been set as no-slip surfaces. Temperature applied to the external boundaries of the duct was set equal to T_{sub} = 298 K. For all other internal boundaries, temperature continuity condition holds.

The two-dimensional nature of the model allows representation of complex flow channel configurations with reduced convergence problems. The method has been used to develop a model of a real micrometric thermal sensor to be simulated by means of the COMSOL Multiphysics™ finite element platform. Structure geometries of Fig. 1.16 are annotated in table 1.II. Simulations have been carried out on the two-dimensional arrangement of Fig. 1.17, where some boundary conditions have been indicated in the caption.
The following solutions have been adopted for the two-dimensional model:

(i) all area quantities in the two-dimensional section have been set in accordance to the correct volume quantities in the three-dimensional case;
(ii) some fictitious material have been introduces, with characteristics that average the material properties encountered along the third dimension (z-axis);
(iii) ad hoc heat loss terms representing the most important fluxes along the z-axis have been introduces.

Issue (i) derives from the equivalence of a two-dimensional x–y simulation with a three-dimensional one involving an extrusion of the simulated 2D section along a unity length portion of the z-axis. Local power density (per unit area) in the polysilicon heater region, accordingly to (i) and (iii), has been set

$$\frac{dP}{dA} = \left[R_H I_H^2 - G\left(T - T_{SUB}\right)\right] \frac{1}{t_{poly} L_{LH1}} \frac{Z_1}{W_H}, \tag{1.7}$$

where I_H is the current fed to the heater, R_H the heater ohmic resistance, T the local temperature, t_{poly} is the polysilicon layer thickness, T_{sub} is the substrate

temperature, while Z_1 is the unit length (1m) along the z-axis that is intrinsically considered in 2D simulations.
The conductance G takes into account the heat flow from the heater to the substrate through the heater membrane and the four suspending arms. It has been calculated in such away as to produce a heater temperature in the simulated 2D section equal to the average of the temperature of the heater along the z-axis. In this way the simulated section is representative of the whole thermopile-heater extension along the z-axis.
The complete expression of the conductance G can be estimated as

$$G = \frac{4}{2R_H^{(T)} + R_B^{(T)}}. \tag{1.8}$$

where, as illustrated in Fig. 1.18, $R_B^{(T)}$ is the thermal resistance of a single suspending arm, including the extension of the metal interconnects on the substrate, while $R_H^{(T)}$ is the equivalent thermal resistance that ties the total power dissipated into the heater to the difference between the average temperature of the latter and the temperature at the extremes of the heater itself. Resistance $R_H^{(T)}$ was calculated with simple analytical arguments and is approximated to

$$R_H^{(T)} = \frac{1}{6}\frac{W_H}{t_H L_{H2} k_H} \tag{1.9}$$

where t_H is the thickness of the heater membrane and k_H is the effective thermal conductivity of the latter, calculated according to (ii).
Issue (ii) is necessary to take into account the fact that materials are not homogeneous even within the extension of the membranes suspending the thermopiles and the heater. Fig. 1.19(a) and (b) shows schematically the top view thermopile and heater patterns, respectively.

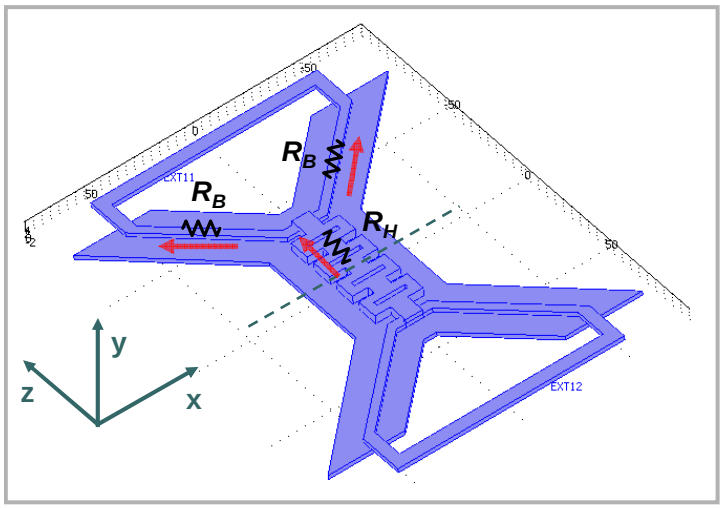


Fig. 1.18 – Heat loss paths in the micro heater.

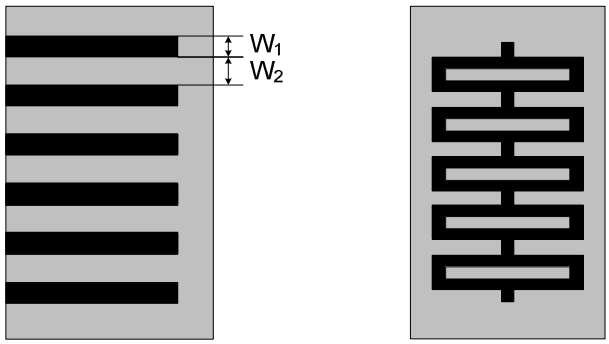


Fig. 1.19 – Details about the actual thermopile (a) and heater (b).

As far as the thermopiles are concerned, the polysilicon layers forming the thermocouples are alternated to silicon dioxide as shown in Fig. 1.19(a). In order to represent this situation, the thermal conductivity of the thermopile layer is calculated by means of the formula

$$k_{TH}^{eff} = \frac{k_{poly}W_1 + k_{ox}W_2}{W_1 + W_2}. \qquad (1.10)$$

where k_{poly} and k_{ox} are the thermal conductivity of polysilicon and silicon dioxide, respectively. Similar weighted averages are used for the heater layer in order to calculate k_H.

Another aspect that, in our opinion, cannot be neglected to obtain quantitative results is the temperature dependence of the physical quantities of the gas under test. This is supported by the consideration that differences up to 200 K between the heater surface and the incoming gas flow can be reached in these devices. For this reason the gas density, thermal conductivity and viscosity temperature dependence have been modelled with precise relationships taken from literature data.

In order to test the validity of the adopted approach, a detailed 3D model has been also developed, where only the thermal equation has been solved. This model, unpractical for flow simulations, was only implemented in order to check the quantitative correctness of eq. (1.7). To do this a fictious material, with zero thermal conductivity (i.e. representing vacuum) was used as fluid. In this condition only conductive heat losses through solid materials take place. Simulated results with proved consistency of temperature heater value calculated through eq. (1.7).

1.3.4. Open loop compensation for sensor structural offset

A perfect geometrical symmetry, identical material properties and thermal symmetry at rest condition are essential requirements for an offset-free sensor. Unfortunately, unavoidable asymmetries of the sensing structure and package deform the heat distribution causing an offset which is could be greater than the sensor resolution [24]. Furthermore, sensor offset cannot be reduced with the traditional methods (e.g. autozero or chopper stabilized amplifiers) used to compensate the offset of the electronic read out circuits, and a significant offset temperature drift can be expected due to the dependence of the sensor signal on the thermal gas properties. This strongly reduces the effectiveness of standard

offset compensation techniques, based on software or hardware subtraction of a constant term (e.g. autozero at power on). Assuming that heat transfer occurs mainly through conduction and forced convection, a linear relationship can be assumed between the auto-generated Seebeck voltages V_{T1} and V_{T2} and the heater power P.

$$V_{sens} = V_{T2} - V_{T1} = f(Q) \cdot P \,. \tag{1.11}$$

where $f(Q)$ is a function of the flow mass rate Q. Equation (1.12) can expressed for very small flow rates as the first two terms of Taylor series:

$$V_{sens} \approx \left(f(0) + \left.\frac{df}{dQ}\right|_{Q=0} \cdot Q \right) \cdot P = f(0)P + \beta Q \,. \tag{1.12}$$

It is clear from eq. (1.12) that an offset voltage $V_{OS} = f(0)P$ may arise in zero flow condition when $f(0) \neq 0$, i.e. when different geometries in the thermal paths, and/or mismatch in Seebeck coefficients of the two thermopiles are present. As mentioned before $f(0)$ involves fluid physical parameters that on temperature, eventually causing sensor offset temperature drift.

A very simple solution to this problem can be obtained by employing a double heater structure of the sensor and driving the two heaters at slightly different power in order to cancel the structural offset. From Fig. 1.20, where the single heater and the double heater signal flows are reported, it is evident that the double heater solution enables an important degree of freedom that can be employed for offset cancellation purpose.

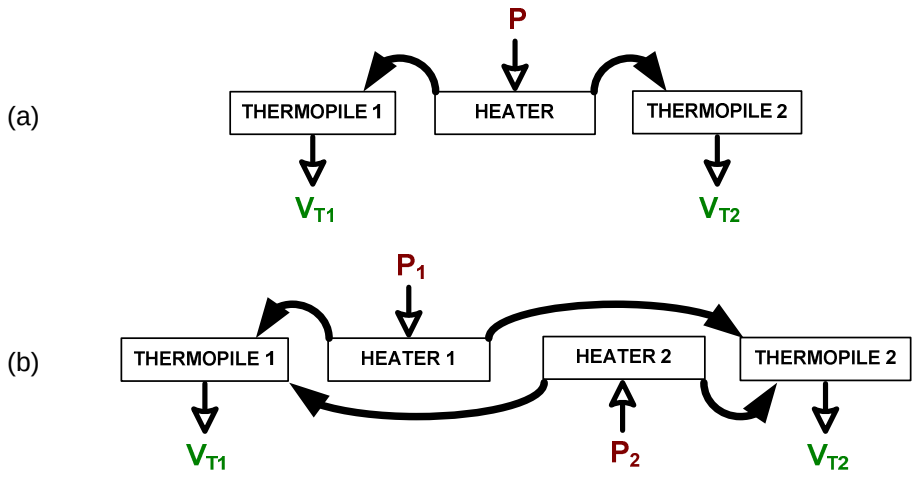


Fig. 1.20 – Schematic representation of heat paths for: (a) single heater and (b) double heater sensor structures.

Sensor output voltage, for a double heater structure, can be rewritten as:

$$V_{sens} \approx f_2(0)P_2 - f_1(0)P_1 + (\beta_2 P_2 - \beta_1 P_1)Q \tag{1.13}$$

where $f_1(0)$ and $f_2(0)$, β_1 and β_2, respectively nominally identical, are obtained applying the same method as below. Nevertheless, eq. (1.13) indicates that a condition of null offset can still be obtained if:

$$\frac{P_2}{P_1} = \frac{f_1(0)}{f_2(0)} . \tag{1.14}$$

Thus, using a double heater structure with a proper power unbalance $P_1 \neq P_2$, open loop offset compensation is enabled. Furthermore, supposing that the $f_1(0)$ and $f_2(0)$ have a very close temperature coefficients, a low residual offset drift can be also expected. The effectiveness of the proposed method has been proven firstly by a FEM model and than confirmed by means of the experiments with a double heater sensor that was fabricated in the BCD3s process of STMicroelectronics and a post-processed following the same techniques described for BCD6 sensor.
The optical photograph of the BDC3s structure is shown in Fig. 1.21, while the respective FEM model is shown in Fig. 1.22. In order to introduce a mismatch between the $f_1(0)$ and $f_2(0)$ a geometrical mismatch in the thermopile-heater gap ΔL_G = 3 µm has been introduced. This structure showed a temperature mismatch between the two thermopiles of 0.47 K, which is consistent with experimental data discussed in following. The needed power unbalance has been then found through a simulation in the pure thermal domain.

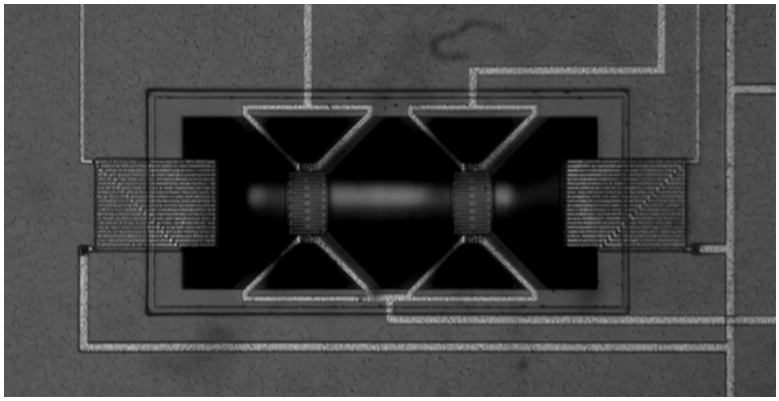


Fig. 1.21 – Optical photograph of BCD3s double heater flow-meter.

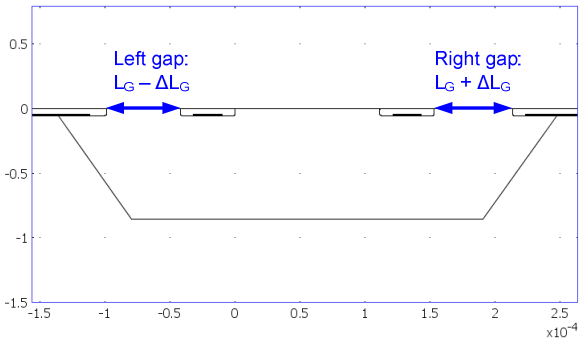


Fig. 1.22 – FEM model of double heater sensor with a gap length L_G mismatch.

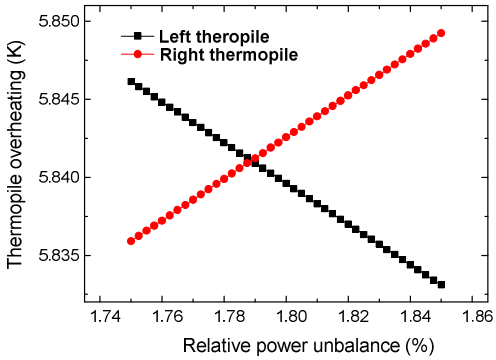


Fig. 1.23 – Temperature overheating of thermopiles as a function of heaters power unbalance for the mismatched structure of Fig. 1.22.

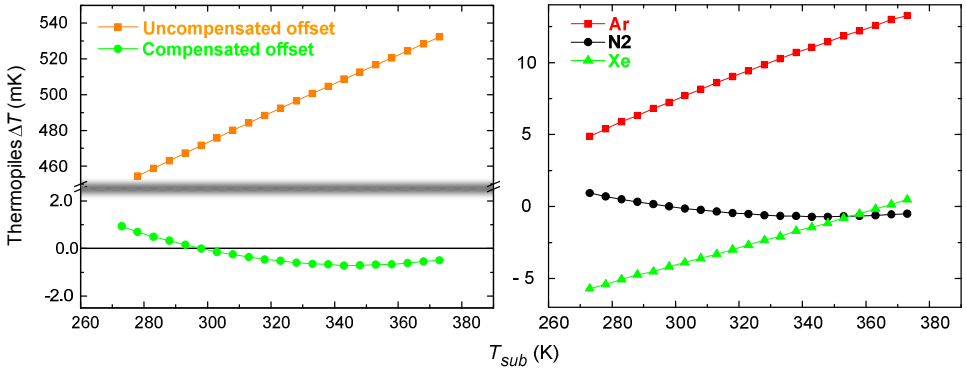


Fig. 1.24 – FEM model of double heater sensor with a gap length L_G mismatch.

Overheating ($T_{hot\text{-}junction} - T_{cold\text{-}junction}$) of both left and right thermopile is shown in Fig. 1.23, where an optimal P_2/P_1 ratio of 1.74 has been found. In this preliminary simulation, the considered fluid medium is nitrogen gas (N_2).

Offset temperature drift has been estimated making the silicon substrate temperature variable, and recording the thermopiles temperature difference. Left graph in Fig. 1.24 shows the behavior of both uncompensated and compensated structure: as expected offset temperature drift has been drastically reduced to 17 ppm/℃ starting from a temperature sensitivity of 7830 ppm/℃ of the case $P_1 = P_2$.

The graph on the right of Fig. 1.24 have been obtained by replacing the N2 gas with argon and xenon in the case of compensated structure in order to check if the gas type has an important effect on the described compensation technique. Results show that the compensation still remains acceptable even changing the gas type.

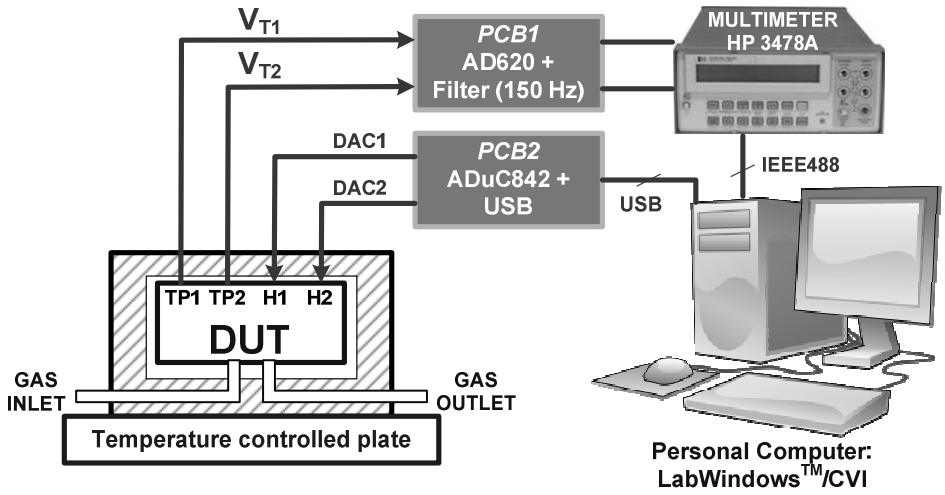


Fig. 1.25 – Schematic view of the experimental set-up used for offset and offset thermal drift characterization: DUT indicates the device under test.

The effectiveness of the proposed method has been also proven by means of the experimental set-up schematically shown in Fig. 1.25. The chip was glued to ceramic DIP cases by means of epoxy resin and wedge bonding was used to connect selected chip pads to the case pins. A PMMA package was designed in order to connect the sensor to a reference gas line, equipped with a precision flow controller (MKS 1179B) with a 10 sccm full scale range. The package was glued to the chip following the procedure described in section 1.3.2. The packaged device was placed inside a hollow aluminium cylinder whose temperature was varied using a Peltier cell driven by an electronic temperature controller. The gas reaches the sensor after passing through pipes drilled through the cylinder walls, in order to get isothermal with the latter. The read out electronics has been developed on two printed circuit boards (PCBs). The first one, connected to a PC via USB, includes a MicroConverter® ADuC842 (Analog Devices) with two 12-bit voltage output DACs used to drive the device heaters. The two DACs have been calibrated to obtain an accuracy of ± 1 mV. The second one, connected to a digital multimeter (HP 3478 A), includes a low noise instrumentation amplifier (AD 620) in cascade with a second order 10 Hz low pass filter used to read the sensor output signal. An application in the National Instruments LabWindows™/CVI environment has been developed in order to drive both the ADuC842 and the multimeter. The offset of the readout electronics was cancelled by subtracting the output voltage measured with both the heaters turned off.

An intrinsic offset of about 24.7 μV has been found when the heaters are biased with the same power ($P_1 = P_2$). The applied power unbalance reduced the offset to a residual value of −1.2 μV applying a power ratio P_1/P_2 of 1.02. The sensor response as a function of the gas flow for two different temperatures, namely 25 ℃ and 70 ℃, is shown in Fig. 1.26. The value of the measured offset at the two temperatures is reported in table 1.III. For comparison, the offset values obtained

with the two heaters biased at the same voltage are also shown. It is important to observe that both the offset and its temperature drift are reduced by almost one order of magnitude.

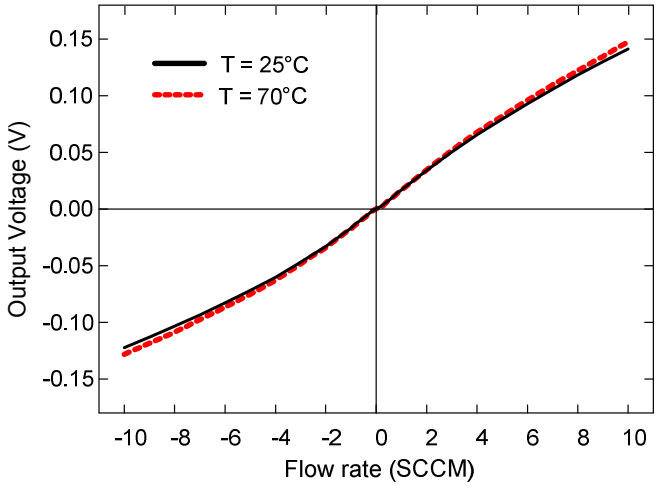


Fig. 1.26 – Amplified output voltage as a function of nitrogen flow rates measured at two different temperatures with offset compensation.

	T = 25 ℃	T = 70 ℃
Offset with P_1/P_2 = 1.02	229 µV	385 µV
Offset with $P_1 = P_2$ (no correction)	2550 µV	3250 µV

Table 1.III – Experimental offset variation (amplified by 150) with temperature.

1.3.5. Heat losses through suspending arms

BDC3s sensors were designed using aluminium as interconnection layer to the heater elements. Aluminium, i.e. a metal layer, was chosen due to the very the low value of sheet resistance, making the voltage drop along the interconnecting pattern negligible with respect to the voltage drop across the heater itself. As an important consequence the power generated by heaters is well determined once their resistance value and the applied voltage or current are known.
Unfortunately, aluminium has also high thermal conductivity, which is responsible of important heat losses along the suspending arms (see eq. (1.7)). Heater temperature is an important parameter for the overall sensitivity of the sensor, as the latter is linearly dependent (in a first order approximation) to the former: the lower is the temperature reached by the heater, the lower the temperature differences between the hot and cold junctions, actually lowering the Seebeck voltages. Minimizing heat losses through suspending arms would reflect on heaters efficiency, enabling the possibility to reach the same overheating with less consumed power. This issue has been addressed in the new design of flow meter in the BCD6s process, by exploiting siliciced polysilicon as interconnecting material instead of aluminium, in fact: (i) it still presents a good electrical conductivity, (ii) it

has lower thermal conductivity as the siliciding process affects only the very surface of polysilicon affecting only few atomic layers, while heat flow concerns the whole section of the polysilicon layer. Figure 1.27 shows the simulated sensor characteristics for positive flow rates in the two cases: aluminium and polysilicon interconnections. In both cases the thermal conductance losses through suspending arms have been introduced in the model following the eqs. (1.7-8), and the same power (4 mW) has been fed to the heater. As expected the structure with polysilicon interconnections has a greater sensitivity. Estimations return a power saving of 40 % when the same sensitivity of the old structures is required.

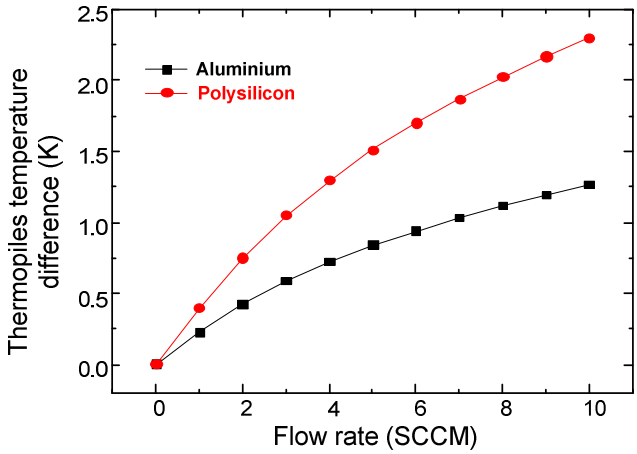


Fig. 1.27 – Thermopiles temperature difference as a function of the flow rate for the two solutions for the heater interconnections: aluminum and unsilicided polysilicon.

1.3.6. Low pressure effects on miniaturized thermal flow-meters

While small size of integrated flow meters represents a clear advantage in terms of pass-band and power consumption with respect to traditional macroscopic sensors, it afflicts sensor sensitivity at pressures low enough to make molecule mean free path comparable with the sensor characteristic dimensions. In some applications, such as propellant control for ionic thrusters on board small satellites and gas delivering in semiconductor processing, accurate flow measurements for gases at low pressure is required and as consequence, use of micron scale flow meters may be partially impaired.

In Fig. 1.27, the experimental response of the sensor to nitrogen flow at four different pressures is shown [25]. Authors found that deviation of the output signal from the value measured at atmospheric pressure is less than 3% for pressures greater than 25 kPa, while for lower pressures the signal begins to reduce significantly.

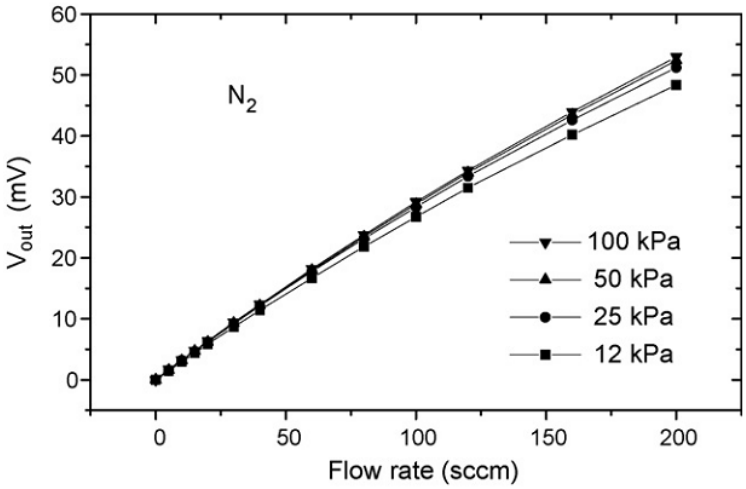


Fig. 1.27 – Output signal as a function of nitrogen flow rate for four different pressure values. Sensor structure is identical to that discussed in section 1.3.1, fabricated starting from the BCD3s processes of STMicroelectronics. The sensor output signal was extracted using a low noise, low offset amplifier (AD620). The total amplification provided is 150. The heater of the sensor was supplied with a 6 V constant voltage.

To make clear the effects of the gas pressure on the response, it is useful to make a distinction between convective and static conductance:

- Convective conductance is related to mass transport between the heater and the thermopiles gap, it is intrinsically dependent on the nature of fluid (here intended as both gas or liquid) as it allows arbitrary displacements of the molecules/atoms forming the fluid itself: in this case heat exchange is due to a transportation of a some moving portion of the fluid.
- Static conductance is due to heat diffusion across the sensor gaps between the heater and thermopiles, without the intervention of any moving part of the fluid. In this case heat exchange takes places between adjacent layers of the medium that are at different temperatures. This heat exchange mechanism is the only allowed within layers of solid materials, while for fluids it happens in conjunction with the convective phenomenon.

To elucidate, we reported here the thermal equation (eq. (1.6c)):

$$\nabla \cdot \left(-k\nabla T\right) + \rho C_P \mathbf{u} \cdot \nabla T = \mathbf{q} \tag{1.15}$$

where the two heat exchange phenomena can be clearly identified:

- $\nabla \cdot (-k\nabla T)$ holds for the pure conduction;
- $\rho C_P \mathbf{u} \cdot \nabla T$ holds for the convection.

Differences in the dependence on pressure can be expected for the two phenomena, especially when dealing with a gas.
The static conductance of the sensor can be estimated by measuring the overheating of the two thermopiles with respect to the substrate in condition of zero flow, while the convective term is related to the difference between the downstream and upstream thermopile temperatures. Comparison between these two terms can be done even when a flow is applied, approximating the former with the average (V_{cm}) of the upstream and downstream thermopile outputs as it has been found to maintain its value in zero flow condition.
With this approach, the sensor output V_{out} and V_{cm} were measured for a fixed flow rate as a function of gas pressure finding out that V_{cm} has a dependence on pressure similar to V_{out}, but it begins to appear at even more higher pressures.
On the other hand, similar pressure dependence are exploited by the Pirani vacuum gauges, whose operating principle is just based on the pressure dependence of a rarefied gas thermal conductivity. A typical Pirani gauge consists of a metal filament put inside the chamber whose vacuum is to be measured. The filament terminals are accessible in order to apply a constant current while measuring its temperature dependent electrical resistance. At high pressures, gas molecules collide frequently with the filament and absorbing thermal energy produced by the filament. As the pressure drops inside the chamber, the number of gas molecules decreases and fewer collisions per unit time with the filament are present, finally resulting in a temperature increase of the latter. This behaviour can be studied considering the Knudsen number *Kn*:

$$Kn = \frac{\lambda}{d} \tag{1.16}$$

where λ is the mean free path of the gas and d is the characteristic length involved in the heat transfer. In rarefied gas dynamics, four different regimes can be distinguished [27]: free molecules ($Kn > 10$), transition ($10 > Kn > 0.1$), temperature jump ($0.1 > Kn > 0.01$) and continuum ($Kn < 0.01$). In the continuum regime, the effective thermal conductivity is pressure independent while in the free molecule regime it depends linearly on pressure. In the temperature jump and transition regimes an intermediate condition exists with a thermal conductivity that gets more and more pressure dependent as *Kn* increases. A common approximation of the conductive heat transfer through a gas, valid for all regimes, is given by:

$$q = \frac{q_{FM}}{1 + q_{FM}/q_C} \tag{1.17}$$

where q_{FM} and q_C are the heat exchange rate calculated using either the free molecule or continuum expressions, respectively. Considering that q_{FM} is linearly dependent on pressure while q_C is pressure-independent, eq. (1.17) can be expressed as

$$q(p) = q_C \cdot \frac{p}{p + p_T} \tag{1.18}$$

where p_T is called transition pressure, which in cases of simple heater geometry can be calculated. For example, in for a gas at rest between two flat plates, p_T is given by [28]:

$$p_T = \frac{k_C}{d} \cdot \frac{2-\alpha}{\alpha} \cdot \frac{2(\gamma-1)}{\gamma+1} \sqrt{\frac{2\pi \cdot M \cdot T_{gas}}{R}} \tag{1.19}$$

where k_C is the gas thermal conductivity in the continuum limit, d the distance between the two plates, α the energy accommodation coefficient for the two surfaces, γ the constant pressure/constant volume specific heat ratio, R the universal gas constant, M_{gas} the gas molecular weight and T_{gas} is the gas temperature.
For the complicated structure of the flow meter, such analytical expression cannot be applied, anyway it has been found [25] that the following expression well approximates the common mode voltage behaviour with pressure:

$$V_{cm} = V_{cm0} \cdot \frac{p}{p + p_T} \tag{1.20}$$

where V_{cm0} is the high pressure limit and p_T can be experimentally extracted for any given gas as it depends on its physical properties (i.e. thermal conductivity at high pressures, molecular mass). A formula similar to eq. (1.20) is commonly used to represent the response of Pirani vacuum gauges to pressure. Surprisingly, a similar equation, but with a different value for the transition pressure, holds also for V_{out}, even if different phenomena, such as mass transport, are involved in producing the signal. The mass transport mechanism seems to reflect only on a lower transition pressure as reported in Fig. 1.28, where the inverse of the normalized signal V_{cm} is plotted as a function of the inverse of pressure for nitrogen. Provided eq. (1.20), the following relations holds:

$$\frac{V_{cm0}}{V_{cm}} = 1 + p_{T-CM} \cdot \frac{1}{p} \tag{1.21a}$$

$$\frac{V_{out0}}{V_{out}} = 1 + p_{T-OUT} \cdot \frac{1}{p} \tag{1.21b}$$

where $p_{T\text{-}CM}$ and $p_{T\text{-}OUT}$ are the transition pressure of V_{cm} and V_{out}, respectively. This pressure sensitivity is an intrinsic phenomenon due to the microscopic feature size of the integrated sensors and cannot be avoided. Anyway, the possibility to extract a common mode signal that depends on pressure, but does not depend on flow rate can be proficiently employed to realize a smart on chip compensation operated by the read out electronic circuitry as will be discussed in chapter 2.

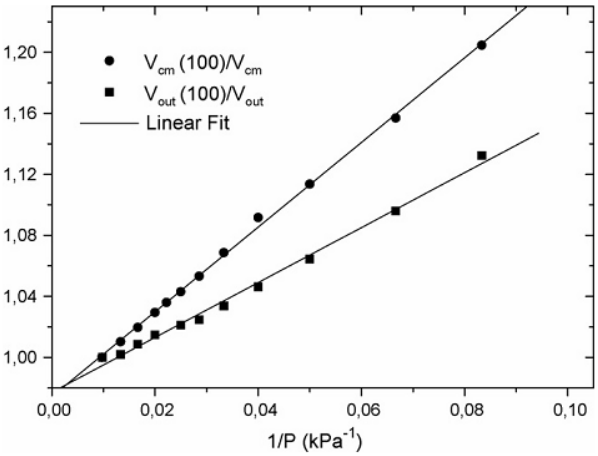


Fig. 1.28 – Plot of the measured $(V_{cm})^{-1}$ ad $(V_{out})^{-1}$as a function of p^{-1}. Following eqs. (1.21a-b), the different transition pressures, $p_{T\text{-}CM}$ and $p_{T\text{-}OUT}$, can be extracted from the slope of the two linear fits.

1.4 A CMOS compatible flow meter for liquids

The possibility of precisely monitoring very small liquid flows is of great importance for biomedical automatic analysis apparatuses and drug delivery systems. Micrometric integrated flow meters are optimal candidates for meeting the requirements of high resolution, compact size and low fabrication costs dictated by biomedical applications. Recently, commercial devices based on placing the chip outside the walls of a thin glass capillary pipe have been introduced into the market [28]. This solution presents clear advantages of robustness and electrical insulation but does not allow exploiting the full sensitivity of the sensing structures and requires chips of proper shape to allow placement of the capillary.
The solution proposed in this thesis match both the need of a low cost packaging technique with compatibility with standard package for electronic components.
The sensing structures are the same described in section 1.3.1, designed in the BCD6 process of STMicroelectronics. The package is of the same type of that described in section 1.3.2. with a slightly modified procedure in order to obtain an even more robust structure. A schematic cross-section of the chip is shown in Fig. 1.29.
The PMMA adapter, have a trench (0.5 mm wide, 1 mm deep) milled into its base which is accessed through two holes, by two stainless steel pipes, inserted into two opposite conveyor lateral sides. The base of the PMMA adapter covers the whole chip area (4 mm × 4mm) with the exception of the external pad frame.
The alignment procedure with the adapter to the sensing structures has been refined in order to precisely align the channel formed by the trench and the chip surface to the sensing structures. The alignment procedure, facilitated by the PMMA transparency, consists of two phases:

(i) a guide with an hole of the same cross-section of the adapter is roughly aligned to the chip centre;

(ii) the adapter is safely inserted into the guide with no risk of hitting the bonding wires and moved over the chip surface by finely adjusting the guide position.

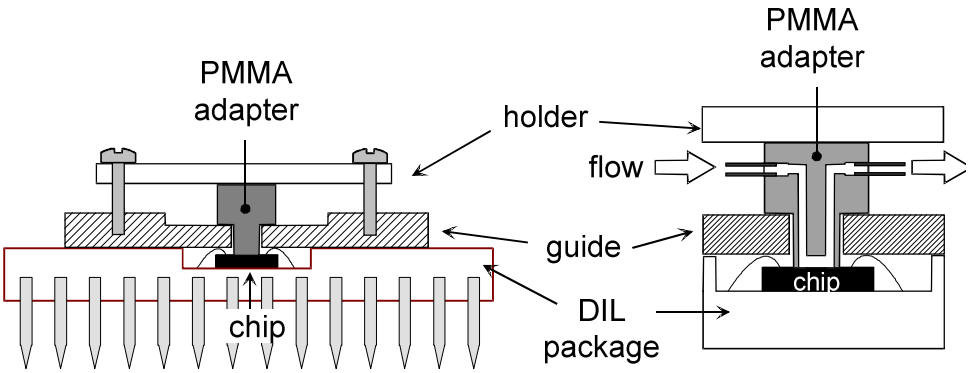


Figure 1.29 – Schematic view of the complete liquid flow sensor.

This operation occurs under an optical microscope while the fine alignment is made thanks to a micromanipulator. When a satisfactory alignment is reached, the guide is glued to the package and finally the conveyor is sealed to the chip by pressing the two parts together while heating the chip up to 110 ºC, slightly over the PMMA glass transition point. This allows an effective channel sealing while avoiding fluid leaks. Epoxy resin is put between the upper surface of the guide and the contrasting part of the adapter. An alternative solution may be represented by pouring directly the epoxy resin into the chip chamber, but in this case the dilatation during the thermal treatment would break the very fragile chip bondings. A proper holder screwed to the guide keeps the conveyor in place, and avoiding that thermal dilatation of the resin would displace the conveyor. The final structure of the packaged sensor is shown in Fig. 1.30.

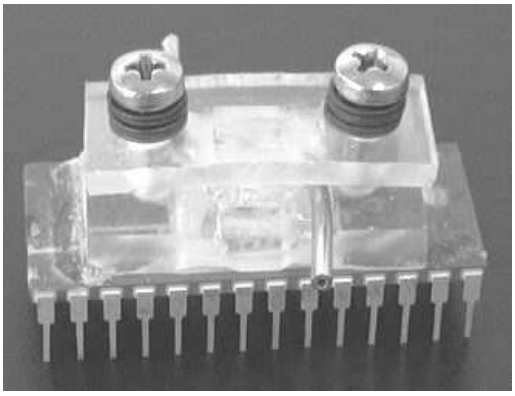


Figure 1.30 – Photograph of the liquid flow meter.

Tests of the sensor have been performed by connecting the device to a calibrated commercial drug delivery system, based on a motorized syringe. Experimental set-up is shown in Fig. 1.31.

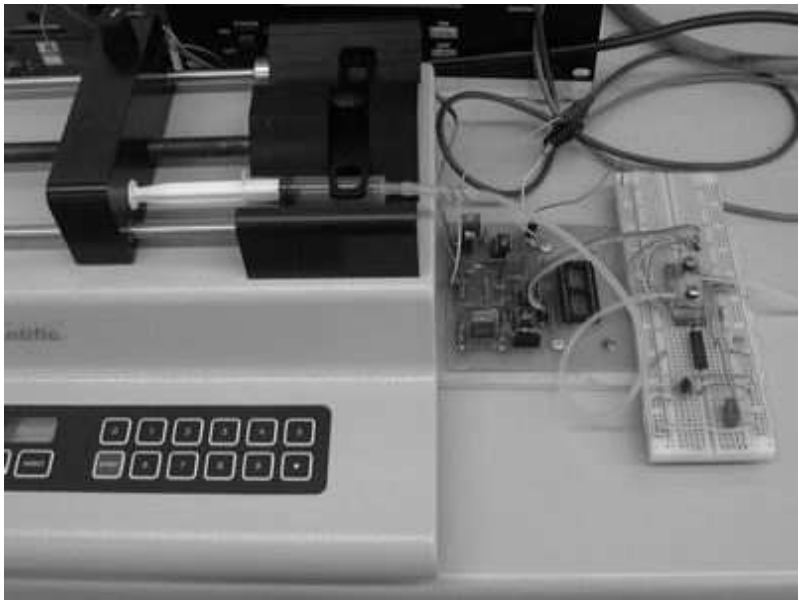


Figure 1.31 – Experimental set-up used to test the integrated liquid flow meter.

A low noise, low offset amplifier was used to read the output signal. The block diagram of the circuit used to bias the heater and read the signal is shown in Fig. 1.32. The thermopile output is read by the instrumentation amplifier IC1 (AD620) and filtered by the Sallen–Key low-pass cell based on IC2 (OP07). The upper band limit was set to 10 Hz in order to improve the signal to noise ratio. The total amplification of the IC1–IC2 cascade is 150. The heater is supplied with a constant voltage, tunable by means of resistor R_V. All the experiments have been performed supplying the heater with a constant voltage of 2 V derived from a resistive partition of the supply voltage, properly buffered with a unity gain connected operational amplifier.
Figure 1.33 shows a typical transient response of the output voltage obtained by incrementing a deionized water flow rate by steps of 2 ml/h. It is worth noting that although an offset is present it is precisely restored at end of the measure proving reversibility of the measure itself. A series of transient records have been performed in order to extract the sensor response. Results are collected in Fig. 1.34 where the responses to deionized water flow and ethanol flow are shown, respectively, after offset subtraction.
Negative flows have been obtained by swapping the inlet and the outlet connection. A sensitivity of 35 μV/(ml/h) for deionized water have been found. A resolution of 0.2 ml/h has been estimated by measuring the output response in condition of zero flow, resulting in a dynamic range in the order of 100. Due to the greater thermal conductivity of the two tested liquids with respect to commonly

used test gasses (N_2, Ar, Xe), the response is affected by fluid thermal conductivity besides specific heat making the sensor characteristic clearly non linear. Anyway it behaves monotonically in the explored ml/h range making the sensor suitable for biomedical application, such as precision drug delivery.

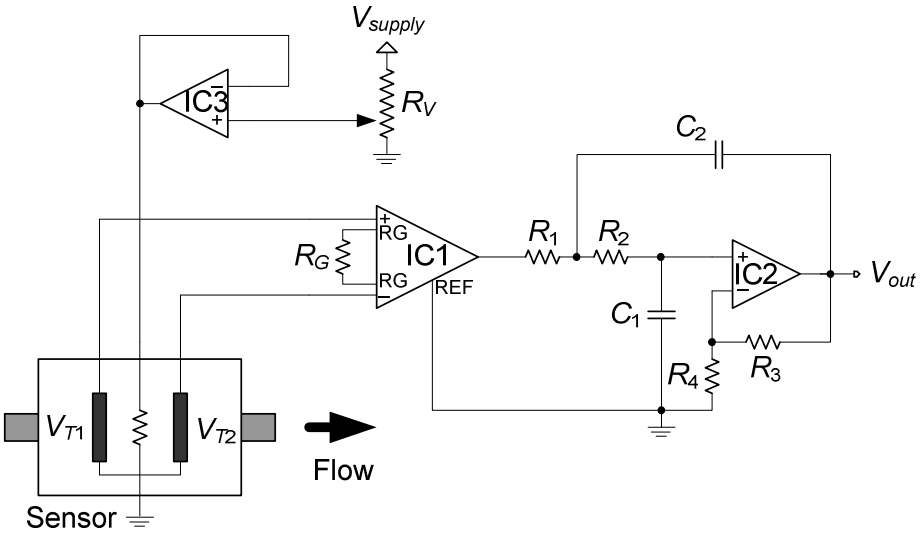


Fig. 1.32 – Schematic diagram of the circuit used to bias the heater and read the thermopile differential voltage.

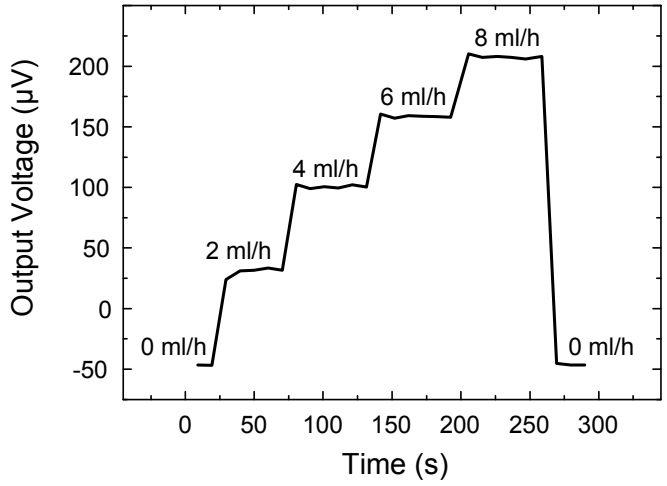


Fig. 1.33 – Schematic diagram of the circuit used to bias the heater and read the thermopile differential voltage

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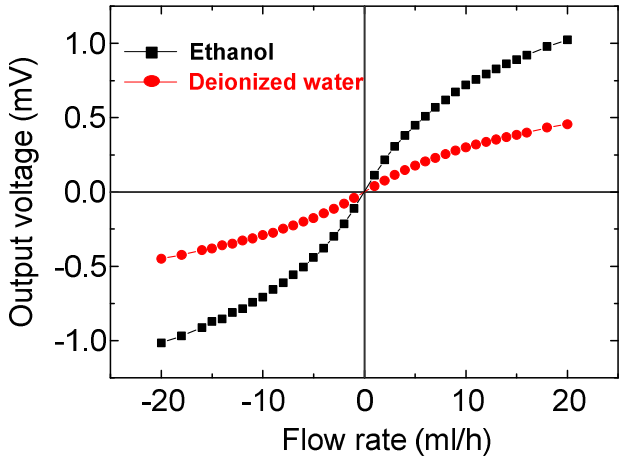


Fig. 1.34 – Schematic diagram of the circuit used to bias the heater and read the thermopile differential voltage

1.5 Prototype of a double channel flow-meter on a single chip

Sensing of multiple flows on the same chip and package is an interesting challenge that would enable an extreme miniaturization of this kind of devices. We explored this possibility with the local conveyor packaging technique described in section 1.3.2. to achieve this purpose. As the chip was designed earlier than the developing of the packaging method, the placement of the sensing structures was not optimized to include them in separate channels.
Nevertheless the method succeeds in overcoming the problems arising from the vicinity of sensing structures and their vicinity of them with respect to the pad frame.
The test chip layout is shown in Fig. 1.35. It was fabricated using the BCD6 process and it was equipped with a certain number of sensing structures similar to that described in section 1.3.1, where three different thermopile types were present: p-polysilicon/Al (PA), p-polysilicon/n-polysilicon (PN) and n-polysilicon/Al (NA). Unfortunately, most structures, designed using NA thermopiles, exhibited a near zero sensitivity, probably due to the low value assumed by the NA couple in the BCD6 process. On the other hand, the only two different structures, one of PA and the other of PN type, showed a high sensitivity; however, their placement was not favourable for the packaging phase, due to their small spacing and vicinity of the bonding pad frame.
A new PMMA adapter purposely designed to include the PA and the PN structures on a separated channels was developed. The adapter face, which is placed into contact with the chip, is slightly smaller than the pad frame, so that it can be easily applied after bonding of the chip. Trenches of proper shape and position are milled on the adapter face, in order to make the gas flow interact with selected chip areas. The trenches are accessed by means of cylindrical holes perpendicular to the chip surface. The holes, that terminates on the opposite adapter face, can be connected to gas lines by means of capillary pipes. Sealing of the trenches to the chip surface was obtained using the thermal procedure explained in section 1.3.2.

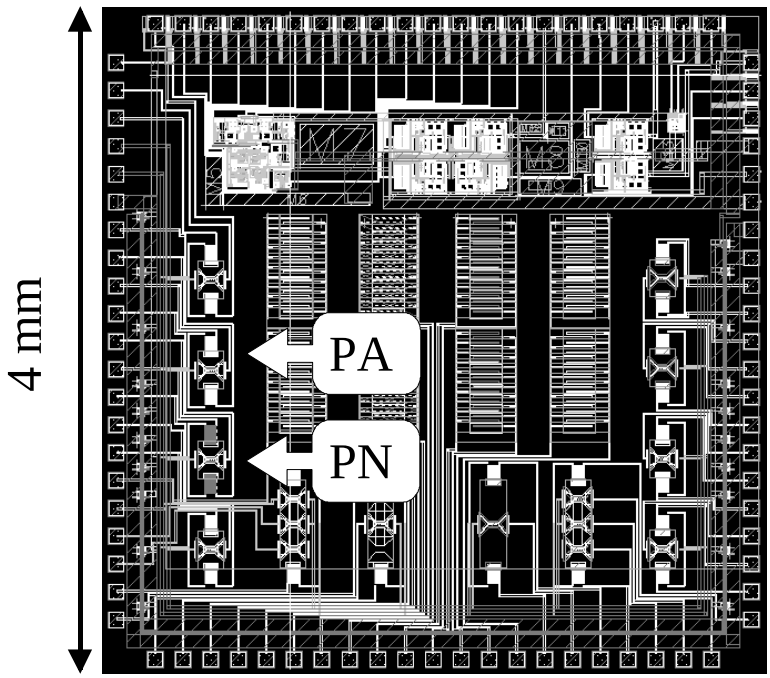


Fig. 1.35 – Placement of the PA and PN sensing structures on the chip layout

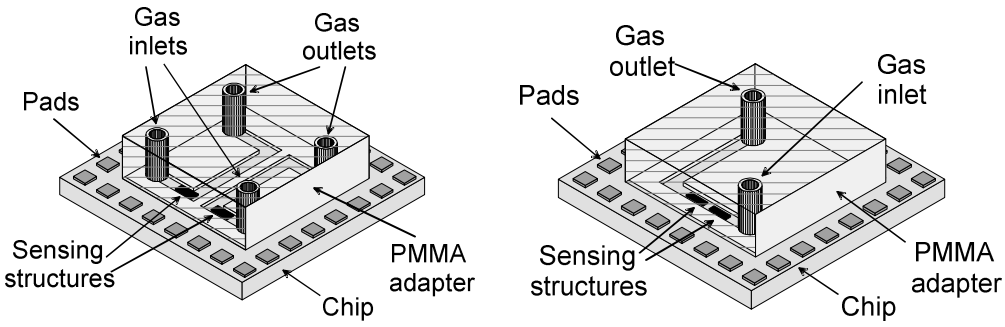


Fig. 1.36 – Perspective view of: (a) the proposed device and (b) the referencesingle channel device

Two different configurations of the trenches were used: the first one, shown in Fig. 1.36(a) consists of two independent U-shaped trenches, including the PA and PN structure, respectively on distinct channels. The second configuration, shown in Fig. 1.36(b), consists of a single L-shaped trench, including both sensing structures on the same channel, is used for reference purposes.

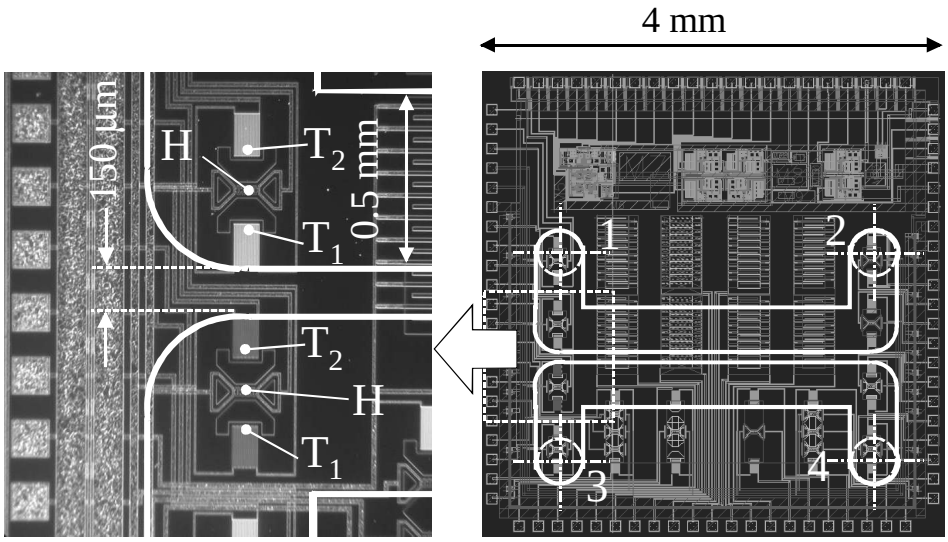
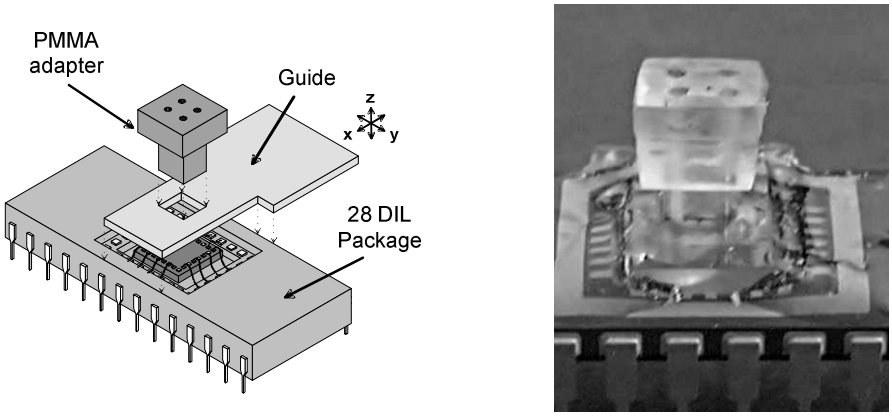


Fig. 1.37 – Layout of the designed chip with the channel path

In both cases the trenches have a 0.5 mm × 0.5 mm rectangular cross-section. The position of the trench on the chip surface in the case of Fig. 1.36(a) is shown in Fig. 1.37 (right), where the actual chip layout and dimensions are reported. The micrograph on the left shows an enlargement where the sensing structures are placed. The thermopiles (T1 and T2) and heater (H) are indicated for both structures.

The small spacing between the sensing structures imposed to reduce the thickness of the wall separating the two trenches (150 µm), requiring a fairly good precision in the mechanical fabrication of the adapter. Hardness of the plastic material was essential to allow the milling of trenches. Alignment of the adapter to the chip was performed using a guide, in the two step method (coarse/fine) described in section 1.4. This allowed: (i) precise alignment of structures with channel preserving the bonding wires to be accidentally hit and (ii) efficient sealing of the channel dispite of any roughness of the chip surface. After the alignment, the guide was glued to the package surface by means of an epoxy resin. A schematic view of the assembling procedure and the final device is shown in Fig. 1.38(a) and (b), respectively. It is important to observe that this manual procedure can be avoided in an industrial process, where it is possible to glue all the chips in a precise position of the package chamber and then simply align the guide to reference marks on the package itself.

Another unwanted consequence of the structure position and orientation was the necessity to place them practically inside a 90° curve of the flow channel. Considering that the type of sensing structure used in this work is sensitive only to the gas velocity component along the thermopile-heater direction, a sensitivity reduction was expected with respect to the case of Fig. 1.36(b), where both structures are oriented along the gas streamlines.



(a) (b)

Fig. 1.38 – (a) Perspective view illustrating the device assembling and (b) photograph of the final device.

Characterization of the devices was performed in nitrogen flow by means of a reference line, equipped with two mass flow controller (MKS 1179B) with 10 sccm and 200 sccm full scale range, respectively. The gas line structure is schematically shown in Fig. 1.39.

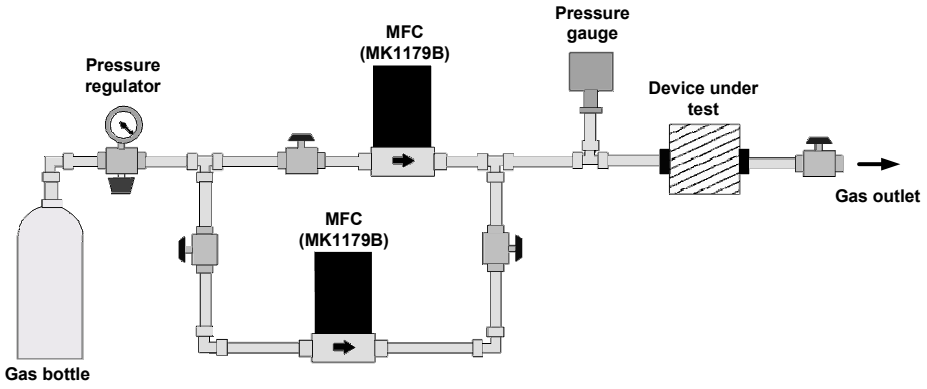


Fig. 1.39 – Structure of the gas line used for sensor characterization.

The gas flow was applied to the devices by inserting a stainless steel pipe of 0.7 mm external diameter (syringe needle), into each one of the four upper orifices, in turn. Shifting the needle to one orifice to the other allowed testing of the two channels in both flow directions. Before each measurement run, the needle was sealed to the orifice by means of silicone glue, which was easily removed after the measurement in order to extract the needle and insert it in the next orifice. The thermopile output signal was read by means of a purposely built interface board, including a low noise instrumentation amplifier (AD 620), a second order 10 Hz low pass filter and a constant voltage source to bias the sensor heaters (see Fig. 1.32). In all the experiments the heaters were supplied by a constant voltage of 2 V,

corresponding to a power of 4 mW for each sensing structure. The output voltage value at zero flow (offset voltage) is subtracted from all the measurements.
As a first test, the cross-sensitivity between the two measurement channels has been tested. To this aim, flow rates up to 50 sccm have been injected into one channel while measuring the output signal of the other one. In all the experiments no measurable cross-talking was detected, confirming the excellent sealing of the channels.

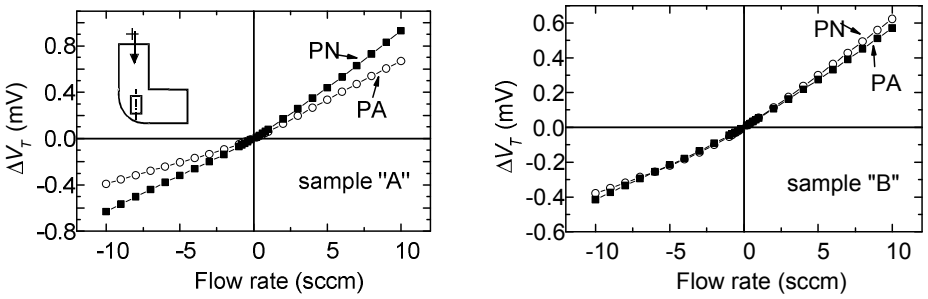


Fig. 1.40 – Response of double channel sensors to nitrogen flow. Plots (a) and (b) refer to distinct samples. For each sample the response of both channels are shown. The channels are identified by the type of thermopile of the corresponding sensing structure (PA = p-poly/ n-poly, PN = p-poly/Al)

The dependence of the thermopile output voltage on the flow rate is shown in Fig. 1.40. Graphs (a) and (b) refer to two distinct samples, nominally identical in terms of fabrication procedure and dimensions and indicated as sample ‘‘A’’ and ‘‘B”, respectively. For both samples, the response of the two channels equipped with the p-poly/n-poly (PN) and p-poly/Al (PA) thermopiles, respectively, is shown in the figure. The conventional positive flow direction is indicated in the inset of Fig. 1.40(a), where the channel elbow with the sensing structure (rectangle) is represented. The dashed line drawn over the rectangle represents the direction of maximum sensitivity of the sensing structure (i.e. the line joining the thermopiles and the heater). Considering Fig. 1.37, conventionally positive flows enter from inlet 1 and inlet 3 for the upper and lower channel, respectively. In the following discussion with the term sensitivity we will indicate the derivative of the response curve at a given flow rate value.
The more evident anomaly, visible in all curves, is the sensitivity mismatch between the responses at negative and positive flows. However, considering sensitivities estimated at very low flow rates (0.2–0.8 sccm) the asymmetry is much less evident, as shown by the data reported in table 1.IV.
It should be noted that the Reynolds number, calculated for straight channels of identical cross-section of those used in this work, is much lower (< 200) than the critical value over the whole flow range. Therefore, transition to turbulent flow cannot be invoked to explain the sensitivity mismatch occurring at moderate flow rates. The only exception is represented by turbulences localized into the bends that can arise at much lower Reynolds numbers than in straight ducts. A reasonable mechanism capable of explaining the observed asymmetry is proposed in next section.

To further characterize the role of the channel geometry in determining the observed response features, experiments have also been performed placing both sensing structures of type PN and PA into a straight channel segment. To this aim, the single channel device configuration of Fig. 1.36(b) has been used. The results, are shown in Fig. 1.41, while the corresponding sensitivities are also reported in table 1.IV (sample ‘‘S’’).

Sample	***Structure***	***Flow 0.2-0.8 sccm***		***Flow 2-10 sccm***	
		+	–	+	–
A	PN	83	80	95	61
	PA	65	55	68	37
B	PN	56	53	64	34
	PA	54	47	68	37
S	PN	610	610	370	270
	PA	380	390	180	170

Table 1.IV – Average slopes (μV/sccm) for double channel (A, B) and single channel (S) samples at low and moderate flow ranges.

The higher symmetry of sample S response clearly indicates that the asymmetry of samples A and B can be ascribed to the placement of the sensing structures into channel bends. The noticeable asymmetry present also for the PN structure of sample S at moderate flow rates is probably due to the proximity of this structure to one of the two channel inlets (Figs. 1.36, 1.37(b)). The data of table 1.IV indicates also that placing the structures into channel bends produces important sensitivity degradation, by a factor varying from 4 to 8, depending on the flow range. Note that comparison between different samples is meaningful only if structures of the same type (PN or PA) are considered.

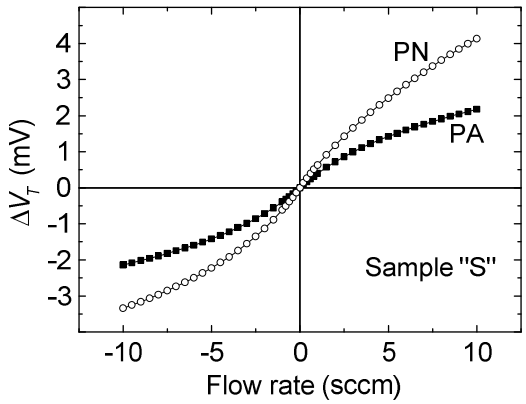


Fig 1.41 – Response of the two sensing structures placed inside the same L-shaped channel (reference sample).

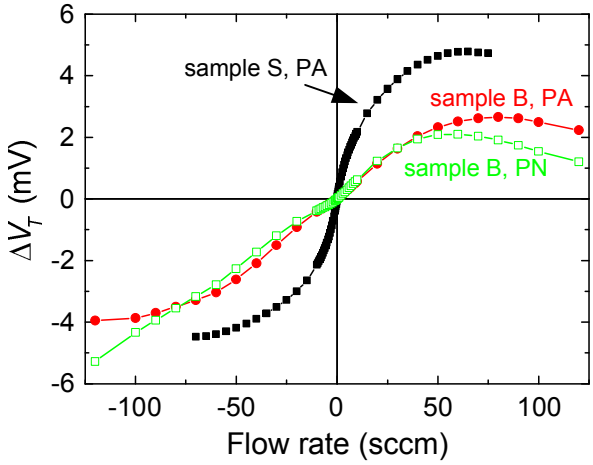


Fig. 1.42 – Comparison between sample S (straight channel) and sample B (structure inside a bend) for high flow rates.

The difference between placing the structures into channel bends or straight segments is also more evident at high flow rates, as shown in Fig. 1.42, where the responses of sample B and S for flow rates up to 120 sccm are compared. In all curves it is possible to observe the tendency to reach a maximum followed by a slope reversal. This is in agreement with the typical behaviour observed in several works about differential thermal flow meters. Explanation of the phenomenon is controversial: possible explanations are

(i) cooling of the entire structure, including the heater
(ii) the reduction of the thermal boundary layer down to the dimension of the heater–thermopile gap [29].

The only exception is the PN structure of sample B at negative flows, where the maximum falls probably at higher flow ranges where it was not possible to extend the investigation due to the onset of large instability in the response.
Note that the response of sample S, albeit getting strongly non linear, remains practically symmetric also in this extended flow range, differently from sample B that reaches a significantly lower maximum value for positive flows than for negative ones. For all cases, the observed strong non linearity practically limits the use of the sensors to the range ±50 sccm.

1.5.1. Fluid-dynamic simulation of the velocity profile

The strongly non-uniform velocity distribution in channel bends combined with the complicated dynamics of convective heat transfer prevent from finding a simple interpretation of the observed response deterioration of the two channel flow sensor (samples A and B) with respect to the single channel sensor (sample S). To add useful information we have created a simple three-dimensional FEM model and solved it by means of the COMSOL Multiphysics™ environment. The model, schematically shown in Fig. 1.43, consists in a channel with a 90° bend. No-slip flow conditions are applied to all the channel walls. A parabolic velocity distribution

is applied either to the P or the N inlet, producing conventionally positive or negative flows, respectively. A pressure of 100 kPa was fixed at the outlet port. The simulated fluid was nitrogen.

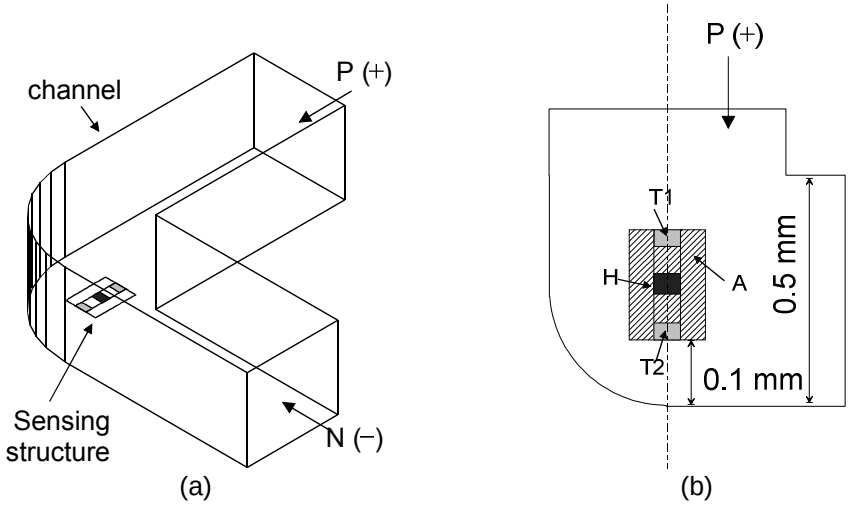


Fig. 1.43 – Model of the flow channel used in the FEM measurements.

The model was solved only for fluid-dynamic equations, in order to determine the velocity distribution over the sensing structure. The latter, placed on the channel bottom wall as shown in Fig. 1.43(a), is represented by a flat (2D) arrangement of areas, shown in Fig. 1.43(b), corresponding to the heater (H), thermopile cantilevers (T1 and T2) and cavity (A). The dimensions of the heater and thermopile areas and the gap between them are the same as in the real configuration. Indicating with T_1 and T_2 the temperatures of the T1 and T2 thermopiles, respectively, we consider as the output signal the difference $T_2 - T_1$. The average gas velocity at the inlet port was varied to simulate flow rates in the same range as the experimental results.

A first important result was that, over the whole explored flow rate range (0-15 sccm), negative and positive flows produce practically symmetrical velocity distributions over the sensing structure area. This clearly indicates that the mentioned hypothesis of asymmetries in the velocity fields caused by localized onset of turbulence cannot be invoked to explain the response anomalies. A more reasonable explanation can be formulated by considering Fig. 1.44, where the simulated velocity field over the sensing structure (on a plane parallel to the channel bottom and 50 μm over the latter) is plotted for a flow rate of 7.5 sccm.

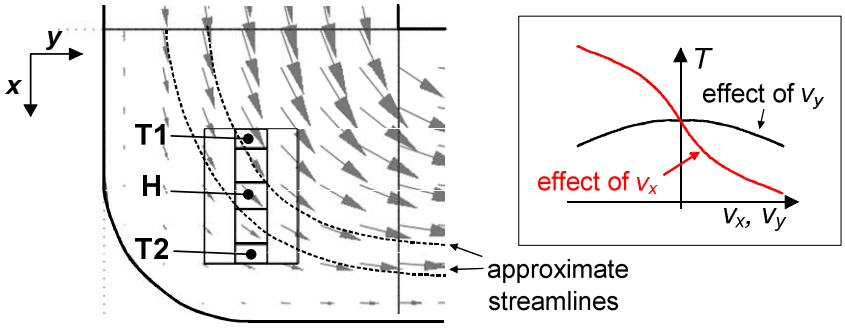


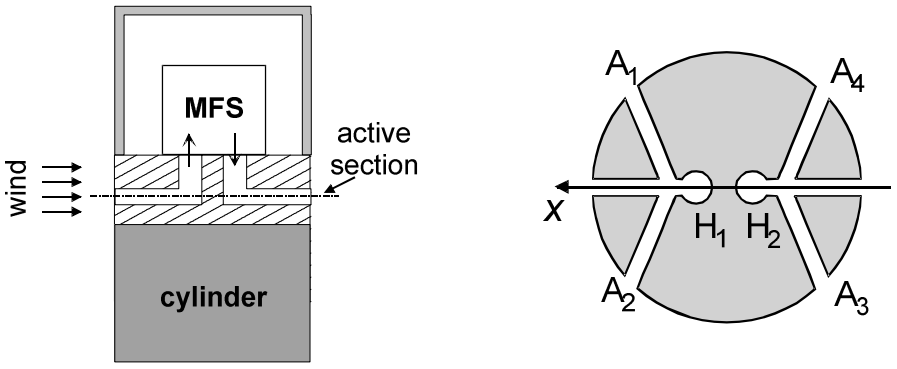
Fig. 1.44 – Simulated velocity field on a channel bend (left) for a 7.5 sccm flow rate and qualitative supposed behavior of the thermopile T1 temperature variations caused by the v_x and v_y components (right).

The heat removed by the flow from the heater tends to be convectively transported along the path confined between the two streamlines shown in the figure.
The fact that most of the thermopile area is out of the main heat convective path is probably the reason of the much smaller sensitivity of samples A and B with respect to sample S. The latter, indeed, being placed into a straight channel is exposed to streamlines parallel to the heater-to-thermopile direction (*x* axis in Fig. 1.44). In order to explain also the response asymmetry, it should be observed that the velocity component along the x axis (v_x) produces heating of a thermopile when directed from the heater to the thermopile and cooling in the opposite case. On the contrary, the *y* component (v_y) removes heat from the thermopile, producing cooling of the latter regardless of the direction. To better illustrate this idea, the temperature variations induced by the two velocity components on T1 has been qualitatively represented in Fig. 1.44 (on the right, inside the dashed box).
A second fact is that, as shown by the arrow length, the gas velocity is much higher at thermopile T1 which, for this reason, will dominate the response at low and moderate flow rates. For positive flows, the effect of v_y on T1 enhances the cooling effect of v_x. For negative flows the two effects are opposite, thus the heating effect of v_x on T1 is reduced (see the inset of Fig. 1.44).
As a consequence, the sensitivity of the response is higher for positive flows than for negative ones, as observed in the results. Since the cooling effect of v_y is symmetrical with respect to flow reversal, its first derivative with respect to v_y should be zero for $v_y = 0$. For this reason the effect of v_y should be negligible at very low flow rates, just where the sensitivity difference tends to disappear (see table 1.VI).
The opposite situation occurs at thermopile T2 but, due to the smaller local intensity of the velocity, the contribution to the output signal variation is smaller and does not compensate the asymmetry introduced by T1. For very high flows (see Fig. 1.41), T1 tends to saturate while T2 becomes more significant. In particular, for high positive flows, a heated gas particle that leaves the heater region and travels downstream following the streamlines has not enough time to diffuse laterally and skips thermopile T2 (see Fig. 1.42). In these conditions, T2 stops increasing flow and eventually starts decreasing, producing the slope inversion visible in Fig. 1.42. For high negative flows, T1 will probably experience a slope inversion as well, but,

since the streamlines going out of the heater does not completely skip the T1 area, this is expected to occur at a higher flow rate.
These complicated phenomena are strongly dependent on the non-uniformity of the velocity intensity and direction in channel bends. The actual position of the structure into the bend is then expected to have a significant influence on the sensor response. Considering the low resolution of the PMMA adapter alignment to the chip, this can be the cause of the difference between the responses of sample A and B.
Reasonably, the design of a new chip with sensing structures with more favourable placement and orientation would eliminate this problem. However, the effective separation of the two flows, even in this critical configuration, has been demonstrated through the local flow confinement technique applied to a standard chips.

1.6 Compact anemometers for wireless sensor network nodes

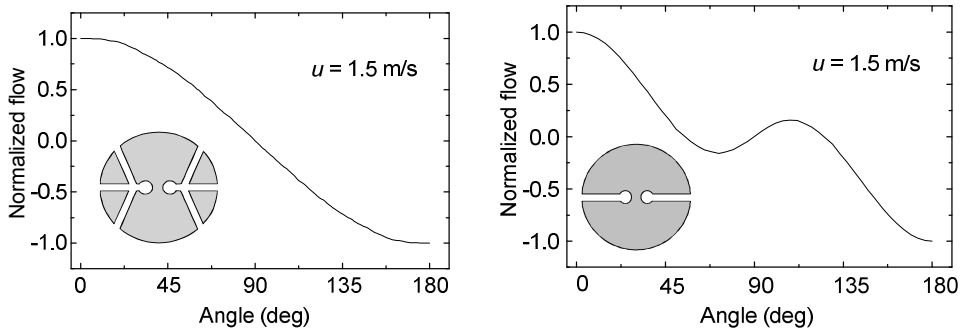
The development of compact anemometers, capable of being interfaced with wireless sensor network (WSN) nodes, has several potential applications, ranging from pollution monitoring, airport wind surveillance, plantation disease spreading prediction and optimization of air circulation in food storage and drying rooms.
The possibility of deploying low cost networks in a short time for capillary detection of the wind distribution can be a key element for predicting the evolution of pollution accidents.
Traditional mechanical anemometers are not easily scalable, since, similarly to micro-motors [30], reduced size devices present unfavourable drag-to-force ratios, resulting in low sensitivity and irregular rotation. Ultrasonic anemometers are being proposed as a relatively robust and durable alternative to mechanical wind sensors. However, the requirement of proper spacing between the acoustical transducers prevented miniaturization below dimensions of several centimeters [31]. Macroscopic thermal sensors are very sensitive devices but their power consumption rules out their application in battery powered WSN nodes [32].
Use of integrated MEMS thermal anemometers is often claimed as a method for significantly reducing power consumption. Unfortunately, their fragility does not allow direct exposure to the wind in real situations. Thus, an innovative approach for protecting MEMS thermal anemometers while providing the necessary interaction with the air flow, has to be investigated.
A possible solution is shown in Fig. 1.45(a). The wind stream creates a pressure distribution around the external surface of the cylinder that depends on both the wind speed and direction. Only wind velocities lying on a plane perpendicular to the cylinder axis are considered (2D anemometer). The pressure differences are sampled by apertures in the cylinder surface, connected to the channel structure depicted in Fig. 1.45(b) [33]. The reference axis of the channel structure is indicated with *x*. Besides the apertures along *x*, other four apertures indicated with $A_{1\text{-}4}$ are introduced. The flow sensor (MFS), identical to that described in section 1.3.1-1.3.2, is connected across H_1 and H_2, thus measuring a flow proportional to the pressure difference across these points.



(a) (b)

Fig. 1.45 – Structure of the proposed anemometer showing the placement of the integrated mass flow sensor (MFS) (a); configuration of the active section (b).

The channel configuration is optimized by means of fluid dynamic simulations in order to produce a flow through the MFS proportional to the cosine of the angle formed by the wind with axis *x*. Simulations have been performed using the COMSOL Multiphysics™ environment. The best cosine approximation was obtained with apertures A_1, A_3 and A_2, A_4 placed across diameters forming angles of 40º and -40º angle with *x*, respectively.
The dependence of the flow rate on the wind direction, obtained with the optimized configuration, is shown in Fig. 1.46(b). The maximum difference from the ideal cosine curve is about 2.5 %. Using this characteristic, a 2D wind sensor capable of detecting the wind direction can be easily obtained by combining two devices such that of Fig. 1.45(a) mounted with perpendicular reference axes. In this way two flows $Q_X = f(u)\cos(\theta)$ and $Q_Y = f(u)\sin(\theta)$, where $f(u)$ is a function of the wind velocity u and θ the angle formed by the wind with *x,* are produced.



(a) (b)

Fig. 1.46 – Simulated flow through the MFS in the case of (a) the optimal structure and (b) a simpler active section with only the two aperture along the reference diameter x.

The wind direction θ and *f*(*u*) can be estimated by simple trigonometric operations, while the wind velocity can be extracted from *f*(*u*) after calibration. It is worth noting that with simpler structures proposed in existing patents [34], where sensing of only one diametric pressure difference is proposed, the non monotonic behaviour of Fig. 1.46(b) can be expected.
This approach was feasible thanks to the very compact packaging approach discussed in the previous sections of this thesis. The cylinder diameter is 3 cm and the height 14 cm. The sensor has been characterized within a small wind tunnel for a velocity range from 1 to 8 m/s. Angle variation was obtained by rotation of the cylinder. An example of curves obtained at a wind velocity of 2.7 and 5 m/s is shown in Fig. 1.47 where the ideal cosine curves fitting the data are shown for reference. A monotonic behaviour in good approximation with the target cosine curve can be observed.

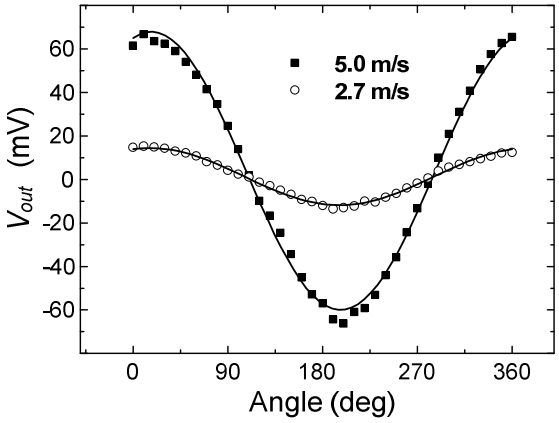


Fig. 1.47 – Figure 3. Sensor output signal as a function of the wind direction (angle θ) measured at two different wind velocities. The solid lines are the best cosinusoidal fittings.

The curves are slightly shifted by about 10 degrees with respect to the zero angle reference possibly due to mechanical misalignment between the actual active section symmetry axis and sample holder used in these preliminary experiments.

2. INTERFACE ELECTRONICS FOR INTEGRATED THERMAL FLOW-METERS

In this chapter will be discussed the electronic interface design for the flow sensors presented in the previous chapter. Starting from the definition of sensors characteristics and requirements, the rational design of an amplification chain based on chopper modulation is presented. The driving circuits, compensating for pressure drop of sensors sensitivity are also discussed. Furthermore, insight in the design of linear CMOS transconductors, usable both for low frequency Gm-C filters and full analog multiplier, is presented.

2.1 Requirements and sensor electrical characteristics

The electronic front end has a fundamental role in the overall performances of the system as it is charged of extracting the very low level signals from the sensing structures preserving its information content, i.e. adding as less noise as possible while preserving it from any form of interferences, or eventually cross-talking.
Besides, band-limiting is always a desirable feature as it is a good method to clean out the useful signal from out of band noise and spurs, and it is needed whenever the signal is be conveyed on a shared channel or when it has to be processed by an A/D conversion stage. For example an A/D conversion is needed prior to a bus or wireless transmission.
In this chapter we will show an interface optimized for integrated flow-meter discussed in the previous chapter. The design of the CMOS integrated interface have been coped with an analytical approach purposed to frame the impact of the high resistance and low signal bandwidth of thermopile sources.
The various cells constituting the electronic front end has been studied and designed with particular attention to the precision *vs.* noise tradeoffs, temperature sensitivity, and silicon area saving.
Despite the techniques described in this chapter are focused on thermal sensors interfacing, they are pertinent to a wide range of general sensing methods. Only to mention some but few examples:

- Bolometers and infra-red thermoelectrical sensors [35,36];
- Chemioresistors, and sensing of chemical quantities [37];
- Spinning current hall plates [38];
- Nerve cuff electrodes [39].

All of this types of sensors, together with the majority of thermal sensors present an electrical resistance, which may range from few kilo-omhs to several hundred of kilo-ohms. Signal bandwidth is restricted to few hundred of hertz beyond the DC component, and hardly can reach the millivolt range at full scale. Thus, with typical required resolutions (greater or equal to 8 bits), precision below few microvolts has to be obtained. This cannot be done with static CMOS amplifiers, as they show offsets of some millivolts, and are affected by flicker noise that tends to diverge at very low frequencies [40]. Dynamic techniques are available such as auto zero (AZ) and chopper stabilization/modulation (CHS).
They works on very different principles as the former periodically samples offset and noise and subtract them to the signal, while the latter is simply a

modulation/demodulation combination that allows to signal to pass through the amplifying stage at frequencies where the noise is less severe.
Due to its intrinsic sampling process, AZ may result unfit in case of an high resistive source, which owns its own high frequency noise, as it will be folded in the base band a number of times proportional to the ratio of amplifier bandwidth over sampling frequency. On the other hand, chopper modulation, which will be briefly described in the following discussion, does not operate any sampling and the noise characteristics of the source are not altered.
As we have already seen in chapter 1m sensing structures are formed by thermopiles, obtained by series connection of several thermocouples, each of those consists in a connection of different conductive layers. In a CMOS/CMOS-compatible process the use of *n*-polysilicon/*p*-polysilicon or *p*-polysilicon/aluminum couples is the typical choice.
The DC signal (V_{TH}) and root mean square (RMS) value of the thermal noise (V_{NTH}) produced by a thermopile, made of a series of *n* thermocouples are given by

$$V_{TH} = n \cdot \alpha \cdot \Delta T \; ; \tag{2.1}$$

$$V_{NTH} = \sqrt{4k_B T \cdot n \cdot R_T \cdot B} \; . \tag{2.2}$$

Here α and R_T are the sensitivity (Seebeck coefficient) and resistance of a single thermocouple, respectively, k_B is the Boltzmann constant, B is the bandwidth of the readout channel and ΔT is the temperature difference sensed by the thermopile. For a given bandwidth, which may be dictated by application, the minimum detectable temperature difference is given by:

$$\min(\Delta T) = \frac{1}{\alpha}\sqrt{\frac{4k_B T \cdot R_T \cdot B}{n}} \; . \tag{2.3}$$

Therefore, to improve the resolution it is desirable to increase *n*. In practice, value of *n* up to a few tens, are customary in MEMS with dimensions of several hundreds microns.
It should be observed that integrated thermopiles are based on polysilicon, which, differently from metals used in conventional thermocouples has sheet resistance in the range 10-100 Ω. As a result R_T, is typically of order of several kilo-ohms and the total thermopile resistance ($n \cdot R_T$) falls around 100 kΩ and beyond. It is also important to observe that, in many thermopile based integrated sensors, such as flow-meters and bolometers, the temperature variations to be detected are as small as to require a resolution of the order of 1 μV on the output signal.
A chopper stabilized (CHS) amplifiers is then required to cancel the input offset and minimize the residual baseband noise. The mentioned high output resistance of integrated thermopiles relaxes the amplifier requirements in terms of input noise, but, at the same time, introduces a few peculiar problems that will be discussed in the following sections.

2.2 Design of CMOS chopper amplifiers for thermal sensor interfacing

Figure 2.1 shows the block diagram of a typical chopper stabilized amplification chain. The thermopile has been considered to be split into two identical parts of

$n/2$ elements each, represented by the sources $V_{dS}/2$ and $-V_{dS}/2$. The central terminal is used to apply a common mode voltage to comply with the input range of the next stage, indicated with AMP. The latter is a CMOS, continuous time fully differential amplifier with gain A_D and an upper frequency limit much higher than the frequency of the input pole, deriving from the input capacitance C_{IN} and source resistance $R_S = nR_T$. The modulator S1 and demodulator S2, controlled by a clock signal of frequency f_{CH}, ideally introduce multiplication by 1 and −1 in the first and in the second half clock period, respectively.
Due to the time constant R_SC_{IN}, the signal at the amplifier input $V_{IN}(t)$ is not an ideal square wave (see Fig. 2.1). As a result, the demodulated signal V_A is not a constant voltage but short pulses at frequency $2f_{CH}$ are present. The latter are suppressed by the low pass filter LP but the output DC value is altered by the amount ΔV, as schematically shown in Fig. 2.1.

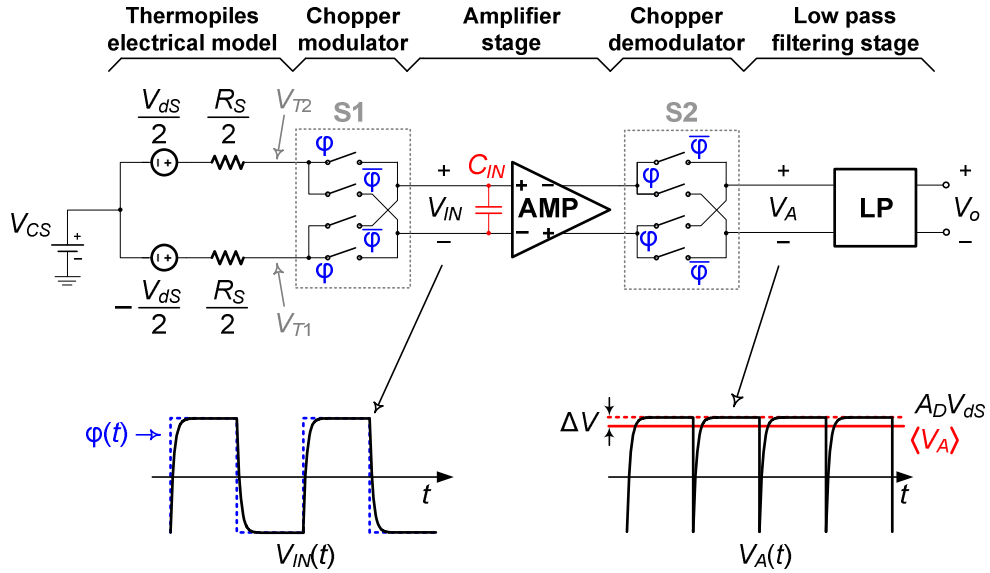


Fig. 2.1 – Block representation of a chopper stabilized amplifier. Waveforms $V_{IN}(t)$ and $V_A(t)$ refer to the case of constant V_{dS}.

It can be shown that, for an input DC signal this effect is equivalent to introduce a gain error, the relative value of which is given by

$$\varepsilon_G = \frac{\Delta V}{A_D V_{dS}} = 2f_{CH}C_{IN}R_S \,. \tag{2.4}$$

where A_DV_{dS} is the ideal output voltage. This error is particularly detrimental and has to be minimized, since it depends on the source resistance and amplifier input capacitance, affected by large temperature and/or process variations.
Since the number n of thermocouples, and thus R_S, is fixed by the desired temperature resolution through eq. (2.3), viable alternatives involve reducing either

C_{IN} or f_{CH}. Unfortunately both options produce an increase of the residual equivalent noise spectral density (S_{Veq}), and should then be applied carefully.
To understand this, we will introduce the following simplifying conditions:

(i) the RTI (referred to the input) noise of block AMP can be completely ascribed to its input MOSFETs;
(ii) the frequency f_{CH} is well below the flicker noise corner frequency, so we can neglect thermal noise;

The first condition can be reached by proper design choices, as shown later, while the second is reasonable, due to the typical high flicker noise coefficients of MOS devices. We will also assume that

(iii) the input capacitance C_{IN} can be written as:

$$C_{IN} = k_C C_{ox} WL \,. \tag{2.5}$$

where W and L are the width and length of the input MOSFETs, respectively, while k_C is a constant factor, depending on the amplifier topology. The intrinsic parasitic capacitance of the thermopile will be assumed to be negligible with respect to the amplifier input capacitance. We will first find a general relationship, useful to estimate the best noise figure that can be achieved. With the above assumptions, the equivalent RTI noise of the chopper amplifier is given by [40]:

$$S_{Veq} \cong 0.85 \cdot \frac{S_{VF}(1)}{f_{CH}} \,. \tag{2.6}$$

where $S_{VF}(1)$ is the RTI flicker noise density at 1 Hz for amplifier AMP.
Using a simple noise model and recalling condition (i):

$$S_{VF}(1) = m \frac{k_F}{WL} \,. \tag{2.7}$$

where k_F is the flicker noise coefficient, m the number of input devices with width W and length L. The noise figure F can be written as:

$$F = 1 + \frac{S_{Veq}}{4kTR_S} \,. \tag{2.8}$$

Putting together Eqns. (2.4–2.8), we get the best noise figure $F_{\min}$:

$$F_{\min} = 1 + 0.85 \cdot \frac{k_F C_{ox}}{2kT} \cdot \frac{mk_C}{\varepsilon_G} \,. \tag{2.9}$$

Equation (2.9) states that, once the acceptable gain error ε_G and the amplifier topology have been decided, the best noise figure depends only on process parameters or physical constants. Another important general expression is obtained relating the noise figure to the chopper frequency f_{CH} and the input transistor area WL. From Eqns. (2.5–2.8), we get:

$$f_{CH} = \frac{0.85 \cdot m \cdot k_F}{4kTR_S(F-1)WL}. \quad (2.10)$$

Equation (2.10) gives the clock frequency necessary to obtain a given noise figure with a given input device gate area. It is important to observe that, in many thermal sensors, the required signal bandwidth is at most a few hundred hertz, allowing the reduction of the clock frequency down to a few kHz with no consequences on the signal. Decreasing the clock frequency proportionally reduces the residual offset due to parasitic spikes introduced by the input modulator that should be otherwise mitigated with more complicated pass band amplifiers [36] or nested chopper configurations [38]. Equation (2.10) clearly states that a low clock frequency is paid in terms of device area; furthermore, for a given noise figure and chip area budget, the higher the source resistance, the lower the clock frequency. The application of these relationships to the design of a practical chopper amplifier will be illustrated in the following discussion.

2.2.1. Instrumentation amplifier topology and analysis

The instrumentation amplifier schematic, shown in Fig. 2.2, is based on conventional folded cascode architecture. The use of the OTAs in the input stage enhances the voltage follower function of M1 and M2, resulting in improved linearity and lower temperature sensitivity of the amplifier. The gain is given by the ratio of the output differential resistor R_2 and the source degeneration resistor R_1, i.e. $A_D = R_2 / R_1$.

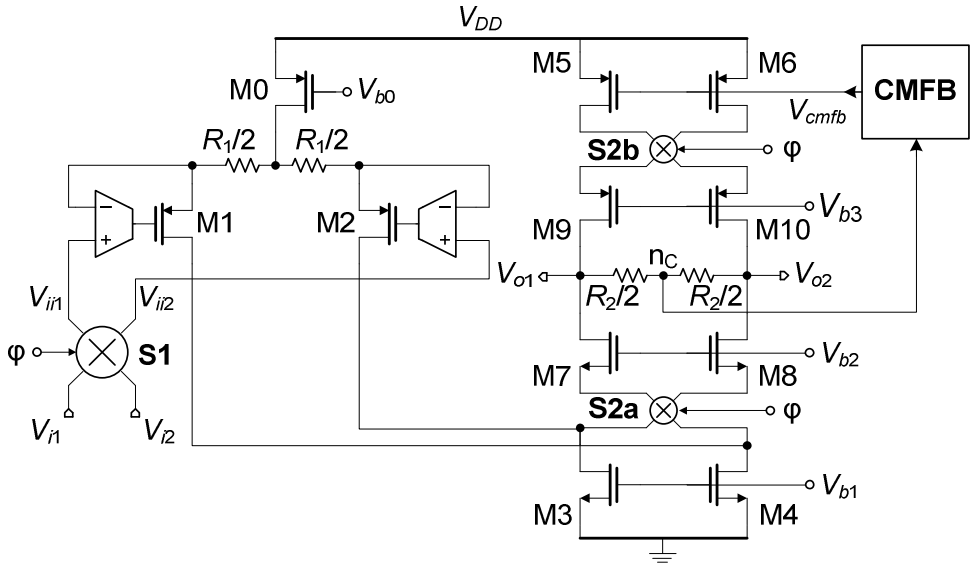
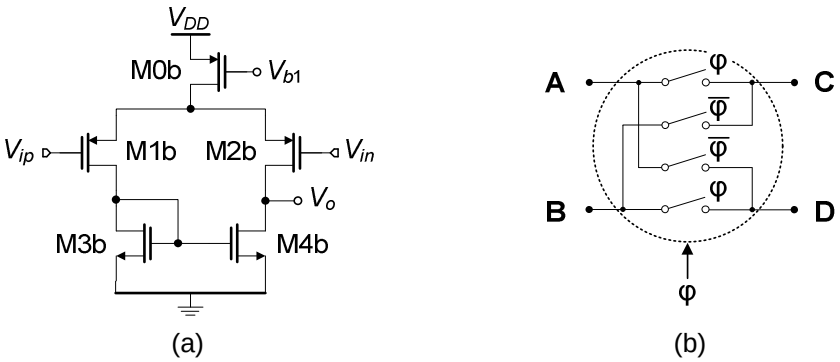


Fig. 2.2 – Schematic view of the instrumentation amplifier

Note that the output demodulator (indicated with S2 in Fig. 2.1) has been incorporated into the amplifier by means of chopper modulators S2a and S2b, shown in Fig 2.3(b). In this way, the output nodes are fed with the base-band

signals, reducing the problems introduced by the bandwidth limitation due to the output port time constant [41]. Even if S2b does not have effect on the signal path, it is necessary in order to modulate also the M5-M6 offset and low frequency noise. The V_{o1}, V_{o2} common mode is fixed by a conventional CMFB circuit that senses the voltage at node n_C and acts on V_{cmfb}. The OTAs are simple p-type differential amplifiers shown in Fig. 2.3(a). The chopper modulator S1 has been implemented by the means of complementary pass-gates, while S2a and S2b are implemented using n-type and p-type pass transistors, respectively.



(a) (b)

Fig. 2.3 – Schematic view of (a) differential amplifier with PMOS input devices; (b) chopper modulators (S1, S2a-b) scheme.

The input referred noise spectrum of the amplifier of Fig. 2.2 can be calculated as

$$S_{V,rti} = 2S_{V,OTA} + 4KTR_1(1+A_D^{-1}) + 2(R_1 g_{m3})^2 S_{V3} + 2(R_1 g_{m5})^2 S_{V5}. \quad (2.11)$$

where $S_{V,OTA}$ and S_{Vi} indicate the PSD (power spectral density) of the OTA input referred noise and device M*i* gate referred noise, respectively. The procedure to calculate the input referred noise will be briefly explicated in the following for the simpler case of the OTA.
Noise of the latter results in:

$$S_{V,OTA} = 2S_{V1b} + 2a^2 S_{V3b}. \quad (2.12)$$

where S_{V1b} and S_{V3b} are the gate referred noise PSDs of the OTA input and mirror devices, respectively, while *a* is a numerical factor given by

$$a = \frac{g_{m3b}}{g_{m1b}} \cong \frac{(V_{GS}-V_t)_{1b}}{(V_{GS}-V_t)_{3b}}. \quad (2.13)$$

This can be easily demonstrated by considering the contribution to the output node of all current noise generators (see Fig. 2.4) of each transistor of the differential amplifier of Fig. 2.3(a). The total output noise voltage V_{on} results

$$v_{on} = r_o(i_{1b} + i_{2b} + i_{3b} + i_{4b}), \quad (2.14)$$

where r_o is the output resistance of the amplifier. The referred to input is obtained by dividing the small signal gain of the stage ($g_{m1b}r_o$):

$$v_{n,OTA} = \frac{i_{1b} + i_{2b} + i_{3b} + i_{4b}}{g_{m1b}} \,. \tag{2.15}$$

As usually, all noise sources are considered as stochastically independent processes, so the expression of the PSD can be calculated simply accounting for each noise current in eq. (2.15), without correlated terms. Gate referred noise (v_n, S_{vn}) of each transistor is related to the noise current (i_n, S_{in}) by

$$v_n = g_m i_n \rightarrow S_{vn} = g_m^2 S_{in} \,. \tag{2.16}$$

Direct application of eq. (2.16) to eq. (2.15) gives eqs. (2.12, 2.13). As commented before, the same procedure can be applied to the scheme of Fig. 2.2 to obtain eq. (2.11). Choosing a, $R_1 g_{m3}$ and $R_1 g_{m5}$ sufficiently small it is possible to reduce the noise contributions of all devices except the input MOSFETs, as required by condition (i) of previous section. Clearly, to obtain this, the gate areas of M3b, M4b, M3-6 should be similar to that of the input devices to make their gate referred noise S_{Vi} comparable. For this reason, a specification of maximum area occupation for the whole cell can be easily converted into an area budget for the input devices.

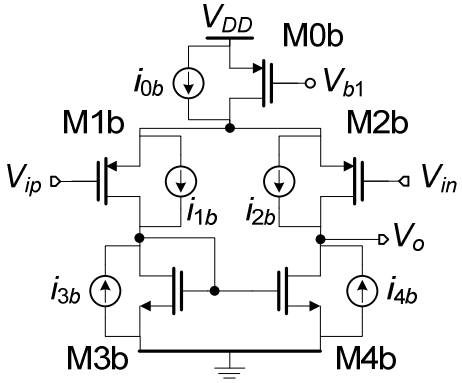


Fig. 2.4 – Differential amplifier with noise current generators explicitly indicated.

2.2.2. Design of the prototype

The prototype of the CHS amplifier has been designed using the CMOS subset of the BCD6s process (0.32 μm / 3.3 V) of STMicroelectronics. All simulations have been realized using ELDO™ spice on the CADENCE framework.

The actual design was arranged with a variable gain A_D whose maximum was fixed to 1000, while the source thermopiles resistance R_S was estimated to be 50 kΩ. We have chosen a target gain error of 0.5 and a maximum area for the input devices less then 20000 μm^2. Considering that we have $m = 4$ input transistors (two for each OTA), the individual input device gate area is WL = 5000 μm^2. With the topology of Figs. 2.2 and 2.3, the k_C factor, determined by AC simulations, is nearly 0.1.

First, we applied eq. (2.9) with k_F and C_{ox} taken from the process documentation, obtaining a best noise figure of 1.12, so we choose this F value as feasible specification. Applying Eq. (2.10), we found a chopper frequency f_{CH} = 10 kHz, which will be used as reference. The main component parameters in Figs. 2.2 and 2.3 are reported in table 2.I.

Device	***W/L* or *R***	**Device**	***W/L* or *R***
M1b-M2b	1970/2.3	M3-M4	549/36
M3b-M4b	293/9.1	M5-M6	99/9.1
R_1	400 Ω	R_2	417.5 kΩ

Table 2.I – Aspect ratios, expressed in µm, of the most significant transistors and resistance values.

The simulated RTI noise voltage spectral density of the amplifier (block AMP) is shown in Fig. 2.5 where the value at the chosen chopper frequency and the thermal/flicker corner frequency are shown. It is possible to observe that, in compliance with the hypothesis, noise flicker dominates at f_{CH}.

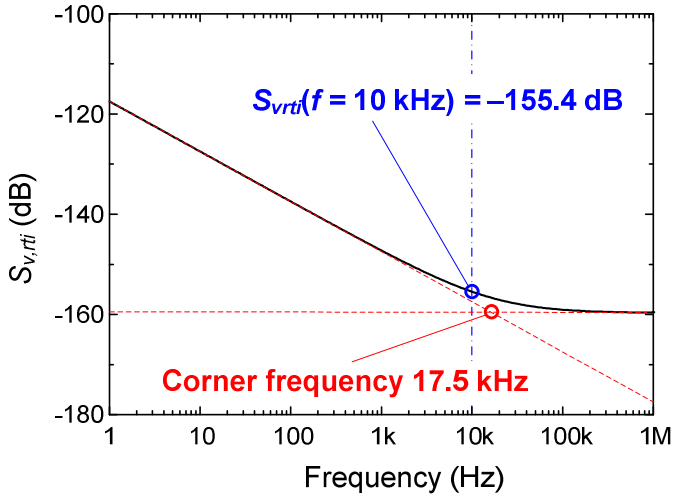


Fig. 2.5 – RTI noise spectrum of the amplifier AMP

The gain error has been estimated by means of transient simulations performed with different DC input voltages V_{dS}. The output DC value is calculated by extracting the mean value from the amplifier output (signal V_A in Fig. 2.1). The resulting transfer characteristic is shown in Fig. 2.6. The actual gain of the chopper amplifier was estimated from the slope of a linear fit calculated for V_{dS} < 200 µV. A gain error of 0.56 % has been estimated.

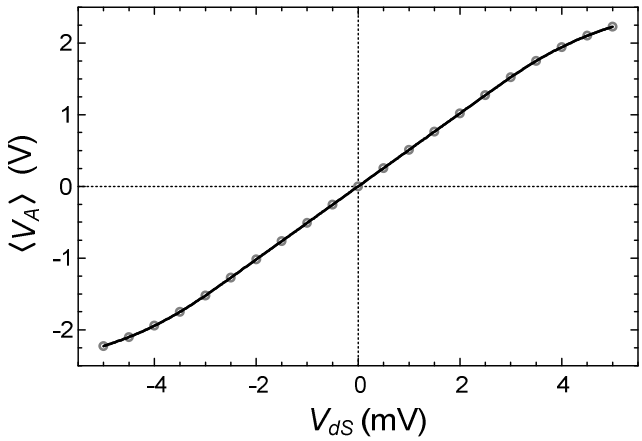


Fig. 2.6 – Simulated input/output characteristic of the amplifier.

The equivalent S_{Veq} has been estimated from the result of NOISETRAN simulations performed over a total time interval of 30 ms. Noise data have been extracted at the output of the low pass filter in Fig. 2.1. To this aim, the filter was implemented with ideal components (*R*, *L*, *C*) to obtain a second order Butterworth low pass transfer function with unity DC gain. The filter cut-off frequency was set to 200 Hz.

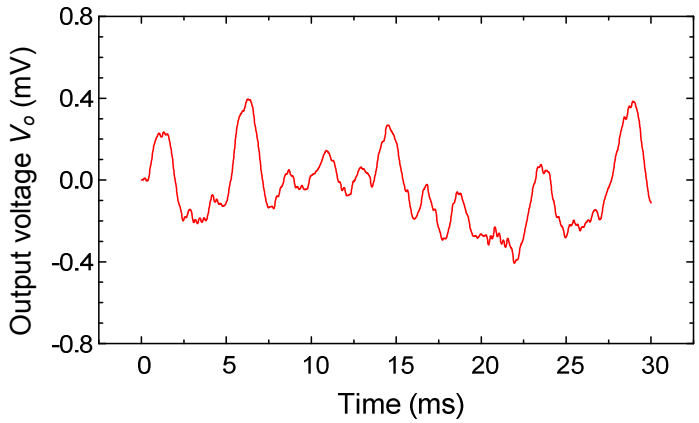


Fig. 2.7 – Output noise waveform with noiseless input source resistance R_S. Effective gain was set to 1000.

The spectral density was estimated by dividing the output RMS value by the filter bandwidth. The result is reported in table 2.II together with other main estimated performance data. The performances estimated simulations are close to the initial specifications. The slightly higher noise figure can be ascribed to having neglected all noise sources except the input MOSFETs.

	Design specification	*Simulated*
Power consumption @ 3.3 V		6 mW
Input device area	2500 μm^2	
Noise Figure	1.12	1.2
Gain error	0.5 %	0.56 %
Gain temperature sensitivity 0÷100 ℃		94 ppm/℃

Table 2.II – Design specifications and simulated performances.

2.3 Gm-C biquadratic cells for chopper amplifier band limiting

2.3.1. Gm-C biquad architecture for low pass filtering

In a typical CHS readout chain a low pass filter is needed as a cascaded stage in order to eliminate modulated offset and clock feed through residuals. The same filter can be effectively used to limit the channel bandwidth to the sensor signal bandwidth which is often of the order of only a few hundred hertz. Typical examples are bandwidth needed for signals produced, other than from flow-meters, also from pressure gauges, accelerometers. Chopper amplifiers are usually implemented in a fully differential (FD) architecture in order to facilitate the modulator/demodulator implementation. Thus the constraints for the filter design can be summarized as follows:

(i) fully differential input;
(ii) very low frequency singularities, and, being cascaded to a high gain amplifier;
(iii) wide input range.

Fig. 2.8(a) and Fig. 2.8(b) show two typical low-pass biquadratic cells, implemented in a fully differential (FD) and single-ended (SE) architecture, respectively. In both cases we have used capacitances with one terminal grounded in order to allow maximum process compatibility. The SE solution is simpler and uses half the number of transconductors and four times less of capacitor area. Furthermore, by using the circuit of Fig 2.8(a), a dedicated FD-to-SE conversion stage has to be added if a unipolar output is required, as generally occurs when the output signal has to be fed to off-chip analog circuitry. In terms of DC precision, it should be observed that the SE cell has a nominal unity gain whose precision relies on the high open loop gain of the transconductors. Conversely, the gain of the FD cell is equal to the ratio G_{m4}/G_{m1}, thus its precision is related to the matching of different transconductors, i.e. matching of a large number of devices (input transistors, current mirrors etc). For this reason the DC gain of the FD cell can be expected to be less accurate.
We had proposed the solutions depicted in Fig. 2.8(c, d) that partly maintain the compactness of the circuit in Fig. 2.8(b), while providing a differential input and intrinsically operating differential to single-ended conversion.

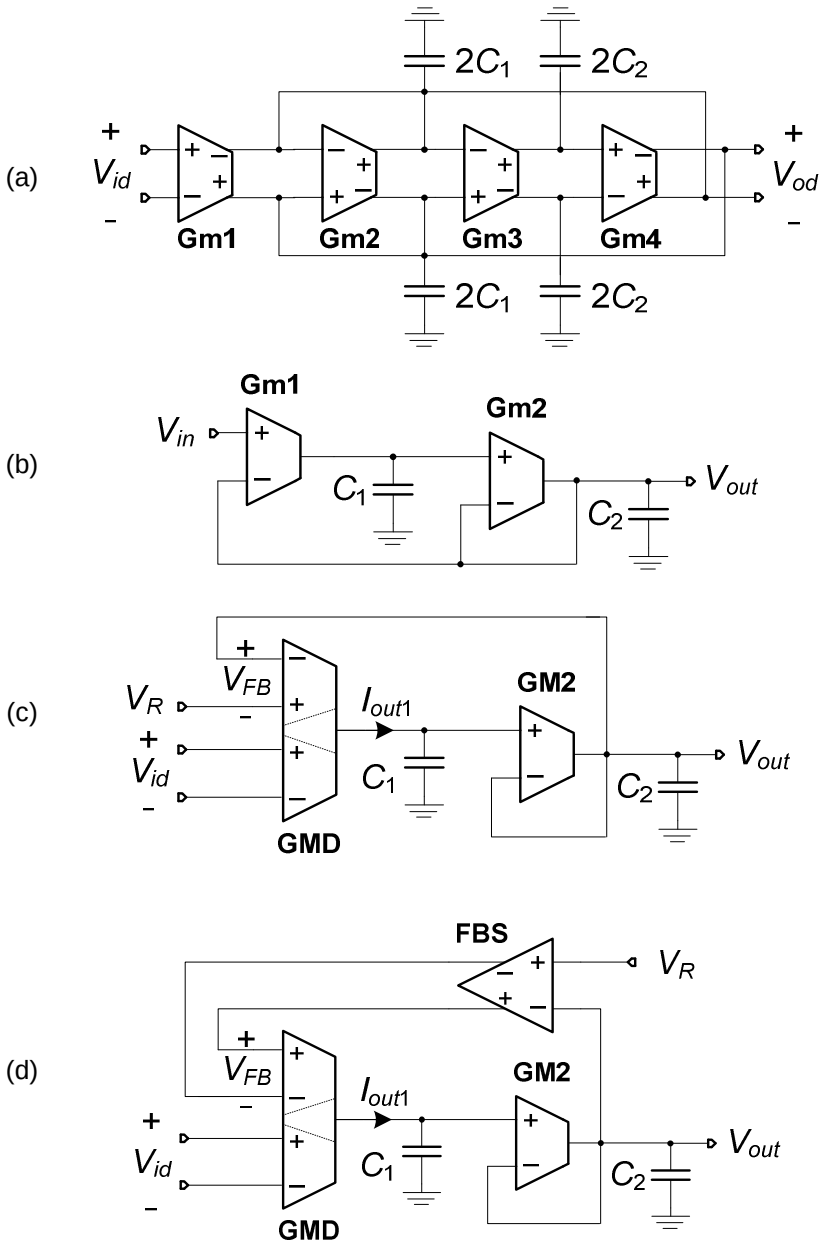


Fig 2.8 – Gm-C low-pass biquadratic cells: (a) fully differential, (b) single ended, (c) proposed architecture.

Let's focus on architecture of Fig. 2.8(d): transconductor GMD provides an output current equal to:

$$I_{out1} = G_{mA}V_{id} + G_{mB}V_{FB}\,. \tag{2.17}$$

where G_{mA}, G_{mB} are tranconductance parameters. The fully differential stage FBS provides a balanced signal V_{FB}, such as:

$$V_{FB} = A \cdot (V_R - V_{out}) \tag{2.18}$$

where A is the differential gain of the stage (block FBS), while V_R is a fixed reference voltage. It can be easily shown that the DC output voltage V_{out} for the circuit in Fig. 2.8(d), results:

$$V_{fb} = A \cdot (V_R - V_{out}) . \tag{2.19}$$

The above equation clearly states that V_R sets the rest value of V_{out} for V_{id} equal to zero. This improves the flexibility of the stage, since V_R can be properly chosen to match the input range of the following stage, e.g. an A/D converter.

$$V_{out} = (G_{mA} / AG_{mB}) \cdot V_{id} + V_R . \tag{2.20}$$

The above equation clearly states that V_R sets the rest value of V_{out} for V_{id} equal to zero. This improves the flexibility of the stage, since V_R can be properly chosen to match the input range of the following stage, e.g. an A/D converter.
The frequency response of the cell results:

$$H(j\omega) = \frac{V_{out}(j\omega)}{V_{id}(j\omega)} = \frac{G}{1 + j\omega/(Q\omega_0) - (\omega/\omega_0)^2} . \tag{2.21}$$

where ω_0, Q and G are the natural frequency, the quality factor, and the gain, respectively. The dependence of ω_0, Q and G on cell parameters is reported in table 2.III. It can be easily demonstrated that eqs. (2.17–2.21) hold also for architecture shown in Fig. 2.8(c) with A = 1.

ω_0	Q	G
$\sqrt{AG_{mB}G_{m2}/C_2C_1}$	$\sqrt{AG_{mB}C_2/G_{m2}C_1}$	G_{mA}/AG_{mB}

Table 2.III – Expressions of important parameters for filter in Fig. 2.8(c, d). For filter 2.8(c), A = 1.

It is important to observe that the DC gain depends on the FBS gain A and on a G_m ratio. The former can be clearly made as precise and stable as a resistance ratio. The G_m ratio refers to the two GMD input ports. As will be described later, block GMD is obtained from a conventional transconductor topology by simply duplicating the transconductor input section (see section 2.3.2.) or only input transistors (see section 2.3.3.). In this way, the precision of the G_m ratio depends only on the matching of few input transistors, which can be improved at layout level by adopting common centroid configurations.
In this thesis work has been implemented a first version based on resistive degenerated transconductors. Although the obtained performance of this first version was satisfactory, fulfilment of requirements led to quite cumbersome, i.e. silicon area consuming, cell. Experiences recollected from this first version served

as stimulus for the development of investigation of area optimized Gm/C filters for low frequency applications that will be discussed in section 2.3.3.

2.3.2. Linear transconductor for low frequency operation (version 1)

Transconductor topology, based source resistive degeneration of input transistors M1-M2 and M1'-M2', is shown in Fig. 2.9. Input p-MOS transistors M1-M2 and M1'-M2' are degenerated through resistors R_1. A feedback loop for each of the input transistor is provided in order to maintain constant the transistors V_{GS} in condition of applied differential voltage. The feedback loop for M1, formed by M3-M5-M9, can be briefly explicated: M9 senses the current mismatch between the (constant) current sunk by M13 and the current provided at the drain of M1. This error signal is fed back through the M3-M5 mirror, resulting in a constant polarization of M1 regardless of the applied gate voltage.

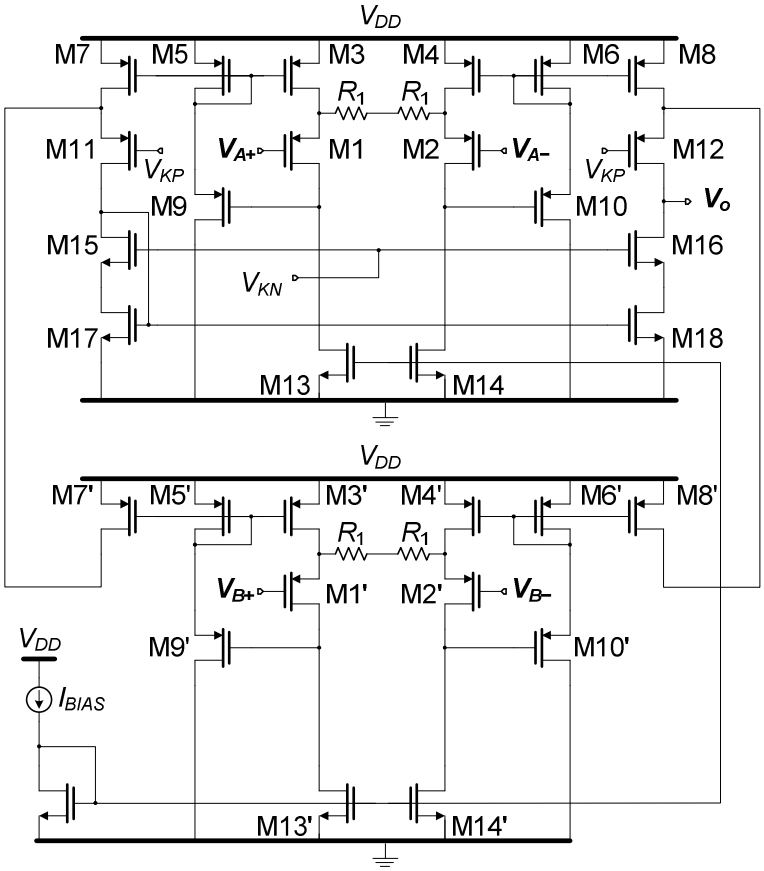


Fig 2.9 – Four input transconductor schematic diagram.

Any differential signal applied to the gates of M1-M2 (M1'-M2') is precisely transferred across the degeneration resistance $2R_1$, causing a current to flow which cannot be provided by M1 (M1') nor M2 (M2') but only by M3 (M3') and M4 (M4').

Finally that current is fed through M3-M7 (M3'-M7') and M4-M8 (M4'-M8') mirrors to the output section of the transcondutor. Thus the transconductance results:

$$G_m = \frac{1}{K_M R_1} \tag{2.22}$$

where K_M is the mirror factor of M3-M7 (M3'-M7') and M4-M8 (M4'-M8). It can be observed that the required G_m can be achieved by designing R_1 to a high value, limited only by practical considerations, and making current reduction factor K_M greater than unity.
The input range V_{DMAX} of the transconductor can be easily calculated considering that mirror transistors have to bear both the bias (I_{BIAS}) and the signal current that can be added or subtracted to the former depending on the sign of input voltage. Thus the following relation holds:

$$V_{DMAX} \leq 2R_1 I_{BIAS} \tag{2.23}$$

Noise of the filter can be calculated by summing up all noise contributions of the transistors, resulting in the following expression:

$$S_{v,rti} = \sum_{i=1,2,\ldots} a_i^2 R_1^2 \cdot g_{mi}^2 S_{vi} \tag{2.24}$$

where a_i is a coefficient that can be calculated depending on which point of the signal path the transistor i , having a transconductance g_{mi} and a PSD S_{vi}, injects its own noise. For example for transistor M7, $a_i = K_M$, and its spectral density noise ($\sqrt{S_{v7}}$) contributes weighted by a factor $K_M R_1 g_{m7}$. As usual g_{m7} can be expressed as a function of the bias current and the overdrive voltage of M7:

$$K_M R_1 \cdot g_{m7} = K_M R_1 \cdot \frac{2I_{BIAS}}{\left|V_{GS} - V_t\right|_7} = K_M \frac{V_{DMAX}}{\left|V_{GS} - V_t\right|_7} = \frac{1}{G_m R_1} \cdot \frac{V_{DMAX}}{\left|V_{GS} - V_t\right|_7} \tag{2.25}$$

where in the second equivalence we recognized the expression given in eq. (2.23), for $V_{DMAX} = 2R_1 I_{BIAS}$, while on the last equivalence we exploited eq. (2.22). The same expression holds also for M8, while for M17 (and M18) its overdrive voltage has to be considered instead of $|V_{GS} - V_t|_7$. It is interesting to note that all other transistors noises contributions are divided by K_M, making them not a concern when noise requirements are given. It has to be noted that filter noise requirements are relaxed respect to the chopper amplifier noise requirements as the sensor signal has been amplified.
A biquadratic low pass cell has been prototyped following the architecture shown in Fig. 2.8(c), under the following requirements: (i) input range of 1 V, (ii) cut off frequency of 1 kHz, (iii) RTI noise smaller than the chopper output noise. Design choices were: $R_1 = 40$ kΩ, $K_M = 40$, $I_{BIAS} = 10.84$ μA, $V_{ref} = 1.25$ V, $C_1 = 141$ pF, $C_2 = 70.5$ pF. Figure 2.10 shows the the DC characteristic V_{out}/V_{id} of the filter for $V_R = 1.25$ V. The deviation from the ideal characteristics ($V_{out} = V_{id} + V_R$) is less than 1% over a ±0.5 V input range. Figure 2.11 shows the frequency response of the filter.

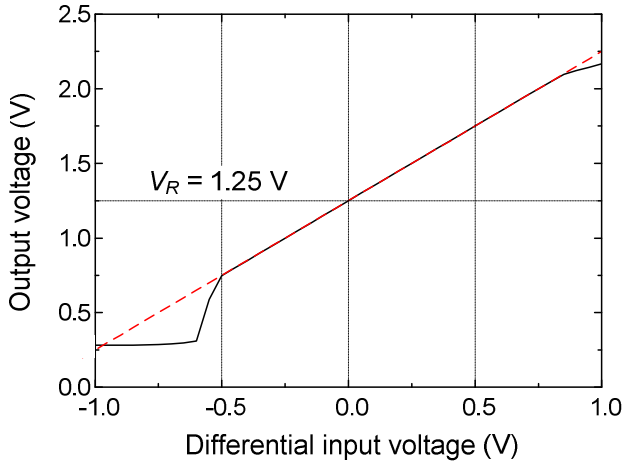


Fig. 2.10 – DC characteristics of the filter, with VR = 2.5. The symmetrical span where the non linearity error is below 1 % is also indicated.

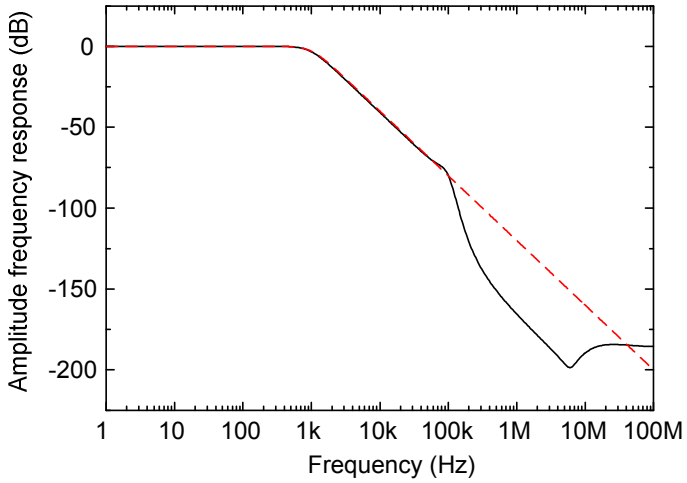


Fig. 2.11 – Amplitude frequency response of the filter. The ideal curve is shown in dashed lines.

2.3.3. Linear transconductor for low frequency operation (version 2)

Most of Gm-C filters use transconductors with input devices operating in saturation region; however these topologies impose very long input transistors for low frequency operation. This can be explained by considering the saturation region g_m expression in table 2.IV: typically, $V_{GS} - V_t$ of the input transistors is set to a large value to maximise the input range, so that the requirement of low G_m's can be satisfied only with extremely low β values, which in turn implies very long devices [42]. For example, for filter singularities around 100 Hz, and capacitance value of 100 pF, the transcondutor G_m should be less than 100 nano-siemens. Keeping

$V_{GS} - V_t$ large to maximize the input range may lead to L / W ratios up to one thousand, which, with the typical widths used in analog design, results in input device lengths of several hundred microns. As an alternative, output current downscaling by means of current mirrors can be effectively used to reduce the overall G_m [43]. Unfortunately this technique typically involves large occupied areas, since, in order to fulfil DC precision requirements (low offset and drift), the current division has to be obtained by placing a single transistor in the output section of the mirror and paralleling a large number of identical devices in the input section. Note that the output transistor should be considerably long to handle the small downscaled current, resulting in a very large input mirror section, where it is replicated a large number of times.
Triode operating devices represents an attractive alternative when a low G_m is required, allowing a relaxed trade-off between L and input range, since the G_m can be made low by reducing V_{DS} (see table 2.IV) with a positive effect also on the input range [44]. As will be discussed later, a V_{DS} lower bound exists, deriving from magnification of the input referred noise voltage.

Operation	g_m	***Input range***
Saturation	$\beta(V_{GS} - V_t)$	$\approx (V_{GS} - V_t)$
Triode	βV_{DS}	$V_{GS} - V_t - V_{DS}$

Table 2.IV – Transconductance and input range comparison. Where as usual $\beta = \mu C_{OX} W / L$, μ *is the carrier mobility,* C_{OX} *is the specific oxide capacitance.*

The topology of the four-inputs triode operating transconductor GMD is shown in Fig. 2.12. Two input pseudo differential p-MOS pairs, M1A-M2A and M1B-M2B, allow a very large input range. The drains of the input transistors are kept at a fixed voltage by means of a feedback loop provided by the block VDS-FB. The VDS-FB is simply derived by merging two different differential amplifiers that compares V_{DS} of M1A,B and M2A,B with V_{TUNE}. For a large loop gain of the V_{DS} feed back loop, we can approximate:

$$\left|V_{DS}\right|_{M1A,B} = \left|V_{DS}\right|_{M2A,B} = V_{DD} - V_{TUNE} \,. \tag{2.26}$$

so that, if β_A and β_B are related to transistors M1A-M2A and M1B-M2B, respectively, we have:

$$G_{mA} = \beta_A \left(V_{DD} - V_{TUNE}\right). \tag{2.27a}$$

$$G_{mB} = \beta_B \left(V_{DD} - V_{TUNE}\right). \tag{2.27b}$$

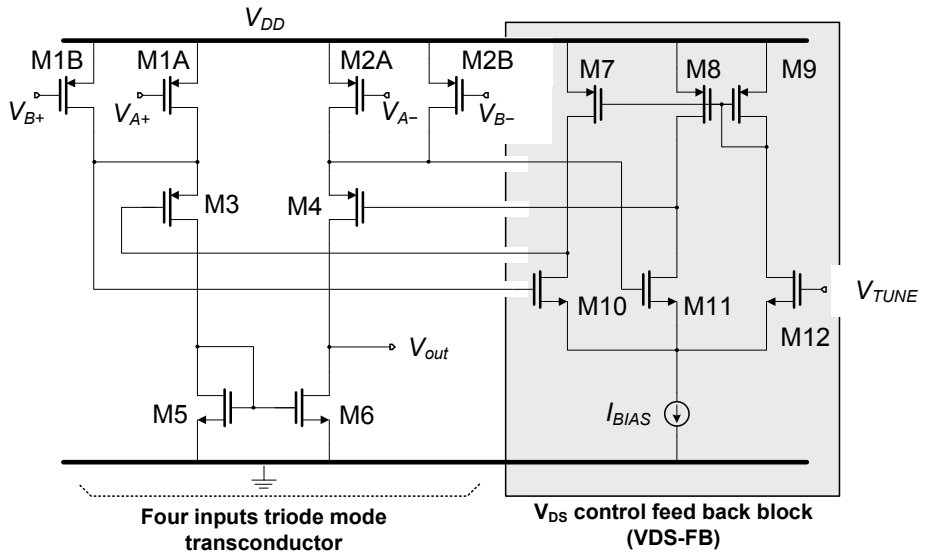


Fig 2.12 – Transconductor GMD schematic diagram.

The FBS stage is required to provide the input V_{fb} of GMD with a differential signal proportional to $V_{out} - V_R$ and a constant common mode voltage, which should match that of V_{id} port. Note that direct connection of V_R and V_{out} to the V_{fb} input would satisfy the differential voltage required but with a common mode voltage that depends on V_{out}. This, through second order effects such as the mobility degradation, produces a dependence of G_{mB} on V_{out}, eventually resulting in distortion, as confirmed by simulations.

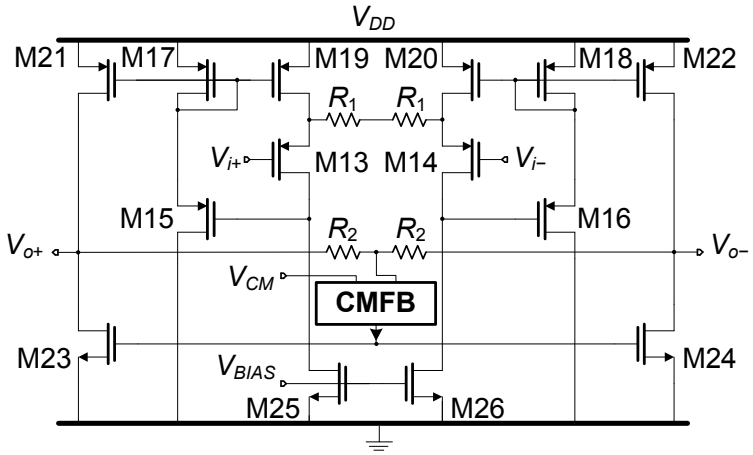


Fig. 2.13 – FBS schematic diagram.

In Fig. 2.13 the FBS topology is shown: it is a rather conventional differential amplifier based on a degenerated source input stage (M13-M14). The input differential voltage is precisely transferred through to the series $2R_1$ by stabilizing

M13 and M14 drain currents through the feedback loops M15-M17-M19 and M16-M18-M20. The current flowing through 2R1 is fed to the series $2R_2$, resulting in a differential gain $A = R_2/R_1$.
For correct dimensioning of the circuit, it is useful to study the relationship between the noise and the input range in the proposed transconductor architecture. For simplicity, we will consider a filter with $G_{mA} = G_{mB} = G_{m1}$, and $A = 1$. In the following discussion we will indicate quantities related to M1A,B and M2A,B with the subscript "1". Using reasonable approximations, it can be demonstrated that the input referred noise power spectral density of the filter is given by:

$$S_{vi} = 4S_{v1} + 2S_{v5} \cdot (g_{m5}/g_{m1})^2 + 2S_{VDS-FB} \cdot (g_{d1}/g_{m1})^2 + S_{vFBS} . \quad (2.28)$$

where the first three terms are the contribution of transconductor GMD, while the fourth term is the PSD of block FBS. S_{v1}, S_{v5} are the PSD of the M1, M5 gate referred noise, respectively. $S_{VDS\text{-}FB}$ is the noise PSD of the VDS-FB given by:

$$S_{VDS-FB} = 2S_{v10} + 2S_{v7} \cdot (g_{m7}/g_{m10})^2 . \quad (2.29)$$

Considering that g_{d1} in (2.28) is the triode region drain-source conductance, it can be demonstrated that (2.28) can be rewritten as:

$$S_{vi} = 4S_{v1} + 4S_{v5} \cdot (\beta_5/\beta_1) \cdot (2\gamma - 1) + 2S_{VDS-FB} \cdot (\gamma - 1)^2 + S_{vFBS} . \quad (2.30)$$

where

$$\gamma = \frac{g_{d1}}{g_{m1}} = \frac{|V_{GS1} - V_t|}{|V_{DS1}|} . \quad (2.31)$$

To find the relationship between noise and differential input range (V_{DMAX}), let us express the latter in terms of γ:

$$V_{DMAX} = 2 \cdot |V_{DS1}| \cdot (\gamma - 1) = 2 \cdot \frac{G_m}{\beta} \cdot (\gamma - 1) . \quad (2.32)$$

At this point, considering table II, we can easily find that, in the case of a saturated device transconductor, V_{DMAX} is simply equal to G_m/β. Comparison with (2.32) indicates that parameter γ can be effectively increased to boost the input range of triode region transconductors, reducing the need of very low β for the input devices. On the other hand, (2.30) shows that γ cannot be increased freely since it acts also as a multiplying factor for a few important noise contributions.

2.3.4. Simulated performances of the redesigned Gm-C filter

A prototype of circuit in Fig. 2.8(d) has been implemented, where $C_1 = C_2 = 50$ pF. Both GMD and GM2 are implemented using the circuit of Fig. 2.9. Transconductor GM2 has been obtained from the same topology as GMD, connecting the two input ports in parallel. Transistors M1A,B and M2A,B of both transcondutors have been sized with $W = 1$ μm, $L = 150$ μm, resulting in $G_{mA} = G_{mB}$ and $G_{m2} = 2 \cdot G_{mA}$. We set $A = 1$, by making resistors $R_1 = R_2 = 50$ kΩ. Transistors have been heuristically sized by means of simulations in order to achieve a dynamic range (DR) value of −80 dB. The DR has been calculated as the ratio of the input range (1 % linearity error) to the RMS noise, estimated by integrating the simulated output noise

spectral density over a 0.01-10^5 Hz bandwidth. The total area, estimated by a preliminary layout, was about 360 × 360 μm^2.
Figure 2.14 shows the DC characteristic V_{out}/V_{id} of the filter for V_R = 1.25 V. The deviation from the ideal characteristics ($V_{out} = V_{id} + V_R$) is less than 1% over a ±0.7 V input range. The characteristic obtained in the same conditions but removing the FBS block and connecting V_{out} and V_R directly to the V_{FB} port of GMD is also shown (see Fig. 2.8(c)). The noticeable non linearity increase demonstrates the necessity of FBS. From preliminary Monte Carlo simulations the maximum input offset voltage and gain spread turned out to be 15 mV and 7 %, respectively.

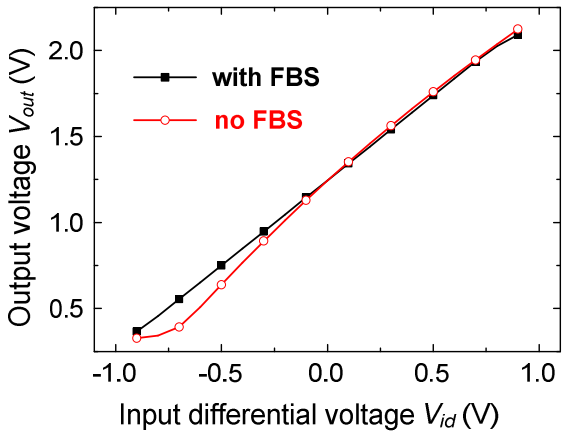


Fig. 2.14 – Simulated DC transfer characteristics with (solid line) and without (dashed line) FBS block.

The amplitude frequency responses for three values of V_{DS1} obtained by means of AC simulations are shown in Fig. 2.15. For each curve, the –3 dB frequency and the estimated DR is indicated.

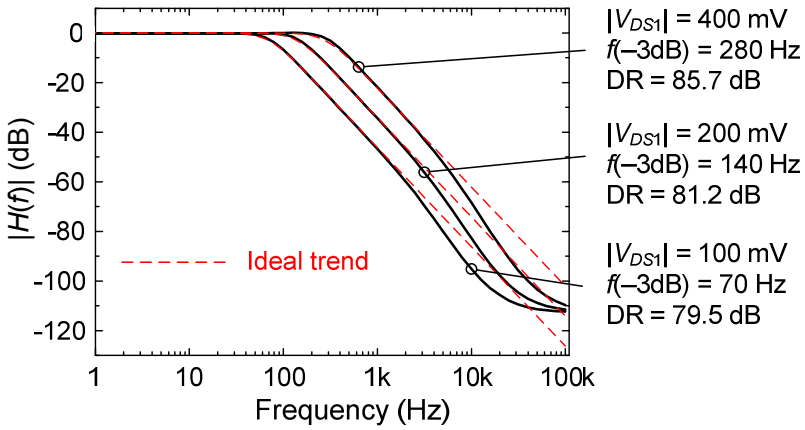


Fig. 2.15 – Amplitude frequency response for three values of the upper band limit f(–3 dB). Respective ideal curves are shown in dashed lines.

The filter behaviour as a cascade stage after a chopper amplifier has been studied by means of a series of transient simulations. We fed the input port with a fixed DC value V_{id} superimposed to a square voltage wave having a peak-to-peak amplitude V_{PP} and a fundamental frequency of 10 kHz, representing the in-band signal and the residual chopped offset to be rejected, respectively. Due to unavoidable non linearity of the filter the output DC value may result affected by the super position of the two input signals. This test can be considered as a two tones test [45], where one of the tones is applied at frequency close to zero. The resulting error on the output DC voltage can be calculated by

$$Error = \left| \frac{(V_{out} - V_R) - V_{id}}{V_{id}} \right|. \tag{2.33}$$

Fig. 2.16 shows the resulting mean value of V_{out} as a function of V_{PP} for two different values of V_{id} and $|V_{DS1}|$ = 400 mV.

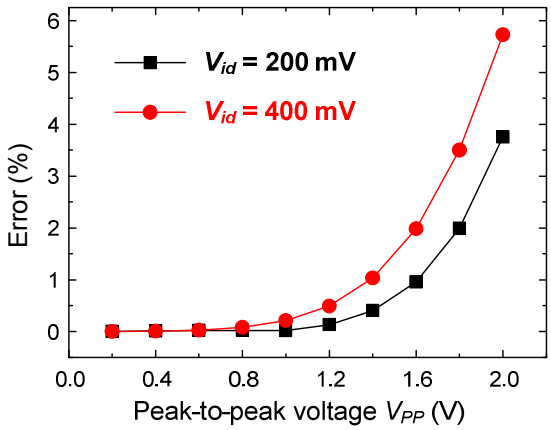


Fig. 2.16 – Error on DC output value due to superimposed square waveform of peak-to-peak amplitude V_{PP} and fundamental frequency of 10 kHz.

2.4 Sensor driving circuits and pressure effects compensation loop

In section 1.3.6 we discussed the pressure effects on sensor response of the integrated flow-meters. Sensitivity to pressure variations can be attributed to the reduction of the air gaps between the sensor elements down to micrometric distances. It should be observed that a mass flow sensor based on thermal principles is practically insensitive to pressure as long as the fluid can be considered as a continuum [46]. This condition begins to be violated when the gas pressure gets low enough that the molecule mean free path becomes comparable with the sensor dimensions. Clearly, the smaller the sensor, the higher the

pressure at which the effect starts being noticeable. For sensors of air gap in the order of 50 µm, this effect is evident yet at a quarter of atmospheric pressure.
We found that both the common mode signal (independent of the flow rate) and the differential signal (dependent on flow rate) produced by the thermopiles behave like a Pirani vacuum gauge, but with different transition pressures. So the common mode signal can be exploited to read the pressure and drive the heater power in order to compensate the pressure dependent signal drop on the differential mode signal. The system that performs this task will be referred as common mode differential chain. It should be noted that the thermopiles signal is read and fed back the heater realizing *de facto* a closed loop operating through both the electrical and thermal domain.
On the other hand, we saw that sensing structures are implemented with two heaters purposed to cancel the structural offset by a applying a proper power unbalance between the two heating elements.
So the task of the driving circuit together with the common mode readout chain is to feed the heaters with an overall power dependent on pressure while providing a programmable unbalance. To better explain the closed loop operation, let us assume that both heaters are fed with a power $W/2$, with an overall power of W; the following relationships of the sensor differential and common mode voltage can be written:

$$\begin{cases} V_{dS}(Q,P) = W \cdot f_{dS}(Q,P) \\ V_{cmS}(P) = W \cdot f_{cmS}(P) \end{cases} . \tag{2.34}$$

where the linear dependence on W derives from assuming a condition of forced convection. Independent variables Q and P indicate the flow rate and the operative pressure, respectively. Functions f_{dS} ad f_{cmS} can be approximated by the following empirical expressions:

$$\begin{cases} f_{dS}(Q,P) = f_{dS}(Q,P_{\infty}) \cdot \dfrac{P}{P+P_D} \\ f_{cmS}(P) = f_{cmS}(P_{\infty}) \cdot \dfrac{P}{P+P_C} \end{cases} . \tag{2.35}$$

where P_{∞}, P_D, P_C indicate a pressure high enough to calculate the asymptotical value of V_{dS} and V_{cmS}, the transition pressure for the differential signal, the transition pressure for the common mode signal, respectively. We remind that both P_D and P_C are called transition pressures and depend on the gas type and the sensor size, in particular the smaller the sensor dimensions, the higher the transition pressure.
In order to understand the compensation method described in the following discussion, it is also important to observe that for various gases $P_C > P_D$. This means that, for $P < P_D$, the relative sensitivity to pressure is larger for V_{cmS} than for V_{dS}. In Fig. 2.17 the complete block level scheme of the common mode chain loop is shown. The common mode signal is calculated by amplifying the output voltages of the two thermopiles separately by means of the amplifiers (with amplification $A_1/2$) and then summing up the two signals. Referring to Fig. 2.17 we obtain a signal

$$V_C = \frac{A_1}{2} \cdot (V_{T2} - V_{CS}) + \frac{A_1}{2} \cdot (V_{T1} - V_{CS}) = A_1 \cdot V_{cmS}. \quad (2.36)$$

The signal V_C is then subtracted to the reference V_{CREF}. The resulting amplified signal is fed to a driver that operates the voltage to current conversion, properly unbalancing the two currents I_{H1} and I_{H2} feeding the sensor heaters. The current unbalance can be set by the digital word DW.

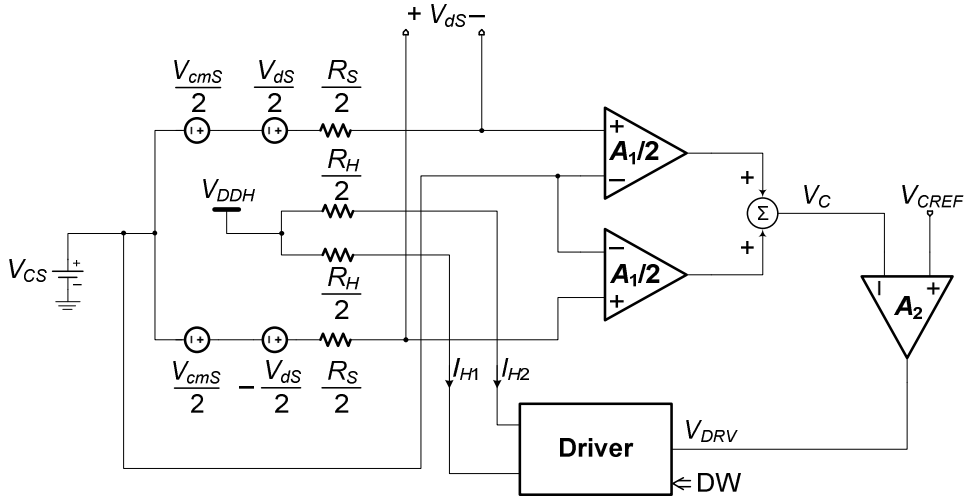


Fig. 2.17 – Schematic diagram of the common mode feed-back chain. Each thermopile voltage has been expressed with the common and the differential mode components. R_S and R_H are the thermopile and the heater resistance, respectively.

Given G the transconductance parameter of the driver, the system equations, in case $I_{H1} = I_{H2} = I_H$, are:

$$V_C(P) = A_1 \cdot V_{cmS}(P) = A_1 \cdot W \cdot f_{cmS}(P). \quad (2.37)$$

$$V_{DRV}(P) = A_2 \cdot (V_{CREF} - V_C(P)). \quad (2.38)$$

$$I_H(P) = G \cdot V_{DRV}(P). \quad (2.39)$$

$$W(P) = 2(R_H / 2) \cdot I_H^2(P). \quad (2.40)$$

As we have already pointed out, V_{cmS} has a relative variation larger than that of V_{dS}. This clearly means that, if we completely cancel the V_{cmS} variations using a loop gain much higher than one, we overcompensate V_{dS}. The idea is then to use a moderate loop gain that under-compensates V_{cmS} but stabilizes V_{dS}. The optimum value for the loop gain has been determined with a first order analysis solution of eqns. (2.34-2.40).

Considering an operating point at a given flow rate Q_0 and pressure P_0, we perform a small signal analysis to calculate the effect of a pressure variation that we will indicate with p. Similarly, we will use lowercase quantities to indicate variations

around the operating point of all the quantities of interest. We find the following linearized expressions:

$$v_{dS}(p,w) = W_0 \cdot \left.\frac{\partial f_{sD}}{\partial p}\right|_{Q_0,P_0} \cdot p + f_{sD}(Q_0,P_0) \cdot w \tag{2.41}$$

$$v_C(p,w) = A_1 \cdot \left(W_0 \cdot \left.\frac{\partial f_{cmS}}{\partial p}\right|_{P_0} \cdot p + f_{cmS}(P_0) \cdot w \right) \tag{2.42}$$

$$v_{DRV}(p,w) = -A_2 \cdot v_C(p,w) \tag{2.43}$$

$$i_H(p,w) = G \cdot v_C(p,w) \tag{2.44}$$

$$w = 2R_H I_{H0} \cdot i_H(p,w) \tag{2.45}$$

Now, recollecting eqs. (2.42-2.45) it possible to express *w* as a function of the pressure *p*:

$$w = -p \cdot W_0 \cdot \frac{1}{f_{cmS}(P_0)} \cdot \left.\frac{\partial f_{cmS}}{\partial p}\right|_{P_0} \cdot \frac{1}{1+(\beta A)^{-1}} \tag{2.46}$$

where the close loop gain β*A* is

$$\beta A = 2R_H G \cdot A_1 A_2 \cdot I_{H0} f_{cmS}(P_0) \tag{2.47}$$

Substituting *w* in eq. (2.41) we finally find:

$$v_{dS} = p \cdot W_0 \cdot f_{dS}(Q_0,P_0) \cdot \left[\frac{1}{f_{dS}(Q_0,P_0)} \cdot \left.\frac{\partial f_{dS}}{\partial p}\right|_{Q_0,P_0} - \frac{1}{f_{cmS}(P_0)} \cdot \left.\frac{\partial f_{cmS}}{\partial p}\right|_{P_0} \cdot \frac{1}{1+(\beta A)^{-1}} \right] \tag{2.48}$$

In order to cancel the effects of pressure it is necessary that the term in square brackets is zero. Finally using the expressions of eq. (2.35) for f_{dS} and f_{cmS} with the approximation of $P >> P_D, P_C$, it is possible to obtain the optimum loop gain value:

$$\beta A = \left(\frac{P_C}{P_D} - 1 \right)^{-1} \tag{2.49}$$

Equation (2.49) represents the optimal value to be given at the close loop gain in order to compensate for pressure lost of sensitivity on sensor signal. In order to check the validity of the discussed analysis, the system shown in Fig. 2.17 has been implemented by the means of a VHDL-AMS model [47]. Using this model, accurate simulations have been done in order to check the correctness of the optimum value of β*A* found with eq. (2.49).
It is worth noting that the optimum β*A* may vary for each gas under test and type of sensor used; in facts, P_C and P_D, as discussed in chapter 1, depend in a complex fashion on gas type and structure geometries. Experimental tests showed that for a BCD3s sensor structure immersed in a nitrogen flow, the optimum value of β*A* = 2

[25]. BCD6 and BCD6s structures have very similar geometries of that of BCD3s structures, thus similar optimum values of β*A* are expected.
The system shown in Fig. 2.17 can be optimized for different specifications (R_H, W, f_{cmS}) depending on the actual sensor used. We chose to make the system flexible and capable to meet a considerable range of sensor characteristics and at the same time we wanted to prevent from large spread of parameters values, in order to tune them finely but without using an excessive number of configuration bits. To due so, a rational design methodology for setting the various system parameters (A_1, A_2, G, V_{CREF}) has to be coped. Let us consider the scheme shown in Fig. 2.18. We will demonstrate that the latter is equivalent to the scheme in Fig. 2.17. From eqs. (2.39-2.40):

$$W = R_H \cdot (G \cdot V_{DRV})^2 \tag{2.50}$$

Substituted in eq. (2.37) we find

$$V_C = R_H \cdot (G \cdot V_{DRV})^2 \cdot A_1 \cdot f_{cmS} \tag{2.51}$$

We can lump together some terms in eq. (2.51) in a fictitious voltage quantity V_{S0}:

$$V_{S0} = \frac{1}{R_H G^2 A_1 f_{cmS}} \tag{2.52}$$

so that eq. (2.52) can be expressed in the compact form

$$V_C = \frac{(V_{DRV})^2}{V_{S0}} \tag{2.53}$$

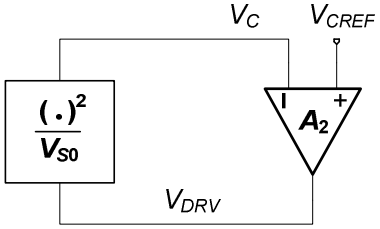


Fig. 2.18 – Reduced schematic diagram of the common mode feed-back chain.

It is useful to express the loop gain (see eq. (2.47)) as a function of the new parameter V_{S0}:

$$\beta A = 2A_2 \frac{I_H}{G} \cdot \frac{1}{V_{S0}} = 2A_2 \frac{V_{DRV}}{V_{S0}} \tag{2.54}$$

As the power fed to heaters cannot increase freely, we can introduce a parameter ψ counting for the ratio of the actual heaters power to the maximum power disposable:

$$\psi = \frac{W}{W_{MAX}} \tag{2.55}$$

ψ is a key parameter of the system that have to can be set in normal operative condition at high pressure (atmospheric pressure):,its reciprocal value determines

how much we can increase the actual power W to compensate for pressure drop of sensitivity. For example for a given W, optimal for the differential mode signal extraction, the smaller ψ the greater has to be W_{MAX}, resulting also in a greater pressure range where the loop compensation is effective. Using eqs. (2.51-2.52), V_{DRVMAX} and V_{CMAX} can be easily found as a function of W_{MAX}, which is very useful from a practical point of view. Besides, using eq. (2.55) we can express V_C and V_{DRV} with respect to their respective maximum value:

$$V_C = \psi \cdot V_{CMAX} \tag{2.56}$$

$$V_{DRV} = \psi^{1/2} \cdot V_{DRVMAX} \tag{2.57}$$

We point out that the introduced parameter V_{S0} carries information about the sensor characteristics (heater resistance R_H, and pressure sensitivity function f_{cmS}), but acting on gain A_1 and the transconductance G we can fix V_{S0} at a constant value for all the desired sensors configurations. Now the values of A_2 and V_{CREF} can be chosen from the ψ (see eq. (2.55)) and βA (see eq. (2.49)) specifications. From simple algebra applied to eqs. (2.54) and (2.57) we find:

$$A_2 = \frac{\beta A}{2} \cdot \frac{V_{S0}}{\psi^{1/2} \cdot V_{DRVMAX}} \tag{2.58}$$

that substituted in eq. (2.38) gives

$$V_{CREF} = \left(\frac{2}{\beta A} + 1 \right) \cdot \psi V_{CMAX} \tag{2.59}$$

Above equations are useful to correctly design the system parameters with respect to the reference sensors considered in this work. Sensors data (experimental or expected) are reported in table 2.V, together with working conditions.

Sensor	**Thermopile type (number of thermocouples)**	**R_H (kΩ)**	**f_{cmS} at high pressure (V/W)**	**f_{dS} at high pressure (V/W)**	**W_{MAX} (mW)**
BCD3s (2 heaters)	poly-n/Al (20)	4.8	0.387	0.025-0.033	6
BCD6 (1 heater)	poly-p/Al (17)	1	0.56	0.10	6
	poly-n/poly-p (7)	1	0.98	0.16	6
BCD6s (2 heaters)	poly-n/poly-p (10)	2	0.6	0.3	2

Table 2.V – Reference sensors data. The maximum power W_{MAX} is expressed for each heater in case of double heater structure. Data regarding BCD6s structures are expected.

From eq. (2.53) and table 2.V we can see the required range of variability for A_1 and G in order to maintain V_{S0} to a constant value. Due to the high value of R_H for BCD3s structures, we can set a special bit b_{CR} that halves the current fed to heaters. This bit is independent to the rest of the bits forming DW and it has the only purpose to identify the correct current range, which should be high for BCD6

structures and low for all the others (including BCD6s sensors). Thus the transconductance of the current driver can be expressed as

$$G = G_0 / 2^{b_{CR}} \tag{2.60}$$

The voltage V_{DRVMAX} has to be chosen inside the input range of the current driver. In order relax linearity constraints on the latter we fix V_{DRVMAX} of below 2 volt for all the considered configurations. Considering G_0 of about 1.6 mS, we obtain data shown in table 2.VI where: (i) we chose to make A_1 coarsely variable between three values (50, 100, 150), (ii) V_{S0} is calculated from eqs. (2.51, 2.59), (iii) A_2 and V_{CREF} are calculated from eqs. (2.57, 2.58) respectively, considering ψ = 2/3 and β*A* equal to 2 (optimal experimental value for nitrogen gas).

Sensor	b_{CR}	A_1	V_{S0} (V)	V_{DRVMAX} (V)	A_2	V_{CREF} (V)
BCD3s	1	100	7.7	1.30	7.40	0.290
BCD6 p/Al	0	100	6.9	1.52	5.67	0.440
BCD6 n/p	0	50	7.8	1.52	6.41	0.386
BCD6s	1	150	7.9	1.46	6.76	0.356

Table 2.VI – Values of design parameters for the common mode amplification chain. A_2 and V_{CREF} have been calculated considering ψ = 2/3 and βA = 2.

2.4.1. Implementation of the common mode amplification chain

The practical implementation of the common mode amplification chain is shown in Fig. 2.19. Input signals are: the two distinct thermopile voltages V_{T1}, V_{T2}, and the voltage V_{CS} applied to the common node of the thermopiles; the output is the voltage V_{DRV} which feed the input of the current driver described in the next section. Gain A_1 of Fig. 2.17 is provided by a cascade of the instrumentation amplifier A_0 and a switched capacitor amplifier providing a further gain (C_{1A}/C_{1B}). Each amplified thermopile voltage is available to pad through a simple sample and hold stage. Gain A_2, signal summation and comparison with V_{CREF} (see Fig. 2.17 and 2.18) is provided by a cascaded switched capacitors stage. Timing diagram of clock phases θ_1, θ_2, θ_3 is also shown in the inset of Fig. 2.19.
It can be easily shown that:

$$A_1 = 2A_0 \cdot \frac{C_{1A}}{C_{1B}} \tag{2.61}$$

$$A_2 = \frac{C_{2A}}{C_{2B}} \tag{2.62}$$

and that V_{DRV} and the pad voltages are:

$$V_{DRV} = A_2\left(\frac{C_{REF}}{C_{2A}}V_{DD} - A_1\frac{V_{T1}+V_{T2}}{2}\right) + V_{REF2} \tag{2.63}$$

$$V_{PAD1(2)} = \frac{A_1}{2}V_{T1(2)} + V_{REF1} \tag{2.64}$$

Note that V_{REF2} is introduces to match with the minimum input voltage of the current driver. Comparison of eq. (2.63) with eq. (2.38) gives:

$$V_C = A_0 \frac{C_{1A}}{C_{2A}}\left(V_{T1} + V_{T2}\right) = A_1 \frac{V_{T1} + V_{T2}}{2} = A_1 V_{cmS} \tag{2.65}$$

$$V_{CREF} = \frac{C_{REF}}{C_{2B}} V_{DD} = A_2 \frac{C_{REF}}{C_{2A}} V_{DD} \tag{2.66}$$

Offset cancellation is obtained by means of the correlated double sampling technique (CDS). Note that the sign of gain A_1 can be reversed by simply swapping the θ_1, θ_2 phases at the input switches, thus uncertain on V_{T1}, V_{T2} sign is allowed to be solved.

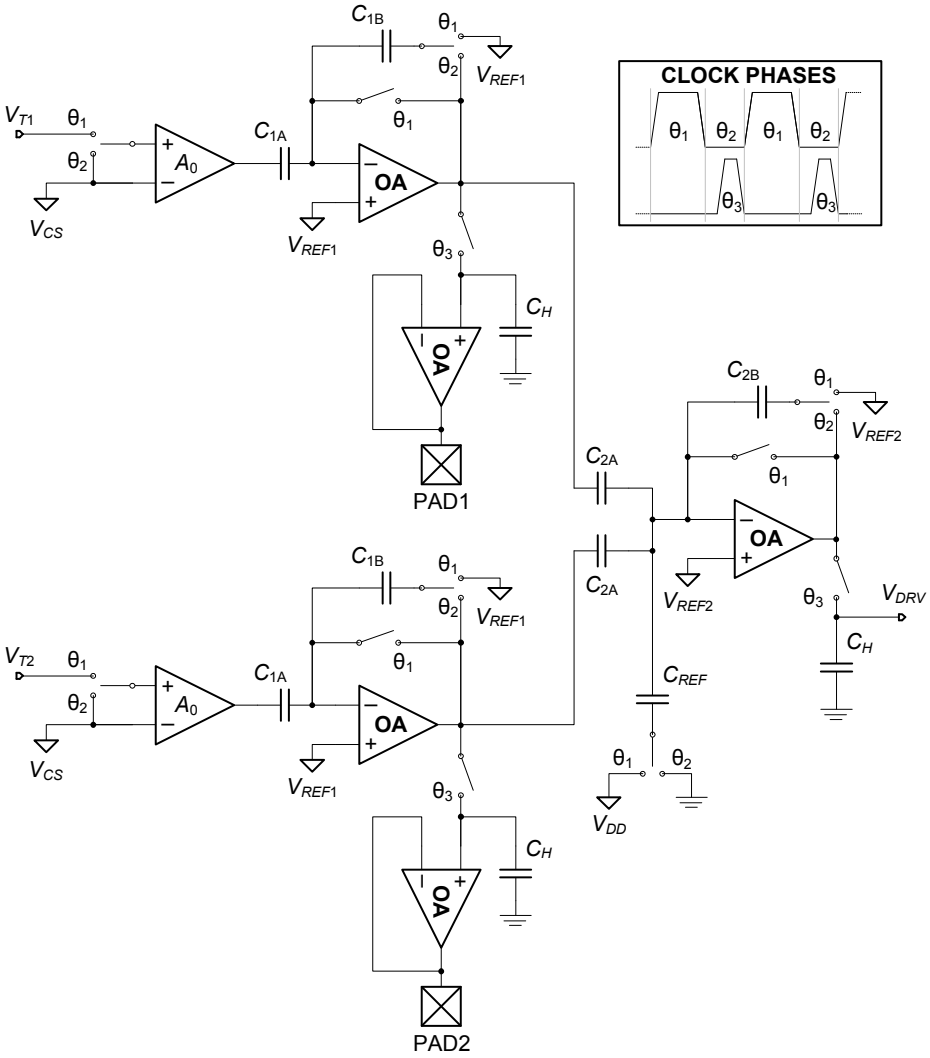


Fig. 2.19 – Schematic diagram of the common mode feed back amplification chain.

The instrumentation amplifier A_0 allows a first amplification of the signal making charge injections effects negligible as they occurs only in the successive stages.

Schematic diagram of the circuit is shown in Fig. 2.20. Principle of operation is very similar to that of circuits described in sections 2.3.2 – 2.3.3. It is easy to find that $A_0 = R_2/R_1$. The operational amplifiers (OAs) are based on a well known rail-to-rail input/class AB output topology shown in Fig. 2.21.

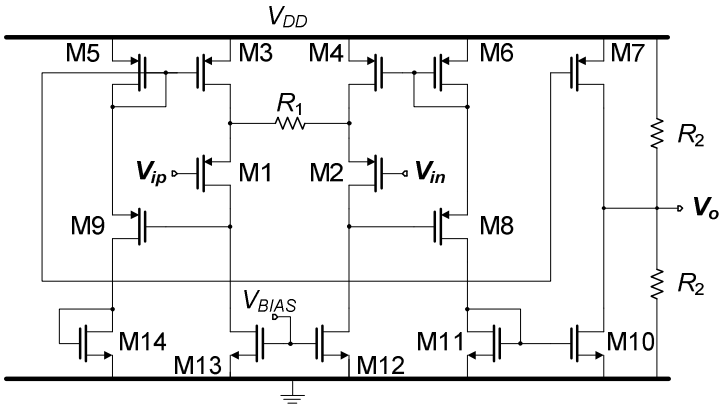


Fig. 2.20 – Instrumentation amplifier (A_0) schematic diagram.

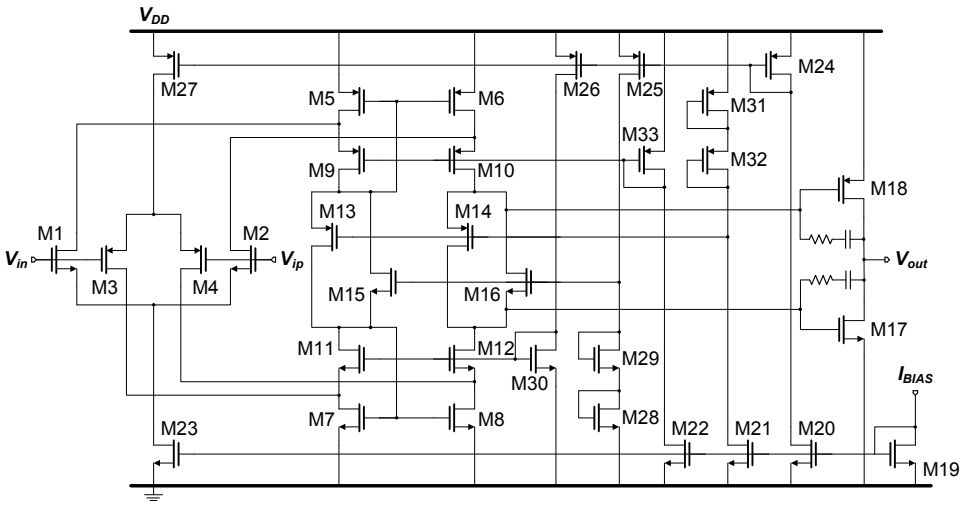


Fig. 2.21 – Operational amplifier (OA) schematic diagram.

In order to allow programmability of the various system parameters (A_1, A_2, V_{CREF}), capacitance C_{1A}, C_{2B} and C_{REF} in scheme of Fig. 2.19 have been made variable by simply parallelizing capacitors through a bit controlled pass gates. Table 2.VII resumes all design assumptions and shows the resulting expressions for A_1, A_2, V_{CREF}.

Capacitors expressions	Elementary capacitance values (type)
$C_{1A} = C_A + \sum_{i=0}^{1} b_{A,i} \cdot 2^i C_A \;;\; C_{1B} = 2C_A$ $C_{2A} = 6C_A \;;\; C_{2B} = C_A + \sum_{i=0}^{4} b_{B,i} \cdot 2^i C_M$ $C_{REF} = C_R + \sum_{i=0}^{1} b_{R,i} \cdot 2^i C_R$	C_A = 1 pF (diffused bottom plate capacitor) C_M = 0.15 pF (metal-oxide-metal capacitor) C_R = 0.468 pF (diffused bottom plate capacitor)
System parameters expressions	
$A_1 = \frac{A_0}{2} \cdot \left(1 + \sum_{i=0}^{1} b_{A,i} \cdot 2^i\right)$ $A_2 = 6 \cdot \left(1 + 0.15 \cdot \sum_{i=0}^{4} b_{B,i} \cdot 2^i\right)^{-1}$ $V_{CREF} = 0.468 \cdot V_{DD} \cdot \left(1 + \sum_{i=0}^{1} b_{R,i} \cdot 2^i\right) \cdot \left(1 + 0.15 \cdot \sum_{i=0}^{4} b_{B,i} \cdot 2^i\right)^{-1}$	

Table 2.VII – Parameters expressions. Note A_1 is set by $\{b_{A0}\ b_{A1}\}$, while A_2 is set by $\{b_{B0} \ldots b_{B4}\}$. The latter together with $\{b_{R0}\ b_{R1}\}$ affects V_{CREF}.

Figure 2.22 shows the characteristics at various temperatures of the instrumentation amplifier. Gain was set to the precise value of 100 through resistor ratio, and it is largely insensitive to temperature within the ±10 mV input range. Figure 2.23 shows the transient response of the operational amplifier configured as a unity gain buffer on a 20 pF capacitive load. The input signal is a 2 V peak to peak square voltage with period of 10 µs. The opamp has been fed with an input bias current of 10 µA for this test.

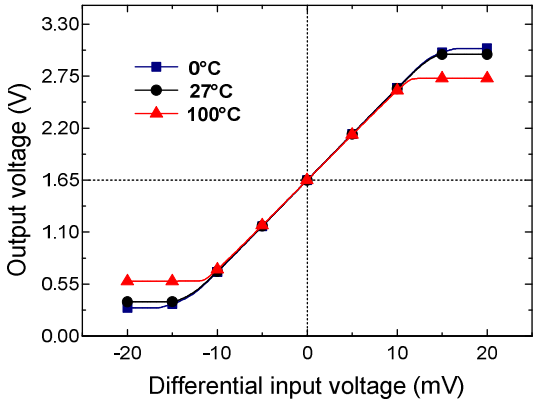


Fig. 2.22 – Instrumentation amplifier characteristics, A_0 = 100.

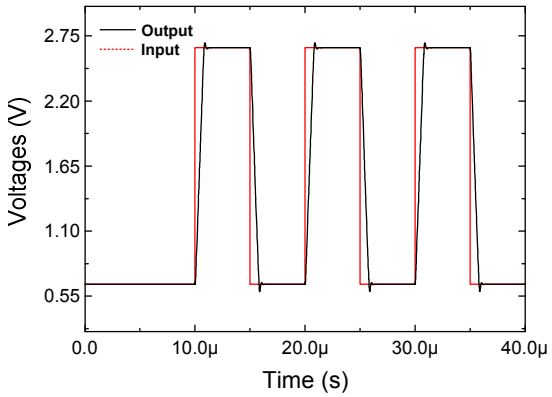


Fig. 2.23 – Operational amplifier transient response when configured as unity gain buffer on a 20 pF load stimulated by a 2 $V_{pk\text{-}pk}$/100 kHz square wave input signal.

2.4.2. Digitally controlled current driver

The loop for the common mode control of Fig. 2.17 is closed through a last block called current driver. This block has to provide two currents I_{H1}, I_{H2} that have to be fed to the heaters of the sensors. As we have already discussed, it has to provide voltage to current conversion and at the same time control by a digital word DW the unbalance between the two output currents. The schematic diagram of the circuit is shown in Fig. 2.24. It is based on a simple differential amplifier (M1-M7) in a unity gain configuration. It can be easily shown that resistors R_{D1} and R_{D2} determine both the transconductance parameter G_{0LP} and the driver minimum voltage V_{DRVMIN}, i.e. the voltage below which both I_{H1} and I_{H2} are zero.

$$G_{0LP} = \frac{1}{R_{D1}} + \frac{1}{R_{D2}} \tag{2.67}$$

$$V_{DRVMIN} = \frac{V_{DD}}{G_{0LP} R_{D1}} \tag{2.68}$$

Voltage V_{DRVMIN} is set equal to V_{REF2} of Fig. 2.17. It can be easily noted that M7 and M8 represent the input section of the digital programmable mirror controlled by DW. Bit b_{CR} sets the low/high current range respectively by enabling (b_{CR} = 1) or switching off (b_{CR} = 0) transistor M8 in parallel with M7. Bit b_{OFF} switches off the entire mirror making zero the outputs currents regardless of V_{DRV} and DW. Bits (b_0 – b_7) forming DW acts on the binary weighted output section of the programmable mirror (multiplicity of each transistor is indicated in round brackets). Drain current provided by M9 is mirrored with to the output section in order to provide an output current I_{H0} = $K_D K_0 I_{D9}$ independent of the value of DW, where K_D is the current mirroring factor provided by the output DMOS mirrors (DM1-DM2 and DM3-DM4), while K_0 is provided by M10-M11 and M12-M13 mirrors. We consider the output currents positive when entering the terminals.

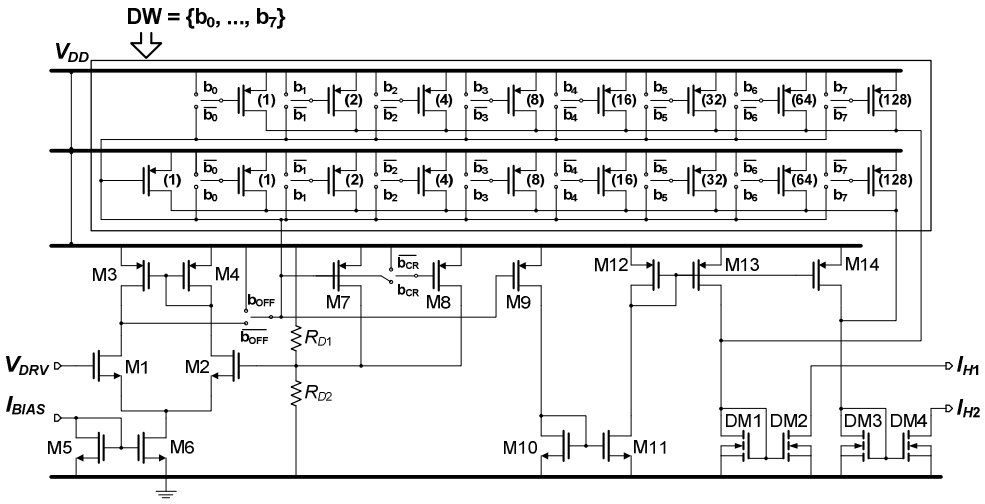


Fig. 2.24 – Digitally controlled current driver schematic diagram.

Considering eqs. (2.66-2.67), the output currents can be expressed as

$$I_{H1} = \overline{b}_{OFF} \cdot \frac{G_{0LP}}{2^{b_{CR}}} \cdot K_D \cdot \left(K_0 + 256 - [\mathrm{DW}]\right) \cdot \left(V_{DRV} - V_{DRVMIN}\right) \tag{2.69a}$$

$$I_{H2} = \overline{b}_{OFF} \cdot \frac{G_{0LP}}{2^{b_{CR}}} \cdot K_D \cdot \left(K_0 + 1 + [\mathrm{DW}]\right) \cdot \left(V_{DRV} - V_{DRVMIN}\right) \tag{2.69b}$$

where

$$[\mathrm{DW}] = \sum_{i=0}^{7} 2^i b_i \tag{2.70}$$

It can be easily found that K_0 sets the maximum current variation respect to the nominal current (i.e. when [DW] = 127 and $I_{H1} = I_{H2}$); from eqs. (2.69a-b)

$$\frac{\max(\Delta I_H)}{I_{HNOM}} = \frac{\left|I_{H1} - I_{H2}\right|_{[\mathrm{DW}]=0,255}}{\left|I_{H1}\right|_{[\mathrm{DW}]=1275}} = \frac{255}{K_0 + 128} \tag{2.71}$$

The global transconductance G of the stage is given by

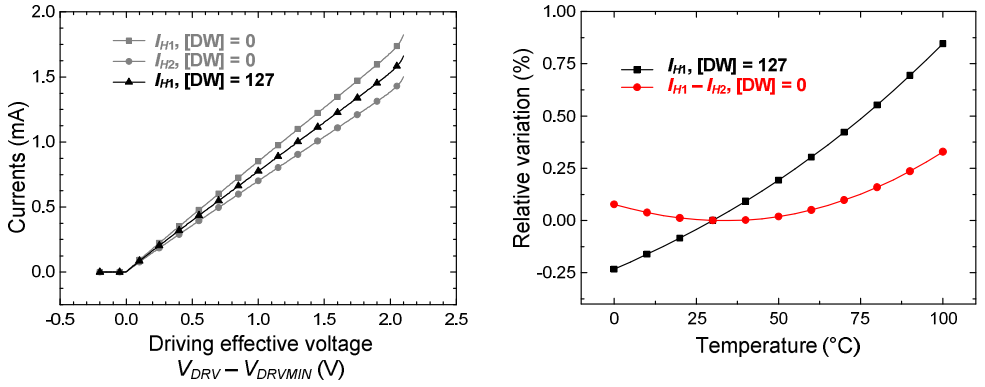
$$G = \overline{b}_{OFF} \cdot \frac{G_{0LP}}{2^{b_{CR}}} \cdot K_D \cdot \left(K_0 + 128\right) \tag{2.72}$$

The value of transconductance G can be inferred from the previous discussion

$$G = \frac{I_{HMAX}}{V_{DRVMAX} - V_{DRVMIN}} = \left(\frac{W_{MAX}}{R_H}\right)^{\frac{1}{2}} \frac{1}{V_{DRVMAX} - V_{DRVMIN}} \tag{2.73}$$

considering the requirements on table 2.V, for example for the BCD6s structure, and considering a maximum input swing of 2 V for the circuit of Fig. 2.24, we find G = 0.5 mS (with b_{CR} = 1). Furthermore we fix the maximum relative current variation (see eq. (2.69)) to 20%. With this values, a prototype has been

implemented with K_0 = 1147, K_D = 32, G_{0LP} = 8.3 µS, V_{DRVMIN} = 1 V, resulting finally in R_{D1} = 396 kΩ, R_{D1} = 172 kΩ. Figure 2.25 shows the characteristics of the prototype and the temperature behaviour for two configurations of DW. Note that the characteristics are linear in the whole desired input range of 2 V, and that relative temperature variations of the output currents (and their difference) are maintained below 1% in the whole 0-100℃ span. Transconductance relative variation ($\Delta G/G$) and input offset voltage ($V_{DRV,OS}$) due to device mismatching has been estimated through several Monte Carlo runs, resulting in less than 7 % and of the order of 3 mV, respectively.



(a) (b)

Fig. 2.25 – (a) Current driver characteristics for the two DW configurations and b_{CR} set in both cases (low current range). (b) Relative temperature variation normalized to the value at T = 30℃ of current output current (I_{H1}) and current difference ($I_{H1} - I_{H2}$) in the two indicated DW configurations, respectively.

2.4.3. Full-analog CMOS current driver

The digitally controlled current driver, discussed in the previous section, effectively fulfils the requirements for the sensor driving application. Despite of this, the possibility of a full analogue cell implementing the same function has been also investigated [48]. Let us elaborate eqs. (2.69a-b) in order to point out some important properties of the cell in Fig. 2.24:

$$I_{H2} + I_{H1} = \bar{b}_{OFF} \cdot \frac{G_{0LP}}{2^{b_{CR}}} \cdot K_D \cdot (2K_0 + 257) \cdot (V_{DRV} - V_{DRVMIN}) = I_{HS} \tag{2.74a}$$

$$I_{H2} - I_{H1} = I_{HS} \cdot \frac{2[\mathrm{DW}] - 255}{2K_0 + 257} = I_{HS} \cdot f([\mathrm{DW}]) \tag{2.74b}$$

where the introduced current I_{HS} lumps the cell important parameters and the driving input voltage. Thus, in the compact description of the above equations, I_{HS} can be regarded as a system input. The other input is the digital word (DW) that appears in eq. (2.74b). It is worth noting that the condition $0 \le f([\mathrm{DW}]) \le 1$ is guaranteed when K_0 is obtained under the condition $0 \le \max(\Delta I_H)/I_{HNOM} \le 1$ (see eq. (2.71)). An equivalent set of equations can be given

$$\frac{I_{H2}}{I_{HS}} = \frac{1+f([DW])}{2} \tag{2.75a}$$

$$\frac{I_{H1}}{I_{HS}} = \frac{1-f([DW])}{2} \tag{2.75b}$$

It is now evident the behaviour of the circuit which inputs a current I_{HS} that is linearly divided between the two output currents I_{H1}, I_{H2} depending on f([DW]). The above equations point out that the current transfer ratios do not depend on the input I_{HS}, but only on the value of DW. Such a property is fundamental for the linearity of the current division operation.
The same function described by eqs. (2.75a-b) can be obtained in a full analog current divider, which operates the linear current division according to fractions set by a control voltage V_d. Such a circuit obeys to this set of equations

$$\frac{I_{H2}}{I_{HS}} = \frac{1+f(V_d)}{2} \tag{2.76a}$$

$$\frac{I_{H1}}{I_{HS}} = \frac{1-f(V_d)}{2} \tag{2.76b}$$

with $f(V_d)$ a general function of V_d. Or equivalently:

$$I_{H2} + I_{H1} = I_{HS} \tag{2.77a}$$

$$I_{H2} - I_{H1} = I_{HS} \cdot f(V_d) \tag{2.77b}$$

A very simple circuital implementation of eqs. (2.77a-b) is based on a differential BJT pair, fed at the common emitter node with I_{HS} and driving the base terminals with a differential voltage V_d. In this case the collector currents represent I_{H1} and I_{H2} as given from eqs. (2.76a-b) with a extremely precision over an I_{HS} range of several decades.
Such a useful property is not retained when the same circuit is implemented with MOSFETs in saturated region and strong inversion. Using the square law approximations for the drain currents and considering an input differential voltage V_d much smaller than overdrive ($V_{GS} - V_t$) of the couple, we would have:

$$I_{H2} - I_{H1} = I_{D2} - I_{D1} = V_d \sqrt{\beta_n I_{HS}} \tag{2.78}$$

where, as usual, $\beta_n = \mu_n C_{ox} W/L$, μ_n is the electron mobility, C_{ox} the gate capacitance per unit area and W/L the transistor aspect ratio. Comparison between eqns. (2.75a-b) and (2.76) confirms that the saturated MOSFET pair does not operate as a linear current divider, except for small I_{HS} variations around the DC bias value. In terms of signal dynamic range, such a limitation is detrimental, since the thermal noise floor (current spectral density) is proportional to the bias current, which, for the discussion above, should be much larger than the maximum signal amplitude, to preserve linearity.
As an alternative, it is possible to exploit the MOSFET subthreshold exponential behavior to mimic bipolar devices [49]. In practice, the usable current range is much smaller than in case of real bipolar devices and the frequency response is sacrificed. This limitation is only partially removed in [50]. A different approach that can be used to improve the linear range of MOSFET current dividers is shown in

Fig. 2.26, where all the devices are supposed to operate in saturation region and M1, M2 , M3 are identical. For a small v_d, we easily get:

$$I_{H2} - I_{H1} = R \cdot (g_{mA} g_{mB}) \cdot v_d \tag{2.79}$$

where g_{mA} and g_{mB} are the transconductances of the MOSFETs in the first and second differential pair, respectively. Let us first consider that the two differential pairs in Fig. 2.26 are identical, thus $g_{mA} = g_{mB} \equiv g_m$. At this stage, let us also set $I_B = 0$. Applying the square law approximation of the drain current we get:

$$I_{H2} - I_{H1} = R \cdot g_m^2(I_{HS}) \cdot v_d = R\beta_n \cdot I_{HS} \cdot v_d \tag{2.80}$$

that, together with eq. (2.77a) implies a linear relationship between I_{HS} and both output currents.

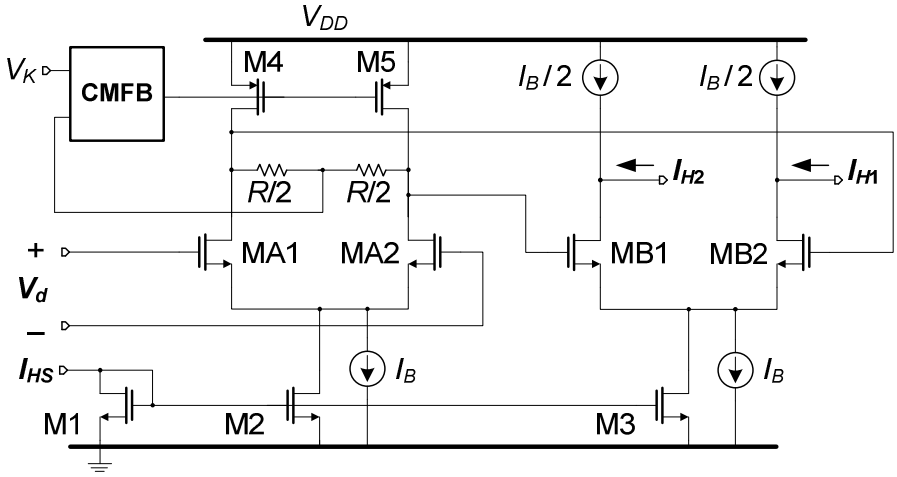


Fig 2.26 – Schematic view of the proposed topology for an analog current divider based on a cascade of two MOSFET differential pairs.

Electrical simulations have been performed with a prototype sized with $W = L = 16$ µm; the high length value was chosen to reduce short channel effects as much as possible. A significant residual non-linearity is visible in Fig. 2.27(a), showing the g_m^2 curve as a function of I_{HS} and its linear fit.

In terms of derivative, shown also in Fig. 2.27(a), two different regions can be distinguished: a low current region, where the derivative increases, and a high current region where the derivative decreases. The former is well explained by the transition to weak inversion while the behavior at high currents originates from field induced mobility degeneration [51]. Both phenomena are precisely modeled by the PHILIPS-9 model provided with the process design-kit. The idea is to make the first differential pair (MA1, MA2) work in the high current region and the second pair (MB1, MB2) in the low current region, trying to balance the two opposite tendencies. To this aim, MB1 and MB2 are now a parallel of k transistors identical to M_{A1} and M_{A2}, so that each element of the parallel receives a current k times smaller than the transistors of the first pair. Equation (2.79) becomes:

$$I_{H2} - I_{H1} = Rk \cdot g_m(I_{HS}) g_m(I_{HS}/k) \cdot v_d = F_K(I_{HS}, k) \cdot v_d \tag{2.81}$$

where the function F_K has been introduces, with independent variable I_{HS} and parametric parameter k:

$$F_K(I_{HS},k) = Rk \cdot g_m(I_{HS}) g_m(I_{HS}/k) \qquad (2.82)$$

An automatic procedure has been implemented in the MATLAB environment to find the optimum k which minimizes the non linearity of F_K. The procedure uses a spline interpolation of the simulated g_m *vs.* I_{HS} curve. The rest value of I_{HS} was chosen equal to 100 µA. It is obvious any desired range of current can be obtained by simple current mirrors. For each integer value of the parameter k, the procedure calculates:

(i) the linear approximation of F_K around the I_{HS} rest point;
(ii) the I_{HS} interval, where the deviation from linearity is less than 1 % (linearity interval).

The optimum k is that for which the linearity interval is maximum.
Applying the procedure to the case mentioned above, (process, MOSFET size and resting point) an optimum value k = 10 turned out.

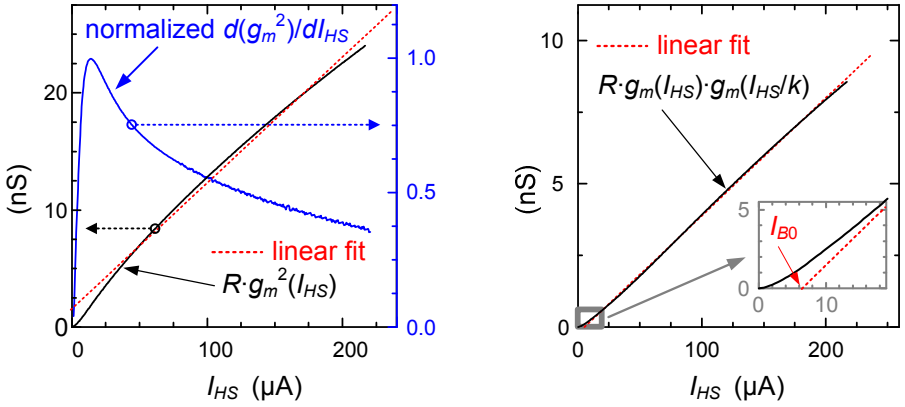


Fig 2.27 – Plot of: (a) Rg_m^2 VS. I_{HS} for a differential pair with W/L = 16/16, R = 1 Ω; (b) the function F_K (with R = 1 Ω) VS. I_{HS} in the optimum condition k = 10.

The corresponding F_K curve is shown in Fig. 2.27(b) along with the linear fit for the interval 20-180 µA. Although is possible to observe a satisfactory linear behavior, the magnification (inset) shows that the linear fit does not pass through the origin, but for the point (I_{B0}, 0) with I_{B0} around 6 µA. Thus, in the linear region, $I_{H2} - I_{H1}$ is not strictly proportional to I_{HS} and, consequently, the ratios I_{H2}/I_{HS} and I_{H1}/I_{HS} are not independent of I_{HS}. To compensate for this error, it is simply possible to add a constant current I_{B0} to I_{HS}, shifting the curve in Fig. 2.27(b) to the left of an amount just equal to I_{B0}. The effect is obtained by simply providing the I_B current sources in as shown in figure, setting $I_B = I_{B0}$. The current sources $I_B/2$ on the output nodes are required to make eqs. (2.76a-b) still hold.

A prototype cell has been designed according to Fig. 2.27(b). Simple current mirrors driven by a single ideal reference current have been used for the sources I_B and $I_B/2$. The following values have been applied: I_B = 6 µA, R = 6 kΩ, V_{DD} = 3.3 V. The output ports indicated with I_{H1}, I_{H2} where terminated onto 2.8 V constant voltage sources for the test.
Fig. 2.28(a) shows the ratio $(I_{H2} - I_{H1})/I_{HS}$ as a function of current I_{HS} for various input differential voltages. The simulations prove that a nearly constant division factor over a wide relative input current range (1:8) can be actually obtained with the proposed approach. The fact that the curves are nearly evenly spaced indicates also a good linearity with respect to the control voltage V_d. It is important to observe that, at the lower limit of the input current range (25 µA), the $V_{GS} - V_t$ of the first and second differential pair is equal to 380 mV and 70 mV, respectively. As a consequence, the first pair operates in strong inversion over the whole input range, while the second pair approaches the weak inversion boundary (nearly three times the thermal voltage) only at the lower end of the input current range. The relative variations of the $(I_{H2} - I_{H1})/I_{HS}$ ratio with respect to the average value over the 25–200 µA current range are shown in Fig. 2.28(b). It should be observed the error remains within ±3 % band.

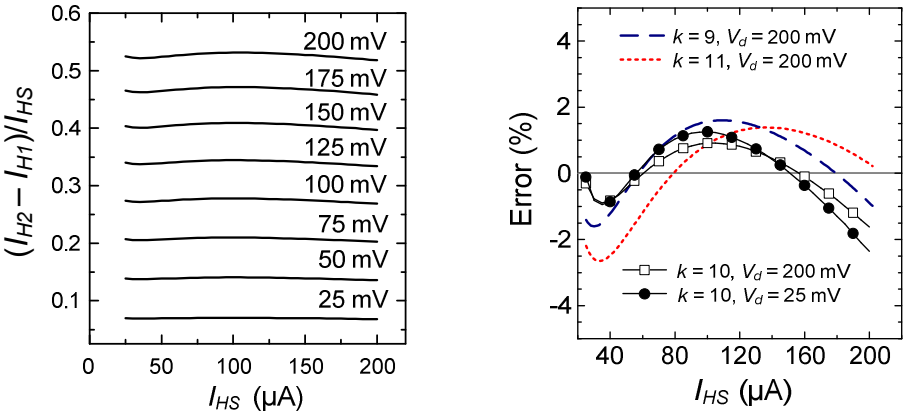


Fig 2.28 – (a) Plot of the $(I_{H2} - I_{H1})/I_{HS}$ ratio as a function of I_{HS} for various input voltages; (b) relative variation of the $(I_{H2} - I_{H1})/I_{HS}$ with respect to its average value (across the whole interval) in four different cases shown in the legends

To prove that the proposed circuit represents a real advantage as a linear current divider with respect to a single MOSFET differential pair, we have studied the dependence of ratios I_{H2}/I_{HS} and I_{H1}/I_{HS} on the input current for a fixed control voltage value. The result is shown in Fig. 2.29(a) where DP10 and SP indicate the proposed circuit and the single differential pair, respectively.
In order to show also the actual effectiveness of scaling down the current density in the second differential pair, we have added the result obtained with the topology in Fig. 2.26 but with no current scaling (curves DP1). MOSFETs with 16/16 aspect ratio have been used for the SP and DP1 cases. The control voltage V_d was individually adjusted to set the I_{H1}/I_{HS} ratio to 0.25 at I_{HS} = 110 µA for all circuits.

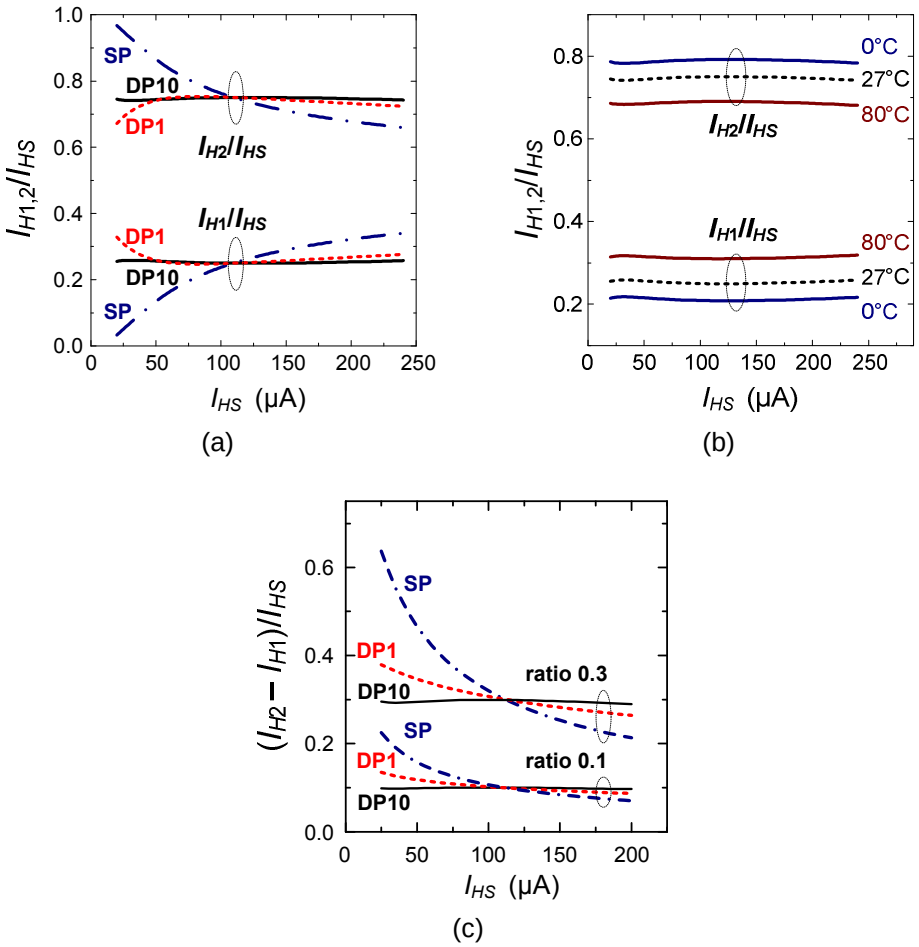


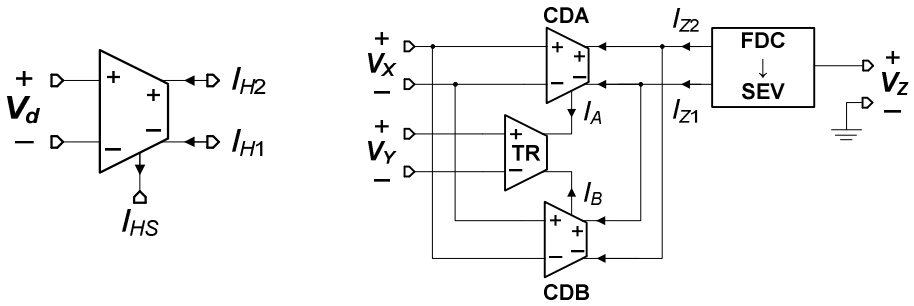
Fig 2.29 – Plot of output-to-input current ratios as the function of the input current for a fixed control voltage. In (a) the proposed circuit (DP10) with the optimum value of k = 10 is compared with the same topology but with k = 1 (DP1) and a single MOSFET differential pair (SP) In (b) the current ratios simulated at three different temperatures are shown for the proposed circuit. In (c) curves of differential output to input currents for the ratio of 0.1 and 0.3 are plotted, with the same comparison as in (a).

It can be observed that, in the single pair, the current ratios are strongly dependent on I_{HS}. The dependence is reduced but still remarkable for the DP1 case, as expected from Fig. 2.27(a), while, with the proposed circuit, nearly input independent current ratios can be observed. In particular, the relative variation of ratio I_{H2}/I_{HS} was 20% for the SP case, 5.3% for the DP1 case and only 0.6% for DP10 case. This proves that the proposed approach can be actually used to obtain a linear controlled current divider. Simulations performed with different control voltages, i.e. different nominal current ratios, substantially confirm the results of Fig. 2.29(a).

The simulations of Fig. 2.29(a) have been repeated varying the temperature from 0 to 80℃, in order to check how temperature affects the linearity of current ratios obtained with the compensation method. The results for the upper and lower limit of the temperature interval are shown in Fig. 2.29(b) for the proposed circuit. The nominal curves simulated at 27℃ have also been reported for comparison purposes. These simulations indicate that the low dependence of the current ratios on the input current is maintained over a wide temperature range. Therefore, a temperature increase from 0 to 80℃ does not alter the linearity properties of the circuit, though a remarkable convergence of both ratios towards the value 0.5 can be observed. This is well explained by the decrease of the g_m factors due to the temperature dependence of electron mobility. Mitigation of this effect can be obtained using a resistors R with a proper positive temperature coefficient, or implementing the resistor with triode operating MOSFET as will be discussed in the next section.
Obviously, the optimization procedure can be easily automated to be applied to different design choices. Reasonably, the degree of linearity that can be actually achieved depends on the process and transistor size considered.

2.4.4. Four quadrant multiplier based on current divider cells

The linear current divider presented in the previous section inspired the realization of a four quadrant CMOS analog multiplier. Let us consider the block representation in Fig. 2.30(a) of the linear analog current divider discussed in the previous section. It is possible to implement a four quadrant multiplier with a Gilbert-like architecture, composing two current divider with few other blocks, as shown in Fig. 2.30(b).



(a) (b)

Fig 2.30 – (a) Block representation of the analog current divider.
(b) Four quadrant multiplier obtained with two current dividers (CDA, CDB).

Block TR is a fully differential transconductor, with constant transconductance G_m. Its output currents, I_A and I_B in Fig. 2.30, are related to a common mode current I_C and a differential component $G_m V_Y$ according to:

$$I_A = I_C + \frac{1}{2} G_m V_Y \tag{2.83a}$$

$$I_B = I_C - \frac{1}{2} G_m V_Y \tag{2.83b}$$

The current difference $I_{Z2} - I_{Z1}$ can be calculate as

$$I_{Z2} - I_{Z1} = \left(I_{H2} - I_{H1}\right)_A - \left(I_{H2} - I_{H1}\right)_B = kG_m \cdot V_Y V_X \tag{2.84}$$

Although the MOSFET square law is not strictly valid, it is still useful to use it to obtain an approximation for the differential output current of each CD block:

$$\left(I_2 - I_1\right)_{A,B} = R\beta_E \cdot I_{A,B} \cdot V_X \tag{2.85}$$

where $\beta_E = (\beta_A\beta_B)^{-1/2}$, while β_A and β_B refer to MA1-MA2 and MB1-MB2 pairs in Fig. 2.26, respectively. To reduce the sensitivity to temperature and process variations introduced by β_E, resistors $R/2$ have been implemented using *n*-MOSFETs with their gates connected to V_{DD}. These devices operates in linear region, providing an equivalent load resistance $R = 2/\beta_T(V_{DD} - V_K - V_t)$. From eq. (2.84):

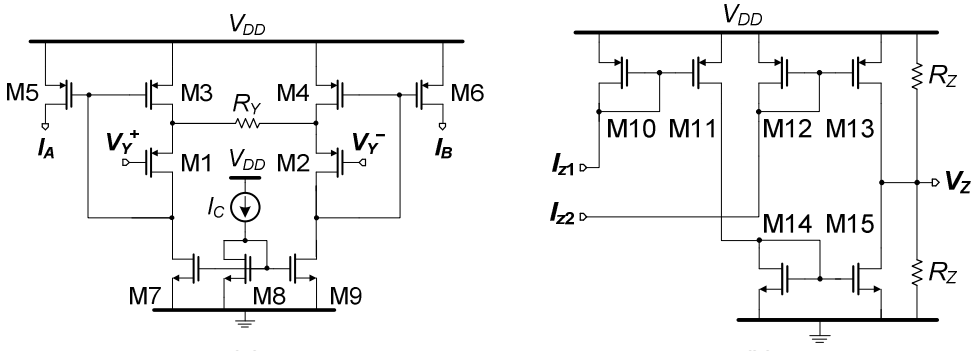
$$\left(I_2 - I_1\right)_{A,B} = \frac{2\beta_E}{\beta_T} \cdot \frac{V_X}{V_{DD} - V_K - V_t} \cdot I_{A,B} \tag{2.86}$$

The block TR of Fig. 1 has been implemented with the source degenerated transconductor shown in Fig. 2.31(a). It can be easily shown that eqs. (2.83a-b) hold for the output currents I_A and I_B with $G_m = 2/R_Y$. In order to obtain a single-ended, wide swing output voltage, currents I_{Z2} and I_{Z1} are subtracted by means of current mirrors and fed to a resistive load as shown in Fig. 2.31(b). The overall multiplier transfer characteristic is then

$$V_Z = K_m V_X V_Y + V_{DD}/2 \tag{2.87}$$

where, the theoretical multiplier gain K_m is given by

$$K_m = \frac{R_Z}{R_Y} \cdot \frac{2\beta_E}{\beta_T} \cdot \frac{1}{V_{DD} - V_K - V_t} \tag{2.88}$$



(a) (b)

Fig 2.31 – (a) Schematic diagram of transconductor TR (b) Fully differential current to single ended voltage (FDC/SEV) schematic diagram.

The validity of the approach has been demonstrated by means of a simple prototype, designed and produced using CMOS devices from the STMicroelectronics BCD6s process. The aim was to evaluate the effectiveness of the method in terms of static characteristics; therefore no speed optimization has been performed. The current dividers have been sized according to the

optimization procedure described in the previous section, with $k = 10$ and active device aspect ratio 16/16. The power supply was 3.3 V with a total supply current of 1.3 mA. Resistors R_Y and R_Z has been set to 10 kΩ and 25 kΩ, respectively (p-polysilicon resistors), while the *n*-MOSFET implementing R have $W = L = 1$ μm. With these values the multiplier gain K_m, estimated by simulations, is 2.92 V^{-1}. An optical micrograph of the multiplier is shown in Fig. 2.32. The total occupied area is 680×310 μm^2. The cell includes also bias current generators and a spare current divider.

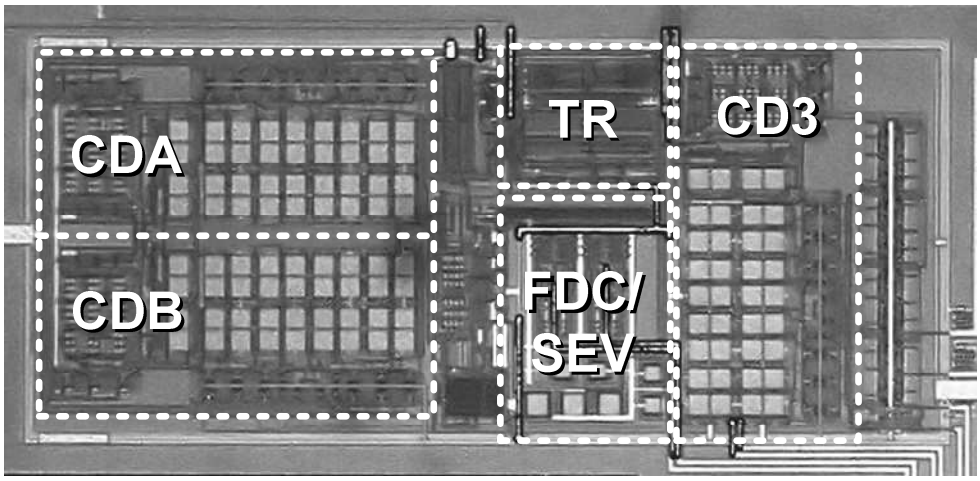
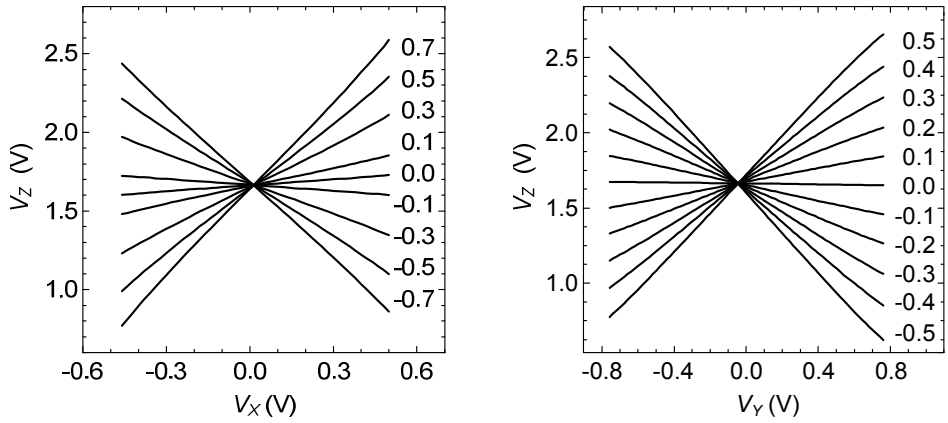


Fig 2.32 – Optical micrograph of the multiplier cell. Blocks names has the same meaning as in Fig. 2.30(b); CD3 is a spare current divider. Chip area is 680×310 μm^2.

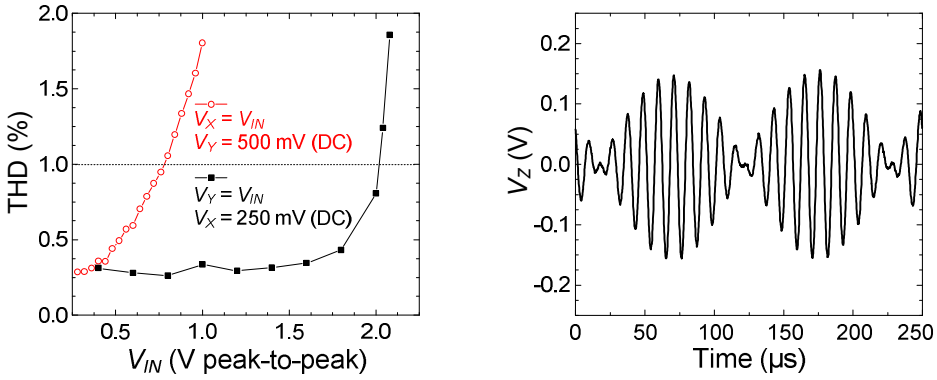
In all the experiments a purposely built circuit has been used to provide differential inputs with a common mode voltage set to 2.2 V and 1.2 V for the X and Y inputs, respectively. The static characteristics have been measured by means of an HP 4145B parameter analyzer. The output voltage dependence on V_X for various V_Y values is shown in Fig. 2.33(a), while the result of sweeping V_Y with constant V_X is shown in Fig. 2.33(b). A wide linearity range can be observed for both inputs. Linearity with respect to the V_X input is achieved by simply setting the gate overdrive voltage differential pairs in the dividers to a value higher than the differential voltage swing at their respective inputs. More interestingly, the good linearity with respect to V_Y is a result of the linear relationship between the input and output currents of the dividers, obtained with the proposed procedure. The offset on the X and Y input was 4 mV and 48 mV, respectively. These values are consistent with the offsets estimated by Monte Carlo simulations. The large Y offset can be ascribed to the use of small area devices in the transconductor TR. The multiplier gain K_m estimated from these measurements was 2.6 V^{-1}.



(a) (b)

Fig 2.34 – Static characteristics obtained sweeping the input V_X with constant V_Y (a) and viceversa (b). The value of the constant voltage is indicated in mV close to each curve.

To confirm the good linearity properties, the total harmonic distortion as a function of the input amplitude has been measured applying a sinusoidal signal to either the X or Y input, maintaining the other input at a constant DC voltage. The output THD was estimated by means of a digital signal analyzer, based on a high resolution acquisition system (Pico Technology Ltd, mod. ADC216). The results obtained at 1 kHz are shown in Fig. 2.34(a). Note that the distortion remains below 1 % for $V_Y < 2\ V_{P-P}$ (peak−to−peak) and $V_X < 0.75\ V_{P-P}$. The simulated small signal bandwidth is around 4 MHz for both inputs X and Y.



(a) (b)

Fig 2.35 – (a) Output THD at 1 kHz as a function of the input amplitude for both inputs X and Y. The voltage of the constant input is reported. (b) Output voltage (with oscilloscope AC coupling) obtained applying a 5 kHz and 100 kHz signal to X and Y, respectively

Finally, Fig 2.34(b) shows the result of a modulation experiment, obtained with V_X : 5 kHz, 600 mV_{P-P}, V_Y : 100 kHz, 400 mV_{P-P}. A DC bias has been added to the Y input to compensate for the large offset. The output voltage was acquired with a Tektronix TDS220 digital oscilloscope.

3. DESIGN OF A SMART CHIP PROTOTYPE FOR INTEGRATED THERMAL FLOW-METERS

This chapter describes the chip floor-plan for the smart flow-meter recollecting information from chapter 1 and 2. Auxiliary circuits, needed for the arrangement of all the sensors and the electronic blocks, are discussed. Preliminary tests are presented in the final section of this chapter.

3.1 Electronic blocks and auxiliary circuits

The block diagram of the chip is represented in Fig. 3.1. The clock generation block produces a master clock (*CKM*) that is shared between the differential mode (DFRC) and the common mode (CMRC) read-out chains. Phases generation occurs inside each of the latter block as will be discussed in the following. A digital communication interface allows the programmability of all the system parameters through a serial interfacing protocol. As the number of required pad is relatively large, the problem of pad limitation has to be faced. A purposely designed digital communication interface (DGI) is provided in order to program of all the system parameters through a serial interfacing protocol, and effectively reducing the number of pad needed. On the other hand few selected bits have been made accessible to pad in order to simply change some fundamental chip parameters without the need of DGI interfacing. To this purpose, an overridable bit technique has been adopted and will be illustrated in section 3.1.5.
Common and differential read-out chains shares TH1 and TH2 terminals too. The voltage reference THC, produced inside the DFRC block, is applied to the common terminal of each thermopile couple (sensors A, B, C). Furthermore it is routed to the CMRC block and has been made available on pin for use in external sensors. Reference THC is needed to adapt the thermopile within the chopper amplifier common mode input range. On board sensors signals and are multiplexed into the electronics readout interfaces through the sensor selection block. Eventually, external sensors can be directly connected to the interface electronics through the EXT_TH1, EXT_TH2, EXT_H1 and EXT_H2 pins; in this case the sensor selector block can be set in order to exclude connections of the internal sensors. This block coherently feed the driver currents (H1, H2) to the heaters of the selected sensor structure. The same selector allows the internal sensors to be accessible through EXT_TH1, EXT_TH2, EXT_H1 and EXT_H2 pins for diagnostic purposes. Heaters supply voltage VDDH is made independent in order to have a further degree of freedom on released heater power. The controlled heating block is used in the sealing phase of package application to chip and will be described in section 3.1.2. Figure 3.2 shows the details of the sensor selection block.

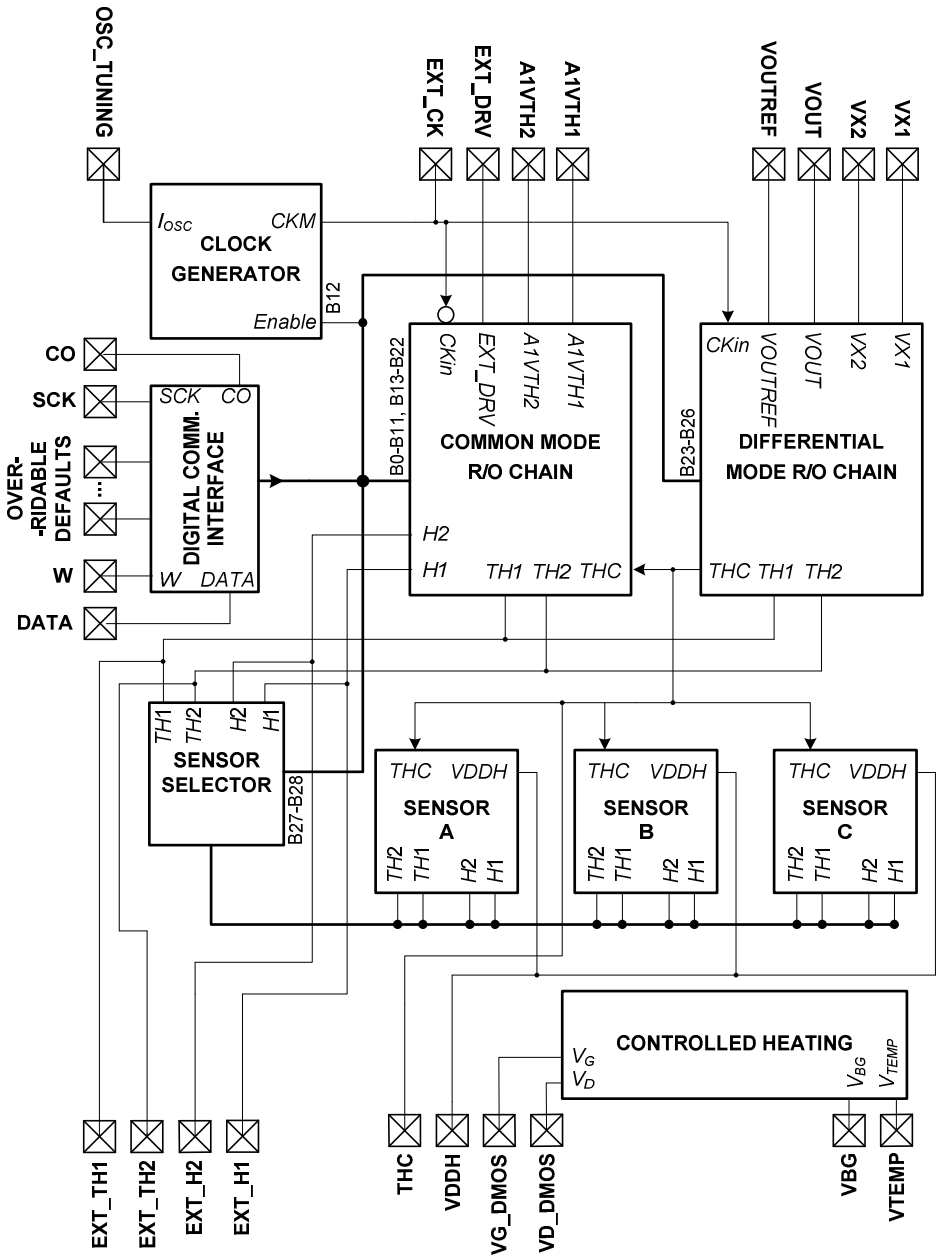


Fig. 3.1 – Block diagram of the chip; some power pins (VDD, VDDC, VDDD, GND) are not explicitly indicated and will be discussed in the following sections.

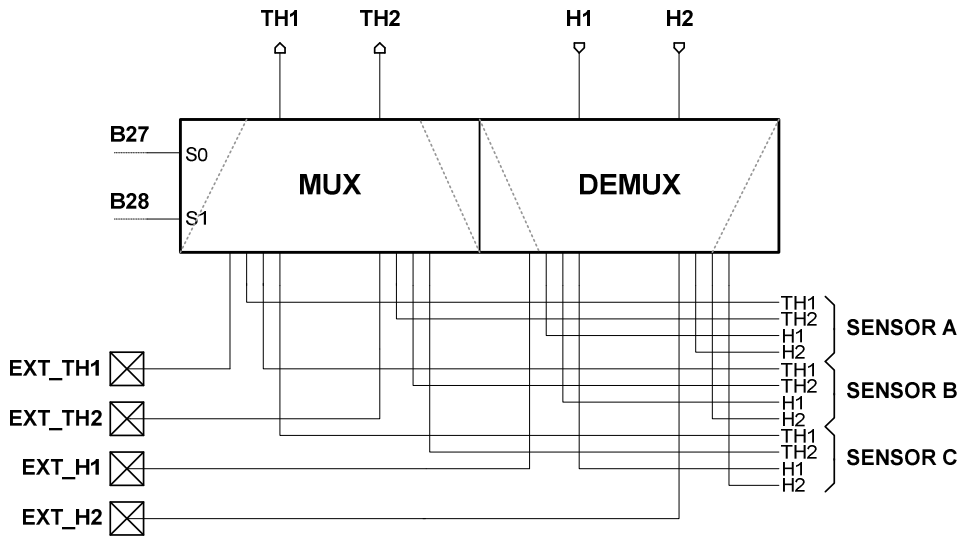


Fig. 3.2 – Block diagram of the sensor selector block.

3.1.1. On chip clock generation

The scheme used to produce the master clock signal *CKM* is shown in Fig. 3.3. The clock generator is simple relaxation oscillator based on current starved inverter (M5, M9 and M12-M13) and a comparator CMP with hysteresis (V_{IS}). Starting from the condition of high Enable and high CMP output we have that M13 is turned on while M12 is turned off. Thus M9 drain current is connected the capacitance *C*, drawing its charge and making V_C decrease. This lasts until V_C reaches the hysteresis low threshold; at this point the comparator output falls down switching off M13 and turning on M12. Now M5 drain current charges capacitor *C*, making V_C increase until it reaches the high hysteresis threshold and finally setting the CMP output high. Thus, in case of constant and equal M5 and M9 drain currents, a symmetric triangular V_C waveform is obtained, whose period is simply given by

$$T_{CKM} = CV_{IS} \cdot \left(\frac{1}{I_{D9}} + \frac{1}{|I_{D5}|} \right) = \frac{2CV_{IS}}{(I_R + I_{OSC})/K_M}; \tag{3.1}$$

where currents I_R and I_{OSC} are simply replicated through M1-M2, M3-M5, M8-M9 mirrors with a reduction factor of K_M. The comparator schematic is shown in Fig. 3.4. It is possible to demonstrate that the hysteresis voltage results

$$V_{IS} = (V_{GS} - V_t)_1 \cdot \left(\frac{\beta_B}{\beta_A} - 1 \right) \cdot \left(\frac{\beta_B}{\beta_A} + 1 \right)^{-1}; \tag{3.2}$$

where β_A and β_B own to transistor M3, M5 and M6, M4 in Fig. 3.4, respectively.

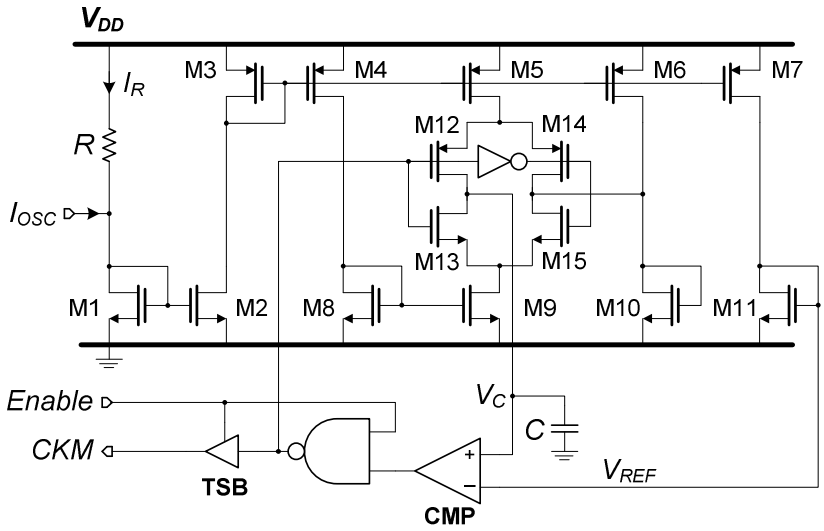


Fig. 3.3 – Schematic diagram of the relaxation oscillator used for the generation on chip of the master clock (CKM).

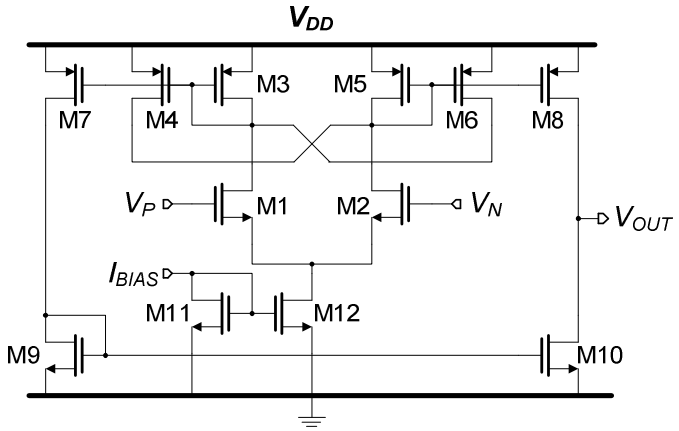


Fig. 3.4 – Schematic diagram of the comparator (CMP) in Fig. 3.3.

Figure 3.5 shows the schematic diagram of the three-state buffer (block TSB) used to disconnect the oscillator output in presence of external clock applied, i.e. when Enable is low. Terminal I_{OSC} is accessible through the OSC_TUNING pin; when left floating the cell has been designed to produce a CKM square waveform with a fundamental period of 10 kHz. The following design choices have been made: R = 305 kΩ, C = 18.4 pF, K_M = 100, V_{IS} = 190 mV. Clock frequency can be easily changed, for example, by connecting an external resistor across the OSC_TUNING and VDD (to increase frequency) or across OSC_TUNING and ground (to lower frequency). In Fig. 3.5 the CKM fundamental frequency *VS.* external resistor R_E value is shown in case the latter is applied between OSC_TUNING and VDD pins.

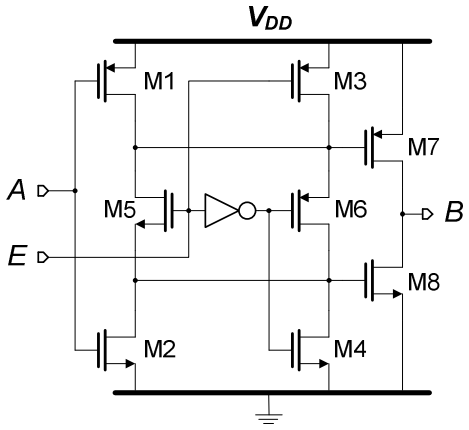


Fig. 3.5 – Schematic diagram of the three-state buffer (TSB) in Fig. 3.3.

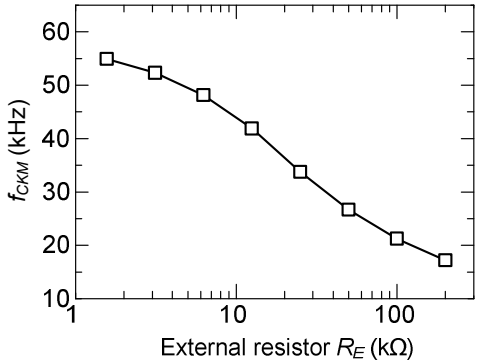


Fig. 3.6 – Plot of CKM fundamental frequency ($f_{CKM} = 1/T_{CKM}$) as a function of the external resistor R_E applied between OSC_TUNING and VDD pins.

The master clock signal *CKM* is shared between both the DMRC and CMRC blocks. In order to minimize any possible interference between the chopper input modulator and the switches at the input of the CMRC block we chose to separate the switching events by an applied delay. The simple solution of shown in Fig. 3.7 allows the generation of all the non overlapped phases needed in the circuits. Separation between switching events in DMRC and CMRC blocks are obtained by halving *CKM* frequency and driving the two frequency dividers, simply implemented with fed back D-latches, with the positive and the negative phases of *CKM*, respectively. This solution allows the θ-phases to be delayed by a quarter of the operative frequency with respect to the corresponding φ-phases. On the other hand a clock division by two ensures a precise 50 % duty cycle waveform needed for correct offset cancellation in the chopper amplifier.
Figure 3.8 shows the simple scheme for inverting the θ-phases at the input switches of the CMRC block, useful to adjust the thermopile common mode voltage sign and guarantee the close loop stability, as discussed in section 2.4.

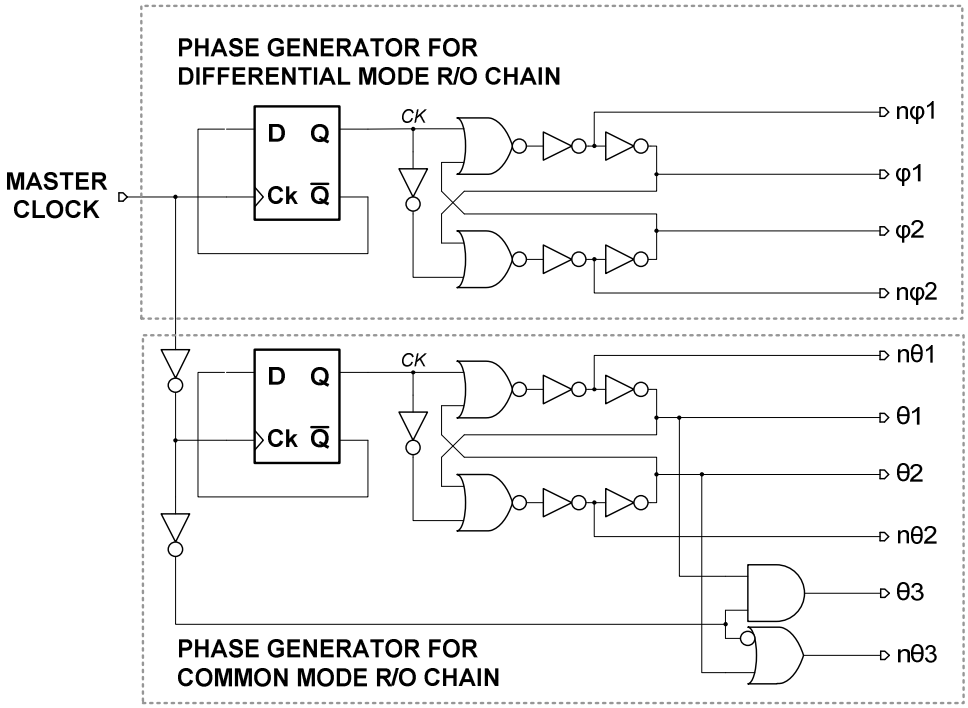


Fig. 3.7 – Schematic diagram of phases generation circuitry for the differential mode and common mode read-out chains.

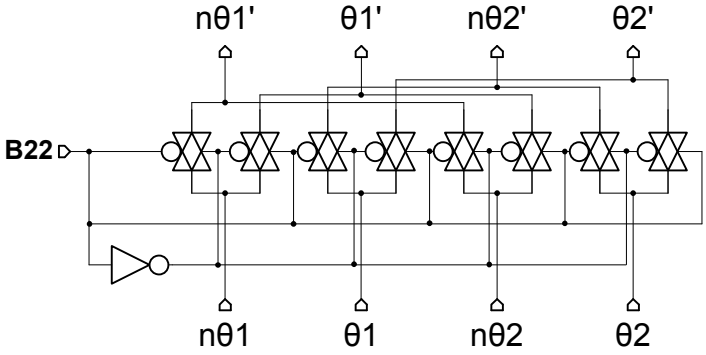


Fig. 3.8 – Schematic diagram of phases inversion circuitry for the input switch of the common mode read-out chain.

3.1.2. Controlled heating of the chip

The chip has been designed in order to easily both apply heating at the bulk and measuring its temperature at the same time. This functionality greatly simplifies the sealing operation of the package, as described in section 1.3.2. To do so, DMOS devices, electrically connected in parallel, have been sparsely placed in the chip; their gate and drain terminal are available through pins VG_DMOS and

VD_DMOS, respectively, in order to make possible the realization of the temperature controlling loop shown in Fig. 1.1.4. The substrate temperature is also measured on chip by the simple ΔV_{BE} temperature sensor shown in Fig. 3.9. The circuit operation is based on the drain currents of transistors M4-M3 and on the equality of V_{GS1} and V_{GS2}. By design, this condition can be achieved making equal both M3-M4 and M1-M2, respectively. Neglecting matching errors, we can write

$$V_{R1} = V_{BE1} - V_{BE2} = \frac{kT}{q} \cdot \ln\left(\frac{I_{S2}}{I_{S1}}\right) \tag{3.3}$$

where V_{R1} is the voltage drop across R_1. The emitter area of Q2 is made n times larger of the emitter area of Q1 (n = 8, in our case), so that the argument of the natural logarithm in eq. (3.3) is n. The same current flowing through R_1 is then mirrored through M3-M6 (by a mirror factor K_m) on resistor R_3, resulting in the output V_{TEMP} voltage equal to

$$V_{TEMP} = R_3 \cdot K_m \frac{V_{R1}}{R_1} = K_m \frac{R_3}{R_1} \frac{kT}{q} \cdot \ln(n) \tag{3.4}$$

The temperature dependence of V_{TEMP} can be studied through its derivative with temperature

$$\frac{T}{V_{TEMP}} \cdot \frac{dV_{TEMP}}{dT} = 1 + T \cdot \left(\frac{1}{R_3} \frac{dR_3}{dT} - \frac{1}{R_1} \frac{dR_1}{dT} \right) \tag{3.5}$$

If the term in brackets is zero, then V_{TEMP} results linearly dependent on temperature. This can be done by simply choosing identical resistors, so that both their resistance values and their TCR (dR/dT) are equal.

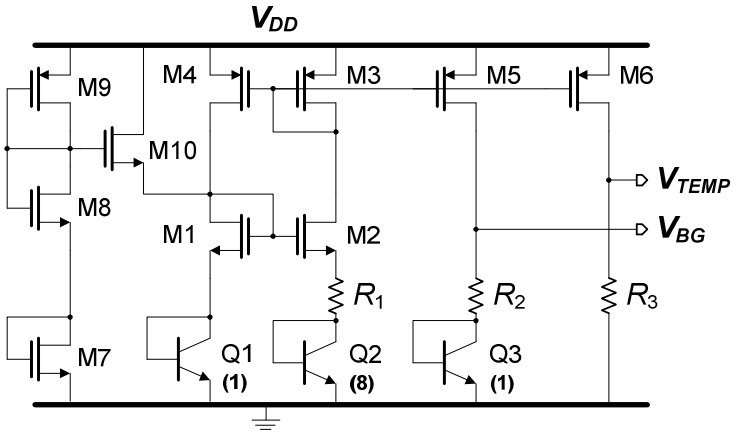


Fig. 3.9 – Schematic diagram of the chip temperature sensor.

A band gap voltage reference V_{BG} providing a temperature independent voltage reference. Thus, the chip temperature can be reliably measured reading the ($V_{TEMP} - V_{GB}$) difference which results independent of the voltage drop over the ground metal paths produced by the high values of currents of the DMOS devices during the heating process. The V_{BG} voltage can expressed as

$$V_{BG} = V_{BE3} + K_{m2}\frac{R_2}{R_1}\frac{kT}{q}\cdot \ln(n) \tag{3.6}$$

where Km2 is the mirror factor of transistors M3-M5. The V_{BG} and V_{TEMP} behaviour on temperature are plotted in Fig. 3.10.

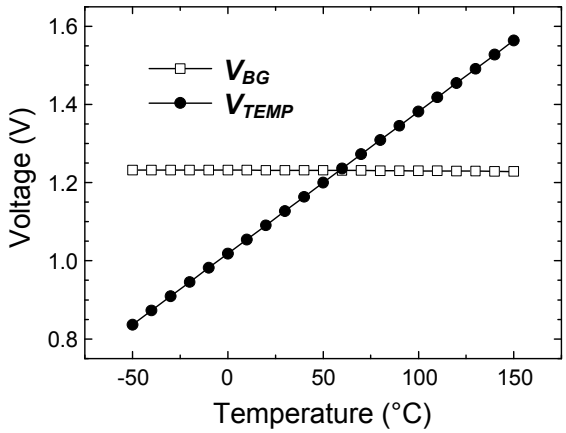


Fig. 3.10 – V_{TEMP} and V_{BG} as function of the operating temperature.

3.1.3. Differential mode readout chain

Details of the differential mode readout chain are given in Fig. 3.11. The chopper amplifier gain can be lowered by paralleling resistor R_A (= 313.2 kΩ) and/or R_B (= 104.4 kΩ) to the output resistor inside the cell (see Fig. 2.2), according to the B25-B26 configuration. The resulting values of the whole chain gain A_D is listed in table 3.I.

B26, B25	A_D
00	1000
01	500
10	200
11	167

Table 3.I – Differential mode chain gain A_D programmable values.

As discussed in section 2.3.2. the output reference voltage of the filter (V_R) has been set to 1.25 V through a V_{DD} (= 3.3 V) resistive voltage divider (R_1 = 38 kΩ, R_2 = 62 kΩ). The actual implementation allows overriding this value through the dedicated pin VOUTREF.

Bits B23 and B24 set the power consumption level of the chopper modulated amplifier and the filter, respectively. At full power mode (B23 = 0, B24 = 0), 6.6 mW and 0.54 mW are drawn from the supply by the chopper amplifier and the filter, respectively. At low power mode (B23 = 1, B24 = 1), power consumption reduces to 1.8 mW and 0.48 mW, respectively. A further power reduction can be obtained lowering V_{DD} from 3.3 V, down to 2.7 V, without affecting input/output dynamics of the critical stages. On the other hand, reducing the chopper amplifier bias current

increases the RTI voltage noise of the latter, depending also on the chopper frequency applied, as discussed in section 2.2. In Fig. 3.12 the plot of the RTI power spectral density $S_{v,rti}$ of the amplifier when choppers are in a fixed position is shown for the two configuration of B23. As expected, only high frequency, i.e. thermal, noise floor is changed, due to the smaller bias current, while low frequency noise maintains unchanged as it only depends on device area. The plot in Fig. 3.12, can be used as a reference for available input noise levels once chosen a chopper frequency (see in section 2.2).

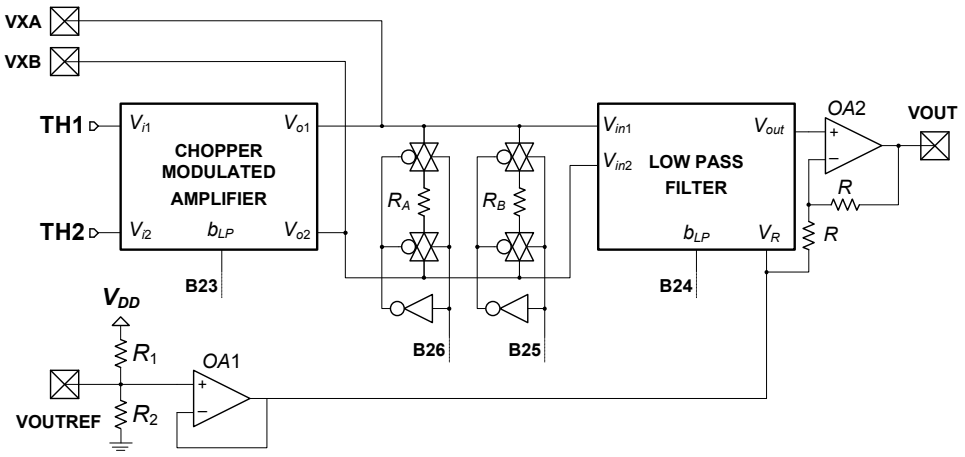


Fig. 3.11 – Block diagram of the complete differential mode read-out chain.

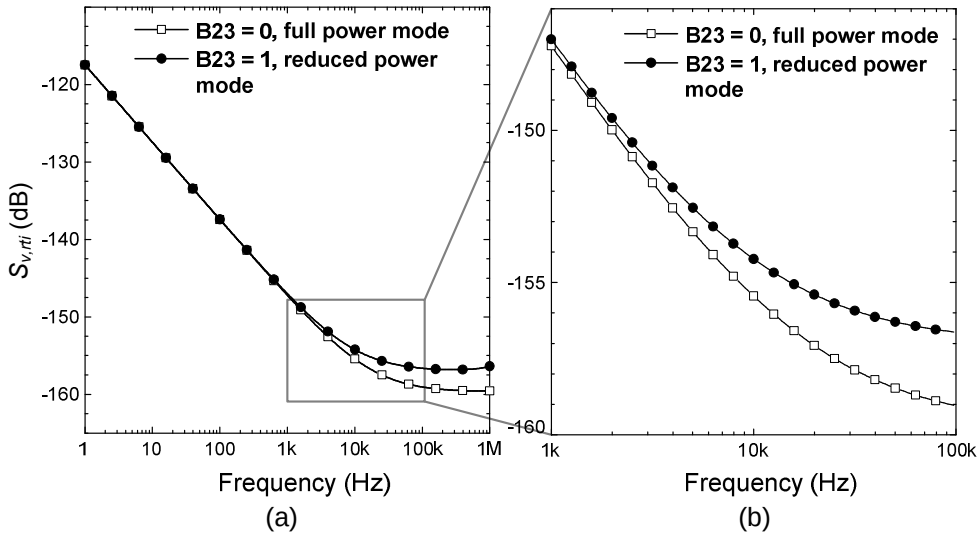


Fig. 3.12 – RTI Power spectral density of the amplifier when choppers are blocked, for the two bias levels set through B23. (b) is an enlargement of (a) in the 1-100 kHz range.

3.1.4. Common mode readout chain

Details of the differential mode readout chain are given in Fig. 3.13. The common mode amplification chain has a separated power pin VDDC, in order to disable power consumption from this block when low pressure operation of the sensor is not needed. The pass gates applied the inputs V_{T1}, V_{T2}, V_{TC} simply disconnects the common mode amplification block when the supply V_{DDC} is not present.
The input of the current driver is directly accessible through pin EXT_DRV. Furthermore, the sensor power driving can operate in an open loop mode, activated by resetting B11, without any external driving, applying a the current driver input two possible default values (V_{DRVH} = 2.3 V, V_{DRVL} = 1.8 V, for V_{DD} = 3.3 V), selectable through B10. For the circuit in Fig. 3.13: R_1 = 87.3 kΩ, R_2 = 42.3 kΩ, R_3 = 157 kΩ.

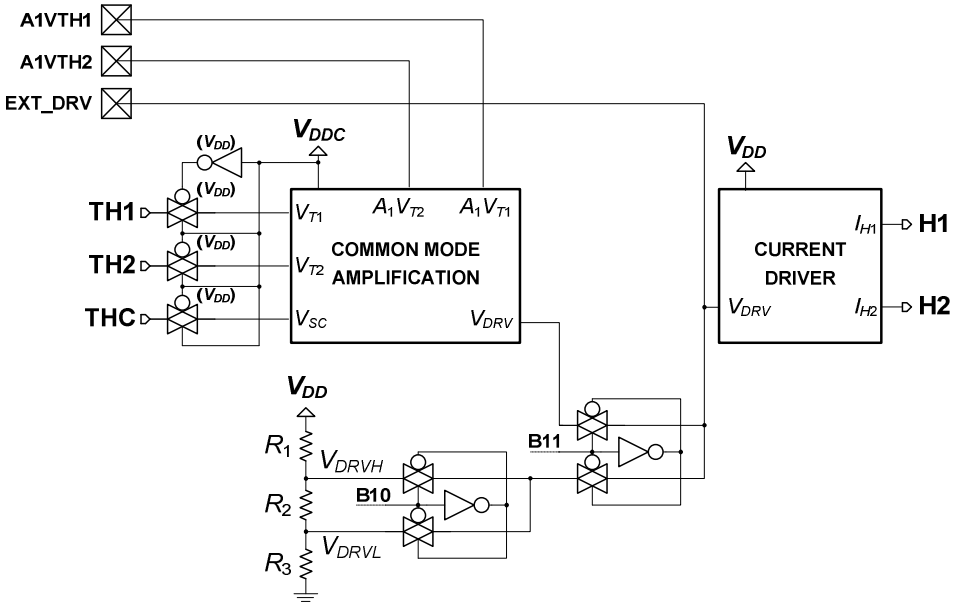


Fig. 3.13 – Block diagram of the complete common mode read-out chain.

3.1.5. Digital communication interface

The digital communication interface provides a link between a serial data channel and the internal registers of the chip holding values of the system parameters. The block diagram is shown in Fig. 3.14, where the inputs W (write), DATA, SCK (serial clock) allow the typical serial communication protocol. The output CO (carry out) can be used for diagnostic purposes. The inputs are equipped with a down resistances allowing, without any external driving, to hold the programmed configuration. Setting (W, DATA, SCK) = (110), the configuration bits (B0-B31) take their default values (B0D-B31D) obtained by simply connections to the ground or to the supply rail. Few defaults are available on external pin (OB23, OB25-OB28), making possible a hard override of their default values, conveniently connecting them through the accessible pins to ground or to the supply rail.

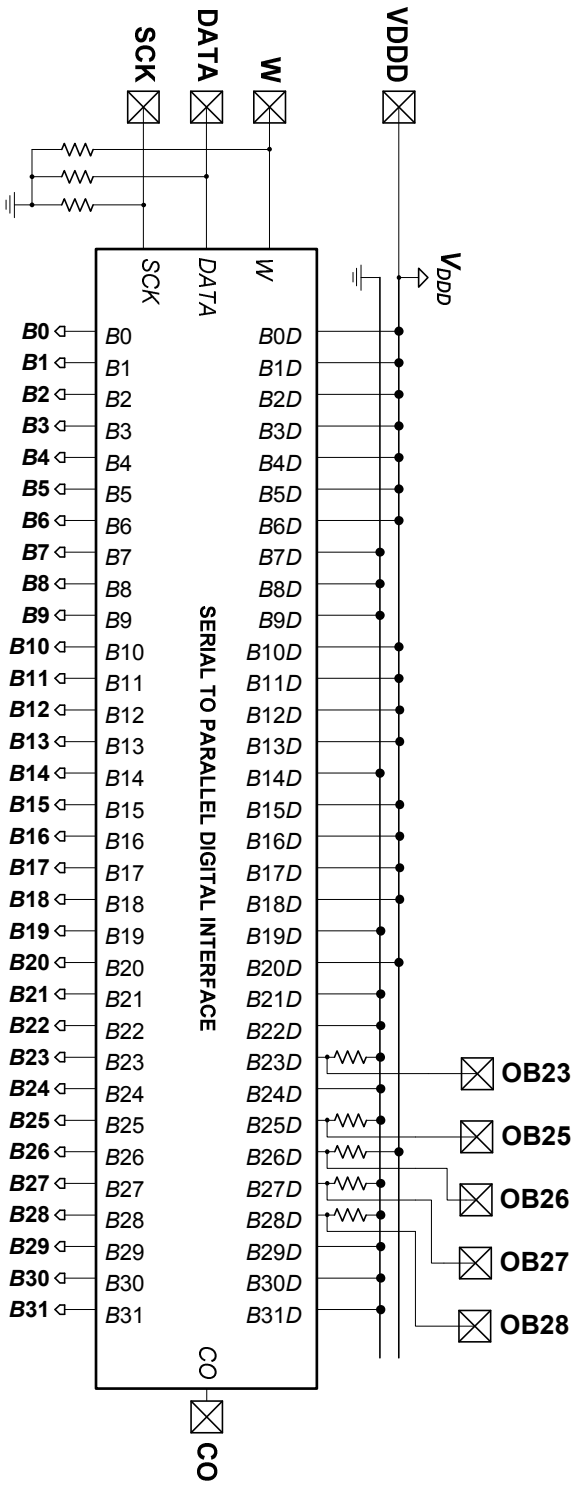


Fig. 3.14 – Block diagram of the complete digital communication interface.

The communication protocol starts with the falling edge of W. As for a common serial-in/parallel-out shift register, each bit is transmitted at the DATA wire and sampled by the positive edge of SCK. The communication protocol ends on the positive edge of W: at this point the bit configuration in the internal shift register is written into the internal hold resister. The modular implementation of circuit in is illustrated in Fig. 3.15, where the single bit slice and connections between bit slices are also shown.
The digital communication interface is designed to be independently supplied (with the pin VDDD), allowing to keep stored the programmed bit configuration even in absence of the other supply sources (V_{DD}, V_{DDC}, V_{DDH}). This feature enables the possibility to implement a smart power save mode, switching off all the analogical circuitry without losing the parameter settings.
Table 3.II resumes the bit default configuration and their respective function.

Bit	Default	Description
B0	1	Current driver output currents unbalance (DW). {B0, B7} ↔ {b_0, b_7}, see eqs. (2.69-2.70)
B1	1	
B2	1	
B3	1	
B4	1	
B5	1	
B6	1	
B7	0	
B8	0	Current driver off (b_{OFF}).
B9	0	Current driver range (b_{CR}), default: low range.
B10	1	Fixed driving voltage range, default: high.
B11	1	Open loop heaters driving enable, default: enabled
B12	1	Internal clock enable, default: enabled.
B13	1	Common mode amplification A_1 settings. {B13, B14} ↔ {b_{A0}, b_{A1}} (see Table 2.VII)
B14	0	
B15	1	Common mode amplification A_2 settings. {B15,…, B19} ↔ {b_{B0},…, b_{B4}} (see Table 2.VII)
B16	1	
B17	1	
B18	1	
B19	0	
B20	1	Common mode amplification V_{CREF} settings. {B13, B14} ↔ {b_{R0}, b_{R1}} (see Table 2.VII)
B21	0	
B22	0	TH sign control: default: convention for positive voltages.
B23	0 (*)	Chopper modulated amplifier bias level selector, default: high
B24	0	LP Filter bias level selector, default: high power.
B25	0 (*)	Differential mode chain global gain selector. Default A_D = 500.
B26	1 (*)	
B27	0 (*)	Sensor selector, default: sensor A
B28	0 (*)	
B29	0	N/A
B30	0	
B31	0	

Table 3.II – Digital interface bit list. Values marked with (*) are overridable.

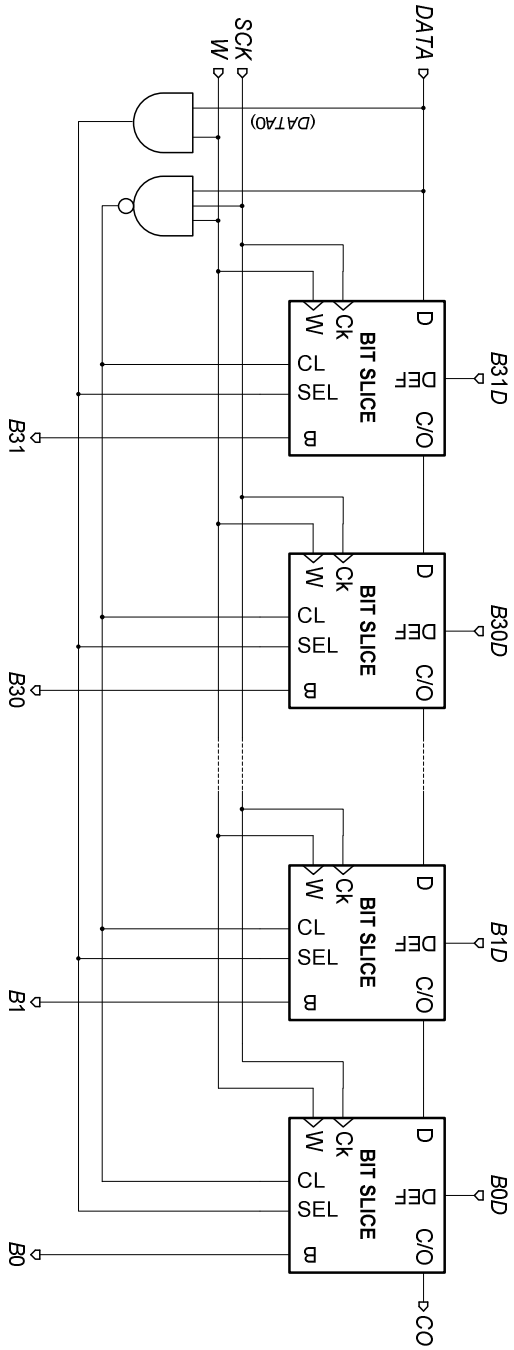


Fig. 3.15 – (On the left) Schematic diagram of the complete digital communication interface. (Bottom) Bit slice schematic diagram.

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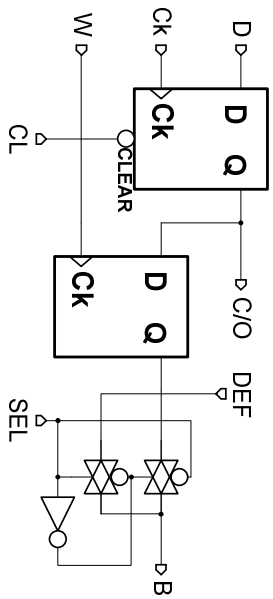


3.2 Chip layout

3.2.1. Sensors layout

The chip has been equipped with three double heater calorimetric flow-meters, described in chapter 1, with the purpose to be capable of multi flow measurements. The layout of each structure is shown in Fig. 3.16. Respects to the previous BCD6 design, some changes have been done. Thermocouples number for each thermopile has been increased from 7 to 10. Thermocouples are formed by n^+-polysilicon/p^+-polysilicon layers as in the previous version. Anyway the same total electrical resistance (45 kΩ) has been maintained by widening the layers forming the thermocouples. This operation should ensure a sensitivity increase of structures with the same noise level as before.
Heaters have are implemented with unsilicided n^+-polysilicon, with the purpose to offer a 2 kΩ electrical resistance. Heaters interconnections through suspending arms are made with siliced n^+-polysilicon layer as it should guarantee a better power efficiency, as discussed in section 1.3.5.
An important performance parameter is the gap between the thermopile tips and the next heater (L_{GAP}): in this case we was conservative with the previous design choice as it was demonstrated by FEM simulations to be a good compromise between range and sensitivity [22]. To have an experimental comparison with simulated results, the chip has been also provided with three single heater structures, as shown in Fig. 3.17, having different L_{GAP} sizes (40.5 µm, 60.75 µm, 81 µm).

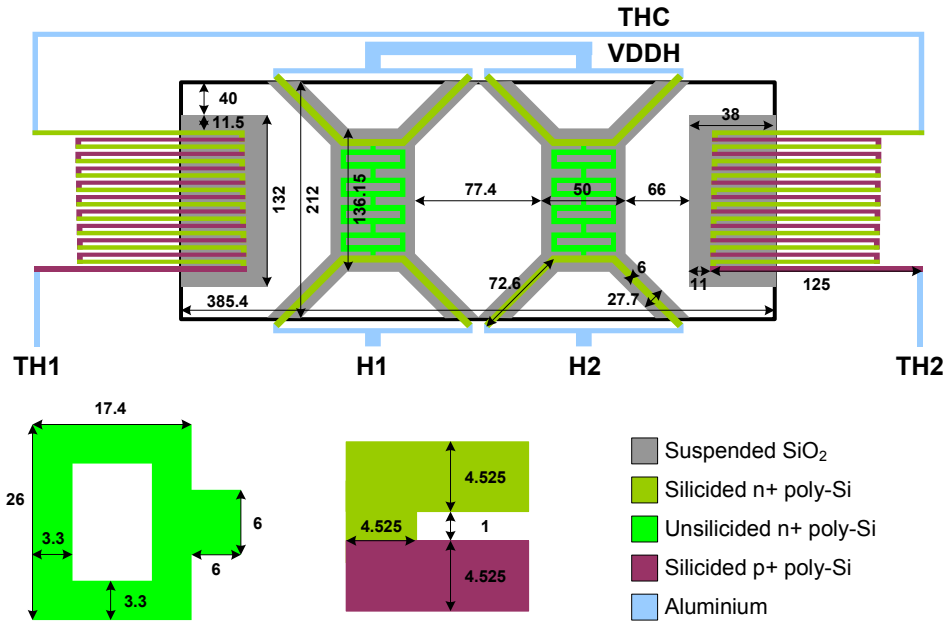


Fig. 3.16 – Schematic top view of the designed double heater BCD6s flow-meter (not to scale). All measures are expressed in µm, but have to be scaled by the shrinking factor 0.92. Details of the heater (bottom left) and the thermocouple (bottom center) geometries are also given.

Figure 3.17 also shows the relative placing of the sensors. They have been put in line and convenient spaced in order to be included in distinct channels with a width of 500 µm. Sensors have been placed in the central part of the chip in order to be included in straight channels and then avoiding the raise of fluid dynamics phenomena leading to severe consequences in sensor characteristics (asymmetry for positive and negative flows and drop of sensitivity), as discussed in section 1.5.

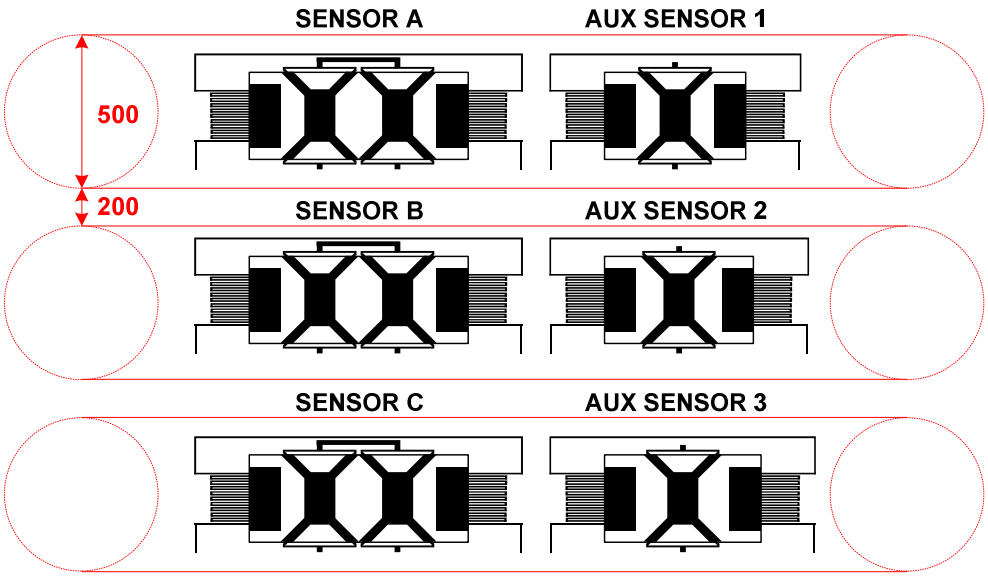


Fig. 3.17 – Schematic top representation of sensors placing on chip. Expected channels geometries are also indicated.

Heaters of sensor B are implemented with unsilicided p^+-polysilicon layers, which, differently from the unsilicided n^+-polysilicon, owns a considerable TCR. This has been done to characterize heaters operative temperature through ΔR measurements.

3.2.2. Pad frame

Pad frame is shown in the chip layout of Fig. 3.18. All the electronic blocks are placed in the top part of the chip, while the central part has been reserved for sensing structures. The chip carry also some other sensing structures from different research groups, not described here. The used pins have been explicitly indicated. Chip dimensions are 3.68 mm × 3.68 mm.

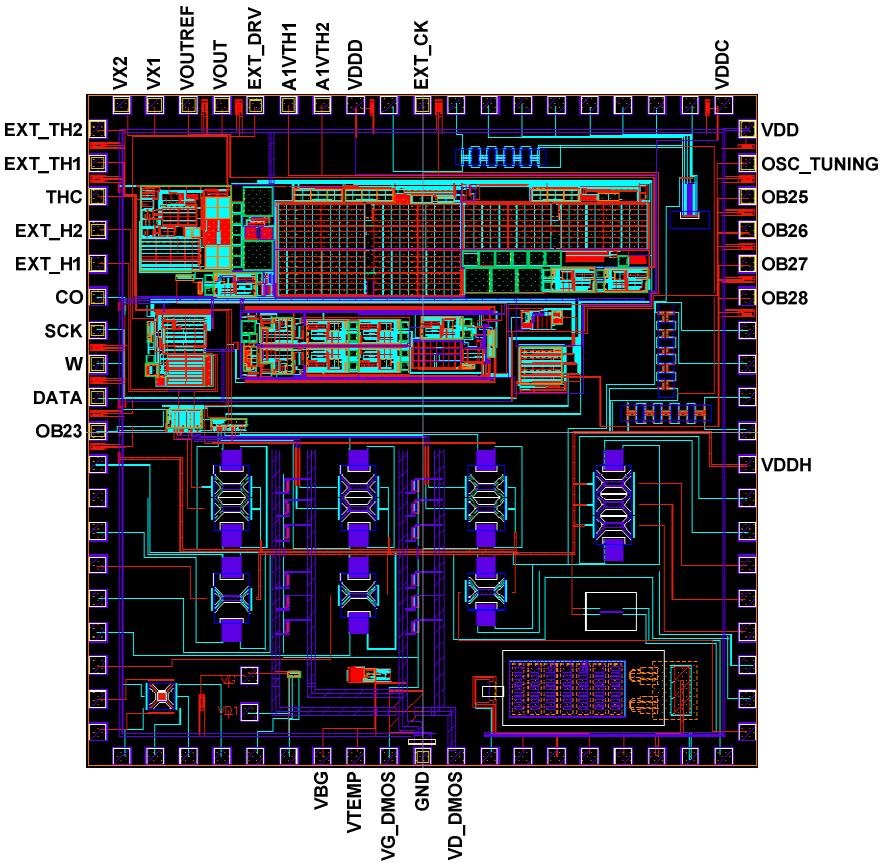


Fig. 3.18 – Chip layout.

3.3 Preliminary tests

Some preliminary tests have been done in order to characterize the chip. The optical photo of the chip is shown in Fig. 3.19, where all the main blocks are also indicated. The double heater sensor structure is shown in Fig. 3.20.
For the tests, a voltage source of 3.3 V has been used. Chopper frequency has been set to 20 kHz. The output voltages of the chopper amplifier and at the end of the all differential mode amplification chain are presented in Fig. 3.21 and 3.22, respectively. The characteristics have been obtained by sweeping the differential input voltage through terminals EXT_TH1, EXT_TH2 by the means of a pair of source/monitor units (SMUs). The expected linearity ranges are confirmed. The visible asymmetries in the input range of characteristics in Fig. 3.22 are due to the low level of the reference voltage chosen for this test (V_{OUTREF} = 1.25 V). Obviously it can be varied in order to better exploit the output voltage linearity range which is included between 0.25 V and 2.95 V. Characteristics are maintained for a applied input common mode voltage between 1.6 V and 2.6 V. Gain values for B25, B26 configurations are reported in table 3.III, together with the respective input linearity range.

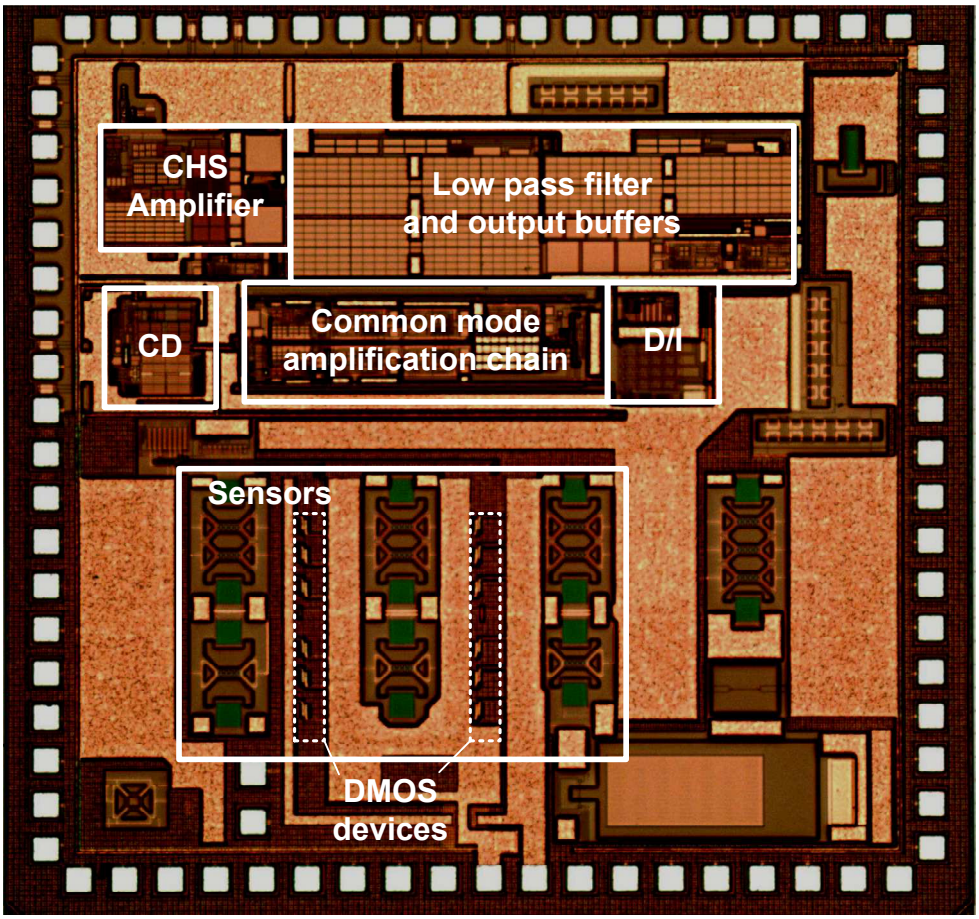


Fig. 3.19 – Optical photograph of the chip. Block CD is the digitally controlled current driver, block D/I is the digital communication interface.

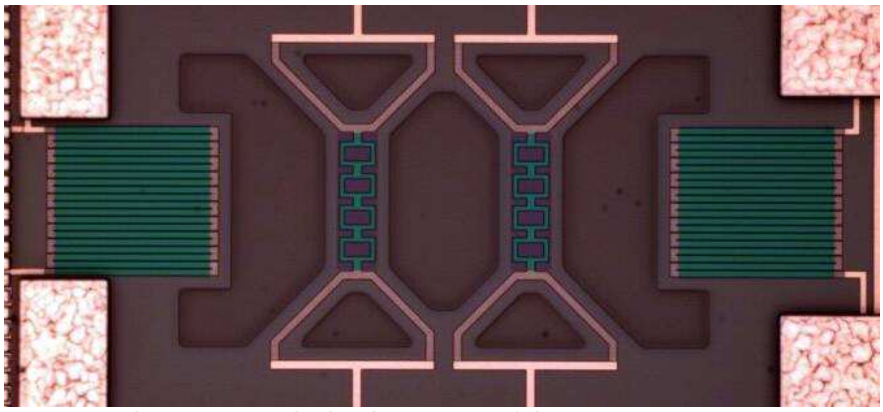


Fig. 3.20 – Optical enlargement of the sensor structure.

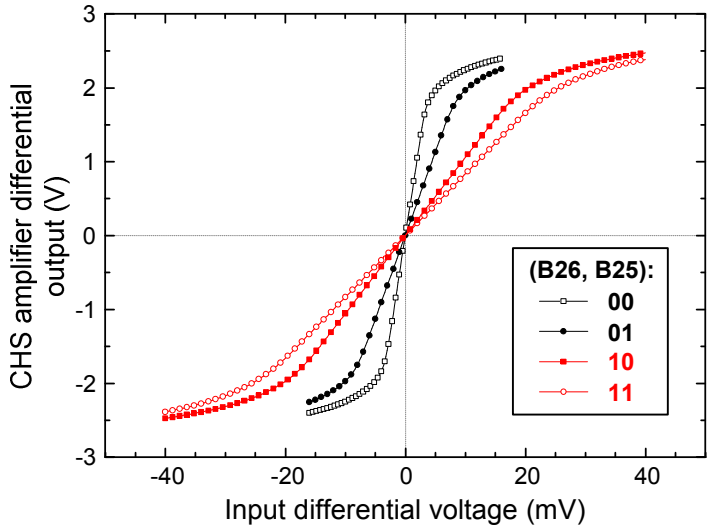


Fig. 3.21 – Chopper amplifier output voltage for different gain configurations.

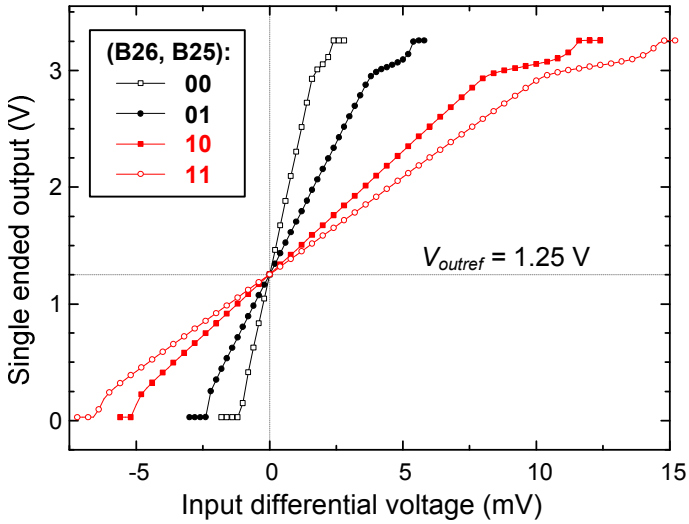


Fig. 3.22 – Differential mode amplification chain output voltage for different gain configurations.

B26, B25	CHS amp	input range (mV)	Diff. mode chain	input range (mV)
00	525	±2.2	1050	–0.8, +1.2
01	226	± 6	451	–2.2, +3.6
10	105	± 6	210	–4.6, +8
11	82.7	±18	165	–5.8, +10

Table 3.III – Measured gains for the differential mode chain.

The low power operation of the differential mode chain has also been tested, repeating the above experiments and setting bits B23 and B24. Results, shown in Figs. 3.23 and 3.24, confirm that, as expected, characteristics are maintained within the respective linear ranges. Power consumption was reduced from 4.5 mW in the high power mode (B23, B24 = 00) down to 3.5 mW for low power mode (B23, B24 = 11).

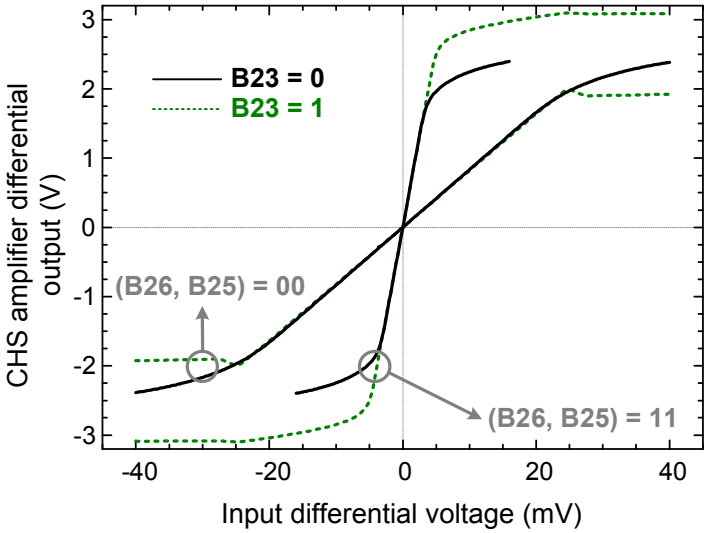


Fig. 3.23 – Comparison of chopper amplifier output voltages for the high power (B23 = 0) and low power (B23 = 1) chopper configuration.

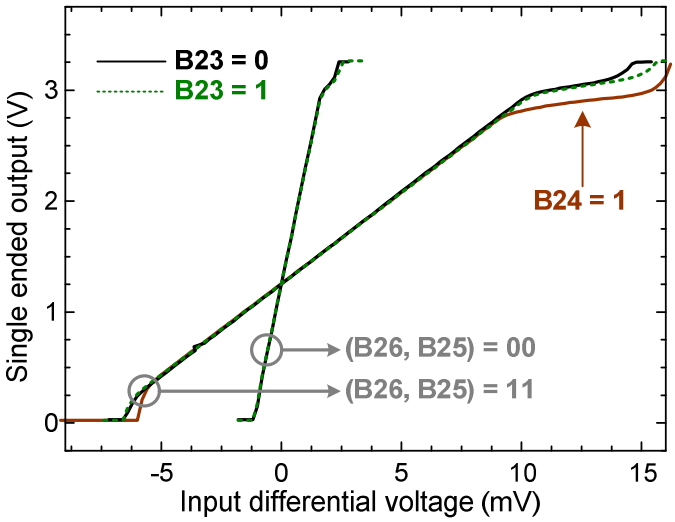


Fig. 3.24 – Comparison of differential mode chain output voltage for the high power (B23 = 0) and low power (B23 = 1) chopper configuration. In the last case, the characteristics for the filter low power configuration (B24 = 1) is also shown.

The characteristics of the instrumentation amplifiers and the first stage of CDS amplifier in the common mode read-out chain have been also tested *vs.* the differential voltage applied. Fig. 3.25 shows the output voltages at terminals A1VTH1, A1VTH2 for the various gain configurations set by B13, B14.

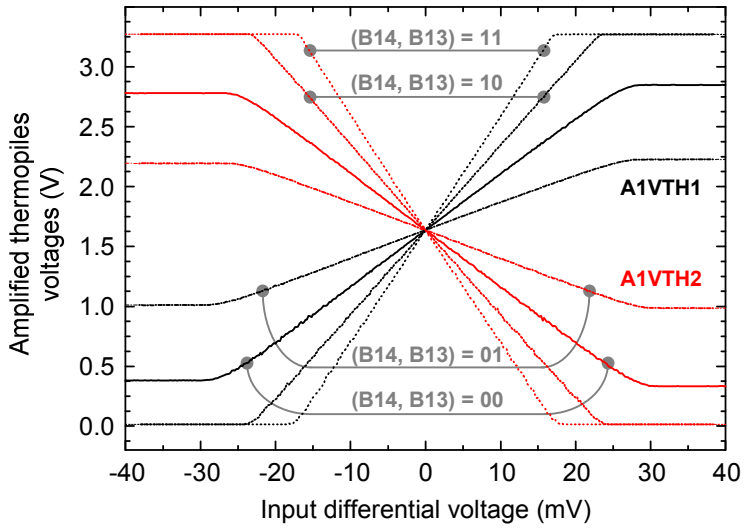


Fig. 3.25 – Voltages from the output terminals A1VTH1, A1VTH2, as a function of differential voltages, for various configuration of the gain A_1.

As a very preliminary test, the interface has been connected to an external sensor. In this test we used the sensor presented in section 1.4. Figure 3.26 shows the output characteristics for N_2 flow rate in the range of ±10 sccm, and for two configurations of the differential mode gain. To the output voltage has been subtracted the rest level V_{refout}.

Noise of the differential mode chain has been also approximately estimated with this arrangement, in the 0-10 Hz bandwidth of a multimeter connected to the output terminal VOUT. For a total amplfification of 1050, the observed peak-to-peak noise band was within ±200 μV. The sensor thermopiles, having a resistance of 80 kΩ, produce an RMS noise of 115 nV in the same bandwidth, which amplified by 1050, gives about 120 μV of RMS output noise. Considering a crest factor of 4 we conclude that the DR range of the sensor itself is preserved by the amplification chain, which was one of the most important goals in this design.

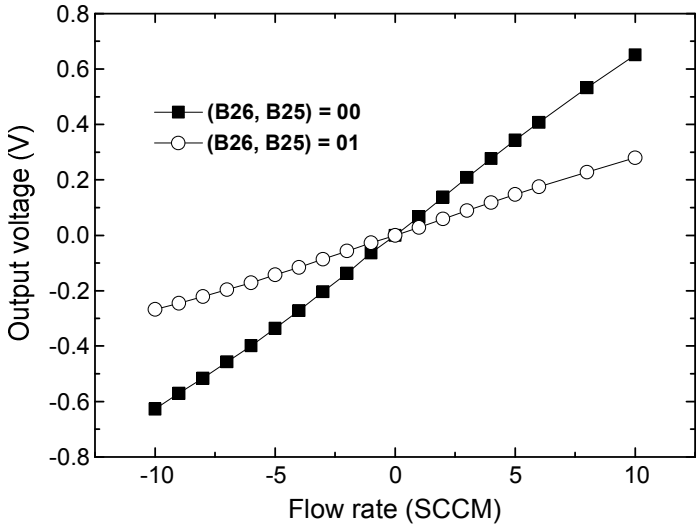


Fig. 3.26 – Characteristics of the differential mode read-out interface connected to the flow-meter of Fig. 1.30.

4. DESIGN OF LOW POWER INTEGRATED INTERFACES FOR CAPACITIVE SENSORS

The design of low power integrated interfaces for capacitive sensors took place in a collaborated activity with Dr. Nicolò Nizza within the Microsystem research group of the Information Engineering Department of the University of Pisa. In this chapter, after a short introduction on capacitive sensors and their read-out methods, an innovative approach, based on capacitance to pulse width modulated (PWM) signal conversion will be presented, extensively discussed also in [52]. The circuit has been designed jointly and it was fabricated using 0.32 μm/ 3.3 V CMOS devices from the BCD6s process of STMicroelectroncs demonstrating very interesting measured performances in terms of excellent linearity, temperature drift (300 ppm/ºC), of power consumption (84 μW from a power supply of 3.3 V), and excellent rejection of interconnection parasitic capacitances. The dynamic range of such circuit is quite low, resulting in 48 dB measured from a not-optimized prototype. Nevertheless some techniques, aiming to improve the resolution capabilities and the accuracy of the interface, are possible. The final part of this chapter is purposed to describe such techniques and discuss the fundamental trade-offs in the design.

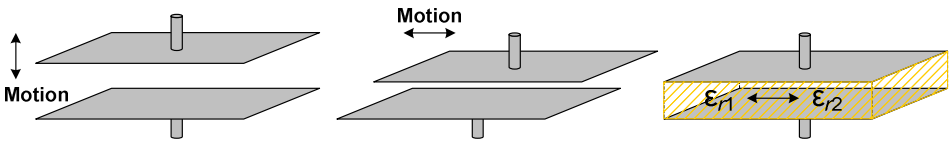
4.1 Integrated capacitive sensing

4.1.1. Capacitive sensors

In the electromagnetic field, the capacitance, expressed in farad unit, is the ability of a body to hold an electrical charge (coulomb), when an electric potential (volt) is impressed on it. An ideal capacitor is a device with two accessible perfectly conducting electrodes, separated by a dielectric material. This device is completely characterized by the capacitance parameter only, which depends on capacitor geometry, and on the dielectric properties of the inner materials.
For the sake of clarity, let us consider a simple parallel plate structure similar to those in Fig. 4.1. Ignoring fringing fields, the capacitance of this simple structure can be expressed as

$$C(\varepsilon_r, A, d) = \frac{\varepsilon_r \varepsilon_0 A}{d} \tag{4.1}$$

where ε_r is the relative permittivity of the material, ε_0 is the vacuum permittivity between the plates, A is the area of overlap between the electrodes, and d is the separation between the electrodes. In a capacitive sensor, same physical quantity cause the variation in one of these parameter, reflected in a capacitance variation as clearly shown in eq. (4.1).
For example, displacement of a movable electrode can be caused by an external force such as pressure, or deriving from acceleration. Alternatively, the dielectric properties of the medium between the electrodes can be influenced by other quantities such as chemical concentration.



(a) (b) (c)

Fig 4.1 – Parallel plate capacitive sensor where (a) d and (b) A is varied by a displacement of the moving electrode; in (c) the relative permittivity is varied.

Figure 4.1(a) shows the simple case where the lower electrode is fixed and the upper electrode moves. In this case the separation *d* is changing and hence the capacitance varies in a nonlinear manner. Figure 4.1(b) depicts a device where the separation is fixed and the area of overlap is varied. In this configuration, there is a linear relationship between the capacitance and area of overlap. Figure 4.1(c) shows a structure where the dielectric material is affected by a variation of relative permittivity.

In integrated technologies, differential capacitive structures are diffusely employed as a general method to prevent the measure quantities to be heavily affected by process corners variations, material aging, and temperature variation effects. Let us consider the structure shown in Fig. 4.2, implementing a differential capacitive sensor; E1 and E3 are fixed electrode, while E2 is free to move in a parallel direction (along the *x* axis).

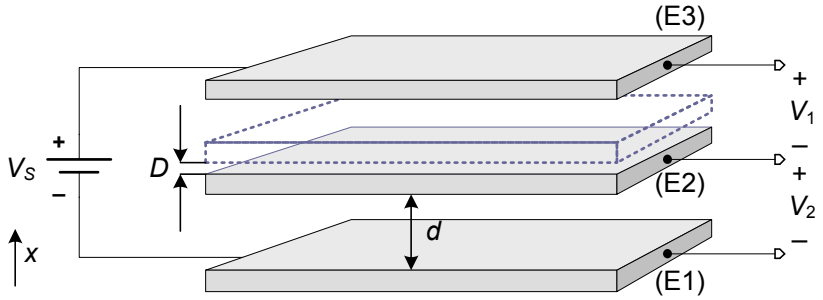


Fig. 4.2 – Schematic representation of a differential capacitive sensor. A supply voltage VS is applied across the fixed electrodes E1 and E3, while E2 is free to move along the x axis. The output signal is given by the voltage difference $V_2 – V_1$.

Two capacitances C_1, C_2 can be calculated between the central electrode and the fixed electrodes E1, and E3 respectively:

$$C_1 = C \cdot \frac{d}{d + D}; \tag{4.2a}$$

$$C_2 = C \cdot \frac{d}{d - D} \tag{4.2b}$$

where *C* is the capacitance calculated, following eq. (4.1), for zero displacement (*D* = 0) of E2. The differential output voltage can be easily calculated as

$$V_1 - V_2 = \frac{C_2 - C_1}{C_1 + C_2} \cdot V_S = \frac{1}{2}\left(\frac{1}{1 - D/d} - \frac{1}{1 + D/d}\right) \cdot V_S \cong \frac{D}{d} \cdot V_S \qquad (4.3)$$

for $D << d$. It is worth noting that common mode effects, i.e. effects acting on both C_1 and C_2 in the identical way, such as C spreading with process or eventual temperature dependence of ε, have been ruled out from eq. (4.3).
A variety of physical quantities can be transformed into capacitance variations, making capacitive sensing particularly important in micro-electro mechanical systems (MEMS). Among all the physical quantities that can be sensed we mention pressure, acceleration and humidity. Furthermore, capacitive sensors are very attractive thanks to their zero static power consumption and their low temperature dependence. Capacitor structures are relatively straightforward to fabricate and membrane-type devices are often used as the basis for pressure sensors and microphones [53, 54]. An example of pressure sensor is schematically represented in Fig. 4.3. More elaborate structures such as that shown in Fig. 4.4, formed by a suspended proof mass, are also used for integrated accelerometers where providing interdigitated capacitors both provide the sensing and the forcing (through capacitive actuators) functionality [55]. For such structures, fringing field effects cannot be ignored, and their capacitance assumes a more complex expression than that in eq. (4.1), although the use of differential structures is still a valid technique for common mode variations/disturbances rejection. Integrated capacitive sensors based on ε variation have been also implemented: in [56] a humidity sensor based on this principle is presented.

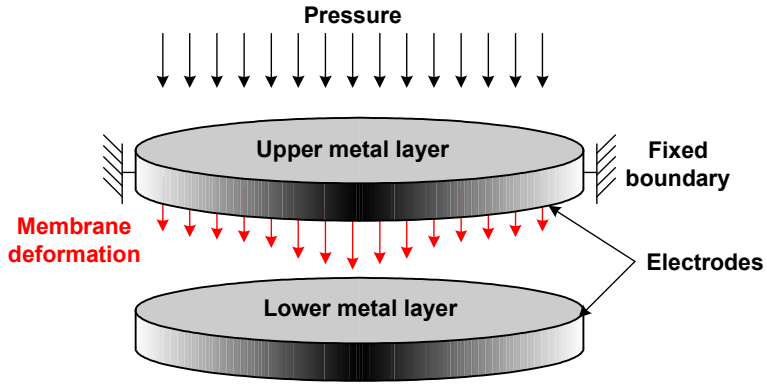


Fig. 4.3 – Schematic representation of a circular membrane pressure sensor.

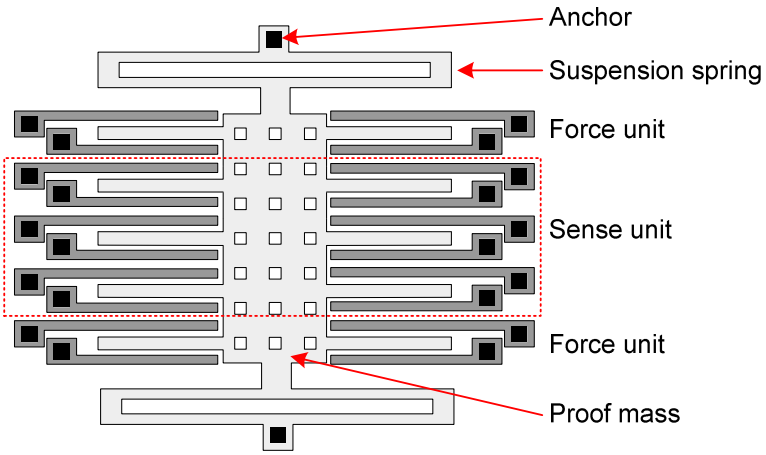


Fig. 4.4 – Typical layout of a proof-mass structure for integrated silicon accelerometers.

4.1.2. Integrated interfaces for capacitive sensing

Integrated accelerometers and pressure sensors are probably the most successful examples of MEMS (Micro Electro Mechanical Systems). Practically the totality of integrated accelerometers and a large fraction of pressure sensors are based on capacitive sensing of either a seismic mass or a membrane. Capacitive sensors offer high relative sensitivity, small temperature dependence, virtually negligible power consumption, and very low level of intrinsic noise. On the other hand, very small capacitance variations have to be detected, typically in the femto-farad range, requiring the interface to be developed carefully designed and tailored to the sensor in order not to degrade the sensor advantages mentioned above.

Systems-on-chip are diffused arrangements where the electronics circuits share the same bulk with the sensing structures. Sometimes, it may result economically more advantageous to process the electronics and the sensors on separated chips [57], each of those with its dedicated process, and making a final assembly on a same package (system-on-package). In this case, conspicuous parasitic capacitances are introduced through connections between the sensor chip and the electronic interface. Insensitivity to parasitic is then an essential requirement for the latter.

Well known approaches for capacitive sensors interfaces are: impedance meters (IM), switched capacitor charge amplifiers (SCCA), and capacitance to frequency converters (C-to-f).

Impedance meter – The IM technique is employed, for example in the Analog Devices ADXL50 [58]. Figure 4.5 shows a simplified schematic diagram of the latter, where a differential sensor structure, such as that of Fig. 4.2 is used.

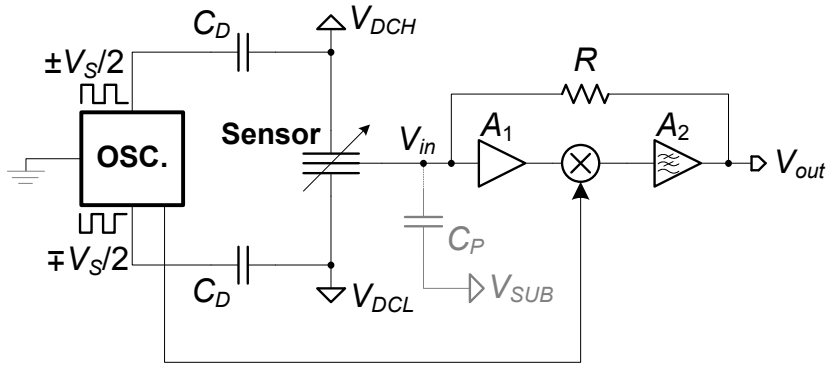


Fig. 4.5 – Block diagram of ADXL50 capacitive sensor interface.

The sensor is typically stimulated by a square wave voltage provided by the oscillation block. Considering the parasitic capacitance C_P, equation (4.3) can be rewritten as

$$v_{in} = \frac{\Delta C}{C_0 \cdot \left(1 + \frac{C_P}{2C_0}\right)} \cdot \frac{v_S}{2} + \frac{C_P}{C_0 \cdot \left(1 + \frac{C_P}{2C_0}\right)} \cdot v_{SUB} \qquad (4.4)$$

where C_0 is the rest capacitance, ΔC is the capacitance difference to be measured, while C_P and V_{SUB} are the parasitic capacitance and the substrate voltage respectively. It is evident from eq. (4.4) the detrimental effects of C_P: (i) it reduces the effective sensor sensitivity; (ii) it allows disturbance injection from the substrate. The signal level at this point is of few microvolt, starting from a V_S in the order of one volt, thus an amplification stage is needed. It is worth noting that the signal carried by ΔC, passes through the amplifier in a modulated fashion as it occurs in a chopper modulated scheme. A synchronous demodulation stage is then provided to bring the signal back to the base band. The capacitance difference ΔC is proportional to the displacement, but only for small values of the latter as already discussed. The ADXL50 uses a negative feedback control loop through resistor R to make sure that the movement of the mass is kept small so that the above expression remains correct. Furthermore a DC path for the sensor central electrode is ensured.

Switched capacitor charge amplifiers – The best dynamic range is obtained using switched capacitors charge amplifiers. Very high dynamic ranges have been demonstrated to be achievable with the scheme shown of Fig. 4.6, extensively discussed in [59]. On the other hand, charge injection, kT/C noise and mismatching between C_{fb1}-C_{fb2} elements impose rather complicated, fully-differential architectures with multiple input and output common mode stabilization, and digital trimming circuits.

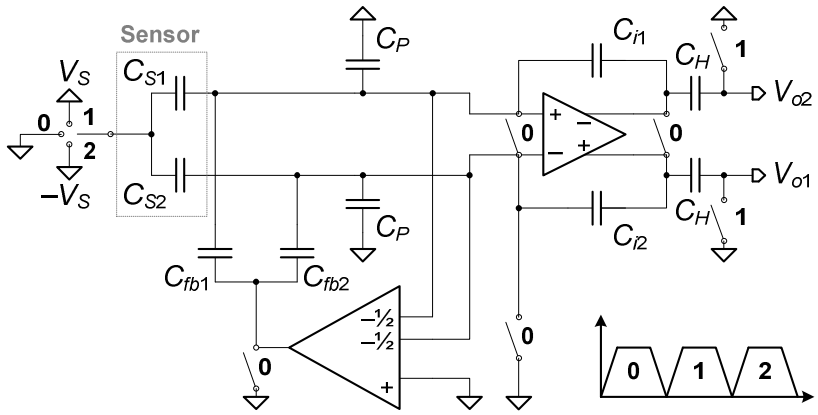


Fig. 4.6 – Block diagram of a fully differential capacitive interface based on charge amplifiers.

The impact of opamp noise can be evaluated considering the simplified scheme reported on Fig. 4.7. The output voltage, at the end on phase 2, can be easily calculated as

$$V_{out} = \frac{C_1 - C_2}{C_i} \cdot \Delta V_S = \frac{\Delta C}{C_i} \cdot \Delta V_S \tag{4.5}$$

Considering the full-scale capacitance difference ΔC_{FS}, we obtain

$$V_{out,FS} = \frac{\Delta C_{FS}}{C_i} \cdot \Delta V_S \tag{4.6}$$

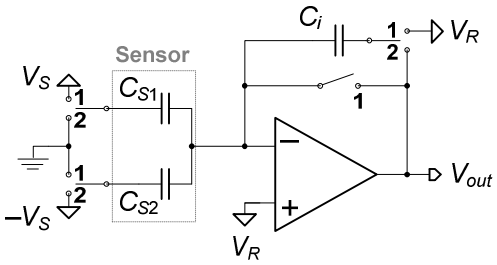


Fig 4.7 – Schematic of a simplified switched capacitor interface for noise analysis.

The input referred power spectral density of the opamp stage can be reduced, through careful design to the only contribution of the input differential pair

$$\frac{\left\langle V^2_{n\_OPAMP,in} \right\rangle}{\Delta f} = \frac{16}{3} \cdot \frac{kT}{g_m} \tag{4.7}$$

In the above equation, flicker noise has not been considered as we suppose that the system is operating at frequency higher enough than the thermal-flicker corner, so that only the thermal contribution dominates. The above expression does only express the opamp PSD noise; as opamp noise has a bandwidth is greater than

the sampling frequency, aliasing occurs, resulting in a fold-over of 2*n* replicas of the PSD in eq. (4.7) in the baseband, where, indicating with B_{OPAMP} and f_{CK} the opamp bandwidth and the sampling frequency, respectively, we have:

$$n = \frac{B_{OPAMP}}{f_{CK}} \tag{4.8}$$

Hence, the output noise power can be estimated

$$\left\langle V_{n,out}^2 \right\rangle = \frac{32n}{3} \cdot \frac{kT}{g_m} \cdot A_i^2 B \tag{4.9}$$

where we supposed to observe the $V_{n,out}$ phenomena only in the strictly necessary sensor bandwidth *B*. The amplification A_i is simply given by:

$$A_i = 1 + \frac{C_1 + C_2}{C_i} \tag{4.10}$$

Now, some substitutions can be done to eq. (4.9), considering the thermal voltage $V_{TH} = kT/q$, and expressing the input couple g_m as a function of I_D and the overdrive voltage ($V_{GS} - V_t$):

$$\left\langle V_{n,out}^2 \right\rangle = \frac{16n}{3} \cdot \frac{V_{TH} \cdot (V_{GS} - V_t)}{I_D} \cdot A_i^2 B \tag{4.11}$$

Equations (4.5), (4.6) and (4.11) can be combined to find an expression of the dynamic range of the circuit in Fig. 4.7

$$\mathrm{DR} = \left(\frac{\Delta C_{FS}}{\Delta C_{\min}} \right)^2 = \frac{V_{out,FS}^2}{\left\langle V_{n,out}^2 \right\rangle} = \frac{3}{16n} \cdot \frac{\Delta V_S^2}{V_{TH}(V_{GS} - V_t)} \cdot \left(\frac{\Delta C_{FS}}{C_i + C_1 + C_2} \right)^2 \cdot \frac{I_D}{qB} \tag{4.12}$$

Equation (4.12) clearly demonstrates how the opamp noise can be reduced by incrementing the input transistors biasing current I_D. The term *qB*, having the unit dimension of a current also, has a very low value in practical designs. For example for *B* = 30 kHz, *qB* is about 4 fA. On the other hand *n*, and the capacitance ratio impose the use of a relatively large I_D, only partially mitigated by the voltages ratio term. A typical design situation is achieved by lowering the thermal noise contribution up to the point that the *kT*/*C* noise is the only contribution to limiting the dynamic range. With the CDS charge approach, a dynamic range as high as 89 dB, with 27 mA drawn from the power supplies have been demonstrated [59].

Capacitance to frequency converters – C-to-f converters are characterized by extremely low power consumptions, on the order of few micro-watt, but present heavy temperature drift in sensitivity and marked non linearity. Examples are illustrated in Fig. 4.8: in (a) a simple relaxation oscillator [60], similar to that described in section 3.1.1. is employed, while in (b) a simple ring oscillator is shown [61], where the sensor C_S is placed in parallel with one of the intrinsic capacitances C_L of the ring. It is worth noting that in these schemes, the differential sensor structure is not used, so that the drift of sensor characteristics adds up to the drift of the interface characteristics, resulting in a very poor accuracy on the measurements.

(a)

(b)

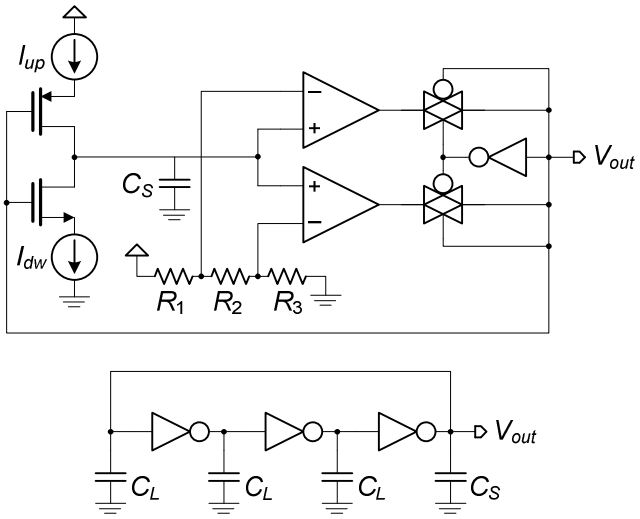


Fig. 4.8 – Schematic diagram of a C-to-f converter: (a) based on relaxation oscillator [60], and on ring oscillator [61]

4.2 Capacitive to PWM signal converters

4.2.1. C-to-PWM converter

In this section, an alternative and original method based on capacitance to pulse width conversion (C-to-PWM), is illustrated. The circuit produces a periodic pulse at the output: the period is set by an external clock, while the duration of the pulse is proportional to the sensing capacitor. With respect to the previously discussed solutions, some peculiar advantages can be pointed out:

(i) the overall integration of the system on chip, without external components, is easily achievable differently from the classic IM, where large decoupling capacitors are needed;
(ii) differently from SCCAs, no aliasing of the high frequency noise occurs, relaxing noise constraints and allowing very low power operation;
(iii) the circuit is synchronized by an external clock, making interfacing with microcontrollers easier than for C-to-f converters. The temperature drift that can be obtained is much lower, and characteristics are much more linear.

Pulse width modulated signals can be transmitted over moderately noisy and channels with non linear characteristics, such as RF or optical links. Furthermore, a PWM signal can be easily read by a low cost microcontroller or converted into an analog signal using only a low pass filter. In the former case the information is extracted by digitally sampling the periodic waveform and counting the number of high bits over the total samples in a period. The same function is performed

analogically by a simple moving window low pass filter, setting the integration window equal to the signal period (or multiples of it in case of averaging is wanted) and (analogically) sampling the filter output at the end of each time frame.

Principle of operation of a C-to-PWM converter. The block diagram of the system is shown in Fig. 4.9(a) where the differential sensor structure is represented by the two capacitors C_R and C_X. The quantity to be acquired is the difference $\Delta C = C_X - C_R$.

CK is a clock signal with 50 % duty cycle, having a period T_{CK} and a frequency f_{CK}. The output signal, indicated with *P* is a sequence of pulses of frequency f_{CK} and duration τ proportional to ΔC. For correct operation of the interface, ΔC should equal or greater than zero. This can be easily achieved in a differential sensor structure where reference C_R is implemented with a dummy structure, i.e. insensitive to the physical quantity to be sensed.

Block RG (ramp generator) produces a triangular waveform $V_S(t)$, synchronous with the clock signal, while block CA is a differential current amplifier with gain 1/2. CMP is a low hysteresis comparator, while CM1 and CM2 are simple chopper modulators of the same kind of that discussed in section 2.1.

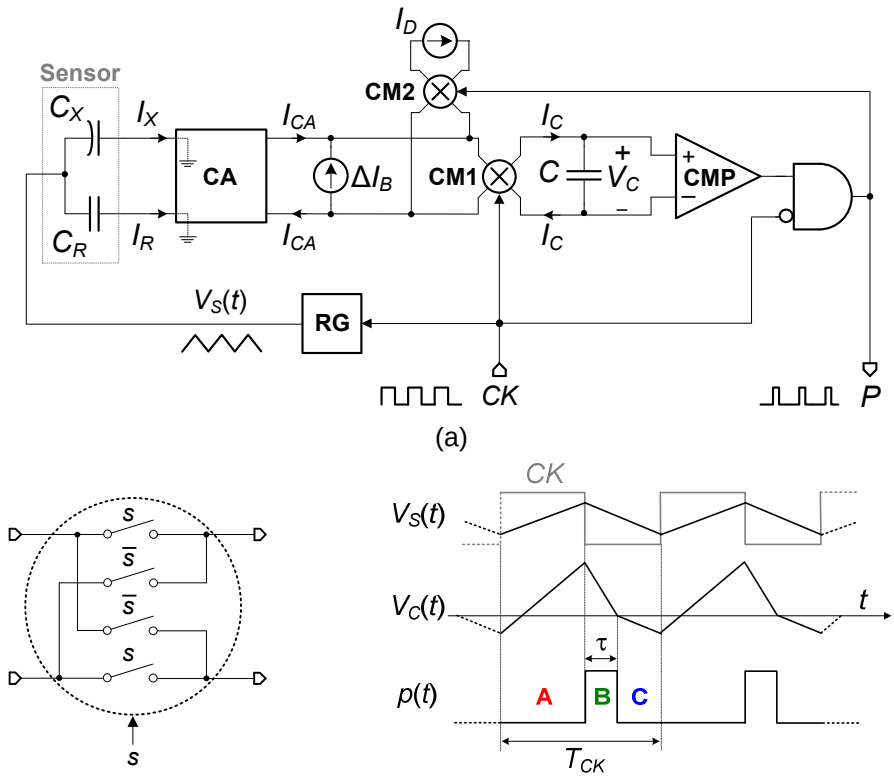


Fig. 4.9 – (a) C-to-PWM schematic block diagrams: (b) functional view of the chopper modulators CM1, CM2, (c) ideal waveforms in the circuit.

Capacitor C, is charged by currents I_{CA}, I_D and ΔI_B, with a sign depending on M1 and M2 state. Currents I_D and ΔI_B, are constant and chosen to satisfy the following conditions:

$$I_D \geq \max\left|I_{CA}\right|; \tag{4.13a}$$

$$\Delta I_B > I_D + \max\left|I_{CA}\right| \tag{4.13b}$$

Clearly, for the waveform V_C to be stationary, the net charge accumulated on C over a clock period (T_{CK}) should be zero. To simplify the comprehension of the measurement cycle, the ideal waveforms in the circuit are shown in Fig. 4.9(c). In the following analysis, the input resistance of CA will be considered zero; this point is important to achieve low temperature dependence and will be addressed in next section. The expression of current I_{CA} is then:

$$I_{CA} = \frac{I_X - I_R}{2} = \frac{1}{2}\frac{dV_S}{dt} \cdot \Delta C\,. \tag{4.14}$$

Note that I_{CA}, which is proportional to ΔC, changes sign at half the clock cycle due to the slope inversion of V_S. However, M1 produces another sign reversal at the same time, so that the charge contribution of I_{CA} is always positive and given by:

$$Q_{CA} = \frac{\Delta C}{2} \cdot \int_0^{T_{CK}/2} \frac{dV_s}{dt} dt - \frac{\Delta C}{2} \cdot \int_{T_{CK}/2}^{T_{CK}} \frac{dV_s}{dt} dt = \Delta C \cdot \Delta V_S\,. \tag{4.15}$$

where ΔV_S is the peak-to-peak amplitude of V_S. On the other hand, the contribution of ΔI_B changes sign at half the clock cycle, so that, the net charge accumulated over a whole clock period is zero. The role of this current is to make V_C increase on the first half clock cycle and decrease on the second one, regardless of the value and sign of I_D and I_{CA}. This is guaranteed by the conditions (4.13b). For this reason, V_C reaches its maximum at the end of the first half clock cycle. As represented in Fig. 4.9(c) we will assume now that the maximum is positive and discuss this point at the end of this section. Considering the effect of CMP and of the cascaded logical gate, the output signal (P) turns on at the beginning of the second clock half cycle, as shown in Fig. 4.9(c).

The contribution of I_D is negative in the first half clock period, due to the sign reversal operated by CM2. At the end of this period, both CM2 and CM1 change state, so that the contribution continues to be negative. Finally, when V_C crosses the zero and CMP changes state, the contribution of I_D becomes positive. Summing up the contributions over the three phases indicated with A, B and C in Fig.1(c), the net charge contribution of I_D is then:

$$Q_D = -2\tau I_D\,. \tag{4.16}$$

Equating to zero the total charge accumulated over a period, (i.e. $Q_D + Q_{CA}$) we obtain the pulse duration:

$$\tau = \Delta C \cdot \frac{\Delta V_S}{2I_D}\,. \tag{4.17}$$

It is easy to show that the system reaches the steady condition regardless of the initial state. Indeed, if the maximum of V_C is negative, CM2 stays in inverted state and, similarly to ΔI_B, I_D gives no charge contribution. Therefore, the unbalanced positive contribution of I_{CA} progressively raises the V_C waveform reaching the

situation in Fig. 4.9(c). On the opposite side, if V_C was always positive, the I_D contribution would be negative over the whole clock period and, due to condition (4.13a), V_C would progressively decrease reaching again the steady situation.

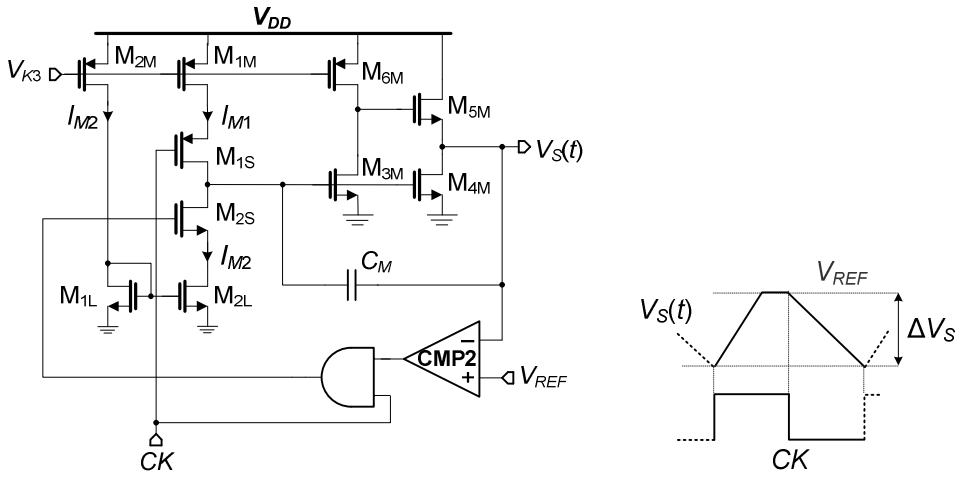


Fig. 4.10 – Schematic view of (a) the RG block and (b) $V_S(t)$ waveform.

Blocks implementation – The RG simplified schematic view is shown in Fig. 4.10. The circuit is composed of a Miller inverting integrator, made up of M_{3M}-M_{6M}, and two current sources M_{1M}, and M_{2M} that can be connected to the integrator input through M_{1S} and M_{2S} respectively.
In the first clock half cycle (CK = 1), M_{2L} draws the current I_{M2} from the integrator, so that V_S increases at a constant rate. Let us suppose that V_S reach V_{REF} before the clock changes state. From this point, CMP2 keeps M_{2S} off and V_S is constant. In the second half period (CK = 0), M_{1S} turns on feeding the current I_{M1} to the integrator. V_S decrease during the whole second half clock period, with a smaller slope than the increasing one ($I_{M1} < I_{M2}$, by design), so that *Vs* really reaches V_{REF} in the following increasing phase, as supposed above. The resulting waveform is reliably synchronous with the clock but not perfectly triangular. However, it can be easily shown that eqns. (4.15) and (4.17) are still perfectly valid and that:

$$\Delta V_S = \frac{1}{C_M} \cdot \frac{T_{CK}}{2} \cdot I_{M1} . \tag{4.18}$$

Combining eqs. (4.17-4.18) we finally find:

$$\tau = \frac{\Delta C}{C_M} \cdot \frac{I_{M1}}{4 I_D} \cdot T_{CK} . \tag{4.19}$$

In this way, we have obtained that the pulse width τ is proportional to the clock period and to Δ*C*, as desired. Note that only current and capacitance ratios appear in (4.19), so that a very small sensitivity to temperature is expected.

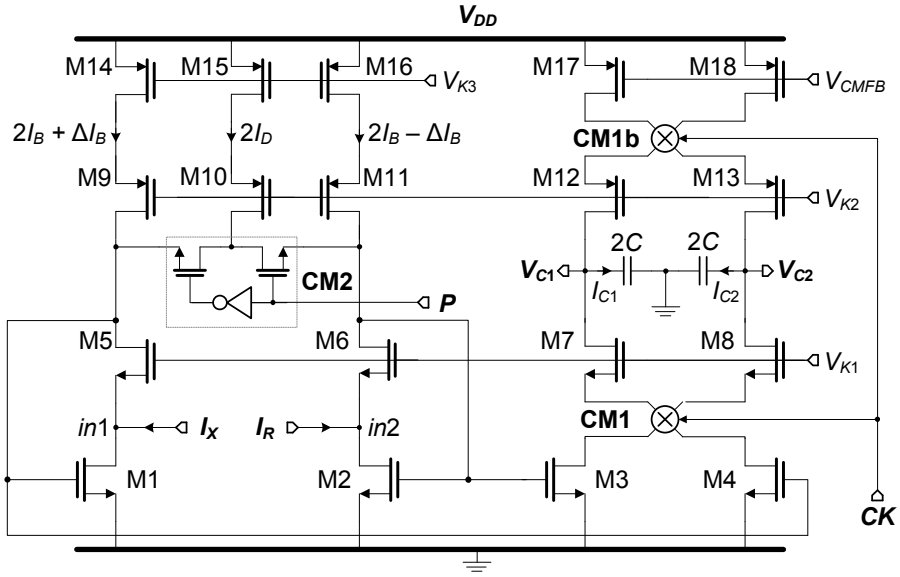


Fig. 4.11 – Current amplifier (CA) schematic diagram including also the function of I_D and ΔI_B current sources and CM1, CM2. Note that the chopper modulator CM2 has been implemented with two complementary controlled switches. Furthermore CM1 has been duplicated (CM1b) in order to modulate the low frequency noise of M17-M18.

Figure 4.11 shows the circuit designed to include the functions of blocks CA, CM1, CM2, and of current sources I_D and ΔI_B. M14, M16 and M15 are constant current sources that set M5 and M6 drain currents. In particular, I_{D15} can be conveyed to M6 or M5 depending on the value of the signal *P*. Currents I_X and I_R enter the CA at the points indicated in the figure with *in*1 and *in*2. Thanks to the M1-M5 and M2-M6 feedback loops, the DC input resistance is of the order of $(1/\, g_m^2 r_d)$.
Clearly, due to the finite bandwidth of the loop gain, the input impedance at the operating frequency ($f_{CK} = 1/T_{CK}$) is higher than the DC value. However, as confirmed by simulations, the resistance is low enough to make the input voltage variations negligible with respect to the V_S swing. This condition is important to keep the input currents independent of the device parameters and temperature. The currents in M1 and M2 are mirrored to M4 and M3, respectively. Therefore:

$$I_{D3} = I_R + I_{D16} + P \cdot I_{D15} \,. \tag{4.20a}$$

$$I_{D4} = I_X + I_{D14} + \overline{P} \cdot I_{D15} \,. \tag{4.20b}$$

The operation of modulator CM1 on currents ID3, ID4 can be easily described introducing the ideal modulating signal *m*(*s*), which assumes the value "+1" when the digital controlling signal *s* is high, and "–1" when the *s* is low. With this convention, we have:

$$I_{D8} - I_{D7} = m(CK) \cdot \left(I_{D4} - I_{D3}\right) = m(CK) \cdot \left(I_X - I_R + I_{D14} - I_{D16} - m(P) \cdot I_{D15}\right). \tag{4.21}$$

The integrating capacitor, *C* in Fig. 4.9(a), is replaced by two grounded capacitors of value 2*C*. The equivalence is guaranteed by the stabilization of the common

mode voltage of nodes V_{C1} and V_{C2}, operated by a conventional feedback loop acting on M17 and M18. Since M17 and M18 are nominally identical, we have that $I_{D17} = I_{D18}$, and applying the Kirchhoff law of current to the output nodes, we easily find:

$$I_{D7} + I_{D8} = I_{D17} + I_{D18} = 2I_{D17}\,. \tag{4.22a}$$

$$I_{C1} = I_{D17,18} - I_{D7}\,. \tag{4.22b}$$

$$I_{C2} = I_{D17,18} - I_{D8}\,. \tag{4.22c}$$

From eqs. (4.22a-c) it can be easily found that $I_{C2} = -I_{C1}$, and from eq. (4.12):

$$I_{C1} = \frac{I_{D8} - I_{D7}}{2} = m(CK)\cdot\left(\frac{I_X - I_R}{2} + \frac{I_{D14} - I_{D16}}{2} - m(P)\cdot\frac{I_{D15}}{2}\right). \tag{4.23}$$

Equivalence with quantities in Fig. 4.9 is given for: $V_C = V_{C1} - V_{C2}$, $I_C = I_{C1}$, $I_D = I_{D15}/2$, $\Delta I_B = (I_{D14} - I_{D16})/2$, proving that the circuit in Fig. 11 actually implements the required function.

It is worth noting that ΔI_B is obtained by making M14 and M16 (i.e. I_{D14} and I_{D16}) different by design. Similarly to this intentional current mismatch, casual offset currents in the CA are modulated by CM1 and produce no effects on the charge balance over a clock period, i.e. on the pulse width. Modulator CM1b has been added to extend this beneficial effect to possible mismatch of the M17-M18 pair. Noise current components at frequency much lower than f_{CK} are also rejected by this mechanism, as it happens in a chopper modulated stage.

Experimental results - A prototype has been designed using the 0.32 µm / 3.3 V CMOS device subset of the STMicroelectronics process BCD6s. Table 4.I shows the main component values for blocks RG and CA. The circuit was designed to work with an external 30 kHz clock. Currents I_D and ΔI_B were set to 20 nA and 53 nA, respectively. Chopper modulators CM1 and CM1b are implemented by means of *n* and *p* MOSFET, respectively.

Ramp generator (SG)		**Current amplifier (CA)**			
M1M	14/50	M1-4	4/12	M14	54/50
M2M	14/50	M5-8	2/2.5	M15	7.5/100
M3M	2.5/8	M9	43.2/10	M16	46/50
M4M	5/8	M10	7.5/20	M17-18	4/4
M5M	4/2	M11	36.8/10	*C*	0.5 pF
M6M	50/50	M12-13	4/1	C_M	3 pF

Table 4.I – Prototype design data: MOSFET aspect ratios W/L are expressed in µm/µm.

Polysilicon/n^+implant capacitors have been used for components *C* and C_M. To facilitate characterization of the device, a dummy sensor was included on the test chip. C_R was a constant capacitor of 500 fF, while C_X was the sum of a constant capacitance, identical to C_R, and a variable capacitor made up of four binary weighted capacitors that could be selectively connected in parallel. The total differential capacitance ΔC could be varied from 16 to 256 fF with step 16 fF through four configuration bits. Due to the required small capacitance values, non-

standard capacitors were designed using overlaps of the three available metal layers. To maximize linearity, all capacitance values were obtained by parallel connection of a single elementary capacitor. Both comparators CMP and CMP2 are conventional comparators having the same topology of that in 3.1.1. To block CMP has been added a simple 6-transistor fully differential amplifier, shown in Fig. 4.12 to obtain a low hysteresis comparator.

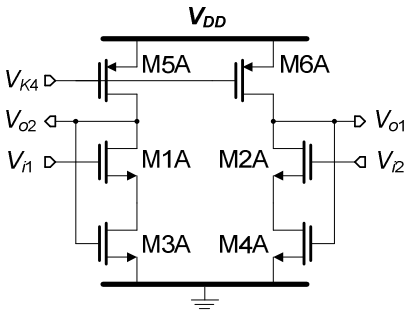


Fig. 4.12 – Schematic diagram of the fully differential amplifier used to lower hysteresis in CMP.

All the constant current sources indicated in the circuit have been derived from a single low power, low temperature drift current source (CS). An *ad hoc* three wire serial interface, identical to that discussed in section 3.1.5, has been included in order to set various configuration bits used to vary the internal dummy sensor and trim selected currents. The main waveforms have been routed to diagnostic pads through low input capacitance buffers. A separate power supply line has been used for the buffers and the serial interface. An optical micrograph of the chip, with the main parts labelled, is shown in Fig. 4.13; the total dimensions of the circuit are $1025 \times 515\ \mu m^2$.

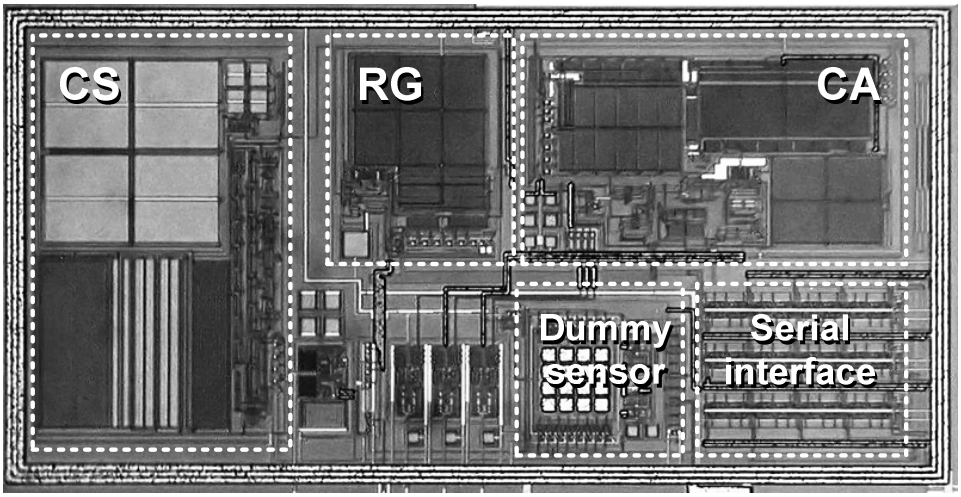


Fig. 4.13 – Layout of the prototype chip with the main blocks indicated. CS: current source; RG: ramp generator; CA: current amplifier.

For all measurements shown in this work, the 30 kHz clock was provided by a HP 33120A signal generator while the waveforms have been acquired with a Tektronix TDS220 digital oscilloscope. The chip temperature was varied by means of a Peltier cell cryostat with 0.1 ºC precision. The power supply was set to 3 V. The main waveform in the circuit are shown in Fig. 4.14 for ΔC = 160 pF. Comparison with the ideal waveform in Fig. 4.9(c) proves the correct operation of the circuit.

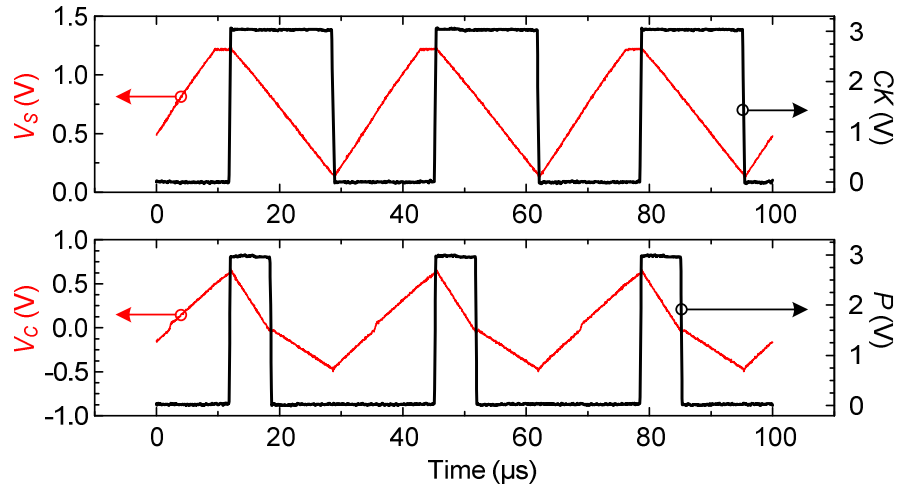


Fig. 4.14 – Experimental waveform measured on the test chip with ΔC = 160 fF.

The dependence of the pulse width on the differential capacitance ΔC is shown in Fig. 4.15 for two different temperatures (0 ºC and 80 ºC). Curves at intermediate temperatures fall in between. It is possible to observe a satisfactorily linear response, with only local deviations that can be ascribed to parasitic capacitances of the dummy sensor.

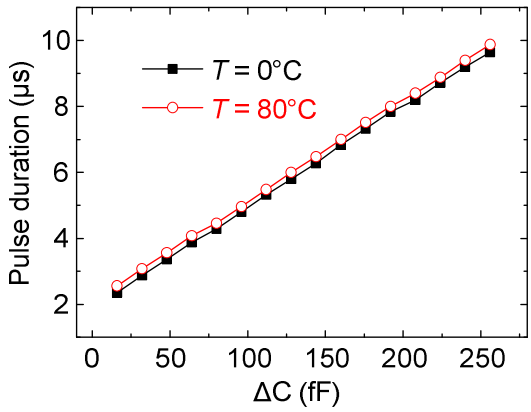


Fig. 4.15 – Measured dependence of the output pulse duration as a function of the sensor differential capacitance for two different temperatures.

The expected low sensitivity to temperature is confirmed. The residual temperature drift over the whole temperature range is less than 2.5 % of full scale, corresponding to 300 ppm/ºC. As far as noise is concerned, the visible effect is the jitter on the output pulse trailing edge. The resulting standard deviation of the pulse duration, estimated over a set of 200 randomly taken measurements, was σ_T = 0.4 % of full scale. The total supply current (diagnostic buffers excluded) is only 28 μA.

4.2.2. Prototype of a capacitance to voltage converter

With a few modifications to the scheme in Fig. 4.9, a very compact capacitance to voltage converter can be obtained. The scheme in Fig. 4.16 shows the block diagram of the C-to-V converter, where blocks CA and RG are very similar to those described in the previous section. More specifically, the block CA is obtained from the scheme in Fig. 4.11 removing the chopper modulators CM1, CM1b and CM2. Besides, current sources providing I_D, ΔI_B are not needed in this scheme, so M15 and M10 are removed, and M14, M16 are made nominally identical.

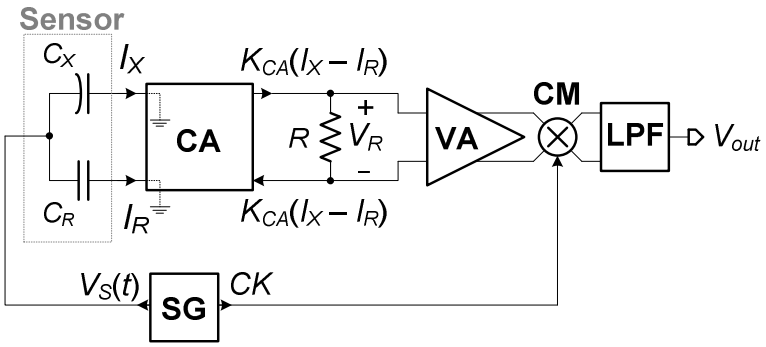


Fig. 4.16 – Block diagram of the capacitance to voltage converter.

Considering an ideal behaviour for the CA, and equal decreasing and increasing slopes for the triangular waveform V_S we simply find:

$$V_R = K_{CA} \cdot R \cdot \Delta C \cdot \frac{dV_S}{dt} = K_{CA} \cdot R \cdot \Delta C \cdot \frac{2\Delta V_S}{T_{CK}} \cdot m(t)\,. \tag{4.24}$$

where V_R is the voltage across R, $\Delta V_S/T_{CK}$ is the absolute value of the slope of the triangular wave and $m(t)$ is the ideal modulating signal introduced in the previous section. It is worth noting that the effect is equivalent to modulate the input quantity ΔC by a square-wave as in chopper stabilized amplifier. The signal V_R, is amplified by the fully differential instrumentation amplifier VA and then demodulated by CM. Neglecting the signal chain delay, we can write:

$$V_{out} = A_{VA} \cdot K_{CA} \cdot R \cdot \Delta C \cdot \frac{2\Delta V_S}{T_{CK}}\,. \tag{4.25}$$

where $m^2(t) = 1$, and A_{VA} is the voltage amplifier gain. The low pass filter LPF limits the bandwidth to that strictly required for the application, reducing the total noise amplitude.

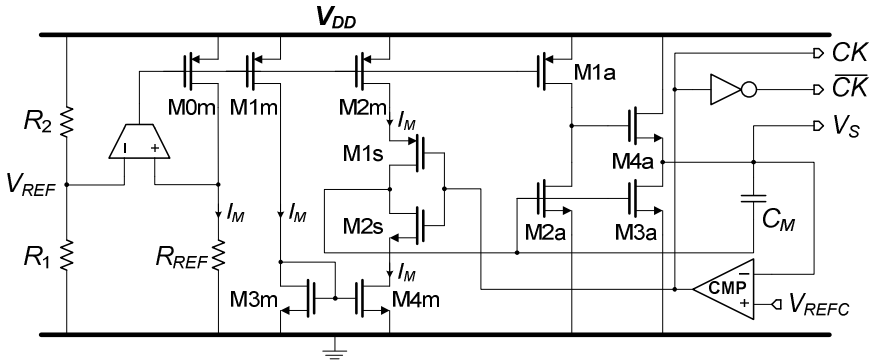


Fig. 4.17 – Schematic diagram of block SG

The SG circuit, shown in Fig. 4.17, is basically a relaxation oscillator made up of a current starved inverter CSI (M0m-M4m, M1s-M2s), a Miller integrator (M1a-M4a) and a conventional comparator, CMP with the same topology of that discussed in the previous chapter (Fig. 3.4). It can be easily demonstrated that the peak-to-peak amplitude of the triangular waveform $V_S(t)$ is equal to the comparator hysteresis, ΔV_S. The comparator output drives the current starved inverter and provides also the clock signal in the demodulator. The current I_M provided (sunk by M4m or sourced by M2m) by the CSI is nominally equally making identical M1m-M2m and M3m-M4m. On the other hand, the same current is derived from the current flowing on R_{REF}, which is fixed by the simple loop formed by M0m, and the OTA. Considering also M0m identical to M1m and M2m, we can calculate the fundamental frequency of signal V_S and *CK*:

$$f_{CK} = \frac{1}{T_{CK}} = \frac{1}{2\Delta V_S}\cdot\frac{I_M}{C_M} = \frac{1}{2\Delta V_S}\cdot\frac{1}{C_M}\cdot\frac{R_{REF}}{V_{REF}} = \\ = \frac{1}{2\Delta V_S}\cdot\frac{1}{C_M}\cdot R_{REF}\cdot\left(V_{DD}\cdot\frac{R_1}{R_1+R_2}\right)^{-1} \quad . \tag{4.26}$$

From eqs. (4.23-4.24), we obtain:

$$\frac{V_{out}}{V_{DD}} = A_{VA}\cdot K_{CA}\cdot\frac{R}{R_{REF}}\cdot\left(1+\frac{R_2}{R_1}\right)\cdot\frac{\Delta C}{C_M} \, . \tag{4.27}$$

Note that the V_{out}/V_{DD} ratio depends linearly on the quantity to be measured (ΔC) and that the expression includes only resistance ratios, capacitance ratios and current mirror gains (K_{CA} and K), and A_V. For this reason a low sensitivity to temperature and process variations can be expected from (4.25), as long as also A_V is precise and stable with temperature.

Design of a prototype **–** A circuit prototype has been designed using the 0.32 µm / 3.3 V CMOS devices of the Bipolar-CMOS-DMOS BCD6s process of STMicroelectronics. The block VA is implemented with the same topology shown in Fig. 2.2, designed to draw only 18 µA from the supply voltage. The voltage V_{REF} was set to $V_{DD}/2$ by making $R_1 = R_2$. The SG was designed to produce a nominal clock frequency of 40 kHz at 27 ºC. Figure 4.18 shows the relevant waveforms of

the circuit obtained by transient simulations with a constant sensor capacitance difference ΔC = 100 fF.

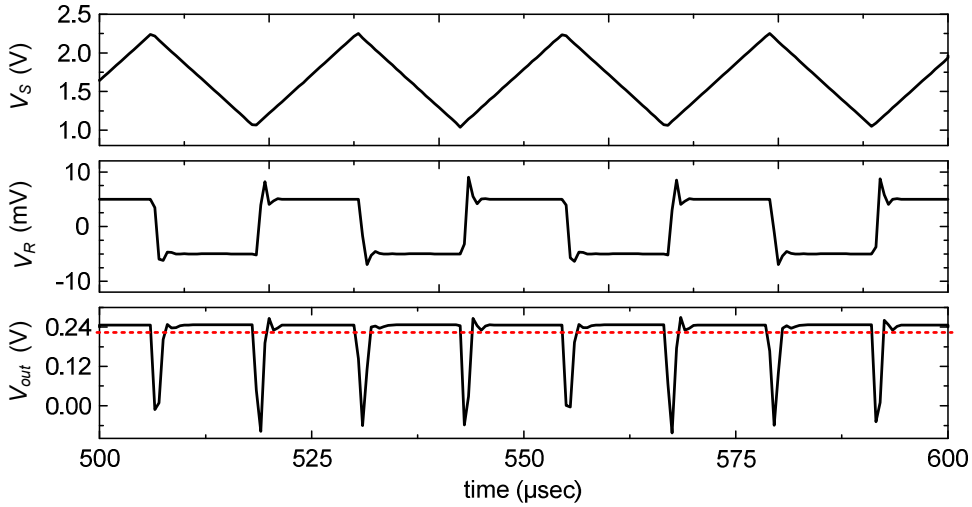


Fig. 4.18 – Relevant waveform in the circuit resulting from transient simulations for ΔC = 100 fF. Dashed line is V_{out} mean value.

Note that the output voltage is not constant but deep spikes are present. This is due to the settling time of the CA after each V_S slope reversal. This disturbance causes the output voltage mean value, indicated with a dashed line in Fig. 4.18, to be lower than expected. It was of primary importance to check whether this phenomenon was a source of sensitivity to temperature or non linearity in the circuit response.

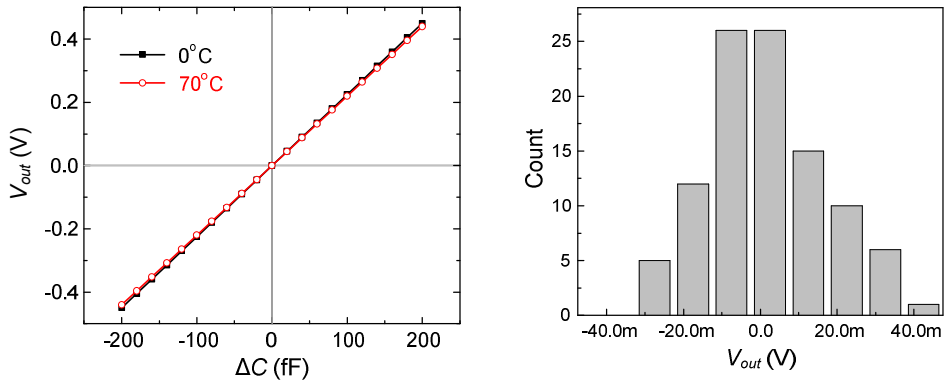


Fig. 4.19 – (a) Simulated output voltage as a function of the sensor capacitance difference for T = 0℃, T = 70℃. (b) Histogram of output voltage given by means of 100 runs of Monte Carlo analysis.

To this purpose, the block LPF has been implemented with an ideal second order Butterworth low pass filter, with a cut-off frequency of 4 kHz. The output voltage is then taken after a period of 2 ms, considerably longer than the filter settling time. Transient simulations were repeated sweeping ΔC at various temperatures. The result is shown in Fig. 4.19(a), where the ΔC to output voltage transfer characteristic is shown for two temperature values (0℃ and 70℃).
A good linearity and low temperature effects (2.2 % over the whole 0–70ºC interval) can be observed. Note that the area of the spike visible on V_{out} in Fig. 4.19 can be reduced increasing the bandwidth of the CA and VA. This is paid in terms of increased supply current.

Consumption	I_{DD} = 35 µA
Estimated cell area ($\Sigma_i W_i L_i$ + area of resistors R, R_1, R_2)	0.035 mm^2
Sensitivity to temperature (0-70℃)	300 ppm/℃
Capacitance range: max(ΔC)	±200 fF
Nominal sensitivity	2.236 mV/fF
Sensitivity to balanced parasitic capacitance	$S(\Delta C/C_{pb})$ = 140 aF/pF
Sensitivity to unbalanced parasitic capacitance	$S(\Delta C/C_{pu})$ = 200 aF/pF
Equivalent noise (RMS), B = 4 kHz	$\sigma_{\Delta C}$ = 450 aF
Equivalent offset capacitance	$\sigma_{\Delta C}$ = 7 fF

Table 4.II – Summary of performances of the proposed C-to-V converter.

With a total supply current of 35 µA, the designed prototype represents a possible compromise between accuracy and power consumption. The main circuit characteristics obtained by means of simulations are reported in Table 4.II. Noise data have been estimated from the result of multiple NOISETRAN simulations performed over a total time interval of 15 ms and considering an ideal low pass filter with a cut-off frequency of 4 kHz. A dynamic range of about 53 dB can be estimated. Effects of parasitic capacitance have been investigated connecting grounded capacitors of various values to one (unbalanced) or both (balanced) inputs. A negligible sensitivity was found in both cases. Monte Carlo analysis (Fig. 4.20(b)) showed that the effect of process variation and device mismatch can be referred to an equivalent input offset capacitance with a standard deviation of 7 fF.

4.3 Improvements to the C-to-PWM interface

4.3.1. Double clock technique for dynamic range extension

The proposed C-to-PWM converter has been derived from the circuit discussed in section 4.2.1 by adding double clock timing as an original strategy for jitter reduction. The advantages in terms of jitter are exposed with a theoretical analysis, at the same time, provides also useful hints for the circuit optimization in terms of bias current. Electrical simulations confirm the validity of the proposed approach, and allow us to draw some important conclusions about the possibilities of this

interface in terms of very low temperature drift, moderate jitter, and very low current absorption.
The block diagram of the proposed circuit is shown in Fig. 4.20, where a frequency divider and a dedicated modulator for ΔI_B have been added to the circuit of Fig. 4.9. The operation of the frequency divider is to produce clock signal *CK*2 of fundamental frequency f_{CK2}, n times slower then the fundamental frequency f_{CK1} of the input clock *CK*1. This allows us to discern to section of the circuit regarding the fundamental frequency of the signals, as indicated in Fig. 4.20. The output PWM signal is synchronous with the slow clock *CK*2, is indicated with *P*.

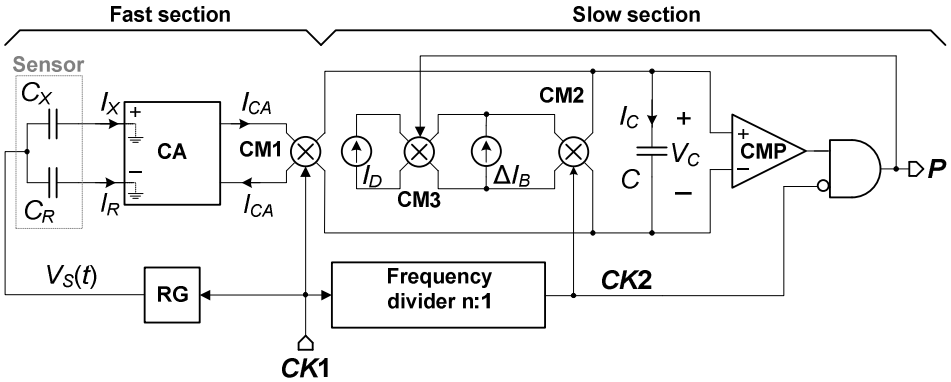


Fig. 4.20 – Block diagram of the double clock C-to-PWM converter.

The block RG, identical to that presented in Fig. 4.10(a), and the block CA function is maintained unchanged. Thus the eq. (4.14) still holds. Due to the slope reversal of V_S, the sign of I_{CA} is reversed every half period of *CK*1. At the same time, CM1 operates a sign change, so that the current fed to the slow section is constantly positive. It is worth noting that the effect is similar to that occurring in chopper modulated amplifiers where the signal (ΔC) is modulated by an ideal square wave and demodulated by the same square wave by CM1. In this way, the offset and low frequency noise components of CA are strongly reduced. The charge integrated for each T_{CK1} period by the current I_{CA} is then given by eq. (4.15), where T_{CK} has to be substituted by T_{CK1}. The T_{CK2} period is n times larger then T_{CK1}, thus the total charge Q_A accumulated on capacitor C results

$$Q_{CA} = n \cdot \left[-\frac{\Delta C}{2} \cdot \int_0^{T_{CK1}/2} \frac{dV_S}{dt} \cdot dt + \frac{\Delta C}{2} \cdot \int_{T_{CK1}/2}^{T_{CK1}} \frac{dV_S}{dt} \cdot dt \right] = n \cdot \Delta C \cdot \Delta V_S \,, \tag{4.28}$$

as we are now interested to consider the charge balance obtained in the slow section of the circuit. Figure 4.21 helps understanding by a graphical representation of the waveforms in the circuit: *CK*1, V_S, I_{CA}, *CK*2, *P*, V_C, and finally the charge contributions of current I_{CA}, I_D and ΔI_B in the period T_{CK2}: where the shaded areas illustrate the total positive and negative accumulated charge.

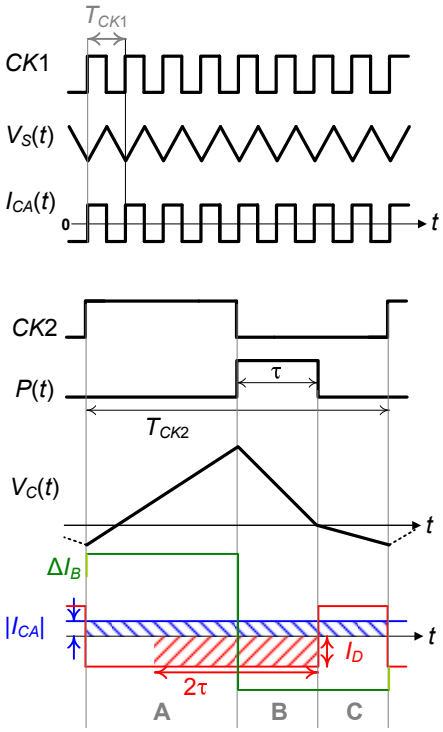


Fig. 4.21 – Important waveforms of the circuit indicating how the charge balance is obtained in the T_{CK2} period: the shaded areas indicate the net positive and the negative charge contribution.

The contribution of ΔI_B is also shown: this current reaches *C* through CM2, which changes state every half cycle of clock *CK*2, so that the net contribution of ΔI_B is zero. As for the previous circuit this current has it is only used to force the voltage V_C across the capacitor *C* to increase in the first *CK*2 half cycle and decrease in the second half, regardless of I_{CA} and I_D. To accomplish this, ΔI_B is made larger than $I_D + |I_{CA}|$. As a result, the waveform V_C assumes the behaviour depicted in Fig. 4.21.

In the first *CK*2 half cycle, the NAND gate keeps *P* low, thus, CM3 inverts while CM2 is in non-inverting state. The contribution of I_D in this period is then negative. Supposing that V_C is positive at the beginning of the *CK2* second half cycle, the signal *P* turns on, starting the output pulse. Both CM2 and CM3 change state at this point, so the contribution of I_D is still negative. The pulse stops, after a duration τ, when V_C crosses the zero level turning low the comparator output and changing the state of CM3. From this point to the end of the clock cycle I_D gives a positive contribution to I_C. The overall charge contribution of I_D over the whole *CK*2 period is then $-2\tau I_D$. In order to have a stationary waveform, the charge balance over a *CK*2 period should be zero, therefore the condition $Q_{CA} = 2\tau I_D$ should hold. Using eqs. (4.28) and (4.18), we get:

$$\tau = \frac{Q_{CA}}{2I_D} = \frac{n \cdot \Delta C \cdot \Delta V_S}{2I_D} = n \cdot T_{CK1} \cdot \frac{I_{M1}}{I_D} \cdot \frac{\Delta C}{4C_M} = T_{CK2} \cdot \frac{I_{M1}}{I_D} \cdot \frac{\Delta C}{4C_M}, \qquad (4.29)$$

Equation (4.29) shows that the pulse duration depends on Δ*C* in a linear fashion and is proportional only to quantities that can be made precise and temperature independent, such as the clock period and capacitance and current ratios.

The current amplifier has to be slightly modified in order to provide the function of CM2 and of CM3. The implementation proposed here, is shown in Fig. 4.22. Note that the switch arrays and constant current sources ΔI_B and I_D have been embedded into the CA block. The currents I_X and I_R enter the stage through inputs *in*1 and *in*2. The required low input resistance is provides by the local feedback loops M1, M5 and M2, M6. The floating integration capacitor C is substituted by two capacitors of value $2C$ referenced to ground. The equivalence is guaranteed by a common mode feedback loop, not shown for simplicity, which fixes the output common mode voltage, acting on M17 and M18 through V_{CMFB}, so that the net current flowing from the capacitors to ground (common terminal) is zero. By inspection of the circuit, and using the same procedure illustrated in section 4.2.1, it can be easily proven that the block in the currents I_D and ΔI_B, corresponds with $I_{D15}/2$ and $I_{D10}/2$, respectively.

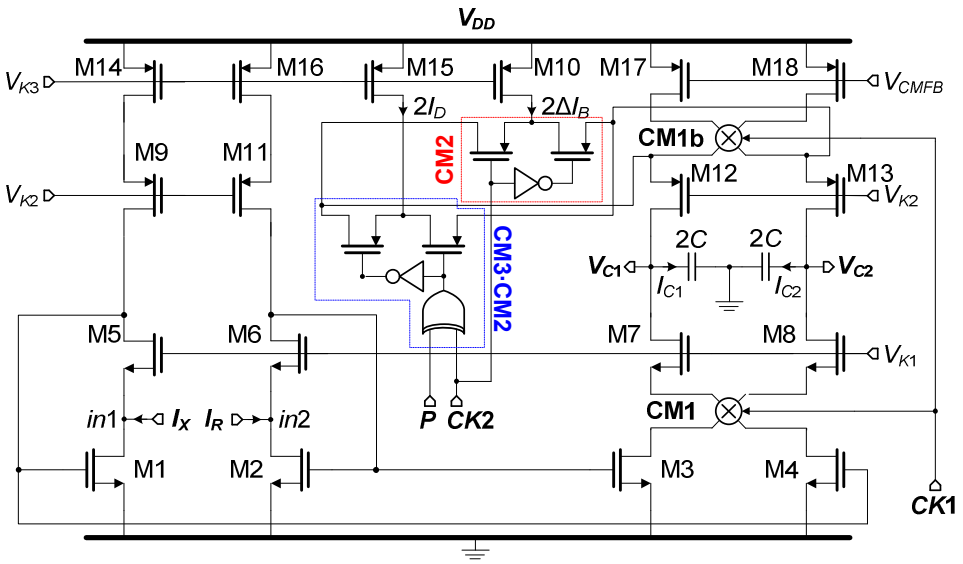


Fig 4.22 – Schematic view of the current amplifier (CA) for the double clock strategy, including the chopper modulators and the current sources ΔI_B and I_D.

Analysis of non idealities – The main origins of non idealities are: (i) the finite input resistance of the current amplifier and (ii) noise. The finite input resistance causes the CA input voltage to be different from zero. This reduces the amount of the V_S amplitude (ΔV_S) that actually falls across the capacitors, and, through (4), reduces the output pulse duration. Since the input resistance is a function of MOSFET parameters, a temperature dependence of the output pulse can be expected. As far as noise is concerned, the visible effect will be a jitter on the pulse τ.

In order to estimate the effects of the finite input impedance, it should be necessary to consider both the frequency dependent expression of the latter and the Fourier series representation of V_S. In order to maintain a simple vision of the circuit, it is possible to refer to the following approximate expression of the input impedance:

$$|Z_{IN}| = \frac{1}{g_{m5}} \cdot \frac{C_{GS1}}{g_{m1}} \cdot \omega = \frac{1}{g_{m5}} \cdot \frac{\omega}{\omega_0}, \tag{4.30}$$

valid for $\omega > (C_{GS1} \cdot r_{d5})^{-1}$. The important information from (4.30) is that the input impedance strongly increases at small bias currents, where the gms of the devices get smaller. The above design indication is in contrast with noise reduction considerations. The effect of noise is that of adding a random charge q_n to Q_{CA} in (4.28). The noise charge derives from integration over a *CK*2 period of noise components superimposed to various currents contributing to I_C.

It is possible to show that, under reasonable simplifications, the dominant component is the noise current of the current amplifier. Fortunately, modulators CM1, CM1b and CM2 shift the low frequency noise components, particularly large in MOSFETs, to higher frequency. As a counterpart, the thermal noise present at high frequencies is shifted back into the baseband and integrated by capacitor *C*. Through mathematical arguments, which will be discussed later, it is possible to estimate the noise charge as follows:

$$\left\langle q_n^2 \right\rangle = \left\langle \left[\int_0^{T_{CK2}} i_n(t) \cdot dt \right]^2 \right\rangle = T_{CK2} S_{IHF}, \tag{4.31}$$

where i_n is the integrated noise current, which, for the above arguments, we have been considered to coincide with the thermal noise of amplifier CA, characterized by the constant power spectral density (PSD) S_{IHF}.

Although it is not mathematically rigorous, the *RMS* fluctuation (jitter) on the pulse duration can be calculated from the noise charge using (4.28-4.29). A more rigorous approach will be presented in the following discussion. The quantity the best represent the circuit resolution is the jitter normalized to the full scale pulse duration, that can be obtained from (4.29) with ΔC equal to its full scale value, ΔC_{FS}:

$$\frac{\tau_{n-RMS}}{\tau_{FS}} \cong \frac{\sqrt{\left\langle q_n^2 \right\rangle}}{2I_D} \cdot \frac{1}{\tau_{FS}} = \frac{\sqrt{T_{CK2} S_{IHF}}}{n \cdot \Delta V_S \cdot \Delta C_{FS}} = \frac{1}{\sqrt{n}} \cdot \frac{\sqrt{T_{CK1} S_{IHF}}}{\Delta V_S \cdot \Delta C_{FS}}, \tag{4.32}$$

Equations (4.28, 4.30) provide useful design indications. The parameters ΔC_{FS} and ΔV_S in (4.30) cannot be changed freely, since the former depends on the sensor only, while the second cannot exceed V_{DD}.

Considering the rightmost term in (4.32), it is important to first consider the case $n = 1$, corresponding to the previously discussed single clock version. In this case, a reduction of the normalized jitter can be obtained by increasing the clock frequency. This is not really effective, since a the increased input current of block CA (see eq. (4.18)) and the increased bandwidth requirements impose an increase of the CA bias current, resulting in an increase of S_{IHF}. The proposed double clock circuit allows an effective reduction of the jitter by increasing the factor *n.* In practice it is possible to keep the fast clock frequency (f_{CK1}) constant, and slow down the second clock *CK*2. The only consequence is an increase of the measurement time (T_{CK2}), generally compatible with the little bandwidth demand of many capacitive sensors.

The other factor to be considered is the noise current PSD S_{IHF}. This quantity is proportional to the g_m of a few MOSFETs in the CA block. Therefore it can be

beneficial to reduce the CA bias current as much as possible. As clearly suggested by (4.30) and related discussion, the side effect is an increase of the sensitivity to temperature. Simulations operated with accurate device models are required to find the optimum trade-off.

Design of a prototype –. The values of the main circuit parameters are reported in table 4.III. The clock frequency ratio n was set to 4. In order to simulate a sensor as much as possible close to a real device, a large constant value (1 pF) was added to both C_X and C_R. Similarly to the case of pressure sensors, C_R was a constant (dummy) capacitor. The various currents required for operation of the circuit where derived by a single reference current. All components present in the prototype were devices actually available in the process. No ideal components were used.

C_X	1pF + ΔC	ΔI_B	80 nA	f_{CK1}	40 kHz
C_R	1pF	I_D	20 nA	f_{CK2}	10 kHz
ΔC	5 - 250 fF	I_{M1}	200 nA	n	4

Table 4.III – Data of the double clock prototype circuit.

The circuit was first sized in such a way that the currents provided by M14, M16, M17 and M18 in the CA were 1 µA. Characterization of the circuit was performed by means of transient simulations; Fig. 4.23 shows the simulated main waveforms of the circuit. In order to characterize the role of the CA bias currents, the initial value of 1 µA was progressively reduced down to 200 nA. This operation was performed together with re-sizing of MOSFETs in the CA in order to maintain their overdrive voltages ($V_{GS} - V_t$) constant. The resulting ΔC-τ transfer characteristics are shown in Fig. 4.24 for bias currents of 200 nA and 1 µA. It is possible to observe the excellent linearity of the response in both cases and a slight reduction of the slope (–4 %) caused by decreasing the bias current. This effect can be ascribed to the bias current dependence of the input impedance discussed below. The effect of CA bias on the temperature drift and jitter on the output pulse have are shown in table 4.IV. The temperature drift was estimated by performing simulations at different temperatures in the range 0-80 ºC, with Δ*C* fixed to a mid-scale value (125 fF). The S_{IHF} values were estimated by ACNOISE simulations of the CA. The relative jitter was calculated from S_{IHF} by means of eq. (4.30). The results in table 4.IV provide quantitative information about the predicted effects of the amplifier bias current on the temperature drift showing how this parameter can be improved at the expenses of jitter. The total supply current of the circuit in the case of highest bias current (1 µA) was 15 µA.

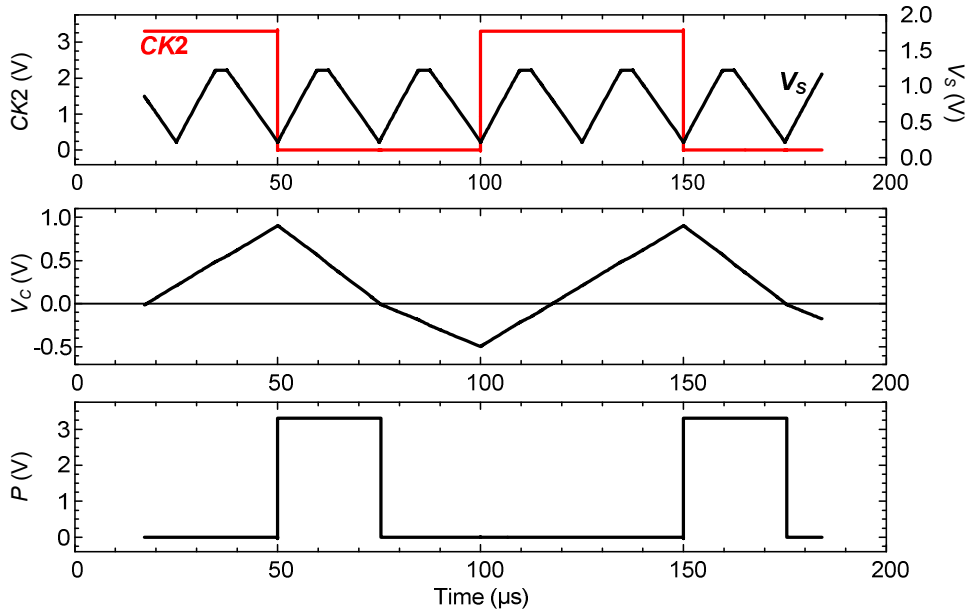


Fig. 4.23 – Simulated main waveforms.

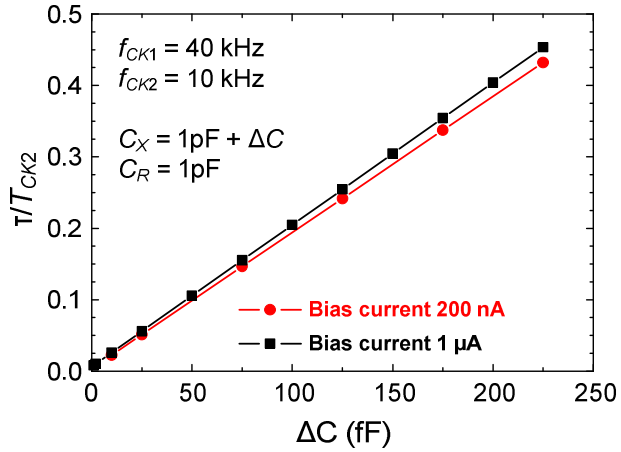


Fig. 4.24 – Pulse duration vs. differential capacitance for two CA bias currents.

Bias current (nA)	Temp. drift (ppm / ºC)	S_{IHF} ((pA)^2/Hz)	Jitter (% RMS)
1000	150	1.73	1.3
320	250	0.44	0.66
200	300	0.27	0.52

Table 4.IV – Temperature drift and jitter data in different bias conditions.

Consideration on effective noise bandwidth – Let us now revise critically some assumptions about the integrated noise that we made before. The duration τ of the periodic output signal *P* can be considered as a numerical sequence, whose samples are made available at the f_{CK2} frequency (i.e. the fundamental frequency of *P*). The sampling phenomenon resides intrinsically in the principle of operation circuit; to explain this let us consider the action of the comparator CMP, in each second half cycle of T_{CK2} (corresponding to phases B and C in Fig. 4.21). The comparator determines the falling edge of P, i.e. determines the duration τ, at every time a zero crossing of $V_C(t)$ is sensed. The period *T* between two consecutive crossings is the time period needed to perfectly balance the integrated currents (including the noise currents), as the global variation of V_C, and of the integrated charge is zero. The noise charge sequence can be expressed as:

$$q_n[k] = \int_{T[k-1]}^{T[k]} i_n(t) \cdot dt \,, \tag{4.33}$$

Periods *T* and T_{CK2} are different, because of the action of the noise, i.e. *T* can be considered of a random sequence, with an average value of T_{CK2} with a super-imposed jitter. If the following condition holds

$$q_n[k] >> \int_{T[k-1]}^{T[k]-T_{CK2}} i_n(t) \cdot dt \,, \tag{4.34}$$

then eq. (4.31) can be approximated as:

$$q_n[k] \cong \int_{T[k]-T_{CK2}}^{T[k]} i_n(t) \cdot dt \cong \int_{(k-1)T_{CK2}+\tau}^{kT_{CK2}+\tau} i_n(t) \cdot dt \,, \tag{4.35}$$

Clearly, this approximation holds for jitters much smaller than the total T_{CK2} period. It is now convenient to separate the sampling process from the integration process. This can be formalized as follows:

$$q_n[k] = \left(q_n(t) : t = T[k] = kT_{CK2} + \tau\right),\ q_n(t) = \int_{t-T_{CK2}}^{t} i_n(t) \cdot dt \tag{4.36}$$

From eq. (4.34) the operation of moving window integration on noise currents is now evident. Considering the PSD we can easily write

$$S_q(f) = T_{CK2}^2 \cdot \mathrm{sinc}^2\left(fT_{CK2}\right) \cdot S_I(f) \,, \tag{4.37}$$

where the sinc(*x*) function of *x* is defined here as $\sin(\pi x)/\pi x$ and $S_I(f)$ is the PSD of the noise currents. As discussed below, we will consider the white spectrum S_{IHF} given by the high frequency contribution (thermal noise) of the CA block. When the sampling is applied, the $S_q(f)$ replicas fold in the baseband, and as $S_q(f)$ has a bandwidth much more greater than f_{CK2}, the aliasing phenomenon occurs. In order to simplify the calculations we can a fictitious flat PSD with a band determined by the equivalent bandwidth approximation. For the sinc^2 function in eq. (4.37), the equivalent bandwidth is given by $f_{CK2}/2$ which accidentally corresponds with the Nyquist frequency, so that under this approximation, the PSD of the $q_n[k]$ sequence can be simply written as

$$S_{[q]}(f) = 2T_{CK2}^2 \cdot S_{IHF} \,. \tag{4.38}$$

This result has been used in eq. (4.31) to estimate the expectation of $q_n^2(t)$. Let us now discuss more rigorously how the charge noise reflects on the jitter. To this purpose we have to calculate the balance in the T period of all the currents, which is expressed by the following equation

$$\int_{T[k-1]}^{T[k]} \left(I_C(t) + i_n(t)\right) \cdot dt = 0 \,. \tag{4.39}$$

The integral in eq. (4.37) can be developed considering the duration of A, B, C phases and the I_C expression for each phase, reported in Fig. 4.25. The following finite difference equation, in the z domain, can be written:

$$a \cdot \tau(z) - (a-1) \cdot z^{-1} \cdot \tau(z) = \frac{T_{CK2} I_{CA}(z)}{2I_D} + \frac{q_n(z)}{2I_D} \,. \tag{4.40}$$

where

$$a = \frac{\Delta I_B - |I_{CA}| + I_D}{2I_D} \,. \tag{4.41}$$

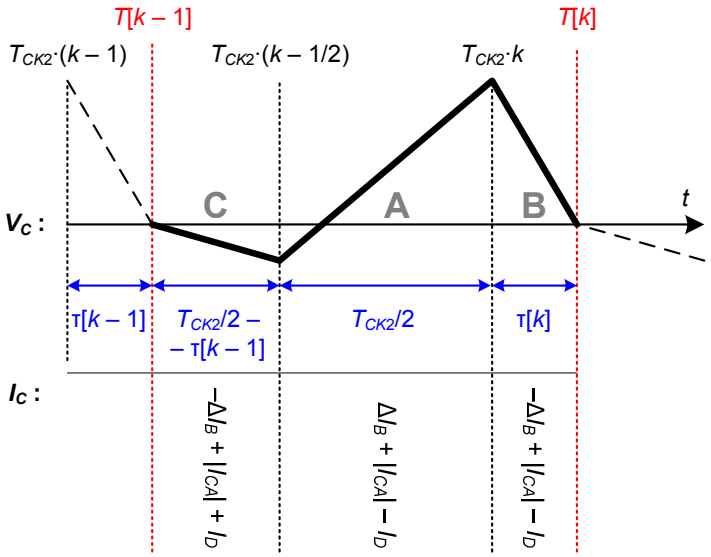


Fig. 4.25 – V_C waveform within a T period.

Now considering the only effect of noise, we can easily find transfer function in the z domain between the pulse duration fluctuations $\tau_n(z)$ and the noise charge $q_n(z)$:

$$H(z) = \frac{\tau_n(z)}{q_n(z)} = \frac{1}{2I_D} \cdot \frac{1}{a - (a-1) \cdot z^{-1}} \,. \tag{4.42}$$

The frequency response of $H(z)$ can be evaluated by the substitution $z = \exp(j\omega T_{CK2})$. As a stochastic process is involved, the quantity $|H(f)|^2$ has to be calculated:

$$|H(f)|^2 = \frac{1}{(2I_D)^2} \cdot \frac{1}{2a(a-1)\cdot[1-\cos(2\pi f T_{CK2})]+1}. \tag{4.43}$$

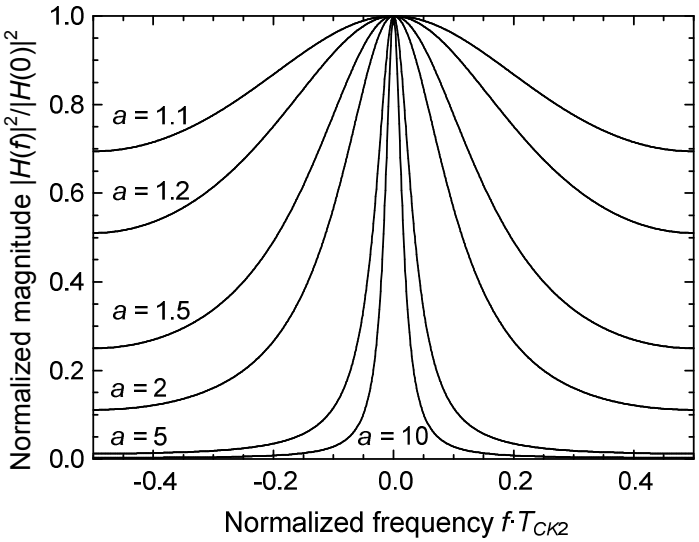


Fig 4.26 – Normalized $|H(f)|^2$ for various values of parameter a.

In Fig. 4.26, $|H(f)|^2$ is plotted for various values of the parameter a. The area under the curve is greater for smaller values of a. To our purpose we can consider the worst case, i.e. when the filtering action of $H(z)$ is weaker, which occurs for the minimum value of a. Reminding conditions in eqs. (4.13a-b), we can make $I_D = \max|I_{CA}|$. With this design choice, which maximize the range of the output characteristics $\tau(\Delta C)$, we have that

$$a_{MIN} = \frac{\Delta I_B}{2I_D} > 1. \tag{4.44}$$

where the condition (4.13b) determines the rightmost term in the equation. The equivalent bandwidth B_{eq} for the filter $H(f)$ can now be calculated in the worst case condition:

$$B_{eq} = \frac{1}{|H(0)|^2}\int_0^{1/2T_{CK2}} |H(f)|^2 \cdot df = \frac{1}{2T_{CK2}} \cdot \frac{1}{\sqrt{4a(a-1)+1}} = \frac{1}{2T_{CK2}} \cdot \frac{1}{2\left(\frac{\Delta I_B}{2I_D}\right)-1}. \tag{4.45}$$

Equation (4.43) clearly shows the beneficial action of the intrinsic filtering effect occurring when the sequence $q_n[k]$ is traduced into the $\tau_n[k]$ samples, thanks to the term related to the current ratio which can be used by the designer to limit jitter. It is worth noting that in the jitter estimation of eq. (4.30), a bandwidth equal to $1/(2T_{CK2})$ was considered. Now, thanks to eqs. (4.38, 4.45) a more rigorous value of $\tau_{n\text{-}RMS}$ can be calculated:

$$\tau_{n-RMS} = \sqrt{S_{[q]} \cdot |H(0)|^2 \cdot B_{eq}} = \frac{1}{\sqrt{(\Delta I_B / I_D) - 1}} \cdot \sqrt{\frac{\cdot T_{CK2} \cdot S_{IHF}}{2 I_D}} \,. \quad (4.46)$$

However it is important to note, that the same filtering effect acts also on the signal, limiting its effective bandwidth. This property is common to all the C-to-PWM converters present in this thesis, is applicable to increase the DR of the systems as long as the desired signal bandwidth is preserved. The same kind of trade-off is presented by the double clock strategy presented in this section.

4.3.2. Dynamic matching of C-to-PWM input ports

In this final section a technique to increment the accuracy of the C-to-PWM converter. This technique can be combined with the double clock strategy described in the previous section. Here we will discuss an implementation starting from the single clock version of the converter. Extension of this technique to the double clock version is straightforward.

In order to focus on the accuracy issue let us consider the simplified schematizations of the single clock C-to-PWM converter shown in Fig. 4.27(a). Here, the input ports of the CA amplifier have been marked with different current gains K_1, K_2, which may be induced by mismatching between the M1-M4 and M2-M3 current mirrors in Fig. 4.11. Thanks to the output common mode control circuit, the output differential current I_{CA} is produced which is proportional to the difference of the mirrored replicas of I_X and I_R. The proportionality factor is 1/2 as demonstrated by eqs. (4.22-4.23). In the case of unmatched input ports, eq. (4.14) have to be modified, resulting in:

$$I_{CA} = \frac{K_1 I_X - K_2 I_R}{2} = \frac{(K_1 C_X - K_2 C_R)}{2} \cdot \frac{dV_S}{dt} = (K_1 C_X - K_2 C_R) \cdot \frac{\Delta V_S}{T_{CK}} \cdot m(t) \,, \quad (4.47)$$

where $m(t)$ is the modulating signal shown in Fig. 4.27(b). The following quantities can be conveniently defined:

$$K_A = \frac{K_1 + K_2}{2} \,; \quad (4.48a)$$

$$\Delta K = K_1 - K_2 \,. \quad (4.48b)$$

In the nominal case $K_A = 1$ and $\Delta K = 0$; in any practical case a mismatch on M1-M4 transistors occurs, making both K_A and ΔK differ from their nominal values. It is interesting to note that we have to deal with a couple of random variables. This is due to two uncorrelated random extraction processes occurring in this case: (i) pairing of two distinct current mirrors, (ii) pairing of two distinct mosfet devices per mirror. The net effect on the charge Q_A integrated on the capacitor C can be calculated as:

$$Q_{CA} = (K_1 C_X - K_2 C_R) \cdot \Delta V_S = (\Delta C - C_0) \cdot \Delta V_{SE} \,, \quad (4.49)$$

where an equivalent slope ΔV_{SE} and an offset capacitance C_0 have been introduced:

$$\Delta V_{SE} = \Delta V_S \cdot K_A \cdot \left(1 + \frac{1}{2} \cdot \frac{\Delta K}{K_A}\right); \quad (4.50a)$$

$$C_0 = \frac{\Delta K}{K_A} \cdot \left(1 + \frac{1}{2} \cdot \frac{\Delta K}{K_A}\right)^{-1} \cdot C_R \approx \frac{\Delta K}{K_A} \cdot C_R \,. \qquad (4.50b)$$

The equivalent slope in eq. (4.49) reflects in a statistical deviation from the nominal sensitivity of the C-to-PWM converter. Anyway, this does not represent a serious issue as the discharge current I_D can be used to adapt the full scale of the sensor to the clock half cycle available for the output pulse, as illustrated by eq. (4.17).
On the other hand, the offset capacitance C_0 may invalidate the interface functionality, especially for small relative variation of the sensor with respect to its rest value ($\Delta C_{FS}/C_R$). For example if $C_0 > 0$, the output pulse is not formed until $\Delta C > C_0$; on the contrary, for $C_0 < 0$, variation range for τ may result considerably compressed as it cannot exceed $T_{CK}/2$.

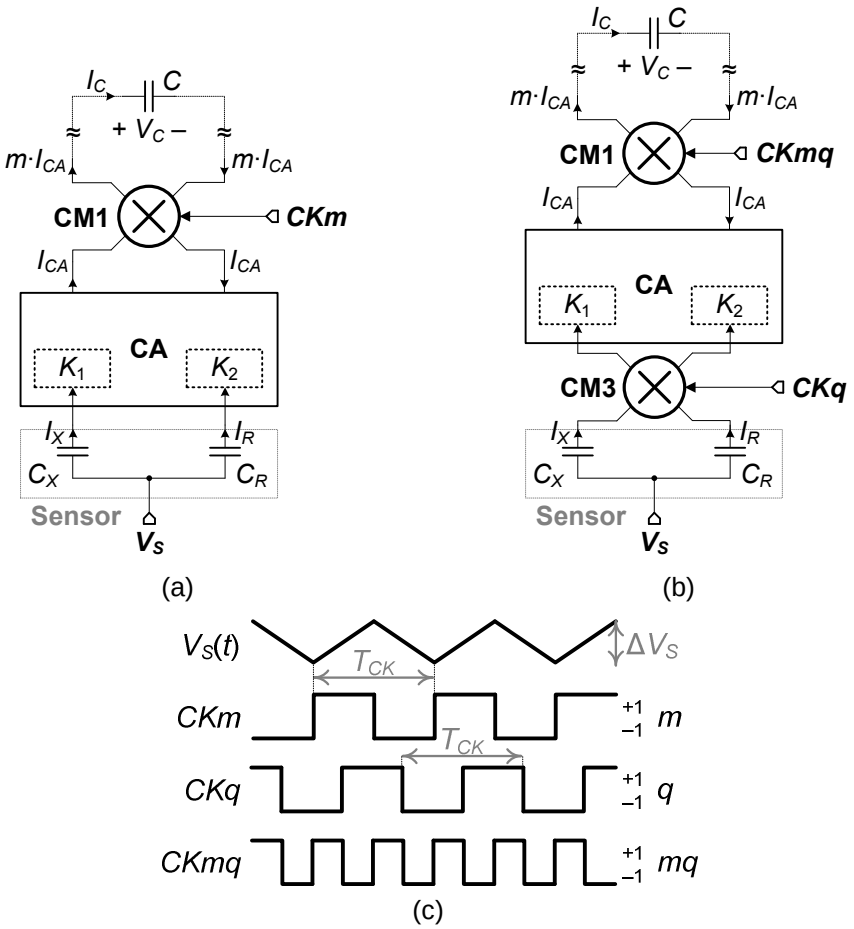


Fig. 4.27 – Simplified schematization of the C-to-PWM converter: (a) focused on the current amplifier (CA) function; (b) including a modulation / demodulation for the I_X, I_R currents. (c) Time diagram of the modulating signals $V_S(t)$, CK_m, CK_q, CK_{mq}.

This issue can be coped by sizing M1-M4 transistors with large gate area, high values of overdrive voltages ($V_{GS} - V_t$), and special matching procedure in the layout phase. Anyway, when dealing with very small bias currents, these design choices reflects on very long channel devices. This issue can be consistently mitigated adopting the scheme shown in Fig. 4.27(b), where a further chopper modulator (CM3) is used, and three clock signals *CKm*, *CKq*, *CKmq* are used. The idea is to realize a dynamic matching between the input ports of the CA block, so that, within a measurement cycle (T_{CK}), the input currents I_X, I_R are processed equally in time by the two K_1, K_2 mirror factors. The effect on currents, operated by a clock signal trough the chopper modulator, can be described by a modulating signal which assumes the (+1, –1) values depending on the clock signal value (high, low). Signal *m*, *q*, *mq*, associated to *CKm*, *CKq*, *CKmq* respectively, are shown in Fig. 4.27(c). For such signals the following relations hold:

$$m \cdot m = q \cdot q = 1; \tag{4.51a}$$

$$m \cdot q = m \cdot q = mq \neq 1. \tag{4.51b}$$

From the implementation point of view, a simple way to obtain the three clock signals is to start from a *CKmq* clock and deriving both *CKm* and *CKq* by halving the frequency on the former. The scheme shown in Fig. 3.7 uses two fed back D-edge flip-flop driven by the trailing and the falling edges of the input clock, respectively. It can be employed to produce *CKm* and *CKq* with a 90-electrical-degree phase relationship (quadrature), satisfying both of eqs. (4.51a-b).
For the circuit in Fig. 4.27(b) we have the chopping effect produced by CM3, we have in the two half cycles of *q*:

$$I_{CA} = \frac{1}{2} \cdot \left(K_1 I_X - K_2 I_R \right) \quad \text{for} \quad (q = 1); \tag{4.52a}$$

$$I_{CA} = \frac{1}{2} \cdot \left(K_2 I_X - K_1 I_R \right) \quad \text{for} \quad (q = -1). \tag{4.52b}$$

Using simple algebra, and eqs. (4.51a-b), we can find

$$I_{CA} = q \cdot \Delta K \cdot \frac{I_X + I_R}{2} + K_A \cdot \frac{I_X - I_R}{2}, \tag{4.53}$$

With respect to the ideal behaviour reported in eq. (4.14), we have the gain variation due to K_A, and a modulated term proportional to the sum of the two currents I_X, I_R. The ΔI_B, I_D and I_{CA} contributions to current I_C can be found. Note that modulation of currents ΔI_B and I_D is left unaffected, so their charge contribution is unchanged. For the $|I_{CA}|$ contribution, we have to consider the *mq* modulation operated by CM1. Using eqs. (4.50a-b):

$$I_C = m \cdot \left(\Delta I_B + \delta I_B + p \cdot I_D \right) + K_A \cdot \frac{\left| I_X - I_R \right|}{2}, \tag{4.54}$$

where the signal *p* has been introduced to describe the action of the output pulse waveform on I_D: p = “1” when P is high, p = “–1” when is low. The equivalent current δI_B has been also introduced

$$\delta I_B = \Delta K \cdot \frac{\left| I_X + I_R \right|}{2}, \tag{4.55}$$

which can be considered as an equivalent random deviation of the ΔI_B around its nominal value. Furthermore, eq. (4.55) is useful in the design phase, where we have to guarantee $\Delta I_B > |\max(\delta I_B)|$ for the correct operation of the circuit.
The circuit shown in Fig. 4.28, derived from scheme in Fig. 4.11, implements the modified CA block including the CM3 chopper modulator.

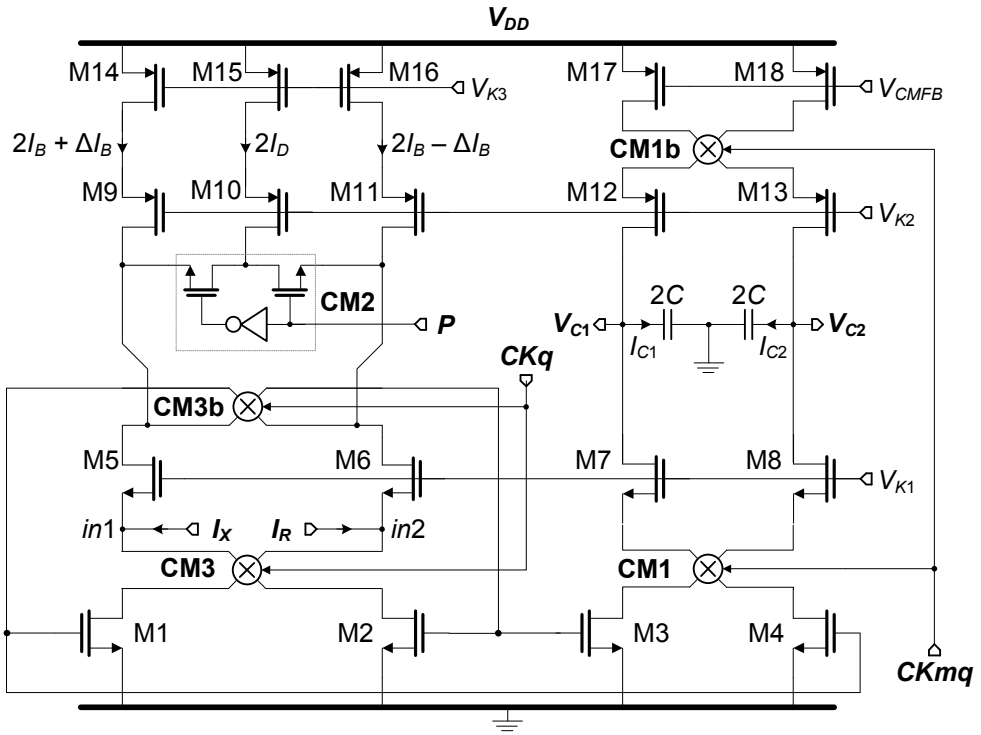


Fig. 4.28 – Schematic diagram of the CA block including also the function of I_D and ΔI_B current sources and CM1, CM2, CM3.

Simulations on a prototype showed an offset reduction on the output pulse up to the 3 % with respect to the full scale range, starting from more than 10 % of the circuit presented in section 4.2.1, on the basis of 20 Monte Carlo runs.

CONCLUSIONS

In this thesis work several aspects of the integrated sensors and their dedicated interfaces have been discussed. Firstly we presented the development of smart flow-meters capable to detect very small flow rates of both gases and liquids usable for numerous of application ranging from industrial, environmental to medical fields. Regarding the design of the sensing structures, sensor geometries have been optimized with the aid of finite element simulations. Prototypes based on very low cost packages have been fabricated and measured. With the implemented packaging technique, based on plastic top cap, distinct channels on a single sensing chip have been fabricated enabling multiple flow rate measurements capabilities.

The design of dedicated circuitry for signal extraction and conditioning has been also discussed. A CMOS instrumentation amplifier, based on chopper modulation has been prototyped under rational design guidelines with the aim to optimize the readout chain, preserving sensors dynamic range. An auxiliary readout chain compensates for pressure effects on sensor sensitivity extending the operative range to very low pressures.

A flexible driving has been exploited to obtain a robust cancellation of native sensor offset. The driving circuits also inspired the realization of an original full analog multiplier prototype.

Another important theme investigated in this work is the development of readout interfaces for capacitive MEMS sensors based on capacitive to pulse width modulation conversion, which can be employed for integrated accelerometers, gyroscopes, pressure sensors, angular displacement and chemical species sensors. Measurements demonstrated the extremely low power consumption (<100μW) and the low temperature sensitivity (<300ppm/℃) of the proposed circuit. Precision capabilities have been further investigated leading to performance improvement through simple topological modifications.

APPENDIX – DESIGN OF PIXEL SENSORS INTERFACE FOR HYBRID CMOS IMAGERS

In this appendix will be sketched the activity developed during an internship within the Integrated Circuits and Systems (ICAS) group of the "Instituto de Microelectrónica de Barcelona" (IMB-CNM) under the guidance of Prof. Lluís Terés i Terés and Dr. Francesc Serra-Graells. This is intended to be a very concise resume as the activity is currently being investigated.

A.1 Fast infrared imager

Imagers or image sensors are devices that capture light from an image and convert it in electrical signals. Nowadays the CCD technology is dominant in the visible and near infra-red (IF) portion of the electromagnetic spectrum. These devices are limited to see only the visible light of an external source (sun, lamps, etc.) reflected by objects. Extension of the detectable spectrum towards longer wavelengths represents an important improvement as it enables a myriad of applications ranging from night-vision protection systems up to non intrusive medical diagnostic systems. For these applications two main competitors can be considered: (i) optoelectronic imagers, (ii) microbolometers.
Optoelectronic imagers, despite their great performances, did not reach the mass market due to the high cost per device due to the complex technologies involved in their fabrication and due to the need to operate at cryogenic temperature. On the other hand amorphous silicon microbolometers can easily be integrated into the CMOS fabrication process, and do not need cooling, making these device more fit to the trend of MEMS market. Nevertheless they suffer from fundamental limitations such as low detectivity, slow response, low spectral discrimination and packaging issues which reduce their number of applications.
Recently, the CMOS/PbSe technology, developed at CIDA (Centro de Investigación y Desarrollo de la Armada, Madrid) laboratories, demonstrated to overcame these limitations [62], enabling the possibility to fabricate photonic IF detectors fully compatible with CMOS IC technology and without the need to be cooled. Other than that, the following characteristics can be remarked:

- good reproducibility;
- good uniformity over big wafer areas;
- long term stability;
- very simple and affordable technology with few added processing steps, and needed masks;
- possibility to integrate monolithically complex multilayer structures implementing spectral selective filters.

PbSe detectors showed higher sensitivities with respect to the silicon microbolometers, and a velocity of response at least one order of magnitude higher than other uncooled thermal detectors. Furthermore, thermals need vacuum to minimize the thermal conductivity associated to the environment surrounding the detector; for this reason, expensive packages are needed to extent the device lifetime, while PbSe devices, being photonic detectors, do not need any special package.

The PbSe/CMOS technology is a hybrid solution where a PbSe layer is deposited on top of a standard CMOS chip, by means of vapour phase deposition (VPS).
The imager sensor is formed by an array light sensing pixels is structured in the so called focal plane array (FPA): detectors are arranged in an array on the top PbSe layer. Each of them produces a current proportional to the incoming IR light. The bottom layer is the CMOS substrate where the active pixel sensor (APS) array circuitry is interfaced with the upper array. Each detector is connected one-by-one with its read-out CMOS circuit cell which conditions the currents coming from the detectors in order to be properly transmitted outside the array.
In the previous generation developed by the ICAS group, the imager design has been based on complete built-in A/D converters per pixel [63]. The image information is than transferred sequential at the end of acquisition phase. With this approach a remarkable performance of 10 kfps (frames-per-second) with a pixel feature size of 200 µm × 200 µm in a 3 × 10 array has been obtained. Now, with area reduction as the main design goal to obtain a pixel pitch of 40 µm for IR image sizes above 64 × 64, exploring a communication different strategy, based on address-event representation (AER).

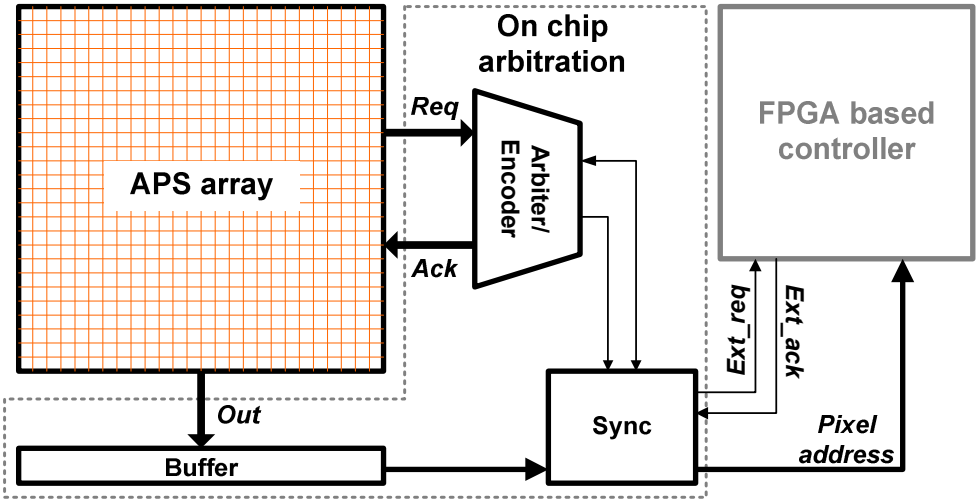


Fig. A.1 – Schematic diagram of an AER based imager.

A.2 Address-Event Representation (AER)

AER is an asynchronous, biologically inspired, communication technique that converts pixel activity in pulse frequency. Each pulse is referred to as event, while pixel activity is proportional to sensed light. All pulses are routed from the pixel array to a single asynchronous bus which is charged to send the address of the pixel producing events. Thus the output of the system is then a stream of addresses corresponding to pulsing pixels (i,j) position inside the array. Figure A.1 represents the typical arrangement of an AER communication scheme. The address stream is than processed by an external controller in order to add image

elaboration at a digital level. The frame can be rebuilt by simply counting the pixel activity in a given time.
Events collision happens when the two distinct events are produced almost synchronously. In order not to loose important information an arbiter has to be provided in order to grant bus access to one of the competitor pixels while queueing all the others. In this way, events collision is resolved by a slight time shift in event appearance. If event frequency is much higher than pixel signal bandwidth, than precise positioning of events in time is not critical. Events can be shifted up to a certain degree, without degrading the information content because the frame reconstruction is done by averaging in time [64].

A.3 Pixel interface electronics

The scheme shown in Fig. A.2 illustrates the architecture of the pixel interface. The sensor has been represented with a current source I_{PIXEL}. The I/DPM block collects the current produced by the sensor integrating it on a capacitor. When the integrated voltage pass a threshold set by a comparator stage the leading edge of the event signal is produced. The AER controller starts the communication protocol by pulling the request line Req[i] which is in common with all the pixels in the same row i. This signal starts the arbitration within requesting rows, if more than one have not yet been attended. At row-arbiter acknowledgement, the Ack[i] is pulled up, letting the AER controller to access to the Out[j] line. Again, Ack[i] is in common for all the pixels in the row i, so that the all row content is written into a buffer connected to all the Out[j] lines. At this point a second level of arbitration is possible between the “1” inside the buffer. This is not only solution, as the whole buffer can be transmitted in parallel through the bus. In this case the information is completed by adding the address of the selected row, realizing a semi-arbitrated AER. Obviously, this solution is more pad hungry but ensures very fast communication.

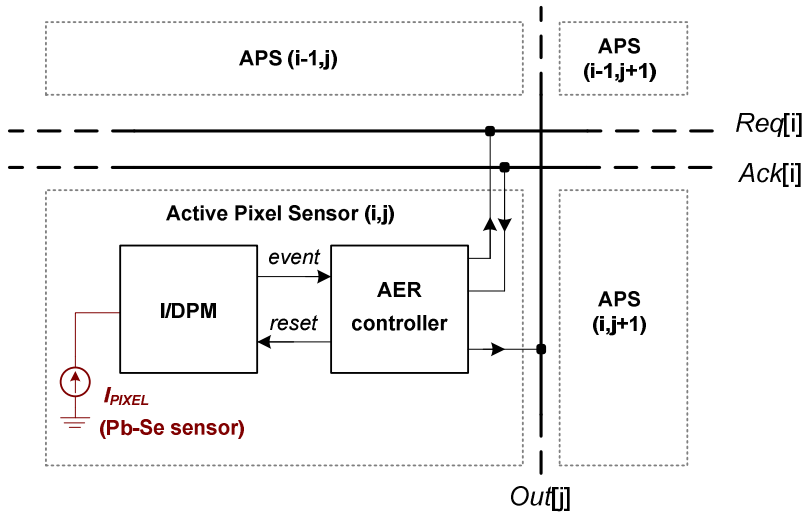


Fig. A.2 – Array architecture: communication wires at pixel level.

When the external device acknowledges the bus, the arbiter pulls down the Ack[i] line, disabling the pixel on row i to accessing the “Out” lines. At the same time the reset signal is transferred to the I/DPM: this signal enables the discharge of the internal capacitor and turn off the event signal so that a new communication cycle can begin.

The scheme of the pulse density modulator (I/DPM), shown in Fig. A.3, is inspired to the circuit in [65]. The integrator stage is formed by M1, M2 nominally identical and capacitors C_1, C_2 also nominally identical. The init switch is used to correctly polarize transistor M1 in the initialization phase. During the integration phase, the event switch is closed while the reset is opened, so that C_1 and C_2 charge simultaneously. The drain voltage of M1 decreases at constant rate (considering I_{PIXEL} constant during the whole integration phase). On the contrary, provided that the gain of M1 is high enough, its gate voltage is maintained constant, so that the V_{GD1} increase at constant rate. The same voltage is fed at the inputs of the OTA based comparator formed by M3-M10. Transistors M3-M4 are sized intentionally different, i.e. with different multiplicity factor, in order to set the threshold voltage of the comparator. Making M4 *m* times wider then M3 we have

$$V_{TH} = \left| V_{GS4} - V_{GS3} \right|_{I_{D3}=I_{D4}} = n \cdot \frac{KT}{q} \cdot \ln m \,, \tag{A.1}$$

supposing weak inversion operation for M3 and M4, where *n* is subthreshold slope according to the EKV MOSFET modelling.

On the setting event capacitor C_2 is disconnected from the drain of M1, maintaining the integrated voltage, while C_1 keeps integrating I_{PIXEL}. When the reset signal is ready C_2 is connected to the input of the integrator, so that the discharge of C_1 is obtained. The latter is not fully discharged and a net charge proportional to the delay δ between the event falling edge and the reset trailing edge is maintained. For the correct operation of the system:

$$\max(\delta \cdot I_{PIXEL}) < C_1 V_{TH} \,, \tag{A.2}$$

However, this arrangement represents a novelty with respect to classical integrator/reset schemes, as the integration of I_{PIXEL} on C_1 is not interrupted during the event time, and the integrator is operating in continuous-time during the full frame. As an important consequence, no signal is lost during the event arbitration phase which is not predetermined as it depends on the global activity of the pixels in the array.

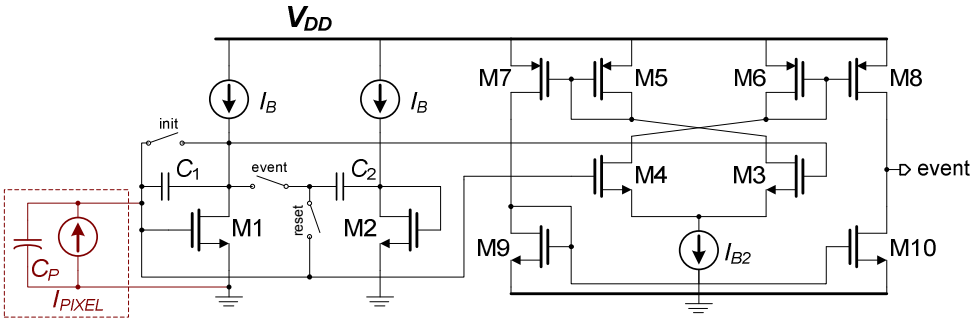


Fig. A.3 – Schematic diagram of I/PDM block.

The maximum pixel activity (pulse frequency) can be expressed as

$$f_{MAX} = \frac{\max(I_{PIXEL})}{C_1 V_{TH}}, \qquad \text{(A.3)}$$

which can be adjusted by choosing convenient values of C_1 and V_{TH}. Anyway, due to the very limited room available for the pixel, C_1 has to be kept quite small, in the 100 fF-200 fF range.
The topology of the AER controller is still object of investigation at present time, and will not be discussed here.
Transmission line delays and distortion on signals may considerably affect the communication protocol, especially when high speed is targeted. To take them in consideration the lumped element net in Fig. A.4 has been chosen to represent parasitics interconnections between adjacent pixel cells. Where R_A, R_B, R_C and C_A, C_B, C_C, C_{BC} are calculated with respect to the pixel pitch and considering the sheet resistances and the parasitic capacitances values given for the process. For the 0.35 µm CMOS used here, considering the typical process corners and implementing the Ack-Req and the Out lines with the metal3 layer (1 µm width, 3 µm spacing), and metal4 layer (1 µm width), respectively, we obtain the parameter values reported in inset table of Fig. A.4.

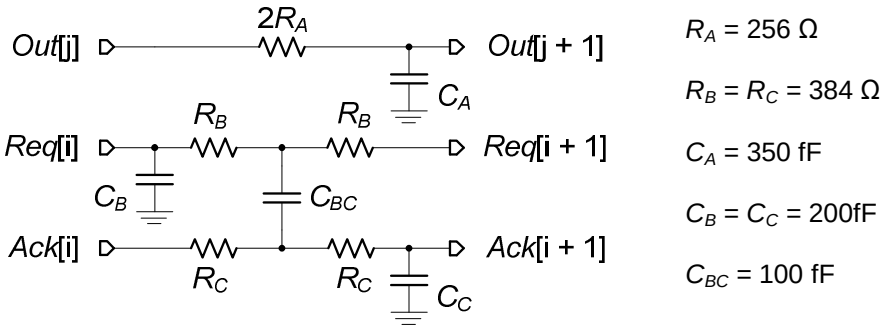


Fig A.4 – Lumped net for modelling line interconnections.

A.4 Arbitration

The main requirements for the arbiter circuit are architectural modularity and the capability to assign a priority code to conflicting events.
The modularity of the arbiter is obtained adopting a tree structure such of that shown in Fig. A.5. Colliding requests are resolved at each arbitration level, which let only one of the input requests (at nodes r1, r2) to access the output ro. The last arbiter node determines the end of the arbitration process; as the ro and ao terminals are shorted the acknowledgement signal retrace the path of the acknowledged request. The arbitration process introduces a delay proportional to the depth of the tree. During this period of time incoming events can be considered synchronous as their presentation time cannot be distinguished. In order to provide a stable arbitration process, each arbiter node A must lock its state once the ro signal is released at its output and hold it until the ao signal has come back.

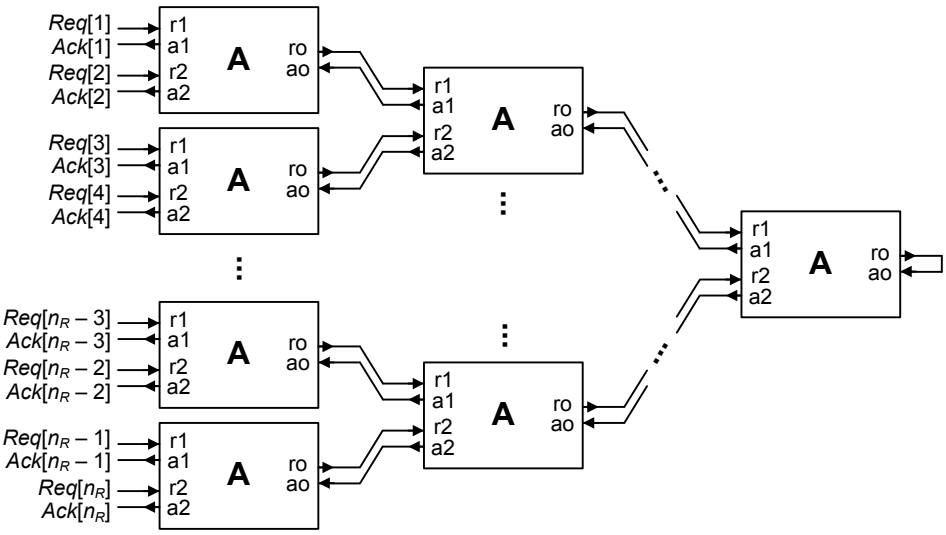


Fig. A.5 – Row arbitration tree structure, n_R is the number of arbitrated rows. Each arbitration node is a binary arbiter.

The row address can be extracted in several ways, for example, the peripheral Ack signal (leftmost in Fig. A.5) can be encoded to the attended row address.
Arbitration nodes based on fair arbitration are present in literature [66, 67]. With such structures, however the priority encoding cannot be implemented and some functionality like target tracking [68], or dynamic scene compression [69] cannot be implemented.

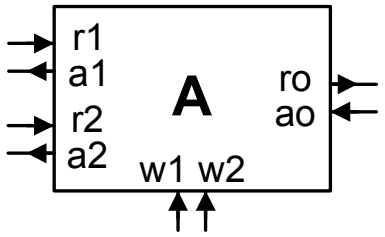


Fig. A.6 – Schematic diagram of an binary arbiter node with priority encoder.

An interesting alternative may be represented by a mixed analogic/digital solution for each arbiter node based on the winner take all (WTA) solution. Referring to the binary arbiter node in Fig. A.6, characteristic equations of an arbiter with priority encoding based on WTA are:

$$ro = r1 + r2 ; \quad (A.4)$$

$$wo = \max(r1 \cdot w1 + r2 \cdot w2) ; \quad (A.5)$$

$$a1 = ao \cdot S ; \quad (A.6)$$

$$a2 = ao \cdot not(S) ; \quad (A.7)$$

where wo is related to the arbitrated state S, and w1, w2 represent the priority encoding words. In facts, wo = w1 if S = 1, wo = w2 if S = 0. The main advantage of an mixed analog/digital solution is that the arbiter node can be easily extended to accept more than two senders (i.e. from binary to n-ary node), reducing the number of nodes required and the depth of the tree with potential benefits on speed. However, the limits of such solution are being still investigated, in order to critically evaluate the achievable performances and the effective advantages with respect to a fully digital arbitration tree when requirements on power consumption and occupied area are imposed.

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