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Analysis of transport properties and photoconductive response of single InAs nanowires

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Ai miei genitori

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Introduction

During the last half century, a dramatic downscaling of electronics has taken place, a miniaturization that the industry expects to continue for at least another decade.

Integrated circuits were invented in the late '50s and, since then, the transistor number on a circuit increased exponentially, doubling approximately every two years. This trend was first observed by Intel co-founder Gordon E. Moore in 1965 [1] and it is commonly known as Moore's law. Incredibly, this empiric law remained valid until nowadays and describes the driving force of a technological and social change in the late 20th and early 21st centuries.

However in the sub-50 nm scale the scaling process reaches technological and fundamental limits. Those distances become comparable to the atom size and quantum effects start to play an important role. Furthermore, reduced size devices are more affected by thermal noise and difficulties arise in controlling material composition (doping concentration).

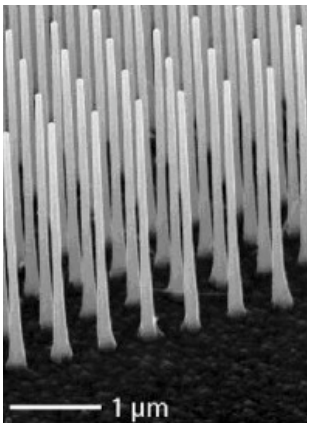


Figure 1: Nanowire *forest* [2].

The problem of miniaturization is not limited to devices, but it also applies to the conducting paths that connect them: lithography techniques are reaching their limits too. This implies that new technologies are needed to overcome the limitations that are raised by present scaling methods.

Semiconductor nanowires are suitable structures to play a fundamental role in this scenario. These objects are artificial structures of nanometer

size with an approximately cylindrical shape. They have an aspect ratio much larger than one so that, in most instances, they can be considered 1D systems. This peculiar property makes nanowires one of the most interesting technologies in the roadmap for electronics downscaling today.

At the moment epitaxial growth techniques allow to realize homogeneous and heterostructured nanowires of different materials, to control their diameter as far as few nanometers, and to create regular arrays as shown in Fig. 1. Nanowires are, however, still the object of scientific research and, even if nanowire transistor devices start to be investigated and developed, many physical aspects and characteristics are still to be understood.

In this thesis I have studied the transport properties of single nanowire transistors in a variety of configurations. The lateral-gate and the back-gate geometry were realized, measured and simulated using a finite element formalism. The simulation that I developed allowed the computation of electron mobility and charge density within the wires and the comparison among the results of different wire structures. Photoconductivity measurements were also attempted in order to directly explore the nanowire electronic band structure.

The thesis is divided into four chapters.

Chap. 1 Semiconductor nanowires. In the first part I will present the peculiarities of a semiconductor nanowire, discussing the features of the semiconductor material and the effect of the low dimensionality. Then I will explain the growth process of the different kinds of nanowires used in this work (homogeneous and radially heterostructured). The nanowires were grown in the NEST laboratory with the Chemical Beam Epitaxy (CBE) technique. The realization of nanowires can be explained with the Vapor-Liquid-Solid (VLS) model for the growth mechanism involving the seed of a gold particle. After the growth an important stage is to check the nanowires produced by Scanning Electron Microscopy (SEM) and Energy Dispersive X-Ray spectroscopy (EDAS).

Chap. 2 Transport and optical properties of nanowires. An introduction is given to the transport in mesoscopic structures distinguishing between ballistic and diffusive transport. The specific case of InAs nanowires transport is taken into account, discussing all the main factors that affect

transport (sample contacts, gate contact, temperature and nanowire size). A transport model is then presented for the single nanowire transistor configuration: with some approximations it is possible to estimate the electron mobility and the charge density in the wire. InAs is sensitive to mid-infrared light because of its small direct gap. After an overview on the electronic transitions related to photoconductivity, general properties of photoconductivity are described.

Chap. 3 Processing and experimental set-up. The fabrication of a nanowire device requires many steps using photo-lithography and electron-lithography techniques. All the steps I employed are accurately described establishing a methodology for the single nanowire transistor configuration. Then the set-up for transport measurements is presented as well as the one for optical measurements.

Chap. 4 Transport and photoconductivity measurements. In the last part the transport and optical measurements I performed are described. Transport results are discussed with the support of a finite element model that simulates the nanowire device. The model I developed in the case of a back-gate and a lateral-gate geometry in order to compute a more accurate capacitance of the nanowire-gate system. In this way a more reliable result on the electron mobility and charge density in the nanowire is estimated and compared with the literature results. First attempts to measure the photoconductive response of individual nanowire are also discussed examining in particular the influence of the substrate.

Chapter 1

Semiconductor nanowires

Nanowires are artificial structures of nanometer size with an approximately cylindrical shape. They can be made of metal, oxide or semiconductor material.

The nanowire's diameter can range from about 3 nm up to 100 nm or more, and the length can reach several microns. A commonly used definition of wire is that the aspect ratio (the length to diameter ratio) is much larger than 1, which is the case for the wires used in this thesis. In such a case we can consider the wire, from a geometrical point of view, to be a one-dimensional (1D) system. From a physics point of view the size at which the nanowire becomes one-dimensional is when its radius becomes comparable to the Fermi wavelength of the carriers. Semiconductors generally have long Fermi wavelength and are thus ideal for studying 1D phenomena, since the wire does not have to be extremely thin.

The nanowires used in this work are made of one semiconductor material (homogeneous nanowires) or by two different materials (heterostructured nanowires). In the latter case, the two semiconductors form a radial heterostructure with an inner InAs core surrounded by an InP shell, usually called "core-shell nanowire". Besides, the nanowires studied here are "free-standing". This means that they are surrounded by air and not buried in other semiconductor materials; it is then possible to transfer the wires on a host surface and subsequently contact and measure them.

In the following sections the peculiarities of a semiconductor nanowire are presented, discussing the features of the semiconductor material and the effect of the low dimensionality (in this case 1D). The last part presents the

growth processes of the different kinds of nanowires used in this work.

1.1 The semiconductor material

Matter can be highly organized in a regular pattern of atoms, ions or molecules with relatively fixed distances between the constituent parts. Such arrangement of a homogeneous solid is called crystal, which differs from amorphous materials with no regular pattern. In an ideal crystal the same structure is periodically repeated in three dimensions; it is then possible to define a lattice, whose sites are linked to a small group of atoms, called the base. The base can be composed by one or several types of atoms. It is important to notice that the crystal structure of the material determines many of its fundamental properties such as density, thermal, electrical and optical properties.

The crystal lattice can be considered in a first approximation as composed by fixed ions in their equilibrium positions. An atomic system organized with this order gives rise to a periodic potential $V(\mathbf{x}) = V(\mathbf{x} + \mathbf{a})$, which reflects itself on the solution form of the Schrödinger equation:

$$H\psi(\mathbf{r}) = [-\frac{\hbar^2}{2m}\nabla^2 + V(\mathbf{r})]\psi(\mathbf{r}) = E\psi(\mathbf{r}) \tag{1.1}$$

The n solutions of this problem can in fact be written in the form:

$$\Psi_{n\mathbf{k}}(\mathbf{r}) = u_{n\mathbf{k}}(\mathbf{r})e^{i\mathbf{kr}} \tag{1.2}$$

where $u_{n\mathbf{k}}(\mathbf{r})$ are functions with the same periodicity of the potential (Bloch functions) and k is a vector defined in the reciprocal space. The functions $\Psi_{n\mathbf{k}}(\mathbf{r})$ are periodic in k, so that $\Psi_{n\mathbf{k}+\mathbf{G}}(\mathbf{r}) = \Psi_{n\mathbf{k}}(\mathbf{r})$, where $\mathbf{G}$ is a vector of the reciprocal lattice. Because of this periodicity, it is common use to consider only $\mathbf{k}$ within the Brillouin zone.

Generic energy levels depend on two indices, n and k, where n is an integer number and k varies continuously in the Brillouin zone (supposing an infinite crystal). They form energy bands and it is possible to calculate the electron dispersion relation developing in a Taylor series close to band extremes. For example in the case of the conduction band:

$$E_n(k) = E_C + k^2 \left.\frac{d}{dk^2}\right|_0 = E_C + k^2\frac{\hbar^2}{2m^*} \tag{1.3}$$

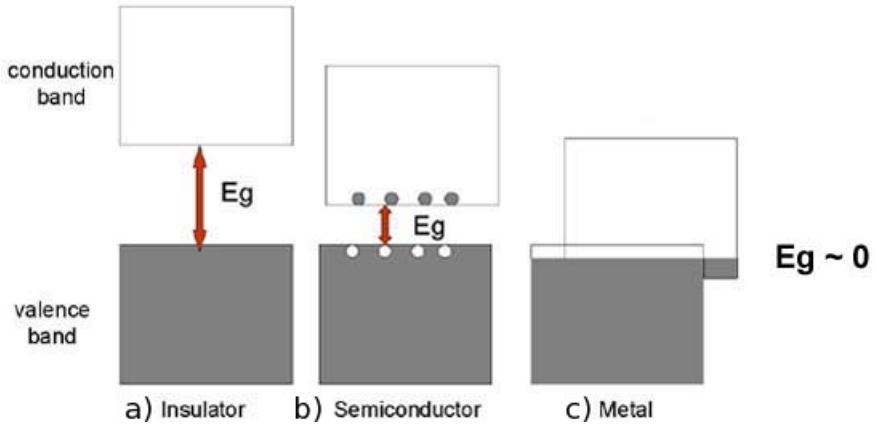


Figure 1.1: The band structure and the energy gap for a) an insulator b) a semiconductor c) a metal.

where m^* is the electron effective mass. The highest occupied energy level is called the Fermi level and its energy, E_F, determines several of the material properties.

Typically in a semiconductor material the energy band structure forms an energy gap [1] which separates the valence band from the conduction band.

The size of the energy gap is decisive for the transport properties of the material. As a matter of fact, to create a current, electrons need enough energy to access to the conduction band. Therefore materials can be labelled according to the energy gap size. While metals present no energy gap, semiconductors and insulators have the valence band fully occupied and the conduction band completely empty at zero temperature. In semiconductors, however, the gap energy is small enough for

Moreover the configuration of the gap is necessary to understand the optical properties phenomena. For instance, if the conduction band minimum and the valence band maximum occur at the same position in momentum space, the bandgap is direct and the material is optically active [3]; the emitted light has a frequency given by the size of the gap.

Silicon is by far the most important and well-known semiconductor material in today's electronic chips. Silicon is found in column IV in the periodic table. It has four valence electrons and a crystal structure called diamond structure. Germanium is another important semiconductor in the

[1] also commonly called "bandgap".

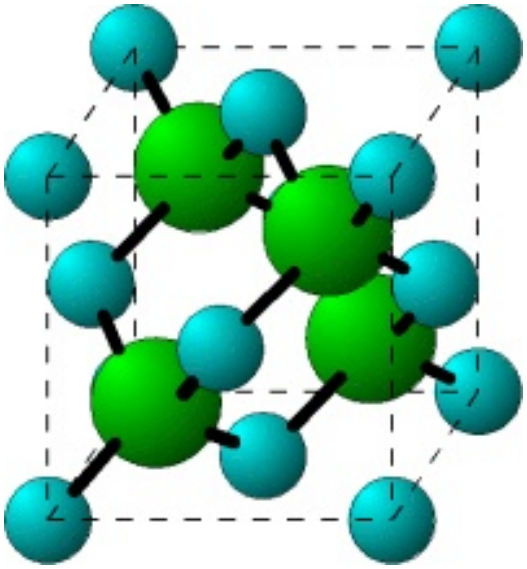


Figure 1.2: Zincblende, the most common crystal structure of III-V materials.

same group. Due to their indirect bandgap, Silicon and Germanium are not able to emit light, which of course is an important aspect in optoelectronic devices such as light emitting diodes or lasers, used for example in CD-players, optical telecommunication, etc. For such purposes another group of semiconductor materials is mostly exploited, the III-V compounds. Semiconductors in the III-V material system consist of atoms from group III (In, Ga, Al, B) and atoms from group V (Sb, As, P, N).

The most common crystal structure of III-V materials is called **zincblende** structure after ZnS (zincblende), which has a face-centered cubic (fcc) structure with two different atoms in the base, see Fig. 1.2. With two identical atoms in the base, the silicon (diamond) structure would be recovered. Alternatively another possible crystal structure for various binary compounds is the **wurtzite** structure. Wurtzite is an example of hexagonal crystal system and is not the favoured form of the bulk crystal, but can be favoured in some nanocrystal forms of the material.

The nanowires grown in our laboratory and studied in this thesis are made of InAs or InAs with a shell of InP, which are, at the moment, the materials providing the best results for the bottom up catalytic growth.

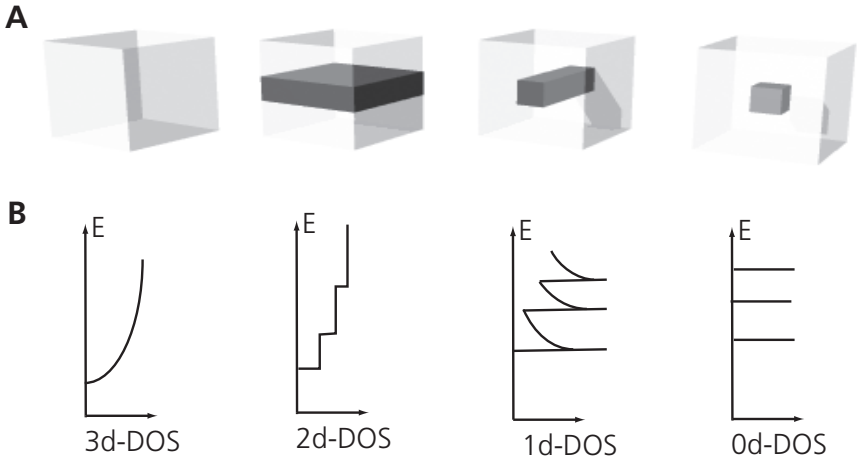


Figure 1.3: Sketch of different dimensionalities (**A**) with corresponding density of states ρ(E) (**B**). From the left to the right: 3D-structure (bulk), 2D-structure, 1D-structure and 0D-structure [4].

1.2 Low dimensionality

When the size of the material sample decreases, the electron motion starts to become confined. At lengths of the order of the electron wavelength, quantization of the electron motion arises and the corresponding structures are called low-dimensional structures. Since for semiconductors the electron wavelength is in the nanometer range, semiconductor nanostructures have to be considered low-dimensional structures.

The dimensionality strongly affects the number of available energy states at a given energy, as it shown in Fig.1.3. The difference between the 3D and the 1D case can be taken as example. In 3D, or bulk case, the density of states (DOS) increases as the energy above the conduction band increases following a square root law. In the 1D, i.e. the quantum wire, the DOS is sharply peaked at each subband edge and decreases with energy. These are the expressions for the two different cases:

$$\rho_{3D}(E) = \frac{(2m^*)^{3/2}}{2\pi^2\hbar^3}(E - E_c)^{1/2} \tag{1.4}$$

$$\rho_{1D}(E) = \sum_{n_x,n_y} \sqrt{\frac{(2m^*)}{\pi^2\hbar^2}\frac{1}{(E - E_{n_x,n_y})}}\Theta(E - E_{n_x,n_y}) \tag{1.5}$$

The peaked nature of the DOS in the 1D case should give very sharp optical emission lines with energies corresponding to the bandgap plus the quantization energy, which is tuneable by changing the diameter of the wire.

As already mentioned at the beginning of the chapter, semiconductor nanowires are suitable as 1D electronic system because the carrier Fermi wavelength is comparable to the nanowire diameter. Electrons can be considered as free along the nanowire axis direction, but are confined in the other two. In the effective mass approximation, the electron wavefunction can be discussed with the envelope-function approach.

The total electron wavefunction $\Psi(\mathbf{r})$ can be written as the product between the lattice-periodic Bloch function of band n at the $\mathbf{\Gamma}$ point (center of the Brillouin zone) $u_n(\mathbf{r})$, varying on the scale of the crystalline periodicity of the host material, and an envelope function $f_\nu(\mathbf{r})$ varying slowly compared to $u_n(\mathbf{r})$:

$$\Psi_\nu(\mathbf{r}) = f_\nu(\mathbf{r})u_n(\mathbf{r}) \tag{1.6}$$

where ν is the quantum number. The envelope function $f_\nu(\mathbf{r})$ depends on the wire potential and on external potentials such as electric and magnetic fields. Equation 1.6 is simply a generalization of the usual Bloch ansatz for a bulk crystal (see Eq. 1.2), where the envelope function $f_\nu(\mathbf{r})$ reduces to a plane wave $e^{i\mathbf{kr}}$.

The calculation of the electronic energy levels reduces to solving the following Schrödinger equation for the envelope function $f_\nu(\mathbf{r})$:

$$\frac{\hbar^2}{2m^*}\nabla^2 f_\nu(\mathbf{r}) + V(\mathbf{r})f_\nu(\mathbf{r}) = \epsilon_\nu f_\nu(\mathbf{r}) \tag{1.7}$$

where $V(\mathbf{r})$ is the confinement potential. This potential depends only on the directions orthogonal to the wire length thus the wavefunction is separable into a transverse part and a longitudinal part. The eigenvalues of Eq. 1.7 can be written as the sum of a discrete energy due to quantum confinement and the kinetic energy relative to the plane wave propagating in the z direction:

$$\epsilon_\nu = E_{n_1,n_2} + \frac{\hbar^2 k_z}{2m^*} \tag{1.8}$$

where n_1 and n_2 are the quantum numbers for the confined directions and k_z is the momentum along the nanowire axis.

1.3 Growth

The growth of a nanowire is the formation of a nearly 1D crystal. The evolution of a crystal from a vapor, liquid or solid mother phase involves two fundamental steps: nucleation and growth. The nucleation can be induced from an high concentration of the mother phase so that homogeneous nuclei are formed. These nuclei serve as seeds for further growth to form larger clusters. Of course in a method for generating nanostructures it is very important to control the dimension shape and uniformity. Several synthesis strategies have been developed for the creation of 1D nanowires, but the most successful methods for generating single-crystalline semiconductor nanowires are based on the introduction of a liquid-solid interface. This method is called vapor liquid solid (growth) mechanism.

1.3.1 The Vapor-Liquid-Solid model

The core of the Vapor-Liquid-Solid (VLS) mechanism is the introduction of a liquid solid interface in growth from vapor-phase , breaking the symmetry of the isotropic substrate crystal, and forming growth of a 1D structure. A metal particle is employed to form a liquid alloy with the material supplied from the vapor phase. At a certain temperature the composition of the alloy will be in equilibrium. When more growth material is supplied at this temperature, the alloyed particle becomes supersaturated, which results in nucleation and growth below the particle itself.

The metal particle will not be consumed during growth and can therefore be seen as a catalyst for 1D growth. The diameter of the wire is dictated by the size of the liquid particle and remains essentially unchanged during the entire growth. The major requirement on the metal in VLS growth is that it must form a liquid solution with the growth material at the growth temperature, and be able to create a supersaturation acting as driving force for crystallization of the nanowire material.

This can be achieved if the metal and the growth material form a eutectic

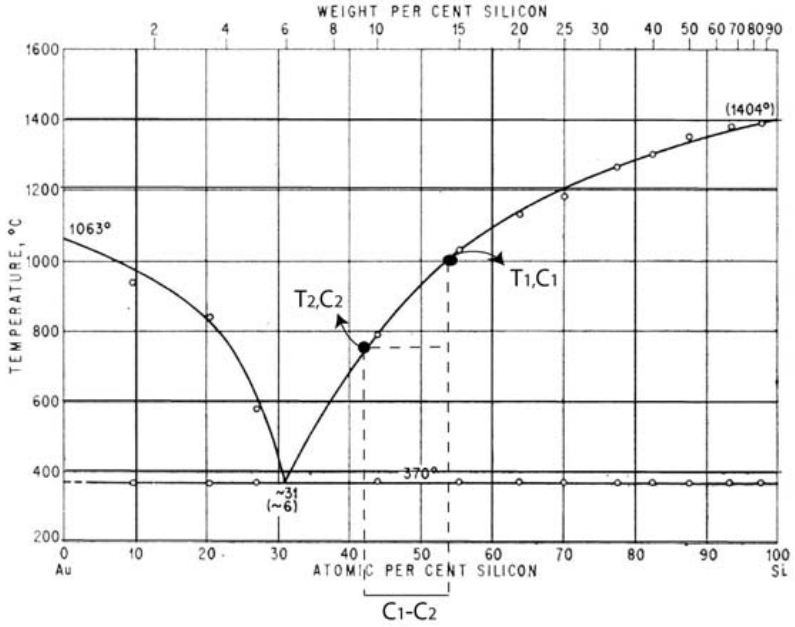


Figure 1.4: Phase diagram of gold and silicon [6].

compound. [2] The so called liquidus line ("melting temperature line") will, in a binary phase diagram, have a minimum at a certain composition; this minimum is called the eutectic point. It is therefore important to analyze the phase diagrams of the metal and the material of the desired nanowire to be able to select an appropriate catalyst.

The VLS process can be explained in view of the binary phase diagram of the material to be grown with the catalytic material. As an example we will describe the growth of silicon nanowires with Au catalyst. The phase diagram is shown in Fig. 1.4. The process is very similar for many other semiconductor systems, including InAs and InP.

First the metal particles, in this case gold, are placed on a semiconductor surface, see Fig. 1.5 **A**). The semiconductor surface with the gold particles is then heated to a temperature T1, higher than the eutectic temperature, where the silicon and gold are forming a liquid alloy of a certain composition C1 (Fig. 1.5 **B**). The temperature is thereafter lowered to the growth tem-

[2] A eutectic or eutectic alloy is a mixture in such proportions that the melting point is as low as possible, and that all the constituents crystallize simultaneously at this temperature from the molten liquid solution [5].

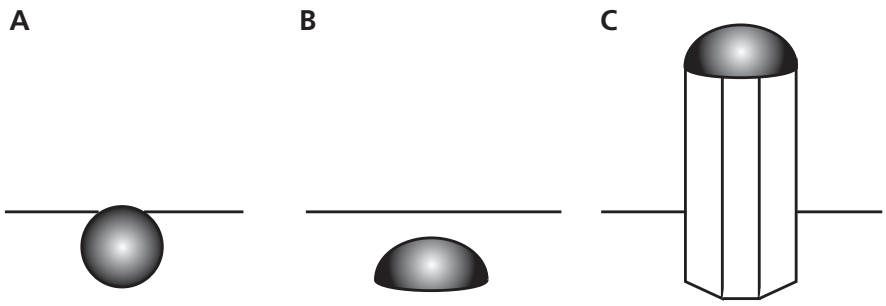


Figure 1.5: The Vapor-Liquid-Solid mechanism **A**) Nanometer sized particles are deposited on the surface of a crystalline substrate. **B**) When the temperature is increased the particles melt and start to incorporate the growth species **C**) An eutectic alloy is formed and when the particle becomes supersaturated the crystal growth starts [4].

perature T2 that, according to the phase diagram, has a lower concentration of silicon C2. The supersaturation now prevailing (C1-C2), acts as a driving force for nucleation and growth. The semiconductor material starts to precipitate at the liquid-solid interface and a dendrite structure will rise under the liquid particle (Fig. 1.5 **C**). To keep the supersaturation, the semiconductor material is supplied to the seed particle via the vapor phase during the whole growth. The molten phase is established on a solid, generally a crystal surface of the same material that is grown. In the case of a crystal substrate the nanowire will inherit the crystal structure. However, the nanowires will grow along some specific crystallografic directions. Si and III-V semiconductor nanowires generally grow preferencially along the <111>B direction.

Depending on which technique is used, the growth species can be atoms or more complex molecules that are decomposed close to or on the substrate surface.

The VLS model was developed over 40 years ago to explain 1D nanowire growth [7], but even now there are some doubts about the completeness of the model in explaining this kind of growth phenomena [8], [9]. A recent review work of K. Dick gives an overview of the different growth theories and describes the progress toward a unified theory of growth, showing that there are still some unclear aspects [10].

1.3.2 Chemical beam epitaxy

Chemical Beam Epitaxy (CBE) combines a physical beam epitaxial technique like molecular beam epitaxy (MBE) and the use of metal-organic gas sources similar to those used in Metal Organic Chemical Vapor Deposition (MOCVD). The apparatus consists of a UHV growth chamber pumped by a high capacity turbo pump so that the chamber base pressure is below 10^{-8} mbar.

At such pressure the mean free path is longer than the distance between the source inlet and the substrate. The transport becomes ballistic (collision free) and occurs in the form of molecular beams. The exclusion of the gas diffusion in the CBE system means that we obtain a fast response in the flow at the substrate surface, which makes it possible to grow atomically abrupt interfaces in heterostructures.

The low pressure condition is maintained by several mechanical vacuum pumps. Additionally a hollow cylinder, filled with liquid nitrogen, (called cryo-shroud) performs the main pumping work for everything except N_2 and H_2. The cryo-shroud helps in pumping away species that desorb from the substrate. It prevents contamination of the growing surface layer and reduces the memory effect of the previously used source chemicals.

The sources used for CBE are in liquid phase and contained in bottles with an overpressure with respect to the chamber. The bottles are stored in constant-temperature baths and by controlling the temperature of the liquid source, the partial pressure of the vapor above the liquid is regulated. The growth sources (precursors) used are the metal-organics trimethylindium (TMIn) as group-III source and tertiarybutylarsine (TBAs) and tertiarybutylphosphine (TBP) as group-V sources.

The vapor is fed into the chamber through an inlet valves. The source injector is responsible for the injection of the gas sources into the growth chamber and for the generation of molecular beams with stable and uniform flux. The source beam impinges directly on the heated substrate surface with an incidence angle from the normal of about 30°.

The group-V precursor is thermally cracked, to predominantly As_2 or P_2 molecules, prior to entering the growth chamber. In contrast, the group-III precursor decomposes at the substrate surface. Either the molecule gets enough thermal energy from the surface substrate to dissociate in all its alkyl radicals, leaving the elemental group-III atom on the surface, or the molecule

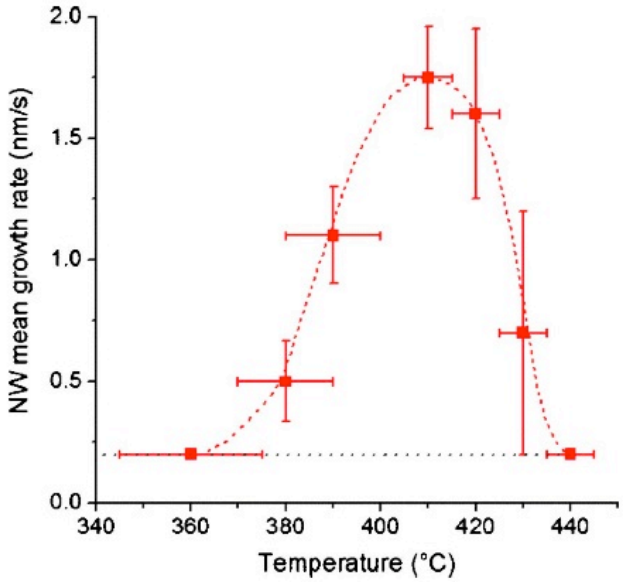


Figure 1.6: InAs NW mean growth rate as a function of temperature. The nominal deposition rate is 0.2 nm/s indicated with a dotted line. The dashed line represents a guide for the eyes. [11].

desorbs in an undissociated or partially dissociated way.

Which of these processes dominates depends on the temperature of the substrate and the arrival rate of the molecules to the surface. At higher temperature the growth rate will be limited by the materials supply and at lower temperatures will be limited by the alkyl desorption, since the alkyl groups block the sites. Fig. 1.6 shows a typical growth rate of nanowires.

Fig.1.7 a schematic diagram depicts the basic CBE set-up. In figure 1.8 shows two photographs of the CBE used in the NEST laboratory.

Technical details about growth

In the following, the details of nanowires growth by CBE will be outlined. The focus will be on InAs nanowires and heterostructures of InAs and InP, but the principle holds for any material. The fabrication starts with an epi-ready InAs <111>B substrate cleaved into smaller pieces, typically 1 cm^2. Au nanoparticles are then deposited on the surface. Such deposition can be obtained by different approaches, for instance by depositing a gold areosol

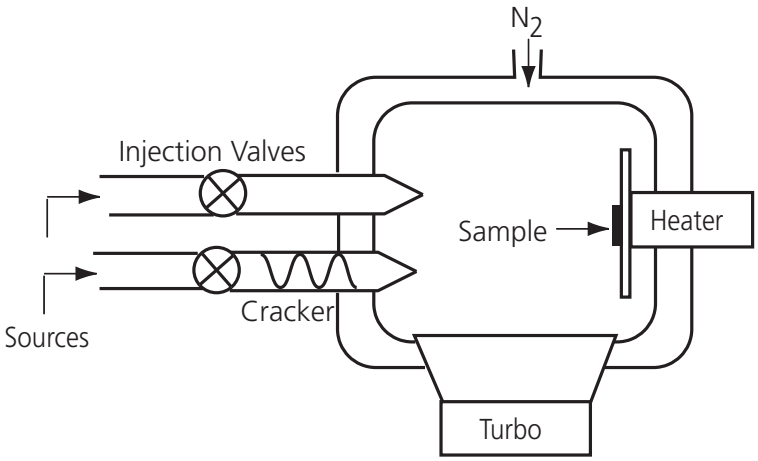


Figure 1.7: Schematic diagram of the CBE system. The sample is mounted on a sample holder inside an ultrahigh vacuum chamber, which is liquid nitrogen cooled. The growth species are introduced into the chamber manually or via computer controlled inlet valves and are directed towards the sample [4].

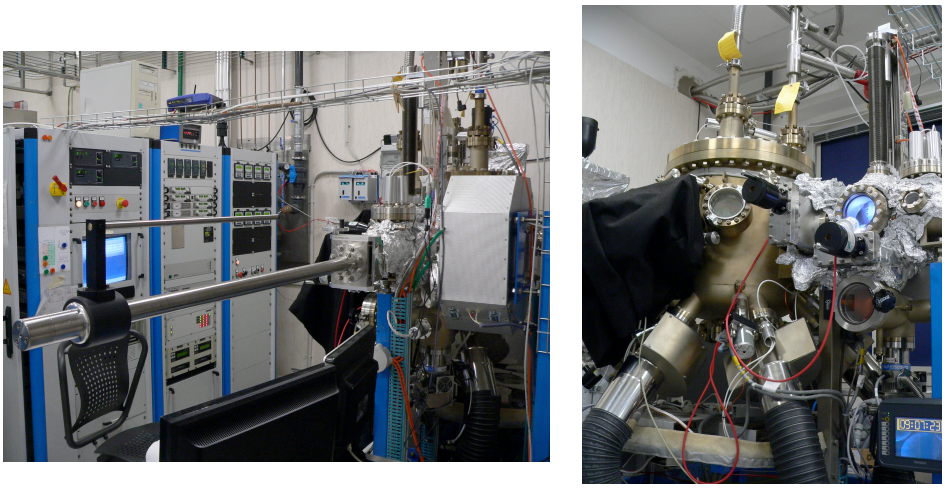


Figure 1.8: Two views of the CBE apparatus used in the NEST laboratory to grow nanowires. The brand and model are RIBER C21.

or by dispersing a colloidal solution containing gold nanoparticles. With both these approaches it is possible to have control of surface coverage and particle diameter (the size distribution is about 10%), for different particle materials. Alternatively other used techniques to create the gold catalytic particles are electron beam lithography (EBL) and nanoimprint lithography

that can be used to define any pattern of Au discs on the substrate surface. A final technique is the deposition of a thin Au film that coalesces into droplets upon substrate heating.

Once the sample is conveniently prepared with one of the techniques listed before, it is mounted on the CBE sample holder. The sample is then loaded into the load lock and transferred to the preparation chamber, where it is heated at around 200 °C to degas adsorbed substances. Once degassed it is mounted in the growth chamber where, for a variable time between 2' and 30' at around 500 °C, deoxidation is performed followed by the growth itself.

The details of the different nanowires used in this work are here summarized:

- 40 nm diameter homogeneous InAs nanowires

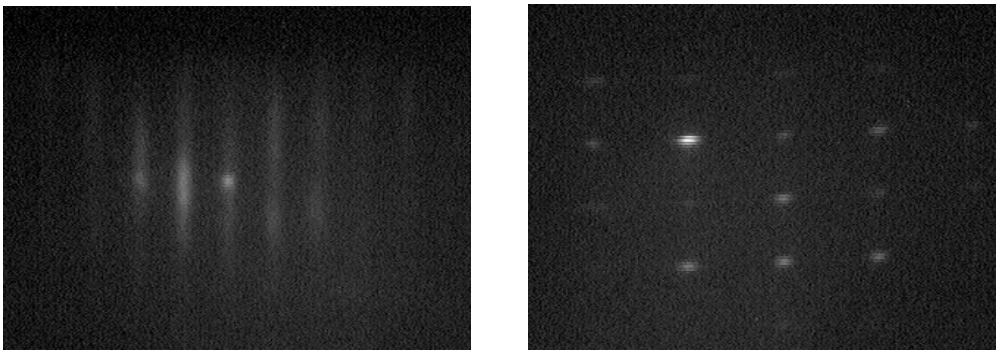
  Nanoparticles with a 30 nm diameter, in a colloidal solution, are used as catalyst. The surface is deoxidated in a TBAs flux, at 503 °C for 20 minutes. The growth temperature is 418 °C and fluxes of TBAs and TMIn are appropriately controlled. Growth time is 45 minutes and, at the end, the flux of TMIn is closed and the sample is cooled down in flux of TBAs.

- 20 nm diameter homogenous InAs nanowires

  A different method to obtain the Au catalyst particles is used. A very thin layer of gold (nominally 0,1 nm) is deposited on the InAs sample with a thermal evaporator. During the deoxidation (2 minutes at 500 °C in TBAs flux) Au particles of about 20 nm diameter are formed by surface de-wetting. The growth conditions are approximately the same of the previous case. In this case the growth time is 120 minutes.

- core-shell nanowires

  The process is similar to the 40 nm diameter homogenous nanowires, but to grow the shell there is a further step. The flux of TBA is interrupted and the temperature lowered from 420 °C to 370 °C . Then fluxes of TBP and TMIn are activated at the same time in order to grow the shell for 5 minutes. The process ends closing the flux of TMIn and cooling down in TBP flux.



(a) (b)

Figure 1.9: RHEED images: (a) after the surface deoxidation and (b) after the nanowires growth.

A reflected high-energy electron diffraction (RHEED) system is installed to control the status of the growth in the chamber and is used to monitor the surface properties of the sample. This allows for instance different surface reconstructions and growth modes (2D or 3D) to be distinguished. A surface oxide gives no diffraction pattern, therefore the deoxidation of a surface can be monitored in-situ as the diffraction pattern forms (see Fig RHEED (a)). Additionally, the formation of 1D structures as nanowires gives a typical signal as shown in Fig. 1.9 (b).

1.4 Nanowire imaging

Once the growth is completed it is necessary to analyse if the nanowires have the desired structure and dimensions. Due to their small size it is not possible to use an ordinary light microscope, which has a resolution limited by the wavelength of the visible light. Instead of light, accelerated electrons can be used as illumination source allowing the imaging of objects down to the order of a few Ångström (10^{-10} m).

Nanowires have been observed and analysed with a scanning electon microscope (SEM) and with a transmission electron microscope (TEM). Besides core shell nanowires were analysed with energy-dispersive x-ray spectroscopy.

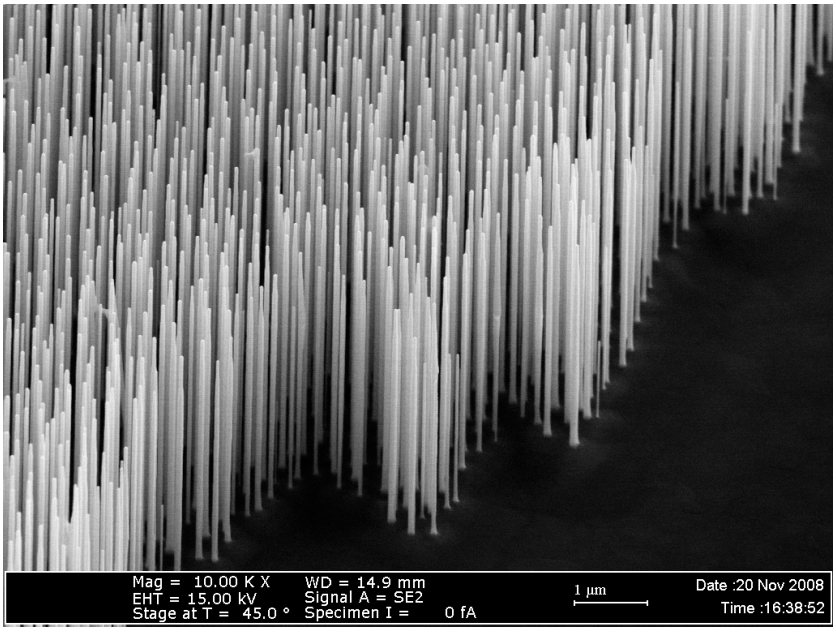


Figure 1.10: This figure shows InAs nanowires grown in our laboratory by CBE. This picture has been taken with the scanning electron microscope (SEM) shown in fig.3.3.

1.4.1 Bulk nanowire imaging

Scanning Electron Microscope

The SEM produces images by probing the specimen with a focused electron beam that is scanned across a rectangular area of the specimen. This scanning is obtained by deflecting the beam with an electromagnetic field. At each point on the specimen the incident electron beam loses some energy, and the lost energy is converted into other forms, such as heat, light emission (cathode-luminescence) or x-ray emission. Among these different effects the basic signal is the detection of electrons that are generated inside the sample, secondary electrons, electrons that have been scattered out of the sample, back-scattered electrons. The resolution of the microscope is determined by how well the electron beam can be focused. A practical limit for the SEM used in this work is 3-5 nm.

The SEM provides valuable information about the structural arrangement, spatial distribution, surface morphology, wire density and geometrical features of the nanowires. Fig. 1.10 shows a SEM image of InAs nanowires.

Transmission Electron Microscope

In order to study the nanowires on the atomic scale and to get more detailed information about material composition, crystal structure and crystal quality, the natural choice of imaging tool is the transmission electron microscope (TEM). The TEM uses electrons that are transmitted and scattered by the sample and therefore the sample or specimen studied needs to be very thin. The scattering of the electrons can be given by different contributions: they can be scattered elastically or inelastically, and they can also be scattered coherently or incoherently, given the wave nature of the electron.

Usually the elastically scattered electrons are coherent, when scattered at small angles, and inelastically scattered electrons are incoherent due to the loss of energy and, hence, the change in wavelength. The scattering can also be characterized by different angular distributions, and electrons are said to be either back or forward scattered. The forward scattering causes most of the signals used in the TEM and includes e.g. elastic scattering, inelastic scattering, and diffraction.

A nanowire TEM image is shown in Fig. 1.11. For two wires the gold cap is clearly visible at the nanowire end. Information on the nanowire structure are given by the different colour intensity; shaded parts are evidences of the fact that these nanowires are not completely straight.

1.4.2 Core-shell nanowire imaging

Energy dispersive X-ray spectroscopy (EDS) is an analytical technique used for the elemental analysis or chemical characterization of a sample. It is one of the variants of X-ray flourescence (XRF) and is particulary suitable to analyse the structure of a nanowire formed of two different chemical substances. As a type of spectroscopy, it relies on the investigation of a sample through interactions between electromagnetic radiation and matter, analyzing X-rays emitted by the matter when hit with charged particles.

To stimulate the emission of characteristic X-rays from a specimen, a high energy beam of charged particles such as electrons or protons, or a beam of X-rays, is focused into the sample under study. EDS characterization capabilities are due in large part to the fundamental principle that each element has a unique atomic structure allowing X-rays that are characteristic of an element's atomic structure to be uniquely identified from each other

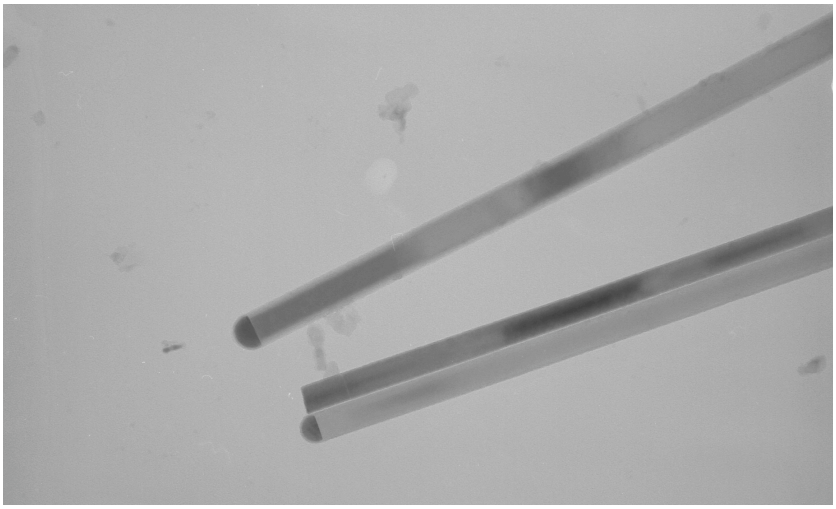


Figure 1.11: TEM image of InAs nanowires. The gold catalyser is clearly visible at the wire top and the shaded part is due to the fact that the nanowires are not perfectly straight.

[12].

EDS applied to core-shell nanowires gives evidence of the inner structure with high precision. Results of such analysis on InAs/InP nanowires are shown in Fig. 1.12. Contributes of phosphorus and arsenic are shown in the first and in the third image respectively. In the third image the two contributions are summed reconstructing the core-shell structure.

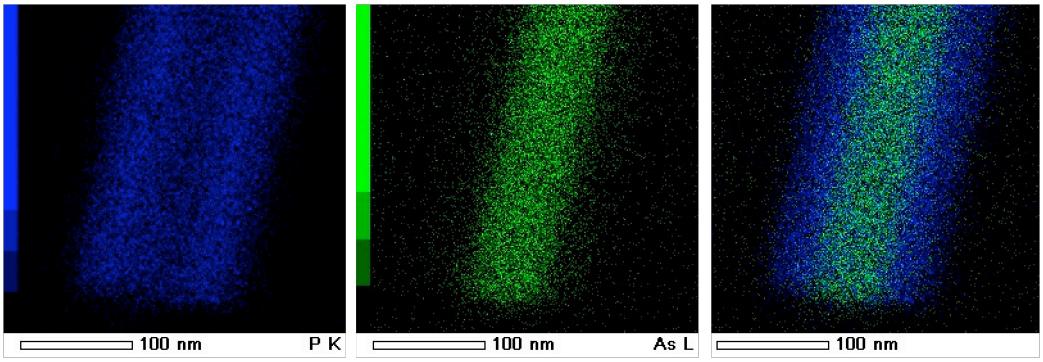


Figure 1.12: Energy dispersive X-ray spectroscopy (EDS) of a core-shell InAs/InP nanowire grown at the NEST laboratory. This analysis was performed in the CNR IMEM Institute in Parma (Italy).

Chapter 2

Transport and optical properties of nanowires

As mentioned in the previous chapter, semiconductor nanowires have interesting properties stemming from their low dimensionality. InAs nanowires are under research focus for their suitable role in advanced electronics. To realize new semiconductor devices based on nanowires it is first necessary to understand their transport properties. In addition III-V semiconductor materials could also be integrated in optical devices. For instance nanowires would offer interesting possibilities in order to create a nanoscale photodetector. Such photodetector could be integrated in photonic circuits, optical switches and interconnects, as well as near-field and high-resolution imaging systems.

In the present work I have focussed on the transport and the optical properties of individual nanowires. This approach necessitates that the single nanowire is electronically contacted. A classic transistor configuration was adopted creating a source, a drain and a gate contact.

In this chapter I discuss first the general properties of transport in nanowires. Afterwards specific InAs nanowire is presented with a simple model that allows to calculate electron mobility. In the second part of the chapter the optical properties of a semiconductor nanowire and its photoconductive response are analysed.

2.1 Transport properties

2.1.1 Transport regimes in nanostructures

The conductance (G) of large samples obeys an ohmic scaling law: $G = \sigma w/L$, where σ is the conductivity and L,w are sample length and width respectively. In general, though, there are two corrections to this law. Firstly there is a resistance independent of the length L at the contact interfaces. Secondly, as we go to nanoscale dimension, the conductance does not decrease linearly with w, as it depends on the number of transverse electronic modes in the conductor but decreases in discrete steps.

This transport regime is called ballistic and differs from the usual diffusive one. It is important to know in which transport regime the device works. Three different length scales have to be considered in electrical transport.

The first one is the electron wavelength λ. It turns out that at low temperature only the electrons within a range of $\sim k_B T$ from the Fermi energy (where k_B is the Boltzmann constant) contribute to the transport, meaning that the important wavelength is the Fermi wavelength λ_F . The Fermi energy is the energy of the highest occupied energy level at zero temperature and is directly related to the carrier concentration.

The second length scale is the mean free path or the elastic scattering length l_e, which is the average distance an electron travels between two successive scattering events. The mean free path is given by:

$$l_e = v_F \tau \tag{2.1}$$

where v_F is the Fermi velocity, related to λ_F, and τ is the average time between two scattering events. From the Drude microscopic model the carrier mobility is defined as:

$$\mu = \frac{e\tau}{m^*} \tag{2.2}$$

where e is the charge and m^* the effective mass of the electron.

The mean time τ is affected by momentum changes caused by scattering on material imperfections such as impurities, surface roughness, phonons, etc.

The third length scale is the phase coherence length l_φ. This is the distance an electron travels before the phase information is lost. For low mobility

samples ($l_e \ll L$) it is given by:

$$l_\varphi = \sqrt{D\tau_\varphi} \tag{2.3}$$

Here D is the diffusion constant and τ_φ is the phase-relaxation time determined by *dynamic* scatterings. *Dynamic* scattering events like electron-phonon and electron-electron scatterings are responsible for the phase relaxation. Impurity scattering too can be phase-randomizing if the impurity has an internal degree of freedom so that it can change its status [13].

These three length scales determine which transport regime is characteristic for a specific sample. Two limiting cases can be readily identified:

- if $l_e \gg L$ and $l_\varphi > w$, ballistic transport takes place. In the ballistic regime the two terminal conductance is given by the Landauer formula [13]:

$$G = \frac{2e^2}{h} M\mathcal{T} \tag{2.4}$$

  The two terminal conductance is then quantized in units of $2e^2/h$, where h is the Plank constant, if the transmission probability $\mathcal{T}$ is equal to the unity. $\mathcal{T}$ is defined as the probability that an electron has to be transmitted from the contact to the sample. The number of occupied conductive channels M, can be estimated by $M = int\{2w/\lambda_F\}$. Each conductive channel corresponds to a quantized state in the transverse direction. For perfect transmission, the resistance should in principle be zero; however, the finite values of Eq.2.4 arise from the scattering taking place at the contact points of the sample. It is worth noting that by using a four terminal configuration it can be experimentally proven that the resistance of a ballistic nanowire vanishes [14].

- when $l_e \ll L$, $l_\varphi \ll w$, $\lambda_F \ll w$, the transport is referred to as diffusive, and the conductivity is given by the Drude expression [15].

$$\sigma = en\mu \tag{2.5}$$

  where n is the carrier concentration.

These are two limiting cases, but many intermediate regimes can be distinguished. For instance semi- ballistic is observed in Ge/Si nanowires [16], however, in most experiments the transport is diffusive.

2.1.2 Transport in InAs nanowires

In the NEST laboratory nanowires are preferably produced in InAs because of their favorable transport properties. As a matter of fact, it turns out that even for small diameter dimension the wires are well populated and can easily conduct, contrary to GaAs nanowires, that are often fully depleted [17]. For a good characterization of the transport, it is necessary to study the dependence of the charge density (n) and the mobility (μ) on the size of the wire, the temperature, the geometrical properties and processing.

In the following the main factors that affect the transport properties are listed.

Sample contacts

To understand how electronic transport behaves in a system it is necessary to establish electrical contacts to it. The contact resistance will certainly affect the wire transport measurements. A possible way that allows to subtract the contact resistance and directly measure the nanowire resistance is the 4-probe configuration [18]. In a 4-probe measurement the outer electrodes are used to drive a known current through the test object, and the voltage drop across a section of the object is then measured with the set of inner probes. It is then possible to determine accurately the resistivity of the object.

For nanoscale objects such as nanowire, however, there are a few limitations to this method. In order to obtain the correct resistivity, the inner probes must be non-invasive, which means that their contact resistance must be large enough not to deviate a considerable amount of electrons in the test object. A too high transmission probability of the inner probes will effectively divide the object into three segments, and a 4-probe measurement will give the same results as a 2-probe measurement [18].

As the 2-probe measurement is the one mainly available for nanowires, all possible efforts must be done to improve the quality of the electrical contacts. In case of non ohmic contacts the sample resistance is strongly affected by the contact resistance. As a consequence, there will be serious difficulties in

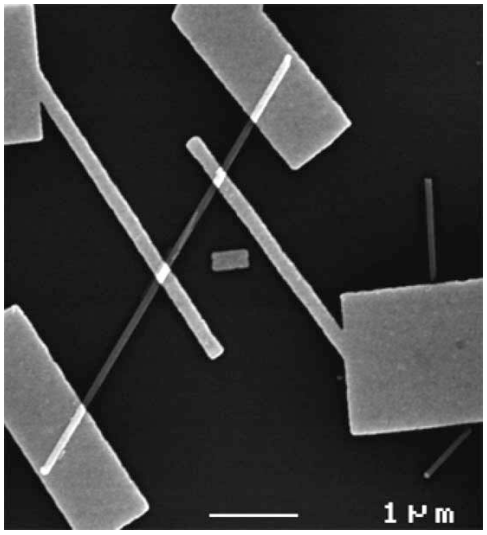


Figure 2.1: Example of an InAs nanowire electrically contacted with a 4-probe configuration [18].

the result interpretation. In order to avoid such problems, great efforts have been dedicated to contact technology in semiconductor systems. In particular, in recent years, III-V compound semiconductors have been investigated and exploited for high speed digital and analog applications as well as optoelectronic ones [19]. Some suitable technical solutions to obtain reliable ohmic contacts are to use low band-gap materials, composition grading, doping and surface techniques [20]. InAs with a band-gap of about 0.4 eV and a surface Fermi level *pinned* in the conduction band is an ideal surface layer for n-type ohmic contacts. The small band-gap implies less probability to form a Schottky barrier at the semiconductor/metal surface. In addition, the Fermi level is pinned (at least for bulk InAs) above the conduction band minimum, corresponding to *downward* band bending at the surface, for major crystal surface orientations. This band bending causes a charge accumulation layer to naturally form at the InAs surfaces and heterojunctions [21]. For these reasons InAs has very good qualities for ohmic contact formation.

A problem arises when the contacts need to be scaled down to nanometer dimensions, as is the case when contacts are made on nanowires with typical diameters in the range 20-70 nm. To reduce the contact resistance, the metal/semiconductor interface must be as clean as possible. The etching procedures that work for macroscopic contacts do not necessarily work for

nm-scale contacts.

In the case of bulk semiconductor a certain amount of surface material can be sacrificed without loss of the device functionality. However, semiconductor nanostructures in general, and nanowires in particular, are extremely sensitive to the removal of surface material. For this reason a treatment in highly diluted $(NH_4)_2S_x$ was used before the evaporation of the contacts. This treatment is shown to be a self-terminating passivation process. An optimized treatment in such a solution leads to formation of reliable ohmic contacts with no considerable etching effects [22].

Gate contact

When a voltage is applied to the gate, the nanowire conductance changes. It was observed that in general a positive voltage increases the conductance of InAs nanowires, while a negative one decreases it, indicating that electrons are the majority carriers. The InAs nanowires should behave as intrinsic semiconductor, because normally the wires are grown without intentional doping materials. However, from the 3D case [23], a n-type behaviour is expected in nanowires too. Such behaviour is probably due to the pinning of the Fermi level.

Remarkable variations of the conductance could be observed applying gate voltages of few volts. The effect of the gate is to change the Fermi level so that the subbands are populated or depopulated. A typical IV curve at different gate voltages and typical sweeps of the gate are shown in Fig. 2.2 and Fig. 2.3 respectively.

The carrier concentration is not directly accessible from measurements, because it would be very hard to perform a Hall measurement. In order to measure a Hall voltage, the nanowire should be contacted sideways with two additional contacts. That would be technically extremely difficult and would also involve the same problems explained in 4-probe measurements. The carrier concentration, however, can be extracted from an electrostatic model of the wire. Considering the nanowire as a degenerate conductor, the carrier concentration can be estimated from the pinch-off voltage of the gate-sweep characteristic. The charge removed from the wire by decreasing the gate voltage is simply

$$Q = C_{wire-gate}V \tag{2.6}$$

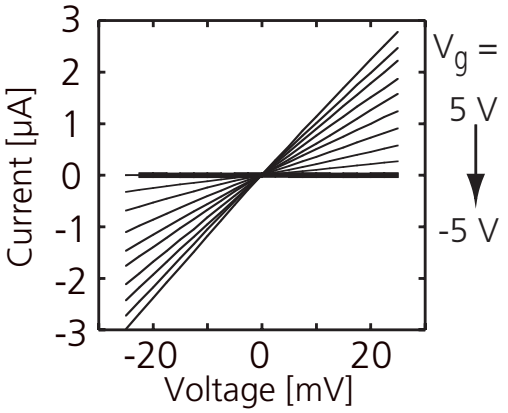


Figure 2.2: Nanowire IV curves at different gate voltages [4].

where $C_{wire-gate}$ is the capacitance of the wire and the gate contact.

Depending on the geometry of the contacts it is sometimes possible to calculate this capacitance by an analytical formula (section 2.1.3). Otherwise for a more complicated geometry it is possible to simulate the sample by creating a 3D model and calculating the capacitance.

Temperature

The conductance of the nanowires is also affected by temperature. Lowering the temperature generally leads to an increase of the electron mobility, but this does not strictly imply that the nanowire resistance has to decrease. In the nanowire case, in which surface effects are not negligible, impurities and defects play a big role. Charge freezing can overcome the electron mobility increase with the result that the resistance increases lowering the temperature.

At low temperature the nanowire chemical potential is lower, with the consequence that a higher voltage is necessary to make the wire conductive. The pinch-off temperature dependence was studied for core-shell nanowires with a diameter of 25 nm [24]. The conductance dependence vs. the gate voltage is shown in Fig 2.3, highlighting a gate pinch-off voltage increase at low temperatures. Results for homogenous InAs nanowires with a 20 nm diameter will be presented in Chap 4 of this thesis.

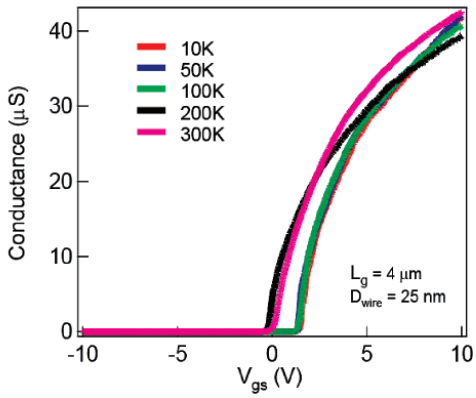


Figure 2.3: Conductance vs. gate voltage data measured at temperatures from 300 to 10 K for a 25 nm diameter InAs/InP back-gated NWFET [24].

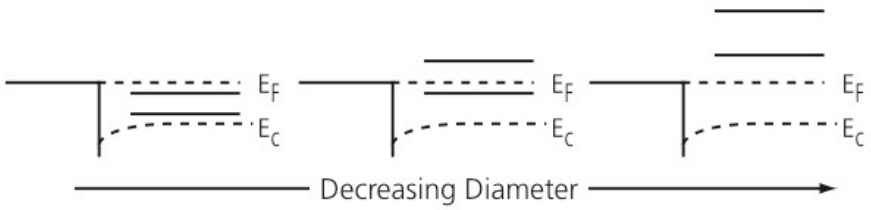


Figure 2.4: Nanowire diameter dependence of the subbands relative position with respect to the Fermi level.

Nanowire size

Large diameter wires have several occupied subbands and the conductance is high. When the diameter is made smaller, one subband after the other are pushed up above the Fermi level due to quantum confinement, and finally the ground state is emptied. At this point transport occurs only if the thermal energy is sufficiently high to excite electrons up into the empty subbands [4]. Larger diameter wires have a lower lying ground state than thinner wires, so it is expected that the pinch-off would takes place at lower gate voltages (see Fig. 2.4).

An evident pinch-off voltage dependence on the nanowire size is shown in Fig. 2.5. These measurements were performed at RT with a source drain bias of 2 mV and are comparable with the measurements performed by myself in Chap. 4.

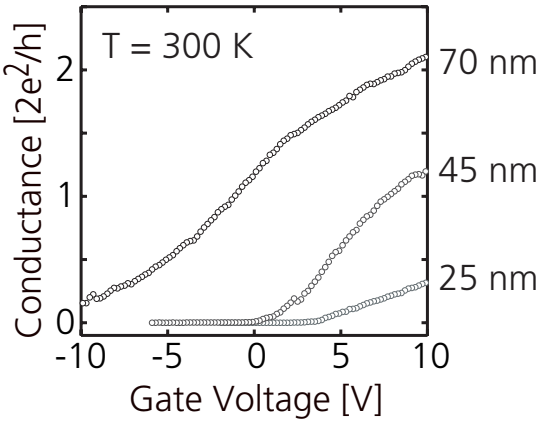


Figure 2.5: Room temperature gate-sweep at an applied source drain voltage of 2 mV for three wires with different diameters [4].

2.1.3 Nanowire transistor model

In the case of a back-gate geometry it is reasonable to approximate the gate contact as an infinite plane so that putting a cylinder in front of the plane, the system capacity [25] is:

$$C_{wire-gate} \cong \frac{2\pi\epsilon\epsilon_0 L}{ln(\frac{2h}{r})} \tag{2.7}$$

where ϵ is the relative dielectric constant of the medium that separates back-gate and nanowire and h is its thickness. L and r are respectively the length and the radius of the nanowire. This formula neglects the contribute of the end circular caps of the cylinder, but this assumption is completely justified considering a large value of the aspect ratio [26]. In addition, in this formula the cylinder is considered as embedded in the dielectric medium, but in reality the wire is only lying on the dielectric surface and it is surrounded by air. Nevertheless the formula makes it possible to predict at least the order of magnitude of the system capacitance.

In the case of a lateral gate is not easy to find an analytical solution. It is preferable to create a 3D model and simulate the problem with a computer. Since most of the devices realized for the present work have the lateral gate configuration, in Chapter 4 all details of the 3D simulation will be presented.

Knowing the capacitance of the gate and wire system, by using a model,

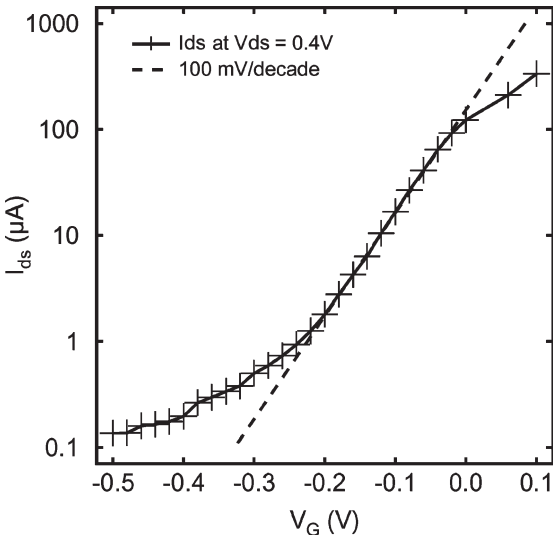


Figure 2.6: Linear fit of a gate-sweep measurement. The angular coefficient of the fit line is the transconductance value [28].

it is possible to estimate the wire electron mobility. The sample configuration either with the back-gate or with the lateral gate can be considered a MOSFET. As already said, the conductance can be tuned by the back-gate from complete depletion to a population of transverse modes and thus the device functions as a transistor. At low source drain voltages the characteristics are linear and from a the model presented in [27], the drain current is given by:

$$I_{SD} = \frac{\mu_n C_{wire-gate}}{L^2}(V_g - V_{th})V_D \tag{2.8}$$

where μ_n is the mobility and V_{th} is the pinch-off voltage. If the capacitance is known, the wire electron mobility can be estimated by using Eq. 2.9. Another equivalent formula useful to estimate the mobility from the transconductance g_m of the device [27] is:

$$g_m = \frac{\partial i}{\partial V_g} = \frac{\mu_n C_{wire-gate}}{L^2}V_D \tag{2.9}$$

In order to estimate the electron mobility the transconductance has to be extracted from the experimental measurements. An example of linear fit to extract a transconductance value is given in Fig. 2.6

Some estracted values of InAs nanowire mobility at room temperature

are here summarized. These mobility values were calculated using the model presented above:

- $\sim$ 3000 cm^2/Vs for 40 nm diameter nanowires with cylindrical gate [28].
- $\sim$ 2740 cm^2/Vs for 30-75 nm diameter nanowires with back-gate [29].
- $\sim$ 11500 cm^2/Vs for a core shell InAs/InP nanowire, 20nm/2nm, with top-gate [24].

It should be noticed that all these values are lower than the typical InAs bulk mobility of 33000 cm^2/Vs [29]. But they are higher than typical mobility values measured for the accumulated free-electron gas on the InAs surface (2000–3000 cm^2/Vs) [30],[31].

This electrostatic model is also applied to nanotubes since they fit in the approximation hypotheses [32] (in this case a mobility of 20 cm^2/Vs was found).

2.2 Optical properties

In the first part of this section the electronic transitions related to photoconductivity are considered. In the second part, the reasons for a photoconductivity experiment are explained . In the last part, the effect of the light on conductance and specifically discussed for semiconductor materials focussing on nanowires.

2.2.1 Electronic transitions

Some of the electronic transitions commonly found in photoconductors are shown schematically in the energy-band diagram of Fig. 2.7. These transitions can conveniently be divided into three types [33]:

- Absorption and excitation (Fig. 2.7 (a))
- Trapping and capture (Fig. 2.7 (b))
- Recombination (Fig. 2.7 (c))

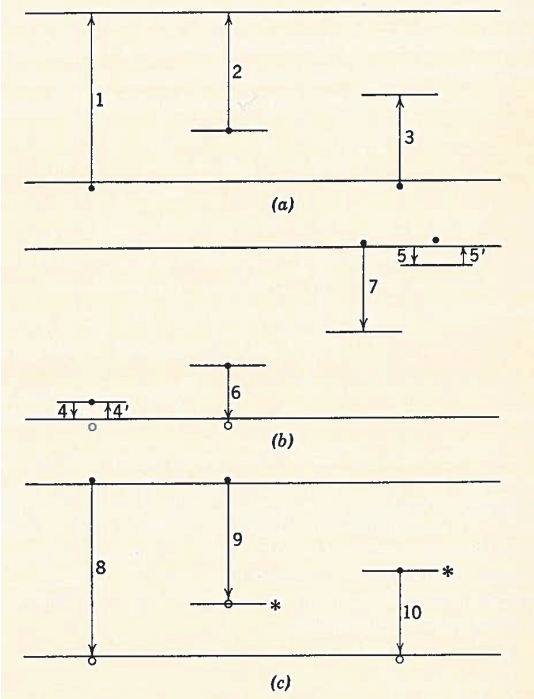


Figure 2.7: Common electronic transitions in photoconductors. (a) Absorption and excitation; (b) trapping and capture; (c) recombination [33].

Absorption and excitation

There are three possible types of absorption transitions resulting in photoconductivity . Transition 1 (see Fig. 2.7 a1) corresponds to absorption by the electronic levels of the crystal itself, producing a free electron and a free hole for each absorbed photon. Transition 2 (see Fig. 2.7 a2) corresponds to absorption at a localized imperfections in the crystal, producing a free electron and a hole bound in the neighborhood of the imperfection for each absorbed photon. Transition 3 (see Fig. 2.7 a3) corresponds to absorption, raising an electron from the valence band to an unoccupied impurity level. This absorption produces a free hole and an electron bound in the neighborhood of the imperfection for each p absorbed photon. These transitions are not the only possible ones, but they are the only ones releasing free carriers.

In an idealized absorption spectrum we can see a cut off of absorption at the minimum energy required for the transition. This minimum corresponds to the band gap for the transition of an electron from the valence band to

the conductance band (Transition 1). For light of greater energy than the minimum required, absorption is continuous, with an intensity, depending on the density of states and the transition probabilities involved, up to a certain maximum energy, which would correspond to a transition from the bottom of the valence band to the top of the conduction band. In most real crystals the conduction band overlaps higher-lying allowed bands and a maximum energy for absorption is not found.

To a first approximation, the photoconductivity has the same dependence on wavelength as the absorption.

An energy-band diagram of the type shown in Fig. 2.7 omits much information which is necessary to fully describe electronic transitions; in particular, the transition selection rules for transition 1 in terms of E vs. k must be considered in terms of a diagram such as Fig. 2.8. In a one dimensional case, the momentum of an electron is:

$$p_e = \hbar k \tag{2.10}$$

and the momentum associated with the absorbed photon is:

$$p_{ph} = 2\pi\hbar\nu n/c \tag{2.11}$$

where ν is the frequency, c is the light velocity and n is the index of refraction. We consider here the conditions for an allowed transition when only photons take part in the transition. Momentum conservation requires that

$$\Delta k = \frac{2\pi\nu n}{c} \tag{2.12}$$

In terms of the representation given in Fig. 2.8, we can now compare this value of Δk with the value of $k_{max} = \pi/a$ to determine the allowed departure from a vertical transition. Assuming energy conservation:

$$\frac{\Delta k}{kmax} = 2na\frac{\Delta E}{hc} \approx \frac{1}{500} \tag{2.13}$$

This shows that the photon momentum can be effectively neglected, and that allowed transitions involving photons only are represented by vertical lines between allowed bands.

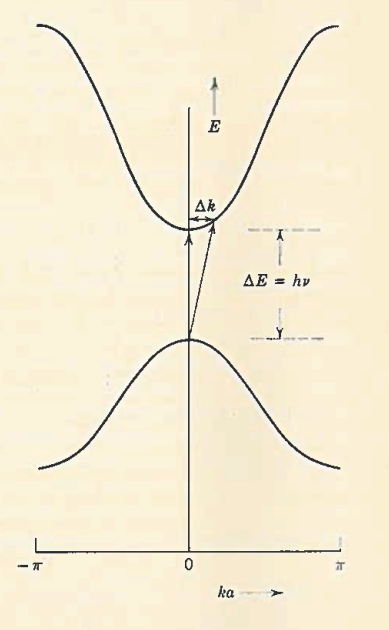


Figure 2.8: Reduced propagation space representation of E as a function of k, in determining how large Δk may be in an allowed transition involving photons only [33].

Trapping, capture and recombination

Once electrons and holes have been freed by absorption of a photon of sufficient energy, they will remain free until they are captured at an imperfection. We may classify these capturing centers in two groups [33]:

- Trapping centers: if the captured carrier has a greater probability of being thermally re-excited to the free state than to recombine with a carrier of opposite sign at the imperfection.

- Recombination centers: if the captured carrier has a greater probability of recombining with a carrier of opposite sign at the imperfection than of being re-excited to the free state.

Fig. 2.7 (b) pictures trapping and thermal release in trapping center and capture in recombination centers for both electrons and holes. Although a center with an energy level lying near one of the band edges will be more likely to act as a trap than as a recombination center, the distinction between trap and recombination centers is a distinction drawn on the basis of the relative

probability of the thermal ejection versus recombination. This means that the difference concerns kinetic conditions and not the intrinsic nature of the centers themselves. A recombination center at given condition of light and temperature may act as a trap at another condition of light and temperature.

A free electron may re-combine directly with a free hole; the probability of this transition is usually rather small. The lost energy is emitted as photon with approximately the energy of the band gap. Such emission is called edge emission (see Fig. 2.7 (c), transition 8). Recombination may also occur, as is the more usual case, through recombination centers: either an electron being captured by an excited center containing a hole (transition 9), or a hole being captured by an excited center containing an electron (transition 10). These transitions may also be radiative.

2.2.2 Photoconductivity

A possible approach for the optical study of a material is to measure its photoluminescence. Another possible approach is the study of the light absorption: this allows to measure not only the lowest excited state(s), i.e. the states closest to the band-gap, but can used to probe higher excited state(s) as well.

For a semiconductor the band structure can be studied with absorption spectroscopy, whereas photoluminescence measurements primarily give information about the band-gap.

The most obvious way to measure the absorption is to pass the excitation light through the sample under study, and detect the transmitted light with a photodetector as a function of the wavelength. Neglecting reflectance, the absorption A is defined as $A = 1 - I_T/I_0$, where I_T is the intensity of the transmitted light and I_0 is the intensity of the light incident on the sample. This method demands that the absorption in the material is substantial, since it is difficult to detect very small changes in a large light intensity.

Another possibility to measure the absorption is to perform photocurrent (PC) measurements. In this method a bias voltage is applied to the sample, creating an electric field in the material that separates the optically excited electrons and the holes. The increase in number of free carriers gives rise to a current. Thus the sample acts as a photodetector for the light, and the magnitude of the current is related to the absorbed intensity.

This method gives information about the transport from the excited state through the material and about the absorption. The transport information, however, cannot be really separated from the absorption information. In addition, the structure under study has to be conductive in its excited state.

In a PC measurement it is indeed possible to single out the absorbed light by the generation of free carriers in the nanowire. On the other hand a single nanowire would give a too small absorption for a transmission measurement and, therefore ,that would not be a suitable method for single nanowire spectroscopy.

Photoconductivity general properties

The absorbed photons cause excitation of electrons with the mechanisms explained in 2.2.1 determining a variation of the conductivity. The expression of the conductivity of a semiconductor is [33]:

$$\sigma = e(n\mu_n + p\mu_p) \tag{2.14}$$

where n (p) are the concentration of negative (positive) carrier and $\mu_n(\mu_p)$ is its mobility coefficient. In a homogeneous material, the density of free electron and holes (respectively n and p) are uniform throughout the material. The photoconductivity results from the variation of the values of n and p:

$$\Delta\sigma = e(\Delta n\mu_n + \Delta p\mu_p) \tag{2.15}$$

In insulators the values of Δn and Δp may be much larger than the corresponding free carrier densities in the dark, n_0 and p_0 . In semiconductors the reverse is often true, and the effect of radiation can be considered as a small perturbation on a large dark carrier density. In a inhomogeneous material in which n and p are not uniform, photoconductivity can result from a second mechanism involving the reduction by radiation of the barrier resistances of in the material.

The lifetime of photoexcited carriers is the key parameter for an understanding of photoconductivity. If light is falling on a photoconductor, and creates f electron-hole pairs per second per unit volume of the photoconductor, then

$$f\tau_n = \Delta n \tag{2.16}$$

and

$$f\tau_p = \Delta p \tag{2.17}$$

Where τ is the carrier lifetime The variation of the conductivity can be rewritten as:

$$\Delta\sigma = fe(\mu_n\tau_n + \mu_p\tau_p) \tag{2.18}$$

This relation shows that the photoconductivity is proportional to the carrier lifetime. In the specific case of a semiconductor slab with ohmic contacts at both ends the photocurrent I_p from the optically excited electrons depends on the light intensity and on the applied voltage as [34]:

$$I_p = qf\left(\frac{\mu_n\tau V}{L^2}\right) \tag{2.19}$$

where V is the applied voltage, L is the length of the sample, and q is the electronic charge. (The current from the holes is given by the same expression with μ_p substituted for μ_n .) The rate f, at which electrons are generated, depends on the intensity of the incident light and the absorption probability.

$$P_{absorbed} = P_{incident}(1 - e^{-\alpha W}) \tag{2.20}$$

$P_{incident}$ is the number of incident photons, $P_{absorbed}$ is the number of photons absorbed, W is the thickness of the semiconductor slab and α is the absorption coefficient.

The absorption coefficient depends on the density of states in the material, and it increases with increasing photon energy E_{ph} as $\sqrt{E_{ph}}$ (3D case). It can be supposed that a sufficiently thick nanowire will have a density of states similar to the bulk density of states. As a consequence, if the photon flow is constant over the excitation energy range (or if the photocurrent is normalized to the incident photon flow), the photocurrent will increase with increasing photon energy.

On the other hand a 20 nm diameter nanowire is subject to the quantization effect so that the density of states is similar to the 1D case (see Eq. 1.5). The 1D density of states characterized by several spikes, so that, in correspondence of a spike, it is reasonable to expect a photocurrent peak.

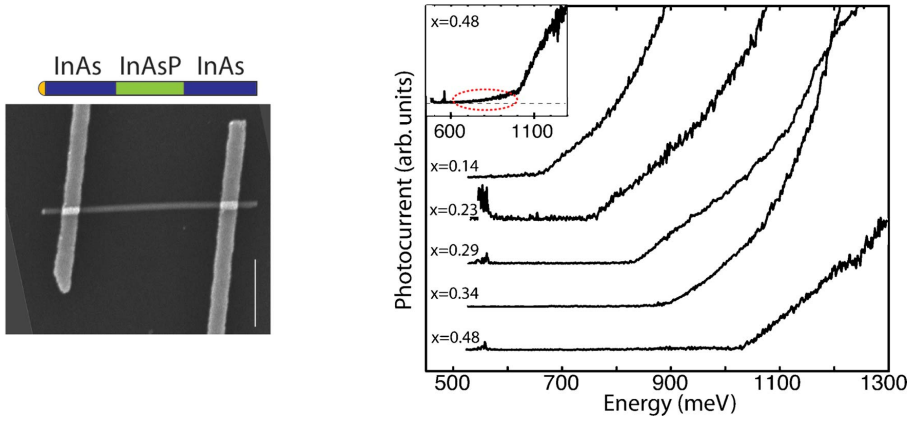


Figure 2.9: On the **left side** a SEM image of the contacted nanowire (the vertical scale bar on the bottom right is 1μ) with on top a schematic of the nanowire. On the **right side** photocurrent spectra from single InAs nanowires with a centrally placed $InAs_{1-x}P_x$ segment for five different compositions. (The small peaks in the spectra at about 550 meV are artifacts) [35].

Photoconductivity of nanowires

It is well known that at the nanometric scale electronic properties of the wires change. The nanowire diameter size affects the band structure and consequently the effective masses of the electrons and holes. Lateral confinement effects on conduction and valence band increase the value of the band gap. Furthermore for GaAs nanowires it has been found that as the lateral size decreases, the conduction band switches the position of its minimum in the Brillouin zone from the Γ point to the L point, and the band structure exhibits a direct-to-indirect band-gap transition [36].

Also the strain can affect the electronic structure of nanowires. Efforts were made to model and simulate the nanowire and to compute the strain effect on the band structure [37]. Experimentally, using photoluminescence measurements, it was found that the subband separation energy is weakly affected by strain and is mainly governed by quantum confinement effects in the conduction band [38].

From the scenario depicted above it is clear that nanowires present very interesting electronic properties at the nanometric scale, mainly due to quan-

tum confinement. As already discussed (Section 2.2.2) photoconductivity is a good tool for the investigation of the crystal electronic structure and can be applied also to nanowires.

Photoconductivity measurements were already performed on longitudinally heterostructured nanowires with a diameter of 85 nm [35]. In the cited paper were used InAs nanowires containing a centrally placed segment of $InAs_{1-x}P_x$, where x is the percentage of phosphorus which ranges from 0 to 1.

The wire with the contacts is shown in Fig. 2.9. The authors were able to measure the band gap as a function of the composition, in the range $0.14 < x < 0.48$, by photocurrent spectroscopy on the single wire. The photocurrent measurements were performed at a temperature of 5 K. The plot in Fig. 2.9 shows how the photocurrent spectra from single InAs nanowires, with the centrally placed $InAs_{1-x}P_x$ segment, for five different compositions, clearly depend on the wire composition.

In the case of InAs the effective mass is lower than GaAs (used in previously cited articles) with the consequence that quantum confinement has stronger effects. As shown in section 1.3.2 it is technologically possible to grow InAs nanowires with a diameter as small as 20 nm. This diameter size is small enough to appreciate quantum confinement effects.

An interesting aim would be to study the electron structure of 20 nm diameter InAs nanowires by photoconductivity measurements. The onset of the photocurrent is expected to be shifted to higher energy values because of the quantization effect but also because of the nanowire wurtzite crystal structure. In addition, information about the electronic structure are expected from the photocurrent curve vs. the light energy.

As already mentioned in section 1.1, bulk InAs has a zincblende crystalline structure, but for nanowires it turns out that the crystalline structure is wurtzite [39]. Performing photoluminescence measurement on InAs/InP core-shell nanowires a blue shift in the spectra onset was observed [40]. The measured shift with respect to the bulk InAs value is $\Delta E_m \simeq 150$ meV. This shift is partially due to the wurtzite crystalline structure, that has a bigger gap respect to the zincblende structure, and to the strain of the InP shell. Thanks to theoretical models it is possible to separate the two contributions [41]. The strain contribution to the energy shift is estimated to be $\Delta E_{Strain} \simeq 100$ meV whereas the different structure increases the energy gap

of $\Delta E_{Wurtzite} \simeq 50$ meV.

The previously cited experiments allow to compute an energy gap for wurtzite InAs of:

$$E_{Wurtzite\,gap} = E_{Zincblende\,gap} + \Delta E_{Wurtzite}$$

$$\simeq 350meV + 50meV \simeq 400meV$$

This energy gap value will be used in section 4.3 to compute the energy level dependence on the nanowire diameter.

A confirmation of a high energy gap value comes also from a preliminary measurement performed in our laboratory on a nanowire array. The light reflected by a nanowire array was measured as function of the temperature, as shown in Fig. 2.10. At 300K the curve minimum, that corresponds to an absorption, is at the left of the water vapor absorption (noise peaks). Cooling down the shape of the spectrum changes and the curve minimum shifts to higher energies. The energy gap, related to the curve minimum, at RT can be estimated at about 430 meV, a value that corresponds to the above estimation and is surely higher than that zincblende InAs gap (350 meV).

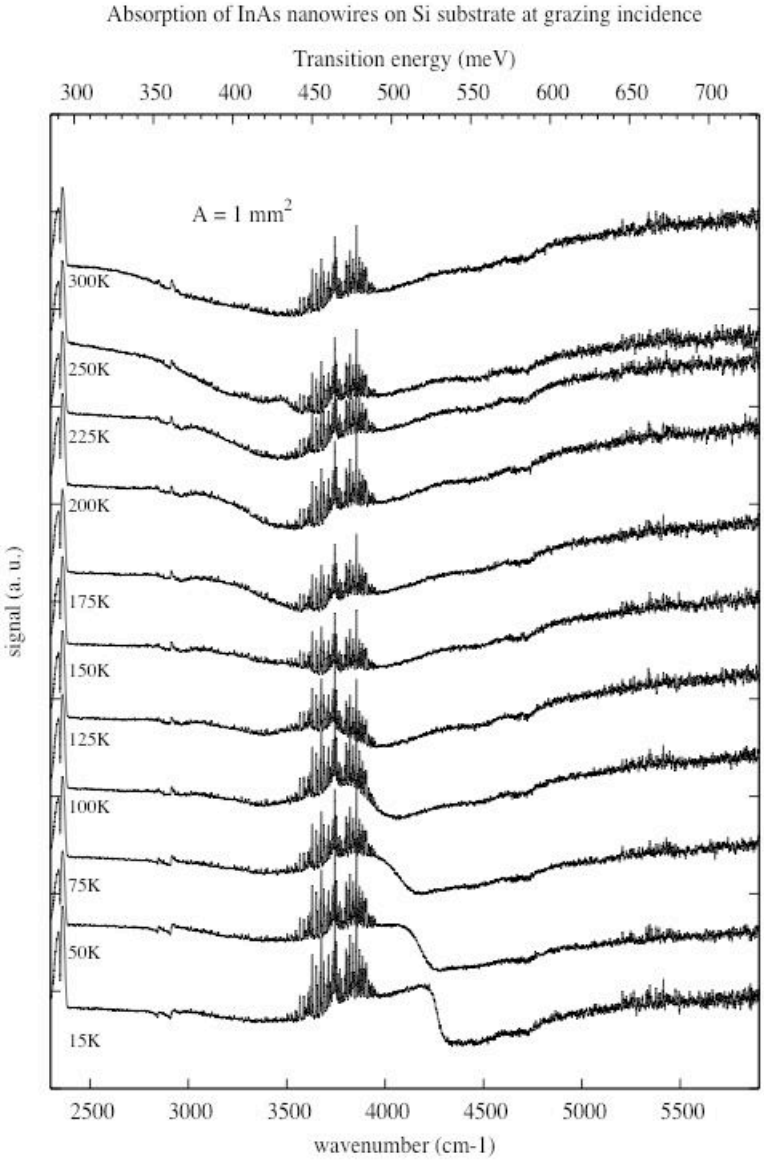


Figure 2.10: Reflection spectra of a nanowire array as function of the temperature.

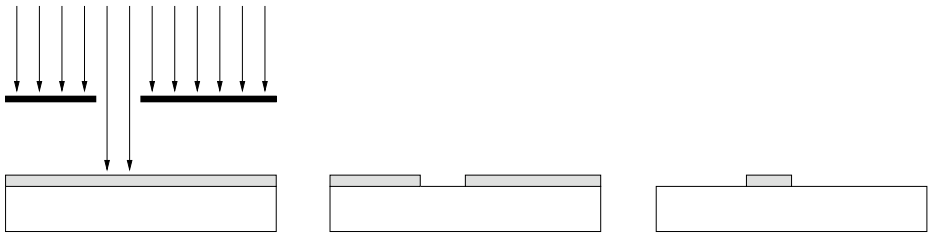
Chapter 3

Processing and experimental set-up

The first part of this chapter describes the device's nano-fabrication, starting with a description of the lithographic techniques (section 3.1). Detailed recipes used during the fabrication are reported in Appendix A.

All the processing took place in the clean room of the NEST CNR-INFM-SNS laboratory. During this work different kinds of devices were realized, with different nanowires and substrates. Many parameters have been optimized in order to fabricate the desired devices. For this reason several attempts were made and a methodology was created for the device processing. Schematically the fabrication can be divided into three main steps:

1. The realization of the deposition lane on the substrate (section 3.2), which in turn results in:
    - Fabrication of the microscopic connection strips and bonding *pad* by optical lithography.
    - Fabrication of a coordinate system of nanoscopic markers by electron beam lithography.
2. The realization of the nanoscopic electrical contacts on the nanowire (section 3.3) obtained by:
    - Deposition and imaging of the nanowires.
    - CAD contact drawing and electron beam lithography.



(a) *Resist* exposure. (b) Positive *resist*. (c) Negative *resist*.

Figure 3.1: *Resist* patterning process. (a) A mask (bold line) is commonly used in the optical lithography. Chemical development allows to remove the exposed *resist* (b) or the non exposed *resist* (c).

3. The final imaging and the sample bonding (section 3.4).

In the second part of the chapter the experimental set-up for the transport and photoconductivity measurements is then described (section 3.5).

3.1 Lithography and metal deposition

All processes of etching or deposition start with a lithographic step.

Lithography is a process used to selectively remove parts of a thin film. It uses light or electrons to project a chosen geometric pattern onto a sensitive chemical *resist* on the substrate. With a chemical treatment it is possible to remove the exposed *resist* (positive lithography) or the non exposed *resist* (negative lithography) (See Fig. 3.1).

Once the *resist* is removed, the surface can be physically or chemically attacked, or a deposition can be obtained. The planar structure precision strongly depends on the lithographic technique. The best resolution that can be achieved in a lithographic process is determined by the diffraction limit and it is of the same magnitude of the exposing wavelength. Ultra violet (UV) lithography, that is the most used photo-lithography technique today, has a resolution of about a μm. On the other hand, Electron Beam Lithography (EBL) has a resolution of about 10 nanometers and it is necessary to operate on nanoscopic devices.

Electronic lithography started to be used between the '60s and '70s and is based on an instrument similar to the Scanning Electron Microscope (SEM,

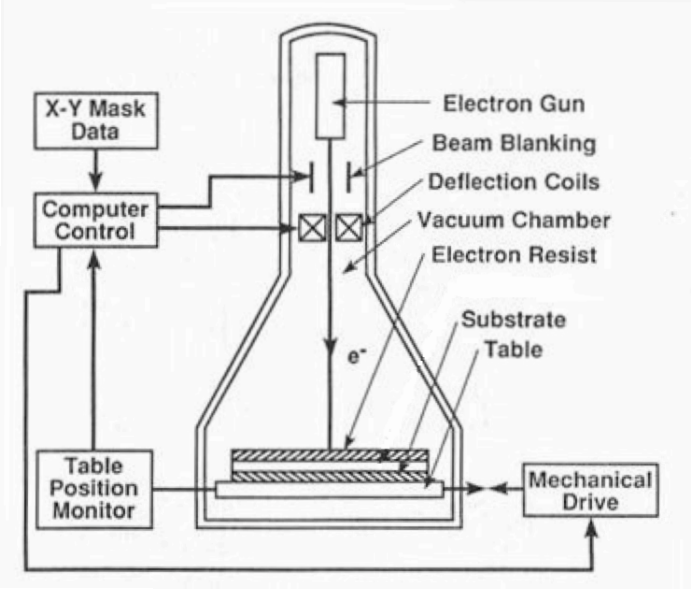


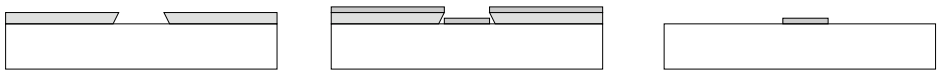
Figure 3.2: Schematic of an EBL instrument.

see section 1.4.1). An EBL instrument schematic is shown in Fig 3.2. As in the SEM, an electron gun emits an electron beam (*e-beam*) in a vacuum chamber. In the EBL the *resist* exposure is performed with a high energy electron beam (10 keV) that is conveniently collimated by deflection coils in order to expose the *resist* to the desired pattern. In order to expose any possible pattern it is necessary to switch the *e-beam* on and off with a beam blanker that diverts the beam and, moreover, to move and to collimate the beam with deflectors.

The whole process is controlled by a computer that guides the *e-beam* along the desired pattern. The EBL precision in the *resist* exposure depends on the *resist* molecule size and on the electron diffusion on the substrate. In this case the elecron wavelength ($\simeq$ 1 Å) is much smaller than the EBL precision of $\simeq$10 nm. The EBL instrument used for this work is shown in Fig. 3.3.

To realize an electric contact it is necessary to evaporate a thin metallic layer on the sample covered by the developed *resist*. A part of the evaporated metal is deposited directly on the substrate surface while the other can be removed with the resist with a procedure called *lift-off*. The *lift-off* is obtained with some appropriate solvents that chemically remove the *resist*. The procedure is sketched in Fig. 3.4.

Figure 3.3: Picture of the EBL instrument in the NEST laboratory, also used for scanning electron microscopy.



(a) Developed *resist*. (b) Metallization. (c) *Lift-off*.

Figure 3.4: Three steps of the lift-off process to create a metal contact.

For a good contact quality the *resist* profile after the development must have an oblique undercut as shown in Fig. 3.4 (a). This *resist* profile favours the separation between the metal deposited on the substrate surface and the metal deposited on the *resist*. Without such a separation there is the risk to remove all metal during the *lift-off* or to obtain ripple contacts. To achieve a good undercut at small distances, two *resist* layers have to be deposited (bi-layer). If the bottom layer is more sensitive with respect to the upper one, more material is removed during the development giving the desired "oblique" profile.

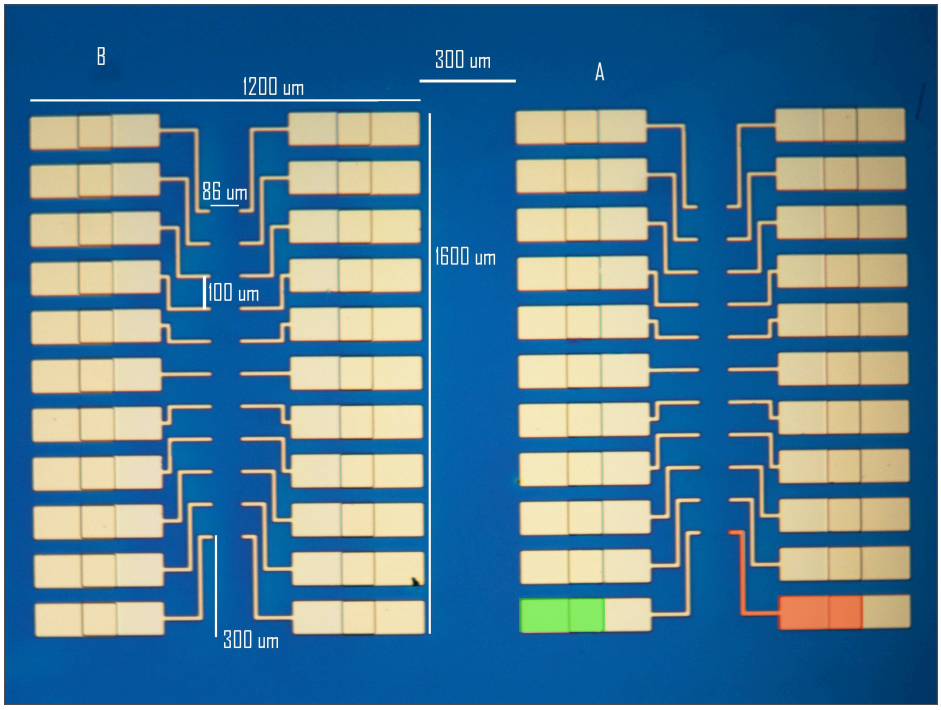


Figure 3.5: Microscopic ohmic contacts picture where relevant distances are indicated. In the bottom right corner microscopic connection strips and bonding *pad* are colored in red and in green respectively.

3.2 Deposition lane

First of all one has to choose the substrate with the aim of improving the transport and the photoconductivity performances. As a matter of fact it will be shown in Chapter 4 that the substrate plays an important role in the photoconductivity measurements.

The three studied substrates are:

- GaAs.
- SiO_2 (250 nm) on doped Si (indicated as SiO_2^* later).
- SiO_2 (500 nm) on intrinsic and insulant Si (indicated as SiO_2^{**} later).

The surface of the substrate must be accurately cleaned before any fabrication step. Impurities are removed with acetone and isopropanol, then the substrate is baked for few minutes to dry it. The suitable structure to host

nanowires is composed of microscopic connection strips, which define a lane with ten fields, and by nanometric markers, which define a coordinate system in each field.

The microscopic connection strips are realized in a planar geometry by ultraviolet (UV) lithography and metal evaporation. They are necessary as a link from the nanoscopic size to the macroscopic size. They are realized in two steps in order to obtain different metal thickness:

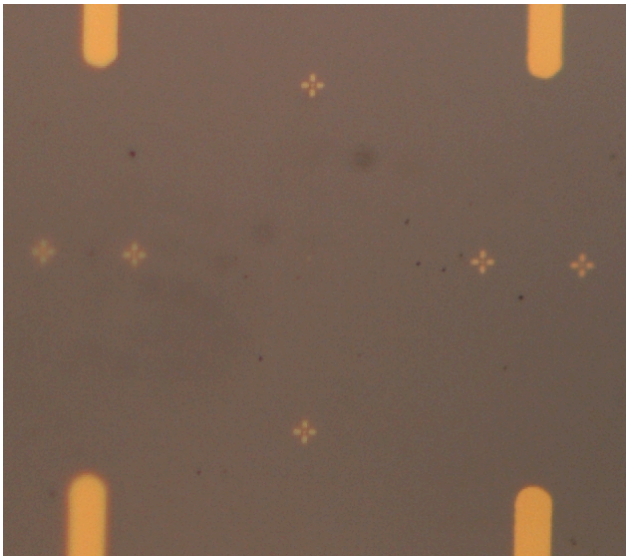
- micrometric connection strips: the contacts close to the nanowire deposition zone must have a width of few μm and, above all, must not be too thick in order to allow the subsequent contact operation with the nanowire. The total thickness chosen for all samples is 45 nm (5 nm of chrome, providing a good sticking to the surface, and 40 nm of gold). Due to the above mentioned micrometric width and to avoid ripple contacts, a bi-layer recipe was used. All details of the used recipe are reported in Appendix A.1.

- bonding *pads*: the pads must be thick enough to support the bonding operation. Generally a thickness of 10 nm of chrome and of 100 nm of gold were evaporated. The *pad* has to be thicker than the connection strips due to the great pressure exerted on the sample by the bonder tip. All details of the used recipe are reported in Appendix A.2

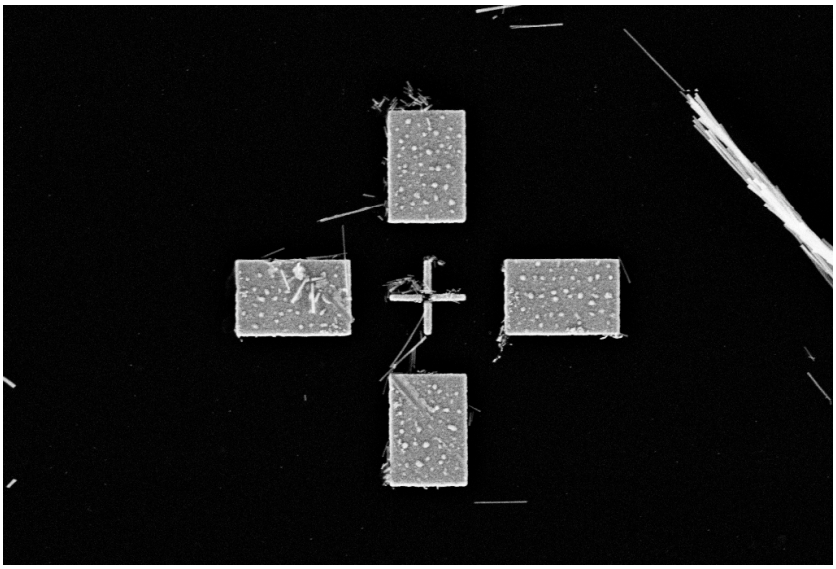
The final result of this fabrication process is shown in Fig. 3.5. The micrometric connection strips lie in the lane center part, where the nanowires are subsequently deposited; one of them is colored in red. The rectangular bonding *pads* are at the lane external borders; one of them is colored in green. In the lane defined by the microscopic contacts ten fields are available.

The same optical mask was used for every substrate and identical parameters of the optical lithography were used for the three different substrates.

A coordinate system in the lane field, defined by the microscopic contacts, has to be realized before the wire deposition on the substrate. This coordinate system consists of four markers and of a small centered cross in each field, in order to align the *e-beam* for each field during the EBL. The four markers in the single field are realized with EBL and are shown in the image of Fig. 3.6 (a). A zoom of the single marker is shown in the SEM image of Fig. 3.6 (b),



(a)



(b)

Figure 3.6: Images of alignment markers: (a) Optical image of a field after the marker fabrication. (b) SEM image of an alignment cross (after the nanowire deposition). This cross has a total lateral dimension of 5 μm.

taken after the nanowire deposition. A detail of the center field small cross is shown in Fig. 3.8.

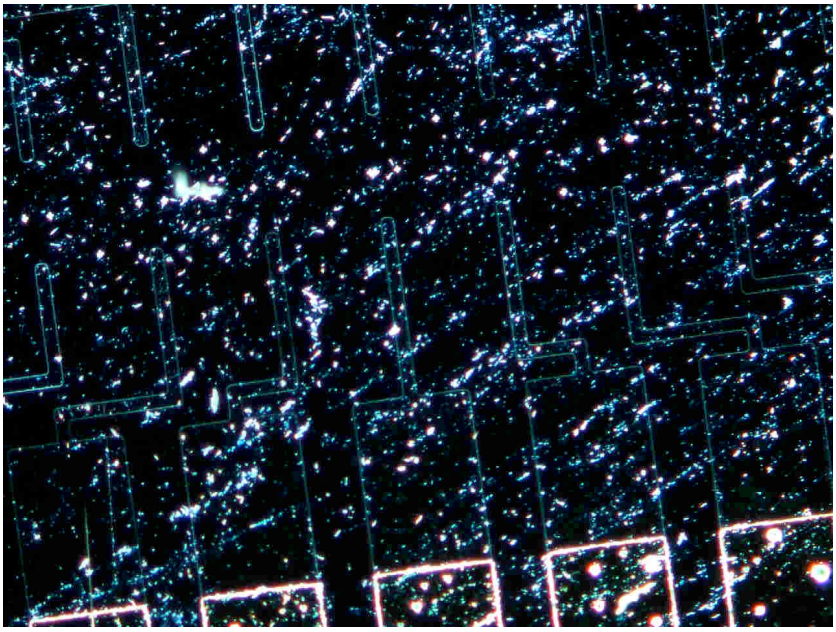


Figure 3.7: Optical microscopic view of the lane in the dark field mode, which highlights nanowires, impurities and contact borders.

3.3 Nanowire ohmic contacts

Once the coordinate system is defined, the nanowires can be deposited on the substrate surface in the field zone. The nanowire types used in this work are listed in Tab. 3.1 specifying the nanowire sample number, the diameter and the materials. All these nanowires were grown in the NEST laboratory with the CBE instrument shown in Fig. 1.8.

The chosen nanowires are distributed on the surface by a so called *dry*

Sample number	Diameter (nm)	Structure
148	40	core-shell (InAs/InP)
162	40	homogeneous (InAs)
179	20	homogeneous (InAs)
245	20	homogeneous (InAs)
265	20	homogeneous (InAs)

Table 3.1: List of the different nanowire samples used in the device fabrication.

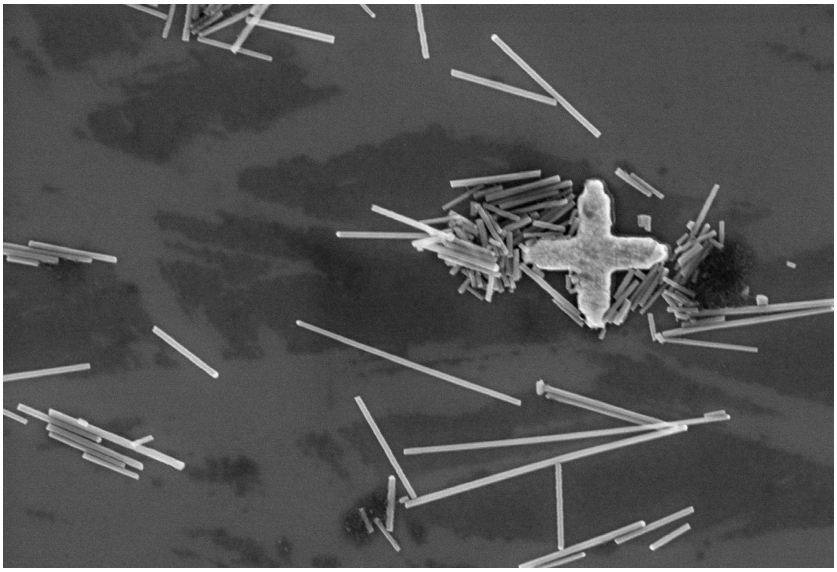


Figure 3.8: SEM image of the central field cross surrounded by deposited nanowires.

deposition. This is accomplished by using a small piece of clean room paper to pick up the nanowires by gently sweeping it across the surface of a substrate containing the as-grown nanowires. The transfer of the wires is performed in the same fashion; sweeping the paper over the sample, in particular over the lane defined by the microscopic contacts. This results in a random deposition of nanowires on the lane zone.

Nanowires are first located by optical microscopy (the presence of nanowires down to 10 nm in diameter can be distinguished by optical microscope [4]). The best way to distinguish deposited nanowires by optical microscopy is in the dark field mode, as shown in Fig. 3.7. This fast check with the optical microscope allows to verify the nanowire distribution in the desired sample zone.

When deposited on the substrate surface, most nanowires stick to it thanks to the electrostatic force, and the surface sample can be cleaned from organic impurities without the risk of removing them.

As shown in Fig. 3.8, the SEM allows resolving single nanowires with high precision. SEM images are used to determine the position of the nanowires relative to the coordinate markers, so that subsequent EBL exposure patterns can be designed and drawn. A typical SEM field image suitable for alignment

should, at the same time, contain at least all the markers and have enough resolution to distinguish the single nanowire (see Fig. 3.9 (a)). A good magnification for a field image is 800 X: in this case also the terminal parts of the connection strips are visible and the connection to them can be easily drawn (see Fig. 3.9 (b)). The field image is then used to locate a single nanowire and to draw the nanometric contact that links the wire to the connection strips.

For each wire at least two nanoscopic ohmic contact must be designed. Those contacts link the nanowire edges to the microscopic connection links and are called source and drain. Besides, a gate is required to control the nanowire charge density and consequently its transport properties.

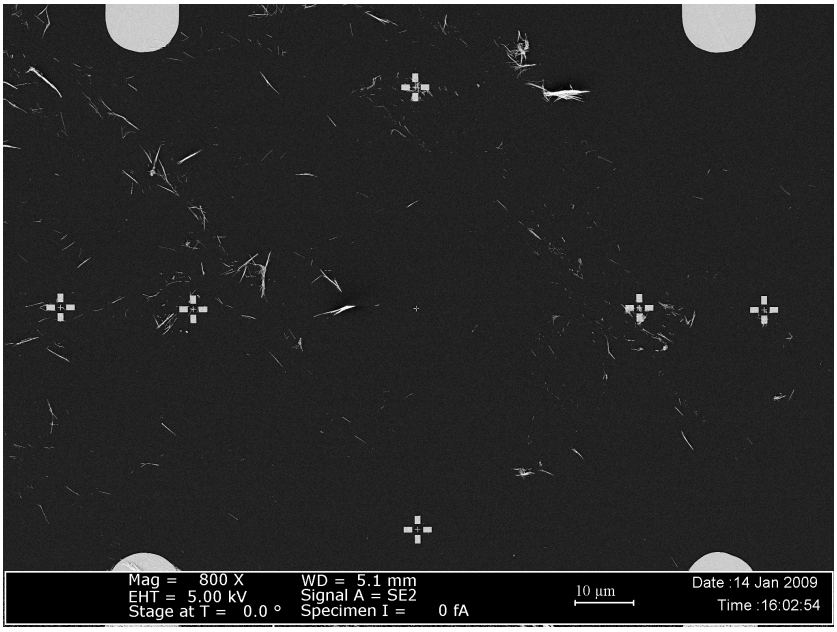
The SiO_2 substrate on doped Si (the second item of the list in section 3.2) allows using the doped Si as a gate, with the result that only two nanoscopic contacts, source and drain, for each wire must be realized. This configuration is called **back-gate** and the same gate can be used for all the sample nanowires. The other substrates do not have this possibility and a gate for each wire must be drawn. A third contact links a microscopic connection strip to the nanowire vicinity (typically from 200 to 400 nm); this is called a **lateral-gate** configuration.

The reason for those two different configurations will be discussed in section 4.3.

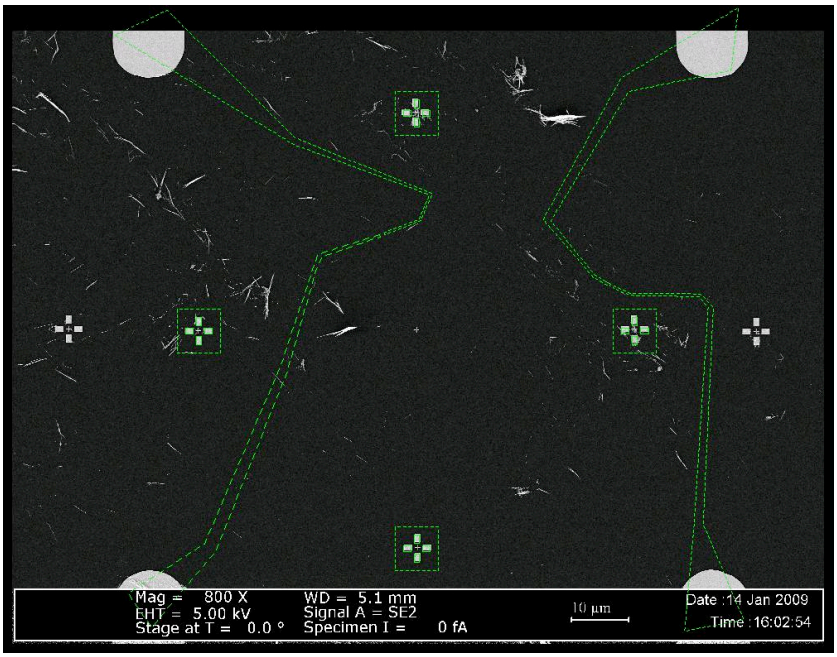
Prior to lithography, the sample is coated with a layer of Polymethyl methacrylate (PMMA, the EBL *resist*), baked at 150 °C and loaded in the EBL instrument chamber (the detailed recipe for the nanowire contacts is reported in Appendix A.3). As already discussed in section 2.1.2, after the exposure and the development the nanowire must be passivated.

The passivation process consists in dipping the device in a $(NH_4)_2S_x$ solution for 30 minutes. This process removes the oxide from the nanowire parts that are not covered by the *resist*. After the passivation, ohmic contacts are immediately evaporated to prevent the new formation of oxide. As indicated in [22], nickel and gold are evaporated, more precisely: 5 nm of Ni and 40 nm of Au.

In the case of core-shell nanowires a further fabrication step is needed: once the oxide is removed it is necessary to etch the shell in the contacted region, in order to expose the InAs core. To this end, immediately after the passivation, samples with core-shell nanowires were put in concentrated HCl



(a)



(b)

Figure 3.9: SEM images. (a) The four alignment crosses and the four terminal parts of the *branch shaped* contacts are visible in this field. (b) CAD drawing of four nanowire contacts on the SEM field image. The green crosses in the CAD drawing must overlap to the four markers of the SEM image.

for 30” and then metallized. The detailed recipe for the nanowire contacts is reported in Appendix A.3.

Sample	Substrate	Used nanowire	Nanowire type	Gate config.
I	GaAs	162	40 nm (homogeneous)	lateral-gate
O_E1	GaAs	162	40 nm (homogeneous)	lateral-gate
P2_M2	GaAs	148	40 nm (core-shell)	lateral-gate
Q1_E3	GaAs	245	20 nm (homogeneous)	lateral-gate
Q2_D1	GaAs	245	20 nm (homogeneous)	lateral-gate
L_J1	SiO_2^*	245	20 nm (homogeneous)	back-gate
R2_E2	SiO_2^{**}	265	20 nm (homogeneous)	lateral-gate

Table 3.2: List of the most important devices for transport and optical measurements.

3.4 Imaging and bonding

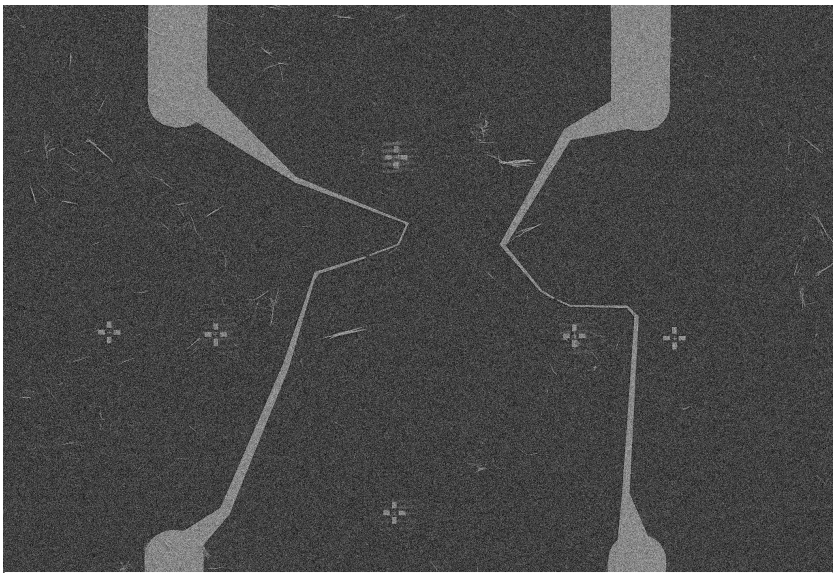
At the end of the fabrication procedure, the samples are screened by SEM imaging in order to check the process result. The quality of the lithographic and metallization processes is verified with an overview and a detailed inspection view of the nanowire for each sample.

An example of this procedure is given in Fig. 3.10 showing the overview and the zoom-in of the same field shown in the previous section (Fig. 3.9). The overview (Fig. 3.10 (a)) ensures that the ohmic nanowire contacts are successfully deposited without discontinuities. The detailed view of the nanowire (Fig. 3.10 (b)) allows to check that the wire is correctly contacted.

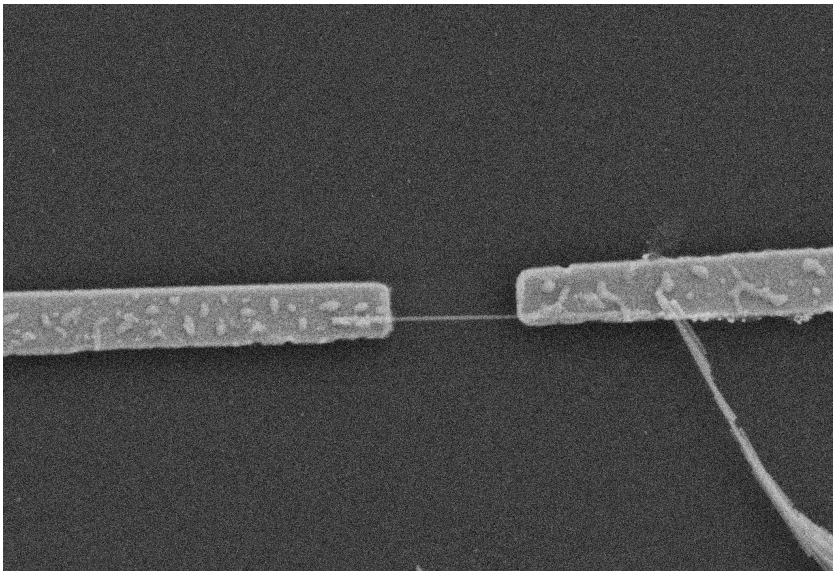
The nanowire shown in Fig. 3.10 (b) is reached by two contacts, the gate is 250 nm under the substrate surface (back-gate geometry). In Fig. 3.11 (a) a detail of a lateral gate configuration is shown where three contacts reach the nanowire. The source and the drain contacts are on the nanowire while the gate contact is only in the vicinity of the wire. As shown in Fig. 3.11 (b) contacts without wire were also realized to measure the substrate contribution to the photoconductivity measurements.

This imaging procedure is very useful in order to know the nanowire condition and further understand measurement results. As a matter of fact the discussed process is not trivial and some possible lithography drawbacks are discussed at the section end.

The fabricated devices are listed in Tab. 3.2 and the main characteristics are summarized. The sample name is composed by two parts. The first

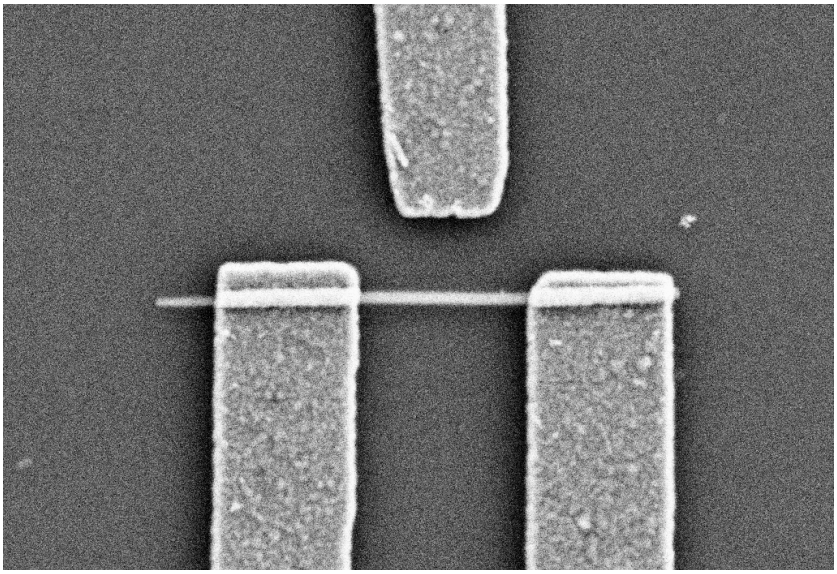


(a)

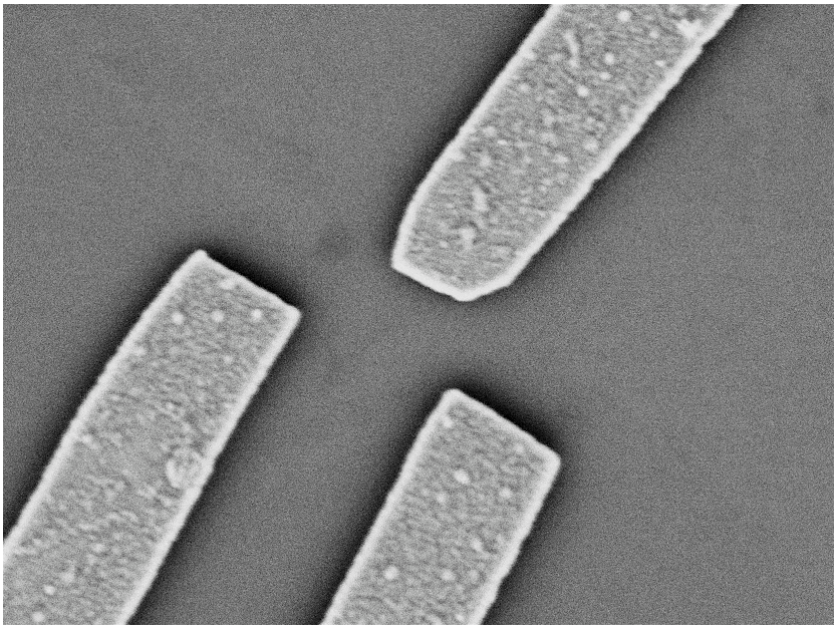


(b)

Figure 3.10: SEM nanowire contact images after passivation and metallization. (a) The same field of Fig. 3.9 with the evaporated contacts. (b) Detail of a contacted nanowire in the back-gate configuration. This is the measured wire of sample L_J1 (see Chap. 4).



(a)



(b)

Figure 3.11: SEM nanowire contact images of a lateral gate geometry. Three contacts are necessary to realize this configuration: source, drain and gate contacts. (a) The nanowire length between the contacts is about 1 μm. (b) Contacts without wire were realized for photoconductivity measurements crosscheck.

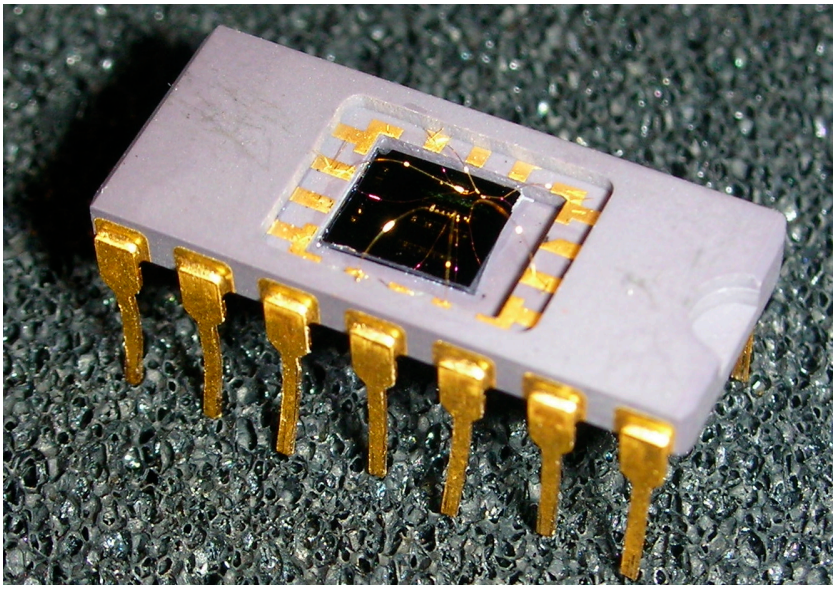


Figure 3.12: Sample bonded in the dual-in-line.

letter indicates the substrate upon which the device has been fabricated. The presence of a number refers to the part of the cleaved wafer. The second letter and the second number refer to the specific lane. The substrates were listed in section 3.2.

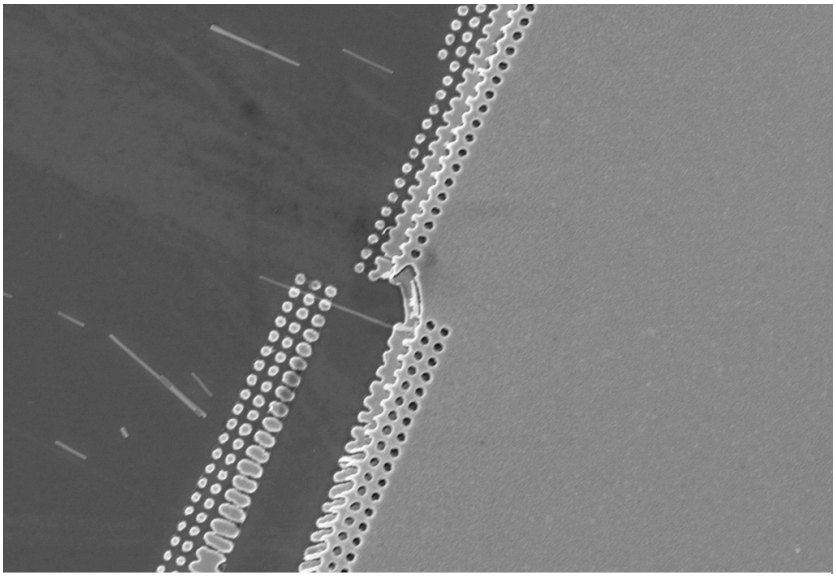
If nanowires are successfully contacted the sample is glued on a dual-in-line package and bonded as shown in Fig. 3.12. Then the dual-in-line can be easily placed in a dual-in-line pin carrier in order to perform measurements. The micro-solderings of the gold wire (25 μm diameter) on the sample and dual-in-line *pads* are realized with a semi-automatic instrument called *bonder*. The *bonder* has a tip that presses the gold wire on the sample with a given pressure and, by applying tuneable ultrasounds, melts the wire edge allowing the soldering. The bonding operation is eased by maintaining the sample at 60 °C during the entire process.

Lithography errors

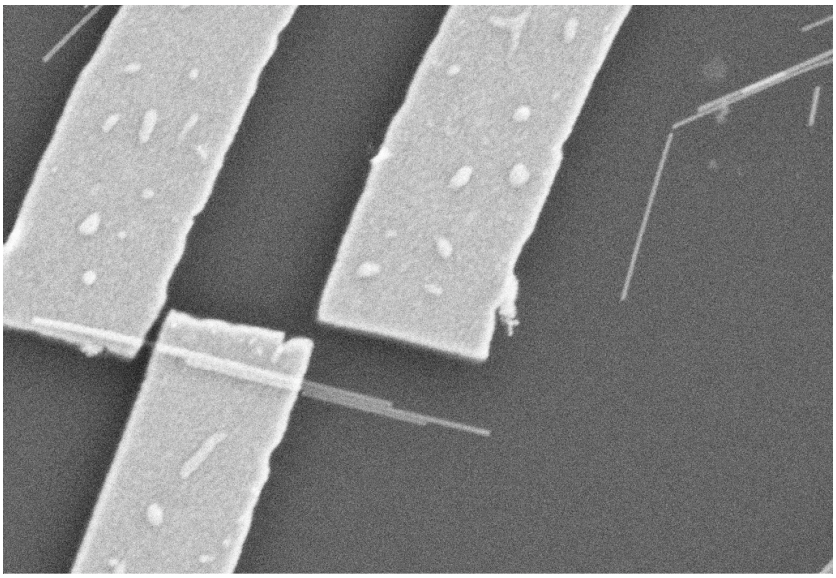
The devices listed in Tab. 3.2 are only a small part of the fabricated ones. In many cases difficulties were encountered in the lithographic process. Unlike for the optical lithography, in the electron beam lithography the control parameters must be changed according to the substrate type.

Different substrates require different exposure doses, in particular, the more insulating the substrate is, the higher the dose. For instance the SiO_2 substrate requires a higher dose than the GaAs substrate which is more conductive. The consequence of a low dose is shown in Fig. 3.13 (a). If the substrate is insulating, as it is the case with the SiO_2 substrates, the electrons of the *e-beam* give rise to charging effect linked to charge trapping on the sample surface. The accumulated charge can deflect the *e-beam*, affecting the lithography process. This effect is called *electron charging* and its consequences are shown in Fig. 3.13 (b). In this case an independent shift of the contacts is observed, with the result that the wire is missed and the gate is almost short-circuited to one of the contacts. In the same picture we see that the contacting attempt was on three sticked wires instead then on a single one. This latter error is due to the small nanowire size, so that in a SEM field view (for example Fig. 3.9 (b)), even with a zoom it is difficult to distinguish a single wire from few wires sticked together.

Besides, the spots on the gold contacts, on the same figure (Fig. 3.9 (b)), are *resist* molecules left after the development. This means that the electron exposure dose was slightly less than the required one (under-exposure). Under-exposed contacts can, however, work correctly and not affect transport measurements.



(a)



(b)

Figure 3.13: Undesired lithography effects. (a) Consequence of the underestimation of the electron exposure dose. (b) Charging effects deviate the *e-beam* and deform the designed contact geometry. Furthermore, with this magnification it is evident that the attempt of contact occurred on three sticked wires and not on a single one.

3.5 Measurement set-up

As discussed in the previous section the nanowire device has to be glued and bonded on the dual-in-line support in order to perform transport and optical measurements. Generally the sample was placed in the liquid nitrogen cryostat shown in Fig. 3.15 (b) but, for transport measurements at 4K, a dip stick to directly immerse the sample in the liquid He dewar was used. The cryostat allows to perform measurements at RT and at 77K and, thanks to its small window, it is possible to illuminate the sample and perform photoconductivity measurements.

Nanowires are very sensitive to electrostatic discharges and mechanical vibrations, thus samples must be handled very carefully. Set-up changing and any kind of displacement are a risk of considerable damage. Even during pumping operations and during measurements a close attention must be paid. Several nanowires were destroyed in these circumstances, probably because of electrostatic shocks.

3.5.1 Transport measurements

A potential difference is applied to the nanowire source contact with a Digital to Analog Converter (DAC 488HR/4). The same instrument, with another port, can independently drive a potential difference to the gate contact. The drain contact is connected to a SRS current amplifier, model SR570, that converts the current to a voltage signal, multiplying the signal by a maximum factor of $10^{12}V/A$. The converted current is read with an Agilent 34401A used as voltmeter reader. The DAC and the voltmeter are directly connected by a GPIB port to a computer in order to control the measurement. The *Labview* software allows to set a potential sweep to both the gate and the source contacts and, at the same time, read the output data.

A precaution was adopted to protect the nanowire from electrostatic shocks. Between the DAC and the nanowire, a voltage divider box was placed in order to apply low biases and to mitigate voltage fluctuations, preventing sample damaging.

A scheme of the transport measurement set-up is shown in the upper part of Fig. 3.14.

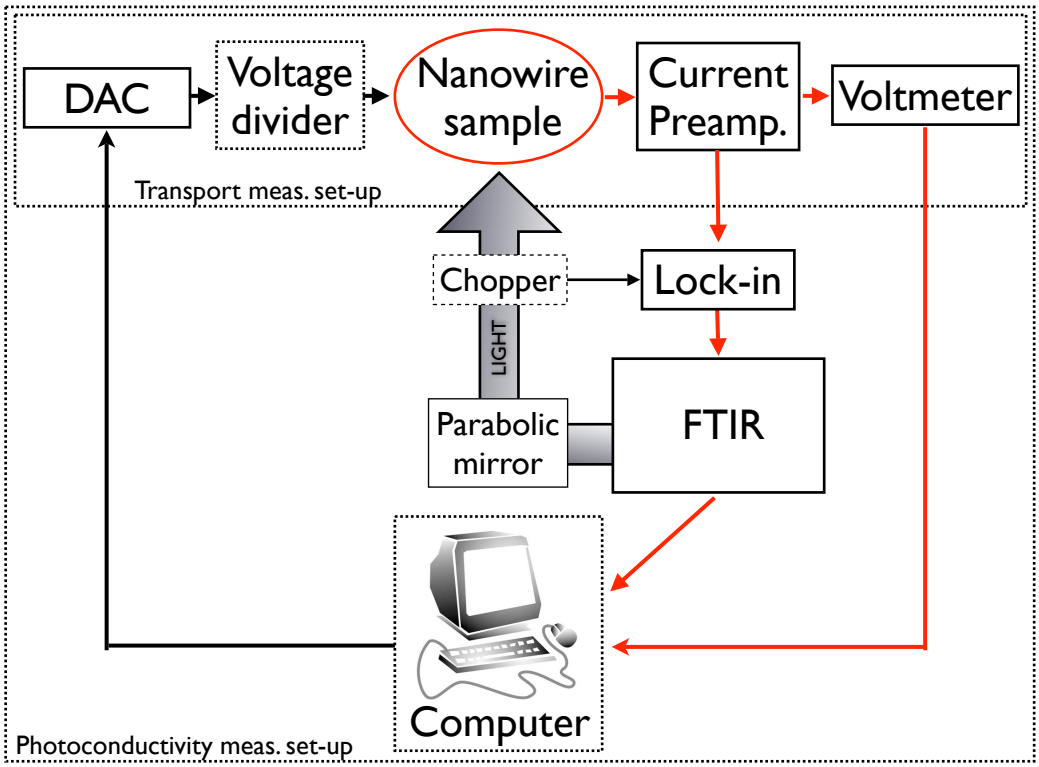
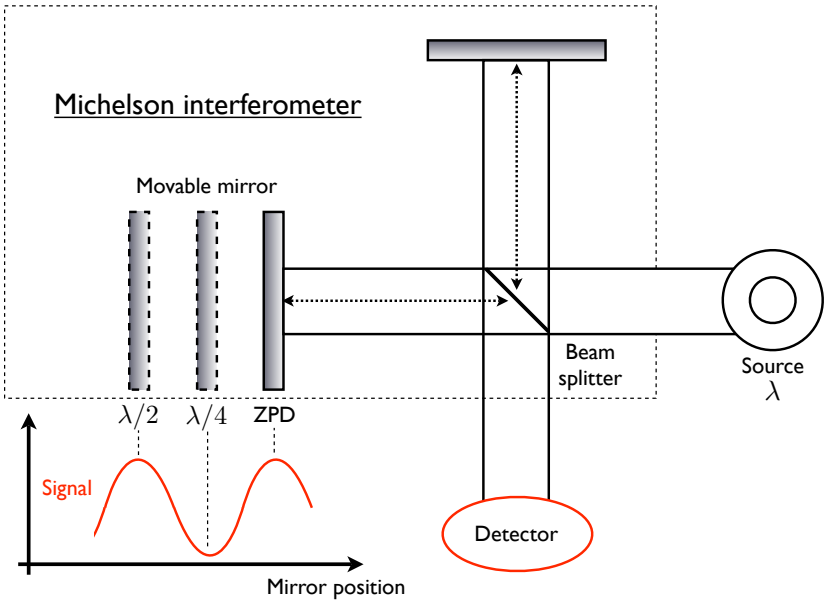


Figure 3.14: Transport and photoconductivity measurement set-up. Black (darker) arrows and red (lighten) arrows represent input and output signals respectively.

3.5.2 Optical measurements

As discussed in Chapter 2.2.2, the InAs nanowire energy gap is expected roughly at 400 meV. To perform photoconductivity measurements as function of the incident photon energy, a Fourier Transform Infrared Spectrometer (FTIR) was used.

The FTIR is a Thermo Nicolet model 870 (see Fig. 3.15 (b)). The working principle of a FTIR is based on Michelson interferometry, which is schematically shown in Fig. 3.15 (a), but can work with a continuum of light frequencies at the same time. Radiation from a source (usually a hot silicon rod, called glowbar) is split up into two beams by a beam splitter; one beam is reflected off a fixed mirror and the other off a moving mirror. The intensity of the two superimposed beams is recorded by a detector as function of the mirror position, giving what is called an interferogram. The



(a)

(b)

Figure 3.15: (a) Scheme of the Michelson interferometer on which the FTIR is based. The movable mirror is drawn in the Zero Path Difference (ZPD) position. (b) The right side of the interferometer is shown with the focussing parabola and the red cryostat.

spectral power density of the light is then obtained by Fourier transforming the interferogram.

The FTIR can work either using an internal detector, resulting very useful for absorption measurements, or with an external detector. In this latter case the FTIR light exits from a side hole and is then focalized on a sample. The external detector signal is then sent again to the FTIR. In our experiment the external detector is the nanowire device.

For certain measurements the photoconductivity set-up requires a chopper and a lock-in to analyze the signal and minimize the noise. A Perkin Elmer lock-in, model 5210, was used to treat the signal coming from the current preamplifier and, subsequently, to send it to the FTIR. Once the signal is sent again to the FTIR the interferogram can be collected and the spectra can be computed by Fourier transforming. The complete photoconductivity measurement setup is shown in Fig. 3.14.

Two different measurement types can be performed with the FTIR.

In the **step scan** measurement the interferometer mirror moves step by step integrating for each mirror position the lock-in signal. For this reason the lock-in integration time must be shorter than the step time. The interferogram is constructed position by position and is Fourier transformed at the end of the measurement. The measurement precision can be increased by increasing the number of positions.

In the **fast scan** measurement the lock-in is not necessary and the current preamplifier signal is directly analyzed by the FTIR. In this case the interferometer mirror moves continuously with a given velocity that generally ranges from 1 to 10 mm per second. The collecting time for a fast scan is short so that a less noisy spectrum is obtained making the average of many spectra.

The spectral intensity distribution that illuminates the sample is determined by the various optical components present in the light path:

- FTIR beam splitter, made of calcium floride (CaF_2):
  transparent to frequencies from 0.150 to 6.2 eV.
- The focussing medium, a parabolic gold coated mirror:
  reflective in the mid-infrared.

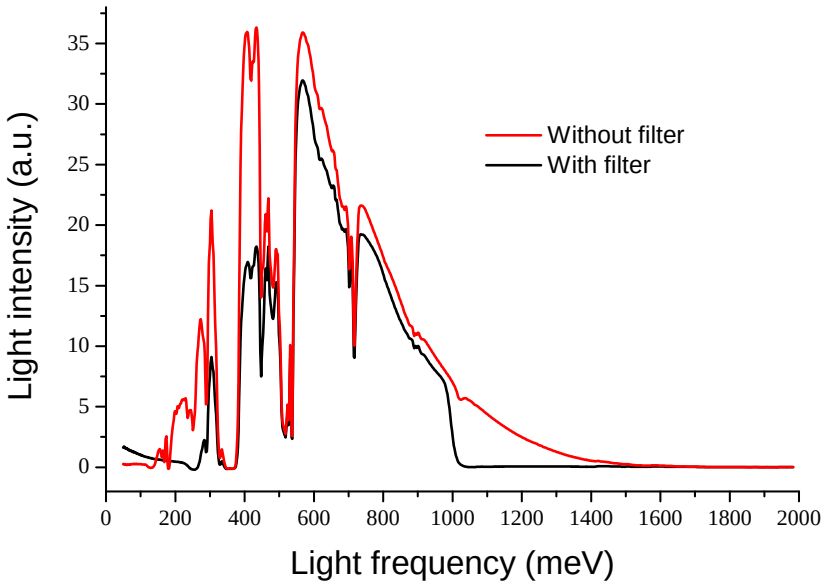


Figure 3.16: Spectra acquired with the FTIR internal detector, without filter (red line) and with filter (black line). It is evident that using the filter light frequencies above 1000 meV are not transmitted.

- The cryostat window, made of potassium bromide (KBr):

  transparent to frequencies from 0.060 to 3.1 eV.

For all optical measurements the white light surce was used. The white light emits in wide range from 0.25 to 3 eV. Considering all the filtering media listed above, the sample is surely illuminated by frequencies from 0.25 to 3 eV.

Filter for GaAs substrate

If the GaAs substrate is used, photons of frequency higher than the GaAs energy gap can generate a photocurrent. This photocurrent would cause an undesired signal, covering the nanowire signal. For this reason a low pass filter was added along the optical path and frequencies that could excite electrons above the GaAs energy gap are cut. The GaAs energy gap is at about 1400 meV [42] and, as shown in Fig. 3.16, the chosen filter cuts frequencies above 1000 meV.

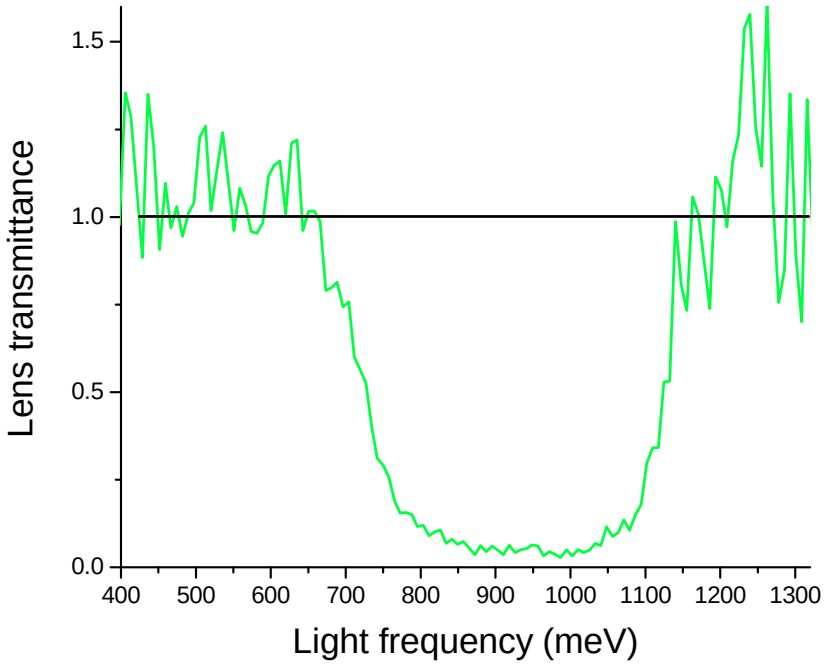


Figure 3.17: Zinc selenide (SeZn) lens transmittance.

Zinc selenide lens

Before employing parabola for focussing the light, the standard converging zinc selenide lens of the set-up was used. It was then discovered that the coating cuts the useful frequency range from 0.7 to 1.1 eV. For this reason the lens was discarded The computed transmittance spectrum of the zinc selenide lens is shown in Fig. 3.17.

Ultra-fast laser

In order to measure the photoconductive response at higher light intensity a laser source was used.

An ultra-fast laser set-up was available. As shown in Fig. 3.18 the ultra-fast set-up is composed by three main parts: a Ti:Sapphire high energy laser (black box behind the monitor), a parametric amplifier (white box on the right) and a Difference Frequency Generator (DFG, white box on the left). The Ti:Sapphire laser belongs to the Libra series of *Coherent* that generates 100 fs pulses of 800 nm wavelength at a repetition frequency of 5 kHz. The *Topas* parametric amplifier from *light conversion* uses the light input of the

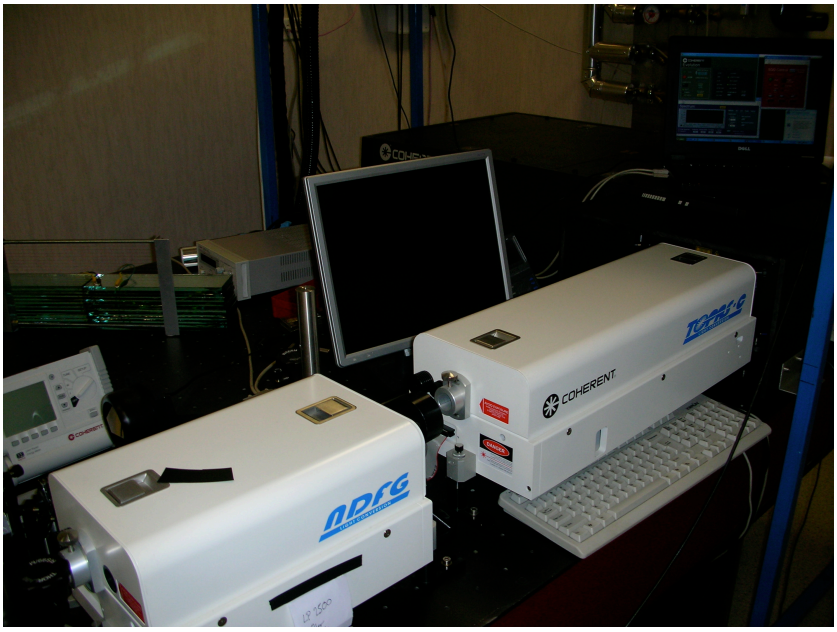


Figure 3.18: Picture of the ultra-fast laser.

Ti:Sapphire laser and generates two beams with wavelength in a range from 1.1 to 2.6 μm. Subsequently the DFG generates the difference frequency of the two, extracting a wavelength ranging from 2.4 to 20 μm. The whole ultra-fast laser set-up is controlled by a computer program. Combining the different instruments, the laser outputs pulses of 100 fs, at 5 kHz, have a maximum power of about 200 mW depending on the output frequency.

Chapter 4

Transport and photoconductivity measurements

4.1 Capacitance model

As mentioned in section 2.1.3 in order to study the transport properties of the nanowires it is necessary to refer to an electrostatic model. The purpose of the model is to calculate the capacitance of the nanowire-gate system, already termed $C_{wire-gate}$. With the value of the capacitance it is then possible to obtain an estimate of the electron mobility μ and of the density charge n in the wire.

In the back-gate configuration the system can be approximated with an infinite conductive plane (the gate) and an infinite conductive cylinder. The system capacitance per length unit of the cylinder is analytically known trough Eq. 2.7. This model, however, has the limit of considering the nanowire as embedded in the dielectric medium that separates it from the gate, while the wire is lying on the substrate surface and it is surrounded by air. The dielectric index changes at the surface and, as a consequence, the charge distribution on the wire is different from the embedded case.

In the lateral-gate geometry it is not trivial to analytically solve the problem because the system is even less symmetric than the back-gate configuration. As a matter of fact in the back-gate configuration (see Fig. 3.10 (b)) the system can be approximated to a cylinder in front of a plane, while a simple approximation is not possible for the lateral gate configuration (see Fig. 3.11). A smaller value of the capacitance is expected anyway in the lateral-

gate geometry, since the coupling between nanowire and gate is weaker. This is due to a generally larger distance from the gate and to the smaller gate surface extension.

In order to calculate more precise values of the transport parameters in the back-gate geometry and to calculate realistic values in the lateral-gate configuration, it was decided to develop a 3D model. An adequate software package [1] based on a finite element analysis has been chosen to draw the geometric configurations and solve the electrostatic problem. The AC/DC module of the package simulates electrical components and devices for electrostatics, magnetostatics and electromagnetic quasi-statics applications. Such a package allows to impose boundary conditions on the necessary surfaces and to solve the electrostatic problem in the whole 3D space.

Considering a system of N conductors, each at potential V_i and with total charge Q_i:

$$Q_i = \sum_{j=1}^{N} C_{ij} V_j \qquad (i = 1, 2, ..., N) \tag{4.1}$$

The coefficents C_{ii} are called capacities or capacitances while the C_{ij}, $i \neq j$, are called induction coefficients. The *capacitance of a conductor is therefore given by the total charge on the conductor when it is maintained at unit potential, all other conductors being held at zero potential* [43].

Considering the nanowire and the gate contact as conductors, the capacitance $C_{wire-gate}$ can be found imposing a potential of 1V on the nanowire surface and 0V (that is equivalent to the ground condition) on the gate. After the computation it is necessary to integrate the surface charge density on the cylinder boundary and this value, in the 3D case, corresponds to the capacitance.

4.1.1 2D model

To check the reliability of the method explained above, a direct comparison was made with the case of the infinite plane in front of the infinite cylinder. The analytical solution expressing the capacitance per unit length is:

[1] *COMSOL*, http://www.comsol.com (formerly FEMLAB)

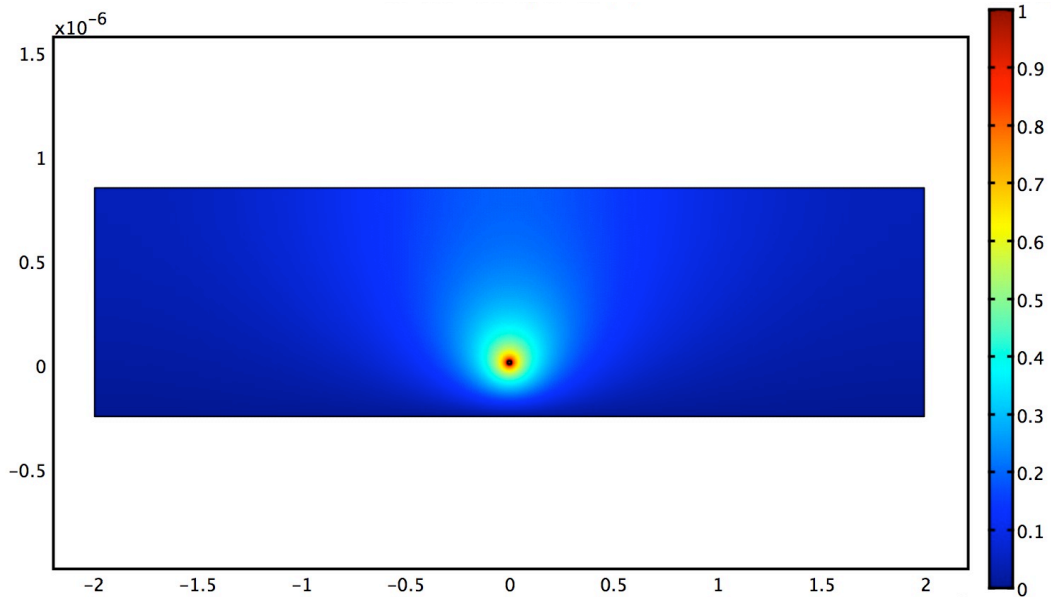


Figure 4.1: Potential 2D plot of a nanowire surrounded by air in the back-gate configuration. The nanowire is represented as a circle and the back-gate is the base edge of the rectangle box.

$$\frac{C_{wire-gate}}{L} \cong \frac{2\pi\epsilon\epsilon_0}{ln(\frac{2h}{r})} \tag{4.2}$$

where r and h are respectively the nanowire radius and its distance from the gate. Considering a 20 nm diameter nanowire embedded in SiO_2 ($\epsilon = 4.5$) placed 250 nm from the gate, we obtain: $C_{wire-gate}/L = 6.34 \cdot 10^{-11} F/m$.

To simulate with the software package the general case of the infinite plane and infinite cylinder, it is convenient to use a 2D model. In Fig. 4.1 the nanowire is represented as a circle and the back-gate is the base edge of the rectangle box. The circle is set at 1V, the base edge at 0V and the other box edges are set at 0 charge. This configuration shows a translational symmetry in the direction orthogonal to the drawing.

For the specific computation the same values of ϵ, h and r as in the analytical case are used. The electrostatic problem in the rectangle was solved and the potential obtained with this configuration is plotted in Fig. 4.1.

By integrating the charge density on the border of the circle, a value of the $C_{wire-gate}/L$ is computed.

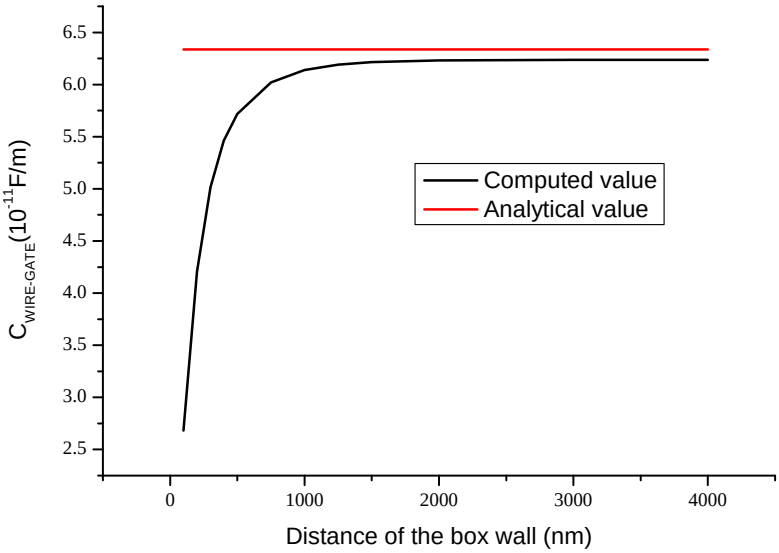


Figure 4.2: The red horizontal line represents the constant value of the capacitance computed with the analytic formula. The black curve links twelve computed values of the capacitance per unit length as function of the box base. A good agreement between the two methods is evident for box bases larger than 3000 nm.

The plane should be infinite so that the rectangle base should be equally infinite. Obviously it is not possible to solve the electrostatic problem in an infinite box size and an approximation is necessary. It is reasonable to draw a rectangle with a base edge much greater than the wire diameter, but on the other hand the larger the rectangle surface the more computationally demanding the problem is. To reach a satisfactory balance between those two requirements, different values of the capacitance per unit length were computed varying the size of the rectangle base.

In Fig. 4.2 it is clear that increasing the base of the rectangle box, the computed value tends with a good approximation to the analytical one. For box larger than 3000 nm (that corresponds to a distance of the box wall from the nanowire of 1500 nm) the agreement between the two methods is greater than 98%.

For the 2D simulation the chosen rectangle height was about four times larger than the nanowire-gate distance. It was verified that once the box base is larger than 3000 nm the box height doesn't affect significantly the

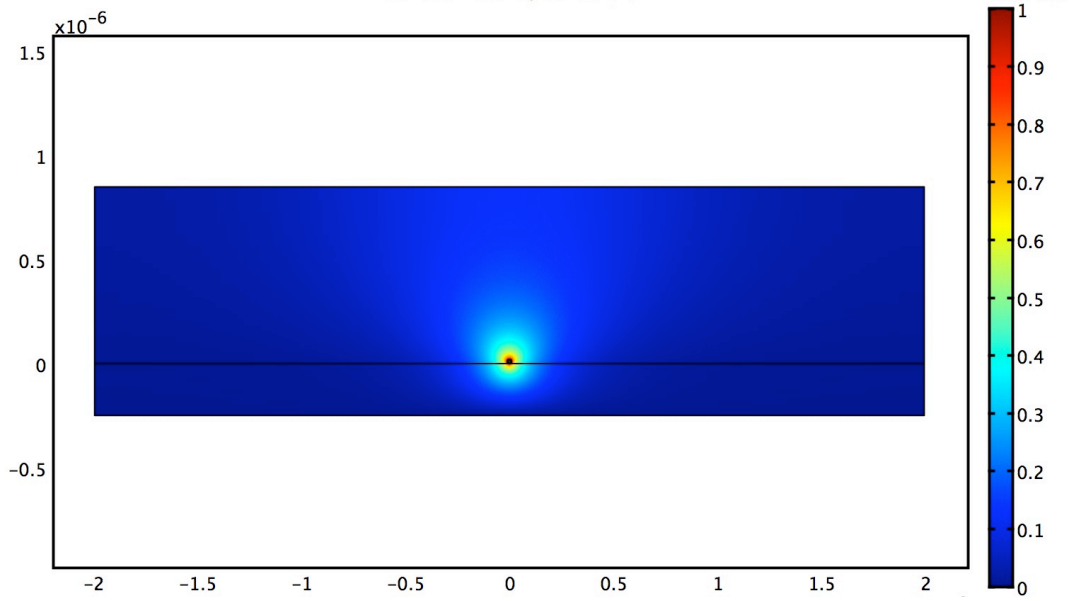


Figure 4.3: Potential 2D plot of an air surrounded nanowire in the back-gate configuration. The nanowire is represented as a circle and the back-gate is the base edge of the rectangle box. The black horizontal line, tangent to the wire, represents the separation edge between the two dielectrics (air and SiO_2).

capacitance per unit length. The plot obtained in Fig. 4.1 was computed in a box of 4000 nm of width giving a $C_{wire-gate}/L = 6.23 \cdot 10^{-11} F/m$.

The good agreement of the finite element simulation with the analytic formula allows to improve the computed $C_{wire-gate}/L$ by assuming a more realistic hypothesis. In reality the wire is not embedded in SiO_2, but is lying on the dielectric surface and it is surrounded by air. This case is simple to solve, dividing the rectangle in two parts, one below the wire with the SiO_2 dielectric constant ϵ, the other in the upper part with ϵ equal to one. The potential plot is shown in Fig. 4.3 and the result is evidently less symmetric than for the embedded case (see Fig. 4.1). In this case the capacitance per unit length is almost halved, $C_{wire-gate}/L = 3.46 \cdot 10^{-11} F/m$.

A summary of the capacitance values obtained with the 2D models is shown in Tab. 4.1.

Method	Linear Capacitance ($10^{-11} F/m$)
Analytical, embedded	6.34
Finite element, embedded	6.23
Finite element, in air	3.46

Table 4.1: Results of the 2D simulation compared with the analytical value.

4.1.2 3D Model

As shown in the previous section, with the 2D model it is possible to correctly calculate the value of the capacitance considering also that the wire is surrounded by air. To take into account the correction of the nanowire finite length and, besides, to simulate the lateral-gate it is necessary to implement the model in 3 dimensions. In 3D the problem is solved in the volume of a parallelepiped box. To chose the box sixe we started from the results of the 2D model. The box width and height were held unchanged, respectively ~ 4000 nm and ~ 1000 nm. The box length was chosen to be approximately the same as the width. It was observed that changing the box length, the total computed capacitance displays only small variations. To cross-check the reliability of the 3D model, an embedded nanowire in the back-gate configuration is simulated. With a nanowire length of 1 μm the computed capacitance is $C_{wire-gate} = 6.90 \cdot 10^{-17} F$.

This value divided by the nanowire length must be compared with the capacitance per unit length computed with the 2D model. It was found that the agreement was within 10%. To understand the cause of this discrepancy the same calculation was performed for other two nanowire lengths, keeping the same box length, and the results are listed in Tab. 4.2. For longer nanowires the capacitance per unit length converges to the capacitance per unit length of an infinite wire. Therefore the above mentioned 10% difference in the computed capacitance appears really due to the finite length of the wire.

Hereinafter the 3D models are shown for every significant geometric configuration. The nanowire length and the distance between gate and wire are approximately the real ones, and can obviously change according to the device.

For simplicity, the nanowire length used in the simulation is restricted

Nanowire Length (μm)	Computed Cap. ($10^{-17}F$)	Corresponding linear Cap. ($10^{-11}F/m$)	Percentage variation
1	6.90	6.9	10,8%
2	12.89	6.45	3.5%
3	18.81	6.27	0.6%

Table 4.2: Computed capacitance in 3D for an embedded nanowire in the back-gate configuration. The result is directly compared with the 2D simulation dividing the capacitance by the nanowire length. The percentage variation from the linear capacitance computed in the 2D model is shown in the last column.

to the part surrounded by air excluding the part covered by metal contacts. In such a way the screen effect of the contacts is not computed; this would tend to reduce the charge on the wire and consequently the capacitance of the system. Five different devices have been simulated.

The three simulations for 20 nm diameter nanowires are:

- L_J1, back-gate configuration.
  Computed capacitance: $C_{wire-gate} = 2.96 \cdot 10^{-17}F$.

- Q1_E3, lateral-gate configuration.
  Computed capacitance: $C_{wire-gate} = 1.32 \cdot 10^{-17}F$.

- R2_E2, lateral-gate configuration.
  Computed capacitance: $C_{wire-gate} = 7.4 \cdot 10^{-18}F$.

The two simulations for 40 nm diameter nanowires are:

- O_E1, lateral-gate configuration, 40 nm diameter nanowire.
  Computed capacitance: $C_{wire-gate} = 1.99 \cdot 10^{-17}F$.

- P2_M2, lateral-gate configuration, 40 nm diameter nanowire.
  Computed capacitance: $C_{wire-gate} = 2.49 \cdot 10^{-17}F$.

Two 3D model images, with a zoom in of the nanowire, are successively shown. A back-gate configuration is shown in Fig. 4.4 (L_J1) and a lateral-gate configuration is shown in Fig. 4.6 (Q1_E3).

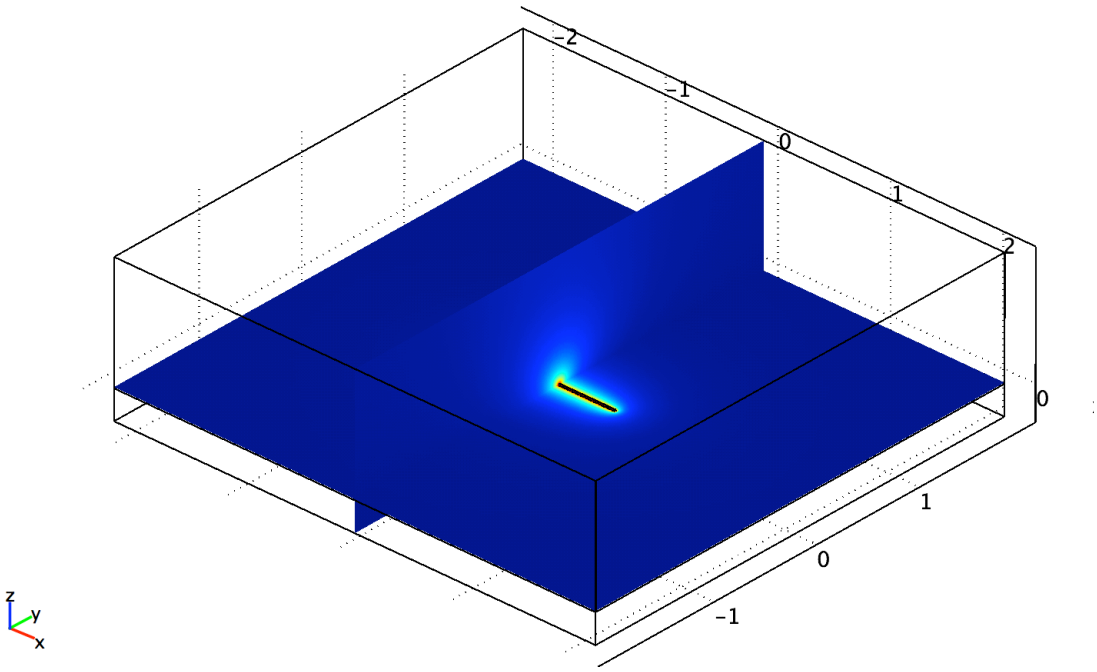


Figure 4.4: 3D model of sample L_J1 with a back-gate geometry. The electrostatic problem is solved in the box volume and two perpendicular planes were chosen to plot the electrostatic potential. Distances on both axes are in μm. A zoom in of the nanowire with the electrostatic potential intensity legend is plotted in Fig. 4.5.

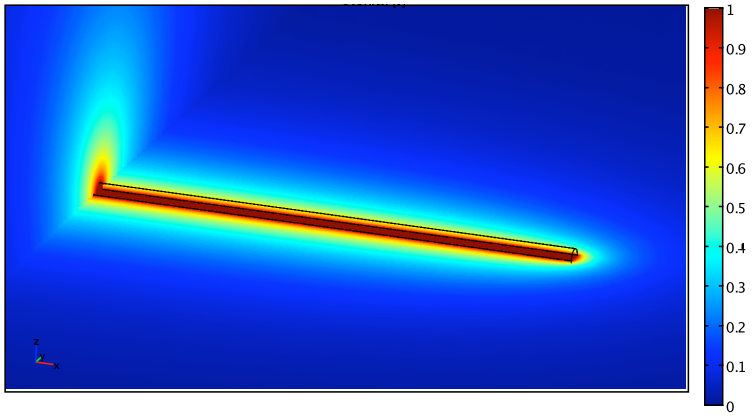


Figure 4.5: Zoom in of Fig. 4.4. Half of the nanowire is shown with a plot of the normalized electric potential.

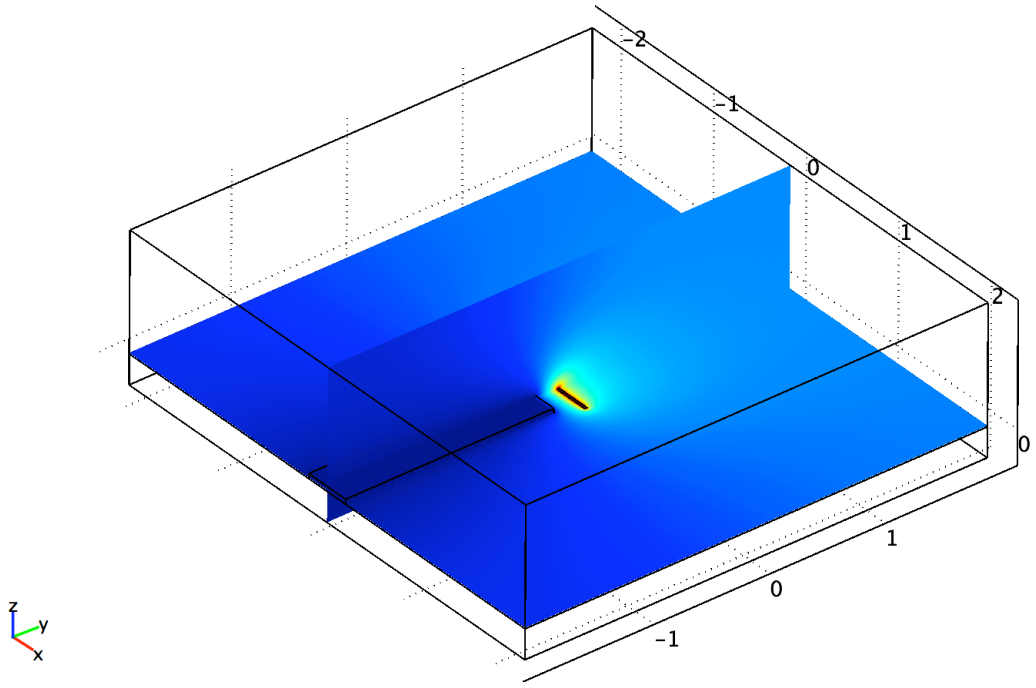


Figure 4.6: 3D model of sample Q1_E3 with a lateral-gate geometry. The electrostatic problem is solved in the box volume and two perpendicular planes were chosen to plot the electrostatic potential. Distances on both axes are in μm. A zoom in of the nanowire with the electrostatic potential intensity legend is plotted in Fig. 4.7. Distances on both axes are in μm.

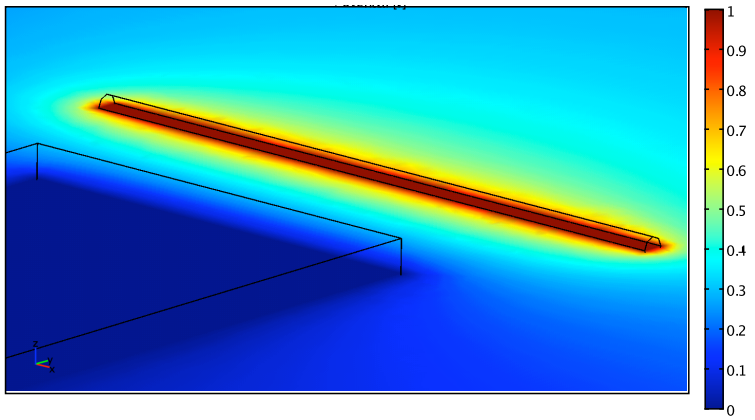


Figure 4.7: Zoom in of Fig. 4.6. The nanowire with an electric potential of 1V is shown aside of the lateral-gate (0V). The normalized electric potential is plotted with different colors.

4.2 Transport measurements

In this section the transport measurements performed on different samples are described and their dependence on measuring conditions and structural parameters, as explained in Chapter 2, are verified. An example of gate-sweep fit, as described in section 2.1.3, is given and then some peculiar effects are pointed out. Those effects must be taken into account in defining an analysis methodology. At the end of the section, the computed electron mobility and charge density are presented and discussed.

Close to zero source-drain voltage an ohmic behaviour is expected for properly contacted nanowires. A useful measurement that confirms that the nanowire is working correctly is then the linear dependence of the source-drain current vs. the source-drain voltage (IV) at different values of the gate. In particular the device *gating* effect has to be verified. More precisely for higher gate voltage values, the nanowire conductance increases and the angular coefficient of the IV curve increases as well (discussed in section 2.1.2).

As an example here I report the IV plot at different gate potentials of the sample L_J1 (back-gate configuration). The measurement was made at room temperature with the gate voltage ranging from 1 V to -0.3 V (see Fig. 4.8). It is evident that the gate works correctly, controlling the nanowire conductance and progressively turning off the wire current.

To estimate the pinch-off voltage and to calculate the transconductance of the device it is useful to measure the source-drain current vs. the gate voltage. This measurement is commonly called gate-sweep and is characterized by a pinch-off voltage at which the nanowire starts to conduct. As expected (see section 2.1.2) the pinch-off depends on the nanowire size and on the temperature.

In Fig. 4.9 three gate-sweep curves are shown for two different nanowires. The green line is a room temperature measurement of a 40 nm diameter nanowire (sample O_E1) with a pinch-off at about -1 V. The red line is the gate-sweep of a 20 nm diameter nanowire (sample Q1_E3) and presents a pinch-off at about -0.5 V. The same 20 nm diameter nanowire was then measured at 77 K and the pinch-off was found higher than 0.5 V (for a comment on the steepness see later). The theoretical predictions of the pinch-off trend as function of diameter and temperature exposed in Chapter 2 are

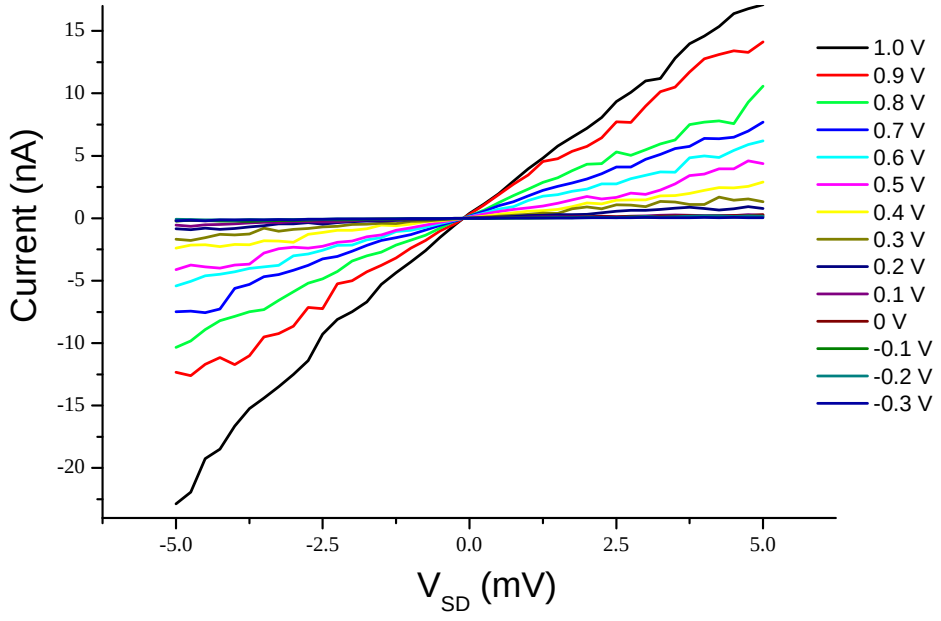


Figure 4.8: Nanowire IV at different gate voltages (V_g) of the sample L_J1 (V_g values are shown in the side legend). An ohmic behaviour is measured for low V_{SD}. The current decreases by decreasing the gate voltage.

indeed verified.

It must be observed that the pinch-off of the 20 nm diameter nanowire at low temperature takes place at a positive gate voltage value. A positive pinch-off voltage means that the nanowire has no free charge and to make it conduct a charge must be provided from the contacts. By applying a positive voltage, electrons are forced to populate the nanowire conduction band. In this case the model presented in section 2.1.3 cannot be applied because no charge is contained in the nanowire.

It has to be noted that the comparison was made between nanowires in different gate configurations. As already specified, the 40 nm diameter nanowire belongs to sample O_E1 and the 20 nm diameter nanometer belongs to the Q1_E3 sample. Those two samples, however, were chosen because of their similar capacitance value (see capacitance data at the end of section 4.1.2).

As previously mentioned, from the gate-sweep curve it is possible to estimate the transconductance of the device. Knowing the nanowire-gate capacitance ($C_{wire-gate}$ computed in the last section) and the transconductance (fitted from the gate-sweep plots), one can then extract the electron mobility

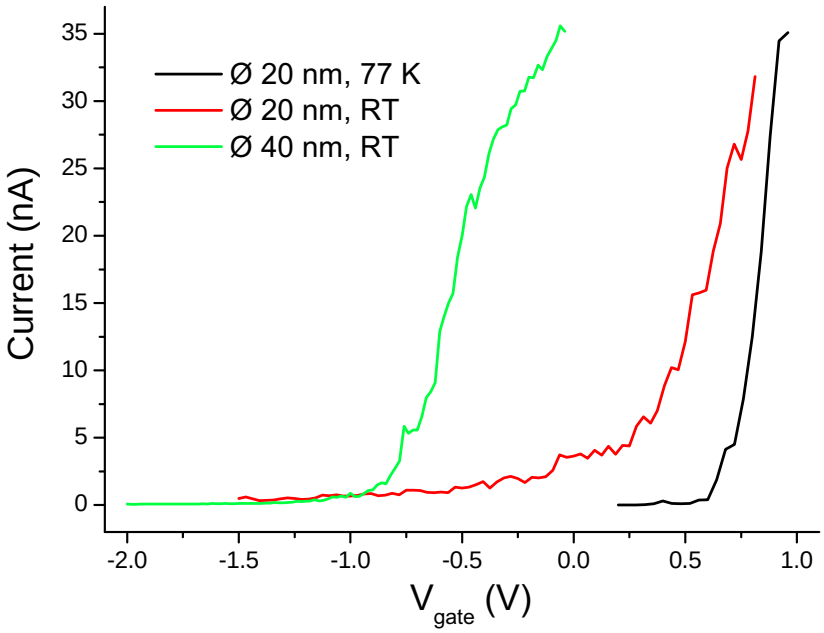


Figure 4.9: Size and temperature dependence of nanowire transport. Three different gate-sweeps are shown: (*green line*) 40 nm nanowire of sample O_E1 at RT, (*red line*) 20 nm nanowire of sample Q1_E3 at RT, (*black line*) 20 nm nanowire of sample Q1_E3 at 77 K.

with the model presented in section 2.1.3.

Estimates of the electron mobility are already existing in the literature for wires from 35 nm diameter up. It is therefore very interesting to investigate the electron mobility in thinner wires, and, at the moment, 20 nm is the smallest diameter that can be produced in our CBE chamber. It has to be stressed that, thanks to the more precise capacitance values computed with the finite element simulation, more accurate values of the electron mobility and of the charge density can be obtained. An ideal procedure is to compute the electron mobility and the charge density for each gate-sweep at a given source-drain voltage. Then an average value with a statistical uncertainty is calculated. For this reason, for every nanowire the gate-sweep was measured at different source-drain voltage values.

Intrestingly, some peculiar effects occur in these transport measurements:

- Gate-sweep hysteresis

  During the gate-sweep measurements of 20 nm diameter nanowires

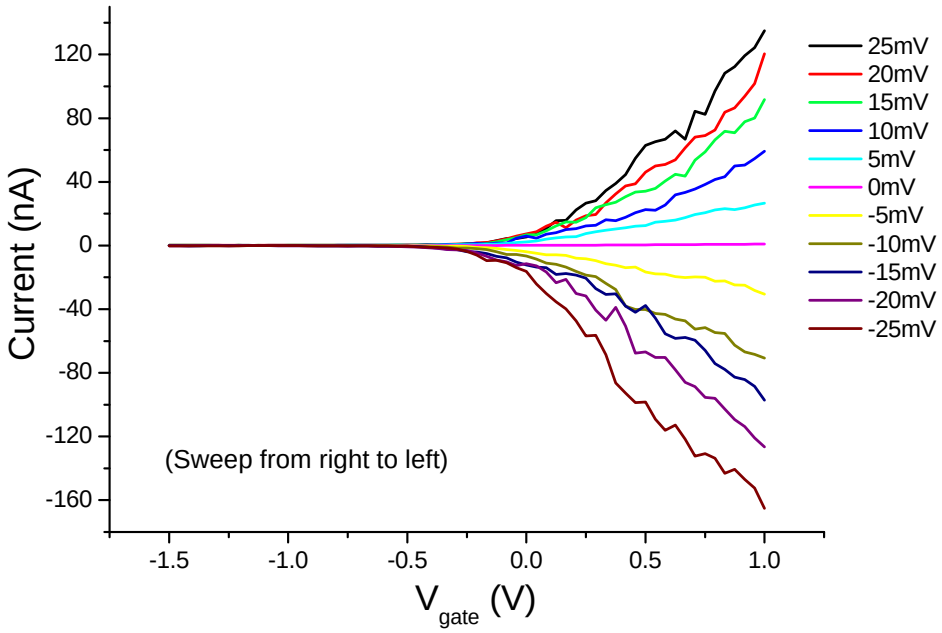


Figure 4.10: Sample L_J1, room temperature. Gate-sweep at different source-drain voltages (V_{SD} values are shown in the side legend). The sweep was made decreasing V_g to study the hysteresis effect.

(Sample L_J1) an hysteresis effect was observed. This means that the gate voltage sweep gives a different current value if performed increasing the V_g or decreasing it. This effect was not observed for 40 nm nanowires and for sample R2_E2.

For this reason two gate-sweep plots for the sample L_J1 were measured. Both measurements are room temperature gate-sweep at different source-drain voltages, in particular:

- Sweep decreasing V_g in Fig. 4.10.
- Sweep increasing V_g in Fig. 4.11.

The hysteresis effect in 20 nm diameter nanowires was measured also at low temperature (77 K) as shown in Fig. 4.12.

- Source-drain voltage sign asymmetry

  Another unexpected effect observed during measurements is the asymmetry of the gate-sweep at different source-drain voltages. It turns out

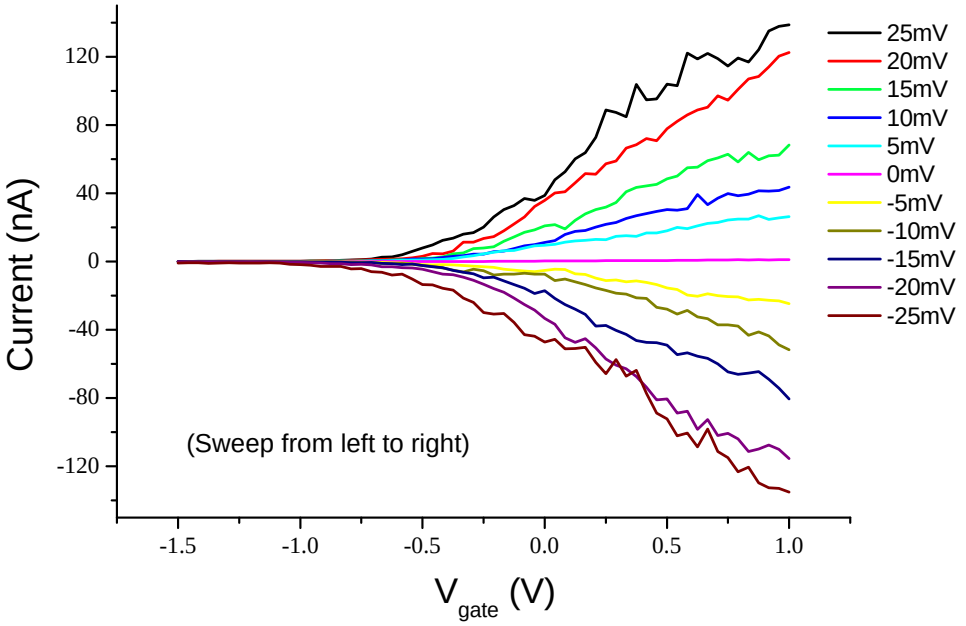


Figure 4.11: Sample L_J1, room temperature. Gate-sweep at different source-drain voltages (V_{SD} values are shown in the side legend). The sweep was made increasing V_g to study the system transconductance.

in certain cases that the gate-sweep curves are not symmetric with respect to the zero current line. An example is given in Fig. 4.13. This effect is due to the differences between the source and the drain contacts making the system not symmetric for a current direction change. Those differences are probably caused by the different size of the surface contacts or impurities between nanowire and metal. This asymmetry confirms the importance, expressed in section 2.1.2, of a good quality ohmic contact for such reduced dimensions. Even if the fabrication is well tested it can happen, as in the above case, that contacts affect transport measurements.

In Fig. 4.14 a typical linear fit of the gate-sweep is shown. Since, as already seen in Fig. 4.9, the trend close to the pinch-off can be more or less steep, I decided to fit the gate-sweep always in a range in which it appears to be linear. Consequently the threshold voltage is given by the intercept of the linear fit with the x-axis. This choice is supported by the example given in Fig 2.6.

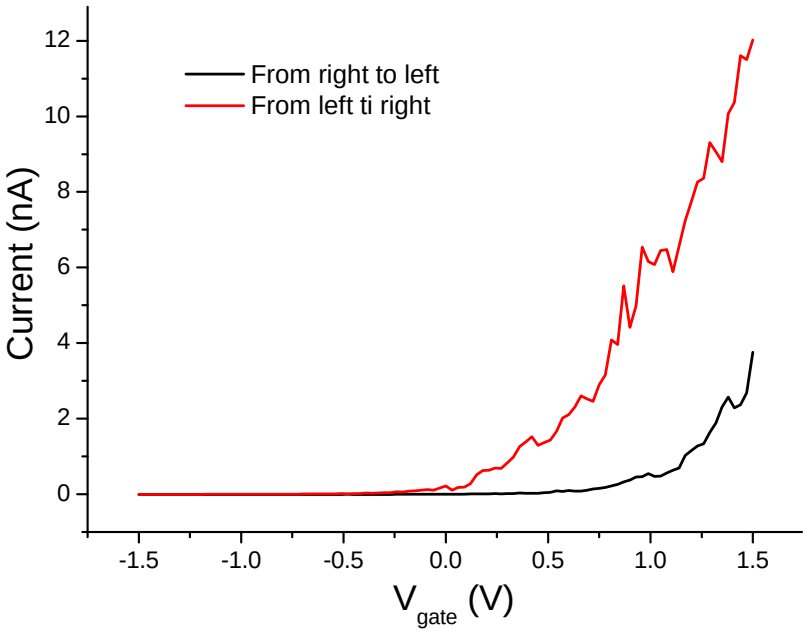


Figure 4.12: Sample L_J1, low temperature (77 K). Gate-sweep for the two opposite sweep directions with an evident hysteresis behaviour.

The hysteresis effect and the source-drain voltage asymmetry force to define different analysis procedures for each sample. In order to compute a more accurate electron mobility value it would be appropriate to have several gate-sweeps at different source-drain voltages as in the case shown in Fig. 4.10, Fig. 4.11 and Fig. 4.13. If the pinch-off has a negative voltage, from each single gate-sweep it is possible to extract a mobility value. This procedure was adopted when possible and allows to compute an error on the mobility. Each series of measurements will be discussed separately in the following.

O_E1 (40 nm diameter, homogeneous)

This is the only sample for which it was possible to apply the model both at RT and at 4K. In both cases the pinch-off voltage is negative and the model can be applied.

At room temperature only one gate-sweep was available and the computed mobility is $\mu_{RT} = 3390\, cm^2/Vs$ that is comparable with the literature values

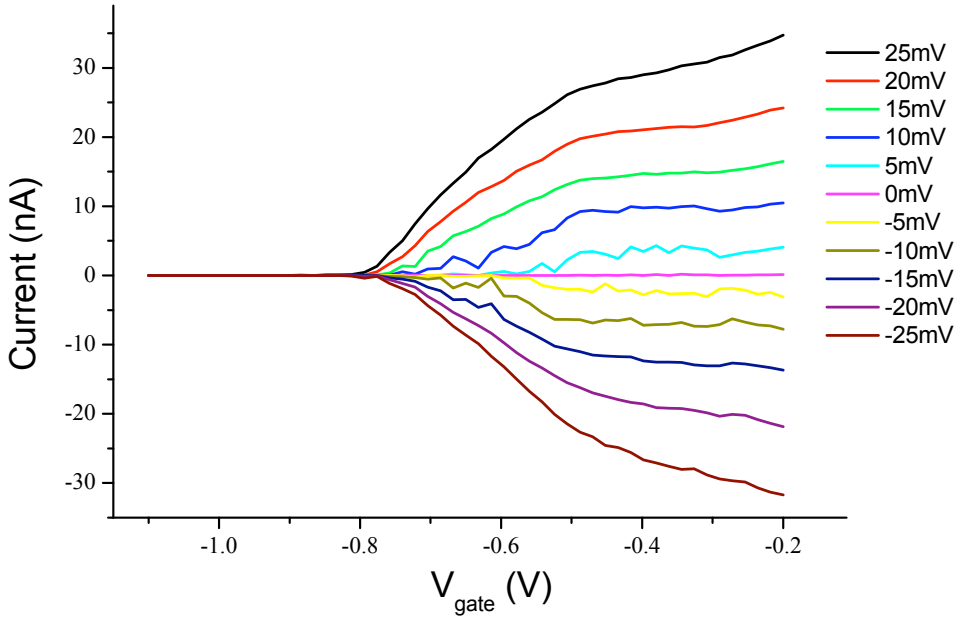


Figure 4.13: Sample O_E1, very low temperature (4 K) gate-sweep at different source-drain voltages (V_{SD} values are shown in the side legend). The asymmetric behaviour of the gate-sweep for positive and negative source-drain voltages can be noticed.

presented in 2.1.3 for nanowires of the same diameter.

At low temperature several gate-sweeps at different source-drain voltages were available (see Fig. 4.13). To have consistent mobility values it was chosen to fit only the four gate-sweeps with source-drain voltage higher than 10 mV. The average electron mobility, with its standard deviation, resulting from the four gate-sweeps, is $\mu_{4K} = 1700 \pm 510\, cm^2/Vs$. A higher value of the mobility for the 4K measurement would be expected, as the mobility increases by decreasing the temperature. However this result could be justified by the electron freezing. Decreasing the temperature, electrons are more easily trapped by the superficial states and the conduction decreases.

P2_M2 (40 nm diameter, core-shell)

Five gate-sweep curves were fitted to obtain a value of the mobility, $\mu_{RT} = 1360 \pm 350\, cm^2/Vs$. All these curves have a positive source-drain voltage. The 3 nm of shell should increase the mobility value with respect to the

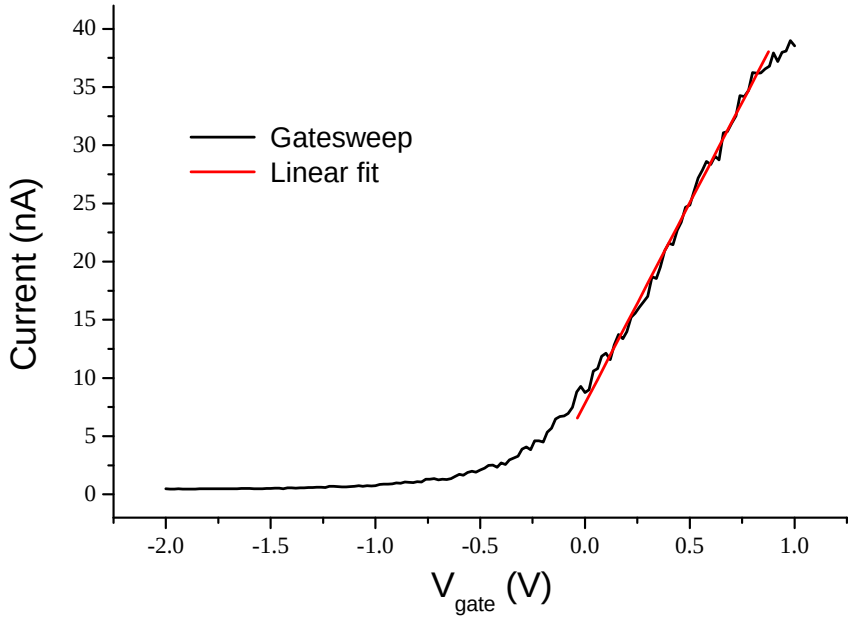


Figure 4.14: The black line is the gate-sweep of O_E1 sample measured at room temperature with a bias V_{SD}=5 mV. The straight red line is the linear fit of the gate-sweep in a chosen range (from 0V to 1V).

previous case, reducing the impact of the surface states, but this does not seem to happen. The cause could be due to imperfections on the shell, barely visible in SEM pictures, but it also can be the by-product of a non perfect HCl treatment (see section 3.3), resulting in high contact resistance.

L_J1 (20 nm diameter, homogeneous)

From both L_J1 gate-sweep groups (Fig. 4.10 and Fig. 4.11) it would be possible to compute an electron mobility value. A criterion must be found to choose on which sweeps to perform a fit. In a paper by S. Roddaro [44] the same hysteresis behaviour was found for the measurement of several nanowires in parallel.

It was already experimentally proved that the capacitance changes depending on the sweep direction. The authors of the above cited paper conclude that only the sweep decreasing the gate voltage ($C_{\downarrow}(V)$) results from an equilibrium distribution of charges. The equilibrium distribution in $C_{\downarrow}(V)$ refers in particularly to the charges at the nanowire interfaces, while a long-

lived out-of-equilibrium distribution is present in the other sweep direction ($C_{\uparrow}(V)$). This assumption is proved by the fact that time dependent measurements indicate that capacitances tend to relax from $C_{\uparrow}(V)$ toward $C_{\downarrow}(V)$ on a time scale of about 30 minutes. The hysteresis behaviour is treated from a phenomenological point of view in the paper of O. Karlstrom [45].

With the support of the previous analysis it was chosen to fit only the data shown in Fig. 4.10 and the average electron mobility value computed from the ten gate-sweeps is $\mu_{RT} = 1970 \pm 180\, cm^2/Vs$. In this case many gate-sweep curves were used to compute the mobility so that the standard deviation is significantly smaller than the previous values.

The computed mobility value is smaller than that of sample O_E1 measured at RT. A possible explanation for this decrease of electron mobility could be due to the combination of the surface trapping effect and the smaller diameter. The surface volume ratio increases by decreasing the diameter and consequently at smaller diameter the surface states play a major role in the electron transport. Hence we suppose that for a 20 nm diameter nanowire the surface trapping can significantly affect carrier conduction with respect to a 40 nm diameter one.

R2_E2 (20 nm diameter, homogeneous)

For the R2_E2 case, as in the case of O_E1, only a gate-sweep was available since most of the measurements were performed at low temperature. The resulting mobility is $\mu_{RT} = 1450\, cm^2/Vs$ that, as the mobility computed for L_J1, is smaller then the one computed for a 40 nm diameter nanowire.

In Tab. 4.3 the electron mobility and charge density results are summarized.

It has to be noticed that the simple model presented in section 2.1.3 considers only the nanowire resistance, while in all our measurements the sum of contacts and nanowire resistance was measured. Therefore the model was applied considering the total resistance due to the wire or, in other words, with the hypothesis of a negligible contact resistance. The consequence of such assumption is an underestimation of the mobility; the computed results must be intended as a lower bound for the electron mobility of InAs nanowires. Obviously higher mobility values could be achieved by subtracting this series

Sample	Temp	Diam (nm)	$C_{wire-gate}$ $(10^{-18}F)$	V_{th}(V)	Mobility μ (cm^2/Vs)	Carrier dens. $(10^{16}cm^{-3})$
O_E1	RT	40	19.8	-0.75	3390	-1.9
O_E1	4K	40	19.8	-0.80	1700 ± 510	-2.0
P2_M2	RT	40	24.6	-0.20	1360 ± 350	-0.5
L_J1*	RT	20	29.6	-0.25	1970 ± 180	-3.7
R2_E2	RT	20	7.4	-0.25	1450	-2.3

Table 4.3: Final results of the electron mobility in nanowires with a negative pinch-off. The columns are, in order: Name of the sample, measurement temperature, nanowire radius, capacitance of the gate-wire system, threshold voltage of the gate-sweep curve, computed electron mobility, computed carrier density. For the lack of errors in the first and last sample electron mobility measurement see text.

resistance term and/or by optimization of the contact transparency.

The computed carrier density is in the order of magnitude of 10^{16} cm^{-3} that is quite smaller than [25] (paper already mention for electron mobility values in section 2.1.2). This low level of unintentional doping attests the high quality of the material produced in our CBE chamber.

4.3 Photoconductance measurements

In section 2.2.2 photoconductive spectroscopy was presented as a measurement tool to investigate the electronic structure of a semiconductor material. The aim of the photoconductivity measurements performed in this work is to study the energetic levels as function of the nanowire size. Reducing the nanowire diameter the quantization effect should increase the energy gap and the energy level distance. This energy shift should be particularly marked in InAs nanowires with respect to other materials because of the small InAs electron effective mass. A very innovative result would be to measure a photoconductance quantization effect due to the energy splitting of the conduction energy levels. The electron energy level problem in the nanowire can be simplified to an infinite potential well in 2 dimensions.

Normally in semiconductor materials the photocurrent starts if the photon energy is greater than the energy gap, which for wurtzite InAs nanowire is expected to be $\simeq 400$ meV (see section 2.2.2). Because of the quantization effects it would be reasonable to measure a higher photocurrent onset. In section 1.2 the general case of a confining potential, $V(\mathbf{r})$, was discussed. Making the assumption that the nanowire is an infinite quantum well (QW) in two directions, the energy levels could be analytically computed. The electrons are free to travel along the nanowire axis direction (direction z), but are confined along the other two directions. The two quantum numbers for the confined directions are n_1 and n_2 so that the energy levels in the quantum well are given by:

$$\Delta E_c(n_1, n_2, d) = \frac{1}{2}\frac{(hc)^2}{m_c^* c^2}\frac{1}{d^2}(n_1^2 + n_2^2) \tag{4.3}$$

where h is the Planck constant, c is light velocity, m_c^* is the electron effective mass and d is the nanowire diameter. The same approximation can be made for holes in the valence band so that energy levels are:

$$\Delta E_v(n_1, n_2, d) = \frac{1}{2}\frac{(hc)^2}{m_v^* c^2}\frac{1}{d^2}(n_1^2 + n_2^2) \tag{4.4}$$

where m_v^* is the hole effective mass. Since $m_v^* > m_c^*$ the conduction level confinement energy is higher than the valence one.

The confinement energy has been studied as function of the well width

(nanowire diameter). The energy gap of a wurtzite nanowire can be approximately estimated as:

$$E_{Nanowire\,gap}(d) = E_{Bulk\,wurtzite} + \Delta E_v(1,1,d) + \Delta E_c(1,1,d) \tag{4.5}$$

Assigning the InAs bulk effective masses [42]:

$$m_c^* = 0.023\, m_e$$

$$m_v^* = 0.46\, m_e$$

where m_e is the electron mass, the data shown in Fig. 4.15 with the lower (black) curve are computed. The upper (red) curve is computed with the same Eq. 4.5, but with $\Delta E_c(1,2,d)$, or the equivalent $\Delta E_c(2,1,d)$, and represents the energy difference from the valence level to the second conduction level. Photons with an energy bigger than this difference can excite electrons in the second conduction level and increase the nanowire conductance. When the photon energy reaches this value a further increase of the photocurrent should be measured. Even though the model is very crude one can see that for the used nanowire diameters (20 and 40 nm) quantization effects should be clearly observable.

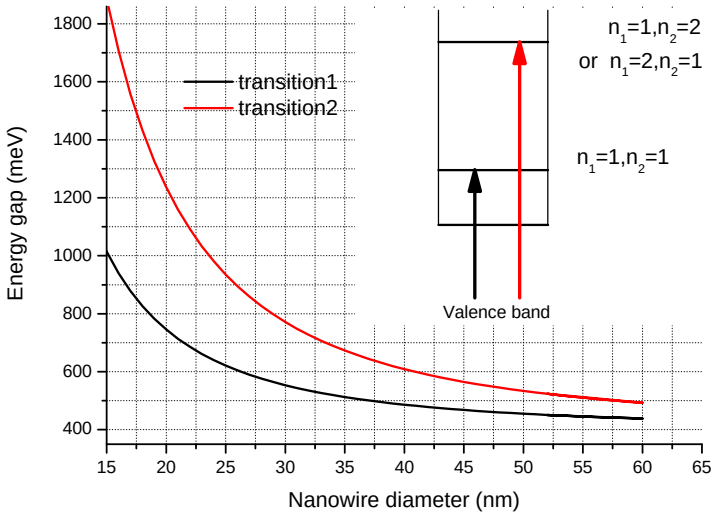


Figure 4.15: Schematic model of the energy gap vs. the nanowire diameter. In the top right corner the conduction energy levels are sketched. Two possible optical transitions are shown by the black and the red arrows. The black curve indicates the value of the energy gap for the optical transition from the valence level to the first excited state ($n_1 = 1, n_2 = 1$). The red line indicates the value of the energy gap for the optical transition from the valence level to the second excited state ($n_1 = 1, n_2 = 2$ or $n_1 = 2, n_2 = 1$).

4.3.1 GaAs substrate

GaAs has a room temperature band-gap of about 1.4 eV that increases by cooling down [42]. This should permit to easily observe the InAs nanowire absorption with a photocurrent measurement using GaAs substrate. The photocurrent onset should start above 400 meV but, even accounting for the quantization effects, the InAs nanowire gap transition should be much smaller than the GaAs energy gap.

In order to collect only the InAs nanowire signal the filter described in 3.5.2 was used. This filter cuts frequencies above 1000 meV, avoiding the GaAs photocurrent contribution.

From the rough computation discussed in the last section (see Fig. 4.15) for 40 nm diameter InAs nanowires we expect a photoconductivity onset at a light frequency of about 500 meV. Then, as discussed in the last section, a photoconductivity increase should be measured at an energy about 100 meV higher, when the photon energy is enough to populate the second nanowire energy subband.

In Fig. 4.16 four spectra of sample I (40 nm diameter, see table 3.2) at 77 K are shown. At V_g = 0 V the photocurrent peak slightly increases by increasing the source-drain voltage. A much consistent increase of the peak is due to the decrease of V_g. For V_g = -2 V the photocurrent signal is more than the double. Several spectra were collected in fast scan mode an step scan mode (see section 3.5.2) with similar results to spectra shown in Fig. 4.16. A strong dependence on the gate voltage is observed while the source-drain voltage does not affect the spectral shape. Furthermore the photocurrent onset is more than 100 meV higher than the expected one.

To verify the correct operation of our set-up, step scan measurements of the nanowire without filter were performed. It was successfully verified that at RT the GaAs energy gap is at about 1.4 eV, as shown in Fig. 4.17 where the black line of the photocurrent has a steep increase. The same measurement was repeated at 77 K (see Fig. 4.17) showing that the energy gap is not visible because at this temperature it is expected at about 1.5 eV [42]. Those measurements confirm the correct operation of the experimental set-up but, on the other hand, gave us interpretative problems about the photocurrent onset and the presence of low energies structures.

Photoconductive measurements were then performed on 20 diameter nanowires on GaAs substrate with the aim to find some difference from the

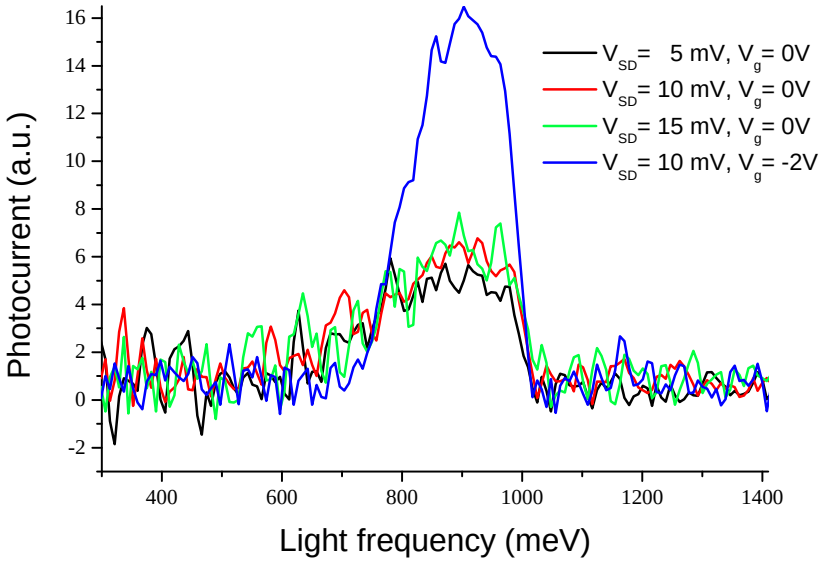


Figure 4.16: Fast scans of sample I at 77 K with a preamplifier sensitivity of 10^{-6}. The signal changes significantly decreasing the gate voltage.

above exposed results. The QW model (section 4.3) predicts for 20 nm diameter nanowires a photocurrent onset at about 700 meV.

Fast scan measurements were performed at RT on the sample Q2_E3 with the filter. A good photocurrent signal was measured at zero source drain voltage; this aspect will be discussed later. As for the previous case of the 40 nm diameter nanowires (sample I) the photocurrent onset is at about 700 meV, but now in agreement with the theoretical prediction. Again a strong gate voltage dependence was observed, both for negative gate voltages, see Fig. 4.18 (a), and for positive gate voltages, see Fig. 4.18 (b). For negative gate voltages the spectra shape changes and the photocurrent peak decreases by decreasing the gate voltage. For positive voltages the shape remains similar and by increasing the gate voltage the peak increases. As in the case of 40 nm diameter nanowires the source drain voltage does not change the photocurrent intensity and seems only to affect the signal to noise ratio (see the purple curve in Fig. 4.18 (b)).

The strong gate voltage dependence and the constant value of the onset photocurrent indicate that there is another contribution to the photocurrent. To measure the substrate contribution a sample with a GaAs substrate (Q2_D1) was fabricated without nanowires. The lateral-gate configuration

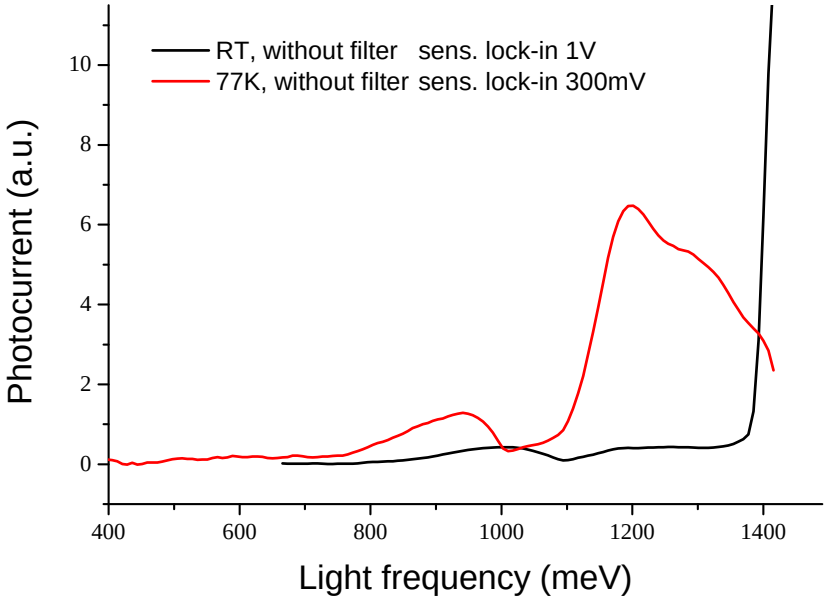


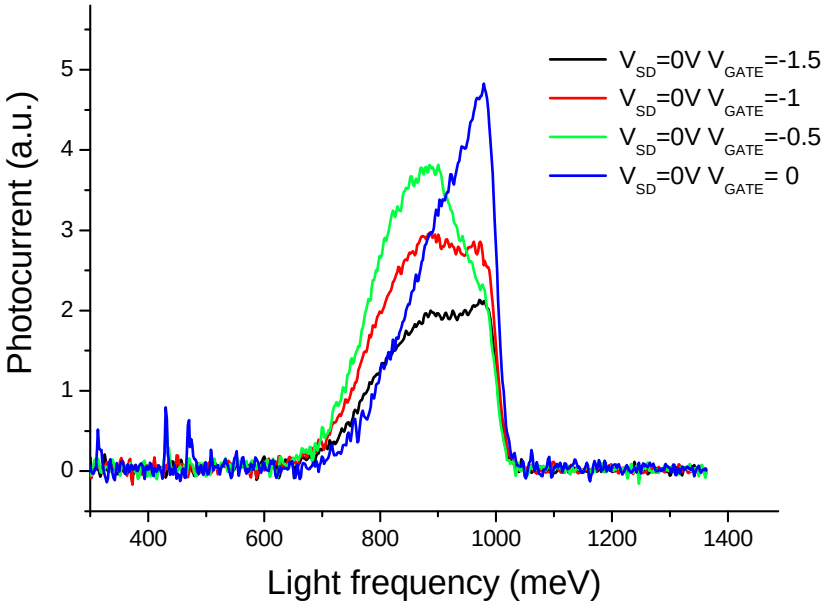
Figure 4.17: Step scans of sample I at 77 K with a preamplifier sensitivity of 10^{-7}. The photocurrent at RT (black line) increases at 1.4 eV in correspondence of the GaAs energy gap. The photocurrent at 77 K is indicated by the red line (note the different sensitivity in the lock-in).

was adopted respecting the typical contact size and distances. A so called *empty* contact is shown in Fig. 3.11 (b). It is important to underline that even without nanowire the passivation was performed to make sure that the only difference is due the nanowire presence. The IV of the *empty* contact was measured giving an ohmic behaviour with a resistance of about 100 $M\Omega$, that is three orders of magnitude larger than the typical resistance of a nanowire. With the light the IV is still linear but the computed resistance is 5 $M\Omega$ that is only one order of magnitude larger than a typical nanowire resistance. Furthermore an off-set in the current was measured, probably due to a contact asymmetry (see Fig. 4.19).

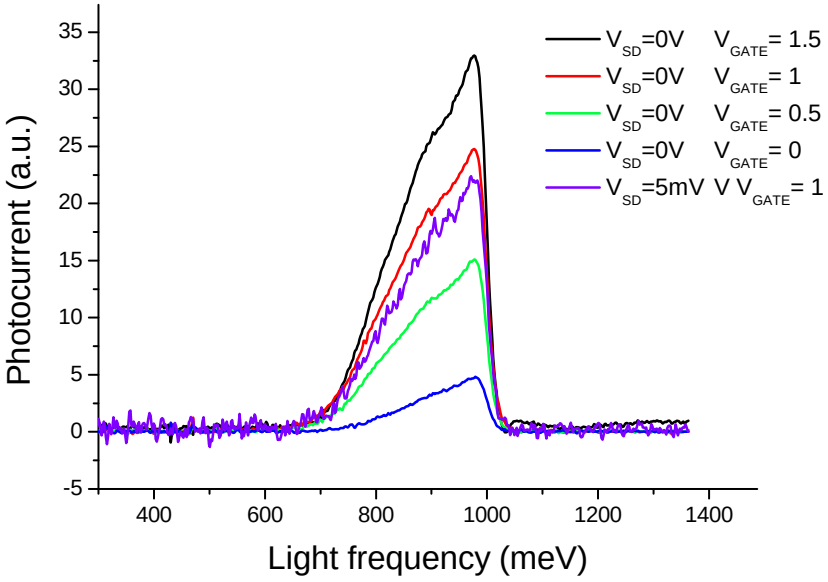
The light changes the substrate conductance more than it was expected. In Fig 4.20 step scan spectra are shown for different values of gate (a) and of source-drain (b) voltages. Those spectra were collected with the filter for GaAs and exhibit results very similar to the ones exposed above for 20 and 40 nm nanowires. In both cases (a) and (b) the photocurrent peak increases by increasing the voltage on the contacts: source, drain or gate. Furthermore

the photocurrent onset is still at about 700 meV.

The photocurrent signal measured is clearly not due to the nanowire but to the substrate. Apparently, at nanometric distances, surface states of the GaAs bulk are available in the energy gap. Surface photoconduction of GaAs layers was already studied as function of different surface treatments: etching, passivation, ion bombardment and Au^{3+} doping [46]. In the cited paper the photoactive surface electron states in GaAs are studied by infrared spectroscopy and depending on the surface treatment the photocurrent onset ranges from about 0.5 eV to 1.1 eV. Our hypothesis is that the fabrication, in particular the passivation, can modify the GaAs surface and create surface states able to give rise to photoconductivity for energies in the forbidden gap.



(a)



(b)

Figure 4.18: Fast scans of sample Q2_E3 at RT with a preamplifier sensitivity of 10^{-7}. (a) Negative gate voltages. (b) Positive gate voltages.

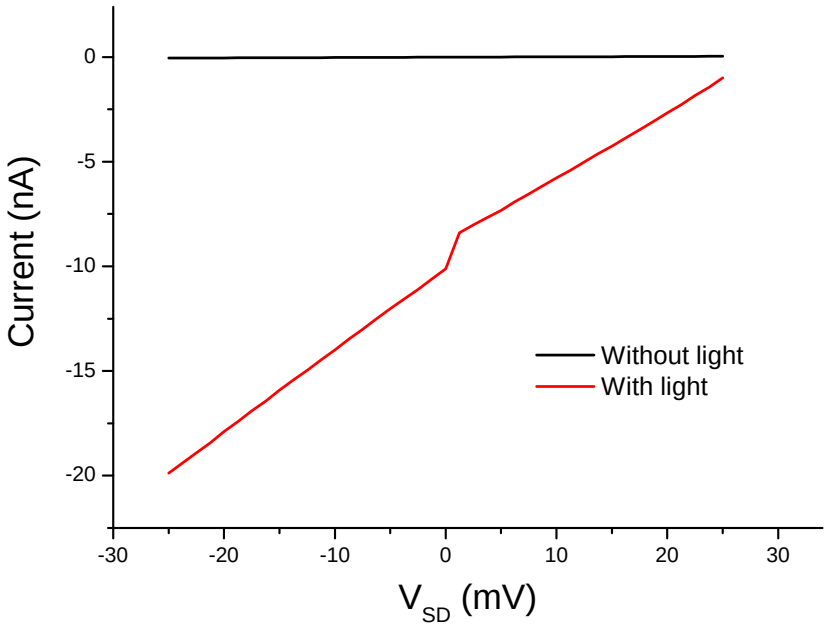
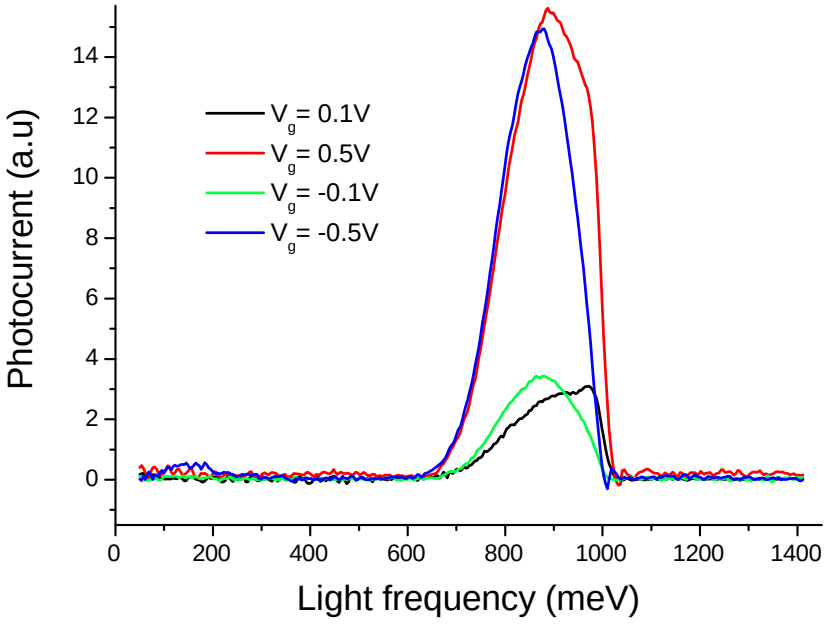
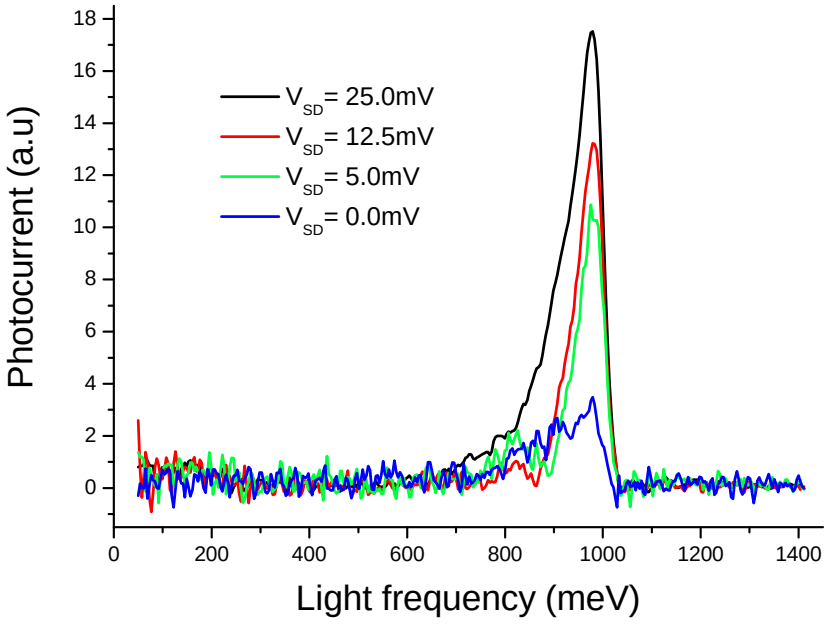


Figure 4.19: IV measurement at RT of the *empty* contact without light (black line) and with light (red line).



(a)



(b)

Figure 4.20: Step scans at RT of sample Q2_D1, *empty* contact, with a preamplifier sensitivity of 10^{-8}: (a) V_{SD} is held at zero voltage, while spectra for different V_g are collected with a lock-in sensibility of 100 mV. (b) V_g is held at zero voltage while spectra for different V_{SD} are collected with a lock-in sensibility of 10 mV.

4.3.2 SiO_2 substrate

In order to eliminate the GaAs surface photoconduction and measure only the nanowire contribution, a SiO_2 substrate was chosen. The first attempt was a 250 nm thick SiO_2 substrate on the top of doped Si. As already explained in section 3.3, this substrate allows to realize a back-gate configuration. This configuration is effective for transport measurements because the gate potential is uniform on the wire. Nevertheless no signal under 1000 meV was detected, even with the chopper and the lock-in (sample L_J1).

We suppose that the back-gate geometry could be not suitable for optical measurements. As a matter of fact the back-gate is conductive so that the electric field of the incident light is forced to have a zero value on the conductive gate surface, precisely at 250 nm from the wire. Since the wavelength at which the nanowire should be sensitive is about $2\mu m$ the light electric field on the wire could be too low.

With the above considerations another attempt was done on a different SiO_2 substrate. The thickness of the oxide layer is 500 nm and the bulk is of intrinsic and insulanting Si. A lateral gate geometry was realized (sample R2_E2).

In this case a signal on the lock-in was detected for frequencies under 1000 meV (with filter). Nevertheless the signal was not stable enough to collect spectra, either at room temperature or at low temperature.

On the other hand without filter, considering frequencies above 1000 meV, a consistent and stable signal was detected. Step scan spectra are shown in Fig. 4.21. In this conditions the spectra do not depend on the gate voltage and have a photocurrent onset close to 1.1 eV. This value corresponds roughly to the Si energy gap, that at RT is 1.12 eV [42]. It is evident that, although many efforts were made to eliminate the substrate contribution, also in the case of intrinsic and insulating silicon an undesired photocurrent is generated. This can be explained through capacitive or inductive coupling of the substrate with the nanowire contacts.

Since the filtered signal was weak and very unstable, we tried to study the sample photoconductivity response to a more intense light. The ultrafast laser was used as light source and measurements of the photocurrent as function of the laser power were performed. The wavelength was held at 2 μm and the laser power was set each time with the help of a power meter. The signal was collected with the current preamplifier and the lock-in, imposing

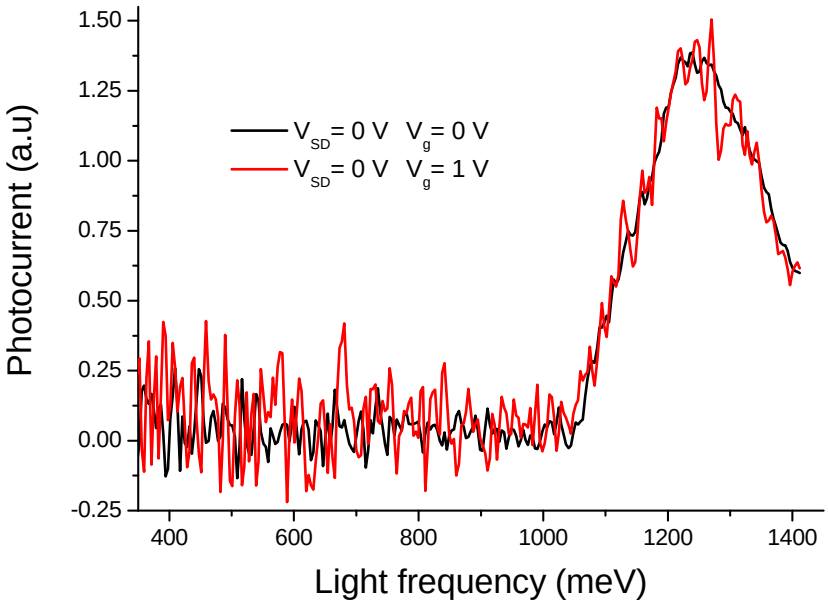


Figure 4.21: Step scan spectra of sample R2_E2 at RT without filter. The preamplifier sensitivity is 10^8 and the lock-in sensitivity 10 mV. The black line is a spectrum at zero gate voltage while the red line is a spectrum with a gate voltage of 1 V.

a source-drain bias of 5 mV.

The results of the lock-in signal vs. the laser power are shown in Fig. 4.22. For a laser power up to 6 mW the lock-in signal increases by increasing the laser power, but afterwards the trend changes. To understand the nature of the signal the data were fitted, in the range from 1 to 6 mW, both with a line and a with a parabola. A linear trend would likely confirm the nanowire response. On the other hand a parabolic trend would indicate a two photon absorption in the substrate. As a matter of fact the 2 μm wavelength corresponds to an energy of 600 meV that is much less than the gap, but in the case of a two photon absorption is sufficient to excite electrons in the Si conduction band (Si energy gap: 1.12 meV). Unfortunately the difference in quality between linear and parabolic fit is not sufficient to unambiguosly discriminate between the two.

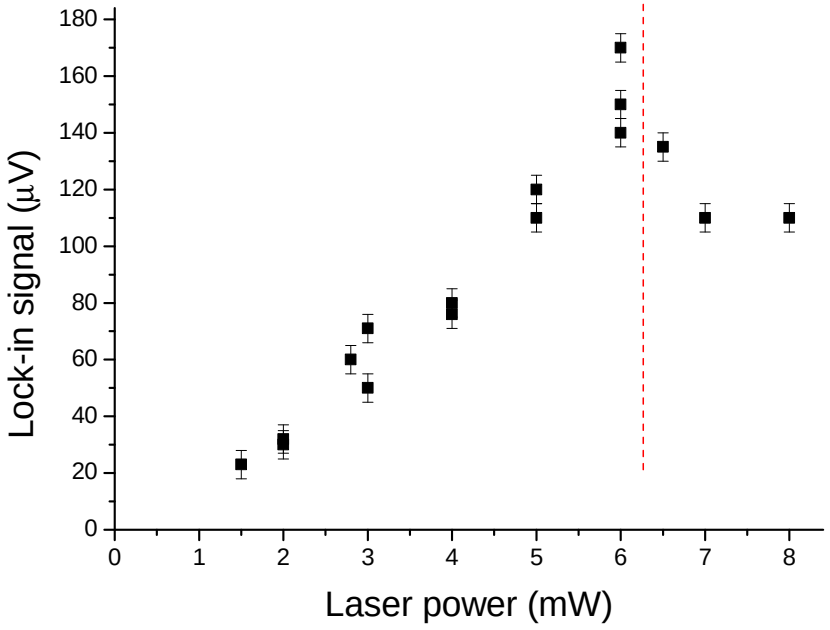


Figure 4.22: Lock-in signal vs. power of the ultra-fast laser. This measurements were performed at RT with a laser wavelength of 2 μm. The signal increases until 6 mW (red dashed line).

Appendix A

Fabrication recipes

A.1 Microscopic connection strips

Recipe for the fabrication of the microscopic connection strips with optical lithography. This is a bi-layer recipe that allows to obtain a good undercut and to avoid rippled borders. Ripple borders would create problems for the subsequently nanoscopic nanowire contacts on the nanowire.

- Surface cleaning:
  - 30” Acetone
  - 15” Isopropanol
  - 5’ Prebake @ 150 °C
- Spin resist LOR 3A:
  - 3” @ 500 rpm
  - 35” @ 3000 rpm
- 5’ Bake @ 170 °C
- Spin resist S1818:
  - 3” @ 500 rpm
  - 60” @ 6000 rpm
- 60” Bake @ 115 °C

- 10” Exposure to ultraviolet light (UV)
- 30” Develop in MF319, stop in H_2O
- 5’ Bake @ 120 °C
- 60” Under-etch in MF319, stop in H_2O
- Metal evaporation:
  - 5 nm Cr
  - 40 nm Au
- Lift-off:
  - Acetone (with the help of a syringe) until necessary
  - 15” Isopropanol
- 30” LOR 3A removal in MF319

A.2 Pad contacts

This recipe was used to realize pads with lateral dimension of 100 μm x 200 μm.

- 60" Spin resist S1818 @ 6000 rpm
- 60" Bake @ 90 °C
- 20" Develop in MF319, stop in H_2O
- 20" Exposure to ultraviolet light
- 20" Hard bake @ 120 °C
- 30" Develop in MF319, stop in H_2O
- Metal evaporation:
  - 10 nm Cr
  - 100 nm Au
- Lift-off:
  - Acetone (with the help of a syringe) until necessary
  - 15" Isopropanol

A.3 Nanowire contacts

Recipe to fabricate contacts with electron beam lithography (EBL) in order to make contacts on the single nanowire.

- 60" Spin resist PMMA 639.04 @ 4000 rpm
- 15' Bake @ 120 °C
- Exposure with EBL
- 2' Develop in AR 600/56, stop in Isopropanol
- Metal evaporation:
  - 5 nm Ni
  - 40 nm Au
- Lift-off:
  - Acetone (with the help of a syringe) until necessary
  - 15" Isopropanol

Conclusions

Differently from the past, technological improvements may not be sufficient to sustain the realization of smaller and smaller electronic devices. Fundamentals limits are being approached and must be taken into account. Semiconductor devices reached nanometric sizes and are inching to the final barrier of the single atom. The electron wavelength becomes comparable with the nanometric structure size. Moreover the nanometer range is the resolution limit for available top-down fabrication techniques, such as electronic beam lithography (EBL). Self assembled nanowires are actually investigated as potential candidates for further developments in electronics downscaling.

My thesis work focused on the study of transport and optical properties of InAs nanowires. Since quantization effects are expected at small size, the smallest nanowires available (diameter of 20 and 40 nm) were used.

I first developed device fabrication techniques based on EBL. I realized single nanowire transistors on different substrates and with different contact geometries.

I then performed transport measurements at room temperature and low temperatures (at 77 K and down to 4K) verifying the correct device operation. Data were successively analysed and a comparison with the transistor performances in the literature was made. In order to compute electron mobility and carrier density values, I simulated the nanowire transistor configuration with a finite element computer program. The 3D model allows to compute the capacitance of the gate-nanowire system with a great versatility in terms of geometrical configuration. This was employed to simulate a lateral-gate configuration and to improve the commonly used estimation of the capacitance in a back-gate configuration.

The obtained electron mobilities resulted comparable to the literature values for larger nanowire diameters. This is a not trivial result taking into

account the really small nanowire diameter (20 nm). These mobility results associated with a low carrier density proved the high quality of the nanowires grown in the NEST laboratory.

Photoconductivity measurements were also performed in order to study the subband structure of the 20 nm diameter nanowires. Different substrates were used but no clear nanowire signal was measured. Nevertheless these attempts have clarified the need to accurately verify substrate contribution and help a future study of the photoconductive response of homogeneous InAs nanowires, that, at the moment, is still missing.

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