Experimental Validation of a Novel Inertia-less VSM Algorithm

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***Abstract*—For years, grid phenomena such as voltage stability, loss of inertia, voltage dips, etc. have been managed by well established solutions. Such solutions include on load tap changing transformers, and synchronous generators. Now, the increased penetration of load and generation interfaced by converter based systems has demanded changes in the way the grid is managed. If the aforementioned issues are not considered, local instability can lead to system-wide instability. One possible solution for the majority of these issues is to change the control logic of the converter, modifying it from the standard vectorial output current theory (DQCl control) to one where the traditional synchronous generator is emulated. These solutions are based within the so called Virtual Synchronous Machine or VSM algorithms. Among them, the so-called Virtual Synchronous Machine Zero Inertia (VSM0H) has been implemented in this paper. Due to its simplicity and efficacy, it has been chosen for experimental testing and analysis. The process to implement the VSM0H algorithm in the lab will be explained; with particular emphasis in the connection process since, with the VSM0H algorithm, the converter becomes a true voltage source, and this procedure can be particularly challenging. An explanation of the blocks added to provide this soft connection will be explained. Additionally, another experiment showing the behavior of the system against changes in the power references will be shown.**

I. Introduction

With the inclusion of renewable generation into the electrical grid, traditional fossil-fueled plants based on synchronous generators have been gradually replaced by converter-based systems. The vast majority of converters installed are commonly controlled using vectorial current control ([1] [2]). From the grid point of view, they are current sources that inject power to the grid but lack, by default, voltage regulation. Absence of this voltage regulation detrimentally effects the voltage quality at the load and, if the proportion of DQCl converter penetration is high enough, can cause the whole grid to become impractical. This voltage quality degradation that appears in big electrical ([3]-[5]) grids is also an issue for converter dominated microgrids, where phenomena that cause instability are even more problematic. In any case, whether the grid is large or small, as the vast majority of the converters already installed are based on the standard DQCl theory, a possible solution is the creation of voltage references nodes (or grid building nodes). These nodes can provide voltage that is stiff enough to allow the remaining neighbor converters to continue the injection of power. This stiff voltage can be assured if the inverters provide smooth positive sequence voltage to the grid, regardless of the events on the grid, i.e. the converters behave as voltage sources. This is the behavior of a synchronous generator, where the machine is typically represented as an ideal voltage source behind an inductance.

Therefore, a straightforward approach is to partially [6], [8] or entirely [7], mimic the behavior of a synchronous machine, and transforming the converter into a true voltage source. In this paper a new algorithm [9] is implemented in a control scheme for a real converter and tested in a microgrid for experimental validation. The main advantage of the VSM0H algorithm is the simple but effective operation in terms of performance against challenging scenarios.

II. Presentation of the system

A. Modification of the algorithm for the experimental implementation

Although the control logic is completely explained in [9], some modifications were made in order to fully implement the system. These modifications are in the last block presented in Fig. 1 shown as *Driving the Voltage Reference* and further described in the block diagram presented in Fig.2. The main function of this block is to transform the magnitude and frequency requested by the control logic into modulating signals and finally pulses for the IGBT's.

There are two modifications required in order for the algorithm to work with the hardware: First, a correction of the instantaneous angle. An instantaneous angle can be acquired by using the frequency, by integrating over one cycle. However, this method does not take into account the offset error between the instantaneous grid angle and the angle approximated by the control logic. In principle, this offset error does not affect to the operation of the converter too much, as the power synchronization calculations remove this offset over time. Nonetheless, it can heavily impact the initial converter connection precess, thus compromising the condition of the IGBTs due to over currents. The second modification is the removal of the DC currents passing through the converter side of the transformer. If the converter is connected to the grid using a transformer (as it is used on this paper) usually it is done using a delta-wye transformer where the converter is connected on the delta side. As the algorithm implements a voltage source,

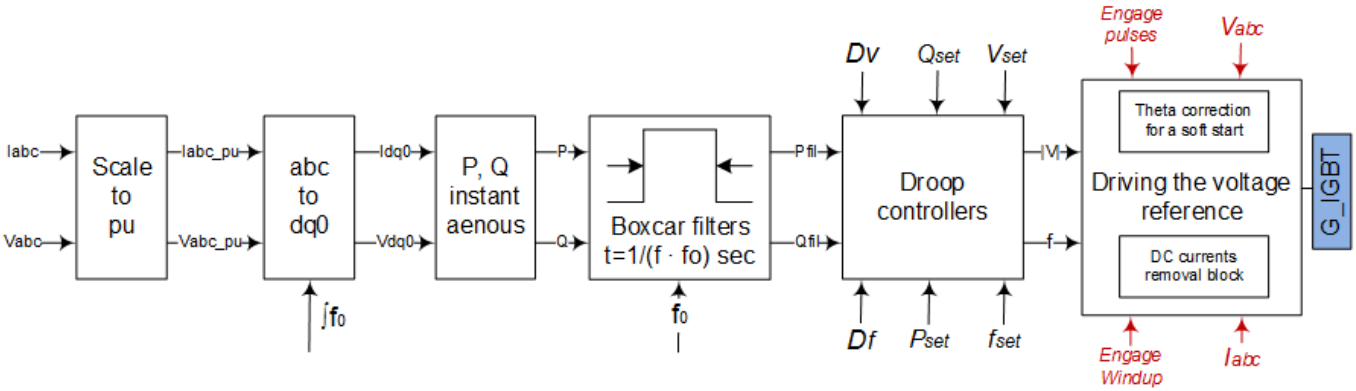

Fig. 1. Schematic diagram of the converter

unnecessary circular DC currents can appear on the converter side due to natural asymmetries of the AC side elements. On the other hand if the inverter is connected transformerless to the grid in wye connection, DC currents will appear as well, but this time going through the neutral line. Depending on the hardware configuration and grid stiffness, these DC currents can provoke several effects; current unbalance resulting in a voltage imbalance or transformer saturation to cite some of them. In the traditional DQCl algorithm, these phenomena do not happen for two reasons. First, the variable of control is the current and, consequently, the current is under complete control during the operation of the system. Second, in DQCl control, there are PI regulators to achieve the output current references; these controllers are tunned to have high values of gain in zero frequency (or DC), and this makes them very responsive against signals on that part of the spectrum. Both modifications will be explained in further detail as following.

1) Correction of the instantaneous angle for a soft-start: This block was used to create an initial voltage that identically represents the measured V_{abc} from the grid. First of all, the converter is enabled with the *Engage Converter Contactor*. This pre-charges the output filter and the DC bus using the anti-windup resistors. Then, the DC breaker and IGBT are enabled to allow the full charge of the DC bus to the nominal values. The pulses are then enabled and, the anti-windup contactor is nearly instantaneously engaged for the bypassing of the antiwindup resistors. From the start of this connection process, the soft-start block has been operating in parallel to remove the phase difference between the angle obtained by the logic and real one and, by the time last contactor has been enabled (which is the most critical one), the antiwindup one, difference of angle is almost zero. This results in an identical voltage between the one generated by the converter and the real one measured in V_{abc}. Consequently, the instantaneous current flowing through the filter and the IGBT's is zero. Finally, the control logic can begin to operate in order to provide active and reactive power once the connection process is complemented.

The block diagram for this process is detailed in Fig. 3. First of all, using the measured voltage, the instantaneous angle is obtained using the well-known arctangential Phase Locked Loop. It converts the voltage V_{abc} into $V_{\alpha\beta}$ using the Clarke transform. Then, the instantaneous angle can be obtained measuring the *arctan* of both components. It is a very fast, light and straightforward configuration but it is very sensitive to noise. However, since it is only used during the connection process, it works very efficiently. Once the instantaneous angle is measured, a phase difference, measured in samples, is calculated between the real angle coming from the grid and the one calculated by the control logic ($\int f_o$). Whilst the flag used to drive the contactor *Engage Windup* is deactivated, the Sample and Hold (*S/H*) is transparent for the control logic. Once the system activates this flag, the last value of delay obtained is maintained until another connection process is initiated. The last block only implements $\int f_o$ for the previous calculated delay, giving a corrected instantaneous

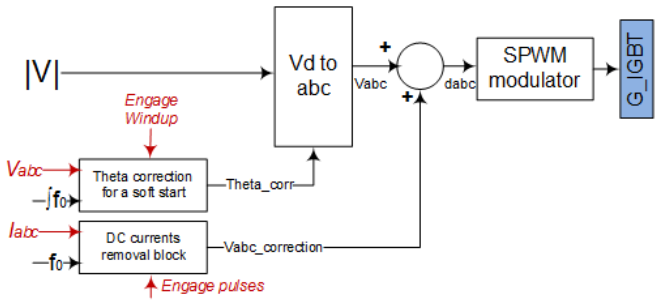

Fig. 2. Block diagram of the Driving voltage subsystem

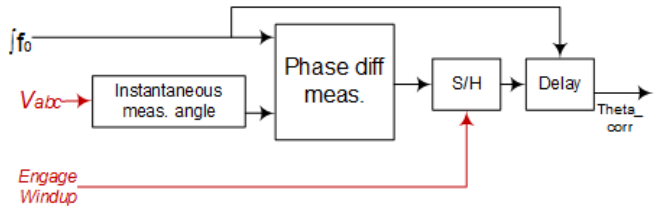

Fig. 3. Theta correction for a soft start

angle ready for the soft start.

2) DC currents removal block: As shown in Fig. 4 this block uses another boxcar filter to provide the measurement of every phase current average value. Exactly in the same manner as the filters included in the main logic of control, the estimated value of frequency f_0 is included as input parameter for this filter. This will provide the filter with the necessary adaptability to the grid frequency. Once the average value is obtained, a control loop is created for each phase currents. Since the value that wants to be achieved for this average value is zero, this will be the reference to follow. The error is then regulated with a Proportional Integral controller (*PI controller*) adjusts the commands in order to achieve the desired set-point value at the converter output. Finally, any zero sequence elements present, are removed.

The most difficult part of this stage is proper tuning of the PI regulator. Since the averaged value of the currents will take a minimum of one cycle to be obtained, this block will not be able to update their references faster than 50 Hz. Following Nyquist theorem, the minimum theoretical value of bandwidth, or crossover frequency (fc), for this control loop will be 25 Hz; this, of course, forces to the control loop to be very slow.

The regulator gains can be calculated by fixing a proper fc and phase margin (PM) for the DC currents removal loop. This calculation is very similar to the one described in [12]. Here, a bode plot is used for an equivalent plant formed by the filter and the converter in feedback configuration. This forces the system to behave with the specific dynamics set as input parameters of the calculation. The same algorithm can be applied here since the controlled plant is the same (approximately $1/Ls$ [13]). Specific values for this case can be found in the appendix.

III. Performance Analysis

The complete assessment and validation of this new algorithm would imply an almost unlimited number of experiments. Thus, just the most basic functionalities will be assessed.

A. Soft-start initialization routine

The results for this experiment are presented in Fig. 5 together with Fig. 6. Fig. 5 shows, from top to bottom, the voltages measured in the converter side V_{abc}, the currents injected to the grid I_{abc}, the references of active and reactive power with their respective outputs, P_{ref}/P_{conv} and Q_{ref}/Q_{conv}

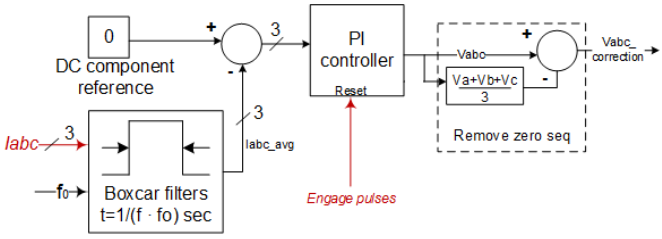

Fig. 4. DC currents removal block

and the operating frequency from the logic of control f_0. Then, a plot of the grid voltage against the modulating signal V_{abc}/d_{abc}, the compensation components which have to be added for the DC currents removal and finally, the delay adjustment, in samples, to provide a soft start. This plot has to be observed in conjunction with the one in Fig. 6, where the contactor and flag signals necessary for the initialization routine are plotted in synchronism with the ones in Fig. 5.

The experiment starts with the system completely disconnected. The connection procedure starts approximately at second 1 when the converter contactor is engaged. From now, until the next switch is connected, the system is pre-charging in order to avoid high inrush currents. At approximately 1.4 sec, the physical connection of the DC bus is engaged and, 300 ms later, the IGBT is connected too, allowing the DC bus charge to its nominal value. Until the pulses are engaged at approximately 2.52 sec. The DC currents removal block and the delay adjustment for a soft-start are working from the start and they are getting ready. Since the IGBT pulses are not active, the DC currents removal blocks gives wrong references until 2.52 sec, when the pulses are activated, and a reset signal is applied to the PI regulators of this block (see Fig. 4). The output becomes 0 and, as it can be observed in the zoomed view of plot V_{abc}/d_{abc}, the signal d_{abc} (dashed lines) almost matches in phase the one of V_{abc} (solid line). The small difference of phase is caused by the discretization error due to the limitation of the control action derived from the finite sampling frequency. At approximately 3 secs, the contactor to bypass the antiwindup resistor is engaged and the system is fully connected. This is the most sensitive step for the system since now, the system is fully connected. A period of transients during the first seconds can occur as it is observed in I_{abc}. This transient is provoked by the adaptation process of all the internal variables and control to this new status where the converter is more responsive to any command. Due to the unintentional absorb of power (as it can be seen P_{ref}), the control reacts dropping the frequency to lower values as synchronous machines do. The DC current removal block also begins to actuate giving small corrections to remove the DC currents created. Since it is a slow control, it will take some seconds until it gets fully removed. Lastly, as it can be observed from Fig. 3, when the contactor is engaged at 3 seconds, the last value from the delay adjustment block is hold and continues being the same until a new connection procedure begins.

B. Changing the power references

The experiment shown previously continues in time with the results shown in Fig. 5. At approximately 3.5 sec, a step in active power P_{ref} of 3 KW is applied to the reference and after some new transients the system satisfies the demand. To do so, it can be seen that the control logic increases the internal frequency of the system like synchronous machine do. This increase in frequency creates a phase displacement between the converter voltage and the grid one, giving as result a rise in the active power injected into the grid. Once

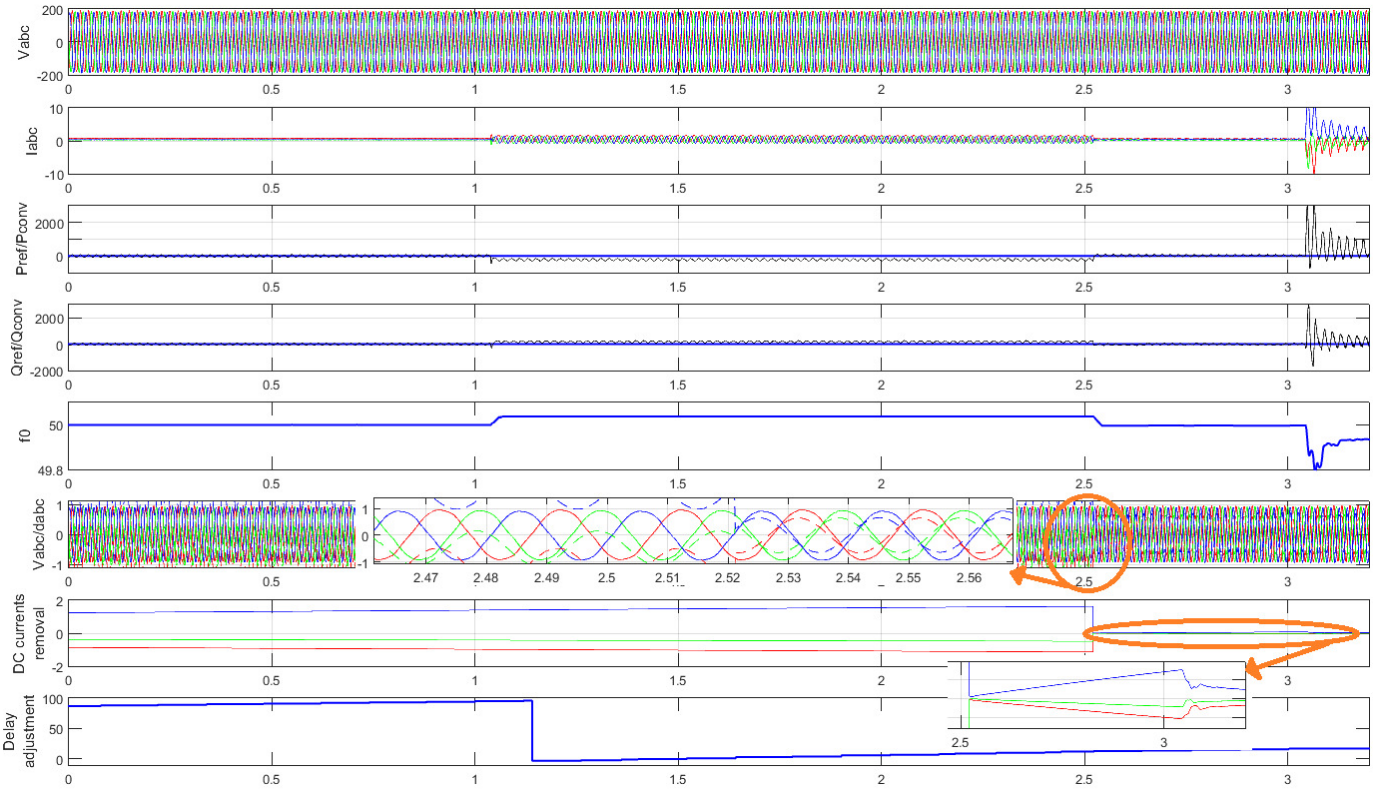

Fig. 5. Connection procedure

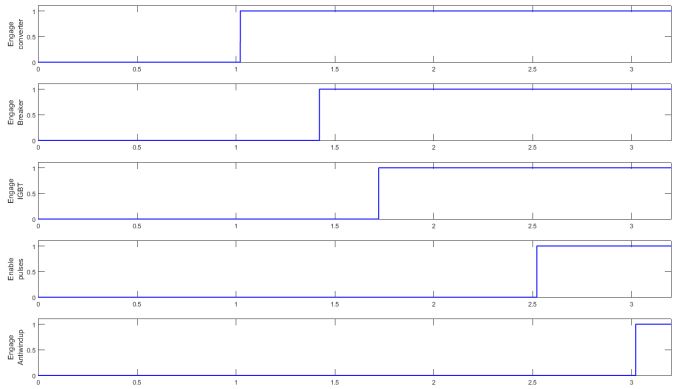

Fig. 6. Initialization routine for the start up process

the converter achieves the demanded, the frequency returns to its nominal value. Some ripples can be observed during the process; this can be customized through the droop constants that control the system. Its numerical values have to be customized depending on how the converter is connected to the grid, the line inductance that connects the converter to the grid, the desired system response and the stiffness of the grid itself. However, the values shown in Table IV can work in the majority of cases.

The DC currents removal block begins to enter into action to mitigate the new DC components created for every change of power. Also, the delay adjustment graph has been included here to show that the number of samples for the perfect coupling between the converter and the grid voltage is hold for the rest of the process.

At approximately 4 sec, a new step in reactive power of 5 KVAr is applied to the system. The control logic reacts increasing the converter voltage to satisfy the new command. However, this rise not only increases reactive power but also active as it can be seen so, in parallel, the frequency drops temporarily to suit the demand. At sec 5, the command of reactive power returns to 0 and at 5.5 the active power too. It is possible to see that the system reacts in the same manner with opposite signs.

IV. Conclusion

The control solution based on the VSM0H algorithm is one among many solutions to face new challenges within converter-based grid systems. Its simplicity and behavior as a real voltage source has a lot of potential as grid-reference (or grid-building) node that other DQCl systems or remaining synchronous generator could follow. However, the particular problematic of a real grid-connected converter that uses the VSM0H algorithm as control logic had never been faced before.

During this paper, modifications of this algorithm to make it practical have been remarked, addressed, solved and finally implemented. Thanks to these changes, the system has been

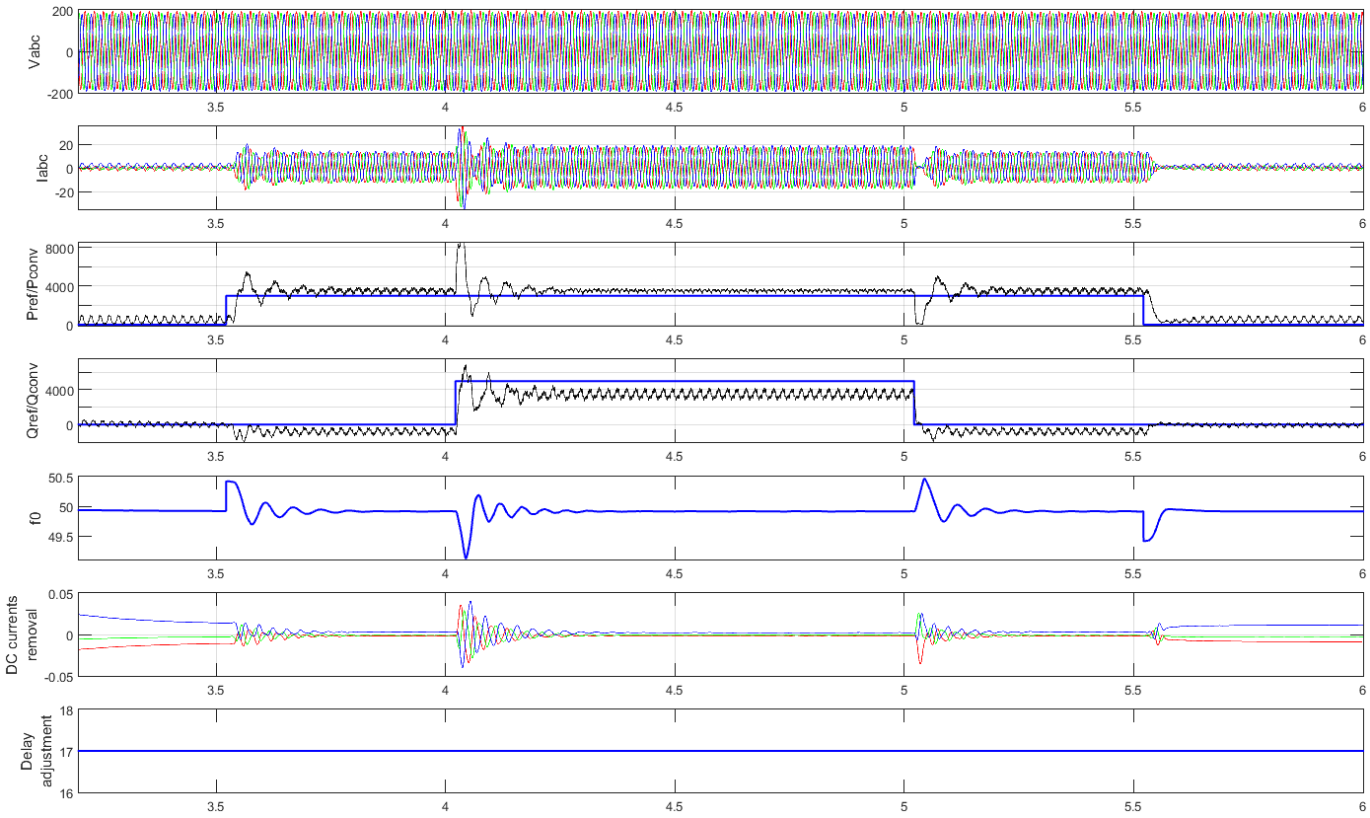

Fig. 7. Changes in the power references

capable to provide a soft-connection to the grid and it is able to satisfy changes in power commands.

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APPENDIX

Experimental System values		
Vcc	600V, 25A	DC power source
S	10KVA	Nominal power of the converter
Rc	10 KΩ	Input Resistance for DC bus discharging
Ci	2.2 μF	Input Capacitor
IGBT	25A, 1200V	Max Current, Max Vce voltage
Lf	3 mH	Output filter inductor
Cf	8.8 μF	Capacitor filter
Rf	22 Ω	LC Resonance frequency damping resistor
Rd	100 Ω	Antiwindup resistor
Output TRF	230/400 Vrms l-l 10KVA	Delta-Star connected
fs	5 KHz	Sampling and logic updating frequency
PI regulator	$7.28 + 4929/s$	Values calculated for the PI regulator, Phase Margin of 75 Hz and crossover frequency of 15 Hz
D_f	5%	Droop constant for the Active power-frequency droop control
D_V	7.5%	Droop constant for the Reactive power-Voltage droop control