High performance organic transistor memory elements with steep flanks of hysteresis**

By Weiping Wu, Yunqi Liu*, Hongliang Zhang, Ying Wang, Shanghui Ye, Yunlong Guo, Chongan Di, Gui Yu, and Daoben Zhu

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[*] Prof. Dr. Y. Q. Liu, W. P. Wu, H. L. Zhang, Y. Wang, S. H. Ye, Y. L. Guo, C. A. Di, Prof. Dr. G. Yu, Prof. D. B. Zhu

Beijing National Laboratory for Molecular Sciences, Key Laboratory of Organic Solids, Institute of Chemistry, Chinese Academy of Sciences, Beijing 100080 (P. R. China)

E-mail: liuyq@mail.iccas.ac.cn

W. P. Wu, H. L. Zhang, Y. Wang, S. H. Ye, Y. L. Guo, C. A. Di

Graduate University of Chinese Academy of Sciences, Beijing 100039, China

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Abstract: High performance organic transistor memory elements with donor–polymer blends buffer layers were presented. These organic memory transistors have steep flanks of hysteresis with ON/OFF memory ratio up to 2×10^4, and retention times in excess of 24 hours. Inexpensive materials such as poly(methyl methacrylate), ferrocene and copper phthalocyanine are used for the device fabrications, providing a convenient approach of producing organic memory transistors at low cost and high efficiency.

Key words: organic field-effect transistors, memory elements, polymer donor blends, steep flanks of the hysteresis

1. Introduction

Organic field-effect transistor (OFET) memory elements have received substantial research and development attention during the last decade for their great potential for memory applications such as part of the radio-frequency identification devices, smart cards and disposable circuitry.[1–4] Organic memory tags (transponders) are the backbone of the radio frequency identification (RFID) system since they contain data that allow the items to be identified. An organic memory tag is made of a non-volatile memory associated with a radio frequency communication block, performing RF signal modulation, demodulation, and power supply regulation, and an antenna. Equally cheap and versatile electrically addressable organic memories would be desirable for the sake of low cost and flexible products.[5,6] In an FET-type memory device, it is required to fix the accumulated charges at the channel region even after switching off a voltage. Generally, inorganic lead titanate zirconate[7,8] and organic ferroelectric (or ferroelectric-like, such as polyvinylidene fluoride,[9,10] nylon[11] or one of their copolymers, e.g. poly(vinylidenefluoride trifluoroethylene)[12,13] gate dielectric materials were used as insulators in the FET-type memory device. Hysteresis in the operation of OFETs has also been observed on the cycling of OFETs with nonferroelectric polymer gate dielectric, but this is typically less than 20% of the whole sweeping voltage range. Ferroelectric organic field-effect transistors (FerrOFET) are written by applying a gate voltage to the device, usually a pulse long enough to polarize the ferroelectric. When the ferroelectric layer has been polarized, a channel is induced or depleted in the semiconducting layer. In inorganic gate OFETs, one mechanism for

the hysteresis is charge trapping and detrapping at the interface between the insulator and the semiconductor.

The low operational voltage is essential for practical applications. In order to achieve this, the memory device should have reliable write/read/erase operations with steep flanks of the hysteresis and high ON/OFF current ratio, which are highly advantageous for applications in non-volatile memory. The flanks of the hysteresis should be as steep as possible, as it determines the operation speed and switching performance of the memory devices. A large ON/OFF current ratio of the device allows the circuit to clearly distinguish between the "0" and "1" states. The importance of steep flanks of the hysteresis with low operation voltage has not been fully realized in previous memory device researches. Moreover, the memory retention and good switching performance of organic memory transistor devices are also big challenges that transistor memories have yet to overcome.

Organic ferroelectric polymers usually are not soluble very well in common solvents and they have relative low surface energy thus an addition layer of polymers, polystyrene (PS) or poly(methyl methacrylate) (PMMA) were required to form highly ordered films for high performance transistors.[10] But the added layer usually strongly weakens the memory effect of FerrOFET devices. Furthermore, both inorganic and most organic ferroelectric gate dielectrics require annealing steps to fully develop their crystallinity and ferroelectric states,[9–13] which will be undesirable for flexible substrates and other temperature sensitive components. The general annealing temperature for the ferroelectric gate dielectrics was reported as high as 600~900 ºC for

inorganic ferroelectric materials[8] and above 130~150 °C for ferroelectric polymers[9]. The high temperature process induced damages of components of OFETs and degradations of transistor performance. Recently, it has been found that it is also possible for simple electrets to function as the memory dielectric.[3,14] Some other dielectric materials which is amorphous rather than crystalline (such as nylons) may display memory effect. One example is poly-(m-xylylenediamine-alt-adipic acid) (MXD6), which has been shown to exhibit a ferroelectric-like polarization hysteresis in its amorphous state, probably due to hydrogen bond alignment.[15]

Here we report high performance organic transistor memory elements with steep flanks of the hysteresis by using donor-polymer blend buffer layers. Our memory device is a single transistor memory that is built on SiO_2 gate insulator with a donor-polymer blend as bluffer layer (Fig. 1b). Organic molecules, including tetrathiafulvalene (TTF), ferrocene (Fc) and 5,10,15,20-tetraphenyl-21H,23H-porphine nickel(II) (NiTPP) were chosen as donors, copper phthalocyanine (CuPc) was used as the active layer of OFETs (Fig. 1a). Several polymers including polyethylene oxide (PEO), polystyrene (PS), poly carbonate (PC) and poly(methyl methacrylate) (PMMA) were used as blend matrix for comparison (Fig. 1a). Besides, all of the donors and polymers are soluble well in solvent and form continuous blend films with donor molecules, which made it possible for flexible device and circuit applications.

2. Results and Discussion

2. 1 Memory OFETs based on TTF blends

The pristine OFET with pure polymer buffer layer only shows weak hysteresis (take PMMA for example, Fig. 2a) as has been reported.[16] OFETs with thin layer of PMMA, PC, PEO and PS showed very week hysteresis with "memory window" ΔV_T less than 5 V as listed in Table 1. The memory window is defined as the difference between the threshold voltages in the "up" and "down" sweeps of the gate voltage. The electrical characteristics of the devices with TTF-PMMA blend buffer layer are shown in Fig. 2b–2d. The hysteresis obtained by employing donor molecules (Fig. 2b) appears to be quite similar to hysteresis loops obtained on OFETs with ferroelectric-like and ferroelectric polymer electrets.[9–13] In the transfer characteristics of OFET with TTF-PMMA buffer layer, the drain current has bistable states within a wide range of gate voltages with a memory ratio of 10^2 (there are two orders of magnitude difference in current between the high conductance ON state and low conductance OFF state).

Similar to regular ferroelectric OFETs, the operating voltage and the so-called "ratio of memory window",[11] can be adjusted by changing the thickness of donor–polymer blends (Fig. 2d) or the concentrations of donor in the solutions. The thickness can be most easily and effectively controlled through adjusting concentration of the spin-coating solution. The absolute value of memory window ΔV_T can be reduced by using thinner or high permittivity gate insulator for practical applications.[17,18] When the blend thickness increased to 30 nm, the devices showed notable memory effect with a ratio of memory window >50% (ΔV_T larger than 100 V). When very thin blend layer was used, the mobility was higher because the mobility is field-dependent, and a different mobility regime is accessed. When very thick blends were used, the memory

effect was even more remarkable but the mobility decreased.

2. 2 Memory OFETs based on ferrocene (Fc) and NiTPP blends

Since TTF is an extremely strong donor, when distributed between the semiconductor and dielectric layer, strong electrical-field-induced charge transfer will occur and produce abundant traps along the conductive channels.[19–21] It should be noted that the effective mobility (0.027 cm^2/Vs) was higher than normal CuPc based OFETs with n-octadecyltrichlorosilane (5.47×10^{-3} cm^2/Vs) or polymers ($2.6 \sim 7.7 \times 10^{-3}$ cm^2/Vs) modified dielectrics. The relative high mobility was due to increased carrier density thus the trapped carriers could be released in a narrow range of gate voltages. The sudden increase of the drain current at high gate voltage might be due to the charge and discharge effect of the stored charges in the buffer layer. This sudden process, however, allowed drain current increase steeply within a narrow gate voltage range. This directly made the mobility at high gate voltage be higher than usual but smaller at low gate voltage. Similar results have also been observed by Naber et al. in FerOFET with P(VDF−TrFE) as the gate dielectric.[22] This made our memory OFETs could be prepared using low mobility materials, and provided another approach to mobility enhancement for OFETs.

In order to overcome the problem of high OFF current when too strong donor molecules were used in the buffer layers, we carefully choose the donor molecules for the blend OFET memories. NiTPP and Fc with proper donor ability are chosen also for their superior solubility and moderate charge transfer characteristics, besides they are

cheap, commercially available. As shown in Fig. 3a, OFETs based on Fc–PMMA showed typical transistor output characteristics. For transfer characteristics, I_{DS} kept at high values in spite of running backwards of the gate voltage, further the I_{DS} showed no gate modulation (Fig. 3b). The on current could be retained as long as 24 hours in the atmosphere without significant increase of the OFF current (Fig. 3c), indicating high operating reliability of the memory devices. This implies that once the buffer layer is charged fully, the relaxation of the charges is a slow process.

TTF and ferrocene (Fc) sublimated nicely in vacuum. When we tried to fabricate OFETs using pure TTF and ferrocene thin buffer layers (without polymers) by sublimation, however, although TTF and ferrocene could be evaporated on to the substrate at early stage, desorption occurred after several minutes under the pressure of 10^{-4} Pa. This unique property during vacuum deposition, however, helped us a lot because it allowed us to remove most of the donor molecules on the surface of the polymer blends (supporting information, Fig. S3a–S3d). We have also tried extended TTFs (such as dibenzotetrathiafulvalene (DBTTF), bis(ethylenedithio)tetrathiafulvalene (BEDT-TTF)) using evaporation method to prepare the buffer layer without polymers. However, only very thin TTF layers made the OFET devices function but without notable memory effect, thicker TTF layers will induce high concentration mobile carriers which caused the channel be more conductive and degenerated the device modulation performances with very low ON/OFF ratios. When weaker donors such as ferrocene and NiTTP were used, the devices could normally function as transistors. We selected TTF as a model because it formed donor states easily, and it is a very classical

donor molecule. However, the memory ON/OFF ratio was relative low (10^2), so we then focus on ferrocene blends as buffer layers instead.

From the AFM imagine of the ferrocene-PMMA film on SiO_2 is shown in Fig. 4a, the surface was clearly very rough. Fig. 4b shows the AFM image of CuPc thin films on the blends, the CuPc molecules formed small grains on the blends. Relative rough surface and small grain size limited the device performance, further improvement of the OFET memories could be achieved by using high mobility materials or by optimizing the film growth conditions. Nevertheless, by balancing the stability[23] and OFF current considerations, it is also a good choice by using CuPc with superior stability.

2.3 Low voltage memory OFETs with polymer dielectrics

For a memory device, reversible and steep flanks of the hysteresis, a small operation voltage and long charge-retention time should be achieved. The low-voltage operation of organic and polymer transistors has been made possible by introduction of high-*k* or ultra thin gate dielectrics. Low voltage operated OFETs and memory elements can be fabricated using polymer dielectric (here we used crosslinked PMMA as shown in Fig. 5a, using 1,6-bis(trichlorosilyl)hexane as crosslinking agent[24,25]). It has been reported that in ferroelectric OFETs, the voltage required to switch the ferroelectric polarization can be reduced to 5 V without loss of ferroelectric properties by decreasing the ferroelectric layer thickness.[26] The OFET devices with crosslinked polymer dielectrics and donor/polymer blend buffer layer showed memory characteristics with reduced operating voltage less than 2V as shown in Fig. 5b and Fig. 5c. On the contrary,

polymer dielectric OFETs without donor blends showed no evidence of memory characteristics (Fig. 5d). When the operating voltage of the memory elements was lowed down, steep flanks of the hysteresis were persistent, and the "ratio of memory window" to the total sweep voltage range was about the same (larger than 50%).The reason why we demonstrated our results on prototype device using 500 nm SiO_2 dielectric is that it prevents leakage problem, and it ensures the reproducibility which is very important for the mechanism discussions.

3 Mechanism

3.1 Effect of the source-drain voltage

On the explanations of large threshold voltage shifts in the "up" and "down" sweeps of the gate voltage of OFETs, we firstly applied different drain V_{DS} voltages to observe sizable I_{DS} values. The memory effect was very large even at very low V_{DS} (e.g., V_{DS} = −5 V) as shown in Fig. 6a (similar results can also be seen in Fig. 3b). The flanks of the hysteresis were persistently steep and showed little dependence on the drain voltage applied (as shown in Fig. 6b).

3.2 Effect of the gate voltage sweep range

There have been observed and identified three hysteresis mechanisms in *p*-channel OFETs: (1) slow polarization of the gate dielectric[9–13], (2) electron trapping in the semiconductor[27], and (3) charge storage in the dielectric.[28] Hysteresis due to mechanism (1) is observed when the gate dielectric is a polymer containing dipolar groups or molecules that can be slowly reoriented by an applied electric field. The

mechanism (2) is due to fast filling of electron traps (acceptors) and slow emptying of filled traps (i.e., hole capture by charged acceptors) in organic semiconductors(or at the interface). The mechanism (3) can be differentiated from mechanism (2), however, by measuring the transfer characteristics in either loop direction. In contrast, hysteresis due to mechanism (3) can be in either loop direction, depending on the sign and location of the injected and stored charge.[5] Our experimental results support this very well (Fig. 2b), so our hysteresis of OFETs tends to be due to mechanism (3).

The mechanism (3) can also be differentiated from mechanism (1) and (2) by measuring I_{DS} current in various range of gate voltage as shown in Fig. 7a – Fig. 7d. Initially at the most positive V_G, negative charge is accumulated in the channel and the electron traps are filled. When V_G sweeps toward negative (i.e., from OFF to ON), more holes are induced than required by the present V_G and gate-to-channel capacitance, because extra holes balance the stored charge, resulting in a net charge that satisfies the charge-voltage relation. Seen in the reverse scan the transistor current remains constantly high when the gate voltage is reduced unless a depletion voltage is applied from the gate. Current in the reverse direction did not decrease with the identical slope as in the forward direction. It has been reported that donor molecules increased charge storage capacity due to increased space charge, at interstitial boundaries.[29] We take this as compelling evidence that the observed shifts of the threshold voltage are caused by the charge storage in the dielectric and the built-in electric field of the donor molecules.[30]

3.3 Detecting the presence of charges in the dielectric

Presence of charges in the dielectric can be detected when scanning the capacitance at low AC frequencies.[31] Metal-Insulator-Metal (MIM) capacitance is measured as a function of the AC frequency. The AC amplitude is set at ± 0.5 V. The capacitance and the dielectric loss angle are plotted as function of the frequency for both PMMA and donor/PMMA samples as shown in Fig. 8a and 8b. The dielectric properties of the donor polymer blends layer start to change when scanning downwards to low frequencies, an increase in capacitance is observed which relates to charge carriers in the bulk of the insulator and gives a response only at low frequencies. The frequency dependent capacitance changes arise because of presence of two different capacitors. The dielectric layer is represented by the SiO_2 which dominates at high frequency range. The donor/polymer blend layer is represented by the donor molecules, which dominates at frequency ranges. The layer-by-layer addition of capacitors should follow the Maxwell-Wagner equation[32] for lossy dielectric capacitors.

3.4 Origin of the charge storage

A possible mechanism of the presence of charges in the dielectric is suggested as follows. Electrical-field-induced charge transfer could occur between semiconducting and donor molecules after applying a gate voltage pulse. Due to the low mobility of organic semiconductor materials, the drift velocity of carriers in an OFET was very small. As a result, programming and erasing can be achieved by pulsing the gate voltage to induce Poole-Frenkel tunneling[33] and/or trap-assisted tunneling.[34] A negative gate voltage raised the energy of electrons in the molecules and results in

tunneling of carriers from the semiconductor to the donor through the barrier polymer layer. A reverse voltage sweep causes carriers to tunnel from the blends to the active semiconducting layer. The tunneling current also strongly depends on the tunnel barrier width, which is directly determined by the polymer thickness at the surface of buried donor molecules. As our device configurations contains randomly distributed multi phase components (donors, semiconductors and polymers), it's hard to determine exactly the physics parameters of the tunneling process. However, note that the energy band diagrams have been well developed to explain complex device physics such as solar cells, we here propose the energy band analysis as shown in Fig. 9a and 9b.

The HOMO of CuPc, TTF and ferrocene are 5.3 eV, 5.09 eV and 4.8 eV, respectively, the LUMO of CuPc, TTF and ferrocene are 3.6 eV[35], 2.33 eV[36] and 1.91 eV[37], respectively. Therefore, the interaction between donor and CuPc may be weak prior to the electronic transition. However, a high electrical field may facilitate electron transfer from the HOMO of TTF to the LUMO of CuPc. Because energies of both LUMO and HOMO of TTF and ferrocene are sufficiently higher than those of CuPc (3.6 and 5.3 eV), respectively, it is energetically favorable for charge transfer effect. For CuPc can function as electron acceptors,[38] especially when being contacted with strong donor molecules. Charge tunneling through the insulator polymer on organic molecules is possible. In other words, donor and CuPc are charged positively and negatively, respectively. Therefore, carriers are generated and the device exhibits a sharp increase in conductivity after the charge transfer.

During the writing process, some of the carriers were generated to be traps due to

charge transfer process. In organic semiconductors, if the HOMO/LUMO position of an incorporated molecule is positioned in the gap of the host molecules it will form a trap state.[39] The charge transfer occurs on a time scale of 40–50 fs and the charge-separated state is metastable.[40] This ensures the fast switching speed and stability of our memory devices between on and off states. Even when the gate field is withdrawn, these charges remain in the dielectrics because of tunneling barrier of the insulating polymer. Since an external gate electrical field induces the charge transfer, the film becomes polarized after the charge transfer, and only a reverse electric field can cause tunneling of the electron from CuPc back to the HOMO of the donor molecules, resulting in a return to the low-conductivity state of the channel.

3.5 Control experiments

In order to confirm the effect of charge transfer, we carried out control experiments based on Fc blended with various polymers. All Fc-polymer OFETs showed memory effects with large memory windows regardless of the kinds of polymer chosen (Table 1), but obviously blends of polymers with carbonyl groups, e.g., PMMA and PC, showed superior performances, maybe due to different chemical nature of the surfaces of polymer blends. The dielectric constants of (PEO), polystyrene (PS), poly carbonate (PC) and poly(methyl methacrylate) (PMMA) are about 2.5, 2.6, 2.9 and 2.6, respectively. As the concentrations of the donor molecules in the polymer blends were very low, the dielectric constants of the blends were almost the same to their corresponding polymer matrixes according to the AC impedance tests. We have also tried polymer blends with high dielectric constant polymers (such as PVA, dielectric

constant 7.8), and the memory effects were more remarkable. So the charges stored in the dielectric play important role as the memory effect, for high dielectric constant buffer layers can store more charges in the dielectric.

When BPFc (1,1'-bis(diphenylphosphino) ferrocene), whose oxidative peak was at 0.24 eV more positive than Fc (Fig. 3e and Fig. 3f),[41] blended with various polymers were used, surprisingly, none of the devices showed any tendency of OFET memories (as an example, Fig. 3d shows the transfer characteristics of OFET based on BPFc–PMMA blend), although all of the Fc–polymer blends showed large memory windows. We also tried to use TCNQ (7,7,8,8-tetracyanoquinodimethane) and $F_{16}CuPc$ (hexadecafluorophthalocyaninatocopper) as acceptor molecules to examine another aspect of our experiment. However, no obvious memory effect was observed as high concentration mobile carriers could be generated due to strong charge transfer effect. Besides, the high concentration mobile carriers also caused the channel be highly conductive and degenerated the device modulation performances with very low ON/OFF ratios.

To further clarify the charge transfer process, we fabricated control devices with an additional thin layer of polymer (20 nm) between the blend and the semiconducting layers. In order not to kill the bottom blend layer, we firstly used water soluble polymers such as PEO (20 nm) to cover the donor molecule containing buffer layer. We also used 20 nm PMMA to cover crosslinked PMMA blends (using 1,6-bis(trichlorosilyl)hexane as crosslinking agent). Devices with crosslinked PMMA blends without 20 nm top PMMA layer showed remarkable memory effect the same as

the uncrosslinked ones. Both the two types of double gate devices with top polymer layers exhibited very feeble memory effect or none at all in some cases as shown in Fig. 10a–10d. The inserted polymer layer stop the semiconductor interacting with donor molecules thus very weak memory effect was observed (ΔV_T less than 3 V). The absence of hysteresis effect indicated that only the blends can capture charges rather than polymers or small molecules themselves. Also, this indicates that the interactions between donor and semiconductor molecules as well as the existing of polymer matrix are both essential for high performance memory elements. Moreover, memory effects must arise primarily from charge stored near the semiconductor-dielectric interface where the charge transfer between the semiconducting and donor molecules occurred.

4. Conclusions

In conclusion, high performance organic transistor memory elements with steep flanks of the hysteresis have been demonstrated using a donor–polymer blend buffer layers. The organic memory transistor elements with donor–polymer blends showed steep flanks of the hysteresis with memory ratio up to 2×10^4, and retention time in excess of 24 hours. This method presented made it possible to produce organic flash memory elements at low cost and high efficiency for practical inexpensive organic circuits and products.

5. Experimental

We build the organic memory transistor elements as close as possible to how OFETs

are normally built to maintain a high degree of compatibility with current OFET production technology. Blends of small molecules (TTF, NiTPP and ferrocene) with polymers (PS, PEO, PC, and PMMA), all polymers are commercial available and used as received) were deposited from solution by spin-coating onto silicon substrate with 500 nm thick SiO_2 layer as the gate dielectric. The layer does not require any annealing treatment, important when dealing with temperature sensitive materials such as plastic substrates or semiconductors. After dried for 15 min under 60 ^oC, CuPc (Aldrich, purified three times by sublimation) was evaporated on top of the blend buffer layer. During the evaporation, the vacuum was around 10^{-4} Pa and the deposition rate was kept at 1 Å /s. Gold source and drain top contacts were also evaporated, at a rate of 10 Å/s. All transistors had a channel width to channel length ratio of 3 mm/0.05 mm. The general device geometry is shown in Fig. 1b.

The organic memory transistor elements were characterized with Hewlett-Packard (HP) 4140B semiconductor parameter analyzer under air at room temperature. During the measurement cycles and stability tests, we did not notice any performance degradation of the entirely unprotected the organic memory transistor elements when being exposed to ambient condition (supporting information, Fig. S1a – S1d). That is one of the reasons why we choose CuPc as active semiconductor layer. To measure the memory effect, we applied a certain drain voltage to the organic memory transistor elements and sweep the gate voltage, this is the so-called transfer characteristic. After a sweep to negative voltages, the organic memory transistor stays “ON” at zero gate voltage, meaning the current flows between source and drain. After a sweep to positive

voltages, the organic memory transistor stays “OFF” and the current is several orders of magnitude lower.

SEM was performed on a Hitachi S-4300 field-emission scanning electron microscope at R. T. Atomic force microscopy (AFM) images were obtained on an SPI3800N machine (SII Seiko instruments Inc.) using tapping mode. The capacitance measurements were performed on the CHI660 electrochemical workstation at room temperature.

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Figure Legends

Figure 1. (a) Chemical structures of donor molecules and polymers for blend organic memory transistor elements. (b) Schematic drawing of the proposed organic transistor memory elements.

Figure 2. Transfer characteristics of a device based on (a) PMMA, (b) TTF–PMMA blend, The gate voltage was firstly applied from 100 V to −100V, then from −100 V to 100V as the forward cycling program. To guarantee the reversible read and write process in both directions, we applied a following test by changing the gate voltage from −100 V to +100V, then from +100 V to −100V, as the reverse cycling program. (c) Output characteristics of b. (d) device parameters of memories with various TTF–PMMA blend thickness.

Figure 3. FET characteristics of a device based on Fc–PMMA: (a) typical output characteristics, (b) transfer characteristics. (c) the retention properties of the memory device, the ON and OFF states have been programmed by a gate voltage pulse (100 ms) of −100 V and +100 V, respectively. (d) Transfer characteristics of control device based on OFET with BPFc–PMMA blend at V_{DS} = −100 V. Cyclic voltammogram of (e) ferrocene and (f) 1,1'-bis(diphenylphosphino) ferrocene (BPFc).

Figure 4. AFM images of (a) Fc–PMMA blends on SiO_2, (b) CuPc films on the blends.

Figure 5. (a) Schematic drawing of organic transistor memory elements using crosslinked polymer as dielectrics. Typical (b) output and (c) transfer characteristics of memory devices with crosslinked polymer as dielectrics, (d) transfer characteristics of control device without donor/polymer blend buffer layer.

Figure 6. (a) Transfer characteristics of memory devices at various V_{DS}, (b) Memory window characteristics at various V_{DS} extracted the same device.

Figure 7. (a) Transfer characteristics of memory devices with V_G scanned from +100 V to various V_G, (b) V_{T1} and V_{T2} as a function of V_G. (c) Transfer characteristics of memory devices scanned various V_G to from −100 V. (d) V_{T1} and V_{T2} as a function of V_G.

Figure 8. Capacitance–frequency of both Metal–Insulator–Metal (MIM) capacitances (A.C. voltage amplitude was 0.5 V). (a) PMMA sample, (b) PMMA/donor sample.On the right hand side dielectric loss angle is also shown.

Figure 9. Schematic energy band diagrams of memory structures under (a) program and (b) erase modes.

Figure 10. (a) Output characteristics, (b) transfer characteristics at V_{DS} = −100 V of control OFET device with an additional water soluble PEO layer between the donor/polymer blend and semiconductor. (c) Output characteristics, (d) transfer characteristics at V_{DS} = −100 V of control OFET device with an additional PMMA layer on the top of crosslinked donor/polymer blends.

Figure 1.

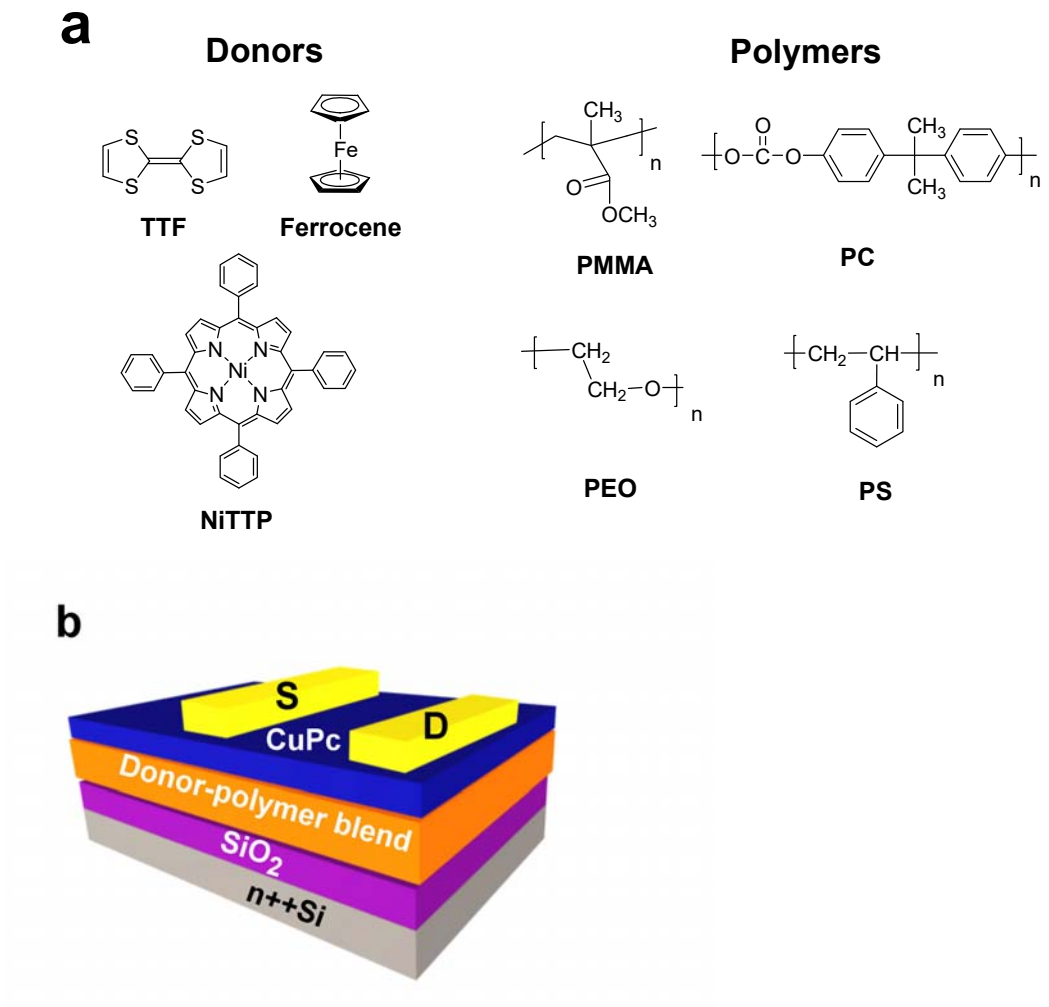

a
Donors
Polymers
TTF
Ferrocene
PMMA
PC
NiTTP
PEO
PS
b
S
D
CuPc
Donor-polymer blend
SiO2
n++Si

Figure 2.

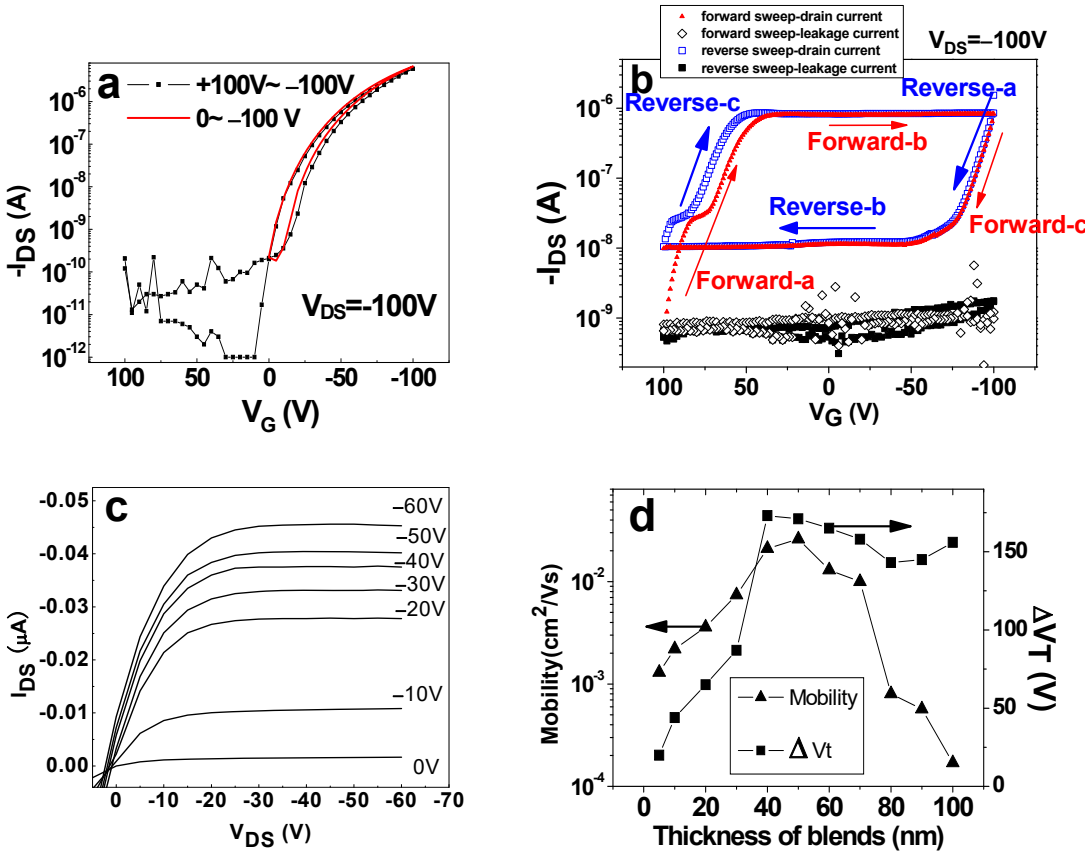

a
+100V~ –100V
0~ –100 V
VDS=-100V
-IDS (A)
VG (V)
b
forward sweep-drain current
forward sweep-leakage current
reverse sweep-drain current
reverse sweep-leakage current
VDS=–100V
Reverse-c
Reverse-a
Forward-b
Reverse-b
Forward-c
Forward-a
-IDS (A)
VG (V)
c
–60V
–50V
–40V
–30V
–20V
–10V
0V
IDS (μA)
VDS (V)
d
Mobility
ΔVt
Mobility(cm2/Vs)
ΔVT (V)
Thickness of blends (nm)

Figure 3

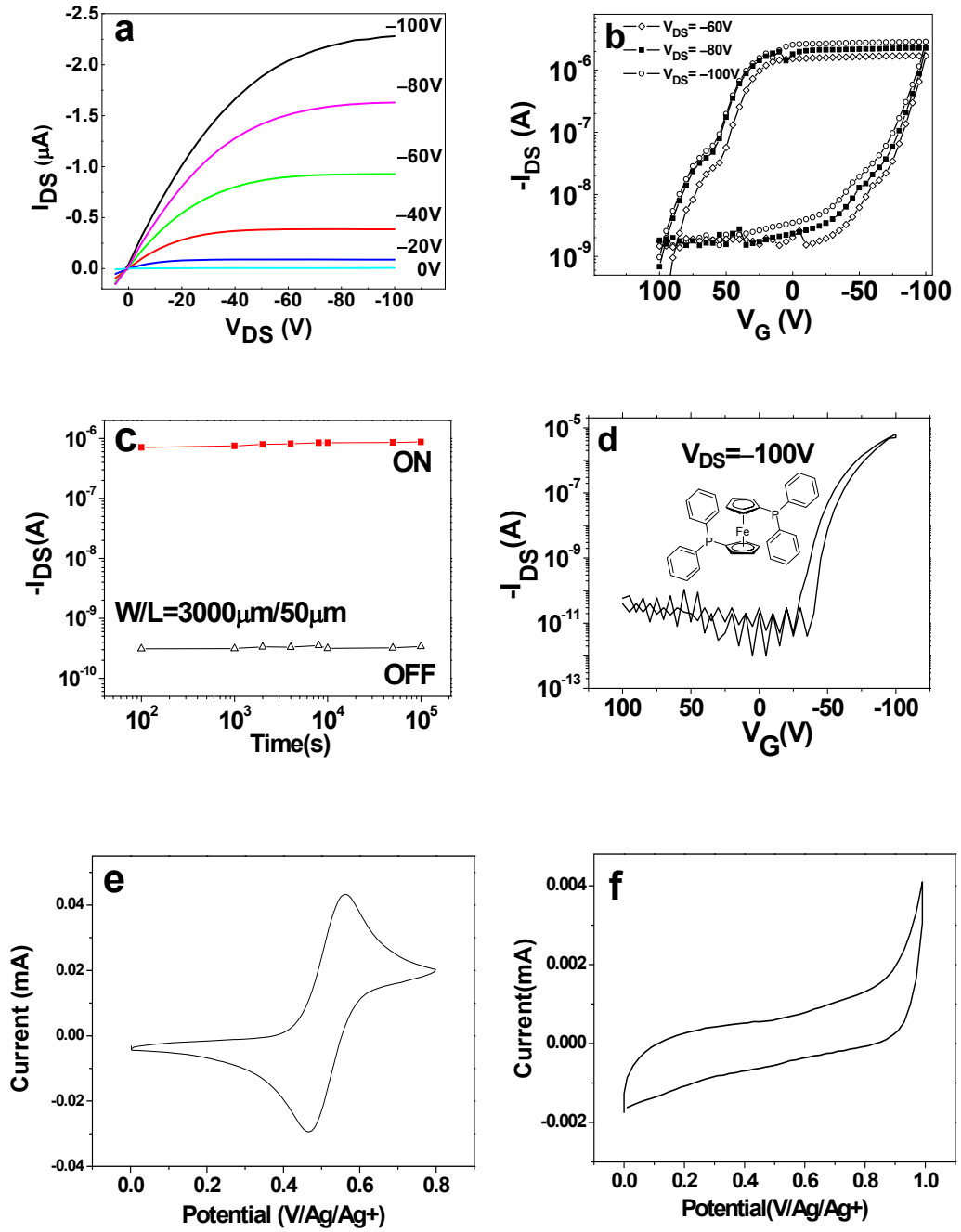

a
–100V
–80V
–60V
–40V
–20V
0V
I_{DS} (μA)
V_{DS} (V)
b
V_{DS}= –60V
V_{DS}= –80V
V_{DS}= –100V
$-I_{DS}$ (A)
V_G (V)
c
ON
W/L=3000μm/50μm
OFF
$-I_{DS}$(A)
Time(s)
d
V_{DS}=–100V
Fe
$-I_{DS}$(A)
V_G(V)
e
Current (mA)
Potential (V/Ag/Ag+)
f
Current(mA)
Potential(V/Ag/Ag+)

Figure 4.

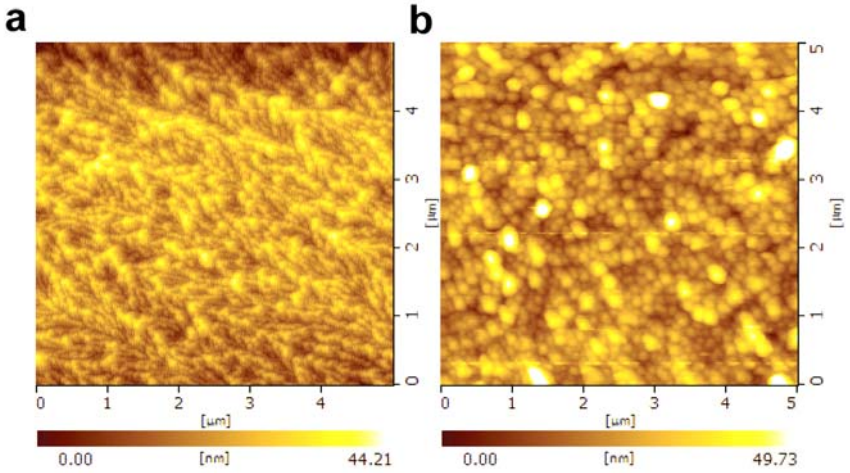


Figure 5

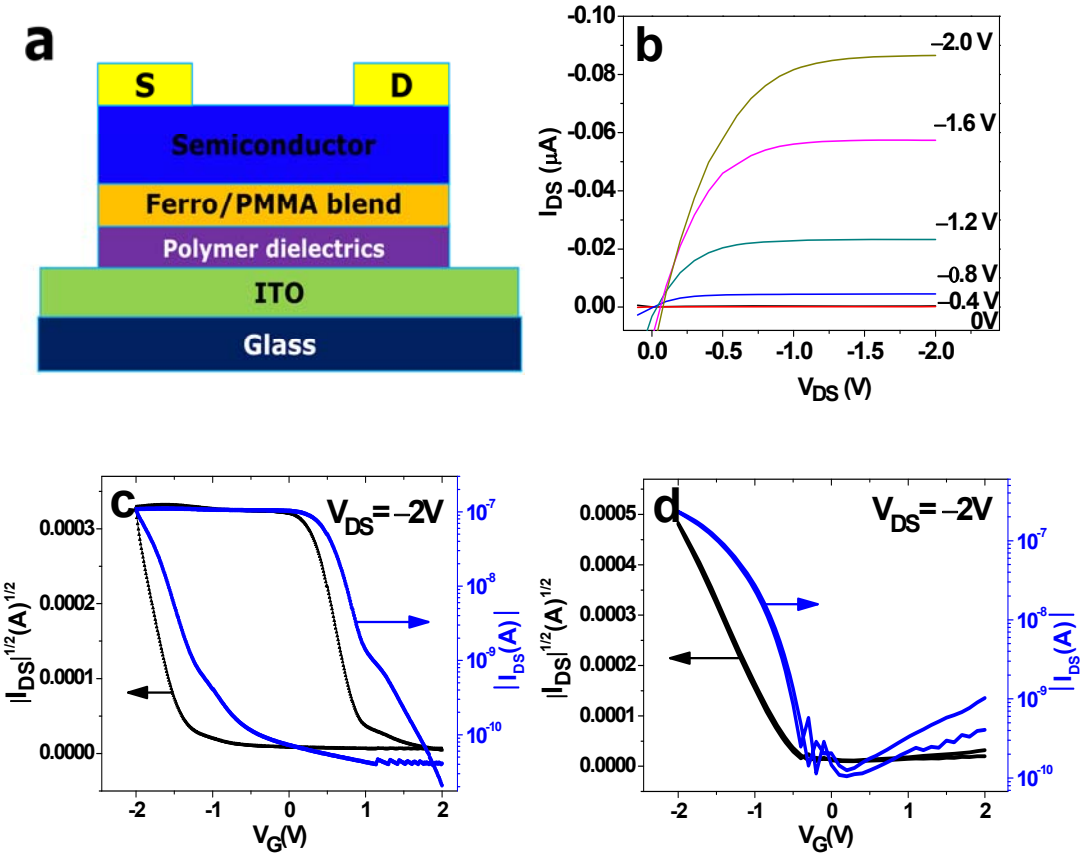

a
S
D
Semiconductor
Ferro/PMMA blend
Polymer dielectrics
ITO
Glass
b
–2.0 V
–1.6 V
–1.2 V
–0.8 V
–0.4 V
0V
I_{DS} (μA)
V_{DS} (V)
c
V_{DS}= –2V
$|I_{DS}|^{1/2}(A)^{1/2}$
$|I_{DS}(A)|$
V_G(V)
d
V_{DS}= –2V
$|I_{DS}|^{1/2}(A)^{1/2}$
$|I_{DS}(A)|$
V_G(V)

Figure 6

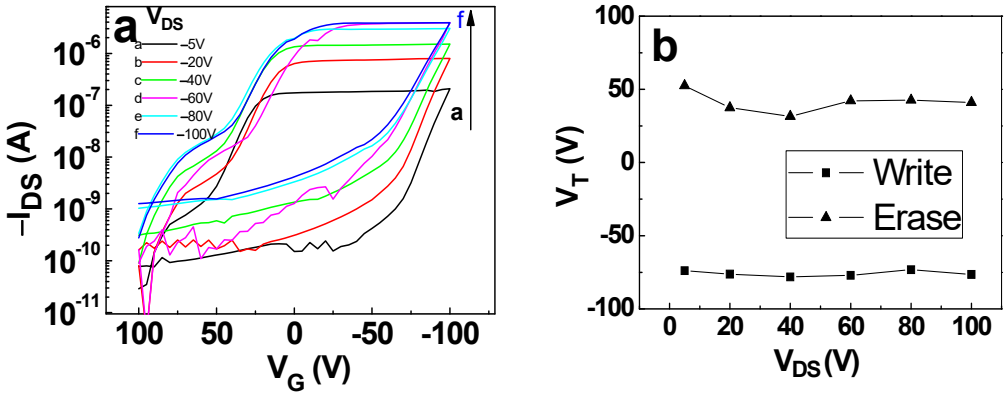

a
V_{DS}
a –5V
b –20V
c –40V
d –60V
e –80V
f –100V
f
a
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
$-I_{DS}$ (A)
100 50 0 -50 -100
V_G (V)
b
100
50
0
-50
-100
V_T (V)
Write
Erase
0 20 40 60 80 100
V_{DS} (V)

Figure 7

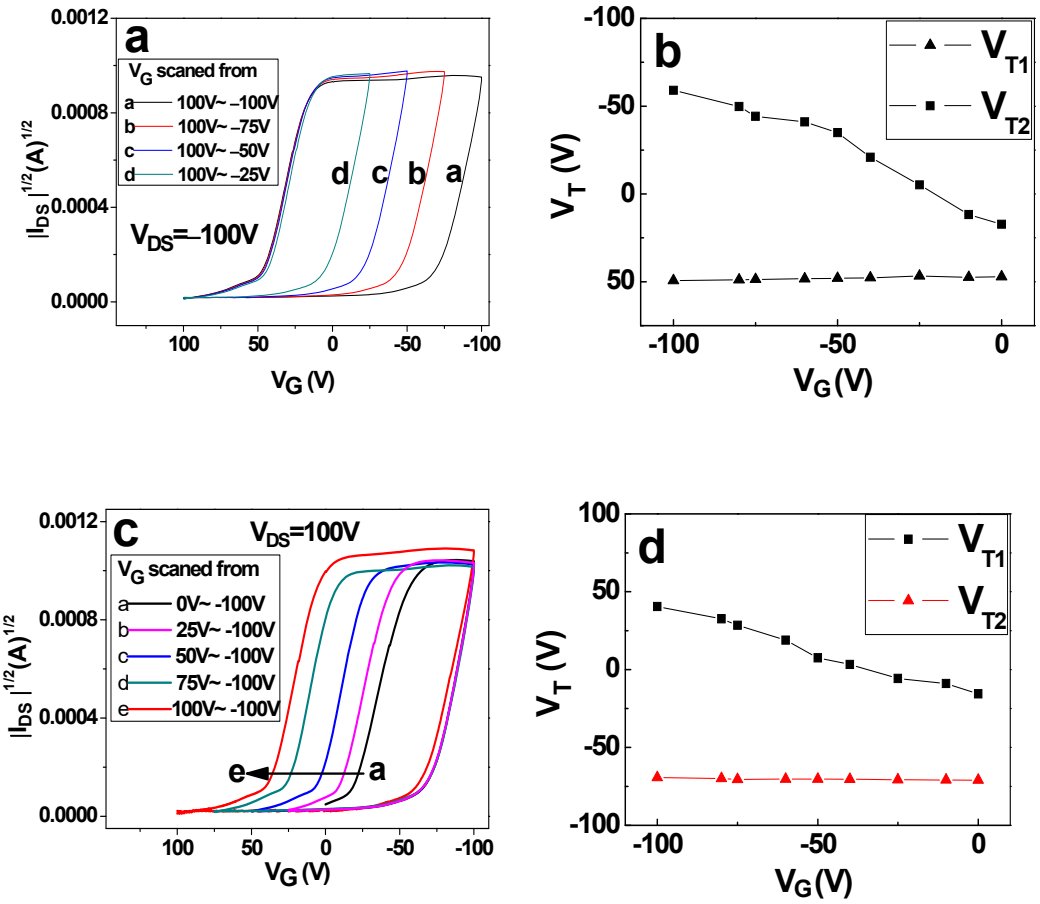

a
V_G scaned from
a 100V~ -100V
b 100V~ -75V
c 100V~ -50V
d 100V~ -25V
d c b a
V_DS=-100V
|I_DS|^1/2(A)^1/2
V_G (V)
b
V_T1
V_T2
V_T (V)
V_G (V)
c
V_DS=100V
V_G scaned from
a 0V~ -100V
b 25V~ -100V
c 50V~ -100V
d 75V~ -100V
e 100V~ -100V
e
a
|I_DS|^1/2(A)^1/2
V_G (V)
d
V_T1
V_T2
V_T (V)
V_G (V)

Figure 8

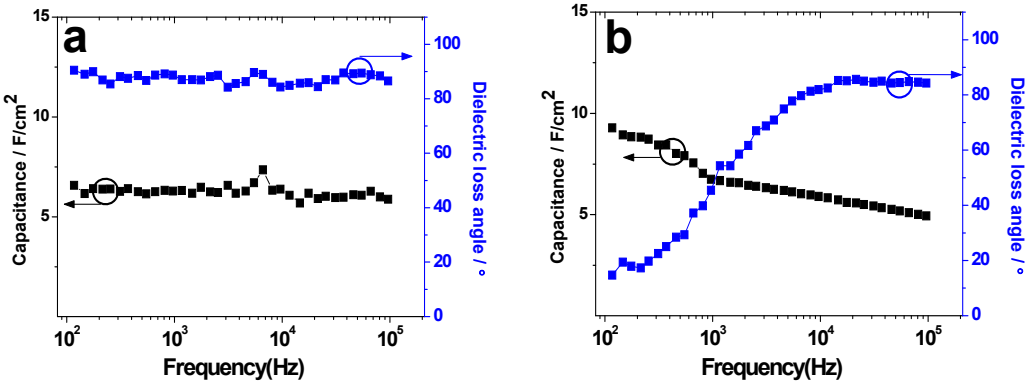

a
b
Capacitance / F/cm2
Dielectric loss angle / °
Frequency(Hz)
15
10
5
100
80
60
40
20
0
10^2
10^3
10^4
10^5

Figure 9

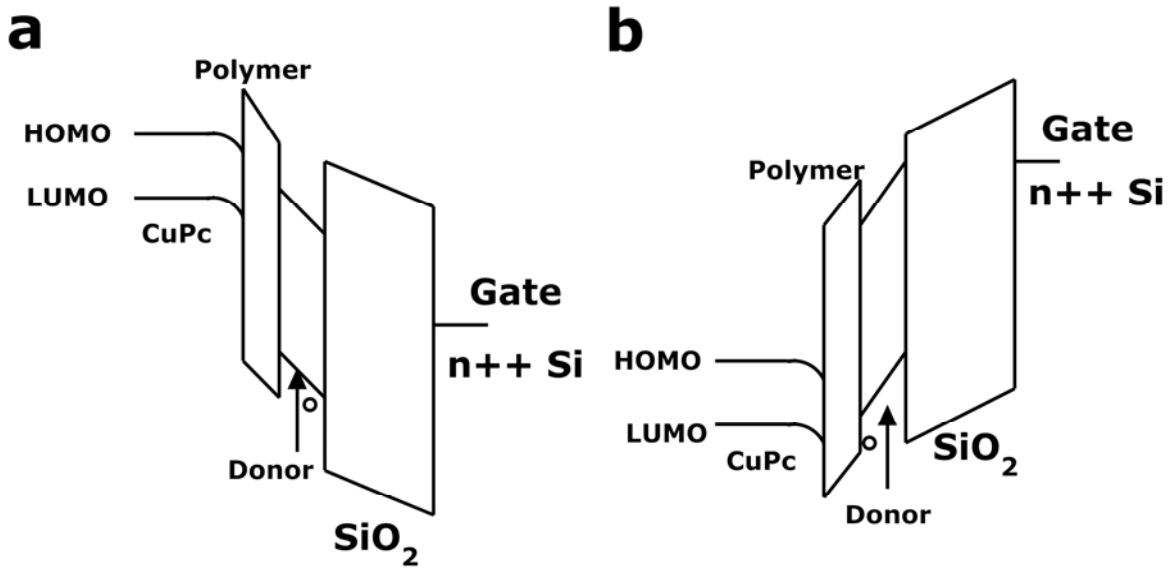

a
Polymer
HOMO
LUMO
CuPc
Gate
n++ Si
Donor
SiO2
b
Gate
n++ Si
Polymer
HOMO
LUMO
CuPc
SiO2
Donor

Figure 10

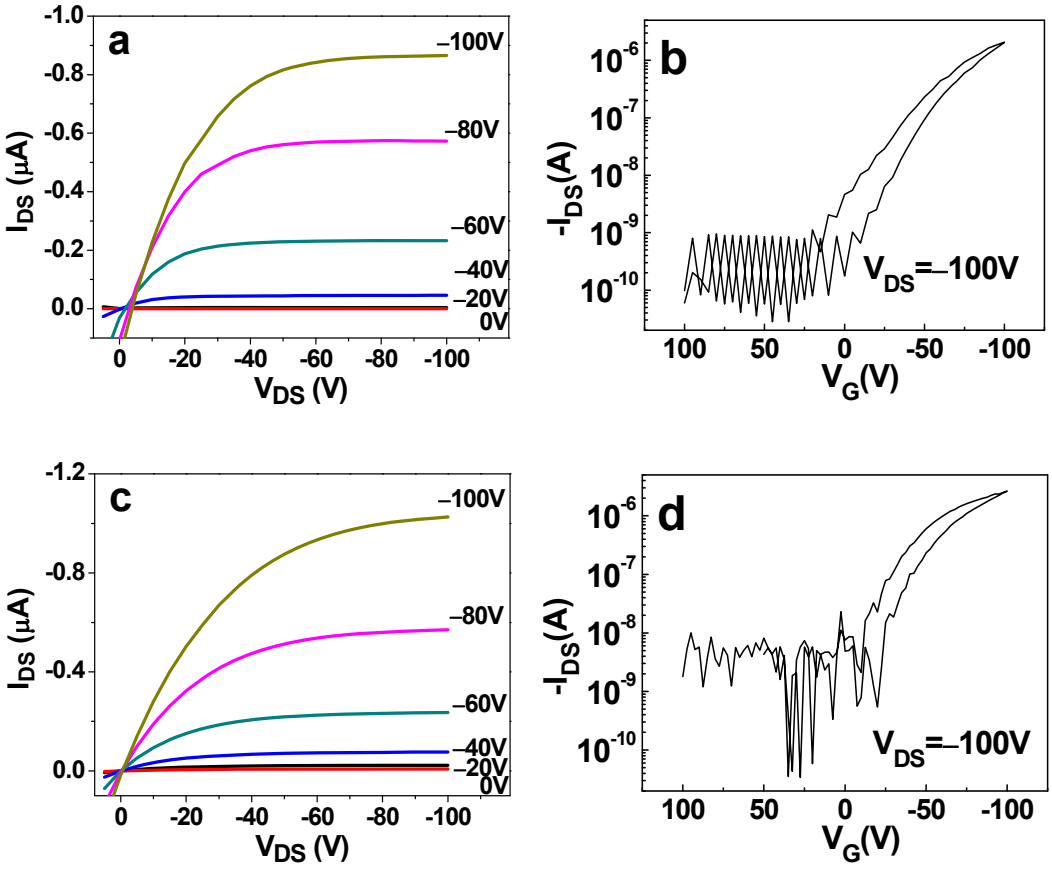

a
-1.0
-0.8
-0.6
-0.4
-0.2
0.0
I_{DS} (μA)
0
-20
-40
-60
-80
-100
V_{DS} (V)
–100V
–80V
–60V
–40V
–20V
0V
b
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
$-I_{DS}$(A)
100
50
0
-50
-100
V_G(V)
V_{DS}=–100V
c
-1.2
-0.8
-0.4
0.0
I_{DS} (μA)
V_{DS} (V)
d
$-I_{DS}$(A)
V_G(V)
V_{DS}=–100V

Table 1. Device parameters of TTF, Fc and BPFc blended with four polymers: PS, PEO, PC, and PMMA

Blend type	**Mobility** (cm^2/Vs)	$\mathbf{I_{ON}/I_{OFF}}$	(V_{T1}, V_{T2})	ΔV_T	Memory Modulations[c]
None	5.47×10^{-3}	4.5×10^{5}	–13V	2V	-[d]
PMMA	4.9×10^{-3}	3.2×10^{5}	–7 V	3V	-[d]
PC	6.2×10^{-3}	9.8×10^{4}	–9 V	1.4V	-[d]
PEO	2.6×10^{-3}	7.3×10^{4}	–11 V	1V	-[d]
PS	7.7×10^{-3}	5.5×10^{5}	–13 V	0.7V	-[d]
TTF–PMMA	0.027[a] 0.024[b]	8.2×10^{3}	(–85V[a],+88V[b])	173V	75
Fc–PC	3.71×10^{-4} 0.016	4.8×10^{4}	(–79V,+77V)	156V	2×10^{4}
Fc–PEO	4.38×10^{-4} 0.011	6.8×10^{5}	(–78V, +12V)	90V	3×10^{4}
Fc–PS	3.73×10^{-5} 2.75×10^{-4}	1.6×10^{4}	(–13V, –71V)	58V	500
Fc–PMMA	2.21×10^{-3} 0.029	5.9×10^{4}	(–82V,+73V)	155V	2×10^{3}
BPFc–PMMA	8.49×10^{-3} 0.014	7.9×10^{5}	(–51V, –56V)	5V	-[d]

[a] forward, [b] reverse;

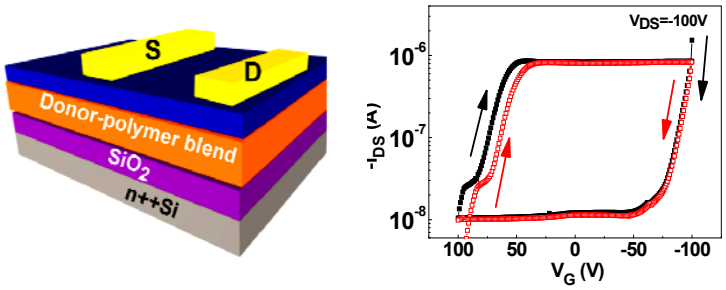
[c] Defined by the factor between the “ON” state drain current and the “OFF” state drain current, usually determined at zero volts gate voltage.

[d] can not be detected (lower than 10)

Table of Contents

High performance organic transistor memory elements with steep flanks of hysteresis

By Weiping Wu, Yunqi Liu*, Hongliang Zhang, Ying Wang, Shanghui Ye, Yunlong Guo, Chongan Di, Gui Yu and Daoben Zhu



Supporting Information

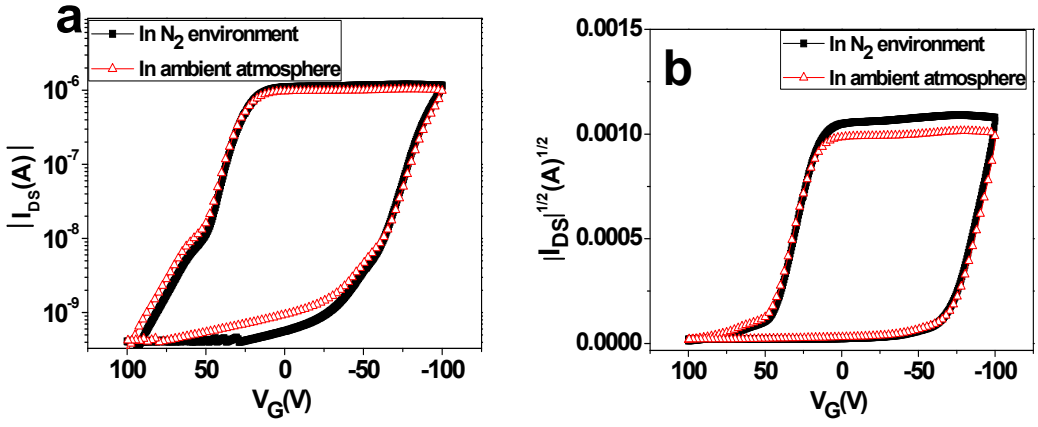
High performance organic transistor memory elements with steep flanks of hysteresis

By Weiping Wu, Yunqi Liu*, Hongliang Zhang, Ying Wang, Shanghui Ye, Yunlong Guo, Chongan Di, Gui Yu, and Daoben Zhu

E-mail: liuyq@mail.iccas.ac.cn

S1. Effect of O_2 and humidity

We found that, the O_2 and did humidity have some effects on the off current, but it not the key factor of our large hysteresis behavior as shown in Fig. S1a–Fig. S1d. In fact, the effect of humidity on the hysteresis behavior of OFETs has been reported,[S1] the hysteresis has something to do with it however it was the minor contribution to our steep hysteresis memory devices. One reason is that so small hysteresis caused by O_2 and did humidity have been hidden by the hysteresis induced by charge storage effects.



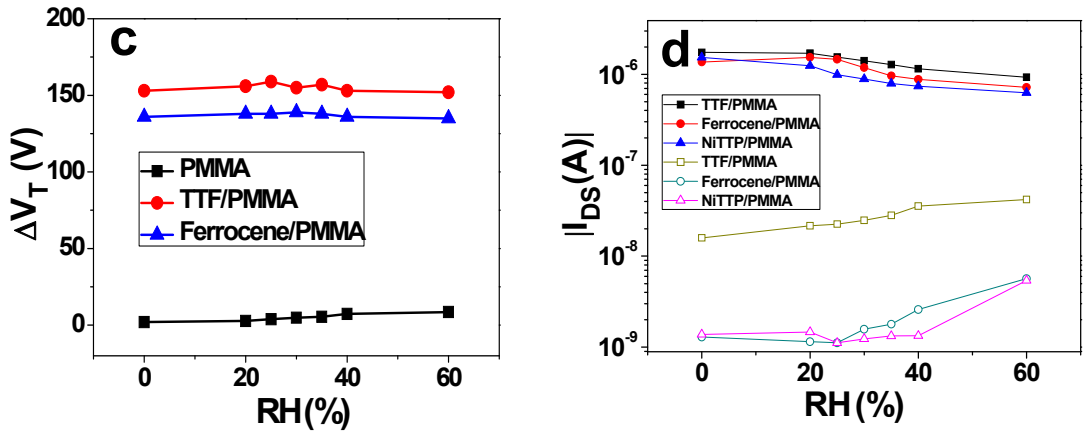


Figure S1. Transfer characteristics of a device based on Ferrocene-PMMA (a) $|I_{DS}|$ vs V_G characteristics, (b) $|I_{DS}|^{1/2}$ vs V_G characteristics. (c) Effect of humidity on the memory window, (d) effect of humidity on channel current.

S2. Device stability

The retention time and stress test of both the ON and OFF states are important for practical applications of nonvolatile electronic memory devices. Devices reported in this work have retained a programmed state for at least 24 hours. The memory window of upon cycling times with various donors and ferrocene blended with various polymers are shown in Fig. S2a and Fig. S2d. All the devices showed stability upon cycling program and erase operations. The stress test of devices for both ON and OFF states is shown in Fig. S2c and S2d. The ON and OFF states were programmed by applying –100V and 100V gate voltage, respectively. The current in both states were stable for at least 24 hours.

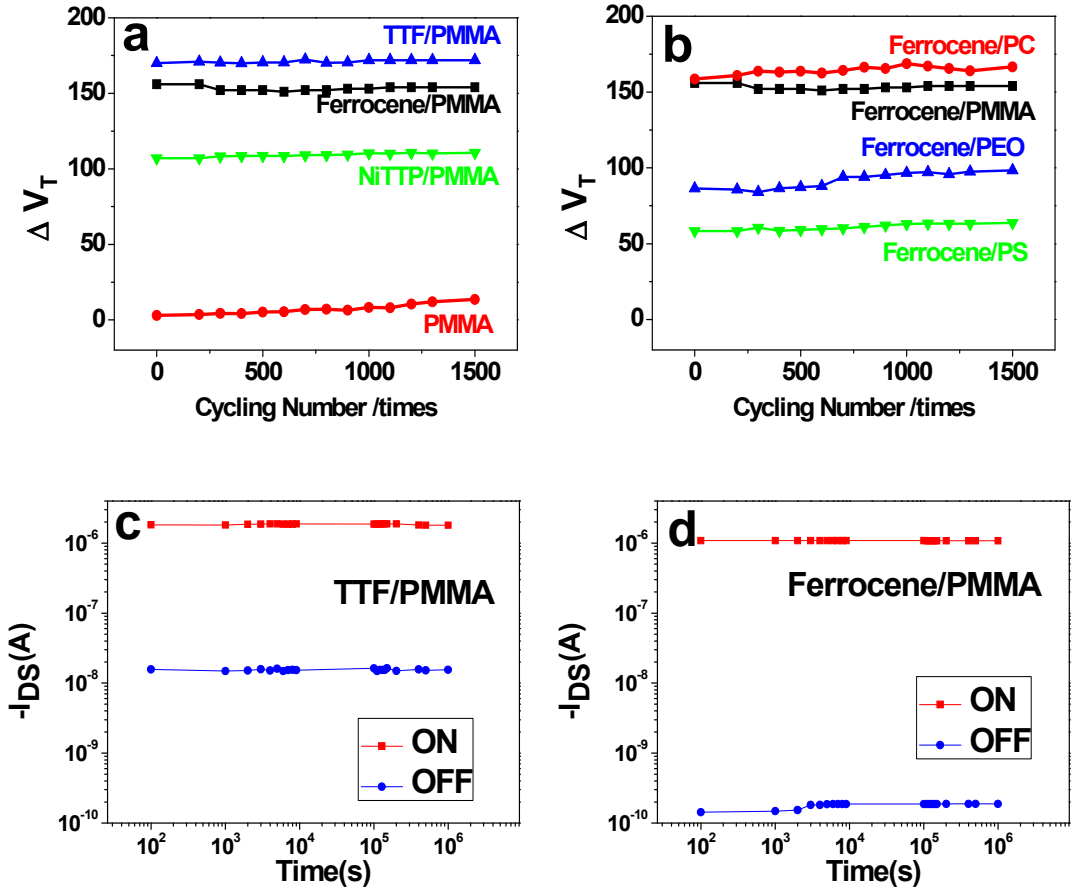


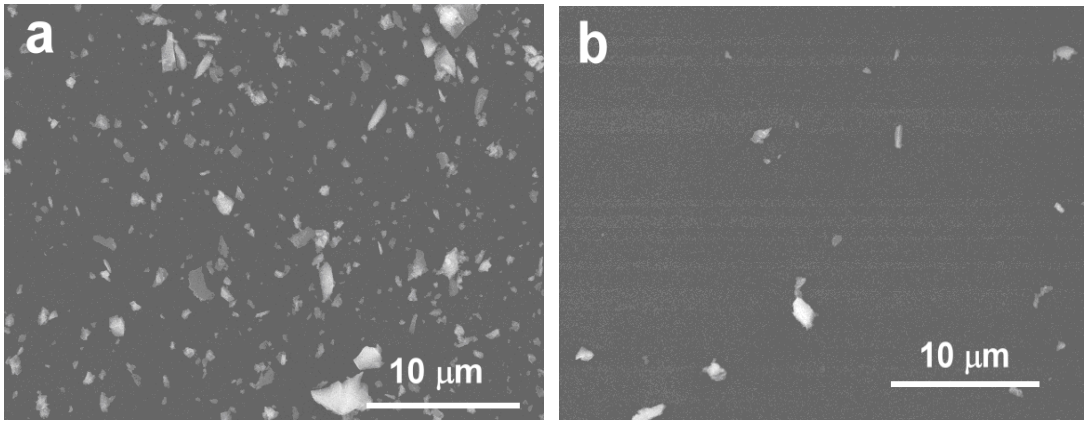
Figure S2. Device stability upon cycling times and holding times. Memory window as the function of cycling times(All of the cycling tests were the forward manner in figure 2b), (a)various blended with PMMA and (b) Ferrocene blended with various as buffer layers. Memory retention characteristics of devices (c) with TTF/PMMA and with (d) Ferrocene/PMMA buffer layers.

Stability of the positive charge on the ferrocene nano aggregations is due to the insulating coating between the buried donor clusters in the polymer matrix and CuPc semiconductor layer, which prevents recombination of the charge after removal of the external electric field. The factor that the devices showed superior stability upon operations indicates the memory of the transistor is due to charge build up and storage.

Charge carriers (space charges) inside the insulating layer will move with the field towards the gate and the interface to the semiconductor respectively. This causes additional polarisation due to charge state at the bulk and at the interface. When a memory OFET is characterized, reversing the gate voltage V_G features large metastable hysteresis with a long retention time due to quasi-permanent charge storage in the bulk of the gate dielectric or interface of the gate dielectric and the semiconductor (see the mechanism part).

S3. Morphology of interfacial layers

Figure S3a and S3b show SEM imagines of ferrocene/PMMA blend on SiO_2 as prepared by spin coating and after being stored at high vacuum for half an hour, respectively. Most donor clusters on the surface could be removed by high vacuum before the deposition of semiconductor layer. In this manner, the donor molecules left could be encapsulated by polymers (Fig. S3c and S3d show the cross section of TTF/PMMA and ferrocene/PMMA blends, respectively), and organic semiconductor/polymer/donor sandwich structures could be formed for memory effects.



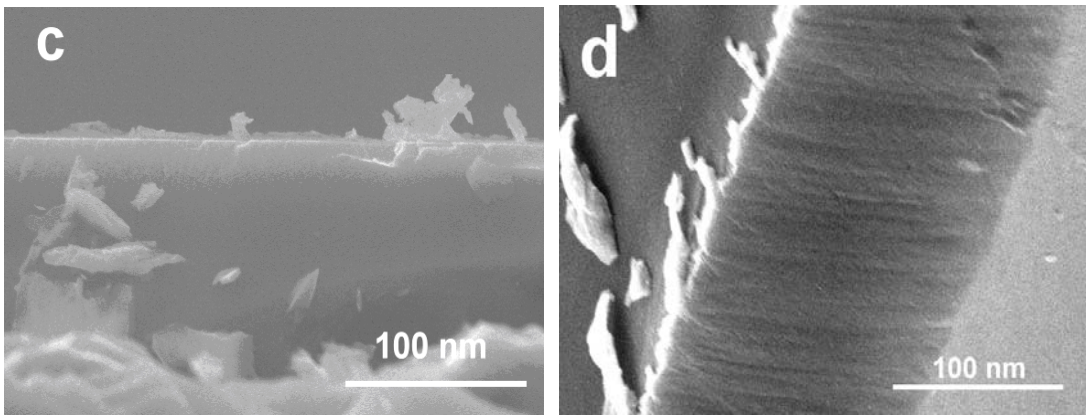


Figure S3. SEM imagines of Ferrocene/PMMA blend on SiO_2, (a) as prepared by spin coating, (b) after being stored at high vacuum for half an hour. SEM imagines of cross section of (c) TTF/PMMA and (d) Ferrocene/PMMA blends.

S3. Pentacene based memory OFET

Pentacene showed high mobility as high as 1–5 cm^2/Vs for OFET applications. Although pentacene OFET memories showed high mobility, the OFF current was high (as shown in Fig. S4a – Fig. S4d) due to the conductivity was determined by the mobility μ and the charge carrier density N_d ,

$$\sigma = N_d q \mu \qquad \text{(S1)}$$

where q is the charge on an electron. High mobility OFET memory elements using high mobility semiconductors are under investigation to control the OFF current (using different device configurations). By balancing the stability and OFF current considerations, it is a also good choice by using CuPc with stability.

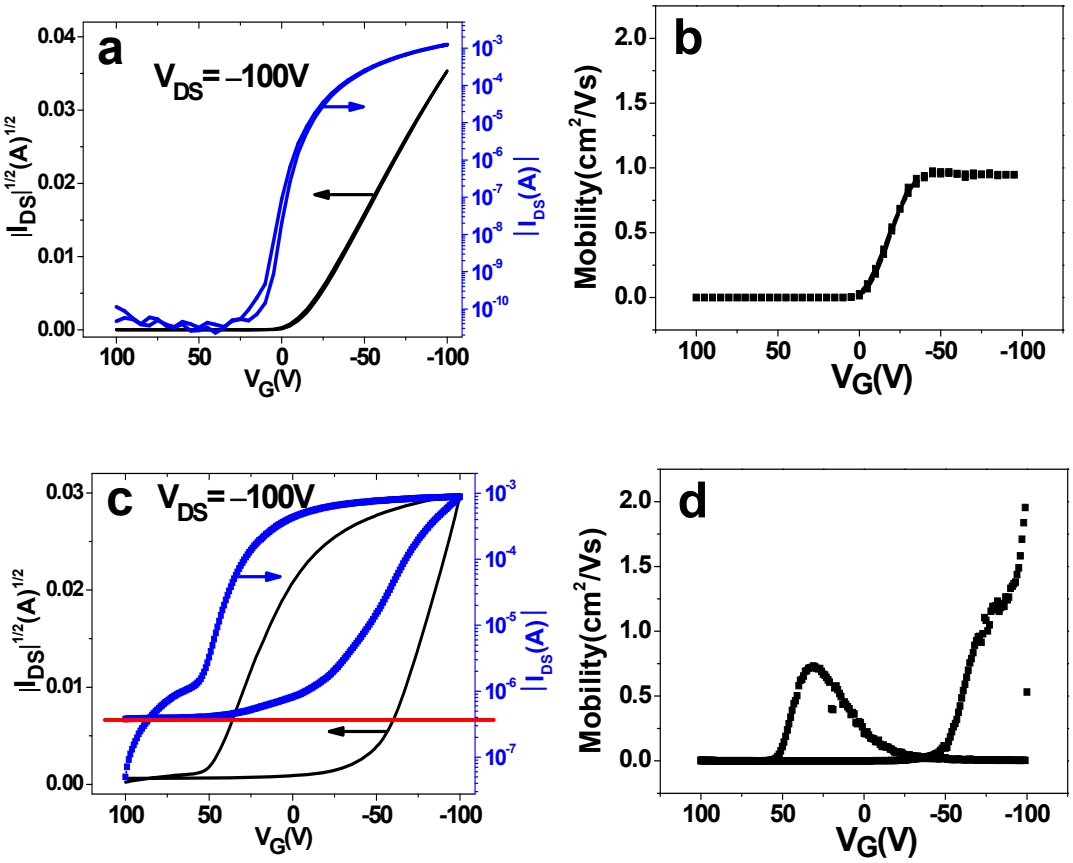


Figure S4. Transfer characteristics of a device based on pentacene on PMMA (a) $|I_{DS}|^{1/2}$ vs V_G characteristics, (b) mobility vs V_G characteristics. Transfer characteristics of a device based on pentacene on Ferrocene–PMMA (c) $|I_{DS}|^{1/2}$ vs V_G characteristics, (d) mobility vs V_G characteristics.

References

[S1]D. W. Li, E. J. Borkent, R. Nortrup, H. Moon, H. Katz, Z. N. Bao, *Appl. Phys. Lett.* **2005**, *86*.