(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
10 December 2009 (10.12.2009)

PCT

(10) International Publication Number
WO 2009/147401 A1

(51) International Patent Classification:
H03M 13/23 (2006.01)

(21) International Application Number:
PCT/GB2009/001406

(22) International Filing Date:
5 June 2009 (05.06.2009)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
0810241.0 5 June 2008 (05.06.2008) GB

(71) Applicant *(for all designated States except US)*: **THE UNIVERSITY OF READING** [GB/GB]; Whiteknights, P.O. Box 217, Reading, Berkshire RG6 6AH (GB).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **SHERRATT, Simon, R.** [GB/GB]; 4 Mannock Way, Woodley, Berkshire RG5 4XW (GB).

(74) Agent: **WILSON, Alan, Stuart**; Barker Brettell LLP, 138 Hagley Road, Edgbaston, Birmingham B16 9PW (GB).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

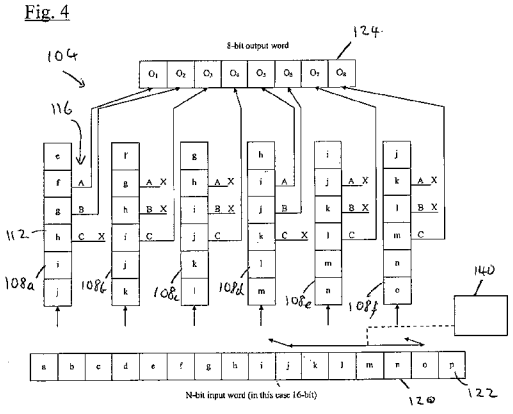
Published:

— *with international search report (Art. 21(3))*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

(54) Title: PARALLEL CONVOLUTIONAL CODER

Fig. 4



(57) Abstract: A parallel convolutional coder (104) comprising: a plurality of serial convolutional coders (108) each having a register with a plurality of memory cells and a plurality of serial coder outputs,- input means (120) from which data can be transferred in parallel into the registers,- and a parallel coder output (124) comprising a plurality of output memory cells each of which is connected to one of the serial coder outputs so that data can be transferred in parallel from all of the serial coders to the parallel coder output.

WO 2009/147401 A1

PARALLEL CONVOLUTIONAL CODER

Field of the Invention

The present invention relates to digital communication systems and in particular to covolutional coders for use in such systems.

Background to the Invention

In data communications, the data to be sent often travels over harsh environments which distort the signal and add noise. A receiver will also add its own thermal noise to the received signal. A convolutional coder accepts the original data bits to be sent and adds redundancy to the data so that, at the receiver, an estimate of the original data input to the encoder can be found even in the presence of noise. A convolutional decoder is required at the receiver; this is almost exclusively a Viterbi decoder, but can take other forms.

A convolutional coder is used in most digital communication systems including Wireless LAN (W-LAN and WiFi), digital television (DVB-T, DVB, ISDB), handheld devices (DVB-H, T-DMB), and Wireless-USB, but also in CD and DVD.

The convolutional coder has a number of interconnected memory elements each of which is in a particular state which changes each clock cycle. It works by accepting a steam of bits to be sent and, with the arrival of each bit, modifying the states of the coder memory elements with the new bit and feedback from the current states of the memory elements. There are also a number of output elements, the state of which depends on the states of the memory elements, and for each new bit input, a corresponding set of output bits is produced. Rather than a single bit, the coder may accept more bits at each step. If a coder accepts k bits in, and outputs n bits out, n must be > k, and the coder is said to be a k/n coder. In many systems

k/n is 1/2 or 1/3. This ratio is generally termed the mother code. The resulting bits are usually collected in series as A, B, C, ... and passed to a puncturing system.

The addition of redundancy in the coder means that the coded data is much larger than the original data before coding; therefore the transmitter would have more data to send. Since the receiver is capable of correcting for errors, and the additional bits are related to the original bits in a known way, it is possible to remove certain bits from the output of the coder and not send then, and use the error correcting capability of the decoder to estimate what the removed bits were. This process is termed puncturing. In the transmitter puncturing is performed after the coder, and in the receiver the opposite step of de-puncturing is performed before the decoder.

Puncturing reduces the number of bits that need to be sent, but also allows for a trade-off between speed and reliability as puncturing takes away some of the error correcting capability of the decoder.

Particular systems generally have variable puncturing levels. For example Wireless-USB ECMA-368 defines a mother code of 1/3, and by varying the puncturing various code rates are achieved, which can be selected at any time depending on the prevailing conditions:

1/3 rate, by doing no puncturing;
1/2 rate, by removing 1 bit of every 3 coded bits, therefore
1/3 * 3/2 = 1/2;
5/8 rate, by removing 7 bits of every 15 coded bits, therefore
1/3 * 15/8 = 5/8;
3/4 rate, by removing 5 bits of every 9 coded bits, therefore
1/3 * 9/4= 3/4.

The order of removal is very important to ensure that the transmitter and receiver are synchronised. The order will be referred to in more detail below.

As data rates get higher, we start to reach fundamental limits for the technology being used to deploy the system. For ECMA-368, various code rates are used for different data rates to achieve the same transmission rates.

For a data rate of 480Mbit/sec – 1/3 rate encodes 1440Mbit/sec, punctures down to an overall 3/4 coder, therefore data out of puncturing block is 640Mbit/sec.
For a data rate of 400Mbit/sec – 1/3 rate encodes 1200Mbit/sec, punctures down to an overall 5/8 coder, therefore data out of puncturing block is 640Mbit/sec.
For a data rate of 320Mbit/sec – 1/3 rate encodes 960Mbit/sec, punctures down to an overall 1/2 coder, therefore data out of puncturing block is 640Mbit/sec.

Considering that the latest Field Programmable Gate Arrays FPGA's are at best capable of clocking at just over 500MHz, then the above clock rates become an issue. It is possible to have a coder that at the same time punctures, thus having a maximum rate of 640MHz, but this rate is still very high.

Summary of the Invention

Accordingly the present invention provides a parallel convolutional coder comprising: a plurality of serial coders each having a register with a plurality of memory cells and a plurality of serial coder outputs; input means from which data can be transferred in parallel into the registers;

and a parallel coder output comprising a plurality of output memory cells each of which is connected to one of the serial coder outputs so that data can be transferred in parallel from all of the serial coders to the parallel coder output.

Preferred embodiments of the present invention will now be described by way of example only with reference to the accompanying drawings.

Brief Description of the Drawings

Figure 1 is a diagram of a serial convolutional coder forming part of an embodiment of the invention;

Figures 2a, 2b and 2c are diagrams illustrating different coding rates and puncturing orders which can be provided using embodiments of the invention;

Figure 3 is a diagram of part of a transmitter including a coder according to an embodiment of the invention;

Figure 4 is a diagram of a coder according to an embodiment of the invention;

Figure 5 is a diagram of a coder according to a further embodiment of the invention;

Figure 6 is a diagram of a coder according to a still further embodiment of the invention;

Figure 7 is a diagram of a coder according to a further embodiment of the invention; and

Figure 8 is a schematic diagram of a transmitter according to a further embodiment of the invention.

Description of the Preferred Embodiments

Referring to Figure 1 a serial convolutional coder 8 which forms part of various embodiments of the invention comprises an input 10 and a shift register comprising a series of memory elements 12a, 12b, 12c, 12d, 12e, 12f. The input is connected to the first memory element 12a so that input data is entered into the first memory element 12a, and the other memory elements are connected together so that the data is forwarded from each one to the next along the series at each clock pulse. A network of EXOR gates 14 are connected between the memory elements 12 and three outputs 16, which are labelled output A, output B and output C. The output bit at each of the outputs therefore changes with each clock pulse, i.e. with each new bit arriving at the input, and is dependent on the contents of several of the memory elements 12, and therefore on a number of consecutive bits in the input bit stream. This coder is a 1/3 coder, and coders with other mother codes operate in a similar manner.

If puncturing is to be applied to the output of the coder 8, then different puncturing structures can be used depending on the degree of puncturing that is required. In embodiments of the invention puncturing and coding can be performed simultaneously, but they will be referred to here as separate steps as that is how they are conventionally performed. Referring to Figure 2a, if an overall rate of the coder and puncturing is to be a 1/2 rate, then one of each group of three output bits needs to be removed by the puncturing, which can be the bit produced at output B. Therefore for each input bit x_0, the coder 8 produces 3 output bits A_0, B_0 and C_0. The puncturing then removes the second of these bits B_0 so that the punctured data includes just two of the bits A_0 and C_0. This is the data that is

transmitted. In the receiver, the two bits A_0 and C_0 are received. The de-puncturing inserts a dummy bit which is an estimate of the original bit B_0 to reconstruct the coded data. The de-coder then decides the coded data stream to determine the original data bit y_0. In embodiments of this invention, several coders each providing a ½ rate can be arranged to operate in parallel as will be described in more detail below.

Referring to Figure 2b, if an overall rate of 5/8 is required, then five consecutive input bits x_0 to x_4 can be input in parallel to five serial coders, with each of the five serial coders producing a group of three output bits A_0 B_0 C_0 for the first serial coder, A_1 B_1 C_1 for the second coder etc. This coded data can then be punctured by removing one bit from three of the groups and two bits from each of the other two groups as shown, leaving eight bits which are used to produce the punctured data stream for transmission. Again, in the receiver, the de-puncturing re-inserts estimated values of the removed bits, and the original data is decoded from the de-punctured data.

Referring to Figure 2c, of an overall rate of 3/4 is required, three consecutive input bits x_1 x_2 x_3 are input in parallel to three serial coders to produce three groups of three bits. This encoded data is then punctured to reduce the nine bits to four bits in the punctured data stream for transmission. The de-puncturing and de-coding is performed in a similar manner.

Referring to Figure 3, a transmitter according to an embodiment of the invention comprises a memory device 100, a parallel side stream scrambler 102 and a parallel convolutional coder 104. A control system is arranged to fetched data from the memory device 100 in words of N bits, in this case N being 16, and input them to the parallel side stream scrambler 102. The scrambler 102 is arranged to scramble the input data

and output it as scrambled data, again in words of N bits. The scrambled data forms the input to the coder 104 which is arranged to output coded and punctured data in words, in this case, of eight bits. Since the coding process increases the number of bits, the coder 104 has to output more than one word for each input word it receives.

Referring to Figure 4, the coder 104 in this embodiment is a parallel ¾ coder and comprises six serial coders 108a, 108b, 108c, 108d, 108e, 108f each of which is essentially the same as the coder 8 of Figure 1 including six memory elements 112 and three outputs 116. The network of EXOR gates between the memory elements 112 and the outputs 116 are present in each serial coder, but omitted from Figure 4 for simplicity. The coder 104 also comprises an input register 120 comprising 16 memory cells 122 into which the input data can be loaded and an output register 124 comprising eight memory cells 126 in which the coder output is held for outputting in parallel as an eight-bit word with bits O_1 to O_8. In other embodiments, the input and output registers can have different sizes, for example the input word could be 32 bits and the output word 16 bits.

Rather than use all of the three outputs A, B, C from each of the serial coders 108a - 108f, in order to perform the equivalent of coding and puncturing at the same time, only eight of the total of 18 outputs are connected to the output register 124. For example, as shown, outputs A and B from the first serial coder 108a are connected to the first and second memory cells in the output register 124 to provide output bits O_1 and O_2, while output C from the first serial coder 108a is not connected to the output register. Only output C from the second coder 108b is input to the output register 124 to provide output bit O_3, as are output C from the third coder 108c to provide output bit O_4, outputs A and B from the fourth coder 108d to provide output bits O_5 and O_6, and output C from

each of the fifth and sixth coders 108e, 108f to provide output bits O_7 and O_8.

It will be seen that the coder of Figure 4 employs the puncturing structure of figure 2c, and codes 6 bits directly into 8 bits (i.e. 6/8 = 3/4 directly computed) using 6 registers of 6 bits each, all in one clock cycle.

In operation the 16 bit word is loaded into the input register 120, and the selected 6 input bits (in this case j..o) are taken from the input register 120 and each input to the start of a respective one of the shift registers. The loading of data into the registers is controlled by an input control system 140 which will be described in more detail below. As in the structure of Figure 2c, the outputs A and B from the first serial coder are used for the first code operation, then only C and then only C, with this code repeated thus we take outputs A_1, B_1, C_2, C_3, A_4, B_4, C_5, C_6 into the 8 bit output word, where A_1 is the A output from the first serial coder etc.. It must be understood that as in Figure 1, previous bits must be allowed to propagate from the start to the end of the short registers, hence bits previous to the current input are present in the registers and affect the outputs A, B, C.

When the coder starts, all the registers will be cleared to 0. The N-bit input word is applied and the first 6 bits are used (a..f) with a being placed into the bottom of register 1 (108a), a being in the second to bottom and b being in the bottom of register 2 (108b), so that each register holds six bits from the input sequence, with each register being one bit ahead in the sequence compared to the previous register. This results in a diagonal structure of stored data, with the bit in each element of each register being the same as the bit in the previous element in the adjacent register. With the encoding of each block of 6 input bits the registers effectively all advance by 6 ready for the next block of 6 bits in

the input word. Therefore at each step, the bit in the first element of the last register 108f moves to the second element in the first register, the third element in the second register, the fourth element in the fifth register etc.

As can be seen all the above operation can be done in one clock cycle all at the same time with the input control system 140 changing the content of each cell in each register to move it on along the input word by a number of places equal to the number of registers, in this case six. Only one clock is needed for the general operation as 6 bits are coded to 8, but the arrival of the N-bit input word must be correct.

It will be appreciated that, with six bits being taken from the input register at each step, after two steps there will only be four bits left in the input register to input to the serial coders 108a-f. Therefore the input control system 140 acts as a buffer between the input register and the serial coders 108a-f. At each clock cycle the input control system has two possible operations depending on whether there are six new bits in the input register to be input to the serial coders 108a-f. If there are, then those bits are input into the serial coders 108a-f. If there are less than six new bits then the input control system 140 stores the remaining bits from the word currently in the input register, then waits for the next 16 bit word to be loaded into the input register, and takes sufficient bits from the beginning of the new word to make up, together with the stored bits, a total of six bits. These six stored bits are then used to update the serial codes and shift them forward another stage of six places. It will be seen that the system will operate in cycles of three input words, the first of which will have its last four bits combined with the first two bits of the second word, the second will have its last two bits combined with the first four bits of the third word, leaving twelve bits from the third word to complete the cycle. As this cycle will be repeated, the input control

system can be set up to simply run through this cycle on a repeating basis. It will be appreciated that the rate at which words are entered into the input register will be lower than the clock rate at which the parallel coder operates.

The action of the coder 8 is to only use a sub-set of the data presented at its input, and code that sub-set in parallel creating a set of coded bits all at the same time.

Referring to Figure 5, a coder according to a further embodiment of the invention is constructed on the same principles as that of Figure 4, but in this case is arranged to provide an overall coding rate of 5/8. The input register 220 and output register 224 again have 16 and 8 memory elements respectively. In this case there are only five serial coders 208a - 208e. To correspond with the puncturing structure of Figure 2b, outputs A and B from each of the first coder 108a, the third coder 108c and the fifth coder 108e, and output C from coders 108b and 108d are input to the output register 224, with the output bits in the output word being taken from the serial coders in order of first 108a to fifth 108b, and in order A to C from the outputs of each coder. In this case, only five bits are taken from the input register at each clock cycle and each of the registers is moved on by five places at each clock cycle.

Referring to Figure 6, a parallel coder according to a further embodiment of the invention is arranged to provide a 1/2 rate, and is again constructed on the same basis as the parallel coder of Figure 4. In this case there are four serial coders 308a-308d, a sixteen bit input register 320 from which bits are taken in groups of four to input to the serial coders, and an output register 324 of eight bits. In this case the outputs A, B, C, from the four coders 308a-308d are connected to the output register 324 so as to mirror the puncturing structure of Figure 2a, with the eight output bits

taken in order from outputs A and C of the four serial coders 308a in order. The shift registers are moved on four places at each coding step.

Referring to Figure 7, in a further embodiment of the invention a single parallel convolutional coder is structured in a similar manner to that of Figure 4 with input register 420, output register 424 and six serial coders 408a-408f. However, in this case the coder is re-configurable so as to operate in the same way as any one of the coders of Figures 4 to 6. to achieve this each of the outputs A, B, C, from each of the serial coders 408a-408f is connected via a switch 450 to each of the output register elements 426 that it needs to be connected to for any one of the three configurations. In this case only serial coders 408a to 408e are used for the configuration of Figure 5, and serial coders 408a to 408d are used for the configuration of Figure 6. For example, output A from the first serial coder 408a is connected via a switch 450 to output element O_1 output B from the first serial coder 408a is connected via a switch to output element O_2 output C from the first serial coder 408a is connected via a switch to output element O_2. Some of the outputs are connected to two of the output elements, for example output C from the second serial coder is connected by switches to output element O_3 as that is required for the configuration of Figure 5 and by a separate switch to output element O_4 as that is required for the configuration of figure 6. Only the connections for the first serial coder 408a are shown in Figure 7 for simplicity. A switch control system 452 is arranged to control all of the switches 450 so that the coder can be switched between the three configurations to provide different coding rates as required. Similarly the input control system 440 is operable in three modes to transfer bits from the input register 420 in groups of six, five or four to the appropriate group of serial coders 408 which are being used for the current configuration.

Referring to Figure 8, in a further embodiment of the invention a transmitter comprises a memory device 500 and a parallel scrambler 502, and three separate parallel convolutional coders 504, 505, 506. One of these is a 3/4 coder of Figure 4, one is a 5/8 coder of Figure 5 and one is a 1/2 coder of Figure 6. A controller 560 is arranged to control operation of the transmitter, and is arranged to switch the output of the scrambler 502 to one of the coders 504, 505, 506, so that the most appropriate coder can be selected in any particular circumstances. Since each of the coders is arranged to receive data into its input register in words of the same length, and to output data in words of the same length, switching between the three coders is a simple operation. Furthermore, because all of the coders are made up of the same basic components: the same basic serial coder units, the same input and the same output, the manufacture of a transmitter having the three coders on it is relatively simple.

The embodiments described have a number of advantages over known systems. Having a two-stage process of coding and puncturing is wasteful as data that is not needed is calculated, and this is avoided with the one stage coding and puncturing of these embodiments. Also the output rate of the parallel convolutional coder is much lower than the conventional convolutional coder. This is important as electrical power dissipation increases as the switching rate increases; thus it is advantageous to keep the rates as low as possible.

Claims

1. A parallel convolutional coder comprising: a plurality of serial coders each having a register with a plurality of memory cells and a plurality of serial coder outputs; input means from which data can be transferred in parallel into the registers; and a parallel coder output comprising a plurality of output memory cells each of which is connected to one of the serial coder outputs so that data can be transferred in parallel from all of the serial coders to the parallel coder output.

2. A coder according to claim 1 wherein each parallel coder output cell is connected to a different one of the serial coder outputs.

3. A coder according to claim 1 or claim 2 wherein there are fewer output memory cells than serial coder outputs and data from some of the serial coder outputs is not transferred to the parallel coder output.

4. A coder according to any foregoing claim wherein each of the serial coders further comprises a network of components connecting the register to the outputs.

5. A coder according to any foregoing claim wherein all of the serial coders are identical to each other.

6. A coder according to any foregoing claim wherein the input means comprises a plurality of input memory cells and input control means arranged to transfer data from the memory cells in parallel to the registers.

7. A coder according to claim 6 wherein the input control means is arranged to input data to the registers in cycles wherein, in each cycle,

each of the registers is moved on by a number of steps equal to the number of serial coders.

8. A coder according to claim 6 or claim 7 wherein there are a greater number of input memory cells than registers.

9. A coder according to any foregoing claim further comprising control means arranged to control the loading of data into the input means so that new data is only loaded into the input means when all of the data currently in the input means has been input to the serial coders.

10. A coder according to any foregoing claim wherein switching means is provided to alter which of the serial coder outputs is connected to which of the output memory cells, so that the code rate of the coder can be altered.

11. A coder according to claim 10 wherein the switch means is arranged to vary the number of the serial coders of which any outputs are connected to the output memory cells.

12. A coder according to claim 11 wherein transfer means is provided to transfer data from the input to the registers, and the transfer means is arranged to alter the number of the registers to which data is input.

13. A transmitter comprising a plurality of parallel convolutional coders each of which is a coder according to any foregoing claim.

14. A transmitter according to claim 13 wherein the parallel convolutional coders are arranged to have different code rates, the

transmitter further comprising control means arranged to select one of the coders depending on the code rate required.

15. A transmitter according to claim 14 wherein all of the coders have parallel coder outputs with the same number of memory cells.

16. A transmitter according to claim 14 or claim 15 wherein all of the coders have input registers with the same size.

Fig. 1

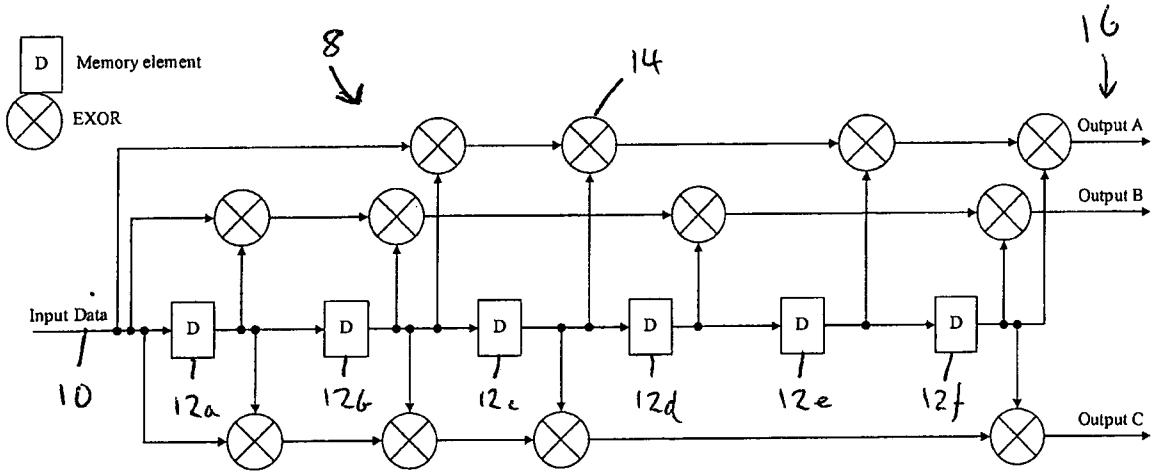

D
Memory element
EXOR
8
14
16
Output A
Output B
Output C
Input Data
10
D
12a
12b
12c
12d
12e
12f

Fig. 2a

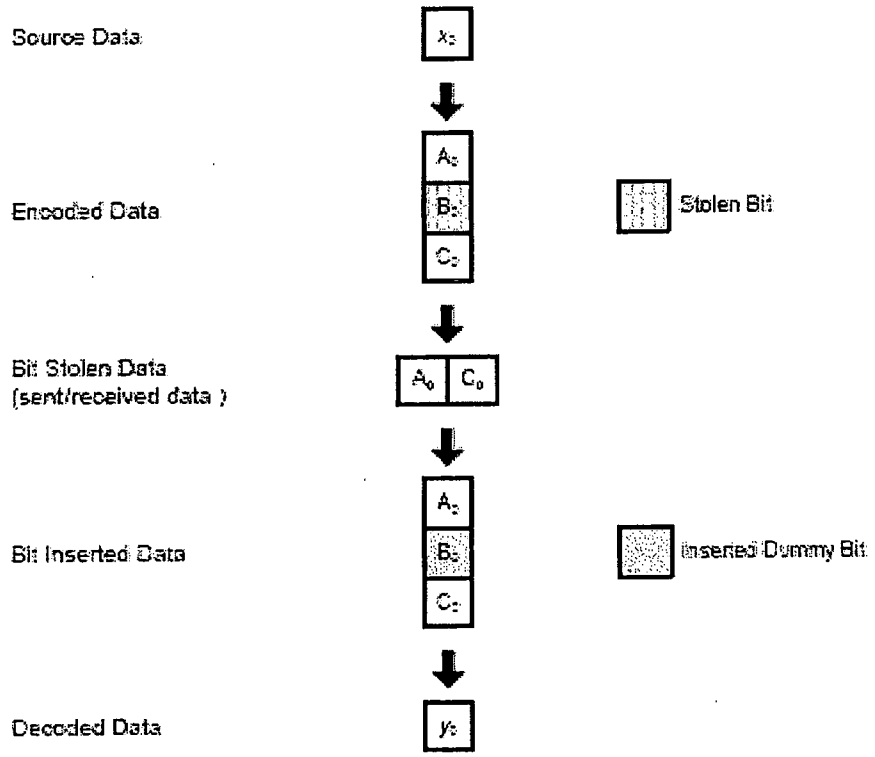

Source Data
Encoded Data
Bit Stolen Data
(sent/received data)
Bit Inserted Data
Decoded Data
Stolen Bit
Inserted Dummy Bit

Fig. 2b

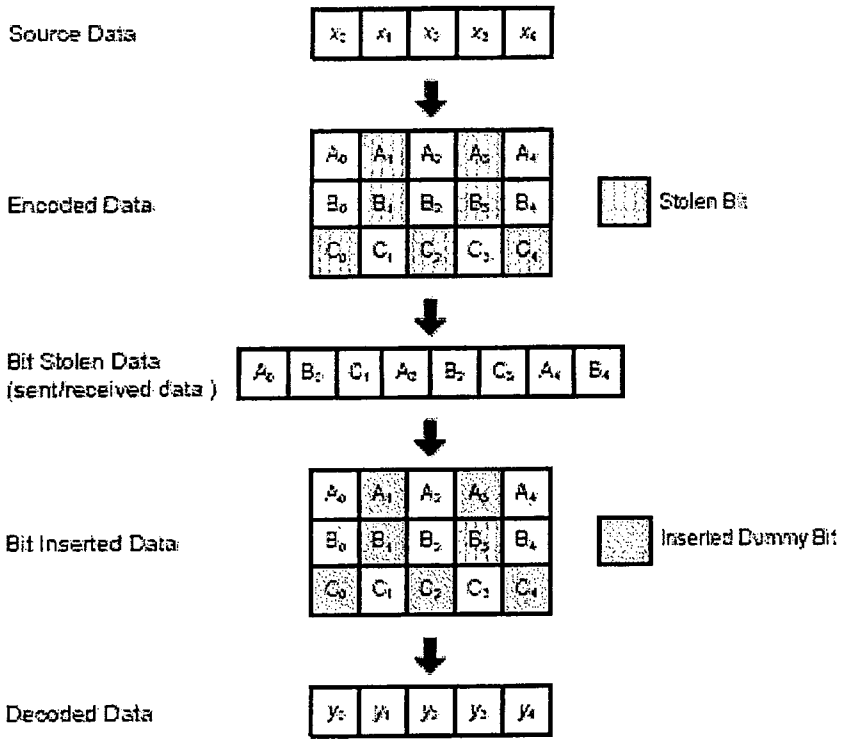

Source Data
Encoded Data
Stolen Bit
Bit Stolen Data
(sent/received data)
Bit Inserted Data
Inserted Dummy Bit
Decoded Data

Fig. 2c

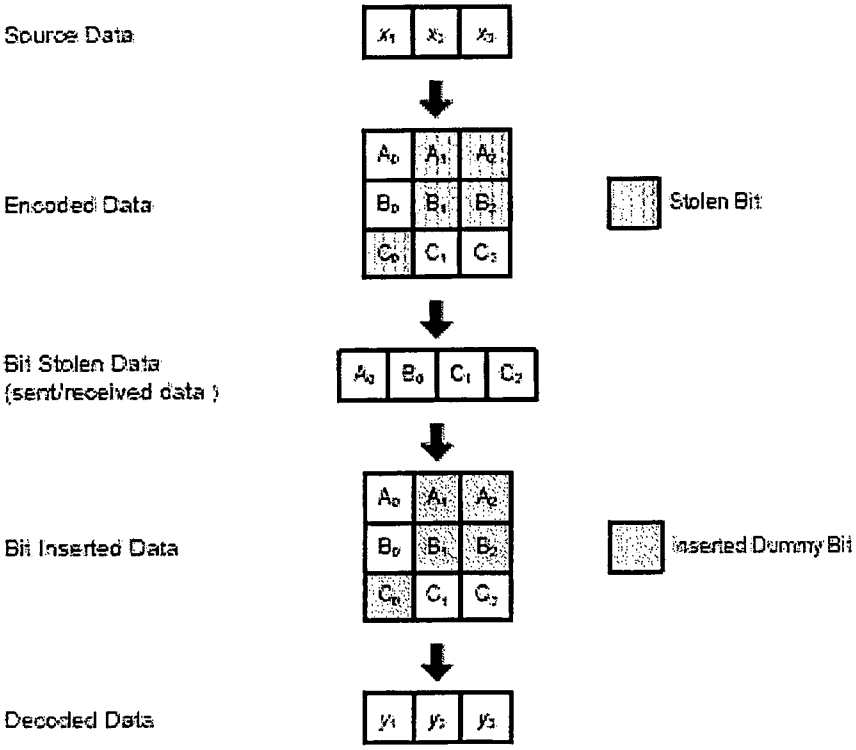

Source Data
Encoded Data
Stolen Bit
Bit Stolen Data
(sent/received data)
Bit Inserted Data
Inserted Dummy Bit
Decoded Data

Fig. 3

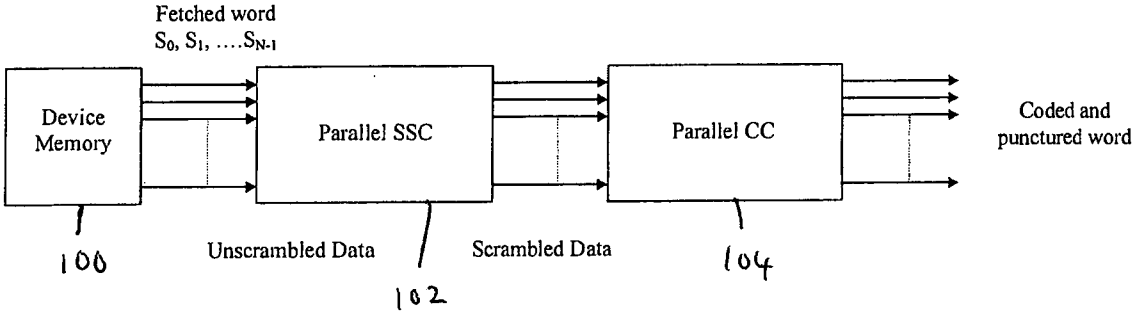

Fetched word
$S_0, S_1, \ldots S_{N-1}$
Device Memory
Parallel SSC
Parallel CC
Coded and punctured word
100
Unscrambled Data
102
Scrambled Data
104

Fig. 4

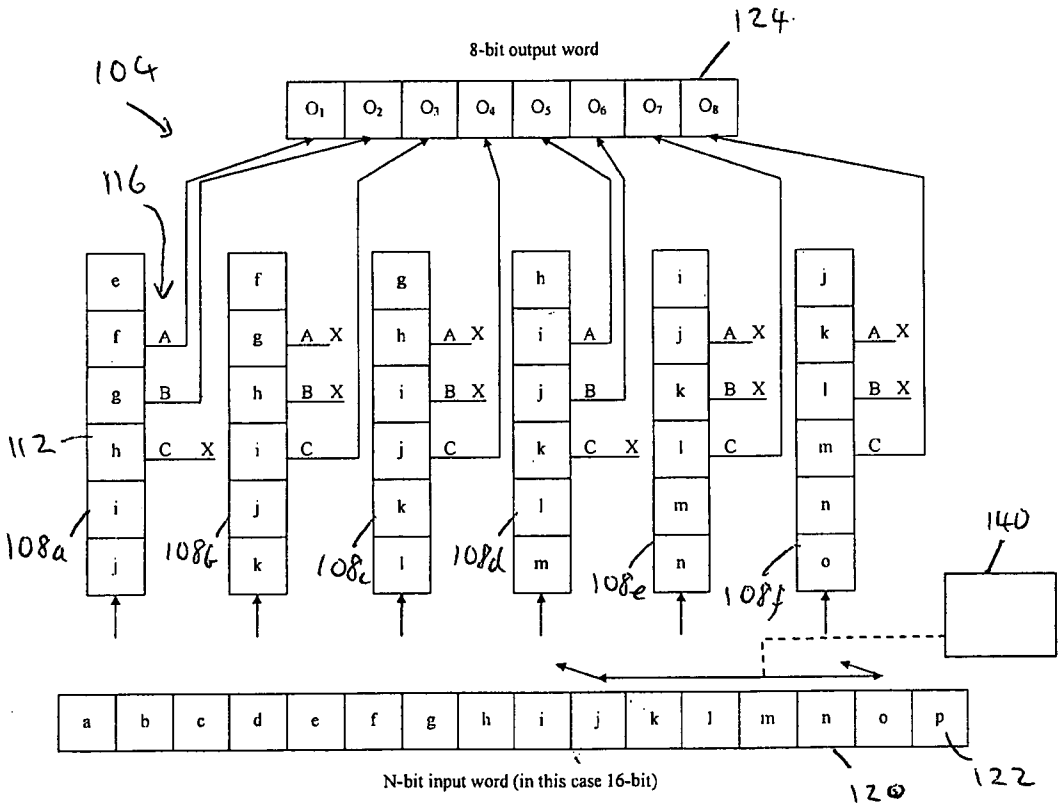

124
8-bit output word
O_1 O_2 O_3 O_4 O_5 O_6 O_7 O_8
104
116
112
108a
108b
108c
108d
108e
108f
140
a b c d e f g h i j k l m n o p
N-bit input word (in this case 16-bit)
120
122

Fig. 5

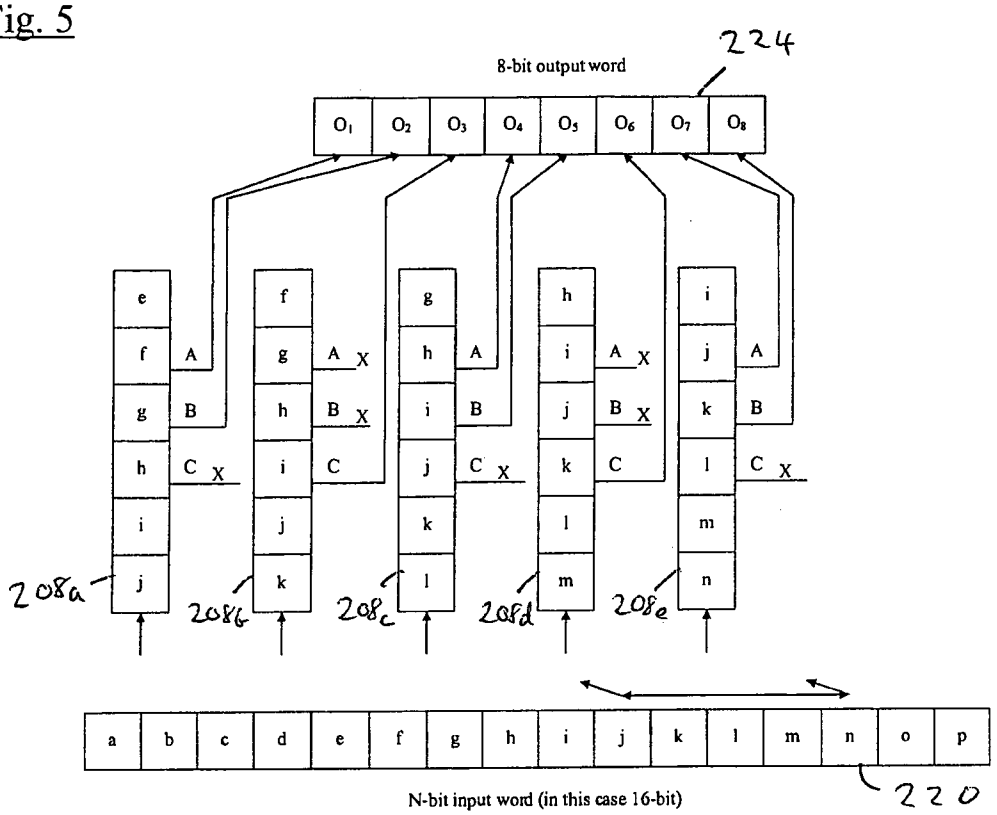

224
8-bit output word
O1 O2 O3 O4 O5 O6 O7 O8
208a
208b
208c
208d
208e
a b c d e f g h i j k l m n o p
220
N-bit input word (in this case 16-bit)

Fig. 6

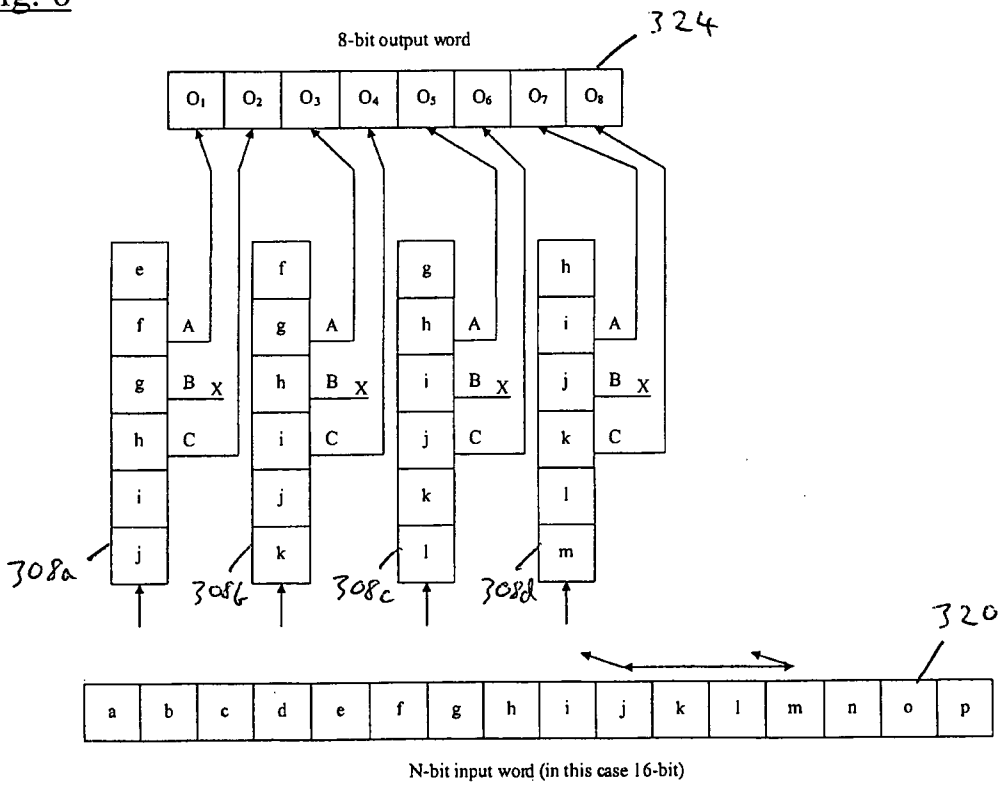

324
8-bit output word
O1 O2 O3 O4 O5 O6 O7 O8
308a
308b
308c
308d
320
a b c d e f g h i j k l m n o p
N-bit input word (in this case 16-bit)

Fig. 7

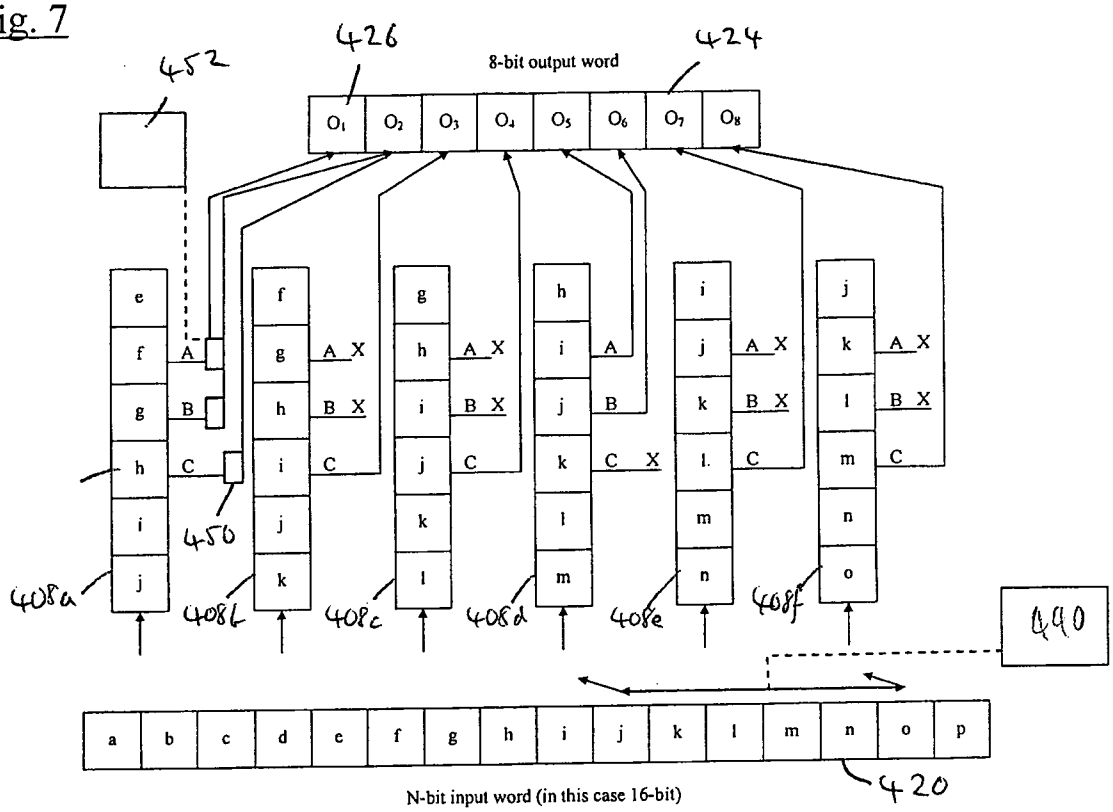
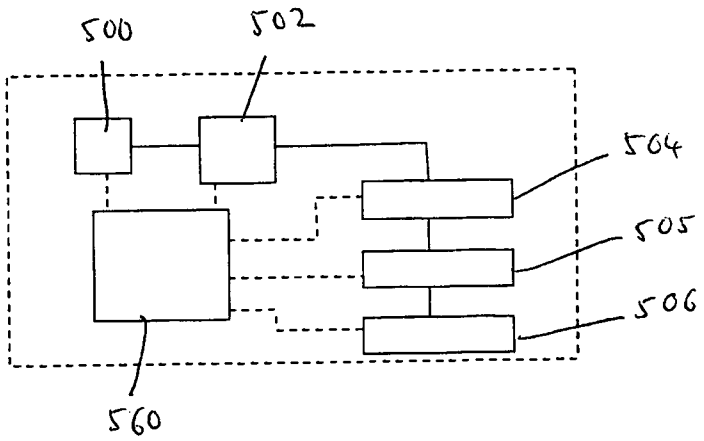


Fig. 8



INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2009/001406

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03M13/23

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, COMPENDEX, INSPEC, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	AHMED O EL-RAYIS; TUGHRUL ARSLAN; AHMET T ERDOGAN ED - ROB BAXTER; STEPHEN BOOTH; MARK BULL; GEOFF CAWOOD; KENTON D'MELLOW; XU GU: "High Performance Embedded Reconfigurable Concatenated ConvolutionPuncturing Fabric for 802.16" SECOND NASA/ESA CONFERENCE ON ADAPTIVE HARDWARE AND SYSTEMS, AHS 2007, IEEE, PISCATAWAY, NJ, USA, 1 August 2007 (2007-08-01), pages 190-194, XP031128147	1,4-6, 8-12
A	page 191 - page 192; figures 3-5	2-3,7, 13-16

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an orat disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular retevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a persen skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 September 2009	05/10/2009

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Burkert, Frank

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2009/001406

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	MSIR A; MONTEIRO F; DANDACHE A; LEPLEY B: "Design of a high speed parallel encoder for convolutional codes" MICROELECTRONICS JOURNAL, MACKINTOSH PUBLICATIONS LTD. LUTON, GB, vol. 35, no. 2, 1 February 2004 (2004-02-01), pages 151-166, XP002522779 ISSN: 0026-2692 [retrieved on 2003-12-02]	1,4-6,9
A	figure 11	2-3,7-8, 10-16
X	HACCOUN D; LAVOIE P; SAVARIA Y: "NEW ARCHITECTURES FOR FAST CONVOLUTIONAL ENCODERS AND THRESHOLD DECODERS" IEEE JOURNAL ON SELECTED AREAS IN COMMUNICATIONS, IEEE SERVICE CENTER, PISCATAWAY, US, vol. 6, no. 3, 1 April 1998 (1998-04-01), pages 547-557, XP000879638 ISSN: 0733-8716	1,4,6,9
A	figure 6	2-3,7-8, 10-16
A	GB 2 380 370 A (MOTOROLA INC [US]) 2 April 2003 (2003-04-02) abstract page 17, line 18 - page 20, line 25 figures 5,6	1-16
A	US 2004/210618 A1 (STEIN YOSEF [US]; PRIMO HAIM [IL]) 21 October 2004 (2004-10-21) the whole document	1-16
A	US 2004/025104 A1 (AMER MAHER [CA]) 5 February 2004 (2004-02-05) the whole document	1-16

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/GB2009/001406

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
GB 2380370 A	02-04-2003	US 2003074627 A1	17-04-2003
US 2004210618 A1	21-10-2004	EP 1611494 A2	04-01-2006
		JP 4037897 B2	23-01-2008
		JP 2006526904 T	24-11-2006
		TW 244034 B	21-11-2005
		WO 2004092873 A2	28-10-2004
US 2004025104 A1	05-02-2004	AU 2003249822 A1	23-02-2004
		WO 2004013974 A2	12-02-2004
		JP 4292298 B2	08-07-2009
		JP 2005535190 T	17-11-2005
		KR 20050045996 A	17-05-2005
		US 2008092023 A1	17-04-2008