DSPWM Multilevel Technique of 27-Levels based on FPGA for the Cascaded DC/AC Power Converter Operation

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***Abstract*—** In this paper a Digital Sinusoidal Pulse Width Modulation (DSPWM) multilevel technique of 27-levels based on FPGA is introduced, as an alternative to control of the DC/AC multilevel power converters. The implementation of this technique with a Field Programmable Gate Array (FPGA) XC3S500E model is achieved in the Xilinx Spartan 3E-FPGA platforms. An experimental prototype is implemented by three-cascaded H-bridges controlled by the DSPWM multilevel technique, generating high efficiency, low cost and lower harmonic content. The efficiency of the DSPWM multilevel technique using R, RL, RC and RLC loads connected to the power network is verified.

***Keywords*—**DSPWM, FPGA, multilevel H-bridges, cascaded DC/AC converters.

I. INTRODUCTION

Through the years, the research attention in the DC/AC multilevel power converters controlled by Pulse Width Modulation (PWM) has increased, in merit to identify technical advantages in the power quality problems solution [1]. Among the different types of multilevel topologies of the DC/AC power converters, three are considered, i.e. Diode-clamped, flying capacitor and cascaded H-bridge [2]. Then, when the multilevel signal implementation is required with a low harmonic content, the cascaded H-bridge topology is used. This topology appeared for the first time in 1975 [3] and this is mainly implemented because it is possible to generate a greater number of levels with a lesser number of switches and electronic components [4-5]. Subsequently, the Total Harmonic Content (THD) is lower among the number of levels

containing a sinusoidal signal [6-7]. In addition, the series connection of multilevel power converters reduces the voltage stress of each switch in the H-bridge module, making DC/AC multilevel converters suitable for high power applications.

Several types of modulation methods have been proposed for multilevel converters based on two approaches, i.e. Pulse Width Modulation (PWM) and Vector Modulation (VM). The vector modulation method generates the converter commutation states from a reference vector, its implementation is more complex and it is more computationally demanding, as this technique requires the coding of N^3 different voltage combinations for the output voltage generation of N-levels [8]. The pulse width modulation is generated by the comparison of modulated and carrier signals. In the multilevel signal generation, several carriers are used; its advantage is the implementation simplicity and low computational cost, because to generate a multilevel signal of n-levels, it is only necessary the comparison between a modulated signal and n-1 carriers [9].

To achieve this aim, the DC/AC multilevel converters control has been progressively migrated from analog to digital operation [10], i.e. the digital modulation techniques are quickly becoming the most generalized framework in modern power electronics applications. Digital Sinusoidal Pulse Width Modulation (DSPWM) is a modulation technique created by the internal generation of the modulated and carrier signals in a digital controller. Hence, different digital controllers, such as microprocessors, Digital Signal Processor (DSP), Application Specific Integrated Circuits (ASIC) and Field Programmable Gate Array (FPGA) are gaining importance in power electronics applications [11], as these allow the DSPWM to be implemented easily with advantages in terms of better performance, reduction of harmonic distortion and low cost of experimental prototypes. However, the operation of some digital controllers is linked to disadvantageous issues, e.g. the use of ASICs is sometimes an effective solution in applications designed for large markets, since its development cost is only justified by large volumes. In DSPs the execution time synchronization is complex and in microcontrollers the generation of multiple output signals is insufficient [12-13].

The importance of developing digital controllers in low-level programming devices (direct control over hardware), such as FPGAs, in the control of switching power converters, remains in the concurrency advantages (it allows the division of complex logical algorithms in a large number of small tasks, which are simultaneously solved) [14-17]; i.e. it is possible the control of multiple switches with high processing speed. This is ideal when a very high switching frequency and bandwidth are required. At the same time, the FPGA is dynamically and partially re-configurable, a fact that can be exploited in order to reduce the total power consumption. The hardware re-configuration allows the constantly non-required functions to be stored in a low power memory and these with the predefined register in the FPGA are configured [18]. Besides, the VHDL (combination between VHSIC (Very High Speed Integrated Circuits) and HDL (Hardware Description Language)) is designed and optimized to describe the behavior of digital systems; which ranges from simple logic gates to custom chips [19]. When the VHDL language is combined with the characteristics of an FPGA as, concurrency and re-configuration, it allows

feasible and efficient implementations of DSPWM control, in merit to its flexibility, versatility and simplicity properties [20].

The DSPWM multilevel technique can be applied in some research works, such as: In [21-23], research investigation on cascaded H-bridge multilevel converters of 27-levels controlled by DSPs is reported, thus generating a complex synchronization of execution time and an excess of unnecessary software, due to the DSP serial programming process**.** In [24], a DC/AC multilevel converter topology that gets all the additive and subtractive combinations of the input DC levels in a real-time simulator is proposed. However, the authors present the multilevel topology simulation generating of 9 and 27-levels, but only an experimental prototype to generate 9-levels is implemented; which is acceptable but not enough, since the control strategy to generate 27-levels through the proposed topology is not detailed. In [25], the control of cascaded H-bridge in a photovoltaic system based on sinusoidal PWM techniques through an FPGA is reported. This is a potential application; however, the authors only report the system simulation. In [26], the control of a voltage source inverter with multilevel technique is performed using the Space Vector Pulse Width Modulation (SVPWM) technique in an FPGA; nevertheless, the authors generate only a 5-levels multilevel signal, which generates a higher Total Harmonic Distortion (THD) in the AC network. To reduce this THD, the number of levels in the output voltage must be increased; this results in an increase of unnecessary software.

In this paper, a DSPWM multilevel technique of 27-levels based on the Xilinx Spartan 3E FPGA platform (XC3S500E model) is implemented, as an alternative of control to a DC/AC multilevel power converter formed by three-cascaded H-bridges, for the THD reduction in different load types. The paper scope is enhanced with the incorporation of R, RL, RC and RLC loads in the power system. Through the parallel data processing of the FPGA architecture a good resolution, high efficiency, low harmonic content and low cost are acquired in the prototype implementation. The paper organization is as follows: in Section II, the technical implementation of the DSPWM multilevel signal of 27-levels is detailed; in Section III, the DSPWM multilevel signal simulation of 27-levels is presented; in Section IV, the results of the prototype implementation detailed in Section II are given and analyzed, and finally in Section IV, the main conclusions of this research work are drawn.

II. Digital Sinusoidal Pulse Width Modulation (DSPWM) Multilevel Technique Description

Different types of multilevel modulation methods are already well established. The Phase Shifted PWM (PSPWM), Phase Disposition PWM (PDPWM), Phase Opposition Disposition PWM (PODPWM) and Selective Harmonic Elimination PWM (SHEPWM) are some examples of sinusoidal Pulse Width Modulation methods. The PSPWM, PDOWM and PODPWM multilevel methods in the power converters controlled with high frequency switching are applied; The SHEPWM technique is applied in converters with very high power, controlled through low frequency switching algorithms [27-29]. In this paper, the DSPWM implementation is made based on the phase disposition method, since this modulation method achieves a lower THD with a higher number of voltage levels in the output signal, in comparison to the methods cited in [30].

The DSPWM generation signal is achieved through direct comparison of a sinusoidal reference signal (modulating signal) and a high frequency triangular signal (carrier signal).

The DSPWM multilevel generation is represented by the expression:

$$nL = n - 1 \tag{1}$$

where n is the number of levels. The modulation index m_a is generated from the carrier signal frequency f_c and the modulating signal frequency f_m is,

$$m_a = \frac{f_C}{f_m} \tag{2}$$

Its function is to reduce stress on the converter switching devices due to high power handling. This is achieved by properly executing the gating signals for the switches control. These modulation techniques need more computational capacity; this requirement is satisfied when the modulation technique in a FPGA is implemented.

A. Modulated Signal Formation

The modulation signal has a frequency of 60Hz; it is created by the data stored in ROM, corresponding to the sinusoidal signal peak-to-peak amplitude. This amount of data has been selected for high precision of the modulation signal. Table 3 shows the stored content in ROM.

An array of 500 locations in the ROM is selected from Table 1. The FPGA model XC3S500E operates at 50MHz, since a sinusoidal modulation signal of 60Hz is needed, then this frequency is decreased. The base modulation signal frequency f_{BMS} is obtained as,

$$f_{BMS} = \frac{f_{FPGA}}{f_{SMS}} \tag{3}$$

where f_{FPGA} is the frequency to operate the FPGA model XC3S500E and f_{SMS} is the frequency of the sinusoidal modulation signal.

Finally, the 500 data store in ROM are assigned by the base modulation signal frequency as,

$$f_{DS} = \frac{f_{BMS}}{500} \tag{4}$$

where f_{BMS} is the base modulation signal frequency and f_{DS} is the frequency of stored data in ROM.

Table 2 shows the process to generate the base modulated signal frequency; this is achieved with f_{DS} by using a counting process of 1666 clock cycles. Table 3 details the process followed to select the 500 ROM locations. In Table 4, the process of value assignation in the corresponding ROM locations to generate the sinusoidal signal is shown. The described tasks in Tables 2, 3 and 4 are simultaneously processed by the FPGA. The stored data in ROM are continuously assigned every 1666 clock cycles. Therefore, the advantages of simplicity, efficiency, versatility and flexibility are achieved.

B. Carrier Signals Formation

Triangular carriers were synthesized using the master clock pulses of the FPGA, which may run at 50MHz. The carrier signal frequency is 10 times higher than the modulating signal frequency; therefore, the signal carrier frequency f_{SC} is obtained as,

$$f_{SC} = \frac{f_{FPGA}}{\left(f_{DS}\right) * 10} \tag{5}$$

where f_{FPGA} is the frequency to operate the FPGA model XC3S500E and f_{DS} is the 500 data stores in ROM.

Table 5 shows the process to generate the carrier signal base frequency by (4) and (5). By increasing its level to a maximum T the main triangular waveform (carrier) is generated, and then decreasing it to zero following a stair pattern. This sequence is continuously repeated until the overall process stops, as shown in Table 6.

$$\begin{aligned}
&Carrier \\
&Carrier + 350 \rightarrow Carrier\left(1\right) \\
&Carrier + 700 \rightarrow Carrier\left(2\right) \\
&Carrier + 1050 \rightarrow Carrier\left(3\right) \\
&\cdot \\
&\cdot \\
&\cdot \\
&Carrier + 8050 \rightarrow Carrier\left(24\right) \\
&Carrier + 8400 \rightarrow Carrier\left(25\right) \\
&Carrier + 8750 \rightarrow Carrier\left(26\right)
\end{aligned} \tag{6}$$

To form each of the remaining triangular signals, an offset is added to the main triangular signal until reaching the peak value, as shown in (6). The modulating signal and the sum of n carrier signals must have the same peak-to-peak amplitude. Finally, the sinusoidal modulation signal is continuously compared against each of the n carrier signals, generating a train of on-to-off switching pulses. That is, if the reference is larger than n carrier signals, then the pulse is active, but if the reference is smaller than n carrier signals, then the pulse is turned off, i.e.:

$$Modulated > Carrier\left(n\right) \rightarrow DSPWM = 1 \tag{7a}$$

$$Modulated < Carrier\left(n\right) \rightarrow DSPWM = 0 \tag{7b}$$

The diagram of Figure 1 shows the generation of the DSPWM signals; these are required to control the twelve switches (IGBTs) of the DC/AC multilevel converter formed by the three-cascaded H-bridges.

Figure 1 Generation of DSPWM multilevel signal

The twelve switching signals are implemented in the FPGA (these signals come from the comparison of the modulated signal and the 26 carrier signals, as shown in Figure 1), due to the required combinational logic complexity for the correct turn on/off of the IGBTs corresponding to the AC/DC multilevel converter.

III. DSPWM Multilevel Signal Simulation of 27-Levels

The Figure 2 shows the simulation of DSPWM multilevel signal of 27-levels. The control technique at the FPGA output has a maximum peak-to-peak voltage of 3.3V. The waveform simulation of Figure 2 is obtained with the Xilinx platform.

Figure 2 Simulation of DSPWM signal of 27-levels

Figure 3 shows the flow diagram that describes the DSPWM multilevel signal. It contains the described codes in Tables 1, 2, 3, 4, 5 and 6.

Figure 3 Flow diagram of the DSPWM multilevel signal

IV. Implementing the DSPWM Signal of 27-Levels

The main advantages linked to the construction of multilevel topologies are the generation of high-quality output voltages, the power increase, the THD mitigation and the reduction of voltage stress in power switching devices [31-33].

In this contribution, the DSPWM multilevel modulation technique is applied in the cascaded H-bridge topology of Figure 4; its operating principle is explained through an H-bridge [34]. The H-bridge of Figure 4(a) consists of four switches S_{T1}, S_{T2}, S_{T3} and S_{T4}. Switches S_{T1} and S_{T3} operate complementary to S_{T2} and S_{T4}, producing three different output voltages through the switching control; the output voltages are $+V_{DC}$, 0 and $-V_{DC}$. In Figure 4(b) the switches S_{T1} and S_{T3} are turned on to generate $+V_{DC}$. In Figure 4(c) switches S_{T2} and S_{T4} are turned on to produce $-V_{DC}$, and to generate 0V. Two options can be followed, i.e., switches S_{T1} and S_{T4} (Figure 4(d)) or S_{T2} and S_{T3} are turned on (Figure 4(e)). It is possible to choose any of these configurations without modifying the final waveforms. For this research work the configuration of Figure 4(e) is selected.

In order to obtain 27-levels in the DC/AC multilevel converter output using three-cascaded H-bridges units, three different DC voltage sources are used, i.e. in the H-bridge 1 the DC voltage source 1 is nine times higher than the DC Voltage source 3 of the H-bridge 3; and in the H-bridge 2 the DC voltage source 2 is three times higher than the DC voltage source 3 of the H-bridge 3. The DSPWM implementation applied to the DC/AC multilevel converter is performed using a XC3S500E FPGA and VHDL.

Figure 4 Topological states of an H-bridge converter. a) H-bridge model; b) +VDC state; c) –VDC state; d) 0 state; e) 0 state

Figure 5 Circuits corresponding to the used combinational logic of Table 8. a) Combinational logic of H-bridge 1; b) Combinational logic of H-bridge 2; c) Combinational logic of H-bridge 3

In Table 7 the turn on/off of each IGBT of the three-cascaded H-bridges are specified. The used combinational logic for the correct IGBTs switching is shown in Table 8. Figure 5 shows the circuits corresponding to the used combinational logic for the correct IGBT switching. Figure 5(a) shows the combinational logic to generate the train of pulses applied to the IGBTs of the H-bridge 1, Figure 5(b) illustrates the combinational logic applied to the IGBTs of the H-bridge 2 and Figure 5(c) shows the combinational logic for the IGBTs of the H-bridge 3.

Figure 6 Three-cascaded H-bridges configuration and equivalent circuit corresponding

Figure 6 shows the three-cascaded H-bridges configurations and the equivalent circuit corresponding to generate a multilevel output signal of 27-levels.

The general output of the DC/AC multilevel converter of Figure 6 is given by,

$$V_{OUT} = \left(S_{T1} + 3S_{T2} + 9S_{T3}\right)V_{DC} \tag{8a}$$

$$V_{OUT} = \sum_{n=0}^{2} \left(3^n\right)\left(S_T * V_{DC}\right) \tag{8b}$$

where $S_T = \varepsilon\{-1,0,1\}$, V_{DC} is the DC voltage and V_{OUT} the DC/AC converter output voltage.

The DC/AC multilevel converters can generate a close to sinusoidal output voltage, depending on the number of signal voltage levels [35-36]. Figure 7(a) shows output voltage of the DC/AC multilevel converter of 27-levels (formed by three-cascade H-bridges). This is close to the sinusoidal waveform generated by a 312V peak-to-peak voltage with a DC input voltage of 156V. Figure 7(b) shows a voltage zoom.

It is important to mention that, since the power electronic converter internally generates series parasite resistances, its output voltage varies with the connection of different types of loads, even if the voltage supply remains constant. In the proposed DC/AC multilevel converter, the series resistances depend on the filtered elements, the series impedance of the DC voltage supply and the conduction and switching losses of the semiconductor devices. For this case, an error of 3% in the I^2R losses is considered, due to the no load and full load variations, with efficiencies between 94% and 97% being generated.

Figure 7 The DSPWM output of 27-levels to single-phase unfiltered H-bridge DC/AC converter. a) Total output voltage; b) Voltage zooms

The multilevel modulation technique functionality generated in the FPGA is verified and analyzed for the connection of different load types, i.e. R, RL, RC and RLC.

Figure 8 Types of loads tested in the DSPWM of 27-levels experimental prototype. a) R load; b) RL load; c) RC load; d) RLC or Second order load

The Different types of load (Z_{LOAD}) considered as impedances in the experimental prototype are shown in Figure 8. Table 9 gives the prototype and hardware data used in the experimental implementation.

In order to analyze the waveforms of the involved electric variables in the DC/AC conversion by the multilevel converter, different connection nodes are selected between the 27-levels modulation process and the load.

Figure 9 Electric variables involved in the DC/AC energy conversion process. a) DSPWM pulse trains generated by FPGA; b) Voltages formed by the three-cascaded H-bridges; c) Voltage and current with *R* load; d) Voltage and current with *RL* load; e) Voltage and current with *RC* load; f) Voltage and current with *RLC* load

Figure 9 shows the experimental results of the selected connection nodes. In particular, in Figure 9(a) the three DSPWM pulse trains: i.e. S_{T11} (yellow), S_{T21} (cyan), and S_{T31} (pink), generated by FPGA (corresponding to the first IGBT of each of the three-cascaded H-Bridge) are shown. Figure 9(b) illustrates the behavior of V_{T1} (yellow), V_{T2} (cyan) and V_{T3} (pink) voltages formed by the H-bridge converters. Please notice the generation of three voltage levels. Besides, the changes in topological states are inversely proportional to DC voltage of each H-Bridge converter. The response of the total output voltage and the load current (yellow and cyan, respectively) for different loads are given in Figures 9(c), 9(d) and 9(e), generated by the R, RL and RC loads, respectively. In these Figures, the converter capacity to work with currents between quadrants of resistive, inductive and capacitive loads for different values of magnitude and phase, and without altering the operation and process of the output voltage (V_{OUT}) is verified. Finally, Figure 9(f) shows the waveforms of a RLC load. It can be observed that the resistive element is supplied with a purely sinusoidal voltage waveform (pink), due to the recovery of the generated fundamental voltage. The THD of the output voltage is 3.06%. The THD of the output current for each load is listed in Table 10. It is important to remark that in practice the resistors (Lab-Volt modules) are built of copper wire, and these have a parasite inductance, which slightly attenuates the measured THD; hence, it is not possible to obtain a completely resistive effect.

The Figure 10 shows the experimental prototype developed to apply the DSPWM multilevel technique of 27-levels with the FPGA. The main stages of implementation are highlighted in rectangles. It shows a *RLC* load (Figure 10(a)); the pulse trains generated by the FPGA (Figure 10(b)); a supply 156V DC voltage consisting on three different DC voltage sources, i.e. a DC voltage 3 of *12V* (Figure 10(c)), a DC voltage 2 of *36V* (Figure 10(d)) and a DC voltage 1 of *108V* (Figure 10(e)); a FPGA device (Figure 10(f)); and a DC/AC converter made with three-cascaded H-bridges (Figure (10g)); generating the AC multilevel output voltage of 27-levels, which produces the filtered waveform of Figure 9(f).

Figure 10 Prototype used to apply the DSPWM multilevel control technique of 27-levels. a) *RLC* load; b) DSPWM pulse trains generated by the FPGA; c) DC source voltage 3 (V_{DC}); d) DC source voltage 2 ($3V_{DC}$); e) DC source voltage 1 ($9V_{DC}$); f) XC3S500E FPGA device; g) H-bridge converters

V. CONCLUSIONS

In this contribution has been proposed a DSPWM multilevel technique of 27-levels using an FPGA model XC3S500E to control a DC/AC multilevel converter formed by three-cascaded H-bridges for the THD reduction in different load types. Its dynamic response with the implemented prototype in laboratory has been successfully verified.

It has been shown that with the characteristics of an FPGA (parallel data processing, re-programmability and concurrency) in conjunction with the VHDL language, it is possible the generation of n-levels signals in multilevel applications, in merit to its flexibility, versatility and simplicity properties without excess of unnecessary software.

The multilevel modulation technique functionality generated in the FPGA has been verified and analyzed with the connection of different actual loads types, such as R, RL, RC y RLC, respectively. This allowed attesting the converter capacity to work with currents within quadrants of resistive, inductive and capacitive loads for different values of magnitude and phase, without altering the operation and process of the output voltage (V_{OUT}).

It has been shown that a DSPWM multilevel signal with a high number of levels generates a higher quality quasi-sinusoidal output signal, with significantly less switching losses in the power converters. This has been tested and verified; i.e. the registered THD with the application of the proposed prototype was 3.06%.

VI. REFERENCES

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VII. TABLES

Table 1 Modulation signal storage in ROM

```
Type ROM_Array is array (0 to 499)  of std_logic_vector (15
down to 0);
Constant Content: ROM_Array :=
(0    => x"1388",
1    => x"13C0",
.             .
.             .
498       => x"1316",
499     => x"134F",
Others     => x"ffff”);
```

Table 2 Modulation signal at 60Hz.

```
Modulation: process(clk, clr)
  begin
    if clr = '1' then
      Modulation_Signal <= (others => '0');
    elsif clk'event and clk = '1' then
```

```
        if Modulation_Signal = 1666
          Modulation_Signal <= (others => '0');
        else
          Modulation_Signal<= Modulation_Signal + 1;
        end if;
      end if;
   end process Modulation;
```

Table 3 Location selection process in ROM.

```
Frequency: process (clr, clk, Modulation_Signal)
  begin
    if clr = '1' then
      period <= (others => '0');
    elsif clk'event and clk = '1'  and Modulation_Signal
= 0 then
       if Modulation_Signal = 0 then
          if period = 499
            period <= (others => '0');
          else
            period <= period + 1;
          end if;
       end if;
    end if;
end process Frequency;
```

Table 4 Location value assignment in ROM

```
 Assignation: process (Read, period)
  begin
     if (reset = '1') then
          Data_out <= "ZZZZZZZ";
     elsif (reset = '0') then
          if (Read = '1') then
            Data_out   <=   Content   (conv_integer
 (period));
           else
                Data_out <= "ZZZZZZ";
           end if;
     end if;
  end process Assignation;
```

Table 5 Carrier signal frequency process

```
Carrier1: process (clk, clr)
begin
      if clr = '1' then
         Carrier_signal_frequency<= (others => '0');
      elsif clk'event and clk = '1' then
         if Carrier_signal_frecuency = 2999 then
                  Carrier_signal_frecuency <= (others => '0');
         else
            Carrier_signal_frecuency <=
Carrier_signal_frecuency  + 1;
         end if;
      end if;
end process Carrier1;
```

Table 6 Carrier signal creation process

```
Triangular: process (clr, clk, Carrier_signal_frequency)
begin
   if clr = '1' then
      Carrier<= (others => '0');
   elsif clk'event and clk = '1' then
      if Carrier_signal_frequency < 1500 then
         Carrier <= Carrier + 1;
      else
         Carrier <= Carrier - 1;
      end if;
   end if;
end process Triangular;
```

Table 7 Combination of witches in the DC/AC converter using three-cascaded H-bridges

Level Number	**V_{DC}**			**H-bridge 1** $+V_{DC} = S_{T11}S_{T13}$				**H-bridge 2** $0 = S_{T22}S_{T23}$				**H-bridge 3** $-V_{DC} = S_{T32}S_{T34}$			
	9	***3***	***1***	S_{T11}	S_{T12}	S_{T13}	S_{T14}	S_{T21}	S_{T22}	S_{T23}	S_{T24}	S_{T31}	S_{T32}	S_{T33}	S_{T34}
13	1	1	1	1	0	1	0	1	0	1	0	1	0	1	0
12	1	1	0	1	0	1	0	1	0	1	0	0	1	1	0
11	1	1	-1	1	0	1	0	1	0	1	0	0	1	0	1
10	1	0	1	1	0	1	0	0	1	1	0	1	0	1	0
9	1	0	0	1	0	1	0	0	1	1	0	0	1	1	0
8	1	0	-1	1	0	1	0	0	1	1	0	0	1	0	1
7	1	-1	1	1	0	1	0	0	1	0	1	1	0	1	0
6	1	-1	0	1	0	1	0	0	1	0	1	0	1	1	0
5	1	-1	-1	1	0	1	0	0	1	0	1	0	1	0	1
4	0	1	1	0	1	1	0	1	0	1	0	1	0	1	0
3	0	1	0	0	1	1	0	1	0	1	0	0	1	1	0
2	0	1	-1	0	1	1	0	1	0	1	0	0	1	0	1
1	0	0	1	0	1	1	0	0	1	1	0	1	0	1	0
0	0	0	0	0	1	1	0	0	1	1	0	0	1	1	0
-1	0	0	-1	0	1	1	0	0	1	1	0	0	1	0	1
-2	0	-1	1	0	1	1	0	0	1	0	1	1	0	1	0
-3	0	-1	0	0	1	1	0	0	1	0	1	0	1	1	0
-4	0	-1	-1	0	1	1	0	0	1	0	1	0	1	0	1
-5	-1	1	1	0	1	0	1	1	0	1	0	1	0	1	0
-6	-1	1	0	0	1	0	1	1	0	1	0	0	1	1	0
-7	-1	1	-1	0	1	0	1	1	0	1	0	0	1	0	1
-8	-1	0	1	0	1	0	1	0	1	1	0	1	0	1	0
-9	-1	0	0	0	1	0	1	0	1	1	0	0	1	1	0
-10	-1	0	-1	0	1	0	1	0	1	1	0	0	1	0	1
-11	-1	-1	1	0	1	0	1	0	1	0	1	1	0	1	0
-12	-1	-1	0	0	1	0	1	0	1	0	1	0	1	1	0
-13	-1	-1	-1	0	1	0	1	0	1	0	1	0	1	0	1

Table 8. Combinational logic corresponding to each IGBT of cascaded H-bridges.

Switch number	Corresponding Combinational Logic
S_{T11}	(DSPWM**18**)
S_{T12}	NOT (S_{T11})
S_{T13}	NOT (DSPWM**9**)
S_{T14}	NOT (S_{T13})
S_{T21}	**[**(DSPWM**24**)**]** OR **[**(NOT(DSPWM**18**)) AND (DSPWM**15**)**]** OR **[**(DSPWM**9**) AND (NOT(DSPWM**6**))**]**
S_{T22}	NOT(S_{T21})
S_{T23}	**[**(DSPWM**21**)**]** OR **[**(NOT(DSPWM**18**)) AND (NOT(DSPWM**12**))**]** OR **[**(DSPWM**9**) AND (NOT(DSPWM**3**))**]**
S_{T24}	NOT(S_{T23})
S_{T31}	**[**(DSPWM**26**)**]** OR **[**(NOT(DSPWM**24**)) AND (DSPWM**23**)**]** OR **[**(NOT(DSPWM**21**)) AND (DSPWM**20**)**]** OR **[**(NOT(DSPWM**18**)) AND (DSPWM**17**)**]** OR **[**(NOT(DSPWM**15**)) AND (DSPWM**14**)**]** OR **[**(DSPWM**12**) AND (NOT(DSPWM**11**))**]** OR **[**(DSPWM**9**) AND (NOT(DSPWM**8**))**]** OR **[**(DSPWM**6**) AND (NOT(DSPWM**5**))**]** OR **[**(DSPWM**3**) AND (NOT(DSPWM**2**))**]**
S_{T32}	NOT(S_{T31})
S_{T33}	**[**(DSPWM**25**)**]** OR **[**(NOT(DSPWM**24**)) AND (DSPWM**22**)**]** OR **[**(NOT(DSPWM**21**)) AND (DSPWM**19**)**]** OR **[**(NOT(DSPWM**18**)) AND (DSPWM**16**)**]** OR **[**(NOT(DSPWM**15**)) AND (NOT(DSPWM**13**))**]** OR **[**(DSPWM**12**) AND (NOT(DSPWM**10**))**]** OR **[**(DSPWM**9**) AND (NOT(DSPWM**7**))**]** OR **[**(DSPWM**6**) AND (NOT(DSPWM**4**))**]** OR **[**(DSPWM**3**) AND (NOT(DSPWM**1**))**]**
S_{T34}	NOT(S_{T33})

Table 9 Prototype and hardware values.

Converter power		400W
V_{OUT}		$110V_{RMS}$
THD (V_{OUT})		3.06%
DC Voltage Sources	*VDC1*	12v
	VDC2	36v
	VDC3	108v
Types of Load	*R*	20
	RL	R=20Ω XL=20Ω
	RC	R=20Ω XC=20Ω
	RLC	R=30Ω XL=12.3Ω XC=240Ω
IGBT		G4PC40UD-E
FPGA		XC3S500E model

Table 10 THD of current in different loads

Load Types	Current THD (%)
R	3.06
RL	0.59
RC	4.27
Second order or RLC	0.63

VIII. BIOGRAPHY

Nadia Maria Salgado-Herrera received her Ph.D. degree in Electrical Engineering from Universidad Michoacana de San Nicolás de Hidalgo (UMSNH) in 2016, the BSc. and M.S. degree in Electronics Engineering and Electrical Engineering from Instituto Tecnológico de Morelia, Michoacán, México, in 2009 and 2011, respectively. She is currently teaching in the Facultad de Ingeniería Eléctrica at the UMSNH. Her research areas include Power electronics, Power Quality and Renewable energy.

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