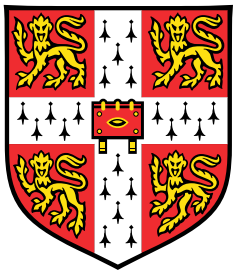
Energy-efficient Interfaces for Vibration Energy Harvesting



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To my wife, Peng Yi.
To my baba, Du Daozhong, and mama, Zhang Xinfeng.

Declaration

I hereby declare that except where specific reference is made to the work of others, the contents of this dissertation are original and have not been submitted in whole or in part for consideration for any other degree or qualification in this, or any other university. This dissertation is my own work and contains nothing which is the outcome of work done in collaboration with others, except as specified in the text and Acknowledgements. This dissertation contains fewer than 65,000 words including appendices, bibliography, footnotes, tables and equations and has fewer than 150 figures.

Sijun Du
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Abstract

Ultra low power wireless sensors and sensor systems are of increasing interest in a variety of applications ranging from structural health monitoring to industrial process control. Electrochemical batteries have thus far remained the primary energy sources for such systems despite the finite associated lifetimes imposed due to limitations associated with energy density. However, certain applications (such as implantable biomedical electronic devices and tire pressure sensors) require the operation of sensors and sensor systems over significant periods of time, where battery usage may be impractical and add cost due to the requirement for periodic re-charging and/or replacement. In order to address this challenge and extend the operational lifetime of wireless sensors, there has been an emerging research interest on harvesting ambient vibration energy.

Vibration energy harvesting is a technology that generates electrical energy from ambient kinetic energy. Despite numerous research publications in this field over the past decade, low power density and variable ambient conditions remain as the key limitations of vibration energy harvesting. In terms of the piezoelectric transducers, the open-circuit voltage is usually low, which limits its power while extracted by a full-bridge rectifier. In terms of the interface circuits, most reported circuits are limited by the power efficiency, suitability to real-world vibration conditions and system volume due to large off-chip components required.

The research reported in this thesis is focused on increasing power output of piezoelectric transducers and power extraction efficiency of interface circuits. There are five main chapters describing two new design topologies of piezoelectric transducers and three novel active interface circuits implemented with CMOS technology. In order to improve the power output of a piezoelectric transducer, a series connection configuration scheme is proposed, which splits the electrode of a harvester into multiple equal regions connected in series to inherently increase the open-circuit voltage generated by the harvester. This topology passively increases the rectified power while using a full-bridge rectifier. While most of piezoelectric transducers are designed with piezoelectric layers fully covered by electrodes, this thesis proposes a new electrode design topology, which maximizes the raw AC output power of a piezoelectric harvester by finding an optimal electrode coverage.

In order to extract power from a piezoelectric harvester, three active interface circuits are proposed in this thesis. The first one improves the conventional SSHI (synchronized switch harvesting on inductor) by employing a startup circuitry to enable the system to start operating under much lower vibration excitation levels. The second one dynamically configures the connection of the two regions of a piezoelectric transducer to increase the operational range and output power under a variety of excitation levels. The third one is a novel SSH architecture which employs capacitors instead of inductors to perform synchronous voltage flip. This new architecture is named as SSHC (synchronized switch harvesting on capacitors) to distinguish from SSHI rectifiers and indicate its inductorless architecture.

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Abbreviations and Acronyms

MEMS	Microelectromechanical systems
CMOS	Complementary metal–oxide–semiconductor
IC	Integrated circuit
VEH	Vibration energy harvesting
PVEH	Piezoelectric vibration energy harvester
PT	Piezoelectric transducer
PH	Piezoelectric harvester
FBR	Full-bridge rectifier
SSHI	Synchronized switch harvesting on inductor
SSHC	Synchronized switch harvesting on capacitors
SSD	Synchronized switch damping
SECE	Synchronous electrical charge extraction
MPP	Maximum power point
MPPT	Maximum power point tracking
AC	Alternative current
DC	Direct current
MSB	Most significant bit
LSB	Least significant bit
WSN	Wireless sensor network
PZT	Lead zirconate titanate
ZnO	Zinc oxide
AlN	Aluminum nitride
STFT	Short-time Fourier transform
SOI	Silicon on insulator

Chapter 1

Introduction

1.1 Motivation and previous research

The very significant advances in microelectronics engineering in the last decades have led to the development of ultra low power wireless sensors and sensor systems [1–4]. These sensor systems are of increasing interest in a variety of applications ranging from structural health monitoring to industrial process control [5, 6]. Compared to wired methodologies, wireless devices provide many advantages, such as flexibility and ease of placing the sensors in some locations that are not accessible by the wired counterparts. The systems can also be ameliorated without considering issues such as wiring and allowance for cabling.

Design consideration of ultra low power plays an important part in the design flow of electronic devices [7]. By minimizing the power consumption, researchers and engineers aim to extend the battery lifetime and to avoid replacing or recharging batteries too frequently. Electrochemical batteries have thus far remained the primary energy sources for such systems despite the finite associated lifetimes imposed due to limitations associated with energy density. However, in certain sensing contexts requiring the operation of sensors and sensor systems over a significant period of time [8, 9], including implantable biomedical electronic devices [10] and tire pressure sensors [11], battery usage may be both impractical and add extra cost due to the requirement for periodic re-charging and/or replacement [12]. In order to address this challenge and extend the operational lifetime of wireless sensors, there has been an emerging research interest to harvest energy from environmental sources [13–23].

For powering wireless nodes, vibration energy harvesters (VEH) are designed by groups in [24–44] through harvesting energy from kinetic vibration sources. Similar VEHs were also implemented in a tire pressure sensing [45]. In [46], a hybrid energy harvesting system of harvesting indoor ambient light and thermal energy is developed to power wireless sensor nodes, where a peak power of around 700 µW was achieved. In terms of structural health

Table 1.1 The output power comparison of different energy harvesting solutions

Solution	Power density in outdoor implementations	Power density in indoor implementation
Solar energy harvesting	15 $\mathrm{mW\,cm^{-2}}$ [56]	100 $\mathrm{\mu W\,cm^{-2}}$ (at 10 $\mathrm{W\,cm^{-2}}$ light density [57])
Thermal energy harvesting	100 $\mathrm{\mu W\,cm^{-2}}$ at 5 °C gradient, 3.5 $\mathrm{mW\,cm^{-2}}$ at 30 °C gradient [57]	100 $\mathrm{\mu W\,cm^{-2}}$ at 5 °C gradient, 3.5 $\mathrm{mW\,cm^{-2}}$ at 30 °C gradient [57]
Vibration energy harvesting	500 $\mathrm{\mu W\,cm^{-2}}$ (piezoelectric method) [7, 58, 59]	500 $\mathrm{\mu W\,cm^{-2}}$ (piezoelectric method) [7]
RF energy harvesting	15 $\mathrm{mW\,cm^{-2}}$ (with a transmitted power of 2-3 W at a frequency of 906 MHz at a distance of 30 cm [59]	15 $\mathrm{mW\,cm^{-2}}$ (with a transmitted power of 2-3 W at a frequency of 906 MHz at a distance of 30 cm [59]
Air flow energy harvesting	3.5 $\mathrm{mW\,cm^{-2}}$ (wind speed of 8.4 $\mathrm{m\,s^{-1}}$) [60]	3.5 $\mathrm{\mu W\,cm^{-2}}$ (air flow speed is less than 1 $\mathrm{m\,s^{-1}}$) [60]
Acoustic energy harvesting	960 $\mathrm{nW\,cm^{-2}}$ (acoustic noise of 100 dB) [56]	960 $\mathrm{nW\,cm^{-2}}$ (acoustic noise of 100 dB) [56]
Electromagnetic wave energy harvesting	0.26 $\mathrm{\mu W\,cm^{-2}}$ (from an electric field of 1 $\mathrm{V\,m^{-1}}$) [61]	0.26 $\mathrm{\mu W\,cm^{-2}}$ (from an electric field of 1 $\mathrm{V\,m^{-1}}$) [61]
Biochemical energy harvesting	0.1-1 $\mathrm{mW\,cm^{-2}}$ [62]	0.1-1 $\mathrm{mW\,cm^{-2}}$ [62]

monitoring, a self-powered pacemaker is proposed in [47] as an example of applying vibration energy harvesting technology in biomedical devices. The group of Canan Dagdeviren also tries to harvest energy from both heart and lung movements [48]. In [49], a hybrid VEH employing linearity and nonlinearity is used for powering pacemakers. Similar researches of VEH on biomedical applications are shown in [50–53]. Wind energy harvesting for structural health monitoring has also become more and more popular [54]. An approach of powering implementable biosensors by harvesting heat flow in [55] also proves the great research potential of environmental energy harvesting technology.

1.2 Different energy harvesting solutions

Small energy harvesters are of increasing interest along with the development of ultra low power electronics and wireless sensor networks (WSN). Many different kinds of energy harvesters have been proposed over the past decade [63–68]. Table 1.1 shows the power densities (harvested power per unit active area) for different energy harvesting solutions.

The solar and air flow energy harvesting systems give impressive power densities in outdoor implementation but the harvested power decreases dramatically while they are implemented indoors or when the weather condition is unsuitable. Because the performance of these two solutions is greatly dependent on the weather condition and an indoor environment cannot provide enough sunlight and wind speed to make the systems work at their optimal performance. RF energy harvester provides a high power density up to 15 $\mathrm{mW\,cm^{-2}}$ in indoor environments. However, a high-power drive of about 2-3 W at a high frequency is needed as the energy source and the transmission distance is limited to tens of centimeters. These limitations make the RF energy harvesters unsuitable for powering WSN but it facilitates remote battery recharging compared to conventional wired charging.

1.3 Objectives of the project

Among all vibration energy harvesting methods, piezoelectric vibration energy harvesting (PVEH) is widely employed due to its high power density, scalability and compatibility with conventional integrated circuit technologies. This project aims to improve the PVEH systems in two directions: output power and system miniaturization. In order to increase output power, piezoelectric transducers (PT) can be improved to generate higher raw AC power and rectification circuits can be improved to increase the energy extraction efficiency. The improvements on PTs are to propose series-connected electrodes and electrode coverage optimization and the work on interface circuits is to improve the existing SSHI rectifier and to propose new system architectures. Since SSHI rectifiers employ large inductors to achieve high energy efficiency, the volume of inductors can be dominant for miniaturized energy harvesting systems. Hence, removing the inductor by achieving comparable or higher performance is another focus of this project.

1.4 Outline of the dissertation

In general, this dissertation is focused on energy efficient interfaces for piezoelectric vibration energy harvesting (PVEH). In the second chapter, the background on piezoelectric energy har-

vesting interfaces is introduced, where state-of-the-art interface circuits and the performance are analyzed and compared. The third chapter proposes a novel connection configuration scheme, which splits the electrode of a piezoelectric transducer (PT) into several regions connected in series and this scheme is found to be able to improve the rectified power of a PT by several times without introducing additional active circuit. In the fourth chapter, the output power of a PT is analyzed by studying the electrode coverage and the results in order to maximize the output power. The fifth chapter presents a new connection configuration interface circuit which dynamically configures the connection of two PTs to increase the rectified power. In the sixth chapter, a new SSHI rectifier is proposed, which can be restarted by an additional startup circuit under low excitation levels; hence, the energy harvesting system can operate over a large excitation range. This circuit has also been experimentally evaluated using real-world vibration data and the results are shown in Appendix B. In the seventh chapter, a novel inductorless bias-flip rectifier is proposed, which employs capacitors to synchronously flip the voltage across the PT instead of using inductors as SSHI circuits. A summary of the contributions of this thesis and a discussion of future work are provided in the last chapter.

Chapter 2

Background on Piezoelectric Energy Harvesting Interfaces

2.1 Introduction

Vibration energy harvesting (VEH) has recently drawn much interest on harvesting environmental kinetic energy [69–76]. As noted in table 1.1, the output power of a vibration energy harvester is often acceptable for powering ultra-low-power wireless sensors [7, 77, 45, 55] and biomedical sensors [78, 79] under the right environmental conditions. Furthermore, VEHs can be fabricated at the MEMS-scale which enables wireless sensors to be implemented in applications where macro-scale energy harvesters cannot be employed [80].

A vibration energy harvester (VEH) is to convert kinetic vibrational energy in form of mechanical movement into electric energy [81–85]. This kind of harvester is often used in an environment with steady or frequent vibration of a specific frequency range [86–92], for example, the vibration caused by passing vehicles, engines, human gait [93–96] or heart beats [48–50]. In recent years, there has been a growing interest in VEH for realizing a decentralized on-board power solution [97–103].

In order to harvest vibration energy from motion, environmental kinetic displacement needs to be converted to electrical energy through a transduction mechanism [104–107]. The transduction mechanism should be designed to maximize the coupling between kinetic energy and electrical energy to improve the raw output power of a harvester and the characteristics of environmental vibration are the only factors that affect the performance of a harvester. A method of implementing vibration energy harvesting is to employ an electromechanical resonator which consists of an inertial mass attached to an inertial frame through a spring-equivalent structure, such as a cantilever. The environmental vibration applied on the inertial

frame is transmitted through a spring to the suspended inertial mass to produce a relative displacement between the frame and the mass. In order to increase the vibration amplitude, a resonant harvester is designed to be operated in or around the resonant frequency to produce a large displacement, hence more output power.

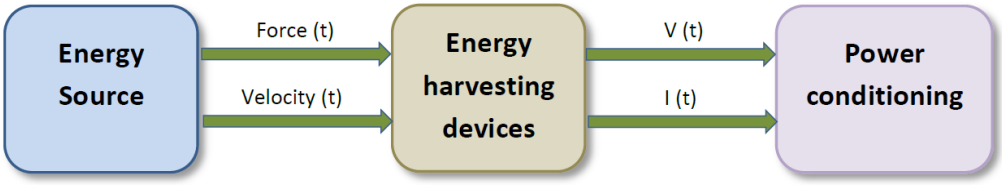


Fig. 2.1 Schematic of energy conversion in vibration energy transducers

A spring-mass system aims to convert vibration energy to relative displacement between the mass and the frame, hence strain in the spring. A transduction mechanism is then required to generate electricity by exploiting the displacement or strain (see figure 2.1 [108–112]). Piezoelectric materials are widely employed due to the relatively high power density and compatibility with conventional CMOS technology compared to other kinds of energy harvesters, such as electromagnetic and electrostatic harvesters [113–117].

2.2 Equivalent circuit of a piezoelectric VEH

A cantilevered piezoelectric transducer (PT) generally consists of a substrate layer, a thin piezoelectric layer and two electrode layers on the both sides of the piezoelectric ceramics [12], as shown in figure 2.2 where the electrode pads are not shown in the figure. Sometimes a mass is added to the tip of the free end to increase the strain and decrease natural frequency [118–123]. Lead-Zirconate-Titanate (PZT) is commonly used for PT due to its relatively high piezoelectric charge constant (d_{31}, d_{33} and d_{51}); some other materials, like Zinc Oxide (ZnO) and Aluminum Nitride (AlN), are mainly used in MEMS-scale harvesters. The equivalent circuit of a piezoelectric harvester can be understood as a damped mechanical spring-mass system coupled to an electrical part, as shown in Fig. 2.3 [124, 125]. There are mechanical and electrical parts shown in the figure, where L_M, C_M and R_M are equivalent to the mechanical mass, spring stiffness and mechanical loss respectively. σ_M represents the input excitation while the PT is excited. The output of the mechanical part (or the input of the transformer n), noted as σ_P, is the response of the PT under the excitation σ_M. The signal σ_P achieves its peak while the resonance frequency of the PT (formed by L_M, C_M and R_M) equals to the excitation frequency of σ_M. σ_P represents the strain (or stress) generated in the

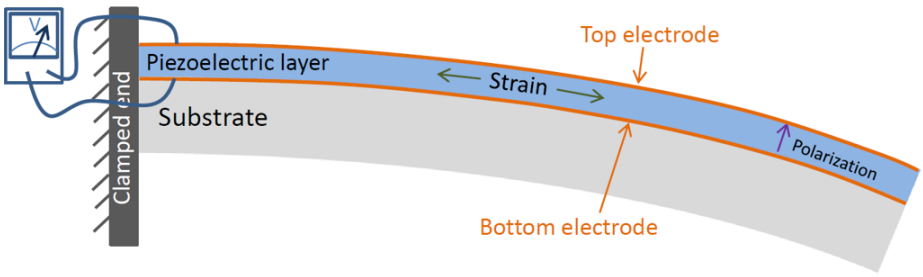


Fig. 2.2 Cantilevered piezoelectric harvester

piezoelectric ceramics. The induced strain is then converted into electrical charge within the piezoelectric elements, resulting in a charge flow representing a current source. Hence, the input of the electrical part (or the output of the transformer n) is a current source noted as I_P. The transformer in the figure represents the work of converting strain to current and the factor n is equivalent to the charge constant of the piezoelectric material, which is d_{31} for most of PTs. More details on piezoelectric materials and widely used charge constants can be found in appendix A.2. In the electrical part, the capacitor C_P is the plate capacitor of the piezoelectric material, which is equivalent to the capacitance formed by the two parallel electrode layers.

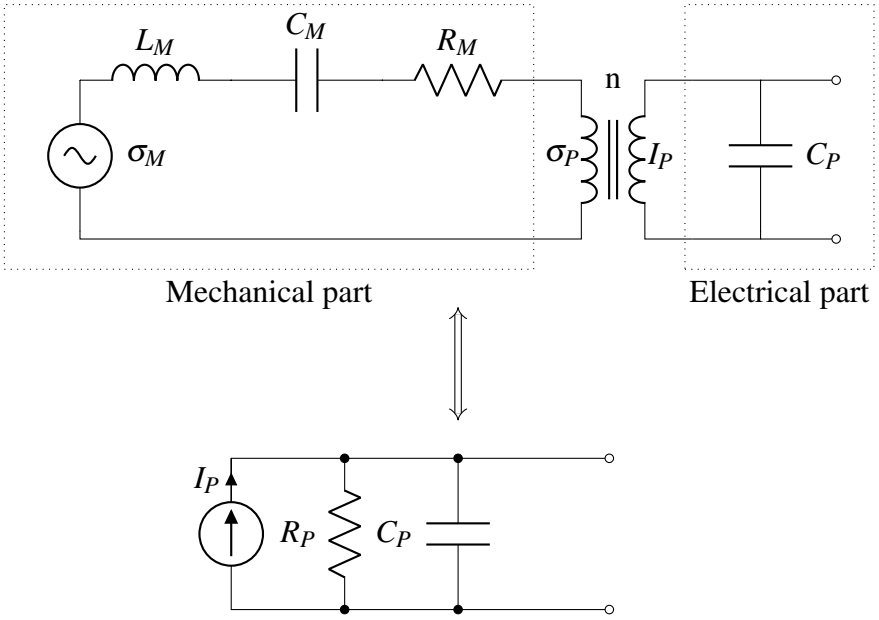


Fig. 2.3 Equivalent circuit of a piezoelectric harvester

While the harvester is vibrating at or near resonance, the whole circuit can then be modeled as an equivalent current source I_P parallel with a capacitor C_P and a resistor R_P [126, 127]. The resistor can be interpreted as the charge leakage resistance between the two

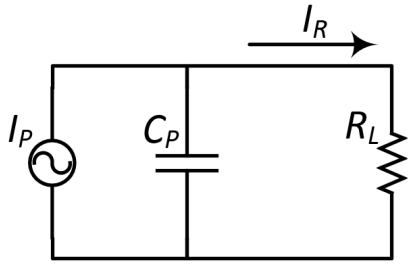


Fig. 2.4 Load resistor connected to a monolithic PT.

plate of the capacitor C_P. The current source I_P directly depends on the strain variation of the mechanism of the harvester. While the harvester is excited at resonance by a sinusoidal vibration, the current source I_P can be modeled as a sinusoidal current source. The expression of I_P can be written as:

$$I_P = I_0 \sin \omega_0 t = I_0 \sin 2\pi f_0 t \tag{2.1}$$

where I_0 depends on the excitation amplitude (or acceleration) and f_0 is the excitation frequency. Unlike a conventional battery or other energy source, the power generated by a piezoelectric transducer (PT) can be an unstable AC output because it depends on the vibration occurrence, amplitude and frequency [128]. It can only generate power while vibration occurs and the output voltage and frequency depend directly on the input excitation. Furthermore, the high output impedance prevents effectively driving load electronics. All of these limitations make an interface circuit indispensable.

2.3 Raw AC power generated by a PT

The raw output power from a piezoelectric transducer (PT) is analyzed in this section. The raw output power means the power consumed in a resistive load connected with the PT with the impedance matching. As discussed in the previous section, a PT can be modeled as a current source in parallel with a capacitor and a resistor. As the impedance of the resistor is typically much larger than that of the capacitor, the resistor is usually ignored to facilitate calculations. While the PT is excited with a sine wave excitation, the current source can be expressed as $I_P = I_0 \sin(\omega t)$, where $\omega = 2\pi f_P$ and f_P is the excitation frequency. Hence, the total charge generated by the PT in a half period (T/2) can be calculated, which is expressed as:

$$Q_{total} = \int_0^{\frac{T}{2}} I_0 \sin \omega t \, \mathrm{d}t = \frac{2I_0}{\omega} \tag{2.2}$$

Assuming the PT is operated as an open circuit, all generated charge Q_{total} flows into C_P. Therefore, the open-circuit zero-to-peak voltage amplitude is calculated as:

$$V_{OC} = \frac{1}{2}\frac{Q_{total}}{C_P} = \frac{I_0}{\omega C_P} \tag{2.3}$$

In order to measure the raw output power generated from a PT, a variable load resistor, R_L, is connected to the PT, as shown in Fig. 2.4. The resistance R_L is varied to match the internal impedance of the PT in order to find the peak output power consumed in the R_L. While a resistor R_L is connected to a PT, the current amplitude in R_L can be expressed as:

$$I_R(j\omega) = I_0\frac{Z_C}{Z_C + R_L} = \frac{I_0}{1 + j\omega R_L C_P} \tag{2.4}$$

Hence, the output power consumed in the resistor R_L can be calculated as:

$$\begin{aligned} P_R &= |\frac{1}{2}I_R^2 R_L| = \frac{I_0^2}{2}|\frac{R_L}{(1 + j\omega R_L C_P)^2}| \\ &= \cdots = \frac{I_0^2}{2}\frac{1}{\frac{1}{R_L} + \omega^2 C_P^2 R_L} \end{aligned} \tag{2.5}$$

The output power P_R attains its peak while $R_L = \frac{1}{\omega C_P}$. Hence, the raw output power of a PT consumed in a matched resistive load is:

$$P_{R(max)} = \frac{I_0^2}{4\omega C_P} \tag{2.6}$$

Equation (2.6) shows the maximal AC power consumed in a matched resistive load. In order to make use of the generated power for load electronic devices, the power needs to be rectified and regulated [129–135]. Hence, interface circuits are required and the power efficiency of the circuits significantly affects the usable energy provided to the loads [136, 137].

2.4 Full-bridge rectifier interface circuit

A typical MEMS piezoelectric transducer (PT) can provide an output power of up to 500 µW per 1 cm^2 [95], which sets a strict constraint on designing an interface circuit for the load circuitry [138–143]. The interface circuit does not only need to consume ultra low power, but it also should be able to extract as higher power as possible from the piezoelectric harvester [144–148]. So in order to make the piezoelectric VEH system to provide a high output

power, the powering conditioning interface is as important as the harvester mechanism. This section provides an overall background on some reported interface circuits and performance analysis on these interfaces. The limitations are discussed and future design considerations are proposed.

A piezoelectric vibration energy harvester vibrating at resonance can be considered equivalent to a current source I_P in parallel with a capacitor C_P and a resistor R_P [25, 149, 150]. As the resistor R_P is very large and is significantly higher than the impedance of C_P, it is usually ignored. According to the previous section, the output voltage and frequency may vary all the time according to the environmental vibration [151–153]. This unstable power source cannot be used directly to power analog or digital load circuitry, such as wireless sensors [8], pace-makers, etc. For this reason, a power conditioning circuit should be added between the piezoelectric transducer (PT) and the load circuitry in order to rectify and store the unstable AC energy into a battery [109, 154], which is usually a super capacitor with low leakage coefficient. As the output of the PT is an unstable or sinusoidal AC current, most of interface circuits use rectifiers to perform an AC-DC conversion before further power conditioning [155].

The most commonly used interface circuit for a piezoelectric vibration energy harvester is based on a full-bridge rectifier (FBR) [156–159], which employs four diodes to perform full-bridge rectification in order to do AC-DC conversion [160, 161]. Fig. 2.5 shows the circuit diagram of a FBR and the associated waveforms. The energy harvested from the output of a full-bridge rectifier is stored in a storage capacitor C_S. Usually, further voltage regulation circuitry is needed to provide a stable DC supply to loads. When the piezoelectric harvester vibrates and it is not connected to any circuit (open-circuit), there is a voltage difference between V_P and V_N, note $V_{PZ(open)} = V_P - V_N$. In order to charge the capacitor C_S, the voltage $V_{PZ(open)}$ should firstly be greater than V_S; in addition, it should also overcome the forward threshold voltages of the diodes. Hence, $V_{PZ(open)} > V_S + 2V_D$ should be satisfied in order to make sure the PT can charge the storage capacitor C_S, where V_S is the voltage across C_S and V_D is the forward voltage drop in a diode.

At the end of a half vibration period, the voltage V_{PZ} equals $V_S + 2V_D$ or $-(V_S + 2V_D)$. V_{PZ} is assumed to be equal to $-(V_S + 2V_D)$ for the following explanation, which is labeled as the time instant t_0 in Fig. 2.5. In order to charge the capacitor C_S in the next half cycle, V_{PZ} should go to $V_S + 2V_D$, which means the PT needs to charge its internal capacitor C_P from $-(V_S + 2V_D)$ to $V_S + 2V_D$ (from time t_0 to time t_1). After $V_{PZ} = V_S + 2V_D$ satisfies, the rest of charge generated by the PT can then be able to be transferred to C_S between the time t_1 and t_2. Noting the peak-to-peak open-circuit voltage of V_{PZ} as $V_{pp(open)}$, the condition for the FBR being able to transfer energy from the PT to C_S is given as:

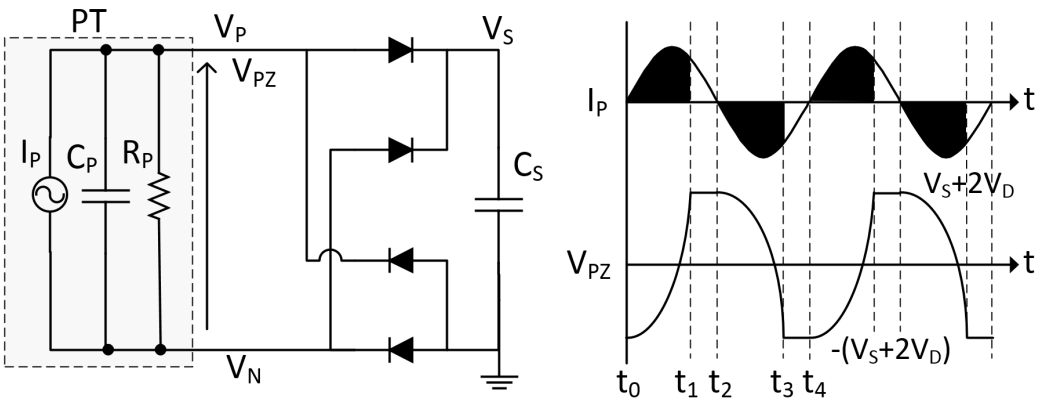


Fig. 2.5 Full-bridge rectifier interface circuit for the piezoelectric harvester and the associated waveforms

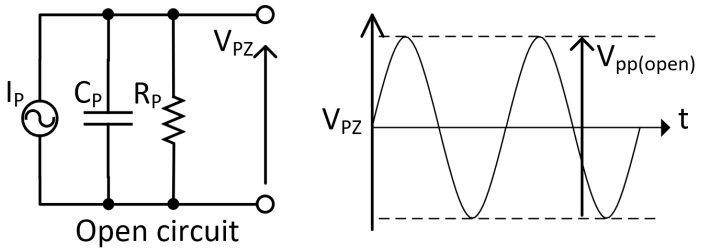


Fig. 2.6 The peak-to-peak open-circuit voltage $V_{pp(open)}$.

$$V_{pp(open)} > 2(V_S + 2V_D) \tag{2.7}$$

The peak-to-peak open-circuit voltage, $V_{pp(open)}$ is illustrated in Fig. 2.6 and it is proportional to the excitation level. As shown in Fig. 2.5, the charge generated by the piezoelectric harvester between t_0 and t_1 is used to discharge and recharge the internal capacitor C_P, which means this amount of charge is wasted [162]. The wasted charge is illustrated as black areas in the figure. The useful charge that can be transferred to the storage capacitor is just in a small time interval between t_1 and t_2 for each half-cycle. Assuming the internal capacitance is C_P, the amount of charge wasted (Q_{wasted}) between t_0 and t_1 for each half I_P cycle is given as:

$$\begin{aligned} Q_{loss(FBR)} &= C_P(V_S + 2V_D) - C_P(-(V_S + 2V_D)) \\ &= 2C_P(V_S + 2V_D) \end{aligned} \tag{2.8}$$

From Fig. 2.5, it can be found that the useful charge that can be transferred into C_S is the time intervals t_1 to t_2, t_3 to t_4, etc. For each half cycle of I_P, V_{PZ} needs to goes from $V_S + 2V_D$

to $-(V_S+2V_D)$ or from $-(V_S+2V_D)$ to V_S+2V_D before C_S can be charged. Therefore, the condition in equation 2.7 needs to be satisfied for the full-bridge rectifier to work. If this condition is not met, the full-bridge rectifier will stop operation and all the energy generated by the harvester is wasted in discharging and recharging C_P. For a $V_{pp(open)}$ that is slightly higher than the threshold $2(V_S+2V_D)$, most of the generated charge is wasted and the power efficiency is extremely low in this case.

In order to calculate the how much percentage of generated charge is wasted, the total charge generated by the harvester in a half cycle T/2 should be calculated, which can be written as:

$$Q_{total} = \int_0^{\frac{T}{2}} I_0 \sin \omega t \, \mathrm{d}t = \frac{2I_0}{\omega} \tag{2.9}$$

Since all the generated charge flows into C_P while the PT is in an open circuit, $V_{pp(open)}$ can be expressed as:

$$V_{pp(open)} = \frac{Q_{total}}{C_P} = \frac{2I_0}{\omega C_P} \tag{2.10}$$

So the percentage of the wasted charge in the total generated charge is given by:

$$\eta_{loss(FBR)} = \frac{Q_{loss(FBR)}}{Q_{total}} = \frac{\omega C_P(V_S+2V_D)}{I_0} = \frac{2(V_S+2V_D)}{V_{pp(open)}} \tag{2.11}$$

While $V_{pp(open)} < 2(V_S+2V_D)$, $\eta_{wasted} = 100\%$ because the threshold is not attained. In order to calculate the harvested power stored in C_S, the charge flowing into C_S should first be found. The amount of total available charge flowing into C_S is the difference between the total generated charge in the PT and the wasted charge in the FBR. Hence, the amount of charge flowing into C_S is given as:

$$Q_S = Q_{total} - Q_{wasted} = 2C_P(\frac{V_{pp(open)}}{2} - V_S - 2V_D) \tag{2.12}$$

As a result, when the voltage increase ΔV_S is very small, the energy transferred into C_S for half-cycle approximately equals to:

$$E_S = V_S Q_S = 2C_P V_S(\frac{V_{pp(open)}}{2} - V_S - 2V_D) \tag{2.13}$$

As this is the energy harvested in a half cycle, the power that can be transferred to C_S is:

$$P_S = \frac{E_S}{T/2} = 4C_P V_S f_P(\frac{V_{pp(open)}}{2} - V_S - 2V_D) \tag{2.14}$$

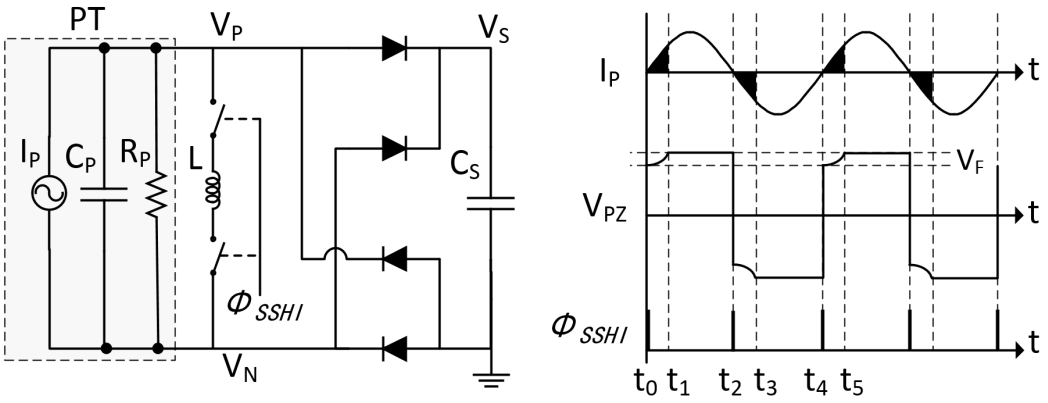


Fig. 2.7 SSHI interface for piezoelectric harvester and the associated waveforms

It can be easily found that the maximum P_S is obtained when $V_S = \frac{V_{pp(open)}}{4} - V_D$. The peak power transferred to C_S is:

$$P_{S(max)} = 4C_P f_P (\frac{V_{pp(open)}}{4} - V_D)^2 \tag{2.15}$$

When ignoring the forward voltage drop of diodes V_D, the peak power can be rewritten as:

$$P_{S(maxFBR)} = \frac{1}{4} C_P f_P V_{pp(open)}^2 \tag{2.16}$$

2.5 Parallel-SSHI interface

In order to minimize the wasted charge due to self-discharging and recharging internal capacitor C_P of the harvester, a scheme of employing synchronous charge inversion was proposed to enhance efficiency of piezoelectric energy harvesting devices [163], which is called "Parallel Synchronized Switch harvesting on Inductor (P-SSHI)". The circuit diagram and the associated waveforms are shown in figure 2.7.

A synchronous switch and an inductor are added in parallel with the piezoelectric transducer in order to flip the voltage. The signal I_P represents the equivalent current source of the piezoelectric harvester. At the time instant t_2, the zero-crossing of I_P is detected by a monitoring circuit and a pulse (ϕ_{SSHI}) is generated to turn ON the switch for a predetermined time to invert the voltage between V_P and V_N. The pulse width of ϕ_{SSHI} should be exactly a half of the period of the RLC oscillation loop.

Figure 2.8 shows a simplified architecture of an SSHI rectifier, which contains a FBR, a zero-crossing detection block, a pulse generation block, a level-shifter, two analog switches

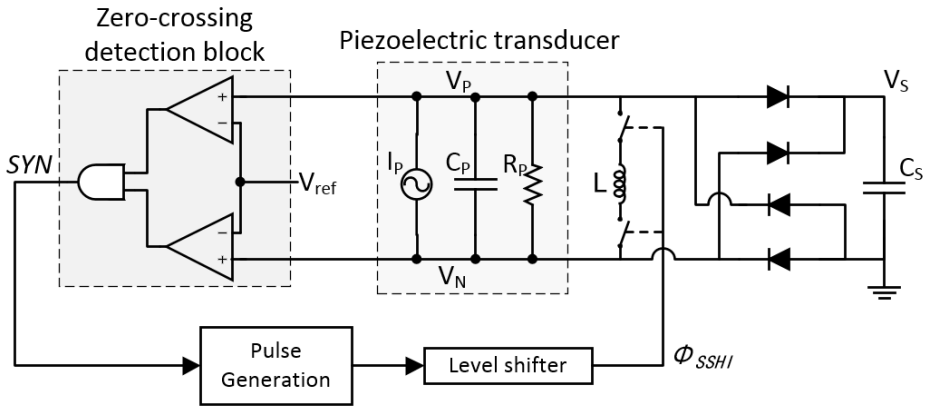


Fig. 2.8 Simplified system architecture of an SSHI interface circuit

and an inductor L. When I_P is close to zero, the diodes of the FBR are just about to turn OFF. At this moment, one of V_P and V_N begins to increase from $-V_D$ and the other one begins to decrease from $V_S + V_D$. One common method to detect the zero-crossing moment of I_P is using two comparators to compare V_P and V_N with a reference voltage V_{ref}. This reference voltage is set slightly higher than $-V_D$ and it aims to finds the moment while V_P or V_N begins to increase from $-V_D$. The outputs of the two comparators are ANDed and the resulting signal SYN presents a synchronous signal to control the switch. For each zero-crossing moment of I_P, a rising edge is generated in SYN and it is used to generate a pulse in the following blocks to control the inductor.

The ON resistance in the switch and any parasitic resistance in the RLC oscillation loop act as the electrical damping and it causes the loss of energy during charge inversion. This amount of energy loss forms a new threshold for the SSHI circuit to transfer charge from piezoelectric harvester to C_S, which can be written as:

$$V_{pp(open)} > V_F = (V_S + 2V_D)(1 - e^{-\frac{\pi}{\sqrt{\frac{4L}{R^2C}-1}}}) = (V_S + 2V_D)\eta_F \tag{2.17}$$

where the threshold V_F is illustrated in figure 2.7, which represents the voltage loss after one flip. η_F is the voltage loss ratio between 0 and 1 and it is expressed as $\eta_F = 1 - e^{-\frac{\pi}{\sqrt{\frac{4L}{R^2C}-1}}}$. The resistance R is the total resistance in the RLC loop, which consists of ON resistance in the switches, DC resistance of the inductor and all other parasitic resistance. Compared to the threshold of the FBR in equation (2.7), the SSHI circuitry decreases the threshold dramatically. Hence it significantly increases power efficiency, especially for small environmental excitations [164–166]. As V_F is the voltage loss after one flip in a half period of the vibration, the charge loss in this period can be written as:

$$Q_{loss(SSHI)} = C_P V_F \tag{2.18}$$

Hence, the amount of charge flowing into the storage capacitor C_S is:

$$Q_{S(SSHI)} = Q_{total} - Q_{loss(SSHI)} = C_P(V_{pp(open)} - V_F) \tag{2.19}$$

where, Q_{total} is given in equation 2.9. As a result, assuming the voltage increase in V_S is very small, the energy transferred into C_S in a half period can be expressed as:

$$E_{S(SSHI)} = V_S Q_{S(SSHI)} = C_P V_S(V_{pp(open)} - V_F) \tag{2.20}$$

Therefore, the extracted power stored in C_S is:

$$P_{S(SSHI)} = \frac{E_{S(SSHI)}}{T/2} = 2C_P V_S f_P(V_{pp(open)} - V_F) = 2C_P V_S f_P(V_{pp(open)} - (V_S + 2V_D)\eta_F) \tag{2.21}$$

The power attains its maximum value when $V_S = \frac{V_{pp(open)}}{2\eta_F} - V_D$ and the maximum power can be calculated as:

$$P_{S(maxSSHI)} = 2C_P f_P \eta_F (\frac{V_{pp(open)}}{2\eta_F} - V_D)^2 \tag{2.22}$$

While V_D is ignored, the peak power of using an SSHI interface circuit can be rewritten as:

$$P_{S(maxSSHI)} = \frac{1}{2\eta_F} C_P f_P V_{pp(open)}^2 \tag{2.23}$$

Comparing the peak power obtained in equations (2.16) and (2.23), the performance improvement of an SSHI rectifier compared to a FBR can be expressed as:

$$\frac{P_{SSHI}}{P_{FBR}} = \frac{P_{S(maxSSHI)}}{P_{S(maxFBR)}} = \frac{2}{\eta_F} \tag{2.24}$$

It can be seen that the performance improvement of using an SSHI rectifier directly depends on the voltage flip efficiency. Smaller η_F means higher voltage flip efficiency, hence higher power performance of the SSHI rectifier.

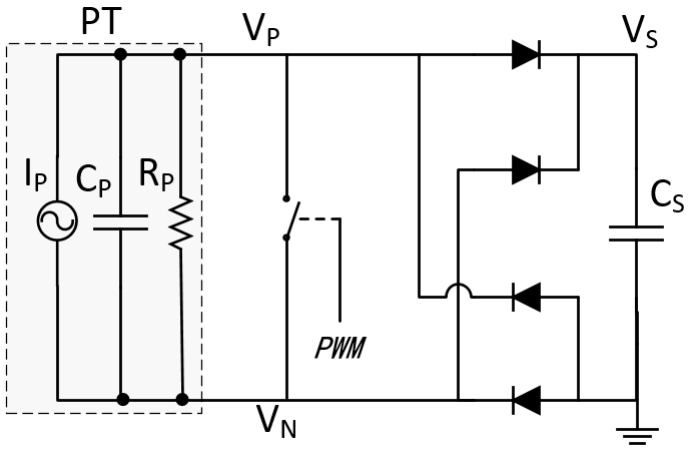


Fig. 2.9 Circuit diagram of the switch-only interface circuit.

2.6 Other circuits

Besides the most commonly used FBR and SSHI interface circuits, there are some other interface circuits being proposed for piezoelectric energy harvesting. Y. Ramadass [167] proposed a scheme, called the switch-only circuit, which is similar to SSHI but only employs a switch without an inductor to discharge the internal capacitor. The circuit diagram of the switch-only interface circuit is shown in Fig. 2.9. This approach aims to reduce the energy wasted in discharging C_P but there is still some energy waste for recharging. Compared to SSHI interface, although this "switch-only" circuit has relatively lower power efficiency, it does not employ an inductor so the complexity and volume of the system is reduces. For a switch-only interface, the equivalent voltage flip loss ratio η_F shown in equation 2.24 is 1 as the voltage across the PT is no flipped but cleared. Hence, according to the equation, the performance of a switch-only interface is improved by $2\times$ compared to a full-bridge rectifier.

Active diodes using CMOS switches and comparators have also drawn much attention for minimizing the effective voltage drop across a “diode”, such as C. Peters’ work in [166, 168]. CMOS switches are employed in these papers to switch ON and OFF by monitoring the voltages at different nodes of the system. However, as the effective voltage drop of a Schottky diode used in piezoelectric vibration energy harvesting can be as low as 100 mV, active diodes do not show significant performance improvement.

2.6.1 Existing issues and challenges

As discussed previously, the main target of power conditioning circuits is to make use of unstable AC power harvested by PTs, which can be realized by many different kinds of

passive and active rectifiers and interface circuits [169]. But one of the important figures for conditioning circuits is the ratio of stored power in battery to generated power by harvesters, which is known as power efficiency. Although the SSHI interface provides a very high efficiency compared to conventional bridge rectifiers, employing an off-chip inductor adds volume and cost of the system. Hence, a scheme of performing charge inversion without employing an inductor will be very attractive. Besides of the power efficiency, the reliability of the system is also an important factor for consideration. The circuit also needs to be able to extract energy effectively under variable vibration conditions.

Chapter 3

A Connection Configuration Scheme to Increase Operational Range and Output Power

3.1 Introduction

In order to increase the power efficiency of a VEH system, most interface circuits seek to develop a mechanism to minimize the energy wasted due to the threshold set by a full-bridge rectifier (FBR) [111, 150, 109, 12]. The interface circuit does not only need to consume ultra-low power, but it also should be able to recover the power as effectively as possible from the piezoelectric transducer (PT) [170, 25, 171, 172, 75]. Therefore, in order to design the piezoelectric VEH system to deliver a high output power, both the interface circuit and the harvester mechanism should be well designed and the design interaction should be thoroughly examined [173, 165, 174, 58]. Approaches such as the SSHI (Synchronized Switch Harvesting on Inductor) interface is considered to provide ideally no charge wastage if the resistance of the RLC loop is negligible [163, 175].

Despite the performance, there are four main drawbacks existing in these active interface circuits. First, the overall volume and complexity of an energy harvesting system are significantly increased by complex interface circuits along with off-chip capacitors, resistors and inductors, where inductors must be implemented off-chip to achieve good performance for most interfaces. Second, active interface circuits continuously consumes energy. Although some reported interface circuits attain sub-μW power loss, there is still an amount of energy is drawn from the energy reservoir when there is no input excitation. This could eventually deplete all stored energy and both the interface circuit and load electronic devices will stop

operating. In addition, SSHI and SECE circuits can only achieve high efficiency at a limited range of excitation levels. This limits the overall performance of the system in real-world implementations. Furthermore, SSHI and SECE interface circuits can only provide higher performance than simple full-bridge rectifiers for weakly coupled piezoelectric transducers due to the Synchronized Switch Damping (SSD) effect [176, 177]. If the the coupling is strong and the PT vibrates at resonance, the periodic current pulses applied to invert or extract charge on a PT result in an electrical actuation that opposes the vibration. All of the above four limitations introduced by system complexity and volume, quiescent power consumption, real-world wide range excitation levels and SSD effect result in the reported active rectifiers achieving acceptable performance only in a limited operating range.

In this chapter, a passive approach using a simple full-bridge rectifier is proposed with associated modifications in the connection configuration scheme for the piezoelectric transducer. This approach is able to achieve comparable performance to some active interface circuits without the drawbacks mentioned above. With the proposed approach, the electrode of a monolithic PT is split into multiple ($n \geq 2$) equal pieces connected in series and the number n can be pre-determined according to the excitation amplitude of the ambient vibration. A suitable value of n helps maximizing the operation range and harvested power. Theoretical studies on output power and threshold voltage for different values of n are provided in equations and figures. The theoretical derivations are validated by experimental results conducted on commercial piezoelectric vibration energy harvesters.

3.2 Full-bridge rectifier

A piezoelectric transducer (PT) vibrating at or close to its resonance frequency can be modeled as a current source I_P in parallel with a capacitor C_P and a resistor R_P [153]. The AC signal generated by the PT needs to be rectified in most cases before further power conditioning. The most commonly used passive rectification circuit for a PT is a full-bridge rectifier, which employs four diodes to perform AC-to-DC conversion (see Figure 2.5). The energy is then stored in a storage capacitor C_S connected to the output of the rectifier. Figure 2.5 also shows the associated waveform of the current source I_P and V_{PZ}, which is a time-varying voltage across the piezoelectric transducer (PT). In order to charge C_S, V_{PZ} needs to attain $V_S + 2V_D$ or $-(V_S + 2V_D)$ to overcome the threshold voltage set by the rectifier, where V_S is the voltage of the storage capacitor C_S and V_D is the voltage drop of the diodes used in the rectifier. Therefore, the energy used for charging the internal capacitor C_P from $V_S + 2V_D$ to $-(V_S + 2V_D)$ (or vice-versa) is wasted, which can be expressed as:

$$Q_{wasted} = 2C_P(V_S + 2V_D) \tag{3.1}$$

The peak-to-peak open-circuit voltage of V_{PZ} is noted as $V_{pp(open)}$. In order to transfer energy from the PT to the storage capacitor, $V_{pp(open)} > 2(V_S + 2V_D)$ should be satisfied. Otherwise, all of the harvested energy by the PT is wasted for discharging and charging C_P. So this critical voltage can be set as a threshold voltage for $V_{pp(open)}$ to ensure that the full-bridge rectifier transfers energy to C_S:

$$V_{pp(open)} > V_{TH} = 2(V_S + 2V_D) \tag{3.2}$$

where $V_{TH} = 2(V_S + 2V_D)$ is the threshold that $V_{pp(open)}$ must attain to transfer any energy to the storage capacitor C_S. If the condition in equation (3.2) is met, the remaining charge can flow into C_S. The wasted charge is used for discharging and charging C_P and the amount of the wasted charge in a half cycle of I_P is $Q_{wasted} = 2C_P(V_S + 2V_D)$. The power conversion efficiency is extremely low if $V_{pp(open)}$ is slightly higher than V_{TH}. Assuming $V_D = 0.5\,\mathrm{V}$ and $V_S = 3\,\mathrm{V}$, the threshold voltage is as high as 8 V. For MEMS (Microelectromechanical Systems) piezoelectric harvesters, this threshold is hard to attain.

3.3 Proposed scheme

A commonly used cantilevered PT consists of a substrate and a piezoelectric layer sandwiched between a pair of metal electrode layers. When the cantilever vibrates, the strain in the piezoelectric layer is transduced to electrical charge by the piezoelectric material and a current is generated to charge the inherent capacitor C_P formed by the two metal electrode layers [178]. As a result, there is a voltage V_{PZ} developed across the PT. As discussed previously, the most important limitations of a full-bridge rectifier are the high threshold voltage and low power efficiency while the threshold is marginally overcome [179]. This chapter proposes an approach by splitting both the top and bottom electrode layers into n equal parts [180]; hence, the monolithic PT turns into a harvester with n regions as a result, which is equivalent to n individual harvesters with exactly the same vibration amplitudes, frequencies and phases, as shown in Figure 3.1. Previous work on split-electrode design has been reported in [181], which segments the electrode of a PT along lines orthogonal to the strain direction. Differently, in this chapter, the electrode is segmented along the primary strain direction so that the total strain in the piezoelectric layers in each region is equal. As a result, the generated voltage from each region is equal in frequency, amplitude and phase.

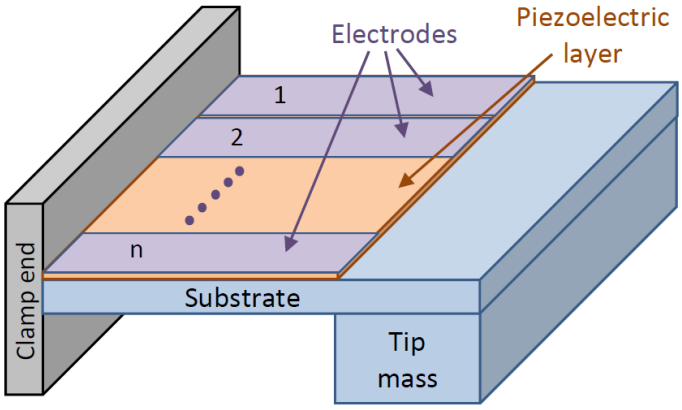


Fig. 3.1 Splitting a monolithic PT into n regions

The current source, internal capacitor and resistor in the monolithic PT are noted as $I_P = I_0 \sin 2\pi f_P t$, C_P and R_P, respectively. The model of the PT used for calculations in this chapter takes consideration of the internal leakage resistor R_P because the resonant frequency of the PT is quite low in this implementation, so that R_P is not negligible compared to the impedance of C_P. After splitting the electrode layers into n equal regions, the area is divided by n for each PT compared to the monolithic model. As the total strain in these regions is the same, the current source amplitudes for them should be equal. For one individual region, the current source amplitude, capacitor and resistor can be noted as I_1, C_1 and R_1 respectively. In a cantilever, the inherent capacitor and generated current amplitude are proportional to the electrode area and the total strain, respectively; the resistance is inversely proportional to the electrode area. Therefore, the parameters of the new PT can be expressed in terms of the parameters of the monolithic PT: $I_1 = \frac{1}{n} I_0 \sin 2\pi f_P t$, $C_1 = \frac{1}{n} C_P$ and $R_1 = nR_P$.

As the generated charge in one region is divided by n compared to the original monolithic PT ($Q_1 = \frac{1}{n} Q_P$) and the capacitor C_1 is also divided by n ($C_1 = \frac{1}{n} C_P$), the open-circuit voltage for one region equals to the voltage of the original monolithic PT ($V_{pp1(open)} = Q_1/C_1 = Q_p/C_P = V_{pp(open)}$). If the n regions are connected in parallel, the resulting harvester works exactly the same as the original monolithic harvester, as shown in Figure 3.2.

As expressed in equation (3.1), the charge wastage due to the self discharging and charging C_P in a half I_P cycle is $Q_{wasted} = 2C_P(V_S + 2V_D)$. In order to minimize Q_{wasted}, C_P can be decreased by connecting the n regions in series. They should be connected with consideration of voltage directions so that the final series harvester model results in a summed-up voltage. Setting the capacitor for each region as C_1, where $C_1 = \frac{1}{n} C_P$, the equivalent capacitor of the series model is $C_{P+} = \frac{1}{n^2} C_P$ (the symbol '+' means series). Therefore, the equivalent capacitor of this series connected PT is $1/n^2$ of the original one, which reduces Q_{wasted} by a factor of n^2. While the harvester is charging the storage capacitor C_S, the voltage $|V_{PZ}|$

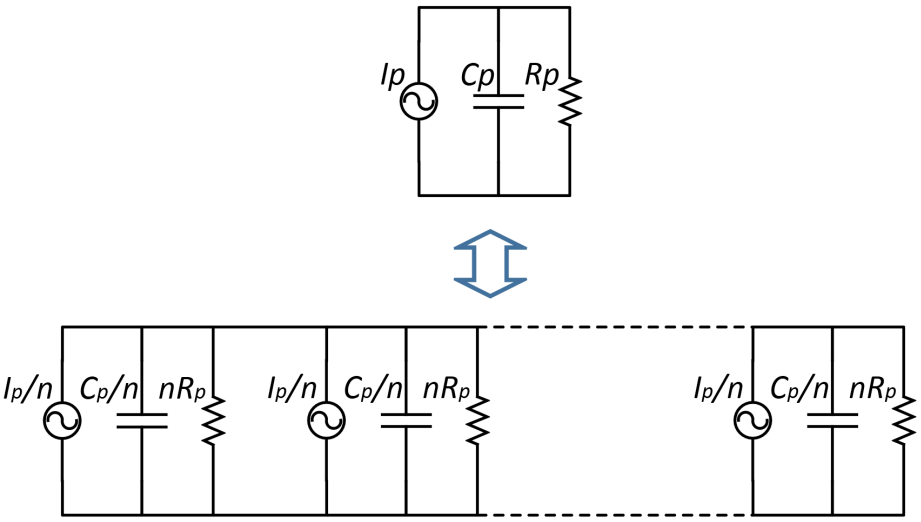


Fig. 3.2 Monolithic harvester (top) and n-region harvester connected in parallel (bottom)

will stay at $(V_S + 2V_D)$. Furthermore, by connecting in series appropriately, the open-circuit peak-to-peak voltage of this new harvester $V_{pp(open)+}$ is now increased by a factor of n. This phenomenon helps retain the rectifier operation even at smaller excitations, as the threshold voltage for the series model is halved.

Similar series configurations of PTs have been mentioned in [182, 183]. However, as opposed to previous researches, series models with variable stages is first thoroughly derived in this chapter and the output performance is calculated to find an optimal series stage number according to variable excitation environments [184, 185].

3.4 Modeling

In this section, theoretical models are developed to establish the effect of series connected PTs on the output power of a full-bridge rectifier. A monolithic PT model is first studied; then the PT is split into n equal regions connected in series. In order to compare the performance between the parallel and series models, the voltage increase in C_S (note ΔV_S) in function of excitation amplitude ($V_{pp(open)}$) for all models can be compared. In addition, the electrical output power of the full-bridge rectifier in function of V_S for different models under the same excitation level is derived and illustrated to find the peak output power for each model.

3.4.1 Monolithic model

Calculations are first performed on a monolithic PT to study the open-circuit peak-to-peak voltage $V_{pp(open)}$ and the corresponding output power with employment of a full-bridge rectifier. Assuming the excitation of the PT is sinusoidal, the current source can be written as $I_P = I_0 \sin \omega t$, where $\omega = 2\pi f_P$. The total charge generated by the PT in a half cycle (T/2) should first be calculated, which can be written as:

$$Q_{total} = \int_0^{\frac{T}{2}} I_0 \sin \omega t \mathrm{d}t = \frac{2I_0}{\omega} \tag{3.3}$$

As discussed previously, a vibrating PT can be modeled as a current source I_P in parallel with an internal capacitor C_P and a resistor R_P. Before the full-bridge rectifier becomes conducting, the current from I_P is divided into two parts inside the piezoelectric harvester, I_C and I_R flowing through the capacitor C_P and resistor R_P, respectively. As the diodes are OFF in this case, the PT can be regarded as an open-circuit. The ratio of the current flowing into C_P to the total current I_P is expressed as:

$$\frac{I_C}{I_P}(j\omega) = \frac{R_P}{R_P + \frac{1}{j\omega C_P}} = \frac{j\omega R_P C_P}{1 + j\omega R_P C_P} \tag{3.4}$$

The charge flowing into the capacitor C_P is:

$$Q_C(j\omega) = Q_{total}\frac{I_C}{I_P}(j\omega) = \frac{2jI_0 R_P C_P}{1 + j\omega R_P C_P} \tag{3.5}$$

As Q_C is the charge that flows into the capacitor C_P to build the voltage V_{PZ}, the rest of the charge flows into the resistive path and it is dissipated by the resistor R_P. According to the formula $V = Q/C$, the open-circuit peak-to-peak voltage $V_{pp(open)}$ can be written as:

$$V_{pp(open)} = |\frac{Q_C(j\omega)}{C_P}| = |\frac{2jI_0 R_P}{1 + j\omega R_P C_P}| = \frac{2I_0 R_P}{\sqrt{1 + \omega^2 R_P^2 C_P^2}} \tag{3.6}$$

To start transferring energy to C_S, $V_{pp(open)}$ after a half cycle $t = \frac{T}{2}$ should overcome the threshold $V_{TH} = 2(V_S + 2V_D)$. Hence, the condition for the rectifier to start transferring charge from the PT to C_S is:

$$\begin{aligned} V_{pp(open)} &> 2(V_S + 2V_D) \\ \Rightarrow \frac{I_0 R_P}{\sqrt{1 + \omega^2 R_P^2 C_P^2}} &> V_S + 2V_D \end{aligned} \tag{3.7}$$

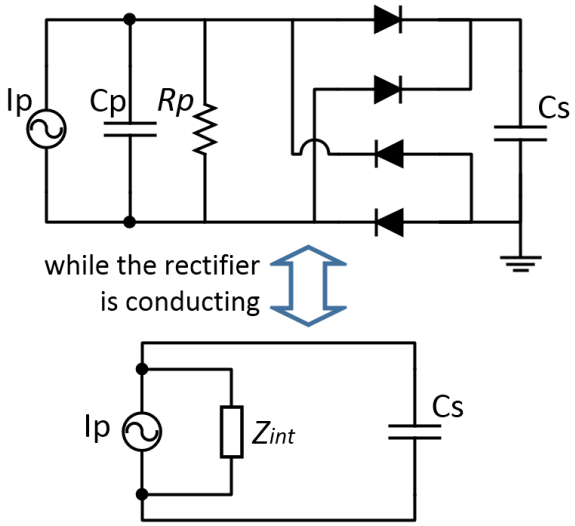


Fig. 3.3 Equivalent circuit while the full-bridge rectifier is conducting

In order to compare the performance between parallel and series models, this condition is assumed to be always satisfied so that both models are valid. The useful charge Q_C in C_P is expressed in equation (3.5) and the wasted charge Q_{wasted} for self discharging and charging C_P is given in equation (3.1). After Q_{wasted} is wasted for self-charging, V_{PZ} equals to $V_S + 2V_D$ (or $-(V_S + 2V_D)$) and the harvester starts to charge C_S. Therefore, the remaining charge going into C_S is the difference between Q_C and Q_{wasted}:

$$\begin{aligned} Q_{remain}(j\omega) &= Q_C(j\omega) - Q_{wasted} \\ &= 2C_P\left(\frac{jI_0R_P}{1+j\omega R_PC_P} - (V_s + 2V_D)\right) \end{aligned} \tag{3.8}$$

After the rectifier becomes conductive, the voltage V_{PZ} attains the threshold and the equivalent circuit transforms to a PT in parallel with C_S and the PT can be regarded as a current source I_P in parallel with its internal impedance, as shown in figure 3.3. The internal impedance is the value that C_P and R_P connected in parallel, expressed as:

$$Z_{int}(j\omega) = \frac{1}{j\omega C_P} // R_P = \frac{R_P}{1+j\omega R_PC_P} \tag{3.9}$$

The charge flowing into C_S can then be written as:

$$\begin{aligned} Q_S(j\omega) &= Q_{remain}\frac{Z_{int}}{Z_{int}+\frac{1}{j\omega C_S}} = Q_{remain}\frac{j\omega Z_{int}C_S}{1+j\omega Z_{int}C_S} \\ &= Q_{remain}\frac{j\omega R_P C_S}{1+j\omega R_P(C_P+C_S)} \\ &= \frac{2j\omega R_P C_P C_S}{1+j\omega R_P(C_P+C_S)}(\frac{jI_0R_P}{1+j\omega R_P C_P}-(V_S+2V_D)) \end{aligned} \tag{3.10}$$

While a full-bridge rectifier is employed, the capacitor C_S is usually chosen at a value much greater than the PT internal capacitor C_P ($C_S \gg C_P$), so that V_S can keep increasing steadily while external excitation is present. In addition, as R_P is usually at a value from hundreds of kΩ to several MΩ, hence $\omega R_P C_S \gg 1$. Therefore, equation (3.10) can be approximately written as:

$$Q_S \approx 2C_P(\frac{I_0R_P}{\sqrt{1+\omega^2R_P^2C_P^2}}-(V_S+2V_D)) \tag{3.11}$$

The voltage increase in C_S for harvesters connected in parallel in a half cycle is expressed as (where the symbol "//" means "parallel", equivalent to a monolithic harvester before splitting its electrode):

$$\Delta V_{S//} = \frac{Q_S}{C_S} = 2\frac{C_P}{C_S}(\frac{I_0R_P}{\sqrt{1+\omega^2R_P^2C_P^2}}-(V_S+2V_D)) \tag{3.12}$$

3.4.2 N-stage series model

While the electrode of the monolithic PT is segmented into n equal regions, the whole PT can be regarded as n individual harvesters connected in series. As the area of piezoelectric layer and electrode layer for each source is $\frac{1}{n}$ of the original PT, so I_{p1}, C_{p1} and R_{p1} for each small PT can be written as:

$$\begin{aligned} I_{p1} &= \frac{1}{n}I_P = \frac{1}{n}I_0 sin\omega t \\ C_{p1} &= \frac{1}{n}C_P \\ R_{p1} &= nR_P \end{aligned} \tag{3.13}$$

Calculations are started by considering only one PT and V_{piezo1} is the voltage generated by this source. As there are n sources connected in series, the total voltage is $V_{PZ} = \sum_{i=1}^{n} V_{piezo_i} =$

nV_{piezo1}. From equation (3.2), the condition to charge C_S is $V_{PZ} > 2(V_S + 2V_D)$, hence this condition for one individual source is:

$$V_{piezo1} > \frac{2}{n}(V_S + 2V_D) \tag{3.14}$$

From this equation, it can be seen that the threshold voltage is now lowered by a factor of n compared to the monolithic model so that harvester is much more likely to start operating at lower excitation levels. Therefore, the wasted charge for dis-charging and charging of one source in a half cycle is:

$$Q_{wasted1} = C_{p1}\frac{2}{n}(V_S + 2V_D) = \frac{2C_p}{n^2}(V_S + 2V_D) \tag{3.15}$$

The total charge flowing into C_{p1} in a half cycle is:

$$\begin{aligned} Q_{\frac{T}{2}1}(j\omega) &= \int_0^{\frac{T}{2}} I_{p1}\frac{R_{p1}}{R_{p1} + \frac{1}{j\omega C_{p1}}} = \int_0^{\frac{T}{2}} \frac{I_0}{n}\frac{nR_P}{nR_P + \frac{n}{j\omega C_P}} sin\omega t dt \\ &= \frac{2I_0}{n}\frac{R_P C_P}{1 + j\omega R_P C_P} \end{aligned} \tag{3.16}$$

Before the condition $V_{piezo1} > \frac{2}{n}(V_S + 2V_D)$ is met, the PTs are disconnected from C_S (as the diodes in the rectifier are not conducting). Once the $V_{piezo1} > \frac{2}{n}(V_S + 2V_D)$ is satisfied, all of the sources are connected together with C_S in series. At this time, C_S starts to be charged and the remaining charge flowing into C_S from each single source is:

$$Q_{left1}(j\omega) = Q_{\frac{T}{2}1}(j\omega) - Q_{wasted1} = \frac{2C_P}{n}\left(\frac{I_0 R_P}{1 + j\omega R_P C_P} - \frac{V_S + 2V_D}{n}\right) \tag{3.17}$$

As only one harvester is considered, superposition theory can be used to turn off the current sources of all other $n-1$ harvesters. While the harvester is charging C_S, the equivalent circuit for one single source is shown in figure 3.4. The internal impedance for each of the source is:

$$Z_{int1}(j\omega) = \frac{nR_P}{1 + j\omega R_P C_P} \tag{3.18}$$

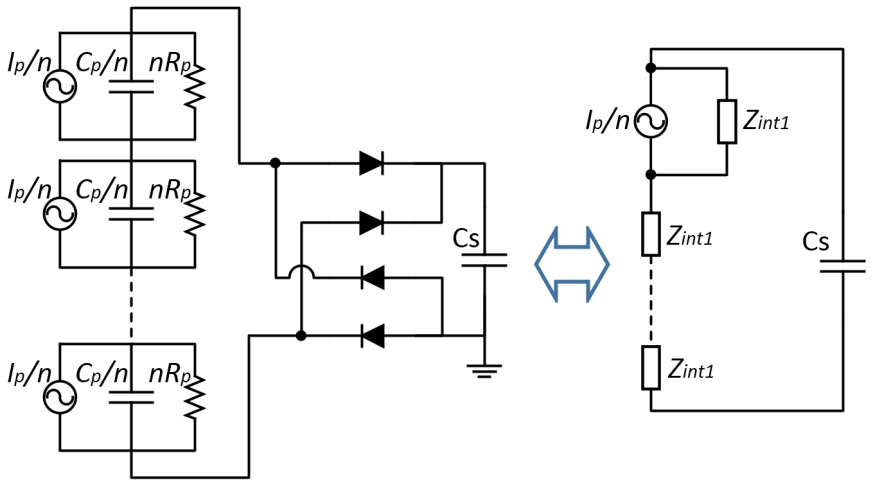


Fig. 3.4 Equivalent circuit for considering only one source in n-region series connected PTs while the rectifier is conducting

It can be seen that all the other $n-1$ impedances are connected in series with C_S, hence the total external impedance for one harvester is significantly increased. Hence, the ratio between the I_{ext} and I_{int} for each source being studied is:

$$\frac{I_{ext}}{I_{int}} = |\frac{Z_{int1}}{Z_{int1} + (n-1)Z_{int1} + \frac{1}{j\omega C_s}}| \approx \frac{1}{n} \quad (as \;\; C_S \gg C_P) \tag{3.19}$$

Therefore, the total charge flowing into C_S from one single harvester is:

$$Q_{S1} = |\frac{1}{n} Q_{left1}(j\omega)| = \frac{2C_P}{n^2}(\frac{I_0 R_P}{\sqrt{1+\omega^2 R_P^2 C_P^2}} - \frac{V_S + 2V_D}{n}) \tag{3.20}$$

While all the n individual harvesters are considered, the total charge flowing into C_S is:

$$Q_{S+} = \sum_n Q_{S1} = \frac{2C_P}{n}(\frac{I_0 R_P}{\sqrt{1+\omega^2 R_P^2 C_P^2}} - \frac{V_S + 2V_D}{n}) \tag{3.21}$$

Hence the voltage increase in C_S can be expressed as:

$$\Delta V_{S+(n)} = \frac{Q_{S+}}{C_S} = \frac{2C_P}{nC_S}\left(\frac{I_0 R_P}{\sqrt{1+\omega^2 R_P^2 C_P^2}} - \frac{V_S + 2V_D}{n}\right) \tag{3.22}$$

where the subscript '+(n)' means "n regions connected in series". From equation (3.6), the open-circuit peak-to-peak voltage of a PT is $V_{pp(open)} = \frac{2I_0 R_P}{\sqrt{1+\omega^2 R_P^2 C_P^2}}$. Therefore, the equation for the voltage increase of a n-region harvester connected in series can be rewritten as:

$$\Delta V_{S+(n)} = \frac{2C_P}{C_S}\left(\frac{V_{pp(open)}}{2n} - \frac{(V_S + 2V_D)}{n^2}\right) \tag{3.23}$$

By setting $n = 1, 2, 4, 8$, the voltage increase in V_S for different n can be written as:

$$\begin{aligned}
\Delta V_{S//(n=1)} &= \frac{2C_P}{C_S}\left(\frac{V_{pp(open)}}{2} - (V_S + 2V_D)\right) \\
\Delta V_{S+(n=2)} &= \frac{2C_P}{C_S}\left(\frac{V_{pp(open)}}{4} - \frac{(V_S + 2V_D)}{4}\right) \\
\Delta V_{S+(n=4)} &= \frac{2C_P}{C_S}\left(\frac{V_{pp(open)}}{8} - \frac{(V_S + 2V_D)}{16}\right) \\
\Delta V_{S+n=(8)} &= \frac{2C_P}{C_S}\left(\frac{V_{pp(open)}}{16} - \frac{(V_S + 2V_D)}{64}\right)
\end{aligned} \tag{3.24}$$

3.4.3 Performance comparison

In order to compare the performance of the monolithic PT and 2-stage series model, $\Delta V_{S+(n=2)} > \Delta V_{S//(n=1)}$ is assumed:

$$\begin{aligned}
\frac{V_{pp(open)}}{4} - \frac{(V_S + 2V_D)}{4} &> \left(\frac{V_{pp(open)}}{2} - (V_S + 2V_D)\right) \\
V_{pp(open)} &< 3(V_S + 2V_D) \quad (for\ n = 2)
\end{aligned} \tag{3.25}$$

Furthermore, $V_{pp(open)} > (V_S + 2V_D)$ should be satisfied for $n = 2$ so that the harvester can overcome the threshold voltage set by the full-bridge rectifier and start charging, so the condition for improving performance corresponding to splitting into 2 regions in series is:

Table 3.1 Simulation results (symbol '-' means 'not working')

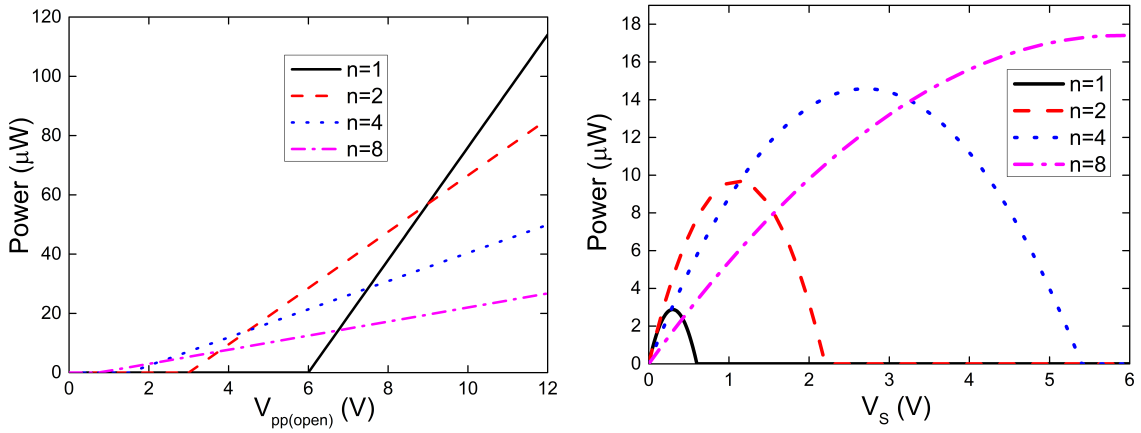
n=	1	2	4	8
$V_{pp} < 0.75V$	-	-	-	-
$0.75V < V_{pp} < 1.125V$	-	-	-	working
$1.125V < V_{pp} < 1.5V$	-	-	-	**best**
$1.5V < V_{pp} < 2.25$	-	-	working	**best**
$2.25V < V_{pp} < 3V$	-	-	**best**	working
$3V < V_{pp} < 4.5V$	-	working	**best**	working
$4.5V < V_{pp} < 6V$	-	**best**	working	working
$6V < V_{pp} < 9V$	working	**best**	working	working
$V_{pp} > 9V$	**best**	working	working	working

$$(V_S + 2V_D) < V_{pp(open)} < 3(V_S + 2V_D) \quad (for\ n = 2) \tag{3.26}$$

In terms of the monolithic model, the threshold is $V_{pp(open)} > 2(V_S + 2V_D)$ for starting charging. In addition, although the monolithic model can charge C_S while $2(V_S + 2V_D) < V_{pp(open)} < 3(V_s + 2V_D)$, the performance is worse than the 2-region series model. Using the same methodology, the conditions when $n = 4$ and $n = 8$ models have the best performance are calculated in equation (3.27). (Other values of n are also possible but the equations below facilitate comparisons with the measured results in the next section)

$$\begin{aligned} \frac{1}{2}(V_s + 2V_D) < V_{pp(open)} < \frac{3}{2}(V_s + 2V_D) \quad (for\ n = 4) \\ \frac{1}{4}(V_s + 2V_D) < V_{pp(open)} < \frac{3}{4}(V_s + 2V_D) \quad (for\ n = 8) \end{aligned} \tag{3.27}$$

By assuming $V_S = 2\,\mathrm{V}$ and the forward threshold voltage $V_D = 0.5\,\mathrm{V}$, the threshold voltage for a monolithic model is $V_{TH} = 2(V_S + 2V_D) = 6\,\mathrm{V}$. Table 3.1 shows comparisons between different series stages and Figure 3.5a illustrates theoretical output power for different excitation levels (0 g to 1 g), which are presented as the open-circuit peak-to-peak voltage $V_{pp(open)}$, varying from 0 V to 12 V, generated by the PT. This figure is generated from equations (3.24) while $V_{pp(open)}$ is considered as the variable, and other parameters are set as $C_P = 360\,\mathrm{nF}$, $C_S = 1\,\mathrm{mF}$ and $V_S = 2\,\mathrm{V}$. These values are chosen to match the experimental conditions.



(a) Theoretical output power while fixing $V_S = 2\,\text{V}$ and varying excitation level

(b) Theoretical output power while fixing excitation level $V_{pp(open)} = 3.2\,\text{V}$ and varying V_S

Fig. 3.5 Theoretical electrical power output of full-bridge rectifier for 1, 2, 4, and 8 series stages

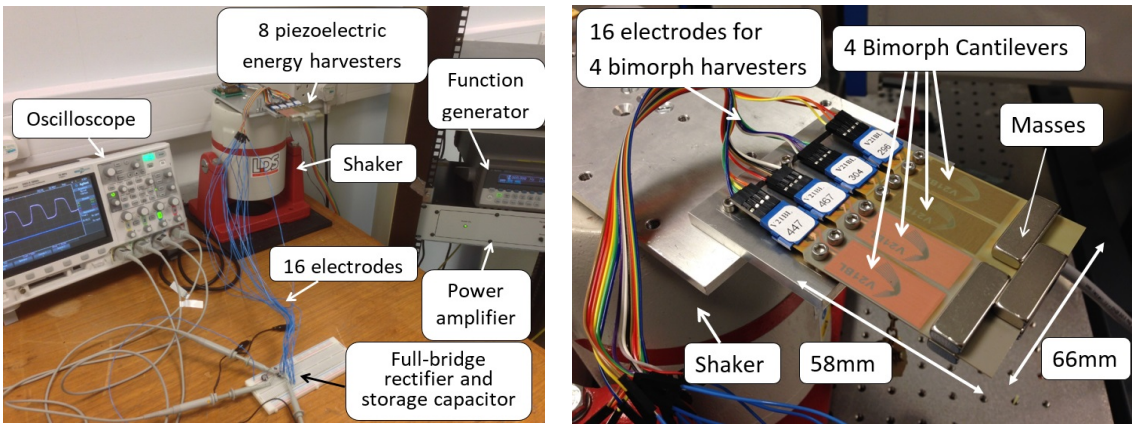
After comparing the performances with a constant V_S while changing the external excitation (changing $V_{pp(open)}$), the output power with a constant excitation level and a varying V_S needs to be examined to find the maximum power points that the rectifier can attain with different series stages. Equation (3.23) shows the voltage increase in C_S in a half cycle of I_P, so the harvested energy by the full-bridge rectifier in a half I_P cycle can be written as:

$$\Delta E_{\frac{T}{2}} = \frac{1}{2} C_S((V_S + \Delta V_S)^2 - V_S^2) \tag{3.28}$$

Hence, the output power is:

$$P = \frac{\Delta E_{\frac{T}{2}}}{T/2} = 2 f_P \Delta E_{\frac{T}{2}} = f_P C_S((V_S + \Delta V_S)^2 - V_S^2) \tag{3.29}$$

where f_P is the excitation frequency and ΔV_S is expressed in equation (3.23). The theoretical power output for $n = 1$, 2, 4 and 8 is plotted in Figure 3.5b. It can be seen that connecting the harvesters in series significantly increases the peak output power. The models with $n = 2$, $n = 4$ and $n = 8$ can theoretically increase the power by around $3\times$, $4.5\times$ and $5.5\times$, respectively, compared to the monolithic PT. According to this figure, the peak output power seems to increase and tend to a limit for higher n. However, more series stages shift the V_S value corresponding to the peak power point to higher voltages. Hence, the voltage regulator circuits placed after the FBRs should be design to handle this high input voltage. Since most of wireless sensors typically require a stable supply between 1.8 V and 3.3 V, the



(a) Experimental setup (b) PTs used in experiments

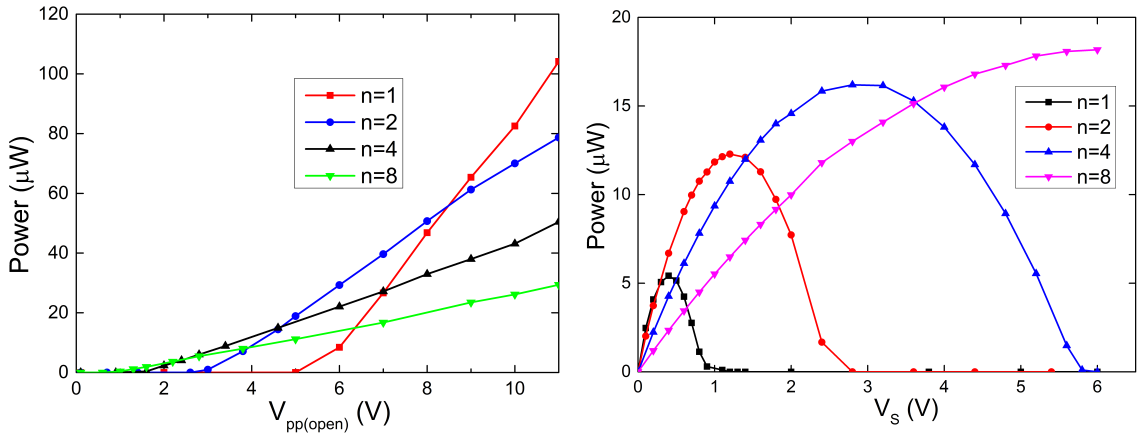
Fig. 3.6 Experimental setup.

V_S values shown in figure 3.5b can meet this requirement well; in contrast, higher V_S may increase the complexity of designing voltage regulators.

3.5 Experiments and discussions

In this section, experiments are performed to validate the theoretical results and practically shows the performance improvement of the proposed approach. Figure 3.6a shows the experimental setup. The piezoelectric transducers used in the experiments consist of four cantilevered bi-morph PTs (Mide Technology Corporation V21BL), so there are eight available PTs for experiments. The dimensions of the PTs are shown in figure 3.6b. The four bi-morph PTs are located side by side and their free-end tips are clamped together with masses in order to enable vibration in the same frequency, phase and amplitude. The resulting PT can, therefore, be considered as a monolithic PT with 8 electrode regions that can be connected in parallel or in series for different stages (n can be 1, 2, 4 or 8 in this implementation). The PT is excited on a shaker (LDS V406 M4-CE) at its natural frequency at 19 Hz and driven by a sine wave from a function generator (Agilent Technologies 33250A 80 MHz waveform generator) amplified by a power amplifier (LDS PA100E Power Amplifier). In the experiment, the storage capacitor connected at the output of full-bridge rectifier is a super capacitor of $C_S = 5.2\,\text{mF}$. A full-bridge circuit is built using four diodes with a measured forward voltage drop of around 0.5 V.

Experiments are performed with the number of series stages $n = 1, 2, 4$ and 8. Figure 3.7a shows the measured output power measured at the storage capacitor C_S for different excitation amplitudes (corresponding to $V_{pp(open)}$) with a constant $V_S = 2\,\text{V}$. For low excitation levels,



(a) Measured electrical output power while fixing $V_S = 2\,\mathrm{V}$ and varying excitation level (corresponding to base acceleration varying from 0 g to 1 g)

(b) Measured electrical output power while fixing excitation level and varying V_S (acceleration = 0.2 g, $V_{pp(open)} = 3.2\,\mathrm{V}$, $V_D = 0.5\,\mathrm{V}$)

Fig. 3.7 Measured performance of the proposed scheme

more series stages seem to perform better. For instance, when $V_{pp(open)} < 6\,\mathrm{V}$, the monolithic model ($n = 1$ while all the eight harvesters connected in parallel) does not harvest any energy as the threshold voltage is not attained. Furthermore, although all the four models can harvest energy for $6\,\mathrm{V} < V_{pp(open)} < 9\,\mathrm{V}$, the one with two series stages ($n = 2$) outputs the highest power. These results closely matches the theoretical calculations.

Figure 3.7b shows the measured electrical power while the excitation acceleration is kept at 0.2 g (corresponding to open-circuit voltage $V_{pp(open)} = 3.2\,\mathrm{V}$). The voltage V_S is varied from 0 V to 6 V to find the maximum power points for different series stages. From the figure, it can be found that the peak power values of $n = 2$, $n = 4$ and $n = 8$ models are 2.2×, 3.1× and 3.6× higher than the monolithic model ($n = 1$), respectively. The performance improvement of series models approximately matches theoretical results shown in Figure 3.5b. The differences between theoretical and experimental results are due to non-ideal diodes used in measurements, which introduce associated leakage current.

Figure 3.8 shows the measured power efficiency for different series stages while the excitation level is swept from zero to $V_{pp(open)} = 12\,\mathrm{V}$. The efficiency is calculated as the power transfered into C_S divided by the raw measured power while PT is only connected to an impedance-matched resistor. The results indicate that each series configuration can attains its peak efficiency point under a specific excitation amplitude range. In other words, for a given implementation environment with a limited range of excitation amplitude, the number of series stages n can be determined to increase the output power and efficiency. While the harvester is implemented in a low excitation environment, more series stages (higher n) are preferred; otherwise, series stages should be less (smaller n) or even not splitting the PT

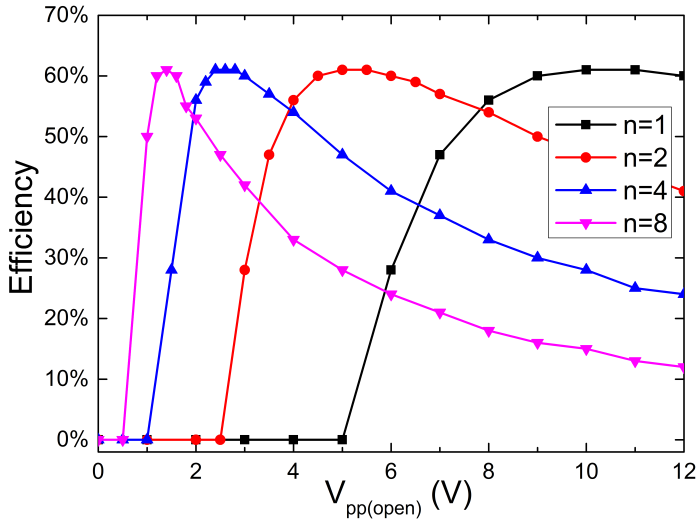


Fig. 3.8 Measured power efficiency while fixing $V_S = 2\,\mathrm{V}$ and varying excitation level

($n = 1$). This approach requires a one-time configuration of the PT to determine the number of series stages before implementations and it passively improves power efficiency without employing any active circuits.

Table 3.2 compares the performance of the proposed series connection scheme against state-of-the-art active rectification implementations for piezoelectric vibration energy harvesting. The second line in the table indicates the type of implementation. The work in this chapter does not employ additional circuits apart from a full-bridge rectifier, so there is no additional power consumption and the simplicity of the system offers the potential for increased stability. Line 5 of the table shows the peak-to-peak open-circuit voltage ($V_{pp(open)}$) produced by the PT for each work. This voltage depends on several factors, such as the excitation amplitude, piezoelectric materials, dimension of the device, internal capacitance, vibration frequency, etc. The last line of the table shows that splitting a monolithic PT into 8 regions connected in series can improve the harvested energy by up to 3.6× compared to the original monolithic harvester. According to Figure 3.7b, splitting into more stages ($n > 8$) connected in series is believed to further increase the performance, although higher n is not experimentally verified in this chapter. The performance boost from the series configurations indicates that using the proposed passive method can also achieve comparable performance compared to some active interface circuits, such as those listed in this table.

Compared to the four drawbacks mentioned in Section 3.1 for reported active interface circuits, the proposed series scheme does not employ any active circuits, inductors or capacitors other than four diodes (for a full-wave bridge rectifier). Hence the overall system volume can be significantly decreased with increased stability. In terms of quiescent power

Table 3.2 Performance comparison with reported active rectifiers

Publication	[160]	[167]	[151]	[175]	This work
Circuit implementation	Discrete	Integrated	Discrete	Discrete	Not required
Power consumption	35.2 µW	2 µW	Not given	20 µW	0
PT	RBL1-006	Mide V22B	T120-A4E-602	Mide V22B	Mide V21BL
$V_{pp(open)}$	40 V	2.4 V	5.84 V	3.28 V	3.2 V
C_P	60 nF	18 nF	33.47 nF	18 nF	42 nF
Frequency	185 Hz	225 Hz	30 Hz	225 Hz	19 Hz
Performance improvement to FBR	3.2×	4×	2×	4.5×	3.6×

loss, a simple full-bridge rectifier used in the proposed scheme does not consume any quiescent power (diode reverse leakage current is assumed to be negligible) so no energy is drained due to the interface circuit while no excitation is present. In addition, Figure 3.8 shows that the power efficiency of the proposed scheme is able to attain its peaks under a wide range of excitation amplitude for different series stages. Hence, in order to achieve an efficiency peak, the number of series stages can be pre-determined according to the average excitation amplitude where the system is implemented. This makes the energy harvesting system configurable to different implementation environments. Furthermore, as a simple full-bridge rectifier does not generate synchronized current pulses in the piezoelectric materials; hence, the proposed scheme is less subject to the SSD effect even for highly coupled PTs. Therefore, the mechanical vibration of the PTs will be less affected or damped, which extends the range over which the rectifier operates efficiently.

3.6 Conclusion

This chapter addresses that a full-bridge rectifier requires a relatively high excitation amplitude to extract energy from the piezoelectric transducer (PT). As a result, a significant part of the generated power is wasted due to the high threshold voltage. A passive scheme of splitting the electrode of a monolithic PT into n equal regions connected in series is proposed in this chapter to lower the threshold voltage and increase power output under low input excitation levels. Comparing with active interface circuits, this scheme significantly decreases system volume and increases the output power without employing active components or consuming extra power. In addition, the PTs employing this method are less affected by SSD effect. By using this principle, PTs can be designed to have n equal regions connected in series,

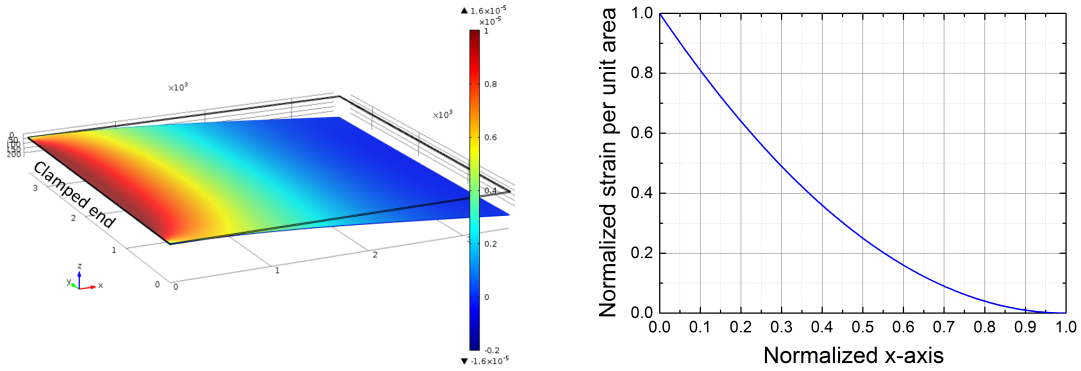
of which the number n should be pre-determined by considering the ambient excitation amplitude for the selected application environment.

Chapter 4

Electrode Design to Maximize Output Power

4.1 Introduction

This chapter is focused on analysis of electrode coverage of a piezoelectric transducer (PT) and the results show that there exists an optimal electrode coverage maximizing the AC output power of the PT. A PT can be modeled as a current source in parallel with an internal impedance. The theoretical electric power generated by a piezoelectric harvester is given as $P = \frac{1}{2} I_0^2 Z_{int}$, where I_0 is the amplitude of the current source and Z_{int} is the equivalent internal impedance of the harvester. In most of reported piezoelectric harvesters, the two electrode layers usually cover all the piezoelectric layer in order to extract as much power as possible [186, 187]. However, due to the distribution of strain in the piezoelectric layer while vibrating, the volumetric strain is higher near the clamped end and very little near the free end of the cantilever, as shown in Fig. 4.1a. Furthermore, larger electrode area means larger C_P capacitance and smaller R_P resistance, hence smaller internal impedance. Therefore, the piezoelectric area near the clamped end should obviously be covered by electrodes due to the high strain density in this area, but the electrodes do not need to cover the free end. Because of the non-uniformly distributed strain along axis x, there should exists an optimal value for the area of electrode to maximize the generated power [188, 189]. In this chapter, the optimal area of electrode layers for a maximum power output is theoretically calculated and experimentally verified with MEMS piezoelectric harvesters.



(a) COMSOL model of a cantilever with size of 3.5 mm × 3.5 mm

(b) Strain distribution on the cantilever along x-axis

Fig. 4.1 COMSOL model of a plain cantilever shows the strain is high near the clamped end and very low near the free end

4.2 Modeling of a plain cantilever

In this section, a cantilevered piezoelectric harvester is analyzed and its theoretical maximum output power is calculated to find an optimal electrode length to maximize the output power. Fig. 4.2 shows a cantilever with geometric parameters used in calculations. The length, width, thickness of the piezoelectric and substrate layers are L, W, H and h respectively. The width of the electrode layer is always W while its length starting from the clamped end is a variable x, which is the value to be determined to maximize the power output. The calculation starts from the Euler-Bernoulli Beam Theory. While the cantilever is vibrating at its first mode, the displacement along z-axis for a specific point of beam at x can approximately expressed as a polynomial:

$$EI\frac{d^4\omega(x)}{dx^4} = q(t) \tag{4.1}$$

where E, I, $\omega(x)$ and $q(t)$ represent the Young's modulus, second moment of area of the entire cantilever, displacement of a point at x and the external excitation force per unit length (N/m). The Young's modulus and second moment of area can be written as:

$$E = E_{piezo}\frac{H}{h+H} + E_{sub}\frac{h}{h+H} = \frac{E_{sub}h + E_{piezo}H}{h+H} \tag{4.2}$$

$$I = \iint z^2 dydz = \int_{-\frac{h+H}{2}}^{\frac{h+H}{2}} \int_{-\frac{W}{2}}^{\frac{W}{2}} z^2 dydz = \frac{W(h+H)^3}{12} \tag{4.3}$$

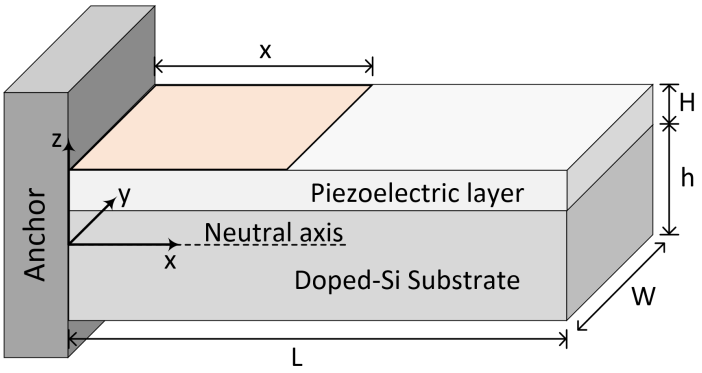


Fig. 4.2 Cantilevered piezoelectric harvester

Assuming that the excitation force is $F = F_0 \sin \omega_0 t$ and the force is uniformly distributed along x-axis, q can be expressed as:

$$q(t) = \frac{F}{L} = \frac{F_0}{L} \sin \omega_0 t \tag{4.4}$$

From the Euler-Bernoulli Beam Theory in Eq. (4.1), $A = \frac{q}{EI}$ is set for simplifying the calculation because it is independent of x, y or z. Hence:

$$\frac{d^4\omega(x)}{dx^4} = \frac{q}{EI} = A \tag{4.5}$$

By integrating Eq. (4.5), hence:

$$\Rightarrow \frac{d^3\omega(x)}{dx^3} = Ax + C_1 \tag{4.6}$$

$$\Rightarrow \frac{d^2\omega(x)}{dx^2} = \frac{1}{2}Ax^2 + C_1x + C_2 \tag{4.7}$$

$$\Rightarrow \frac{d\omega(x)}{dx} = \frac{1}{6}Ax^3 + \frac{1}{2}C_1x^2 + C_2x + C_3 \tag{4.8}$$

$$\Rightarrow \omega(x) = \frac{1}{24}Ax^4 + \frac{1}{6}C_1x^3 + \frac{1}{2}C_2x^2 + C_3x + C_4 \tag{4.9}$$

According to Dirichlet Boundary Conditions, initial conditions can be set as $\omega' = \omega = 0$ at the clamped end and $\omega''' = \omega'' = 0$ at the free end. Therefore, the following four equations is formed:

$$\begin{aligned} \frac{d^3\omega(L)}{dx^3} &= 0 \\ \frac{d^2\omega(L)}{dx^2} &= 0 \\ \frac{d\omega(0)}{dx} &= 0 \\ \omega(0) &= 0 \end{aligned} \tag{4.10}$$

With the four equations in Eq. (4.10), it can be solved that $C_1 = -AL$, $C_2 = \frac{1}{2}AL^2$, $C_3 = 0$, $C_3 = 0$. Replacing the parameters in Eqs. (4.9) and (4.7), so:

$$\omega(x) = \frac{1}{24}Ax^4 - \frac{1}{6}ALx^3 + \frac{1}{4}AL^2x^2 \tag{4.11}$$

$$\frac{d^2\omega(x)}{dx^2} = \frac{1}{2}Ax^2 - ALx + \frac{1}{2}AL^2 \tag{4.12}$$

For a symmetrical bending, the tensile stress experienced by the beam can be expressed as:

$$\sigma_{(x,y,z)} = \frac{Mz}{I} \tag{4.13}$$

where M is the bending moment which is given by $M = -EI\frac{d^2\omega(x)}{dx^2}$, I is the second moment of area calculated in Eq. (4.3), so the stress can be written as:

$$\begin{aligned} \sigma_{(x,y,z)} = -zE\frac{d^2\omega(x)}{dx^2} &= -zE(\frac{1}{2}Ax^2 - ALx + \frac{1}{2}AL^2) \\ &= -z\frac{q}{I}(\frac{1}{2}x^2 - Lx + \frac{1}{2}L^2) \end{aligned} \tag{4.14}$$

Where $\sigma_{(x,y,z)}$ is the stress per unit area ($\mathrm{N/m^2}$) and its variable z starts from the neutral axis as shown in Fig. 4.2. In order to convert the kinetic energy to electrical energy, the piezoelectric charge constant d_{31} needs to be used. Therefore, the amount of charge generated by the strain is expressed as:

$$Q_{(x,y,z)} = d_{31}\sigma_{(x,y,z)} = -zd_{31}\frac{q}{I}(\frac{1}{2}x^2 - Lx + \frac{1}{2}L^2) \tag{4.15}$$

This is the charge generated per unit area $dxdy$ in the piezoelectric material. In order to calculate the total charge across the two electrode layers $z_{bottom} = \frac{h-H}{2}$ and $z_{top} = \frac{h+H}{2}$

(assuming the substrate is thicker than the piezoelectric layer, $h > H$), Eq. (4.15) needs to be integrated along x, y:

$$Q_{total} = \int_0^x \int_o^W Q_{(x,y,z)} dydx \Big|_{z=\frac{h-H}{2}}^{z=\frac{h+H}{2}} \tag{4.16}$$

$$\begin{aligned} \Rightarrow Q_{total} &= \int_0^x \int_o^W -Hd_{31}\frac{q_{(t)}}{I}(\frac{1}{2}x^2 - Lx + \frac{1}{2}L^2)dydx \\ &= -q_{(t)}d_{31}\frac{WH}{I}(\frac{1}{6}x^3 - \frac{1}{2}Lx^2 + \frac{1}{2}L^2x) \end{aligned} \tag{4.17}$$

According to equation 4.4, the excitation force $q_{(t)}$ is a function of time $q = \frac{F_0}{L}\sin\omega_0 t$. Hence, the total generated charge is:

$$Q_{total} = -d_{31}\frac{F_0}{L}\frac{WH}{I}(\frac{1}{6}x^3 - \frac{1}{2}Lx^2 + \frac{1}{2}L^2x)\sin\omega_0 t \tag{4.18}$$

A piezoelectric harvester can be modeled as a current source I_P in parallel with a capacitor C_P and a resistor R_P. The capacitor C_P together with the resistor R_P can be considered as the internal impedance Z_P of the harvester. In order to calculate the generated power by the harvester, it is needed to calculate I_P, C_P and R_P. The calculation starts from determining I_P. As the total charge between the two electrodes is found in Eq. (4.18), the generated current can be deduced by calculating the derivative of charge to time.

$$\begin{aligned} I_P = \frac{dQ_{total}}{dt} &= -d_{31}\frac{F_0\omega_0}{L}\frac{WH}{I}(\frac{1}{6}x^3 - \frac{1}{2}Lx^2 + \frac{1}{2}L^2x)cos(\omega_0 t) \\ &= I_0 cos(\omega_0 t) \end{aligned} \tag{4.19}$$

$$\left(with\ I_0 = -d_{31}\frac{F_0\omega_0}{L}\frac{WH}{I}(\frac{1}{6}x^3 - \frac{1}{2}Lx^2 + \frac{1}{2}L^2x)\right)$$

The capacitance and resistance can be expressed in Eq. (4.20) and Eq. (4.21) according to the mechanical size of electrodes.

$$C_P = \varepsilon_r\varepsilon_0\frac{xW}{H} \tag{4.20}$$

$$R_P = \rho\frac{H}{xW} \tag{4.21}$$

In the equations, ε_r and ε_0 represent dielectric constant of piezoelectric material and electric constant respectively; ρ is the electrical resistivity of piezoelectric material. Therefore, the internal impedance can be expressed as:

$$Z_p = C_P//R_P = |\frac{\frac{R_P}{2\pi C_P}}{R_P + \frac{1}{j\omega_0 C_P}}| = \frac{\rho}{\sqrt{1+\omega_0^2\varepsilon_r^2\varepsilon_0^2\rho^2}}\frac{H}{xW} \tag{4.22}$$

The generated power by the harvester is:

$$P_0 = \frac{1}{2}I_0^2 Z_p \tag{4.23}$$

$$\Rightarrow P_0 = \frac{1}{2}\Big(-d_{31}\frac{F_0\omega_0}{L}\frac{WH}{I}(\frac{1}{6}x^3 - \frac{1}{2}Lx^2 + \frac{1}{2}L^2x)\Big)^2 \frac{\rho}{\sqrt{1+\omega_0^2\varepsilon_r^2\varepsilon_0^2\rho^2}}\frac{H}{xW} \tag{4.24}$$

$$\Rightarrow P_0 = d_{31}^2F_0^2\omega_0^2\frac{WH^3}{2I^2L^2}\frac{\rho}{\sqrt{1+\omega_0^2\varepsilon_r^2\varepsilon_0^2\rho^2}}x(\frac{1}{6}x^2 - \frac{1}{2}Lx + \frac{1}{2}L^2)^2 \tag{4.25}$$

From Eq. (4.3), the expression of the second moment of area is $I = \frac{W(h+H)^3}{12}$, Hence:

$$\begin{gathered} P_0 = B(\frac{1}{36}x^5 - \frac{1}{6}Lx^4 + \frac{5}{12}L^2x^3 - \frac{1}{2}L^3x^2 + \frac{1}{4}L^4x) \\ \Big(with\ B = d_{31}^2F_0^2\omega_0^2\frac{72H^3}{WL^2(h+H)^6}\ \frac{\rho}{\sqrt{1+\omega_0^2\varepsilon_r^2\varepsilon_0^2\rho^2}}\Big) \end{gathered} \tag{4.26}$$

The expression of the generated electrical power by the piezoelectric harvester is given in Eq. (4.26) and it is a function of x. The normalized power is plotted in the dash line in Fig. 4.3 and the horizontal axis is the normalized x axis along the cantilever where $x = 0$ is the anchor and $x = 1$ is the free end. The dash-dot line in the figure shows the normalized strain along the x-axis and its expression is given in Eq. (4.14). It can be seen that the output electrical power of a plain cantilever reaches its peak at $x \approx 0.44L$, which means the electrode layer covering 44% of the cantilever from the clamped end maximizes the power.

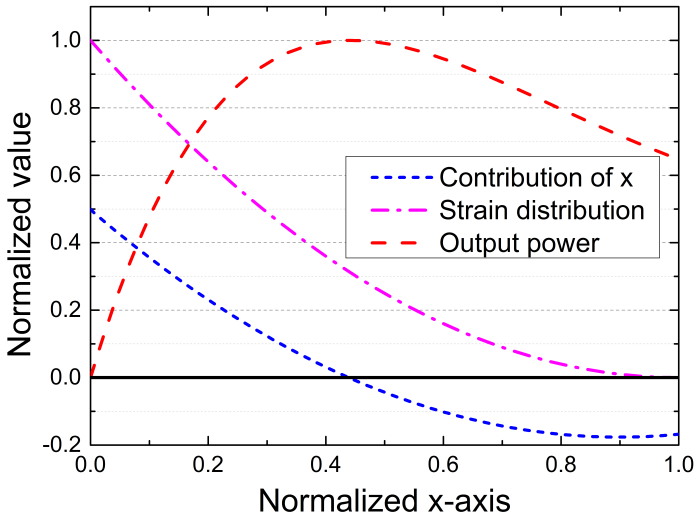


Fig. 4.3 Simulation results

4.3 Modeling of a structure with arbitrary strain distribution

In order to increase the generated power and adjust frequency bandwidth of piezoelectric harvesters (PH), different structures of harvesters have been proposed. Tip masses are added in many cantilevered harvesters to tune the natural frequency and increase output power [182, 140, 39]. Other structures, such as clamped-clamped beams [99, 29] and more complicated structures [32, 123] have also been presented in recent years for output power and bandwidth enlargement purposes. The electrode design rule for a plain cantilever is calculated in the previous section; however, it is important to find a generalized rule on designing the electrodes for different structures of PHs to maximize the output power.

This section presents a generalized method to analyze the optimal electrode coverage for any kind of structure. Fig. 4.4 shows a piezoelectric harvester, in which the strain distributed along x is assumed to be arbitrary and decreasing. The reason of using the arbitrary strain distribution is to make the model working for any kind of structure, such as cantilever, clamp-clamp beam, etc.

The highest strain is at the clamped end. It is assumed first that the electrode layer covers a region 1 of length L. The region 1 is then increased by a very small region 2, with length e, where $e \ll L$. The analysis turns to calculate if the output power of region 1+2 is greater or less than that of the region 1; so that it can be found if it worths to increase the region 1 and if the region 1 is the optimal electrode coverage.

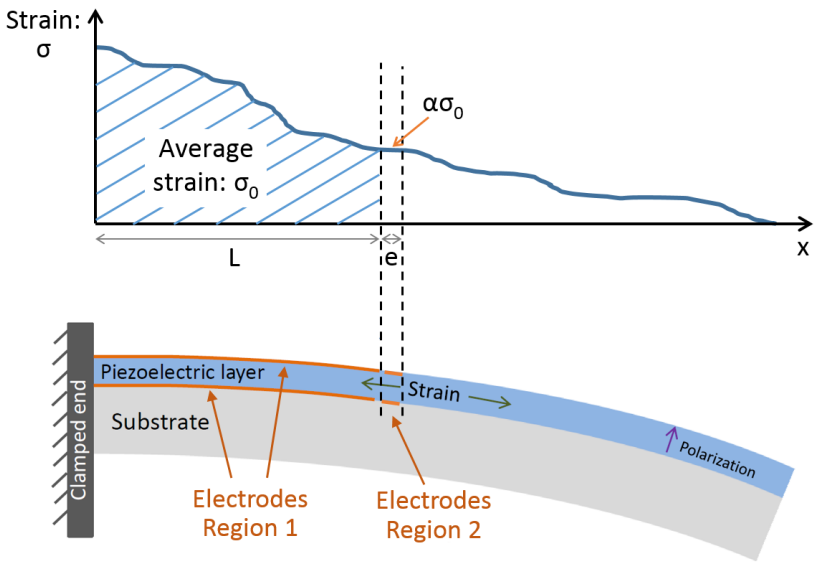


Fig. 4.4 A piezoelectric vibration energy harvester with arbitrary decreasing strain along axis x (L is the length of the electrode region 1 and e is the length of an extract electrode region 2, where $e \ll L$. the average strain in the region 1 is noted as σ_0, α is a factor between 0 and 1 and $\alpha\sigma_0$ is the strain for the small region 2)

It is assumed that σ_0 is the average strain per unit length in the region 1 and $\alpha\sigma_0$ is the strain per unit length in region 2, where α satisfies $0 < \alpha < 1$. In the following parts, the output power values generated by the electrode coverage of region 1 and region 1+2 are separately calculated and compared to find the contribution of the additional electrode area in region 2.

4.3.1 Output power with electrode covering region 1

As the average strain per unit length in the region 1 is σ_0, the total strain in this region is expressed as:

$$\sigma_1 = \sigma_0 L \sin \omega t \tag{4.27}$$

where ω is the excitation frequency. The total charge generated in region 1 is:

$$Q_1 = d_{31}\sigma_0 L \sin \omega t \tag{4.28}$$

The equivalent current source can be written as:

$$I_1 = \frac{\mathrm{d}Q_1}{\mathrm{d}t} = \omega d_{31}\sigma_0 L \cos \omega t \tag{4.29}$$

Assuming the inherent capacitance per unit length of the electrode is C_0, the capacitance for region 1 is $C_1 = C_0 L$. The internal impedance for region 1 while the PVEH is vibrating is expressed as:

$$|Z_1| = \frac{1}{\omega C_0 L} \tag{4.30}$$

Therefore, according to the equations Eq. (4.29) and Eq. (4.30), the output power while the electrode only covers the region 1 is calculated as:

$$P_1 = \frac{\omega^2 d_{31}^2 \sigma_0^2 L^2}{2} \frac{1}{\omega C_0 L} = \frac{\omega d_{31}^2 \sigma_0^2 L}{2C_0} \tag{4.31}$$

4.3.2 Output power with electrode covering regions 1+2:

After obtaining the output power with electrode overing only the region 1, the small region 2 is added in this section to see how this additional electrode coverage contributes to the total output power. As the strain per unit length in the region 2 is expressed as $\alpha\sigma_0$, which is shown in Fig. 4.4, the total strain in regions 1+2 is:

$$\sigma_{1+2} = \sigma_0 L \sin \omega t + \alpha \sigma_0 e \sin \omega t \tag{4.32}$$

The total charge generated in regions 1+2 can be expressed as:

$$Q_{1+2} = (L + \alpha e)\sigma_0 d_{31} \sin \omega t \tag{4.33}$$

Hence, the equivalent current source for the electrode covering regions 1+2 is:

$$I_{1+2} = \frac{\mathrm{d}Q_{1+2}}{\mathrm{d}t} = \omega(L + \alpha e)\sigma_0 d_{31} \cos \omega t \tag{4.34}$$

The inherent capacitance and internal impedance formed by of electrode in regions 1+2 are expressed as:

$$C_{1+2} = C_0(L+e) \Rightarrow |Z_{1+2}| = \frac{1}{\omega C_0 (L+e)} \tag{4.35}$$

According to equations Eq. (4.34) and Eq. (4.35), the output power for a PVEH with electrode covering region 1+2 is:

$$P_{1+2} = \frac{\omega^2 d_{31}^2 \sigma_0^2 (L+\alpha e)^2}{2} \frac{1}{\omega C_0 (L+e)} = \frac{\omega d_{31}^2 \sigma_0^2 (L+\alpha e)^2}{2C_0 (L+e)} \tag{4.36}$$

4.3.3 Contribution analysis of additional electrode coverage in region 2

In order to find how the additional electrode in the region 2 contributes to the total output power of the PVEH, the output power calculated in equations Eq. (4.31) and Eq. (4.36) are compared:

$$\begin{aligned} P_{1+2} &> P_1 \\ \Rightarrow \frac{\omega d_{31}^2 \sigma_0^2 (L+\alpha e)^2}{2C_0(L+e)} &> \frac{\omega d_{31}^2 \sigma_0^2 L}{2C_0} \\ \Rightarrow \frac{(L+\alpha e)^2}{L+e} &> L \\ \Rightarrow L^2 + \alpha^2 e^2 + 2L\alpha e &> L^2 + Le \\ \Rightarrow \alpha^2 e^2 + 2\alpha Le &> Le \\ \Rightarrow \alpha^2 \frac{e}{L} + 2\alpha &> 1 \end{aligned} \tag{4.37}$$

Since the region 2 is assumed to be much smaller than the region 1 ($e \ll L$), so $e/L \approx 0$. After applying this approximation into the result of equation Eq. (4.37), the variable α can be found as:

$$\alpha > 0.5 \tag{4.38}$$

The above result implies that the additional electrode in region 2 will increase the total output power of the PVEH only if the unit strain in this region is greater than a half of the average strain in region 1. If the unit strain at the edge of the region 1 equals to the half of the average strain in region 1, the existing electrode is the optimal coverage outputting maximum electrical power and any additional electrode will decrease the total power. Hence, in order to maximize the output power of the piezoelectric energy harvester, the electrode layer should cover from the peak strain end to a position, where the unit strain in this position is a half of the average strain of the area covered by the electrode layer.

Fig. 4.3 shows the simulation results for a plain cantilevered piezoelectric energy harvester. The short-dash line is the normalized strain $\sigma(x)$ per unit length along the x axis, which is expressed in Eq. (4.14). The dash-dot line represents the contribution to the total output power of an additional region 2 at the position x. This line is plotted according to the function $Contribution = \sigma(x) - \frac{\int_0^x \sigma(x)\,\mathrm{d}x}{2}$, which represents the difference between the unit strain at x and a half of the average strain before x. The strain $\sigma(x)$ in the function is given

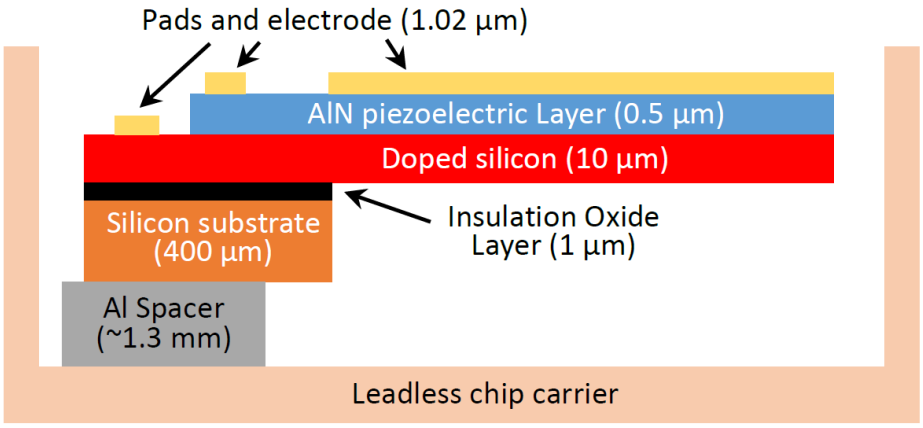


Fig. 4.5 MEMS device fabrication process

in Eq. (4.14). This function is formed according to the result obtained in the equation Eq. (4.38). From the dash-dot line, it can be seen that the contribution of electrode at a specific x keeps positive for $x < 0.44$ and it goes to negative for $x > 0.44$, which implies that 44% is the optimal electrode coverage for a plain cantilevered PVEH. This result matches the peak output power of the dash line, which is calculated from the Euler-Bernoulli Beam Theory.

In the next section, two MEMS devices have been fabricated and experimentally tested to verify the results obtains in the calculations.

4.4 Experimental Validation

In this section, two piezoelectric harvesters (PH) of different structures are fabricated in MEMS process to experimentally validate the theoretical calculations. Both MEMS devices are fabricated using the MEMSCAP piezoMUMPs fabrication technology, which involves a 400 µm silicon substrate, a 10 µm doped silicon layer, a 0.5 µm AlN (Aluminum Nitride) piezoelectric layer and a 1.02 µm electrode layer. The process is illustrated in Fig. 4.5. The MEMS device to be tested is clamped in a chip socket, which is fixed on a shaker. The shaker (LDS V406 M4-CE) is excited at the natural frequency of each MEMS device and driven by a sine wave from a function generator (Agilent Technologies 33250A 80 MHz waveform generator) amplified by a power amplifier (LDS PA100E Power Amplifier).

4.4.1 MEMS plain cantilever

The first device to be tested is a plain cantilever without a proof mass, which is shown in Fig. 4.6. The size of the cantilever is 3.5 mm $\times$ 3.5 mm and the electrode layer is split into

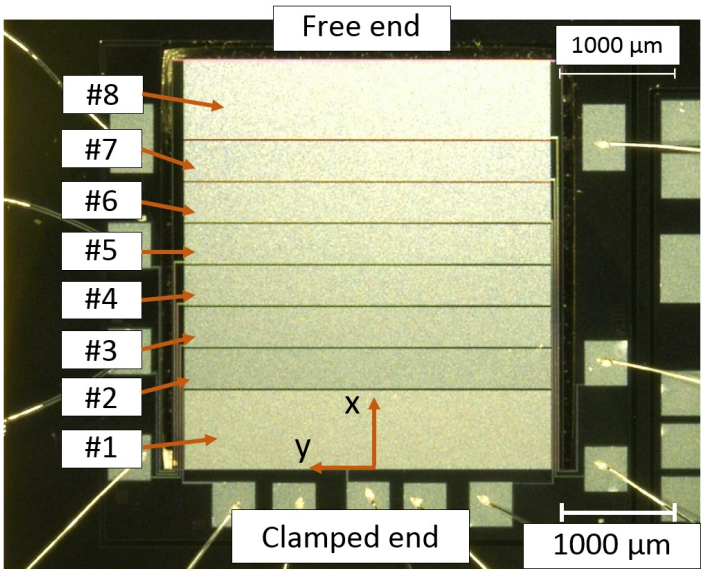


Fig. 4.6 Microscopic view of a MEMS plain cantilevered PVEH

8 segments. From region #1 to region #8, they sequentially occupy 20%, 10%, 10%, 10%, 10%, 10%, 10% and 20% respectively, of the total length of the cantilever. The device in the figure contains 12 electrode pads where there are 8 pads for 8 regions and 4 pads for ground. The natural frequency of the cantilever is 1208 Hz and the input acceleration level for the experiment is 0.5 g.

Experiments are performed in two steps. The first step is using the theoretical result obtained in Eq. (4.38) to estimate the optimum electrode coverage: the open-circuit voltage of each individual electrode is measured to detect the electrode on which the voltage is half of the average voltage on the previous electrodes. The second step consists in gradually increasing the electrode area by adding regions from #1 to #8 and measuring the output power to find the optimal electrode coverage. For each measurement point, the load resistor is adjusted to match the internal impedance. The result is then compared with step 1 to validate the theoretical calculations.

Table 4.1 shows the measured open-circuit voltage and contribution for each individual region from #1 to #8 and the measured output power while gradually adding the electrodes from #1 to #8. The results are plotted in Fig. 4.7, where the x axis is presented in Fig. 4.6. The measured values of open voltage and contribution for the eight regions correspond to the positions at the centers of the regions, which are x = 0.1, 0.25, 0.35, 0.45, 0.55, 0.65, 0.75 and 0.9. The contribution value, for region #6 for example, is the voltage value at region #6 minus the half of the average value of all previous regions. This is expressed as: $Contribution_6 = V_6 - \frac{1}{2}\frac{\sum_{i=1}^{5} V_i}{5}$. Although the condition in equation Eq. (4.38) is calculated

Table 4.1 Measured open-circuit voltage and output power contribution for each region of the MEMS cantilever PVEH (frequency: 1208 Hz, acceleration: 0.5 g)

Region	Capacitance (nF)	Open-circuit voltage (mV)	Contribution to power	Output power (nW)
#1	0.464	970	485.0	140
#2	0.294	661	176.0	180.6
#3	0.27	507	99.3	214.1
#4	0.273	389	32.7	222
#5	0.272	291	-24.9	213.2
#6	0.272	193	-88.8	199.5
#7	0.272	92	-158.9	189.6
#8	0.472	23	-198.6	153.6

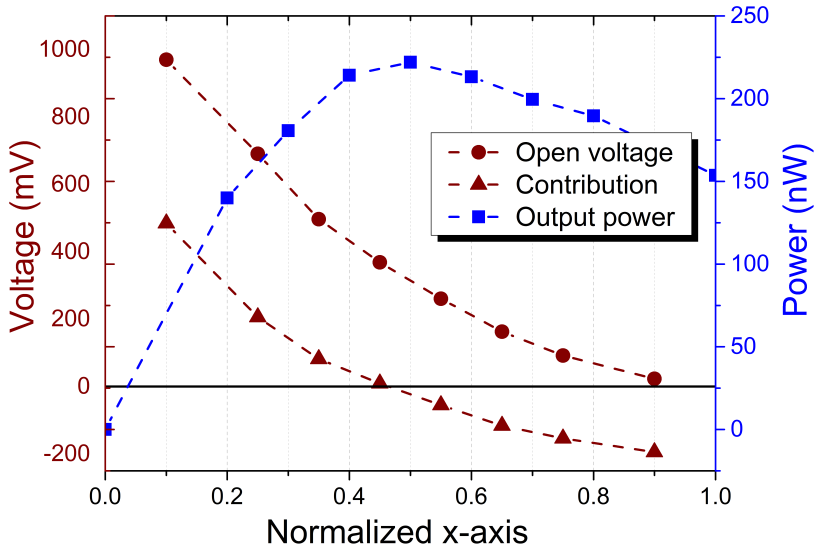


Fig. 4.7 Measured results for MEMS plain cantilevered PVEH

in terms of strain, open-circuit voltage is used to represent the strain here. Indeed, the open-circuit voltage is proportional to the generated charge, which is proportional to the total strain in a region. Positive values in the "Power contribution" column means adding these regions into the electrode can increase the output power. It can be seen from the figure that the "contribution" line crosses zero at around $x = 0.48$, which means a 48% electrode coverage is the theoretical optimal electrode side to maximize the output power. The peak power measured in step 2 is found at around 50% or slightly smaller if applying a polynomial fitting, which closely matches the results read from the contribution line.

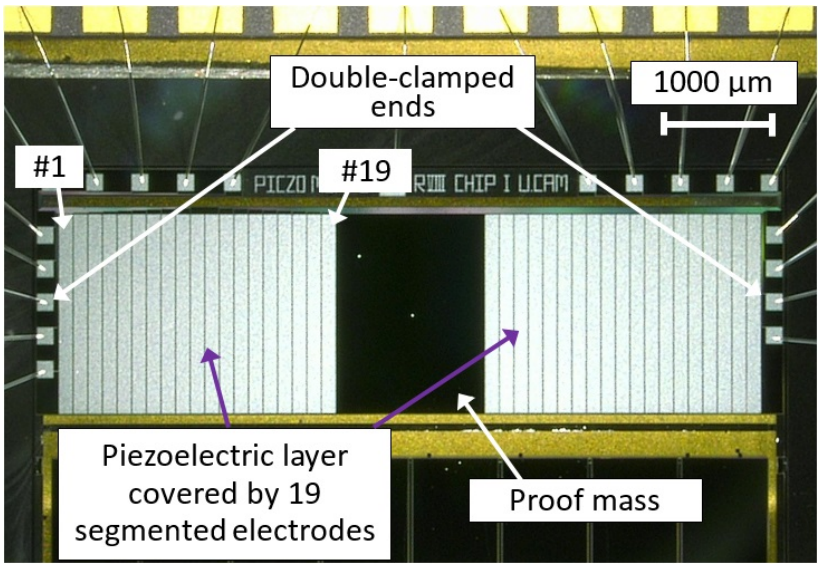


Fig. 4.8 Microscopic view of a MEMS double-clamped beam PVEH with a centered proof mass

4.4.2 MEMS double-clamped beam

The second MEMS device to be tested is shown in Fig. 4.8. This is a double-clamped beam PVEH where the left and right sides of the beam are clamped and a proof mass is suspended in the center. For each side of the beam, the electrode layer is segmented into 19 pieces, hence 38 pieces in total for both sides. As the strain distribution for both sides is theoretically symmetric, only the 19 electrode pieces on the left side of the beam are routed out to 19 pads. The other 19 pieces on the right side are not connected and they are designed to keep the mechanical symmetry of the device. The electrode regions to be tested are labeled from #1 to #19.

Similar to the previous experiments on the plain cantilever, the measurements on this device are also performed in two similar steps. In the first step, the double-clamped beam is excited at its natural frequency 1430 Hz under an excitation level of 0.5 g. The optimal electrode is estimated according to the theoretical calculations, by measuring the open-circuit voltage for each of the 19 regions. In the send step, the output power is directly measured as a function of the electrode length, to validation the results obtained in step 1. In comparison with a cantilever, the strain distribution in a clamped-clamped beam is not continuously decreasing along the length of the beam. From region #1, it decreases until it attains zero in the near center (region #10) and increase until region #19. Taking that into account, step 2 of experiments is performed in two sub-steps: increasing the electrode from #1 to #10 in a first part, and from #19 to #11 in a second part. Hence, the experiments are performed by

Table 4.2 Measured open-circuit voltage and output power contribution for each region of the MEMS clamped-clamped beam PVEH (frequency: 1430 Hz, acceleration: 0.5 g)

Region	Capacitance (nF)	Open-circuit voltage (mV)	Contribution to power	Output power (nW)
#1	0.111	1210	605	91.22
#2	0.118	1070	465	172.15
#3	0.113	944	374	219.75
#4	0.113	821	283.7	259.44
#5	0.113	677	171.4	282.84
#6	0.113	544	71.8	293.13
#7	0.115	410	-28.8	297.07
#8	0.116	272	-133.4	287.93
#9	0.117	149	-222.8	271.24
#10	0.119	23	-315.7	250.16
#11	0.123	46	-293.6	230.36
#12	0.121	180	-195.3	250.67
#13	0.12	331	-79.3	265.61
#14	0.121	478	33.5	274.33
#15	0.117	606	126.1	259.50
#16	0.113	749	234	233.68
#17	0.119	890	340	212.58
#18	0.121	1020	430	164.35
#19	0.119	1180	590	93.00

considering the regions #1 to #19 as two parts: one part from #1 to #10 and the other part #19 to #11.

Table 4.2 shows the measured open-circuit voltage, contribution value for each of the 19 regions and the output power for the two parts of electrode regions and the results are plotted in Fig. 4.9. The formula for calculating the contribution values is the same as the one used in the previous cantilever measurements but the contribution points in the left and right parts are calculated from regions #1 and #19, respectively. According to the figure, the contribution crosses zero between #6 and #7, and then again between #13 and #14. The results indicates that the regions from #7 to #13 have negative contributions to the output and they should not be added into electrode design.

Regarding the left part of the output power, it can be seen that it reaches a peak at region #7, and adding any further regions decreases the output power. Similarly, for the right part, gradually increasing electrode coverage from #19 increases the output power until it reaches its peak at #14, and any additional regions will decease the power. The two peaks of the

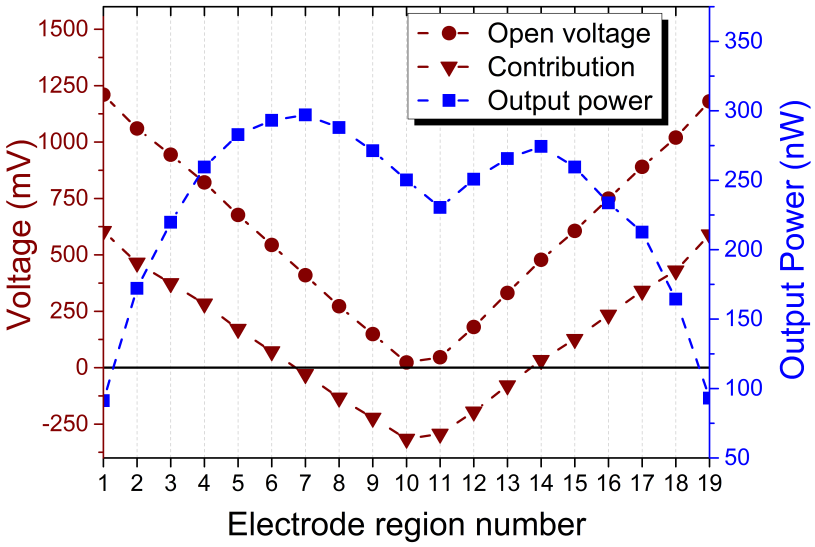


Fig. 4.9 Measured results for MEMS double-clamped beam PVEH

output power closely match the two points where the contribution line crosses zero, and thus validate the theoretical calculation for the clamped-clamped beam.

The output power for all the regions #1 to #19 is the sum of the power obtained from the left and right part and the total output power of the double-clamped beam energy harvester should be further multiplied by 2 as there are identical 19 electrode regions on the other side of the structure, as shown in Fig. 4.8

4.4.3 Discussion

According to the results of the plain cantilever in Fig. 4.7, if the electrode covers the entire area (100% coverage), the resulting output power is 153.6 nW. However, the proposed design on the electrode increases the power to 222 nW with an output power improvement of 144.5%. For the results of the double-clamped beam in Fig. 4.9, the total estimated output power for the entire device is 936 nW (twice the sum of power at #10 and #11) while all the electrode regions are used. If the electrodes are optimized, the output power can achieve 1178 nW (twice of the sum of power at the two peaks). The power improvement is around 126%.

4.5 Conclusion

In this chapter, theoretical calculations were performed to find an optimal electrode area for maximizing output power of a PVEH. The results show that maximizing active area does not

always increase output power; in the contrast, power can be reduced if the low-strain area is covered. According to the calculations, the low-strain area is defined as an area, where the strain is less than a half of the average strain in other high strain areas. This result can also be interpreted as the optimal electrode coverage for maximizing the output power of a PVEH is the coverage from the peak strain area to a place, where the strain is equal to a half of the average strain in all the previously covered high-strain area. With the proposed electrode design, the output power can be improved by 145% and 126% for cantilevers and clamped-clamped beams, respectively. The theoretical calculations are validated with measured results based on a MEMS cantilevered harvester and a MEMS double-clamped beam harvester and the discrepancy between the theoretical and experimental results were explained. The reason of the using two different MEMS devices is to validate that the calculated results can be applied to different structures with different strain distributions.

According to the results of this chapter, while designing a piezoelectric vibration energy harvester (PVEH) at either macroscopic or MEMS scale, the active electrode layer does not necessarily need to cover the entire piezoelectric layer. Before fabricating the PVEHs, simulation results on the strain distribution can be used to find the approximate optimal electrode coverage and apply this consideration in the design to maximize the output power. This design approach can also be applied to other structural topologies and mode shapes for piezoelectric vibration energy harvesters.

Chapter 5

An Inductorless Dynamically Configured Interface Circuit

5.1 Introduction

In order to increase the power efficiency of a VEH system, most of active rectifiers seek to develop a mechanism to minimize the energy wasted in charging C_P. An SSHI (Synchronized Switch Harvesting on Inductor) rectifier was presented in [163] to employ an inductor to flip the voltage V_{piezo} at zero-crossing points of I_P. Chip and board level measurements of SSHI rectifiers have been previously implemented in [167, 175] to demonstrate their high power efficiency. Other synchronized switch interfaces, such as Synchronous Electric Charge Extraction (SECE), are also widely used for high-efficiency circuits [190].

Although SSHI and SECE rectifiers can transfer most of the generated charge to a storage capacitor under specific conditions, they have a few main drawbacks that need to be mentioned. First, SSHI and SECE circuits require inductors, which must be implemented off-chip to achieve good performance and such an inductor can be the main factor in increasing the overall volume of the energy harvesting system. In addition, SSHI circuits can only achieve high efficiency over a limited range of excitation levels. This limits the overall performance of the circuit in real-world implementations, where the excitation level varies with time unpredictably in a wide range. Although this is not an issue for an SECE circuit due to its different architecture to extract energy, it requires more complex circuits to be implemented compared to other circuits. Furthermore, SSHI and SECE can only provide higher performance than simple full-bridge rectifiers for weakly coupled piezoelectric transducers due to the synchronized switch damping effect. If the the coupling is strong and the PT vibrates at resonance, the periodic current pulses applied to invert (for

SSHI) or extract (for SECE) charge on a PT result in an electrical actuation that opposes the vibration, which is known as Synchronized Switch Damping (SSD) [176, 177]. Due to the relatively strong nonlinear damping introduced, this principle has also been used for wave reflection/transmission reduction [191], where an architecture similar to SSHI was used to perform the charge inversion to increase the electrical actuation. This negative force feedback is basically introduced by the first harmonic of the current pulses. If the current pulses are lower and wider (lower amplitude and lower first harmonic frequency), the SSD becomes less significant and synchronized switch circuits can thus transfer charge. All of the above limitations introduced by inductors, real-world wide range excitation levels and SSD effect result in the SSHI and SECE rectifiers achieving acceptable performance only in a limited operating range.

This chapter proposes a fully integrated CMOS interface circuit interfaced to a bimorph PT to automatically switch the connection of the two PTs to increase output power based on the amplitude of the input excitation, thereby enabling a significant improvement in power extraction efficiency for the immediate electrical interface. With the proposed circuit, the two PTs are connected in parallel or in series according to the environmental excitation level by periodically evaluating the excitation amplitude. As compared to the SSHI or SECE rectifiers, the proposed circuit does not employ any inductor, which significantly decreases the expected overall volume of the system, especially for MEMS low-volume energy harvesters. In addition, dynamically switching between parallel and series configurations allows the energy harvester to achieve a high power efficiency over a wide range of input excitation amplitudes. In terms of the SSD problems for SSHI and SECE rectifiers, the proposed circuit enables shifting between different configurations instead of performing synchronized charge inversion or extraction. Hence it avoids introducing negative force feedback and it is less subject to the SSD introduced by the circuit, which extends the range over which the circuit can operate efficiently.

This chapter consists of six sections presenting the proposed circuit covering modeling and experimental validation. In the next section, parallel and series connections of two PTs are theoretically studied to identify the conditions when one configuration is working better than the other one. Identifying the switching condition between parallel and series models is very important to implement the associated algorithms in designing the circuit. The third section gives an overall description of the proposed interface circuit and the fourth section provides details of the circuit implementation of each functional block of the system. The fabricated chip is experimentally evaluated in the fifth section and the final section provides a summary and conclusion.

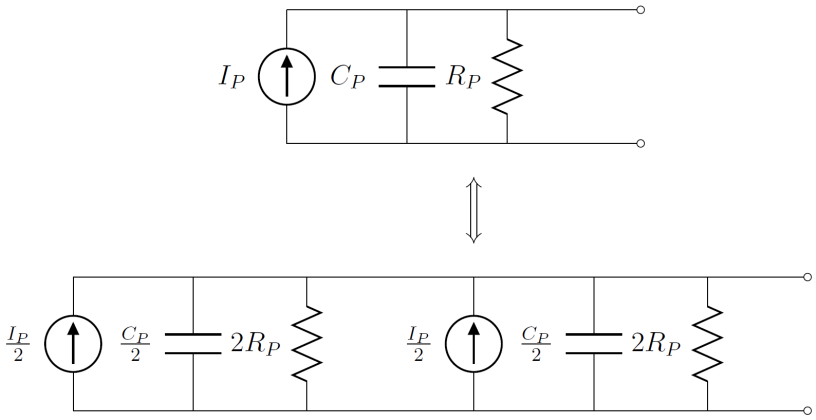


Fig. 5.1 A monolithic PT (top) and two PTs connected in parallel (bottom).

5.2 Modeling of parallel and series configurations

In this section, theoretical models are developed to compare the performance between parallel and series connections of a bimorph cantilever. In order to compare the performance, there are two methods to evaluate the output power from the both models. One way is to change excitation amplitude (corresponding to voltage V_{piezo}) with a fixed V_S; another way is to change the voltage V_S for a fixed excitation amplitude. The proposed rectifier aims to choose an appropriate connection type according to both excitation amplitude and V_S value to maximize output power.

5.2.1 Parallel model

As the two piezoelectric transducers (PT) are located on the both sides of a single bimorph cantilever, they have exactly the same frequencies, amplitudes and phases. While the two PTs are connected in parallel, the parallel model can be considered as a $2\times$ larger monolithic PT with frequency, amplitude and phase unchanged, see Fig. 5.1. Assuming the excitation is sinusoidal, the current source, capacitor and resistor for the resulting parallel model can be written as $I_P = I_0 \sin 2\pi f_P t$, C_P and R_P. Hence, the corresponding parameters for one single PT are $\frac{1}{2}I_P$, $\frac{1}{2}C_P$ and $2R_P$. For the parallel model, the total generated charge in a half cycle T/2 should first be calculated and can be written as:

$$Q_{total} = \int_0^{\frac{T}{2}} I_0 \sin \omega t \mathrm{d}t = \frac{2I_0}{\omega} \tag{5.1}$$

Before the full-bridge rectifier becomes conducting, the current from I_P is split into two parts inside the piezoelectric harvester, I_C and I_R flowing through the capacitor and resistor respectively (see Fig. 5.2). As the rectifier is not yet conducting in this case, the PT can be

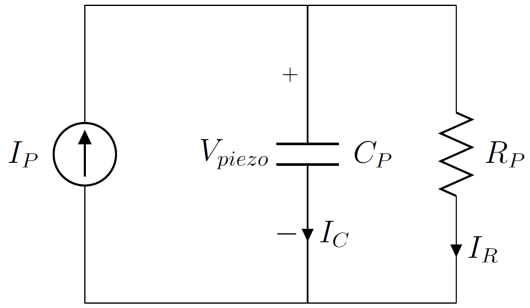


Fig. 5.2 Current flow in a piezoelectric generator.

regarded as operating in an open-circuit. Hence, the charge flowing into the capacitor C_P can be written as:

$$Q_C(j\omega) = Q_{total}\frac{I_C}{I_P}(j\omega) = \frac{2jI_0R_PC_P}{1+j\omega R_PC_P} \tag{5.2}$$

Besides the charge flowing into C_P to form the voltage V_{piezo}, the rest of the charge is dissipated by the resistor R_P. According to the formula $V = Q/C$, the open-circuit peak-to-peak voltage $V_{pp(open)}$ is expressed as:

$$\begin{aligned} V_{pp(open)} = |\frac{Q_C(j\omega)}{C_P}| &= |\frac{2jI_0R_P}{1+j\omega R_PC_P}| \\ &= \frac{2I_0R_P}{\sqrt{1+\omega^2R_P^2C_P^2}} \end{aligned} \tag{5.3}$$

In order to be able to charge the capacitor C_S, the voltage $V_{pp(open)}$ should be greater than the threshold $V_{TH} = 2(V_S + 2V_D)$. Hence, the condition for the rectifier to start transferring charge from the PT to C_S is:

$$\begin{aligned} V_{pp(open)} &> 2(V_S+2V_D) \\ \Rightarrow \frac{I_0R_P}{\sqrt{1+\omega^2R_P^2C_P^2}} &> V_S+2V_D \end{aligned} \tag{5.4}$$

Assuming $V_S = 2\,\mathrm{V}$ and $V_D = 0.3\,\mathrm{V}$, the condition for commencing transferring energy for the parallel model is $V_{pp(open)} > 2(V_S + 2V_D) = 5.2\,\mathrm{V}$. In order to compare the performance between parallel and series models, this condition is assumed to be always satisfied. The charge flowing into C_P is expressed in (5.2). After a part of charge is wasted for charging C_P, V_{piezo} equals to $V_S + 2V_D$ (or $-(V_S + 2V_D)$) and the rectifier starts conducting. The wasted

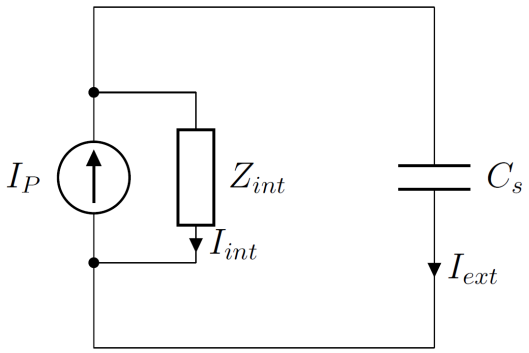


Fig. 5.3 Current flow while charging C_S - parallel model.

charge can be expressed as: $Q_{wasted} = 2C_P(V_S + 2V_D)$. Therefore, the charge going through the rectifier is the difference between Q_C and Q_{wasted}:

$$\begin{aligned} Q_{remain}(j\omega) &= Q_C(j\omega) - Q_{wasted} \\ &= 2C_P\left(\frac{jI_0R_P}{1+j\omega R_PC_P} - (V_S + 2V_D)\right) \end{aligned} \tag{5.5}$$

After the rectifier becomes conducting, the voltage V_{piezo} attains the threshold and the equivalent circuit transforms to a harvester in parallel with C_S as shown in Fig. 5.3. The internal impedance of the piezoelectric harvester is the value that C_P and R_P in parallel, expressed as $Z_{int}(j\omega) = \frac{1}{j\omega C_P} // R_P = \frac{R_P}{1+j\omega R_PC_P}$. Hence, the charge flowing into C_S can be written as:

$$\begin{aligned} Q_S(j\omega) &= Q_{remain}\frac{Z_{int}}{Z_{int} + \frac{1}{j\omega C_S}} \\ &= \frac{2j\omega R_PC_PC_S}{1+j\omega R_P(C_P+C_S)}\left(\frac{jI_0R_P}{1+j\omega R_PC_P} - (V_S + 2V_D)\right) \end{aligned} \tag{5.6}$$

The capacitor C_S at the output of the rectifier is usually chosen at a value much higher than the PT internal capacitor C_P ($C_S \gg C_P$), so that V_S can keep increasing steadily. In addition, as R_P is usually between hundreds of kΩ and several MΩ, hence $\omega R_PC_S \gg 1$. Therefore, (5.6) can be approximately written as:

$$\begin{aligned} Q_S &\approx 2C_P\left(\frac{I_0 R_P}{\sqrt{1+\omega^2 R_P^2 C_P^2}} - (V_S + 2V_D)\right) \\ &= 2C_P\left(\frac{V_{pp(open)}}{2} - (V_S + 2V_D)\right) \end{aligned} \tag{5.7}$$

So that the voltage increase in C_S for the parallel model in a half I_P cycle is expressed as (where the subscript "//" means "parallel"):

$$\Delta V_{S//} = \frac{Q_S}{C_S} = \frac{C_P}{C_S}(V_{pp(open)} - 2(V_S + 2V_D)) \tag{5.8}$$

5.2.2 Series model

For the two PTs connected in series, the calculation starts with considering a single harvester, for which the internal current flow is similar to that shown in figure 5.3 and V_{piezo1} is the voltage generated by one single source. As there are two PTs connected in series, the total voltage is $V_{piezo} = \sum_{i=1}^{2} V_{piezo_i} = 2V_{piezo1}$. As the condition to charge C_S is $V_{piezo} > 2(V_S + 2V_D)$, hence this condition for each individual source is $V_{piezo1} > V_S + 2V_D$. It can be seen that the threshold voltage is now lowered by two times compared to the parallel model so that harvester is more likely to start operating at lower excitation levels. Hence, the charge flowing into C_{P1} in a half cycle is:

$$Q_{\frac{T}{2}1}(j\omega) = \int_0^{\frac{T}{2}} I_{p1} \frac{R_{P1}}{R_{P1} + \frac{1}{j\omega C_{p1}}} = \frac{I_0 R_P C_P}{1 + j\omega R_P C_P} \tag{5.9}$$

The wasted charge for dis-charging and charging in one source in a half cycle is:

$$Q_{wasted1} = C_{p1}(V_S + 2V_D) = \frac{C_p}{2}(V_S + 2V_D) \tag{5.10}$$

Before the condition $V_{piezo1} > V_S + 2V_D$ is met, the harvester is disconnected from C_S (as the diodes in the rectifier are not conducting). Once the $V_{piezo1} > V_S + 2V_D$ is satisfied, all of the sources are connected together with C_S in series. At this time, C_S starts being charged and the remaining charge for each single source that can be used for charging is:

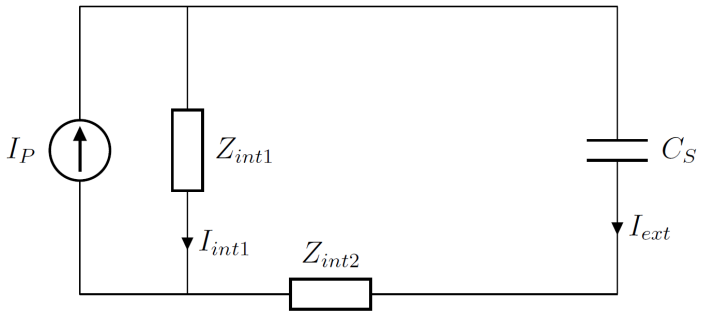


Fig. 5.4 Equivalent circuit for two PTs connected in series for charging C_S.

$$\begin{aligned} Q_{remain1}(j\omega) &= Q_{\frac{T}{2}1}(j\omega) - Q_{wasted1} \\ &= C_P\left(\frac{I_0 R_P}{1+j\omega R_P C_P} - \frac{V_S+2V_D}{2}\right) \end{aligned} \tag{5.11}$$

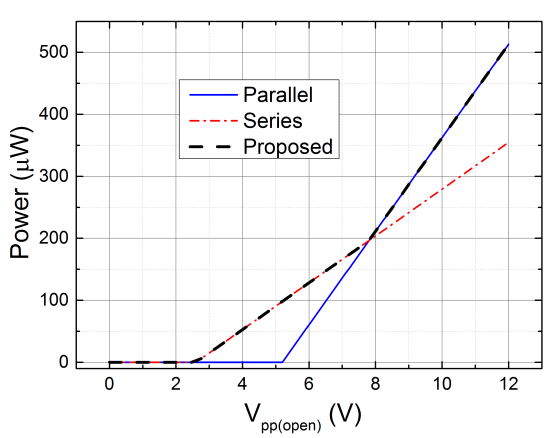
As only one harvester is considered, superposition theory can be used to turn off the current source of the other harvester. While the rectifier is conducting, the equivalent circuit for one single source is shown in figure 5.4. As the total internal capacitance and resistance for the parallel model are C_P and R_P, these values for one single PT becomes $C_P/2$ and $2R_P$. Hence, the internal impedance for one PT is $Z_{int1}(j\omega) = \frac{2}{j\omega C_P} // 2R_P = \frac{2R_P}{1+j\omega R_P C_P}$. Therefore, the ratio between the I_{ext} and I_{int} for each source being studied is:

$$\begin{aligned} &\frac{I_{ext}}{I_{int}} = \left|\frac{Z_{int1}}{Z_{int1}+Z_{int2}+\frac{1}{j\omega C_S}}\right| \approx \frac{1}{2} \\ &(\text{as } C_S \gg C_P \text{ and } Z_{int1} = Z_{int2}) \end{aligned} \tag{5.12}$$

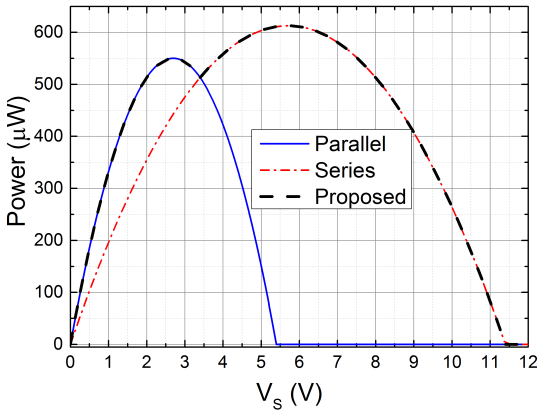
Therefore, the total charge that flows into C_S from one single source is:

$$Q_{S1} = \left|\frac{1}{2}Q_{left1}(j\omega)\right| = \frac{C_P}{2}\left(\frac{I_0 R_P}{\sqrt{1+\omega^2 R_P^2 C_P^2}} - \frac{V_S+2V_D}{2}\right) \tag{5.13}$$

With consideration of the other PT, the total charge that flows into C_S is (the subscript "+" in the expression represents series connection):



(a) Output power in function of excitation level with fixed $V_S = 2\,\mathrm{V}$.



(b) Output power in function of V_S with fixed excitation level of $V_{pp(open)} = 12\,\mathrm{V}$ (acceleration: 8.0 g).

Fig. 5.5 Theoretical output power for parallel model, series model and proposed model (diode voltage drop set as $V_D = 0.3\,\mathrm{V}$).

$$Q_{S+} = 2Q_{S1} = C_P\left(\frac{I_0 R_P}{\sqrt{1+\omega^2 R_P^2 C_P^2}} - \frac{V_S + 2V_D}{2}\right) \tag{5.14}$$

The voltage increase in C_S is:

$$\Delta V_{S+} = \frac{Q_{S+}}{C_S} = \frac{C_P}{C_S}\left(\frac{V_{pp(open)}}{2} - \frac{V_S + 2V_D}{2}\right) \tag{5.15}$$

5.2.3 Performance comparison and proposed scheme

The voltage increase values in V_S for both parallel and series models are expressed in (5.8) and (5.15). As these are the voltage variation in a half I_P period, the output power for both models can be calculated by dividing the increased energy stored in C_S by the half period:

$$P = \frac{\frac{1}{2}C_S\left((V_S + \Delta V_S)^2 - V_S^2\right)}{T/2} = f_P C_S\left((V_S + \Delta V_S)^2 - V_S^2\right) \tag{5.16}$$

where ΔV_S can be either $\Delta V_{S//}$ expressed in (5.8) for the parallel model or ΔV_{S+} expressed in (5.15) for the series model. With given diodes (fixed V_D), there are two variables in (5.16): $V_{pp(open)}$ and V_S. The performance of both models can be compared while fixing one of these variables and varying the other one. Fig. 5.5 shows the theoretical comparison of parallel and series models in function of excitation amplitude (Fig. 5.5a) and in function of V_S (Fig. 5.5b), where the diode voltage drop is set as $V_D = 0.3\,\mathrm{V}$. It can be seen that each model has an

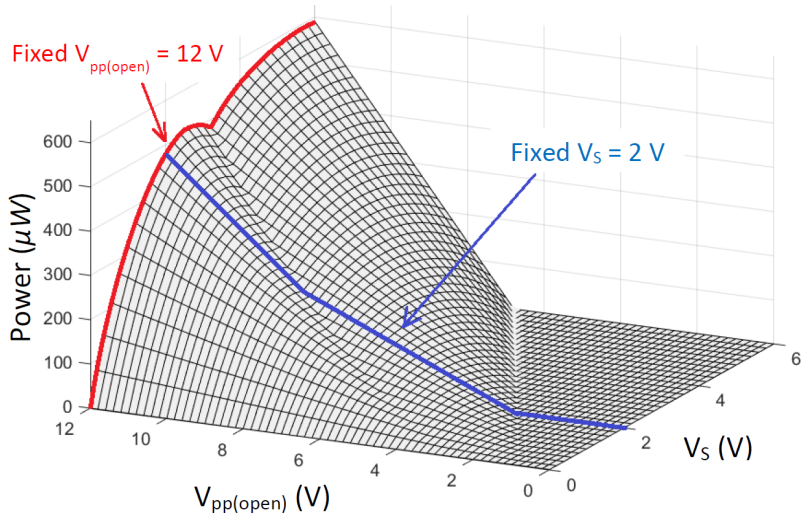


Fig. 5.6 3-D surface plot of theoretical output power in function of $V_{pp(open)}$ and V_S.

optimal operation range compared to the other model. Hence, it is useful to find the condition when the parallel model outputs higher power than the series model. This condition can be found by setting $\Delta V_{S//} > \Delta V_{S+}$:

$$\begin{aligned} \frac{C_P}{C_S}(V_{pp(open)} - 2(V_S + 2V_D)) &> \frac{C_P}{C_S}(\frac{V_{pp(open)}}{2} - \frac{V_S + 2V_D}{2}) \\ \Rightarrow V_{pp(open)} &> 3(V_S + 2V_D) \end{aligned} \tag{5.17}$$

It should be noticed that the value $V_{pp(open)}$ is the voltage while the two PTs are connected in parallel because this value doubles for the series model. The inequality in (5.17) shows the condition that the parallel model can generate more output power than the series model. This is key rule used in the proposed system to determine an appropriate connection configuration (parallel or series) under different excitation levels. Fig. 5.5 shows that the output power difference from the two models can be significant in some cases. Therefore, making a good choice between parallel and series connections in a specific condition can increase the output power and the operational excitation range. The proposed interface circuit in this chapter is able to check the condition in (5.17) periodically and connect the two PTs in parallel if the condition is satisfied; otherwise, in series. The expected output power of the proposed circuit is shown in dash curves.

According to (5.8), (5.15) and (5.16), the output power while using the proposed circuit can be expressed as:

$$P = f_P C_S((V_S + \Delta V_S)^2 - V_S^2) \quad \text{where}$$

$$\Delta V_S = \begin{cases} \frac{C_P}{C_S}(V_{pp(open)} - 2(V_S + 2V_D)) \\ \qquad \text{if } V_{pp(open)} \geq 3(V_S + 2V_D) \\ \\ \frac{C_P}{C_S}(\frac{V_{pp(open)}}{2} - \frac{V_S + 2V_D}{2}) \\ \qquad \text{if } (V_S + 2V_D) \leq V_{pp(open)} < 3(V_S + 2V_D) \\ \\ 0 \\ \qquad \text{if } V_{pp(open)} < (V_S + 2V_D) \end{cases} \tag{5.18}$$

If both the two variables $V_{pp(open)}$ and V_S are swept $0\,\text{V} \rightarrow 12\,\text{V}$ and $0\,\text{V} \rightarrow 6\,\text{V}$ respectively, a three dimensional surface plot of output power can be plotted, which is shown in Fig. 5.6. Planes of $V_S = 2\,\text{V}$ (corresponding to Fig. 5.5a) and $V_{pp(open)} = 12\,\text{V}$ (corresponding to Fig. 5.5b) are highlighted in this figure. It can be seen that higher V_S requires higher $V_{pp(open)}$ to start transferring energy to the storage capacitor. With a fixed V_S, the series model is able to output much higher power than the parallel model in low excitation levels. While $V_{pp(open)}$ goes higher, this difference becomes smaller but two peak power points allows a high output power in a wide range of V_S.

5.3 Proposed interface circuit

Fig. 5.7 shows the implementation of the proposed interface circuit between two PTs (a bimorph cantilever is used in this implementation) and a full-bridge rectifier. An off-chip voltage regulator is employed to provide a stable power supply $V_{DD} = 1.5\,\text{V}$ to power the interface circuit itself and any possible future load electronics. The two PTs are the two piezoelectric layers on a bimorph cantilever, so that they have the same frequencies, amplitudes and phases. The system architecture of the proposed circuit is also shown in the figure, which consists of a connection switching block, a power management block, a calibration block, an internal clock generator and switched-capacitor (SC) DC-DC converters. The connection switching block enables parallel or series configurations of the PTs according to the signal *PARA* (high for parallel and low for series). The power management block is a digital block that sets the system in the "sleep mode" for most of the time and in "calibration mode" to evaluate excitation amplitudes and re-connect the two PTs. The

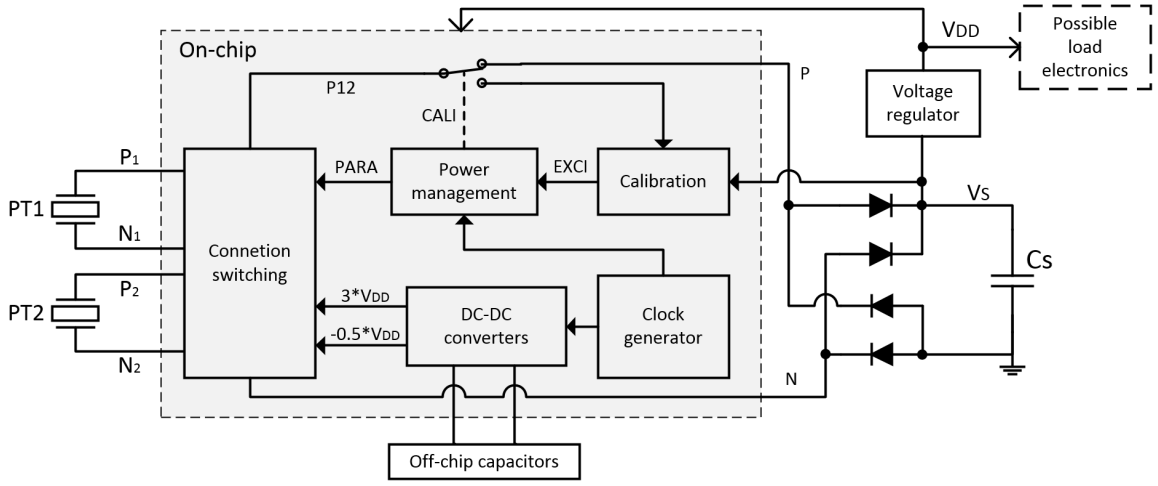


Fig. 5.7 Architecture of proposed interface circuit.

calibration block performs the algorithm to check the condition in (5.17) and generates *EXCI* pulses if the condition is satisfied. The signal *EXCI* (short for 'excitation') indicates that the environmental excitation is high enough to make the circuit choosing parallel connection. The DC-DC converters aim to generate a high voltage level and a negative voltage level to overdrive the gates of analog switches in the connection switching block.

While the system is in "sleep mode", the calibration block is powered OFF to minimize the overall power consumption. The duration of the "sleep mode" is controlled by a digital counter in the "power management block" driven by an internally generated clock signal. This counting time can be externally set. While the "sleep mode" ends, the system goes into "calibration mode". In this mode, the connection is forced to be parallel with a high *PARA* signal and the node P_{12} is disconnected from the node *P* by signal *CALI* (short for 'calibration'); because the value $V_{pp(open)}$ in (5.17) requires that the two PTs are connected in parallel and in an open-circuit (not connected to the diodes). In this mode, the voltage at node P_{12} and the voltage V_S are used for comparison in an algorithm corresponding to the condition in (5.17). If the excitation level is high to satisfy the condition, *EXCI* pulses will be generated to the power management block, which gives a final decision on the signal *PARA* and the "calibration mode" finishes.

5.4 Circuit implementations

This section describes the circuit implementations of the proposed connection auto-switching interface circuit as a CMOS circuit. Some key blocks shown in Fig. 5.7 are presented in this section with circuit diagrams and relevant calculations.

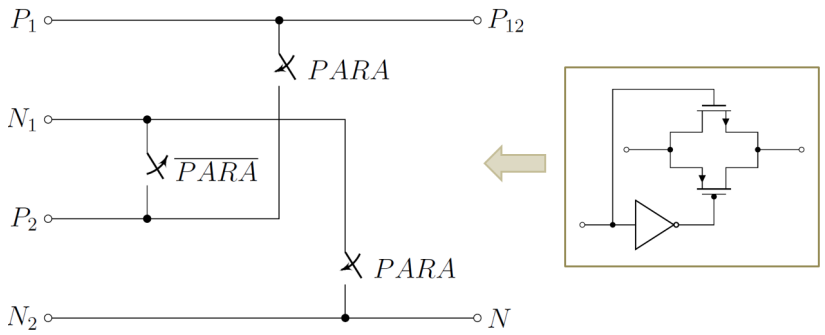


Fig. 5.8 Parallel-series connection switching circuitry with CMOS analogue switches.

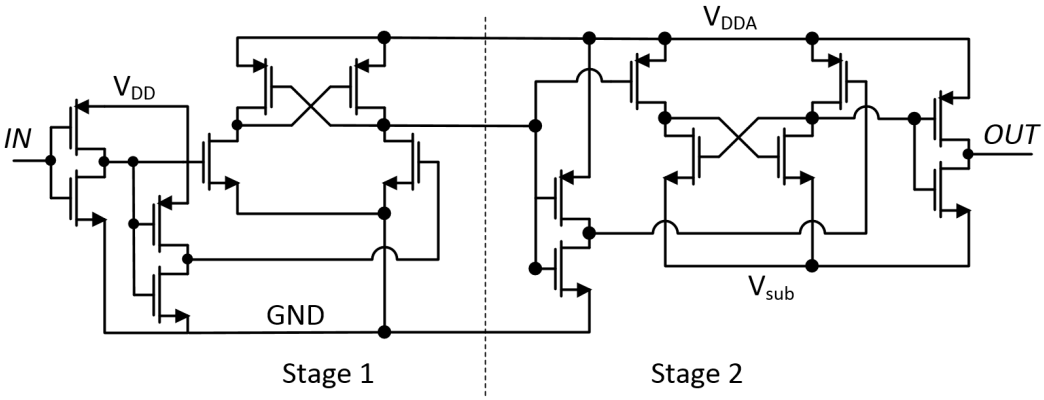


Fig. 5.9 Two-stage level-up shifter.

5.4.1 Parallel-series connection switching block

The parallel-series connection switching circuitry utilizes three CMOS switches, as shown in Fig. 5.8. The nodes P_1, N_1, P_2 and N_2 are the electrodes of the two PTs. The node N is one of the inputs of full-bridge rectifier. The node P_{12} is connected to the other input of the rectifier while the system is in "sleep mode" and to the calibration block in "calibration mode", as shown in Fig. 5.7. In order to make sure that the switches are fully switched ON and OFF for relevant *PARA* signals, the gate driving voltage of *PARA* should fully cover the voltage ranges of all the six nodes in the figure. According to the FBR diagram shown in Fig. 2.5, the voltages of V_P and V_N are between $-V_D$ and $V_S + V_D$. Hence, the low level of signal *PARA* should be lower than $-V_D$ and its high level should be higher than $V_S + V_D$. In this implementation, voltage levels of $V_{sub} = -0.75\,\mathrm{V}$ and $V_{DDA} = 4.5\,\mathrm{V}$ are chosen to drive the switches. The N-channel MOSFETs used in the switches are isolated high-voltage transistors with a negative bulk voltage V_{sub} and the bulk voltage of the P-channel MOSFETs is V_{DDA}.

As the signal *PARA* is generated from the power management block, which is a digital block, the voltage levels of *PARA* are *GND* and V_{DD}, where $V_{DD} = 1.5\,\mathrm{V}$ is used in this

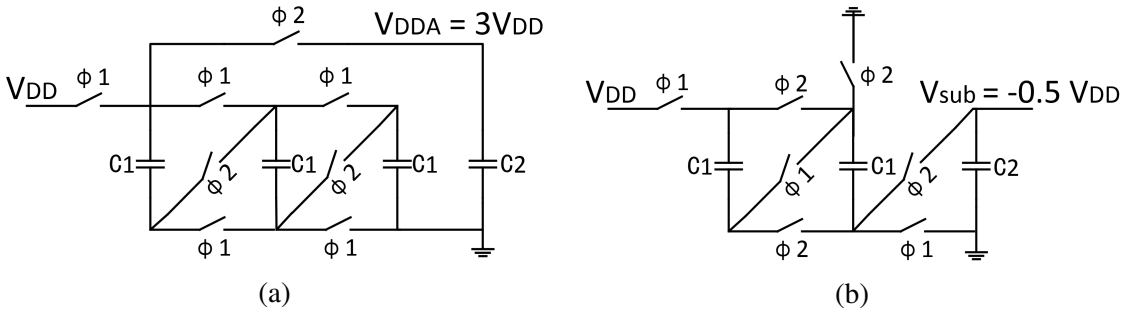


Fig. 5.10 Switched-capacitor (SC) converters used to generate gate overdriving voltage levels: (a) $V_{DD} \rightarrow 3V_{DD}$, (b) $V_{DD} \rightarrow -0.5V_{DD}$.

implementation. Hence, before the signal *PARA* from the power management block can be used to drive the switches, a level-up shifter is needed to shift the voltage level 0 V to -0.75 V and 1.5 V to 4.5 V. The reason for choosing -0.75 V and 4.5 V as the most negative and positive voltage levels in the circuit is due to the maximum allowed voltages for the selected transistors in the HV CMOS process used in this implementation. The absolute maximum allowed voltages V_{GS} and V_{DS} for these transistors are 5.5 V and the oxide breakdown voltage is 7 V. Hence, choosing -0.75 V and 4.5 V voltage levels makes a maximum 5.25 V voltage difference, which makes sure all the transistors operating safely. Fig. 5.9 shows a two-stage level-up shifter to shift the high level of the input signal to a higher voltage and the low level to a lower voltage. The different voltage levels shown in the figure are $GND = 0\,\text{V}$, $V_{DD} = 1.5\,\text{V}$, $V_{DDA} = 4.5\,\text{V}$ and $V_{sub} = -0.75\,\text{V}$. The first stage employs a cross-coupled PMOS load and it aims to shift logic voltage levels from [0 V, 1.5 V] to [0 V, 4.5 V]. The second stage employs a cross-coupled NMOS load to further shift logic levels from [0 V, 4.5 V] to [-0.75 V, 4.5 V]. The typical quiescent current at room temperature for supply V_{DDA} is around 80 pA and for supply V_{DD} is around 10 pA, so the typical total quiescent power consumption of this level-up shifter is around 0.5 nW. Considering the process and temperature variations by using Monte-Carlo simulations, the maximum quiescent power consumption can go up to 7.3 nW at 150 °C. However, this high temperature will unlikely happen in most implementations except for specific high-temperature purposes. Besides the static power loss, the total power consumption of a shifter should also include dynamic power loss, which depends on input signal frequency and gate capacitance of switches being driven. The total power consumed by all the level shifters employed in the system will be listed in a power consumption breakdown table in Section 5.5.

In order to provide gate overdriving voltages V_{DDA} and V_{sub}, switched capacitor (SC) DC-DC converters are employed. Fig. 5.10 shows the circuit diagrams of the two DC-DC converters. These two DC-DC converters perform voltage conversions with ratios $\frac{3}{1}$ and

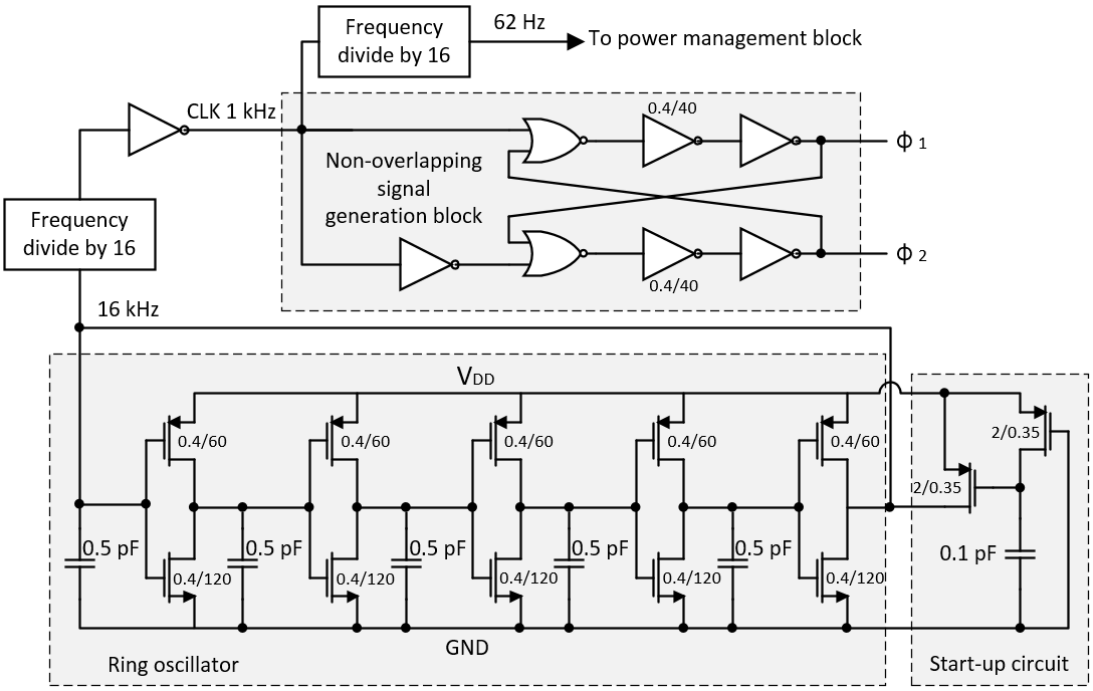


Fig. 5.11 Nano-watt power ring oscillator to provide digital clock for the SC converters and power management block, including the start-up circuitry and the non-overlapping signal generation block.

$-\frac{1}{2}$ respectively. Due to the limited chip design area reserved for this circuit, the capacitors used in the converters are off-chip SMD capacitors with $C_1 = C_2 = 1\,\text{nF}$. Hence, there are totally 7 off-chip 1 nF capacitors employed for the DC-DC converters in this implementation. However, simulations show that the total quiescent current flowing through V_{DDA} and V_{sub} for the whole circuit is 0.3 nA and the total average dynamic current is 2 nA, which make capacitors of $C_1 = C_2 = 50\,\text{pF}$ sufficient to provide the required driving ability. Capacitors with these values can be readily designed on-chip to make the proposed interface circuit fully integrated.

The voltage converters are driven by two non-overlapping complementary clock signals, ϕ_1 and ϕ_2, which are generated from a single clock signal by cross-coupling the clock and its inverted version with two NOR gates and two weak inverters. Before ϕ_1 and ϕ_2 can be used to drive the converters, their levels need to be shifted through level shifters. In this implementation, the clock signal is generated by an internal on-chip ring oscillator, as shown in Fig. 5.11. The ring oscillator generates a raw clock signal at around 16 kHz; this clock is then divided by 16 to drive the DC-DC converters and further divided by 16 (to 62 Hz) to drive the power management block. In order to supply the gate-overdriving voltage levels to make sure the parallel and series configurations are firmly held, the ring oscillator and

SC converters are kept powered ON. Simulations show that the ring oscillator consumes an average power of 260 nW and the voltage tripler and voltage half-inverter (in Fig. 5.10) consume 9 nW and 4 nW respectively with open outputs. Besides employing SC DC-DC converters, there are many other techniques to provide the switch gate-overdriving voltage levels, such as selecting the highest available voltage in the circuit nodes using a higher supply (HS) circuit for V_{DDA} and using a negative voltage converter (NVC) for V_{sub}, which are presented in [173]. As ring oscillators are normally power hungry and the low frequency ring oscillator employed in this chapter consumes 260 nW power (SC converters consumes 13 nW extra power), using HS and NVC circuits can decrease this power consumption to 96 nW (calculated according to [173]). However, the circuit in this chapter requires a clock signal to drive the power management block presented in section 5.4.3 in order to periodically put the system in sleep mode, and it cannot be guaranteed that the future load electronics can provide a such clock signal. As designing a ring oscillator is necessary in this implementation, SC DC-DC converters only consume 13 nW additional power while the HS and NVC circuits would consume more.

5.4.2 Calibration block

In the calibration state, the two harvesters are forced to be connected in parallel, so $P1$ and $P2$ are connected to $P12$; $N1$ and $N2$ are connected to N. For calibrating, $P12$ is disconnected form P, so the PTs are in an open-circuit. As $N1$ is still connected to N, the voltage at node $N1$ equals to $-V_D$ due to the diode voltage drop between the ground reference and node $N1$. Therefore, the peak-to-peak open-loop voltage between nodes $P12$ and N is now $V_{pp(open)} = 2(V_{P12} + V_D)$ (as $V_{pp(open)} = (V_{P12} - V_N)_{max} - (V_N - V_{P12})_{max} = 2(V_{P12} - V_N)_{max} = 2(V_{P12} + V_D)$). Replacing the term in (5.17), it becomes:

$$\begin{aligned} V_{pp(open)} &> 3(V_S + 2V_D) \\ 2(V_{P12} + V_D) &> 3(V_S + 2V_D) \\ 2V_{P12} &> 3V_S + 4V_D \\ 2(V_{P12} - 2V_D) &> 3V_S \\ \frac{1}{5}(V_{P12} - 2V_D) &> \frac{3}{10}V_S \end{aligned} \tag{5.19}$$

Fractions on both sides of the inequality are to make sure that the values on the two sides are in the operational range of the comparator. Fig. 5.12 shows the circuit diagram of calibration block to perform the comparison of (5.19). The two diodes used in the circuitry

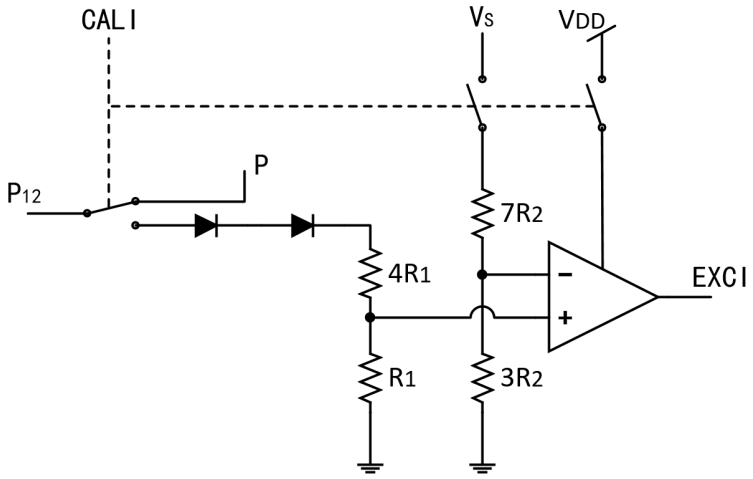


Fig. 5.12 Circuit diagram of the calibration block.

are the same as the ones used in the full-bridge rectifier in order to make sure they have same V_D. From this circuitry, the non-inverting input of the comparator is $\frac{1}{5}(V_{P1} - 2V_D)$ and the inverting input is $\frac{3}{10}V_S$. The unit resistances R_1 and R_2 in the circuit are set to 0.6 MΩ and 0.5 MΩ respectively, hence the total resistances for each of the two resistive paths are 3 MΩ and 5 MΩ. The resistors are on-chip implemented. The current on these two branches depends on the voltage at node P_{12} and the voltage V_S. During the calibration mode while P_{12} is disconnected from the full-bridge rectifier, the voltage on the R_1 branch approximately equals to the open-circuit voltage of the PT, which can have an amplitude varying from 0 V to 12 V. Choosing the middle value 6 V for estimation, the power loss due to this path is 3 µW (V_{P12} is a sine signal between 0 V and 6 V). In terms of the R_2 branch, the V_S usually varies from 2 V to 6 V; hence the average power loss due to this path is 3.2 µW (taking $V_S = 4$ V). As the two branches are cut from P_{12} and V_S in sleep mode, which takes a very majority of time, the total average power loss on these two branches equals 6.2 µW $\times\, d_{cali}$, where d_{cali} represents the duty ratio of the calibration mode. The base power loss 6.2 µW for these two resistive branches can be further reduced by increasing the resistances or using off-chip resistors to provide much higher resistances. Although larger value resistors are able to reduce the base power loss to less than 1 µW, they can take up additional area, either on the chip or on the test board with off-chip resistors. The resistance R_2 can be increased to a much higher value as the variation of V_S is slow. However, the value of R_1 should be below a reasonable limit because the frequency of V_{P12} signal can be quite high and the input transistors of the comparator have large sizes (500/0.5). Hence, high R_1 along with the large input capacitance of the comparator form a passive RC low-pass filter which filters out high frequency V_{P12} signal.

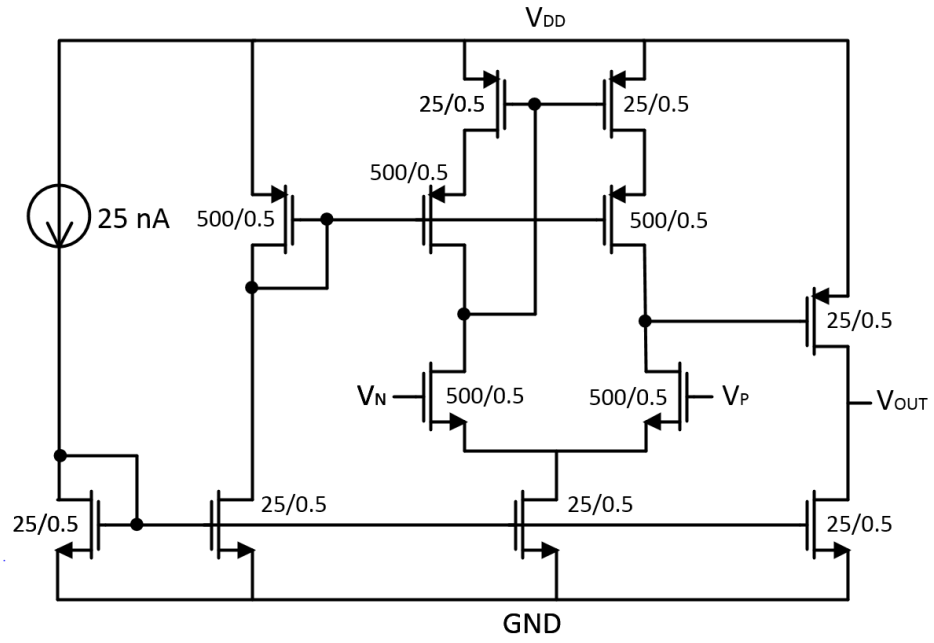


Fig. 5.13 Continuous time comparator to evaluate the input excitation level.

The output signal of this block, *EXCI*, indicates that the environmental excitation is high enough to satisfy the condition in (5.19). For generating the *EXCI* signal, a continuous-time comparator is employed [192], which is shown in figure 5.13. A trade-off between the power loss and the performance determines the biasing current. With a 25 nA biasing current, the settling time of the comparator is around 40 µs, which is acceptable for most of PTs as it is much shorter than the periods of PTs and the static power loss is decreased to 150 nW. In addition, the comparator is powered OFF in the sleep mode to further decrease power loss.

5.4.3 Power management block

Fig. 5.14 shows a power management circuitry employed to power OFF some parts of the system for a certain time while they are not in use and to generate digital control signals. As shown in the figure, the power management circuit utilizes a 10-bit digital counter for determining the duration of sleep mode. The clock signal of this 10-bit counter is of around 62 Hz. The 10-bit counting number D[9:0] of the counter is set externally and the system goes into "calibration mode" once it counts to the preset value D[9:0]. For instance, if D[9:0] = 255, the counter will be reset after 255 cycles of *CLK*, which is approximately 4 seconds. The maximum value can be set to 1023, or 16 seconds. Once the counter finishes counting, a pulse *DONE* is generated and the counter is synchronously reset to restart counting from 0. In order to make the power management block working as expected to let system go into

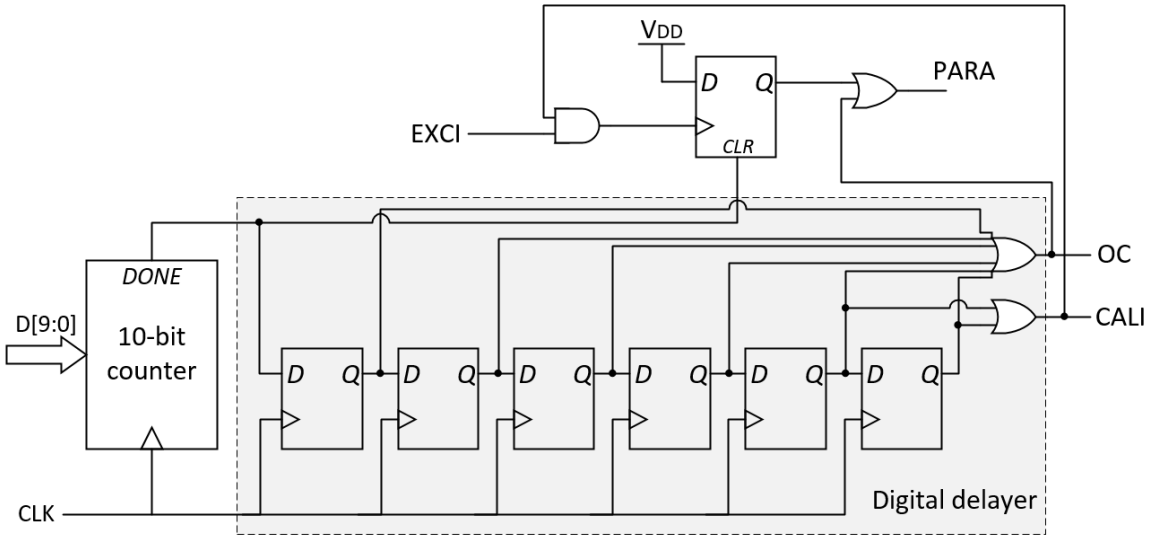


Fig. 5.14 Power management and parallel-series determining circuitry.

the two different modes alternatively for reasonable durations, the four LSBs D[3:0] are internally set to 4'b1111 and cannot be configured.

After the counter, a digital delayer using six simple D-flip-flops is employed. When the counter finishes counting, a pulse of *DONE* generates a pulse of *OC* (short for 'open-circuit') lasting for 6 clock periods and a pulse of *CALI* (short for 'calibration') lasting for 2 clock periods. If the input of the counter is set to the maximum value D[9:0] = 1023, the calibration mode only takes $6/1024 \approx 0.6\%$ of the total time, which means the average power consumption and current leakage associated to the calibration mode are largely reduced to 0.6%. The pulse *OC* is used to set the prerequisite conditions for performing the algorithm in the calibration block: forcing the two PTs to be connected in parallel and in an open-circuit. During the pulse of *OC*, the calibration block is powered ON but its output *EXCI* is disabled until the pulse *CALI* is present (the last two period of the pulse *OC*). Because suddenly putting the PTs in open-circuit from a closed circuit may cause issues on the reference voltage, which can make the voltage at the node P_{12} going to an unexpected voltage level and the voltage at node N does not equal to $-V_D$. This is because before an *OC* pulse, node P_{12} is connected to one electrode of the storage capacitor C_S through a diode and node N (the other electrode of PTs) is connected to the other electrode of C_S through a another diode (refer to Fig. 5.7). In this case, the two diodes connect P_{12}, N and C_S and form a closed loop. As there is current flowing in this loop when energy is transferred to C_S, N should be equal to $-V_D$ (assuming N is the lower potential node). Once P_{12} is disconnected from the diode connected to C_S, there is no closed loop between P_{12} and N nodes. Although N is connected to the ground through a diode, there is no current flowing through the diode to ensure that the

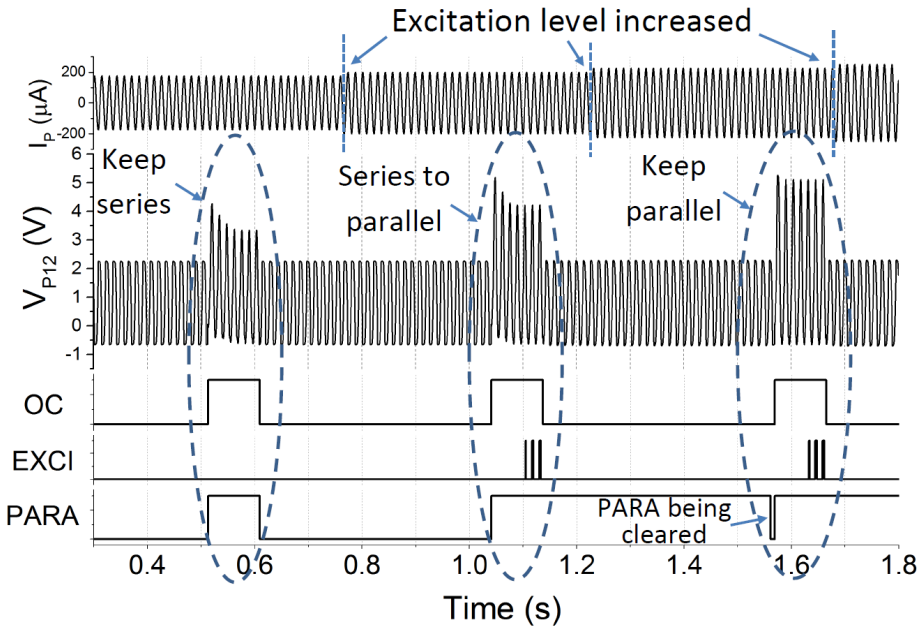


Fig. 5.15 Simulation results of the proposed interface circuit.

potential at N is $-V_D$. In this case, the voltage potential at N is not stable and it equals to the ground (0 V) at the instant of OC goes high. This introduces an V_D offset to the voltage at P_{12} because the inequality derived in (5.19) requires the voltage at N is $-V_D$. In order to make V_N be able to attain $-V_D$ while $V_{P(12)}$ goes high, some time is needed after OC goes high to let the diode between N and the ground "slowly" set $V_N = -V_D$. In this implementation, four periods of CLK is given. In the following two periods of CLK, $CALI$ pulse is generated which enables $EXCI$.

Fig. 5.15 shows the simulated waveforms of the proposed circuit. The signal I_P at the top represents the excitation amplitude, in unit of μA, which is increased gradually. The second signal V_{P12} is the voltage at the node $P12$ shown in Fig. 5.12. From the figure, the calibration mode is entered three times, where OC is high, in this simulation. When OC is high, the PTs are in open circuit and V_{P12} exceeds the limit $V_S + V_D$. It can be seen that V_{P12} needs a little time to stabilize before the signal $EXCI$ is enabled and can be generated at the end of the calibration state. During the first calibration mode, although the signal $PARA$ is forced to high to evaluate the excitation level, it goes low again after the calibration mode as the $EXCI$ pulse is not generated due to low excitation amplitude. After this calibration mode, I_P is increased. During the second calibration mode, it can be seen that three pulses of $EXCI$ is generated because the circuit chooses a parallel connection according to the excitation input. It is worth mentioning that the $EXCI$ pulses are generated according to the amplitude of V_{P12}, which has a frequency of 82 Hz. As mentioned before, the $EXCI$ signal is only enabled for

two *CLK* cycles and the frequency of *CLK* is 62 Hz. This explains why three *EXCI* pulses are generated in two *CLK* cycles. If the excitation frequency goes higher (or lower), there will be more (or less) *EXCI* pulses generated in two *CLK* cycles if the amplitude is high enough. If the excitation frequency is less than 31 Hz (half frequency of *CLK*) such that the period of the excitation is longer than two *CLK* cycles, an excitation peak cannot always be observed in the two *CLK* cycles. Hence, *EXCI* pulses cannot always be generated in this case. This may occasionally result in an unexpected series connection while the parallel connection is preferred under high excitation levels. Therefore, the proposed system requires the excitation frequency higher than 31 Hz to ensure correct connection switching. Before the third *OC* pulse, the excitation level is further increased and the PTs are expected to be connected in parallel. Right before the third *OC* pulse, *PARA* goes low for one clock cycle and it goes back to high level. This is because the top single D-flip-flop in Fig. 5.14 is reset first before each calibration mode, which allows *PARA* to be cleared to low level before it is forced to go high by the *OC* signal.

The single D-flip-flop in this block is used to provide a decision on the connection type based on the signal *EXCI*, which is generated in the calibration block in Fig. 5.12. While the counter finishes counting, the signal *DONE* resets the flip-flop to a low level regardless the previous connection type (parallel or series). The *CALI* pulse is used to enable the *EXCI* signal. If one or more *EXCI* pulses are present in the calibration mode during the pulse of *CALI*, the output of the flip-flop goes high and keeps the two PTs connected in parallel after the calibration state. If the excitation is too low to generate a pulse of *EXCI*, *PARA* signal will go back to low level after the calibration mode ends. An external one-time reset is performed on all of the flip-flops once the circuit is implemented and powered ON. During the simulation shown in Fig. 5.15, the input of the counter is set to D[9:0] = 32. This value is very small and is very impractical because the calibration mode takes a large percentage of the time (duty ratio is around $6/32 \approx 18.7\%$). During this mode, some extra energy is consumed and no energy can be transferred from the PT to the storage capacitor due to the open circuit of the PT. However, this small value chosen here is to clearly show the working principle of the proposed interface circuit and to decrease the simulation time due to the slow simulation speed. As discussed above, if the maximum value D[9:0] = 1023 is chosen for the counter, the duty ratio of the calibration mode is only 0.6%.

As discussed above, a smaller calibration duty ratio results in lower power consumption but the system also reacts slowly to variations in environmental excitation. Hence, there exists a trade-off between power consumption and circuit response time. The general principle is to keep the calibration duty ratio as small as possible while the circuit is able to react to the environmental excitation amplitude variation. As the four LSBs of the input signal D[3:0] for

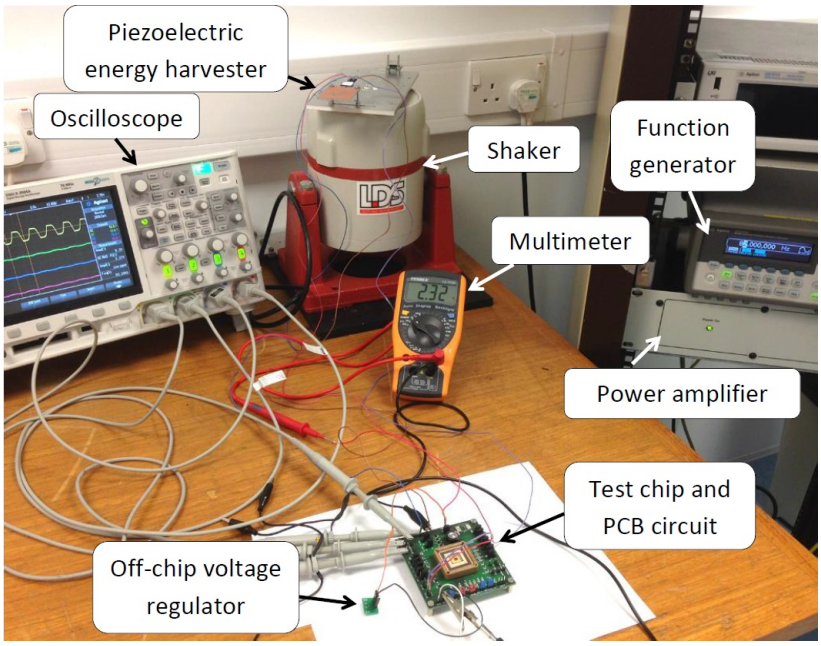


Fig. 5.16 Experimental setup.

the counter are internally set to 4'b1111, the shortest sleep time is around 0.25 s with a 37% calibration duty ratio. Hence, the proposed system cannot react to significant variation in excitation level faster than this value. However, the shortest sleep time preset by the circuit is impractical due to the large calibration duty ratio. Therefore, the proposed system is not suitable in environments with uncertain base vibration without target periods of time when the excitation level is high.

5.5 Measurement results and discussions

The proposed connection auto-switching interface circuit was experimentally evaluated (see Fig. 5.16) using a commercially available bimorph cantilevered piezoelectric harvester with dimension 47 mm $\times$ 36 mm (Mide Technology Corporation V20W). A shaker (LDS V406 M4-CE) was excited at the natural frequency of the cantilever at 82 Hz and driven by a sine wave from a function generator (Agilent Technologies 33250A 80 MHz waveform generator) amplified by a power amplifier (LDS PA100E Power Amplifier). The test chip was powered by an external power supply at 1.5 V (can go up to 1.8 V for higher V_S) and an off-chip voltage regulator (ON Semiconductor NCP4681DSQ15T1G) with ultra-low ground leakage current ($I_{GND} \approx 1.5\,\mu A$) is also available to allow for the system to be self-powered. The components on the PCB board include a storage super capacitor (AVX BestCap

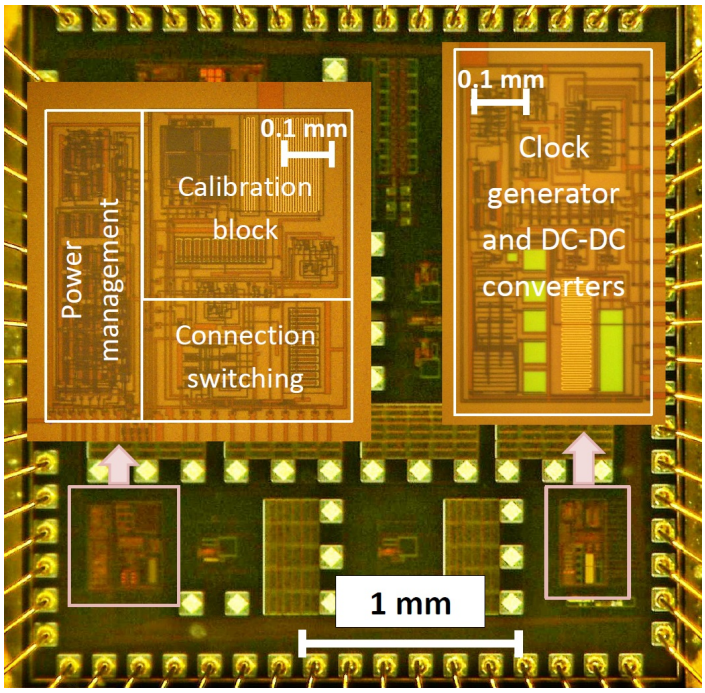


Fig. 5.17 Micrograph of the test chip fabricated in a 0.35 µm CMOS foundry process. The overall die size is 2.8 mm × 3.2 mm. The active area for the proposed circuit is around 0.5 mm^2 excluding the pads and the remaining die area is occupied by circuits of other projects.

BZ05CA103ZSB, measured capacitance $C_S \approx 5.2$ mF), a few 1 nF SMD capacitors for SC DC-DC converters, external digital inputs and pins for observing some key signals.

The proposed chip was implemented in a 0.35 µm CMOS process. Fig. 5.17 shows the die photo of the test chip. The active area of the proposed connection auto-switching circuit together with the DC-DC converters and the clock generator is around 0.5 mm^2. The micrograph of the chip identifies the area occupied by the clock generator, DC-DC converters, power management block, calibration block and connection switching block.

Table 5.1 lists the simulated power loss due to different parts of the energy harvesting system. The values for the individual circuit blocks are simulated results. In terms of the power loss due to the calibration block, the duty ratio of calibration mode during the measurement is chosen at 2.4%, corresponding to D[9:0] = 256 for the digital counter in the power management block. With a 62 Hz clock, the calibration mode is expected to be entered every 4 s and this can be observed from Fig. 5.18. Hence the effective power loss due to this block is 6.35 µW × 2.4% = 152.4 nW. The simulated total power consumption of the interface circuit with a 2.4% calibration mode duty ration is 452 nW, which is smaller than the measured value 500 nW. This is possibly due to the excitation level and the voltage

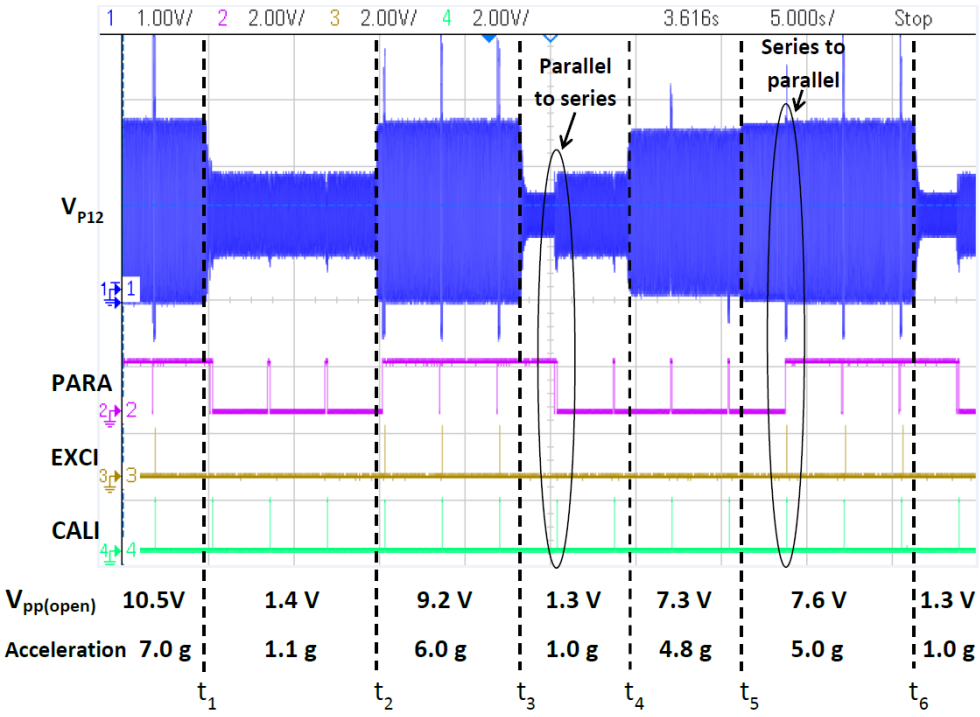


Fig. 5.18 Measured waveforms of signal V_{P12}, *PARA*, *EXCI* and *CALI* in a period of 50 s.

Table 5.1 Breakdown of the chip power loss and other power loss sources with simulated and measured results

Loss mechanism	Power loss	Percentage
Ring oscillator	260 nW	57.5%
DC converters	13 nW	2.9%
Level shifters	25.7 nW	5.7%
Power management	0.6 nW	0.1%
Switching block	0.3 nW	0.1%
Calibration block *	152.4 nW	33.7%
Total (circuit)	452 nW	100%
Measured circuit loss	$\sim 0.5\,\mu$W	
C_S leakage	$\sim 0.24\,\mu$W	

(* depends on the calibration duty ratio)

across the storage capacitor C_S during the measurements are relatively high, which increase the power loss due to the resistive branches in the calibration block as shown in Fig. 5.12. The storage capacitor C_S is an off-chip super capacitor of 5.2 mF and the power loss due to its internal leakage has been experimentally evaluated. The measurement was started by charging C_S to 4.21 V. After 1 day 19 hours and 7 minutes of leaving it disconnected from any electronic devices, the voltage decreased to 1.86 V and the power loss is calculated by dividing the energy loss in the capacitor over the time. As the leakage current of C_S depends on the voltage across it, the measured power loss [0.24 µW] should be regarded as an average value for V_S between 1.86 V and 4.21 V.

Fig. 5.18 shows measured waveforms from an oscilloscope of four signals: V_{P12}, *PARA*, *EXCI* and *CALI* (from top to bottom). The signals were measured in a period of 50 s by changing the input excitation amplitude. The signal V_{P12} is the voltage at the node P_{12}; the signal *PARA* indicates the connection type that is being used; the signal *EXCI* is the output signal from the calibration block indicating that the condition in (5.17) is satisfied and the signal *CALI* is the output signal from the power management block indicating that the system is in "calibration mode". From the *CALI* signal, it can be seen that the "calibration mode" was entered periodically for every 4 s (approximately). According to the section 5.4.3, the "calibration mode" starts when the digital counter finishes counting. The first cycle after the counting ends, a signal *DONE* is generated to reset a flip-flop to have a series connection (refer to Fig. 5.14). This explains why the signal *PARA* goes low for a very short time (actually for one clock cycle) when "calibration mode" starts with a high level *PARA*. After the *PARA* is reset to low level, the signal delayer in the power management block forces *PARA* to high level for a few cycles to evaluate the excitation. This forced high *PARA* pulses can also be seen from the Fig. 5.18 corresponding to pulses *CALI*. The signal *EXCI* indicates the result after evaluating the excitation amplitude according to the algorithm in (5.19). If a pulse of *EXCI* is present for a "calibration mode", the signal *PARA* keeps high after the mode ends; otherwise, *PARA* goes low because the excitation is too low to generated a *EXCI* pulse.

During the 50 s measurement, the excitation amplitude was changed 6 times, which are marked as t_1, t_2, t_3, t_4, t_5 and t_6 in the figure. The excitation amplitudes for all the time intervals are shown at the bottom of the figure as the peak-to-peak open-circuit voltage of the PT $V_{pp(open)}$ and the corresponding acceleration level in unit of the gravity. As t_1 and t_2 are slightly before calibration states start, the effect of different connection types on the signal V_{P12} is not observable. Hence, explanations on the figure will be based on the period after t_2. From the figure, several *CALI* pulses can be found between t_2 and t_3, where pulses of *EXCI* are generated. This means the excitation level is high to satisfy the condition in (5.19).

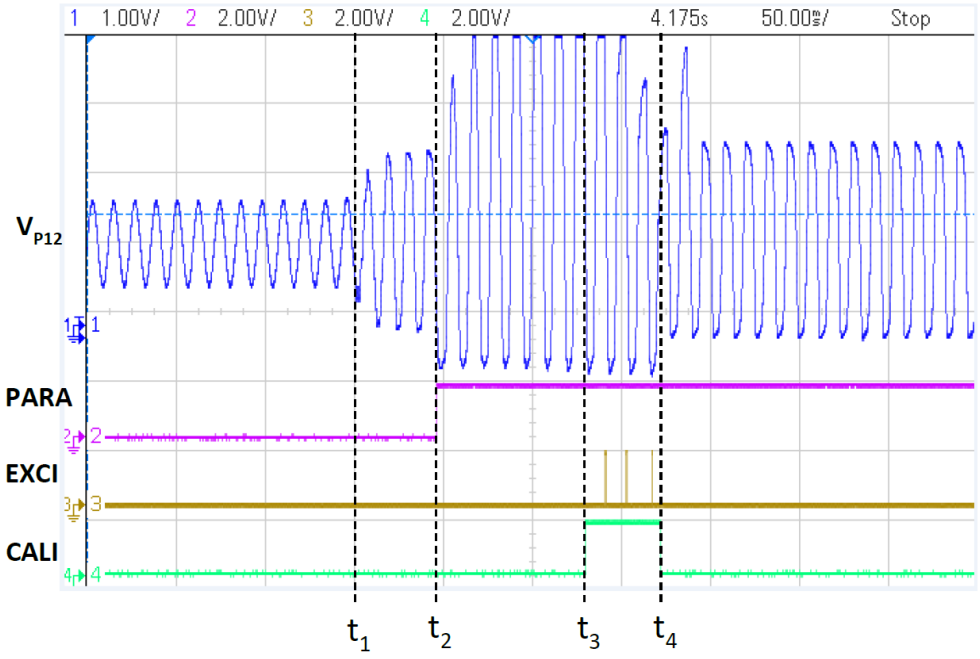


Fig. 5.19 Measured waveforms in 0.5 s while connection is being changed from series to parallel.

As a result, *PARA* keeps at high level after each calibration mode. During the calibration modes, it can be seen that spikes are present in the signal V_{P12}. This is because the PTs are disconnected from the full-bridge rectifier during the calibration mode (open-circuit), hence V_{P12} is not limited below $V_S + V_D$ and it can go higher. Similar spikes can also be observed for some of the other calibration states but spikes are not present for low excitations when V_{P12} cannot attain $V_S + V_D$. The excitation amplitude is then significantly decreased at time t_3 and a sudden drop in V_{P12} can be observed. During the calibration state after t_3 (marked in the left ellipse), no *EXCI* pulse is present, which results in a series connection. Once the PTs are connected in series, the amplitude of signal V_{P12} can be observed to be doubled because series connection doubles the voltage across the PTs.

The excitation is then increased at time t_4 where a sudden amplitude increase of V_{P12} can be observed. However, the *EXCI* signal still keeps low for the following two calibration states because the excitation level is not high enough. The excitation is further increased at t_5. The following calibration state confirms that the condition in (5.19) is satisfied and a pulse *EXCI* is generated. As a result, the *PARA* goes high (marked in the second ellipse).

Fig. 5.19 shows the waveforms of the four signals in a short period of time while the connection is being changed from series to parallel. At time t_1, the excitation is increased and the resulting V_{P12} can be observed from the figure. From time t_2 to t_4, the connection is forced to be parallel and *PARA* goes high. During this time, the PTs are in an open-circuit

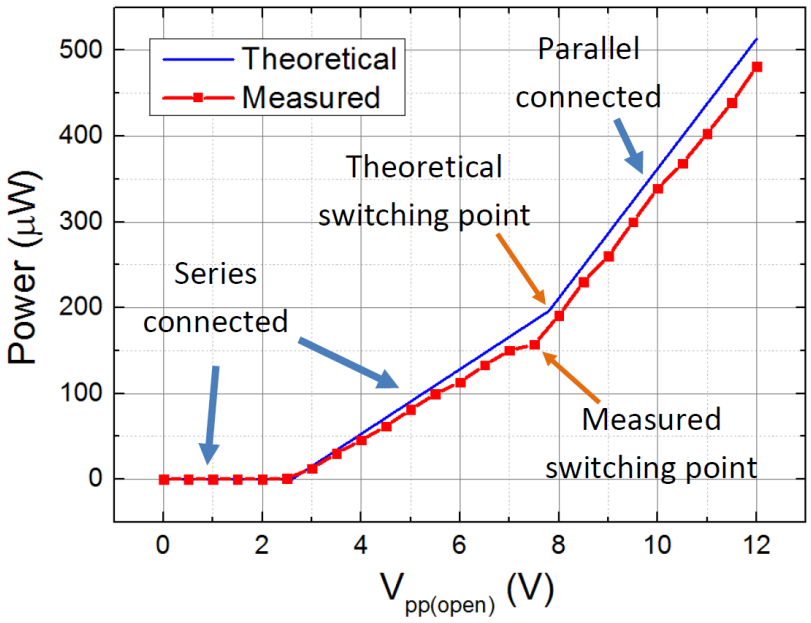
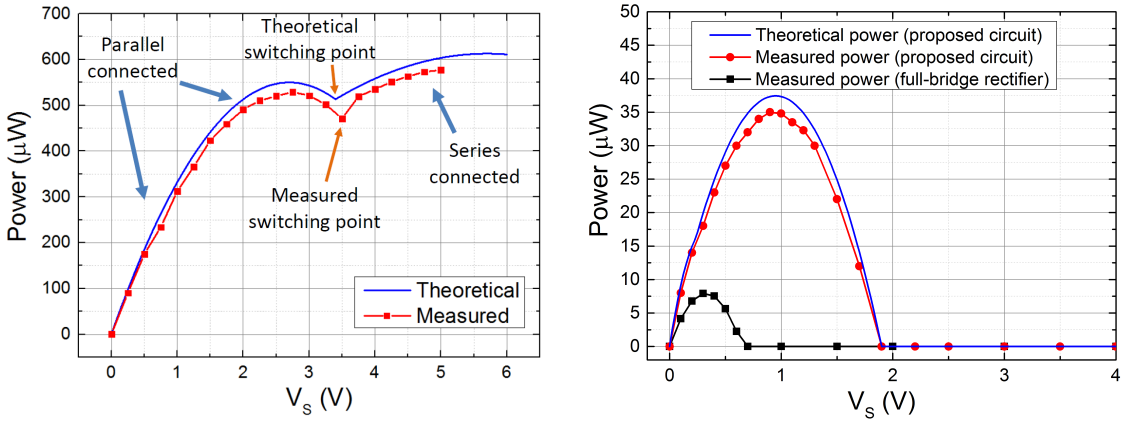


Fig. 5.20 Output power comparison between theoretical and measured results as a function of excitation level with fixed $V_S = 2\,\mathrm{V}$ (diode voltage drop $V_D = 0.3\,\mathrm{V}$).

hence V_{P12} can go very high. Between t_2 and t_3, the excitation evaluation is not enabled because a little time is needed to let V_{P12} become stable (detailed explanations are in section 5.4.3). Between t_3 and t_4, the signal *CALI* goes high to enable the *EXCI* signal; therefore, three *EXCI* pulses are generated due to satisfying the condition in (5.19). These pulses indicate that the connection will be parallel after the calibration state; hence, *PARA* keeps high after t_4.

In order to measure the output electrical power transferred to the storage capacitor C_S at a given $V_{pp(open)}$ and V_S, the voltage increase in C_S in a short period of time is measured to calculate the energy increase in this time. The formula of calculating the output power is: $P = C_S(V_{S(end)}^2 - V_{S(start)}^2)/2T$, where $V_{S(start)}$ is the starting voltage of V_S, $V_{S(end)}$ is the ending voltage of V_S and T is the time used to charge C_S from $V_{S(start)}$ to $V_{S(end)}$. As V_S is increasing during measurement and the output power should be obtained at some fixed V_S values, the $V_{S(start)}$ and $V_{S(end)}$ are chosen to be close to make the results accurate. While measuring the output power at $V_S = 2\,\mathrm{V}$, for instance, $V_{S(start)}$ and $V_{S(end)}$ are chosen at 1.9 V and 2.1 V with a fixed excitation level $V_{pp(open)}$. The time consumed to charge C_S from 1.9 V to 2.1 V is recorded by a stopwatch (of a smart phone) and the output power transferred to C_S can therefore be calculated.

Fig. 5.20 shows the measured output power compared to theoretical results with fixed $V_S = 2\,\mathrm{V}$ and changing excitation level, where the highest $V_{pp(open)}$ (12 V) corresponds to



(a) (b)

Fig. 5.21 Theoretical and measured output power in function V_S using proposed circuit and full-bridge rectifier under different excitation levels. (a) With a fixed excitation level of $V_{pp(open)} = 12\,\text{V}$ (equivalent to acceleration level of 8.0 g); (b) $V_{pp(open)} = 2.5\,\text{V}$ (equivalent to 1.8 g). Diode voltage drop $V_D = 0.3\,\text{V}$.

acceleration of 8.0 g. As $V_S = 2\,\text{V}$ and $V_D = 0.3\,\text{V}$ are used in experiments, the expected threshold voltage for pure parallel model is $2(V_S + 2V_D) = 5.2\,\text{V}$ and the expected switching point for parallel and series connection is $3(V_S + 2V_D) = 7.8\,\text{V}$. Compared to the pure parallel model, the proposed circuit can let the rectifier start extracting energy from the PTs at a lower threshold voltage 2.6 V. Compared to the pure series model, the circuit extracts more energy while excitation amplitudes are higher than the switching point such that $V_{pp(open)} > 7.8\,\text{V}$. The measured results show that the switching point is shifted to near 7.5 V and this is due to non-ideal diodes used in measurements. Non-ideal diodes allow forward leakage current flowing through while the forward voltage is lower than V_D; hence the effective V_D is lower than 0.3 V, which makes the switching point shifting leftwards on the graph.

Fig. 5.21 shows the measured results with the proposed circuit and a full-bridge rectifier at fixed excitation levels ($V_{pp(open)} = 12\,\text{V}$ in the left figure and $V_{pp(open)} = 2.5\,\text{V}$ in the right figure) with V_S varying from 0 V to 5 V. The results in Fig. 5.21a show that the switching point is measured at $V_S = 3.5\,\text{V}$, which is slightly higher than the theoretical value 3.3 V. This is also due to the non-ideal diodes used in measurements. The switching point is set as $V_{pp(open)} = 3(V_S + 2V_D)$. While non-ideal diodes have lower V_D values, V_S goes higher to keep a constant $V_{pp(open)}$. This explains the difference between theoretical and measured results. At a high excitation level ($V_{pp(open)} = 12\,\text{V}$) in Fig. 5.21a, there exists a maximum power point for each of the two connection types. With the proposed interface circuit, the energy harvesting system is able to attain both of the two peak power points at $V_S = 2.6\,\text{V}$ and $V_S = 5.5\,\text{V}$, which enable a wide range of V_S to obtain high output power. The same

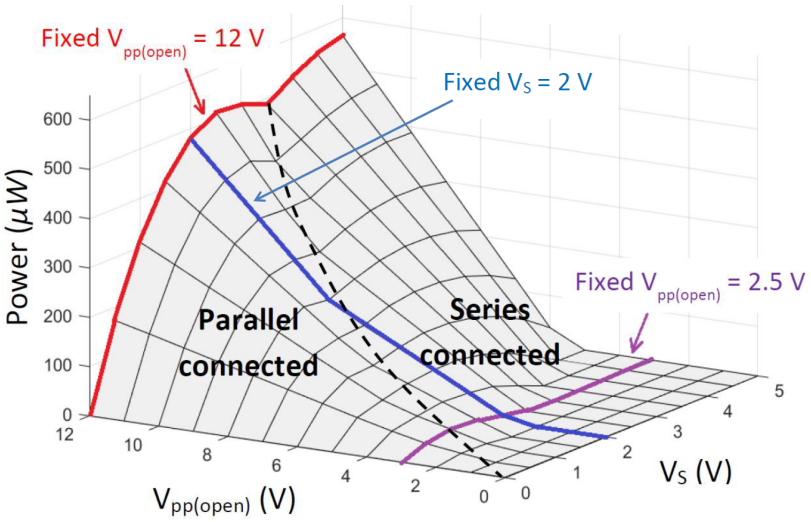


Fig. 5.22 3-D surface plot of measured output power in function of $V_{pp(open)}$ and V_S.

experiments were performed at a low excitation level ($V_{pp(open)} = 2.5\,\text{V}$) in Fig. 5.21b. The results show that the output electrical power using the proposed circuit can attain a peak power of 34.9 µW, which is 4.5× higher than the power obtained from a simple full-bridge rectifier, which is 7.8 µW. This is due to the series connection chosen by the circuit because the series model outputs much higher power than the parallel counterpart at low excitation levels. In addition, it can be seen that the extra power consumption introduced by the interface circuit 0.5 µW shown in Table 5.1 is far lower than the extra power extracted by this circuit compared to using a simple full-bridge rectifier.

Fig. 5.22 shows the measured electrical output power while $V_{pp(open)}$ is varied from 0 V to 12 V with steps of 1 V and V_S is varied from 0 V to 5 V with steps of 0.5 V. There are 13 $V_{pp(open)}$ values and 11 V_S values chosen, hence totally 143 output power values measured. This figure illustrates the performance of the circuit in the full ranges of excitation level and V_S. The results shown in Fig. 5.20 and Fig. 5.21 are highlighted in the $V_S = 2\,\text{V}$, $V_{pp(open)} = 12\,\text{V}$ and $V_{pp(open)} = 2.5\,\text{V}$ planes. The middle dashed curve separates the parallel and series configurations according to different values of $V_{pp(open)}$ and V_S.

Fig. 5.23 shows the measured power efficiency of the proposed interface circuit while an external power supply is used and it is self-powered with an off-chip voltage regulator. While the circuit is self-powered using an off-chip voltage regulator, the efficiency is reduced significantly. Although the leakage current of chosen voltage regulator is as low as 1.5 µA, the energy conversion efficiency is relatively low, which pulls down the overall efficiency. [193] presents an on-chip high-efficiency SC DC-DC converter with a nominal output voltage 1.5 V and efficiency up to 92%, which can be a very good substitute of the off-chip voltage

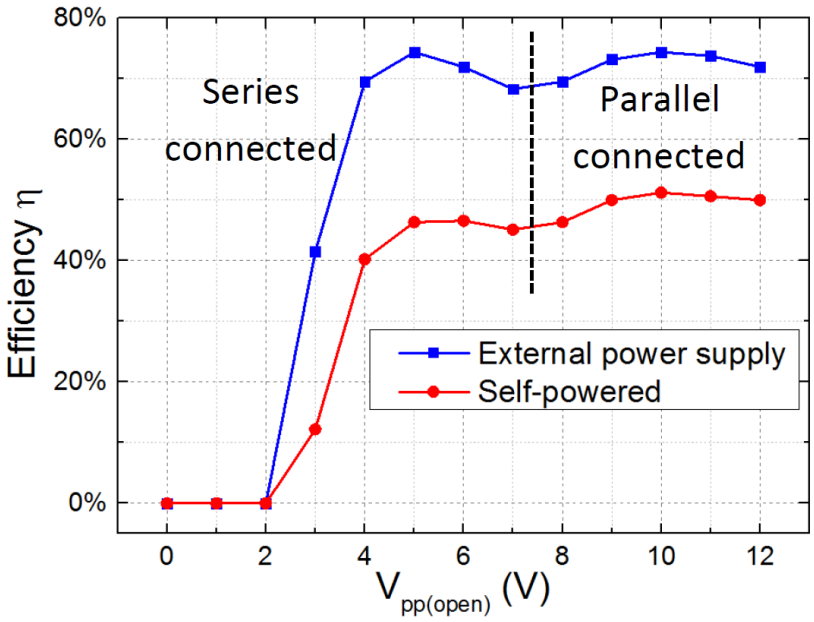


Fig. 5.23 Measured power efficiency of the proposed interface circuit while it is externally powered and self-powered ($V_S = 2\,\mathrm{V}$).

regulator to increase the overall efficiency. However, the voltage regulator employed here is just to allow for the possibility of the proposed circuit being self-powered for an energy autonomous module. The performance of the interface circuit itself should be the highlight of this chapter. From the figure, it can be clearly found that there are two peak efficiency points because the circuit is trying to configure the PTs in a better way to output higher power. While $V_{pp(open)}$ goes high from 0 V, the power efficiency goes higher and attains its first peak near $V_{pp(open)} = 5\,\mathrm{V}$. When the excitation level keeps being increased, the efficiency decreases. When $V_{pp(open)}$ goes higher than 7 V, the interface circuit configures the connection of the two PTs from series to parallel in order to keep the high power efficiency; therefore, the circuit is able to attain a second peak efficiency point. The dashed line in the figure shows the different connections the circuit chooses and it can be found that the first peak is due to series and the second peak is due to parallel connection. Compared to many other interface circuits, the proposed circuit enables a high power efficiency in a wide range of excitation levels.

Table 5.2 compares the performance of the proposed circuit against some reported interface circuits for piezoelectric vibration energy harvesters. Apart from the circuit presented in this chapter, all other circuits require inductors to improve performance and some may require inductors in the range of millihenries. A fully-integrated design in this chapter makes a significant contribution to reducing the overall volume of the system. Although the

Table 5.2 Performance comparison with reported interface circuits

Work	Technique	Power consumed	PT	$V_{pp(open)}$	C_P	f_P	Inductor	Power boost
JSSC2010 [167]	Bias-flip	2 µW	Mide V22B	2.4 V	18 nF	225 Hz	Yes	4×
TIE2012 [151]	SSHI	N.A.	T120-A4E Piezo	5.84 V	33 nF	30 Hz	Yes	2×
JSSC2012 [195]	PSCE	5.8 µW	Mide V22B	12.6 V	19 nF	174 Hz	Yes	1.23×
JSSC2014 [190]	MS-SECE	$\geq$ 1 µW	Murata	40 V	23 nF	100 Hz	Yes	N.A.
JSSC2014 [196]	Energy-investing	0.63 µW	Mide V22B	2.6 V	15 nF	143 Hz	Yes	3.6×
TPEL2015 [175]	SSHI	20 µW	Mide V22B	3.28 V	18 nF	225 Hz	Yes	4.5×
TPEL2016 [197]	SECE	0.43 µW	Q220-A4–303YB	2 V	52 nF	60 Hz	Yes	3×
This work	Connection switching	0.5 µW	Mide V22W	2.5 V	115 nF	82 Hz	No	4.5×

PT employed in this implementation is relatively big compared to a SMD inductor and an inductorless design does seem to reduce the overall system volume significantly; however, using an inductorless and fully-integrated interface circuit is a very practical consideration for volume-limited MEMS piezoelectric energy harvesters [194]. All the devices needed for the proposed power management circuit are a 2.8 mm $\times$ 3.2 mm chip (wire-bonder can be used instead of a chip carrier and socket), a 5.2 mF storage capacitor and a SC-70-5 case voltage regulator (in the case that the voltage regulator is not implemented on-chip); hence the volume is expected to be less then 0.5 cm^3.

As discussed in section 5.2.3 and experimentally verified in this section, the proposed scheme lowers the required excitation level by 50% and always chooses the connection type in order to output higher power. In real world implementations, the ambient vibration amplitude is likely to vary with time and the proposed circuit is able to detect the excitation level in order to achieve high power efficiency in a wide range of excitation amplitudes. Concerning the performance boost compared to a full-bridge rectifier, the voltage drop of diodes used in the listed publications (including this work) are different, making any fair comparison difficult to carry out. For example, the diodes used in [196] are with nearly zero

voltage drop. If [196] employs the same diodes as this chapter, the performance boost should have a higher value and may be even higher than the performance achieved by the circuit in this chapter. However, the highlight of the proposed interface circuit is not to achieved a highest possible output power; it aims to moderately increase the performance compared to a full-bridge rectifier while addressing the three drawbacks of SSHI and SECE circuits. A sub-micro watt inductorless fully-integrated interface circuit design allows for a significant decrease in the volume in compact system designs. In addition, the proposed circuit presents a different architecture and it dynamically configures the connection of two PTs to achieve higher power efficiency over a wide range of excitation amplitudes. Furthermore, as it does not generate synchronized current pulses in the piezoelectric materials, the proposed circuit is less subject to the SSD effect even for highly coupled PTs. Therefore, the mechanical vibration of the PTs will be less affected or damped, which extends the range over which the rectifier operates efficiently.

5.6 Conclusion

An adaptive sub-micro watt design for a piezoelectric energy harvesting interface circuit is proposed in this chapter. The proposed circuit can be used to automatically connect two piezoelectric transducers (with same frequencies, amplitudes and phases) in parallel or in series according to the environmental excitation level and the voltage across the storage capacitor. The theoretical output power of both parallel and series models are calculated and compared in order to find the condition to switch between the two connection types.

The proposed circuit facilitates transferring energy from the piezoelectric material to the storage capacitor at lower excitation amplitudes and it can maintain performance at high energy conversion efficiency over a wide range of excitation levels. This shows its strong suitability to real world vibration, where the excitation amplitude varies unpredictably. As opposed to other high-performance synchronized switch interface circuits, such as SSHI or SECE, the proposed circuit does not introduce current pulses to invert or extract charge from PTs. Hence, the performance is less affected from synchronized switch damping, especially when highly-coupled PTs are employed. Furthermore, the inductorless design enables a fully integrated CMOS implementation, which enables a reduction in overall system volume, especially for compact systems such as MEMS energy harvesters.

Chapter 6

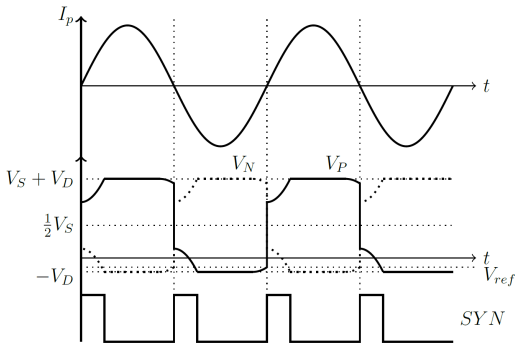
An Enhanced SSHI Interface Circuit with Auto-Startup Circuitry

6.1 Introduction

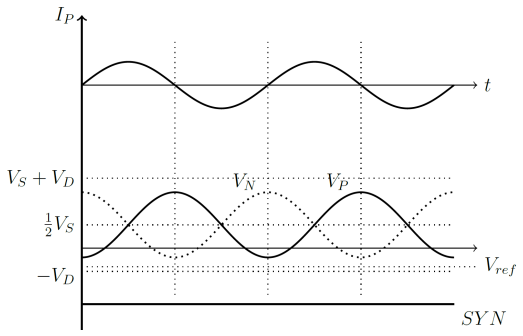
This section addresses a startup issue existing in conventional SSHI rectifiers and proposes a startup circuit which enables the system operating in an increased excitation range. Fig. 2.7 shows the SSHI interface circuit and its associated waveforms. At each zero-crossing point of I_P, the switches are synchronously closed for a short period of time to invert the charge on C_P from $-(V_S+2V_D)$ to $(V_S+2V_D)-V_F$, where V_F represents the energy loss due to the resistance of the RLC network and $V_{piezo}=V_P-V_N$ is the voltage across the PT. Despite the performance of the SSHI rectifier, a startup issue exists which may prevent the system from commencing operation and no energy can be extracted as a result. In Section 6.2, the conventional SSHI rectifier is modeled and the startup issue is addressed with theoretical calculations and simulations. Section 6.3 presents an overall view of the proposed SSHI rectifier. The detailed circuit implementations are presented in Section 6.4 and the simulation results in Section 6.5. Section 6.6 shows the measured results and a conclusion is given in the last section.

6.2 Modeling

In a conventional SSHI circuit, the switches controlling the inductor (see Fig. 2.7) are synchronously turned ON to invert the voltage on C_P while I_P crosses zero. When I_P is close to zero, the diodes of the full-bridge rectifier are just about to turn OFF. At this instant, one of V_P and V_N is close to $-V_D$ and the other one is close to V_S+V_D. One method to detect the



(a) Waveforms while SSHI is operating properly.



(b) Waveforms while SSHI is not operating.

Fig. 6.1 Associated waveforms of SSHI interface while the circuit is operating properly and not operating.

zero-crossing of I_P is to compare either V_P or V_N (depending on the sign of V_{piezo}) with a reference voltage V_{ref} using continuous-time comparators [164]. The reference voltage V_{ref} is set slightly higher than the negative value of the voltage drop of the diodes ($-V_D$). Fig. 6.1a shows the waveforms while the SSHI circuit is operating properly, where SYN is the synchronous signal used to generate the switching signal ϕ_{SSHI}. For each I_P zero-current point, a rising edge is generated in SYN. The condition for generating the rising edge is that either V_P or V_N should go below V_{ref} attaining $-V_D$. If the excitation input is too small to make V_P or V_N attain $-V_D$, SYN will stay high and no synchronous rising edge can be generated, as illustrated in Fig. 6.1b. In this case, the switches in the SSHI circuit are kept open and no energy can be extracted.

For no or very weak input excitation, both of V_P and V_N are equal to $\frac{1}{2}V_S$ or oscillate around this voltage. This is because the high and low limits of these two voltages are $V_S + V_D$ and $-V_D$. If the four diodes match with same voltage drop, the value of V_P and V_N will approximate the middle balance voltage $\frac{(V_S+V_D)+(-V_D)}{2} = \frac{1}{2}V_S$. If there is a mismatch for the diodes, this balance voltage may be shifted a bit but this effect can be partially absorbed by the mismatch of other diodes. As a result, some, or even most, of effect contributing to shift the balance voltage is canceled. In this implementation, the diodes are carefully selected and experimentally measured for minimal mismatch. Hence the balance voltage for V_P and V_N should be very close to $\frac{1}{2}V_S$. Noting $V_{pp(open)}$ is the peak-to-peak voltage of V_{piezo} ($V_{piezo} = V_P - V_N$) while the piezoelectric transducer (PT) is in open-circuit , so $V_{pp(open)}$ needs to be greater than $2(V_S + 2V_D)$ in order to make V_P (or V_N) attain $-V_D$ to trigger the comparators and to start generating the synchronous signal SYN. Therefore, the condition to start SSHI circuits is:

$$V_{pp(open)} > 2(V_S + 2V_D) \tag{6.1}$$

This is also the condition for a full-bridge rectifier to start transferring energy. While flipping the voltage V_{piezo} at each zero-crossing moment, there is an electrical damping in the RLC loop due to the resistance. Assuming the voltage V_{piezo} is flip from $V_S + 2V_D$ towards $-(V_S + 2V_D)$, the damped expression of V_{piezo} is: $V_{piezo} = (V_S + 2V_D)e^{\frac{t}{\tau}} \sin(2\pi f_0 t)$, where $\tau = 2L/R$ and $f_0 = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \frac{1}{\tau^2}}$. After a half pseudo-period where $t = \frac{1}{2f_0}$, the resulting V_{piezo} equals to $-(V_S + 2V_D)e^{-\frac{\pi}{\sqrt{\frac{4L}{R^2C}-1}}}$. Hence the voltage loss V_F due to flipping (illustrated in Fig. 2.7) can be expressed as:

$$V_F = (V_S + 2V_D)(1 - e^{-\frac{\pi}{\sqrt{\frac{4L}{R^2C}-1}}}) \tag{6.2}$$

Besides the electrical damping calculated above, synchronized current generated to flip V_{piezo} in the SSHI circuit produces an electrical actuation that opposes the vibration, which increases the effective damping of the mechanical system. This effect is known as Synchronized Switch Damping (SSD) [176, 177]. SSD can significantly affect the mechanical vibration for strongly-coupled piezoelectric transducers; however this effect is limited or negligible for weakly-coupled PTs. Hence, the SSD effect has not been considered here and is assumed to be negligible. According to the voltage loss in (6.2), in order to make V_P (or V_N) attain $-V_D$ to keep the SSHI circuit operating after the charge inversion, the open-circuit peak-to-peak voltage of V_{piezo} should be greater than V_F. Therefore, the condition to maintain operation is:

$$V_{pp(open)} > V_F \tag{6.3}$$

After comparing the two threshold voltages in (6.1) and (6.3), the condition for starting the SSHI circuit is usually much more difficult to be satisfied than the condition for keeping it working while it is already operating. In real-world implementations, the ambient vibration is unpredictable and periods corresponding to no input vibration (or very small vibrations that cannot satisfy the condition in (6.3)) are very likely to occur. Therefore, once an SSHI circuit stops operating, the minimal excitation requirement for the circuit to extract energy is increased from (6.3) to (6.1), which means the input excitation needs to overcome a much higher threshold to start the circuit.

Figure 6.2 shows the simulated waveforms to illustrate how the SSHI circuit fails to restart after a period of weak excitation. The signal I_P (top) represents the input excitation amplitude and it is expressed as $I_P = I_0 \sin \omega t$, where the I_0 values corresponding to different

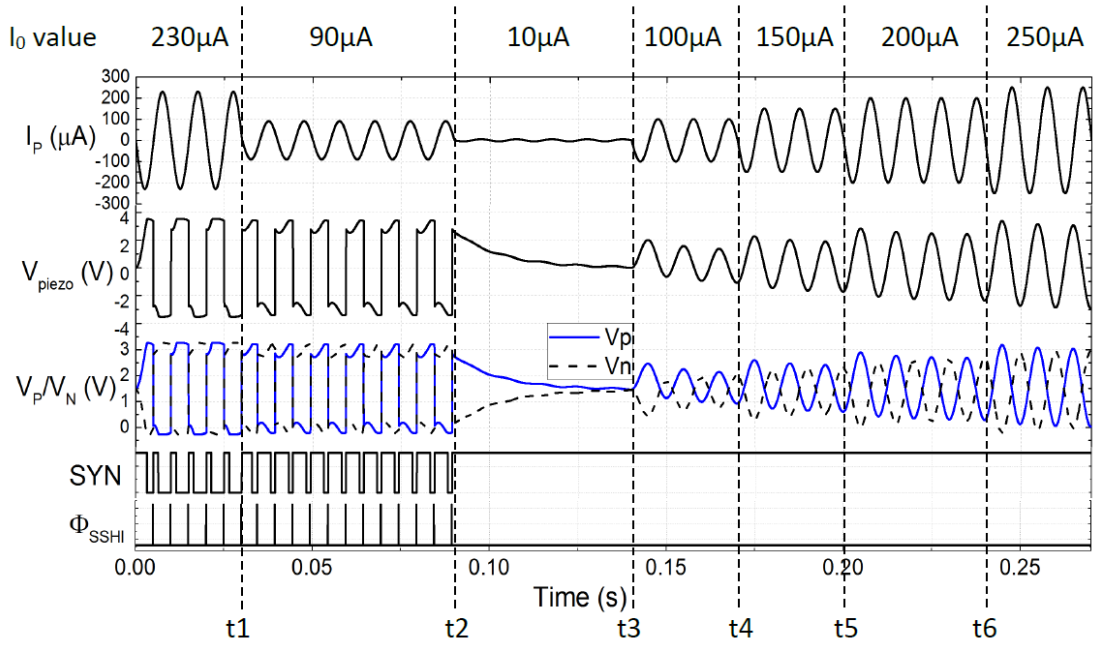


Fig. 6.2 Simulation waveforms showing the SSHI circuit fails to restart.

periods of time are shown above the signal. V_{piezo} ($V_{piezo} = V_P - V_N$) is the voltage across the PT and V_P and V_N are the voltage at the two electrodes of the PT. SYN is the synchronous signal to invert the voltage across the PT and ϕ_{SSHI} is the synchronous switch signal generated from SYN to flip V_{piezo}. Before time t_1 as shown in Fig. 6.2, an excitation level at $I_0 = 230\,\mu A$ makes the SSHI operate properly with the signal SYN generated correctly. Between t_1 and t_2, the excitation is decreased to a value such that the condition in (6.3) is marginally satisfied. During this time, SYN can still be generated and V_{piezo} can be properly inverted. After t_2, the excitation input is further decreased to a near-zero value to simulate the condition for very weak excitation, so that the SSHI circuit cannot maintain operation. In this case, the synchronous signal SYN maintains a high level. As the charge on the internal capacitor C_P of the PT cannot be inverted, the remaining charge on C_P diminishes due to the internal leakage. As a result, V_P and V_N tend towards $\frac{1}{2}V_S$ and V_{piezo} tend towards zero, where V_S is set to 3 V in the simulation. From t_3 the excitation input is gradually increased to $I_0 = 100\,\mu A$, $150\,\mu A$, $200\,\mu A$ and $250\,\mu A$. When the excitation is increased to a level much higher than $90\,\mu A$, the SSHI circuit cannot be restarted while both V_P and V_N are oscillating around $\frac{1}{2}V_S$ and they cannot attain $-V_D$. Although the excitation level of $I_0 = 90\,\mu A$ is sufficient to maintain the SSHI circuit (between t_1 and t_2), it cannot restart the SSHI, even at a higher value of $I_0 = 250\,\mu A$.

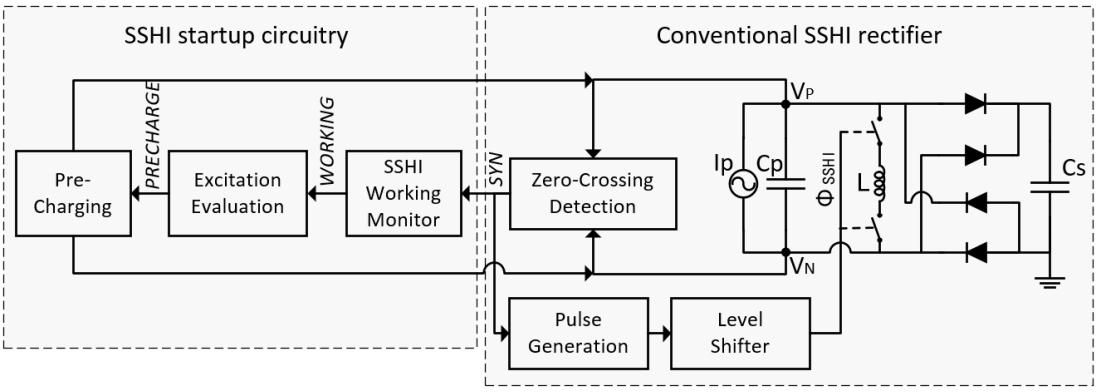


Fig. 6.3 System architecture of the proposed SSHI interface with self-startup circuitry.

The simulation results show that the operational range of this SSHI rectifier implementation is limited as it requires high input excitation to be restarted. In the following sections of this chapter, a new SSHI architecture is introduced, which is able restart the SSHI circuit when required to increase the effective operational range.

6.3 Proposed architecture

This section proposes an improved SSHI rectifier able to automatically restart the SSHI circuit while it is not working [198]. Fig. 6.3 shows the block architecture of the proposed system containing a conventional SSHI rectifier and an SSHI startup circuitry. The synchronous signal *SYN* is generated from the "zero-crossing detector" block while a zero-crossing moment of I_P is detected. This signal is used in the conventional SSHI rectifier to flip the voltage across the PT and it is also used by the "SSHI working monitor" block to monitor if the SSHI interface is operating correctly. Once the SSHI circuit stops generating the *SYN* signal, the signal *WORKING* goes low indicating that the SSHI is not operating now. A low *WORKING* signal turns ON the power supply for the following "Excitation evaluation" block. This block aims to evaluate the input excitation because restarting the SSHI circuit is only needed if the input excitation is stable (not an instant shock) and the amplitude is high (the condition $V_{pp(open)} > V_F$ is satisfied for the SSHI circuit being able to maintaining operating once started). If either of these two conditions are not met, the "excitation evaluation" block will not restart the SSHI circuit as it will stop working again after being restarted and the energy "invested" in restarting is wasted. If this block determines that the SSHI circuit can be restarted under the given excitation, a signal *PRECHARGE* will be generated to allow the "pre-charging" block to charge the PT to a voltage value sufficient to generate the *SYN* signal. Once *SYN* is generated, "SSHI working monitor" block reads this signal and send a high

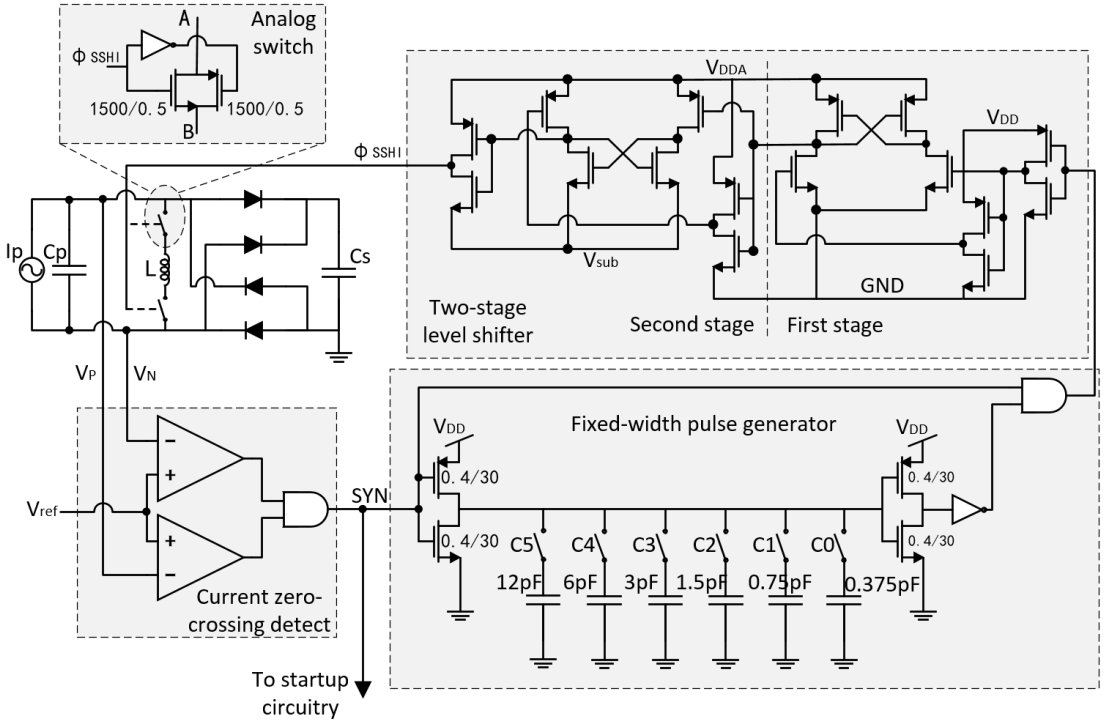


Fig. 6.4 Conventional SSHI rectifier.

WORKING signal to indicate that the SSHI circuitry is operating. Therefore, the following two blocks "excitation evaluation" and "pre-charging" are powered OFF to minimize power loss.

Using the proposed circuit, the threshold of starting an SSHI circuit is lowered from (6.1) to (6.3) and both thresholds depend on V_S. If the diodes are with zero voltage drop and V_S is high, say 4 V, the threshold for conventional SSHI circuits ($V_{pp(open)} > 8\,\mathrm{V}$) is relatively hard to attain for some PTs implemented in low excitation environments. If a load device is present and continuously consumes the energy in C_S, weak excitation prevents the system from harvesting any energy and V_S keeps decreasing. Assuming V_S is decreased to 0.5 V after a long period of time without any input excitation, the threshold in (6.1) is lowered to $2V_S = 1\,\mathrm{V}$ and a conventional SSHI circuit can be started from a much lower threshold $V_{pp(open)} > 1\,\mathrm{V}$ (a stable power supply generated from this low V_S with a boost converter is assumed to be available). While conventional SSHI circuits becomes easier to be started, the same principle also applies to the proposed SSHI rectifier with startup circuitry, where the threshold in (6.3) is also significantly decreased to $V_{pp(open)} > V_S(1 - e^{-\frac{\pi}{\sqrt{\frac{4L}{R^2C}-1}}})$, which can be around $0.2\,\mathrm{V} \sim 0.5\,\mathrm{V}$. Hence, the proposed circuit always shows an increased operational range for different V_S values although this improvement becomes less obvious for low V_S.

Besides providing a "kick" with the invested energy from the battery to start the SSHI circuit as proposed in this chapter, another method is also possible by using a different means to detect zero-crossing points and flipping V_{piezo} until it exceeds $V_S + 2V_D$. For this method, detecting if the SSHI circuit can extract any energy from the PT is also useful (equivalent to "working" and "non-working" phases in this chapter). This is because if the excitation is too small to meet the condition in (6.3), neither V_P nor V_N can attain $V_S + V_D$ or $-V_D$; hence repeatedly flipping V_{piezo} in this case will waste the energy used to drive the large W/L CMOS switches without any energy harvested. In order to distinguish these two phases, additional blocks need to be designed, which add extra power consumption and complexity, while the proposed SSHI startup circuit can just use the SYN signal to do the same job. Distinguishing between "working" and "non-working" phases can not only decrease the chip power consumption in this case, but it also provides an important signal for the load electronics, such as a wireless sensor node, to indicate if any energy is being harvested. Therefore, the load electronics can dynamically manage the power consumption in the case of very low environmental vibration or no vibration.

Fig. 6.3 presents a block level diagram to describe the working principle of the entire system and the detailed transistor-level circuits for different blocks will be presented in the next section.

6.4 Circuit implementation of the proposed SSHI circuit

This section describes the implementation of the self-startup SSHI rectifier as a CMOS circuit. As shown in the block diagram of Fig. 6.3, there are four main blocks in the proposed circuit: a conventional SSHI circuit, a working monitoring block, an excitation evaluation block and a pre-charging block. These blocks and the internal transistor-level circuit diagrams will be presented and explained in this section.

6.4.1 Conventional SSHI circuit

Fig. 6.4 shows the circuit diagram of the conventional SSHI rectifier. In order to find the current zero-crossing point of I_P, two continuous-time comparators are employed to compare V_P and V_N with a reference voltage V_{ref}, which is set slightly higher than $-V_D$. Details of this method to detect the zero-crossing point is explained in Section 6.2. As $V_{ref} < 0\,\mathrm{V}$, the negative power supply of the comparators is connected to a negative voltage level in order to keep V_{ref} in the operational range of the comparators. In this chapter, the comparators are powered with supplies of $-0.75\,\mathrm{V}$ and $1.5\,\mathrm{V}$. The signal SYN from the outputs of these two

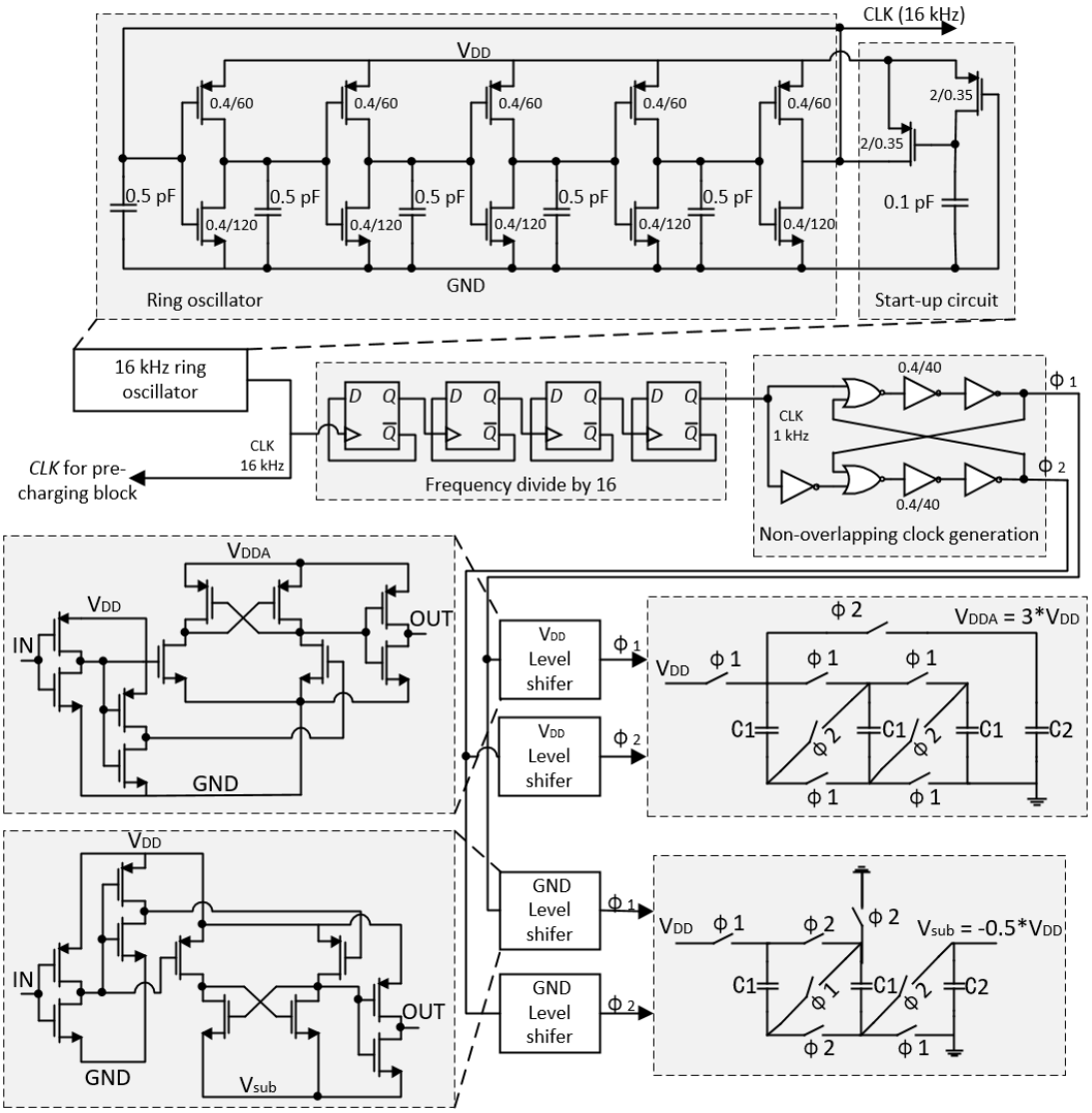


Fig. 6.5 Ring oscillator and DC-DC converters to generate gate over-driving voltage levels.

comparators is the synchronous clock signal having a rising edge at each I_P zero-crossing point. Each rising edge of SYN is used to generate a fixed-width pulse in the following delay block. The pulse width is adjusted to control the ON-time of the two switches of the inductor.

The fixed-width pulse generator aims to generate the fixed-width pulse signal from SYN. This pulse generator is a simple AND gate where the synchronous signal SYN is ANDed with the delayed and inverted version of SYN. The delay is performed using two weak inverters charging up capacitors, where the total capacitance is controlled by a 6-bit signal C[0:5]. The pulse width is adjustable over a wide range from 2 µs to 70 µs with resolution of 1.1 µs, which is able to accommodate large inductors up to 2 mH. The 6-bit delay control signal C[0:5] statically controls the width of the generated pulse equal to a half pseudo-period of the RLC oscillation system. In this implementation of the proposed SSHI rectifier, the 6-bit signal C[0:5] is set externally. For a given inductor (with inductance L) and a given PT (with internal capacitance C_P), the duration of putting the switches ON is fixed. Hence, before implementation, it is necessary to do a one-time calibration for the 6-bit signal C[0:5]. Although this static settling of flipping phase can be precisely tuned, possible unpredictable variation of the parameters of the PT due to fatigue (e.g. internal micro-cracks) during operation may change the internal capacitance C_P and make the static settling method invalid. Alternative auto-timing solutions presented in [25, 175] can be considered in future designs to dynamically settle the flipping phase.

The switch-controlling signal obtained from the delay block cannot be directly used for driving the two switches because different voltage levels are needed. The voltages of the two sides of the switches are V_P and V_N, which vary over a wide range between $-V_D$ and $V_S + V_D$; however, the voltage levels of the pulse signal obtained from the delay block are 0 V and 1.5 V (the V_{DD} used in this implementation is 1.5 V). In order to fully switch ON and OFF the two switches, the driving signal on the switches should have an ON voltage higher than $V_S + V_D$ and OFF voltage lower than $-V_D$. Assuming the voltage V_S does not go higher than 4 V and the energy stored on C_S will be transferred to a battery capacitor when V_S attains this threshold, so voltage levels of -0.75 V and 4.5 V are suitable to fully drive the switches. For this reason, a level-up shifter is needed to shift the voltage level 0 V to -0.75 V and 1.5 V to 4.5 V. A two-stage level-up shifter is shown in the figure, which is able to shift the high level of the input signal to a higher voltage and the low level to a lower voltage. The different voltage levels shown in the figure are $GND = 0\,\text{V}$, $V_{DD} = 1.5\,\text{V}$, $V_{DDA} = 4.5\,\text{V}$ and $V_{sub} = -0.75\,\text{V}$. The first stage employs a cross-coupled PMOS load aims to shift logic voltage levels from [0 V, 1.5 V] to [0 V, 4.5 V]. The second stage employs a cross-coupled NMOS load to further shift logic levels from [0 V, 4.5 V] to [-0.75 V, 4.5 V].

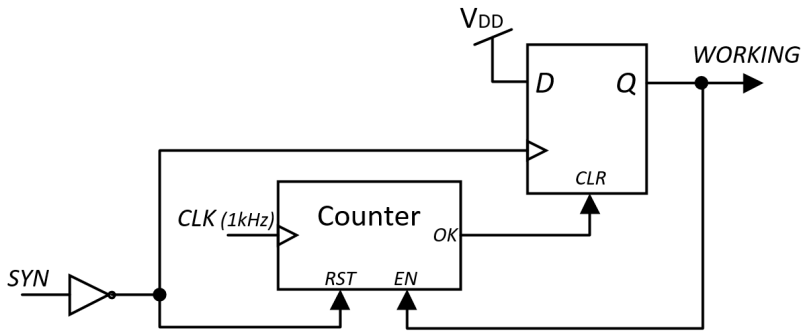


Fig. 6.6 Circuit diagram of SSHI working monitoring block.

In order to provide gate overdriving voltages V_{DDA} and V_{sub}, switched capacitor (SC) DC-DC converters are employed, which are driven by an internally generated clock signal. Fig. 6.5 shows the circuit diagrams to provide gate over-driving voltage levels and a clock signal for the other blocks. A 16 kHz clock is generated from a ring oscillator and its frequency is reduced to 1 kHz to drive the converters. The 1 kHz is then cross-coupled with its delayed inverted version with two NAND gates to generate two non-overlapping signals ϕ_1 and ϕ_2. These two clock signals are shifted with two different level shifters to drive the DC converters. Besides employing SC DC-DC converters, a higher supply (HS) circuit for V_{DDA} and a negative voltage converter (NVC) for V_{sub} are also good options as presented in [173]. As ring oscillators are normally power hungry and the one in this implementation consumes 260 nW power (other circuits in Fig. 6.5 consume additional 13 nW), using HS and NVC circuits can decrease the power consumption to 96 nW. However, the circuit in this work requires a clock signal to drive the counters in other blocks. Due to this reason, SC DC-DC converters only consumes 13 nW additional power while the HS and NVC circuits would consume more.

6.4.2 SSHI working monitoring block

In order to monitor the conventional SSHI circuit, the synchronous signal *SYN* is used in the "SSHI working monitoring" block, which is shown in Fig. 6.6. This block employs a 8-bit digital counter (two MSBs can be set externally and other bits are connected to V_{DD}) driven by an internally generated 1 kHz clock signal. The counting-down time of the counter is set several times longer than the longest period of the current source I_P. For this implementation, the PT has a natural frequency of 82 Hz, hence the count is set to 128, which is approximately 10 times of the period of the PT. The counter can be reset by a low *SYN*, which represents one of the voltages V_P and V_N attains $-V_D$. Hence, while the SSHI circuit is working and the signal *SYN* is generated correctly, the counter can be reset at each zero-crossing point

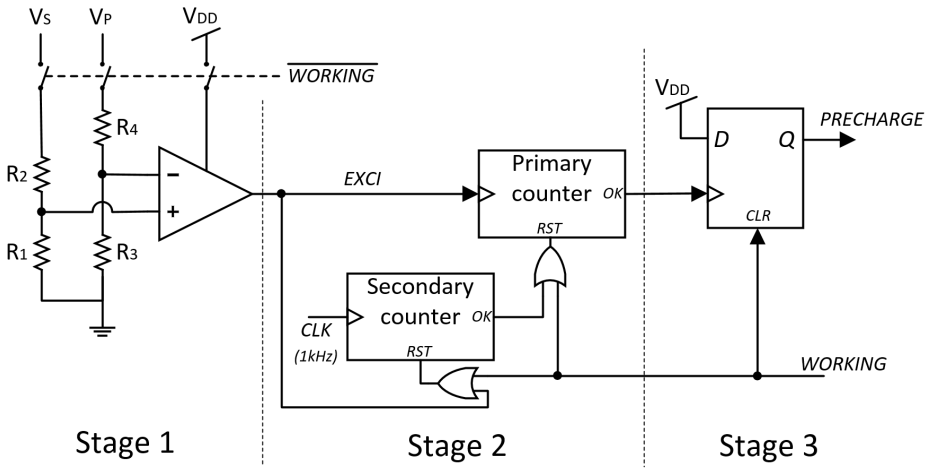


Fig. 6.7 Circuit diagram of excitation evaluation block.

of I_P. While the SSHI circuit stops working, the signal SYN will keep at high level. As a result, the counter cannot be reset until it finishes counting and sends a reset signal to the D-flip-flop so that the signal $WORKING$ goes to low level indicating that the SSHI circuit is not working. While the SSHI is not working, the $\overline{WORKING}$ also disables and resets the counter to initialize it for the next time when the SSHI restarts operation. During the non-working state, once the signal SYN can be generated correctly, the output of the D-flip-flop takes the value of the input V_{DD} so that $WORKING$ goes to high level. Based on the signal $WORKING$, the following blocks can be cut off from power while the SSHI is working.

6.4.3 Excitation evaluation block

When the signal $WORKING$ is low, the system goes to "non-working" state and it tries to restart the SSHI circuit; however, the system needs first to evaluate whether the startup is rewarding. If the excitation is just a weak impulse (producing a weak vibration attenuating to zero) or it is stable (not an impulse) but not high enough to maintain the operation of the SSHI circuit, restarting is not rewarding because the circuit will stop operating shortly after it is restarted and the invested energy is completely wasted. It should be mentioned that if the excitation levels in these two cases satisfy $V_{pp(open)} > 2(V_S + 2V_D)$, the SSHI startup circuitry will not be used and the SSHI circuit will be automatically started. Hence, for restarting the circuit in low excitation levels, an "excitation evaluation" block is necessary to provide the decision as to whether to restart the SSHI circuit. There are two things that the "excitation evaluation" block needs to evaluate before making a decision: the excitation amplitude and its duration. Fig. 6.7 shows the circuit diagram of this block which consists of three stages.

Stage 1 aims to evaluate the excitation amplitude, stage 2 aims to evaluate the duration of the excitation satisfying the previous stage and stage 3 provides the signal to the next block to restart the SSHI circuit.

In stage 1, the excitation amplitude is evaluated by comparing a fraction of V_S with a fraction of V_P. The rule of evaluating the excitation amplitude is that the SSHI circuit can at least maintain operation and generation of the *SYN* signal once it is restarted. (6.3) gives the condition for maintaining the SSHI in operational mode. Hence, the peak-to-peak voltage of $V_P - V_N$ (or V_{piezo}) should be greater than V_F. If only V_P is monitored instead of considering $(V_P - V_N)$, this condition is equivalent to that the zero-to-peak amplitude of V_P should be greater than $\frac{1}{4}V_F$.

While the SSHI circuit is not working, both V_P and V_N are around a balance voltage $\frac{1}{2}V_S$. So a comparison can be performed between voltages V_P and $(\frac{1}{2}V_S - \frac{1}{4}V_F)$. If V_P goes lower than $(\frac{1}{2}V_S - \frac{1}{4}V_F)$, it means the excitation amplitude is high enough to satisfy the condition in (6.3) to maintain the SSHI circuit in the "working" state. From the expression of V_F in (6.2), the condition above can be written as:

$$V_P < \frac{1}{2}V_S - \frac{1}{4}V_F \Rightarrow V_P < \frac{1}{2}V_S - \frac{V_S + 2V_D}{4}(1 - e^{-\frac{\pi}{\sqrt{\frac{4L}{R^2C} - 1}}}) \tag{6.4}$$

In this implementation, off-chip diodes are used in the rectifier because the CMOS process accessed for this implementation does not support Schottky diodes. The forward voltage drop V_D of the diodes is measured at around 0.2 V. Assuming $V_S \gg 2V_D$, the inductor is $L = 1\,\text{mH}$, the internal capacitance of the PT is $C_P = 115\,\text{nF}$ and the total ON resistance of the two switches is $R = 20\,\Omega$, so $\frac{4L}{R^2C} \gg 1$. Hence, (6.4) can be approximately written as:

$$V_P < \frac{1}{2}V_S - \frac{V_S}{4}(1 - e^{-\frac{\pi R}{2}\sqrt{\frac{C}{L}}}) \Rightarrow V_P < \frac{1}{4}V_S(1 + e^{-\frac{\pi R}{2}\sqrt{\frac{C}{L}}}) \tag{6.5}$$

With the L, R and C chosen above, $e^{-\frac{\pi R}{2}\sqrt{\frac{C}{L}}} \approx 0.72$. Hence (6.5) can be expressed as $V_P < \frac{1.72}{4}V_S$. Considering the shift of the balance voltage $\frac{1}{2}V_S$ due to diode mismatch and the fabrication tolerances of the CMOS process, a suitable condition is chosen as $\frac{1}{2}V_P < \frac{3}{16}V_S$, where the fractions on the both sides are to make sure the voltages in the operational range of the comparator. Hence the resistance ratios in Fig. 6.7 are: $\frac{R_2}{R_1} = \frac{13}{3}$ and $R_3 = R_4$. In this implementation, the resistors are chosen as $R_1 = 60\,\text{M}\Omega$, $R_2 = 260\,\text{M}\Omega$, $R_3 = R_4 = 50\,\text{M}\Omega$ and these resistors are implemented off-chip. While the SSHI circuit is operating and the *WORKING* signal is high, the two resistive branches and power supply of the comparator are cut off to decrease unnecessary power loss, which totally consume around 151 nW static

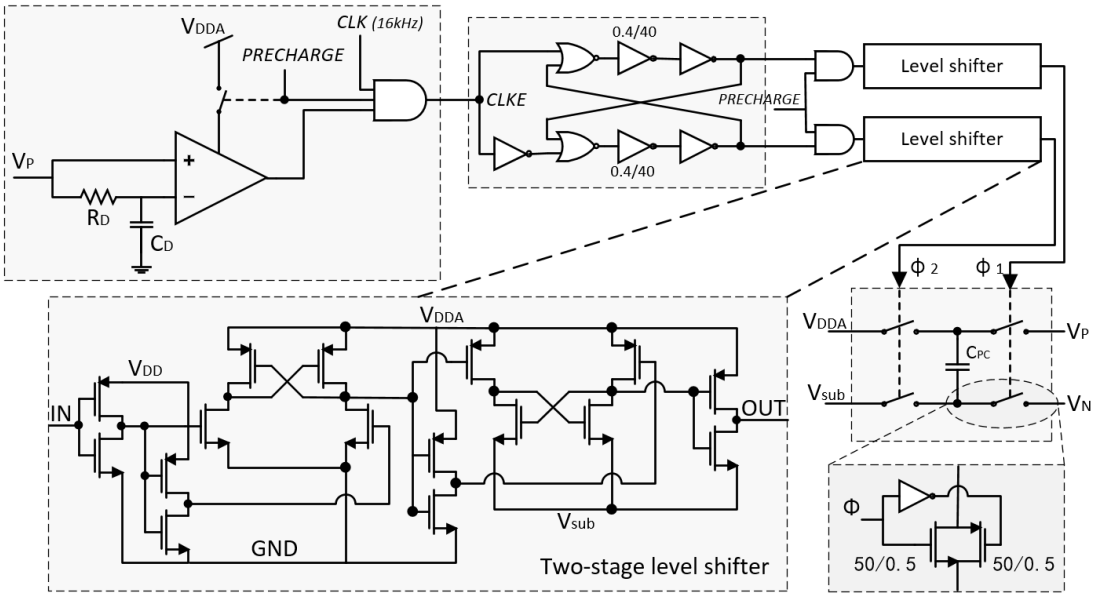


Fig. 6.8 Circuit diagram of the pre-charging block with on-chip $R_D = 7.5\,\mathrm{M\Omega}$ and $C_D = 30\,\mathrm{pF}$.

power. Once the condition $\frac{1}{2}V_P < \frac{3}{16}V_S$ is met, *EXCI* goes high, which means the excitation amplitude is high enough.

The stage 2 of this “excitation evaluation" block aims to filter any vibration impulses by employing two digital counters. The primary (10-bit) counter takes *EXCI* as the clock signal and counts the number of pulses in *EXCI* in order to determine if the excitation is stable. The 7 LSBs of the primary counter are set to 7’b1111111 internally and its 3 MSBs can be set externally, which enables a counting number varying from 127 to 1023. As the startup circuitry aims to restart the SSHI circuit under excitation levels between $V_F < V_{pp(open)} < 2(V_S + 2V_D)$, the counting number set for this counter is determined by the vibration cycles of a PT attenuating from $V_{pp(open} = 2(V_S + 2V_D)$ to $V_{pp(open} = V_F$ without applying any stable excitation, which depends on the mechanical characteristics of the PT. After experimentally measuring the PT that is used in the measurements, it takes around 45 vibration cycles while it attenuates between these two excitation levels. That takes 0.55 s as its natural frequency is 82 Hz. Hence the counting number for the primary counter is set to 127 (around 1.6 s for this PT) in order to fully cover 45 attenuation cycles. For different PTs, the attenuation cycles are different but the maximum value 1023 is believed to be compatible with most of low frequency and high Q PTs.

The secondary counter (8-bit) in this stage is employed to reset the primary counter after a period of time while no *EXCI* pulse is present. This counter is reset by the pulses of the signal *EXCI* and it is driven by a 1 kHz *CLK* signal, which is internally generated. While an impulse excitation is present, a number of pulses of *EXCI* will be generated to clock the

primary counter. If the counting number is set sufficiently large, no *EXCI* will be generated and the reset input of the secondary counter is released to start counting. After a period of time without *EXCI* pulses, the secondary counter resets the primary counter and the input excitation is determined as an impulse. The counting time for this counter should ideally be set to a value much higher than $2/f_P$, where f_P is the natural frequency of the PT. In the case that the input excitation is stable, a pulse *EXCI* will be generated for each vibration cycle to reset the secondary counter before it counts out, and this finally allows the primary counter to finish counting. The finishing *OK* signal from the primary counter is generated and sent to the next Stage. The stage 3 simply employs a D-flip-flop to give the decision of this block. Once it receives a pulse from the primary counter, the output *PRECHARGE* goes to high level to the next block to pre-charge the piezoelectric device until the SSHI circuit goes back to work. When the SSHI circuit is restarted, the *WORKING* signal resets this flip-flop.

In this implementation, the power supply of the comparator and the two resistive paths in the stage 1 are cut off with the signal *WORKING* while the SSHI circuit is operating properly to minimize the power consumption. The following two digital counters and the flip-flop is not powered OFF as they consumes very little static power; instead, they keep being reset by a high level *WORKING* signal until *WORKING* goes low to enable the excitation evaluation block.

6.4.4 Pre-charging block

Another important block in the proposed SSHI rectifier is the pre-charging block, which performs the function of restarting the SSHI circuit while it receives an *PRECHARGE* signal from the excitation evaluation block. Fig. 6.8 shows the circuit diagram of this block. This whole block is controlled by a key signal *PRECHARGE*, which indicates if pre-charging is needed and it also cuts the power supply to this block when it is at a low level to minimize power loss. Once a high *PRECHARGE* signal is present, the comparator is powered ON and some digital signals in the following sub-blocks are enabled. While the comparator finds the right time to perform pre-charging, its high output enables the 16 kHz *CLK* and the enabled clock signal *CLKE* copies *CLK*. Two non-overlapping signals ϕ_1 and ϕ_2 are generated and shifted to higher voltage levels in the following two sub-blocks. The shifted signals ϕ_1 and ϕ_2 are then used to drive a charge pump circuit to pre-charge the PT to $V_{DDA} - V_{sub}$, which has a 5.25 V voltage difference. The flying capacitor used in the charge pump is implemented off-chip with $C_{PC} = 50\,\text{nF}$. Theoretically, $V_{piezo} = V_P - V_N$ can attain a maximum value of 5.25 V after several cycles of *CLKE*; however, this value is limited by $V_S + 2V_D$ due to the diodes of the bridge rectifier. While V_{piezo} is charged to $V_S + 2V_D$, V_P equals to $V_S + V_D$ and V_N equals to $-V_D$. As V_N attains $-V_D$, *SYN* goes low due to the comparator in the current

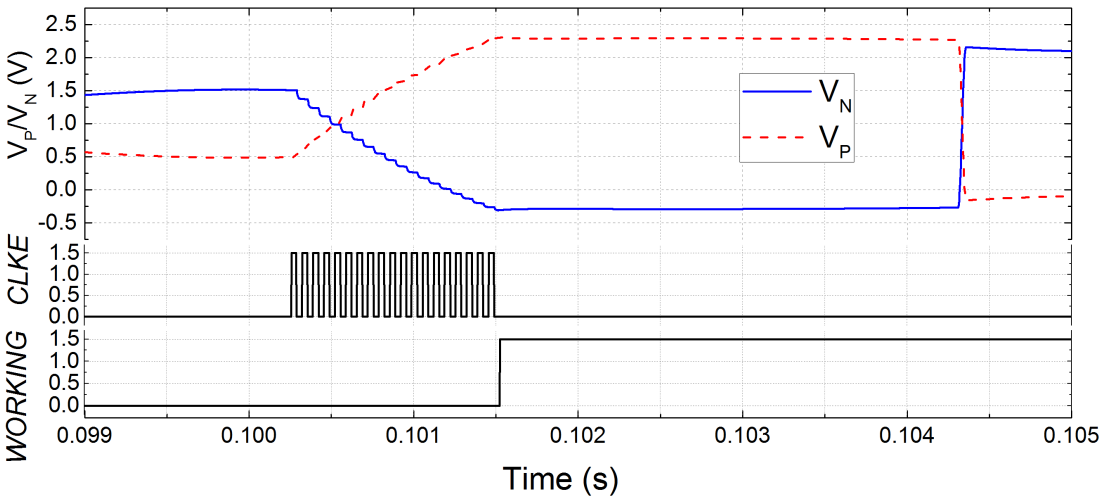


Fig. 6.9 Simulation waveforms of pre-charging block.

zero-crossing detection block in Fig. 6.4. A low level *SYN* then puts *WORKING* signal high in the "SSHI working monitoring block" in Fig. 6.6 and, a high level *WORKING* resets the *PRECHARGE* signal to low level in the stage 3 of the "excitation evaluation block" in Fig. 6.8. As *PRECHARGE* in this "pre-charging block" goes low, this whole block is powered OFF and the signals ϕ_1 and ϕ_2 are disabled to low, which turn the switches OFF in the charge pump shown in Fig. 6.8. Therefore, the pre-charging finishes automatically when $V_P - V_N$ is charged to $V_S + 2V_D$ and the SSHI circuit starts operating again.

Fig. 6.9 shows the simulated waveforms of the pre-charging block. It can be seen that the pre-charging starts while V_P is about to increase from its minimum. When the pre-charging starts, the signal *CLKE* copies *CLK* to drive the charge pump to charge C_P. Once V_N attains $-V_D$, the *WORKING* signal goes back to high level and the pre-charging state finishes. During the pre-charging period while *CLKE* signal is present, the power consumption is as high as 1.4 mW for a time period lasting less than 1 ms. Hence, a certain amount of energy (less than 1.4 µJ) is "invested" for restarting the SSHI circuit.

6.5 Simulation results

The simulations in this chapter were performed using Virtuoso, Cadence version IC6.1.5. The waveforms of the chip-level simulation are shown in Fig. 6.10. From the figure, it can be seen that the SSHI works to specification and the voltages V_P and V_N are correctly inverted before 0.125 s. Between 0.125 s and 0.19 s, there is no excitation so both the V_P and V_N go towards $\frac{1}{2}V_S$ due to the leakage (which is 1 V as $V_S = 2$ V in the simulation). After a period of time from 0.125 s, the "SSHI working monitoring" block finds that the SSHI is not working

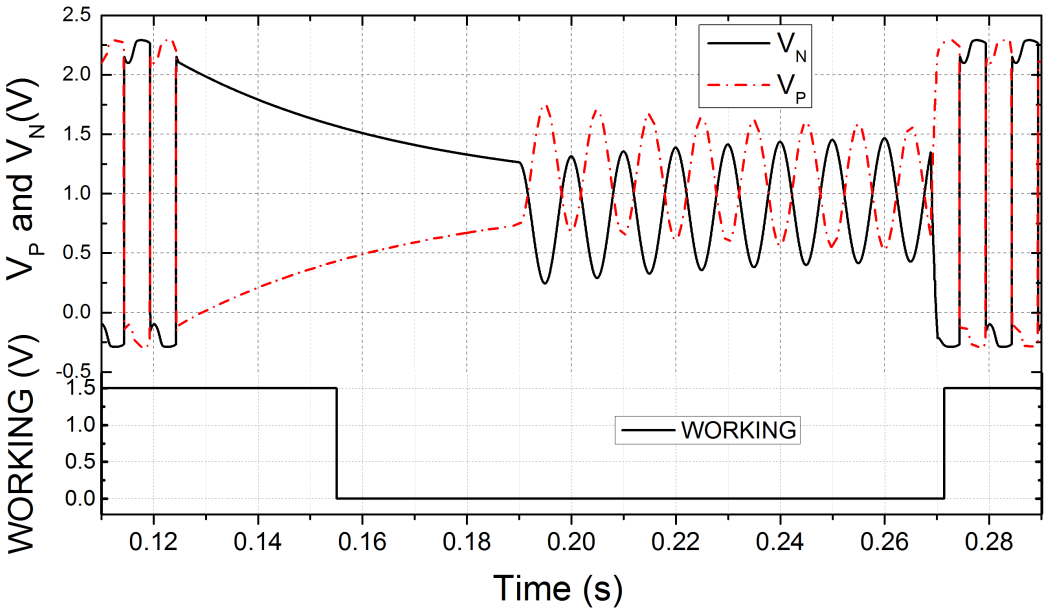


Fig. 6.10 Chip-level simulation waveforms.

and makes *WORKING* signal go to a logic low level. From 0.19 s, a weak excitation is present. The amplitude of this excitation satisfies the condition $V_{pp(open)} > V_F$ but it cannot satisfy $V_{pp(open)} > 2(V_S + 2V_D)$. Hence, the conventional SSHI circuit will not work in this case and will not extract any energy. But in the proposed SSHI rectifier with self-startup circuitry, the SSHI circuit is restarted after several periods of excitation evaluation. The pre-charging occurs at the time 0.27 s. When V_N approaches $-V_D$, the *WORKING* signal goes back to high level so the SSHI circuit is now restarted.

6.6 Measurement results and discussion

The proposed SSHI rectifier with self-startup circuitry was experimentally evaluated using a commercially available piezoelectric transducer (PT) of dimension 47 mm $\times$ 36 mm (Mide Technology Corporation V20W). A shaker (LDS V406 M4-CE) was excited at the natural frequency of the PT at 82 Hz and driven by a sine wave from a function generator (Agilent Technologies 33250A 80 MHz waveform generator) amplified by a power amplifier (LDS PA100E Power Amplifier). An off-chip voltage regulator (ON Semiconductor NCP4681DSQ15T1G) with ultra-low ground leakage current ($I_{GND} \approx 1.5\,\mu A$) was employed to provide a stable 1.5 V if $V_S \geq 1.5$ V. When the system is self-sustained and at a fully-discharged state, the system simply works as a full-bridge rectifier (threshold is very low due to low V_S) and V_S needs to be charged to 1.5 V before the proposed circuit starts working.

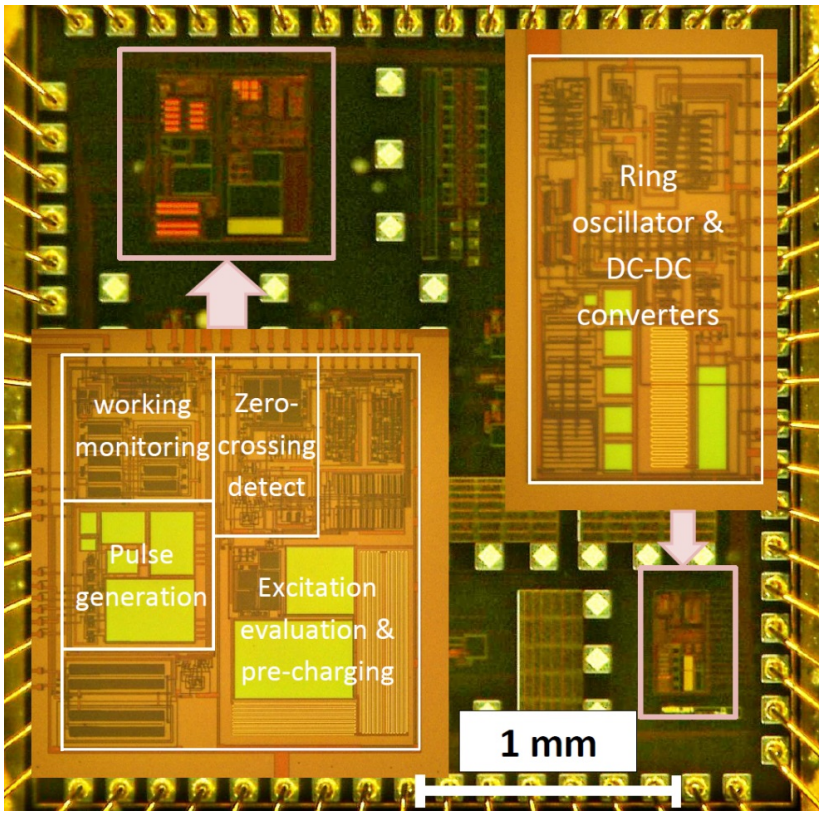


Fig. 6.11 Micrograph of the test chip fabricated in a 0.35 µm CMOS foundry process. The overall die size is 2.8 mm × 3.2 mm. The active area for the proposed circuit is around 0.6 mm^2.

Hence, an external power supply at 1.5 V was also used for some cases. A super capacitor is employed as the energy storage capacitor (AVX BestCap BZ05CA103ZSB, measured capacitance $C_S \approx 5.2$ mF) and four off-chip diodes (DIODES INC. DFLS130L-7, measured voltage drop when working in a bridge rectifier is $V_D \approx 0.2$ V) are employed to build a full-bridge rectifier. The voltage drop of the diodes can be measured by employing a full-bridge rectifier (refer to Fig. 2.5) and measuring the higher and lower limits of V_P and V_N to obtain the effective voltage drop of the four diodes. The proposed chip was implemented in a 0.35 µm HV CMOS process. Fig. 6.11 shows the die photo of the test chip. The active area of the proposed SSHI rectifier together with the DC-DC converters and clock generator is 0.6 mm^2. Off-chip capacitors are used for the SC converters due to limited design area and the rest of the chip is occupied by other circuits for other projects.

Table 6.1 lists the power loss due to different blocks of the interface circuit. While the SSHI circuit is operating, the level shifters consumes high dynamic power due to driving switches, especially the big W/L CMOS switches controlling the inductor. As these two switches have very large transistor width for low ON-resistance purposes, the parasitic capac-

Table 6.1 Breakdown of the chip power consumption.

	Power loss	
Loss mechanism	SSHI working	SSHI not working
Ring oscillator	260 nW	260 nW
DC converters	13 nW	13 nW
Level shifters	286 nW	19 nW
Zero-crossing detect	211 nW	198 nW
Pulse generator	6 nW	0.1 nW
Work monitoring	0.4 nW	0.4 nW
Excitation evaluation	0.2 nW	152.4 nW
Total	776.6 nW	642.9 nW

itance associated with the gate is extremely large, which increases the energy consumption per switch. When the SSHI circuit is not working, the driving signal ϕ_{SSHI} of the big W/L switches is kept at low level, hence the power loss due to level shifters is significantly decreased. As the comparator in the zero-crossing detection block constantly outputs a high SYN signal while SSHI is not working, there is no dynamic power loss for this comparator. But the excitation evaluation block is powered ON which consumes extra power while SSHI is not working. From the table, the power consumption while the SSHI circuit is not working is found to be less than when the SSHI circuit is working. Another power-consuming block not listed in the table is the pre-charging block, which consumes 1.4 µJ for one startup. The average power loss due to this 1.4 µJ startup energy is difficult to be calculated as it depends on the environmental vibration and how frequently the SSHI rectifier needs to be restarted. Assuming the SSHI circuit needs to be restarted for every 100 s, the duty ratio for this block is around 0.001% and the average power loss is around 14 nW.

Fig. 6.12 shows waveforms of V_N, ϕ_{SSHI}, $WORKING$ and $PRECHARGE$ from an oscilloscope. The signals were measured in a period of 20 s by changing the input excitation amplitude when necessary and $C_S = 2$ V. Before the time t_1, the SSHI circuit is working and the input excitation is high enough to maintain operation of the SSHI interface. Pulses ϕ_{SSHI} are generated correctly to invert V_{piezo} and the signal $WORKING$ is at high level. Between t_1 and t_2, the excitation is decreased to a very low level. As a result, ϕ_{SSHI} cannot be generated and $WORKING$ goes to a low level indicating that the SSHI is not working. Between t_2 and t_3, the excitation is slightly increased but the condition for maintaining the SSHI operational is still not satisfied. This weak excitation is evaluated by the “excitation evaluation" block, which decides not to restart the SSHI circuit. From t_3, the excitation is further increased. After evaluating the input excitation for 1.6 s to make sure that it is not a

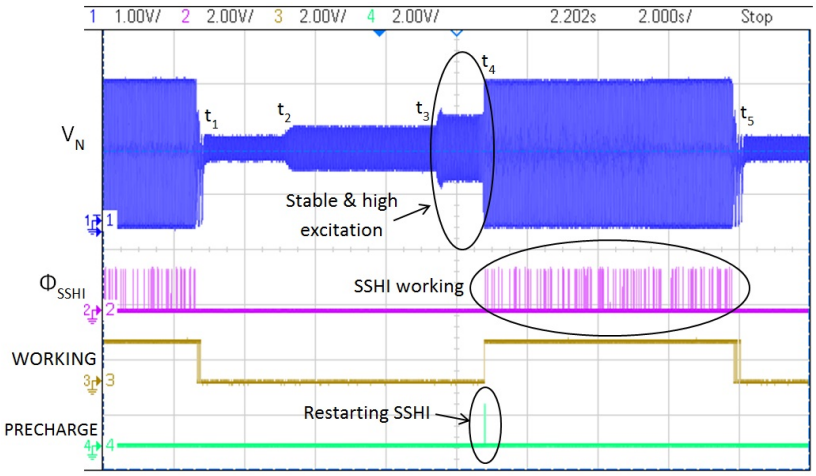


Fig. 6.12 Measured waveforms of signal V_N, ϕ_{SSHI}, *WORKING* and *PRECHARGE* in a period of 20 s.

shock, a *PRECHARGE* pulse is generated to restart the SSHI circuit at time t_4. From this instant, *WORKING* goes back to a high level until the input excitation is decreased to a very low level at time t_5.

The waveforms in a short period of time while restarting the SSHI circuit is shown in Fig. 6.13. After the excitation evaluation block decides to restart the SSHI circuit, a *PRECHARGE* pulse is generated to pre-charge the PT. During the pulse of *PRECHARGE*, *CLKE* copies the 16 kHz clock and V_N is charged to $-V_D$. Once V_N attains $-V_D$, *WORKING* goes high, which clears the signal *PRECHARGE* and the pre-charging state terminates. As the SSHI circuit is now working, the signal ϕ_{SSHI} can be correctly generated to invert the voltage across the PT at each I_P zero-crossing point. The waveforms obtained are consistent with the operation as described in Sections 6.4 and 6.5.

Fig. 6.14 shows the measured power obtained at the output capacitor C_S of the rectifier for different V_S. The PT was excited at 82 Hz with an open-circuit voltage $V_{pp(open)} = 2.8\,\text{V}$ (equivalent to 2.0 g) for the measurements. The experiments were performed with a full-bridge rectifier and the proposed SSHI rectifier with self-startup circuitry while the value of the inductor is changed. With the fabricated chip, the full-bridge rectifier can be achieved by forcing the voltage-inverting signal ϕ_{SSHI} being at low level and disabling the SSHI circuit. According to the figure, the full-bridge rectifier was able to provide a maximum output power of 13.5 µW with an optimal V_S voltage of 0.6 V. As expressed in (6.1), the condition for starting the SSHI circuit is $V_{pp(open)} > 2(V_S + 2V_D)$; hence, the theoretical condition for that the SSHI circuit can be started is $V_S < \frac{V_{pp(open)}}{2} - 2V_D$, or $V_S < 1.2\,\text{V}$. As shown in Fig. 6.14, region 1 and region 2 represent the allowed region and the forbidden region for the conventional SSHI rectifier, respectively. Compared to the conventional SSHI rectifier,

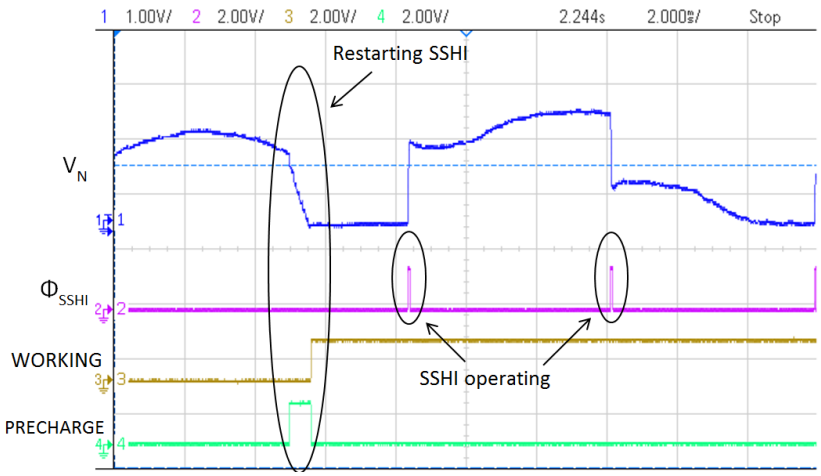


Fig. 6.13 Measured waveforms in a short period of time while restarting the SSHI circuit.

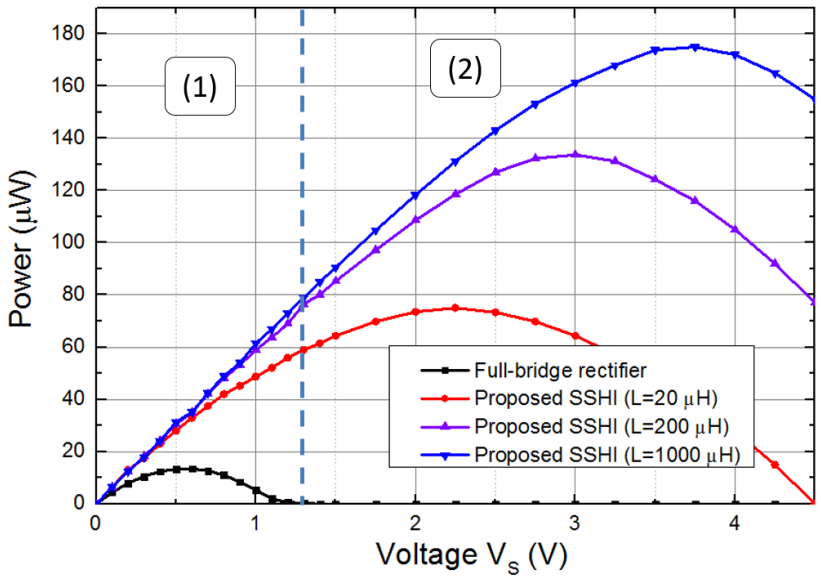
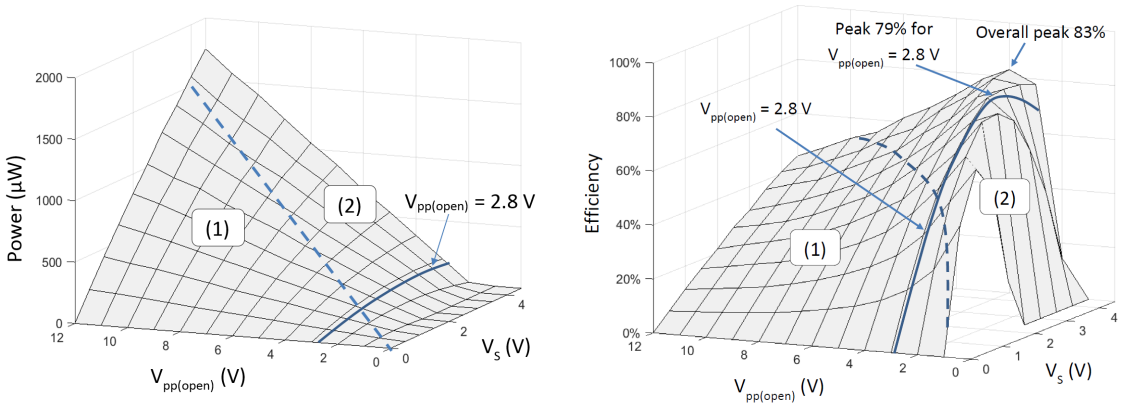


Fig. 6.14 Measured electrical power output of full-bridge rectifier and the proposed SSHI rectifier with off-chip diodes ($V_D = 0.2\,\mathrm{V}$), where the horizontal axis V_S represents the voltage across the storage capacitor C_S and $V_{pp(open)} = 2.8\,\mathrm{V}$.



(a) Power.

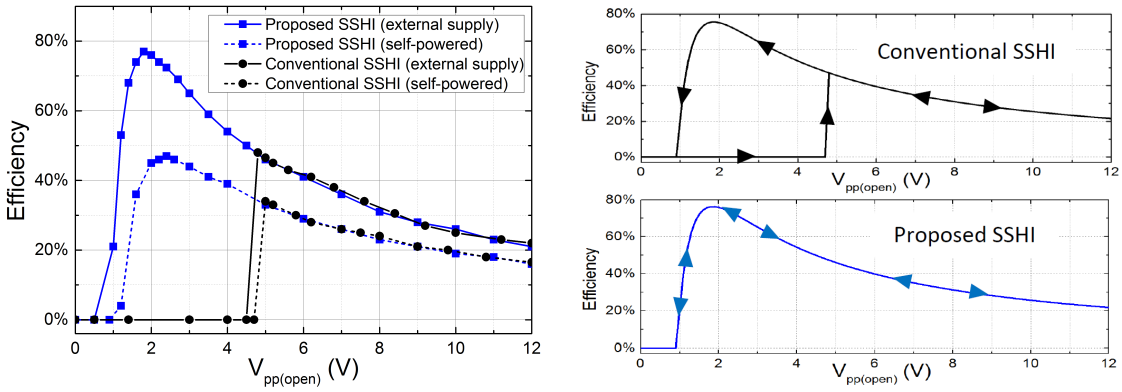
(b) Efficiency.

Fig. 6.15 3-D surface plot of measured output electrical power and efficiency in function of $V_{pp(open)}$ and V_S while the inductor is chosen at $L = 1\,\text{mH}$ (with external stable 1.5 V power supply and the conversion efficiency of voltage regulator is not considered).

the improved SSHI rectifier with self-startup circuitry is able to start the SSHI circuit at a lower excitation amplitude (or at a higher V_S for a given $V_{pp(open)}$), as expressed in (6.3). Considering the startup issues of conventional SSHI rectifiers, the proposed circuit can easily achieve theoretical maximum power points while the conventional SSHI circuit cannot work at these points if not previously re-started. Hence, the proposed SSHI is allowed to work in both regions 1 and 2.

Similar experiments and output power plots for conventional SSHI rectifiers have been presented in [167, 175, 151], in which the SSHI startup issue was not addressed. Although some of the implementations use other methods to detect the voltage peak and are able to flip V_{piezo} until it attains $V_S + 2V_D$ (or $-(V_S + 2V_D)$) to start the SSHI circuits, employing "working monitor" and "excitation evaluation" blocks can be considered as useful and significant additions to determine when to start the SSHI circuit in order to avoid energy loss due to flipping V_{piezo} at weak excitation levels. According to the theoretical calculation and experimental results in Fig. 6.14 in this chapter, if an SSHI rectifier is not started, a high V_S voltage prevents the rectifier from harvesting energy while the SSHI circuit is not working. In real-world implementations, it is impractical to perform manual startup (such as shaking the harvester) after each period of time, where the excitation level is extremely low, when the SSHI circuits stop working. Hence, adding a startup circuitry in an SSHI rectifier is practically essential to increase the average output power so that energy can still be extracted at moderate or low excitation levels.

Fig. 6.15 shows the measured electrical output power and efficiency in a surface plot while $V_{pp(open)}$ is varied from 0 V to 12 V with steps of 1 V and V_S is varied from 0 V to



(a) (b)

Fig. 6.16 (a) Measured power efficiency for the proposed SSHI with startup circuitry and the conventional SSHI without startup circuitry while the circuit is externally powered and self-powered using an off-chip voltage regulator. (b) Efficiency variation while excitation level is swept in two directions.

4.5 V with steps of 0.5 V representing 130 independent measurements. The regions 1 and 2 separated by dotted curves represent the allowed and forbidden regions, respectively, for conventional SSHI circuits. The inductor used in these measurements was chosen at 1 mH and the $V_{pp(open)} = 2.8\,\mathrm{V}$ plane (corresponding to Fig. 6.14) is highlighted. It can be seen that while the excitation level $V_{pp(open)}$ is small (less than 3 V), the maximum power point in function of V_S can be attained over the measured V_S range ($0\,\mathrm{V} \rightarrow 4.5\,\mathrm{V}$). However, when the excitation goes higher, the maximum power point is shifted to higher V_S. As the peak power points under higher excitation levels cannot be achieved as $V_{pp(open)}$ goes higher, the power efficiency decreases although the output power increases. From Fig. 6.15b, it can also be found that the startup circuitry allows the proposed SSHI rectifier to achieve efficiency peaks in region 2 while the conventional SSHI rectifier can only work in the region 1.

Fig. 6.16a shows the measured power efficiency from the PT to the storage capacitor C_S for the proposed SSHI with startup circuitry and the conventional SSHI without startup circuitry while the circuit is externally powered and self-powered. The voltage across the storage capacitor is $V_S = 2\,\mathrm{V}$, the inductor is chosen at 1 mH and the excitation level is swept for $V_{pp(open)} = 0\,\mathrm{V} \rightarrow 12\,\mathrm{V}$. For conventional SSHI circuits, if the SSHI circuit is not manually started, the circuit does not harvest any energy until $V_{pp(open)}$ goes higher than $2(V_S + 2V_D) = 4.8\,\mathrm{V}$. However, for the proposed SSHI circuit, $V_{pp(open)}$ just needs to overcome V_F, which is around 1 V. This allows the proposed circuit to achieve the theoretical peak efficiency point and it can harvest energy over an increased input range. Fig. 6.16b shows the efficiency variation while the excitation level is swept from low to high and from high to low. The conventional SSHI circuit is only able to achieve the theoretical peak

performance when the excitation moves from high to low because the SSHI circuit has been started by high excitation before; but from low to high, the conventional SSHI cannot work as expected until it overcomes the $2(V_S + 2V_D)$ threshold. However, the proposed SSHI circuit is able to achieve the expected performance in both excitation sweeping directions.

6.7 Conclusion

This chapter identified a startup problem that exists with the conventional SSHI interface circuits that are commonly used in piezoelectric energy harvesters due to the high power efficiencies. This startup issue limits the operational range of conventional SSHI rectifiers making it difficult to extract any energy under low excitation input. An improved SSHI architecture is introduced in this chapter to dynamically detect the operation of the SSHI circuit and automatically restart the circuit when it is not operational and the excitation input meets startup conditions. Theoretical calculations and measured results show that the proposed SSHI interface circuit is able to extract energy in an increased input range starting from a much lower excitation amplitude. With an increased input range, the proposed SSHI circuit can achieve the theoretical maximum power point and the maximum efficiency point while the conventional SSHI circuit can only attain these points if it has been previously started off at a higher excitation amplitude. This approach thus provides the ability to re-start the SSHI circuit and increase the operational range under practical excitation conditions without consuming additional power. This work also sets the stage for future designs that can tune the configuration of the interface power conditioning circuit for energy harvesters with a view towards maximizing output power by dynamically evaluating the operating environmental conditions.

Chapter 7

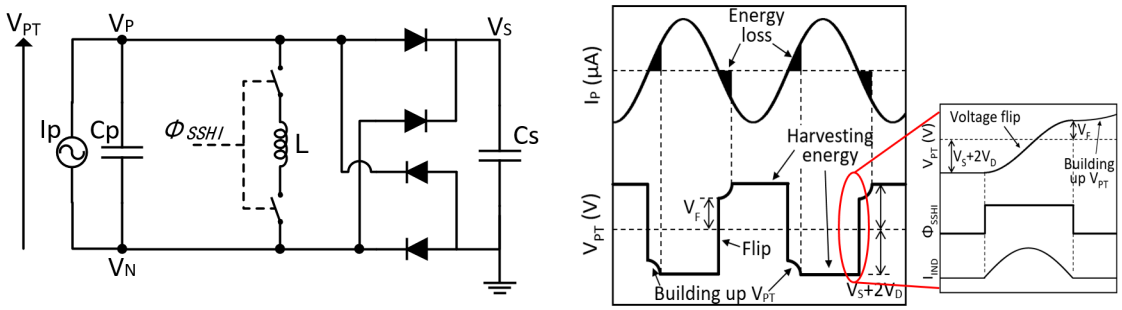
An Inductorless Bias-flip Rectification Circuit

7.1 Introduction

In this chapter, an alternative Synchronized Switch Harvesting on Capacitors (SSHC) approach is proposed to synchronously flip the voltage across the PT using one or multiple switched capacitors instead of an inductor [199]. Compared with the well-known SSHI circuit, this design does not require any inductor, thus significantly reduces the required system volume. This feature is especially suitable for miniaturized energy harvesting systems, such as implantable devices and miniaturized wireless sensor nodes. Compared to reported state-of-the-art interface circuits, the proposed circuit also achieves higher voltage flip efficiency, hence higher energy extraction efficiency. The background and conventional SSHI interfaces are presented in Section 7.2. The proposed interface circuit and circuit implementations are shown in Section 7.3 and Section 7.4, respectively. Section 7.5 provides measured results and comparisons with state-of-the-art interface circuits and a summary and conclusion is provided in Section 7.6.

7.2 Inductor-based SSHI interface

Fig. 7.1a shows the circuit schematic of a parallel-SSHI rectifier, which consists of a full-bridge rectifier (FBR) with a switch-controlled inductor to synchronously flip the voltage across the PT. A piezoelectric transducer (PT) is modeled as a current source I_P in parallel with a capacitor C_P. The associated waveforms of the SSHI circuit are shown in Fig. 7.1b. Before zero-crossing instants of the current source I_P, the voltage across the PT, V_{PT}, equals



(a) Circuit diagram of an SSHI interface

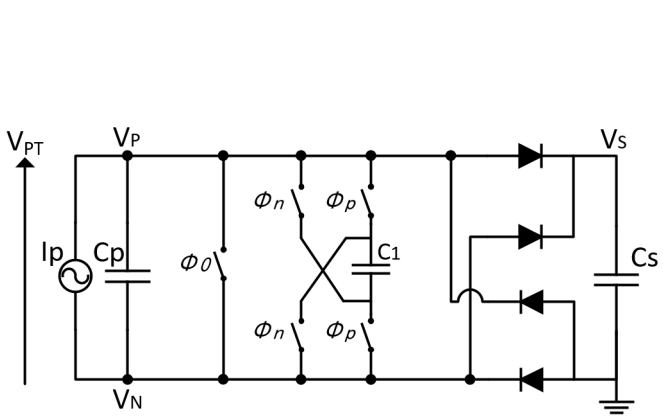
(b) Waveforms

Fig. 7.1 SSHI interface circuit and the associated waveforms

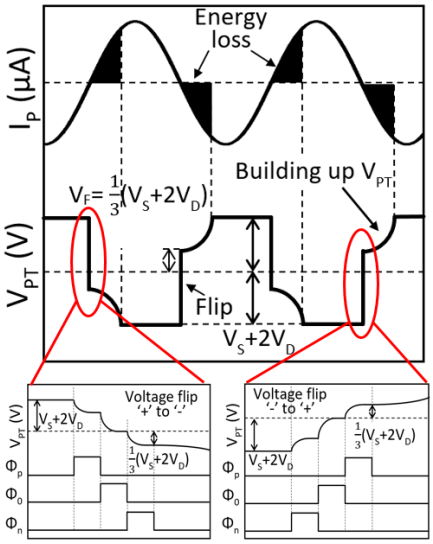
to $V_S + 2V_D$ or $-(V_S + 2V_D)$. In order to overcome the threshold set by the FBR and transfer energy into the storage capacitor C_S in the next half-cycle, V_{PT} needs to be flipped from $V_S + 2V_D$ to $-(V_S + 2V_D)$ (or vice-versa). In an SSHI interface, analog switches driven by a synchronized pulse signal ϕ_{SSHI} are employed to control the RLC oscillation loop to flip the voltage. The resulting flipped voltage V_F is always lower than $V_S + 2V_D$ due to the resistive damping in the RLC loop, which can written as $V_F = (V_S + 2V_D)e^{-\frac{\pi}{\sqrt{\frac{4L}{R^2C}-1}}}$. After the voltage flip, $|V_{PT}|$ needs to be charged from V_F to $V_S + 2V_D$ and this amount of energy is wasted. Therefore, the power efficiency of an SSHI interface usually depends on the voltage flip efficiency, which is expressed as:

$$\eta_{SSHI} = \frac{V_F}{V_S + 2V_D} = e^{-\frac{\pi}{\sqrt{\frac{4L}{R^2C_P}-1}}} \tag{7.1}$$

where C_P, L and R represent the internal capacitor of the PT, the inductor and total resistance in the RLC loop, respectively. As C_P is inherently constant for a given PT, η_{SSHI} can only be increased by increasing L or decreasing R. In order to miniaturize the system, L is typically chosen in the range of a few mH; however, an inductor of this value still occupies significant system volume. While decreasing R, the transistor sizes of the two analog switches shown in Fig. 7.1a need to be designed to be very large, increasing the gate capacitance of the transistors. These large switches are usually power-hungry when driven, especially for high frequency PTs since the synchronized switches are turned ON and OFF more frequently in this case. The following sections of this chapter propose a novel interface circuit with the ability of performing highly efficient voltage flipping without employing inductors, hence the energy efficiency is increased with smaller required volume.



(a) SSHC interface with one charge-swap capacitor



(b) Waveforms

Fig. 7.2 Proposed SSHC interface circuit and the associated waveforms

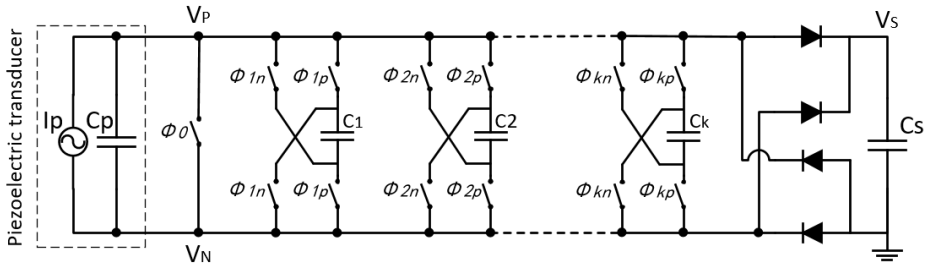
7.3 Proposed inductor-less SSHC interface circuit

In this section, an inductor-less interface circuit is introduced, which employs one or multiple synchronized switched capacitors to increase voltage flip efficiency and hence power extraction efficiency. The performance is then compared with an SSHI interface circuit.

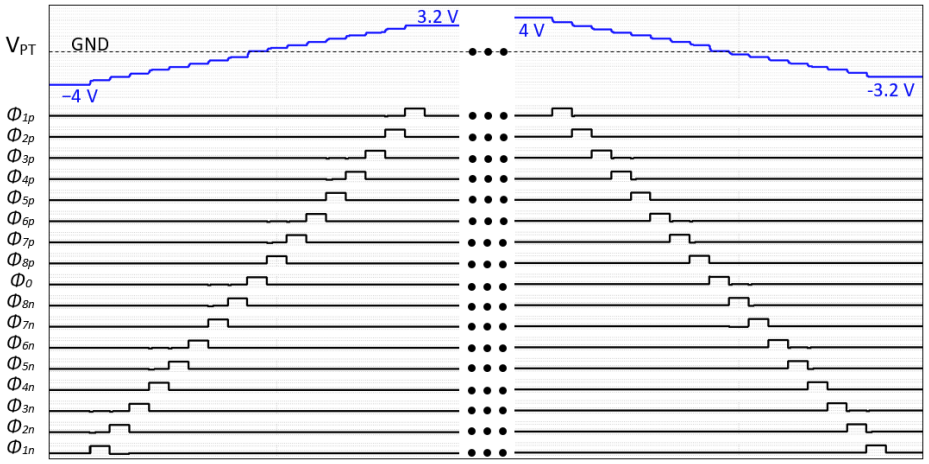
7.3.1 SSHC with one capacitor

Fig. 7.2a shows the circuit diagram of the proposed SSHC (synchronized switched harvesting on capacitors) interface circuit with one switched capacitor C_1, or it can be called a charge-swap capacitor. In order to perform the charge inversion, five analogue switches driven by three pulse signals (ϕ_p, ϕ_0 and ϕ_n) are used. The three non-overlapping switching signals are synchronously generated to turn ON the five switches sequentially in a specific order. The order of the three pulses depends on the polarization of the voltage V_{PT}.

Fig. 7.2b shows the waveforms of the voltage V_{PT} and the three pulse signals driving the five switches. At each zero-crossing moment of I_P, the three pulse signals (ϕ_p, ϕ_0 and ϕ_n) are sequentially generated to flip the voltage V_{PT}. Assuming $V_{PT} = V_S + 2V_D$ before the flipping instant (the left zoom-in figure), V_{PT} needs to be flipped towards negative. In this case, the pulse ϕ_p is first generated to damp a part of charge from C_P into the charge-swap capacitor C_1. Then, the pulse ϕ_0 clears the residual charge in C_P and the pulse ϕ_n charges C_P from C_1 in the opposite sense. This allows the voltage V_{PT} to be partially flipped. While



(a) SSHC interface with k synchronized switched capacitors



(b) Simulated waveforms of V_{PT} flip instants for the SSHC interface with 8 synchronized switched capacitors

Fig. 7.3 Proposed SSHC interface circuit with k synchronized switched capacitors

V_{PT} is supposed to be flipped from $-(V_S+2V_D)$ towards positive polarity, the three pulses are now generated in an inversed order: $\phi_n \rightarrow \phi_0 \rightarrow \phi_p$ (the right zoom-in figure). As shown in the figure, the optimal resulting voltage after flipping is $V_F = \frac{1}{3}(V_S+2V_D)$. Hence, the optimal flipping efficiency while employing one switched capacitor is $\eta_{SSHC-1} = 1/3$ and the calculation of this efficiency will be presented in Section 7.3.3.

7.3.2 SSHC with multiple capacitors

In order to flip additional charge across the capacitor C_P, more synchronized switched capacitors can be added to transfer more charge from C_P into a series of capacitors and conversely charge C_P to a higher voltage level. Fig. 7.3a shows the proposed SSHC interface circuit with k switched capacitors. In this design, there are $4k+1$ analog switches and $2k+1$ switching signal phases: ϕ_0, ϕ_{1p}, ϕ_{1n}, ϕ_{2p}, ϕ_{2n}, ϕ_{3p}, ϕ_{3n}, etc.

Assuming the number of switched capacitors is $k = 8$, the instant when V_{PT} is being flipped from $-(V_S+2V_D)$ towards positive polarity and from V_S+2V_D towards negative

are shown in Fig. 7.3b. The voltage V_{PT} and the 17 (as $2k+1$ while $k=8$) phases of the switching signals are shown in the figure. From the figure, it can be seen that, in order to flip V_{PT} from $-(V_S+2V_D)$ towards positive polarity, the phase order of the 17 pulses is: ϕ_{1n}, ..., ϕ_{8n}, ϕ_0, ϕ_{8p}, ..., ϕ_{1p}. The first 8 phases aim to sequentially transfer charge from C_P to the 8 switched capacitors, C_1 to C_8. The phase ϕ_0 clears the residual charge in C_P and the following 8 phases sequentially connect the 8 switched capacitors in an opposite sense to flip the voltage V_{PT}. While V_{PT} needs to be flipped from V_S+2V_D towards negative, the phase order of the 17 pulses is completely reversed, as shown in the figure.

7.3.3 Performance analysis

In this section, the voltage flip efficiency of the proposed SSHC interface circuit is calculated and its performance is compared with the SSHI interface.

Assuming only one switched capacitor is present in the SSHC interface circuit, as previously shown in Fig. 7.2a, and the voltage V_{PT} needs to be flipped from positive to negative at the first I_P zero-crossing moment, this voltage equals to V_S+2V_D. Before the first flipping is performed, the voltage across the switched capacitor is zero, noted as $V_1=0\,\mathrm{V}$. At the first zero-crossing moment of I_P, the first pulse ϕ_p is present. C_P and C_1 are connected and the charge flows into C_1 until the voltages across the two capacitors are equal. As the total charge keeps unchanged, the voltage across C_P and C_1 at the end of first phase ϕ_p is:

$$V_{PT}=V_1=\frac{C_P}{C_P+C_1}(V_S+2V_D) \tag{7.2}$$

where V_1 is voltage across the switched capacitor C_1. At the second phase, a pulse ϕ_0 is generated to clear the residual charge in C_P. The charge in C_1 remains unchanged during this phase. Hence the voltage across C_P and C_1 at the end of the second phase is:

$$\begin{aligned} V_{PT}&=0\\ V_1&=\frac{C_P}{C_P+C_1}(V_S+2V_D) \end{aligned} \tag{7.3}$$

At the third phase ϕ_n, C_1 is connected with C_P in an opposite sense to charge C_P to a negative voltage. Due to the conservation of charge in these two capacitors, the remaining charge in C_1 after the second phase is shared between C_P and C_1. Hence the voltages V_{PT} and V_1 at the end of the third phase are:

$$V_{PT}=V_1=-\frac{C_PC_1}{(C_P+C_1)^2}(V_S+2V_D) \tag{7.4}$$

It can be seen that V_{PT} is a negative value after three phases of voltage flipping. By setting the derivative of the above expression to 0, it can be found that V_{PT} attains its minimum value when $C_1 = C_P$. Therefore, the minimum value of V_{PT} at the end of the first voltage flipping is:

$$V_{PT} = V_1 = -\frac{1}{4}(V_S + 2V_D) \quad (while\ C_P = C_T) \tag{7.5}$$

The resulting voltage obtained in the above equation is under the assumption that the initial voltage across the switched capacitor C_1 is 0 V at the beginning. However, before the second zero-crossing moment where V_{PT} needs to be flipped from negative to positive, V_1 is not 0 V but it equals to $V_1 = -\frac{1}{4}(V_S + 2V_D)$. Assuming $C_1 = C_P$ is chosen for future calculations, V_{PT} and V_1 values after each phase of ϕ_n, ϕ_0 and ϕ_p during the second voltage flipping stage are:

$$\begin{aligned}
&before\ \phi_n:\ V_{PT} = -(V_S + 2V_D),\ \ V_T = \frac{1}{4}(V_S + 2V_D) \\
\Rightarrow &after\ \phi_n:\ V_{PT} = -V_1 = -(\frac{1}{4} + 1)\frac{1}{2}(V_S + 2V_D) \\
\Rightarrow &after\ \phi_0:\ V_{PT} = 0\,\mathrm{V},\ \ V_1 = (\frac{1}{4} + 1)\frac{1}{2}(V_S + 2V_D) \\
\Rightarrow &after\ \phi_p:\ V_{PT} = V_1 = (\frac{1}{4} + 1)\frac{1}{4}(V_S + 2V_D) = ((\frac{1}{4})^2 + \frac{1}{4})(V_S + 2V_D) = \frac{5}{16}(V_S + 2V_D)
\end{aligned} \tag{7.6}$$

It can be seen from (7.6) above, more charge is inverted in the second zero-crossing moment compared to the first one. Due to the accumulation of remaining charge in C_T, the resulting $|V_{PT}|$ at the end of the n^{th} voltage flipping stage is:

$$\begin{aligned}
&|V_{PT}| = ((\frac{1}{4})^n + \cdots + (\frac{1}{4})^2 + \frac{1}{4})(V_S + 2V_D) = \sum_{1 \le i \le n} (\frac{1}{4})^i (V_S + 2V_D) = \frac{\frac{1}{4} - (\frac{1}{4})^n}{1 - \frac{1}{4}}(V_S + 2V_D) \\
&\Rightarrow \lim_{n \to \infty} |V_{PT}| = \frac{1}{3}(V_S + 2V_D)
\end{aligned} \tag{7.7}$$

While n tends to infinity, $|V_{PT}|_{n\to\infty} = \frac{1}{3}(V_S + 2V_D)$, which means that the optimal voltage flip efficiency for the SSHC interface circuit with one switched capacitor is $\eta_{SSHC-1} = \frac{1}{3}$ while $C_1 = C_P$. Similar calculations can be performed for SSHC circuits with multiple synchronized switched capacitors. Considering SSHC interfaces with up to 8 switched

Table 7.1 Performance comparison between SSHI and SSHC

SSHC capacitor number	Voltage flip efficiency	Required L for SSHI (mH)
1	1/3	0.26
2	1/2	0.61
3	3/5	1.09
4	2/3	1.71
5	5/7	2.48
6	3/4	3.38
7	7/9	4.42
8	4/5	5.60

capacitors, the voltage flip efficiencies are calculated and shown in Table 7.1. The first column is the number of switched capacitors employed for a SSHC interface and the second column shows the calculated voltage flip efficiencies. The flip efficiencies shown in the table are the values under assumptions that all the switched capacitors have the same capacitance of the PT internal capacitor C_P, such that $C_1 = C_2 = ... = C_8 = C_P$. The third column shows the calculated inductor value required for a SSHI interface circuit to achieve the same voltage flip efficiencies. The equation for calculating the SSHI flip efficiencies is given in (7.1). In the calculations, the capacitance is set as 45 nF, which matches the C_P for the measurements in this chapter, and the total resistance in the RLC loop is assumed to be 70 Ω, which depends the ON resistance of analog switches, DC resistance of the inductor and all parasitic resistance including wires and vias.

From the table, it can be found that the SSHI interface circuit requires large inductors to achieve equal voltage flip efficiencies as the SSHC interface circuit. An inductor in the mH scale typically occupies a volume of $\sim$ 100's mm^3; however, a surface-mount ceramic capacitor (0402 package) can take up a volume of less than 1 mm^3. Hence, the proposed SSHC interface circuit significantly reduces the system volume by employing capacitors instead of inductors. This advantage is particularly suitable for miniaturized harvesting systems. In the next section, the circuit implementations of the proposed SSHC interface circuit will be presented.

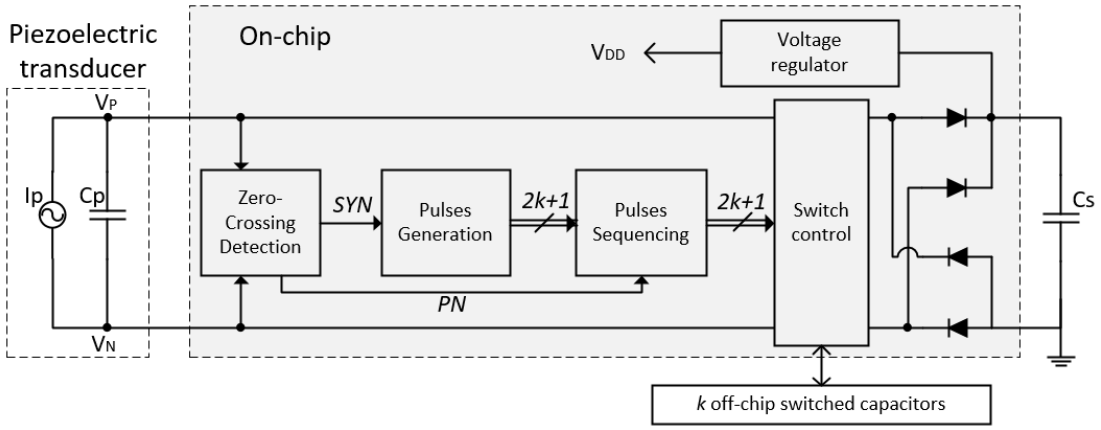


Fig. 7.4 System architecture of the proposed SSHC interface circuit

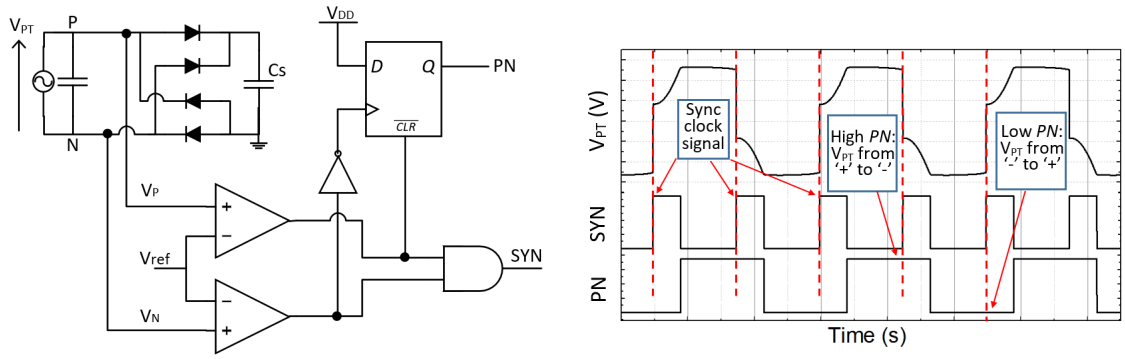
7.4 Circuit implementation of the proposed SSHC interface

7.4.1 System architecture

The system architecture of the proposed SSHC interface circuit is shown in Fig. 7.4. The five blocks implemented on-chip are "zero-crossing detection", "pulse generation", "pulse sequencing", "switch control" and "voltage regulator" blocks. At each zero-crossing moment of I_P, a rising edge is generated in signal SYN and the signal PN indicates the direction that V_{PT} will be flipped, where $V_{PT} = V_P - V_N$. The signal PN is needed because the pulse phase orders for different voltage flip directions are different, as shown in Fig. 7.3b. Assuming there are k switched capacitors employed in the SSHC circuit, after the "pulse generated" block reads a rising edge in SYN, $2k+1$ sequential pulses are generated. In the following "pulse sequencing" block, these $2k+1$ signals are sequenced according to the level of the signal PN. Then, these sequenced $2k+1$ signals are used to drive analog switches in the "switch control" block to perform voltage flipping with the k off-chip capacitors. In order to achieve the optimal voltage flip efficiency, the values of the k off-chip capacitors are chosen as $C_1 = C_2 = ... = C_k = C_P$. A voltage regulator with over-voltage protection is employed to make the system being self-powered. The internal transistor-level circuit diagrams and operations for each block are presented and explained in the following sections.

7.4.2 Zero-crossing detection

Fig. 7.5a shows the circuit diagram of the zero-crossing detection block. In order to find the zero-crossing moment of the current source I_P, two continuous-time comparators are



(a) Circuit diagram of zero-crossing detection block

(b) Associated waveforms

Fig. 7.5 Zero-crossing detection block

employed to compare V_P and V_N with a reference voltage V_{ref}. While I_P is close to zero, the diodes of the full-bridge rectifier (FBR) are just about to turn OFF. At this moment, one of V_P and V_N is close to $-V_D$ and the other one is close to $V_S + V_D$. Hence, the reference voltage V_{ref} is set slightly higher than the negative value of the voltage drop of a diode ($-V_D$) so that either V_P or V_N going from $-V_D$ towards positive can trigger the comparator and generate a synchronous signal. The outputs of these two comparators are ANDed so that a rising edge in the SYN signal is generated to flip the voltage V_{PT} for each zero-crossing moment of I_P. Fig. 7.5b shows the associated waveform of this block. A signal named PN is also generated in this block, which indicates the polarization of V_{PT} before it is flipped at each zero-crossing moment. This signal is then used in the "pulse sequencing" block to help sequence the switch-driving pulses.

7.4.3 Pulse generation

Fig. 7.6 shows the circuit diagram of the pulse generation block for up to 8 switched capacitors in the SSHC interface circuit. 17 pulse cells are employed in this block to generate up to 17 sequential pulses, of which the pulse width can be tuned externally. The input signal SYN is the synchronous clock signal generated from the zero-crossing detection block. A rising edge in SYN drives the 17 pulse cells sequentially to generate one individual pulse in each cell. The 8 off-chip switched capacitors can be selectively enabled by input signals $EN_1 - EN_8$ and signal EN_0 enables the phi_0 switch, which aims to clear the residual charge in C_P. These 9 digital input signals can be set externally according to the number of switched capacitors employed. If all of these 9 signals are low, the interface circuit simply works as a full-bridge rectifier. The input EN_0 is forced to high if any of $EN_1 - EN_8$ are high because

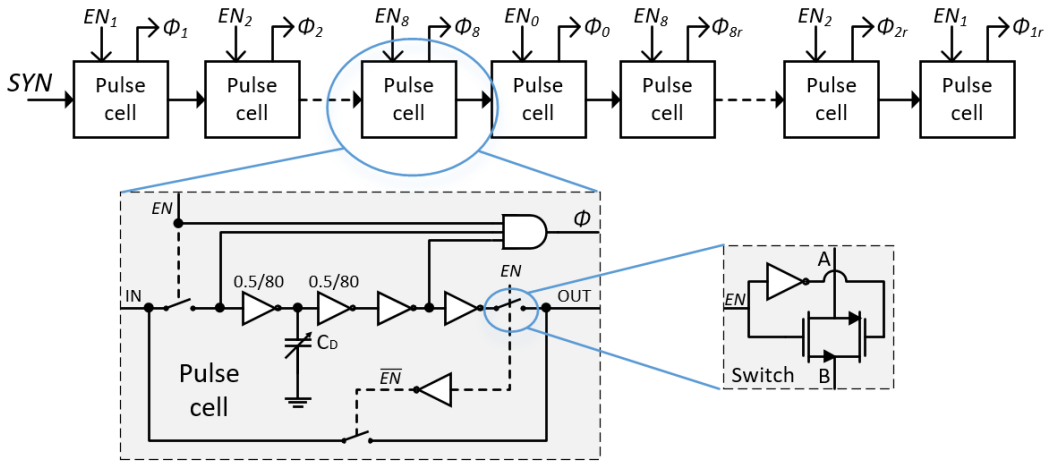


Fig. 7.6 Circuit diagram of the pulse generation block

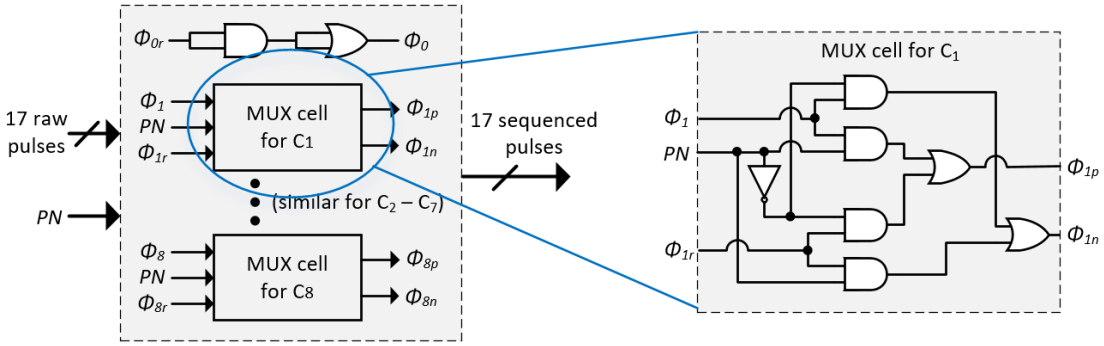


Fig. 7.7 Circuit diagram of the pulse sequencing block

the residual charge in C_P needs to be cleared in the middle phase of the voltage flipping process. The diagram for the pulse cell is also illustrated in the figure. The pulse signal is generated by ANDing the delayed and inverted versions of the input signal. For the very first pulse cell, the input signal is SYN and the input signals for the following cells are delayed versions of SYN. The delay in one pulse cell is performed by using two weak inverters charging a capacitor. The pulse width of the generated pulse for each cell can be tuned by adjusting the variable capacitor, which can be set externally. The three switches in one pulse cell are CMOS analog switches, which aims to enable and bypass the selected pulse cells. If any of $EN_1 - EN_8$ signals are low, the corresponding pulse cells for the disabled capacitors are bypassed so that the SYN signal has nearly no delay while bypassing these cells.

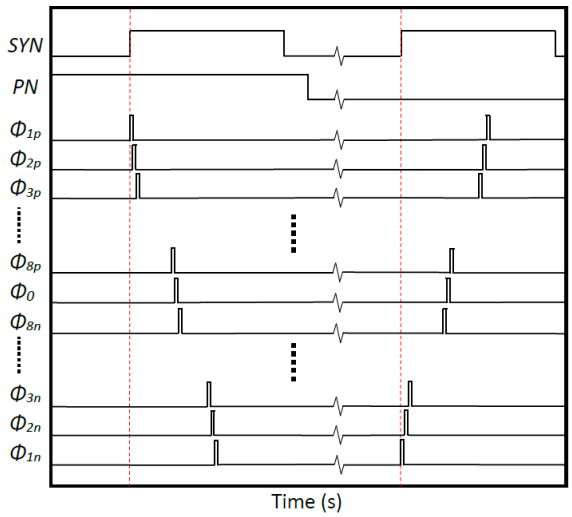


Fig. 7.8 Associated waveforms of the pulse sequencing block

7.4.4 Pulse sequencing

After the up to 17 sequential pulses are generated, they need to be sequenced before driving the switches to flip V_{PT}. Fig. 7.7 shows the pulse sequencing block, which consists of 8 multiplexers. While the input signal *PN* is high, V_{PT} needs to be flipped from positive to negative. In this case, the output sequence of the 17 pulses after the sequencing block should be $\phi_{1p} \rightarrow \phi_{2p} \rightarrow \phi_{3p} \rightarrow \phi_{4p} \rightarrow \phi_{5p} \rightarrow \phi_{6p} \rightarrow \phi_{7p} \rightarrow \phi_{8p} \rightarrow \phi_0 \rightarrow \phi_{8n} \rightarrow \phi_{7n} \rightarrow \phi_{6n} \rightarrow \phi_{5n} \rightarrow \phi_{4n} \rightarrow \phi_{3n} \rightarrow \phi_{2n} \rightarrow \phi_{1n}$. While *PN* is low, the pulse sequence is completely inversed. The pulse ϕ_0 is always in the middle of the sequence so it does not need sequencing. However, two redundant gates (AND and OR gates) are added for ϕ_0, which aims to ensure that all pulses have the same delay to avoid overlapping. Fig. 7.8 shows the associated waveforms of this block for different *PN* levels.

7.4.5 Switch control and voltage regulation blocks

Fig. 7.9 shows the circuit diagram of the switch control block, which consists of 17 two-stage level shifters and 33 analog CMOS switches. The 8 capacitors $C_1 - C_8$ are implemented off-chip as their capacitances are 45 nF, which are equal to the internal capacitance of the piezoelectric transducer C_P. The sequenced pulses obtained from the pulse sequencing block cannot be directly used for driving the 33 switches because different voltage levels are needed. For each switch, the voltage on either side varies over a wide range between $-V_D$ and $V_S + V_D$; however, the voltage levels of the pulses signals from the pulse sequencing block are 0 V and 1.5 V ($V_{DD} = 1.5$ V is used in this implementation). Therefore, the high

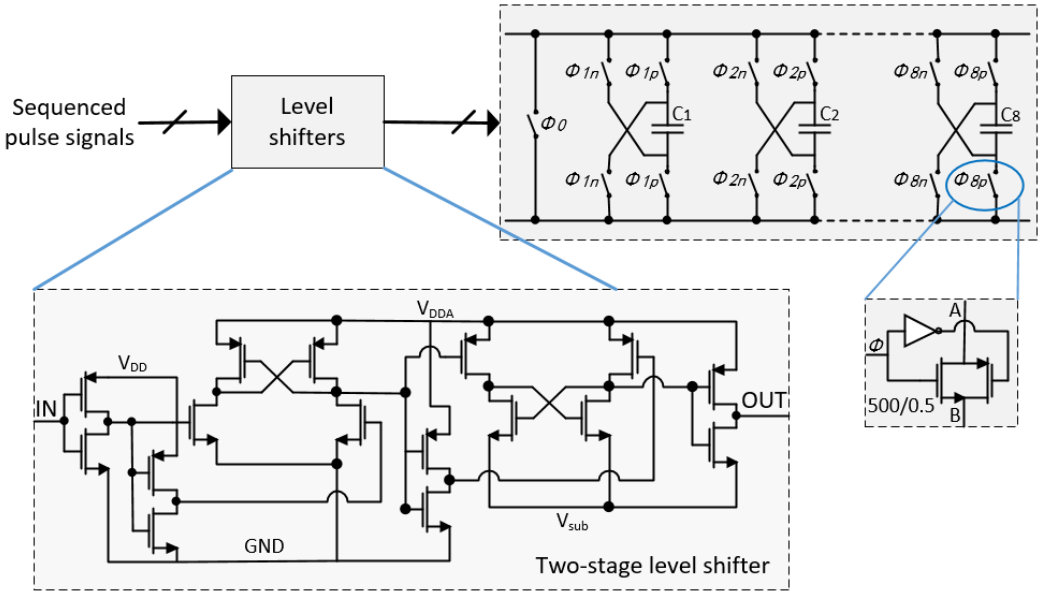


Fig. 7.9 Circuit diagram of the switch control block

and low levels of the switch driving signals should be shifted to a large voltage range in order to fully turn ON and OFF the 33 switches.

Fig. 7.10 shows the implementation of an over-voltage protection (OVP) and a voltage regulator. The OVP aims to limit the voltage stored in the capacitor C_S and the voltage regulator is employed to provide a stable 1.5 V supply to the interface circuit with the harvested energy. The resistors are off-chip implemented with values $R_1 = 100\,\mathrm{M\Omega}$, $R_2 = 10\,\mathrm{M\Omega}$, $R_3 = 50\,\mathrm{M\Omega}$, $R_1 = 100\,\mathrm{M\Omega}$.

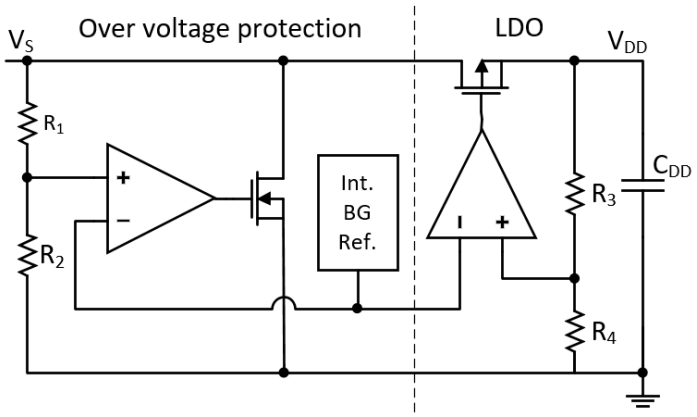


Fig. 7.10 Circuit diagram of the voltage regulator and over-voltage protection

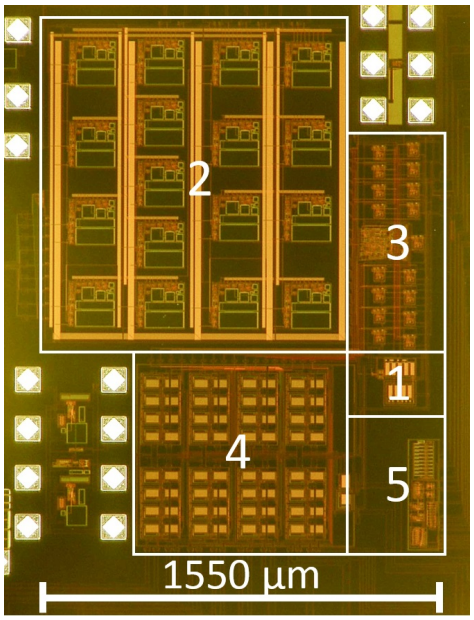


Fig. 7.11 Micrograph of the test chip fabricated in a 0.35 µm CMOS foundry process. The active area for the proposed circuit is 2.9 mm^2. (1. zero-crossing, 2. pulse generation, 3. pulse sequencing and level shifters, 4. switch control, 5. OVP and voltage regulator)

7.5 Measurement results

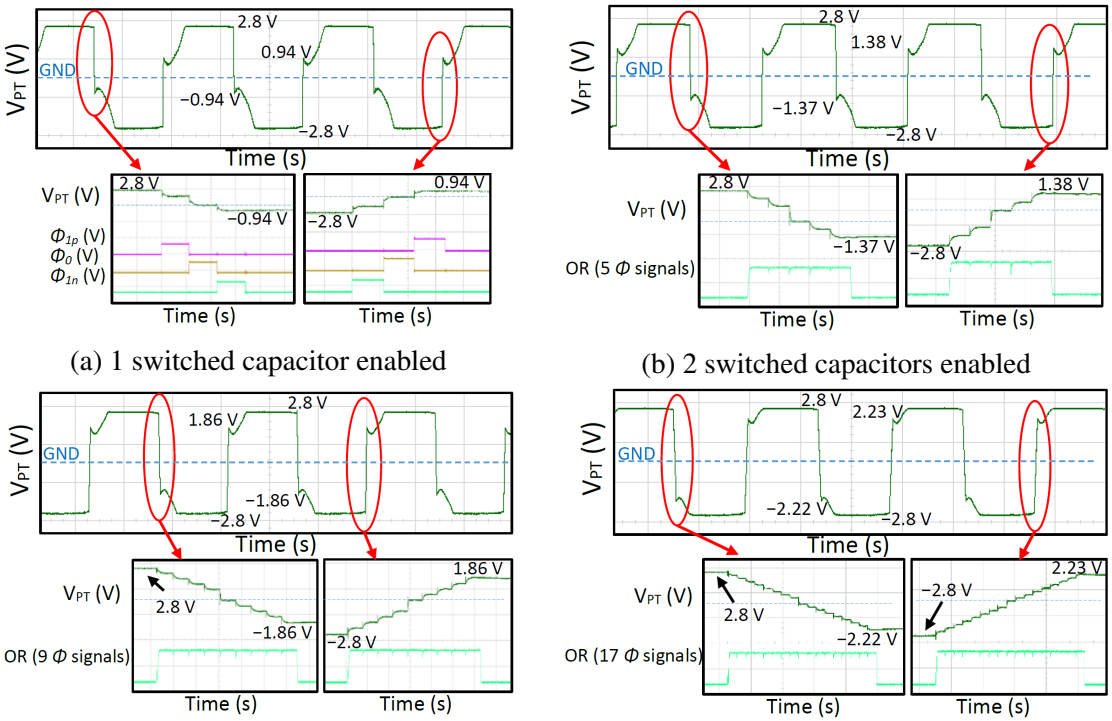
The proposed SSHC interface circuit was designed and fabricated in a 0.35 µm HV CMOS process. The system was experimentally evaluated using a commercially available piezoelectric transducer (PT) of dimension 58 mm × 16 mm (Mide Technology Corporation V21BL). This PT has an measured internal capacitance of $C_P = 45$ nF and the 8 off-chip switched capacitors are chosen with the equal capacitances of 45 nF to achieve the optimal voltage flip efficiency. During the measurement, a shaker (LDS V406 M4-CE) was excited at the natural frequency of the PT at 92 Hz and driven by a sine wave from a function generator (Agilent Technologies 33250A 80 MHz waveform generator) amplified by a power amplifier (LDS PA100E Power Amplifier). A super capacitor is employed as the energy storage capacitor (AVX BestCap BZ05CA103ZSB) with a measured capacitance $C_S \approx 5.2$ mF. As the circuit is self-sustained with an on-chip voltage regulator, the voltage supply from the voltage regulator is only available when voltage across the storage capacitor satisfies $V_S \geq 1.5$ V. While $V_S < 1.5$ V, the interface circuit simply works as a full-bridge rectifier (FBR) as all the 33 switches are OFF until V_S is charged to 1.5 V. Hence, an external power supply at 1.5 V was used while measuring the harvested power for $V_S < 1.5$ V. Fig. 7.11 shows the die photograph of the test chip.

Table 7.2 Breakdown of the chip power consumption.

Loss mechanism	Power loss	Percentage
Zero-crossing detection	189 nW	13.2%
Pulse generation	93 nW	6.5%
Pulse sequencing	0.3 nW	0.02%
Switch control	690 nW	48.3%
Voltage regulator	458 nW	32%
Total	1.43 μW	100%

Table 7.2 lists the power consumption due to different blocks of the proposed SSHC interface circuit. The values shown in the table are obtained from simulations with assumptions that 8 switched capacitors are employed (with 80% voltage flip efficiency) and the PT resonant frequency is 92 Hz. While employing fewer switched capacitors, the power loss due to the "pulse generation" and "switch control" blocks can be much lower. This is because less pulse signals will be generated and less switches in the switch control block will be driven in this case. The PT resonant frequency also affects the power consumption of these two blocks because a series of pulse signals are generated for every half period of the excitation frequency. Hence, higher frequency results in more pulse signals and more power consumed in generating pulses and driving switches.

Fig. 7.12 shows the measured waveforms and the four sub figures show the cases while the numbers of enabled switched capacitors are set to 1, 2, 4 and 8, respectively. From Fig. 7.12a, it can be seen that the voltage across the piezoelectric transducer V_{PT} is flipped from ± 2.8 V to ∓ 0.94 V. The voltage flip efficiency is around 1/3, which matches the calculated efficiency shown in table 7.1. The zoom-in voltage flipping instants for V_{PT} flipped from positive to negative and from negative to positive are also shown in the figure with the three switch signals ϕ_{1p}, ϕ_0 and ϕ_{1n}. There are only 3 switch signals needed for 1 switched capacitor because the switch signal number required for k switched capacitors is $2k+1$, as mentioned previously. In order to flip V_{PT} in two different directions, the sequence of the switched signals is reversed, as previously explained. While 2, 4 and 8 switched capacitors are enabled (Fig. 7.12b, Fig. 7.12c and Fig. 7.12d), V_{PT} is flipped with efficiencies of 1/2,



(a) 1 switched capacitor enabled

(b) 2 switched capacitors enabled

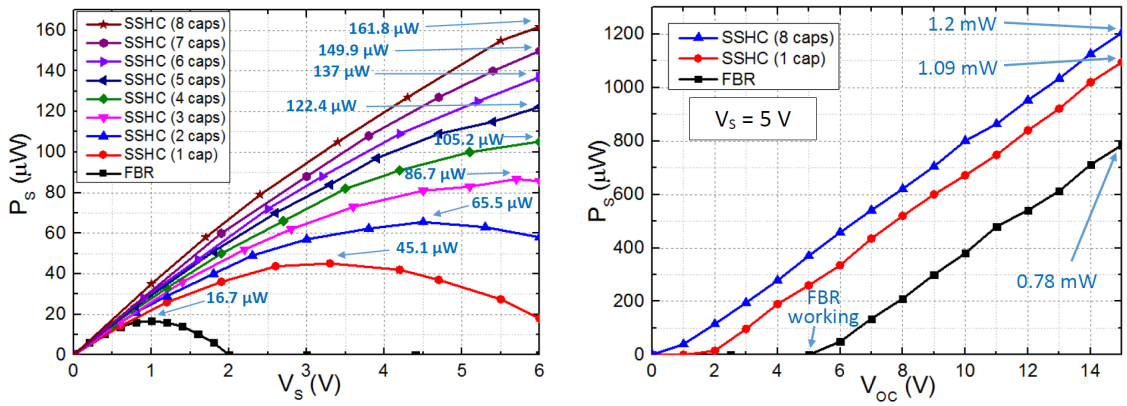
(c) 4 switched capacitors enabled

(d) 8 switched capacitors enabled

Fig. 7.12 Measured transient waveforms of V_{PT} and switch signals (some switch signals are ORed for display due to the limited number of oscilloscope channels)

2/3 and 4/5, respectively. These results closely match the calculations. As more switch signals are needed to drive more capacitors, these signals are ORed for display due to the limited number of oscilloscope channels. Although the sequence of the switched signals cannot be seen from the ORed version, their sequences for different voltage flip direction are completely inversed. As explained in section 7.3.2, the middle signal ϕ_0 aims to clear the residual charge in C_P after most of charge has been transferred into the switched capacitors. From the zoom-in voltage flip instants of the figures, it can be seen that V_{PT} goes to 0 V at the very middle pulse and it is flipped to an opposite polarization during the following pulses.

Fig. 7.13 shows the measured electrical output power of the PT with a conventional full-bridge rectifier (FBR) and with the proposed SSHC rectifier with up to 8 switched capacitors. The electrical output power is measured and calculated from a small voltage increase of V_S in a short period of time, where V_S is the voltage across the storage capacitor C_S connected to the output of a FBR (refer to Fig. 7.3a). The power at a specific V_S is calculated as $P = \frac{1}{2T} C_S((V_S + \Delta V_S)^2 - V_S^2)$, where ΔV_S is a small voltage increase in V_S and T is the time elapsed. In Fig. 7.13a, the voltage across the capacitor C_S is varied to measure the peak power points for each configurations of the interface circuits. During these measurement,



(a) (b)

Fig. 7.13 Measured electrical output power of a FBR and the proposed SSHC interface circuit with up to 8 switched capacitors. (a) Output power in a range of V_S with a fixed $V_{OC} = 2.5\,\text{V}$ (equivalent to an acceleration level 1.2 g). (b) Output power measured over a wide range of excitation levels (up to $V_{OC} = 15\,\text{V}$, equivalent to 7.5 g) with a fixed $V_S = 5\,\text{V}$

the PT is excited at an acceleration level of 1.2 g, which produces an open-circuit voltage amplitude of $V_{OC} = 2.5\,\text{V}$ across the PT. From the figure, it can be seen that the output power of an FBR is around 16.7 µW while the proposed SSHC with only 1 switched capacitor can output 45.1 µW power with 2.7× relative performance improvement with respect to the FBR. While two switched capacitors are employed, the output power increases to 65.5 µW with 3.9× overall improvement. In this implementation, the maximum supportable number of the switched capacitors is 8, which increases the output power to 161.8 µW. Hence, the output power with 8 switched capacitors improves the performance by 9.7*times* compared to an FBR. The trend of the power curve in the figure also implies that the output power for 8 switched capacitors can go higher for higher V_S values; however, the peak power point cannot be achieved in this implementation as the CMOS circuit is not designed to work at such high voltages. Fig. 7.13b shows the output power with a fixed voltage $V_S = 5\,\text{V}$ and the excitation level is varied from 0 g to 7.5 g (equivalent to V_{OC} varying from 0 V to 15 V). The proposed SSHC interface with 8 switched capacitors can provide output power up to 1.2 mW.

Table 7.3 shows the performance comparisons among state-of-the-art interface circuits for piezoelectric energy harvesters and the proposed SSHC interface with up to 8 switched capacitors. The second column from the left shows the employed techniques. The three following columns are the specifications of the piezoelectric transducers, including models of the PTs, internal capacitances and resonant frequencies. The column starting with "V_{OC}" shows the open-circuit voltage amplitudes of the PTs used for measurements and column "Inductor" shows the inductor values required for different interface circuits. The "normalized

Table 7.3 Performance comparison with state-of-the-art interface circuits

Work	Technique	PT	C_P	f_P	V_{OC}	Inductor	Normalized volume	$\frac{P_{IC}}{P_{FBR}}$	FOM
JSSC2010 [167]	Bias-flip	Mide V22B	18 nF	225 Hz	2.4	820 µH	4.6	4	0.87
JSSC2012 [195]	PSCE	Mide V22B	19.5 nF	173 Hz	9 V	10 mH	46.1	2.1	0.045
JSSC2014 [196]	Energy-investing	Mide V22B	15 nF	143 Hz	2.6 V	330 µH	2.4	3.6	1.5
JSSC2014 [25]	MS-SECE	Custom MEMS	8.5 nF	155 Hz	8.2 V	470 µH	3	2.5	0.83
TPEL2015 [175]	SSHI	Mide V22B	18 nF	225 Hz	3.28 V	940 µH	5.2	5.8	1.12
ISSCC2016 [200]	SSHI	MIDE V21B	26 nF	134 Hz	2.45 V	3.3 mH	15.9	4.4	0.28
This work	SSHC	Mide V21BL	45 nF	92 Hz	2.5 V	None	$1-1.6$	$2.7-9.7$	$2.7-6.1$

volume" is an estimated value for each start-of-the-art interface circuit, which includes the integrated circuit (IC) and all off-chip components except the PT. The IC chips for all the interface circuits are assumed to occupy $10\,\text{mm}^3$ with sufficient clearance to surrounding components. As a surface-mount device can be as small as $1\,\text{mm}^3$, each off-chip capacitor or resistor is assumed to occupy $2\,\text{mm}^3$ with $1\,\text{mm}^3$ of clearance. The unit volume for a highly compact inductor (including estimated clearance) is assumed to be $100\,\text{mm}^3/\text{mH}$. If multi-layer circuit boards are used, the clearance between components can be further decreased and wires can be placed on the inner layers of the board. Therefore, the total estimated volume for each interface circuit is the mathematical sum of the chip, off-chip capacitors, resistors and inductors with considerations of clearance. It can be seen that the proposed SSHC interface circuit occupies less volume than state-of-the-art circuits due to its inductor-less design. The normalized volume values for this work varies between 1 and 1.6 for different numbers of switched capacitors that are employed. The column $\frac{P_{IC}}{P_{FBR}}$ shows the output power performance improvement of the interface circuits compared to an FBR. The figure of merit (FOM) represents the performance improvement per unit volume, which is given by $FOM = \frac{P_{IC}}{P_{FBR}} \frac{1}{V_{NOR}}$, where V_{NOR} is the normalized volume. The FOM shows that although the SSHC interface with 8 switched capacitors takes more room with additional off-chip capacitors, the extra capacitors still have positive contributions to the FOM as a surface-mount capacitor is extremely small compared to other components in the system, such as inductors.

7.6 Conclusion

This chapter introduced an inductor-less interface circuit for piezoelectric vibration-based energy harvesters employing switched capacitors to synchronously flip the residual charge across the piezoelectric transducer (PT) to significantly improve key circuit metrics. Compared to reported state-of-the-art interface circuits, such as SSHI (synchronized switch harvesting on inductor), SECE (synchronous electrical charge extraction) and other approaches, the proposed interface circuit completely removes the requirement for an inductor to flip the voltage across the PT. With theoretical calculations, the voltage flip efficiency is 1/3 when only one switched capacitor is employed and this efficiency approaches 80% with 8 switched capacitors. In order to achieve these optimal theoretical voltage flip efficiencies, the capacitances of the switched capacitors should equal to the internal capacitance of the PT. For an SSHI interface circuit to achieve equal voltage flip efficiency, a large inductor is required, which is very impractical in miniaturized systems for real-world implementations. The measured results show that the proposed SSHC interface circuit improves the performance by 9.7$\times$ compared to a full-bridge rectifier. The performance boost is higher than reported inductor-based interface circuits with smaller system volume requirements due to the proposed capacitor-based design and hence a much higher energy efficiency per unit volume is obtained. Future work is currently addressing full on-chip integration of the circuit and switched capacitors for piezoelectric MEMS energy harvesters that could enable a new-class of fully integrated self-powered CMOS-MEMS sensor nodes.

Chapter 8

Conclusions and Future Work

8.1 Conclusion of the work

This thesis investigated the performance of PVEHs (piezoelectric vibration energy harvester) and associated interface circuits. In order to improve the performance of a PVEH while using a passive full-bridge rectifier, a novel connection configuration scheme was proposed in Chapter 5. The scheme split the electrode of a PVEH into several regions connected in series and the performance improvement is experimentally evaluated to be comparable with some active interface circuits [184, 185]. In Chapter 4, the output power of a PVEH was analyzed and it was found that the electrode layer coverage could potentially affect the raw electrical power. A new method was then proposed to determine the optimal electrode coverage for different structures of PVEHs. Two different MEMS harvesters were tested and the output power was found to be improved by around 120% for the optimal value of electrode coverage [188].

Besides the topologies proposed on piezoelectric harvesters, new active interface circuits have also been introduced and published to increase the power extraction efficiency. Chapter 5 presents a novel interface circuit, which fundamentally differs from reported circuits employing synchronous nonlinear rectification techniques. The proposed circuit dynamically evaluates the ambient vibration level and connect two PVEHs in parallel or in series to increase the output power and achieve its optimal power points [201]. Chapter 6 investigated the popular SSHI interface circuit and addressed a startup issue exists in conventional SSHI circuits. An improved SSHI rectifier with a startup circuitry was proposed to allow the circuit restart and sustain operation in an increased excitation conditions [198]. Although SSHI rectifiers show high power extraction efficiency, they require large inductors to achieve good efficiency. A novel SSHC interface circuit was proposed in Chapter 7, which completely

eliminates the requirement of inductors and achieves higher power efficiency than SSHI rectifiers.

8.2 Suggestions for future work

8.2.1 Fully integrated system

Although the proposed SSHC circuit removes the requirement of inductors, a few off-chip capacitors are still needed. Full integration can significantly decrease the system size into one single die without employing any off-chip components, excluding energy storage capacitors. In order to build a fully-integrated system with the proposed SSHC architecture, the key concern is to decrease the charge-swap capacitors, which need to be equal to the internal capacitor of the piezoelectric capacitor, noted as C_P, as shown in Fig. 8.1.

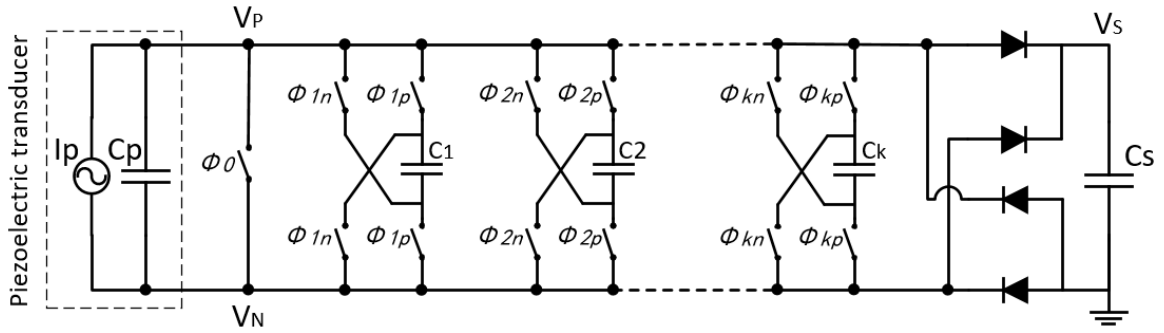


Fig. 8.1 SSHC interface with k synchronized switched capacitors

If the k charge-swap capacitors can be on-chip implemented, then the system can be fully integrated. In order to implement these capacitors on-chip, they need to be very small, ideally smaller than 200 pF. The easiest method is to decrease the C_P so that the required C_k capacitance is also decreased since $C_k = C_P$. Two common ways to decrease the internal capacitance, C_P, of a piezoelectric transducer (PT) is to decrease the electrode area and to increase the thickness of the piezoelectric layer. An inductorless interface circuit for ultrasonic energy transfer is proposed in [202] and the C_P of the PT used in this work is 80 pF. If the SSHC circuit is employed for the PT used in [202], the totally required capacitance for 8 charge-swap capacitance is 640 pF, which is smaller than the required capacitance 1.44 nF presented in [202]. From this point of view, the proposed SSHC circuit in this thesis requires less chip area to achieve comparable performance than the circuit proposed in [202] if the same PT is employed. Since eight 80 pF capacitors can be easily implemented on-chip, the system can be fully integrated if a PT with a small C_P is employed.

Another method is to decrease the required charge-swap capacitors to match a large C_P. In order to achieve this, the chapter 3 on split-electrode series configuration and the chapter 7 on the SSHC rectifier can be combined to build a new system. Assuming the electrode of a PT is split into n regions, the capacitance of each region is decreased to C_P/n. If all the n regions are connected in series, the resulting capacitance becomes C_P/n^2, which is significantly smaller than the original C_P for a monolithic electrode. As a result, the required charge-swap capacitors used in the proposed SSHC rectifier is n^2 times smaller than the internal capacitance of the PT. For a MEMS PT, the internal capacitance, C_P, is typically between 500 pF and 5 nF depending on the area of the device and the thickness of the piezoelectric layer. Splitting the electrode into n regions (n can be any integer larger than 1) makes the charge-swap capacitors small enough to be implemented on-chip.

8.2.2 System cold startup

While the energy harvesting system is initially implemented, all the energy storage capacitors in the system are out of charge and this state is called the cold state. This cold state can also be attained due to the quiescent power consumption or leakage after a long period of time without ambient vibration. In this state, there is no power supply for active circuits in the system; hence, neither SSHI nor SSHC rectifier (or SSH rectifier) will work. Hence, starting the system from the cold state is an outstanding question that should be addressed through further research.

During the cold state, the whole system simply works as a full-bridge rectifier (FBR) since there is no DC supply to power the active SSH rectifier. As discussed in the section 2.4, a FBR requires much higher open-circuit voltage to extract energy from the PT compared to active rectifiers since the voltage across the PT cannot be flipped. In this case, the system may never be started if the ambient vibration level is too low to generate high open-circuit voltage, noted as $V_{pp(open)}$. In order to address the startup issue and let the FBR extract energy until enough energy is stored in the system to start the SSH rectifier, one possible way is to increase $V_{pp(open)}$ when the system is in the cold state.

The split-electrode design presented in chapter 3 provides a method to increase $V_{pp(open)}$ without any active circuit. From the chapter 3, it has been studied that splitting the electrode of a PT into n equal regions connected in series can increase the open-circuit voltage generated by the PT by n times. Fig. 3.5a on page 31 also shows that the series connection decreases the required $V_{pp(open)}$ voltage to start extracting energy using a FBR. With the theory and experimental validations presented in chapter 3, the n regions of a PT can be connected in series before the system is started (or before a valid V_{DD} power supply is available to power the SSH rectifier). After the system is started and the SSH rectifier is operating to

synchronously flip the voltage across the PT, the connection configuration of the n electrode regions can be determined by the ambient excitation level and the preferred output voltage value of the rectifier. Because the excitation level determines the output voltage values, V_S, corresponding to the maximum power points (MPP) for different connection configurations, according to Fig. 3.5b. The preferred V_S value should also be considered to choose a connection configuration outputting highest power after the system is started.

Another possible way to increase $V_{pp(open)}$ is the electrode design topology presented in chapter 4. From Fig. 4.1b on page 38, it can be seen that the strain distributed in a vibrating cantilever is high near the clamped end. According to the strain distribution, the electrode layer on a PT can be split into two regions and this time, the segmentation is performed along a line orthogonal to the primary strain direction, such as the work presented in [181]. One region is close to the clamped end, noted as C_1, and the other region is close to the free end, noted as C_2. Due to the strain distribution, the open-circuit voltage generated in C_1 will be higher than two regions connected together (before electrode segmentation). When the system is in the cold state, the region C_2 can be disconnected from the system by default; so that only the C_1 is connected into the system and the high voltage generated in C_1 can easily overcome the threshold set by the FBR even under lower excitation levels. Although the region C_2 pulls down the open-circuit voltage if it is connected, there is still some amount of energy generated in this region. Hence, after the SSH circuit is powered, the region C_2 should be connected back into the system to maximize the performance of the energy harvesting system.

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Appendix A

Characteristics of piezoelectric transducers

A.1 Modeling of a resonant system

In this section, a mechanical resonant system is modelled upon a conventional second-order spring-mass resonant system with linear damping [203–205], as shown in figure A.1. This system is based on an inertial mass, m, a spring of stiffness, k and a damping coefficient, c. These components are placed in an inertial frame which is excited by an external vibration $y(t) = Y\sin(\omega t)$. This excitation results in a relative displacement, $x(t)$, between the mass and frame [206, 178]. Assuming that the mass of the inertial frame is significantly greater than the inertial mass, the vibration of the frame is not affected by the presence of the inertial mass. As the external excitation on the frame is harmonic, so the excitation on the inertial mass is also harmonic. Hence, the differential equation of motion of the inertial mass can be expressed as [207–217]:

$$m\ddot{x}(t) + c\dot{x}(t) + kx(t) = -m\ddot{y}(t) \tag{A.1}$$

Since the energy of this spring-mass system is stored in the relative displacement between the frame and the inertial mass, the general solution for the relative displacement of the inertial mass is given by:

$$x(t) = \frac{\omega^2}{\sqrt{(\frac{k}{m} - \omega^2)^2 + (\frac{c\omega}{m})^2}} Y\sin(\omega t - \phi) \tag{A.2}$$

where ϕ is the phase determined by:

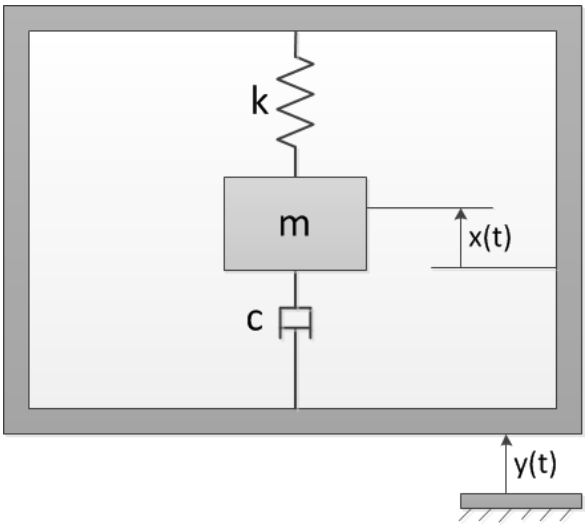

Fig. A.1 Equivalent spring-mass-damping system of an inertial resonator

$$\phi = \arctan\left(\frac{c\omega}{k - \omega^2 m}\right) \tag{A.3}$$

Taking the damping into account, the power dissipated due to the spring-mass-damping system is given by [104, 210–212] (which is also the maximum possible power extracted by the transduction mechanism)

$$P = \frac{m\zeta Y^2 \frac{\omega^6}{\omega_n^3}}{[1 - (\frac{\omega}{\omega_n})^2]^2 + [2\zeta \frac{\omega}{\omega_n}]^2} \tag{A.4}$$

where $\zeta = c/2m\omega_n$ is the damping ratio. Maximum power is attained while the inertial mass is excited at its natural frequency, where $\omega = \omega_n$. So the maximum power can be expressed as:

$$P_{max} = \frac{mY^2\omega_n^3}{4\zeta} \tag{A.5}$$

From the equation, a damping factor $\zeta = 0$ would generate infinite power at resonance, but it is impossible in practice. As the value ζ is greater than zero, the maximum power of the system is finite and it depends on the geometry of the generator [218, 219]. The relative displacement $x(t)$ can be increased by reducing the damping factor; however, the practical maximum displacement is limited by the size and geometry of the device [220–224]. So the damping factor should be designed to an appropriate value to prevent the inertial mass displacement $x(t)$ exceeds the limit. Equation A.6 also give the expression of maximum power in terms of the excitation acceleration magnitude of the excitation:

$$P_{max} = \frac{mA^2}{4\zeta\omega_n} \tag{A.6}$$

Where A is excitation acceleration magnitude and it is given by $A = \omega Y$, ζ is the damping ration ($\zeta = q/2m\omega_n$, Y is the amplitude of vibration and ω_n is the resonant frequency ($\omega_n = \sqrt{1-\zeta^2}\omega$, ω is the excitation frequency).

A.2 Piezoelectric materials

Piezoelectric generators are widely used amongst the three popular mechanical-to-electrical transduction mechanisms due to their relatively high power density, scalability and compatibility with conventional integrated circuit technologies [12, 87, 225, 58]. When the piezoelectric material is heated above a certain point known as Curie Point and a strong electric field is applied, the electric dipoles in the material are reoriented to a direction relative to the applied electric field.

Piezoelectric materials can be used as energy generators by applying mechanical deformation. Similarly, deformation occurs when an electric field is applied, what is known as the converse-piezoelectric effect. To be used as a VEH, the charge constant of the piezoelectric material is the most important factor impacting on the performance. There are two commonly used charge constants:

- d_{33}: induced polarization in direction 3 (parallel to direction in which ceramic element is polarized) per unit stress applied in direction 3
- d_{31}: induced polarization in direction 3 (parallel to direction in which ceramic element is polarized) per unit stress applied in direction 1 (perpendicular to direction in which ceramic element is polarized)

The subscripts represent the directions, which are shown in figure A.2. Direction 3 is the same as polarization. The first subscript gives the direction of induced polarization and the second subscript is the direction of applied stress. When the piezoelectric element is used for VEH, say the form of a cantilever (figure A.3), the constant d_{31} is normally used to generate a voltage in direction 3 while the strain is along direction 1.

The performance of a piezoelectric VEH is fundamentally determined by the piezoelectric material properties. The material properties of some commonly used piezoelectric materials are given in table A.1 [226]. The materials included in the table consists of AlN (Aluminum Nitride), ZnO (Zinc Oxide), Barium Titanate ($BaTiO_3$), soft PZT piezo-ceramics (PZT-5H),

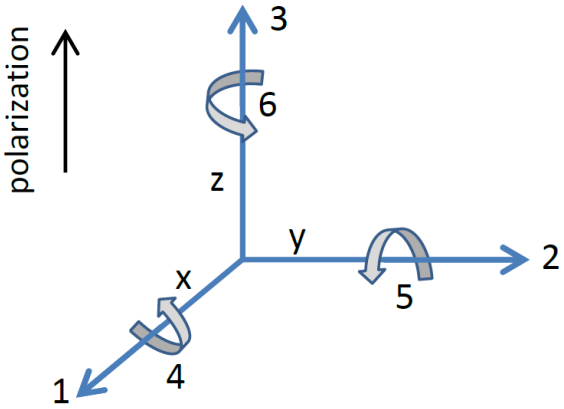

Fig. A.2 Directions of forces affecting a piezoelectric element

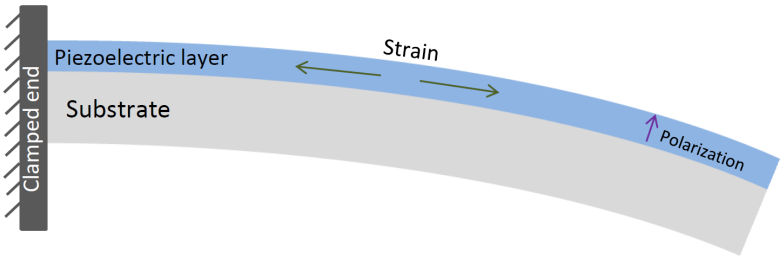

Fig. A.3 Strain in a vibrating unimorph piezoelectric cantilever

hard piezo-ceramics (PZT-5H), PMN-PT and Polyvinylidene fluoride (PVDF). The figures given are typical values and they may vary with age, stress, temperature and other conditions. The charge constants (d_{33} and d_{31}) of ferroelectric materials are found to have an order to magnitude larger than AlN and ZnO, which are non-ferroelectric materials. Besides, the relative permittivity values ε_{33}^{T} of ferroelectric materials are around two orders of magnitude larger than AlN and ZnO. These two properties are among the most important factors to be considered when choosing an appropriate material for piezoelectric VEH.

Table A.1 Material properties of most common piezoelectric materials

Material	AlN	ZnO	$BaTiO_3$	PZT-1 hard PZT	PZT-5H soft PZT	PMN-PT	PVDF
Const. strain rel. perm. (ε_{33}^T)	10	8.81	910	635	1470	680	5-13
Const. stress rel. perm. (ε_{33}^T)	11.9	11.0	1200	1300	3400	8200	7.6
d_{33} pCN^{-1}	5	12.4	149	289	593	2820	-13
d_{31} pCN^{-1}	2	-5	58	123	274	-1330	21
Mechanical quality (Q_m)	2490	1770	400	500	65	43-2025	3-10
Electro-mechanical coupling (k_{21})	0.23	0.18	0.49	0.7	0.75	0.94	0.19
s_{11}^E (pPa^{-1})	2.854	7.86	8.6	12.3	16.4	69	365
s_{13}^E (pPa^{-1})	2.824	6.94	9.1	15.5	20.8	119.6	472

Appendix B

MEMS piezoelectric device fabrication process

In order to improve the performance of energy harvesters, precise deposition and patterning of piezoelectric materials have become one of the key points for consideration. With current MEMS fabrication technology, many piezoelectric materials can be deployed in MEMS-scale energy harvesters [227–229], such as ZnO, AlN, $BiTO_3$, PZT ($PbZr_xTi_{1-x}O_3$) thin film or thick film, etc. The MEMS devices to be used for experiment in this research are fabricated by MEMScap, which employs AlN as the piezoelectric materials. So this section is focused on the deposition and patterning techniques of AlN.

Figure B.1 shows a fabrication process flow for a MEMS vibration energy harvester using AlN on SOI in a multi project wafer process provided by MEMSCAP. There are six key stages in the fabrication process:

- Silicon doping: As a first step, a phosphosilicate glass layer (PSG) is deposited on the wafer and the wafer is heated to 1050 °C for 1 hour in Argon. This process aims to drive the Phosphorous dopant into the Silicon layer of the wafer. At the end of this stage, the PSG layer is then removed using wet etching.

- Thermal oxide: A 2000 Angstrom thermal oxide is then grown on the surface of silicon layer. The first level mask (PADOXIDE) is used to lithographically pattern the wafer by exposing the photoresist. This oxide layer is wet-etched and it is followed by an acid resist strip.

- Piezoelectric film: The piezoelectric layer (aluminum nitride) is then deposited over the wafer by reactive puttering and employing the second level mask (PZFILM).

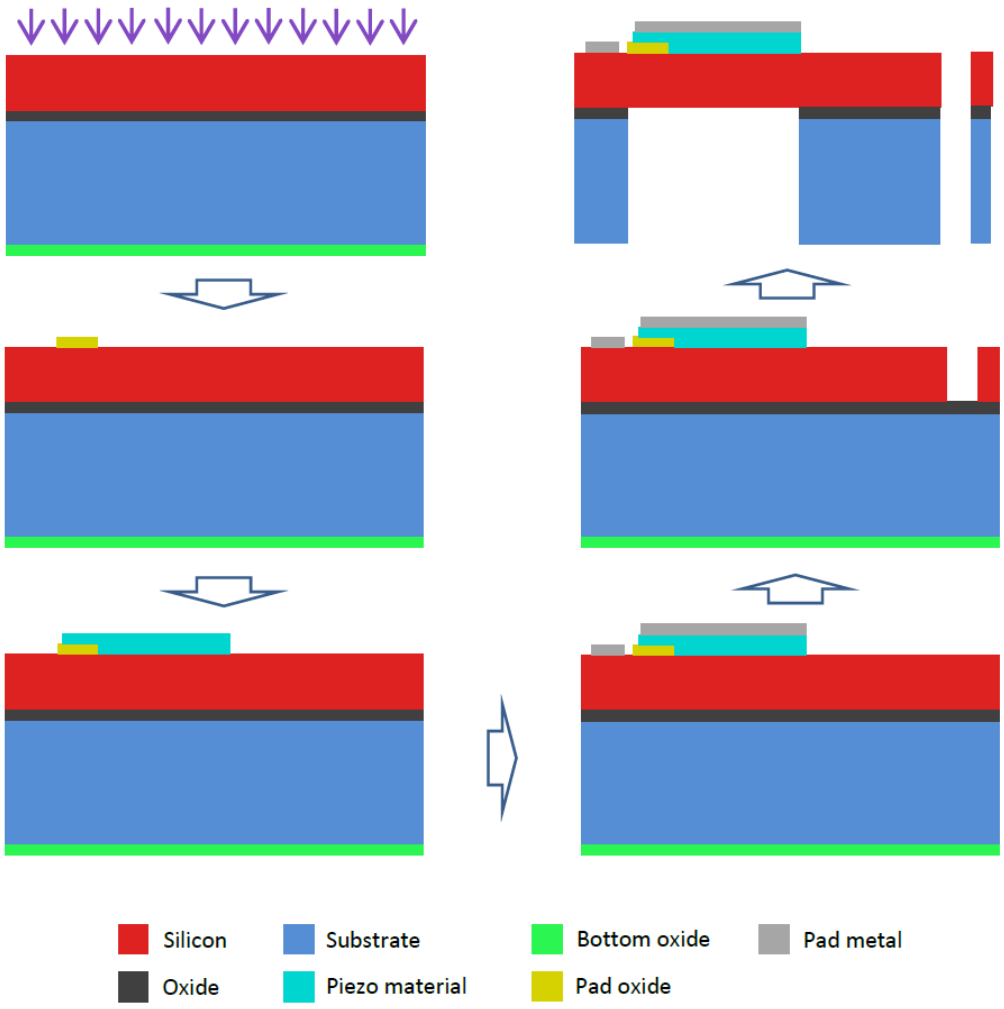

Fig. B.1 Micromachining process flow

- Pad metal: The third level mask (PADMETAL) is then employed to coat the wafer and a metal of aluminum is deposited over the photoresist pattern by beam evaporation.
- Silicon patterning: The wafer now coasted with UV-sensitive photoresist and fourth level mask (SOI) is lithographically patterned by exposing to UV light.
- Substrate patterning: Reactive ion etching (RIE) is to remove the bottom oxide. Then the bottom side of the wafer is coated with photoresist and lithographically patterned through the fifth level mask (TRENCH). The DRIE silicon etching is used to etch the substrate layer through the mask until the oxide layer.

Generally, a polyimide coating is added and removed on the top surface of the patterned silicon layer before and after trench etching in order to hold the wafer together securely

through the bottom side etching. Compared to macro-scale harvesters, the MEMS technology facilitates the design and fabrication of piezoelectric harvesters.

Appendix C

Real-world assessment of the self-startup SSHI interface circuit

C.1 Introduction

The interface circuit presented in Chapter 6 shows an improved SSHI rectifier with a self-startup circuitry, which is able to start the SSHI rectifier while it is not operating under weak excitation levels. This feature enables the proposed rectifier to operate in an increased excitation range, hence to increase the extracted electrical power. The experiments in Chapter 6 were only performed under a sine wave excitation, as well as most of published papers on active rectifiers for PVEH. However, the performance obtained under a sine wave excitation cannot represent the performance while the energy harvesting system is implemented in the real world. This is because the real-world vibration contains much white noise and band-limited noise and it is highly unpredictable. This chapter implements the circuit in a real-world environment for a first time to see how the circuit works in the real world. The measurements are performed with vibration data collected from a tram in Birmingham, UK and it lasts for 500 seconds. The tests were performed to see how the proposed SSHI circuit works better than a full-bridge rectifier and conventional SSHI circuits for real-world applications [230].

C.2 Measurement results

The proposed rectifier is designed and fabricated in 0.35 μm HV CMOS process and the die photo has been shown in Fig. 6.11. The proposed rectifier contains a conventional SSHI rectifier and a startup circuit. Hence experiments on both the conventional and the proposed

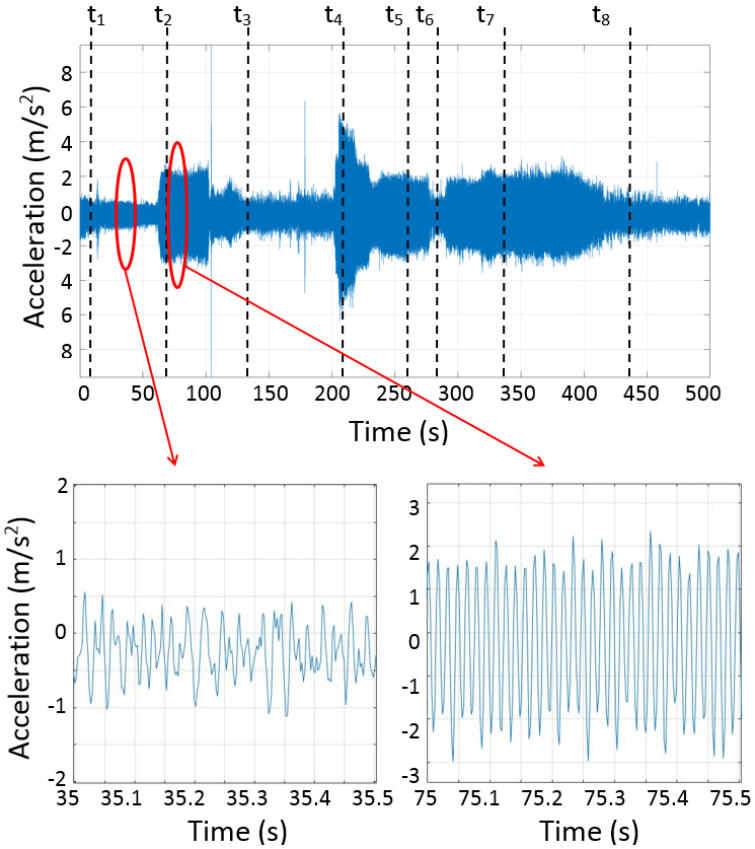

Fig. C.1 Time-domain acceleration plots of the measured real-world vibration data of length 500 s collected from a tram in Birmingham, UK.

SSHI can be performed with the chip by disabling and enabling the startup circuit to compare the performance. The power consumption of the chip is 0.8 μW while the SSHI rectifier is operating. After the SSHI rectifier stops operation, the consumption goes down to 0.65 μW as the voltage-flipping signal ϕ_{SSHI} is not generating in this case to drive the analog switches.

Fig. C.1 shows the vibration data collected from the body of a tram in Birmingham, United Kingdom. The data lasts for 500 seconds and it can be seen that it is very noisy and the vibration amplitude randomly varies with time. Eight time moments, t_1 to t_8, are labeled in the figure to facilitate explanations. The two zoomed-in figures shows short periods at 35 t and 75 t while the tram is stationary and moving, respectively. Fig. C.2 shows the STFT (Short-time Fourier Transform) plot of the vibration data. Comparing the two figure, it can be seen that the low amplitude periods (t_1, t_3, t_6 and t_8) shown in Fig. C.1 represents the time while the tram stops. These are either due to tram stations (t_1, t_3 and t_8) or traffic lights (t_6). It can be observed from the STFT plot that while the tram is moving, the vibration frequency is centered and peaked at around 65 Hz; however, while the tram stops, the vibration is very noisy and is no longer centered to any specific frequencies. This phenomena can also be

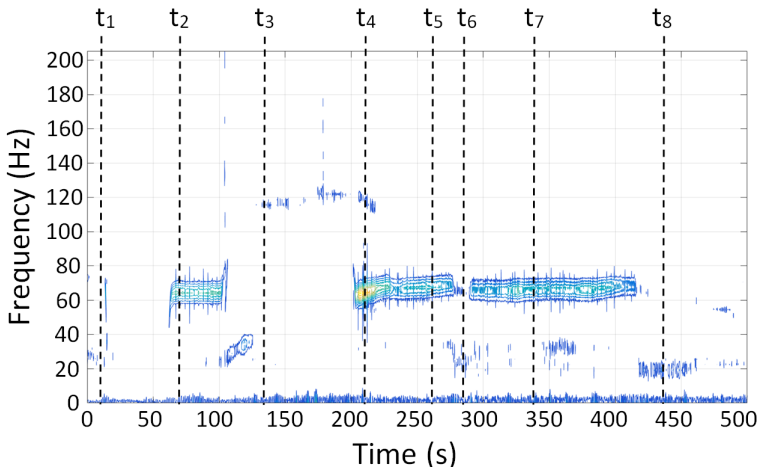

Fig. C.2 STFT (Short-time Fourier Transform) plot of the vibration data

observed from the two zoomed-in figures in Fig. C.1. While the tram is stationary (left sub-figure), the captured acceleration data is very noisy and while the tram is moving (right sub-figure), the data looks more like a sinusoidal signal of frequency around 65 Hz with a little noise. In terms of the vibration amplitude, it varies for different periods while the tram is moving. For example, the amplitudes at t_2, t_6 and t_7 are relatively low but the amplitude at t_4 is much higher. This can be due to rail track conditions and the speed of the tram.

The measurements were performed using a commercially available cantilevered piezoelectric harvester (Mide Technology V20W) with the nature frequency of 82 Hz. In order to use this piezoelectric transducer (PT) with the vibration data shown in Fig. C.2, the natural frequency of this PT was tuned to 65 Hz by adding a tiny tip mass. The 500-second vibration data was downloaded into a waveform generator (Agilent Technologies 33250A 80 MHz waveform generator) and the signal was amplified by a power amplifier (LDS PA100E Power Amplifier) to match the acceleration level with the real-world vibration. The modified piezoelectric harvester was then excited on a shaker (LDS V406 M4-CE) driven by the signal to test different interface circuits.

First, the vibration data is used to measure the performance of a passive full-bridge rectifier (FBR). As the threshold to extract energy for a FBR is very high as given in (6.1 at page 89), only the short period with high excitation level (around t_4 in Fig. C.1) attains the threshold. However, as most of energy is wasted due to flipping the voltage, the power efficiency is extremely low in this case. Measurements show that V_S is increased from 2.91 V to 2.96 V in this 500-second measurement. C_S is a super capacitor (AVX BestCap BZ05CA103ZSB) with measured capacitance $C_S = 5.2\,\text{mF}$, so the energy extracted in this 500 s is $\frac{1}{2}C_S(2.96^2 - 2.91^2) = 0.76\,\text{mJ}$ and the average power over the 500 s is 1.53 μW.

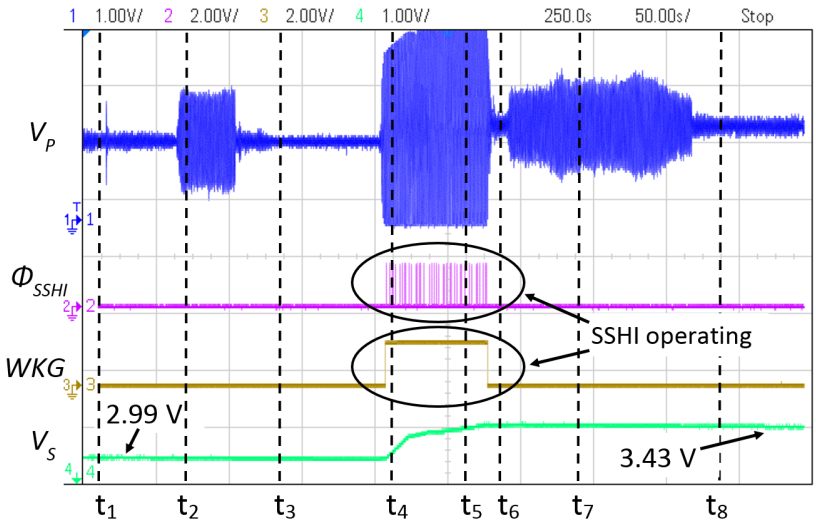

Fig. C.3 Waveforms of the conventional SSHI rectifier

The conventional SSHI rectifier without startup circuit is then tested. Fig. C.3 shows measured waveforms for 500 s. The signal V_P is the voltage at one electrode of the harvester. ϕ_{SSHI} is the inductor-control signal to flip the voltage across the harvester. WKG is the signal indicating if the SSHI rectifier is working and V_S is the voltage across the storage capacitor C_S connected at the output of the full-bridge rectifier. These signals are also labeled in Fig. 6.3 (page 91).

At t_1, the SSHI rectifier is not working as the tram stops; hence, ϕ_{SSHI} is not generated, WKG keeps at low and no energy is transferred into C_S. Although the tram starts moving at t_2, the condition for the conventional SSHI to start working is still not satisfied as the required excitation level is very high as shown in (6.1 at page 89). At t_4, the tram starts moving again and the excitation level at this moment is very high (refer to t_4 in Fig. C.1). The condition is satisfied and the conventional SSHI rectifier is started. Therefore, the voltage across the PT is correctly flipped by the signal ϕ_{SSHI} and WKG goes high. V_S is also increased as charge flows into C_S. From Fig. C.1, it can be seen that, after a short period of high excitation, the excitation level is decreased at t_5 although the tram still keeps moving. However, the conventional SSHI rectifier does not stop working because it is already started and the condition to sustain its operation is much lower as expressed in (6.2 at page 89). Then the tram stops due to the traffic lights at t_6 and the rectifier stops working. Once the SSHI rectifier stops working, the condition to restart it is now again difficult to be satisfied. Hence, the following moderate excitation level after the tram starts moving at t_7 cannot restart the conventional SSHI rectifier and the vibration energy during this period is wasted. During this 500 s measurement, the storage capacitor C_S is charged from 2.99 V to 3.43 V. Hence, the

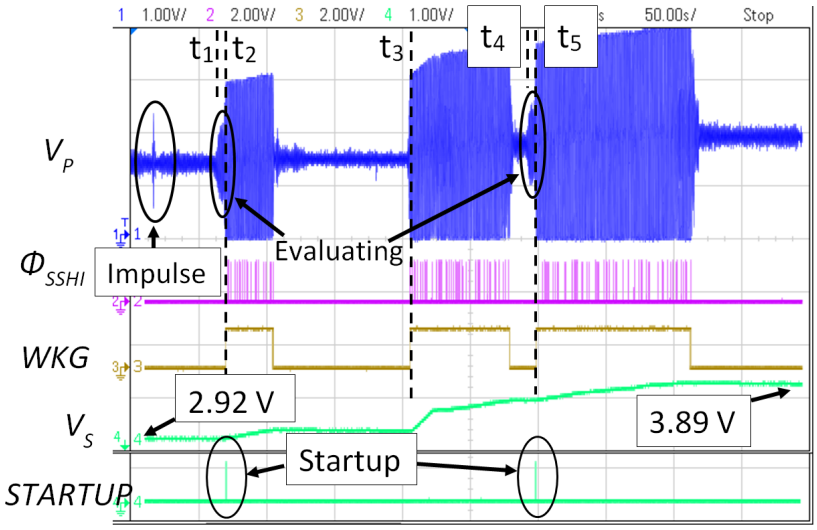

Fig. C.4 Waveforms of the proposed SSHI rectifier with startup circuit

energy extracted by the circuit is $\frac{1}{2}C_S(3.43^2 - 2.99^2) = 7.344\,\text{mJ}$ and the average electrical power over the 500 s is 14.68 μW.

The same vibration data is used again to test the proposed SSHI rectifier with startup circuit. Fig. C.4 shows the waveforms, where there are five signals. The signals are labeled in the system architecture in Fig. 6.3 (page 91) and the last signal $STARTUP$ is the signal sent to the startup block to restart the SSHI circuit. From the signal V_P, it can be seen that there is a short impulse at the beginning. As this impulse is too short, the evaluation block (Fig. 6.7 at page 97) does not approve a restart operation. The tram starts moving from t_1 and the evaluation block begins to evaluate the amplitude and duration of the excitation. After a short period of time at t_2, the excitation is evaluated as high and stable; hence a $STARTUP$ pulse is generated and the SSHI rectifier is restarted. During the remaining time while the tram is moving, WKG keeps high and ϕ_{SSHI} pulses are generated to flip the voltage until the tram stops. At t_3, the tram starts moving again. As the excitation level at this moment is very high so that the condition to restart is satisfied, the SSHI rectifier is directly self-started without using the startup circuit. The startup mechanism at this moment is the same as the conventional SSHI rectifier. Hence, neither the short evaluation period nor the $STARTUP$ pulse is present at this time. During the short stop of waiting for traffic lights, the SSHI rectifier stops working again. While the tram starts moving at t_4, the startup circuit starts evaluating the excitation and another $STARTUP$ pulse is generated at t_5 to restart the SSHI rectifier. During the 500 s measurement, V_S is increased from 2.92 V to 3.89 V, hence the extracted energy is calculated as 17.2 mJ and the average power is 34.4 μW.

C.3 Conclusion

This chapters implements an enhanced SSHI rectifier with startup circuits in a real-world vibration environment. The chip is designed in a 0.35 μm CMOS process. Instead of using a sine wave excitation signal, the chip is experimentally evaluated under the excitation of a 500-second real-world collected vibration data from a tram in Birmingham, UK. The real-world vibration data is much noisier than a sine wave signal and the excitation level is highly unpredictable. The measured results shows that the proposed SSHI rectifier is able to operate over an increased excitation range and extract more power compared to conventional SSHI rectifiers. Over the 500 s operational time period, the startup circuit helps the SSHI rectifier restart twice and the total extracted energy is 2.3$\times$ higher than the conventional SSHI circuit. Compared to a passive full-bridge rectifier, the conventional and the proposed SSHI rectifiers improve the performance by 9.6$\times$ and 22.5$\times$, respectively.

Appendix D

List of publications

Journal publications

- S. Du, Y. Jia, C. Do and A. A. Seshia, "An Efficient SSHI Interface With Increased Input Range for Piezoelectric Energy Harvesting Under Variable Conditions," *IEEE Journal of Solid-State Circuits*, vol. 51, pp. 2729-2742, 2016.
- S. Du, Y. Jia and A. A. Seshia, "Piezoelectric vibration energy harvesting: A connection configuration scheme to increase operational range and output power," *Journal of Intelligent Material Systems and Structures*, p. 1045389X16682846, 2016.
- S. Du, Y. Jia, C. Do and A. A. Seshia, "An Efficient Inductorless Dynamically Configured Interface Circuit for Piezoelectric Vibration Energy Harvesting," *IEEE Transactions on Power Electronics*, vol. 32, pp. 3595-3609, 2017.
- S. Du and A. A. Seshia, "An Inductor-less Bias-flip Rectifier for Piezoelectric Vibration Energy Harvester," *IEEE Journal of Solid-State Circuits*, vol. 52, 2017.
- S. Du, Y. Jia, S. Chen, C. Zhao, B. Sun, E. Arroyo and A. A. Seshia, "A New Electrode Design Method in Piezoelectric Vibration Energy Harvesters to Maximize Output Power," *Sensors and Actuators A: Physical*, vol. 263, pp. 693-701, 2017.
- S. Du, Y. Jia, C. Zhao, S.-T. Chen, and A. A. Seshia, "Real-world evaluation of a self-startup SSHI rectifier for piezoelectric vibration energy harvesting," *Sensors and Actuators A: Physical*, vol. 264, pp. 180-187, 2017.
- S. Du, Y. Jia, C. Zhao, G. A. J. Amaratunga and A. A. Seshia, "A Passive Design Scheme to Increase Rectified Power of Piezoelectric Energy Harvesters," *IEEE Transactions on Industrial Electronics*, Major revision submitted.

- S. Du, G. A. J. Amaratunga and A. A. Seshia, "A Cold-Startup SSHI Interface for Piezoelectric Energy Harvesters with Split Electrode Design," *IEEE Transactions on Power Electronics*, Under review.

Conference proceedings

- S. Du and A. A. Seshia, "8.9 A Fully Integrated Split-Electrode Synchronized-Switch-Harvesting-on-Capacitors (SE-SSHC) Rectifier for Piezoelectric Energy Harvesting with Between 358% and 821% Power-Extraction Enhancement," *2018 International Solid-State Circuits Conference (ISSCC)*, San Francisco, USA, February 11-15, 2018. (Accepted)

- S. Du, Y. Jia, E. Arroyo and A. A. Seshia, "Rectified Output Power Analysis of Piezoelectric Energy Harvester Arrays under Noisy Excitations," *Proceedings of the 17th International Conference on Micro- and Nanotechnology for Power Generation and Energy Conversion Applications (PowerMEMS 2017)*, Kanazawa, Japan, November 14-17, 2017.

- S. Du, S.-T. Chen, Y. Jia, E. Arroyo, and A. Seshia, "Connection Configurations to Increase Operational Range and Output Power of Piezoelectric MEMS Vibration Energy Harvesters," *Proceedings of the 16th International Conference on Micro- and Nanotechnology for Power Generation and Energy Conversion Applications (PowerMEMS 2016)*, Paris, France, December 6-9, 2016.

- S. Du, Y. Jia and A. A. Seshia, "Maximizing output power in a cantilever piezoelectric vibration energy harvester by electrode design," *Proceedings of the 15th International Conference on Micro- and Nanotechnology for Power Generation and Energy Conversion Applications (PowerMEMS 2015)*, Boston, USA, December 1-4, 2015.