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A Silicon Carbide Power Management Solution for High Temperature Applications

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A Silicon Carbide Power Management Solution for High Temperature Applications

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Abstract

The increasing demand for discrete power devices capable of operating in high temperature and high voltage applications has spurred on the research of semiconductor materials with the potential of breaking through the limitations of traditional silicon. Gallium nitride (GaN) and silicon carbide (SiC), both of which are wide bandgap materials, have garnered the attention of researchers and gradually gained market share. Although these wide bandgap power devices enable more ambitious commercial applications compared to their silicon-based counterparts, reaching their potential is contingent upon developing integrated circuits (ICs) capable of operating in similar environments.

The foundation of any electrical system is the ability to efficiently condition and supply power. The work presented in this thesis explores integrated SiC power management solutions in the form of linear regulators and switched capacitor converters. While switched-mode converters provide high efficiency, the requirement of an inductor hinders the development of a compact, integrated solution that can endure harsh operating environments.

Although the primary research motivation for wide bandgap ICs has been to provide control and protection circuitry for power devices, the circuitry designed in this work can be incorporated in stand-alone applications as well. Battery or generator powered data acquisition systems targeted towards monitoring industrial machinery is one potential usage scenario.

Acknowledgements

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I am also thankful for the former and current students of the MSCAD IC design group including Shamim Ahmed, Matt Barlow, Affan Abbasi, Sajib Roy, Aminta Castillo, Maria Benavides, Austin Gattis, Chase Rowlett, and Kyle Addington. The project related experience they shared with me has played an instrumental role in the design work presented.

The assistance from the late Dr. Michael Glover and Michael Steger during their time at the High Density Electronics Center (HiDEC) was invaluable when packaging circuits. The time they put in, even after normal working hours, to help our entire group made this work possible.

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Dedication

I would like to dedicate this work to the IC design group. They've always attempted to answer any design related questions that I had, even if it wasn't specifically related to their role in a project. My hope is that this work will serve to assist them throughout the process of finishing their degrees.

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CHAPTER 1 INTRODUCTION

1.1 Overview of Power Management Integrated Circuits

Developing power management solutions to efficiently condition and regulate a power supply voltage has presented a continuing challenge to designers and researchers. The ubiquity of battery powered, portable devices such as smartphones and tablets has been a driving force behind efforts to improve power management designs. Motivating factors for the continued emphasis on power management circuitry include the demand for improving efficiency, decreasing response time to load transients, and reducing system footprint (e.g. moving to a system-on-chip solution).

Without a well-regulated supply voltage, applications with transient loads can experience undesirable performance variations or even fail to operate. In the case of smartphones, a combination of analog and digital circuitry is reliant upon a battery to supply the energy. However, a battery will not provide a consistent voltage throughout its charge/discharge cycle. Even within a relatively small time sample of this cycle, the clock dependent load transients of digital circuitry can cause a noticeable voltage swing from the battery. This is due in part to the battery chemistry and the corresponding internal resistance, which produces a voltage drop during the load transients.

The regulation of the battery voltage is accomplished with DC-DC converters, which can include a combination of linear regulators and switched-mode converters. Switched-mode converters encompass several different topologies, with the most common being the traditional buck (step-down) and boost (step-up) converters. More complex topologies include the single-ended primary-inductor converter (SEPIC) which offers the functionality of both the buck and boost converters.

Linear regulators provide functionality similar to the buck converter by stepping down the supply voltage. The generic diagrams for a linear regulator and buck converter are illustrated in Fig. 1.1 and Fig. 1.2, respectively. One noticeable difference is the use of an inductor in the switched-mode converter. Although commonly used, an inductor is not required for all switching converter implementations. The inductor-less topologies are often referred to as "charge pumps" and while they generally do not have the same output current capabilities, a system-on-chip topology is made possible by eliminating the need for a discrete inductor.

An operational amplifier (op-amp) is used in both the linear regulator and switched-mode converter to compare the output voltage with a reference voltage. The difference between the reference and output voltages is amplified to give a control signal. The mixed-signal nature of the buck converter's feedback loop is one of the key differences between the switching converter and its linear regulator counterpart. The linear regulator functions by dynamically controlling the conductance of a series pass transistor with its feedback loop to obtain a desired output voltage.

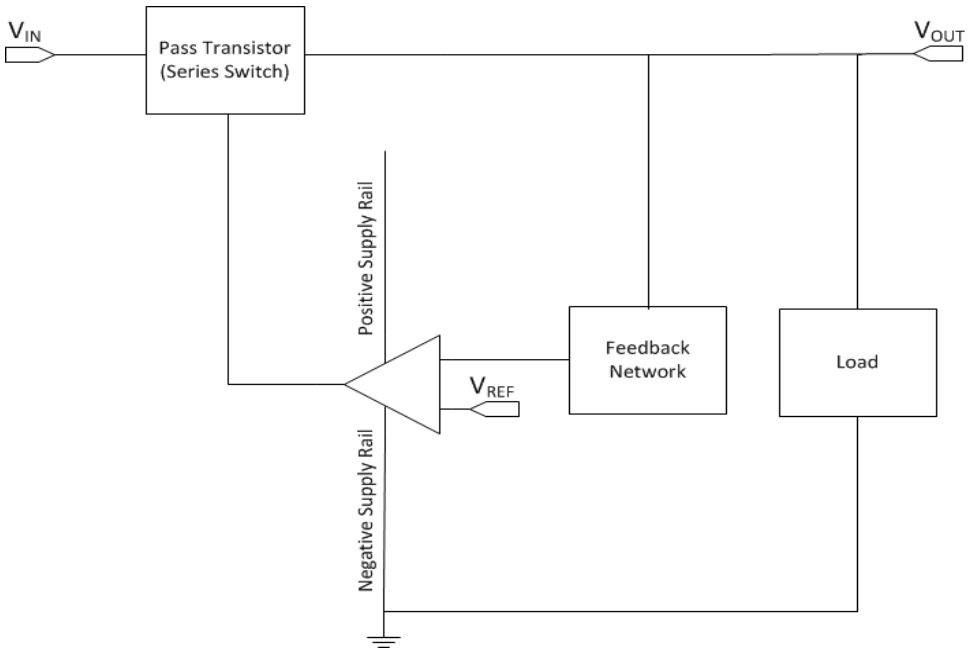

Fig. 1.1. A generic diagram of a linear regulator.

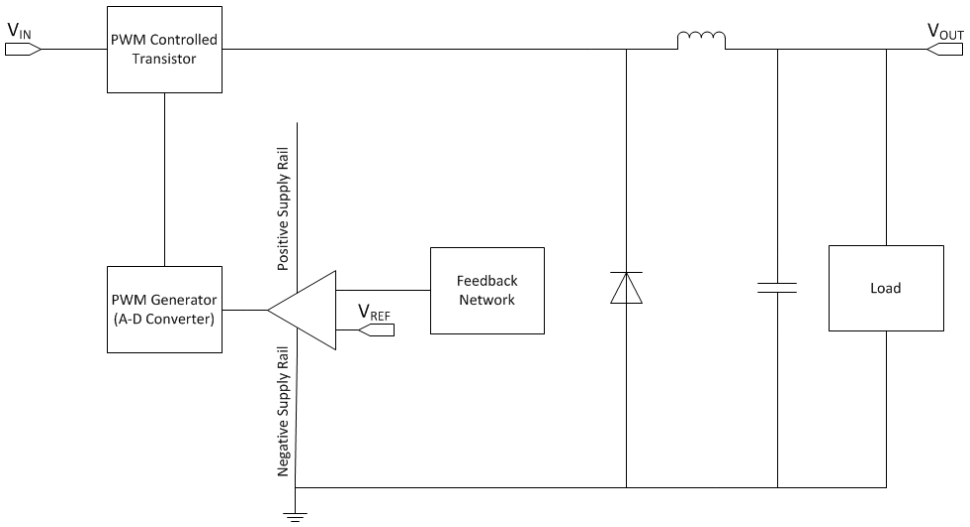

Fig. 1.2. A generic diagram of a buck converter.

On the other hand, the buck converter uses an op-amp in conjunction with a pulse-width-modulation (PWM) generator to control the switching transistor with a digital pulse-train.

Another major difference is that the buck converter can provide higher efficiency compared to the linear regulator. The linear regulator achieves a lower output voltage by dropping part of the input voltage across a pass transistor which results in wasted power proportional to the load current. A switched-mode converter stores energy in an ideally lossless inductor and capacitor during half of the switching cycle and discharges the stored energy during the other half of the cycle. Low-dropout linear regulators present a possible exception in regards to limited efficiency since the input voltage can be made close to the selected output voltage, reducing the voltage drop across the pass transistor and lowering the power loss.

Despite the potential for higher efficiency operation, there are multiple drawbacks to switched-mode operation that result in the linear regulator having inherent advantages. In addition to eliminating the need for a discrete inductor, linear regulators produce less noise and have lower response times. The reduction in noise is due to the linear regulator not having abrupt signals (i.e. a digital pulse-train) driving a power transistor which can inject noise into the output as is the case

for switch-mode converters. The slower response times of switched-mode converter topologies can be linked in part to the requirement of more components and the mixed-signal nature of the control scheme. Whereas the feedback network for a linear regulator topology consists primarily of an op-amp, switched-mode converters often require multiple mixed-signal blocks including a non-overlapping clock generator, pulse-width modulation generator, sawtooth waveform generator, and an op-amp.

The bandwidth of a switched-mode converter also limits its response times since it must be below the switching frequency. Although a higher switching frequency allows for higher bandwidth and smaller passive components, due to less energy storage requirements per cycle, the switching losses of the converter will increase. At higher switching frequencies, the high frequency noise component of the digital signals can also substantially impact the control circuitry and necessitate the use of filters. For these reasons, the switching frequency of switched-mode converters is typically between 20 kHz and 10 MHz. The feedback and compensation required to ensure stable operation further limit the regulator's bandwidth below the selected switching frequency.

1.2 Motivation for Silicon Carbide

Traditional silicon process technologies have been unable to keep pace with the continued demand for increasing power density and operating temperature capabilities of commercial applications. Due to the maturity of silicon, it has become imperative to identify new semiconductor materials to allow for continued improvement. Silicon carbide's properties as a wide bandgap semiconductor material have enabled the development of power devices capable of lower switching losses along with higher temperature and voltage capabilities [1]. Although SiC power devices are commercially available, exploring their potential remains a focus within the

research community. Packaging continues to be one such area of research. While a SiC power MOSFET is theoretically capable of sustained operation at high temperatures, the materials the power module is composed of must also be fully capable of enduring the extreme operating environment. Similarly, the ability to achieve higher switching frequencies is dependent on the parasitic wiring inductances within the power module. Research teams are continuing to examine the optimal solders, wire bonding techniques, epoxies, and a host of other packaging related concerns.

Another barrier to unlocking the full potential of SiC power devices is the control and protection circuitries around the devices. The present solution is to use silicon and silicon-on-insulator (SOI) integrated circuitry, but these solutions are limited to approximately 125 ºC and 250 ºC before reliability concerns begin to arise [2], [3]. In order to withstand the extreme operating environments, heat sinks or cooling systems must be used with silicon based ICs. Both solutions are costly and result in larger system footprints. Given that the IC must be thermally isolated from the heat source, it also prohibits a complete module, or system-in-package, design. This ultimately becomes a detriment to the application by increasing parasitic elements due to longer wires while reducing system reliability as well as power density [4] – [6].

The demand for developing IC technology with operating temperature capabilities similar to SiC power devices has been a driving force behind current research efforts in SiC ICs. However, it is not the only motivating factor. Research efforts are currently underway to design stand-alone sensing and data acquisition ICs capable of operation beyond 300 ºC. From a power management standpoint, literature has been published demonstrating the operation of linear regulators fabricated on SOI and all-NFET SiC processes at approximately 225 ºC and 300 ºC, respectively [7], [8]. Raytheon Systems Limited (RSL) has fabricated SiC CMOS ICs capable of operating at

temperatures exceeding 400 ºC, representing a viable path towards creating more complex mixed-signal circuitry [9] – [11]. This work aims to present the design of SiC CMOS power management circuitry in the form of linear regulators and a switched capacitor converter, each of which can become a crucial building block for future mixed-signal solutions for high temperature applications.

1.3 Thesis Structure

This thesis is organized into the following chapters.

- Chapter 1: Introduction – A brief overview is presented for power management integrated circuits along with the motivation for silicon carbide devices and ICs.
- Chapter 2: Silicon Carbide Integrated Circuits – The properties of silicon carbide are briefly analyzed and characteristics of the Raytheon HiTSiC® CMOS process are described. Publications detailing the successful fabrication and testing of SiC ICs are reviewed.
- Chapter 3: Overview of Circuits and Systems – A more detailed presentation of power management integrated circuitry, specifically linear regulators and switched capacitor converters, is given. Standard linear regulator topologies are described and the state-of-the-art switched capacitor converters are reviewed.
- Chapter 4: Design and Simulation – The design process of the SiC CMOS linear regulators and switched capacitor converter is presented. Multiple operational amplifier topologies are examined for the linear regulators. The building blocks of the switched capacitor converter ranging from the digital controller to the voltage-controlled oscillator are described. The schematic and simulation results are provided for each of the circuits.

- Chapter 5: Chip Fabrication and Test Results – The fabrication and test results of the Vulcan II linear regulator are presented. Vulcan II is the codename for the University of Arkansas's second fabrication with RSL, which is described in Chapter 2.
- Chapter 6: Conclusions and Future Work – The conclusions from designing the linear regulators and switched capacitor converter are given along with recommendations for future work in integrated SiC CMOS technology.

CHAPTER 2 SILICON CARBIDE INTEGRATED CIRCUITS

2.1 Properties of Silicon Carbide

Wide bandgap semiconductor devices including GaN and SiC have inherent advantages over silicon (Si) in power electronics applications. The wide bandgap materials provide higher breakdown electric fields and greater thermal conductivity [6]. The development of power semiconductor devices using these materials has led to superior breakdown voltages, operation at higher junction temperatures, and lower switching losses.

A comparison between wide bandgap semiconductors and silicon is given in Table 2.1 [6], [12]. SiC is reported to have over 150 different polytypes, but research and commercialization has primarily focused upon 4H-SiC and 6H-SiC [6]. The breakdown, or critical, electric field of SiC is nearly 10 times that of silicon, making it an attractive solution for high voltage applications.

Table 2.1. A comparison of silicon and wide bandgap semiconductor properties.

Material	Bandgap Energy E_g (eV)	Intrinsic Carrier Concentration n_i (cm^{-3})	Relative Dielectric Constant ε_s	Electron Mobility μ_n ($cm^2/V*s$)	Breakdown Electric Field E_B (MV/cm)	Thermal Conductivity λ (W/cm*K)
Si	1.1	1.5×10^{10}	11.8	1350	0.3	1.5
GaN	3.39	1.9×10^{-10}	9.0	900	3.3	1.3
4H-SiC	3.26	8.2×10^{-9}	9.76[a] 10.32[b]	1020[a] 1200[b]	2.2[a] 2.8[b]	4.5
6H-SiC	3.02	2.3×10^{-6}	9.66[a] 10.03[b]	450[a] 100[b]	1.7[a] 3.0[b]	4.5
Diamond	5.45	1.6×10^{-27}	5.5	1900	5.6	20

Note: [a] – Perpendicular to c-axis, [b] – Parallel to c-axis.

As stated in Table 2.1, the thermal conductivity of SiC is three times greater than that of silicon. It should be noted that the thermal conductivity is reported to vary substantially across temperature in [12]. Despite the temperature dependency, SiC remains superior to Si with respect to thermal conductivity and is able to achieve higher operating temperatures.

In an application with a given voltage rating, the advantages of SiC allow power devices to be fabricated at a fraction of the size of silicon devices. The result is not only a smaller footprint with increased power density, but also the potential for lower switching losses. The material characteristics and advantages have led to the adoption of discrete SiC devices within the power electronics market. Nevertheless, the potential of SiC cannot be fully realized without the ability to place mixed-signal circuitry in the same module or package as the power device.

2.2 Background on SiC ICs

Driven by the motivation of developing a single module consisting of an integrated gate driver alongside the power device, research into SiC ICs began in the 1990s. The first literature reports of SiC ICs demonstrate the successful fabrication of building block analog and digital circuitry in 6H-SiC processes [13] – [16]. A gate driver was successfully designed and fabricated in 5 µm 6H-SiC technology by 1999 [17], but manufacturing challenges ultimately led to the stagnation of research efforts in SiC IC technology while these fundamental concerns were addressed.

The manufacturing challenges pertaining to both SiC ICs and power devices are reported to be linked in part to trapped charges at the SiC/SiO_2 interface [18] – [20]. Literature suggests that charges become trapped in the oxide, leading to a reduction in mobility, threshold voltage instability, and ultimately performance degradation. Improvements to 4H-SiC manufacturing

techniques have lowered the change in mobility and threshold voltage by methods such as implanting nitrogen in the gate oxide prior to fabrication [21], [22].

Process improvements and production of discrete power devices as well as LEDs in 4H-SiC led to the development of Cree's 2 µm all-NFET 4H-SiC process. The successfully fabricated and tested circuits included a linear regulator and UVLO [8], [23]. General Electric has also reported operation of an all-NFET 4H-SiC technology at 500 ºC [24]. Building block circuitry such as differential amplifiers and inverters have also been reported in 4H-SiC BJT, JFET, and MESFET technologies [25] – [27]. However, the inability to fabricate a 4H-SiC CMOS process with minimal defects has prevented the design of more complex and power efficient circuitry.

2.3 Raytheon's HiTSiC® Process

The 1.2 µm CMOS HiTSiC® process developed in 4H-SiC by Raytheon Systems Limited has provided a path towards designing more complex ICs. An n-type substrate is used in the process as shown in Fig. 2.1 [28]. NFETs are formed in isolated P-wells while PFETs are fabricated in the substrate without isolated N-wells. Due to the PFETs being fabricated in the substrate, the body connection of each PFET must be tied to the substrate. The n-type substrate must be connected to the highest voltage seen by the chip as a result of the p-n junctions between

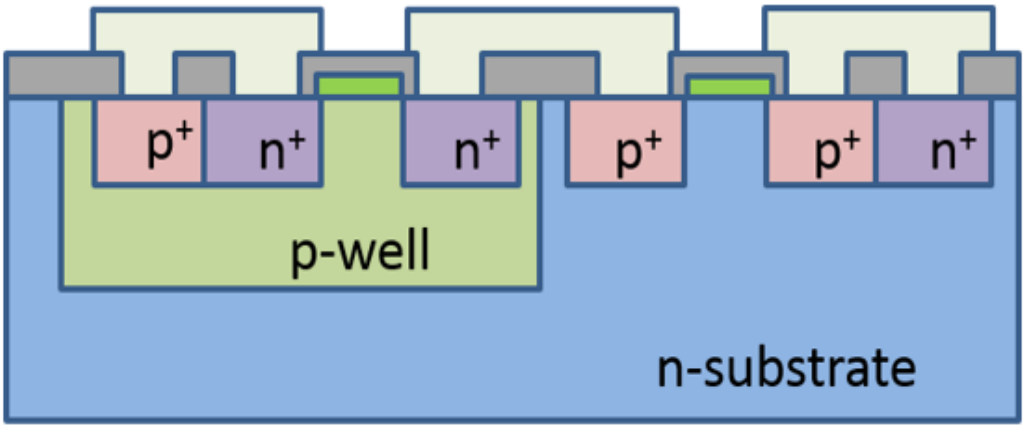

Fig. 2.1. The cross-section of Raytheon's HiTSiC® process.

the n-type substrate, p-wells, and p+ regions for PFET drains/sources. If the n-type substrate is connected to a voltage less than the source of a PFET, then there is a risk of the formation of a forward biased diode. Another consequence of fabricating PFETs in the common n-type substrate is that body effect must be taken into consideration when cascoding PFETs.

The process utilizes a 40 nm thick gate oxide and incorporates a single metal layer for routing [28]. Two poly layers are available, both of which can be used to form resistors. One of the poly layers has a relatively low sheet resistance that makes it a possible second layer for routing. On-chip diodes and capacitors are also available in the process.

The target temperature for the HiTSiC® process was 400 ºC. The initial circuits designed and fabricated by RSL were functional at 300 ºC and demonstrated the potential for higher operating temperatures as the process matured [28], [29]. In cooperation with Ozark IC, the University of Arkansas Mixed-Signal Computer (MSCAD) Laboratory developed a process design kit (PDK) for the HiTSiC® process [30], [31].

During the first fabrication run with RSL, code named Vulcan I, isothermal BSIM3 models were created for 25 ºC, 100 ºC, 200 ºC, and 275 ºC using process control monitor (PCM) test structures provided by RSL. The silicon based temperature scaling built into the models necessitated making separate models at each of the selected temperatures. For each temperature, binned models were added for FET lengths of 1.2 µm, 2 µm, and 5 µm. Model corners were also provided to simulate the behavior of commonly observed process variation, described as slow, typical, and fast with respect to "typical" devices. The culmination of the effort in Vulcan I resulted in the fabrication of voltage and current references, an operational amplifier, a phase-locked-loop (PLL), as well as synchronous and asynchronous digital logic [31] – [33].

The second fabrication run, Vulcan II, coordinated between RSL and the University of Arkansas led to the fabrication of the linear regulator presented in Chapters 4 and 5 [34]. In Vulcan II, isothermal BSIM4 models replaced the use of BSIM3 models. The inability of BSIM3 models to properly characterize trapped charges at the SiC/SiO_2 interface and SiC based parameters such as carrier concentration were motivating factors for the transition.

Similar to Vulcan I, the BSIM4 models were binned at 25 ºC, 100 ºC, 200 ºC, and 300 ºC. Model corners were added as before to predict the effects of potential process variation and aging on performance. Slow (S), typical (T), and fast (F) corners were developed for both NFETs and PFETs at each temperature. For example, the TF model corner predicts the device performance based on typical NFETs and fast PFETs. Beyond the world's first integrated SiC CMOS linear regulator presented in this work, the circuits fabricated on Vulcan II included a comparator, a gate driver, an RS-485 transceiver, and digital circuitry [11], [35], [36].

The work presented in this thesis is designed for Raytheon's HiTSiC process using the BSIM4 models that have been developed. Additional SiC IC foundries exist and the work presented here will be applicable to those processes as well if the models and designs, specifically FET and passive sizes, are adjusted to account for different process related parameters.

CHAPTER 3 OVERVIEW OF CIRCUITS AND SYSTEMS

This chapter presents an overview of the circuits designed to form a power management solution in 4H-SiC. The top-level designs that will be detailed are linear regulators and a switched capacitor (SC) converter. The discussion will also extend to the lower-level circuitry required, such as operational amplifiers for linear regulators and digital control logic for switched capacitor converters.

3.1 Linear Regulators

The demands for eliminating the noisy output of switching converters and delivering a stable output under a variety of loading conditions while achieving a smaller footprint, particularly in system-on-chip applications, are factors behind the continued popularity of linear regulators. Linear regulators are commonly designed in a low-dropout (LDO) configuration with a PFET pass transistor to achieve greater efficiencies due to the supply voltage being closer to the selected output voltage. The dropout voltage indicates the supply voltage at which the linear regulator is no longer able to provide the output voltage target due to the minimum FET on-resistance.

The potential for improved efficiency with the LDO makes it popular in low power designs targeted towards portable, battery-powered applications. In cases where energy efficiency is less critical, high-bandwidth linear regulators with relatively high dropout voltages are alternative solutions. In either configuration, however, the efficiency is limited by the power dissipation across the pass transistor plus the regulator's quiescent current as expressed by (3.1).

$$\boldsymbol{Efficiency} = \frac{\boldsymbol{P_{out}}}{\boldsymbol{P_{in}}} = \frac{\boldsymbol{P_{OUT}}}{(\boldsymbol{V_{SUPPLY}})(\boldsymbol{I_Q} + \boldsymbol{i_{LOAD}})} \tag{3.1}$$

The power dissipation across the pass transistor is inherent to the linear regulator operation. The step-down voltage conversion is a result of the voltage drop across the pass transistor, which has a feedback loop dynamically controlling its channel resistance. The quiescent current, I_Q, is primarily due to the op-amp used within the feedback loop. To illustrate this more clearly, the basic schematic of an LDO is shown in Fig. 3.1. This topology has quiescent current flowing through the feedback network consisting of the feedback resistors R_{F1} and R_{F2} along with the op-amp, which is commonly referred to as the error amplifier.

The feedback resistors sample the output voltage in a resistor divider and connect the sampled voltage to the error amplifier terminal. In the topology given in Fig. 3.1, the feedback voltage is connected to the non-inverting input terminal of the error amplifier while the inverting terminal is connected to the reference voltage. When the output voltage increases above a calculated threshold, the resistor divider will provide a voltage greater than the reference voltage

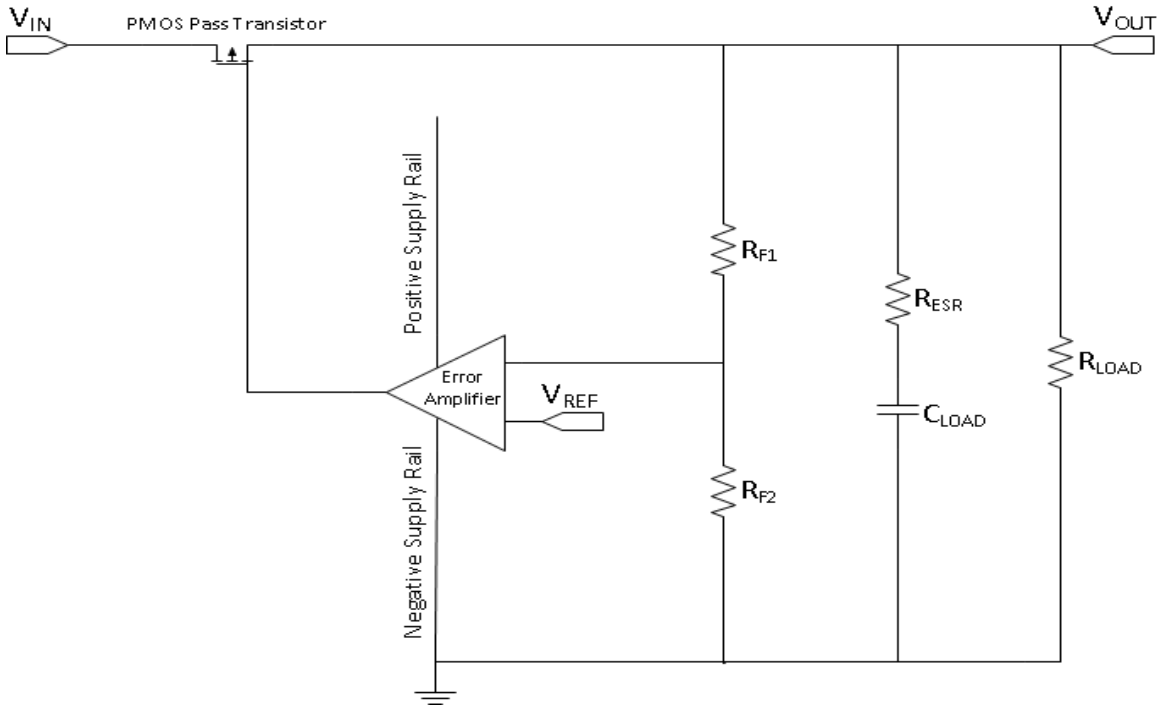

Fig. 3.1 An LDO schematic based on a PFET pass transistor.

to the non-inverting terminal of the error amplifier. This will cause the op-amp to provide an output voltage greater than zero, up to the positive supply rail, to the PFET pass transistor. As the V_{SG} of the pass transistor decreases, it will begin to shutoff and the output will fall back to the desired value.

Typically, R_{F1} and R_{F2} will be relatively large resistance values and will not significantly increase the quiescent current. This leaves the op-amp as the main source of quiescent current. The bandwidth of the linear regulator is heavily dependent on the op-amp's bandwidth, which increases with higher bias currents. This creates a tradeoff between the frequency response capabilities of the linear regulator and its quiescent current as well as maximum efficiency.

Due to the linear regulator's feedback loop, it is essential that the system remains stable. An open-loop phase shift of less than 180º at the frequency the linear regulator's gain crosses the 0 dB, or unity gain, point is needed for stability. Note that proper error amplifier operation also depends on the same stability criterion. Intuitively, the requirement of less than 180º of phase shift can be understood by the need to keep the system operating with negative feedback.

For example, the feedback loop will act to turn the PFET pass transistor off when the output voltage increases. If the closed-loop system has more than 180º phase shift, then an AC disturbance at the non-inverting input of the error amplifier will produce positive feedback and ultimately cause the system to oscillate. The error amplifier's output will be high during the negative half of the AC disturbance and will cause the output of the regulator to go low, which is considered positive feedback. Similarly, during the positive half of the AC disturbance the error amplifier's output will go low and increase the linear regulator's output voltage. The system is operating with positive feedback in both halves of the AC disturbance waveform, which causes the system to

continuously oscillate. When the system has negative gain, meaning it has transitioned below the 0 dB point, a phase shift of more than 180º is permissible since negative gain will negate the positive feedback.

There are two poles and one zero in the system shown in Fig. 3.1 that dictate the stability of the regulator. As will be discussed in the following sections, it is also possible to have relatively high frequency poles due to the op-amp topology selected and if a bypass capacitor is utilized. Regardless of additional poles, the potential of an unstable system exists with two poles and one zero. This is because each pole will provide a -20 dB/decade gain roll off and a phase shift of approximately -90º over two decades (starting one decade before and ending one decade after the pole location). Although not always the case, a zero is generally complementary to a pole in that it provides +20 dB/decade of gain and a phase shift of +90º over two decades. The system is therefore conditionally stable depending on the pole and zero locations since the total contribution of two poles is -180º of phase shift. To ensure stability, the zero location must be near to or lower than the second pole.

The first pole is formed by the output resistance of the PFET pass transistor along with the load capacitance and its associated equivalent series resistance (ESR). The expression for the first pole is given by (3.2) and it is typically the dominant pole in the system, although internally compensated regulators provide an exception.

$$\boldsymbol{f_{p1} = f_{3dB} = \frac{1}{2\pi(R_{o,pass} + R_{ESR})(C_{LOAD})}} \tag{3.2}$$

The location of the second pole in the system is a function of the error amplifier's output resistance and the inherent capacitances of the pass transistor as expressed by (3.3).

$$f_{p2} = \frac{1}{2\pi(R_{o,EA})(C_{PassFET})} \tag{3.3}$$

Linear regulators commonly use a bypass capacitor that is generally an order of magnitude or lower than the load capacitance and has low ESR. It is placed between the output of the linear regulator and ground. The pole it forms is typically located beyond f_{p1} and f_{p2} due to C_{LOAD} being greater than C_{Bypass} and $R_{o,EA}$ being much larger than R_{ESR}. The expression for the third pole associated with the bypass capacitor is given by (3.4).

$$f_{p3} = \frac{1}{2\pi(R_{ESR})(C_{Bypass})} \tag{3.4}$$

The zero is a result of the load capacitor's ESR. Although it is detrimental to the regulator's efficiency due to the power dissipation when the load capacitor is charging/discharging, it is beneficial for stability. If a bypass capacitor is used, then the zero will need to be either near the second pole or at a lower frequency. The location of the zero is determined by (3.5).

$$f_{z1} = \frac{1}{2\pi(R_{ESR})(C_{LOAD})} \tag{3.5}$$

Due to f_{p1} being dependent upon the output resistance of the pass transistor, there is a corresponding dependence of the pole's location on the amount of current passing through the PFET pass device. While in the saturation region, a MOSFET will have an output resistance given by (3.6).

$$r_o = \frac{1}{\lambda I_D} \tag{3.6}$$

The output resistance is therefore dependent upon the channel-length modulation parameter (λ) and the current through the pass transistor. Equations (3.2) and (3.6) indicate the first pole location will be at higher frequencies when the load current is at its maximum value and at relatively low frequencies when the regulator is in the no-load condition. The value of R_{ESR} for typical ceramic capacitors is only a few milliOhms, which allows the f_{p1} location to extend out to

high frequencies that may be the same order of magnitude as f_{p2} or f_{p3} (if C_{Bypass} is used). It follows that the worst-case stability condition is for high load currents where f_{p1} begins to cluster around the other poles, because the gain will not start to roll off until high frequencies. The 0 dB point will extend out to higher frequencies, increasing the bandwidth of the regulator but decreasing its phase margin (i.e. the phase at the unity gain frequency) to the point of possible instability. For this reason, some applications may require the use of a discrete R_{ESR} resistor to minimize the movement of f_{p1}.

The open-loop gain of the system is the product of the gain provided by the pass transistor, the error amplifier, and the sampling network formed by R_{F1} and R_{F2}. The expression for the open-loop gain is given by (3.7), where the gain of the sampling network is given as (3.8).

$$\boldsymbol{A_{OL} = A_{PassFET} * A_{EA} * A_{Sampling}} \tag{3.7}$$

$$\boldsymbol{A_{Sampling} = \frac{V_{REF}}{V_{OUT}}} \tag{3.8}$$

Three of the fundamental linear regulator parameters that depend upon the open-loop gain are line regulation, load regulation, and power-supply rejection ratio (PSRR). Line regulation is defined as the change in output voltage for a given change in input voltage and is expressed in (3.9). This demonstrates the ability of the regulator to provide a constant output from a supply that may vary relatively slowly over time (not an AC disturbance).

$$\boldsymbol{Line\ Regulation = \frac{\Delta V_{OUT}}{\Delta V_{IN}}} \tag{3.9}$$

Deriving the line regulation begins by solving for the change in output voltage as in (3.10).

$$\boldsymbol{\Delta V_{OUT} = (\Delta V_{IN})\left(\frac{R_{LOAD}}{R_{ds,pass} + R_{LOAD}}\right) - (\Delta I_{LOAD})(R_{LOAD})} \tag{3.10}$$

The expression for the change in load current is given in (3.11).

$$\Delta I_{LOAD} = (A_{PassFET})(A_{EA})(\Delta V_{OUT})(\frac{R_{F2}}{R_{F1}+R_{F2}})(\frac{1}{R_{o,pass}}) \quad (3.11)$$

Substituting (3.11) into (3.10) results in (3.12). The expression in (3.12) can be rearranged into (3.13), then the line regulation can be approximated as in (3.14).

$$\Delta V_{OUT} = \frac{(\Delta V_{IN})(R_{LOAD})}{R_{ds,pass}+R_{LOAD}} - (A_{PassFET})(A_{EA})(\Delta V_{OUT})(\frac{R_{F2}}{R_{F1}+R_{F2}})(\frac{1}{R_{o,pass}})(R_{LOAD}) \quad (3.12)$$

$$\Delta V_{OUT}\left[1 + (A_{PassFET})(A_{EA})(\frac{R_{F2}}{R_{F1}+R_{F2}})(\frac{1}{R_{o,pass}})(R_{LOAD})\right] = \frac{(\Delta V_{IN})(R_{LOAD})}{R_{ds,pass}+R_{LOAD}} \quad (3.13)$$

$$\textbf{Line Regulation} \approx \frac{\Delta V_{OUT}}{\Delta V_{IN}} = \frac{1}{R_{ds,pass}+R_{LOAD}} * \frac{R_{o,pass}}{(A_{PassFET})(A_{EA})(\frac{R_{F2}}{R_{F1}+R_{F2}})} \quad (3.14)$$

Improving the line regulation performance is dependent upon increasing the system's open-loop gain. It should be noted that the line regulation derivation neglects the voltage reference's drift over temperature. The voltage reference also commonly uses the unregulated input as its supply voltage and will vary slightly with a change in supply.

The regulator's load regulation is defined as the change in output voltage for a given change in output current and is expressed by (3.15).

$$\textbf{Load Regulation} = \frac{\Delta V_{OUT}}{\Delta I_{LOAD}} \quad (3.15)$$

The change in output current is determined by the system's open-loop gain and is given by (3.11). The change in output voltage given by (3.16) assumes that the feedback resistor values in the sampling network are much larger than the load resistance and that the input voltage is constant. The combination of the two expressions yields (3.17) as the load regulation.

$$\Delta V_{OUT} = (\Delta I_{LOAD})(R_{LOAD}) \quad (3.16)$$

$$\textbf{Load Regulation} = \frac{\Delta V_{OUT}}{\Delta I_{LOAD}} = \frac{R_{o,pass}}{(A_{PassFET})(A_{EA})(\frac{R_{F2}}{R_{F1}+R_{F2}})} \quad (3.17)$$

Equation (3.17) shows improved load regulation performance with a larger open-loop gain.

Whereas the line and load regulation are steady-state performance metrics, PSRR indicates the regulator's ability to reject supply noise (e.g. 60 Hz noise). The expression for PSRR is given in (3.18), where A_{OL} is the open-loop gain given in (3.7) for low frequencies.

$$\boldsymbol{PSRR} = \frac{\boldsymbol{\Delta V_{supply}}}{\boldsymbol{\Delta V_{out}}} * \boldsymbol{A_{OL}(s)} \tag{3.18}$$

PSRR is dependent upon the supply noise frequency and the regulator's gain over frequency. Commercially available linear regulators with datasheets reporting PSRR performance typically list PSRR values for multiple frequencies for a given test condition. Most linear regulators have poorer PSRR at high frequencies, beyond their bandwidths, compared to low frequencies which is a result of the characteristic gain roll off.

3.1.1 Operational Amplifiers

The op-amp forms the core of the linear regulator's feedback loop and serves as a building block for a wide range of mixed signal applications. Parameters such as gain and bandwidth are vital to the op-amp's performance, particularly in closed-loop feedback systems. Additional parameters such as input common mode range, maximum output swing, power dissipation, and slew rate can also vary in degrees of importance based on the application. Outside of a general-purpose design, the application specifications and understanding of tradeoffs between parameters are essential for designing a high-performance op-amp. This section aims to provide an analysis of the common op amp topologies, describe design techniques, and compare the characteristics of each topology. Note that the analysis throughout this section will be provided based upon long-channel device characteristics.

3.1.1.1 Two-Stage Op-Amp

The first op-amp that will be discussed is the traditional two-stage op-amp shown in Fig. 3.2. The first stage is a differential amplifier biased by M1 while the second stage is a common source amplifier formed by M7 and its biasing transistor M6. Since the op-amp has a high-impedance node at the drains of M3 and M5, which is neither the input nor the output, it is not considered an operational transconductance amplifier (OTA). The stability of the op-amp will often require the resistor R_Z and capacitor C_C to be used for compensation, although it will be shown why this is not always the case.

The input common mode range of the op-amp is one of the first parameters to consider. The minimum common mode voltage is determined to be (3.19) with a KVL between either of the two inputs and ground.

$$\boldsymbol{V_{CM,MIN} = V_{GS2,3} + V_{DS,SAT1}} \tag{3.19}$$

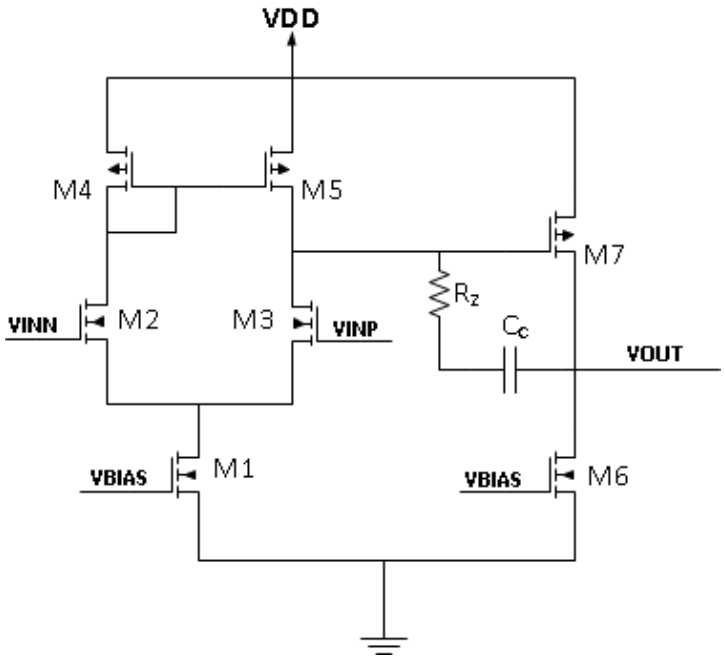

Fig. 3.2. The schematic of a two-stage op-amp.

Similarly, equation (3.20) expresses the maximum common mode voltage. To simplify this equation, it is necessary to find the drain voltage on the NFET M2 (or M3). Rearranging (3.21) to (3.22) and (3.23) shows the condition that keeps M2 or M3 in the saturation region. Plugging (3.23) into (3.20) yields (3.24).

$$\boldsymbol{V_{CM,MAX} = VDD - V_{SG4,5} - V_{DS2,3} + V_{GS2,3}} \tag{3.20}$$

$$\boldsymbol{V_{DS} \geq V_{GS} + V_{TH}} \tag{3.21}$$

$$\boldsymbol{V_D - V_G \geq V_{TH}} \tag{3.22}$$

$$\boldsymbol{V_G - V_D \leq V_{TH}} \tag{3.23}$$

$$\boldsymbol{V_{CM,MAX} = VDD - V_{SG4,5} + V_{THN2,3}} \tag{3.24}$$

A key takeaway from expressions (3.19) and (3.24) is that the value of $V_{CM,MAX}$ will typically be closer to VDD than $V_{CM,MIN}$ is to ground. The use of both an NFET and PFET input pair allows for obtaining a wider input common mode range, which can extend from below ground up to approximately VDD.

The maximum output swing of the op-amp is limited by the $V_{SD,SAT}$ value of the output stage PFET M7 whereas the minimum output swing is limited by the current sink M6's $V_{DS,SAT}$. The output swing can be increased by designing M6 or M7 with a larger width. However, the tradeoffs for this design choice include an increase in power consumption, the potential for systematic offset, and a change in the frequency response of the circuit.

With respect to the types of offsets, random offset results in threshold voltage and mobility differences between devices that are intended to be matched such as the NFET pair M2 and M3 in Fig. 3.2. These mismatches can be minimized with offset cancellation schemes and with layout practices such as the common centroid layout technique. Systematic offset is a function of the design and can be seen in simulations. Systematic offset arises when FET pairs within the same

stage are not matched (e.g. M2 and M3) or a PFET/NFET branch (e.g. M6 and M7) is not matched to sink and source equal amounts of current. Systematic offset is eliminated by making a symmetrical design such that the DC bias currents satisfy the equations given in (3.25) and (3.26).

$$\boldsymbol{I_{D2} = I_{D3} = I_{D4} = I_{D5}} \tag{3.25}$$

$$\boldsymbol{I_{D6} = I_{D7}} \tag{3.26}$$

The low frequency, open-loop gain of the two-stage op-amp shown in Fig. 3.2 is a product of the gains of the differential and output stages, as given by equations (3.27) to (3.30).

$$\boldsymbol{A_{OL,DC} = A_{Stage1} * A_{Stage2}} \tag{3.27}$$

$$\boldsymbol{A_{Stage1} = g_{m3}(r_{o3} // r_{o5})} \tag{3.28}$$

$$\boldsymbol{A_{Stage2} = g_{m7}(r_{o6} // r_{o7})} \tag{3.29}$$

$$\boldsymbol{A_{OL,DC} = g_{m3}g_{m7}(r_{o3} // r_{o5})(r_{o6} // r_{o7})} \tag{3.30}$$

Based on the hybrid-pi model, the locations of the first and second poles are expressed as (3.31) and (3.32), respectively. The values of C_1 and C_2 in the second pole equation are determined by the inherent MOSFET capacitances as shown in equations (3.33) and (3.34).

$$\boldsymbol{f_{p1} = f_{3dB} = \frac{1}{2\pi(g_{m7})(r_{o3} // r_{o5})(r_{o6} // r_{o7})C_C}} \tag{3.31}$$

$$\boldsymbol{f_{p2} = \frac{g_{m7}C_C}{2\pi[(C_C)(C_1)+ (C_C)(C_2)+ (C_1)(C_2)\,]}} \tag{3.32}$$

$$\boldsymbol{C_1 = C_{gd3} + C_{gd5} + C_{sg7}} \tag{3.33}$$

$$\boldsymbol{C_2 = C_{LOAD} + C_{gd6}} \tag{3.34}$$

A takeaway from the equations for the first and second poles is that the locations of the two poles will split apart with a larger C_C, a common technique referred to as pole splitting. The C_C is critical for stability since it effectively provides a large capacitance on the gate of the PFET in the second stage (i.e. M7) and a relatively small capacitance at the output of the second stage. The input and output capacitances of the second stage, provided by C_{gd7}, can be expressed as in

(3.35) and (3.36) using Miller's theorem, where A_V is the gain of the common source amplifier formed by M7.

$$\boldsymbol{C_{IN} = C_{gd7}(1 + |A_V|)} \tag{3.35}$$

$$\boldsymbol{C_{OUT} = C_{gd7}(1 + \frac{1}{|A_V|})} \tag{3.36}$$

Intuitively, the input capacitance becomes effectively larger since it is charged without the gain provided by the common source amplifier. The gain of the amplifier charges the output capacitance faster and is the underlying reason for the effective decrease in output capacitance. This demonstrates the importance of pole splitting and why increasing C_C results in f_{p1} and f_{p2} moving farther apart.

However, ignoring R_Z momentarily, a larger value of C_C results in the output of the differential amplifier shorting with the output of the second stage at lower frequencies. As the output of the first stage shorts to the output of the second stage, the common source amplifier is bypassed and there is no longer an inversion. This creates a zero in the right half plane (RHP), which leads to a +20 dB/decade gain and a -45º/decade phase roll off as given by equation (3.37).

$$\boldsymbol{f_z = \frac{1}{2\pi(C_C)(\frac{1}{g_{m7}})}} \tag{3.37}$$

A zero in the RHP is undesirable due to the decrease in phase. To achieve high speed operation, this zero needs to be moved to the left half plane (LHP) such that it contributes +20 dB/decade gain and +45º/decade phase. The nulling resistor R_Z is inserted in series with the compensation capacitor C_C to attenuate the feedforward current (from the 1st stage to 2nd stage) and either cancel the zero ($R_Z = 1/g_{m7}$) or move the zero into the LHP ($R_Z > 1/g_{m7}$). Implementing an R_Z greater than $1/g_{m7}$ forces the feedforward current through the capacitor to be in-phase with

the output current such that it negates the effects of the output pole and recovers the phase lost. The location of the zero is then determined by the expression (3.38).

$$f_z = \frac{1}{2\pi(C_C)(\frac{1}{g_{m7}} - R_Z)} \tag{3.38}$$

When the RHP zero is eliminated, the frequency response of the op-amp is that of a single pole system with a phase margin of nearly 90º. However, in practical applications it is difficult to make $1/g_{m7}$ and R_Z equal over all process corners. A solution is to use an op-amp with an indirect compensation technique, as in Fig. 3.3, that injects C_C's feedforward current from the 2nd stage output, through a low-impedance node (M5A's source), and into the high impedance node at M3's drain. The RHP zero is eliminated with this method since the feedforward path is blocked (1st to 2nd stage), but the output can still feed back to the input at high frequencies to reduce the gain.

This scheme improves the frequency response by moving f_{p2} to a higher frequency because M3's drain is no longer loaded by C_C. The split length devices (e.g. M4A and M4B, M5A and M5B, as well as M7A and M7B) are used to reduce the offset by keeping the PFET V_{DS} and V_{GS} values the same in both the first and second stages. A PFET based differential amplifier can be added to make the input common mode range nearly rail-to-rail, as shown in Fig. 3.4.

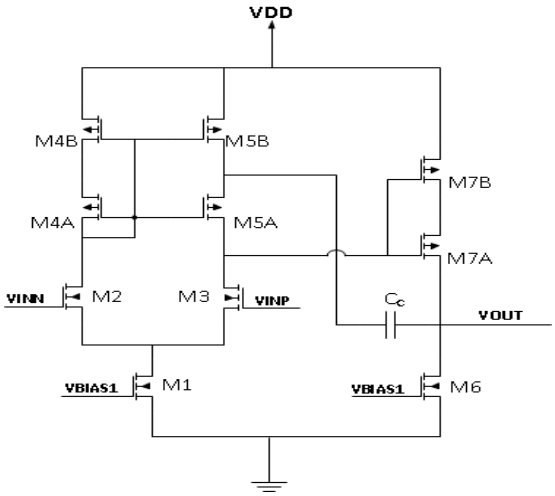

Fig. 3.3. An indirect compensation technique for the two-stage op-amp.

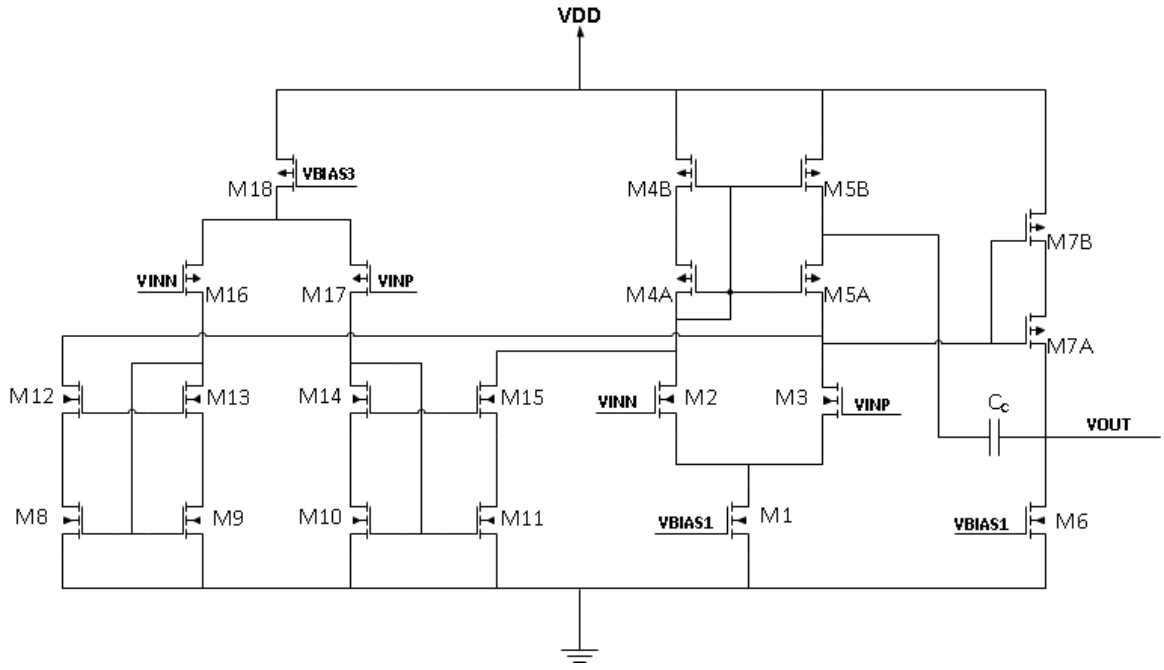

Fig. 3.4. A rail-to-rail two-stage op-amp with indirect compensation.

3.1.1.2 Folded-Cascode Op-Amp

The conventional folded-cascode topology shown in Fig. 3.5 offers an improvement in the low-frequency, open-loop gain compared to a single stage differential amplifier or a two-stage op-amp if an output stage is included. The cascoded devices in this topology allow for a relatively high output resistance and large DC gain. One of the most notable distinctions of the folded-cascode topology compared to the two-stage op-amp is that the load capacitance plays a key role in the frequency response.

The maximum value of the input common-mode range is determined by expression (3.39). Using the long channel saturation condition equations, as in the two-stage op-amp analysis, allows for rearranging the equation into (3.40).

$$\boldsymbol{V_{CM,MAX} = VDD - V_{SD,SAT4,5} - V_{DS,SAT2,3} + V_{GS2,3}} \tag{3.39}$$

$$\boldsymbol{V_{CM,MAX} = VDD - V_{SD,SAT4,5} + V_{THN2,3}} \tag{3.40}$$

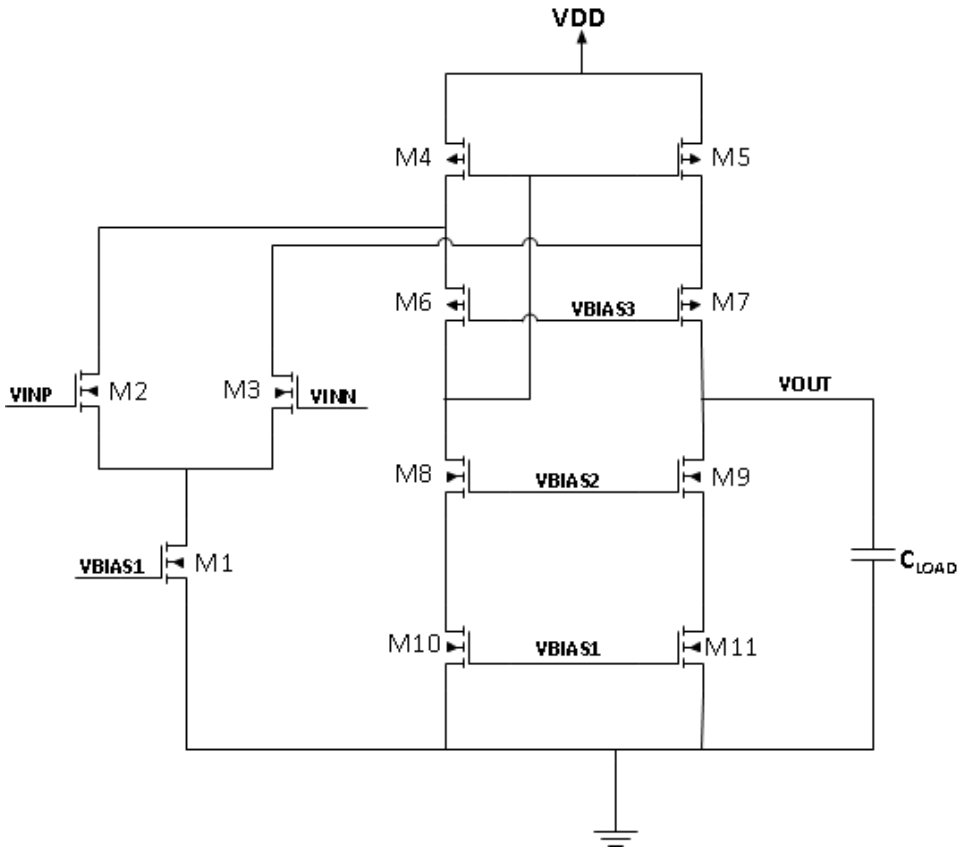

Fig. 3.5. A conventional folded-cascode topology with an NFET input pair.

The minimum value of the input common mode range is expressed in equation (3.41). A solution for designing a nearly rail-to-rail input common mode range for the folded-cascode is to add a PFET differential amplifier similar to the two-stage topology in Fig. 3.4.

$$\boldsymbol{V_{CM,MIN} = V_{GS2,3} + V_{THN2,3}} \tag{3.41}$$

If a PFET input pair is added, then the drain of each PFET connects to the drain of either M10 or M11. Note that this will change the sizing of the existing FETs. In the configuration shown in Fig. 3.5, the PFETs M4 and M5 are both sourcing current to the differential amplifier and the cascode structures. To mitigate systematic offset, the DC current flowing through one branch of the differential amplifier should be the same as the corresponding branch of the cascode structure. The width of M4 and M5 should therefore be sized appropriately (i.e. twice that of M6 and M7).

With a PFET input pair added, the NFETs M10 and M11 would likewise need to have their widths doubled to account for sinking current to two different branches with equal DC currents.

The wide swing cascode current mirror configuration implemented by connecting the drain of M6 to the gate of M4 (and M5) more accurately mirrors the current through M5's branch. The operation of the current mirror can still be intuitively understood as a single gate-drain connected PFET that mirrors current. However, the goal of this approach is to bias M4's gate such that the V_{SD} of M4 places it on the edge of saturation, which closely matches with the V_{SD} of M5.

If a gate-drain connection was made with M4 and a separate gate-drain connection was made with M6, then the finite output resistances of the FETs would result in more poorly matched currents through M4 and M5. The gates of M4 and M5 would be biased to (3.42). Likewise, the gates of M6 and M7 would be set to (3.43).

$$\boldsymbol{V_{G4,5} = VDD - V_{SD4,5} - V_{THP4,5}} \tag{3.42}$$

$$\boldsymbol{V_{G6,7} = V_{G4,5} - V_{SD6,7} - V_{THP6,7}} \tag{3.43}$$

From equation (3.42), the gate voltage of M4 and M5 is set to a threshold drop beyond the saturation condition. By decreasing the gate voltage to only $V_{SD4,5}$ below VDD, the devices can be placed on the edge of saturation. This allows for more accurately mirrored currents and it also decreases the supply voltage requirement, leading to either lower power consumption or increased speed. The wide swing cascode current mirror shown in Fig. 3.5 accomplishes this since the drains of M4 and M5 follow equation (3.44).

$$\boldsymbol{V_{D4,5} = VDD - V_{SD4,5}} \tag{3.44}$$

Similarly, the gates of M6 and M7 can now be biased to (3.45), which eliminates a second threshold drop as seen by equations (3.42) and (3.43).

$$V_{G6,7} = V_{D4,5} - V_{SD6,7} - V_{THP6,7} \tag{3.45}$$

The output swing of the folded-cascode topology shown in Fig. 3.5, regardless of whether a PFET differential pair is added, is limited to (3.46) and (3.47) for the minimum and maximum, respectively.

$$V_{OUT,MIN} = V_{DS,SAT9} + V_{DS,SAT11} \tag{3.46}$$

$$V_{OUT,MAX} = VDD - V_{SD,SAT5} - V_{SD,SAT7} \tag{3.47}$$

From the equations given above, it is apparent that the greatest output swing occurs when M4 – M7 and M8 – M11 are all biased to be on the edge of saturation.

The low-frequency, open-loop gain is improved due to the cascoded FETs which result in an output resistance that is simplified in equation (3.48). The output resistance of M7 and M9 are expressed in (3.49) and (3.50), respectively, which yields (3.51) as the combined output resistance. The open-loop DC gain can then be expressed as (3.52). Note that if a PFET differential amplifier is also included in the folded-cascode configuration to enable a nearly rail-to-rail input common mode range, then the open-loop gain may be up to twice that given in (3.52).

$$R_o = R_{o7} // R_{o9} \tag{3.48}$$

$$R_{o7} = (g_{m7}r_{o7})(r_{o3} // r_{o5}) \tag{3.49}$$

$$R_{o9} = (g_{m9}r_{o9})(r_{o11}) \tag{3.50}$$

$$R_o = (g_{m7}r_{o7})(g_{m9}r_{o9})(r_{o11})(r_{o3} // r_{o5}) \tag{3.51}$$

$$A_{OL,DC} = \frac{V_{OUT}}{V_{IN}} = (g_{m3})(R_o) \tag{3.52}$$

The folded-cascode topology given in Fig. 3.5 is considered to be an operational transconductance amplifier (OTA) since the input and output are the only high impedance nodes and every other node is low impedance, meaning they are either gate-drain connected or are connected to sources. The frequency response of this topology is therefore more dependent on the

load capacitor than the two-stage op-amp. The dominant pole in the folded-cascode OTA is a function of the output resistance and load capacitance as given by (3.53).

$$\boldsymbol{f_{p1} = \frac{1}{2\pi(C_{LOAD})(R_o)}} \tag{3.53}$$

Multiple high frequency poles exist within the OTA that are due to the inherent MOSFET capacitances. The first non-dominant pole, meaning it is the lowest in frequency outside of the dominant pole, is generally given by (3.54).

$$\boldsymbol{f_{p2} = \frac{g_{m7}}{2\pi(C_{gs7} + C_{gd5})}} \tag{3.54}$$

The folded-cascode will typically operate as a single pole system such that the high frequency poles do not hinder its stability. As will be explained in Chapter 4, however, compensation may be necessary in scenarios where an output stage is used and the op-amp is no longer an OTA.

3.1.1.3 Telescopic Differential Amplifier

The final op-amp topology that will be analyzed in this section is the telescopic differential amplifier. A schematic of one telescopic differential amplifier topology is shown in Fig. 3.6. Devices in cascode are the foundation of the telescopic op-amp, as with the folded-cascode topology. The output resistance and DC gain of the telescopic op-amp in Fig. 3.6 are given by (3.55) and (3.56), respectively.

$$\boldsymbol{R_o = g_{m3} r_{o3} r_{o5} \,//\, g_{m7} r_{o7} r_{o9}} \tag{3.55}$$

$$\boldsymbol{A_{OL,DC} = \frac{V_{OUT}}{V_{IN}} = (g_{m3})(R_o)} \tag{3.56}$$

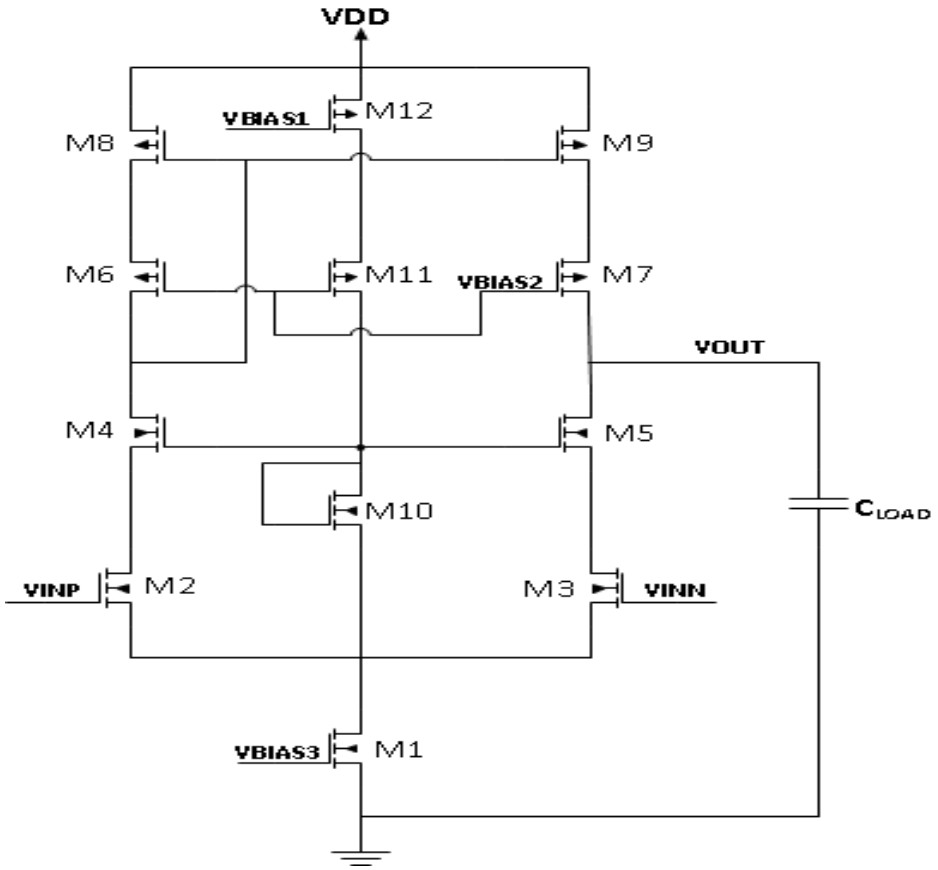

Fig. 3.6. The schematic of a telescopic differential amplifier.

The drain of M10 is connected to the gates of M4 and M5 as well as to the source of M11. This forms a wide swing cascode current mirror configuration and ensures that the V_{GS} of M5 and the V_{DS} of M3 stay constant within the input common mode range while keeping each of the devices in saturation. The reason for this is the constant current flowing through M10, set by the cascode current mirror of M11 and M12. When the input common mode voltage rises, it results in an increase in the source voltages of M2 and M3. This causes the voltage on the gates of M4 and M5 to increase, leading to higher drain voltages on M2 and M3. The maximum input common mode voltage is given in (3.57) and is limited to when M4 and M5 are no longer in saturation.

$$\boldsymbol{V_{CM,MAX} = VDD - V_{SG8,9} - V_{DS,SAT4,5} + V_{THN2,3}} \tag{3.57}$$

The minimum input common mode voltage is given by (3.58).

$$V_{CM,MIN} = V_{GS2,3} + V_{DS,SAT1} \tag{3.58}$$

Another wide swing cascode current mirror is formed by M6 and M8. Again, this is used to keep both M8 and M9 at the edge of saturation to more accurately mirror the current and increase the maximum output voltage swing. The minimum and maximum output voltages are provided in (3.59) and (3.60), respectively.

$$V_{OUT,MIN} = V_{DS,SAT5} + V_{DS,SAT3} + V_{DS,SAT1} \tag{3.59}$$

$$V_{OUT,MAX} = VDD - V_{SD,SAT9} - V_{SD,SAT7} \tag{3.60}$$

The telescopic op-amp has either comparable or worse input common mode range and output voltage swing compared to the folded-cascode. However, it offers relatively high bandwidth. The dominant pole is given in (3.61) and is a function of the load capacitance along with the output resistance, similar to the folded-cascode OTA.

$$f_{p1} = \frac{1}{2\pi(C_{LOAD})(R_o)} \tag{3.61}$$

Multiple high frequency poles exist such as at the source of M4 and the source of M7. The first non-dominant pole is typically found in the path from M4 to the output (i.e. M4 to M8, mirrored over to M9 and then to the output). The total capacitance in the path, ignoring the body terminal, can be approximated as in (3.62).

$$C_{Total} = C_{gd4} + C_{gs8} + C_{gd8} + C_{gs9} + C_{gd9} + C_{gs7} \tag{3.62}$$

The first non-dominant, or second, pole can then be determined to be (3.63).

$$f_{p2} = \frac{g_{m8}}{2\pi(C_{Total})} \tag{3.63}$$

3.1.1.4 A Comparison of Topologies

The stability of the op-amps discussed hinges upon minimizing the number of poles in the signal path. For each op-amp stage used, there will be at least one pole added to the system. The

folded-cascode and telescopic op-amps previously discussed are single stage systems and contain a dominant pole followed by multiple high frequency poles. Although compensation techniques can be implemented, it will typically not impact the op-amp's bandwidth considerably due to already having a dominant pole.

The two-stage op-amp contains two poles that are relatively close to each other, with one pole located at the output of the first stage and the other at the output of the second stage. In the two-stage op-amp, pole splitting acts to compensate the op-amp by making a dominant pole. Creating a more dominant pole causes the gain to roll off at low frequencies and causes a noticeable decrease in bandwidth.

Literature has demonstrated the operation of multistage op-amps, such as the three-stage op-amp [37] – [39]. The same principle of at least one additional pole per stage applies to these topologies. While the gain will increase due to the total gain being a product of each stage, the bandwidth will decrease as more compensation is necessary for added stages.

A comparison of the topologies discussed is presented in Table 3.1. Although the two-stage op-amp performs relatively well in all categories except bandwidth, the folded-cascode and telescopic op-amps discussed were only a single stage. Adding an output stage to the folded-cascode or telescopic op-amps will increase the gain, but will require compensation and lead to a reduced bandwidth. However, publications have recently shown improvements to the folded-cascode topology that increase the bandwidth and gain by turning biasing transistors into signal paths [40] – [42].

Table 3.1. A comparison of the two-stage, folded-cascode, and telescopic topologies.

Topology	Input Common Mode Range	Output Swing	Gain	Bandwidth
Two-stage	High	High	High	Low
Folded-cascode	High	Medium	Medium	Medium
Telescopic	Medium	Medium	Medium	High

The improved folded-cascode topology is referred to as the recycling folded-cascode. The potential of this topology exceeds both the two-stage and telescopic designs, particularly when an output stage is added. Apart from the two-stage op-amp in the Vulcan II linear regulator, the recycling folded-cascode will be the basis of op-amp design in this work and is discussed in greater detail in Chapter 4.

3.1.1.5 Additional Op-Amp Considerations

Three other op-amp parameters are common-mode rejection ratio (CMRR), power-supply rejection ratio (PSRR), and slew rate. Both the CMRR and PSRR of an op-amp are in part a function of the DC open-loop gain of the op-amp. As the name implies, the CMRR is the ability of the op-amp to not let the input common-mode voltage influence the output. In the two-stage op-amp, for example, the total common-mode gain is a product of the second stage gain (A_2) with the first stage's common-mode gain (A_C). The CMRR of the two-stage is given in (3.64).

$$\boldsymbol{CMRR = 20log\left(\frac{A_{OL}}{A_C * A_2}\right) = 20log\left(\frac{A_1 * A_2}{A_C * A_2}\right)} \tag{3.64}$$

The PSRR is critical in applications where the output voltage must be precise or if the supply voltage is not well regulated. The PSRR is given by the expressions in (3.18) and (3.65).

$$\boldsymbol{PSRR = 20log\left(\frac{A_{OL}}{v_{out}/\Delta v_{supply}}\right) = 20log\left(\frac{A_1 * A_2}{v_{out}/\Delta v_{supply}}\right)} \quad (3.65)$$

Finally, the slew rate is defined as the change in output voltage versus time. It's primarily a function of the bias current in the output branch of the op-amp. By increasing the widths of FETs to set a higher bias current, the slew rate can be increased. However, the tradeoff is that the power dissipation will increase. The slew rate of an op-amp can be expressed as in (3.66). For capacitive loads, the equation in (3.67) can be rearranged to express the slew rate as (3.68).

$$\boldsymbol{Slew\ Rate = \left(\frac{dV_{out}}{dt}\right)} \quad (3.66)$$

$$\boldsymbol{I_{BIAS} = (C_{LOAD})\left(\frac{dV_{out}}{dt}\right)} \quad (3.67)$$

$$\boldsymbol{Slew\ Rate = \left(\frac{I_{BIAS}}{C_{LOAD}}\right)} \quad (3.68)$$

Typically slew rates are on the order of several Volts per microsecond and are not a significant concern except for high speed applications, which are generally silicon based and outside of the scope of this work, or if a significant amount of compensation is added.

3.1.2 Stability Criteria and Considerations

As mentioned in the previous sections, a stable system requires the open loop response of the feedback network to have a phase shift of less than 180º. Every node in a system's small signal path will introduce parasitic capacitances due to inherent MOSFET capacitances. These capacitances will shunt the signals to AC ground, but generally create poles that lie at relatively high frequencies and ideally come into play only after the system's gain has dropped below 0 dB.

Both linear regulator and op-amp designs typically target a phase margin of at least 45º, which indicates the difference between the phase at the unity gain frequency and 180º of total shift. If the phase shift at the unity gain frequency has exceeded 180º, then the system does not have any phase margin and is unstable. To ensure a system has the desired phase margin, compensation

schemes can be implemented to force a dominant pole that causes the system's gain to roll off sooner and reach 0 dB at lower frequencies. The result is that the system behaves similarly to a single pole system and has a total phase shift that approaches only 90º.

The difference between a phase margin of 45º and 90º is the system's transient response to a disturbance. With 45º of phase margin, the system will typically oscillate three times with a relatively large overshoot and undershoot before settling to a steady-state value after three time constants. In this scenario, the system is underdamped and the time constant is related to the closed-loop bandwidth of the system by (3.69).

$$\boldsymbol{\tau = \frac{1}{2\pi(f_{BW,CL})}} \tag{3.69}$$

Designing for a phase margin below 45º is not desirable for most applications since component variation can result in a phase margin closer to 0º in a fabricated device which can cause additional oscillations or instability. For a phase margin of 90º, however, the system behavior is more representative of an overdamped system in which there is not an overshoot or undershoot. The trade-off is that the system can take longer to settle. This follows theoretical operation since a larger phase margin requires the system's gain to roll off quicker to avoid interference by another pole and the resulting bandwidth is lower.

A compromise is to design a system with a phase margin between 60º and 80º. This causes the system to have behavior closer to that of a critically damped system where the system either doesn't have an overshoot/undershoot or it is minimal. Simultaneously, the system bandwidth is not reduced as much as in the case with 90º of phase margin.

3.2 Switched Capacitor Converter

The higher efficiencies offered by switching converters make them desirable in power management designs. With the rise of wide bandgap semiconductors and the growing demand for high temperature applications, passive components required for switching converters have begun to receive an increasing amount of attention [43]. Inductors capable of operating up to 700 ºC have been reported recently, indicating that state-of-the-art inductors are not a limiting factor for traditional inductor-based switching converters [44].

Motivated by the need for per-core power management solutions for multicore processors and fast point-of-load regulation, research efforts have brought fully integrated inductor-based switching converters closer to realization [45] – [47]. However, obstacles to achieving financially viable, production level fully integrated switching converters still remain due to the relatively low energy density of on-die inductors as well as the requirement of augmenting the process with magnetic materials or thick metal layers [48]. The literature reports demonstrating fully integrated DC-DC converters utilize silicon processes that enable high switching frequencies and relatively small passive components. A similar solution in SiC IC technology therefore faces additional obstacles since current processes provide substantially lower switching frequencies.

Unlike off-chip ceramic capacitors that can have relatively small surface mount device (SMD) package sizes, inductors suitable for typical switching converters are large enough to substantially alter the footprint of a package. Ceramic capacitors are preferable for high temperature applications not only due to their small footprint, but also because certain ceramics (e.g. C0G ceramic materials) offer extremely temperature stable dielectrics. This is one factor benefiting the design of a switched-capacitor (SC) converter with off-chip components consisting entirely of capacitors. Recent literature publications have highlighted the high power density and

efficiency of SC converters [49] – [54]. One report has demonstrated superior performance in a step-down configuration compared to the traditional inductor-based buck converter [55].

A multitude of SC converter architectures exist and the degree of complexity can vary tremendously. The use of SC converters has historically been limited to relatively low power applications such as providing memory cells with boosted voltages [56]. The N-stage Dickson charge pump shown in Fig. 3.7 is an example of one architecture that is simple and commonly used for boosting a given voltage [57]. The MOSFETs act as diodes due to the gate-drain connection. When CLK goes low, the source voltage of the NFET MN1 becomes VDD - V_{THN}. When CLK is high, the source voltage of MN1 becomes 2VDD - V_{THN} and MN2 turns on such that its source becomes 2VDD – 2V_{THN}. The analysis can be continued throughout each stage, yielding (N)(VDD) – (N)(V_{THN}) and (N+1)VDD – (N)(V_{THN}) as the output voltage depending on whether CLK is high or low. The resulting output voltage swing can be reduced by using a larger capacitor C_N.

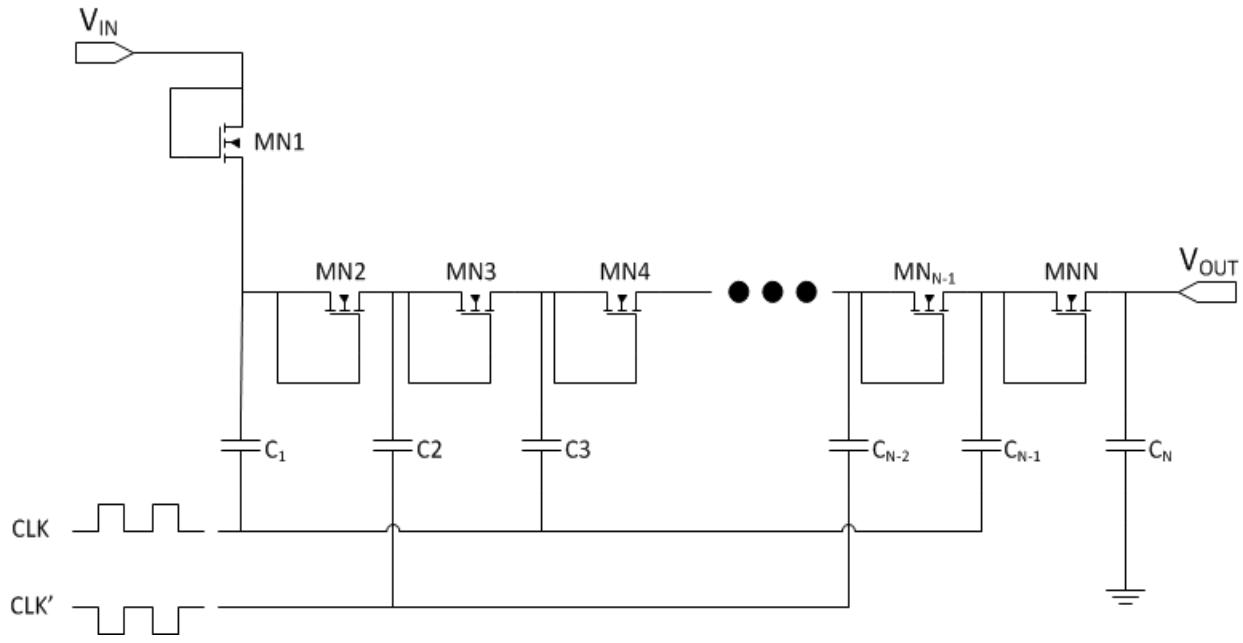

Fig. 3.7. The schematic of a generic N-stage Dickson charge pump.

In practice, an excessively large number of stages becomes a challenge due to process related constraints. The constraints that are essential to consider for the Dickson charge pump, as well as any SC converter, are the breakdown voltages of the capacitors and the MOSFET's gate oxide. With respect to the Dickson charge pump, the number of stages must be limited such that the increasing voltage of each stage does not exceed the ratings of the capacitors or oxide.

A simple 2:1 step-down SC converter configuration is shown in Fig. 3.8. After the MOSFETs and capacitor voltage ratings have been determined to be adequate for a given application, the operation can be analyzed in two phases. The MOSFETs operating in phase 1 (PH1) are switched on when the clock is high. When the inverse of the clock signal is high, then the MOSFETs designated for phase 2 (PH2) are switched on. The theoretical operation assumes that both PH1 and PH2 have a 50% duty cycle. Literature has reported operation with the two phases having variable duty cycles, but optimal efficiency has been determined to occur with a 50% duty cycle [52].

During the PH1 operation of the circuit shown in Fig. 3.8, current flows through MN1, C1, and MN4 to the output such that the circuit behavior corresponds to equation (3.70). In PH2, MN1 and MN4 are off while MN2 and MN3 are on. The capacitor discharges to the load in this phase

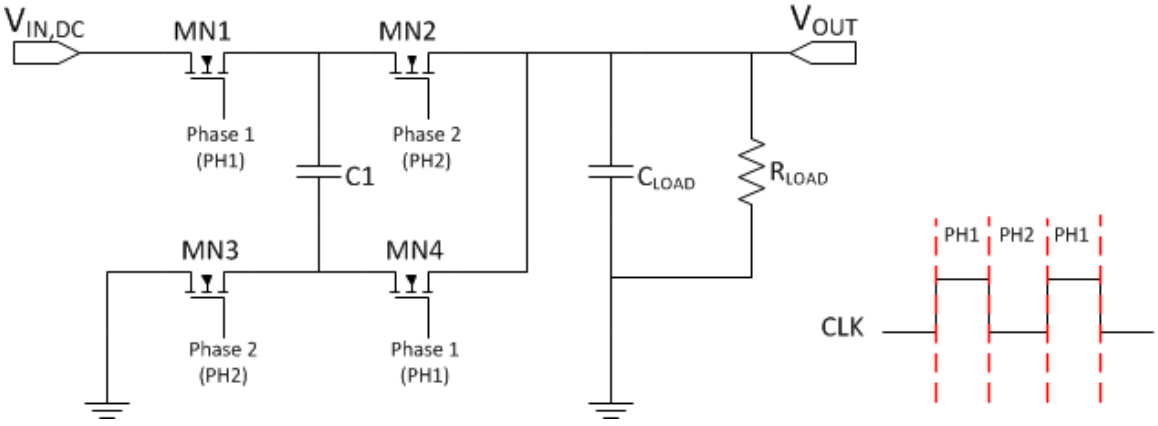

Fig. 3.8. The schematic of a 2:1 step-down SC converter.

and the circuit follows the expression in (3.71). Substituting the expression for V_{C1} found in equation (3.71) into (3.70) yields (3.72). Rearranging expression (3.72) to (3.73) proves the resulting 2:1 step-down ratio.

$$\boldsymbol{V_{OUT} = V_{IN,DC} - V_{C1}} \tag{3.70}$$

$$\boldsymbol{V_{OUT} = V_{C1}} \tag{3.71}$$

$$\boldsymbol{V_{OUT} = V_{IN,DC} - V_{OUT}} \tag{3.72}$$

$$\boldsymbol{V_{OUT} = \frac{1}{2} V_{IN,DC}} \tag{3.73}$$

The 2:1 step-down converter presented in Fig. 3.8 acts as a unit cell. Expanding from a single unit cell configuration allows for achieving multiple conversion ratios. A single SC converter can therefore support step-down conversions such as 2:1, 3:2, or 4:3. An example of a SC converter composed of two unit cells and supporting 2:1 as well as 3:2 conversion ratios is shown in Fig. 3.9. When operating with a 2:1 conversion ratio, the MOSFET MN5 is off in both PH1 and PH2. Ignoring added switching losses due to the additional unit cell, the resulting circuit behavior is identical to the single unit cell shown in Fig. 3.8 and follows the expressions in (3.70) to (3.73).

When the SC converter in Fig. 3.9 operates with a 3:2 conversion ratio, the MOSFETs that are conducting in PH1 in each unit cell remain the same as in the 2:1 conversion ratio operation. The capacitors C1 and C2 are both charged since they are connected between the input and output in this phase. In PH2, however, MN5 is turned on and MN7 is switched off. This forms two capacitors in series discharging to the output. The operation for the 3:2 conversion ratio follows expressions (3.74) and (3.75) for PH1 and PH2, respectively. Substituting the equation for V_{OUT}

given by (3.75) into (3.74) produces (3.76), which can be rearranged into the expression given in (3.77) to verify the 3:2 conversion ratio.

$$\boldsymbol{V_{OUT} = V_{IN,DC} - V_{C1,2},\ phase\ 1} \tag{3.74}$$

$$\boldsymbol{V_{OUT} = 2 * V_{C1},\ phase\ 2} \tag{3.75}$$

$$\boldsymbol{V_{OUT} = V_{IN,DC} - (\frac{1}{2})V_{OUT}} \tag{3.76}$$

$$\boldsymbol{V_{OUT} = \left(\frac{2}{3}\right) V_{IN,DC}} \tag{3.77}$$

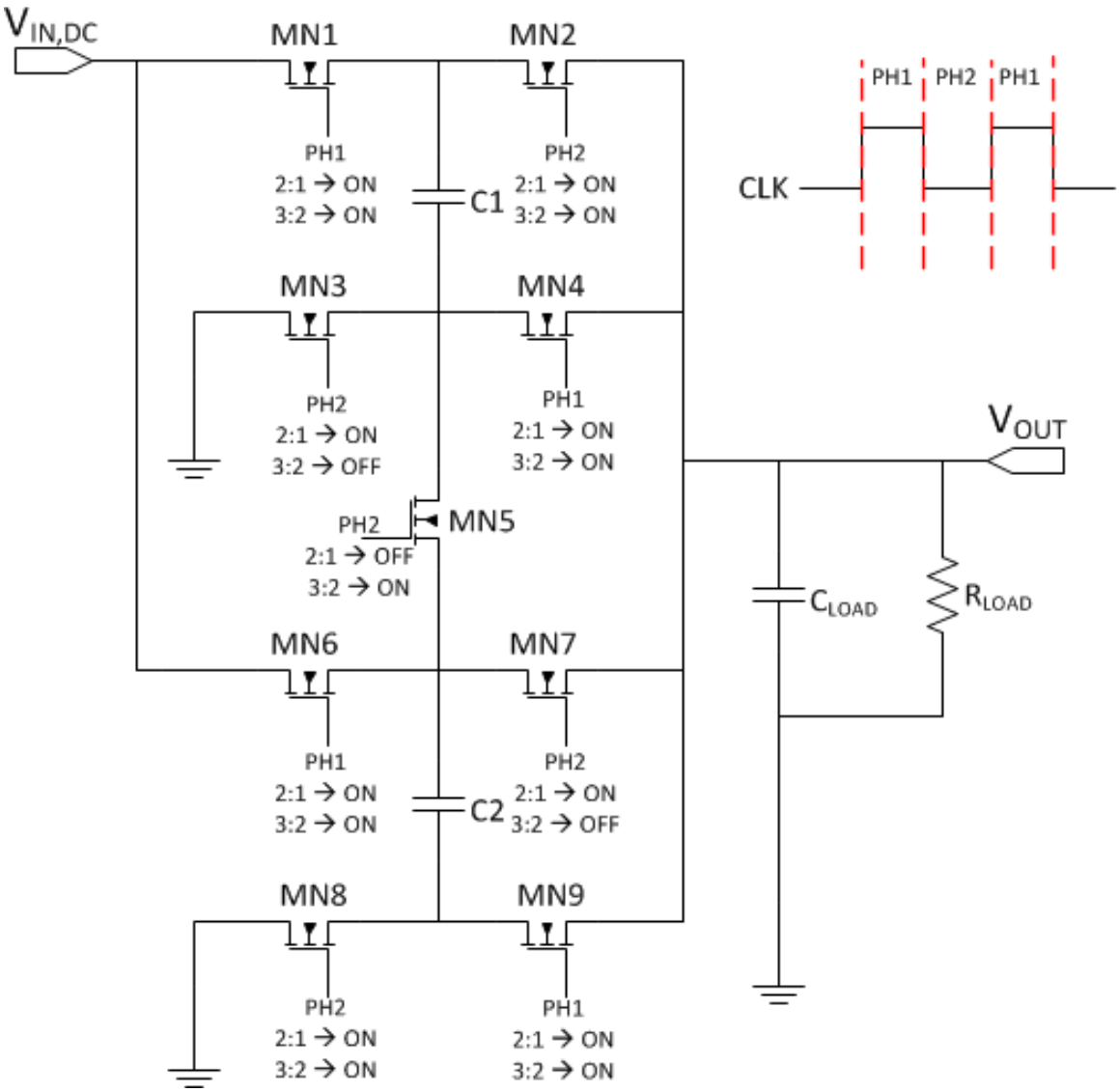

Fig. 3.9. A schematic of a SC converter supporting 2:1 and 3:2 conversion ratios.

3.2.1 Efficiency Considerations

The complexity of a SC converter can result in power losses due to multiple factors including the control logic to determine the conversion ratio to use, clock generators, and level shifters. Switching losses due to charging/discharging the gate capacitances of the MOSFETs are also present as with any switching converter and can be expressed as in equation (3.78). The constant α is considered due to each MOSFET's activity factor being dependent upon the conversion ratio. However, switching losses inherent to the selected SC converter topology should also be taken into consideration.

$$\boldsymbol{P_{Gate,loss} = \alpha(V_{GS})^2(C_{GATE})(f_{sw})} \tag{3.78}$$

As with traditional inductor-based switching converters, the capacitors in the SC converter must be appropriately sized to ensure enough charge is stored in each phase. Ignoring C_{LOAD}, the switching cycle will typically be faster than the charge/discharge time constant formed by R_{LOAD} and the flying capacitors (e.g. C1 and C2 in Fig. 3.9). The reason for this is that the losses associated with the SC converter can be attributed in part to the voltage ripple across the output and flying capacitors [58]. Referring to the simple 2:1 step-down converter provided in Fig. 3.8, the loss across the flying capacitor is given by equations (3.79) through (3.81). The constant "N" in equations (3.80) and (3.81) is determined by the converter topology and its output resistance [52].

$$\boldsymbol{P_{C1} = (I_{LOAD}) * (\frac{\Delta V}{2})} \tag{3.79}$$

$$\boldsymbol{\Delta V = \frac{2 * I_{LOAD}}{(N)(C1)(f_{sw})}} \tag{3.80}$$

$$\boldsymbol{P_{C1} = \frac{{I_{LOAD}}^2}{(N)(C1)(f_{sw})}} \tag{3.81}$$

For a given topology and load, the loss due to the flying capacitor C1 can be minimized by either increasing the switching frequency or the capacitance. Equation (3.78) has shown that the switching loss due to the MOSFET gate capacitance is proportional to the switching frequency, which will act to offset the benefit of lowering the flying capacitor losses. The remaining method for reducing the flying capacitor losses is to increase the capacitance value. The available chip area ultimately restricts the amount of capacitance that can be used in fully integrated solutions.

The total conduction loss of each MOSFET is another key factor and is given by equation (3.82). The constant $N_{sw,active}$ is the total number of active switches in a conversion ratio and is given by (3.83), where N_{PH1} and N_{PH2} refer to the total number of active switches in the corresponding phase of operation. The value of $R_{DS,ON}$ can be reduced with a larger channel width, although this comes at the expense of an increase in chip area, gate capacitance, and switching losses.

$$\boldsymbol{P_{R_{DS,ON}} = (N_{sw,active})(I_{LOAD})^2 R_{DS,ON}} \tag{3.82}$$

$$\boldsymbol{N_{sw,active} = N_{sw,total}[\left(\frac{1}{2}\right)(N_{PH1}) + \left(\frac{1}{2}\right)(N_{PH2})]} \tag{3.83}$$

The result of the efficiency analysis is that the three factors under a designer's control are the switching frequency, the on-resistance of a switch, and the capacitance values used [52]. The tradeoffs associated with each factor make it critical to optimize the design to a specific application. In addition, a SC converter with a topology for multiple conversion ratios will have more losses compared to a converter with a single conversion ratio. This is due to not only the overhead of the control logic, but also the greater number of switches and larger total gate capacitance that the control signals will be charging/discharging.

3.2.2 Control Logic and Supporting Circuitry

Although the fundamental operation is simple for both the 2:1 and 3:2 SC converters presented in the previous section, the control logic and supporting circuitry can lead to a relatively complicated design. From a power efficiency perspective, the digital circuitry is ideally operated from the lowest available supply voltage in the system. In addition, a separate supply is needed to ensure proper start-up given that the input voltage is potentially poorly regulated.

A linear regulator is a suitable approach to providing a supply voltage to the control circuitry. The inherent power dissipation of the linear regulator does present a disadvantage. However, the regulator can be designed such that it has a relatively low quiescent current and its output current capability also does not need to be excessive. The lower quiescent current can be achieved by reducing the current consumption of the selected op-amp which will lower its bandwidth. It is preferable to design for a bandwidth of approximately an order of magnitude higher than the switching frequency, although this is ultimately dependent upon the application.

Clock generation is the next core component of the design. Two possible options for clock generation, assuming an external clock is unavailable, are a ring oscillator or a voltage-controlled oscillator (VCO). The schematic of the generic ring oscillator is shown in Fig. 3.10 and the schematic of the current-starved VCO is provided in Fig. 3.11 [57].

The ring oscillator consists of a chain of inverters which are connected to the output of a NAND gate. The number of inverters in the chain must be even since the NAND gate acts as an inverter when its enable signal is a logic high. The other input of the NAND gate is the output of the inverter chain, which allows for the oscillatory nature of the inverter chain's output. The drive strength of the inverters determines the rise and fall times of the resulting square wave. Targeting

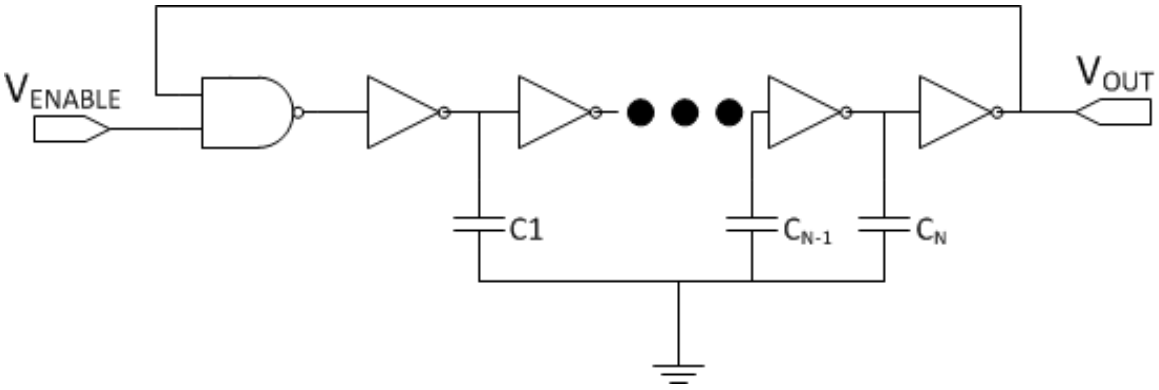

Fig. 3.10. The schematic of the ring oscillator.

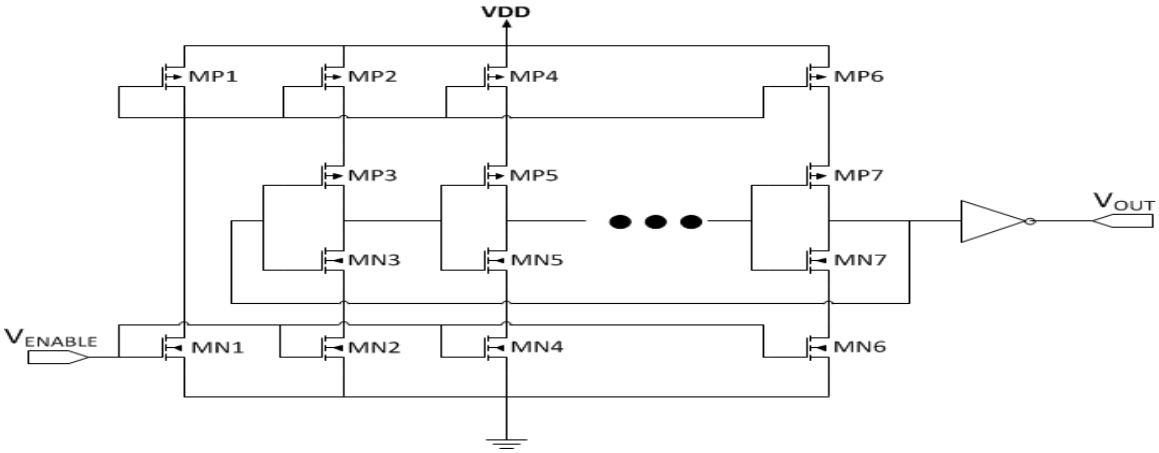

Fig. 3.11. The schematic of the current-starved VCO.

lower rise and fall times leads to greater static and dynamic current consumption, which forms a tradeoff with power consumption. Load capacitance can be added to slow the transition of each inverter's output and produce a lower frequency.

The operation of the current-starved VCO is similar to the ring oscillator. An input voltage greater than V_{THN} is provided to the gate of MN1 to control its current, which is identical to the current through MP1 due to the series connection. A current mirror configuration between MP1 and each of the top PFETs in the inverter chain as well as between MN1 and the bottom NFETs in the inverter chain serve to starve the current to each inverter. The VCO operation follows from the standard capacitor charge/discharge equation in (3.84), where I_D assumes the pull-up and pull-down strengths are equal, to yield the oscillation frequency in (3.85). The value of C_{total} combines

the gate capacitance of the inverter FETs, such as MN5 and MP5 in the second stage, with the output capacitance of the inverter.

$$\boldsymbol{I_D = \frac{(C_{total})(VDD)}{dt}} \tag{3.84}$$

$$\boldsymbol{f_{osc} = \frac{I_D}{(N_{stages})(C_{total})(VDD)}} \tag{3.85}$$

A non-overlapping clock generator is a requirement for either the ring oscillator or current-starved VCO. The two phases of operation are ideally each kept at a 50% duty cycle, but a stand-alone ring oscillator or VCO can potentially make both phases a logic high at the same time. This will create a short-circuit condition between the input, output, and ground. The non-overlapping clock generator presented in Fig. 3.12 is a solution for ensuring a deadtime between the two phases such that both are not high at the same time [57]. The amount of deadtime generated for each of the two phases can be controlled by the number of inverters in the chain, along with their drive strengths, and the input/output capacitance being charged during each transition. This has an impact on efficiency and overall performance since the ideal 50% duty cycle of each phase decreases slightly.

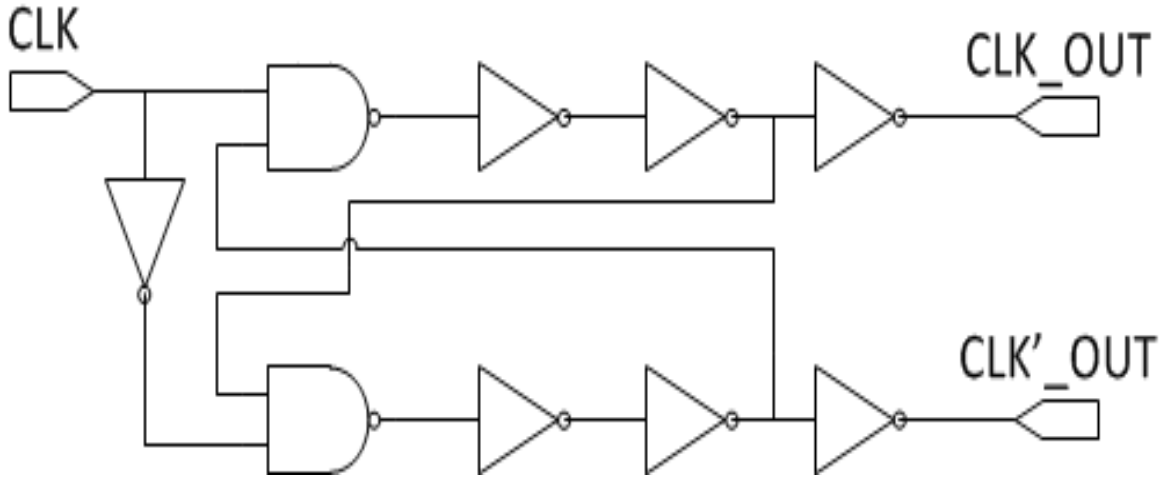

Fig. 3.12. The schematic of the non-overlapping clock generator.

The Dickson charge pump presented in Fig. 3.7 is necessary for boosting the relatively low supply voltage available for the control and support circuitry. This is due to some of the MOSFETs in the SC converter requiring a gate voltage larger than the available supply voltage, which is a possibility for MN1 in Fig. 3.9. It is essential to account for the voltage ratings associated with the MOSFET. For example, a maximum V_{GS} rating of 30 V will be exceeded if the MOSFET source is connected to ground and the gate is connected to a 3-stage Dickson charge pump with a VDD of 15 V and an output of 45 V (ignoring V_{TH} drops).

Level shifters are required for translating the digital logic high values, that are limited to a relatively low supply voltage, to the larger voltages available from a Dickson charge pump. The schematic in Fig. 3.13 provides a general-purpose CMOS approach to the issue. Additional solutions exist that vary in complexity and overhead. An example of a second solution is to connect the input to an inverter and then connect the inverter's output to the gate of an NFET in a common source amplifier configuration as is shown in Fig. 3.14. The disadvantages of this solution are the

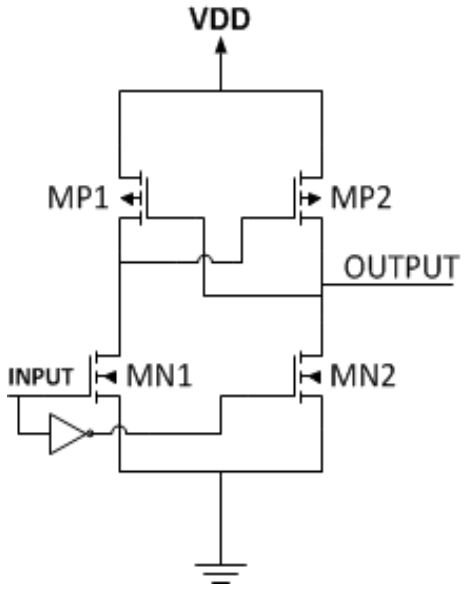

Fig. 3.13. A schematic of a cross-coupled level shifter.

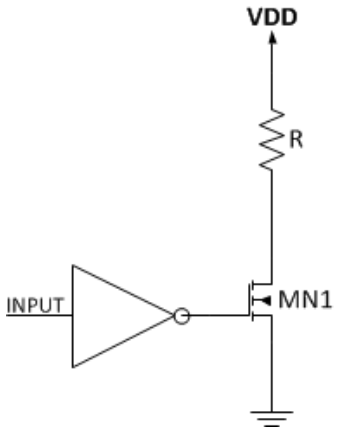

Fig. 3.14. A level shifter utilizing a common source amplifier with an inverted input.

static power consumption when the MOSFET is on and the need for the NFET to block up to VDD when it is off.

The final core component of the SC converter design is the digital control logic. The degree of complexity, and power consumption overhead, will undoubtedly rise as the number of possible conversion ratios becomes greater. The design that is discussed in Chapter 4 supports up to four conversion ratios and therefore the control logic must determine when to swap conversion ratios. For example, the application may benefit from an efficiency standpoint if a 2:1 conversion ratio is used for an input voltage range of 45 V to 50 V while a 3:2 conversion ratio is advantageous when the input is between 40 V and 44 V. Given the complexity of the logic when constructed at the gate level, the use of a Verilog synthesizer can be justifiable.

To determine the input voltage, the digital control logic relies upon comparators. Comparators are a building block for a wide range of mixed-signal circuitry including analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). Various comparator architectures exist and can range from using an operational amplifier in an open-loop configuration, to a topology with a cross-coupled load that implements a hysteresis band. For typical SC converter applications, the input ranges to detect are relatively large at 100 mV to

several Volts. In addition, the input voltage should not vary significantly over a period of several milliseconds. This means that the comparator does not need to be high bandwidth or high resolution, as would be the requirement for comparators in general-purpose ADCs.

A general-purpose comparator that is suitable for use in a SC converter is shown in Fig. 3.15 [57]. The comparator is composed of pre-amplification, decision, and output stages. The pre-amplification stage can be formed by one or more differential amplifiers. Its purpose is to amplify a signal to a large enough voltage that the decision circuit can see and act upon. The differential amplifier used in the pre-amplification stage can also have PFET input transistors added if a larger common-mode voltage is desired. In the configuration shown in Fig. 3.15, the minimum common mode input voltage is represented by equation (3.86). The equation assumes the standard long-channel saturation conditions for an NFET given in equations (3.87) and (3.88). By simplifying

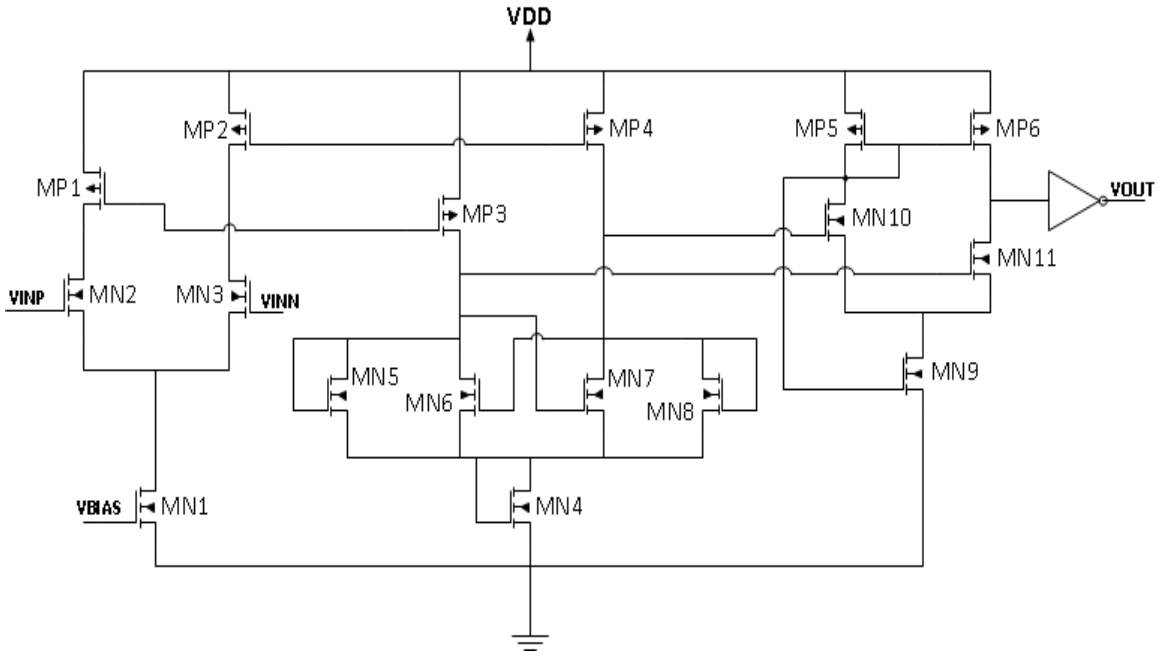

Fig. 3.15. A comparator with pre-amplification, decision, and output buffer stages.

the saturation condition in (3.88) to (3.89), the maximum common mode voltage can be determined by (3.90).

$$\boldsymbol{V_{CM,MIN} = V_{GS,MN2,3} + V_{DS,SAT,MN1}} \tag{3.86}$$

$$\boldsymbol{V_{GS} > V_{THN}} \tag{3.87}$$

$$\boldsymbol{V_{DS} \geq V_{GS} - V_{THN}} \tag{3.88}$$

$$\boldsymbol{V_{D} \geq V_{G} - V_{THN}} \tag{3.89}$$

$$\boldsymbol{V_{CM,MAX} = VDD - V_{SG,MP1,2} - V_{THN}} \tag{3.90}$$

The decision circuit consisting of MN4 – MN8, MP3, and MP4 as shown in Fig. 3.15 is based on a cross-coupled configuration to increase gain and provide hysteresis if necessary. As the non-inverting input of the differential amplifier rises above the inverting input, the voltage on the drain of MN5 and MN6 will increase as will the gate voltages of MN5 and MN7. The drain voltage of MN7 and MN8 will simultaneously decrease, leading to MN6 and MN8 being turned off. The outputs of the decision circuit transition at the point when the current through each branch is equal. If MN5 – MN8 are perfectly matched, then the design has no hysteresis. To create a hysteresis band, the (W/L) or V_{THN} values of the FETs must differ. In a practical implementation, an offset voltage will be present even if MN5 – MN8 are placed in a common centroid layout and will create hysteresis.

The output stage is necessary for translating the output voltages of the decision circuit into digital high or low signals. A differential amplifier can be utilized in the output stage in conjunction with an inverter. The differential amplifier acts as a gain stage after the decision circuit, allowing for a higher overall comparator speed. The inverter isolates the differential amplifier from potential loading effects, with the amplifier's output only seeing the input capacitance of the inverter. The inverter also forms a secondary gain stage.

CHAPTER 4 DESIGN AND SIMULATION

This chapter details the design process and simulation results for the top-level circuits listed in Chapter 3. The discussion will include the design of the externally compensated Vulcan II linear regulator, fully on-chip linear regulators, and a switched capacitor converter. The designs of the sub-circuits for each of the top-level designs, such as op-amps for the linear regulators, will also be described.

4.1 Vulcan II Linear Regulator: Design and Analysis

The design specifications for the Vulcan II linear regulator were to provide a stable output voltage of 15 V with an input voltage range of 20 V to 30 V as well as a load current of between 0 mA and 100 mA. The specifications were to be met for an operating temperature range of 25 ºC to 300 ºC. The intent was to provide a general-purpose linear regulator to serve as a supply for a variety of SiC CMOS mixed-signal circuitry. Due to the potential applications requiring fast load transients with unknown durations or frequencies, it was necessary to use a load capacitance to momentarily provide for the transients if the regulator's bandwidth was not sufficient.

The schematic of the Vulcan II linear regulator is shown in Fig. 4.1. The regulator is composed of the pass transistor (MN1), sampling network, op-amp, and the corresponding level shifting and compensation networks. The bias and reference voltages utilized by the op-amp were intended to be provided by external sources for the Vulcan II run.

The starting point for the design was to select a pass transistor. The overview of linear regulators provided in Chapter 3 revolved around using a PFET pass transistor, which is necessary for LDOs. Relatively small dropout voltages, lower footprint, and higher gain are the primary advantages of using a PFET pass device as opposed to an NFET.

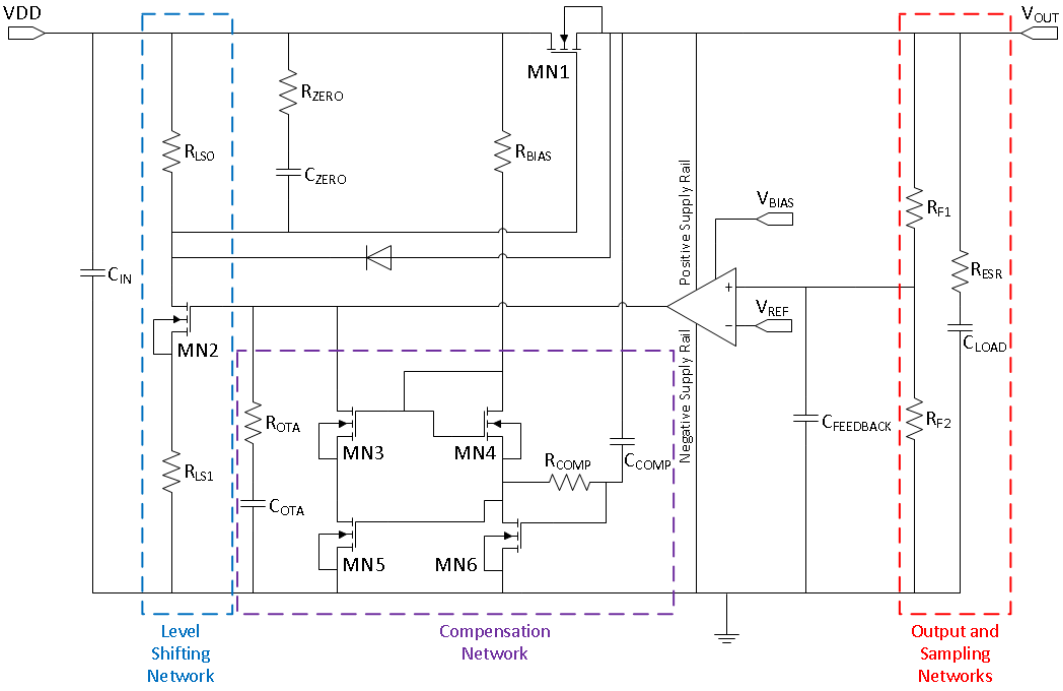

Fig. 4.1. The schematic of the Vulcan II linear regulator.

The lower dropout voltage is a result of the maximum V_{SG} applied to the PFET being the difference between the input voltage and ground. In contrast, an NFET pass device has a maximum V_{GS} that is limited to the difference between the input voltage and output voltage. The ability to provide a larger magnitude V_{SG} to the PFET allows the pass transistor to have a smaller magnitude of $V_{SD,SAT}$ for a given load current. A smaller $V_{SD,SAT}$ leads to the PFET based regulator's minimum input voltage being lower than that of its NFET based counterpart, leading to a higher possible efficiency. A benefit of the NFET device is the higher transition frequency (f_T) for a given V_{GS} due to lower inherent MOSFET capacitances. However, depending on the process parameters, a smaller PFET with reduced MOSFET capacitances and a relatively high V_{SG} magnitude can potentially achieve an equivalent f_T value compared to the NFET.

Similarly, a PFET device improves the open-loop DC gain of the regulator due to the common source (CS) configuration. The gain of the common-source configuration is given by

(4.1), which can be greater than one. The NFET pass transistor is limited to a gain of one or less as given by (4.2) due to the common drain (CD) configuration.

$$\boldsymbol{A_{V0,CS} = -g_m(R_{LOAD} \,//\, r_o)} \tag{4.1}$$

$$\boldsymbol{A_{V0,CD} = g_m(R_{LOAD} \,//\, \frac{1}{g_m})} \tag{4.2}$$

Referring to Fig. 2.1, the lack of an isolated N-well in the HiTSiC® process presents a problem for a PFET pass transistor based design. Without an isolated N-well, every PFET on a single die must have its body tied to the N-type substrate. To avoid forward biasing a parasitic diode (e.g. when the N-type substrate potential is a diode drop below a P+ region), it is necessary to connect the N-type substrate to the highest voltage in the system. If a PFET pass transistor is used, then the input voltage must be the substrate voltage. Mixed-signal circuitry connected to the linear regulator's output, including the op-amp shown in Fig. 4.1, would be required to connect any PFET body terminals to the substrate. The result is a significant body effect for all PFETs in the system except for the pass transistor. The increased threshold voltage from the body effect led to the PFET pass transistor not being a viable option for the Vulcan II linear regulator.

Proceeding with an NFET pass transistor, the next design step was to size it such that 100-mA of continuous load current could be provided for the various simulation corners. To determine the necessary size of the NFET under worst-case performance, the typical NFET and typical PFET (TT) model corner binned at 25 ºC was selected. A safety margin was added to the design such that the NFET provided for a load current of at least 150 mA with a V_{DS} of 4 V, corresponding to an input voltage of 19 V when using the level shifter formed by R_{LS0}, MN2, and R_{LS1} in Fig. 4.1.

The simulation results for the V_{DS} versus load current are shown in Fig. 4.2 for six different effective (W/L) values. The (W/L) = 58,333 curve satisfied the safety margin imposed on the

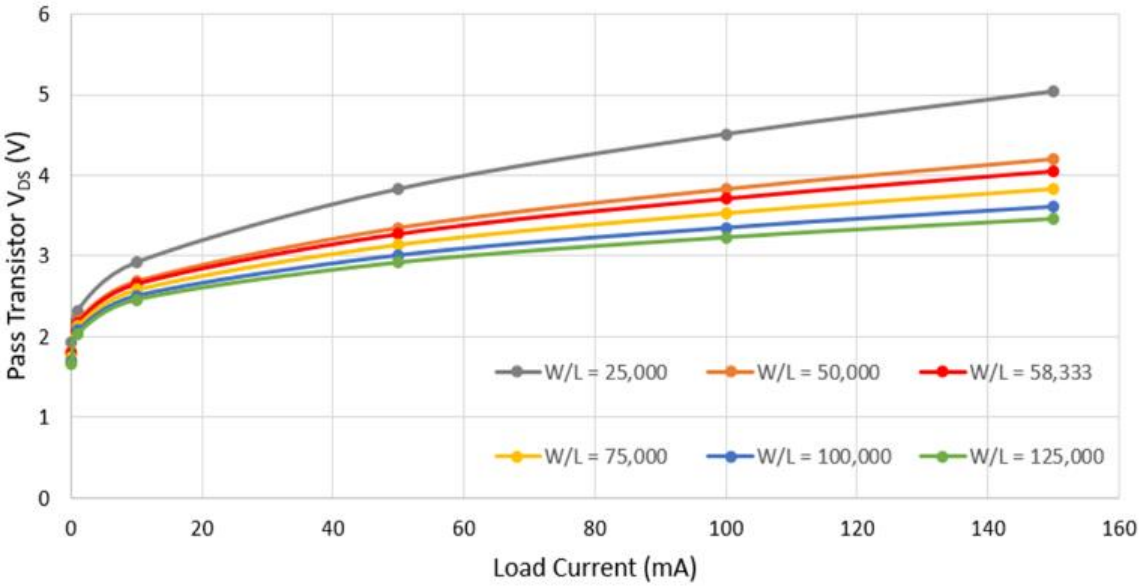

Fig. 4.2. The V_{DS} vs. I_{LOAD} at 25 ºC (TT) for various pass transistor (W/L) values.

design, therefore an effective (W/L) of 70,000 µm / 1.2 µm was selected for the NFET pass transistor. The final layout of the device was segmented into a 25 by 50 array of (W/L) = 56 µm / 1.2 µm devices, allowing for a compact pass transistor footprint while retaining the effective (W/L).

Concerns regarding the potential yield of circuitry in Vulcan II motivated the selection of the op-amp. The two-stage op-amp fabricated in Vulcan I had been successfully tested and was reported in [31]. Therefore, it was deemed to be a low risk implementation in Vulcan II and was selected for use in the linear regulator. The schematic of the two-stage op-amp is provided in Fig. 4.2. Note that the reference voltage (VINN) was set to 7.5 V and the bias voltage was 4.5 V in this design. In addition, as shown in Fig. 4.1, the op-amp utilizes the linear regulator's output as its supply voltage. Load transients change the op-amp's gain momentarily while the regulator's feedback loop reacts, but the effect is minimal for the rated maximum current of 100 mA or less.

Due to the op-amp's maximum output voltage being limited to a $V_{DS,SAT}$ drop below its positive supply rail (the linear regulator's output), the NFET pass transistor could not be placed in

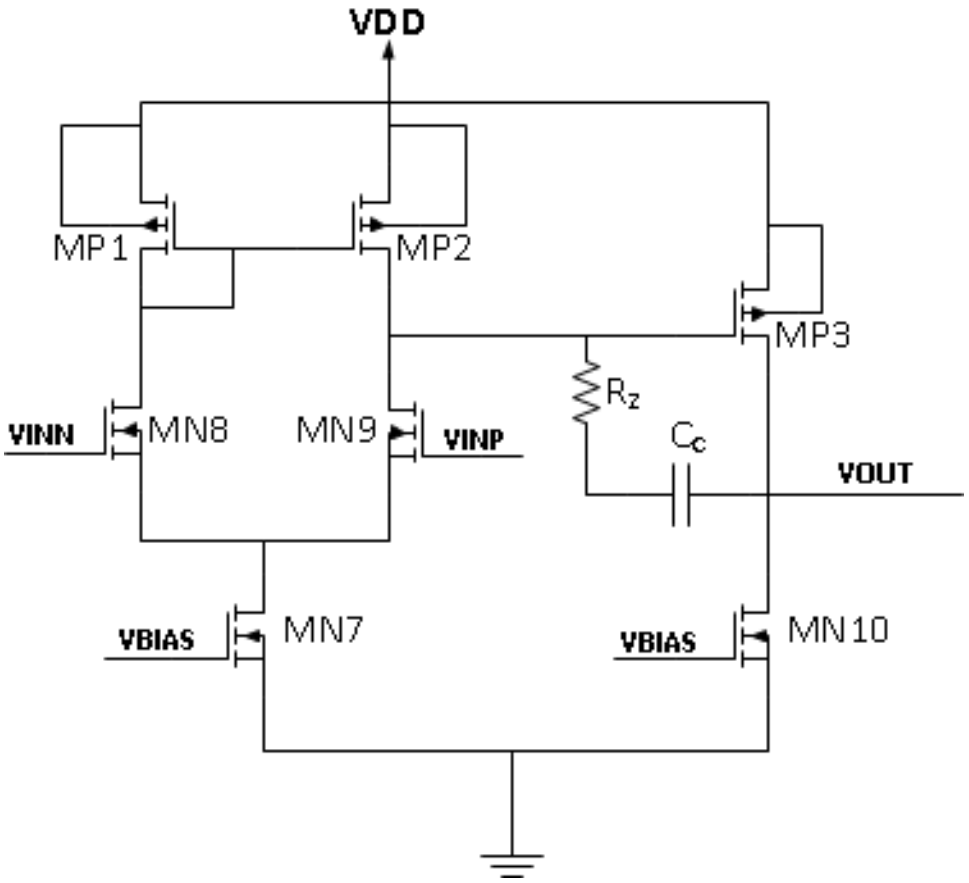

Fig. 4.3. The schematic of the two-stage op-amp used in the Vulcan II linear regulator.

the saturation region by directly connecting its gate to the op-amp's output. A level shifting network formed by R_{LS0}, R_{LS1}, and MN2 as shown in Fig. 4.1 was necessary to provide a V_{GS} suitable for turning on the pass device MN1. With the level shifting network, the maximum V_{GS} of the linear regulator is limited only by the difference between the input and output voltages. However, the common source configuration of the level shifter consists of a source degeneration resistor (R_{LS1}) and impacts the system gain as given by (4.3).

$$\boldsymbol{A_{LS}} = \frac{-(\boldsymbol{g_{m,MN2}})(\boldsymbol{R_{LS0}})}{\mathbf{1}+(\boldsymbol{g_{m,MN2}})(\boldsymbol{R_{LS1}})} \tag{4.3}$$

The linear regulator schematic in Fig. 4.1 and its op-amp schematic in Fig. 4.2 can be analyzed to determine the linear regulator's change in load current as expressed by (4.4). The open-

loop gain of the two-stage op-amp, or error amplifier, denoted as $A_{EA,OL}$ follows the analysis provided in Chapter 3 and is given in (4.5).

$$\mathbf{\Delta I}_{LOAD} = (A_{PassFET})(A_{LS})(A_{EA})(\frac{R_{F2}}{R_{F1}+R_{F2}})(\mathbf{\Delta V}_{OUT})(\frac{1}{R_{o,pass}}) \quad (4.4)$$

$$A_{EA,OL} = (g_{m,MN9})(r_{o,MN9}//r_{o,MP2})(g_{m,MP3})(r_{o,MN10}//r_{o,MP3}) \quad (4.5)$$

The compensation network given in Fig. 4.1 forms a resistance, denoted as R_{MIRROR}, which varies with the frequency of an AC disturbance. The result of the compensation is a resistance between the op-amp's output and ground. Modifying the open-loop gain given by (4.5) to account for the compensation results in (4.6), where the closed-loop gain is denoted as $A_{EA,CL}$ and is specific to this linear regulator configuration.

$$A_{EA,CL} = (g_{m,MN9})(r_{o,MN9}//r_{o,MP2})(g_{m,MP3})(r_{o,MN10}//r_{o,MP3}//R_{MIRROR}) \quad (4.6)$$

The open-loop gain of the linear regulator can then be determined by (4.7).

$$A_{OL,REG} = (A_{PassFET})(A_{LS})(A_{EA,CL})(\frac{R_{F2}}{R_{F1}+R_{F2}}) \quad (4.7)$$

From (4.6) and (4.7), it can be determined that the resistance due to the compensation network decreases the open loop gain of not only the op-amp but also of the linear regulator. This results in a slightly higher load regulation value, which is expressed as.

$$\textbf{Load Regulation} = \frac{\mathbf{\Delta V}_{OUT}}{\mathbf{\Delta I}_{LOAD}} = \frac{R_{o,pass}}{(A_{PassFET})(A_{LS})(A_{EA,CL})(\frac{R_{F2}}{R_{F1}+R_{F2}})} \quad (4.8)$$

The derivation of the Vulcan II linear regulator's line regulation follows the same approach given in Chapter 3 and is expressed as (4.9).

$$\textbf{Line Regulation} \approx \frac{\Delta V_{OUT}}{\Delta V_{IN}} = \frac{1}{R_{ds,pass}+R_{LOAD}} * \frac{R_{o,pass}}{(A_{PassFET})(A_{LS})(A_{EA,CL})(\frac{R_{F2}}{R_{F1}+R_{F2}})} \quad (4.9)$$

Proceeding to the frequency analysis of the linear regulator, the wide range of operating conditions presents multiple design challenges related to stability. For example, the threshold

voltage of NFETs was found to vary from approximately 1.5 V at 300 ºC up to 2.5 V at 25 ºC. The PFETs were more extreme with a threshold voltage range of about 2.5 V at 300 ºC to 5 V at 25 ºC. It follows from the large range of threshold voltages that g_m and r_o values will likewise vary substantially over temperature.

In addition, conventional linear regulators form a dominant pole with a large output capacitor to ensure system stability. Material constraints have limited commercially available capacitors to maximum temperature ratings of approximately 250 ºC, beyond which the dielectric performance begins to degrade [59]. Specialized high temperature ceramic capacitors are available with temperature ratings of above 250 ºC, but they must be ordered directly from the manufacturer and performance over temperature is not readily available. The capacitance for a given package size also decreases substantially for ceramic capacitors with greater maximum temperature ratings.

The compensation scheme for the Vulcan II linear regulator was developed to minimize the system footprint while still retaining the ability to provide for fast transient loads. This was accomplished by shifting the dominant pole to the op-amp's output rather than the linear regulator's output. The design process was influenced by a silicon based external capacitor-less LDO presented in [60]. The core of the compensation scheme in Fig. 4.1 consists of MN3 – MN6, R_{BIAS}, R_{COMP}, and C_{COMP}. The components form a differentiator and allow for creating a dominant pole without relying on the output capacitor. The differentiator senses the changes on the output and dynamically alters the resistance connected to the output of the op-amp (i.e. MN3 – MN6) to vary its gain. At higher frequencies, R_{OTA} and C_{OTA} will also play a role by lowering the output resistance of the op-amp and causing a subsequent decrease in gain.

The dominant pole of the linear regulator can be approximated by (4.10).

$$f_{p1} \cong \frac{1}{2\pi(g_{MN9})(r_{o,MN8}//r_{o,MP2})(g_{MP3})(r_{o,MN10}//r_{o,MP3})(g_{MN6})(C_{COMP})(R_{COMP})} \quad (4.10)$$

The location of the pole is dependent upon C_{OTA} not exceeding approximately 10 nF since the value of R_{OTA} selected is 400 Ohms. Increasing the value of C_{OTA} results in a low resistance path from the op-amp's output to ground at proportionally lower frequencies. The system's gain would therefore roll-off at lower frequencies and change the expression for the pole's location.

The intent of the compensation network was to allow the linear regulator to have a frequency response similar to a single-pole system. As discussed in Chapter 3, a single-pole system results in a phase margin approaching 90º which produces a stable but relatively slow response to load transients. For this application, a phase margin of at least 45º over all corners was deemed to be sufficient for minimizing the risk of instability. The subsequent poles and zeroes are given by equations (4.11) to (4.14), where R_{MIRROR} in (4.14) denotes the resistance to ground formed by MN3 and MN5.

$$f_{z1} \cong \frac{1}{2\pi(g_{MN6})(C_{COMP})(R_{COMP})} \quad (4.11)$$

$$f_{p2} \cong \frac{(g_{MN6})(g_{MP3})}{2\pi(C_C)} \quad (4.12)$$

$$f_{z2} \cong \frac{g_{MN2}}{2\pi(C_C)} \quad (4.13)$$

$$f_{p3} \cong \frac{(g_{MN2})(R_{ESR}//R_{DS,MN1})(R_{OTA}//R_{MIRROR})}{2\pi(C_{G,MN1})(R_{LOAD}//(R_{(F1)}+R_{(F2)}))(g_{MN1})} \quad (4.14)$$

The combination of two poles and two zeroes effectively cancels out with the appropriate selection of component values. A phase margin of 90º is unlikely due to the locations being approximations and other high frequency poles existing within the system. However, a phase margin of at least 45º over the operating temperature range is achieved with the linear regulator configuration given in Fig. 4.1 and the device sizes provided in Table 4.1.

Another takeaway from the expressions for the locations of each pole and zero is that the load capacitance does not play a central role. The load capacitance does influence a pole located at relatively high frequencies and can reduce phase margin. This occurs if the regulator is operating at the lower end of the input voltage range (e.g. 20 V) and the load capacitance is on the order of several hundred nanofarads.

Although an on-chip load capacitance of only a few pF can be used while maintaining stability, there are two essential caveats. The first is that the linear regulator still requires capacitors in the nanofarad range. Specifically, C_{COMP} and C_{OTA} were designed to be 1.5 nF and 6.8 nF, respectively. This means that the capacitors are too large to be located on-chip unless a significant amount of die area is used.

The second caveat is that the Vulcan II linear regulator is intended for general purpose use and the targeted application will determine the amount of load capacitance required. For example, an on-chip load capacitance of 10 pF will not be able to provide for a 100 mA load transient lasting 100 ns. A significant undershoot will occur on the regulator's output voltage in this example, because there is nothing to provide for the load transient while the feedback loop attempts to react.

The sizing of the components used in the Vulcan II linear regulator is provided in Table 4.1. Note that "m" stands for the number of fingers for FETs. In addition, R_{ZERO} and C_{ZERO} do not impact the design and the intent was to provide a probe point at the gate of the pass transistor. $C_{FEEDBACK}$ was made to be 1 pF to provide a small amount of protection against noise at the op-amp's non-inverting input. Finally, the values of C_{IN} and C_{LOAD} are not listed in Table 4.1. For commercial linear regulators, a 1 µF capacitor is typically used as the C_{IN}. The C_{LOAD} is application dependent, although the testing results in Chapter 5 use a C_{LOAD} of 940 nF unless otherwise noted.

Table 4.1. Component sizing for the Vulcan II linear regulator.

Component	Device Size	Comment
MN1	20 µm / 1.2 µm (m = 3,500)	Pass transistor
MN2	20 µm / 2 µm (m = 200)	Level shifting network
MN3 – MN6	20 µm / 2 µm (m = 200)	Compensation network
MN7	20 µm / 5 µm (m = 22)	Op-amp biasing (1^{st} stage)
MN8, MN9	20 µm / 2 µm (m = 7)	Op-amp input (1^{st} stage)
MN10	20 µm / 2 µm (m = 66)	Op-amp biasing (2^{nd} stage)
MP1, MP2	20 µm / 2 µm (m = 36)	Op-amp active loads (1^{st} stage)
MP3	20 µm / 2 µm (m = 224)	Op-amp CS amplifier (2^{nd} stage)
R_Z	7.7 kΩ	Op-amp compensation
C_C	2.2 pF	Op-amp compensation
R_{F1}, R_{F2}	28 kΩ	Sampling network
R_{BIAS}	20 kΩ	Compensation network biasing
R_{COMP}	2.5 kΩ	Compensation
C_{COMP}	1.5 nF	Compensation
R_{OTA}	400 Ω	Compensation
C_{OTA}	6.8 nF	Compensation
R_{LS0}	10 kΩ	Level shifting network
R_{LS1}	500 Ω	Level shifting network

4.1.1 Vulcan II Linear Regulator: Simulation Results and Test Setups

The testing results of the fabricated linear regulator were found to be closely predicted by the typical NFET, fast PFET (TF) model corner at each temperature. Unless otherwise noted, the simulation results presented in this section are based upon the TF model corner.

Table 4.2. The simulation results for the Vulcan II linear regulator.

Parameter	Test Condition	25 °C (TF Model)		100 °C (TF Model)		200 °C (TF Model)		300 °C (TF Model)	
		C_{LOAD} = 10 pF	C_{LOAD} = 940 nF	C_{LOAD} = 10 pF	C_{LOAD} = 940 nF	C_{LOAD} = 10 pF	C_{LOAD} = 940 nF	C_{LOAD} = 10 pF	C_{LOAD} = 940 nF
DC Loop Gain	I_{LOAD} = 100 mA, V_{IN} = 20 V	50.2 dB	50.2 dB	51.4 dB	51.4 dB	57.3 dB	57.3 dB	58.7 dB	58.7 dB
Phase Margin		71.0 °	50.8 °	81.5 °	68.4 °	82.1 °	67.8 °	83.4 °	63.1 °
Bandwidth		380 kHz	295 kHz	499 kHz	455 kHz	584 kHz	521 kHz	745 kHz	629 kHz
I_Q		3.2 mA	3.2 mA	4.0 mA	4.0 mA	4.3 mA	4.3 mA	4.2 mA	4.2 mA
PSRR	Frequency = 10 Hz, I_{LOAD} = 100 mA, V_{IN} = 20 V	54.5 dB	54.5 dB	56.3 dB	56.3 dB	57.1 dB	57.1 dB	58.3 dB	58.3 dB
Overshoot (ΔV_{OUT})	Full load transient (ΔI_{LOAD} = 100 mA), V_{IN} = 20 V	3.33 V	0.41 V	2.68 V	0.40 V	2.53 V	0.38 V	2.68 V	0.39 V
Undershoot (ΔV_{OUT})		3.89 V	0.47 V	3.09 V	0.50 V	3.14 V	0.50 V	3.32 V	0.50 V
Maximum Setting Time (99% of nominal V_{OUT})		0.7 µs	1.0 µs	1.2 µs	0.5 µs	1.2 µs	0.5 µs	1.1 µs	0.4 µs
Line Regulation	ΔV_{IN} = 20 V to 30 V, I_{LOAD} = 100 mA	3.1 mV/V	3.1 mV/V	2.6 mV/V	2.6 mV/V	2.2 mV/V	2.2 mV/V	1.9 mV/V	1.9 mV/V
Load Regulation	ΔI_{LOAD} = 100 mA, V_{IN} = 20 V	16 mV/A	16 mV/A	11 mV/A	11 mV/A	13 mV/A	13 mV/A	12 mV/A	12 mV/A

An overview of the simulation results is presented in Table 4.2. The Vulcan II linear regulator achieves a DC open-loop gain of over 50 dB between 25 ºC and 300 ºC while maintaining a bandwidth of at least 295 kHz over the temperature range. Similarly, the phase margin ranged between 50.8º and 82.1º over temperature. As pointed out in the previous section, a load capacitance on the order of hundreds of nanofarads introduces a pole near the unity gain frequency which results in a lower phase margin in the 940 nF load capacitance case than the 10 pF case.

The setup for testing the DC open-loop gain, bandwidth, and phase margin requires injecting an AC signal into the non-inverting terminal of the op-amp. It is essential to block the AC signal from the sampling network, thus a large AC resistance (i.e. a 1 H inductor) is required to be in series with the non-inverting terminal. In addition, the DC component should be blocked from interacting with the AC signal being injected. A large DC resistance (i.e. a 1 F capacitor) can be used for this configuration. The test configuration shown in Fig. 4.4 demonstrates how the AC simulations of the linear regulator were performed. In this case, R_{AC} is a large AC resistance such

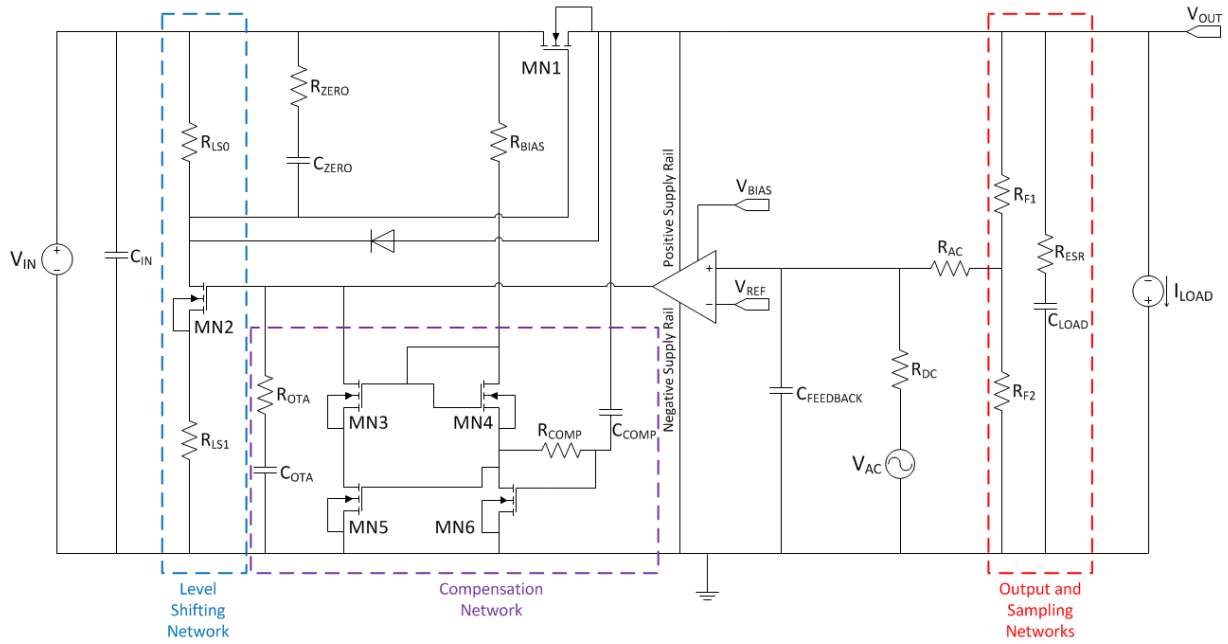

Fig. 4.4. The AC test configuration for the Vulcan II linear regulator.

as a 1 H inductor while R_{DC} is a large DC resistance such as a 1 F capacitor. The AC signal into the non-inverting terminal is injected by the AC source rather than the overall feedback loop.

In Table 4.2, the quiescent current is shown to range from a minimum of 3.2 mA at 25 ºC to a maximum of 4.3 mA at 200 ºC. The quiescent current of the linear regulator is function of the current consumption of the op-amp along with the compensation, level shifting, and sampling networks. The sampling network has large resistances and accounts for a small percentage of the quiescent current. The level shifting and compensation networks consist of relatively low resistance paths to ground, which lead to quiescent currents nearly equal to the op-amp. Lowering the quiescent current requires altering the op-amp or either of the two networks, each of which impacts the regulator's frequency response.

The test setup for PSRR requires placing an AC source in series with the DC supply as shown in Fig. 4.5. The AC signal to the non-inverting terminal of the error amplifier is blocked with a large AC resistance in this configuration, which allows for obtaining the power supply gain

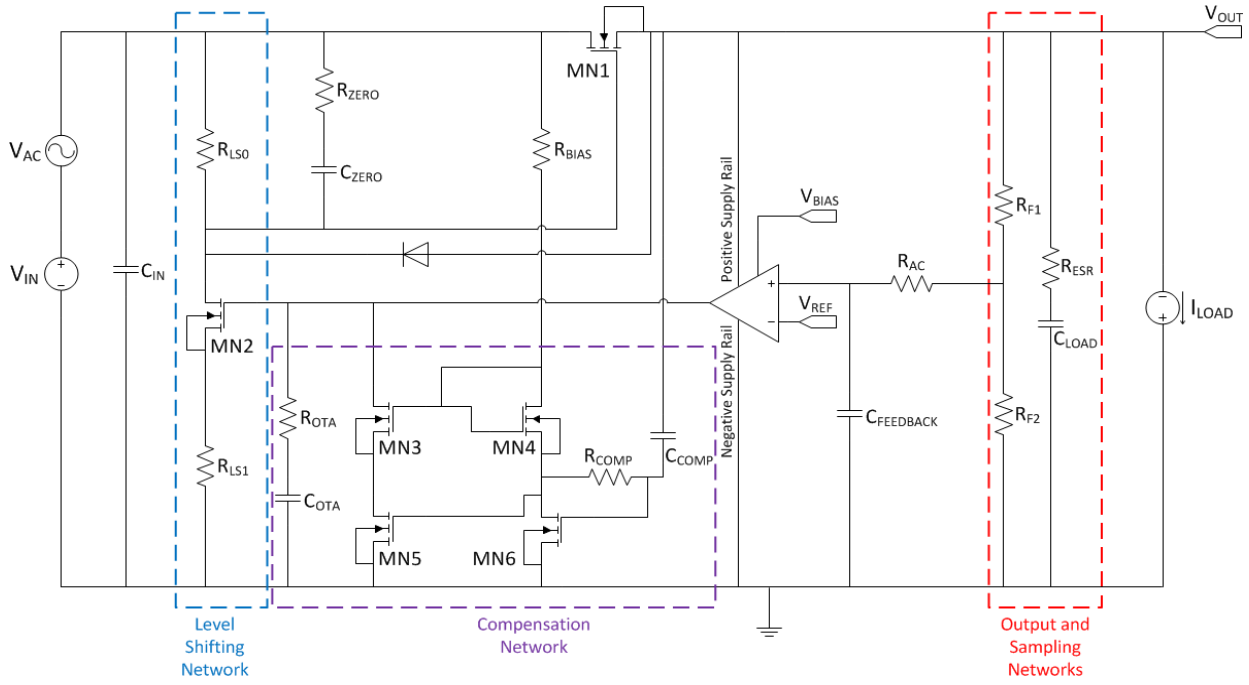

Fig. 4.5. The test configuration used to determine the Vulcan II linear regulator's power supply gain.

over frequency. To obtain the PSRR value, the supply gain is subtracted from the linear regulator's open-loop gain. The simulated PSRR values of at least 50 dB at 1 kHz, as provided by Table 4.2, show that the regulator can adequately reject supply noise at low frequencies. The PSRR values versus frequency at 300 ºC (TF) are shown in Fig. 4.6 for multiple combinations of input voltages and load currents. Similar trends occur at lower temperatures, albeit with slightly lower PSRR values due to the decrease in open-loop gain.

The undershoot and overshoot voltages provided in Table 4.2 for a sudden no-load to full-load transient follow the expectations that performance will suffer significantly with a smaller load capacitor. Although the regulator is able to settle to within 1% of its nominal output voltage in less than 1.2 µs in each test case, a 10 pF load capacitor results in an output swing of up to 26%. This could lead to mixed-signal circuitry on the output going into a failure or reset mode, making a 10 pF load capacitance undesirable for general-purpose applications despite minimizing system footprint.

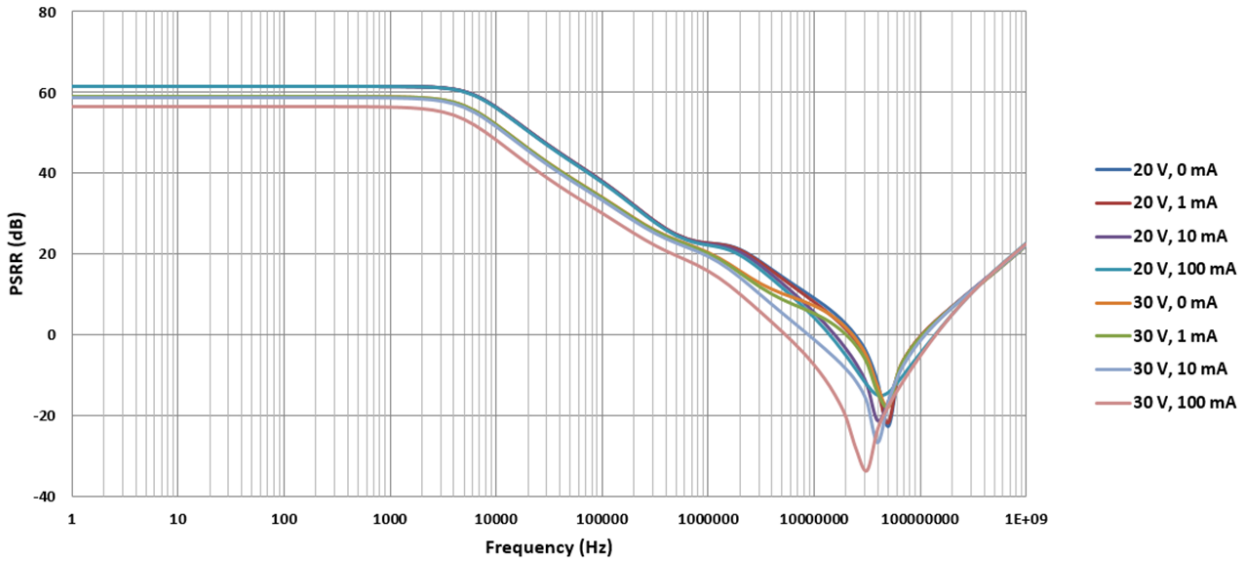

Fig. 4.6. The PSRR simulation results of the Vulcan II linear regulator at 300 ºC.

The line and load regulation values perform exceptionally well compared to silicon based linear regulators, particularly given the developing nature of SiC CMOS technology. As an example, the datasheet for Texas Instrument's LM78LXX family of LDOs reports a typical line regulation of 1.38 mV/V at 25 ºC for an input voltage increase from 7 V to 20 V [61]. A line regulation of between 1.9 mV/V to 3.1 mV/V is achieved in the Vulcan II linear regulator over the operating temperature range.

The same LM78LXX product line also has a reported typical load regulation of 0.2 mV/mA for a load changing from 1 mA to 100 mA at 25 ºC. Referring to Table 4.2, the load regulation when stated in the same units is 0.011 mV/mA to 0.016 mV/mA over the temperature range. The load regulation provided in Table 4.2 is also for a full-load swing, whereas the LM78LXX datasheet is already conducting 1 mA before transitioning to its full-load condition. It is important to note that the datasheet reports measured results, thus a more complete comparison will also need to involve the data that will be presented Chapter 5.

4.2 Fully On-Chip Linear Regulators

For high temperature applications, one notable design constraint is the availability of discrete capacitors capable of enduring the harsh operating environment. Capacitors able to withstand up to 280 ºC have been reported in [43]. Specialty manufacturers currently offer capacitors with dielectric materials that are stated to operate up to approximately 350 ºC, although the performance over temperature and reliability information are not publicly available at the time of this writing. The intent of this work is to provide a fully on-chip linear regulator solution that eliminates the dependence on an external capacitor while still providing stability for all operating conditions.

With respect to off-the-shelf linear regulators, an external output capacitor of 1 μF or more is generally relied upon to provide for sudden transient loads while the regulator reacts. A fully-on chip solution must limit its on-chip load capacitance based on the amount of die area available, which typically constrains the capacitor size to no more than the single digit nanofarad range. Due to the output capacitance limitation, the regulator's bandwidth is ideally made as large as possible to quickly counter $I = C(dv/dt)$ effects.

Improving the regulator's bandwidth significantly requires replacing the two-stage op-amp utilized in the Vulcan II linear regulator. In the following sections, multiple op-amps will be designed and evaluated in simulation. A comparison of the op-amps will be provided and the linear regulator's performance with the selected op-amp will be analyzed. The design specifications for the linear regulator will limit the op-amp to a total current consumption of approximately 1.5 mA. Note that for high performance applications, a larger power budget will enable the regulator to achieve greater bandwidths. Similarly, implementing two separate op-amps in parallel as suggested in [62] can lead to relatively high bandwidths while also providing a large DC gain.

4.2.1 Operational Amplifiers

To provide a consistent basis for design, each of the op-amps presented in this section targets a total current consumption of approximately 1.5 mA and a phase margin of 70º at 300 ºC (TF) with a 3 V common-mode voltage. The current consumption requirement is driven by stand-alone high temperature applications with limited amounts of power available. The phase margin of 70º corresponds to a relatively fast transient response with a small amount of undershoot/overshoot. It also provides a large safety margin for avoiding instability due to process variation or from process parameter (e.g. threshold voltage) changes over the operating temperature range. The choice to use a 3 V common-mode input voltage was made due to the bandgap reference that will be utilized by fabricated circuits, which will provide a reference voltage of approximately 3 V. In addition, each of the op-amps are internally biased and a capacitive load of 4.5 pF is added to each op-amp's test bench.

4.2.1.1 Two-Stage Op-Amp

The conventional two-stage op-amp consisting of an NFET input pair, shown in Fig. 3.3, will be operating on the edge of its input common mode range (V_{ICMR}) with a common-mode voltage (V_{CM}) of 3 V. Implementing a PFET input pair along with the NFET input pair similar to Fig. 3.4 allows for a rail-to-rail V_{ICMR}. The schematic shown in Fig. 4.7 modifies the rail-to-rail op-amp design presented in Fig. 3.4 to enable internal biasing. The biasing scheme uses the V_{GS} (or V_{SG}) drops from MN1 – MN3 and MP1 to provide a suitable bias voltage to gates within the core of the op-amp. For example, "VBIAS_N1" is a single V_{GS} drop from MN2 and is used for MN12 and MN15 that have gate potentials of one V_{GS} drop above ground. The bias current is primarily a function of R_{IBIAS}, thus R_{IBIAS} should have the lowest possible temperature coefficient.

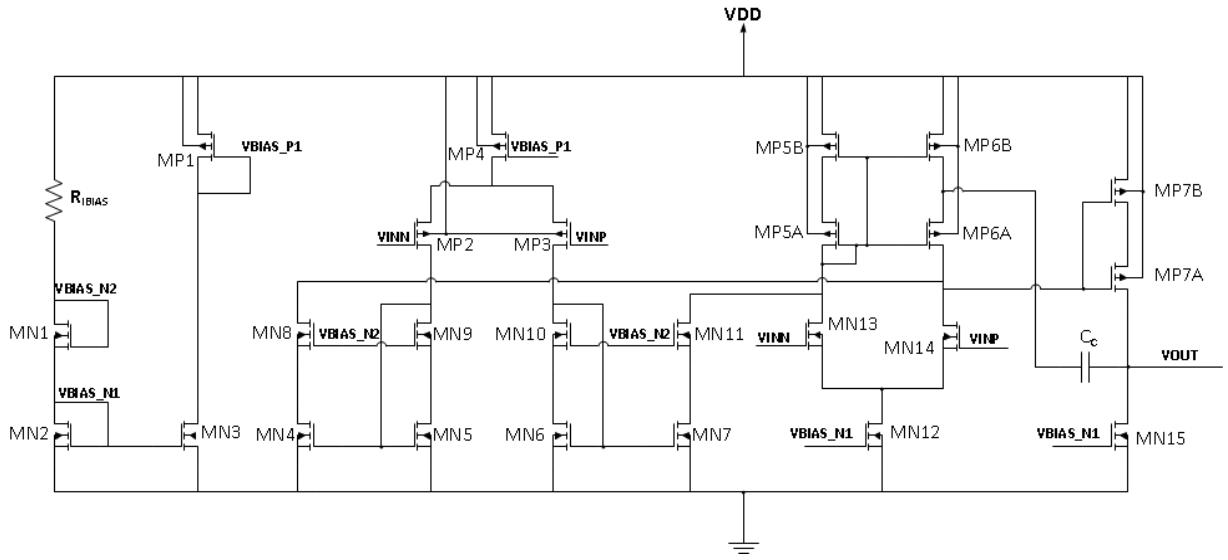

Fig. 4.7. The rail-to-rail two-stage op-amp schematic with indirect compensation.

An indirect compensation scheme is used such that the compensation capacitor C_C is connected between the op-amp's output and the source of MP6A to avoid a right-half plane (RHP) zero without relying on a nulling resistor [63]. Referring back to Fig. 3.2, the RHP zero is a result of the compensation capacitor C_C and the gate-drain capacitance of M7A ($C_{GD,M7}$) forming a feedforward path from the differential amplifier output (1st stage) to the op-amp's output (2nd stage) node. Since C_C and $C_{GD,M7}$ are feeding forward current and adding energy to the output of the op-amp while also inverting the polarity of the op-amp's output, there is a RHP zero formed. By using the indirect compensation approach shown in Fig. 4.7, the feedforward current path is blocked but the output can still feed back to the input. This eliminates the RHP zero and causes the unity gain frequency to increase since MN14's drain is no longer loaded by C_C.

Table 4.3 lists the device sizing for the two-stage op-amp shown in Fig. 4.7. As required by the specifications, the design achieves a total current consumption of 1.5 mA and a phase margin of approximately 70º at 300 ºC (TF). The simulated open-loop frequency response of the op-amp over temperature for a 3 V common-mode voltage is provided in Fig. 4.8.

Table 4.3. The device sizes for the two-stage op-amp shown in Fig. 4.7.

Component	Device Size	Comment
MN1 – MN11, MN13 - MN15	20 µm / 1.2 µm (m = 16)	Biasing, differential amplifiers, output stage
MN12	20 µm / 1.2 µm (m = 32)	NFET differential amplifier biasing
MP1 – MP3	20 µm / 1.2 µm (m = 64)	Biasing, PFET differential amplifier
MP4 – MP7	20 µm / 1.2 µm (m = 128)	Differential amplifiers biasing and active loads, output stage
R_{IBIAS}	110 kΩ	Biasing
C_C	60 pF	Compensation capacitor

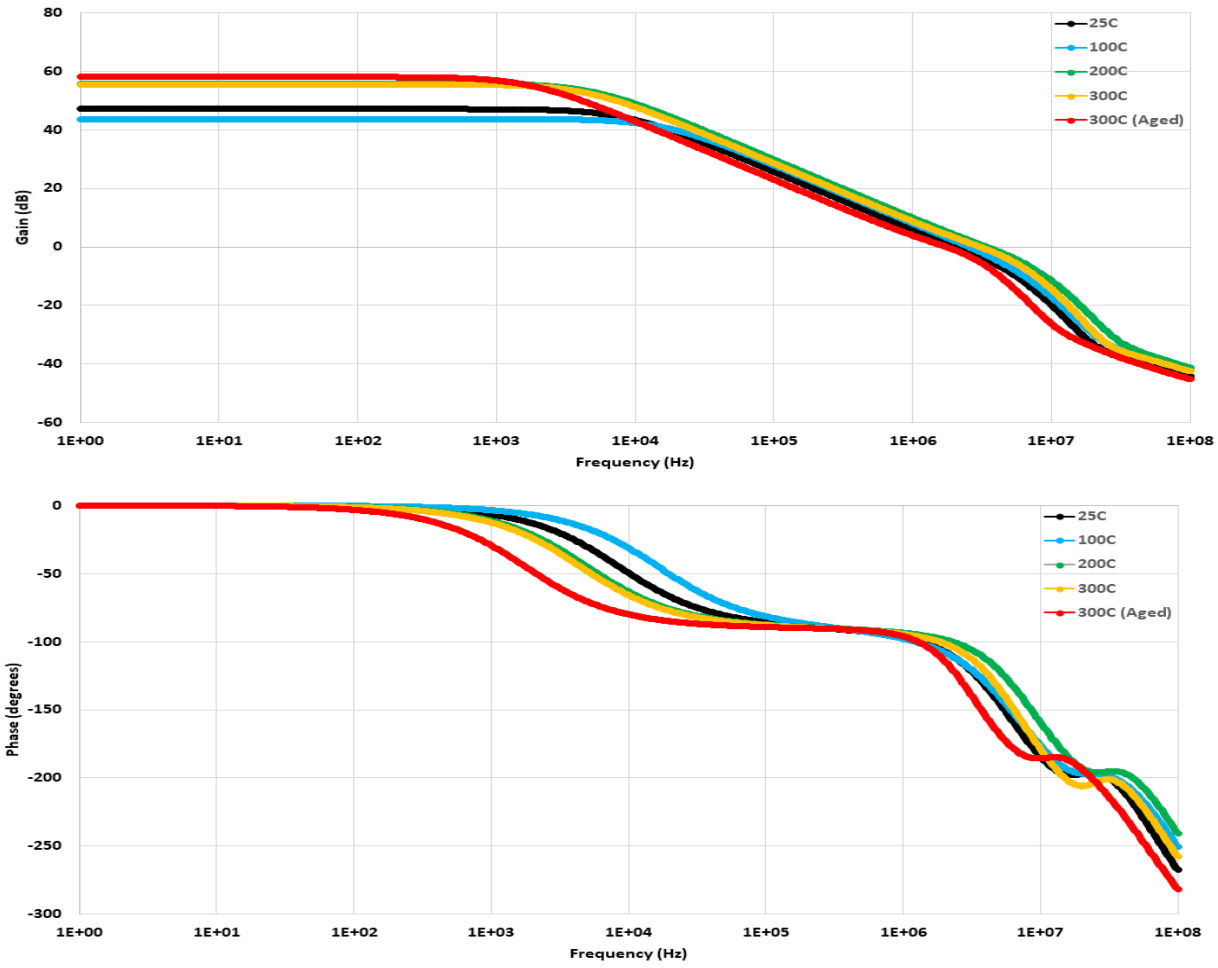

Fig. 4.8. The frequency response of the two-stage op-amp shown in Fig. 4.7.

A summary of the frequency response parameters including open-loop gain, phase margin (PM), and unity-gain bandwidth (UGBW) over temperature and for a V_{ICMR} of 0 V to 15 V is

presented in Fig. 4.9. The NFET and PFET input pairs allow for a common-mode input voltage range spanning from approximately 0 V to 11 V over temperature, with the 300 ºC (TT) aged

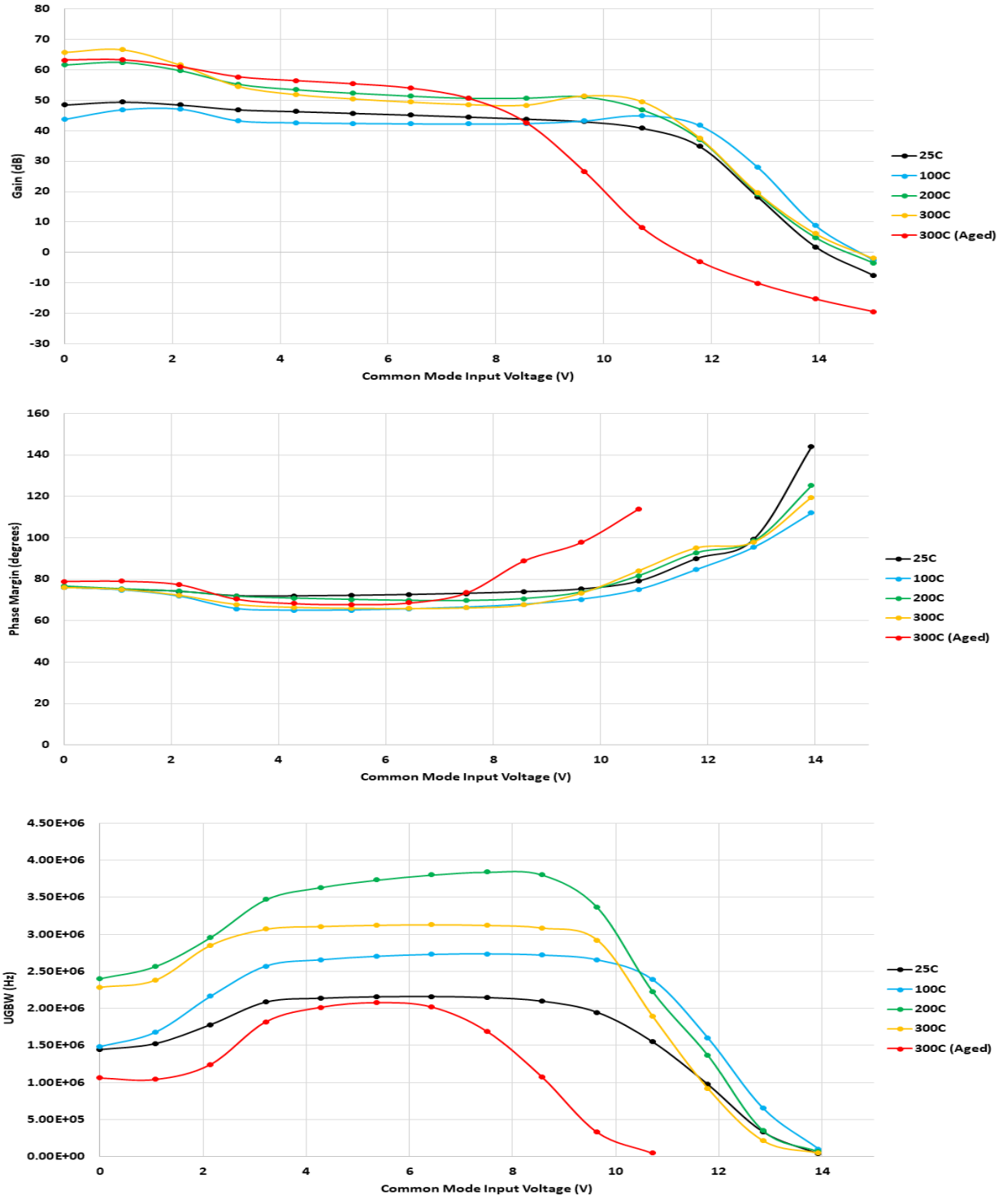

Fig. 4.9. The open-loop DC gain, PM, and UGBW over temperature and a 0-15 V common mode input voltage for the two-stage op-amp with indirect compensation in Fig. 4.7.

models being more limited at 0 V to 9 V. The open-loop DC gain ranges between 43 dB and 67 dB over temperature, with 200 ºC and 300 ºC offering the best performance. This indicates that stacking PFETs and cascoding NFETs (e.g. MN4 – MN11) result in V_{DS} drops that approach the supply voltage at lower temperatures where threshold voltages are generally higher. While the aged NFETs do not have an appreciably higher threshold voltage at 300 ºC (TT) than for unaged NFETs, the aged PFETs threshold nearly doubles compared to the unaged PFETs at 300 ºC. Due to the FETs dropping out of saturation at lower input voltages, the V_{ICMR} is limited along with the gain for the 300 ºC (TT) model.

The UGBW of the op-amp peaks in the middle of the common-mode input voltage range with 200 ºC and 300 ºC providing up to 3.13 MHz and 3.84 MHz, respectively. The PM remains consistent at approximately 70º within the V_{ICMR} for each temperature, which achieves the design goal. A PM of 70º yields a transient response that does not produce significant undershoot/overshoot voltages due to a nearly overdamped nature. To illustrate this point, Fig. 4.10 shows the transient response of the op-amp in a unity-gain buffer configuration at 300 ºC for a 50-mV step input and a load capacitance of 4.5 pF.

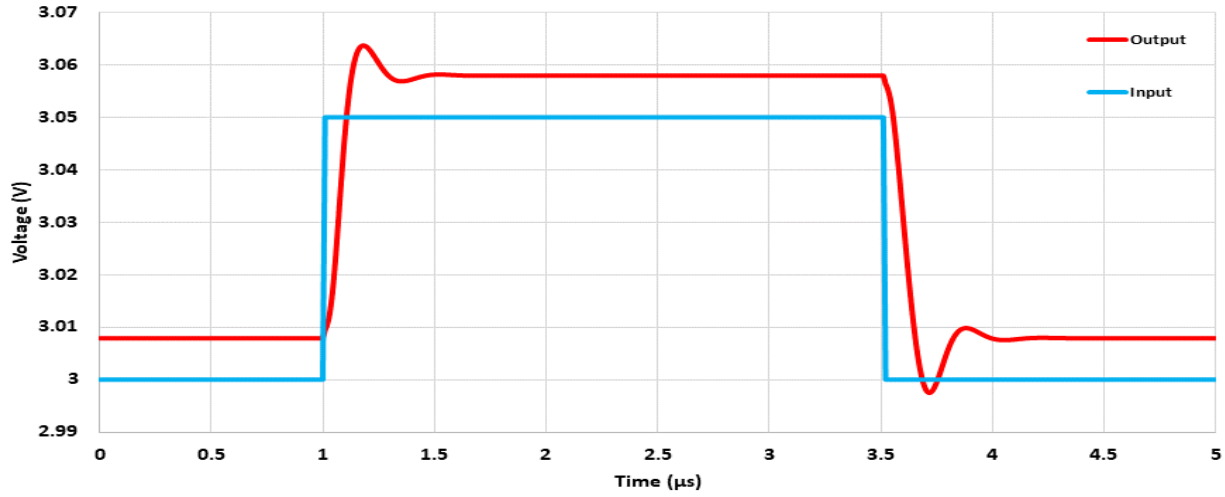

Fig. 4.10. The transient response of the two-stage op-amp shown in Fig. 4.7 driving a 4.5 pF load at 300 ºC (TF) for a 50 mV step input in a unity-gain configuration.

A systematic offset of approximately 7.9 mV is present due to the NFETs and PFETs not sinking/sourcing exactly the same amount of current. While the sizing can be adjusted for one temperature to nearly eliminate the systematic offset in simulations, it does not necessarily hold for another temperature. In addition, the random offset in a fabricated device will ultimately lead to some mismatch in the drive strength of the NFETs and PFETs.

The 1% settling time (for the rising edge) of 0.40 μs in Fig. 4.10 closely matches with the simulated UGBW of approximately 3 MHz at 300 ºC. Note that the 1% settling time denotes the time taken to transition from the steady-state output of 3.008 V (accounting for offset) to within approximately 0.5 mV of its output after the 50 mV step input. The falling edge of the output is dependent on the slew rate of the op-amp. The undershoot while the output is being pulled down is the result of the PFET in the 2nd stage (MP7) being shut off during slewing followed by being pulled up to the quiescent value once both inputs are the same voltage. The amount of time it takes MP7 to go from being turned off to being pulled back up to the quiescent gate voltage results in the brief undershoot of approximately 10 mV.

The fall time and undershoot can be reduced by increasing the size of the 2nd stage NFET (MN15) at the expense of added power consumption or decreasing C_C at the risk of instability. The relationship between slew rate and the 2nd stage NFET size as well as the value of C_C can be expressed as (4.15).

$$\boldsymbol{Slew\ Rate} = \frac{\boldsymbol{I_{D,MN15}}}{\boldsymbol{C_C}} \tag{4.15}$$

Increasing the NFET size will result in more quiescent current flowing through the 2nd stage, but forms a lower resistance path to ground that the output can discharge through. The slew rate is also inversely proportional to C_C since a smaller capacitance is discharged faster. Altering

either the NFET size or C_C will result in a different frequency response. A larger NFET increases systematic offset as the drive strength of the output stage's NFET and PFET begin to differ more.

While the rising edge of the op-amp's transient response in Fig. 4.10 is stable, the frequency response yielded a PM of 70º which should have almost no overshoot. This is a problem exclusive to the unity-gain configuration when the indirect compensation technique is used. The issue is also present in other op-amp topologies and is due to the impedance of C_C decreasing towards the $1/g_m$ value of MP6A. However, using a conventional compensation technique as shown in Fig. 3.2 where C_C and a nulling resistor are connected between the 1st stage and 2nd stage outputs results in the expected transient response that is nearly critically damped. In order to form a basis for comparison with other op-amp topologies, Fig. 4.11 shows the transient response of the op-amp in a non-inverting configuration with a closed-loop gain of two and a 50 mV step input at 300 ºC. In this case, the 1% settling time is 0.52 µs.

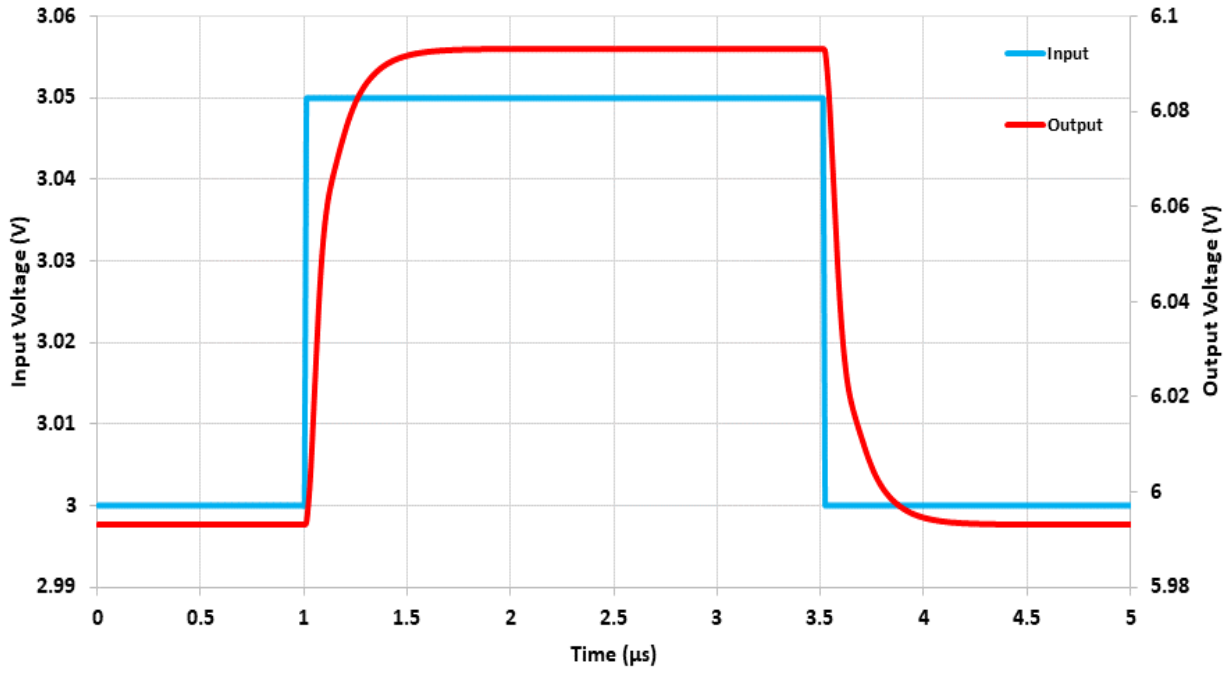

Fig. 4.11. The transient response of the two-stage op-amp driving a 4.5 pF load at 300 ºC (TF) for a 50 mV step input in a non-inverting configuration.

4.2.1.2 Telescopic Op-Amp

A modified version of the telescopic op-amp discussed in Chapter 3 (Section 3.1.1.3) is shown in Fig. 4.12. The schematic includes an output stage and utilizes the indirect compensation technique. Rather than connecting C_C between split-length devices, as in Fig. 4.7 with MP6A and MP6B, it is connected between cascoded PFETs. However, the advantage of the method remains the same since the node formed by the drain of MP5 and the source of MP7 is still low-impedance as with the split-length devices.

The goal of this compensation technique, as stated in the previous section, is to avoid a RHP zero created in the case where C_C is connected between the 1st stage output and the 2nd stage output. Although a nulling resistor can be used to shift the RHP zero to the LHP if C_C is connected between the output of each stage, the resistance value is subject to process variation, shifts over temperature, and even aging effects at higher temperatures. A resistance changing substantially can lead to instability. In the case of indirect compensation, the value of C_C is more stable since capacitors in the HiTSiC® process typically have less process variation and shift over temperature.

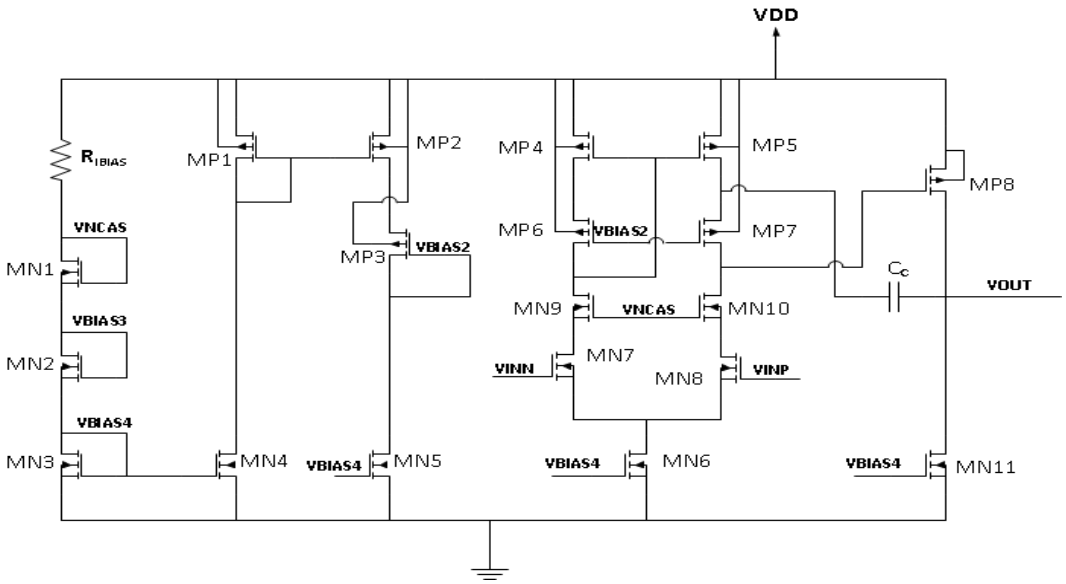

Fig. 4.12. The telescopic op-amp schematic with an output stage and indirect compensation.

Table 4.4. The device sizes for the telescopic op-amp shown in Fig. 4.12.

Component	Device Size	Comment
MN1 – MN5, MN7 – MN11	20 µm / 1.2 µm (m = 16)	Biasing, differential amplifiers, output stage
MN6	20 µm / 1.2 µm (m = 32)	NFET differential amplifier biasing
MP1 – MP8	20 µm / 1.2 µm (m = 128)	All PFETs
R_{IBIAS}	35 kΩ	Biasing
C_C	21 pF	Compensation capacitor

The device sizes listed in Table 4.4 are for the telescopic op-amp shown in Fig. 4.12. As with the two-stage op-amp presented in the previous section, the design targets a total current consumption of 1.5 mA and a phase margin of approximately 70º at 300 ºC (TF). The simulated open-loop frequency response of the telescopic op-amp over temperature and for a 3 V common-mode voltage is shown in Fig. 4.13. The open-loop DC gain of the telescopic op-amp steadily trends downwards with temperature, with the maximum of 78 dB occurring at 300 ºC (TF) and the minimum of 63 dB at 25 ºC.

The output stage of the telescopic op-amp allows its gain to outperform its two-stage counterpart. A single stage telescopic op-amp, however, is limited with regards to gain as stated in Table 3.1. The overall frequency response of the two-stage telescopic op-amp is representative of a typical single pole system similar to the two-stage op-amp using indirect compensation. A large value of C_C can therefore be used to create a dominant pole while forcing the second pole well beyond the unity-gain frequency.

The open-loop DC gain, PM, and UGBW over temperature and for a 0 to 15 V common mode input voltage are shown in Fig. 4.14. The DC gain is at 40 dB or above from approximately 2 V to 9 V for each temperature, which is to be expected for an NFET input pair. Within the V_{ICMR},

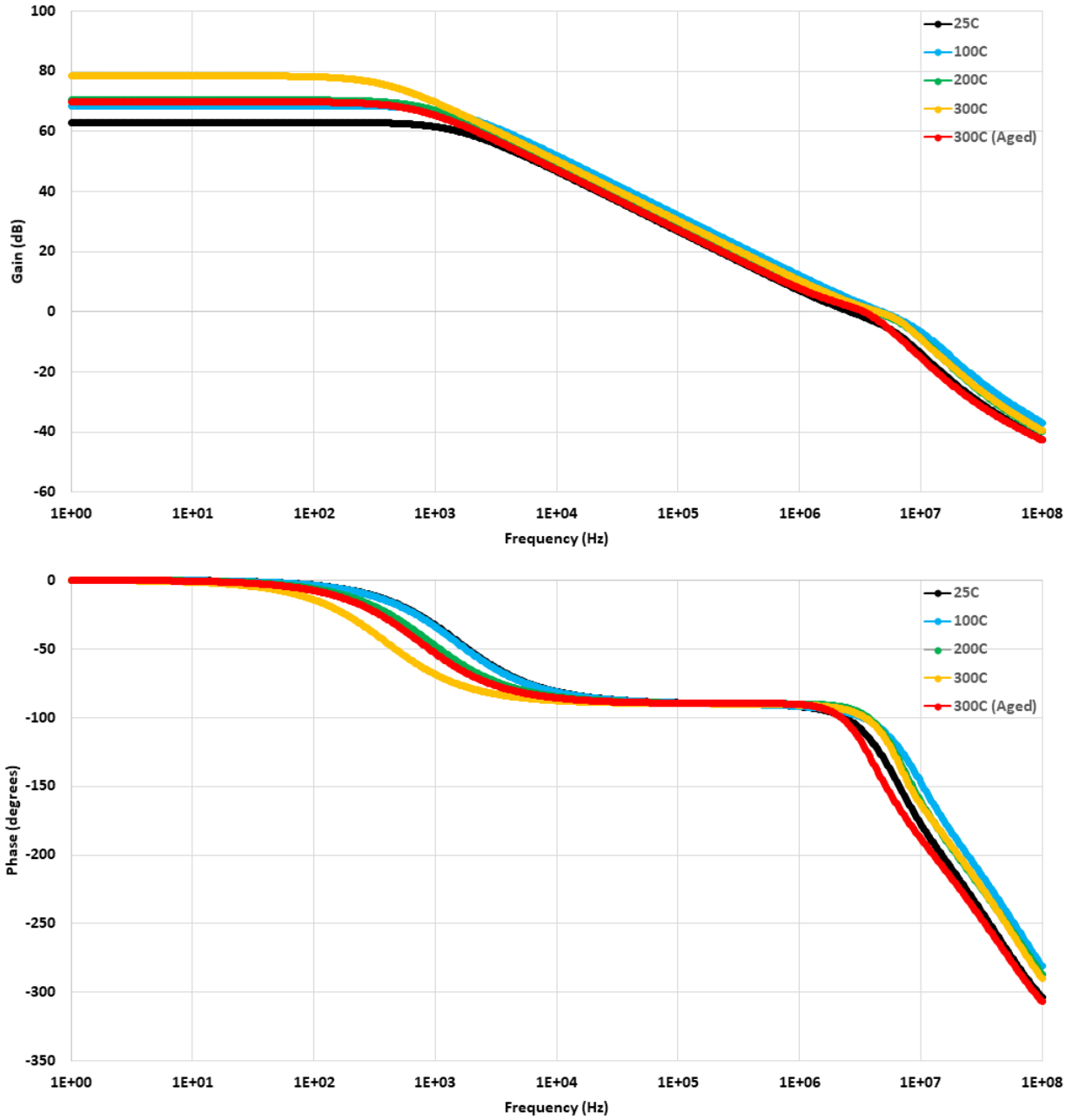

Fig. 4.13. The frequency response of the telescopic op-amp shown in Fig. 4.12.

the PM exceeds 60º in each case except for the aged 300 ºC models which show a minimum PM of 40º. The aged models indicate that a C_C larger than 21 pF is required for adequately splitting the 1st and 2nd poles apart. The UGBW peaks between a V_{ICM} of 3 V to 6 V, with the maximum of approximately 7 MHz occurring in the 200 ºC scenario.

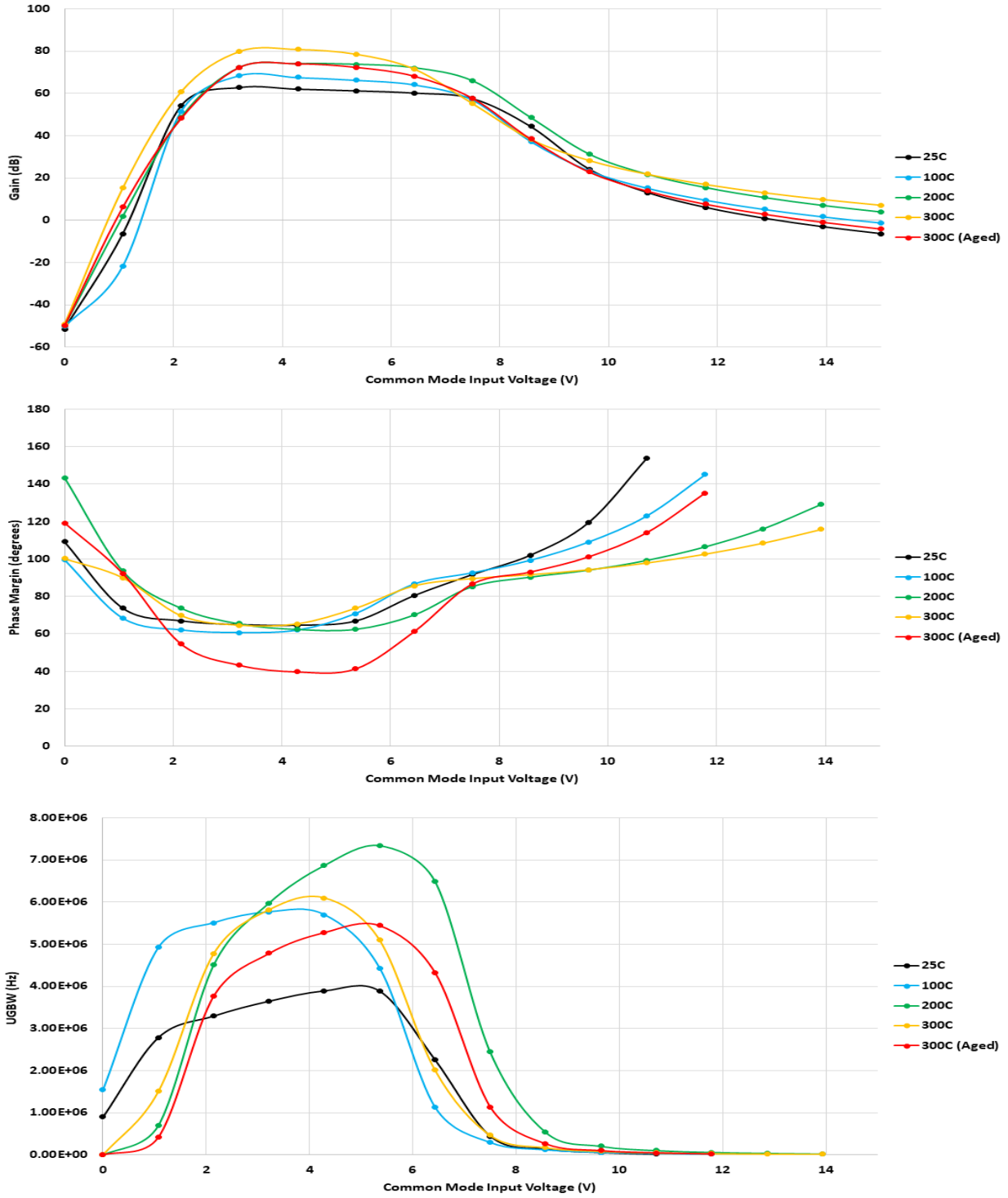

Fig. 4.14. The open-loop DC gain, PM, and UGBW over temperature and a 0-15 V common mode input voltage for the telescopic op-amp with indirect compensation in Fig. 4.12.

The transient response of the telescopic op-amp for a 50 mV step input in a unity-gain and non-inverting (A_V = 2) configurations are shown in Fig. 4.15 and Fig. 4.16, respectively. Despite

the design having 72º of PM for a V_{CM} of 3 V at 300 ºC, the unity-gain configuration displays oscillations similar to an underdamped response with approximately 30º of PM. As stated in the previous section for the two-stage op-amp, this is a problem exclusive to the unity-gain configuration. A transient analysis of the telescopic op-amp for the same conditions, but in the

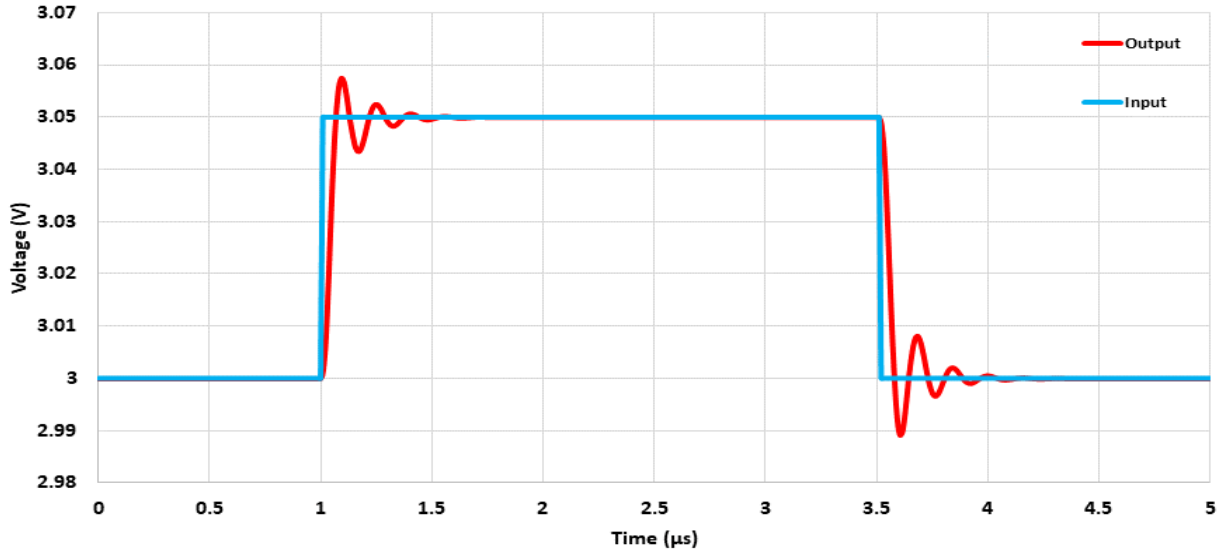

Fig. 4.15. The transient response of the two-stage telescopic op-amp driving a 4.5 pF load at 300 ºC (TF) for a 50 mV step input in a unity-gain configuration.

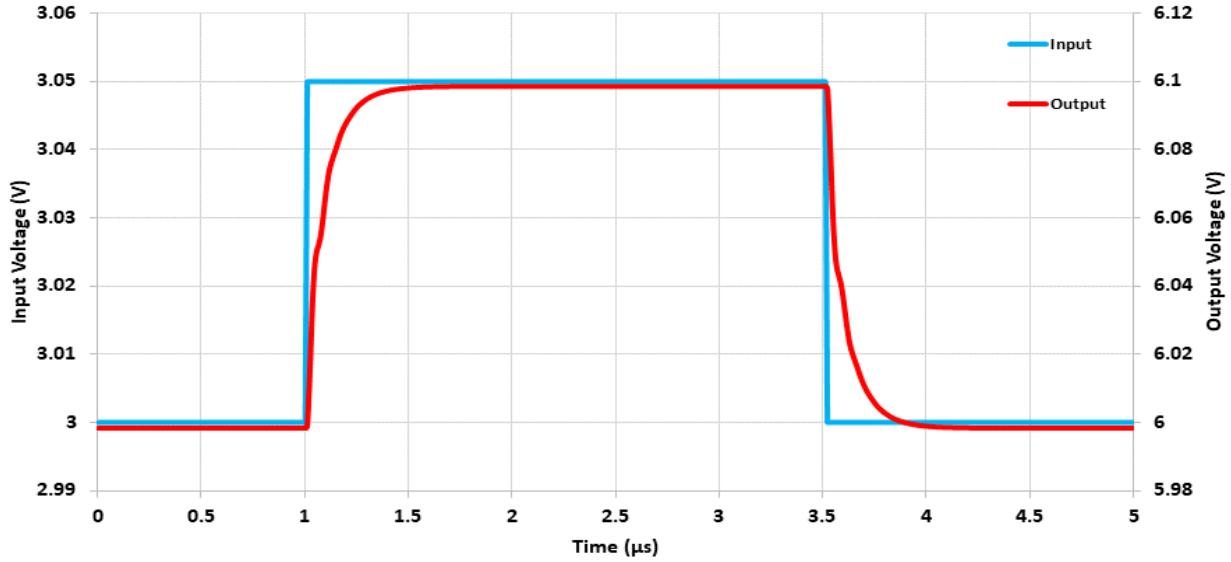

Fig. 4.16. The transient response of the two-stage telescopic op-amp driving a 4.5 pF load at 300 ºC (TF) for a 50 mV step input in a non-inverting configuration.

non-inverting configuration yields a behavior similar to the expected critically damped or overdamped response without any oscillations.

The 1% settling time for the unity-gain response in Fig. 4.15 is 0.36 μs, whereas the settling time for the non-inverting configuration is 0.42 μs. With a bandwidth of nearly 6 MHz at 300 ºC (TF) and for a 3 V input voltage, as shown in Fig. 4.14, the transient response times are slightly slower than expected. Both configurations show better performance than the two-stage counterpart presented in the previous section, with the non-inverting configuration being 0.10 μs faster under the same conditions.

4.2.1.3 Traditional Folded-Cascode Op-Amp

A rail-to-rail folded-cascode op-amp with indirect compensation and an output stage is shown in Fig. 4.17. As with the two-stage telescopic op-amp, the two-stage folded-cascode op-amp connects C_C between cascoded PFETs in the 1st stage and the output in the 2nd stage. The rail-to-rail nature of the op-amp is made possible by incorporating NFET and PFET differential pairs.

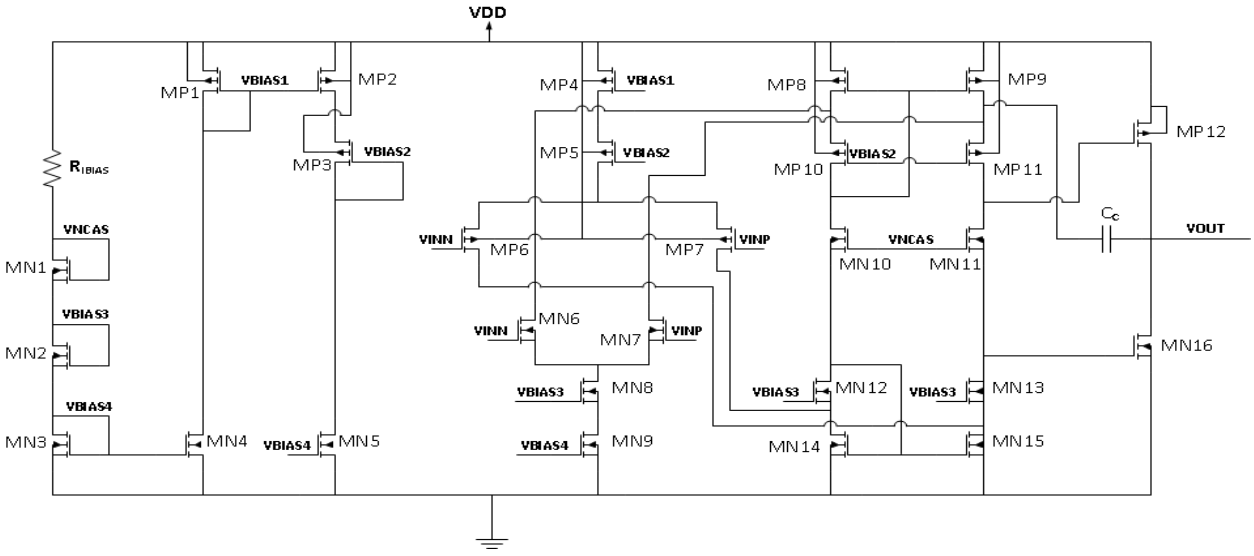

Fig. 4.17. The modified traditional folded-cascode op-amp schematic with an output stage and indirect compensation.

Having both an NFET and PFET pair increases the gain when both are in saturation, although the power dissipation will increase. The gain is also increased by cascoded biasing transistors, specifically MP4/MP5 and MN8/MN9. When the NFET input pair is on, it steals current from the biasing FETs MP8 and MP9. Similarly, the PFET input pair sinks current through the lower biasing FETs MN14 and MN15 when it is on. Requiring MN14, MN15, MP8, and MP9 to sink or source up to twice the amount of current compared to other FETs in the circuit means that they should be sized with twice the effective width. A complete list of the device sizes for the traditional folded-cascode op-amp is given in Table 4.5.

The frequency response of the folded-cascode op-amp at 300 ºC (TF) and for a common mode input voltage of 3 V is shown in Fig. 4.18. The system's frequency response is similar to the two-stage telescopic op-amp presented in the previous section. Indirect compensation is again incorporated into the design and enables pole splitting to ensure an adequate phase margin. In this design, a compensation capacitor of only 4.5 pF is necessary for achieving a 70º PM at 300 ºC (TF), which leads to a significantly higher slew rate.

Table 4.5. The device sizes for the traditional folded-cascode op-amp shown in Fig. 4.17.

Component	Device Size	Comment
MN1 – MN5, MN6, MN7, MN10 – MN13, MN16	20 µm / 1.2 µm (m = 16)	Biasing, NFET input pair, cascode devices, output stage
MN8, MN9, MN14, MN15	20 µm / 1.2 µm (m = 32)	Diff pair biasing and cascode biasing
MP1 – MP5, MP8, MP9	20 µm / 1.2 µm (m = 128)	Biasing
MP6, MP7, MP10, MP11, MP12	20 µm / 1.2 µm (m = 64)	PFET input pair, cascode devices, output stage
R_{IBIAS}	375 kΩ	Biasing
C_C	4.5 pF	Compensation capacitor

Fig. 4.18. The frequency response of the folded-cascode op-amp shown in Fig. 4.17.

Fig. 4.19 provides the open-loop DC gain, PM, and UGBW for each temperature and a V_{ICMR} of 0 - 15 V. For a V_{CM} of 3 V, the maximum gain of 56 dB occurs in the 300 ºC (TF) condition while the minimum gain is 43 dB at 100 ºC. The design provides a gain of at least 33 dB throughout the input range and over temperature, demonstrating the advantage of the rail-to-rail topology. However, the telescopic op-amp yields a higher gain for a V_{CM} of 3 V to 7 V.

The PM of the folded-cascode op-amp is significantly more stable over the input range than its telescopic counterpart, which is again a benefit of the rail-to-rail topology. The minimum

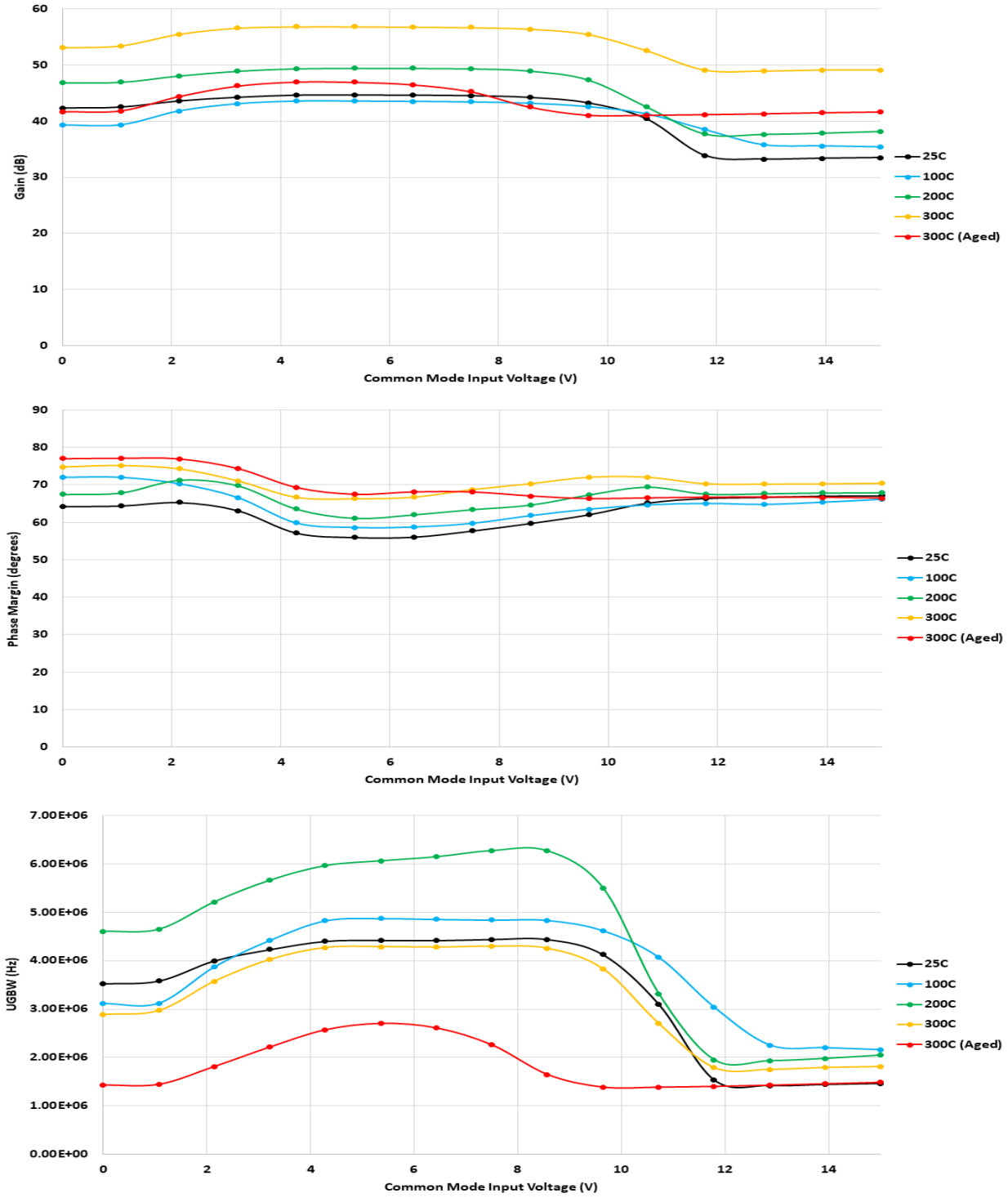

Fig. 4.19. The open-loop DC gain, PM, and UGBW over temperature and a 0-15 V common mode input voltage for the folded-cascode op-amp with indirect compensation in Fig. 4.17.

phase margin of 56º occurs in the 25 ºC case and still provides for a stable transient response. The UGBW is lower than the peak values of the telescopic op-amp, but appreciably higher than the basic two-stage op-amp.

The transient response of the folded-cascode op-amp in a unity-gain configuration and for a 50 mV step input at 300 ºC (TF) is shown in Fig. 4.20. Oscillations are again present due to the indirect compensation technique despite a PM of 70º. As with the telescopic op-amp, a nulling resistor and compensation capacitor between the output of each stage yields no issue for the same PM. Repeating the non-inverting configuration for the folded-cascode op-amp results in the transient response given in Fig. 4.21.

A 1% settling time of 0.36 µs is obtained in the unity-gain configuration, while the non-inverting configuration yields a settling time of 0.28 µs. The settling time in the non-inverting configuration is therefore decreased by 0.24 µs and 0.14 µs compared to the standard two-stage and telescopic op-amp topologies, respectively.

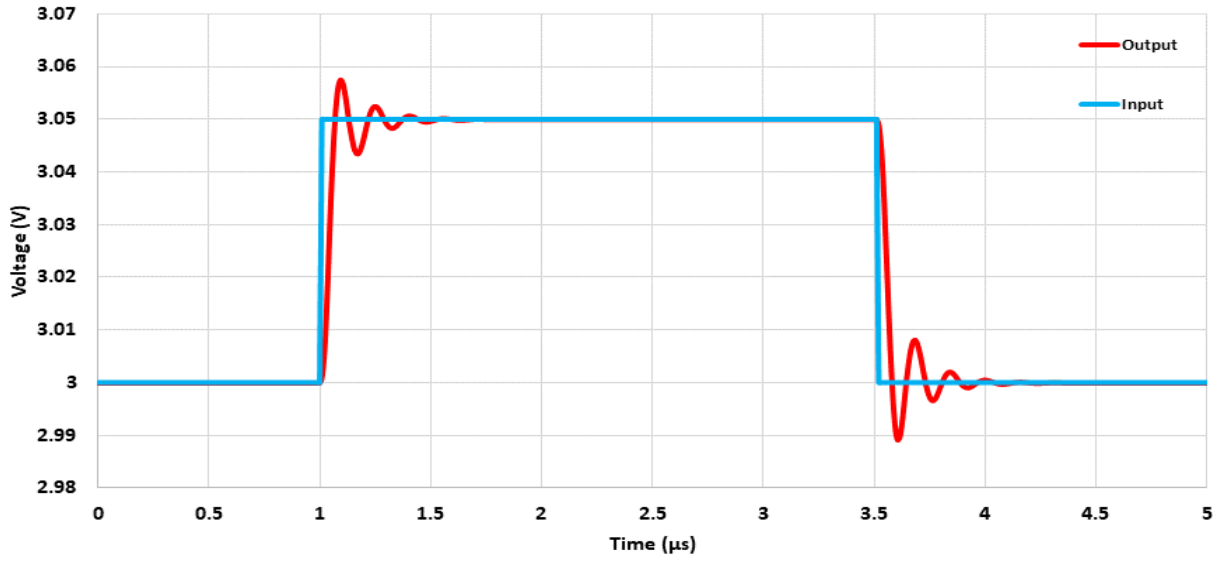

Fig. 4.20. The transient response of the traditional folded-cascode op-amp driving a 4.5 pF load at 300 ºC (TF) for a 50 mV step input in a unity-gain configuration.

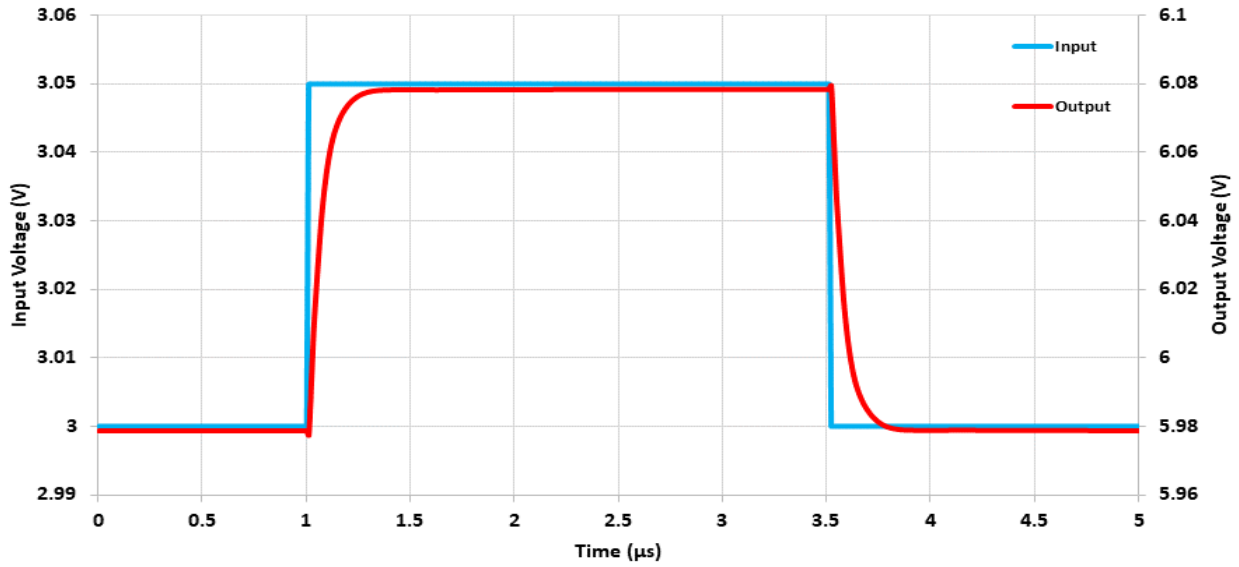

Fig. 4.21. The transient response of the traditional folded-cascode op-amp driving a 4.5 pF load at 300 ºC (TF) for a 50 mV step input in a non-inverting configuration.

4.2.1.4 Recycling Folded-Cascode Op-Amp

The traditional folded-cascode topology is commonly used in a multitude of high frequency applications. Similar to the two-stage telescopic op-amp, the traditional folded-cascode was shown to provide a single parasitic pole approximately one decade after the unity-gain frequency for an appropriately sized C_C. The discussion in Chapter 3, Section 3.1.1.2 gave the pole locations of the folded-cascode OTA (no output stage) with an NFET input pair. The dominant pole is determined by the output resistance and capacitive load while the non-dominant pole is located at the source of the cascode FET which is having its current stolen by the differential input pair (i.e. M7's source in Fig. 3.5).

With respect to the dominant pole, the capacitive load is determined by the application while the output resistance can be altered by changing the sizes of the cascoded FETs. Reducing the widths of the FETs leads to a higher output resistance but comes at the cost of reduced bandwidth, a smaller output voltage swing, and potentially forcing the FETs out of saturation.

Similarly, increasing the lengths of the cascoded FETs increases the output resistance but will result in lower bandwidth. For these reasons, it is generally not desirable to alter the location of the dominant pole by design. To enable higher frequency operation, the non-dominant pole must be shifted to higher frequencies. This can be achieved by using the recycling folded-cascode (RFC) topology shown in Fig. 4.22 [40] - [42].

The improvement over the traditional folded-cascode topology is a result of turning the biasing FETs into signal paths. For example, MN14 and MN15 in Fig. 4.17 conduct a relatively large amount of current in the conventional folded-cascode topology but only function as current sinks. In the RFC op-amp MN14 corresponds to MN8 and MN9, where MN9 mirrors its current over to MN8. The same approach applies to MN15 which now corresponds to MN10 and MN11. The mirroring FET (MN9 or MN10) typically has 1/3 of the width of its corresponding FET (MN8 or MN11) sinking current from the cascode stage.

Although not used in [41], the combination of MN7 and MN10 forms a wide-swing cascode current mirror, allowing for the design to benefit from increased gain while the necessary

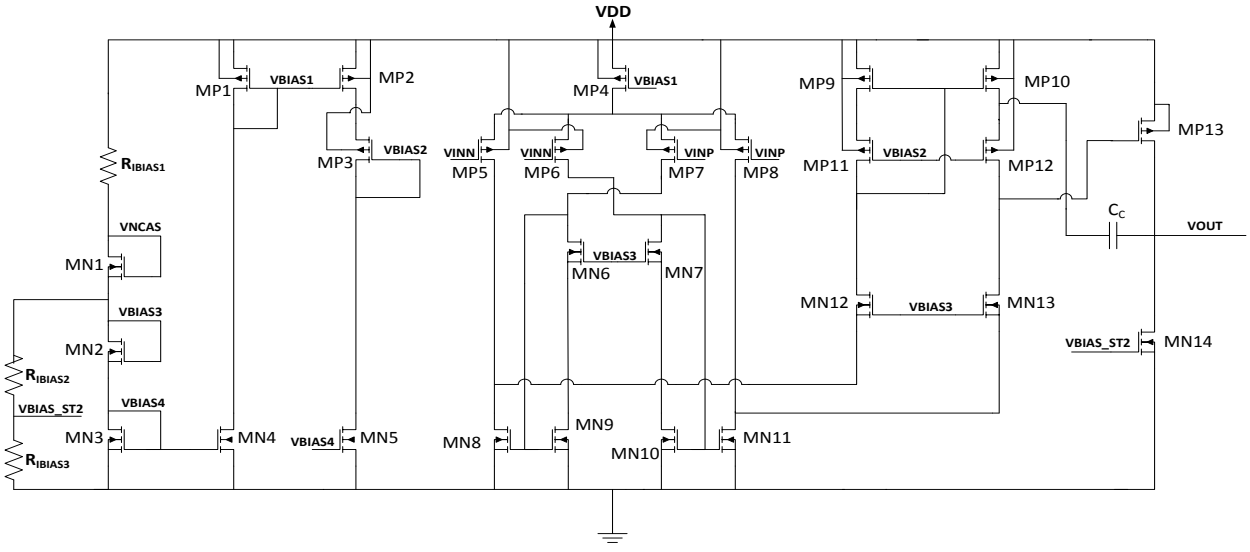

Fig. 4.22. The RFC op-amp schematic with an output stage and indirect compensation.

supply voltage overhead is not substantially increased. Another wide-swing current mirror is formed by MN6 and MN9. In each case, the current mirror can be thought of as a single diode connected FET.

The signal path consisting of MP6-MN7-MN10-MN11-MN13 forms a current-mirror as presented in [41] which allows the op-amp to have a higher slew rate and a lower setting time. The other signal path from MP8-MN11-MN13 results in a feedforward path as in the traditional folded-cascode op-amp. The signal paths combine in-phase at the source of MN13, resulting in a LHP zero that counters the dominant pole (albeit at relatively high frequencies). The pole and zero locations are approximated in [41] and are listed in expressions (4.16) to (4.18).

$$\boldsymbol{f_{p1} \approx \frac{g_{m10}}{2\pi(C_{GS,MN10})(1+N)}} \tag{4.16}$$

$$\boldsymbol{f_{z1} \approx \frac{g_{m10}}{2\pi(C_{GS,MN10})}} \tag{4.17}$$

$$\boldsymbol{f_{p2} \approx \frac{g_{m11}}{2\pi(C_N)}} \tag{4.18}$$

In the equation for f_{p1}, the value of N refers to the ratio between the current mirroring devices (i.e. MN10 to MN11) which is set to 1:3 in this design as previously specified. The value of C_N in the f_{p2} expression refers to the total capacitance at the source of MN13.

A complete list of the device sizes for the RFC using indirect compensation is given in Table 4.6. The frequency response at 300 ºC (TF) and for a common mode input voltage of 3 V is shown in Fig. 4.23. The gain follows a typical single pole system response with a -20 dB/decade drop until approximately 10 MHz in each case. The low-frequency gain has a maximum of 67.5 dB at 300 ºC and decreases to 60.3 dB at 25 ºC. For the 300 ºC aged models, the low-frequency gain is only 50.8 dB which indicates that the supply voltage overhead is approaching the available 15 V because of the PFET threshold voltage increase.

Table 4.6. The devices sizes for the recycling folded-cascode schematic in Fig. 4.22.

Component	Device Size	Comment
MN6, MN7, MN9, MN10, MN12, MN13	20 µm / 1.2 µm (m = 8)	Wide swing current mirrors, cascoded FETs
MN8, MN11	20 µm / 1.2 µm (m = 24)	Current sinks
MN1 – MN5, MN14	20 µm / 1.2 µm (m = 32)	Biasing, 2nd stage NFET
MP5 – MP12	20 µm / 1.2 µm (m = 32)	Input pair and cascoded devices
MP1 – MP4, MP13	20 µm / 1.2 µm (m = 128)	Biasing for input pair and cascoded FETs, 2nd stage PFET
R_{IBIAS1}	80 kΩ	Biasing (1st stage)
R_{IBIAS2}	50 kΩ	Biasing (2nd stage)
R_{IBIAS3}	125 kΩ	Biasing (2nd stage)
C_C	21 pF	Compensation capacitor

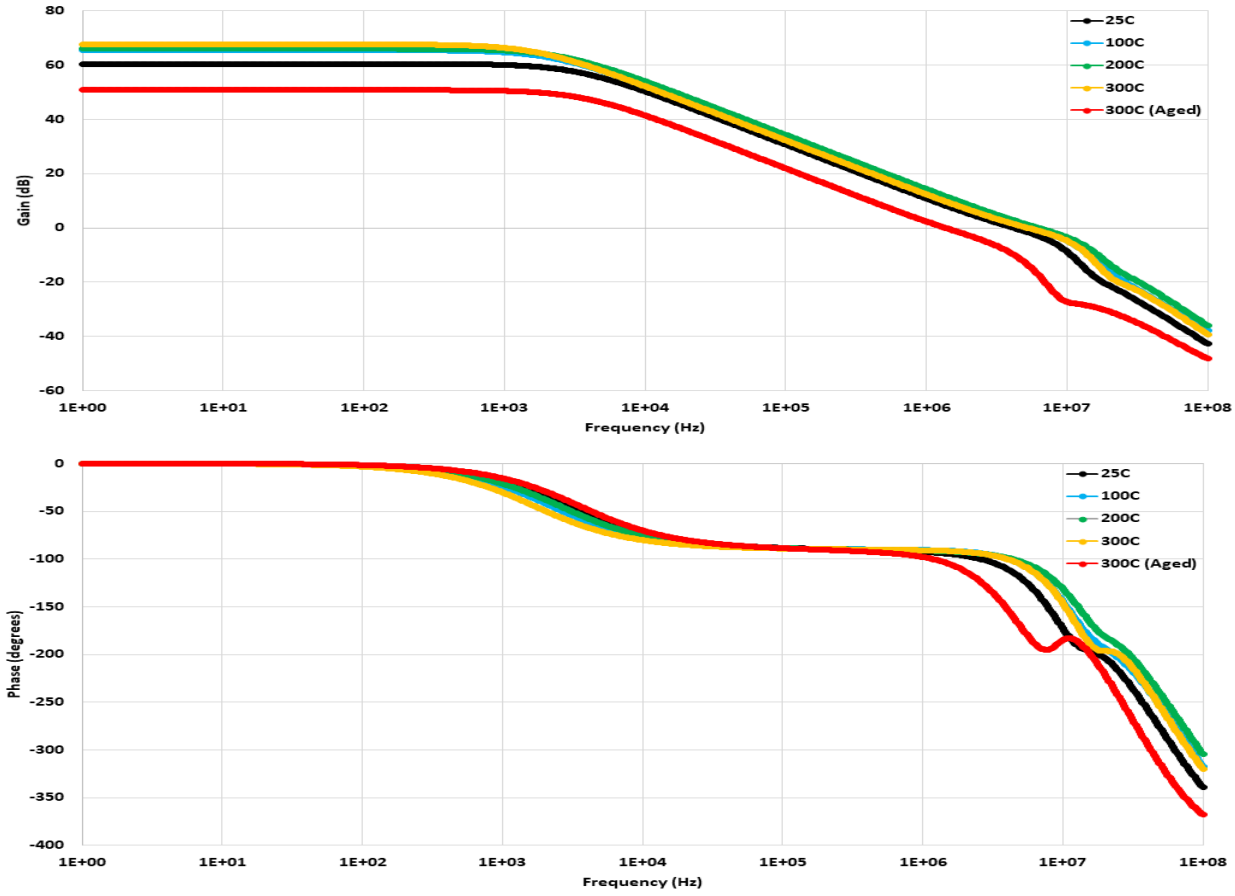

Fig. 4.23. The frequency response of the recycling folded-cascode op-amp in Fig. 4.22.

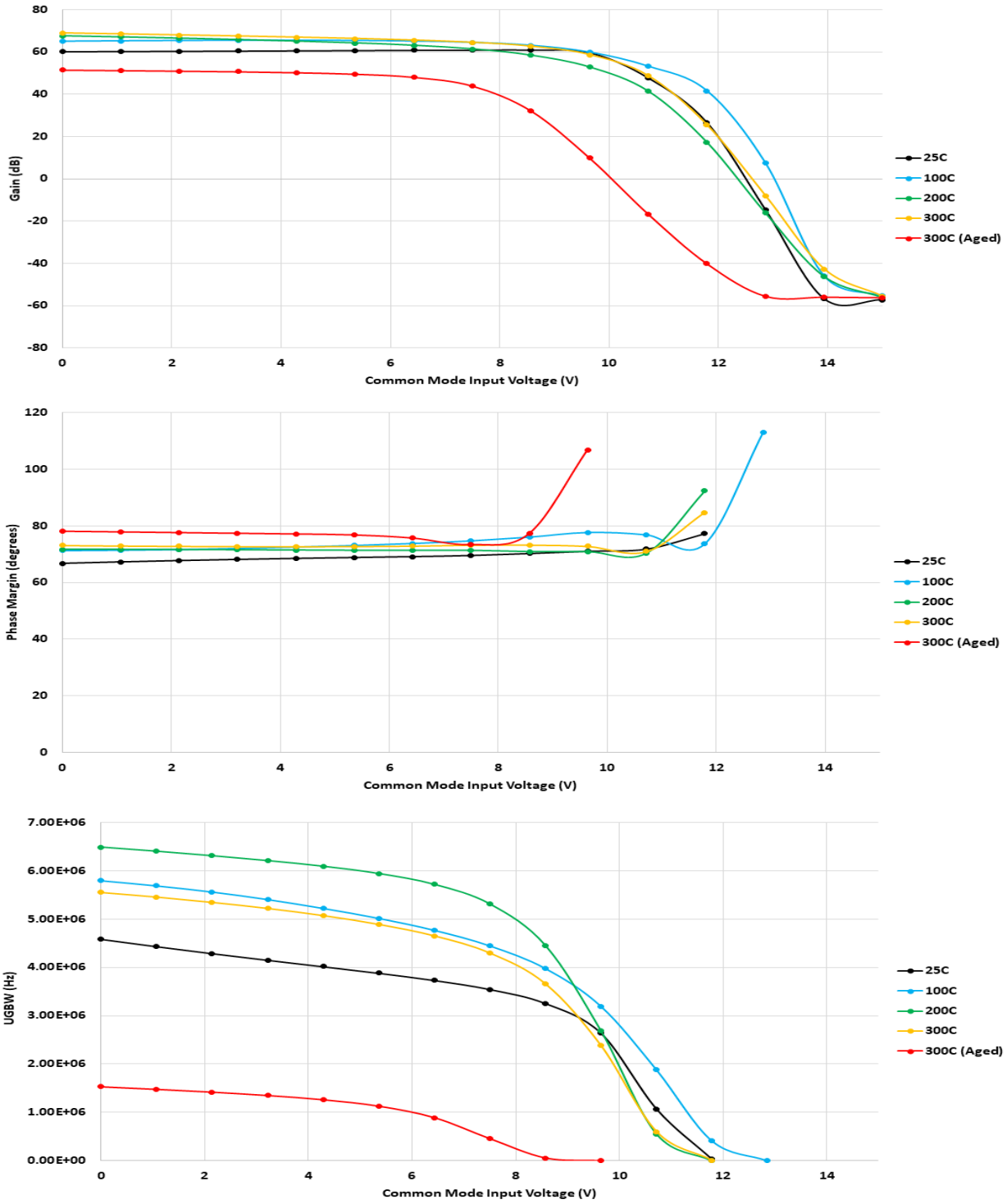

Fig. 4.24. The open-loop DC gain, PM, and UGBW over temperature and a 0-15 V common mode input voltage for the recycling folded-cascode in Fig. 4.22.

A summary of the RFC's frequency response parameters is presented in Fig. 4.24. The low-frequency open-loop gain is about 10 dB lower than the telescopic within the respective V_{ICMR}

of each op-amp. However, the V_{ICMR} is significantly greater for the RFC and it also has a more consistent PM across the operating temperature range. The peak UGBW is slightly lower than for the telescopic for each case, except for 300 ºC (TT) which is limited by the supply voltage headroom.

The transient response of the RFC in a unity-gain configuration at 300 ºC and for a 50 mV step input is shown in Fig. 4.25. The indirect compensation again exhibits oscillations on the rising and falling edges, although there isn't a significant undershoot or overshoot as should be expected for 70º of PM. In a non-inverting configuration with the same operating conditions, the RFC's transient response is shown in Fig. 4.26. The 1% settling times are 0.19 µs and 0.34 µs for the unity-gain and non-inverting configurations, respectively. In the unity-gain configuration, this marks a 0.17 µs improvement over the traditional folded-cascode. However, the RFC performs slightly worse in the non-inverting configuration versus the folded-cascode with a 0.06 µs longer settling time.

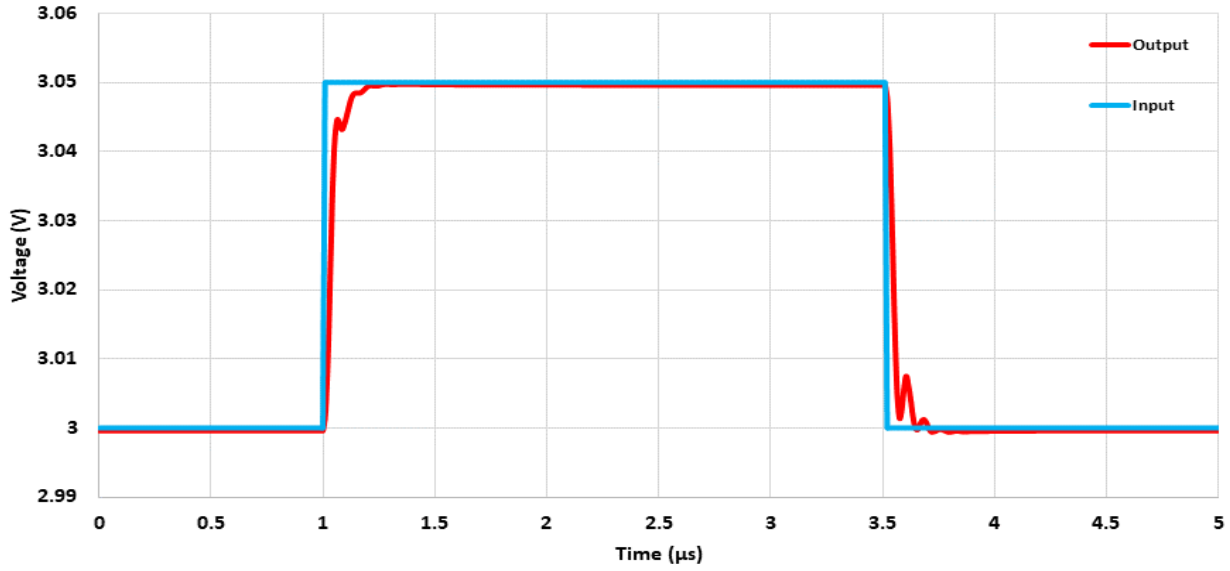

Fig. 4.25. The transient response of the recycling folded-cascode op-amp driving a 4.5 pF load at 300 ºC (TF) for a 50 mV step input in a unity-gain configuration.

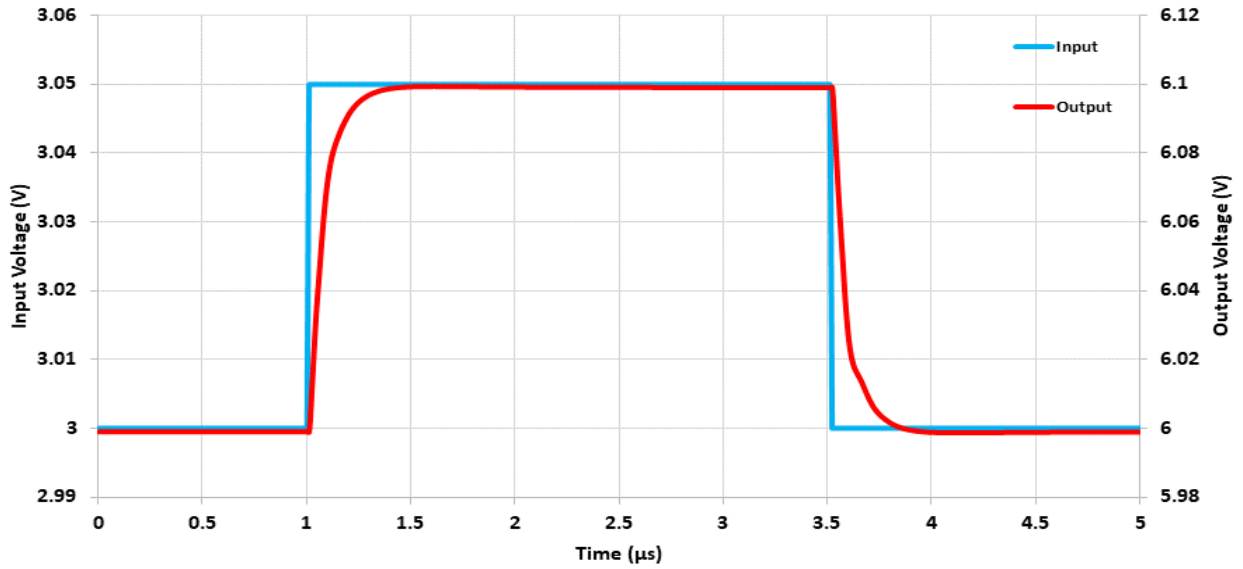

Fig. 4.26. The transient response of the recycling folded-cascode op-amp driving a 4.5 pF load at 300 °C (TF) for a 50 mV step input in a non-inverting configuration.

4.2.1.5 Multipath Recycling Folded-Cascode Op-Amp

In the RFC op-amp presented in the previous section, the AC signal followed the same path as the DC current. The multipath RFC shown in Fig. 4.27 increases the overall transconductance of the op-amp by separating the AC and DC paths as suggested in [64]. The DC current path for the non-inverting input goes through MN7 and MN10, whereas the AC path goes through MN6

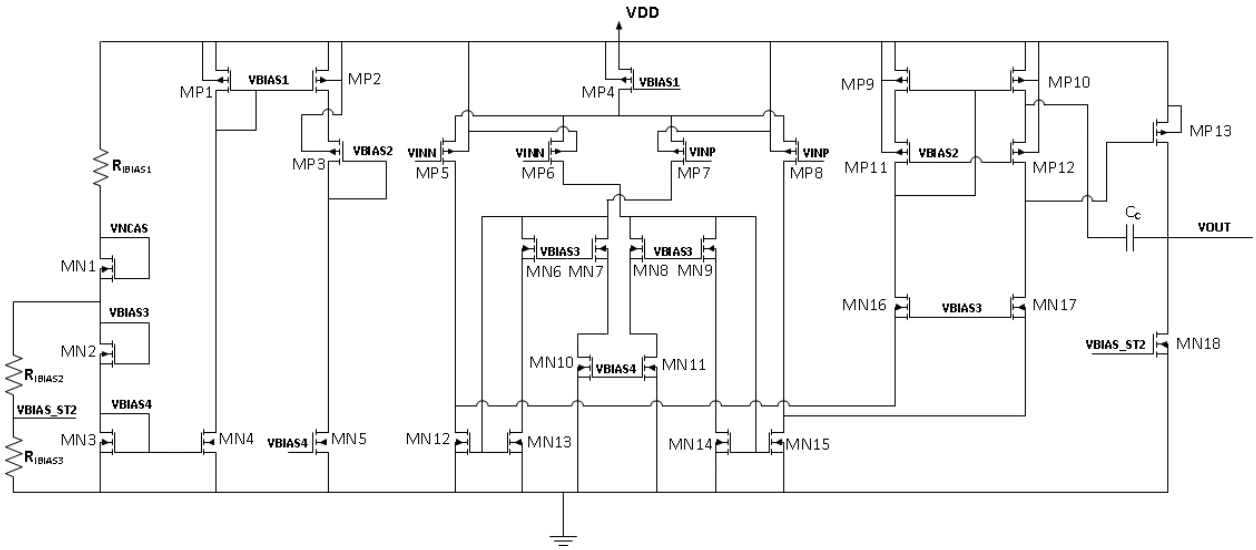

Fig. 4.27. The multipath RFC op-amp schematic.

and MN13 before it's mirrored through MN12 to the cascode structure. The result is that the multipath RFC provides an increase in gain for the same MN12:MN13 sizing ratio. Alternatively, the ratio of MN12:MN13 can be increased since a smaller width of MN13 pushes the parasitic pole at its gate to higher frequencies, resulting in a larger bandwidth where the 2nd pole is effectively cancelled out by the zero. Additional literature publications have expanded upon the multipath approach to achieve higher gain and bandwidth [65], [66].

The device sizes of the multipath RFC are listed in Table 4.7. The frequency response across the operating temperature range and for a V_{CM} of 3 V is shown in Fig. 4.27. At 300 ºC and with no increase in power consumption, the low-frequency gain of 78 dB is a significant boost over the 67 dB provided by the conventional RFC. This advantage can be traded for a slightly higher UGBW by decreasing the sizes of MN13 and MN14. The pole and zero expressions are largely unchanged, therefore the system's phase response is similar to the RFC as expected.

Table 4.7. The devices sizes for the multipath RFC schematic in Fig. 4.27.

Component	Device Size	Comment
MN6 – MN11, MN12 – MN14, MN16, MN17	20 µm / 1.2 µm (m = 8)	Wide swing current mirrors, cascoded FETs, added DC path
MN12, MN15	20 µm / 1.2 µm (m = 24)	Current sinks
MN1 – MN5, MN18	20 µm / 1.2 µm (m = 32)	Biasing, 2nd stage NFET
MP5 – MP12	20 µm / 1.2 µm (m = 32)	Input pair and cascoded devices
MP1 – MP3, MP13	20 µm / 1.2 µm (m = 128)	Biasing for cascoded FETs, 2nd stage PFET
MP4	20 µm / 1.2 µm (m = 128)	Biasing for input pair
R_{IBIAS1}	80 kΩ	Biasing (1st stage)
R_{IBIAS2}	50 kΩ	Biasing (2nd stage)
R_{IBIAS3}	130 kΩ	Biasing (2nd stage)
C_C	36 pF	Compensation capacitor

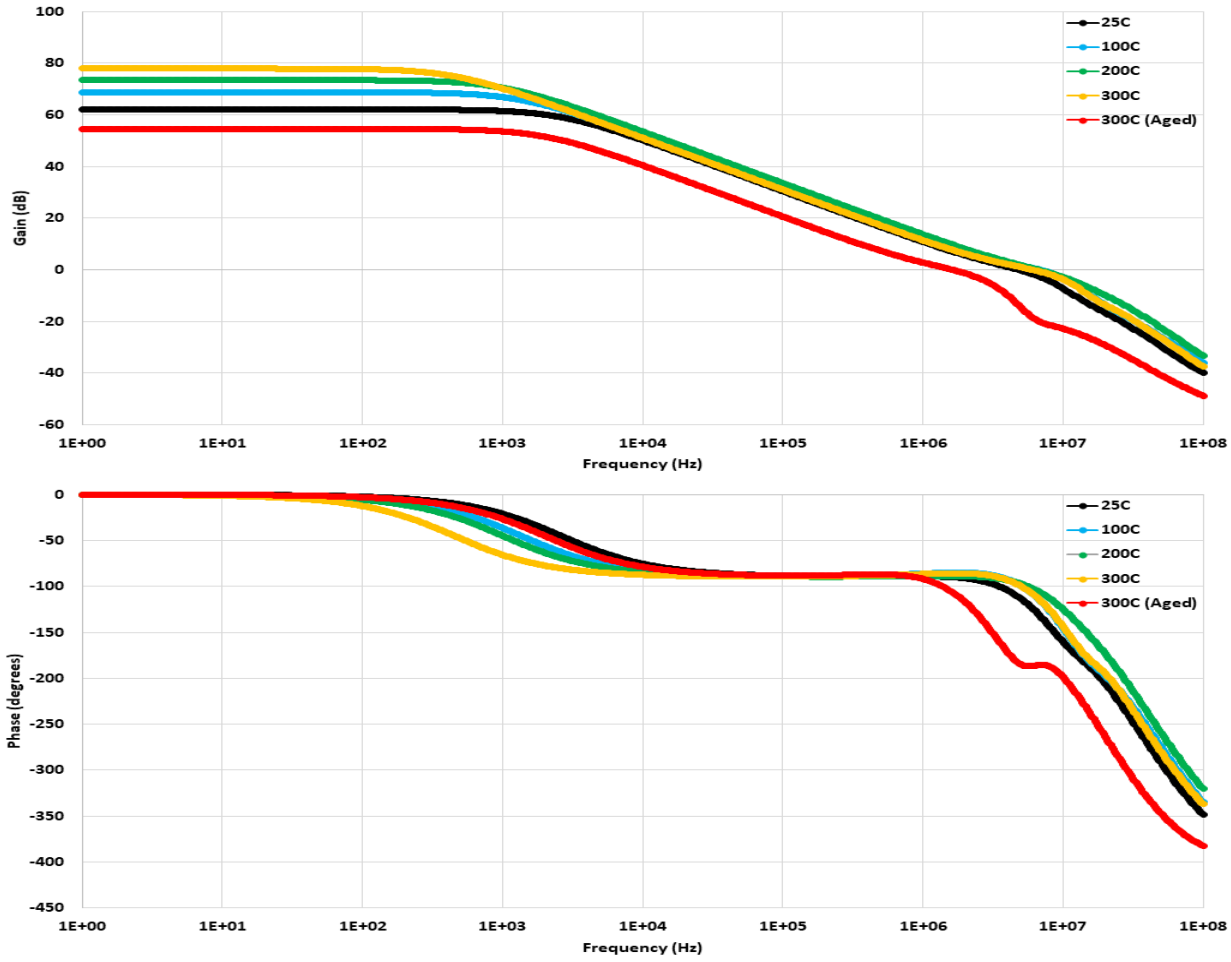

Fig. 4.28. The frequency response of the multipath RFC op-amp in Fig. 4.27.

The DC open-loop gain, PM, and UGBW results over the operating temperature range and for a V_{CM} of 0 V to 15 V are provided in Fig. 4.29. The largest increase in DC gain is present in the 200 ºC and 300 ºC cases, although the other temperatures each increase by about 2 to 4 dB as well. The PM is relatively consistent as it was in the RFC design with the maximum shift being about 15º over the entire temperature range while operating inside the V_{ICMR}. The UGBW is improved for each temperature versus the conventional RFC. Compared to the telescopic op-amp, the multipath RFC only loses in the 200 ºC case for a V_{CM} of 4 V to 7 V and for the 300 ºC (TT) aged models where the supply voltage headroom serves as the constraint.

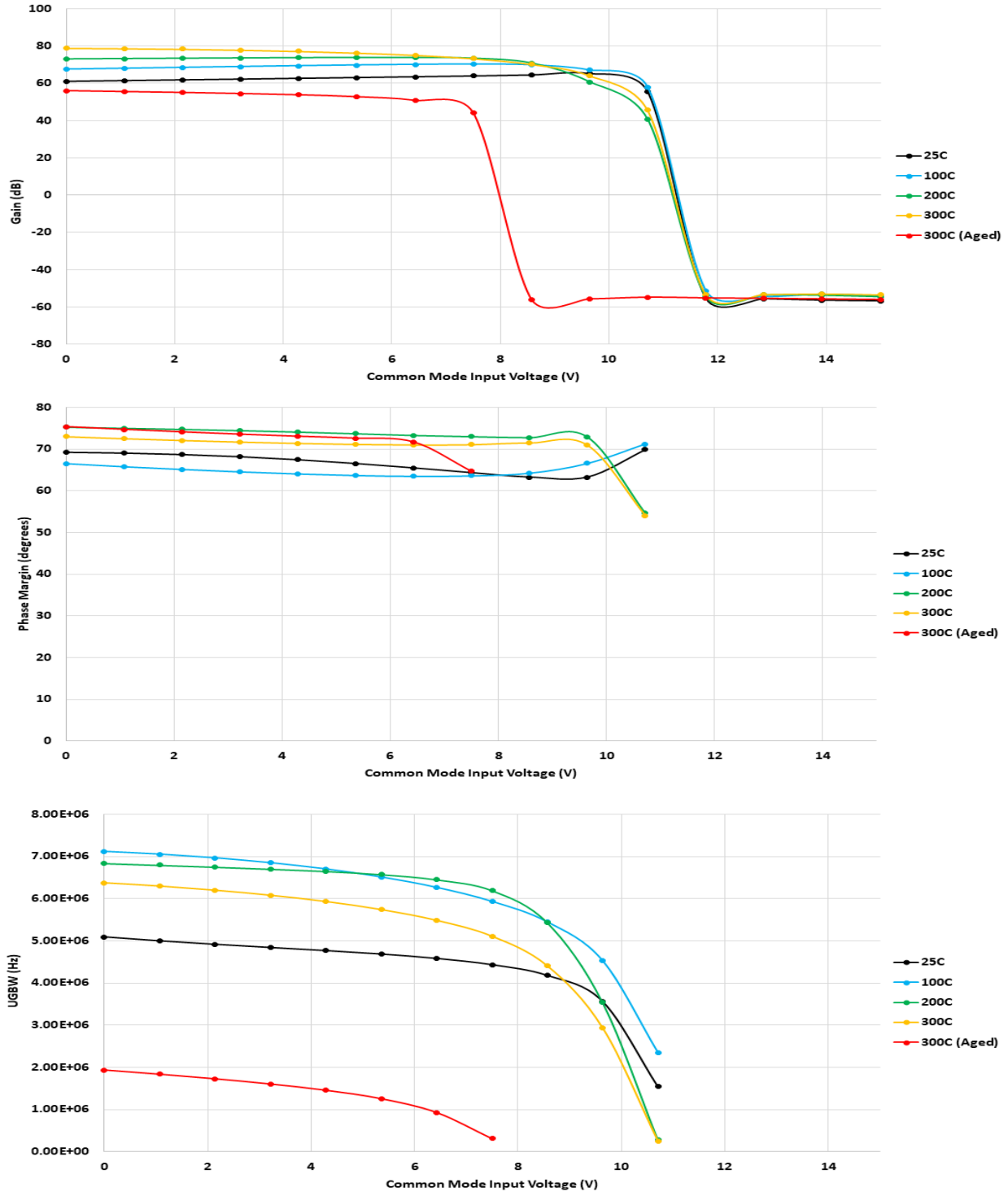

Fig. 4.29. The open-loop DC gain, PM, and UGBW over temperature and a 0-15 V common mode input voltage for the multipath RFC in Fig. 4.27.

The transient response of the multipath RFC at 300 ºC in the unity-gain and non-inverting configurations is shown in Fig. 4.30 and Fig. 4.31, respectively. The 1% settling time in the unity-

gain configuration is 0.32 µs versus 0.37 µs for the non-inverting configuration. With respect to settling time, the multipath RFC underperforms slightly compared to the conventional RFC. The non-inverting configuration settling time is only 0.03 µs longer in the multipath topology, but the unity-gain configuration is 0.13 µs slower.

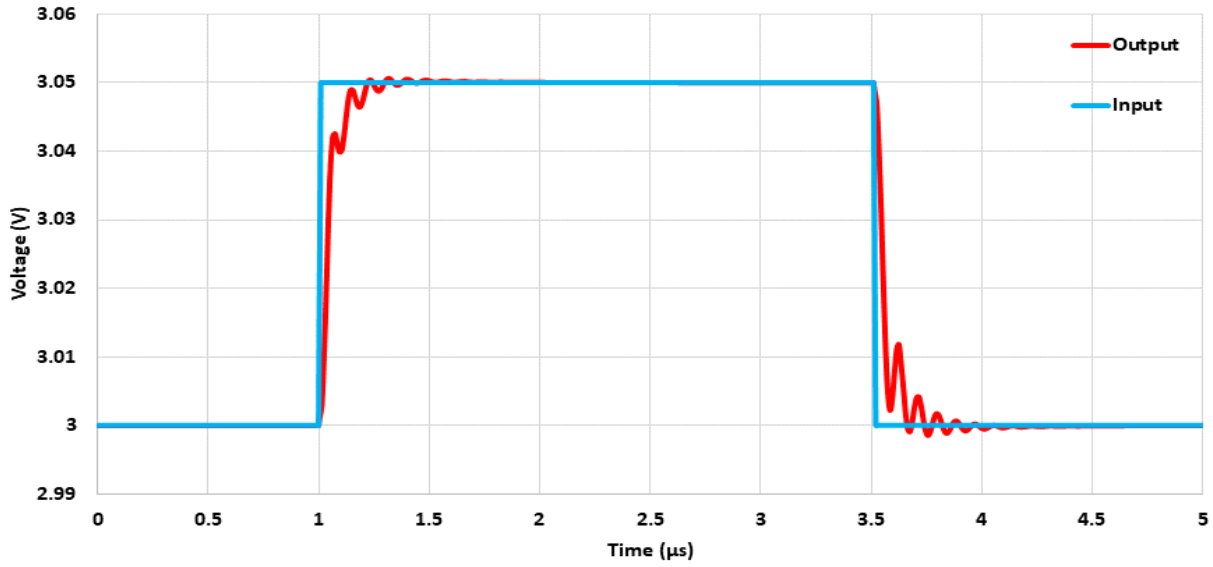

Fig. 4.30. The transient response of the multipath RFC driving a 4.5 pF load at 300 ºC (TF) for a 50 mV step input in a unity-gain configuration.

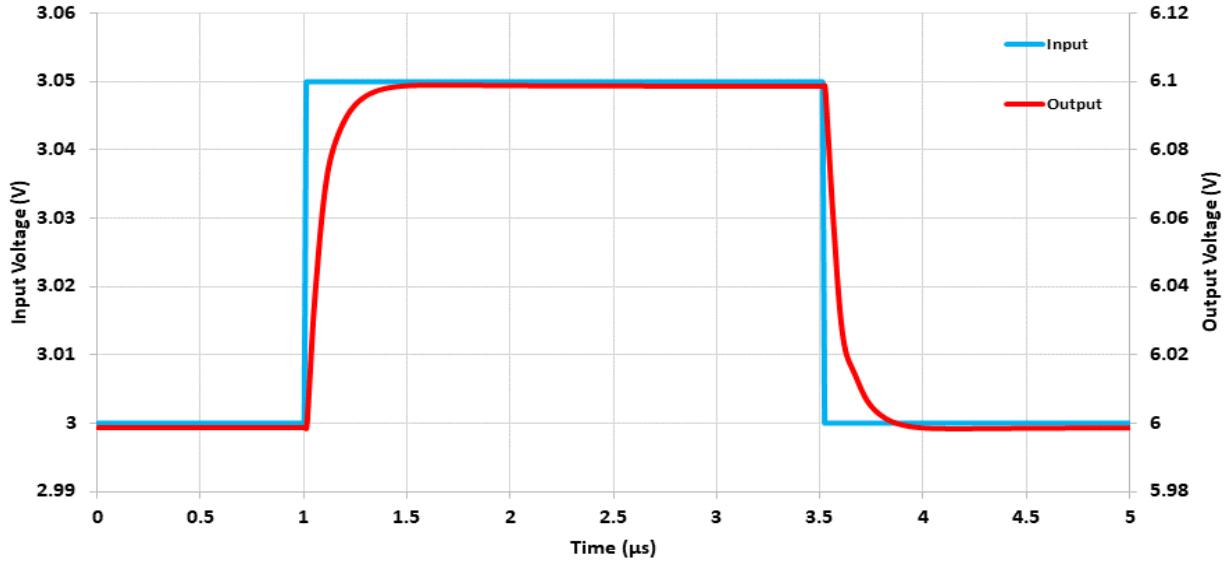

Fig. 4.31. The transient response of the multipath RFC driving a 4.5 pF load at 300 ºC (TF) for a 50 mV step input in a non-inverting configuration.

4.2.1.6 Comparing the Op-Amp Architectures

The foundation of a fully-on chip linear regulator requires a high bandwidth, high gain op-amp with a frequency response that is nearly representative of a single pole system. Each of the op-amps designed and presented in the previous sections have targeted a 70º PM using an indirect compensation scheme to split the 1st and 2nd poles of the system. Achieving a high bandwidth for the overall linear regulator hinges upon splitting the op-amp's poles apart to a degree that the 2nd pole only marginally impacts the frequency response.

The two-stage op-amp implemented in the Vulcan II linear regulator had a high bandwidth, but relatively close 1st and 2nd poles that lead to a low PM. This ultimately required a significant amount of compensation at the top-level of the regulator and resulted in a decreased UGBW. To improve upon the Vulcan II regulator design, Table 4.8 provides a comparison of the op-amps designed along with the Vulcan II op-amp.

The first item to note from Table 4.8 is that the Vulcan II op-amp is presented for its original design in which it had a V_{CM} of 7.5 V whereas the fully-on chip linear regulators will be utilizing a bandgap reference that provides approximately 3 V [67]. The performance with a V_{CM} of 7.5 V has a high UGBW as previously stated, but lacks phase margin. It also uses more than the 1.5 mA current budget. To form a more direct comparison with the op-amps designed, the total current consumption is lowered to 1.5 mA and the compensation network is altered such that it provides a 70º of PM (R_Z = 830 Ω and C_C = 8.8 pF in Fig. 4.3). This results in the UGBW decreasing to 3.12 MHz, although the settling time remains nearly constant. The settling time in the non-inverting configuration is not reported since the results are limited by the 15 V supply rail for A_V = 2 and V_{IN} = 7.5 V.

Table 4.8. An op-amp performance comparison at 300 ºC (TF).

Parameter	Vulcan II Two-Stage	Two-Stage (Indirect comp.)	Telescopic	Folded-Cascode	RFC	Multipath RFC
Current Consumption	2.3 mA	1.5 mA	1.5 mA	1.5 mA	1.5 mA	1.5 mA
V_{CM}	7.5 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V
Capacitive Load	4.5 pF	4.5 pF	4.5 pF	4.5 pF	4.5 pF	4.5 pF
DC Gain	64.0 dB	55.5 dB	78.4 dB	56.4 dB	67.5 dB	77.9 dB
UGBW	9.37 MHz	3.05 MHz	4.40 MHz	3.95 MHz	5.24 MHz	6.10 MHz
Phase Margin	30.3º	68.4º	72.0º	71.9º	72.7º	71.6º
1% Settling Time (Unity-gain)	0.21 µs	0.40 µs	0.36 µs	0.36 µs	0.19 µs	0.32 µs
1% Settling Time (Non-Inv.)	-	0.52 µs	0.42 µs	0.28 µs	0.34 µs	0.37 µs
Input Common Mode Range	4.4 – 12.4 V	0 – 11.6 V	1.6 – 8.4 V	0 – 15 V	0 – 10.3 V	0 – 10.9 V

The op-amps designed with an indirect compensation scheme also do not rely upon a nulling resistor, which is a significant advantage given the process variation observed in Vulcan I and Vulcan II. Of the op-amps designed in the previous sections, the telescopic and multipath RFC have the best overall performance. An issue for the telescopic op-amp is its input common mode range. In Table 4.8, the V_{ICMR} is the voltage range that provides a gain greater than 40 dB. As shown in Fig. 4.14, the telescopic op-amp's low-frequency gain over temperature begins to decrease significantly below 3 V V_{CM}. If the bandgap reference drifts downwards from the ideal 3 V, then the performance of the telescopic op-amp will degrade rapidly. Due to these factors, the multipath RFC is the best selection for the fully on-chip linear regulator's op-amp. Note that the

performance of the multipath RFC may differ slightly from Table 4.8 when it is implemented in the fully-on chip linear regulator. The reasoning for this is that the dominant and non-dominant poles will be split further apart to ensure an acceptable phase margin over all operating conditions.

Before proceeding, the PSRR and CMRR of the multipath RFC are provided in Fig. 4.32 and Fig. 4.33, respectively. As a comparison to a general-purpose op-amp, Texas Instrument's silicon based LMC660C op-amp reports a (measured) PSRR and CMRR of 63 dB with a total current consumption of approximately 0.4 mA [68]. The multipath RFC therefore outperforms the silicon based part in all cases except for the PSRR at 25 ºC. Finally, the multipath RFC has a slew rate of approximately 15 V/µs at 300º C versus 1.1 V/µs (at 25 ºC) for the LMC660C.

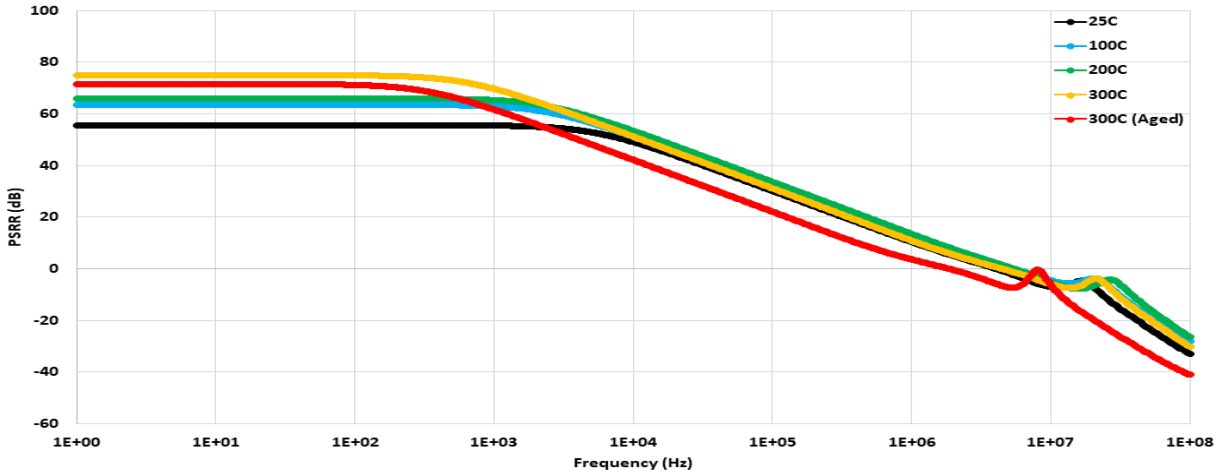

Fig. 4.32. The PSRR of the multipath RFC over the operating temperature range.

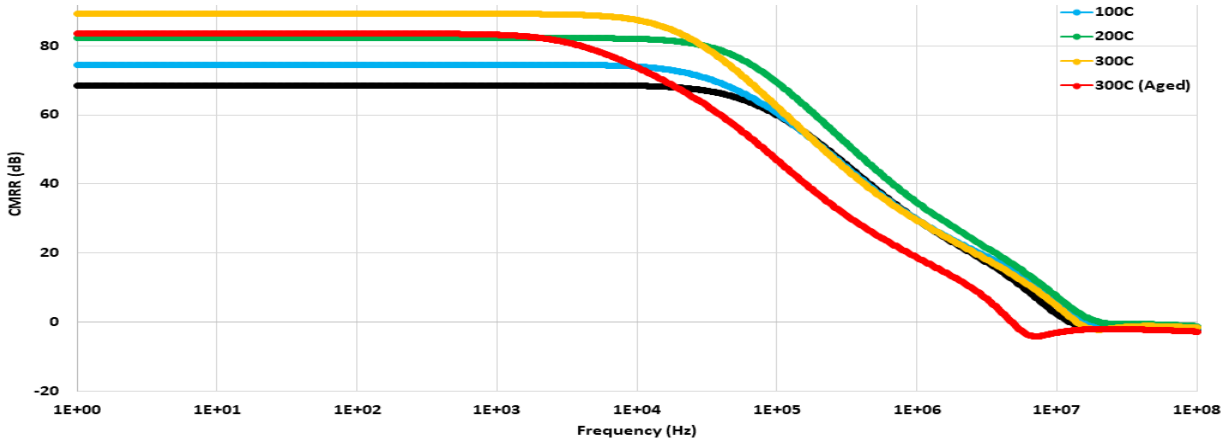

Fig. 4.33. The CMRR of the multipath RFC over the operating temperature range.

4.2.2 Fully On-Chip NFET Pass Transistor Based Linear Regulator

The proposed schematic of the fully-on chip linear regulator is shown in Fig. 4.34 with the multipath RFC now forming the foundation of the feedback loop. The design procedure and compensation scheme both derive from the Vulcan II linear regulator in which a fast auxiliary path is implemented with a differentiator that dynamically alters the output resistance of the op-amp to counter sudden transient disturbances. The R_{ESR} connected with C_{LOAD} in the Vulcan II linear regulator has been removed to allow the capacitor to better assist with fast transient loads while the regulator reacts. This on-chip linear regulator is primarily intended for relatively low-power, stand-alone applications. The total quiescent current is therefore limited to 3 mA at 300 ºC.

Subsequent design specifications include a maximum load current of 50 mA and an input voltage range of 20 V to 50 V for 25 ºC to 300 ºC. A safety margin has been added to provide up to 50 mA for an input voltage of 19 V at 25 ºC, resulting in MN1's width being less than half that

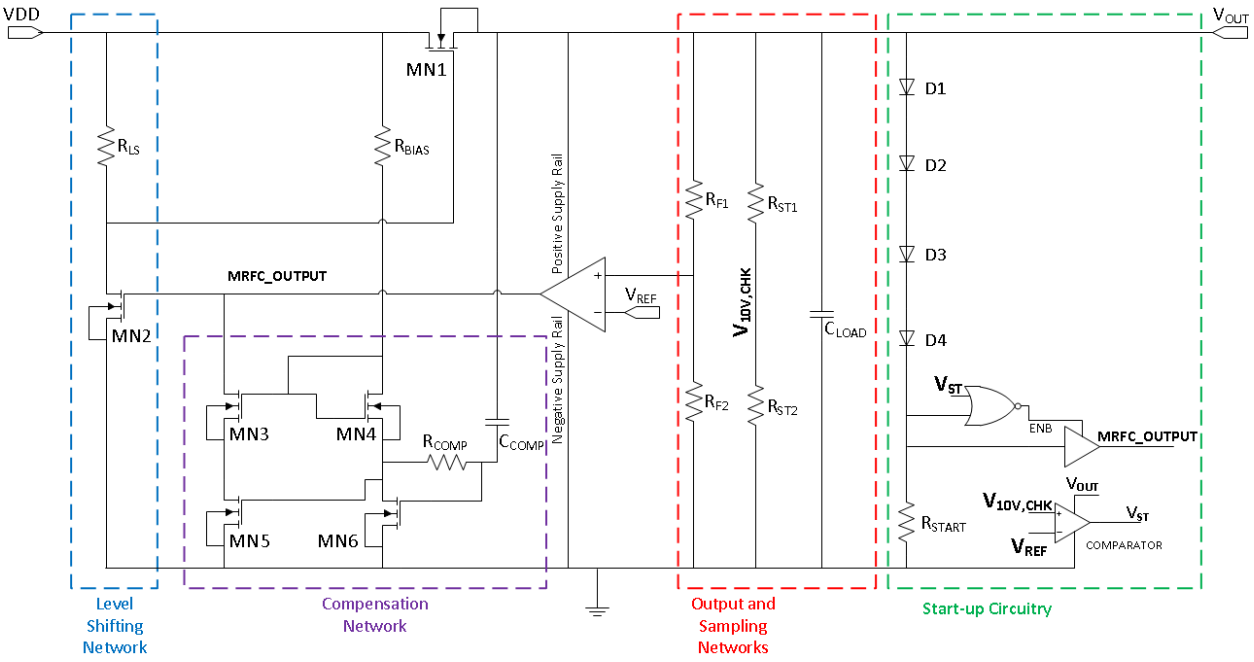

Fig. 4.34. The schematic of the fully on-chip linear regulator with an NFET pass device.

of the Vulcan II's pass device. With respect to the frequency response, the design targets a minimum PM of 45º for all operating conditions.

The process and temperature variation observed in the HiTSiC® resistors make it imperative to limit the design's dependence on resistance values. Inserting R_{COMP} into the system, for example, yields an improved PM and a decrease in UGBW as it pushes a zero near the unity-gain frequency to lower frequencies. System stability is not critically dependent upon $R_{COMP,}$ but is slightly improved by it. From an efficiency and power budget perspective, perhaps the most critical component in the system given the process and temperature variation observed in SiC IC technology is R_{IBIAS}. This sets the current flowing through the differentiator and lower values of R_{IBIAS} create a proportionally lower resistance path to ground from the op-amp's output. Selecting the lowest temperature coefficient resistor available while also making a longer and wider device is one approach to mitigating variation.

Preliminary simulations indicated that for certain operating conditions the linear regulator either had a long start-up time (greater than 100 μs) or never reached the target 15 V output. Under these simulation conditions, the output of the regulator was less than 10 V. The start-up circuitry shown in Fig. 4.34 was implemented to eliminate this issue. With a drop of approximately 2 V per diode and a V_{THN} of 2 V, the start-up circuit detects when the output is below 10 V. If the output is below 10 V, then the start-up circuit provides a digital low to the level shifting NFET (MN2) to turn it off. This applies the full input voltage to the NFET pass transistor (MN1) and ensures the system turns on properly. Due to using a tri-state buffer, the start-up circuit's output goes into a high impedance state once the output transitions above 10 V and does not impact the regulator's performance. Inserting an enable pin to momentarily short the input and output is another solution.

Table 4.9. The device sizes used in the fully on-chip NFET based linear regulator.

Component	Device Size	Comment
MN1	20 µm / 1.2 µm (m = 1,500)	NFET pass transistor
MN2 – MN6	20 µm / 1.2 µm (m = 8)	Level shifting, differentiator
R_{LS}	25 kΩ	Level shifting
R_{IBIAS}	100 kΩ	Biasing - differentiator
R_{COMP}	7.5 kΩ	Compensation - differentiator
R_{F1}	240 kΩ	Feedback network (sampling)
R_{F2}	60 kΩ	Feedback network (sampling)
R_{ST1}	210 kΩ	Start-up circuit (sampling)
R_{ST2}	90 kΩ	Start-up circuit (sampling)
R_{START}	200 kΩ	Start-up circuit
C_{COMP}	24 pF	Compensation - differentiator
C_{LOAD}	90 pF	Output capacitor

The fully on-chip NFET based linear regulator's device sizes are listed in Table 4.9. The component sizing used in the multipath RFC are provided in Table 4.7, although C_C has been increased to 66 pF to further split the op-amp's 1st and 2nd poles. The comparator used in the start-up circuit is a modified version of the design in [11] and is discussed later in Section 4.3.6. The gates used in conjunction with the tri-state buffer have a pull-up to pull-down ratio of 4:1, a minimum NFET width of 4 µm along with a PFET width of 20 µm, and use a length of 1.2 µm.

The frequency response of the fully on-chip linear regulator across all operating temperatures is shown in Fig. 4.35 for an input voltage of 20 V and a load current of 50 mA. The low-frequency gain reaches a maximum of 73 dB at 300 ºC and decreases to a minimum of 52 dB at 25 ºC. Pole splitting due to indirect compensation within the op-amp has resulted in the system

behaving similar to a single pole system until the unity-gain frequency. The UGBW for each temperature exceeds 1 MHz with the exception for 300 ºC (TT) which reaches the unity-gain frequency at 830 kHz.

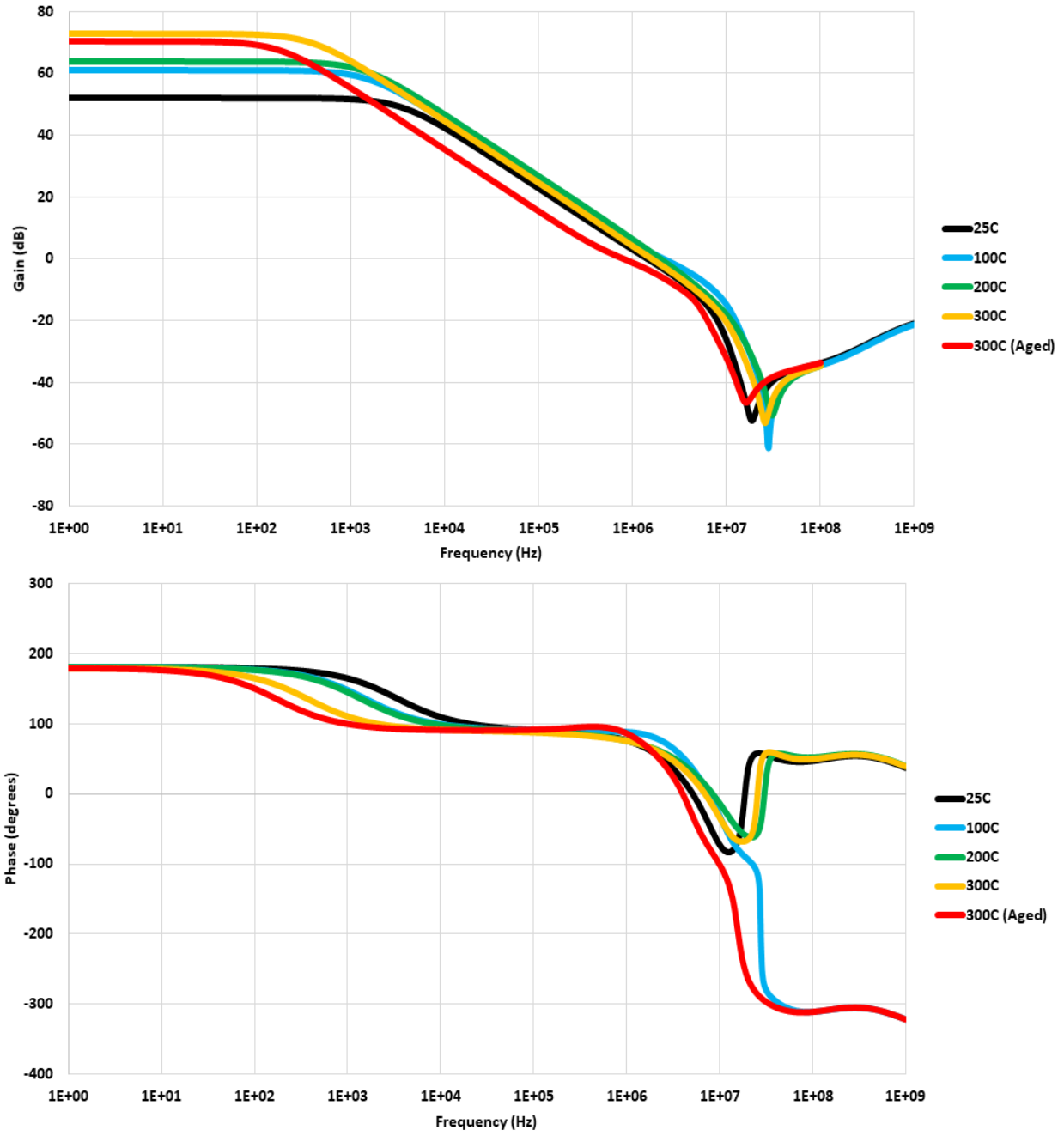

Fig. 4.35. The frequency response of the fully on-chip NFET linear regulator for V_{IN} = 20 V and I_{LOAD} = 50 mA across the operating temperature range.

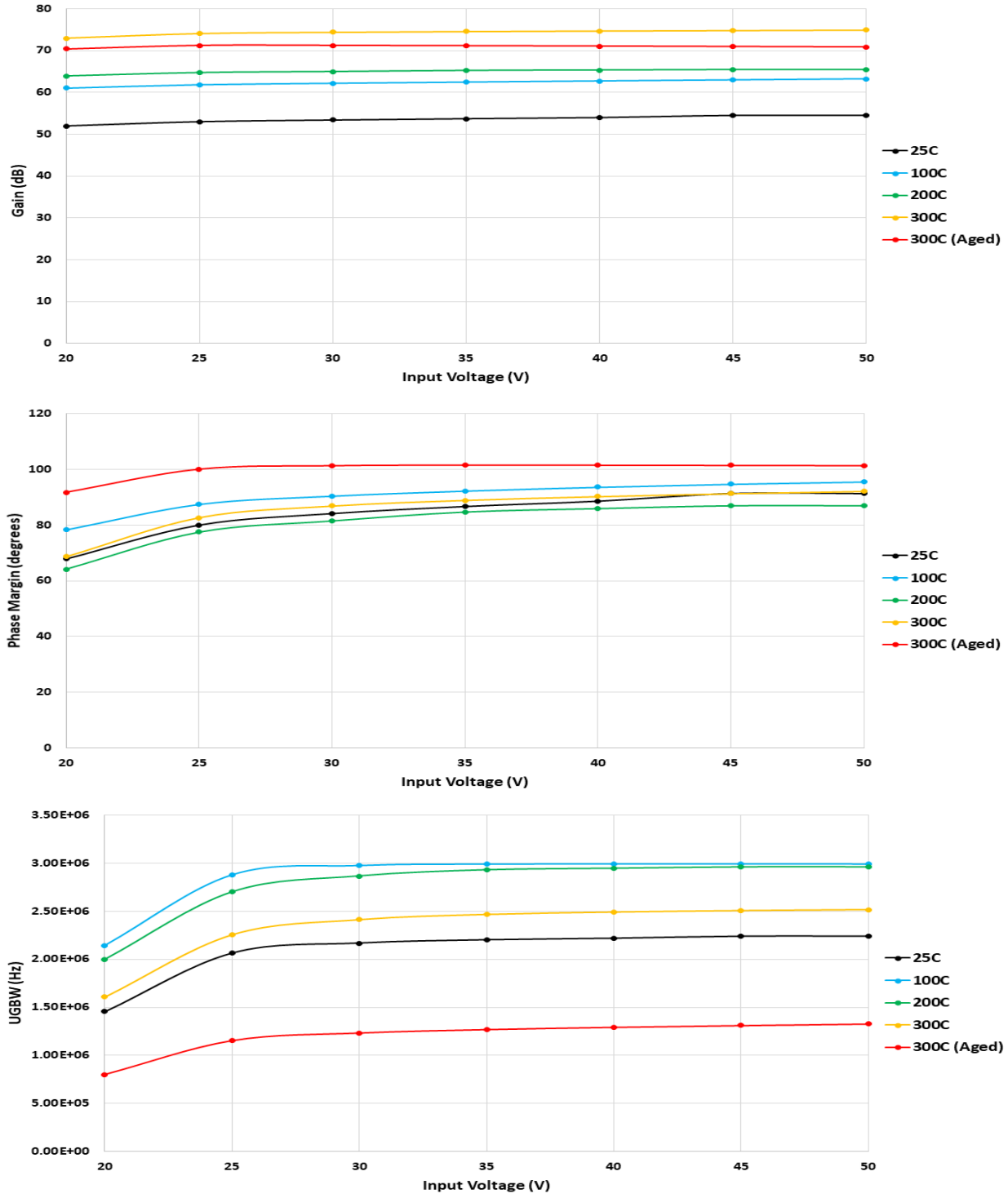

Fig. 4.36. The low-frequency gain, PM, and UGBW of the fully on-chip NFET linear regulator with an I_{LOAD} = 50 mA across the temperature range.

The low-frequency gain, PM, and UGBW are shown in Fig. 4.36 for each temperature, an input voltage range of 20 V to 50 V, and a load current of 50 mA. The same frequency parameters

are subsequently shown in Fig. 4.37 at 300 ºC (TF) over the input voltage range for various load currents.

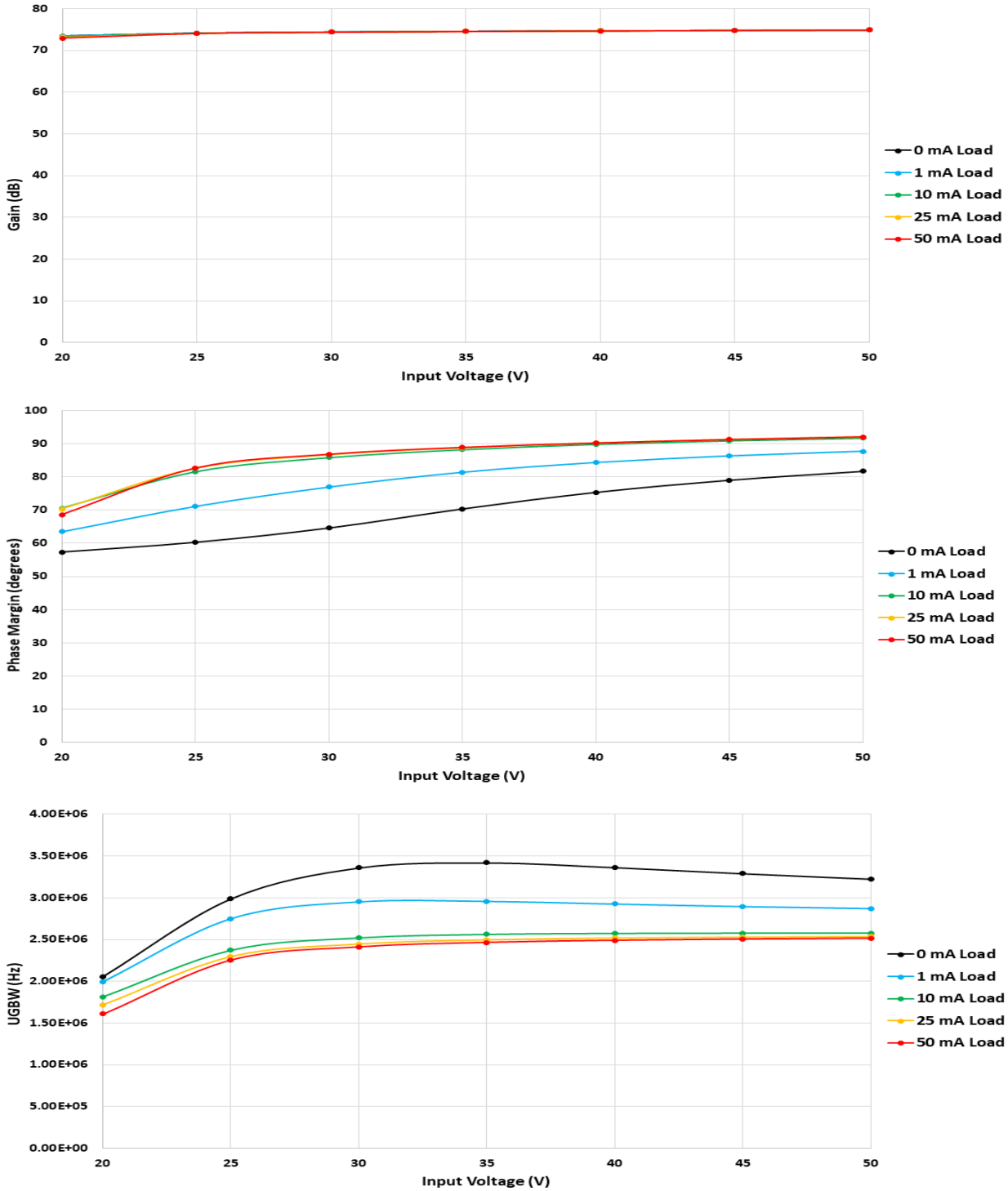

Fig. 4.37. The low-frequency gain, PM, and UGBW of the fully on-chip NFET linear regulator for various load currents over the input voltage range at 300 ºC (TF).

The low-frequency gain of the linear regulator is shown to be proportional to temperature in Fig. 4.36 and then constant with different load currents in Fig. 4.37. During the op-amp design, the trend of gain was found to be somewhat ambiguous between 100 ºC and 300 ºC. However, the increase in gain over temperature generally follows expectations that the g_m value will go up faster than the r_o value will decrease. Due to the total system gain being a product of the gain of each stage, the relatively high gain for 300 ºC (TT) in Fig. 4.36 indicates that the op-amp is no longer hitting a supply voltage headroom as shown in Fig. 4.29. The gain of the regulator being stable for various load currents in Fig. 4.37 is expected since the gain of the common-drain pass NFET is ideally the only factor that will change.

A decrease in output resistance of the pass device for higher load currents causes a pole near the unity-gain frequency to shift to lower frequencies as expressed by (4.14), where the output resistance is considered in place of R_{ESR}. This leads to the unity-gain frequency being the highest at lower load currents, as shown in Fig. 4.37, and then trending downwards as load current increases. As the pole near the unity-gain frequency is pushed outwards for lower load currents, parasitic poles begin impacting the system's frequency response and result in a decrease in PM.

The PSRR of the NFET based linear regulator is shown in Fig. 4.38. Considering a supply ripple frequency of 60 Hz, the maximum PSRR value reaches 96.0 dB at 300 ºC for the 50 mA load while the minimum value is 75.6 dB at 25 ºC. The design benefits substantially from not only the high gain multipath RFC, but also the configuration of the topology. One influencing factor is the use of the level shifting transistor (MN2) in a common-source configuration without also using a source degeneration resistor. A second factor is that the op-amp uses the output of the regulator as its supply and is shielded from power supply ripple to a degree. This allows the system to

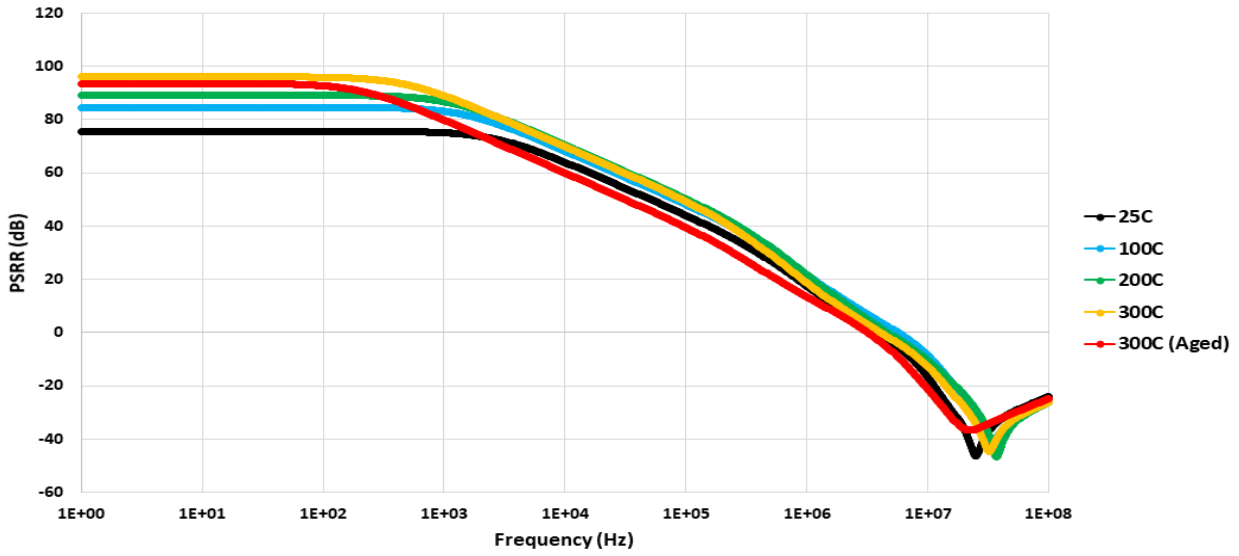

Fig. 4.38. The PSRR of the fully-on chip linear regulator for V_{IN} = 25 V and I_{LOAD} = 50 mA over the operating temperature range.

outperform the multipath RFC's stand-alone PSRR given in Fig. 4.32. For a comparison to a commercially available linear regulator, the datasheet for Texas Instrument's UA78L15 linear regulator reports a typical PSRR of 39 dB for a 120 Hz ripple frequency [69].

The transient response of the linear regulator at 300 ºC (TF) for a continuous load current of 25 mA, a pulsed load current of 25 mA, and an input voltage of 25 V is shown in Fig. 4.39. The load pulse has rise and fall times of 10 ns. The time taken to reach the 14.85 V to 15.15 V nominal output band after a disturbance, or the 1% settling time, is 0.27 µs on the load's rising edge and 0.61 µs on its falling edge. The output undershoots to 14.10 V and then overshoots to 15.78 V during the load transient, despite the 10 ns rise/fall times, and keeps the regulator within 10% of its nominal value without the need for a discrete load capacitor.

Similarly, Fig. 4.40 shows the transient response of the regulator at 300 ºC (TF) for a pulsed load current of 50 mA, no continuous load current, and an input voltage of 25 V. The larger pulsed load and 10 ns rise/fall times result in an undershoot to 11.85 V and an overshoot to 16.8 V. The

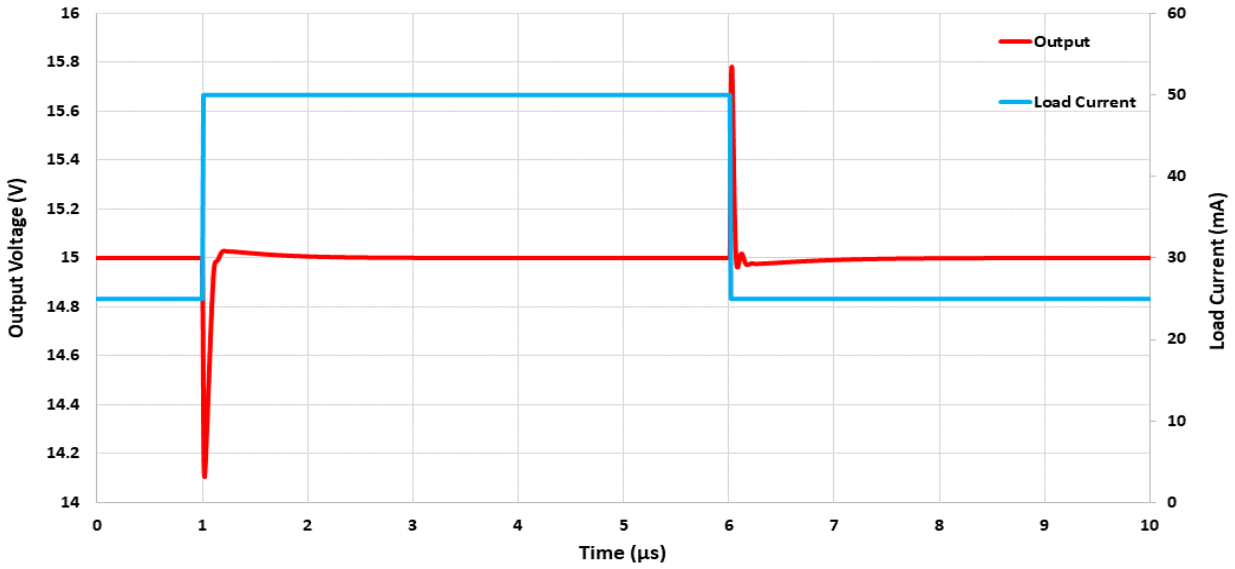

Fig. 4.39. The transient response of the fully on-chip NFET linear regulator at 300 °C (TF) for V_{IN} = 25 V, a $I_{LOAD,CONT}$ = 25 mA, and a I_{PULSE} = 25 mA.

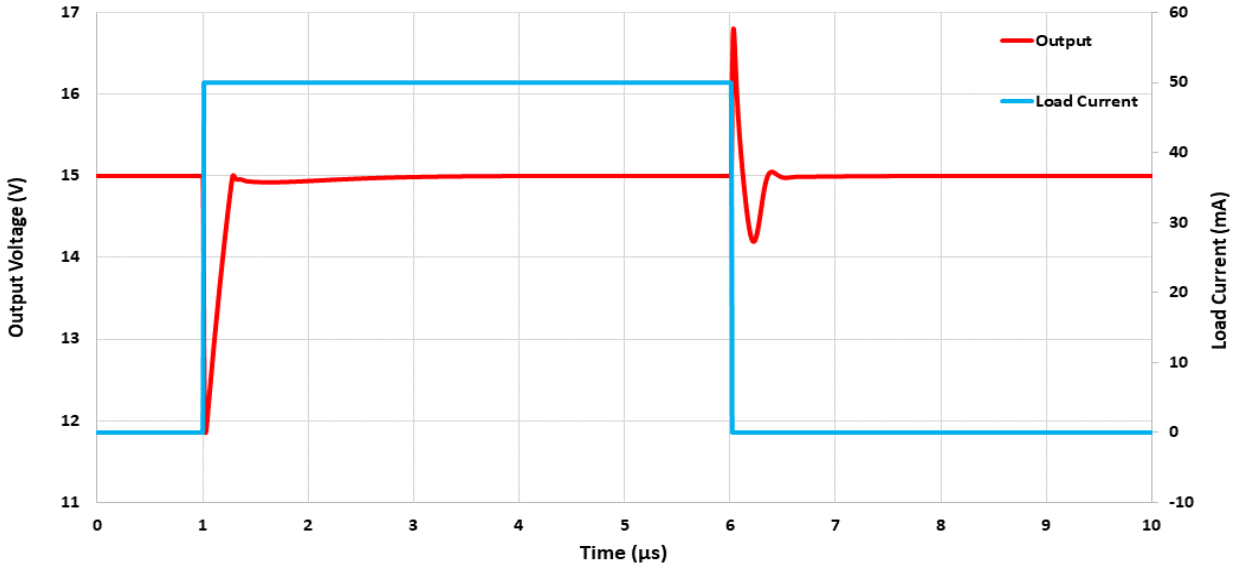

Fig. 4.40. The transient response of the fully on-chip NFET linear regulator at 300 °C (TF) for V_{IN} = 25 V, a $I_{LOAD,CONT}$ = 0 mA, and a I_{PULSE} = 50 mA.

regulator is able to quickly response with a 1% settling time of 0.26 µs on the load's rising edge and 0.64 µs on its falling edge. If the application is anticipated to have sudden no load to full load, such as with a 10 ns rise and fall time, then a larger on-chip load capacitor (e.g. 500 pF) can be justified. However, this will cause a high frequency pole to shift towards the unity-gain frequency.

The line regulation of the NFET based linear regulator is provided in Table 4.10 for an input voltage range of 20 V to 50 V and over the operating temperature range. Line regulation is inversely proportional to the regulator's gain and proportional to load current, as specified by equation (4.9), thus the trends shown in Table 4.10 meet expectations. Drawing a comparison to Texas Instrument's UA78L15 linear regulator which has a maximum current of 100 mA and an input voltage range of 17.5 V to 30 V, the fully on-chip linear regulator achieves line regulation performance that is approximately 1 to 2 orders of magnitude lower and therefore superior [69].

The load regulation of the fully on-chip linear regulator also outperforms the silicon based counterpart as shown in Table 4.11. As indicated by expression (4.8), the load regulation is inversely proportional of the linear regulator's gain and has improved performance for higher input voltages. In comparison to TI's UA78L15 regulator, the fully-on chip regulator achieves superior performance by at least 1 order of magnitude and nearly 3 orders of magnitude at 300 ºC.

Table 4.10. The line regulation of the fully on-chip NFET based linear regulator over temperature for V_{IN} = 20 V to 50 V compared to TI's UA78L15 linear regulator.

Load Current	25 ºC	100 ºC	200 ºC	300 ºC (TF)	300 ºC (TT)	Texas Instruments UA78L15*
0 mA	0.625 mV/V	0.238 mV/V	0.135 mV/V	0.059 mV/V	0.081 mV/V	5.8 mV/V Typical
1 mA	0.628 mV/V	0.239 mV/V	0.136 mV/V	0.059 mV/V	0.081 mV/V	
5 mA	0.633 mV/V	0.240 mV/V	0.137 mV/V	0.060 mV/V	0.082 mV/V	
10 mA	0.639 mV/V	0.241 mV/V	0.138 mV/V	0.060 mV/V	0.083 mV/V	
25 mA	0.652 mV/V	0.244 mV/V	0.141 mV/V	0.062 mV/V	0.085 mV/V	
50 mA	0.670 mV/V	0.248 mV/V	0.144 mV/V	0.063 mV/V	0.087 mV/V	

*Test conditions: V_{IN} = 20 V to 30 V, I_{LOAD} = 40 mA, junction temperature (T_J) = 25 ºC

Table 4.11. The load regulation of the fully on-chip NFET based linear regulator over temperature for I_{LOAD} = 0 mA to 50 mA compared to TI's UA78L15 linear regulator.

Input Voltage	25 ºC	100 ºC	200 ºC	300 ºC (TF)	300 ºC (TT)	Texas Instruments UA78L15*
20 V	36.9 mV/A	8.46 mV/A	6.78 mV/A	3.49 mV/A	5.00 mV/A	385 mV/A Typical
25 V	21.3 mV/A	5.03 mV/A	3.81 mV/A	1.72 mV/A	2.41 mV/A	
30 V	17.3 mV/A	4.30 mV/A	3.02 mV/A	1.31 mV/A	1.88 mV/A	
35 V	14.6 mV/A	3.44 mV/A	2.55 mV/A	1.08 mV/A	1.60 mV/A	
40 V	12.4 mV/A	3.23 mV/A	2.19 mV/A	0.93 mV/A	1.39 mV/A	
45 V	10.7 mV/A	3.00 mV/A	1.90 mV/A	0.81 mV/A	1.23 mV/A	
50 V	9.44 mV/A	2.64 mV/A	1.66 mV/A	0.73 mV/A	1.13 mV/A	

*Test conditions: V_{IN} = 23 V, I_{LOAD} = 1 mA to 40 mA, junction temperature (T_J) = 25 ºC

The quiescent current of the NFET based linear regulator is shown in Fig. 4.41. Although the design goal of less than 3.0 mA at 300 ºC is achieved, the quiescent current does increase at lower temperatures. The resistance connected between the input and the drain of the level shifting FET is a driving factor for the seemingly inconsistent trend. At 25 ºC, for example, the resistance is 25 kΩ and then increases over temperature to its maximum of 46.7 kΩ at 300 ºC. This is opposite

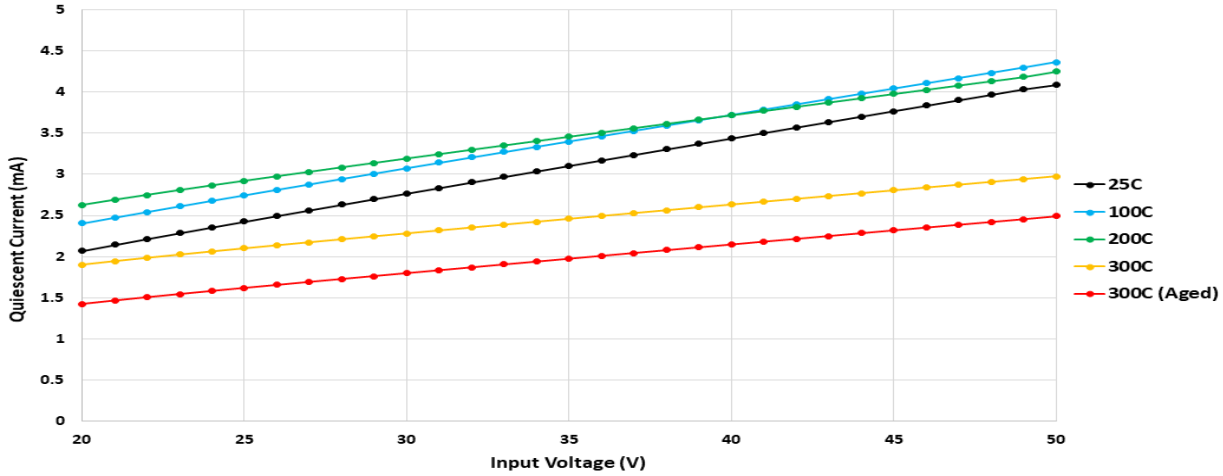

Fig. 4.41. The quiescent current of the fully on-chip NFET based linear regulator for each operating temperature and an I_{LOAD} = 0 mA.

of the observed trend for HiTSiC® resistances formed with poly, which can decrease substantially (-50% of the nominal value has been observed) over temperature. The current consumption of the op-amp is another factor for the quiescent current trends. The level shifting NFET (MN2) has a lower V_{THN} at higher voltages, but the pass transistor (MN1) also has a lower V_{THN}. Therefore, it's not straightforward to determine the voltage required from the output stage of the multipath RFC which makes the current through the output stage difficult to predict.

The dropout voltage of the fully on-chip linear regulator's NFET pass transistor is shown in Fig. 4.42. As stated at the beginning of the section, a safety margin is added to the design such that the maximum load current of 50 mA can be provided for a 19 V input at 25 ºC. At 300 ºC, ignoring aging effects, the dropout voltage reduces to approximately 3.2 V.

A summary of the fully on-chip SiC linear regulator results is given in Table 4.12 along with a comparison to external capacitor-less silicon based parts. The SiC regulator has a higher quiescent current than the two silicon parts due to factors such as a larger feature size and increased

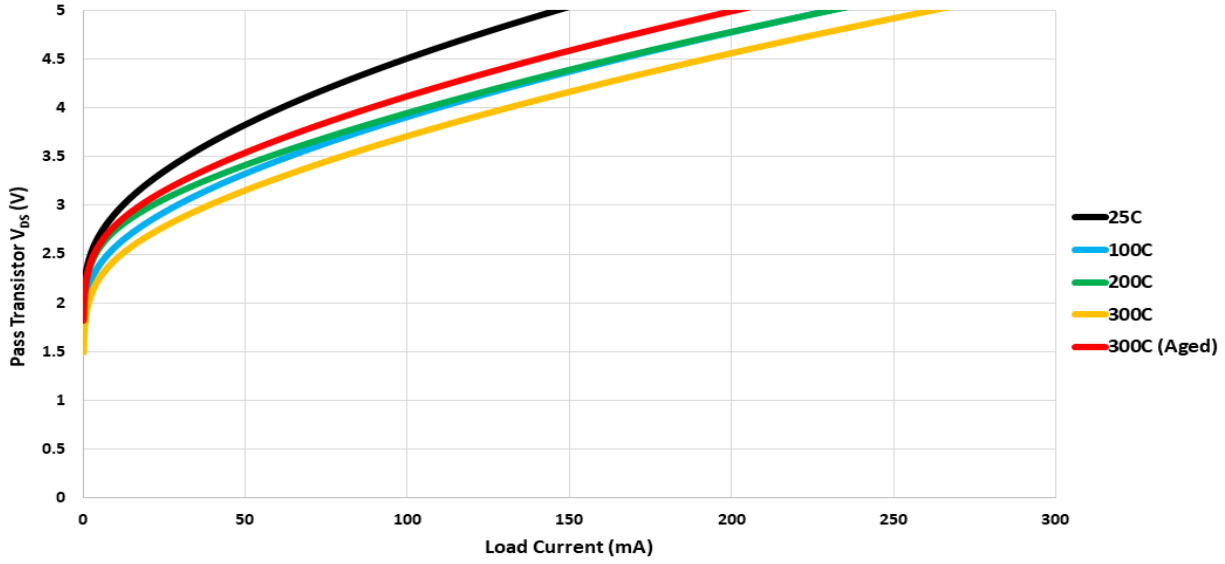

Fig. 4.42. The dropout voltage (V_{DS}) of the fully on-chip linear regulator's NFET pass transistor over temperature.

threshold voltage, but it is competitive in every other listed metric. For frequency response parameters, it outperforms or matches [60] in every case except for the gain at 25 ºC. While [60] does report undershoot and overshoot values of 90 mV (3.2%), the test setup uses 1 µs rise and fall times for the load pulse. Extending the rise and fall times to 1 µs for the SiC linear regulator in this section, rather than the 10 ns initially used, limits the undershoot/overshoot to no more than +/- 0.5 V (3.3%). Finally, the fully on-chip SiC linear regulator outperforms TI's TPS731 by more than an order of magnitude for load regulation and also has superior line regulation at 300 ºC.

Table 4.12. A summary of the fully on-chip NFET linear regulator and a comparison to silicon based parts.

Parameter	Test Condition (this work only)	25ºC (TF)	300 ºC (TF)	300 ºC (TT)	Fully On-Chip Silicon Regulator [60]	Texas Instruments TPS731 (Cap-Free) [70]
DC Loop Gain	**I_{LOAD} = 50 mA, V_{IN} = 25 V**	53.0 dB	74.0 dB	71.1 dB	62 dB	N/A
Phase Margin		80.0º	82.6º	100º	50º (min. value)	N/A
Bandwidth		2.06 MHz	2.25 MHz	1.15 MHz	220 kHz (min. value)	N/A
PSRR	**F = 100 Hz, I_{LOAD} = 0 mA, V_{IN} = 25 V**	75.6 dB	95.9 dB	92.6 dB	57 dB (@ 1 kHz)	58 dB (@ 100 Hz)
$I_{QUIESCENT}$	**I_{LOAD} = 0 mA, V_{IN} = 25 V**	2.4 mA	2.1 mA	1.6 mA	0.065 mA	0.4 mA
Overshoot ΔV_{OUT}	**ΔI_{LOAD} = 50 mA, V_{IN} = 25 V (full load transient)**	2.16 V	1.80 V	2.11 V	N/A	N/A
Undershoot ΔV_{OUT}		3.22 V	3.14 V	3.48 V	N/A	N/A
1% Settling Time		0.23 µs	0.26 µs	0.41 µs	3 µs (full load transient)	2 µs (full load transient)
Line Regulation	**ΔV_{IN} = 20 V to 50 V, I_{LOAD} = 50 mA**	0.670 mV/V	0.063 mV/V	0.085 mV/V	N/A	0.35 mV/V
Load Regulation	**ΔI_{LOAD} = 50 mA V_{IN} = 25 V**	21.3 mV/A	1.72 mV/A	2.41 mV/A	N/A	70 mV/A

4.2.3 Fully On-Chip PFET Pass Transistor Based Linear Regulator

For applications that can utilize a multi-chip module, a PFET pass transistor based linear regulator is an alternative to its NFET based counterpart. To avoid body effect, the linear regulator must be sub-diced such that any circuitry connected to the output no longer shares a common substrate with the regulator. The intended role of a PFET based linear regulator is in applications where the input voltage headroom is relatively low compared to the desired output voltage. Its ability to lower the dropout voltage versus the NFET based regulator is a result of the V_{GS} magnitude available to drive the pass transistor being limited by only the supply rails.

The proposed schematic of the fully on-chip PFET based linear regulator is presented in Fig. 4.43. The design targets a maximum load current of at least 50 mA, a minimum phase margin of 45º, and an input voltage range of 17.5 V to 30 V at 25 ºC. To account for an additional 1 V safety margin for the supply headroom, the PFET pass device is selected to have an effective width of 10,000 μm / 1.2 μm. The dropout voltage of the linear regulator is plotted across temperature in

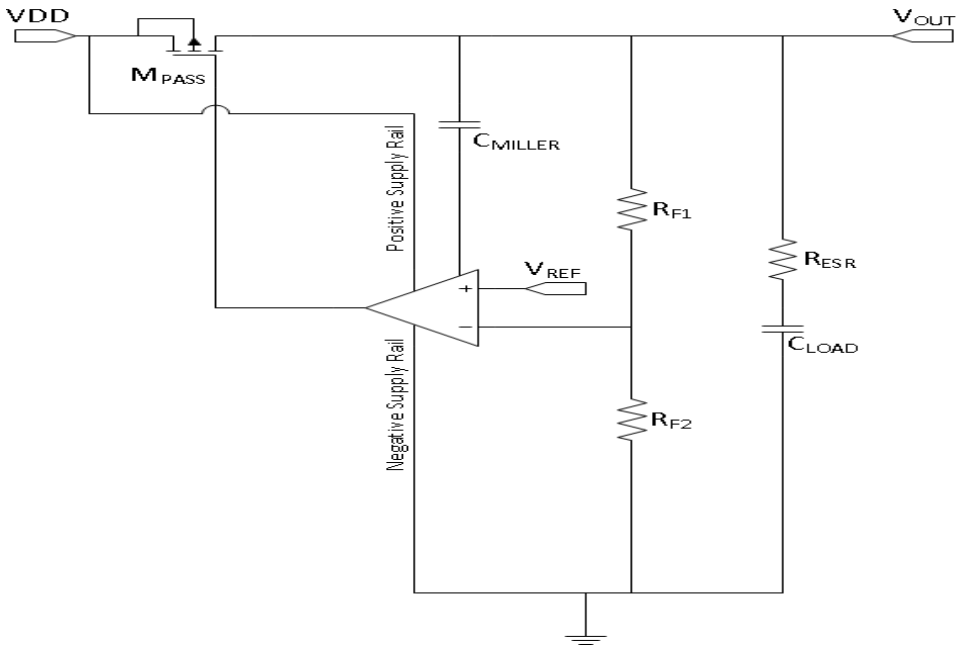

Fig. 4.43. The schematic of the fully on-chip linear regulator with a PFET pass device.

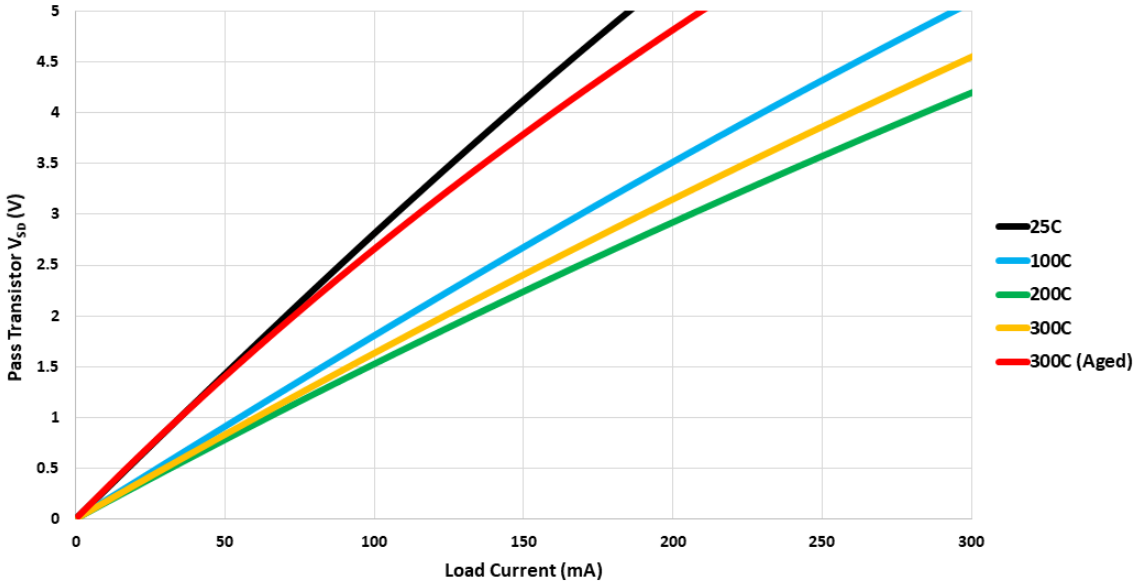

Fig. 4.44. The dropout voltage (V_{SD}) of the fully on-chip linear regulator's PFET pass transistor over temperature for a W/L = 10,000 µm / 1.2 µm.

Fig. 4.44. At 100 ºC and above, the linear regulator achieves a dropout voltage of below 1 V. Aged models at 300 ºC provide an exception to this since the threshold voltage begins to increase towards the typical values at 25 ºC.

As opposed to inserting a large output capacitor to create a dominant pole that effectively compensates the loop and ensures stability, the goal of this design is to internally compensate the system. As with the fully on-chip NFET based linear regulator, the dominant pole must now be at the op-amp's output. With the added gain from the common source amplifier, the open-loop gain is often intentionally reduced to avoid having the unity-gain frequency (f_{0dB}) extend out to the parasitic pole region (approximately 10 MHz). As stated in [71], the system's open-loop gain is generally made to be between 40 dB and 50 dB which subsequently drops the f_{0dB} for the same 3dB frequency (f_{3dB}) to mitigate the impact of parasitic poles on loop stability.

Since the loop gain is a product of each stage, the multipath RFC presents a problem in that it can increase the regulator's low-frequency gain to beyond 90 dB and result in a f_{0dB} that falls

within the parasitic pole region if not properly compensated for. A compromise is to reduce the multipath RFC to a single stage at the cost of lower gain and potentially a severe degradation of line and load regulation. However, it reduces design complexity with respect to the compensation scheme since the multipath RFC becomes an OTA with the output being the only high impedance node in the system other than the inputs. If the two-stage multipath RFC had been used, then the typically dominant pole at the output of the op-amp's 1st stage would be within a decade of the pole at the output of its 2nd stage due to the relatively large input capacitance of the pass transistor.

The compensation scheme can now be implemented with pole splitting techniques and by introducing pole-zero pairs in which a relatively low frequency pole causes the gain to roll off quicker while a higher frequency zero acts to recover the phase. Leveraging the gain of the pass transistor, a common source amplifier, Miller's theorem can be indirectly applied by connecting a capacitance between the regulator's output and the source of MP12 as shown in Fig. 4.45. Compared to connecting the Miller capacitance directly to the op-amp's output, this eliminates the reliance upon a nulling resistor and the possibility of a RHP zero that degrades stability.

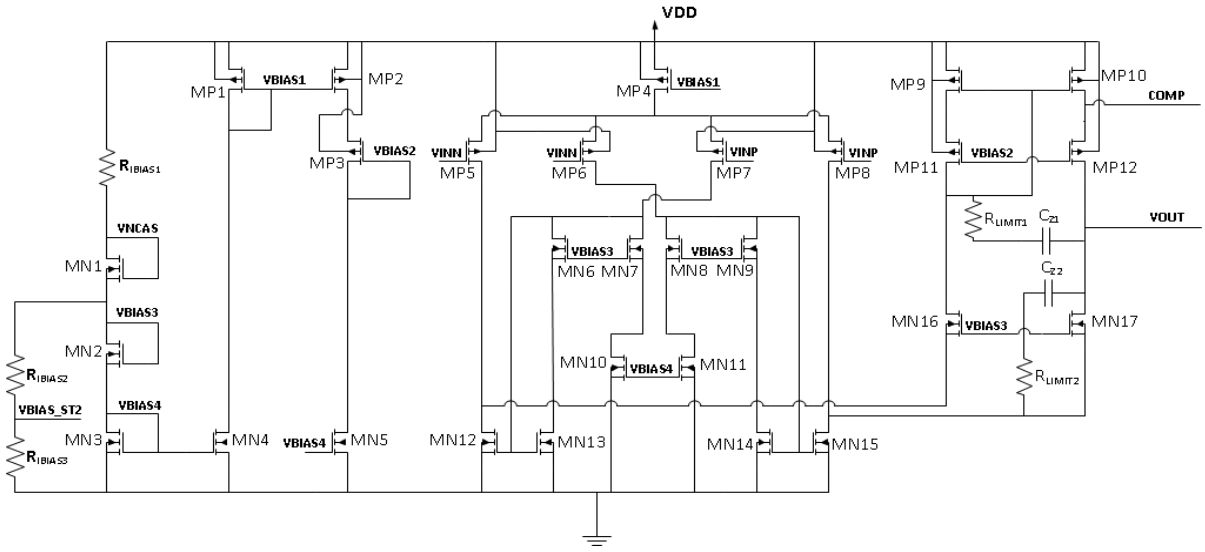

Fig. 4.45. The multipath RFC op-amp schematic modified for the PFET linear regulator.

Introducing pole-zero pairs, specifically R_{LIMIT1}-C_{Z1} and R_{LIMIT2}-C_{Z2}, further compensates the system. Both C_{Z1} and C_{Z2} feed forward in-phase signals from the differential pair to the output of the 1st stage, but neither has a current surpassing MP12's or MN17's when the current limiting resistors are inserted and no feedforward zeroes occur. The result is that C_{Z1} shunts the op-amp's output resistance and the associated $1/g_m$ resistance of MP9 at a pole location slightly beyond f_{3dB}. The same applies to C_{Z2}, although the $1/g_m$ resistance it shunts is MN17's. The current through $C_{Z1,2}$ is then limited by $R_{LIMIT1,2}$ which forms an in-phase LHP zero. The zeroes are located prior to the f_{0dB} point if $C_{Z1,2}$ are appropriately sized and $R_{LIMIT1,2}$ are large enough that the feedforward currents do not exceed the current flowing through MP12 or MN17. Therefore, the poles accelerate the fall of the gain and the LHP zeroes recover the phase lost prior to the f_{0dB}.

The sizes of the components in the fully on-chip PFET based linear regulator are given in Table 4.13 along with relevant changes to the multipath RFC. The lower sampling network resistances improve the PM by decreasing the output resistance of the pass transistor and shifting the output pole to higher frequencies according to equation (3.2), but add quiescent current.

Table 4.13. The component sizes of the PFET based regulator.

Component	Device Size	Comment
M_{PASS}	20 µm / 1.2 µm (m = 500)	PFET pass transistor
R_{F1}	12 kΩ	Sampling network
R_{F2}	48 kΩ	Sampling network
R_{ESR}	250 Ω	ESR resistance – adds zero determined by equation (3.5)
R_{Z1}, R_{Z2}	7.5 kΩ	Compensation
C_{Z1}, C_{Z2}	60 pF	Compensation
C_{MILLER}, C_{LOAD}	90 pF	Compensation, load capacitance

The frequency response of the PFET based linear regulator is shown in Fig. 4.46 for an input voltage of 20 V and a 50 mA load. The response is characteristic of a single pole system until the unity-gain frequency due to the dominant pole formed by the indirect compensation technique. The pole-zero pairings first introduce a zero near the unity-gain frequency, recovering phase lost from the dominant pole, then introduce a pole to kill off the gain. The low-frequency gain decreases over temperature similar to the multipath RFC and NFET based linear regulator, with a maximum value of 70.4 dB at 300 ºC (TF) and a minimum value of 53.5 dB at 25 ºC.

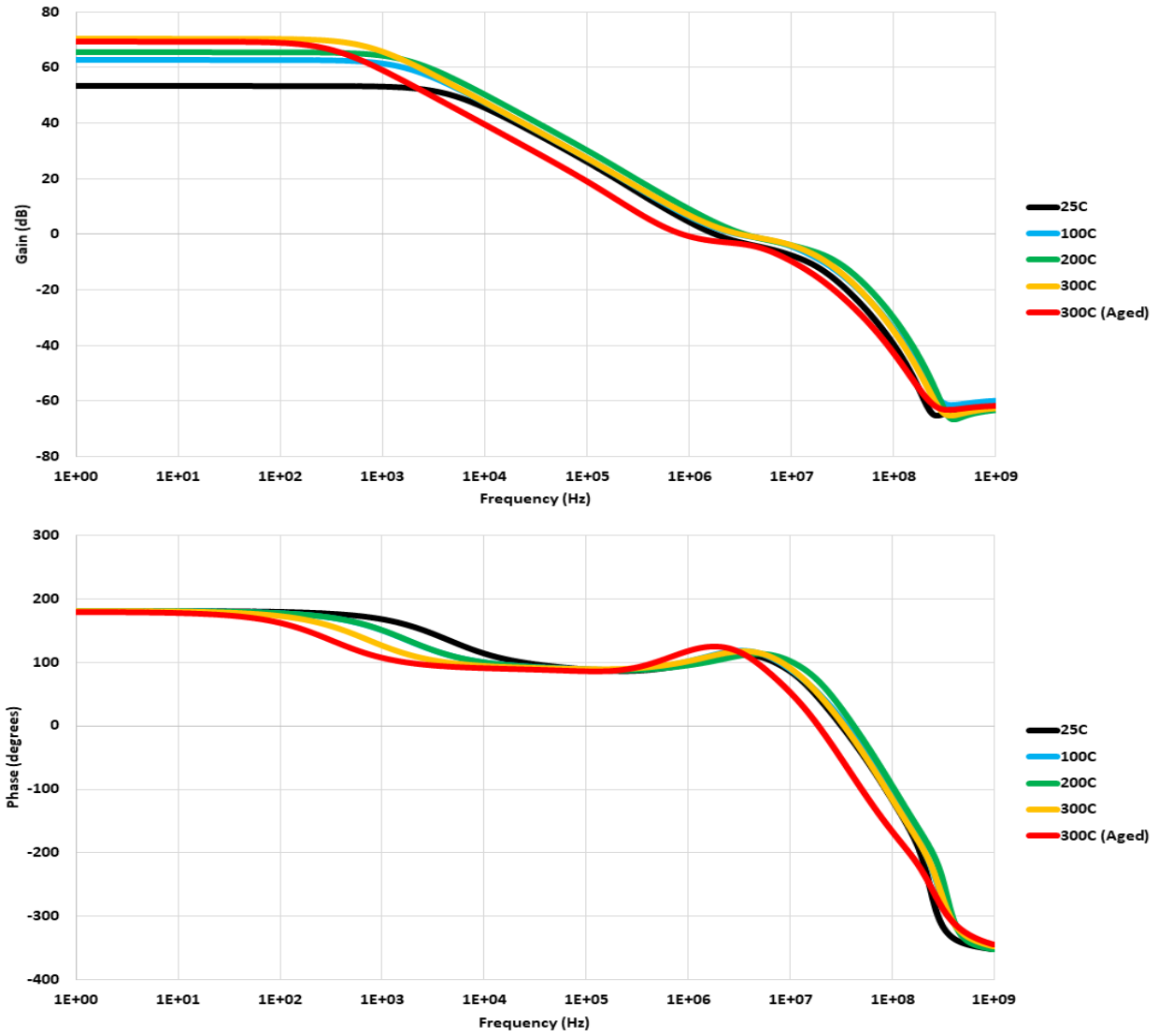

Fig. 4.46. The frequency response of the fully on-chip PFET based linear regulator for V_{IN} = 20 V and I_{LOAD} = 50 mA across the operating temperature range.

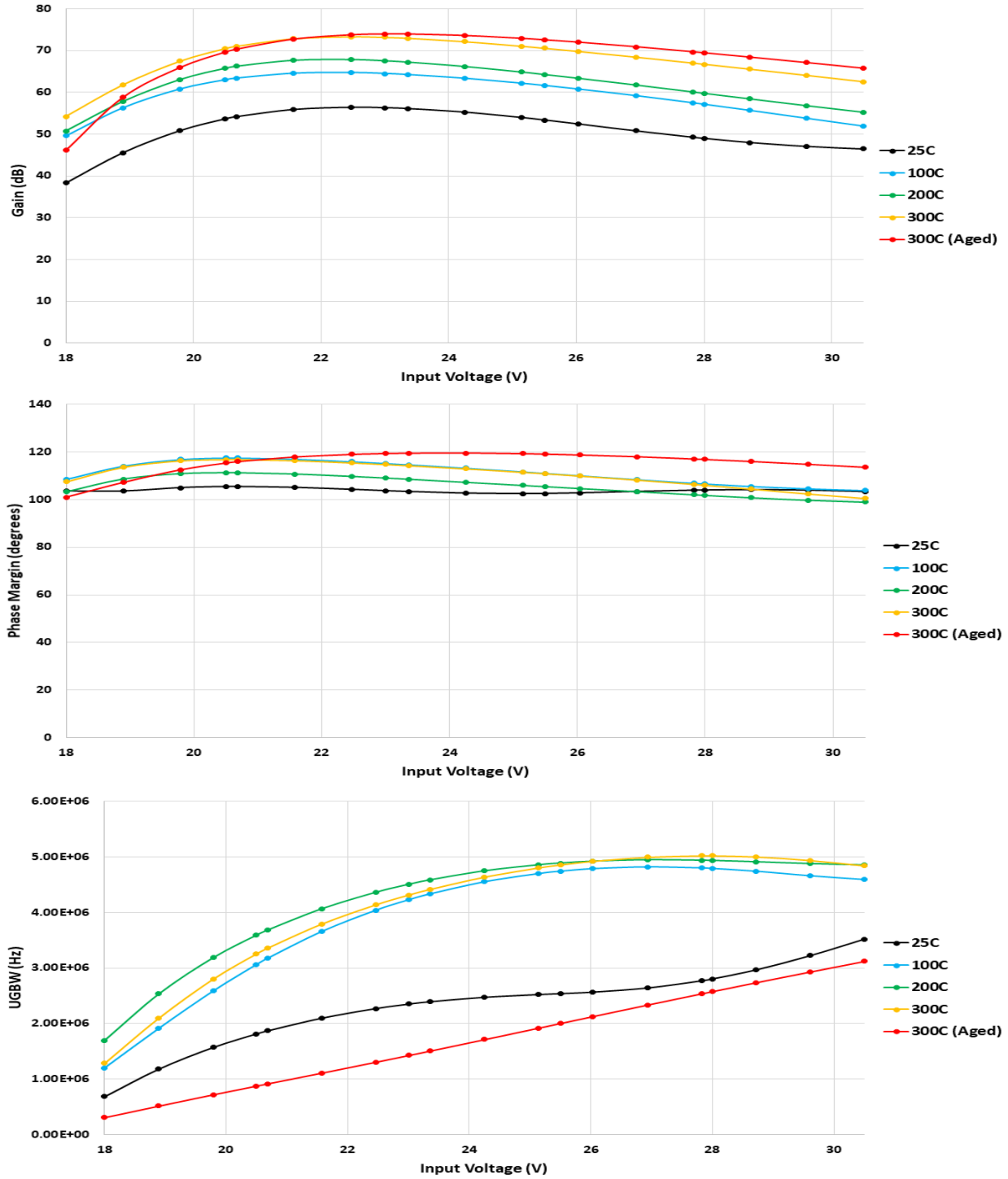

Fig. 4.47. The low-frequency gain, PM, and UGBW of the fully on-chip PFET linear regulator with an I_{LOAD} = 50 mA across the temperature range.

The low-frequency, PM, and UGBW are shown across temperature in Fig. 4.47 for a load of 50 mA load. The gain of the regulator rises until about 22 V as the pass transistor saturates, then

begins to decline due to the op-amp's bias current increasing with the input voltage. The UGBW also increases with input voltage due to the op-amp's bias current increasing.

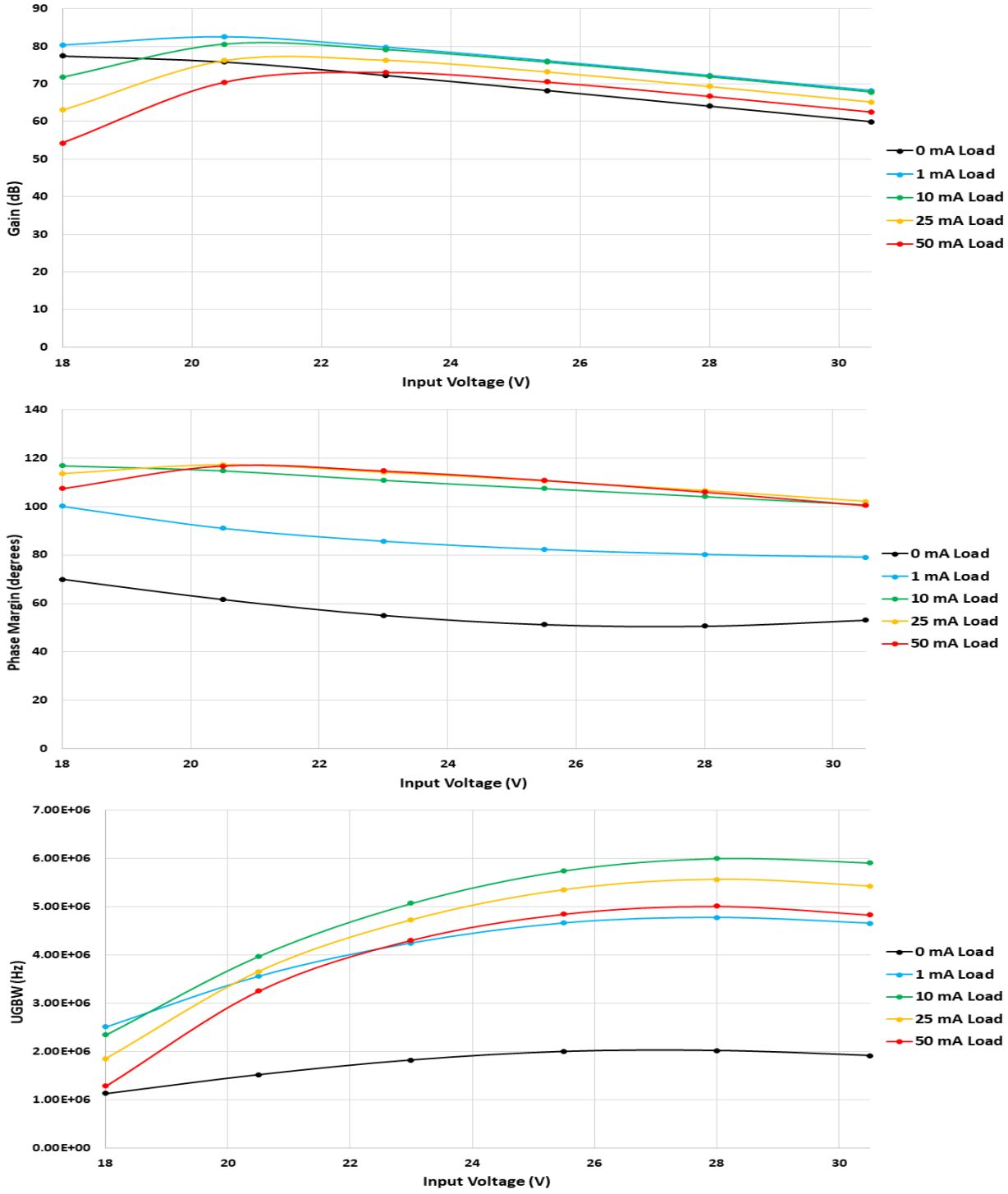

Fig. 4.48. The low-frequency gain, PM, and UGBW of the fully on-chip PFET linear regulator for various load currents over the input voltage range at 300 ºC (TF).

In Fig. 4.48 on the previous page, the low-frequency gain, PM, and UGBW are shown for different input voltages and load currents. The gain generally decreases for a higher load current because the load acts a source degeneration resistance. On the contrary, the PM rises with load current as the output resistance of the pass transistor drops and pushes the output pole to higher frequencies. The UGBW has a minimum at 0 mA load due to the relatively low frequency output pole, while the behavior at other loading conditions becomes more complex due to the compensation scheme's impact.

The PSRR of the PFET linear regulator is shown in Fig. 4.49 for a 20 V input and a load of 50 mA. Outside of the 200 ºC case, the PSRR underperforms versus the NFET linear regulator. This is a result of the op-amp drawing its supply voltage directly from the input. However, the regulator's PSRR value for all temperatures still exceeds the commercially available UA78L15 linear regulator that is stated as having a PSRR of 39 dB at 120 Hz [69].

The transient response of the PFET linear regulator is shown in Fig. 4.50 for a continuous load current of 25 mA in addition to 25 mA pulses at 300 ºC and an input voltage of 25 V. The 1%

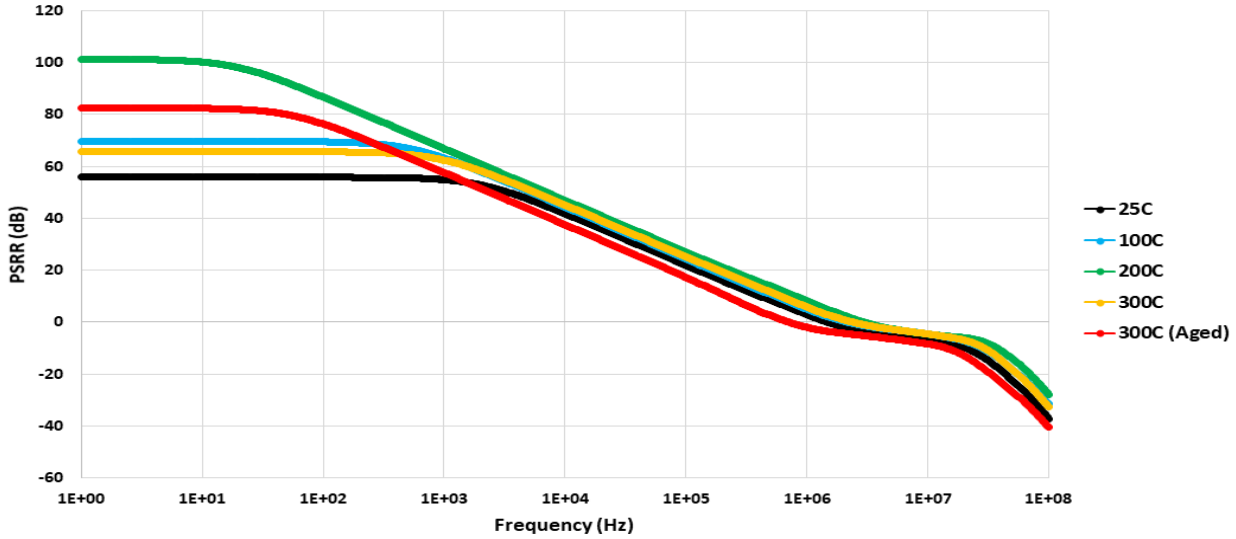

Fig. 4.49. The PSRR of the fully-on chip PFET based linear regulator for V_{IN} = 20 V and I_{LOAD} = 50 mA over the operating temperature range.

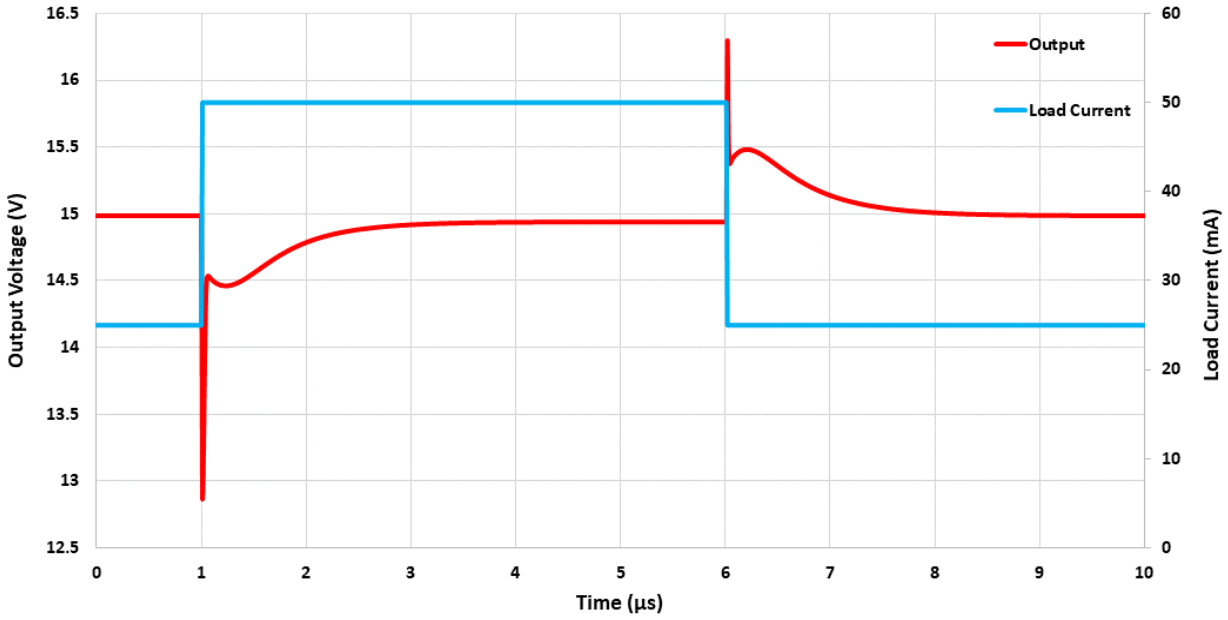

Fig. 4.50. The transient response of the fully on-chip PFET linear regulator at 300 ºC (TF) for V_{IN} = 25 V, a $I_{LOAD,CONT}$ = 25 mA, and a I_{PULSE} = 25 mA.

settling time is noticeably longer than the NFET regulator at 1.02 µs. The difference is in part due to the PFET regulator's op-amp having a larger effective capacitance at its output, which limits its slew rate. The bias current through the op-amp increases with input voltage, but not significantly enough to offset the larger capacitance. The problem worsens at larger loads, resulting in undershoot and overshoot values that increase along with settling time.

The load regulation is noticeable in Fig. 4.50 since the steady-state output voltage does not return to 15 V after the 25 mA pulse. The problem arises from the decrease in gain of the regulator due to eliminating the 2nd stage of the op-amp for stability purposes. A comparison of the load regulation values over temperature with the UA78L15 part is given in Table 4.14. The results are anticipated to be worse than the NFET regulator due to the difference in gain and the op-amp using the input voltage as its supply, therefore the units are stated as mV/mA rather than mV/A as in Table 4.11.

Table 4.14. The load regulation of the fully on-chip PFET based linear regulator over temperature for I_{LOAD} = 0 mA to 50 mA compared to TI's UA78L15 linear regulator.

Input Voltage	25 ºC	100 ºC	200 ºC	300 ºC (TF)	300 ºC (TT)	Texas Instruments UA78L15*
17.5 V	6.00 mV/mA	2.70 mV/mA	2.07 mV/mA	1.19 mV/mA	2.01 mV/mA	0.385 mV/mA Typical
20 V	7.04 mV/mA	3.52 mV/mA	2.62 mV/mA	1.44 mV/mA	1.26 mV/mA	
22.5 V	10.56 mV/A	5.35 mV/mA	4.08 mV/mA	2.17 mV/mA	1.79 mV/mA	
25 V	17.88 mV/mA	8.56 mV/mA	6.84 mV/mA	3.47 mV/mA	2.64 mV/mA	
27.5 V	-	14.23 mV/mA	-	5.67 mV/mA	3.94 mV/mA	
30 V	-	-	-	9.36 mV/mA	6.02 mV/mA	

*Test conditions: V_{IN} = 23 V, I_{LOAD} = 1 mA to 40 mA, junction temperature (T_J) = 25 ºC

For the values not reported, the output of the regulator is above 15.0 V for both the 0 mA and 50 mA steady-state loads. This illustrates a limitation arising from eliminating the 2nd stage of the op-amp and not having isolated N-wells. The op-amp's bias current increases along with PFET threshold voltages at higher input voltages, resulting in a larger V_{SD} across the cascoded FETs. The op-amp must provide the PFET pass transistor's gate with a voltage relatively close to the input voltage to ensure the output is regulated to 15 V. However, the op-amp's output swing is limited by $V_{SD,MP10} + V_{SD,MP12}$ which results in the inability to properly regulate the output voltage.

A variety of solutions exist for this problem, although each comes with a trade-off. The 2nd stage can be added back in such that the op-amp's maximum output swing is only limited by one $V_{SD,SAT}$ drop. This will require a more complex compensation strategy and result in a lower bandwidth. Another alternative is to eliminate the cascoded current mirror in the single stage op-amp such that the maximum output swing is again only limited by one $V_{SD,SAT}$. Eliminating the cascoded device reduces gain, which creates the added problem of the other load regulation values

going up. A third approach is to either reduce the bias current of the op-amp to achieve lower $V_{SD,SAT}$ values, leading to a lower UGBW, or increase the size of the existing FETs for the given bias current which results in lower frequency parasitic poles.

The line regulation performance presented in Table 4.15 suffers from low gain and high $V_{SD,SAT}$ values similar to the load regulation. The values not reported did not have an output voltage of 15.0 V or below for the input voltage range, indicating that the $V_{DS,SAT}$ drops are an obstacle to increasing performance. For higher load currents, the pass transistor needs a lower gate voltage and the design provides the desired 15 V output. The low gain remains a factor for poor performance, however. The SiC PFET linear regulator eventually outperforms the silicon based part at 300 ºC for a load current of 50 mA.

The quiescent current of the linear regulator is given in Fig. 4.51. Higher input voltages lead to substantial increases in quiescent current as expected due to the op-amp drawing its supply voltage from the input. Finally, a summary of the simulation results are provided in Table 4.16 along with a comparison to silicon based parts.

Table 4.15. The line regulation of the fully on-chip PFET based linear regulator over temperature for V_{IN} = 17.5 V to 30 V compared to TI's UA78L15 linear regulator.

Load Current	25 ºC	100 ºC	200 ºC	300 ºC (TF)	300 ºC (TT)	Texas Instruments UA78L15*
0 mA	-	-	-	-	-	5.8 mV/V Typical
1 mA	-	-	-	-	-	
5 mA	-	78 mV/V	-	22 mV/V	12 mV/V	
10 mA	209 mV/V	68 mV/V	75 mV/V	19 mV/V	6.1 mV/V	
25 mA	183 mV/V	48 mV/V	59 mV/V	12 mV/V	1.7 mV/V	
50 mA	145 mV/V	27 mV/V	40 mV/V	3.3 mV/V	1.9 mV/V	

*Test conditions: V_{IN} = 20 V to 30 V, I_{LOAD} = 40 mA, junction temperature (T_J) = 25 ºC

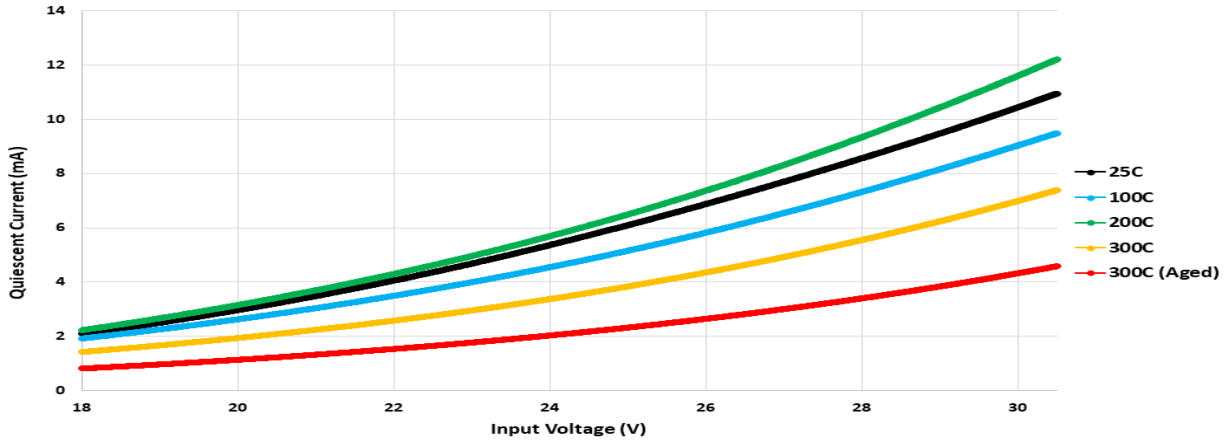

Fig. 4.51. The quiescent current of the fully on-chip PFET based linear regulator for each operating temperature and an I_{LOAD} = 0 mA.

Table 4.16. A summary of the fully on-chip PFET linear regulator and a comparison to silicon based parts.

Parameter	Test Condition (this work only)	25ºC (TF)	300 ºC (TF)	300 ºC (TT)	Fully On-Chip Silicon Regulator [60]	Texas Instruments TPS731 (Cap-Free) [70]
DC Loop Gain	I_{LOAD} = 50 mA, V_{IN} = 25 V	53.3 dB	70.5 dB	72.5 dB	62 dB	N/A
Phase Margin		102º	111º	119º	50º (min.)	N/A
Bandwidth		2.54 MHz	4.88 MHz	2.00 MHz	220 kHz (min.)	N/A
PSRR	F = 100 Hz, I_{LOAD} = 0 mA, V_{IN} = 25 V	55.8 dB	65.6 dB	76.3 dB	57 dB (@ 1 kHz)	58 dB (@ 100 Hz)
$I_{QUIESCENT}$	I_{LOAD} = 0 mA, V_{IN} = 17.5 V	2.1 mA	1.4 mA	0.8 mA	0.065 mA	0.4 mA
Overshoot ΔV_{OUT}	ΔI_{LOAD} = 25 mA, V_{IN} = 25 V	1.64 V	1.29 V	2.06 V	N/A	N/A
Undershoot ΔV_{OUT}		1.97 V	2.20 V	3.45 V	N/A	N/A
1% Settling Time		1.31 µs	1.02 µs	1.93 µs	3 µs (full load transient)	2 µs (full load transient)
Line Regulation	ΔV_{IN} = 17.5 V to 30 V, I_{LOAD} = 50 mA	145 mV/V	3.3 mV/V	1.9 mV/V	N/A	0.35 mV/V
Load Regulation	ΔI_{LOAD} = 50 mA V_{IN} = 25 V	N/A	9.36 mV/mA	6.02 mV/mA	N/A	0.07 mV/mA

4.3 Switched Capacitor Converter

The switched capacitor (SC) converter designed in this work follows the operation principles set forth in Chapter 3, Section 3.2. The core of the SC converter is provided in Fig. 4.52, in which the control logic and support circuitry are not explicitly shown. Due to requiring external capacitors, the design is limited by the high temperature capability of state-of-the-art dielectric

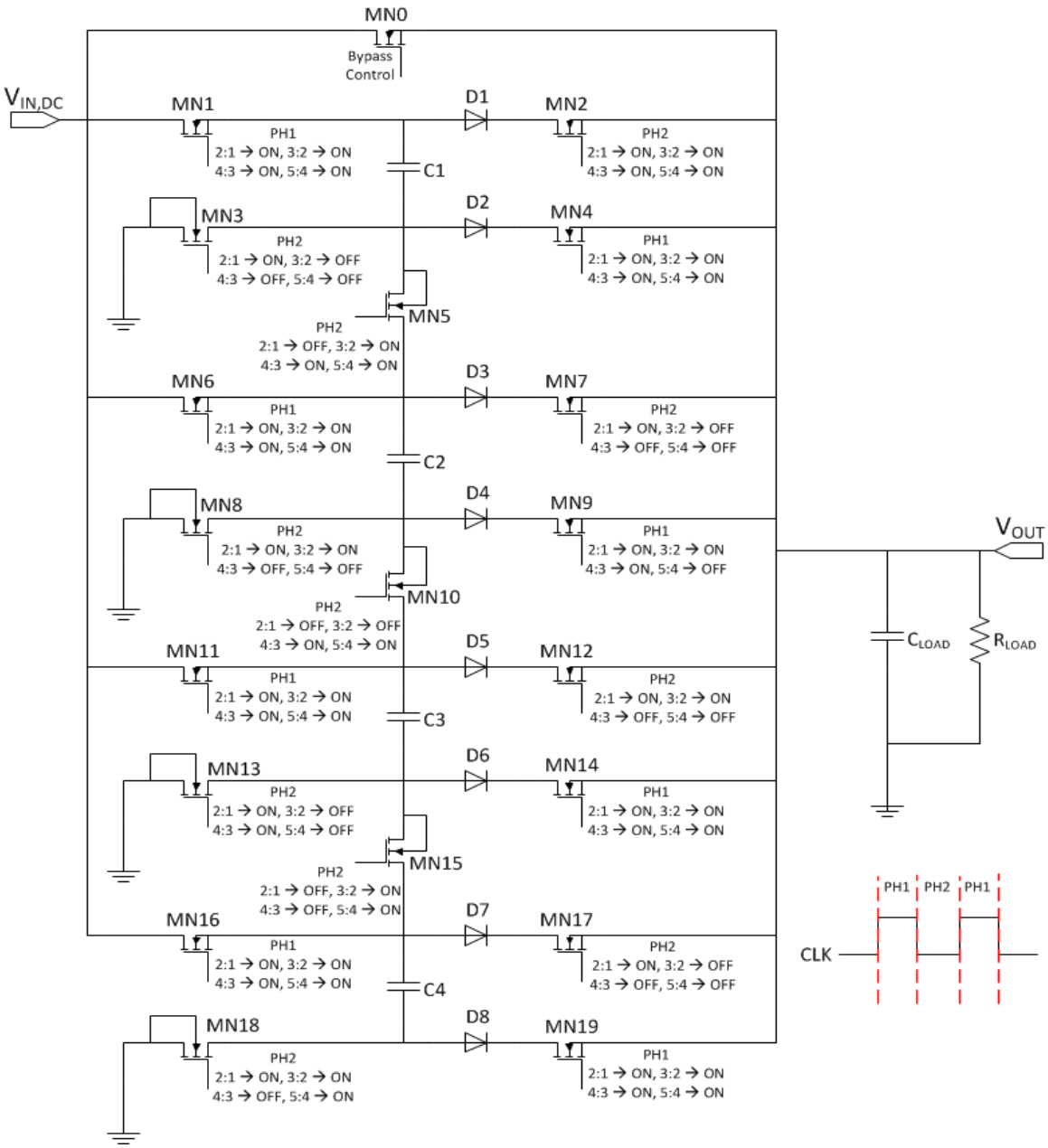

Fig. 4.52. The top-level view of the reconfigurable switching converter.

materials and the available PCB area in the application. One notable change from the theoretical operation presented in Chapter 3 is that diodes have been added to ensure the converter never discharges the output. Without the diodes, it is possible that the charging cycle will cause current to flow from the (intended) source to the drain of the PH2 controlled NFETs. The voltage drop across the diodes when forward biased will be one source of power dissipation in the SC converter.

The unit-cells are stacked in the topology given in Fig. 4.52 to allow for a reconfigurable conversion ratio. Based on the input voltage, the control logic selects the appropriate NFETs to switch on in PH2 to give the desired output voltage. With only a single conversion ratio, the topology would be limited to providing a set fraction of the input voltage at the output. The derivation for which FETs should turn on for a given conversion ratio is based on the theory presented in Chapter 3. For example, a 4:3 conversion ratio requires three capacitors (or a multiple of three) to be charged in parallel by the input voltage in PH1. During PH2, the output is charged by the three capacitors in series. The derivation of the 4:3 conversion ratio begins with KVL's for PH1 and PH2 given by equations (4.19) to (4.20), respectively.

$$\boldsymbol{V_{OUT} = V_{IN,DC} - V_{C1,2,3},\ phase\ 1} \tag{4.19}$$

$$\boldsymbol{V_{OUT} = 3 * V_{C1},\ phase\ 2} \tag{4.20}$$

Substituting the output voltage in (4.20) into (4.19) yields (4.21).

$$\boldsymbol{V_{OUT} = V_{IN,DC} - (\frac{1}{3})V_{OUT}} \tag{4.21}$$

Simplifying the equation results in (4.22).

$$\boldsymbol{V_{OUT} = \left(\frac{3}{4}\right) V_{IN,DC}} \tag{4.22}$$

This theory can be extended to a desired number of conversion ratios. A larger number of conversion ratios provides greater control for what the converter's output voltage can be set to.

However, as will be discussed, there are efficiency related trade-offs associated with using an increasing number of conversion ratios.

The application of the SC converter designed in this work has an input voltage that can gradually vary over time between 20 V and 50 V. The mixed-signal circuitry required for the application operates with a 15 V supply. A linear regulator is desirable to provide the 15 V supply voltage since it eliminates switching noise, provides a stable output for a multitude of operating conditions, and can be integrated fully on-chip as shown in the previous sections. However, the linear regulator inherently dissipates an increasing amount of power as the input voltage rises. The switching converter is designed to efficiently convert the input voltage to a relatively low voltage that allows the linear regulator to operate with less power dissipation.

The linear regulators previously discussed have minimum input voltages of approximately 19 V under the worst-case operating conditions (e.g. full-load, 25 ºC). Therefore, the first design specification for the development of a power efficient SC converter is to provide an output voltage of between 20 V to 25 V. This allows the linear regulator to remain stable and properly regulate its output voltage while being relatively efficient when the input voltage of the system is high.

The second design requirement is to optimize the number of conversion ratios based on switching losses and the power overhead of control circuitry. As the number of conversion ratios increases, the reconfigurable SC converter can allow for input voltages closer to the desired output voltage. However, the switching losses will rise due to more FETs in the converter. The control logic will also become more complex and increase power consumption.

The next specification is to optimize the SC converter's switching frequency with the switching losses. A trade-off is created between the amount of capacitance needed (e.g. the size of

C1, C2, and C3 in Fig. 4.52) and the switching losses. A higher switching frequency reduces the necessary size of the capacitors but increases the MOSFET switching losses. The application allows for approximately 200 nF of off-chip capacitance, therefore the design target is 20 nF or less for each flying capacitor. Similarly, the output capacitor is to be 100 nF or less.

The final specification is that the SC converter must outperform the efficiency of a stand-alone linear regulator for loads of up to 50 mA. For example, if the overhead of control logic and switching losses reduce the SC converter's efficiency to 70% while the input voltage is only 26 V, then it is more power efficient to stop the switching action and short across the SC converter. This is the purpose of MN0 shown in Fig. 4.52. As will be discussed, the design limits the operation of the SC converter to input voltages of between 34 V and 50 V. MN0 is switched on above 34 V and the input is connected directly to the linear regulator.

The block diagram shown in Fig. 4.53 provides an overview of the SC converter's operation along with the necessary control logic and support circuitry. For the control and support circuitry, the reconfigurable SC converter uses a pre-regulator to provide a stable 15 V output. A modified version of the NFET based fully on-chip linear regulator will be utilized. Its bandwidth, power consumption, and impact on overall efficiency are reduced for this application.

A voltage-controlled oscillator (VCO) is implemented to generate a square waveform and is supplied by the 15 V output of the pre-regulator as shown in Fig. 4.53. A non-overlapping clock generator then takes the input of the VCO and provides two clocks with a duty cycle of slightly less than 50%. Without a non-overlapping clock generator, the switching patterns of PH1 and PH2 can lead to the input shorting directly to the output or ground. Next, an array of comparators allows the SC converter to determine the magnitude of the input voltage. Note that the comparators do

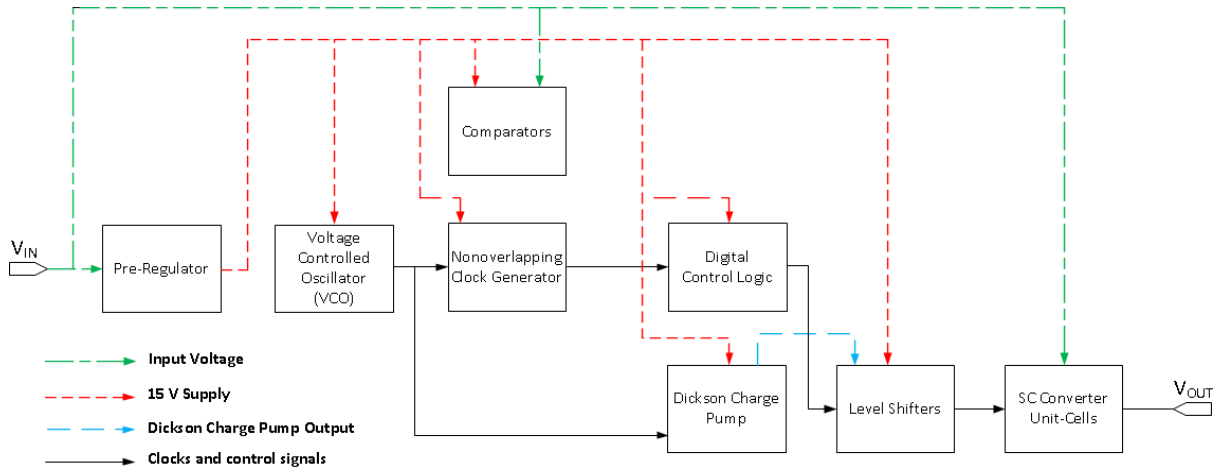

Fig. 4.53. The block diagram of the reconfigurable SC converter.

require a reference voltage, as does the linear regulator, which can be an on-chip SiC CMOS solution as demonstrated by the Vulcan II bandgap reference [67].

Depending on the output provided by the comparators, digital control logic will determine the appropriate switching algorithm to control each FET in the SC converter's unit-cells. The digital control logic operates from a 15 V supply to minimize power consumption. Since the output of the digital logic is limited to 15 V, a Dickson charge pump is used to generate a relatively large voltage. Level shifters are implemented such that the relatively low voltage logic provided by the controller is boosted up to the required voltage for switching each FET in the unit-cells.

The following sub-sections provide a discussion of each block's design. The section concludes with the simulation results of the complete SC converter. It should be noted that a SC converter design ultimately depends on the process limitations, such as oxide breakdown voltage and maximum V_{GS} ratings. The design presented in this work is based on the HiTSiC® process specifications that included a 70 V breakdown voltage. For lower breakdown voltages, the input voltage range of the SC converter may need to be altered. Similarly, the output voltage of the Dickson charge pump can be lowered to support different V_{GS} requirements.

4.3.1 Low Power, Fully On-Chip Pre-Regulator

The requirements for the pre-regulator are to provide an output voltage of 15 V and a maximum load current of 10 mA from an input voltage range of 20 V to 50 V while keeping the quiescent current below 2 mA at 300 ºC. The fully on-chip NFET based linear regulator presented in Section 4.2.2 is modified to reduce power consumption, primarily by lowering the op-amp's current consumption. This will cause a decrease in bandwidth, but it is acceptable given the relatively low switching frequency of the SC converter. In addition, the unity-gain frequency shifts inwards and away from the parasitic pole region such that the design remains stable.

The changes in device sizes to the linear regulator and its op-amp are listed in Table 4.17. The pass transistor size can be reduced if area is a concern, but it isn't necessary for stability. The transient response of the regulator is subsequently shown in Fig. 4.54 for a load pulse of 10 mA and an input voltage of 50 V.

Table 4.17. The relevant device size changes made in the pre-regulator and multipath RFC.

Component	Device Size	Comment
R_{LS}	50 kΩ	Level shifting
R_{IBIAS1}	300 kΩ	Biasing – multipath RFC

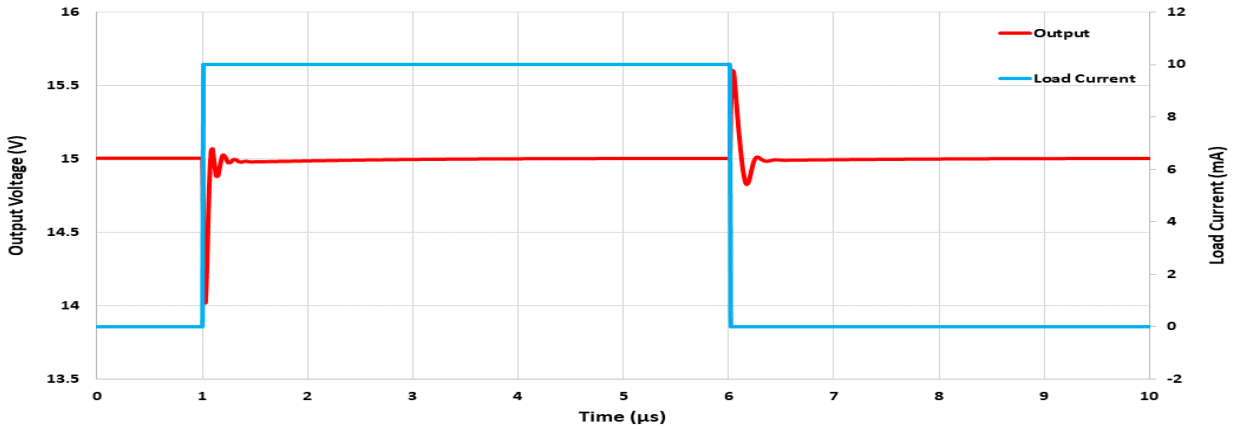

Fig. 4.54. The pre-regulator's transient response - I_{PULSE} = 50 mA and V_{IN} = 50 V (300 ºC).

4.3.2 Dickson Charge Pump

The application for the SC converter has a maximum input voltage of 50 V, which is significantly greater than the 15 V available to the digital logic. The PH1 FETs in Fig. 4.52 with their drains connected to the input voltage require a gate voltage of approximately a threshold drop above the input voltage to turn on. The maximum threshold voltage of NFETs approaches 3 V, which leads to a gate voltage requirement of about 53 V on PH1 FETs such as MN1, MN6, MN11, and MN16 when the input voltage is at 50 V.

To convert the 15 V logic high signals to a voltage sufficient for turning on the FETs in the SC converter's unit-cells, a Dickson charge pump is used. The operation follows the theory presented in Chapter 3 where each added stage boosts the input voltage by approximately the magnitude of the input voltage minus one threshold voltage drop. In the discussion provided in Chapter 3, the N-stage Dickson charge pump utilized MOSFETs in gate-drain connected configurations that act as diodes. For this Dickson charge pump design, diodes are used rather than MOSFETs acting as diodes. MOSFETs can be used for the charge pump, but each MOSFET body terminal must be connected to the drain to ensure the FET acts as a diode.

To calculate the number of stages required for boosting 15 V up to at least 53 V, equations (4.23) and (4.24) can be used to calculate the minimum and maximum voltages of each stage.

$$\boldsymbol{V_{OUTN,MAX} = (N + 1)(V_{IN,DC}) - (N)(V_D)} \tag{4.23}$$

$$\boldsymbol{V_{OUTN,MIN} = (N)(V_{IN,DC}) - (N)(V_D)} \tag{4.24}$$

Setting V_{OUT} equal to 53 V in (4.23) and assuming a diode drop of 3 V at 25 ºC, a total of four stages are required. Note that some literature specifies the number of stages to be equal to the number of diodes (or gate-drain connected FETs). The number of stages specified in this work excludes the last diode, which allows expressions (4.23) and (4.24) to hold true for N-stages. The

schematic of the 4-stage Dickson charge pump is shown in Fig. 4.55. Each capacitor is 900 pF and is ideally off-chip to conserve die area. The simulation results are given in Fig. 4.56 for the 4-stage Dickson charge pump with a 500 kHz clock operating from 25 ºC to 300 ºC (TF).

As shown in Fig. 4.56, the maximum voltage of about 66 V at 300 ºC follows expectations since the voltage drop across the diode reduces at higher temperatures. If a voltage less than the maximum is needed, then a lower stage can be connected to a diode and a capacitor can be used to reduce the output ripple as has been done to the last stage in Fig. 4.55. This is important for a process that may have a relatively low absolute maximum V_{GS} rating.

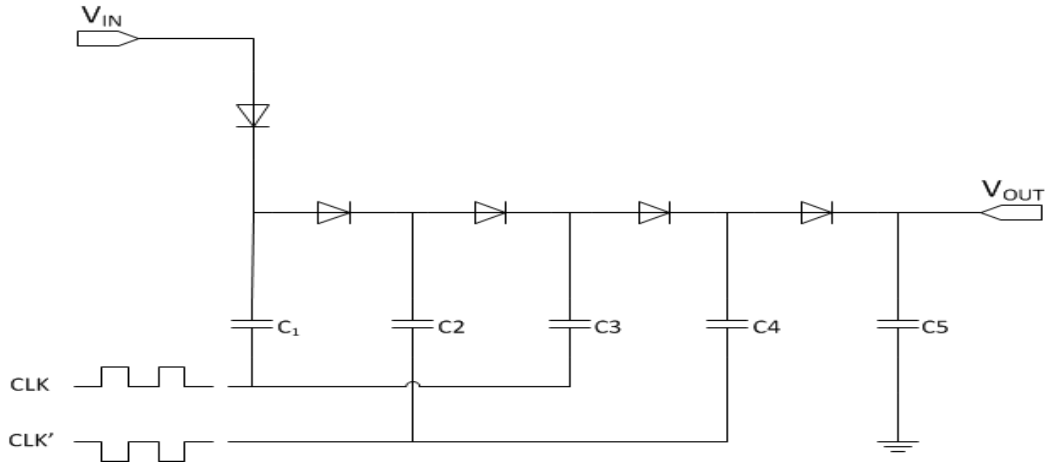

Fig. 4.55. The schematic of the 4-stage Dickson charge pump used in the SC converter.

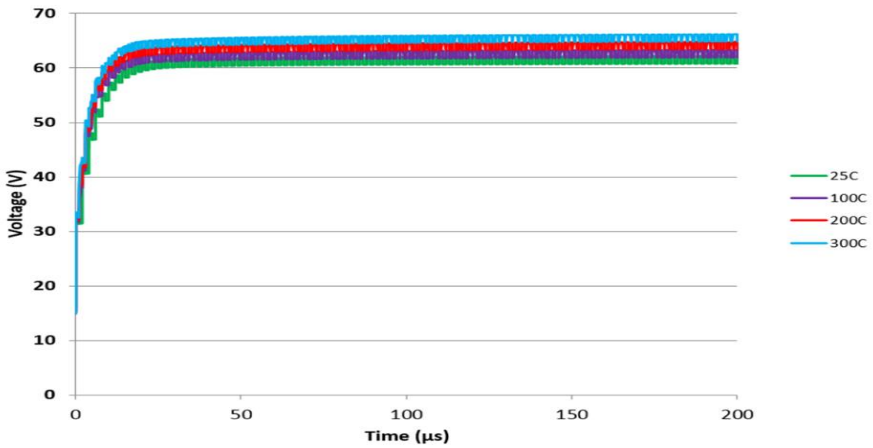

Fig. 4.56. The simulated output voltage of the 4-stage Dickson charge pump.

4.3.3 Level Shifters

With digital logic providing a maximum output of 15 V, level shifters are necessary to convert the logic signals into the higher voltages provided by the Dickson charge pump. The basic topology of the level shifter is shown in Fig. 4.57. The circuit requires that the input be the relatively low-voltage signal and the VDD be provided by the larger voltage such as one of the Dickson charge pump stages. Note that a multi-chip module or isolated N-wells may be required.

Analyzing the circuit in this context will show that a low-voltage logic high input of only 15 V to the gate of MN1 will cause MN1's drain to short to ground. On the contrary, MN2's gate will be a logic low and it will be turned off. Since MP2's gate is connected to the drain of MN1, it will also be connected to ground. With MP2's gate set to 0 V, it is turned on and the VDD coming from a Dickson charge pump stage is provided at the output.

For a 0 V input, MN1 is turned off and MN2 is turned on. With MN2 turned on, MP1 is on which leads to MP2's gate being set to approximately VDD. This results in MP2 being turned off.

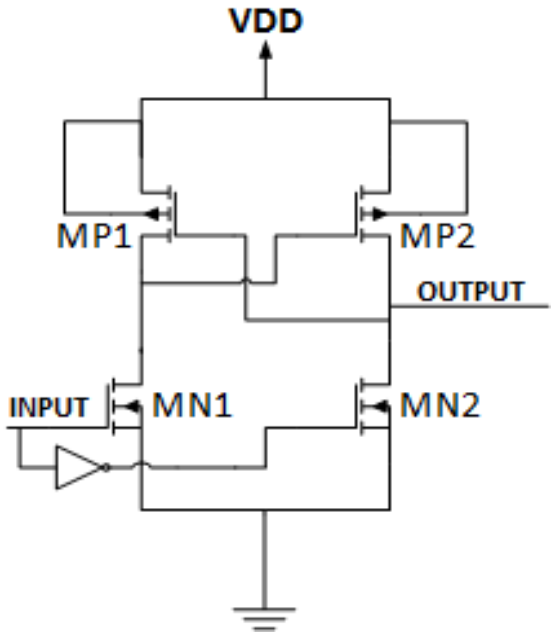

Fig. 4.57. A schematic of a basic level shifter.

Therefore, the level shifter acts as intended for converting a relatively low-voltage logic high to a higher voltage while keeping a logic low held at 0 V.

The schematic of the level shifter used in the reconfigurable SC converter is provided in Fig. 4.61. The fundamental operation of the modified level shifter remains the same as the basic level shifter given in Fig. 4.57. The addition of buffers at the output of the first stage of the level shifter (i.e. the drain of MN2) allows for increased drive strength. The buffers are beneficial for driving the large gate capacitances of the NFETs composing the SC converter's unit-cells.

The advantage of this technique is that the digital logic can be made smaller, and have reduced power consumption because it is isolated from driving a large capacitive load. The first stage of the level shifter has relatively small FETs and presents a small capacitive load to the control logic. The buffer chain then increases in size such that the rise and fall times of each stage is nearly the same.

The size of each FET in Fig. 4.58 is provided in Table 4.18. The inverter with its output tied to the gate of MN2 is contained within the digital controller and is not listed in the table.

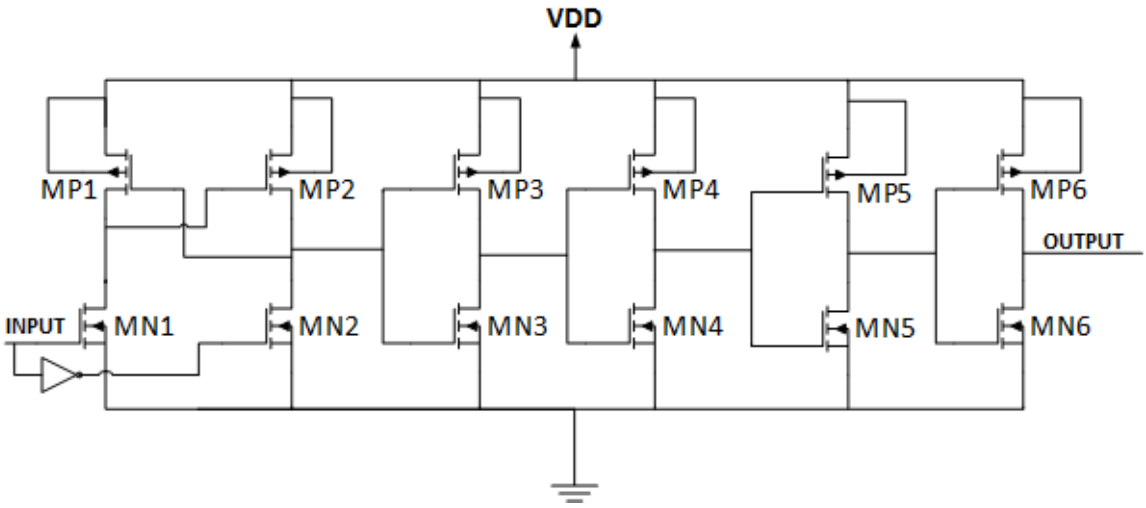

Fig. 4.58. The level shifter used in the reconfigurable SC converter.

Table 4.18. The sizes of the devices used in the level shifter presented in Fig. 4.58.

Component	Device Size	Comment
MN1 - MN3	4 µm / 1.2 µm (m = 4)	Level shifter – 1st stage, 1st buffer
MN4	4 µm / 1.2 µm (m = 8)	1st buffer
MN5	20 µm / 1.2 µm (m = 4)	2nd buffer
MN6	20 µm / 1.2 µm (m = 8)	2nd buffer
MP1, MP2	4 µm / 1.2 µm (m = 4)	Level shifter – 1st stage
MP3	4 µm / 1.2 µm (m = 16)	1st buffer
MP4	4 µm / 1.2 µm (m = 32)	1st buffer
MP5	20 µm / 1.2 µm (m = 16)	2nd buffer
MP6	20 µm / 1.2 µm (m = 32)	2nd buffer

The simulation results of the level shifter are shown in Fig. 4.59 for a 1 MHz square wave input and operating at 300 ºC (TF). Although a small amount of propagation delay exists, the level shifter accomplishes its intended function of converting the 15 V input to a 50 V supply voltage.

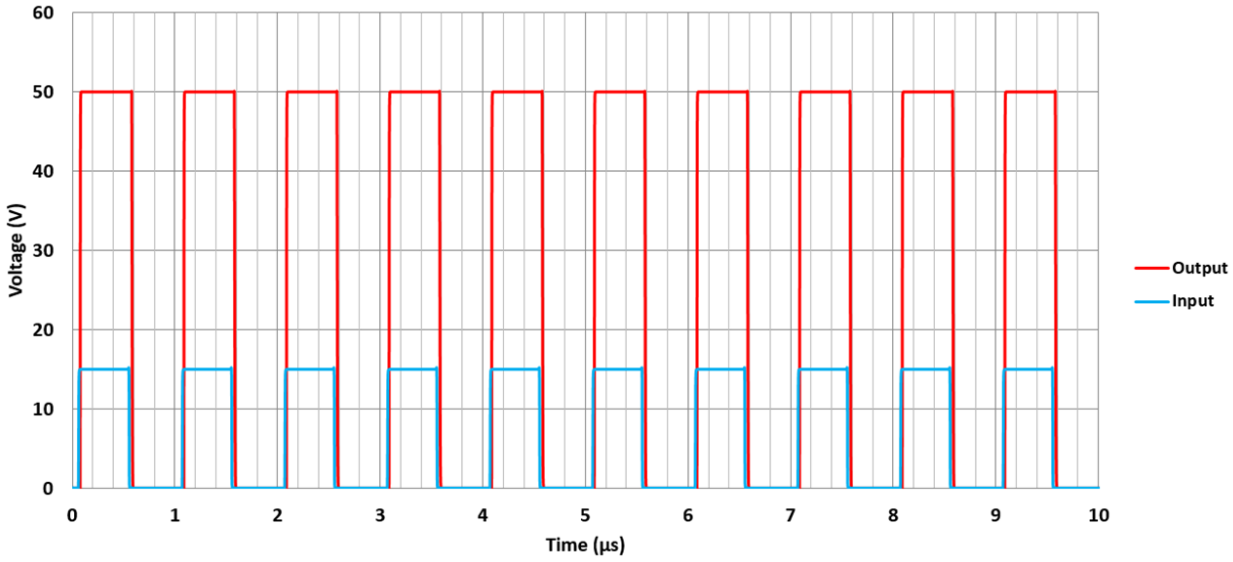

Fig. 4.59. The level shifter simulation results for a 1 MHz square wave input at 300 ºC (TF).

A potential problem of applying a large supply voltage to the level shifters is exceeding the breakdown voltage of the MOSFETs. For example, when an input voltage above V_{THN} is applied, the level shifter's output will go high since MP2 in Fig. 4.58 is turned on. If a supply voltage of 50 V is applied, then the V_{SG} of MP2 will also be 50 V. As stated previously, the rated breakdown voltage of the HiTSiC® process is 70 V. For other processes, the viability of using a level shifter at relatively high voltages such as 50 V will be a function of the oxide thickness. A quick approximation for the breakdown voltage is given in (4.25), where $E_{Critical}$ is the maximum electric field of the gate oxide (approximately 10 MV/cm).

$$\boldsymbol{V_{Breakdown} = \frac{E_{Critical}}{t_{ox}}} \tag{4.25}$$

Considering the oxide thickness (t_{ox}) to be 40 nm, the breakdown voltage is calculated to be 40 V. This reinforces the underlying importance of accounting for process parameters in order to determine if the MOSFETs (or capacitors) can safely operate in the application.

4.3.4 Voltage-Controlled Oscillator

The intended application for the SC converter does not have an external clock available. Two possible solutions for internally generating a clock include a ring oscillator or a voltage-controlled oscillator (VCO) as presented in Fig. 3.10 and Fig. 3.11, respectively. Since the application is intended to operate over a wide range of temperatures, it should be expected that there will be some deviation in clock frequency over temperature. By controlling the voltage of the VCO over temperature, more control over the clock frequency is possible.

Internally modifying the control voltage over temperature is accomplished by the VCO schematic shown in Fig. 4.60. With an increase in temperature, $V_{GS,MN1}$ will decline slightly since the NFET threshold voltage has been observed to decrease by approximately 1 V from 25 ºC to

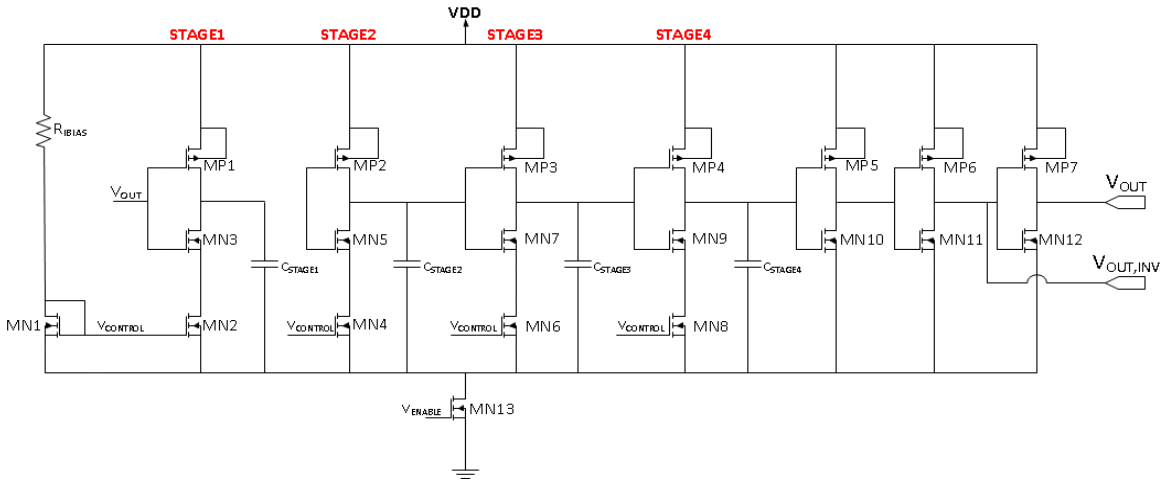

Fig. 4.60. The voltage-controlled oscillator used in the SC converter.

300 ºC. A method to counter threshold voltage decline is to use an R_{IBIAS} with a positive temperature coefficient to lessen the current through MN1. The mirroring of MN1's current to the biasing FETs, such as MN2 and MN4, sets the current through each stage. Eliminating the PFETs acting as current sources in Fig. 3.11 is advantageous for this application since the PFET thresholds vary substantially over temperature from approximately 2.5 V to 5 V. As a result, implementing the PFETs in the circuit would cause the bias current to change significantly over temperature. This would result in the inverter of each stage having large variations in charge/discharge rates, leading to a wide range of output frequencies.

The design process of the VCO begins by estimating the SC converter's optimal switching frequency. As stated at the beginning of Section 4.3, the load of the target application will be up to 50 mA and the acceptable range of output voltages is 20 V to 25 V. The change in output voltage due to the switching pattern will be limited to the same 5 V range or less. With the maximum output capacitance of 100 nF specified at the beginning of the section, the minimum switching frequency for the 5 V output swing can be calculated by (4.26) to (4.28).

$$\boldsymbol{I_{LOAD} = C_{LOAD}\left(\frac{dV_{OUT}}{dt}\right)} \tag{4.26}$$

$$\mathbf{50\ mA} = (\mathbf{100\ nF})(\frac{\mathbf{5\ V}}{\mathbf{dt}}) \tag{4.27}$$

$$\boldsymbol{f_{sw}} = \frac{\mathbf{1}}{\mathbf{dt}} = \mathbf{100\ kHz} \tag{4.28}$$

The calculated minimum switching frequency of 100 kHz represents a worst-case scenario since the flying capacitors C1 through C4 in Fig. 4.52 will also assist with keeping the output voltage constant leading to an output swing of less than 5 V. To partially account for the assistance of the flying capacitors, while also further constraining the output swing, a 150 kHz switching frequency is selected. This keeps switching losses relatively small while also ensuring that the output voltage ripple isn't extreme.

Proceeding with a design requirement of 150 kHz, the next parameters that must be set are the number of stages and the VCO's bias current through MN1. Selecting a 4-stage configuration and setting the I_{BIAS} to 100 μA, the capacitance between each stage is calculated by the expression (4.29).

$$\boldsymbol{C_{STAGE1,2,3,4}} = \frac{\boldsymbol{I_{BIAS}}}{(\boldsymbol{N_{STAGES}})\ (\boldsymbol{f_{sw}})(\boldsymbol{VDD})} \tag{4.29}$$

The calculated result of 11.1 pF is based on the assumption that $V_{CONTROL}$ is set to ½ of VDD. While this is not exact due to the assumption along with imperfect current mirrors, it does provide a starting point for determining a final value via simulation. Based on iterating the design in simulation, a final value of 22.5 pF is chosen for C_{STAGE1} through C_{STAGE4}. The list of device sizes used in the VCO design is provided in Table 4.19.

A summary of the simulation results from 25 ºC to 300 ºC (TF) is given in Table 4.20 for a C_{LOAD} of 10 pF. The dependence of the bias current on the threshold voltage of MN1 and the value of R_{IBIAS}, which trend in opposite directions over temperature, results in 300 ºC having a lower oscillation frequency than 100 ºC and 200 ºC.

Table 4.19. The sizes of the devices used in the VCO presented in Fig. 4.60.

Component	Device Size	Comment
MN1 – MN10	4 µm / 1.2 µm (m = 4)	VCO inverters, 1st buffering inverter
MN11	4 µm / 1.2 µm (m = 8)	2nd buffering inverter
MN12, MN13	4 µm / 1.2 µm (m = 16)	3rd buffering inverter
MP1 – MP5	20 µm / 1.2 µm (m = 4)	VCO inverters, 1st buffering inverter
MP6	20 µm / 1.2 µm (m = 8)	2nd buffering inverter
MP7	20 µm / 1.2 µm (m = 16)	3rd buffering inverter
R_{IBIAS}	100 kΩ	Biasing resistor
C_{STAGE1} – C_{STAGE4}	22.5 pF	Output capacitance per inverter stage

Table 4.20. Simulation results of the low-frequency VCO from 25 ºC to 300 ºC.

Parameter	25 ºC	100 ºC	200 ºC	300 ºC	300 ºC (TT)
f_{sw}	123.8 kHz	171.9 kHz	175.9 kHz	149.6 kHz	97.8 kHz
Rise Time	38.5 ns	28.3 ns	22.8 ns	26.2 ns	51.1 ns
Fall Time	38.6 ns	32.8 ns	30.9 ns	32.9 ns	33.2 ns
Avg. Supply Current	357 µA	495 µA	494 µA	429 µA	268 µA

A second VCO is designed to provide a higher clock frequency to the Dickson charge pump, allowing it to operate with smaller capacitors while limiting the output voltage ripple. The high frequency VCO is designed for a switching frequency of approximately 600 kHz at 300 ºC (TF) and utilizes two additional inverter stages. Note that the FET driven by an enable signal in Fig. 4.60, which is used to reduce power consumption when the input voltage falls below the limit of the SC converter, cannot be used in the high frequency VCO. This is due to the Dickson charge pump requiring the high frequency VCO. Without it, the charge pump cannot turn on MN0 in Fig. 4.52 to bypass the SC converter.

The high frequency VCO's simulation results over the operating temperature range are provided in Table 4.21. The device sizes are also listed in Table 4.22.

Table 4.21. Simulation Results of the high-frequency VCO from 25 ºC to 300 ºC.

Parameter	25 ºC	100 ºC	200 ºC	300 ºC	300 ºC (TT)
f_{sw}	517.3 kHz	716.3 kHz	733.9 kHz	627.3 kHz	411.2 kHz
Rise Time	4.04 ns	3.05 ns	2.77 ns	2.99 ns	4.72 ns
Fall Time	3.5 ns	2.63 ns	2.47 ns	2.64 ns	4.29 ns
Avg. Supply Current	1.21 mA	1.75 MHz	1.74 mA	1.55 mA	0.87 mA

Table 4.22. The device sizes used in the high frequency VCO and Dickson charge pump.

Component	Device Size	Comment
MN1 – MN9	4 µm / 1.2 µm (m = 4)	VCO inverters
MN10	4 µm / 1.2 µm (m = 8)	1st buffering inverter
MN11	20 µm / 1.2 µm (m = 8)	2nd buffering inverter
MN12	20 µm / 1.2 µm (m = 32)	3rd buffering inverter
MN_{ADDED1}	20 µm / 1.2 µm (m = 64)	4th buffering inverter
MN_{ADDED2}	20 µm / 1.2 µm (m = 128)	5th buffering inverter
MP1 – MP4	20 µm / 1.2 µm (m = 4)	VCO inverters
MP5	20 µm / 1.2 µm (m = 8)	2nd buffering inverter
MP6	20 µm / 1.2 µm (m = 32)	2nd buffering inverter
MP7	20 µm / 1.2 µm (m = 64)	3rd buffering inverter
MP_{ADDED1}	20 µm / 1.2 µm (m = 128)	4th buffering inverter
MP_{ADDED2}	20 µm / 1.2 µm (m = 512)	5th buffering inverter
R_{IBIAS}	100 kΩ	Biasing resistor
C_{STAGE1} – C_{STAGE4}	4.8 pF	Output capacitance per inverter stage
C_1 – C_5	900 pF	Dickson charge pump, see Fig. 4.55

4.3.5 Non-Overlapping Clock Generator

The two clock phases used in the switched capacitor converter, as shown in Fig. 4.52, necessitate the implementation of a non-overlapping clock generator. If a VCO is used and its output is inverted to form the second phase, then the rise and fall times of the output square waves create a high probability of PH1 and PH2 FETs being on at the same time. This leads to the input shorting to the output as well as to ground. Therefore, a non-overlapping clock generator is needed to slightly alter the duty cycle of each clock phase from the ideal 50% such that when the non-inverted clock is high, the inverted clock is low and vice versa.

The non-overlapping clock generator follows the configuration provided in Fig. 3.12. The delay created by the inverters connected to the output of each NAND gate leads to the time separation between the two clock phases being high. The schematic of the non-overlapping clock generator is shown in Fig. 4.61. A capacitor is connected between the output of the INVX1 and ground in both branches to add delay between each clock phase. The size of each device is listed in Table 4.23. The notation of the gates, such as INVX1, indicates that the NFETs and PFETs each have one finger. The NAND gates have two NFETs in series, hence the doubled width.

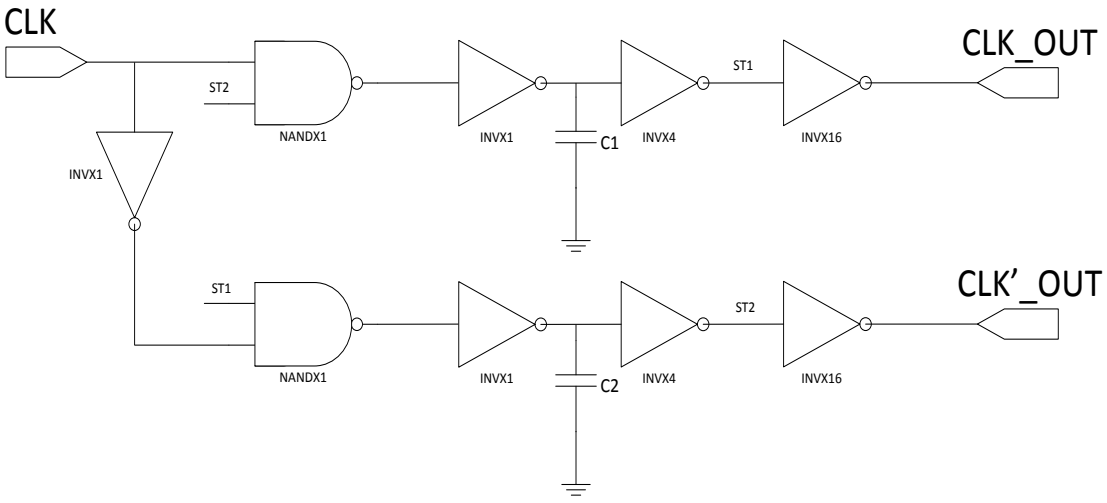

Fig. 4.61. The schematic of the SC converter's non-overlapping clock generator.

Table 4.23. Device sizes for the SC converter's non-overlapping clock generator.

Component	Device Size	Comment
MN,INVX1	4 µm / 1.2 µm (m = 1)	NFET in INVX1
MN,NANDX1	8 µm / 1.2 µm (m = 1)	NFET in NANDX1
MNX4	4 µm / 1.2 µm (m = 4)	NFET in INVX4
MNX16	4 µm / 1.2 µm (m = 16)	NFET in INVX16
MPX1	20 µm / 1.2 µm (m = 1)	PFET in INVX1 and NANDX1
MPX4	20 µm / 1.2 µm (m = 4)	PFET in INVX4
MPX16	20 µm / 1.2 µm (m = 16)	PFET in INVX16
C1, C2	1.2 pF	Additional C_{LOAD} for INVX1 in delay chains

An evaluation of the non-overlapping clock generator's performance is conducted by placing it in a test bench with the VCO and level shifters, as shown in Fig. 4.62. The output of the VCO is connected to the input of the non-overlapping clock generator. Each of the two level-shifted phases of the non-overlapping clock are connected to a 10 pF load capacitance, which is intended to represent the gate capacitance of one of the SC converter's core FETs.

Table 4.24 presents the simulation results from 25 ºC to 300 ºC (TF) for an input voltage of 50 V. Note that the duty cycles are not 50%, thus the switching frequencies do not exactly match with the VCO results presented in Table 4.20. The dead time values indicate the amount of time that each clock phase (prior to level shifting) is below 1 V before one of the phases transitions to a logic high. The rise time of the level shifted PH1 and PH2 is the time it takes the signal to go from 5 V (10%) to 45 V (90%), with the inverse being true for the fall times. Finally, the 15 V and 50 V supplies implemented in the test bench are ideal. In the final implementation, the 15 V will be provided by the pre-regulator and the voltage greater than 50 V will be provided by the Dickson charge pump.

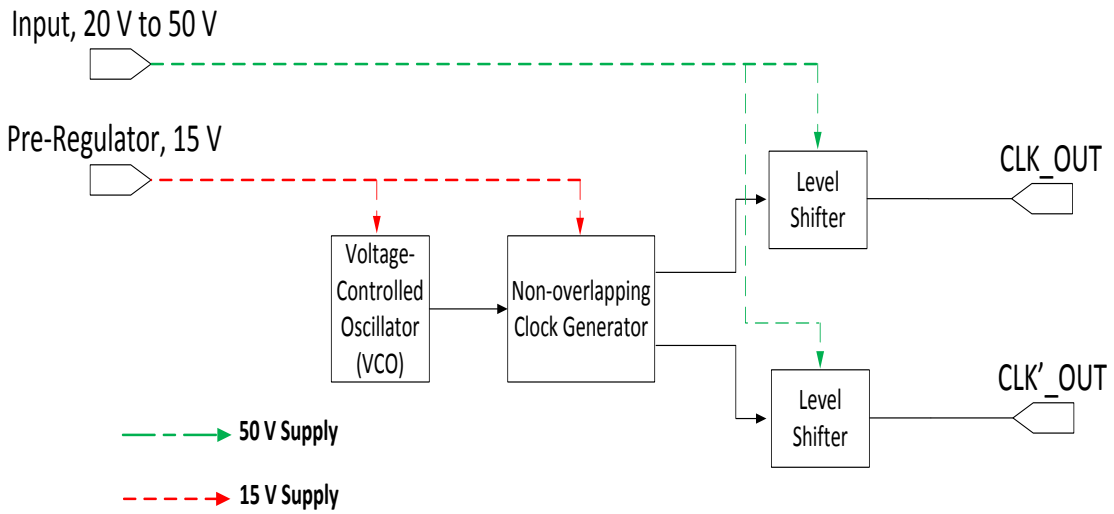

Fig. 4.62. The test bench used for the SC converter's non-overlapping clock generator.

Table 4.24. Simulation results for the non-overlapped clock generator from 25 ºC to 300 ºC.

Parameter	25 ºC	100 ºC	200 ºC	300 ºC	300 ºC (TT)
f_{sw}	124.6 kHz	173.4 kHz	177.3 kHz	150.8 kHz	98.3 kHz
Duty Cycle – PH1	50.6 %	50.7%	46.9 %	47.4 %	44.4 %
Duty Cycle – PH2	47.2 %	47.4%	43.7 %	44.4 %	41.6 %
Dead Time (PH1 falling, PH2 rising)	42 ns	30 ns	27 ns	28 ns	65 ns
Dead Time (PH1 rising, PH2 falling)	43 ns	31 ns	28 ns	29 ns	67 ns
Rise Time (PH1 and PH2)	350 ns	277 ns	338 ns	331 ns	560 ns
Fall Time (PH1 and PH2)	253 ns	217 ns	207 ns	208 ns	227 ns
Avg. Supply Current (15 V)	346 µA	493 µA	488 µA	433 µA	257 µA
Avg. Supply Current (50 V)	218 µA	376 µA	595 µA	504 µA	555 µA

4.3.6 Digital Controller

The SC converter's controller is composed of digital logic along with comparators implemented to detect the input voltage range. The comparator selected for this purpose is a modified version of the reported Vulcan II comparator [67]. The schematic of the modified comparator is shown in Fig. 4.63 and the device sizes are listed in Table 4.25. The operation principles follow those presented for the general-purpose comparator in Chapter 3, Section 3.2.2. In addition to the pre-amplification, decision making, and output stages, a fourth stage is added to internally bias the comparator. Note that hysteresis can be added intentionally by sizing the FETs in the decision stage differently. However, it's not critical for this application and process variation will inevitably add hysteresis.

The changes made to the comparator allow it to operate without external biases and with relatively low current consumption. A decrease in bandwidth will result from the lower bias current, but it is an acceptable trade-off in this application since the input voltage to the SC

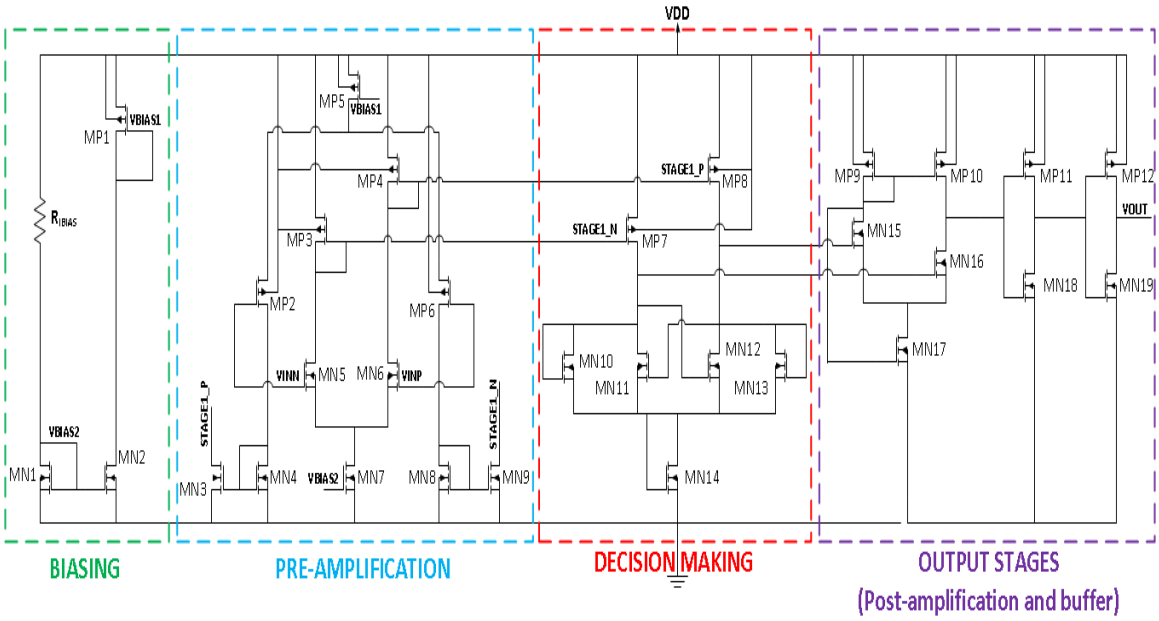

Fig. 4.63. The SC converter's comparator used in conjunction with the digital controller.

converter will change slowly. The transient response of the comparator with its non-inverting input at 3 V and inverting input varying from 2.9 V to 3.1 V is shown in Fig. 4.64 for 300 ºC (TF).

Table 4.25. Device sizes for the comparator used in conjunction with the digital controller.

Component	Device Size	Comment
MN1, MN2, MN5, MN6	20 µm / 2 µm (m = 8)	Biasing, Pre-amplification
MN3, MN4, MN8 – MN13, MN19	20 µm / 2 µm (m = 4)	Pre-Amplification, decision making, output stages
MN7	20 µm / 5 µm (m = 4)	Pre-Amplification (biasing)
MN14, MN17	4 µm / 5 µm (m = 8)	Decision making and output (post-amplification) biasing
MN18	4 µm / 2 µm (m = 4)	Output stage (1st inverter)
MP1	20 µm / 2 µm (m = 32)	Biasing
MP2 – MP4, MP6 – MP8	20 µm / 2 µm (m = 8)	Pre-amplification, decision making
MP5	20 µm / 5 µm (m = 8)	Pre-amplification (biasing)
MP9, MP10	4 µm / 5 µm (m = 16)	Output stage (pre-amplification)
MP11	4 µm / 2 µm (m = 16)	Output stage (1st inverter)
MP12	20 µm / 2 µm (m = 16)	Output stage (2nd inverter)

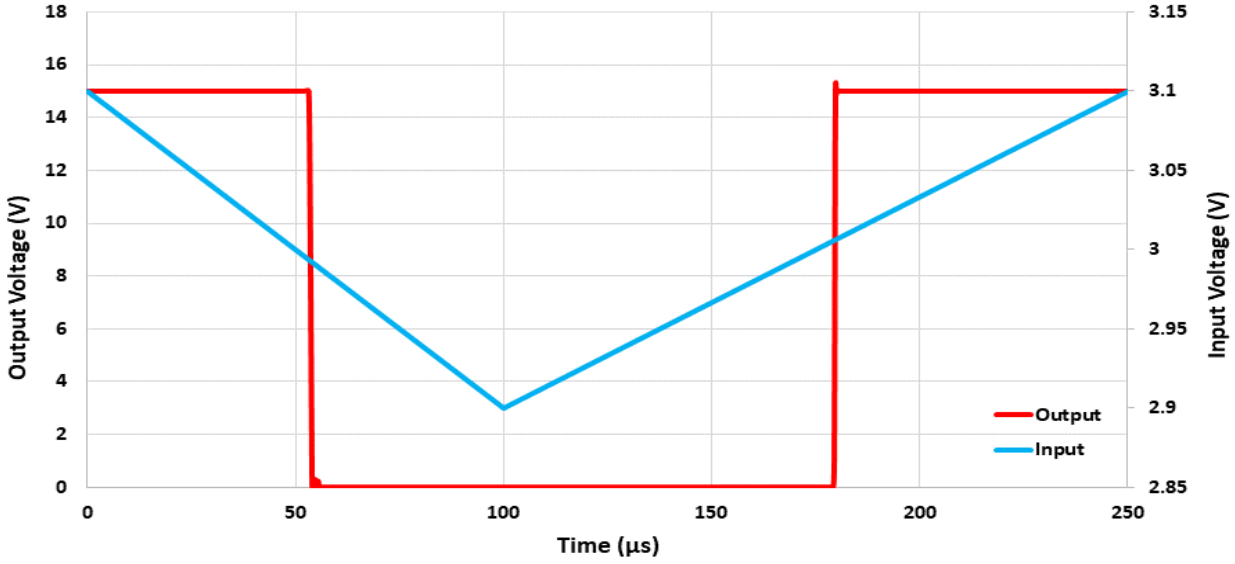

Fig. 4.64. The transient response of the comparator for V_{REF} = 3 V and a ramp input from 2.9 V to 3.1 V at 300 ºC (TF).

A total of four comparators are implemented alongside the digital controller to determine if the input voltage is above 34 V, 37 V, 42 V, or 49 V. With the comparators determining the range that the input voltage falls in, the digital controller selects the conversion ratio that provides the desired output voltage of 20 V to 25 V. The controller choses the conversion ratio as follows:

(1) A 2:1 conversion ratio is selected for $49\ V \leq V_{IN}$

(2) A 3:2 conversion ratio is selected for $42\ V \leq V_{IN} <\ 49\ V$

(3) A 4:3 conversion ratio is selected for $37\ V \leq V_{IN} <\ 42\ V$

(4) A 5:4 conversion ratio is selected for $34\ V \leq V_{IN} <\ 37\ V$

(5) The bypass MOSFET MN0, shown in Fig. 4.52, is switched on for $V_{IN} <\ 34\ V$

The MOSFETs in Fig. 4.52 that operate in PH1 are independent of the conversion ratio, thus the controller is only intended for the MOSFETs switched on in PH2. The digital controller used in the SC converter is shown in Fig. 4.65. Other controller implementations are possible and a synthesizer can be beneficial given the increasing complexity with each added conversion ratio. The device sizing for each gate follows the convention presented in Table 4.23, where a width of 4 µm (m = 1) and a length of 1.2 µm is the smallest feature size for an NFET. Similarly, a width of 20 µm (m = 1) and a length of 1.2 µm is the smallest feature size of a PFET.

Both the non-inverted and inverted outputs for each PH2 MOSFET's control logic is provided. This is necessary since the control logic of each FET must be level shifted from 15 V to a voltage that provides a large enough V_{GS} for turning on the FET.

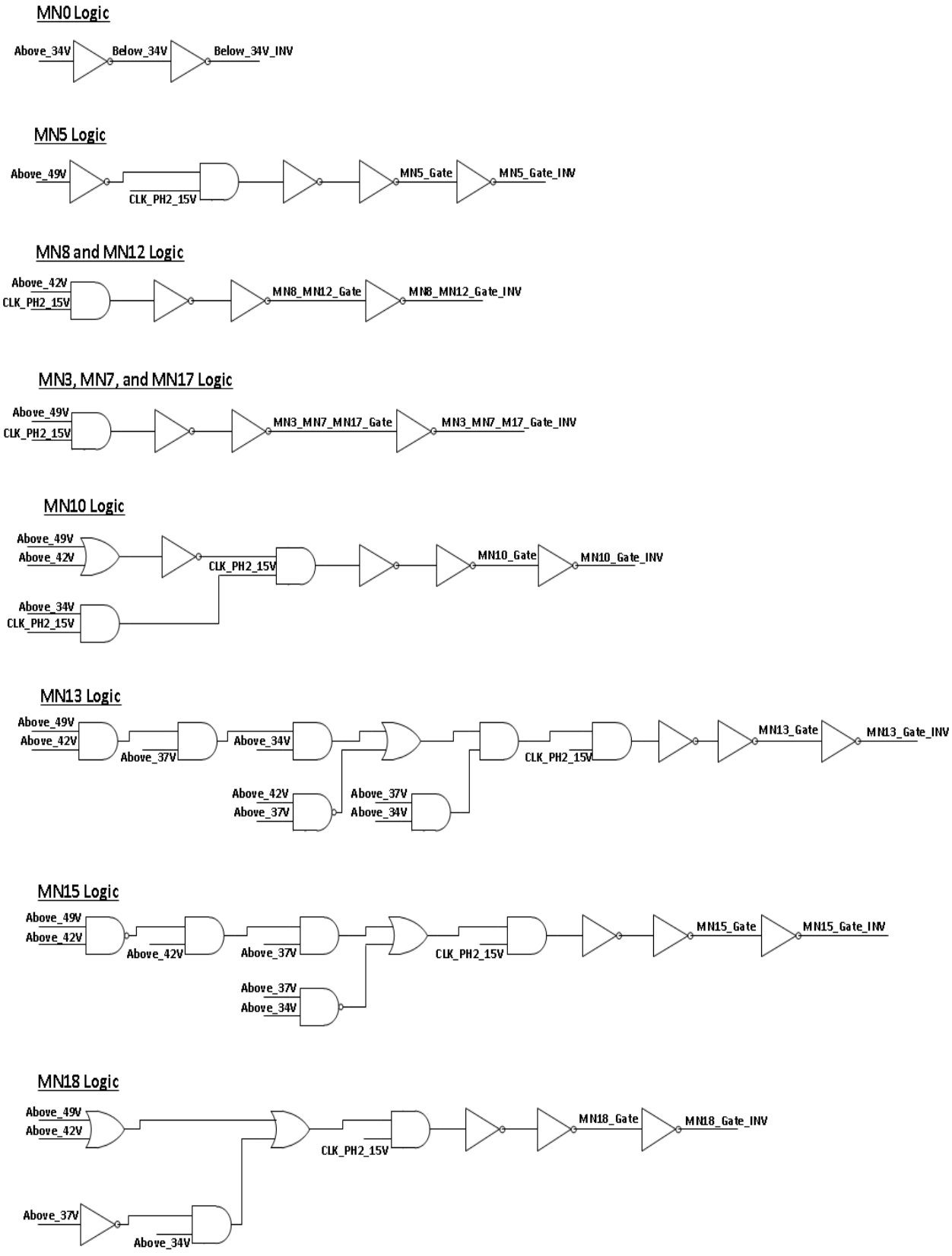

Fig. 4.65. The schematic of the SC converter's digital controller.

4.3.7 Switched Capacitor Converter: Simulation Results

The final SC converter implementation includes the pre-regulator, VCOs, non-overlapping clock generator, digital controller, Dickson charge pump, level shifters, and the core unit-cells. The digital controller operates based off of the PH2 clock from the non-overlapping clock generator and the controller outputs are connected to level shifters. The supply voltage for each level shifter is generated by the Dickson charge pump and is selected based upon the required V_{GS} of the unit-cell FETs. In the simulation results presented, the bypass NFET MN0 shown in Fig. 4.52 has a W/L equal 20 µm / 1.2 µm (m = 500). This allows the input to be shorted to the output whenever the input voltage is below 34 V and the SC converter can no longer properly convert the input to the desired output voltage.

The transient response of the SC converter is shown in Fig. 4.66 and Fig. 4.67 for NFETs with a W/L equal to 20 µm / 1.2 µm (m = 25) at 25 ºC and 300 ºC (TF), respectively. In each case,

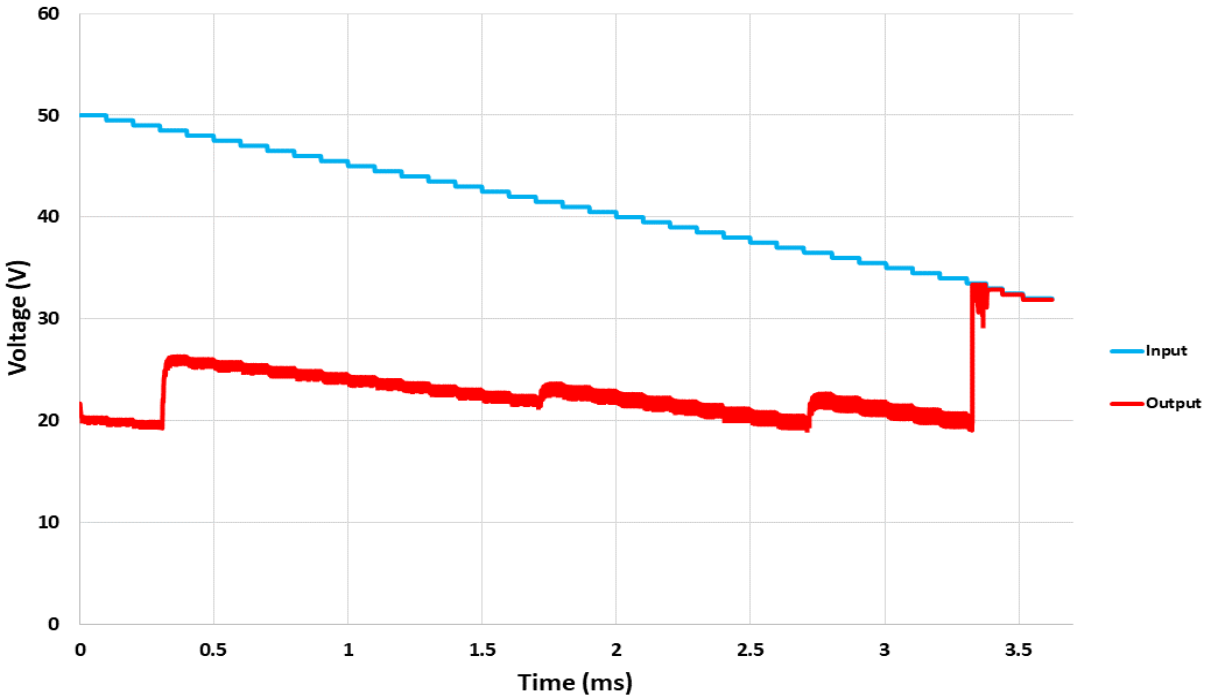

Fig. 4.66. The transient response of the SC converter at 25 ºC for NFETs in the unit-cells sized to be 20 µm / 1.2 µm (m = 25) and I_{LOAD} = 50 mA.

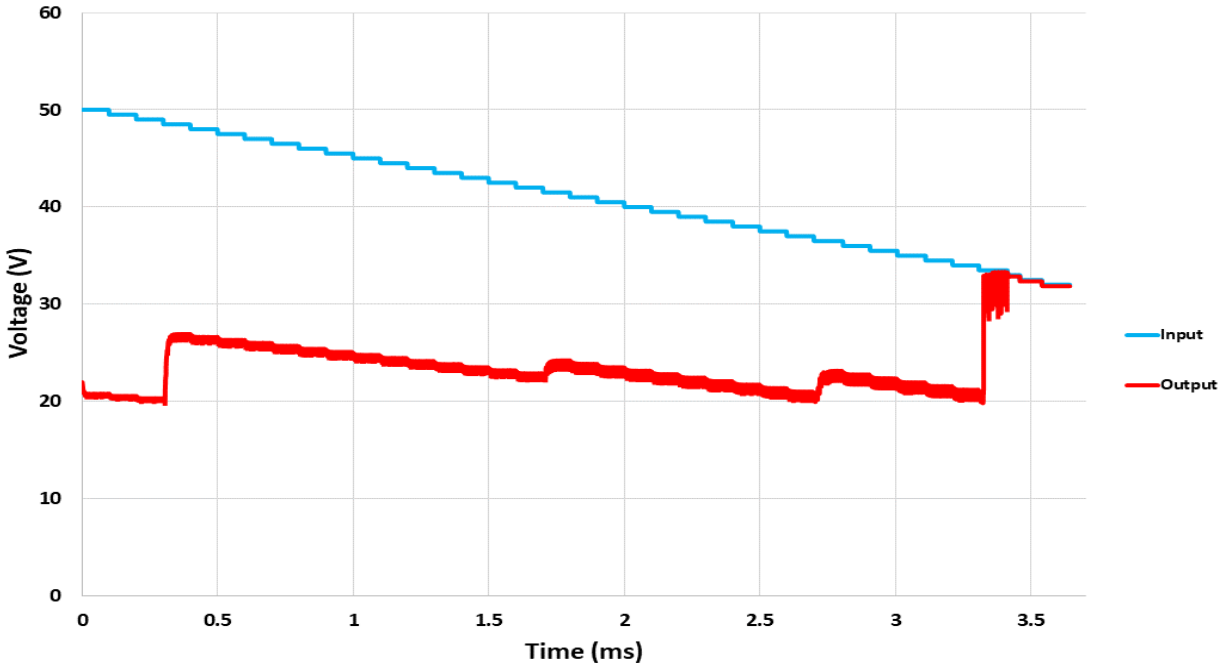

Fig. 4.67. The transient response of the SC converter at 300 ºC (TF) for NFETs in the unit-cells sized to be 20 µm / 1.2 µm (m = 25) and I_{LOAD} = 50 mA.

the input voltage is stepped down in 0.5 V increments every 0.1 ms. The reconfigurable operation of the SC converter results in an average output voltage that is above 20 V for all input voltages at 300 ºC (TF). At 25 ºC, the minimum voltage is approximately 19.5 V due to the NFETs having larger V_{DS} values and the forward diode voltage drops increasing. While the desired output voltage is 20 V and 25 V, the fully on-chip NFET linear regulator was designed with a safety margin to allow for a minimum input voltage of 19.0 V at any operating temperature and a 50 mA load.

The efficiency of the SC converter over the operating temperature range and for FETs with m = 25 is shown in Fig. 4.68. The simulation test bench incorporates the complete system and accounts for all of the support circuitry along with the power dissipation arising from V_{DS} and diode drops in the core unit-cells. At 25 ºC and 300 ºC (TT), the efficiency ranges from approximately 75% and 85% between a 34 V and 48 V input voltage. The reasoning for these two temperatures offering the greatest efficiency is a result of the VCO switching frequencies decreasing and subsequently lower switching losses. Other circuitry, such as the pre-regulator, also

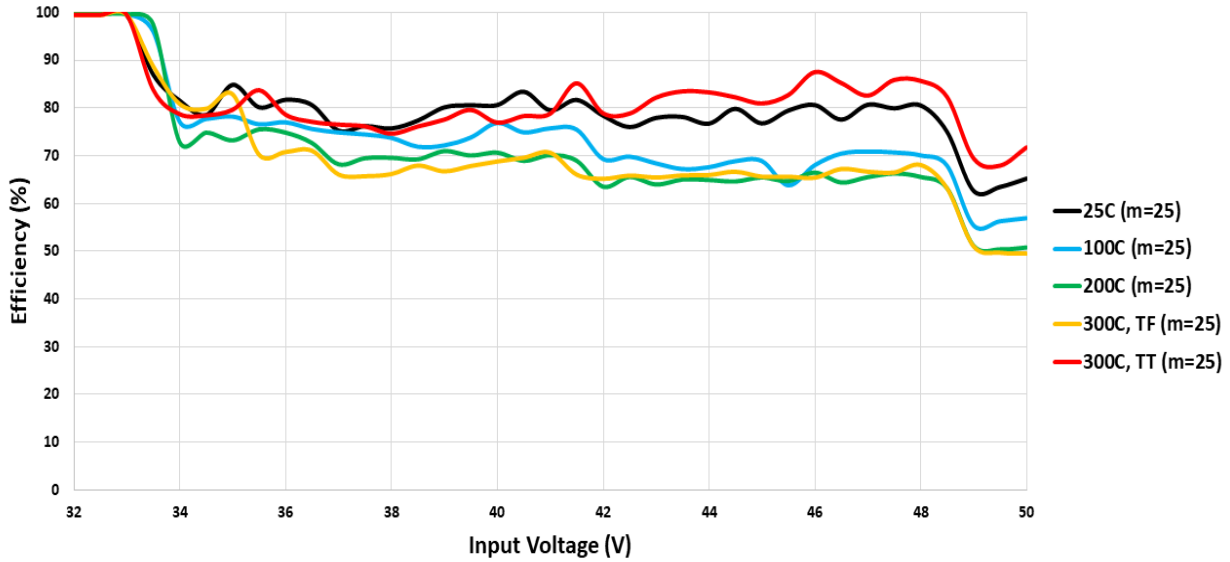

Fig. 4.68. The efficiency of the SC converter across the operating temperature range for NFETs in the unit-cells sized to be 20 µm / 1.2 µm (m = 25) and I_{LOAD} = 50 mA.

generally has lower power dissipation at these temperatures compared to higher temperatures without aging conditions. The downside of the lower switching frequency is that the overall swing of the output voltage will increase given the flying and output capacitor values do not change.

Increasing the NFET sizes in the core unit-cells to 20 µm / 1.2 µm (m = 50) results in the transient response waveforms shown in Fig. 4.69 and Fig. 4.70 for 25 ºC and 300 ºC (TF), respectively. The V_{DS} drops across the NFETs in the unit-cells are decreased at the expense of increased switching losses. A comparison of the SC converter's efficiency is shown Fig. 4.71 for 25 ºC, 300 ºC (TF), and 300 ºC (TT) when the NFETs are sized for m=50. The results at 25 ºC and 300 ºC (TT) again outperform the 300 ºC (TF) case. Comparing the efficiency results in Fig. 4.68 to those given in Fig. 4.71, in which the FETs were half the size with m=25, shows a decrease in efficiency of approximately 10%. For load currents below 50 mA, the efficiency will decrease as the static power dissipation of the support circuitry will begin to dominant the conduction and switching losses.

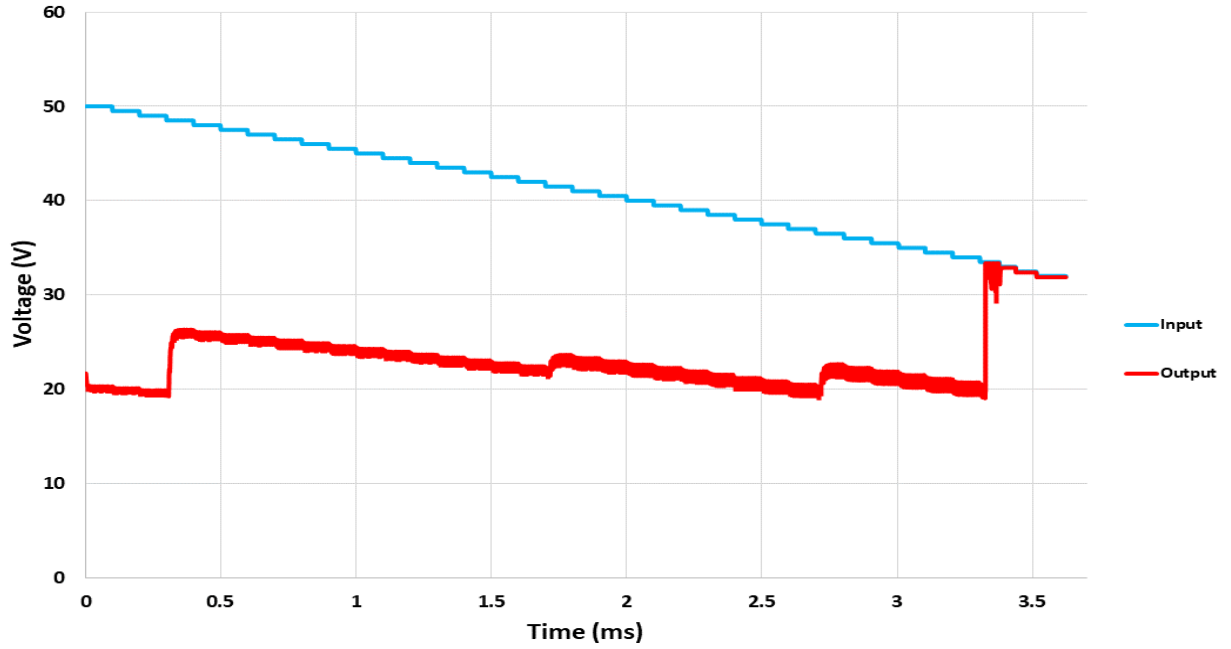

Fig. 4.69. The transient response of the SC converter at 25 ºC for NFETs in the unit-cells sized to be 20 µm / 1.2 µm (m = 50) and I_{LOAD} = 50 mA.

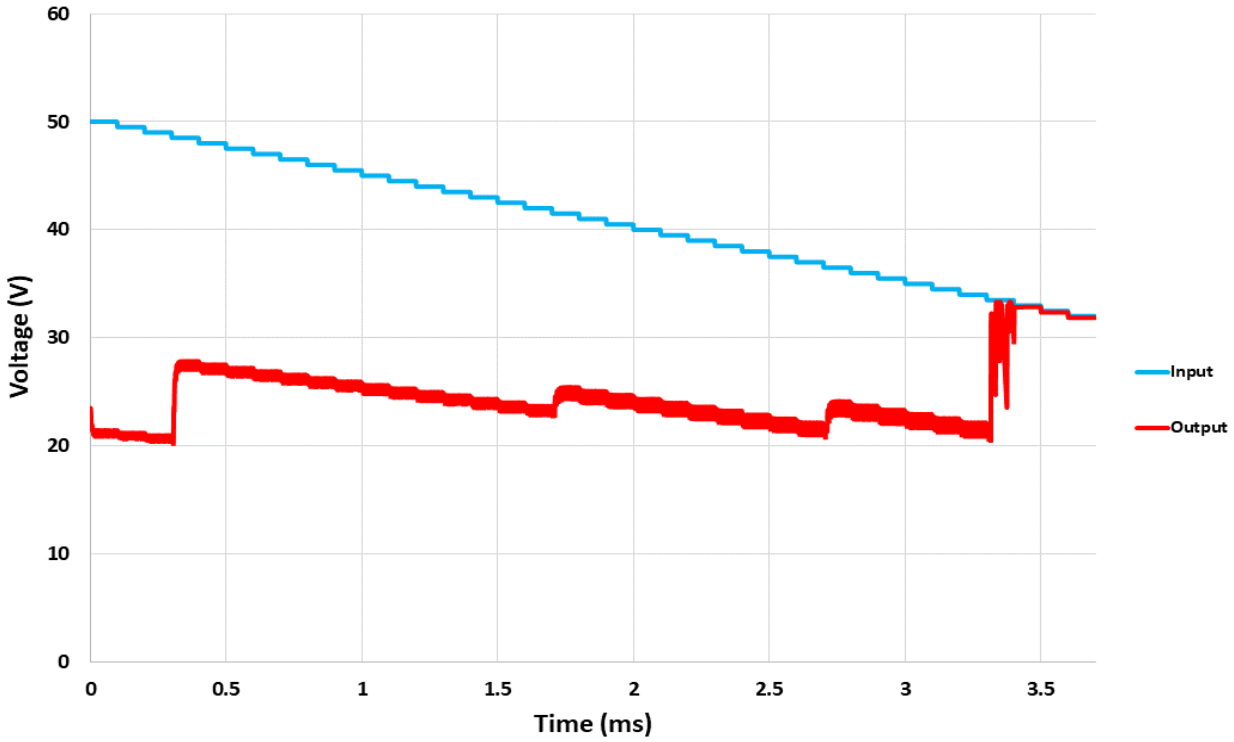

Fig. 4.70. The transient response of the SC converter at 300 ºC (TF) for NFETs in the unit-cells sized to be 20 µm / 1.2 µm (m = 50) and I_{LOAD} = 50 mA.

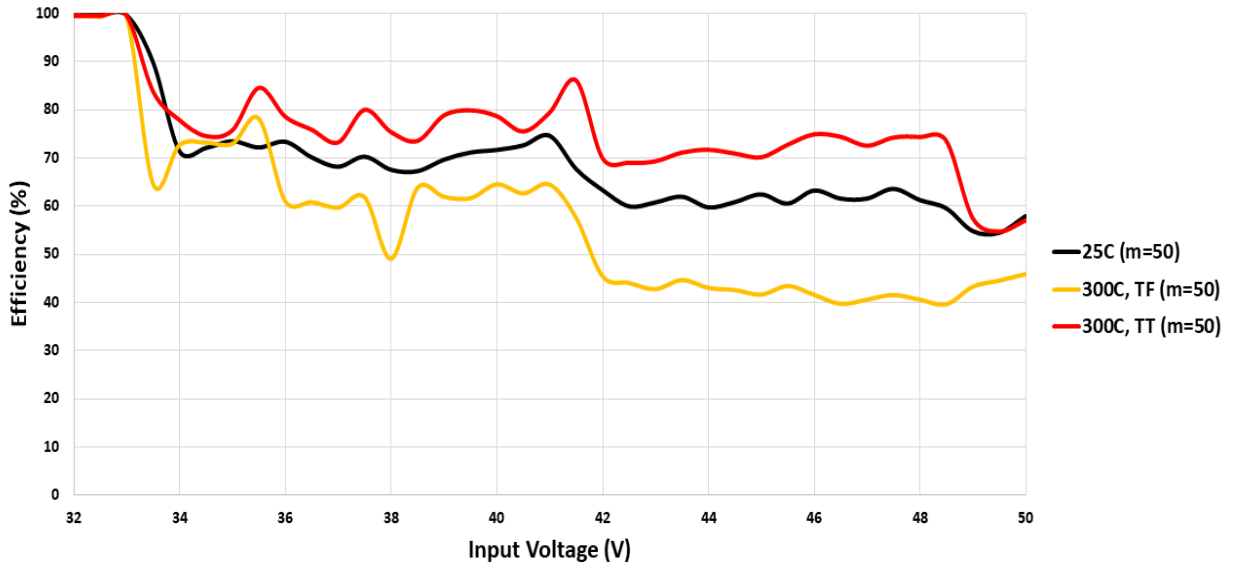

Fig. 4.71. The efficiency of the SC converter across the operating temperature range for NFETs in the unit-cells sized to be 20 µm / 1.2 µm (m = 50) and I_{LOAD} = 50 mA.

4.3.8 Switched Capacitor Converter: Optimizations

The efficiency results presented demonstrate that the SC converter has the best performance for NFETs sized with m=25. One area of optimization is the VCOs which were both designed to have sufficiently low rise and fall times for the m=50 case. Decreasing the buffer sizes in each of the VCO's output stages by half the original size will lead to lower dynamic and short-circuit power dissipation during the PH2 clock's rise and fall times. If the current consumption of the VCO's are decreased, then the pre-regulator is an additional component of the design that can have lower power dissipation. Lower current pulses due to the resized VCO means that the regulator's design requirements can be relaxed.

Another area of optimization is the level shifters. Each NFET gate voltage was driven by level shifters which had a VDD of 55 V to 65 V as provided by the Dickson charge pump. For NFETs connecting to the output, the V_{GS} value can be decreased to approximately 35 V which will lessen the dynamic and short-circuit power consumption of the level shifters.

CHAPTER 5 CHIP FABRICATION AND TEST RESULTS

5.1 Chip Fabrication, Packaging, and Test Setup

The SiC CMOS linear regulator designed for the Vulcan II run was fabricated on 4-inch wafers consisting of 21 mm by 12.5 mm reticles. The reticles were arranged into a total of twelve different subsites. Circuits designed by the University of Arkansas MSCAD team were primarily organized into seven different 5 mm by 5 mm subsites. Between every subsite, 200 µm wide dicing lanes were inserted to allow for individually dicing out the subsites.

The linear regulator is highlighted in red on the die micrograph of an individual reticle shown in Fig. 5.1. An image of the linear regulator die with labels indicating the pin configurations is shown in Fig. 5.2. A total of 18 pads were implemented in the linear regulator and were arranged based upon the layout size relative to adjacent circuits in the subsite. Multiple pads were used for

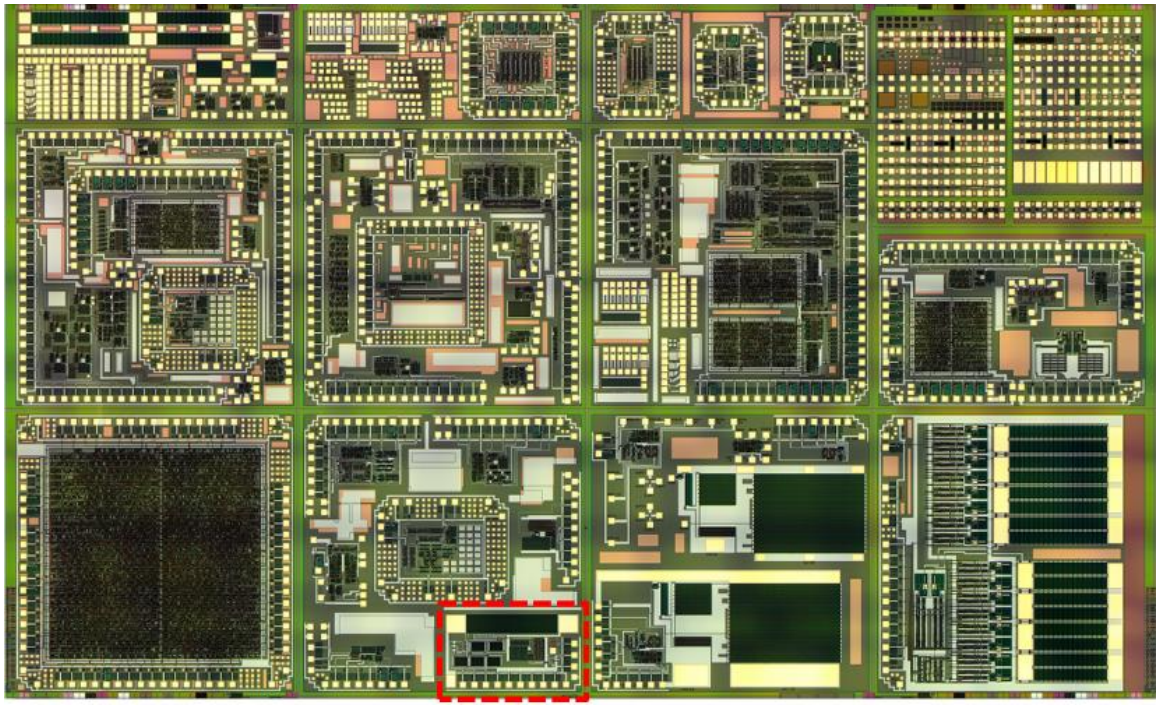

Fig. 5.1. The complete die micrograph from the Vulcan II fabrication run. The linear regulator is highlighted in red.

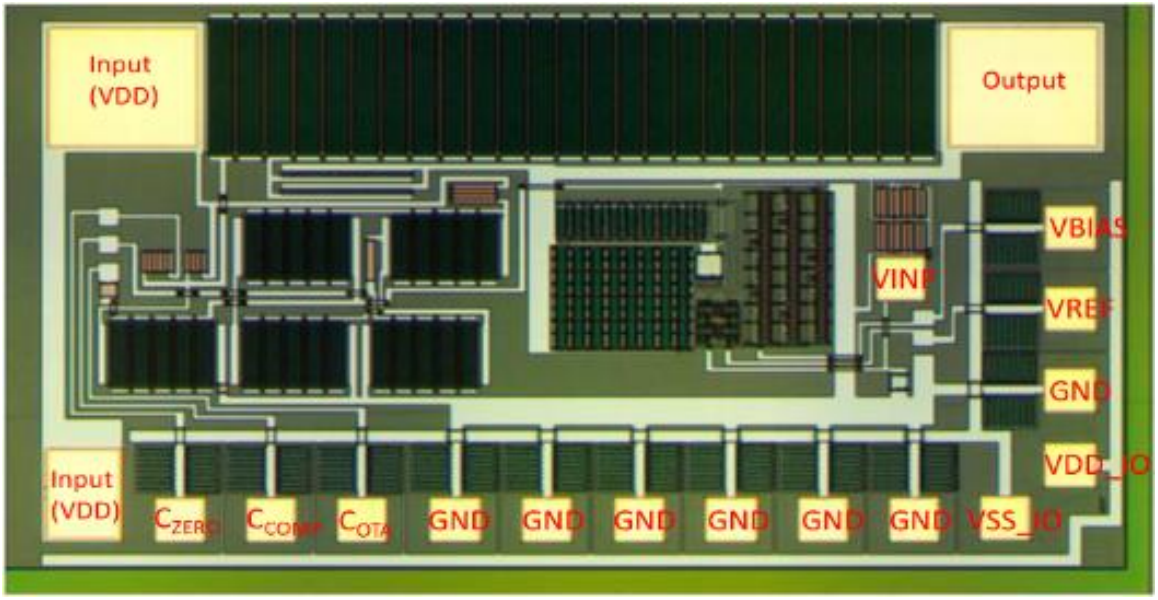

Fig. 5.2. A die micrograph of the linear regulator without adjacent circuitry.

the ground connection, while the input and output pads were made substantially larger than the standard 100 µm by 100 µm analog pads. Other pads, such as VINP, were not necessary for a preliminary pass/fail test. Due to only 6 of the 18 pads being required for a heartbeat test, initial testing was conducted with the Semiprobe probe station. After determining that the circuit was functional, a wafer was diced and the individual die were attached to 68-pin ceramic leaded chip carrier (LDCC) packages with Epotek P1011 conductive epoxy.

Wire bonds between the die and package were then formed with 1 mil gold ball bonding using the K&S 4700 wirebonder in the University of Arkansas High Density Electronics Center (HiDEC). The package with the attached die and wire bonds to the pads is shown in Fig. 5.3. Next, the package was soldered onto a Rogers 4350 printed circuit board (PCB) consisting of header pins to make external connections to breakout boards, oscilloscope probes, etc. The module consisting of the LDCC package soldered onto the Rogers 4350 board is shown in Fig. 5.4. Mounting holes were created in the PCB to allow the board to be supported by a testing fixture when using a hot plate and focusing heat on the die.

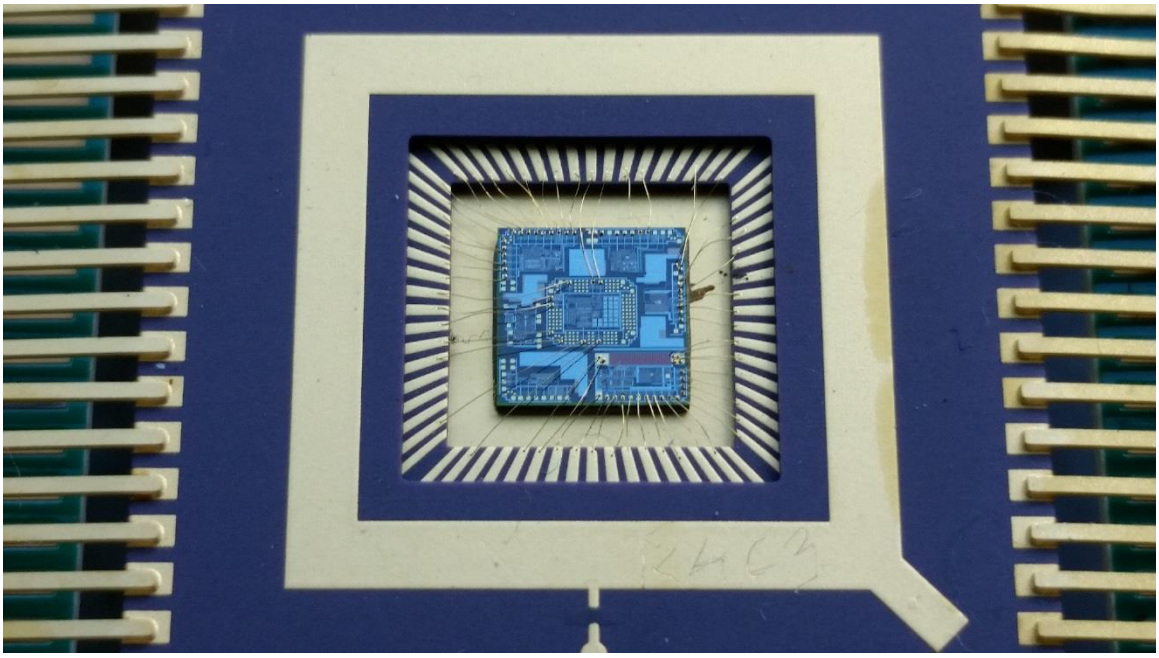

Fig. 5.3. The diced linear regulator subsite die attached to the LDCC package with connections formed by wirebonds.

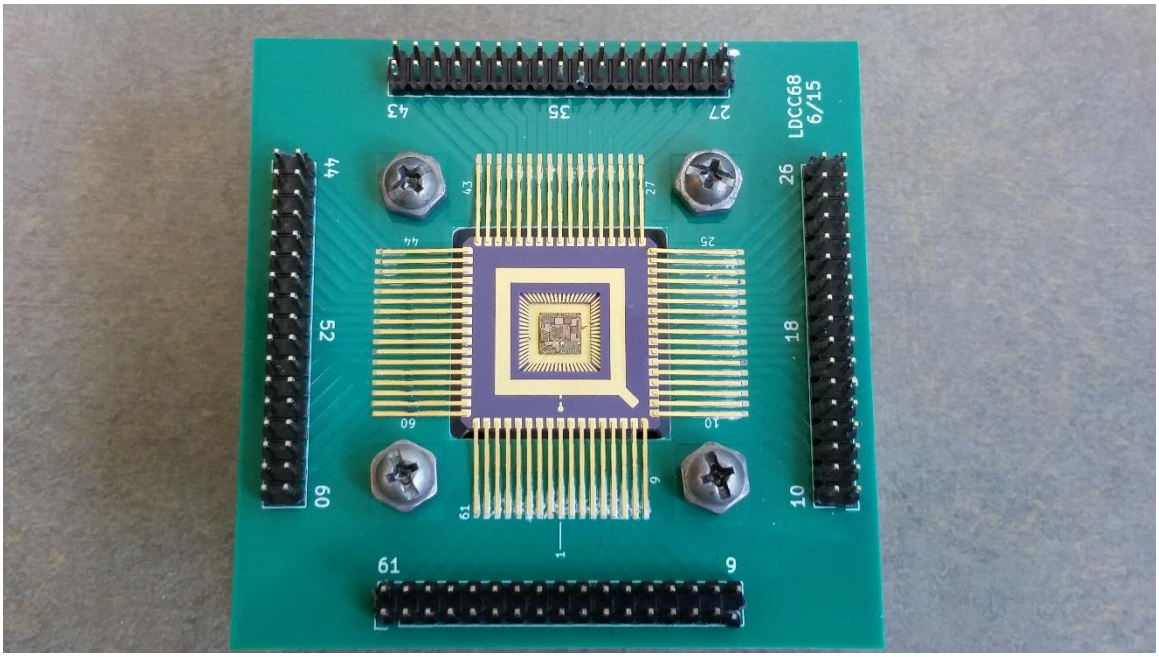

Fig. 5.4. The LDCC package soldered onto the Rogers 4350 board.

Following the LDCC package being soldered onto the Rogers 4350 board, the module was mounted onto the aluminum apparatus shown in Fig. 5.5. The apparatus was constructed with four mounting stands corresponding to the PCB drill holes and a center cylindrical support (or "hot

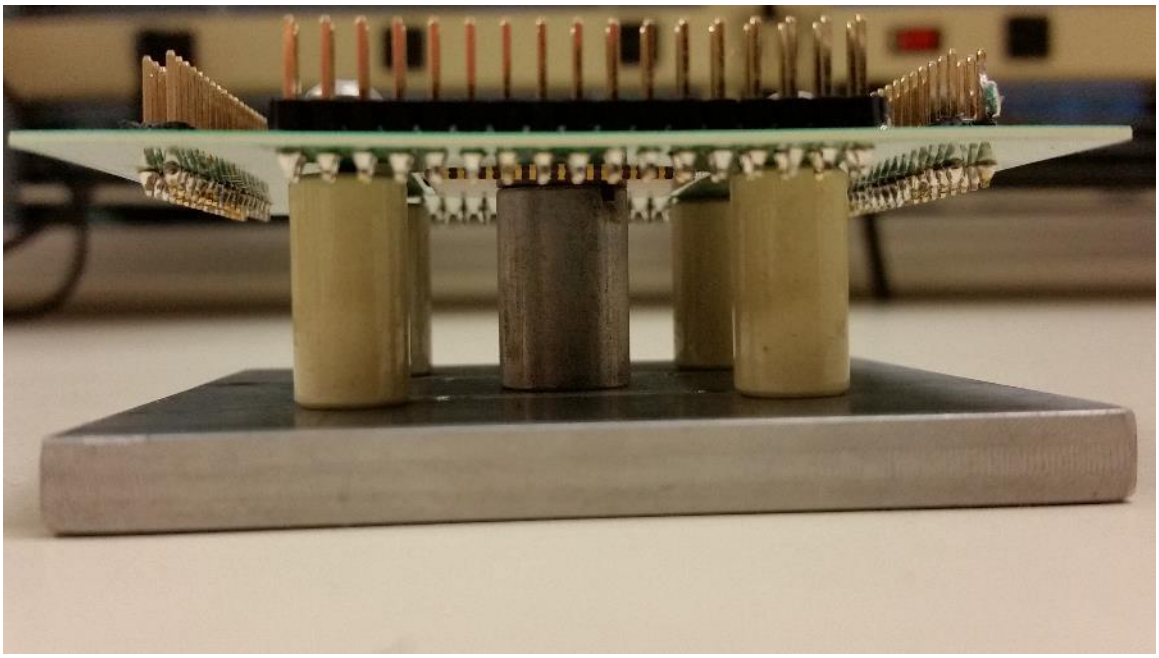

Fig. 5.5. A side-view of the high temperature test fixture.

finger") for applying focused heating to the bottom of the die. A notch was made in the hot finger to insert a thermocouple probe and accurately measure the temperature seen by the die. The thermocouple was then connected to the hot plate being used, allowing the hot plate to be set to a desired temperature. The bottom of the LDCC package underneath the SiC die is ideally the only point to see the heat source. However, the ambient temperature around the Rogers-4350 board will rise proportionally to the temperature seen by the IC. With the hot plate temperature set to approximately 400 ºC, the ambient temperature rises significantly enough that the solder joints between the LDCC package and Rogers-4350 board will reflow. Extended high temperature testing was typically limited to 400 ºC due to the packaging concerns along with performance degradation due to aging and multiple temperature cycles.

The breakout board shown in Fig. 5.6 was designed to connect to the linear regulator die mounted on the high temperature testing apparatus. The intent of the breakout board was to thermally isolate components necessary for characterizing the linear regulator, such as capacitors

Fig. 5.6. The breakout board created for characterizing the linear regulator.

which are limited to approximately 250 ºC unless ordered from a specialty manufacturer. Potentiometers were also soldered onto the breakout board to characterize the linear regulator with various load currents. Similar functionality could have also been achieved with a source meter such as the Tektronix Series 2600B. To create a pulsed load scenario with the potentiometers, a MOSFET was placed in series with each of the potentiometers. A function generator providing a square waveform pulse-train to the gate of the MOSFETs could therefore create load transients.

A block diagram of the linear regulator test setup, excluding the optional source meter and function generator, is shown in Fig. 5.7. In addition to the supply voltage, the reference and bias voltages for the two-stage op-amp were provided by the external power supply. The complete high temperature test setup is shown in Fig. 5.8. Although an oscilloscope was utilized throughout the testing procedure to measure transient outputs, the resolution limitations of the oscilloscope did necessitate the use of a digital multi-meter (DMM) for more accurate output voltage measurements in steady-state scenarios.

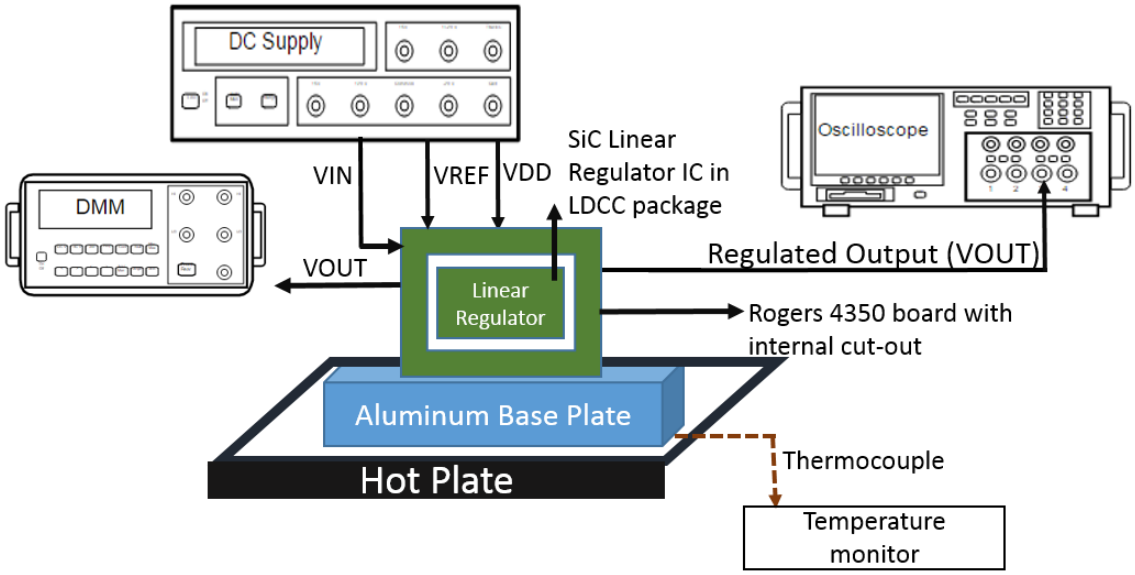

Fig. 5.7. A block diagram for the linear regulator test setup.

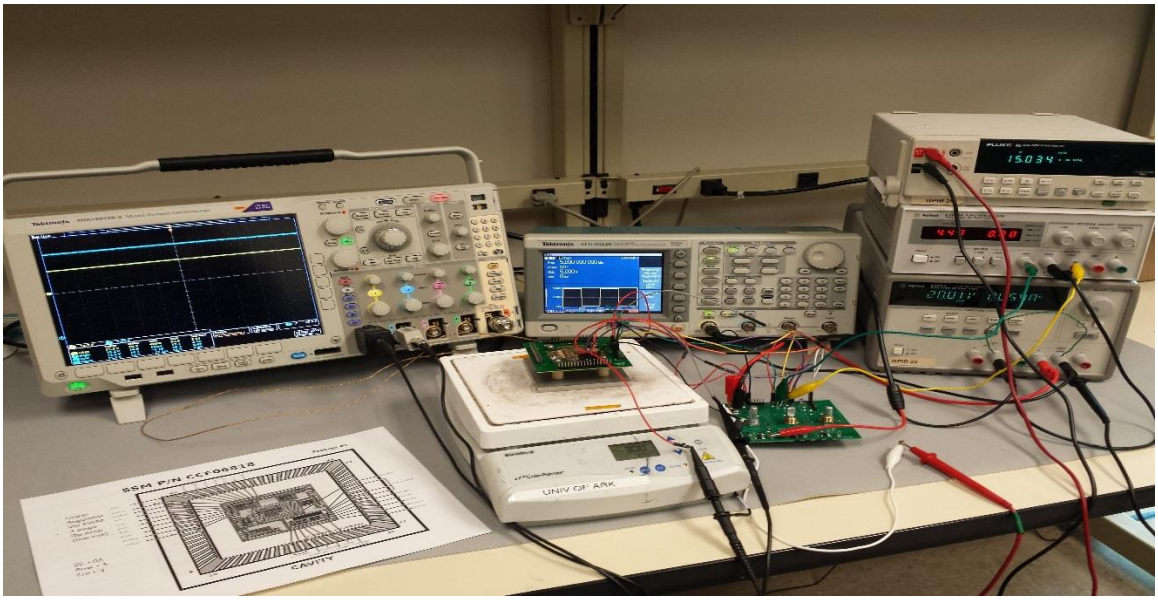

Fig. 5.8. The linear regulator high temperature test setup.

An automated test script, provided in Appendix A, was written in Python to characterize the linear regulator. The script was created for reliability testing in which the output load was set to a fixed 100 mA. The potentiometers on the PCB were used in this case rather than implementing the source meter into the setup. The goal of the automation script was to replicate an offset compensation scheme used in conjunction with the linear regulator.

5.2 Test Results

After performing an initial heartbeat test on the linear regulator using the Semiprobe probe station, seven different reticles were packaged. The packaged reticles are represented by shaded cells on the wafer map shown in Fig. 5.9. Each of the packaged reticles was tested and determined to have yielded properly. Variations in threshold voltages, even between devices that were intended to be matched, were the primary source of performance differences.

The most notable variation is within the two-stage op-amp where the input FETs, along with the PFET active loads, were placed in a common centroid configuration with the intent of being matched. However, the FET mismatches caused the reference voltage required to obtain a 15 V output to vary significantly from the ideal 7.5 V. In the case of the Row 5, Column 2 (R5C2) reticle, a 6.90 V reference voltage was necessary to obtain a 15 V output at 300 ºC. For comparison, a 7.20 V reference voltage was necessary for the same output voltage from the R4C2 reticle.

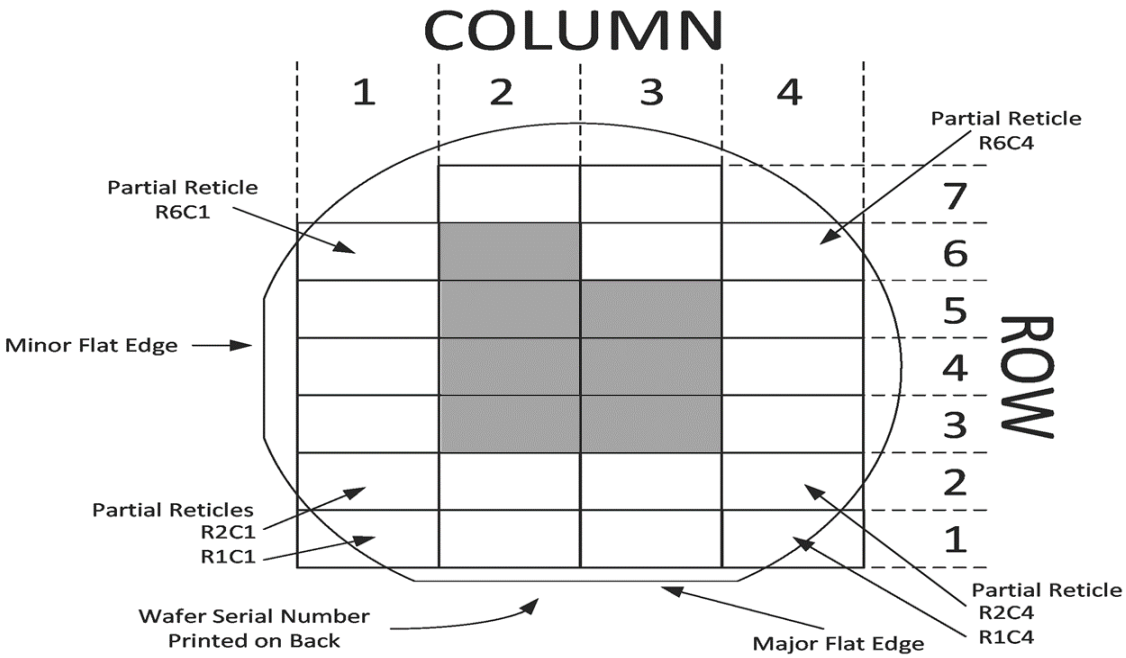

Fig. 5.9. The wafer map with shaded cells indicating the tested reticles.

As mentioned in the previous section, the performance of the linear regulator was found to degrade after operating at high temperature for long periods of time and multiple temperature cycles. For this reason, all but one test was limited to 400 ºC or less. In addition, not all of the packaged linear regulator die were used for the same experiment. Throughout the testing process, a bias voltage of 4.5 V was applied to the op-amp. The reference voltage applied to the VINN terminal of the op-amp was also calibrated such that the offset voltage was cancelled out.

The dropout voltage was the first parameter measured. For the clarity of this test, the dropout voltage is defined as being the difference between input and output voltages when the linear regulator output drops below 95% of its nominal value as the input voltage is decreased. The dropout voltages measured over various load currents and temperature are shown in Fig. 5.10. A limitation of 180 mA was placed on the experiment, which was achieved by the linear regulator for each of the temperatures tested.

The safety margin added to the linear regulator, as discussed during the design section, was intended to allow for 150 mA of load current at 19 V according to the 25 ºC TT models. With a

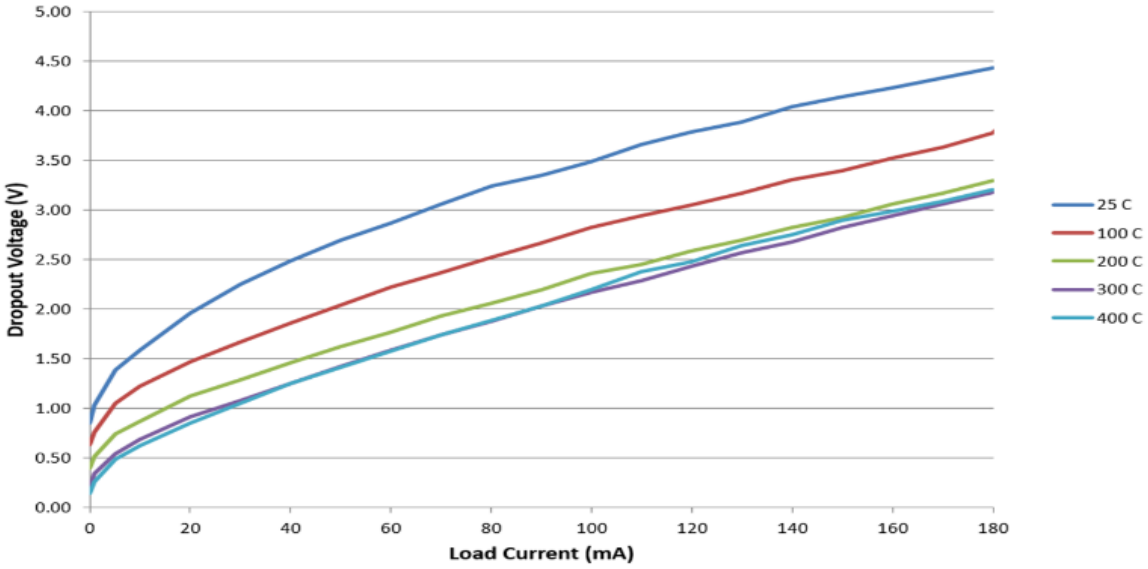

Fig. 5.10. The dropout voltage of the linear regulator (R4C2 reticle).

dropout voltage of 4 V corresponding to a 19 V input voltage, the results provided in Fig. 5.10 show that the goal was nearly achieved on this reticle. Rather than the desired 150 mA, the linear regulator in this reticle (R4C2) was able to provide approximately 140 mA. This indicates that the NFET pass transistor's threshold voltage is marginally higher than predicted by the 25 ºC TT models. Nevertheless, the safety margin ensured that the targeted maximum load current of 100 mA was achieved at each of the tested temperatures.

Line regulation was the next parameter tested. Defined as being the change in output voltage for a given change in input voltage, line regulation is an indicator of the linear regulator's performance over a range of input voltage. The line regulation measurements for the 100 mA, or full load, condition are shown in Fig. 5.11. The line regulation of 1.5 mV/V at 400 ºC represents the worst-case operation during the full load case. On the contrary, the best line regulation performance of 0.8 mV/V occurs at 300 ºC for the full load case. The measured line regulation under the no-load condition is shown in Fig. 5.12. Without a load applied, the worst-case line

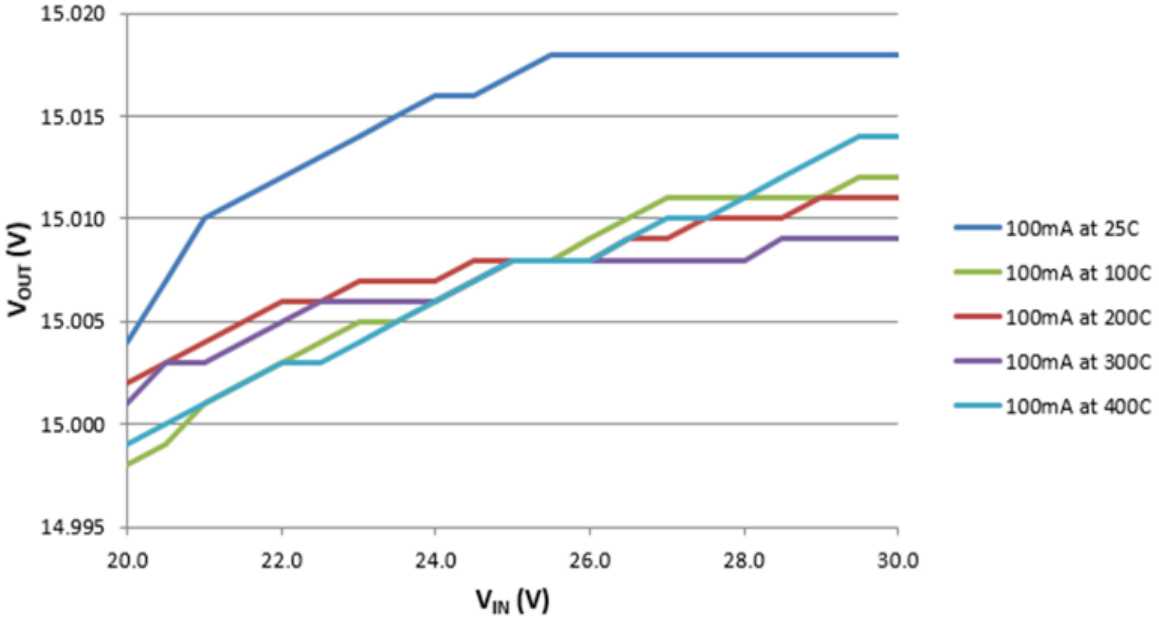

Fig. 5.11. Measured line regulation at full load (100 mA) from 25 ºC to 400 ºC.

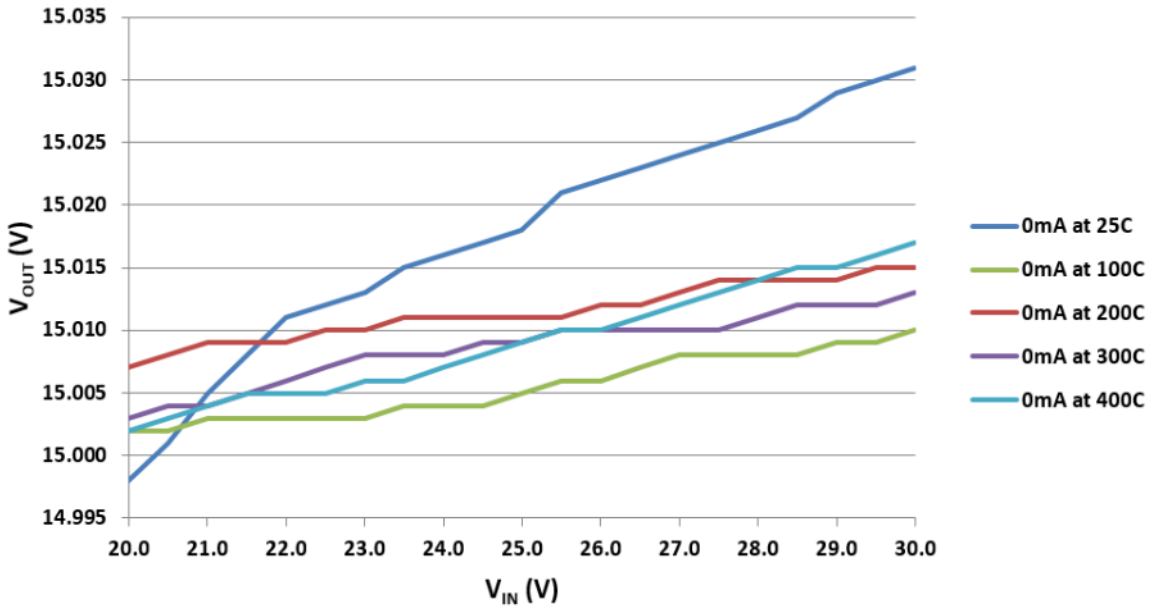

Fig. 5.12. Measured line regulation with no load from 25 ºC to 400 ºC.

regulation performance is measured to be 3.3 mV/V at 25 ºC whereas the best performance is 0.8 mV/V at 100 ºC and 200 ºC.

Table 5.1 on the following page shows the line regulation measurements in mV/V and as a percentage. Table 5.2 compares the measured and simulated results for the line regulation at 100 mA load. Models are not available for 400 ºC, therefore only the measured results have been listed for this item in Table 5.2. An analysis of the linear regulator shows a dependence of the line regulation on the loop gain, load resistance, and the R_{DS} value of the pass transistor. The line regulation performance is expected to improve over temperature, since the loop gain increases and the R_{DS} of the pass transistor decreases per the simulation models. This is generally the case for both the 0 mA and 100 mA cases. A comparison of the measured results at 25 ºC to the results at 300 ºC shows that the line regulation performance is noticeably better. However, the 400 ºC performance indicates that the trend of devices improving over temperature is not uniform. In addition, the trend between 100 ºC and 300 ºC is not clearly defined.

Table 5.1. The line regulation performance over temperature with 0 mA and 100 mA loads.

I_{LOAD} (mA)	Temp (ºC)	Line Regulation (mV/V)	Line Regulation (%)
0	25	3.3	0.22
	100	0.8	0.05
	200	0.8	0.05
	300	1.0	0.07
	400	1.5	0.10
100	25	1.4	0.09
	100	1.4	0.09
	200	1.3	0.09
	300	0.8	0.05
	400	1.5	0.10

Table 5.2. A comparison of the measured and simulated values for line regulation with a 100 mA load.

I_{LOAD} (mA)	Temp (ºC)	Line Regulation (mV/V)		Line Regulation (%)		Texas Instruments UA78L15
		Measured	Simulated	Measured	Simulated	Measured*
100	25	1.4	3.1	0.09	0.021	5.8 mV/V Typical
	100	1.4	2.6	0.09	0.017	
	200	1.3	2.2	0.09	0.015	
	300	0.8	2.2	0.05	0.015	
	400	1.5	-	0.10	-	

*Test conditions: V_{IN} = 20 V to 30 V, I_{LOAD} = 40 mA, junction temperature (T_J) = 25 ºC

A comparison of the Vulcan II linear regulator's line regulation to TI's UA78L15 linear regulator is also given in Table 5.2. At all operating temperatures, the Vulcan II regulator outperforms the UA78L15 regulator. Other commercially available regulators can provide slightly improved performance, as shown in Table 4.12 with TI's TPS731, which generally traces back to an op-amp with a higher gain.

Load regulation indicates the ability of the linear regulator to provide a consistent output voltage over a range of load currents. It is defined as being the change in output voltage for a given change in load current. The load regulation of the linear regulator is shown in Fig. 5.13 and Fig.

5.14 for 20 V and 30 V, respectively. For a 20 V input, the worst-case load regulation at 400 ºC was measured to be 33 mV/A. Similarly, the test conducted at 400 ºC yielded the worst performance for a 30 V input with 42 mV/A.

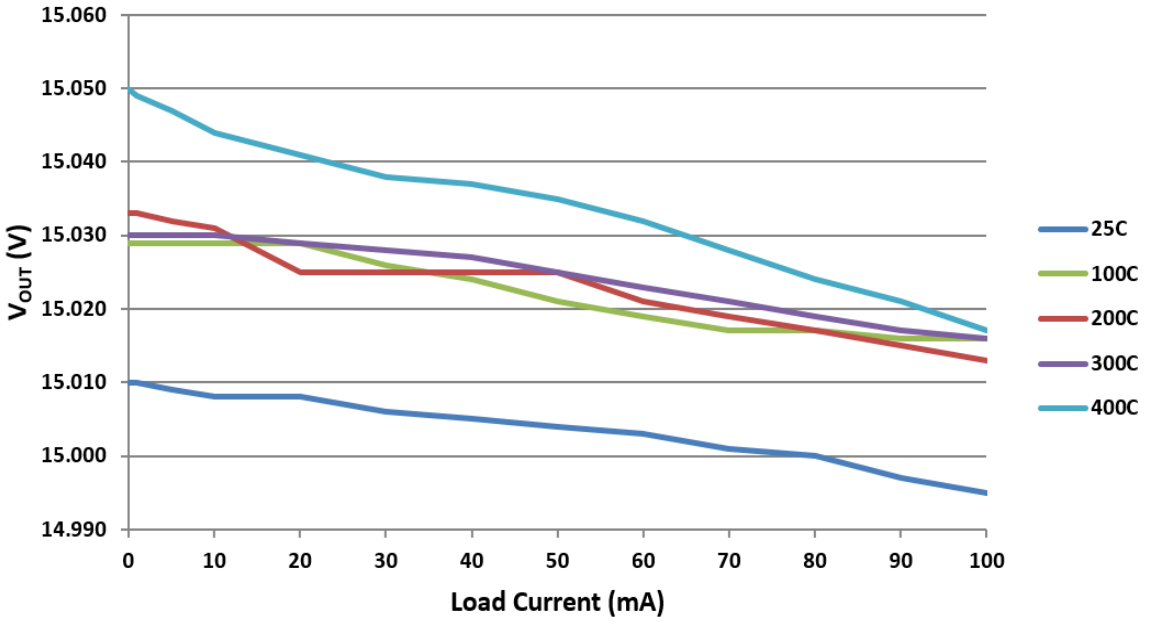

Fig. 5.13. The measured load regulation over temperature for a 20 V input.

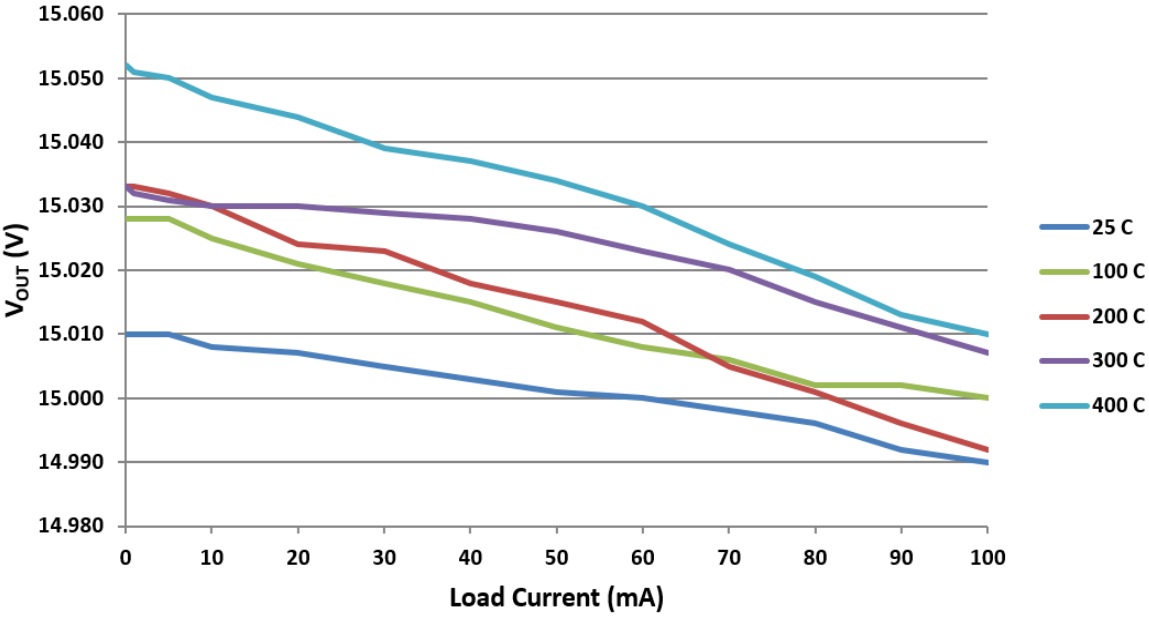

Fig. 5.14. The measured load regulation over temperature for a 30 V input.

The simulation values indicate the load regulation should improve at temperatures above 25 ºC, although there isn't a consistent trend between 100 ºC to 300 ºC. A theoretical analysis points towards a consistently improving load regulation over temperature since it is proportional to the loop gain, which does generally rise with increasing temperature. The remaining factors for the discrepancy between simulations and measurements is the output resistance of the pass transistor and the channel-length modulation. The measured results are summarized in Table 5.3 and a comparison is given with the simulation results in Table 5.4 for the 20 V input case. A comparison to TI's UA78L15 regulator is also provided.

Table 5.3. The load regulation over temperature for input voltages of 20 V and 30 V.

V_{IN} (V)	Temp (ºC)	Load Regulation (mV/mA)	Load Regulation (%)
20	25	0.15	0.010
	100	0.13	0.009
	200	0.20	0.013
	300	0.14	0.009
	400	0.33	0.022
30	25	0.20	0.013
	100	0.28	0.019
	200	0.41	0.027
	300	0.26	0.017
	400	0.42	0.028

Table 5.4. A comparison of the measured and simulated load regulation values over temperature for the 20 V case.

V_{IN} (V)	Temp (ºC)	Load Regulation (mV/mA)		Load Regulation (%)		Texas Instruments UA78L15
		Measured	Simulated	Measured	Simulated	Measured*
20	25	0.15	0.16	0.010	0.011	0.385 mV/mA
	100	0.13	0.11	0.009	0.007	
	200	0.20	0.13	0.013	0.009	
	300	0.14	0.12	0.009	0.008	
	400	0.33	-	0.022	-	

*Test conditions: V_{IN} = 23 V, I_{LOAD} = 1 mA to 40 mA, junction temperature (T_J) = 25 ºC

The quiescent current of the Vulcan II linear regulator is shown in Fig. 5.15. A maximum quiescent current of approximately 5 mA occurs at 30 V for 200 ºC to 400 ºC. The rise over temperature is due to the op-amp bias current increasing as threshold voltages decrease and the current consumption of the level shifter also increasing as the resistance values drop. An increase in input voltage further increases the quiescent current primarily due to the voltage drop across the resistances of the level shifting and the compensation scheme. Comparing the measured results to the simulated values in Table 4.2, which listed the quiescent current for an input voltage of 20 V, the measured quiescent current of the linear regulator was lower than in simulations. For the die tested for Fig. 5.15, this is primarily attributed to larger resistances than designed for.

After characterizing the linear regulator's dropout voltage, quiescent current, along with line and load regulation performance, the R4C2 die used throughout the measurements was taken up to 530 ºC to determine its functionality. The packaging concerns for operating temperatures

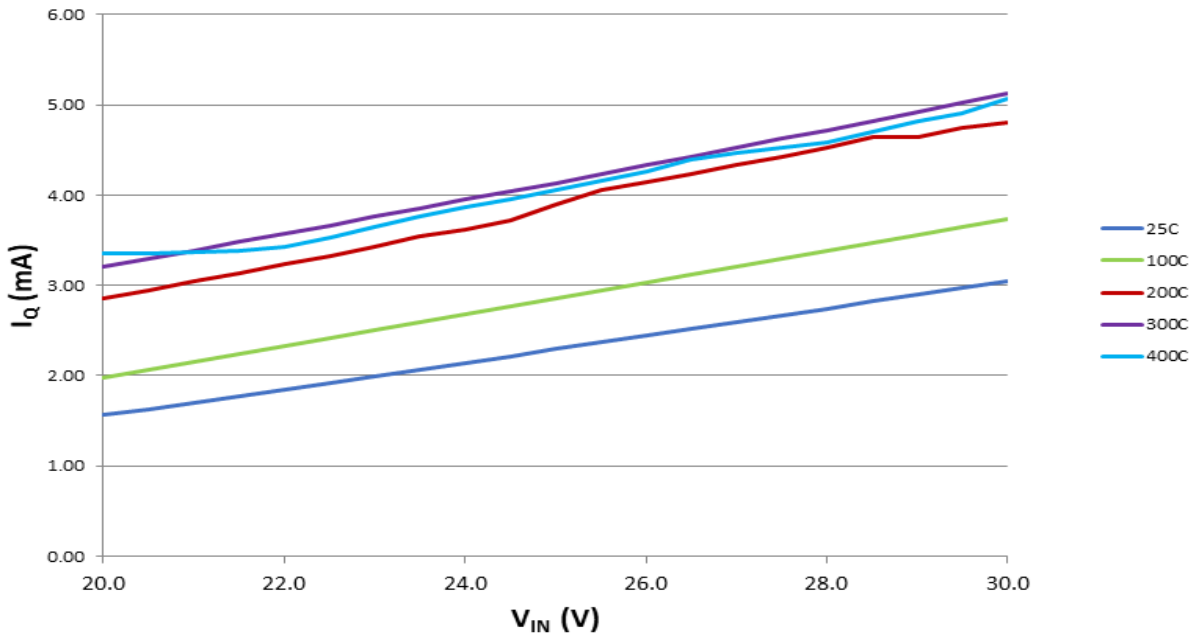

Fig. 5.15. The measured quiescent current of the Vulcan II linear regulator over temperature and input voltage.

above 400 ºC, primarily the reflow of solder joints, limited the amount of time available to test using the test configuration with a hot plate. Therefore, pulsed load tests were performed such that the input voltage was 20 V and the load current was varied from 0 mA to 100 mA.

An initial pulsed load test was conducted at 300 ºC to serve as a reference. The results in Fig. 5.16 show the input and output voltage, both of which are AC coupled. During the load transient, the AC coupled output spikes by approximately 140 mV from the nominal 15.0 V DC output on the 100 mA to 0 mA load transition. The output then drops by approximately 300 mV during the 0 mA to 100 mA transition. In each case, the output has a 1% settling time of less than 10 µs which is consistent with the simulation results reported in Chapter 4.

The results of the pulsed load test at 530 ºC are shown in Fig. 5.17. Note that the time scale has changed to 2 µs per division from 40 µs per division in Fig. 5.16. In addition, the output is DC coupled as opposed to AC coupled. The spike of the output voltage during the 100 mA to 0 mA

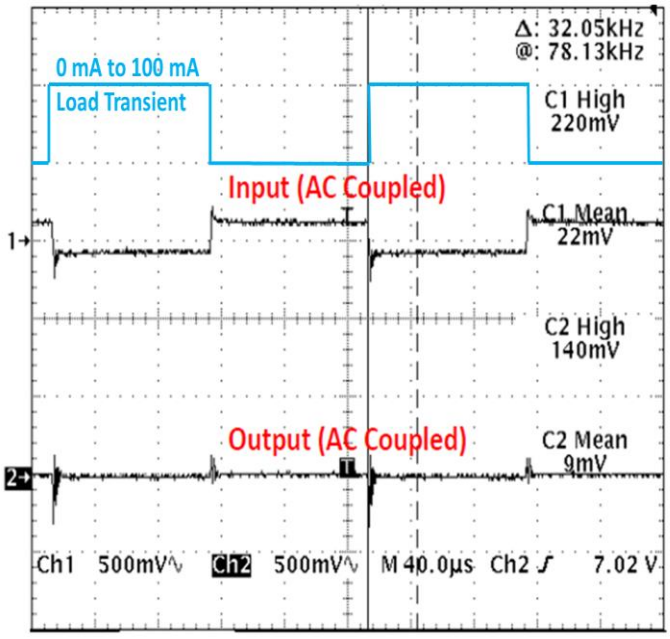

Fig. 5.16. The 100 mA pulsed load test at 300 ºC.

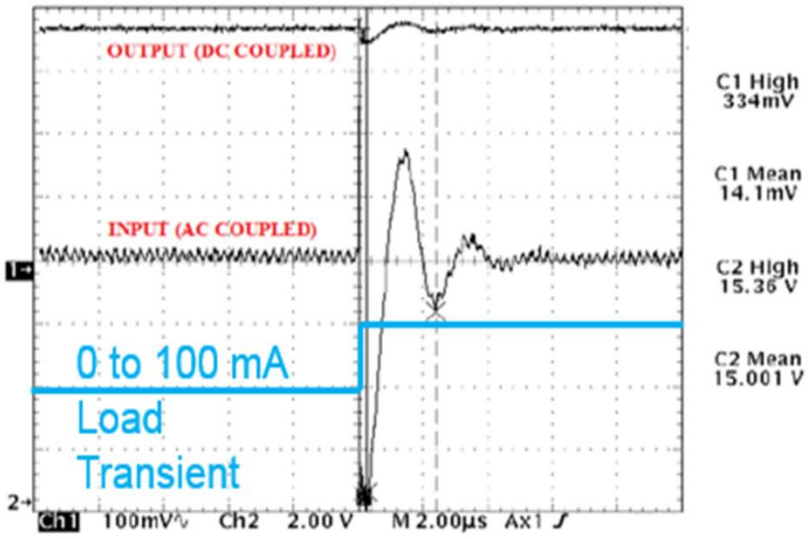

Fig. 5.17. The 100 mA pulsed load test at 530 ºC.

load transient is approximately 200 mV. Similarly, the drop of the output voltage during the 0 mA to 100 mA transition is approximately 400 mV. Neither case marks a drastic difference from the 300 ºC pulsed load test. This is to be expected since the load capacitance in each case is 940 nF. However, the settling time of the output voltage decreases to less than 5 µs in the 530 ºC test. This indicates that the linear regulator's bandwidth has extended out to higher frequencies, supporting the trend of FETs becoming faster at higher temperatures.

The reliability of the linear regulator was the final point of emphasis in the testing process. Future SiC power management ICs can be better optimized by finding potential failure mechanisms with the Vulcan II linear regulator. Due to previously observed aging and temperature cycling effects, it was decided that an untested die would be more suitable for this effort than continuing to use R4C2. The R5C2 reticle was therefore selected for this test.

The automation script for reliability testing presented in Appendix A was used to measure the input and output voltages every five minutes. The reference voltage was also calibrated when necessary throughout the test to keep the output voltage within +/- 100 mV of the nominal 15 V

output. The reference voltage shifts based upon the two-stage op-amp's offset voltage that results from mismatches in the active load PFETs and input NFETs. The calibration technique was implemented to represent the potential of an offset compensation scheme. Prior to starting the reliability test, the op-amp had a 0.6 V offset voltage at 300 ºC. With the feedback network set to provide a 7.5 V input to the op-amp with a 15.0 V output, the required reference voltage due to the offset was 6.9 V.

The output voltage of the regulator operating over 30 hours is shown in Fig. 5.18. The automatically calibrated reference voltage is subsequently shown in Fig. 5.19. Sustained operation of the circuit was carried out in 10 hour increments followed by cool down periods of 14 hours. The results indicate that there was an initial burn-in period in which the offset voltage gradually increased. The offset voltage then began to decrease, reaching 6.90 V at the end of the 1st temperature and power cycle. Beginning with the 2nd cycle, the reference voltage started closer to the ideal value at 6.92 V. The offset again increased and caused the reference to once more stabilize

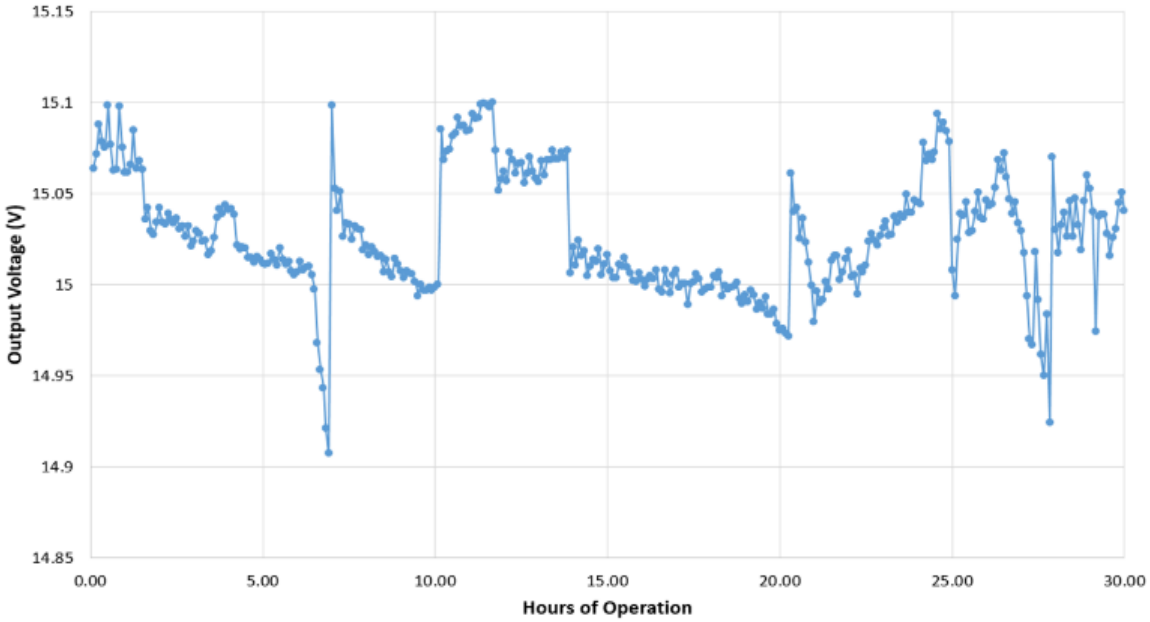

Fig. 5.18. The regulator's output voltage over the 30-hour reliability test at 300 ºC

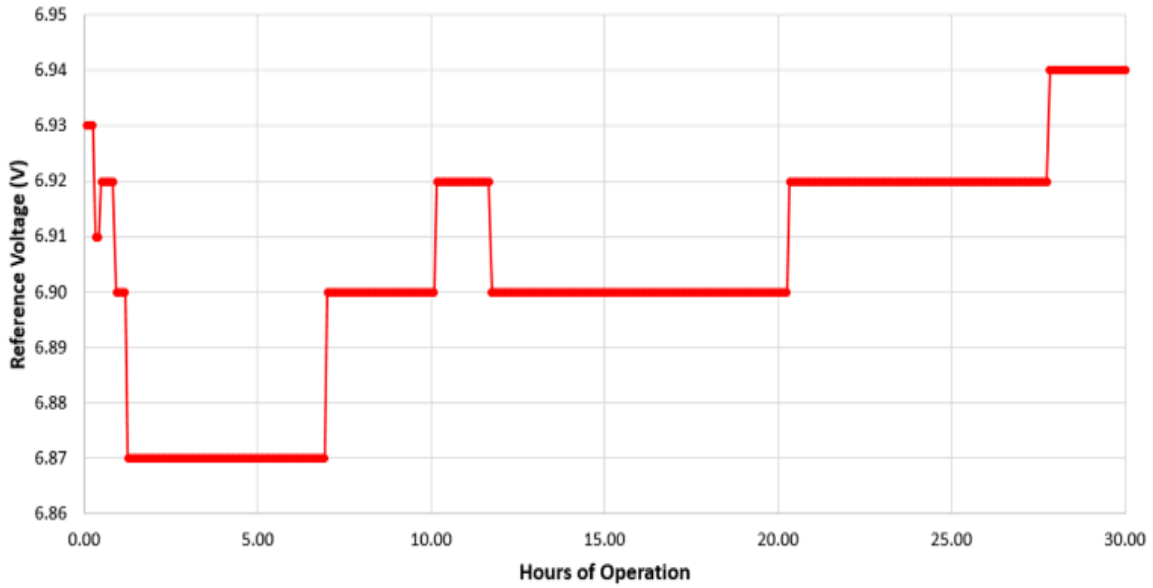

Fig. 5.19. The reference voltage applied to the regulator throughout the reliability test.

at 6.90 V. The offset voltage primarily decreased throughout the 3rd cycle, resulting in a higher reference voltage.

The results of the reliability test demonstrate the difficulty of accurately modeling a trend of the offset voltage over power and temperature cycles. Nevertheless, the reference voltage only shifted by a maximum of 40 mV from its original value of 6.90 V corresponding to an output voltage delta of approximately 80 mV. Accounting for the reference voltage variation and the maximum output voltage change of 100 mV in Fig. 5.17, the overall shift of the output voltage did not exceed +/- 200 mV over the 30-hour reliability test. A 200 mV potential variation equates to a change of only 1.33%, which is relatively stable performance given the developing nature of SiC IC technology.

CHAPTER 6 CONCLUSION AND FUTURE WORK

6.1 Conclusions and Contributions to the State of the Art

This work has presented multiple solutions for the advancement of power management integrated circuitry in SiC. The first SiC CMOS linear regulator was designed for operation from room temperature to over 300 ºC and was subsequently fabricated and determined to be functional up to 530 ºC. Reliability testing was conducted on the linear regulator and showed stable performance with only 1.33% change in output voltage over 30 hours of operation at 300 ºC.

The design of the linear regulator has been refined in the form of fully on-chip linear regulators. A low-dropout linear regulator design with a PFET pass transistor has been shown along with an NFET pass transistor based design. These regulators reduce the system footprint by eliminating the requirement of external surface mount capacitors. The reliability and operating temperature range of the regulator are both improved since there is no longer a constraint posed by capacitor dielectric materials, which are limited to 250 ºC in commercially available capacitors or approximately 350 ºC when ordered from specialized manufacturers.

In conjunction with the effort to design the fully-on chip linear regulators, multiple operational amplifier architectures were designed and evaluated in simulation. The multipath recycling folded-cascode op-amp was determined to be suitable for the on-chip linear regulators since it provided high gain (60 dB or more over temperature) and relatively high bandwidth. It also allowed for an acceptable distance between the frequency of the 1st and 2nd poles, which ultimately improved the stability and overall frequency response of the linear regulators.

Due to the relatively high gain of the multipath recycling folded-cascode op-amp, the NFET pass transistor based fully on-chip linear regulator has demonstrated significantly improved

line and load regulation performance in simulations versus the Vulcan II linear regulator. In Chapter 4, the performance was compared to Texas Instrument's TPS731 external capacitor-less silicon linear regulator. With respect to the silicon based counterpart, the fully on-chip SiC linear regulator with an NFET pass transistor offers a line regulation that is almost one order of magnitude better and a load regulation that is superior by nearly two orders of magnitude. Line and load regulation performance can be further improved by using a high gain op-amp, such as a standard three-stage or four-stage op-amp, in parallel with the multipath recycling folded-cascode op-amp. The enhanced performance allows applications with potentially large output current and input voltage swings to suffer less severe changes in supply voltage.

Finally, a switched capacitor converter was designed to provide a more efficient DC-DC converter solution. As discussed in Chapters 3 and 4, this design is contingent upon the application requirements and the MOSFETs being rated to withstand certain gate voltages. If the MOSFETs have the necessary voltage ratings, then the switched capacitor converter can enable step-down efficiencies of more than 70% according to simulations. This enables remote, extreme environment applications to demand less power while also being more flexible to the available power supply. For system-in-package applications such as sensing and data acquisition system, the enhanced power efficiency can allow for devoting more power to the state-of-the-art SiC analog-to-digital converter (ADC) and improving its resolution [72].

6.2 Future Work

As SiC IC technology continues to develop and proceed to commercially available products, process variation and reliability of the circuits will be key issues. Identifying an offset cancellation scheme to negate transistor mismatches within the linear regulator's op-amp will be one challenge to overcome. It has been shown in Chapter 5 that MOSFETs in a common centroid

configuration can have a threshold difference of hundreds of millivolts, making an offset cancellation scheme vital for obtaining a well-regulated output.

Multiple sub-circuits ranging from a VCO and digital controller were used to form the switched capacitor converter. For new process technologies, an efficiency analysis of each block will be required to determine how to size the MOSFETs, what switching frequency to use, and how many conversion ratios to implement. Another potential improvement is simplifying the digital logic if possible. Utilizing a synthesizer, with the appropriate timing analysis, can lead to a more power efficient digital controller.

BIBLIOGRAPHY

[1] P. G. Neudeck, R. S. Okojie, and L.-Y. Chen, “High-temperature electronics - a role for wide bandgap semiconductors?” *Proc. IEEE*, vol. 90, no. 6, pp. 1065–1076, Jun. 2002.

[2] H. Kappert, N. Kordas, S. Dreiner, U. Paschen, and R. Kokozinski, “High temperature SOI CMOS technology and circuit realization for applications up to 300°C,” in *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2015, pp. 1162–1165.

[3] J. M. Hornberger, E. Cilio, R. M. Schupbach, A. B. Lostetter and H. A. Mantooth, "A High-Temperature Multichip Power Module (MCPM) Inverter utilizing Silicon Carbide (SiC) and Silicon on Insulator (SOI) Electronics," *Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE*, Jeju, 2006, pp. 1-7.

[4] H. A. Mantooth, M. D. Glover, and P. Shepherd, “Wide Bandgap Technologies and Their Implications on Miniaturizing Power Electronic Systems,” *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 2, no. 3, pp. 374–385, Sep. 2014.

[5] T. Funaki, J. C. Balda, J. Junghans, A.S. Kashyap, H. A. Mantooth, F. Barlow, T. Kimoto, and T. Hikihara, “Power Conversion With SiC Devices at Extremely High Ambient Temperatures,” *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1321–1329, Jul. 2007.

[6] A. Elasser and T. P. Chow, “Silicon carbide benefits and advantages for power electronics circuits and systems,” *Proc. IEEE*, vol. 90, no. 6, pp. 969–986, Jun. 2002.

[7] B. W. Ohme and M. R. Larson, "Control circuit design for high temperature linear regulators," in *High Temperature Electronics Conference, 1998. HITEC. 1998 Fourth International*, Albuquerque, NM, 1998, pp. 45-50.

[8] J. A. Valle-Mayorga, A. Rahman, and H. A. Mantooth, "A SiC NMOS Linear Voltage Regulator for High-Temperature Applications," in *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2321-2328, May 2014.

[9] A. M. Francis, J. Holmes, N. Chiolino, M. Barlow, A. Abbasi, and H. A. Mantooth, “High-Temperature Operation of Silicon Carbide CMOS Circuits for Venus Surface Application,” in *IMAPS High Temperature Electronics Conference (HiTEC)*, 2016, vol. 2016, pp. 242–248.

[10] P. G. Neudeck, D. J. Spry, L.-Y. Chen, G. M. Beheim, R. S. Okojie, C. W. Chang, R.D. Meredith, T. L. Ferrier, L. J.. Evans, M. J. Krasowski, N. F. Prokop, “Stable Electrical Operation of 6H–SiC JFETs and ICs for Thousands of Hours at 500 degrees Celsius,” *Electron Device Lett.*, May 2008.

[11] A. Rahman, K. Addington, M. Barlow, S. Ahmed, H.A. Mantooth, "High-Temperature SiC CMOS Comparator and op-amp for Protection Circuits in Voltage Regulators and

Switch-Mode Converters," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 935-945, Sept. 2016.

[12] Tsunenobu Kimoto and James A. Cooper, "Physical Properties of Silicon Carbide," in *Fundamentals of Silicon Carbide Technology:Growth, Characterization, Devices and Applications*. Wiley-IEEE Press, 2014.

[13] D. B. Slater, G. M. Johnson, L. A. Lipkin, A. V. Suvorov, and J.W. Palmour, "Demonstration of 6H-SiC CMOS technology*," in Proc. 3rd Int. High-Temperature Elec. Conf. (HiTEC)*, 1996, pp. XVI- 27–XVI-32.

[14] S. Ryu and K. T. Kornegay, "Design and fabrication of depletion load NMOS integrated circuits in 6H-SiC," in *Inst. Phys. Conf.*, ch. 4. London, U.K., 1996, pp. 789–792.

[15] W. Xie, J. Cooper J. A., and M. R. Melloch, "Monolithic NMOS digital integrated circuits in 6H-SiC," *IEEE Electron Device Lett.*, vol. 15, no. 11, pp. 455–457, Nov. 1994.

[16] D. M. Brown, M. Ghezzo, J. Kretchmer, V. Krishnamurthy, G. Michon, and G. Gati, "High temperature silicon carbide planar IC technology and first monolithic SiC operational amplifier IC," *in Proc. 2nd Int. High-Temperature Elec. Conf. (HiTEC)*. Vol. 1. 1994.

[17] J.-S. Chen, K. T. Kornegay, and S.-H. Ryu, "A silicon carbide CMOS intelligent gate driver circuit with stable operation over a wide temperature range," *IEEE J. Solid-State Circuits*, vol. 34, no. 2, pp. 192– 204, Feb. 1999.

[18] M. Gurfinkel, J. Suehle, J. B. Bernstein, Y. Shapira, A. J. Lelis, D. Habersat, and N. Goldsman, "Ultra-fast characterization of transient gate oxide trapping in SiC MOSFETs," *Proc. 45th Annual IEEE Int. Rel. Phys. Symp*., pp. 462–466, 2007.

[19] A. J. Lelis, D. Habersat, G. Lopez, J. M. McGarrity, F. B. McLean, and N. Goldsman, "Bias stress-induced threshold-voltage instability of SiC MOSFETs," *Materials Science Forum*, vol. 527–529, p. 1317-1320, 2006.

[20] S. Suzuki, S. Harada, R. Kosugi, J. Senzaki, W. Cho, and K. Fukuda, "Correlation between channel mobility and shallow interface traps in SiC metal–oxide–semiconductor field-effect-transistors," *Journal of Applied Physics*, vol. 92, no. 10, pp. 6230–6234, Nov. 2002.

[21] A. Poggi, F. Moscatelli, S. Solmi, and R. Nipoti, "Investigation on the Use of Nitrogen Implantation to Improve the Performance of N-Channel Enhancement 4H-SiC MOSFETs," *IEEE Transaction on Electron Devices*, vol. 55, no. 8, Aug. 2008.

[22] A. Agarwal, M. Das, B. Hull, S. Krishnaswami, J. Palmour, J. Richmond, S. H. Ryu, and J. Zhang, "Progress in Silicon Carbide Power Devices," *Device Research Conference*, pp. 155-158, 2006.

[23] M. D. Glover, P. Shepherd, A. M. Francis, M. Mudholkar, H. A. Mantooth, M. N. Ericson, S. S. Frank, C. L. Britton, L. D. Marlino, T. R. McNutt, A. Barkley, B. Whitaker, and A. B. Lostetter, "A UVLO Circuit in SiC Compatible With Power MOSFET Integration," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 3, pp. 425-433, Sept. 2014.

[24] C.P. Chen and R. Ghandi, "Designing silicon carbide NMOS integrated circuits for wide temperature operation," in *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, Lisbon, pp. 109-11, 2015.

[25] S. Kargarrazi, L. Lanni, S. Saggini, A. Rusu, and C.-M. Zetterling, "500 °C Bipolar SiC Linear Voltage Regulator," *IEEE Transactions on Electron Devices*, vol. 62, no. 6, pp. 1953–1957, Jun. 2015.

[26] S. L. Garverick, C.-W. Soong, and M. Mehregany, "SiC JFET integrated circuits for sensing and control at temperatures up to 600 °C," *2012 IEEE Energytech*, pp. 1–6, 2012.

[27] M. Alexandru, V. Banu, P. Godignon, M. Vellvehi, and J. Millan, "4H-SiC MESFET specially designed and fabricated for high temperature integrated circuits," *Proceedings of the European Solid-State Device Research Conference (ESSDERC)*, pp. 103–106, 2013.

[28] D. T. Clark, E. P. Ramsay, A. E. Murphy, D. A. Smith, R. F. Rhompson, R. A. R. Young, J. D. Cormack, C. Zhu, S. Finney, and J. Fletcher, "High temperature silicon carbide CMOS integrated circuits," in *Materials Science Forum*, vol. 679, pp. 726-729. 2011.

[29] E. P. Ramsay, D. T. Clark, J. D. Cormack, A. E. Murphy, D. A. Smith, R.F. Thompson, R. A. R. Young, and S. Finney, "Digital and Analogue Integrated Circuits in Silicon Carbide for High Temperature Operation," in *IMAPS High Temperature Electron. Conf., Albuquerque, NM, USA*. 2012.

[30] A. M. Francis, T. Moudy, J. A. Holmes, A. Rahman, M. Barlow, S. Ahmed, H.A. Mantooth, "Towards standard component parts in silicon carbide CMOS," in *2015 IEEE Aerospace Conference*, 2015, pp. 1–9.

[31] A. Rahman, P. D. Shepherd, S. A. Bhuyan, S. Ahmed, S. K. Akula, L. Caley, H.A. Mantooth, J. Di, A.M. Francis, and J. A. Holmes, "A family of CMOS analog and mixed signal circuits in SiC for high temperature electronics," in *Aerospace Conference, 2015 IEEE*, pp. 1-10. IEEE, 2015.

[32] P. Shepherd, A. Rahman, S. Ahmed, A. M. Francis, J. Holmes, and H. A. Mantooth, "500 kHz – 5 MHz Phase-Locked Loops in High-Temperature Silicon Carbide CMOS," *Additional Conferences (Device Packaging, HiTEC, HiTEN, & CICMT)*, vol. 2014, no. HITEC, pp. 76–83, Jan. 2014.

[33] N. Kuhns, L. Caley, A. Rahman, S. Ahmed, J. Di., H.A. Mantooth, A.M. Francis, and J. Holmes, "Complex High-Temperature CMOS Silicon Carbide Digital Circuit Designs,"

IEEE Transactions on Device and Materials Reliability, vol. 16, no. 2, pp. 105- 111, Jun. 2016.

[34] R. C. Murphree, S. Ahmed, M. Barlow, A. Rahman, H. A. Mantooth, and A. M. Francis, "A CMOS SiC Linear Voltage Regulator for High Temperature Applications," *International Conference on High Temperature Electronics (HiTEC)*, vol. 2016, pp. 106–111, Jan. 2016.

[35] M. Barlow, S. Ahmed, H. A. Mantooth, and A. M. Francis, "An integrated SiC CMOS gate driver," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 1646–1649, 2016.

[36] M. R. Benavides *et al.*, "Low Power Silicon Carbide RS-485 Transceiver," *International Conference on High Temperature Electronics (HiTEC)*, vol. 2016, pp. 257–262, Jan. 2016.

[37] B. K. Thandri and J. Silva-Martinez, "A robust feedforward compensation scheme for multistage operational transconductance amplifiers with no Miller capacitors", *IEEE J. Solid-State Circuits*, vol. 38, no. 2, pp. 237-243, Feb. 2002.

[38] R. Mita, G. Palumbo, and S. Pennisi, "Design guidelines for reversed nested Miller compensation in three-stage amplifiers," *IEEE Trans. Circuits Syst. II Analog Digit. Signal Process.*, vol. 50, pp. 227-233, May 2003.

[39] D. Grasso, G. Palumbo, and S. Pennisi, "Advances in Reversed Nested Miller Compensation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 7, pp. 1459-1470, Jul. 2007

[40] R. Assaad and J. Silva-Martinez, "Enhancing general performance of folded cascode amplifier by recycling current," *Electronics Letters*, vol. 43, no. 23, pp. 1243–1244, 2007.

[41] R. Assaad and J. Silva-Martinez, "Recent Advances on the Design of High-Gain Wideband Operational Transconductance Amplifiers," VLSI Design, vol. 2009, Article ID 323595, 11 pages, 2009.

[42] R. S. Assaad and J. Silva-Martinez, "The Recycling Folded Cascode: A General Enhancement of the Folded Cascode Amplifier," in *IEEE Journal of Solid-State Circuits*, vol. 44, no. 9, pp. 2535-2542, Sept. 2009.

[43] C. Zou, N. Zhang, D. Kushner, R. Orchard, C. Mi, and S. Zhang, "High Temperature Capacitors With High Energy Density," in IEEE Int.l Power Modulator and High Voltage Conf. (IPMHVC), pp. 419– 421, 2012.

[44] J. Colmenares, S. Kargarrazi, H. Elahipanah, H.P. Nee, and C.M. Zetterling, "High-Temperature Passive Components for Extreme Environments," in *2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Fayetteville, AR, 2016, pp. 271-274.

[45] J. Wibben and R. Harjani, “A high-efficiency DC-DC converter using 2 nH integrated inductors,” IEEE J. Solid-State Circuits, vol. 43, no. 4, pp. 844–854, Apr. 2008.

[46] C. Huang and P. K. T. Mok, “An 84.7% efficiency 100-MHz package bondwire-based fully integrated buck converter with precise DCM operation and enhanced light-load efficiency,” IEEE J. Solid-State Circuits, vol. 48, no. 11, pp. 2595–2607, Nov. 2013.

[47] M. Lee, Y. Choi, and J. Kim, “A 500-MHz, 0.76-W/mm Power Density and 76.2% Power Efficiency, Fully Integrated Digital Buck Converter in 65-nm CMOS,” IEEE Transactions on Industry Applications, vol. 52, no. 4, pp. 3315–3323, Mar. 2016.

[48] S. R. Sanders, E. Alon, H.P. Le, M. D. Seeman, M. John, and V. W. Ng, “The Road to Fully Integrated DC-C Conversion via the Switched-Capacitor Approach,” IEEE Transactions on Power Electronics, vol. 28, no. 9, pp. 4146–4155, Sept. 2013.

[49] V. Ng, M. Seeman, and S. Sanders, “Minimum PCB footprint point-of-load DC–DC converter realized with switched-capacitor architecture,” in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2009, pp. 1575–1581.

[50] L. Chang, R. K. Montoye, B. L. Ji, A. J. Weger, K. G. Stawiasz, and R. H. Dennard, “A fully-integrated switched-capacitor 2:1 voltage converter with regulation capability and 90% efficiency at 2.3 A/mm2 ,” in *Proc. 2010 IEEE Symp. VLSI Circuits (VLSIC)*, 2010, pp. 55–56.

[51] H. Meyvaert, T. Van Breussegem, and M. Steyaert, “A 1.65 W fully integrated 90 nm bulk CMOS intrinsic charge recycling capacitive DC–DC converter: Design & techniques for high power density,” in *Proc. IEEE Energy Conver. Congr. Expo. Phoenix*, 2011, pp. 3234–3241.

[52] H. P. Le, S. R. Sanders, and E. Alon, “Design techniques for fully integrated switched-capacitor DC–DC converters,” *IEEE J. Solid-State Circuits*, vol. 46, no. 9, pp. 2120–2131, Sep. 2011.

[53] G. V. Pique, “A41-phase switched-capacitor power converter with 3.8mV output ripple and 81% efficiency in baseline 90 nmCMOS,” in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers* , Feb. 2012, pp. 98–100.

[54] T. M. Anderson, F. Krismer, and J. W. Kolar, “A 4.6 W/mm2 power density 86% efficiency on-chip switched capacitor DC-DC converter in 32 nm SOI CMOS,” in *Proc. IEEE Appl. Power Electron. Conf.*, Mar. 2013.

[55] V. Ng, “Switched Capacitor DC-DC Converter: Superior where the Buck Converter has Dominated," Ph.D. dissertation, U.C. Berkeley, August 2011.

[56] J. F. Dickson, “On-chip high-voltage generation in NMOS integrated circuits using an improved voltage multiplier technique,” *IEEE J. Solid-State Circuits*, vol. 11, no. 6, pp. 374–378, Jun. 1976.

[57] R. J. Baker, *CMOS: Circuit Design, Layout, and Simulation*. John Wiley & Sons, 2011.

[58] M. D. Seeman and S. R. Sanders, “Analysis and optimization of switched-capacitor DC-DC converters,” *IEEE Trans. Power Electronics*, vol. 23, no. 2, pp. 841–851, Mar. 2008.

[59] E. Alberta, W. Hackenberger, C. Stringer, C. Randall, T. Shrout, and G. Schwarze, “High-Temperature Ceramic Capacitors,” in CartsConference, vol. 26, p. 141, Components Technology Institute Inc., 2006.

[60] R. J. Milliken, J. Silva-Martinez and E. Sanchez-Sinencio, "Full On-Chip CMOS Low-Dropout Voltage Regulator," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 9, pp. 1879-1890, Sept. 2007.

[61] Datasheet available online at: http://www.ti.com/lit/ds/snvs754k/snvs754k.pdf

[62] G. A. Rincon-Mora, “Current Efficient, Low Voltage, Low Drop-Out Regulators”, Ph.D. dissertation, Dept. Elect. Eng., Georgia Inst. of Technology, Atlanta, GA, Nov. 1996.

[63] Saxena, V., and Baker, R. J., “Indirect Feedback Compensation of CMOS Op-Amps,” in IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED), pp. 3-4, Apr. 2006.

[64] Y. L. Li, K. F. Han, X. Tan, N. Yan and H. Min, "Transconductance enhancement method for operational transconductance amplifiers," in *Electronics Letters*, vol. 46, no. 19, pp. 1321-1323, Sept. 16 2010.

[65] Q. Zhang, X. Zhao, X. Zhang, Q. Zhang, and X. Zhao, “Multipath recycling method for transconductance enhancement of folded cascade amplifier”, in *International Journal of Electronics and Communications* (2016).

[66] M. Ahmed, I. Shah, F. Tang and A. Bermak, "An improved recycling folded cascode amplifier with gain boosting and phase margin enhancement," *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, Lisbon, 2015, pp. 2473-2476.

[67] A. Rahman, A. M. Francis, S. Ahmed, S. K. Akula, J. Holmes and A. Mantooth, "High-Temperature Voltage and Current References in Silicon Carbide CMOS," in *IEEE Transactions on Electron Devices*, vol. 63, no. 6, pp. 2455-2461, June 2016.

[68] Datasheet available online at: http://www.ti.com/lit/ds/symlink/lmc660.pdf

[69] Datasheet available online at: http://www.ti.com/lit/ds/symlink/ua78l.pdf

[70] Datasheet available online at: http://www.ti.com/lit/ds/symlink/tps731.pdf

[71] G. A. Rincon-Mora, *Analog IC Design with Low-Dropout Regulators*. 2nd edition. McGraw-Hill, 2014.

[72] A. Rahman, L. Caley, S. Roy, N. Kuhns, A. Mantooth, J. Di, A. M. Francis, and J. Holmes, *IEEE Tranactions on Electron Devices*. vol. 64, no. 4, pp. 1426-1432, Apr. 2017.

APPENDIX A

A.1 Python Script #1: Automated Reliability Testing

```
# Linear Regulator - Automated Reliability Testing

# ----- Required Equipment List -----
# 1. Utilize a Tektronix MSO 4104 Mixed Signal Oscilloscope to capture the following:
#   (a) Input voltage
#   (b) Output Voltage (Mean)
#   (c) Output Voltage (High)
#   (d) Output Voltage (Low)
# 2. Utilize a Rigol DP832 Programmable DC Power Supply to provide the following:
#   (a) The supply voltage to the linear regulator
#   (b) The bias voltage of 4.5 V to the error amplifier.
#   (c) The reference voltage to the error amplifier of 7.5 V.
# ----- End of Required Equipment List -----

# ----- Test Plan -----
# 1. Connect the linear regulator to the PCB and set the output voltage to 15 V.
#   (a) Adjust the reference voltage to keep the output voltage fixed at 15 V.
#   (b) Record the reference voltage required to keep a 15 V output.
#   (c) Record the resistances of R_F1 and R_F2 (At 25C and 300 C)
#   (d) Taking into account the feedback resistances and the reference voltage, determine
the error amplifier offset.
# 2. Measure the mean of the input voltage.
# 3. Measure the high, low, and mean of the output voltage.
# ----- End of Test Plan -----

import sys
import os
import re
import datetime
from time import gmtime, strftime
from time import sleep, time

# The line below will allow for importing all instruments.
from instruments import *

#import utils.input as input

import logging
#import utils.log

import time
import string
```

```
import subprocess
import csv

def data_Write():
        # Writes the data to a .txt file.
        # Note: In the open(x, y) format, using an "a" in place of the "y" will append the data written. This is necessary for multiple tests.
        # In order to write to a file one time, simply use "w" in place of the "y".

   f = open('LinearRegulator_R' + str(reticleRow) + 'C' + str(reticleColumn) + '_TXT.txt', "a")
   f.write("----- The time is: " + str(current_Time) + " -----" + "\n" )
   f.write("The measurement # is: " + str(measurementNumber) + "\n" )
   f.write("Input voltage (mean): " + str(inputMean) + "\n" )
   f.write("Output voltage (mean): " + str(outputMean) + "\n" )
   f.write("Output voltage (high): " + str(outputHigh) + "\n")
   f.write("Output voltage (low): " + str(outputLow) + "\n")
   f.write("Reference voltage: " + str(referenceVoltage) +  "\n" )
   f.write("Input supply current: " + str(readCurrent1) +  "\n" + "\n")

   f.write("-------------------------------------------")
   f.write( "\n" + "\n" )
   f.close()

        # End of data writing.

def csv_Write():
        # Writes the data to a .csv file.
        # Note #1: In the "with open(x, y)" format, using an "ab" in place of the "y" will append the data written. On the contrary, using "wb" in place of the "y" will overwrite the file and not append new data.
        # In order to write to a file one time, simply use "wb" in place of the "y".

    with open('LinearRegulator_R' + str(reticleRow) + 'C' + str(reticleColumn) + '.csv', 'ab') as csvfile:
        wr = csv.writer(csvfile, delimiter=',')
        data_2 = [runNumber, str(measurementNumber), current_Time, str(inputMean), str(outputMean), str(outputHigh), str(outputLow), str(referenceVoltage), str(readCurrent1)]
        wr.writerow(data_2)

# Creates the .csv file to be used during the automation run
def csv_Create():
   with open('LinearRegulator_R' + str(reticleRow) + 'C' + str(reticleColumn) + '.csv', 'ab') as csvfile:
       wr = csv.writer(csvfile, delimiter=',')
```

```
        data_1 = ['Run Number', 'Measurement #', 'Time', 'Input Voltage (Mean)', 'Output Voltage (Mean)', 'Output Voltage (High)', 'Output Voltage (Low)', 'Reference Voltage', 'Input Supply Current']
        wr.writerow(data_1)

# ----- Configuring the instruments -----
#

# Configuring the Rigol DP832 DC power supply.
psu = PSU_RIGOL_DP832()
print('The power supply has been turned on.')
sleep(1)

# The first PSU output will be connected to the linear regulator supply voltage rail (VDD)
def psu_Output1_ON():
    psu.enable(1)
    supplyVoltage_Increment = 0
    while supplyVoltage_Increment <= supplyVoltage:
        psu.setVoltage(1, supplyVoltage_Increment)
        supplyVoltage_Increment = supplyVoltage_Increment + 1
        sleep(0.2)
    psu.enableOverCurrentProtection(1)
    psu.setCurrentLimit(1, 0.150)
    readCurrent1= psu.readCurrent(1)
    print('The current supplies by channel 1 is: ' + str(readCurrent1) + ' A')
    sleep(1)

# The second PSU output will be connected to the reference voltage (error amplifier)
def psu_Output2_ON():
    psu.enable(2)
    referenceVoltage_Increment = 0
    while referenceVoltage_Increment <= referenceVoltage:
        psu.setVoltage(2, referenceVoltage_Increment)
        referenceVoltage_Increment = referenceVoltage_Increment + 0.1
        sleep(0.05)
    psu.enableOverCurrentProtection(2)
    psu.setCurrentLimit(2, 0.005)
    readCurrent2 = psu.readCurrent(2)
    print('The current supplies by channel 2 is: ' + str(readCurrent2) + ' A')
    sleep(1)

# The third PSU output will be connected to the bias voltage (error amplifier)
def psu_Output3_ON():
    psu.enable(3)
    biasVoltage_Increment = 0
    while biasVoltage_Increment <= biasVoltage:
```

```
        psu.setVoltage(3, biasVoltage_Increment)
        biasVoltage_Increment = biasVoltage_Increment + 0.1
        sleep(0.05)
    psu.enableOverCurrentProtection(3)
    psu.setCurrentLimit(2, 0.005)
    readCurrent3 = psu.readCurrent(3)
    print('The current supplies by channel 3 is: ' + str(readCurrent3) + ' A')
    sleep(1)

print('The power supply has been configured.')

# Configuring the MSO 4104 oscilloscope.
scope = SCOPE_MSO4104()
print('The oscilloscope has been turned on.')
sleep(1)

# Set the oscilloscope time scale to 10 us. This allows for enough resolution to capture
potential oscillations.
scope.setTimePerDiv(0.00001)

# The first channel will read in the measurements (e.g. rise times, fall times, and duty cycle)
from the variable PWM.
scope.enableChannel(1)
scope.setVoltsPerDiv(1, 5)
scope.movePositionTo(1, -2)
scope.sync()
scope.configureMeasurement(1, "MEAN", 1)

# The second channel will read in the voltage of the reset pin from the FPGA.
# In addition, the scope will be set to trigger on 14.9 V of Channel 2.
scope.enableChannel(2)
scope.setVoltsPerDiv(2, 2)
scope.movePositionTo(2, -5)
scope.sync()
scope.configureMeasurement(2, "MEAN", 2)
scope.configureMeasurement(3, "HIGH", 2)
scope.configureMeasurement(4, "LOW", 2)

# Sets the oscilloscope to trigger at 14.9 V on Channel 2.
scope.setTriggerSource(2)
scope.setTriggerLevel(2, 14.9)

print('The oscilloscope has been configured.')
sleep(1)

# ----- End of Instrument Configuration -----
```

```
# Channel 1: Reads the input voltage.
# Channel 2: Reads the output voltage.

# Print out the row and column of the reticle being tested.
reticleRow = 5
reticleColumn = 2
print('The reticle being tested is SS02_R' + str(reticleRow) + 'C' + str(reticleColumn) + '.')

# Sets the Rigol DP832 output voltages.
supplyVoltage = 30
referenceVoltage = 4.5
biasVoltage = 4.5
psu_Output1_ON()
psu_Output2_ON()
psu_Output3_ON()

runNumber = 1                    # Denotes the run number (e.g. temperature number of temperature cycles)
measurementNumber = 1            # Denotes the measurement number within a single run.
timeScale = 0.00001              # Denotes the oscilloscope time scale used. Must be changed when taking PSRR measurements.
csv_Create()                     # Create the CSV file for the run.

scope.setTimePerDiv(0.00001)
psu.enable(1)
psu.setVoltage(1, 30)
sleep(1)
print('Starting the automated test script.')

# Start taking measurements with a supply voltage of 12 V, then repeat the measurements for a supply voltage of 15 V.
while 1:

    # Read in the input and output voltages from the oscilloscope.
    # Also read in the input current from the Rigol DP832 power supply.
    inputMean = scope.readMeasurement(1)
    outputMean = scope.readMeasurement(2)
    outputHigh = scope.readMeasurement(3)
    outputLow = scope.readMeasurement(4)
    readCurrent1= psu.readCurrent(1)
    current_Time = time.strftime('%X, %x')

    # Calibration of the reference voltage.
    while outputMean < 14.9:
        referenceVoltage = referenceVoltage + 0.01
```

```
        psu.setVoltage(2, referenceVoltage)
        sleep(0.1)
        outputMean = scope.readMeasurement(2)
        sleep(0.1)
    while outputMean > 15.1:
        referenceVoltage = referenceVoltage - 0.01
        psu.setVoltage(2, referenceVoltage)
        sleep(0.1)
        outputMean = scope.readMeasurement(2)
        sleep(0.1)

    #Print out the measurements to the console.
    print('----------------------------------------')
    print('----- Run #: ' + str(runNumber) + ' -----')
    print('The current time is: ' + str(current_Time))
    print('The current measurement number is: ' + str(measurementNumber))
    print('The input voltage (mean): ' + str(inputMean) + ' V')
    print('The output voltage (mean): ' + str(outputMean) + ' V')
    print('The output voltage (high): ' + str(outputHigh) + ' V')
    print('The output voltage (low): ' + str(outputLow) + ' V')
    print('The reference voltage is: ' + str(referenceVoltage) + ' V')
    print('The input supply current is: ' + str(readCurrent1) + ' A')
    print('-------------- End of Run --------------')

    data_Write()
    csv_Write()

    measurementNumber = measurementNumber + 1

    # Sleep for 5 minutes before taking another measurement.
    # A for() loop is implemented to allow for easily stopping the program.
    for i in range (0, 299):
        sleep(1)
    i = 0

# ----- End of automation script -----
```