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Spintronic device modeling and evaluation using modular approach to spintronics

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SPINTRONIC DEVICE MODELING AND EVALUATION USING MODULAR APPROACH TO SPINTRONICS

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A journey of self-growth that a pursuit of a Doctor of Philosophy affords takes one through episodes of self-doubt and occasional despair punctuated with exhilarating moments of revelations that are built on top of those very darker moments. Samiran Ganguly who entered the Graduate Program at Purdue a few years ago and the Samiran Ganguly who emerged from it are very different persons. The change is, hopefully, for good.

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ABBREVIATIONS

GMR	Giant Magneto-Resistance
TMR	Tunneling Magneto-Resistance
MTJ	Magnetic Tunnel Junction
IMA	In-plane Magnetic Anisotropy
PMA	Perpendicular Magnetic Anisotropy
LLG	Landau-Lifshitz-Gilbert Equation
STT	Spin-Transfer Torque
MRAM	Magnetic Random Access Memory
GSHE	Giant Spin-Hall Effect
ISHE	Inverse Spin-Hall Effect
RSO	Rashba Spin-Orbit Coupling
TI	Topological Insulator
YIG	Yttrium Iron Garnet
VCMA	Voltage Controlled Magnetic Anisotropy
ME	Magneto-Electric
MESH	Magneto-Electric and Spin-Hall
ST(N)O	Spin-Torque (Nano) Oscillator

ABSTRACT

Ganguly, Samiran Ph.D., Purdue University, December 2016. Spintronic Device Modeling And Evaluation Using Modular Approach to Spintronics. Major Professor: Supriyo Datta.

Spintronics technology finds itself in an exciting stage today. Riding on the backs of rapid growth and impressive advances in materials and phenomena, it has started to make headway in the memory industry as solid state magnetic memories (STT-MRAM) and is considered a possible candidate to replace the CMOS when its scaling reaches physical limits. It is necessary to bring all these advances together in a coherent fashion to explore and evaluate the potential of spintronic devices. This work creates a framework for this exploration and evaluation based on Modular Approach to Spintronics, which encapsulate the physics of transport of charge and spin through materials and the phenomenology of magnetic dynamics and interaction in benchmarked elemental modules. These modules can then be combined together to form spin-circuit models of complex spintronic devices and structures which can be simulated using SPICE like circuit simulators. In this work we demonstrate how Modular Approach to Spintronics can be used to build spin-circuit models of functional spintronic devices of all types: memory, logic, and oscillators. We then show how Modular Approach to Spintronics can help identify critical factors behind static and dynamic dissipation in spintronic devices and provide remedies by exploring the use of various alternative materials and phenomena. Lastly, we show the use of Modular Approach to Spintronics in exploring new paradigms of computing enabled by the inherent physics of spintronic devices. We hope that this work will encourage more research and experiments that will establish spintronics as a viable technology for continued advancement of electronics.

1. INTRODUCTION

Parts of this chapter are adapted from: Samiran Ganguly, Kerem Yunus Camsari, Supriyo Datta, "Evaluating Spintronic Devices Using The Modular Approach" [1]

Over the past three decades, the field of spintronics has grown from the realm of theoretical predictions [2–4] and cryogenic experiments [5–9] to commercially available memory and logic chips [10–12], made possible due to continued experimental breakthroughs that has effectively combined together the two distinct physical phenomena of spin-transport and magnetics. New materials and phenomena continue to be discovered at an impressive rate [13–22] and this has provided an ever-increasing toolbox for the design of novel functional spintronic devices [23–31] in a quest for the new transistor. It is natural to ask whether these developments can be harnessed to meet the increasing interest in finding new ways to meet the challenge of continuing the celebrated Moore‘s law in the coming decades.

Broadly speaking, from the perspective of a functional device design, the relevant developments in spintronic materials and phenomena belong in two categories, those that enable conversion of electrical information into magnetic information (the WRITE function) and those that enable the reverse process (the READ function). READ and WRITE functions are of course central to memory devices and it has also been shown that they can be integrated into a transistor-like device, with gain and input-output isolation, that we call a "spin switch" which can be used as a building block for logic circuits [24, 32].

1.1 Scientific Contribution, Scope and Significance of this Work

A natural question to ask is how such a spin switch compares with a standard switch based on CMOS (complementary metal oxide semiconductor) technology, and several authors have addressed different aspects of this question [33–36]. In this work we establish a systematic framework to evaluate the impact of different READ and WRITE units on the key performance criteria for logic devices, namely their static power dissipation (I^2R), switching energy (E), switching delay (τ), and the switching energy- switching delay product ($E \times \tau$) which is a well established metric for dynamic dissipation.

This framework is based on Modular Approach to Spintronics [37] and the accompanying open source Modular Spintronics Library [38] where different materials and phenomena are represented by experimentally benchmarked modules. The input and output voltages and currents of the terminals of these modules have four components, one for charge and three for spin (fig. 1.1 a). These modules can then be combined to build circuit models for devices and simulated using a SPICE-like software environment to evaluate circuit and system level performance.

In this work we first analyze a series of spin switches based on a magnetic tunnel junction (MTJ) for the reader and the spin Hall effect (SHE) for the writer providing a direct comparison of switching currents and power with a series of CMOS inverters (fig. 1.1 b). The purpose for this exercise is to pinpoint the factors underlying the inferior static power and energy-delay product of spin switches relative to a CMOS switch. Based on these findings we then evaluate a family of spin switches utilizing several alternative readers and writers (fig. 1.2 a) which show a potential improvement in performance that could perhaps make them comparable to CMOS.

Since Moore‘s law has been made possible by a doubling of the number of switches in a given area every two years, this cannot continue without a significant reduction in the energy-delay product relative to CMOS which seems difficult based on present state-of-the-art in spintronics. However, it has been noted that from a consumer

perspective, Moore's law represents a doubling of "user value" every two years and this could be enabled through enhanced functionality [39]. It has been recognized that nanomagnets could provide enhanced functionality over CMOS through their unique physics that provides a natural bistability, threshold response and stochastic operation.

We end with an evaluation of two types of logic using spin switches (fig. 1.2 b). One is a simple majority gate implementing standard Boolean logic, while the other is a simple version of a restricted Boltzmann machine featuring stochastic spin switches [40–44]. Such "stochastic computers" are commonly implemented virtually using software algorithms on a deterministic hardware platform, but nanomagnets could provide a natural physical hardware for their efficient implementation [45–47]. A detailed evaluation of different options and possibilities has not been attempted in this work. Our purpose here is simply to use Modular Approach to Spintronics to establish a common framework for connecting from basic materials and phenomena all the way to circuits and systems, both deterministic and stochastic.

1.2 Organization of this Work

The thesis is organized as per the following chapters:

Modular Approach to Spintronics

In this chapter we introduce Modular Approach to Spintronics and the accompanying open source Modular Spintronics Library that has been used throughout rest of this work. We briefly trace the origins of this approach from the very first works of spintronic modeling in terms of "2-Current Model" to Density Matrix based transport approaches developed from S-Matrix and NEGF theories, which were later transformed into a "4-Current Model" and then integrated with the Landau-Lifshitz-Gilbert Equation. This integration led to the establishment of Modular Approach to Spintronics, a multi-physics, multi-component circuit framework that seamlessly

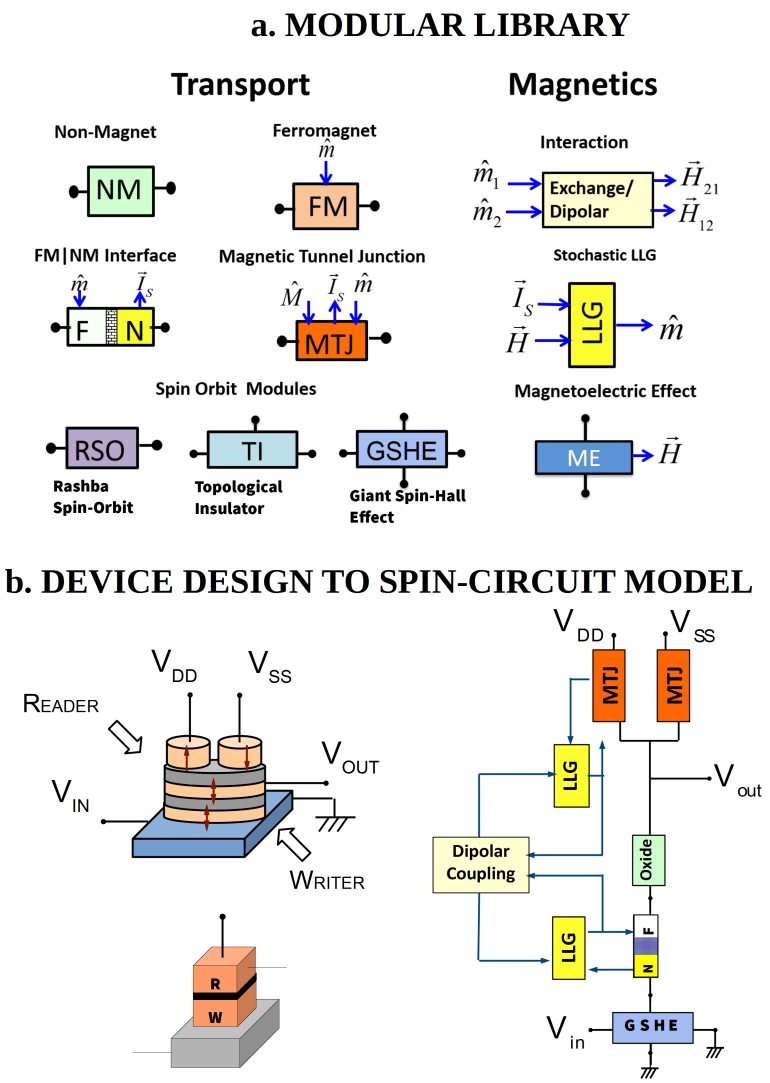


Fig. 1.1. **a. Modular Spintronic Library:** Benchmarked modules for charge and spin transport and magnetic phenomena that can be used to create spin-circuit models for spintronic devices. **b. Device Design to Spin-Circuit Model:** (top left): Spin switch, an example spintronic logic device. (bottom left): Compact representation of spin switches used throughout this work. (right): Spin-circuit models for a device can be built by connecting together various modules, using 4-component currents and voltages and simulated in SPICE like programs.

integrates the physics of transport of charge and spin in magnetic materials as well magnetic phenomena for a SPICE-like circuit simulation environment.

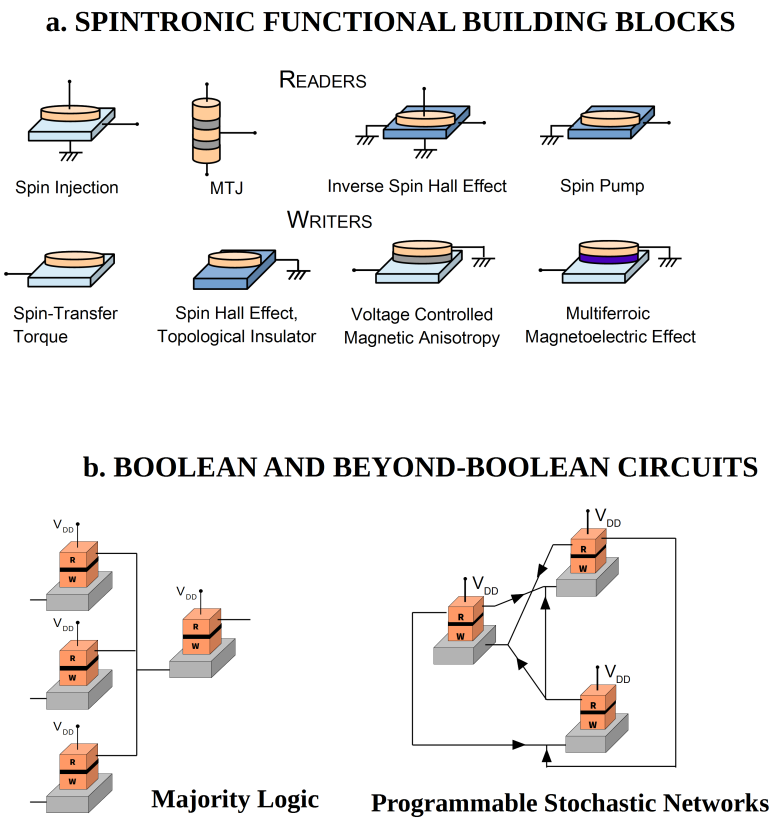


Fig. 1.2. **a. Spintronic Functional Building Blocks:** A sampling of various readers and writers that can be used to build spintronic devices. **b. Boolean and beyond-Boolean Circuits:** Spin-circuit models can be used to design and evaluate novel, ultra-compact, and efficient spintronic-based circuits and architectures.

We briefly describe the essentials of the Modular Spintronics Library including the modules which encapsulate transport physics in various materials or magnetic phenomena such as thin film magnet dynamics and interaction. Modular Approach to Spintronics and Modular Spintronics Library both have been covered in a previous work [48] in much more depth, therefore we refrain from going in the details of the modules, though in the appendix we provide the analytical expressions for the physics of the modules.

Spintronic Device Modeling Using Modular Approach to Spintronics

In this chapter we demonstrate the use of the Modular Spintronic Library in creating spin-circuit models of functional spintronic devices.

We first create spin-circuit models for Giant Spin-Hall Effect (GSHE) and Voltage-Controlled Magnetic Anisotropy effect (VCMA) assisted Perpendicular Magnetic Anisotropy (PMA) Magnetic Tunnel Junction (MTJs) intended to be used in the Spin-Transfer Torque Magnetic RAM (STT-MRAM) cells. Using the spin-circuit models we study the efficacy of the assisting mechanisms in reducing the drive current density required as well as the effect on the switching energy $\times$ switching delay product per switching event ($E \times \tau$) for the write process of these cells.

We then create spin-circuit model for the proposed Spin Switch (also known as the *CSL* device). Using the spin-circuit model we extract the device characteristics, which show that the device works as an inverter with built-in 1 bit memory. We then demonstrate its use in building the fundamental logic gates *AND* and *OR*.

Finally, we create a spin-circuit model for a proposed spintronic oscillator known as the MESH nano-oscillator which integrates the physics of Giant Spin-Hall Effect, Magneto-Electric Effect, and Magnetic Tunnel Junctions to form a high performance spintronic oscillator. Using the spin-circuit model of the oscillator device, we study the physics of the oscillator, extract its characteristics and frequency response. We then further demonstrate injection-locking in the oscillator along with its ability to reduce the phase noise in the oscillator.

The overall aim of this chapter is to demonstrate the use and power of Modular Approach to Spintronics in modeling, and exploring device and circuit design for spintronic devices, in a wide variety of applications: memory, logic, oscillators.

Dissipation: Spin Switch vs. CMOS

In this chapter using a detailed spin-circuit model we delve into the details of dissipation of the spin switch working as a logic device. We compare and contrast the physics behind dissipation in spin switch with a contemporary CMOS design. We look at both static (I^2R) as well as dynamic ($E \times \tau$) dissipation in both the spin

switch and CMOS inverters and relate them to the physical properties of the devices, opening a pathway to more optimal design.

The aim of this chapter is to establish a framework for performance analysis of spintronic devices using Modular Approach to Spintronics and establish it as tool for in-depth engineering analysis.

Alternative Spin Switch Designs

In this chapter using Modular Approach to Spintronics we explore various alternative designs of the spin switch which incrementally enhance the dissipative performance of the device through the use of material and design enhancements. Using Modular Approach to Spintronics we demonstrate that the performance of the spin switch can be improved considerably and approach the performance of a CMOS logic switch.

Complex Boolean and Beyond-Boolean Circuits Using Spin Switch

In this chapter we explore the advantages of spintronic devices in general, and spin switch in particular, in implementing complex Boolean and beyond-Boolean circuits efficiently due to its inherent physics.

We explore the use of building logic circuits using the $\{MAJ, NOT\}$ basis, a natural consequence of spintronic device physics, which can provide alternatives to the more common $\{AND, NOT\}$ and $\{OR, NOT\}$ basis set which are suited for CMOS based logic. We show that using an ME based spin switch, the dissipative performance of such a gate can be similar to CMOS.

We further explore the use of superparamagnetic spin switches to build hardware probabilistic logic circuits which may have applications in implementing deep belief networks and machine learning. These circuits may replace the present software based solutions for these increasingly important computing applications.

Conclusion and the Future

In this chapter we reflect back on our work. We present an executive summary of the work and the grounds that have been covered. We close the chapter, and the work with a glance on what future may hold for spintronics.

Appendices

In the appendices we have covered the analytical device equations for the family of the spin switch devices, analytical estimates for operating points of these devices, equations for assisted writing for PMA MTJs, a brief presentation of the modules in the Modular Spintronics Library, software codes for the spin switch family, and finally a material parameter table/database used in this work.

1.3 Journal Publications and Conference Presentations pertaining to this Work

- Samiran Ganguly, Kerem Yunus Camsari, Supriyo Datta, "Evaluating Spintronic Devices Using The Modular Approach", In Review.
- K. Y. Camsari, S. Ganguly, and S. Datta, "Modular Approach to Spintronics," Scientific Reports, vol. 5, p. 10571, June 2015.
- S. Ganguly, M. M. Torunbalci, S. A. Bhave, and K. Y. Camsari, "MESH Nano-Oscillator: An All Electrical Doubly Tunable Spintronic Oscillator," in Device Research Conference (DRC), 2016 74th Annual, IEEE, 2016.
- Kerem Y. Camsari, Samiran Ganguly, Deepanjan Datta, "A Modular Spin-Circuit Model for Magnetic Tunnel Junctions", in Device Research Conference (DRC), 2016 74th Annual, IEEE, 2016.
- Samiran Ganguly, Zeeshan A. Pervaiz, Kerem Y. Camsari, Supriyo Datta, Ernesto E. Marinero, "Comparative Analysis of Assisted Writing Mechanisms in PMA Magnetic Tunnel Junctions", APS March Meeting 2015.
- K. Y. Camsari, S. Ganguly, D. Datta, and S. Datta, "Physics based factorization of Magnetic Tunnel Junctions for modeling and circuit simulations," in Proceedings of IEDM, 2014.

- Samiran Ganguly, Kerem Y. Camsari, Supriyo Datta, "LibSpin: A Verilog-A/SPICE Library for Spintronics", TECHCON, 2014.

- Samiran Ganguly, Kerem Y. Camsari, Deepanjan Datta, "Spin Currents in Magnetic Tunnel Junctions (MTJ) Devices: From Quantum to Compact Model", International French-US Workshop Towards Low Power Spintronic Devices, 2013.

2. MODULAR APPROACH TO SPINTRONICS

In this chapter we describe our multi-physics framework for modeling of spintronic devices and structures. We briefly describe the theoretical underpinning of our approach, namely, the multi-component spin-circuit formalism. Then we describe Modular Spintronics Library based on this formalism which consists of theoretically and experimentally benchmarked modules that incorporate the physics of charge and spin transport through various materials and magnetic structures, as well as dynamics and interaction of nano-magnets. These modules can be used to build together circuit models for spintronic devices of arbitrary complexity and simulated in a SPICE-like circuit solver.

Modular Approach to Spintronics has been developed over the work of various authors that incrementally laid the theoretical foundation, proved its utility as a useful tool for analysis, and then expanded its scope as a general framework for modeling and evaluation of spintronic devices. The purpose of this chapter is to provide an overview of the approach and the accompanying Modular Spintronics Library. For more details on the Modular Spintronics Library and illustrative examples of devices and structures that can be modeled, please visit the website of the project portal and repository [49].

2.1 4-Component Spin-Circuit Formalism

Genesis of the multi-component spin-circuit formalism can be traced back to the *2-Current Model* [50] for the analysis of the Current-Perpendicular-to-Plane Giant Magneto-Resistance (CPP GMR) devices in the *collinear* configuration, wherein the two contact magnets are either parallel or anti-parallel to each other. This was later extended [51] to incorporate *non-collinear* transport in terms of density ma-

trix theory. This expanded approach was later adapted for electrical circuit analysis methods [52] by relating the non-equilibrium density matrix to the electro-chemical potentials and quasi-Fermi levels for the charge and spins explicitly by defining a *4-Current model* and integrated with the Landau-Lifshitz-Gilbert Equation to incorporate time-dependent magneto-dynamics. This approach was shown then to be amenable for SPICE-like circuit analysis [53] and then formalized as **Modular Approach to Spintronics** [37], along with the open source Modular Spintronics Library [38], and example circuit models built using the Modular Spintronics Library in the accompanying project portal [49]. Ever since this approach has been used widely by the spintronics community for modeling and analysis of myriad spintronic devices (see e.g. [28, 54]).

At the heart of Modular Approach to Spintronics lies *4-component currents and voltages* and conductance matrices relating them. In Modular Approach to Spintronics, the spin currents and voltages are explicit terminal quantities along with the usual charge currents and voltages, therefore a spin-circuit is composed of circuit elements (*modules*) whose terminal voltages and currents are 4-component vectors (standing for charge along with the three component of the spins: x, y, z) rather than pure scalars (charge only) as it is in the traditional electrical circuits. Explicit accounting for spin currents and voltages at the terminals allows for concatenating these modules together to model complex geometries and materials, even though individual modules may use completely different theoretical approaches for modeling the transport of charge and spins through them. This further allows for creating magnetics modules that model magnetic interaction and dynamics to be used in conjunction with the transport modules. The magnetics modules use 3-component terminals which represent magnetic fields and magnetization vectors rather than currents and voltages. For further details we invite the reader to [37, 48, 49] and the appendix of this work.

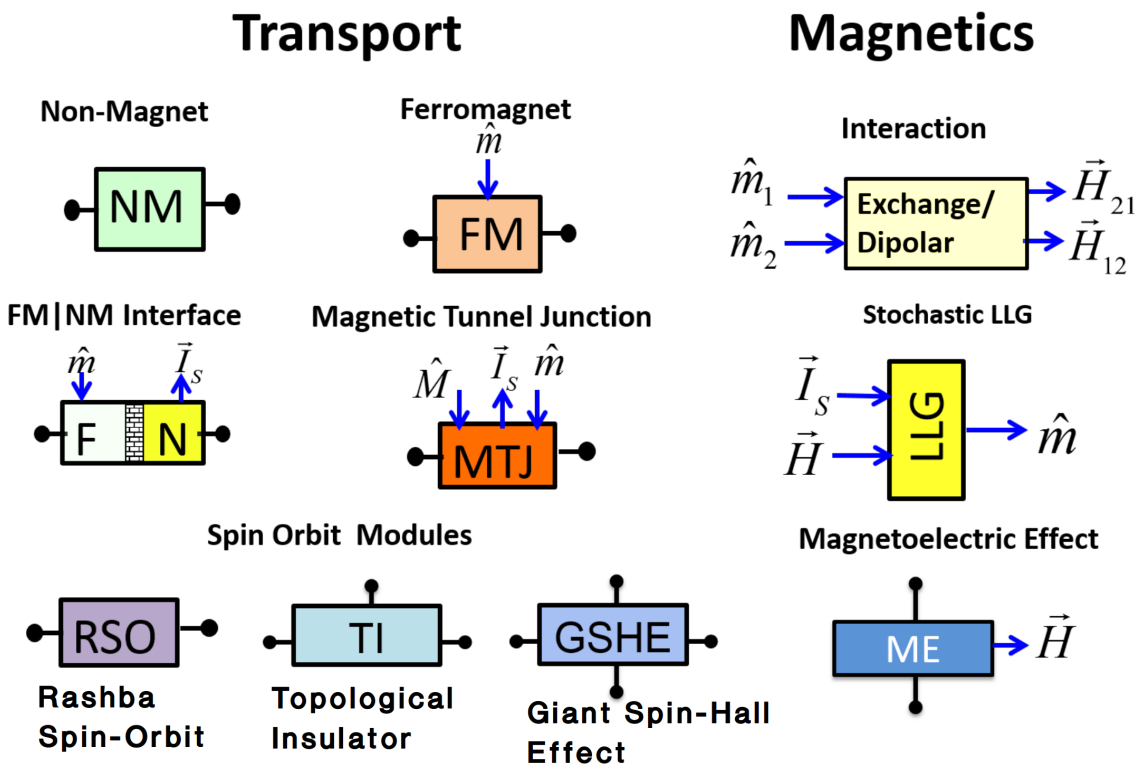


Fig. 2.1. **Modular Spintronics Library:** Modular Spintronics Library broadly consists of two types of modules: (a) *Transport Modules* which model transport properties of charge and spin through various materials. These modules are based on different physical theories such as spin-diffusion equation, S-matrix theory or NEGF based coherent transport. (b) *Magnetic Modules* which model dynamics of nano-magnets using LLG equation, their mutual interaction using dipolar and exchange coupling as well multiferroic phenomena such as magnet-electric effect

2.2 Modular Spintronics Library

Modular Spintronics Library (fig. 2.1) consists of state-of-the-art experimentally and theoretically benchmarked modules that encapsulate the 4-component spin-circuit formulations of transport through various materials and interaction and dynamics of nano-magnets. The terminal quantities of these modules are charge and spin currents and voltages, as well other non-electrical quantities such as magnetization, mag-

netic fields, and spin-torque currents expressed as 3-component voltages and currents. These modules can be connected together to build circuit models of spintronic devices and structures and simulate them in a SPICE-like circuit program. The collection of the modules and their usage in building spin-circuit models as well as analysis of performance is documented extensively in the online project repository [49] where new models are released and old ones updated.

2.2.1 Transport Modules

The transport modules cover charge and spin transport through various materials. All the terminals are 4-component (1 for charge and 3 for spin) unless specified otherwise. Connected together, these modules capture charge and spin transport through a large variety of structures, both homogeneous as well as heterogeneous. The modules, at present, in the Modular Spintronics Library are:

Normal−Metal (NM)

This module captures the transport of charge and spin-currents through a non-magnetic material, such as metals like Cu, Au etc. or semiconductors such as Si, graphene etc. The module is based on the 4-component charge and spin diffusion theory and accounts for spin randomization and decay during transport through the material.

Ferromagnet (FM)

This module captures the transport of charge and spin-currents through a ferromagnetic material, such as $\mathrm{NiFe}, \mathrm{CoFeB}$ etc. The module is based on the 4-component charge and spin diffusion theory and accounts for bulk spin polarization, bulk transverse and longitudinal spin decay, and magneto-resistance.

NM−FM Interface (NM−FM)

This module captures the transport of charge and spin-currents through the interface of the NM and FM materials. The module is developed from NEGF based coherent transport formalism of charge and spin through the interface. This module accounts for interface spin polarization, interface charge and longitudinal resistance, magneto-resistance, and transverse spin-torque currents on the FM material. This module can be connected with the LLG Solver module to obtain dynamics of the FM due to spin-current injection from the NM, as well as spin-pumping into the NM layer due to precession of the FM.

Magnetic Tunnel Junction (MTJ)

This module captures the transport of charge and spin-currents through a magnetic tunnel junction. The module is based on NEGF based coherent transport theory [55] since an MTJ cannot be broken down into individual FM and NM modules using traditional circuit theory as explained in [56]. This module accounts for charge resistance of the MTJ, including tunneling magneto-resistance, and spin-torque currents on the free layer which can be coupled with an LLG module to obtain a fully working MTJ model.

Rashba Spin-Orbit (RSO)

This module captures the transport of charge and spin-currents through a material with Rashba Spin-Orbit coupling such as GaAs modeled using a NEGF based coherent transport theory. This module accounts for charge and longitudinal spin resistance, transverse spin rotation and decay, and spin polarization due to RSO effect.

Giant Spin-Hall Effect (GSHE)

This module captures the transport of charge and spin-currents through a material with giant spin-Hall effect such as Pt, CuBi, Ta, W etc. which has been modeled using a 4-component charge and spin diffusion theory. This module accounts for both spin-Hall and inverse spin-Hall effects, and spin decay due to strong Rashba spin-orbit coupling in the Heavy Metal (HM).

Topological Insulator (TI)

This module captures the transport of charge and spin-currents through a material with TI surface states such as $Bi_2Se_3, Bi_2Te_3, HgTe$ etc. and is modeled using a 4-component charge and spin diffusion theory. This module accounts for spin polarized current due to spin-Hall effect as well as inverse spin-Hall effect.

2.2.2 Magnetics Modules

The magnetic modules cover the interaction and dynamics of nano-magnets and magnetic materials. These modules interact with other magnetic and transport modules through 3-component nodes which represent various physical quantities such as magnetization, magnetic field, and spin-torque current. The modules, at present, in the Modular Spintronics Library are:

Landau-Lifshitz-Gilbert Solver (LLG)

This module captures the dynamics of nano-magnets in a monodomain approximation using the Landau-Lifshitz-Gilbert equation. The module accepts magnetic field and spin-torque current as its inputs and generates the magnetization vector as a function of time. The two variations of the module are noted below.

Stochastic LLG

This module extends the basic LLG module to include the effect of thermal noise on the dynamics of the nano-magnet.

Voltage Controlled Magnetic Anisotropy (VCMA-LLG)

This module extends the basic LLG module to include the effect of voltage-controlled magnetic anisotropy effect on the dynamics of the nano-magnet. It can be used for noisy VCMA+LLG simulations as well.

Magnetic Coupling (Coup)

These modules models the magnetic interaction between two nano-magnets. The two versions of the modules capture the two different magnetic interactions, dipolar coupling, and exchange interaction coupling. The magnets are assumed to be monodomain.

Dipolar Coupling

This module models the dipolar coupling field between two nano-magnets. The inputs to the model are the magnetization vectors of the two nano-magnets and the output are the magnetic fields on the two nano-magnets due to each other.

Exchange Coupling

This module models the coupling between two nano-magnets due to exchange interaction as magnetic fields. The inputs to the model are the magnetization vectors of the two nano-magnets and the output are the magnetic fields on the two nano-magnets due to each other.

Magneto-Electric (ME)

The module captures the magnetic field applied on an FM layer due to the magneto-electric effect of a multi-ferroic material, such as $BiFeO_3$ and when coupled with an LLG module produces the switching characteristics due to the ME effect.

2.3 Summary

In this chapter we took a bird's eye view of Modular Approach to Spintronics and its theoretical underpinnings. We briefly reviewed the 4-component Spin-Circuit formalism and its development, and the Modular Spintronics Library based on it. We describe the various transport and magnetic modules available in the Modular Spintronics Library that can be used to model spintronic structures and devices.

The next chapter illustrates the use of these modules in building spin-circuit models of spintronic devices using three examples: (a) Write Assisted PMA MTJ, which are building blocks for STT-MRAM bit cells, (b) Spin switch, which is a logic device, and (c) MESH oscillator, which is a spintronic oscillator.

3. SPINTRONIC DEVICE MODELING USING MODULAR APPROACH TO SPINTRONICS

Parts of this chapter are adapted from: Samiran Ganguly, Mustafa M. Torunbalci, Sunil A. Bhave, Kerem Y. Camsari, "MESH Oscillator: All Electrical Doubly Tunable Spintronic Oscillator", Proceedings of the 74th Annual Device Research Conference (DRC). [57] and from Samiran Ganguly, Zeeshan A. Pervaiz, Kerem Y. Camsari, Supriyo Datta, Ernesto E. Marinero, "Comparative Analysis of Assisted Writing Mechanisms in PMA Magnetic Tunnel Junctions", APS March Meeting 2015. [58]

In this chapter we demonstrate the use of Modular Approach to Spintronics in modeling and simulation of spintronic devices. While a large number of spintronic devices have been proposed in the past decade, as we have listed in the introduction chapter, we choose three classes of device in particular as examples here.

The first device we choose is a write assisted PMA Magnetic Tunnel Junction that can be used to build a 1-bit non-volatile memory cell (STT-MRAM). The second device is a logic device called the spin switch, also known as the CSL (charge-spin logic) device, which demonstrates how a spintronic logic devices with built-in gain and directivity can be built as a combination of WRITER and a READER sub-units we mentioned in chapter 1. The final device is a spintronic oscillator based on combination of Magneto-Electric Effect and Giant Spin-Hall Effect that provides materials based solutions for longstanding engineering problems associated with these oscillators.

This chapter does not go into the detailed physics of the devices, rather our purpose here is to illustrate the use of Modular Approach to Spintronics in building spin-circuit models of spintronic devices and simulating them with SPICE to obtain device characteristics and explore their use in example circuits.

All the device models and simulation codes are provided in the appendix and shall be available for free download eventually from Modular Approach to Spintronics portal and the project repository at [49].

3.1 Write Assisted PMA Magnetic Tunnel Junctions for STT-MRAM cells

Discovery of the spin-torque effect in 1996 [3, 4] raised the possibility of building solid state integrated magnetic memories that can work at GHz speeds and maintain compatibility with the existing CMOS circuits and process flow. Since the first experimental demonstration of the STT writing in MTJs, in just over a decade STT-MRAMs have reached the stage of commercialization as a niche non-volatile memory (NVRAM) for the embedded and enterprise markets.

To improve the efficiency of the spin-torque writing in the present "3rd generation" STT-MRAM bit cells employing PMA MTJs, various write assistance mechanisms can be incorporated. These mechanisms provide an additional torque that enables a smaller amount of spin-torque current from the fixed polarizer magnetic layer of the MTJ (write current from the self-polarization) for switching. This reduction of the required spin-torque can improve the reliability and lifetime of the device by reducing the write-current densities necessary for the operation of the bit cell.

While a wide variety of assisted mechanisms can be considered, in this chapter we look at Giant Spin-Hall Effect (GSHE) and Voltage Controlled Magnetic Anisotropy (VCMA) as two example mechanisms. A few other possible mechanisms are thermal assistance, strain assistance, and magneto-electric assistance.

Fig. 3.1 a shows the schematic of GSHE assisted PMA MTJs and its spin-circuit model and fig. 3.1 b shows the schematic of VCMA assisted PMA MTJs and its spin-circuit model built using the modules in the Modular Spintronics Library. Other assist mechanisms such as thermal, magneto-electric, and strain can be similarly modeled by incorporating appropriate modules from the Modular Spintronics Library.

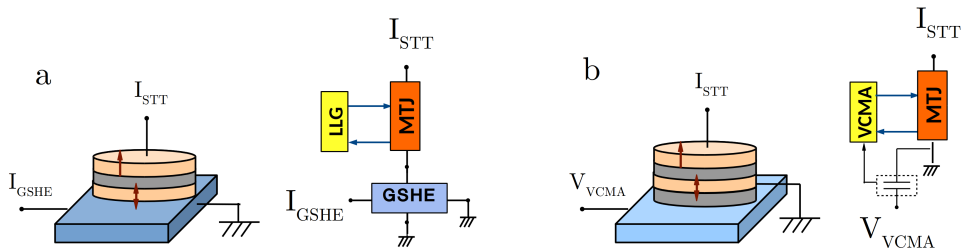


Fig. 3.1. **a. GSHE assisted PMA MTJ:** Schematic and the spin-circuit model [59] of the GSHE assisted PMA MTJ for STT-MRAM bit cells. The spin-circuit is built using the MTJ, GSHE, and the LLG modules. **b. VCMA assisted PMA MTJ:** Schematic and the spin-circuit model of the VCMA assisted PMA MTJ STT-MRAM bit cells. The spin-circuit is built using the MTJ, a capacitor to model the oxide and its electric field, and the VCMA-LLG modules.

3.1.1 Scaling Issues of PMA MTJ STT-MRAM bit cells

For a non-volatile memory cell a critical measure of performance is the state retention time, i.e. the expected timeframe for which the cell will retain its state without any external intervention. For a uniaxial PMA magnet this is given by the Arrhenius rleation: $\tau_r = \tau_0 e^{U/k_B T}$ where $2U = M_s \Omega H_k$ is the barrier height separating the two energy minima states of the magnet, τ_r is the expected retention time and τ_0 is the average time for a $U = 0\ k_B T$ magnet to flip, and is experimentally determined to be about $0.1 - 1\ ns$ [60]. Assuming $\tau_0 \approx 1\ ns$, it can be shown that a $U = 40\ k_B T$ magnet has a state retention time of nearly a decade and is the preferred minimum energy barrier for NVRAM bit cell designs.

For a Magnetic Tunnel Junction with Perpendicular Magnetic Anisotropy (PMA) the minimum spin current necessary to switch is given by $I_{stt} = 4q\alpha U/\hbar$ [61], that is only dependent on the barrier height U and the Gilbert damping factor α which is typically ~ 0.1 for highly scaled PMA magnets. Therefore, for a $U = 40\ k_B T$ magnet, the minimum spin-current necessary to switch the magnet $I_{stt;crit.} \approx 100\ \mu A$.

This calculation shows that as the STT-MRAM bit cells scale down, a major challenge will be to address the current density scaling up $\propto d^2$, where d is the diameter of the magnet. As an example, for a $d = 100\ nm$ MTJ pillar the $\overrightarrow{J}_{stt} = 1.2\ MA/cm^2$ whereas for $d = 20\ nm$ pillar it will be $\overrightarrow{J}_{stt} = 30\ MA/cm^2$. Write assist mechanisms can help reduce this high write-current density by providing an additional torque mechanism.

3.1.2 Effectiveness of the Write Assist Mechanisms

We can use our spin-circuit models to study the efficacy of the write assist mechanisms. While there are multiple ways to quantify the efficacy of the write mechanisms, in this short demonstration we only explore how much do these write mechanisms help in reducing the spin-torque write-current densities.

GSHE assisted Writing

In our simulation, we apply a simultaneous square pulse train of 0.5 ns of both GSHE and the spin-torque currents after which the GSHE current pulse is stopped and the write pulse is applied for a further 0.5 ns (pulse type 1 in fig. 3.2 a). There is nothing special about the choice of these particular pulse timings and have been chosen for purely demonstration purposes. Fig. 3.2 b,c show the switching phase diagram for a $d = 100\ nm$ and $d = 20\ nm$ MTJ pillars with both having $U = 40\ k_BT$ barrier height.

It can be seen that in the larger MTJ, the GSHE can substantially help in reducing the current density. In fact as the GSHE current density is increased, the lower the write current density gets. This is understandable as the GSHE helps bring the MTJ in the hard-axis in-plane direction, from which only a minimal push is necessary to let the magnet switch in the desired direction. Also, at $\overrightarrow{J}_{stt} = 0$, the magnet fails to switch due to the absence of this push and stays in the hard-axis direction due to the GSHE current. However, for the scaled down magnet, this assistance is minimal

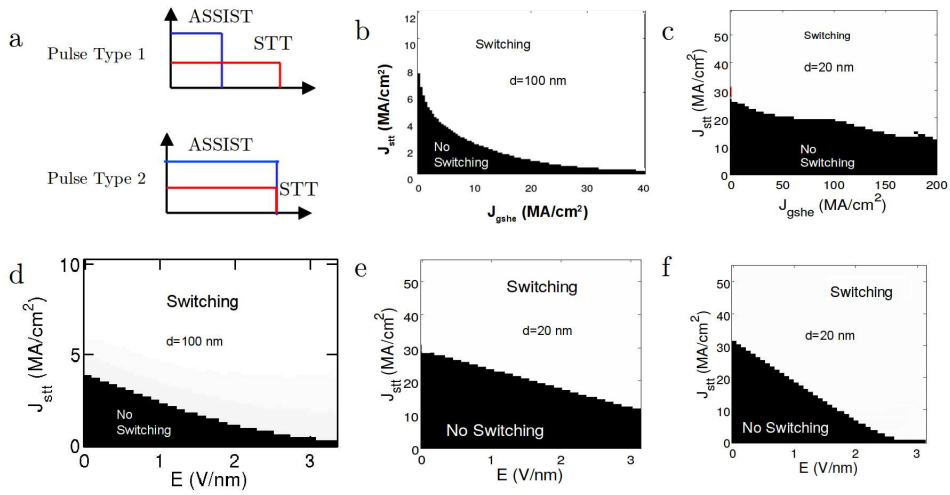


Fig. 3.2. **a. Two types of pulses applied for writing:** Pulse type 1 is a simultaneous application of assist and write pulses for 0.5 ns and then a write only pulse for a further 0.5 ns. Type 2 is a simultaneous pulse application of both assist and write for the full 1 ns. **b.** Switching phase diagram for GSHE assisted writing for $d = 100$ nm MTJ with a pulse type 1. **c.** Switching phase diagram for GSHE assisted writing for $d = 20$ nm MTJ with a pulse type 1. **d.** Switching phase diagram for VCMA assisted writing for $d = 100$ nm MTJ with a pulse type 1. **e.** Switching phase diagram for VCMA assisted writing for $d = 20$ nm MTJ with a pulse type 1. **f.** Switching phase diagram for VCMA assisted writing for $d = 20$ nm MTJ with a pulse type 2.

because the geometrical gain due to the GSHE ($\theta_{sh}L/t(1 - sech(t/\lambda_s))$ is reduced substantially due to reduction in L (which reduces hand-in-hand with the reduction in d of the magnet) for the same amount of current pumped in, as evidenced from the switching phase diagram.

We conclude that while GSHE based assistance can help substantially in write assistance to reduce the write current densities, the magnitude of the assistance will be much smaller for aggressively scaled bit cells.

VCMA assisted Writing

VCMA effect [20] provides write assistance by reducing the anisotropy field strength H_k, thereby reducing the U and lowering the write current magnitude. We apply two types of pulses: (a) a staggered pulse scheme with the assist pulse applied for half the duration of write pulse, and (b) assist pulse applied continuously throughout the duration of the write pulse of 1 ns (pulse type 1 and 2 respectively in fig. 3.2 a).

Fig. 3.2 d,e show the switching phase diagram with a pulse type 1 for a $d = 100\ nm$ and $d = 20\ nm$ MTJ pillars with both having $U = 40\ k_BT$ initial barrier height. Fig. 3.2 f shows the switching phase diagram for pulse type 2. The VCMA effect scales down with a decrease in the area and for a magnet with area $A = 1\ nm^2$, electric field $E = 1\ V/nm$, and $\eta = 1\ \frac{\mu J/m^2}{V/nm}$ reduces the barrier height by $\Delta U = 2.4 \times 10^{-4}\ k_BT$ at room temperature. Therefore for a $d = 20\ nm$ and $\eta = 200$ the electric field necessary to reduce the barrier height to 0 is about $E \approx 2.7\ V/nm$ which needs to be applied continuously. However for a larger magnet with $d = 100\ nm$, a shorter VCMA pulse duration is sufficient as seen in fig 3.2 d.

We conclude that VCMA based assistance can help in reducing the write-current densities substantially for larger bit cells, however the magnitude of the assistance will be smaller for scaled bit cells due to scaling down of the effect with the area reduction. This can be countered with longer assist pulse durations, which is at the cost of lower lifetime of the oxide layer caused by the high field dielectric breakdown accelerated by longer pulses.

The purpose of modeling these device and study of the effectiveness of the write assist mechanisms was to demonstrate the power of Modular Approach to Spintronics in performing analyses of practical importance. In later chapters we show in details how Modular Approach to Spintronics enables detailed analysis of static and dynamic dissipation in spintronic devices as well as provides a platform for exploration of various material, design, and circuit based solutions to reduce dissipation in spintronic devices.

3.2 Spin Switch

Spin switch was originally proposed as a logic device [24] with built-in gain and electrical isolation, useful for building large scale logic circuits without repeaters, buffers or amplifiers. In the spin switch the WRITER is composed of a GSHE layer applying spin-torque to an adjacent free FM layer and an complementary dual MTJ pairs as the READER. These two units are connected magnetically through dipolar coupling. The gain in the device is obtained due to the geometrical gain of charge-to-spin current in the GSHE [62], while the dipolar coupling through an electrical oxide provides the electrical isolation. A schematic of the device is shown in fig. 3.3 a

Using the modules from the Modular Spintronics Library, we can build a spin-circuit model of the spin switch as shown in fig. 3.3 b. Looking at the circuit model, it is evident that Modular Approach to Spintronics allows us to build a family of spin switches by using different materials to design alternative combinations of WRITERs and READERs, which was first recognized in [32]. In chapter 5 we illustrate a few of these possible alternatives in our search for a higher performance spin switch.

3.2.1 Device Characteristics

The circuit model can be used to obtain the device characteristics of the spin switch. A transient simulation with a sweep of the input current (with a sweep time $\gg$ the switching time of the spin switch) produces one half of the characteristic curve in fig. 3.3 c, whereas a sweep in the reverse direction produces the second half of the plot. Both the sweep directions are as indicated by the arrows. The full characteristic shows hysteresis, which is expected from a magnetic device. In addition, the device shows inverted signal, as well as gain, meaning the output current levels can be higher than the required minimum input current levels to operate the device, without degrading the expected functionality of the device. This shows that the device works as an inverter with built in memory and gain, which means it can have a fan-out of

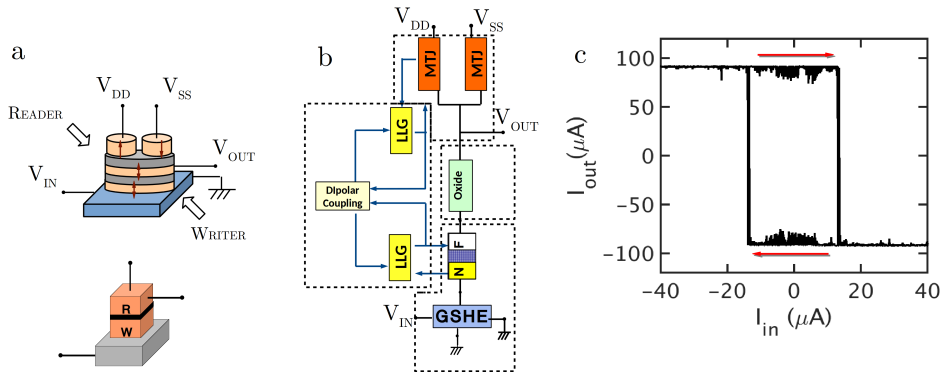
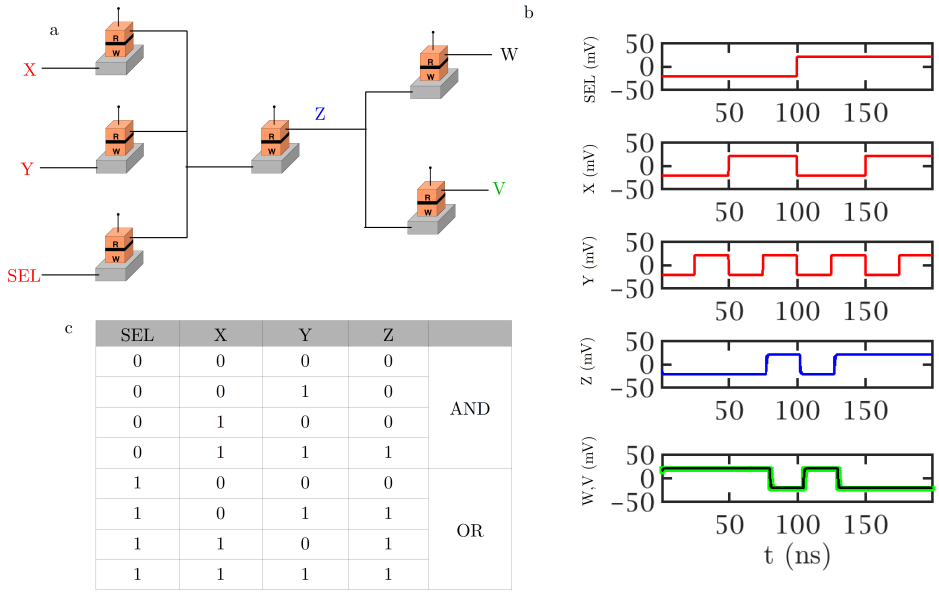


Fig. 3.3. **a. Spin switch schematic:** Device structure of the spin switch. The WRITER is built using a GSHE driving an FM using the spin-torque. The READER is a complementary dual MTJ pair whose two pillars act as pull-up and pull-down resistors, depending on the state of the free layer. The free layer of the MTJ is coupled magnetically to the WRITER FM. **b. Spin-circuit model:** Circuit model of the spin switch built using the modules from the Modular Spintronics Library. The modular principle allows us to explore other combinations of materials and designs for readers and writers by swapping out the modules as needed. **a. Device characteristics:** The device characteristics of the spin switch. An input sweep of the signal produces an output response which is inverted and hysteretic in nature, due to the non-volatility of the magnet. The device therefore acts as an inverter with built-in memory.

more than one, a necessary feature to be used in logic circuits without repeaters or amplifiers.

3.2.2 Logic Circuits Using Spin Switch

Spintronic devices like spin switch are current driven threshold devices, i.e. when the total current at the input exceeds a certain critical threshold they switch due to spin-torque action. Spin switch can naturally act as majority gate device since the switching current can be provided from a multitude of other spin switches whose output currents all add up naturally in the interconnect leading into the input terminal of the spin switch. Majority gate formed by the spin switch can be converted into



SEL	X	Y	Z	
0	0	0	0	AND
0	0	1	0	
0	1	0	0	
0	1	1	1	
1	0	0	0	OR
1	0	1	1	
1	1	0	1	
1	1	1	1	

Fig. 3.4. **a. Universal logic gates using the spin switch:** A three input majority logic function implemented using the spin switch. This circuit can be dynamically reconfigured as an AND or an OR function of two inputs (X and Y) using the control input (SEL). The output (Z) can drive multiple devices at the next stage of the pipeline. **b. Transient simulation of the circuit:** A transient simulation showing the working of the circuit as an AND and an OR gate. The last stage shows the spin switch with fan-out of 2 without any amplifiers or repeaters. **c: Truth Table for the Logic Gate:** The truth table of the Z as a function of X, Y. The SEL reconfigures the gate to either function as an AND or an OR gate.

a dynamically reconfigurable basic gates of Boolean logic, i.e. AND and OR gates. In chapter 6 we discuss more on building circuits using the majority gate and its connection to the physics of spin switches.

Fig. 3.4 a shows a 3-input gate that can be converted to a 2-input AND or OR gate by appropriately choosing one of the inputs as the *SEL* signal as shown in the simulation (fig. 3.3 b). It can be seen that the truth table followed by the 4 gates (associated with the signals SEL, X, Y, Z) is as shown in fig. 3.4 c. It can be seen that the *SEL* signal can configure the same circuit into an AND or an OR gate. We

can further see from fig. 3.3 b that the spin switch can drive multiple devices at its output (fan-out) without any amplifier or repeater which is important for any logic device to work as a CMOS replacement.

3.3 MESH Oscillator

Our third illustrative application of Modular Approach to Spintronics is a spintronic oscillator (STO) based on a combination of the Magneto-Electric Effect (ME), Giant Spin-Hall Effect (GSHE), and Magnetic Tunnel Junctions, therefore called the MESH (Magneto-Electric Spin-Hall) nano-oscillator.

Spin-torque oscillators have been experimentally realized for more than a decade now [63, 64], however they have a few challenges associated with them that prevent their commercial uptake, even though they are an attractive prospect due to their inherent compactness and high tunability [65]. Some of these challenges are: (a) low ac output power (b) low Q and high phase noise (c) necessity of an external magnetic field for robust operation. There is a vast body of literature on resolving these outstanding problems and develop better understanding of the complex magnetic dynamics of spin-torque oscillators [66].

The recently proposed MESH oscillator [57] resolves some of these issues using a combination of newly discovered physics of Magneto-Electric phenomena, Giant Spin-Hall Effect, separate READ and WRITE paths, and circuit techniques, such as injection locking, to make STOs an attractive alternative to CMOS based solid-state oscillators. Along with addressing the outstanding issues, the MESH oscillator increases the range of tunability, and possibility of voltage based synchronization of large arrays of oscillators. Since it is easier to distribute a voltage based signal of equal magnitude to multiple devices in a circuit compared to a current based signal, MESH oscillator provides a larger circuit design space than other STOs.

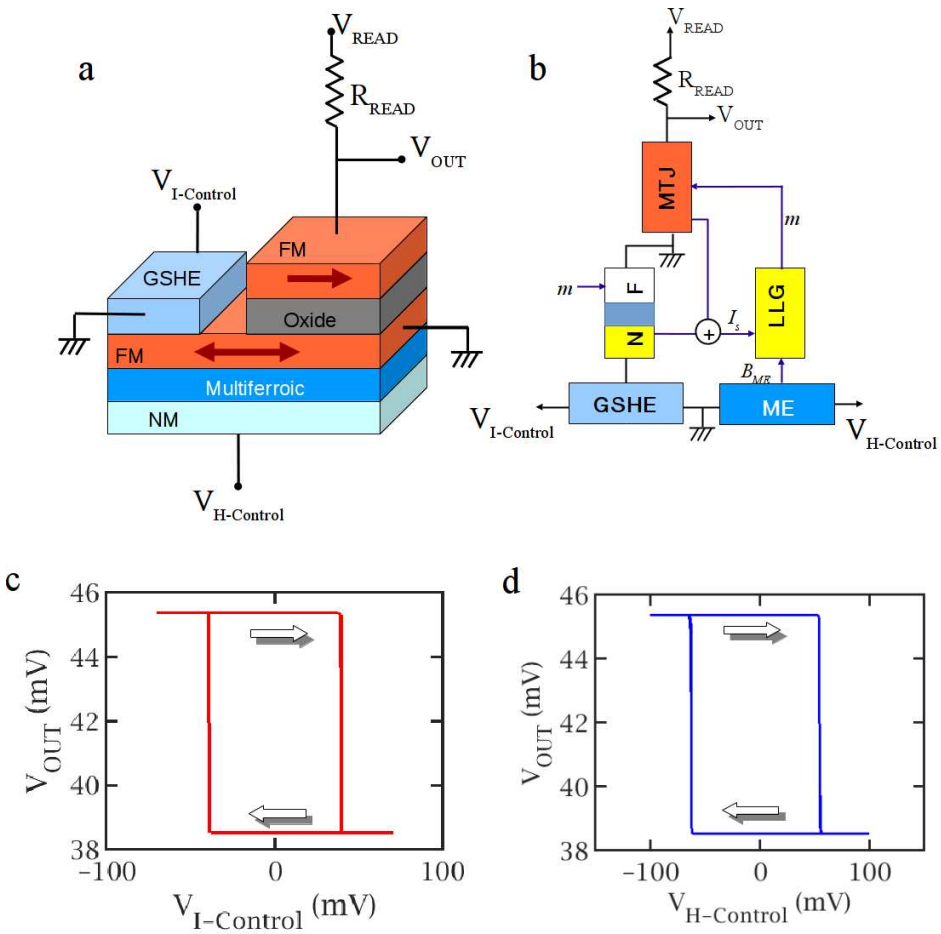


Fig. 3.5. **a. MESH oscillator schematic:** Device structure of the MESH oscillator. The input stage is composed of the GSHE driving an FM using the spin-torque and ME providing the controllable opposing magnetic field torque. The output is an MTJ whose resistance varies due to precession of the free layer. **b. Spin-circuit model:** Circuit model of the MESH oscillator built using the modules from the Modular Spintronics Library. **c. Device control through GSHE:** The device can be controlled using only the *I-Control* which controls the spin current torque applied through the GSHE input. **d. Device control through ME:** The device can be controlled using only the *H-Control* which controls the magnetic field torque applied through the ME input.

3.3.1 Device Characteristics

The device schematic is shown in fig. 3.5 a and the circuit model in fig. 3.5 b. The output stage of the device is an MTJ that generates the output ac signal, due to periodic change in the resistance of the device between "P" and "AP" states of the free layer, which is controlled by the ME and the GSHE inputs. Therefore, the device has a separate output path and can be biased for higher output ac power as compared to a two terminal device with a common READ/WRITE path.

The ME effect was recently shown [17] to be able to fully switch an in-plane anisotropy magnet by applying a voltage controllable exchange-interaction based magnetic field on an adjacent FM layer. While, the switching mechanism in itself was a complex two step process, which is not captured fully in the present ME model, this device only uses the ME effect to produce a controllable magnetic field, to remove the requirement of an external magnetic field, which in the more traditional designs is provided by a simple magnetic field source, such as an FM layer built into the device structure and is not controllable. The other control is applied through a spin-torque current generated by the GSHE on the free layer of the MTJ.

The two controls can independently switch the device as shown in fig. 3.5 c,d. However, when applied together but in opposition, the two torques try to switch free layer in their own direction which are opposite to each other. Therefore, the magnet keeps precessing due to the action of the two torques giving rise to steady state oscillations (fig. 3.6 a) even though the applied controlling signals are purely dc in nature. The phase space of the oscillator shows that the magnetization precesses in the plane of the magnet (fig. 3.6 b) The spectrum of the oscillation, without any noise, can be seen in fig. 3.6 c.

3.3.2 Injection Locking

Injection locking in oscillator happens when the frequency of a driven oscillator is pulled to the frequency of an external source and locked onto it [67]. It is a phenomena

of interest [68–70] since it allows tuning and synchronization of oscillators with wide ranging applications, one of them being phase noise reduction.

While the frequency of the traditional oscillators can be tuned by varying the spin-torque current on it, the MESH oscillator can be doubly tuned using both the spin-torque current as well as the voltage controllable magnetic field due to the ME (fig. 3.6 d,e). The dual tunability opens up a path for synchronization of a large array of oscillators because the external rf source can be applied as a voltage signal, which is easier to distribute across many oscillators without the problems of matching impedances as compared to a current source. We show an example simulation of phase noise reduction in a single oscillator. An rf source is applied to the $H - Control$ terminal of the oscillator and we can see from the spectrum of the oscillator that the phase noise is reduced significantly compared to an unlocked oscillator (fig. 3.7 a,b).

Spintronic oscillator's ability to dynamically tune, synchronize, and injection lock can have applications in building phase-locked loops (PLLs), clock recovery, on-chip antennas, signal amplifiers etc. which are usually implemented using analog circuits. MESH oscillator, which solves the longstanding engineering issues with STOs, can be a strong candidate for the role of the integrated solid- state oscillator of choice due to its inherent compactness, high tunability range, voltage-based injection locking, and integrability with CMOS and spintronics fabrication process.

3.4 Summary

In this chapter we demonstrated the use of Modular Approach to Spintronics in building spin-circuit models through three examples: (a) Write assisted PMA-MTJ STT-MRAM bit cells that can be used to build on-chip non-volatile memory, (b) Spin switch which is a logic device intended for digital logic applications, and (c) MESH nano-oscillator which is a solid-state tunable spintronic oscillator which may be used in analog applications such as signal processing and communication. We

further demonstrated how spin-circuit models for these models can be used to explore various aspects of these devices including performance and circuit applications.

The next chapter further demonstrates the power of Modular Approach to Spintronics as an analytical and diagnostic tool by delving into the physics of dissipation in spintronics devices using the spin switch as the example device.

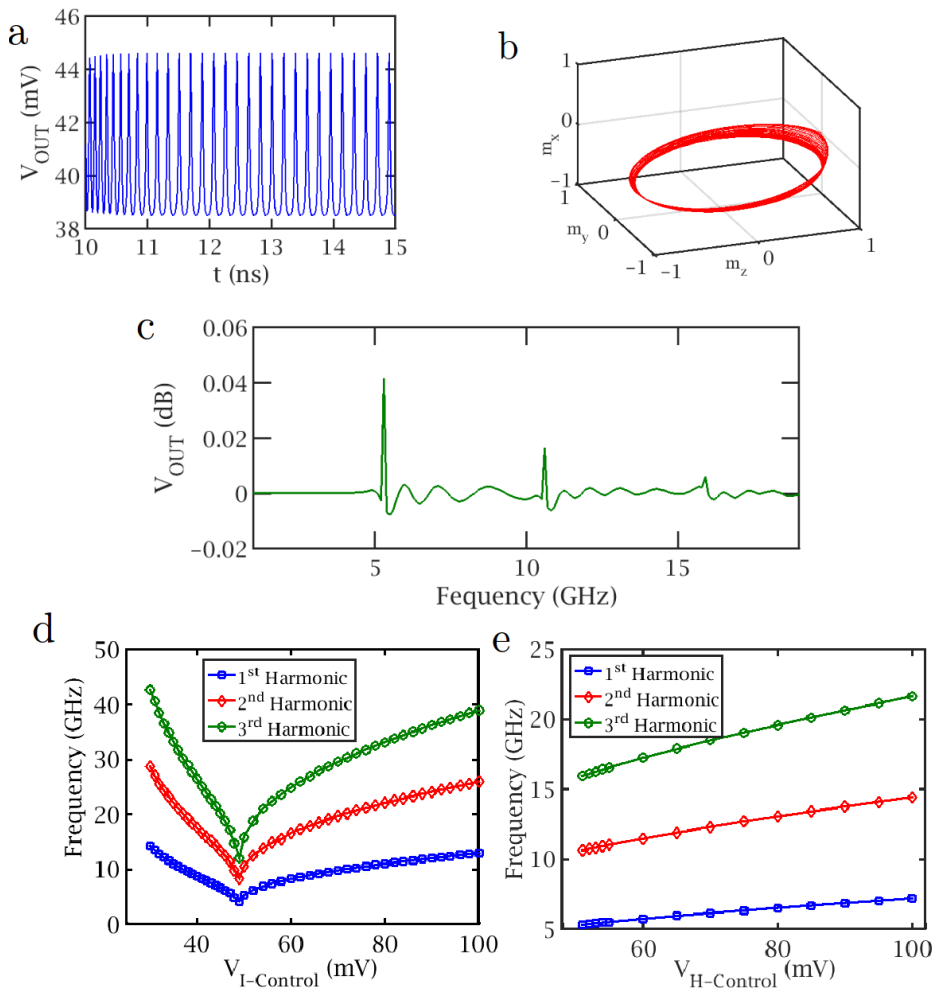


Fig. 3.6. **a. Transient simulation of MESH oscillator:** A transient simulation showing the oscillatory behavior of the MESH device. The resistance of the MTJ reader changes as a function of time which results an ac signal at the output. **b. Phase-space of the oscillation:** The magnetization of the free layer magnet under the influence of the opposing torques rotates in the plane of the magnet giving rise to the oscillations. **c. Spectrum of the oscillation:** Fourier transform of the oscillator response showing the fundamental and higher harmonics. **d. Frequency tuning through spin-torque current:** The frequency of the oscillation can be tuned by changing spin-torque applied through the $I - Control$ terminal which controls the spin current injected in to the FM from the GSHE. **e. Frequency tuning through ME magnetic field:** The frequency of the oscillation can be tuned by changing magnetic field torque applied through the $H - Control$ terminal which controls the magnetic field applied to the FM from the ME.

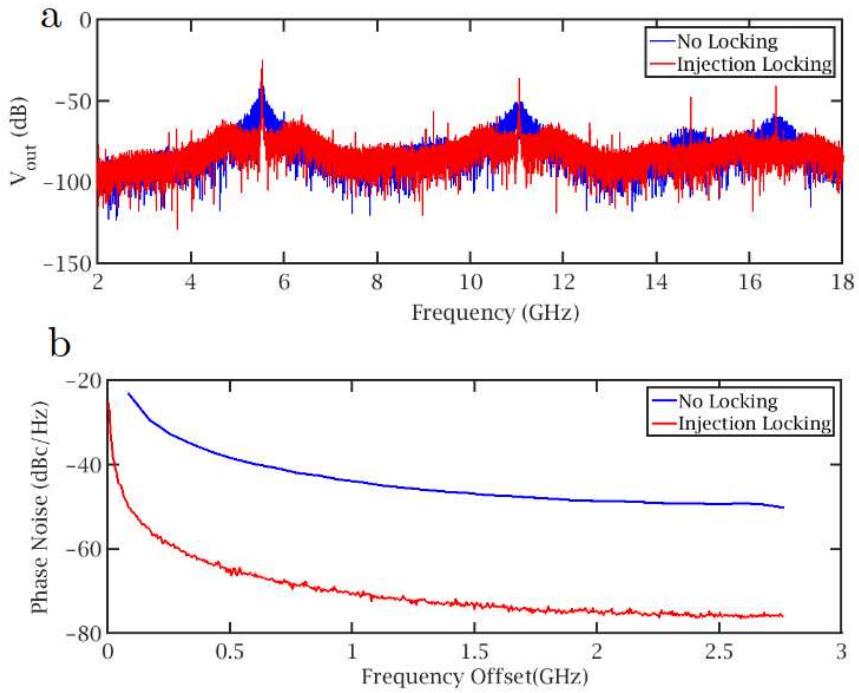


Fig. 3.7. **a. Spectra of noisy unlocked and injection locked oscillator:** A transient simulation showing the oscillatory behavior of the MESH device when the spin-torque and magnetic torques are in opposition and balanced. The resistance of the MTJ reader changes as a function of time which changes the resistance of the voltage divider at the output stage and as a result an ac signal is produced at the output. **b. Phase noise reduction in injection locked oscillator:** Phase noise is reduced in the injection locked oscillator compared with the unlocked oscillator.

4. DISSIPATION: SPIN SWITCH VS. CMOS

This chapter is adapted from Samiran Ganguly, Kerem Yunus Camsari, Supriyo Datta, "Evaluating Spintronic Devices Using The Modular Approach" [1]

In this chapter we use Modular Approach to Spintronics to investigate the fundamental factors that lie at the heart of dissipation in spintronic logic devices. As Moore's law comes to an end enforced by physical limits of sclaing down the CMOS, the search for an alternative is at full pace. Many alternatives have been envisioned, which range from modification of the basic design of planar MOSFET to wrap-around gates or FinFETs, Tunneling FETs, to different materials such as graphene nanno-ribbons, to completely new physics such as spintronics.

To make sense of these new alternatives and create a uniform apples-to-apples comparison, the product of switching energy and switching delay ($E \times \tau$) per switching event of a logic unit has been proposed as a universal comparative metric. The merit of such a metric lies in the fact that to work as a drop-in replacement for CMOS both of these quantities need to be small compared to CMOS. As a result smaller the $E \times \tau$ of a device, better is its prospect as a CMOS replacement.

However, $E \times \tau$ analysis is limited to the dissipation only during the active or dynamic conditions. It is important to capture the static dissipation (I^2R at steady state) as well, since a logic switch may "leak" currents even under standby conditions which eats in to the thermal design budget of the circuits. This work, for the first time, discusses the static dissipation along with dynamic dissipation together, through the context of spintronic logic devices.

Our methodology of analysis of dissipation of logic devices is following:

- Creation of spin-circuit model of the device using Modular Approach to Spintronics.
- Benchmarking and verification of the model in a circuit testbench.
- Measuring the static power dissipation, switching energy, switching delay, total and switching charge consumed per switching event.

In this chapter we focus on the dynamic and static dissipation in the originally proposed spin switch [24] as an example to examine the physics of power dissipation in spintronic devices. The spin switch, as discussed in the previous chapter, uses a complementary dual MTJ stack for READ, while WRITE is through a GSHE layer driving a ferromagnet (FM), and these two stages are coupled magnetically. The GSHE-based writing provides electrical gain in its I/O characteristics, whereas the electrical isolation is provided by magnetic-only coupling. In the previous chapter we developed the spin-circuit model of the spin switch and demonstrated its use as a logic switch in a small circuit.

As a reference point, we use a CMOS inverter built from ASU-PTM models for 14nm HP-FinFETs [71,72] to highlight the differences and similarities between physics of switching and power dissipation in both charge based and spin based devices.

The circuit testbench used in this work is a simple Fan-out of 1 (FO-1) inverter chain. This is the simples testbench that can be used and keeps the analysis focused on the devices itself. Other possible testbenches that may be used are FO-4 chain, Half and Full Adders, MUX etc. Fig. 4.1 a,b show a FO-1 inverter chain built using CMOS and the spin-switch respectively. Details on simulation parameters are listed in the appendix.

4.1 Static Dissipation: I^2R

Static power dissipation in a logic device is the Joule heating ($I^2R = V^2/R$) losses at steady state, i.e. when the device is not switching. In a circuit a logic device may

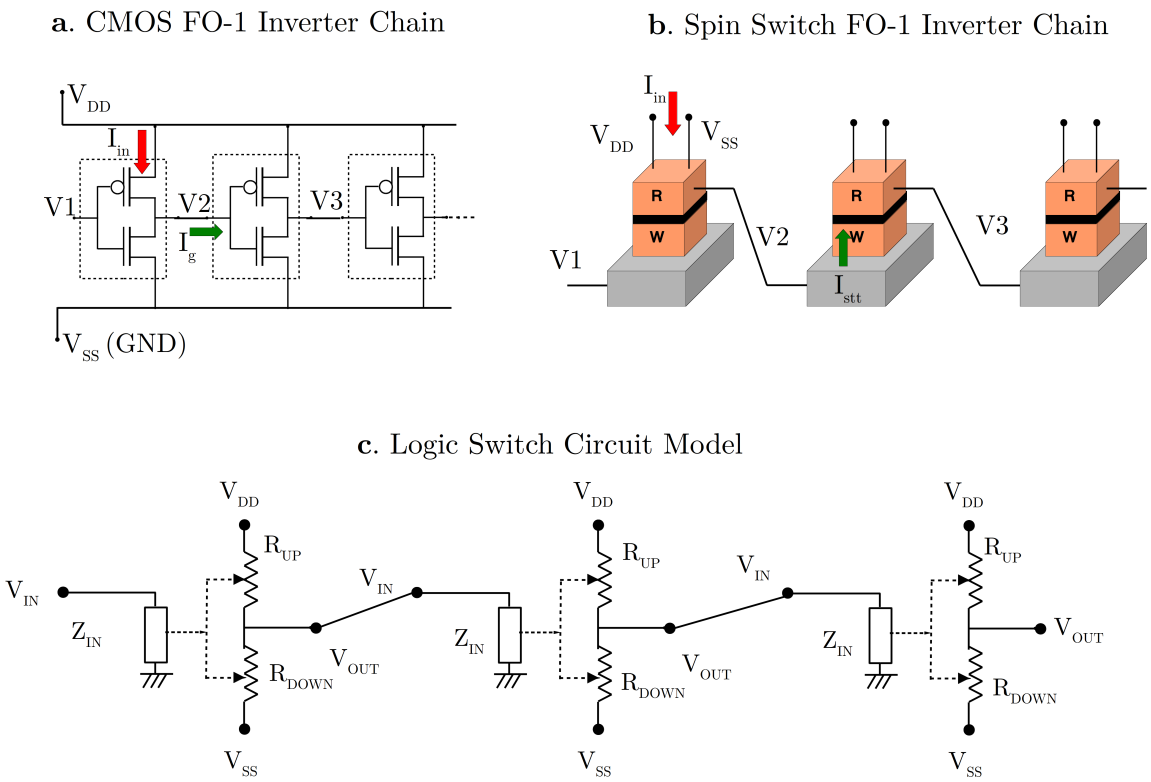


Fig. 4.1. **a. Circuit testbench for CMOS:** FO-1 Inverter chain built using CMOS inverters. **b. Circuit testbench for spin switch:** FO-1 Inverter chain built using spin-switch. **c. Circuit Model for Logic Switch:** A logic switch like CMOS or spin switch is composed of a pull up and pull down impedances whose magnitudes are controlled by the input signal.

spend only a short duration when it is switching during a given computation, it is important to analyze a logic device in terms of its static dissipation, along with its dynamic dissipation, to obtain a complete picture of its total dissipative performance.

Using our FO-1 circuit testbench, we can measure the static dissipation for both CMOS and spin switch devices. Since the static dissipation depends on the voltage applied ($P = V_{DD}^2/R$) to the device, lowering the supply voltage helps in lowering the static dissipation, it is desirable to keep the supply voltage to as low as possible. However, low supply voltages may not be able to provide enough device performance

in terms of power delivery and speed, therefore choosing a bias point is an exercise of compromise in terms of static dissipation and device performance. While this optimal bias point is a function of specific circuit design, for our analysis we do not try to optimize the V_{DD} values and just use a value that is moderately higher than the threshold for both CMOS and spin switch.

Fig. 4.2 a,b show transient simulation of a switching event and the resultant toggling of the voltages causally ($V1 \rightarrow V2 \rightarrow V3$) in the three switches of the FO-1 logic pipeline. The supply voltage levels used in HP-CMOS are typically $700 - 900\ mV$, whereas in spin-switch at minimal overdrive, it can range from $10 - 100\ mV$, ($80\ mV$ in this case) and is sufficient to generate the threshold spin current necessary ($100 - 200\ \mu A$) to switch a typical nanomagnet with a $40\ k_BT$ stability, given the characteristic resistances of all the components (GSHE, MTJ) are around $0.5 - 2\ k\Omega$ (a complete list of parameters are listed in the appendix). These resistances are comparable to the "ON" state resistance of the MOSFETs composing the CMOS ($3 - 5\ k\Omega$).

The static power levels in HP-CMOS are of the order of nW (inset of fig. 4.2 c) as expected from the leakage current levels [73], which is much lower compared to dynamic power levels.

Since the voltage level required in spin switch is an order of magnitude smaller and the component resistances are similar to CMOS values, it may be expected that the static dissipation in spin switch should be nearly two orders of magnitude smaller than CMOS.

However, the static power dissipation in spin switch is nearly the same as the dynamic power dissipation because the spin switch does not turn off at steady state (fig. 4.2 d). If we look at the circuit model of a logic switch (fig. 4.1 c), at steady state, the resistances of one of the complementary R_{UP} and R_{DOWN} pair is *ON* and the other one is turned *OFF*. In the MTJ the R_{ON} corresponds to the parallel state resistance of the MTJ pillar R_P, while the R_{OFF} corresponds to the anti-parallel state resistance of the MTJ pillar R_{AP}. In a typical MTJ structure the resistance

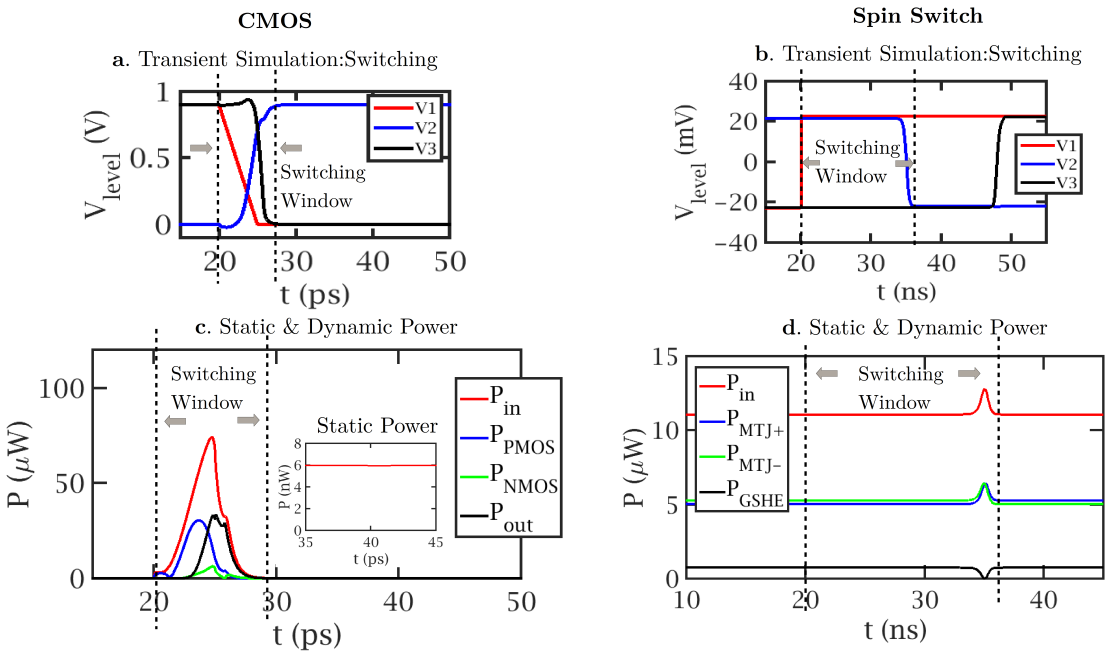


Fig. 4.2. **a. Simulation of CMOS FO-1 testbench:** The transient simulation shows a switching event. A change in V1 from high to low level cause V2 and V3 to change sequentially. **b. Simulation of spin switch FO-1 testbench:** The transient simulation shows a switching event. A change in V1 from high to low level cause V2 and V3 to change sequentially. **c. Static and Dynamic Power in CMOS:** Dynamic power dissipation in first CMOS inverter in the chain. Power dissipated in the PMOS and the NMOS transistors, the output (the next stage), and the total power provided by the supply rail are shown. **(Inset)** Power dissipation at the steady state. **d. Static and Dynamic Power in CMOS:** Static and Dynamic power dissipation in the first spin switch. Power dissipated in the two MTJs (reader), the output (GSHE of the next stage), and by the total power provided by the supply rails are shown.

ratio R_{AP}/R_P is around is $3-4$, corresponding to the spin current polarization $P \sim 0.7-0.8$, compared to CMOS where R_{OFF}/R_{ON} of the PMOS−NMOS pair is $10^4 - 10^5$. Additionally, the input side of the spin switch (the GSHE layer) is a static low impedance resistive component ($Z_{IN} \sim 1\ k\Omega$), unlike the CMOS where the MOSFET gate terminal is a high impedance capacitive components which becomes open circuit at steady state ($Z_{IN} \sim 1/\omega C$ where $\omega \to 0$ at steady state). As a result

of these two static current flows, the static power dissipation never reaches nW levels for the spin switch.

This analysis is evidenced by fig. 4.2 d where it can be seen that the major contribution to static dissipation is attributable to the dissipation in the individual MTJ pillars of the READER component of the spin switch, and a small constant static dissipation in the WRITER component of the spin switch. Whereas in the CMOS (fig. 4.2 c) most of the power consumption is during the switching process and at the steady state the power consumption is a few nW due to very low dissipation of very high resistive path due to one of the MOSFETs in the CMOS pair being in cut-off mode.

4.2 Dynamic Dissipation: $E \times \tau$

Any alternative to CMOS technology needs to be competitive in terms of both the switching delay and switching energy. Therefore, a useful measure of dynamic (switching) dissipation is the product of the switching energy $\times$ switching delay ($E \times \tau$ product) per switching event, because a switch can be overdriven for lower switching delay, resulting in higher switching energy or vice versa.

It has been shown [74] that the $E \times \tau$ product can be related to the charge consumed during the switching process, i.e. $E \times \tau = (I_{sw}^2 R\tau) \times \tau = Q_{sw}^2 R$, where Q_{sw} is the charge necessary to complete the switching mechanism of device drawn over the effective resistance R of the device. In CMOS, the switching mechanism is the gate capacitors of the CMOS transistors being charged and discharged, whereas in spin-torque devices it is the minimum charge necessary to switch the magnet. In spin-based devices employing pure spin-currents, such as All Spin Logic device [23], this resistance is measured along the charge current path drawn from the supply, whereas for spin switch it is the resistance of the GSHE layer.

The $E \times \tau$ metric recast as $Q_{sw}^2 R$ provides a powerful insight in understanding the fundamental limits of dynamic dissipation in a device by quantitatively relating

it to its material properties and physical dimensions and opens a pathway to better component design for higher performance by scaling the device dimensions and using materials of desired properties wherever possible.

Based on this understand of dynamic dissipation, we look at the switching delay and the switching energy of the CMOS and the spin switch devices and relate them to the switching charge.

Switching Delay: τ

The timescale of switching in a scaled CMOS inverter, a 14 nm FinFET in this case, is of the order of $\approx 1 - 10$ ps (fig. 4.1 a). The switching delay for magnets is dependent on the current overdrive: At *large overdrives* the delay can be determined by angular momentum considerations, where a total amount of charge that is twice the number of spins ($M_s\Omega/\mu_B$) needs to be deposited for a complete reversal of magnetization. This means that the switching delay inversely scales with the driving current, i.e. $\tau \sim 2eM_s\Omega/\mu_B I_s$ and near *zero overdrive* conditions, the delay is determined by the characteristic time scale of the magnet, $\tau_0 \sim 1/\alpha\gamma H_k$, which is closer to the conditions simulated here and is about 20 ns for the parameters used. In both cases, however, the exact switching delay is a strong function of the initial angle of the magnetization [61]. In our simulations, the initial angle is chosen to be the rms of the equilibrium deviation from the easy axis [23].

Sluggish dynamics of magnets at low to moderate overdrives is a major handicap of spintronic devices and any measure to improve switching delay reduces the dynamics dissipative. Therefore, it is preferable to find material solutions for higher switching speeds rather than using ultra-high overdrives, as it negatively impacts the static power dissipation and reduces reliability.

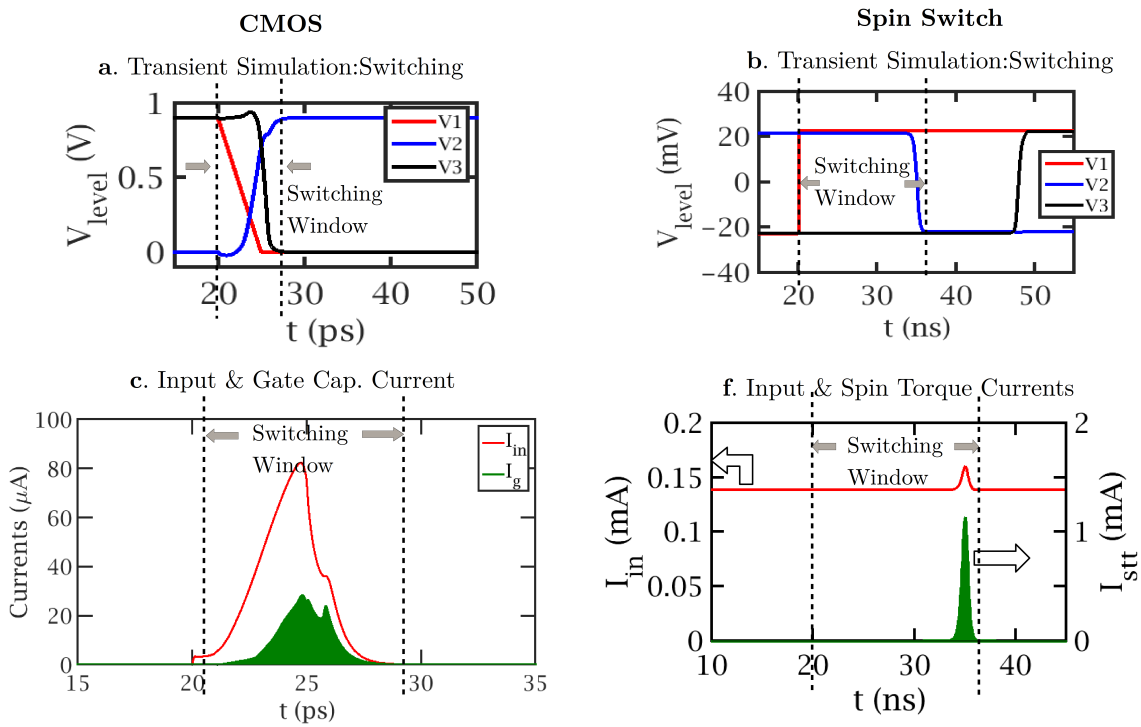


Fig. 4.3. **a. Circuit Testbench for CMOS:** The transient simulation shows a switching event. A change in V1 from high to low level cause V2 and V3 to change sequentially. **b. Circuit Testbench for spin switch:** The transient simulation shows a switching event. A change in V1 from high to low level cause V2 and V3 to change sequentially. **c. Switching (Q_{sw}) and Total ($Q_{tot.}$) Charge in CMOS:** (Green area) Charge involved in switching the CMOS inverter, i.e. the charging of the gates , and (red) total charge supplied by the source in the switching process. **f. Switching (Q_{sw}) and Total ($Q_{tot.}$) Charge in spin switch:** (Green area) Charge involved in switching the spin switch, i.e. the spin-torque switching of the write magnet, and (red) total charge supplied by the source in the switching process.

Switching Energy: E and Switching Charge: Q_{sw}

Switching energy of both the CMOS and the spin switch can be obtained numerically by simply integrating the power between the switching window. However to gain better physical understanding of dynamic dissipation, we look at the switching charge, as discussed at the beginning of the section.

To do so from our FO-1 circuit testbench, we first integrate the input supply current (red arrows indicated in fig. 4.1 a,b) pumped in from the supply rails connected to $V_{DD;SS}$ within the switching window, whose starting point is the time-point at which the input signal starts changing and the ending point is the time-point at which the output signal is within 1% of the final value. This provides the total charge per switching event.

Additionally, we integrate the net current deposited to the CMOS input terminal (gate terminals of the PMOS and NMOS) and we do the same for the analogous quantity for magnets, the z-component of the spin-torque current ($I_{STT;z} = (\hat{m} \times \overrightarrow{I_s} \times \hat{m})_z$) generated by the GSHE layer on to the NM−FM interface. These currents are indicted on both the CMOS and the spin switch by the green arrows in fig. 4.1 b.

We find that the area under the green curve for the CMOS (fig. 4.3 c) is about $220e^-$, equivalent to the charge deposited to the CMOS gates $Q_{sw} = (C_{gate}^{PMOS} + C_{gate}^{NMOS})V_{DD}$, whereas the green area for the spin-switch (fig. 4.3 d) is about $Q_{sw} = 2qN_s \approx 1,600,000e^-$ where $N_s = M_s\Omega/\mu_B$ is the total number of spins (μ_B). The quantity Q_{sw}/V_{DD} may be considered as equivalent "gate capacitance" of the spin switch, even though there is no physical capacitor in the switch. Therefore, reducing the dynamic dissipation for spin switch and indeed any logic device involves scaling the switching charge Q_{sw} [75,76] by reducing the supply voltage level and the physical dimensions and better material properties, better device design or through voltage control of the magnetism.

It should be noted that the switching charge Q_{sw} in this discussion is an approximate measure of $E \times \tau$ since it does not incorporate the steady state currents discussed in static dissipation section. Additionally, a device in a circuit needs to drive other devices (fan out) at its output stage. The power necessary to drive these fan-outs has to be supplied by the device as well, unless buffer stages are used.

Using our methodology, we can relate the Q_{sw} to the total charge Q_{tot} provided by the supply which includes the static currents as well as the load of the fan-out (FO-1 here). As an example in fig. 4.3 d, the area under the red curve integrated

in the switching window, gives the total charge Q_{tot} pumped in by both the supplies (V_{DD}, V_{SS}) during one switching event. This area is about 10 times the green area which gives the Q_{sw}, in the case of spin-switch. For the CMOS inverter (fig. 4.3 c), the total charge $Q_{tot.}$ pumped is about 6 times the switching charge Q_{sw}. Any improvement in scaling down the dynamic dissipation will then involve reducing the switching charge Q_{sw} as well the total charge consumption Q_{tot} during switching by better component design.

4.3 Fundamental Quantities for Dissipation

Metric	**HP-CMOS**	**Spin Switch**
Voltage Level	$\sim 700 - 1000\ mV$	$\sim 10 - 100\ mV$
Static Power	$\sim 10^{-3}\ \mu W$	$\sim 10\ \mu W$
Dynamic Power	$\sim 10^{2}\ \mu W$	$\sim 10\ \mu W$
Switching Delay	$\sim 10^{-2}\ ns$	$\sim 10\ ns$
Switching Charge, $\mathbf{Q_{sw}}$	$\sim 10^{2} - 10^{3}\ e^{-}$	$\sim 10^{5} - 10^{6}\ e^{-}$
$\mathbf{R_{OFF}/R_{ON}}$	$\sim 10^{5}$	~ 4

Table 4.1
Comparison between HP-CMOS and Spin Switch Dissipation

We can summarize the analysis of static and dynamic dissipation carried out in this chapter in table. 4.3.

It is commonly touted that low voltage $(10 - 100\ mV)$ operation of spintronic devices promise higher energy efficient computing over CMOS. To test this assumption, we looked into fundamental factors behind the static and dynamic dissipation in the spin switch, as an example spintronic logic device whose spin-circuit model was discussed in the previous chapter. We used a projected model of 14nm FinFET based CMOS to compare and contrast the spin switch and highlight these factors.

For static dissipation we found that the critical difference between the CMOS and the spin switch is the ratio of the resistance between ON and OFF states of the device. In CMOS this ratio is of the order of $10^4 - 10^5$ which is primarily obtained due to resistance ratio between the saturation and cut-off regimes of modern transistor operation. Also a capacitive input terminal ensures that the resistance ratios remain high by blocking any static currents paths at steady state. However in spin switch the typical resistance ratio between the P and the AP states is $3 - 4$. In addition, the input terminal of the spin switch is a relatively low resistance terminal in steady state. Altogether this causes the static dissipation to be to be orders of magnitude higher than CMOS.

Therefore, the fundamental quantity that determines the static dissipation in a logic switch is the resistance ratio R_{ON}/R_{OFF}, which is dependent only on the physical properties of the device and can be identified directly from a geometry and materials based analysis of the device.

For dynamic power, we focused on the $E \times \tau$ as a metric for the dynamic dissipation, since it attempts to quantify it in terms of both switching delay and switching energy together, since both are critical measure of performance of a logic switch and lower is $E \times \tau$ better a switch is. We noted that the $E \times \tau$ can be recast as the product $Q_{sw}^2 R$ where Q_{sw} is the charge that needs to be provided to the device to switch it through a path whose the resistance is R.

We measured the switching charge Q_{sw} for the CMOS and found it to be the charge deposited on the CMOS input gate terminals and was the order of $Q_{sw} \sim 200 - 300\ e^-$, whereas in the spin switch it was the integral of the **z**-component of the spin torque on the magnet. We found it to be equivalent to twice the total number of spins in a magnet and was the order of $Q_{sw} \sim 10^5 - 10^6\ e^-$ for unoptimized magnet designs. The total charge $Q_{tot.}$ consumed during switching can be related to the Q_{sw} through the loading conditions and details of the device's transport properties, both of which can be captured in the spin-circuit model.

Therefore, the fundamental quantity that determines the dynamic dissipation in a logic switch is the switching charge Q_{sw}, which again is dependent on the physical properties of the device and can be identified directly from a geometry and materials based analysis of the device.

It should be noted that while a geometrical and materials analysis of a logic device, backed by Modular Approach to Spintronics, can provide important insights in the dissipative performance of the device, the full picture can only be obtained by incorporating proper loading conditions of the circuit the device is used in and for such an analysis Modular Approach to Spintronics becomes critically important due to its ability to connect material properties to systems aspect of device operation.

While the details of the physics of these examples (CMOS and spin switch) depend on the specifics of circuit and device design, material properties and overdrive conditions, we believe that the measure of static power in terms of R_{OFF}/R_{ON} (READ) and dynamic power in terms of Q (WRITE) are general notions that are applicable to any logic device.

4.4 Summary

In this chapter we demonstrated the use of Modular Approach to Spintronics in analyzing static and dynamic dissipation in spintronic devices, using the spin switch as an example. We used an FO-1 inverter chain as a circuit testbench to measure the dissipation in details, a capability offered by Modular Approach to Spintronics through details spin-circuit modeling of the spin switch. We identified the fundamental factors behind both static and dynamic dissipation in terms of physical properties of the device which opens up a path for improving dissipative performance through better component design.

The next chapter explores various pathways to improve the dissipative performance of the spin switch device. We again demonstrate the power of Modular Approach to Spintronics in making such an exploration possible due to the modular

design of the spin-circuit which allows to incrementally modify the design one-by-one to obtain a completely new design with better performance.

5. ALTERNATIVE DESIGNS FOR SPIN SWITCHES

This chapter is adapted from Samiran Ganguly, Kerem Yunus Camsari, Supriyo Datta, "Evaluating Spintronic Devices Using The Modular Approach" [1]

In this chapter we explore various alternatives that can improve the dissipation in spin switches. Using Modular Approach to Spintronics we modify the spin switch design we presented in chapter 3 with different materials, magnetic stacks, and magnetic phenomena based on the findings of the chapter 4, we show how the spin-switch device can be made made more efficient and a more viable candidate for replacing the CMOS technology in circuit designs.

Modular Approach to Spintronics based device optimization enables us to project performance enhancements quantitatively and build possible roadmaps for optimized spin-switch devices. In this chapter we have covered only a small sampling of possible optimizations and design space for spintronic devices. Our main purpose in this chapter is to demonstrate the power of Modular Approach to Spintronics in component design and comparative evaluation.

In addition to the alternative designs based on new physics and materials, Modular Approach to Spintronics can be used effectively to explore circuit techniques such as power-gating by leveraging the non-volatility of spin-switches, as demonstrated in our proof-of-concept example at the end of the chapter.

In fig. 5.1 we show a host of material and design optimizations that can be conceivably incorporated into the spin switch design to make it optimized for lower dissipation. In the READER side, we can use Heusler alloys ($CoMnSi, CoFeAl$) to increase the TMR of the complementary MTJ pair. Instead of complementary MTJ pair, we can use an Inverse Spin-Hall Effect (ISHE) based component ($\beta - Ta, W, Pt$). Similarly, in the WRITER side, we can use materials with very high

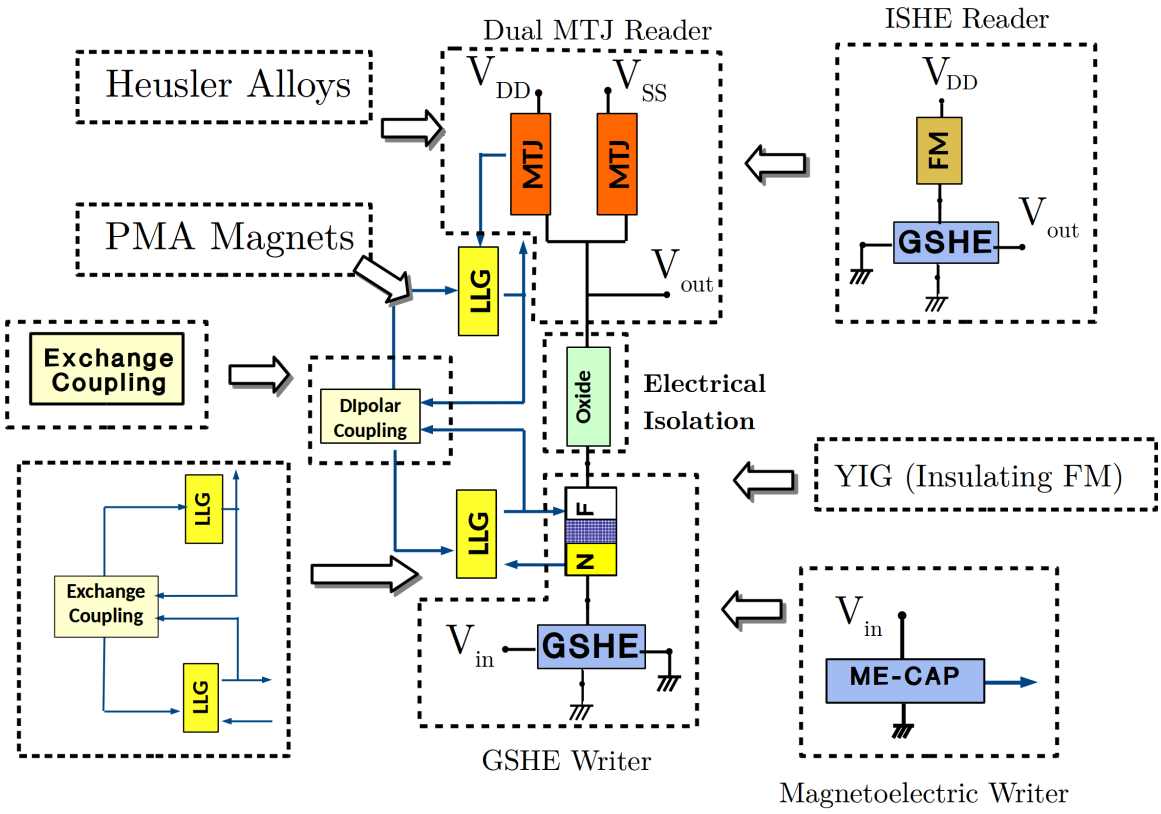


Fig. 5.1. **Alternative Designs for spin switch:** Modular Approach to Spintronics allows us to create alternative designs by replacing an individual module with another or changing the materials, without changing the full spin-circuit model, either one at a time or altogether. Each of these alternative designs can then be evaluated for their $E \times \tau$ and static power and compared with other posible designs. The figure illustrates modification to the spin switch can be incorporated in using Modular Approach to Spintronics by swapping appropriate modules in the spin-circuit model, due to the built-in modularity of the spin switch in terms of READ and WRITE units. A few possible alternatives shown here are High Anisotropy PMA magnets, Heusler Alloys, High spin-Hall angle materials and Topological Insulators, Ferromagnetic Insulators (YIG, BFO), exchange-coupled magnets using magnetic oxides, Synthetic Ferrimagnetic stacks, Multiferroics, and Inverse Spin-Hall Effect based readers.

spin-Hall angle, say Topological Insulators ($Bi_2Se_3, Bi_2Te_3, HgTe$), or use different magnetic phenomena such as Magneto-Electric effect of the single phase multifer-

roics ($BiFeO_3, LaMnO_3, CrO_3$) or compound multiferroics which concatenate multiple ferro- phenomena. The magnets can be replaced by scaled high anisotropy (H_k) PMA magnets, perhaps necessitating the use of magnetic oxides ($NiFeO$) to provide stronger Exchange-interaction based coupling between the READER and the WRITER of the spin switch. We may even replace single magnets with magnetic stacks composed of smaller magnets ($CoFe - Ru - CoFe$), forming synthetic or composite ferrimagnets, or ferromagnetic insulators such as Yttrium Iron Garnets (YIG) or magnetic oxides ($BiFe_12O_19$) which can act as both the WRITE magnet as well as the isolating layer.

The purpose of listing an expansive list of possible alternatives is to point out that spintronics is a constantly evolving enterprise and that Modular Approach to Spintronics provides a powerful tool to quickly incorporate these new materials and phenomena into existing device designs and test their efficacy in performance enhancement of spin switch or any other spintronic device.

In this chapter we have shown three example trajectories of how the spin-switch can be optimized by stacking one change on top of the other and observe its effect in reducing the static and the dynamic dissipation. The rest of the chapter describe the changes we introduce to the spin switch design that are stacked on top of each other. While each of these improvements can be applied independent of each other, the presented information shows how the performance of the spin-switch can improve dramatically when these optimizations are applied in succession.

The numbers reported in this section are from the measurements of static power ($S = I^2R$), switching delay (τ), and the switching energy (E) of simulations performed for spin switch with magnet of barrier height $U = 40\ k_BT$ in a FO-1 circuit testbench, as described in details in the chatper 4. These numbers would vary if a different testbench, such as FO-4 or 32-bit adder, is chosen, since it will change the loading conditions.

While some of the spin-switch designs explored in this chapter could work with ultra low voltages ($< 20\ mV$), a realistic circuit may not be able to provide $V_{DD;SS} <$

50 mV [77] due to the inherent inability to deliver sufficient power at such low voltages. Access transistors could be used in conjunction with each spin-switch to obtain lower voltages and such transistors will have their own dissipation. We have used a minimum supply voltage level of 35 mV in some of the alternative designs but do not include dissipation numbers of transistors in such cases.

In this chapter our analyses are limited to the devices themselves and we do not measure dissipation in interconnect and supply rails, which are important considerations and to a large extent depend on layout of the circuits. These considerations can be included for specific circuits by using transport modules from the Modular Spintronics Library to model the interconnects.

We have provided analytical device equations for the family of the spin-switch described in this chapter and also provide estimates for minimum operating points for these devices. The materials database in the appendix has all the parameters required for the estimates.

5.1 Perpendicular Magnetic Anisotropy

The first improvement we make to the device design is the replacement of both READ and WRITE magnets which have in-plane magnetic anisotropy (IMA) primarily due to shape anisotropy with thin ($t_{FM} < 2nm$ for $CoFeB$) circular magnets which primarily show surface/interfacial perpendicular magnetic anisotropy (PMA), i.e. the easy axis of magnetization lies in the out-of-the-plane direction of the magnetic layer.

This change keeps the magnet's barrier same, since $2U = M_s \Omega H_k$ but can reduce the minimum switching current required by getting rid of the demagnetizing field ($h_d = 4\pi M_s/H_k$), since in the monodomain approximation the in-plane minimum switching current is given by [61]:

$$I_{s;crit} = \frac{4q}{\hbar}\alpha U(1 + \frac{h_d}{2}) \tag{5.1}$$

However GSHE-based switching employing PMA magnets introduces the well-known problem of indeterministic switching. The polarization of the injected spin-current from the GSHE is given by $\hat{\sigma} = \frac{\overrightarrow{J}_s \times \overrightarrow{J}_c}{|J_s J_c|}$. Since the FM is on top of the GSHE, the $\overrightarrow{J}_s$ is in the out-of-plane direction and the polarization of the spin current generated is in the in-plane direction. This in-plane polarized spin current can only bring the magnetization of the FM layer to in-the-plane of the FM through spin-torque action. This "hard axis" in-plane direction is energetically unfavorable for the magnet and is an unstable position, i.e. the magnet has an equal chance of going back to its original easy axis position or switch to the other opposite direction, determined solely by thermal noise once the torque is removed.

It was found that a small magnetic field ($\overrightarrow{h}_{bias} = \overrightarrow{H}_{bias}/H_k$) in the direction of the charge current ($\overrightarrow{J}_c$) helps break the symmetry of this equilibrium position and push the magnetization towards an easy axis deterministically (given by $\hat{\sigma} \times \overrightarrow{h}_{bias}$).

This field may be provided either through a global magnetic field, locally through an extra passive magnetic layer built in the structure of the device [78], or as a small exchange-bias field also built within the structure of the magnetic stack [79]. Whatever be the mechanism of providing the bias field, we can incorporate this field in our model simply as an additional external field provided to the LLG modules in the spin-circuit model.

For a GSHE driven PMA magnet in presence of the bias field, the minimum spin-current necessary to switch the magnet is a modified version of the minimum hard axis switching current:

$$I_{s;crit} = \frac{4q}{\hbar}\frac{U}{2} \tag{5.2}$$

and is approximately given by [80]:

$$I_{s;crit} = \frac{4q}{\hbar}U(\frac{1}{2} - \frac{h_{bias}}{\sqrt{2}}) \tag{5.3}$$

It is interesting to note that the threshold current for "hard-axis" switching does not benefit from a one to two orders of magnitude reduction due to the absence of the damping factor α that is present in eq. 5.1.

In both fig. 5.2 and fig. 5.3 for the low H_k PMA design points we observe that changing the magnetic layers in the spin switch from IMA to PMA reduces both the switching energy as well the static power dissipation, due to the relatively lower switching currents that allow reduced supply voltages.

While the threshold switching current for PMA magnets (eq. 5.3) could be smaller or larger than IMA magnets (eq. 5.1) depending on magnet design and material parameters, we show in the next optimization how going PMA over IMA can open a pathway for aggressive scaling of magnets for higher performance devices.

5.2 High Anisotropy Magnets

Using PMA magnets in spin-switch opens up the possibility of using high anisotropy magnets commonly used in the magnetic recording industry. This can be achieved by aggressively scaling down the grain volume (Ω) and saturation magnetization (M_s) while increasing the effective anisotropy (H_k) to maintain a given thermal stability since the barrier height is given by $2U = M_s \Omega H_k$.

The reason for choosing PMA magnets rather than IMA magnets for scaling is that PMA magnets are circular or nearly circular in shape, to have a large interfacial or surface anisotropy in the out-of-the-plane direction rather than in the in-plane direction, which is the common mode of obtaining anisotropy in PMA since intrinsic bulk magnetocrystalline anisotropy can not be scaled.

This circular profile is much easier to scale down compared to the rectilinear profile of IMA magnets whose anisotropy is obtained largely due to aspect ratio, in which easy axis lies in the longer direction. At aggressive limits of scaling it will difficult to control or indeed even create very large shape anisotropy due to lithographic and

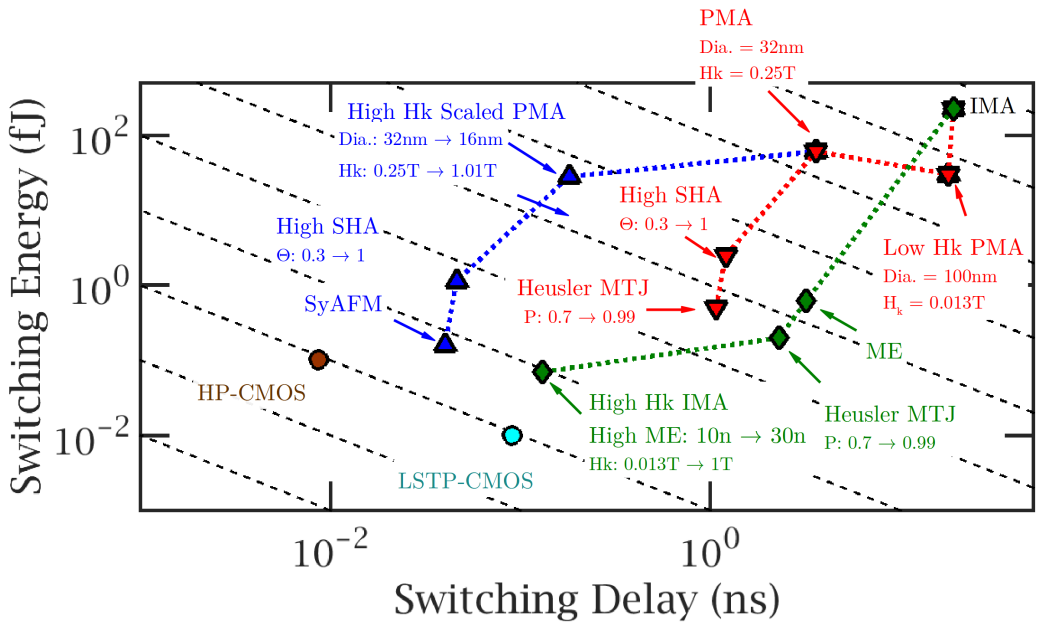


Fig. 5.2. **E $\times \tau$ Improvement through Material Optimization:** Investigating the improvement of $E \times \tau$ under various alternative materials and device shown in three different design trajectories, and comparison with CMOS. The three trajectories employ innovations such as high H_k scaled PMA magnets, Heusler alloys, high spin-Hall angle (SHA) materials, multiferroics (ME), and synthetic ferrimagnets (Sy-AFM). The optimizations applied together can bring the performance of spin switches to within an order of magnitude of $E \times \tau$ of both high performance and low standby power CMOS (HP-CMOS, LSTP-CMOS).

fabrication issues, along with the difficulty of maintain a close-to-monodomain limit for IMA magnets with large aspect ratios.

For scaled PMA with high anisotropy design that maintains a constant barrier height, the minimum spin-current necessary to switch remains the same since it depends only on the barrier height (eq. 5.2), the current density necessary to produce this current increases quadratically with the reduction in the geometrical profile of the magnets, which can severely limit the reliability of the device as discussed in chapter 3 in context of write assisted PMA MTJs.

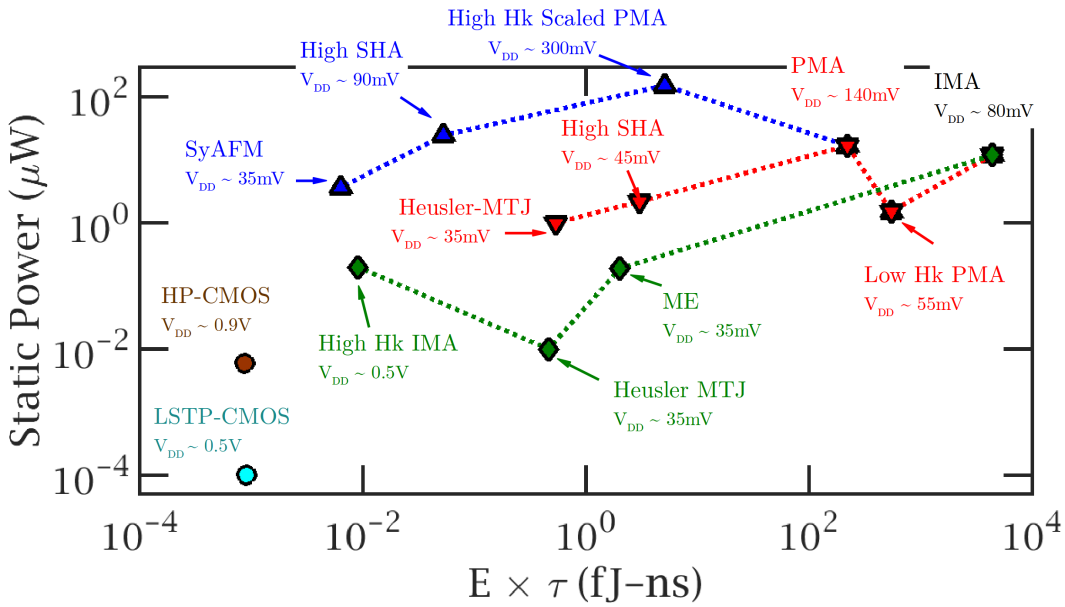


Fig. 5.3. **Static Power Improvement through Material Optimization:** Investigating the static energy dissipation for the three different design trajectories (same as in fig. 5.2) and comparison with CMOS. Each material optimization changes the static power dissipation hand-in-hand with $E \times \tau$ improvement due to change in the required supply voltages, and can be within 2 orders of magnitude as compared to HP-CMOS.

In addition to current density issues, the supply voltage level required to produce the minimum switching current *increases* as compared to unscaled PMA magnets due to two reasons: (a) increase in the resistance of the GSHE writer due to decrease in the width and hence the area of cross section of the charge current flow, and (b) reduction of the geometrical gain due to a decrease in the length of the GSHE metal.

However, using high H_k and low $M_s\Omega$ reduce Q_{sw} $(= 2M_s\Omega/\mu_B)$ in the magnet, significantly improving the $E\times\tau$ as shown in fig. 5.2, since $E\times\tau = Q^2R$. On the other hand, the reduction in $E \times \tau$ comes at a cost of increase in the static power (fig. 5.3) due to increased supply voltages, as shown in both red (medium scaled PMA) and blue (high scaled PMA) trajectories.

Increasing the H_k of the magnets could necessitate changing the coupling mechanism between the WRITE and the READ units, since dipolar coupling may not provide strong enough interaction necessary for successful device operation.

Advancements in magnetic oxides [81] can open a pathway for stronger exchange-interaction based coupling of high H_k magnets (fig. 5.1). With use of insulating FM such as Yttrium Iron Garnets (YIG) or ferrites $BiFe_12O_19$ [82] can further simplify the design of the spin switch by eliminating the insulating layer between the READ and the WRITE stages and any leakage currents through them altogether.

However, the thickness of the oxide layer necessary to provide exchange coupling is a critical issues that may interfere with the electrical isolation of the WRITE and the READ units through leakage currents due to tunneling effect, forming a parasitic MTJ between them. Our analysis does not account for such non-idealities in the coupling layer.

Additional issues with such PMA magnets are: (a) reliability issues such as electromigration and thermal breakdown (b) fabricating and creating contacts on highly scaled device could have lithographic challenges.

These practical concerns may require change in the device design of the spin switch and is out of scope for our present study. Our focus here is to show how Modular Approach to Spintronics can be used to project performance enhancement assuming such challenges could be met.

5.3 High Spin-Hall Angle

In the previous optimization we saw that using scaled high H_k PMA magnets can help improve Q_{sw} and the dynamic dissipation by reducing the $M_s\Omega$ of the magnets. However, the scaling down of the magnets causes higher static dissipation due to increased voltage levels required to generate the equivalent amount of spin-torque on the magnet.

Using materials with large spin Hall angles can help in spin switches with scaled PMA magnets by lowering the supply voltage levels necessary for operation, since smaller charge currents in the GSHE can now produce larger spin-current, ultimately producing higher spin-torque. As a result we can obtain either lower static dissipation due to lower $V_{DD;SS}$ for the same dynamic dissipation, or higher speeds (with same $E \times \tau$) obtained through overdrives generated by higher spin-current for the same voltage level, and therefore with same static dissipation as compared to previous optimization.

For projection purposes, we choose a spin-Hall angle of 1 to lower the supply voltages. In both blue (high scaled PMA) and red (medium scaled PMA) trajectories in fig. 5.2 and fig. 5.3, the $E \times \tau$ is reduced by two orders of magnitude and static dissipation is reduced by one order of magnitude due to lower supply voltage levels.

In this simulation we have assumed that the resistance of the GSHE material remains the same, which may not necessarily hold true. In fact it has been suggested that charge resistance of most GSHE materials may increase hand in hand with the Hall angle due to increased back-scattering of the carriers which contributes to high spin-Hall angle equally with intrinsic spin polarization materials in such materials [62], and this may reduce the magnitude of the $E \times \tau$ and static power improvements projected.

To overcome this problem, it might require use of materials like Topological Insulators (TI) with very high channel polarization or the use of composite structures such as an artificial "spin-funnel" that was proposed recently [83].

In the spin-funnel structure, a spin conduction layer is put between the GSHE and the WRITE magnet and this layer acts as a collector of spins from GSHE surface that is not directly underneath the magnet. This collector can then channel this spin collection in to the magnet, which acts a pseudo-ground for the spins. With this structure it may be possible to obtain large spin-Hall angles from small spin-Hall angle materials, though such a layer will add an extra impedance to the spin currents from the GSHE to the magnet due to the spin-funnel layer.

Innovations in advanced materials and device engineering could provide ways to obtain large spin-Hall angles without a large resistance penalty to open a pathway for beneficial integration of high spin-Hall angle materials in spin switches. We have not done detailed simulation of spin switches with these ideas, rather we have only approximately capture the effect of high SHA materials, since our purpose here is to understand the implications of these advances.

5.4 Magneto-Electric Effect

Spin-torque based switching is fundamentally limited by the effective number of spins in a magnet that needs to switched which is given by $Q_{sw} = 2qM_s\Omega/\mu_B$. As we saw in chapter 4, this large Q_{sw} fundamentally limits the efficiency of spin-torque switching. However, it is possible to switch a magnet through mechanisms other than spin-torque.

Multiferroics are a class of materials where two or more "ferro-"phenomena (ferroelectric, ferromagnetic, ferroelastic, ferrotoroidic) exhibit together and are intimately coupled. Spin devices have been proposed that leverage this property of the multiferroics to switch the WRITE magnet using a voltage based mechnaism by concatenating the various ferroic phenomena together. As an example, in compound multiferroics based proposal the mechanism is ferroelectric $\rightarrow$ ferroelastic which reduces the magnet's anisotropy field through distortion of the shape, making it possible to switch with a smaller spin-torque. These compound multiferroics are composed of multiple materials stacked on top of each other (to concatenate ferroic orders) and are still subject to experimental realization.

However, recently it was shown experimentally that $BiFeO_3$ (BFO), a single phase multiferroic is capable of switching an IMA magnet deterministically [17] at room temperature. The mechanism in single phase multiferroics is ferroelectric $\rightarrow$ ferrimagnetism (antiferromagnetic with a residual ferromagnetic order) [84]. The resultant magneto-electric effect enables the application of a voltage controllable ex-

change bias field on the adjacent magnetic layer which can then switch the magnet. Indeed, various device proposals have used this mechanism as part of their device designs [27, 57, 85].

It should be noted that this phenomenon is not the Voltage-Controlled-Magnetic-Anisotropy (VCMA) effect (encountered in chapter 3) where the anisotropy field H_k and consequently the barrier height U of a thin PMA magnet are controlled by applying an electric field. This effect can reduce the barrier height by reducing the anisotropy field strength (H_k) and therefore reduce the minimum threshold current for switching (eq. 5.1). Since this effect does not change the total magnetic moment ($M_s\Omega$) of the magnet, it does not reduce the Q_{sw}. Any decrease in minimum current is compensated by the increase in the delay necessary to switch the magnet ($\tau \propto 1/H_k$).

The switching process using magnet-electric (ME) effect fundamentally requires only $Q_{ME} = C_{ME}V_{ME}$ amount of charge, where C_{ME} is the capacitance of the ME material and V_{ME} is the voltage applied across the ME material. Since the switching mechanism is not spin-torque, it can be much smaller compared to $Q_{sw} = 2qM_s\Omega/\mu_B$, opening a pathway for much more efficient switching.

Additionally, using an ME capacitor instead of GSHE as a WRITER unit in spin switch is also attractive from a device design point of view because it creates a high input impedance device similar to a CMOS inverter and reduces static dissipation. Indeed, it is seen in fig. 5.2 and fig. 5.3 that the green trajectory that replacing the GSHE writer with an ME based writer reduces both $E \times \tau$ and static power drastically.

It should be noted that the ME module used in this work does not consider the ferroelectric polarization caused by the electric field and hence is not a comprehensive model for the multiferroic material. Additionally, the dynamics of the ME based switching was deduced to be a complex 2-step process composed of two partial switchings in two different directions, ultimately causing a full reversal in the experiment [17]. Coupling the LLG with an ME module produces only a single step switching.

Since the detailed physics of multiferroic switching is not fully understood at this time, these projections are subject to change as a better understanding of voltage based multiferroic switching develops. Our purpose here is to simply evaluate the implications of a simple model using Modular Approach to Spintronics.

5.5 Synthetic Ferrimagnets

In the previous optimization, we looked at using alternative physical mechanism for switching the WRITER magnet of the spin switch because of low Q_{sw} necessary for the switching mechanism.

Another way to switch the WRITER magnet while still using the spin-transfer torque is to engineer the magnet itself to consume smaller amount of spins. It was recently proposed [76] that instead of using a single monolithic magnet for WRITER, a stack of composite magnets can be used. In this stack the magnets are strongly coupled anti-ferromagnetically, but their individual magnetic momenta ($M_s\Omega$) are different. As a result the whole stack acts like a ferrimagnet.

Usage of synthetic ferrimagnet (Sy−AFM) stacks instead of monolayer magnets opens up an avenue of performance improvement of the spin-switch. The stability of the stack, coupled with strong exchange interaction, is due to the stability of both the individual magnets ($M_s\Omega_{total} = M_s\Omega_1 + M_s\Omega_2$), however, the effective Q_{sw} is reduced because the magnets are in antiferromagnetic configuration ($Q = 2qM_s\Omega_{eff}/\mu_B$), where ($M_s\Omega_{eff} = M_s\Omega_1 - M_s\Omega_2$). Detailed physics of the effect based on conservation of angular momentum between the spin-current and the magnetic stack and proof of the concept is provided in [76]

In the blue trajectories (high scaled PMA) of fig. 5.2 and fig. 5.3 we use an Sy−AFM stack where $(M_s\Omega_1 - M_s\Omega_2)/(M_s\Omega_1 + M_s\Omega_2) \approx 1/3$. This provides an order of magnitude improvement in $E \times \tau$ alongside a *reduction* of voltage levels by 40% which helps reduce the static power. Optimized designs of Sy−AFM stacks may yield even higher performance gains.

5.6 Heusler Alloy

Till now we have discussed alternatives and optimizations that can help reduce the Q_{sw} and dynamic dissipation, and the static dissipation improvement was a side effect. In chapter 4 we saw that a big component of both static and dynamic dissipation is attributable to the static current flow in the READER unit of the spin switch. One way this static parasitic current can be decreased is by increasing the $R_{OFF} = R_{AP}$ of the MTJs by increasing the junction resistance (R_0) since:

$$R_{AP} = R_0/(1 - P_1 P_2 \hat{m}_1 \cdot \hat{m}_2) \tag{5.4}$$

However, this is counterproductive since any increase in R_0 increases R_P as well and therefore increases the dynamic dissipation since $E \times \tau = Q_{sw}^2 R$ and increase in R_0 causes and increase in overall R of the device. Therefore, it is better to improve the ratio R_{AP}/R_P by increasing the TMR of the MTJS which is given by:

$$TMR = \frac{R_{AP} - R_P}{R_P} = \frac{2P_1P_2}{1 - P_1P_2} \tag{5.5}$$

By increasing the polarizations of the two junctions P_1 and P_2 we can substantially increase the R_{AP}/R_P while keeping the R_P small. In fact it can be seen that as $P_1P_2 \rightarrow 1, TMR \rightarrow \text{inf}$.

Such high polarizations can be obtained through the use of "half metallic magnets" (such as Heusler alloys) in fabrication of MTJ or Spin-Valve based READERs It can be shown from TMR formula (eq. 5.5) that to achieve the same R_{OFF}/R_{ON} ratio as a well-designed CMOS inverter ($\sim 10^5$), the interface polarization that would be required is $P_{1;2} = 0.99999$.

For the sake of performance projection we have chosen an optimistic value of $P = 0.99$ (close to experimentally reported value of $P \approx 0.96$ at low temperatures [86]) which gives $R_{AP}/R_P \approx 100$.

Use of Heusler alloys ($CoMnSi, CoFeAl$ etc.) helps in reducing the static power loss in the reader by reducing the supply voltages $V_{DD;SS}$ and bringing V_{out} closer

to the supply voltages (fig. 5.1). However, the high P of the MTJ reader imposes a upper limit on the overdrive that can be applied to the spin-switch, because the spin-current generated in the MTJ may start switching the device in competition with the GSHE writer, especially in scaled spin-switches where the geometrical gain in GSHE given by $\theta_{SH}L/t(1 - \text{sech}(t/\lambda_{sf}))$ is limited by scalability of GSHE thickness t and spin-flip length λ_{sf} compared to length L [62].

In fig. 5.2 and fig. 5.3 we see the effect of a reduction of both $E \times \tau$ and static power due to Heusler alloy MTJs in both red (medium scaled PMA) and green (ME spin-switch) trajectories.

5.7 Power Gating

The alternatives discussed in the preceding sections to reduce static and dynamic dissipation were materials and device design focused. However, it can be possible to exploit some of the physical properties of spintronics to reduce the dissipation using purely circuit techniques.

One such physical property that we can exploit is the non-volatility of the magnets in the spin switch. It is possible to completely shut off sections of a circuit built using the spin switches during static conditions and not lose any computational states, unlike CMOS where the interconnect lines will get discharged and need powered cache-memory to load back computational states from. In effect we are using the non-volatility of the spin switch to act as a local cache that does not need to be powered and if the magnets with barrier height $U = 40\ k_BT$, these caches have retention time of nearly a decade.

The fig. 5.4 a shows such an example demonstration of a power-gated circuit. In this example the supply rails are turned on periodically using the two driving transistors using the V_{PG} signal that charges them to V_{DD} and V_{SS}. Any WRITE process that happens at the first cycle can be the read off at the next sequence of pulses as can be clearly seen in fig. 5.4 b. In the meantime, even though the circuit

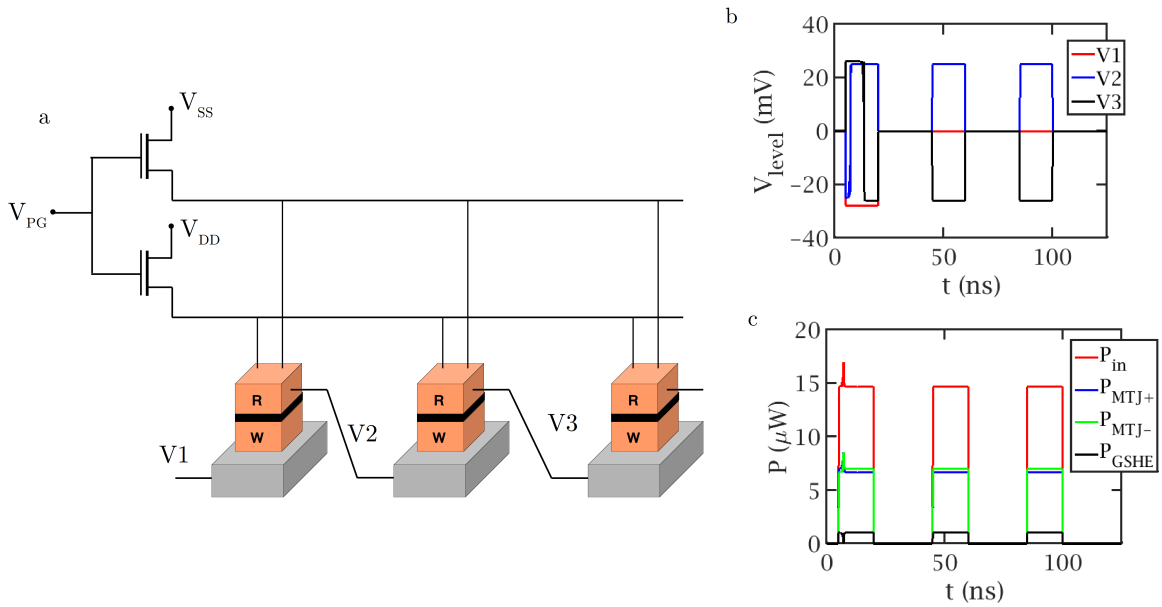


Fig. 5.4. **Power-Gating of Spin Switch Circuits to Reduce Static Dissipation a:** FO-1 logic pipeline with power-gating. **b:** An initial WRITE and two subsequent READs in the power-gated circuit. **c:** Static and Dynamic power dissipation in power-gated circuit.

is completely turned off, the state of the computation is stored as can be seen from fig. 5.4 b,c.

It should be noted that implementing power-gating comes at an increased circuit cost of pulse generator and synchronization. Since the spin switches are level triggered devices, it is tolerant to synchronization errors.

In principle it will be preferable to create a spin switch device through better material and device designs, some of which are illustrated previously, to reduce the static power rather than power-gating. However, it can be a stop-gap solution before those material and fabrication targets are achieved.

In the case of power-gating the static dissipation averaged over a cycle is given by (fig. 5.4 c):

$$S_{avg} = \alpha S_{on} \tag{5.6}$$

Where, S_{avg} is the static power dissipation over a cycle, α is the activity factor or duty cycle, and S_{on} is the static dissipation when the power supply is on. However, there is an increased cost of charging and discharging of supply rails and the power transistors that will be necessary to drive such a pipeline that we have not accounted for here. This scheme will be beneficial in a scenario where the static dissipation in the spin switch is a large enough factor to justify the added complexity and dissipation cost of driving and synchronization circuitry associated with power gating.

5.8 Summary

In this chapter we explored optimized component designs for lower dissipation in spin switch. We used Modular Approach to Spintronics to modify the spin-circuit model of the spin switch to include various alternative materials, phenomena, device designs, and magnetic stack designs and tested their effect of the static and dynamic dissipation of the switch. We found that if integration of these advanced materials and designs are achieved, the spin switch can be made considerably more performant and reach the efficiency of contemporary CMOS technology within an order of magnitude. Though the example device we used here was spin switch, other spintronic devices can be expected to report similar gains when these alternatives are incorporated in their designs.

The next chapter we take a walk up the technology stack and explore the use spin switch not as a mere drop-in replacement for CMOS in logic circuits. We show two circuit applications where spin switch can have an edge over CMOS in implementing logic functions due to its inherent physics of spin transport and magnetics.

6. COMPLEX BOOLEAN AND BEYOND-BOOLEAN CIRCUITS USING SPIN SWITCHES

This chapter is adapted from Samiran Ganguly, Kerem Yunus Camsari, Supriyo Datta, "Evaluating Spintronic Devices Using The Modular Approach" [1]

In this chapter we look at spintronics from a higher perch than individual devices and use Modular Approach to Spintronics to reveal intrinsic advantages spintronics devices have may have in circuit applications. We look at functionalities that are enabled by the inherent physics of spintronic and magnetic devices, which opens up a pathway for compact and efficient computation using spintronics compared to an implementation based on CMOS or other competing technologies.

First we look at majority function and its implementation using spin switch based circuits. We point out the inherent physics that enables implementing this function in a smaller energy footprint as compared to a CMOS based implementation.

Then we look at implementing probabilistic logic using spin switches. We show how deliberately a spin switch can be used as programmable and controllable stochastic signal accumulator and decision circuit element that can have applications in wide ranging class of circuits using a simple proof of concept demonstration. Conversely spintronics may enable bringing this circuit to widespread use in mainstream computing architectures by providing a compact natural hardware implementation.

6.1 Majority Logic

Majority function (MAJ) for n inputs evaluates to 1 or 0 if more than half of them are 1 or 0 respectively. Along with the NOT function it forms a functionally

complete basis set for all Boolean functions [87,88], much like the $\{AND, NOT\}$ and $\{OR, NOT\}$.

A spin switch naturally exhibits the $\{MAJ, NOT\}$ set of functions as we have shown in chapter 3 and will further demonstrate here. Therefore, a spin switch can be used to implement any logic function through functional composition using this set itself, rather than the more commonly employed $\{AND, NOT\}$ and $\{OR, NOT\}$ set which fits the physics of the CMOS inverter better. In this section we use Modular Approach to Spintronics to investigate the physics of spin switch that allows for compact implementation of $\{MAJ, NOT\}$ set of functions using the spin switch.

In fig. 4.3 we showed that critical charge necessary to switch a magnet can be related to the total number of spins $2M_s\Omega/\mu_B$ comprising the magnet, and in the case of ME writer, it is the threshold charge accumulated (eq. 6.1) on the ME capacitor. This charge can be provided through currents coming in from multiple inputs all adding in without any extra circuitry, since it is natural to add currents in metal interconnects unlike adding voltages. This fan-in capability of spintronic devices leads to the realization that MAJ function based logic are a natural domain of spintronics and indeed many proposed devices have demonstrated the MAJ function implementation [25, 89, 90]. It should be noted that Quantum Cellular Automata (QCA) also exhibits the MAJ function naturally.

6.1.1 Majority Function using the Magnetoelectric Spin-Switch

We investigate the physics of a MAJ function implemented using a single ME spin switch and show that this may open the pathway for low dissipation complex logic circuits compared to those built using larger number of basic logic gates implemented through CMOS inverters [91]. Fig. 6.1 a shows a 3 input MAJ function being implemented using an ME spin switch (fig. 6.1 b). The output $V4$ is the output of the MAJ function over the input signals $V1, V2, V3$ as can be seen from the simulation in fig. 6.1 c.

It should be noted that the spin switch actually implements $\overline{MAJ}$ due to its inverting characteristics. Therefore we have implemented the MAJ function using its self-duality property, i.e. $MAJ(a, b, c) = \overline{MAJ(\bar{a}, \bar{b}, \bar{c})}$, where the complement of the inputs are provided from the spin switches on the left of the circuit and the complement of the MAJ in built within the right spin switch.

In the last plot of the fig. 6.1 d we plot the current in to the output switch, and the fig. 6.1 e shows the current zoomed in for the second transition event.

6.1.2 Dissipative Cost of ME-SS Majority Function

It can be shown that the minimum charge necessary to switch the magnet is given by:

$$Q_{sw} = \epsilon_0 \epsilon_r \frac{A_{ME} H_k}{\alpha_{ME}} \tag{6.1}$$

For the chosen parameters the critical charge to switch the output device is $Q_{sw} = 100e^-$. Numerically we find that in the switching window (for either of the switching events): $Q_{ME} = \int I_{ME} dt = \int I_{sw1} dt + \int I_{sw2} dt + \int I_{sw3} dt \approx 190e^-$, which is close to the theoretical limit Q_{sw}. Note: the simulation was preformed at a 30% overdrive for higher switching speeds and this can account for the $Q_{ME} > Q_{sw}$.

This relatively small number for Q_{ME} demonstrates that for the dissipative cost of just one CMOS inverter ($\sim 200\ e^-$ for 14nm FinFET based CMOS in chapter 4), ME spin-switch can implement a MAJ function gate. The ME spin switch based MAJ gate can form the basis of more complex arbitrary logic functions, such as full adders that need a large number of CMOS inverters to implement [92], or neural networks [90]. It should be noted that while we used the ME spin switch in the deomnstration, in principle any other spin switch design can be used since they all have the necessary physics for $\{MAJ, NOT\}$ based logic (see chapter 3).

It should be further noted that the existing toolchain of digital logic synthesis is built using $\{AND, NOT\}$ and $\{OR, NOT\}$ basis functions and generate optimal

circuits based on these functions. The $\{MAJ, NOT\}$ basis function can produce both $\{AND, NOT\}$ or $\{OR, NOT\}$ basis functions with an extra bit as we showed in chapter 3, and the spin switch can behave as a drop-in unit for implementing $\{AND, NOT\}$ and $\{OR, NOT\}$ based logic circuits. However, the extra input necessary with every bit will have additional dissipation and layout issues for large circuits. Therefore, to optimally utilize the spin switch's functionality as a logic unit, $\{MAJ, NOT\}$ based logic synthesis methods and tooling will need to developed.

6.2 Probabilistic Logic

A big thrust of spintronic research is the use of spin devices as ultra-compact *deterministic* nodes of hardware neural networks [93–96] due to their ability to accumulate a large number of input signals and switch at a designed threshold logic level to either "1" or "0" states, in a sharp transition [90]. In this respect, the advantage of using spin-switches primarily lie in their ability to reduce dissipation and simpler circuit design due to reduced hardware cost compared to CMOS based implementations.

In this rest of the chapter we will explore an application of spin switch where thermal noise inherent in the dynamics of magnets with low barrier heights combined with the natural MAJ function like behavior can give rise to new paradigms of computing with spins that goes beyond the Boolean logic.

6.2.1 Stochastic Magnet Dynamics

Our spin-switch designs discussed up to this point have used magnets with $U = 40\ k_BT$ with state retention of nearly a decade. The state retention and barrier height is related by $\tau_r = \tau_0 e^{U/k_BT}$, where $\tau_0 \sim 0.1 - 1$ ns. Even though we have not explicitly included thermal noise in our analysis so far, as noted in [97], when $U/k_BT \gg 1$, there is only a minor effect on the switching dynamics due to thermal agitation, and the switching delay is largely determined by the initial angle of the magnet. We have approximately taken this initial angle variation into consideration

by using mean initial angles that are in consistent with results from equilibrium statistical mechanics [48].

However reducing the barrier height to superparagmagnetic values, for example $U \approx 3\ k_BT$, makes the magnetization stochastic and the statistical average of the magnetization lies between "up" and "down" states. As an example, fig. 6.2 a shows a transient simulation of a magnet with $U = 2.75\ k_BT$ only under the influence of a thermal noise field [98]. The magnetization keeps flipping back and forth between the up and down states, since the state retention time is of the order of $0.2 - 2\ ns$. This stochastic behavior along with spin-torque or magnetic field switching can yield building blocks for probabilistic computers [45,46] where probabilistic behavior comes naturally due to inherent physics of the device itself. Feynman envisioned [99] that probabilistic computers built using probabilistic hardware could efficiently solve problems involving classical probability, through the removed burden of simulating stochasticity on a deterministic computer by time averaging or ensemble averaging, therefore providing enormous parallelism.

6.2.2 Stochastic Spin Switch: Building Block of Probabilistic Networks

Fig. 6.2 b shows a stochastic spin switch operating under room temperature conditions. As explained in the Majority Logic section, the spin switch naturally accumulates multiple input signals at its input node (analogous to synaptic addition in a neuron) and switches.

When this switching happens at a finite temperature, the output of the spin switch instead of being a deterministic function whose output is "0" or "1", instead turns into a stochastic one whose average can be controlled by the input current (blue background curve in fig. 6.2 c). This output when passed through a simple R-C low pass filter circuit ($\tau_{RC} = 225ns$ in the simulation) that extracts the average value produces a transfer function which instead of being a sharp transition, turns into a

sigmoidal function (red foreground curve in fig. 6.2 c), useful for building probabilistic and fuzzy logic circuits [100, 101].

The stochastic regime of operation of the spin-switch and its use as a building block for probablistic networks was first identified in [45], where it was called a *transynapse*. The major distinction between the previous paper and this work is our use of spin switches with in-plane magnets in the superparamagnetic regime [102, 103] and a time-averaged measurement, rather than averaging an ensemble of thermally stable magnets undergoing hard axis switching.

Since the computation with stochastic spin switch is statistical unlike deterministic switching, a direct comparison of performance with another technology is highly implementation dependent and is not attempted here. Our main purpose is to demonstrate the Modular Approach to Spintronics enables the exploration of stochastic spin switches to build novel beyond-Boolean circuits.

6.2.3 Programmable Stochastic Networks

By connecting the stochastic spin switches together we can create novel beyond-Boolean circuits, an example being the Ising network, a computational model that is widely used to solve complex optimization and pattern recognition problems [104–108]. The nodes of the network interact with each other through the charge currents in the GSHE, which can be controlled by either changing the voltage between the nodes (through sign and magnitude) or by using an external CMOS circuitry. The network can then be annealed to its ground state providing a solution of the problem.

While the Ising model in itself is purely deterministic, stochasticity of the superparamagnets helps the system to traverse the configuration space of the network at the speed of the magnet retention time, which could be a few ns or less for superparamagnets.

As an example, fig. 6.3 b,c shows two different solutions mapped in the steady state statistical configuration of the 3-node Ising network (fig. 6.3 a), ferromagnetic

and frustrated spin-glass, obtained by tuning the interaction strength and sign (by changing the supply voltage applied to the devices) between the three nodes.

One way to achieve this is by an external circuitry that implements a weighing logic of the form $V_{in;i} = \sum w_{ij} V_{out;j}$ where $V_{in;i}$ is the input voltage for the ith node, $V_{out;j}$ is the output of the jth node and w_{ij} is the weight logic and the elements of the Ising Hamiltonian for the given problem. In this problem $w_{ii} = 0$ and all positive w_{ij} creates ferromagnetic interaction, whereas all negative w_{ij} creates anti-ferromagnetic interaction. The magnitude of the $w_{ij} = \pm w_o$ is chosen to ensure that the average output of the nodes are in the "saturated" region of the fig. 6.2 c.

If the interactions are tuned to make the chain ferromagnetic, the configuration space obtained after a time averaged measurement is shown in fig. 6.3 b where nodes prefer the 000 or 111 state, i.e. all of the nodes are in the same state. However, for antiferromagnetic interaction, the nodes take up the other 6 possible states equally distributed statistically (fig. 6.3 c), forming a frustrated spin-glass, since the interaction strengths are equal in this simulation.

This proof of concept demonstration points towards a possibility of building larger dynamically programmable stochastic networks (as shown in [46, 47]) that can provide energy efficient hardware that solve both large scale problems of combinational Boolean-logic as well as algorithms of data mining, optimization, searching, and machine learning (Deep Belief Networks) [109] which at present are commercially implemented as software solutions. These stochastic networks map complex and composite logic functions directly into the physics of the spintronics, paving the way of creating ultra-compact and efficient learning networks.

6.3 Summary

In this chapter we used Modular Approach to Spintronics to explore circuit applications of spin switch where the inherent physics of the device brings in new applications and modes of circuit design. We showed how spin switch can form a compact

natural hardware unit for solving problems in optimzation and machine learning due to its ability to accumulate signals and switch stochastically with controllable statistics.

In the next chapter we summarize the work and conclude by examining what future may hold for spintronics.

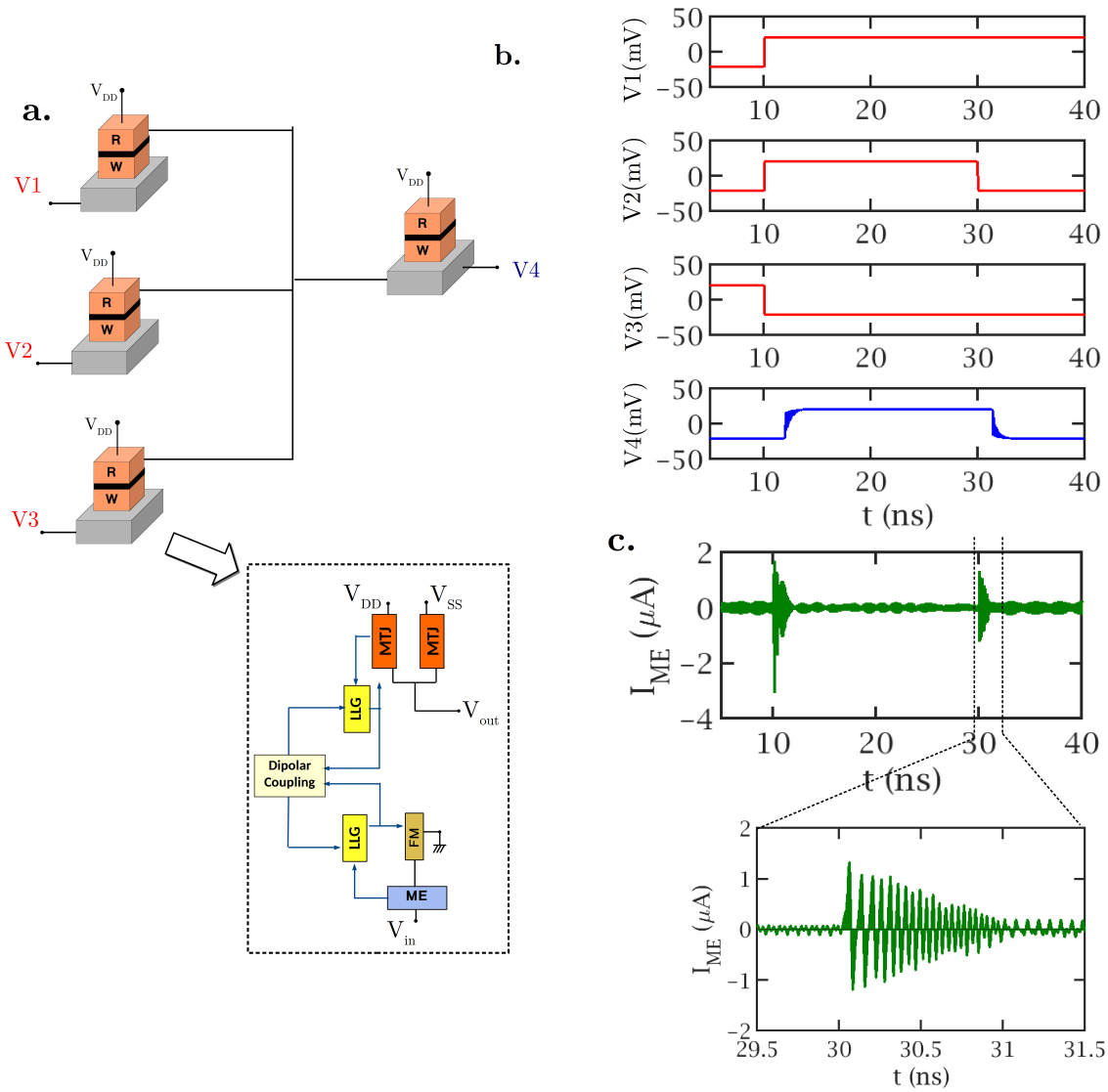


Fig. 6.1. **a. Majority Gate Circuit using Spin Switch:** A 3-input majority logic circuit using the ME Spin-Switch. **b. Demonstration of Majority Function:** A simulation showing the MAJ function realization using ME spin switch based circuits. The output is $V4 = MAJ(V1, V2, V3)$ at steady state of the circuit as evident from the time trace of the inputs $V1, V2, V3$ and the output $V4$. **c. Switching Charge Q_{sw} for ME Spin Switch:** Net input current into the output switch for the second switching event. Integral of the current in the switching window > threshold charge on ME capacitor for switching, and is comparable to a CMOS inverter's Q.

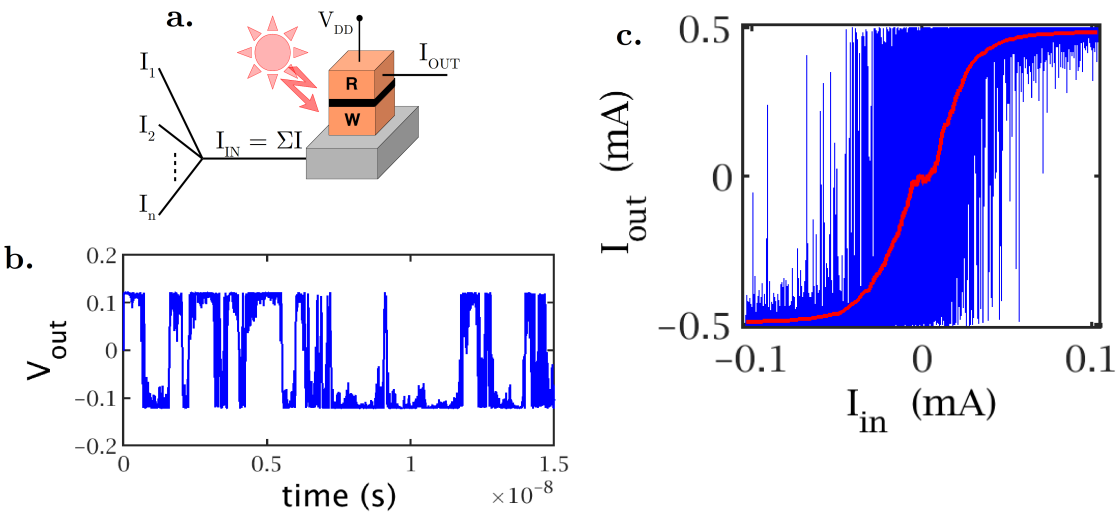


Fig. 6.2. **a. Stochastic Magnet Dynamics:** A low U magnet keeps switching back and forth between "up" and "down" states when interacting with a thermal bath. This fluctuation can be read by looking at the output of the spin switch. **b. Spin-Switch as a Stochastic Circuit Building Block:** Physics of spin-torque switching at the room temperature allows a spin-switch to behave as a building block for stochastic networks. **c. Sigmoidal Transfer Characteristics of Stochastic Spin Switch:** A stochastic simulation showing the sigmoid function like transfer characteristics of the stochastic spin switch (blue background curve) whose mean magnetization can be changed by application of a magnetic field or, in this case, by a spin current. The time averaged mean (red foreground curve) can be obtained by passing the output of the spin switch through a low pass filter.

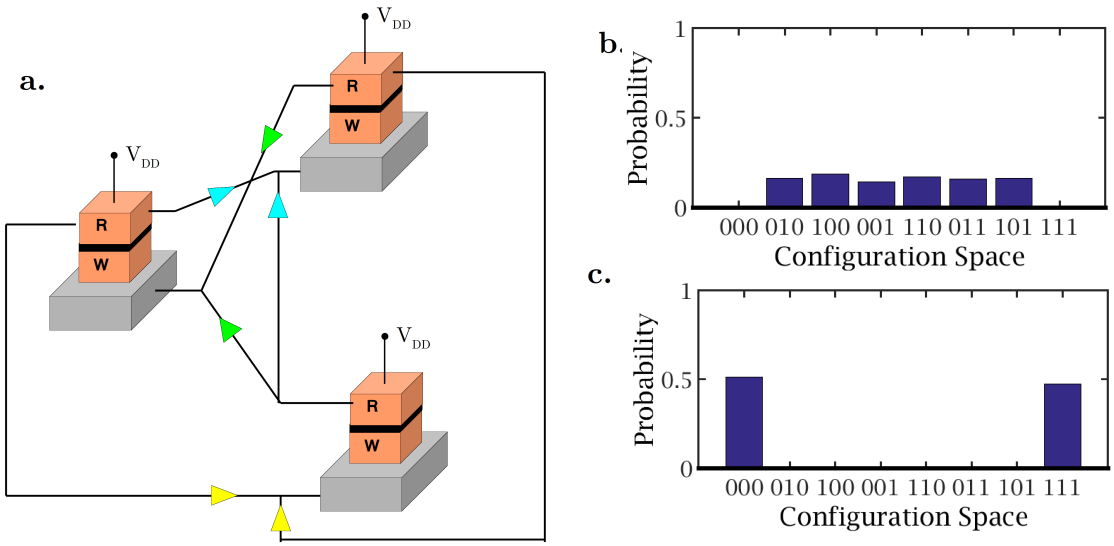


Fig. 6.3. **a. Probabilistic Networks:** A three node Ising network built using the stochastic spin switch. Each node is driven by the other two nodes through the charge currents whose magnitude and sign can be programmed dynamically through supply voltages. **b. Configuration Space – Ferromagnetic:** Statistical sampling of the Ising network programmed for ferromagnetic type interaction shows that the network anneals to FM like states 000 and 111. **c. Configuration Space – Frustrated Spin Glass:** Statistical sampling of the Ising network programmed for anti-ferromagnetic type interaction shows that the network anneals to frustrated spin-glass states.

7. CONCLUSIONS AND THE FUTURE

In this work we have used **Modular Approach to Spintronics** to demonstrate how functional spintronics devices could be modeled in details to evaluate their performance in comparison with existing technologies. We established a framework for analyzing and identifying bottlenecks in the designs of the spintronic devices and explored alternatives based on advanced materials, magnetic stack designs, new physical phenomena, and circuit based techniques. We then looked at simple circuit based examples of application domains where spin switch, and indeed spintronics, can have an advantage over other competing technologies in providing a natural hardware unit due to its inherent physical properties.

Based on the results in this work, we can briefly summarize our conclusions under these headings:

7.1 Outlook for Spintronics as a CMOS Drop-in Replacement

We compared and contrasted the spin switch with a 14nm FinFET based CMOS inverter in a simple circuit testbench to evaluate their performance in terms of static and dynamic dissipation. From the simulations we identified critical metrics and physical factors underlying these two dissipations in any logic switch. We identified the ratio R_{OFF}/R_{ON} of a logic device as the critical physical quantity that decides the static power dissipation. We also identified the minimum required charge for switching Q_{sw} that underlies the dynamic dissipation. Therefore improving a logic device's performance involves scaling up the R_{OFF}/R_{ON} and scaling down Q_{sw}.

Using Modular Approach to Spintronics we went through a host of alternatives in terms of materials and designs that improve the expected performance of the spin switch many orders of magnitude. We found that spin switches can approach the

performance of contemporary scaled FinFET based CMOS if integration of various high performance materials along with careful device engineering and advanced lithographic and fabrication abilities are achieved. Meanwhile CMOS technology in itself is a moving target, considering recent developments such as negative capacitance [110], therefore it is difficult to see how an individual spin device could outperform the CMOS inverter in the near future. Spintronics has enjoyed many breakthroughs in the past decade with new materials and phenomena being discovered, therefore an attitude of cautious optimism may be warranted. Modular Approach to Spintronics due to its ability to integrate these new materials and phenomena in to existing device designs such as the spin switch is a vital tool for such explorations.

7.2 Outlook for Spintronics in Logic Circuits

We saw in chapter 6 that the natural domain of spintronics could be in complex circuits where the inherent physics of a single device can map to a higher order logic function that requires many basic logic gates to implement, as argued in [111]. These devices can then be deployed as compact and efficient computational nodes in complex Boolean and Beyond-Boolean architectures.

We demonstrated the natural ability of spintronics to directly implement majority function which opens up a whole new regime of logic synthesis and circuit design that forms the basis of neuromorphic computing which is of wide ranging interest. It is hoped that spintronics can enable efficient compact nodes for large scale learning networks that will propel a new generation of smart devices.

We also investigated, as a proof-of-concept, the use of superparamagnets in the stochastic regime to show how they can be used to design beyond-Boolean architectures, an example being the Ising network. Spintronic "Ising Computers" can potentially be much more efficient than analogous CMOS implementations due to their natural mapping of the physics of the hardware to the problems at hand. Even though the computation paradigm was entirely different from what is conventionally

discussed in spin-logic proposals, the Modular Approach to Spintronics allowed us to perform systems-level analyses.

We have barely scratched the surface in terms of possibilities for spintronics in circuit applications considering salient features such as non-volatility of spintronic devices did not naturally enter our analysis. Modular Approach to Spintronics advances this research by enabling detailed material-device-circuits-systems codesign and simulation.

7.3 Outlook for Spintronics in Non-Logic Applications

Our goal in this work was to demonstrate the power of Modular Approach to Spintronics in modeling and evaluating the performance of functional spintronic devices. Our focus on the evaluation part was limited to logic devices, through a family of spin switch designs. However, the exploration of spintronics from an engineering perspective should not only be limited to purely logic devices. With the coming age of what is being billed as "Internet of Things" there is a huge market for devices that are low power, high speed, high reliability, and can be scaled down aggressively. These devices are not just limited to logic cells but include memories, sensors, communication, signal processing devices etc. packaged together as a System-on-Chip (SoC).

Solid state spintronic memories have already made a niche for themselves in the storage industry, however, they are facing stiff competition from other non-volatile memories such as RRAM and PCM-RAM. Additionally, spintronic memories face the same problems of static and dynamic dissipation as the logic devices and will benefit from the same component design alternatives we have discussed in chapter 5, meanwhile similar challenges of integration of high performance materials and stacks will have to be overcome. If these challenges are met there is a strong possibility that spintronic memories may replace register-cache-RAM-permanent storage hierarchy into a flat "universal memory" architecture [112], simplifying circuit design and remove

critical bottlenecks of I/O bound operations which limit computing performance, impacting both embedded and mobile devices, as well back-end server performance.

Other possibilities of spintronics are in the fields of oscillators and sensors, that we have not touched in this work, except briefly in chapter 3. These devices are still in the realms of research and can be expected to benefit from material and designs advancements discussed in this work. Modular Approach can play a critical role in advancements of these devices through detailed modeling and evaluation as described in this work. Improved performance of these devices can enable them to find a place in the increasingly important "More-than-Moore" class of devices.

7.4 Parting Words

Overall, we see that there are wide range of possibilities for spintronic devices, riding on a constant wave of materials advancements and discovery of new physical phenomena that the field has enjoyed over past two decades which has advanced it from cryogenic physics experiments to real world commercial devices. There are still challenges that have to be met and Modular Approach to Spintronics, by reliably integrating emerging physics into existing physics at the device, circuit, and systems level, can play a vital role in exploring possibilities of new designs and applications, and guiding research and development that can lead spintronics to be the technology of the future.

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APPENDIX

.1 Device Equations and Operating Points for the Family of Spin Switch Devices

This section is adapted from Samiran Ganguly, Kerem Y. Camsari, Supriyo Datta, "Evaluating Spintronic Devices Using The Modular Approach" [1]

For the spin switch with grounded GSHE layer, the minimum logic voltage level ($V_{1,2,\cdots} = V_{LL}$) and supply voltage levels (V_{DD}, V_{SS}) necessary for switching are given by the following set of equations.

LLG equation for time evolution of magnetization:

$$\frac{1+\alpha_w^2}{\gamma H_{k;w}}\frac{d\hat{m}_w}{d\tau_w} = f_{LLG}(\hat{m}_w, \overrightarrow{h}_{w;tot.}, \overrightarrow{i_s}) \tag{1}$$

$$\frac{1+\alpha_r^2}{\gamma H_{k;r}}\frac{d\hat{m}_r}{d\tau_r} = f_{LLG}(\hat{m}_r, \overrightarrow{h}_{r;tot.}) \tag{2}$$

Here $h_{w;tot.}$ and $h_{r;tot.}$ are the total time varying magnetic field on the write and the read layer FMs of the spin switch. f_{LLG} is the shorthand for the LLG kernel.

Basic fundamental material properties:

$$2U = M_s \Omega H_k \tag{3}$$

$$g_{MTJ;P} = g_{MTJ;0}(1 + P_1 P_2 \hat{M} \cdot \hat{m}_r(t)) \tag{4}$$

$$g_{MTJ;AP} = g_{MTJ;0}(1 - P_1 P_2 \hat{M} \cdot \hat{m}_r(t)) \tag{5}$$

$$g_{GSHE} = \rho_{GSHE}\frac{L_{GSHE}}{W_{GSHE} t_{GSHE}} \tag{6}$$

$$g_{FM-NM} = \Re(g_{\uparrow\downarrow}) A_{FM} \tag{7}$$

$$g_{ME} = \Re(j\omega C_{ME}) \tag{8}$$

Critical spin current for IMA magnet:

$$I_{s;crit} = 4q\alpha U(1 + \frac{2\pi M_s}{H_k}) \tag{9}$$

Critical spin current for PMA magnet:

$$I_{s;crit} = 4qU(\frac{1}{2} - \frac{H_{external}}{\sqrt{2}H_k}) \tag{10}$$

Transport relationship between GSHE charge current and critical spin current for switching the magnet:

$$k_1 = \theta_{sh}\frac{A_{FM}}{W_{GSHE}t_{GSHE}}\frac{\frac{g_{FM-NM}}{g_{GSHE}}}{csch(\frac{t_{GSHE}}{\lambda_{sf}}) + tanh(\frac{t_{GSHE}}{2\lambda_{sf}}) + \frac{g_{FM-NM}}{g_{GSHE}}}g_{GSHE} \tag{11}$$

Voltage divider equation between the READ stage of the spin switch and the next stage (load):

$$k_2 = \frac{g_{MTJ;P} - g_{MTJ;AP}}{g_{MTJ;P} + g_{MTJ;AP} + g_{load}} \tag{12}$$

Relationship between the logic voltage level and the critical spin current:

$$V_{LL} = \frac{I_{s;crit}}{k_1} \tag{13}$$

From the constitutive relationship between the electric and magnetic fields in the ME:

$$\alpha_{ME} = \mu_0\frac{dM}{dE} \tag{14}$$

we can derive the relationship between logic voltage level and critical switching field for ME-FM system in ME spin switch (the threshold switching field of a magnet is $H_{sw} = H_k$, in a monodomain approximation) is :

$$V_{LL} = \frac{H_k t_{ME}}{\alpha_{ME}} \tag{15}$$

Relationship between the logic voltage level and supply voltage levels:

$$V_{DD;SS} = (\pm)\frac{V_{LL}}{k_2} \tag{16}$$

The symbols are noted in parameters section, V_{LL} is the minimum logic voltage level necessary to switch a device and is not necessarily the same as the supply voltages $V_{DD;SS}$. The simulation performed for fig. 4.1 are at near minimal overdrive to be close to the numerically conditions described by the analytical expressions at switching threshold.

The g_{load}, in the device equations stands for the output loading on the device and can be substituted (for a GSHE-SS based FO-1 circuit) with g_{gshe} as a reasonable approximation of the input admittance of the next stage due to the GSHE material. We ignore the spin-Hall magnetoresistance effect (SMR effect) [113] due to the write magnet of the next stage and its dynamics while switching. The SMR effect is automatically incorporated in the numerical spin-circuit model through the GSHE module but does not introduce a significant discrepancy from the above analytical expressions at steady state since it is a second-order effect proportional to $\theta_{SH}^2 \ll 1$. For the ME-SS, at steady state the load is an open circuit, due to charged up ME capacitor.

From the device equations above, it is possible to calculate the minimum operating point currents and voltages for the spin switch. The table below lists these operating points for the devices discussed in section III of the main paper. These points are calculated from the equations above and use the parameters provided in the last section of the appendix.

Device	$I_{s;crit}$ (μA)	V_{LL} (mV)	V_{DD} (mV)
IMA Spin Switch (SS)	401.9	22.7	80
Low H_k PMA SS	235.8	17	55
PMA SS	189.1	42.6	138.2
High H_k Scaled PMA SS	196.7	88.6	287.3
High SHA high H_k PMA SS	196.7	26.6	86.1
SyAFM SS	65.4	8.8	28.7
High SHA PMA SS	189.1	12.8	41.5
Heusler MTJ PMA SS	189.1	12.8	20.7
ME SS	-	13	26.5
Heusler MTJ ME SS	-	13	13.2
High ME SS	-	433.3	442.2

.2 Modular Spintronics Library

Parts of this section are adapted from Kerem Y. Camsari, Samiran Ganguly, Supriyo Datta, "Modular Approach to Spintronics", Scientific Reports, June 2015 [37], and from Samiran Ganguly, Kerem Y. Camsari, Supriyo Datta, "Evaluating Spintronic Devices Using The Modular Approach" [1]

The software codes for the individual modules are available from the project portal and repository at [49].

The basis vector for the 4-components are assumed to be organized in $\{c\ z\ x\ y\}^T$, i.e. the current is given by $\{I_c\ I_z\ I_x\ I_y\}^T$ and the voltages are given by $\{V_c\ V_z\ V_x\ V_y\}^T$.

The modules used in the work are described below.

.2.1 Transport Modules

These modules capture the physics of spin and charge transport through various materials and structure. The modules used in this work are:

Non-Magnet (NM)

$$[G_{se}]^{NM} = \begin{bmatrix} G_c & 0 & 0 & 0 \\ 0 & G_s & 0 & 0 \\ 0 & 0 & G_s & 0 \\ 0 & 0 & 0 & G_s \end{bmatrix} \quad [G_{sh}]^{NM} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & G'_s & 0 & 0 \\ 0 & 0 & G'_s & 0 \\ 0 & 0 & 0 & G'_s \end{bmatrix} \tag{17}$$

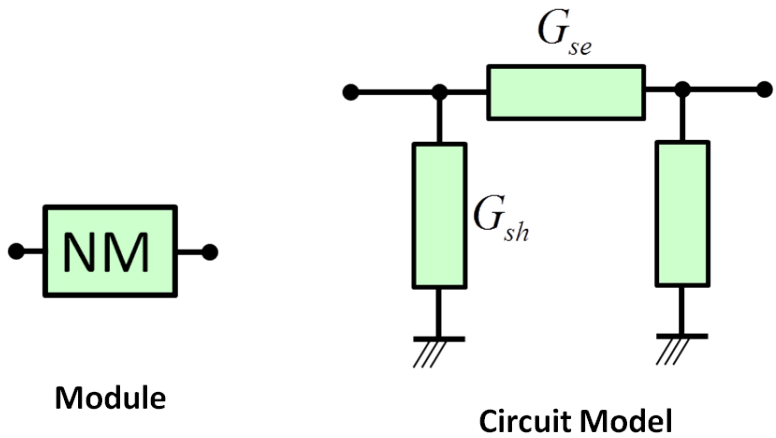

Fig. 1. Circuit model for Non-Magnetic module

where $G_c = A/(\rho L)$ $\quad G_s = A/(\rho\lambda)\text{csch}(L/\lambda)$ $\quad G'_s = A/(\rho\lambda)\tanh(L/2\lambda)$.

Parameter	**Symbol**	**Units**
Length	L	m
Area	A	m^2
Resistivity	ρ	$\Omega - m$
Spin-flip Length	λ	m

Ferromagnet (FM)

$$[G_{se}]^{FM} = G_c \begin{bmatrix} 1 & P & 0 & 0 \\ P & \alpha & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \quad [G_{sh}]^{FM} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & G_s & 0 & 0 \\ 0 & 0 & G'_s & 0 \\ 0 & 0 & 0 & G'_s \end{bmatrix} \tag{18}$$

$G_c = A/(\rho L)$ $\quad G_s = A/(\rho L)(1-P^2)L/\lambda \tanh(L/2\,\lambda)$ $\quad G'_s = A/(\rho L)L/\lambda' \tanh(L/2\lambda')$

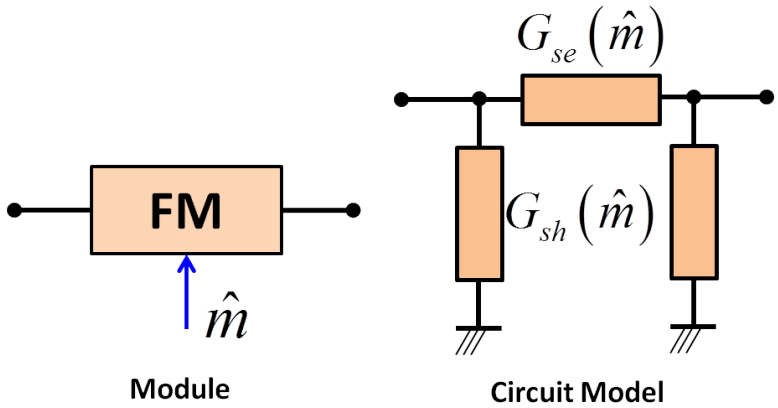

Fig. 2. Circuit model for Ferromagnet module

Parameter	**Symbol**	**Units**
Length	L	m
Area	A	m^2
Resistivity	ρ	$\Omega - m$
Polarization	p	-
Longitudinal Spin-flip Length	λ	m
Transverse Spin-flip Length	λ'	m

FM−NM Interface

$$[G_{se}]^{FM-NM} = (G_0)\begin{bmatrix} 1 & P & 0 & 0 \\ P & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \quad [G_{sh}]^{FM-NM} = (G_0)\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & a & b \\ 0 & 0 & -b & a \end{bmatrix} \tag{19}$$

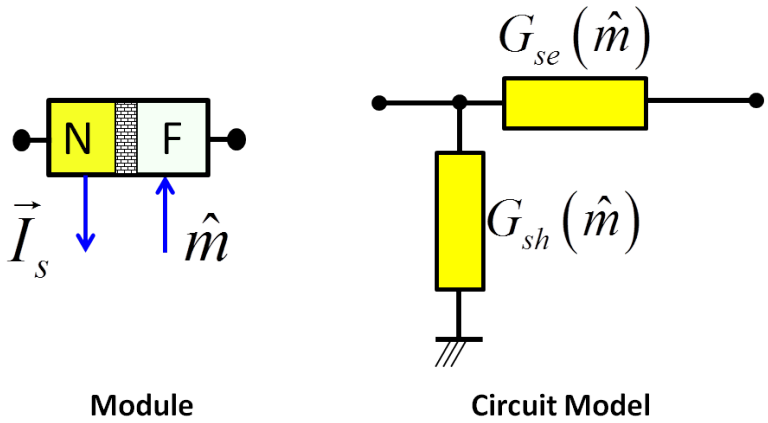

Fig. 3. Circuit model for FM-NM module

Parameter	Symbol	Units
Conductance	G_0	S
Polarization	p	-
In-plane torque coeff.	a	-
Out-of-plane torque coeff.	b	-

Giant Spin Hall Effect (GSHE)

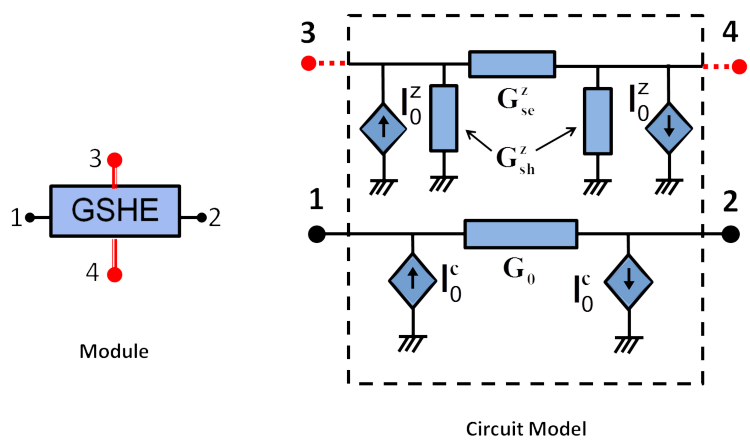

Fig. 4. Circuit model for GSHE module

$$G_{se}^{z} = \sigma \frac{LW}{\lambda} \tanh(\frac{t}{2\lambda}) \quad G_{sh}^{z} = \sigma \frac{LW}{\lambda} \mathrm{csch}(\frac{t}{\lambda}) \tag{20}$$

$$I_0^z = \beta G_0 (V_1^c - V_2^c) \tag{21}$$

$$G_0 = \sigma \frac{tW}{L} \quad \beta = \theta_{SH} \frac{L}{t} \tag{22}$$

$$I_0^c = \beta G_0 (V_z^c - V_4^z) \tag{23}$$

Parameter	**Symbol**	**Units**
Spin Hall angle	θ	-
Length	L	m
Width	W	m
Resistivity	ρ	$\Omega - m$
Thickness	t	m
Spin-flip Length	λ	m

Magnetic Tunnel Junction (MTJ)

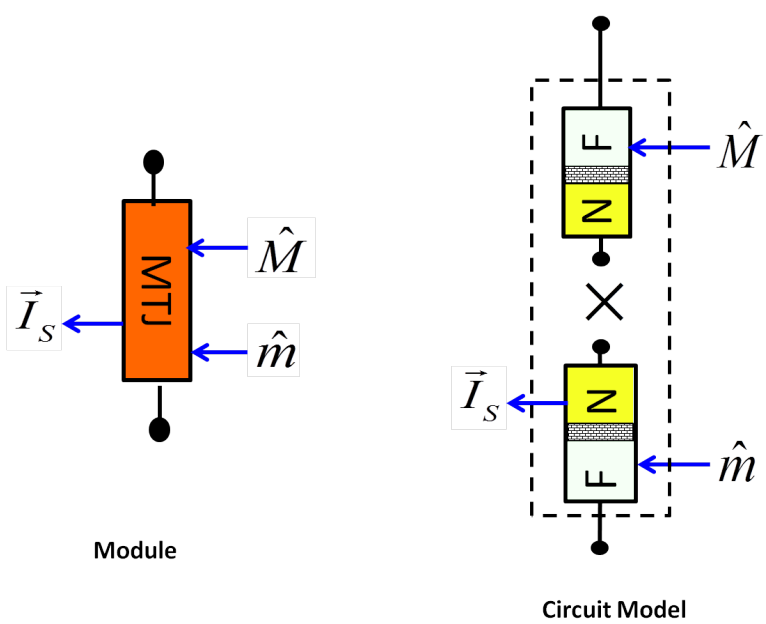

Fig. 5. Circuit model for MTJ module

The MTJ model that is used in this paper is based on a physics-based compact model [56]. The current in the spacer reads:

$$\begin{pmatrix} I_1 \\ I_2 \end{pmatrix} = \begin{bmatrix} G_{21} & -G_{12} \\ -G_{21} & G_{12} \end{bmatrix} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} \tag{24}$$

$$G_{21}^{MTJ} = \left[\begin{array}{c|c} & c \\ \hline c & 1 + P_M P_m \cos(\theta) \\ \hat{M} & P_M \\ \hat{m} & P_m \\ \hat{m} \times \hat{M} & P_m(b) \end{array}\right] \tag{25}$$

$$G_{12}^{MTJ} = \left[\begin{array}{c|c} & c \\ \hline c & 1 + P_M P_m \cos(\theta) \\ \hat{M} & P_M \\ \hat{m} & P_m \\ \hat{m} \times \hat{M} & -P_m(b) \end{array}\right] \tag{26}$$

Parameter	**Symbol**	**Units**
Conductance	G_0	S
Polarization of fixed layer	p_M	-
Polarization of free layer	p_m	-
In-plane torque coeff.	$a = 1$	-
Out-of-plane torque coeff.	b	-

The modules not covered here are: Rashba Spin-Orbit (RSO), Topological Insulator (TI), Spin Pumping

.2.2 Magnetics Modules

These modules capture the physics of spin and charge transport through various materials and structure. The modules used in this work are:

Landau-Lifshitz-Gilbert Equation Solver (LLG)

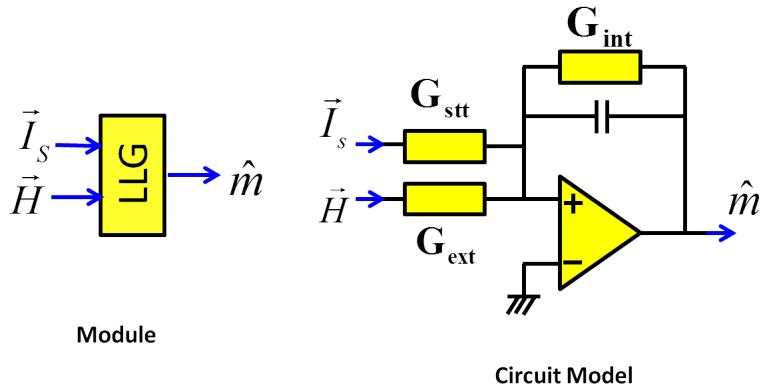

Fig. 6. Circuit model for LLG module

LLG equation in normalized units is given by:

$$\left(\frac{1+\alpha^2}{\gamma H_k}\right)\frac{d\hat{m}}{dt} = -\hat{m}\times\vec{h} - \alpha\ \hat{m}\times\hat{m}\times\vec{h} - \hat{m}\times\hat{m}\times\vec{i_s} + \alpha\ \hat{m}\times\vec{i_s} \tag{27}$$

In our method, LLG equation is solved by an opamp based integrator circuit as shown in the figure.

At the + node of the opamp the nodal equation is given by:

$$C\frac{d\hat{m}}{dt} = G_{int}\ \hat{m} + G_{ext}\vec{H}_{ext} + G_{stt}\vec{i_s} \tag{28}$$

Since the nodal equation has the same form as the LLG, the voltage appearing at the output of the opamp is the solution of the LLG equation. The internal/self magnetic field is constructed from the output of the opamp as a feedback using the matrix relation given below:

$$\begin{Bmatrix} \vec{H}_x \\ \vec{H}_y \\ \vec{H}_z \end{Bmatrix}_{int} = \begin{bmatrix} K_x & 0 & 0 \\ 0 & K_y & 0 \\ 0 & 0 & K_z \end{bmatrix} \begin{Bmatrix} \hat{m}_x \\ \hat{m}_y \\ \hat{m}_z \end{Bmatrix} \tag{29}$$

The vector products appearing on the RHS of the LLG equation are carried out by the 3×3 conductance matrices which can be viewed as operators acting on the magnetic field and spin torque current. These are given as:

$$G_{int} = X(1+\alpha X)\frac{K_{int}}{H_k} \quad G_{stt} = X(X+\alpha)\frac{1}{qN_sH_k} \quad G_{ext} = X(1+\alpha X)\frac{1}{H_k} \tag{30}$$

where X is the cross product operator with $\hat{m}$:

$$X = \begin{bmatrix} 0 & -m_z & m_y \\ m_z & 0 & -m_x \\ -m_y & m_x & 0 \end{bmatrix} \tag{31}$$

Stochastic LLG

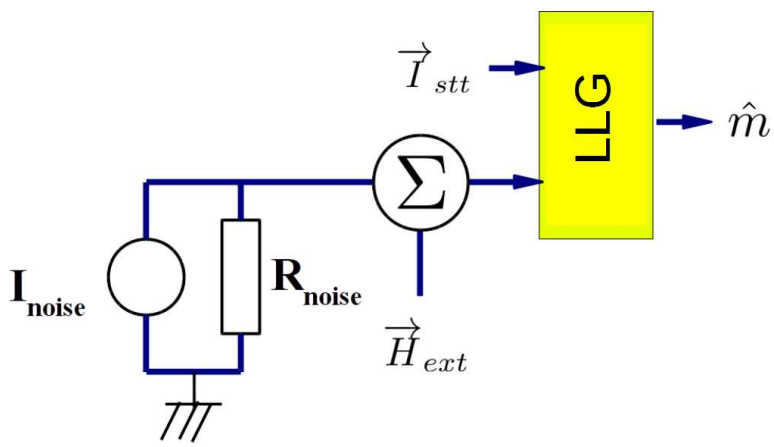

Fig. 7. Circuit model for LLG module

This is a generalized LLG solver that can incorporate the effect of the thermal noise during the time evolution of the magnetization vector. The noise is incorporated using the built-in machinery of SPICE for solving the thermal noise in resistors. The noise field is generated by a noisy current source and a resistor of scaled valued. The voltage generated by this source is then applied as an extra magnetic field to the core LLG solver covered earlier.

$$R_{noise} = \frac{\gamma M_s \Omega}{2\alpha} \tag{32}$$

For details on the scaling of the noise source and its implementation see [49].

Voltage Controlled Magnetic Anisotropy (VCMA)

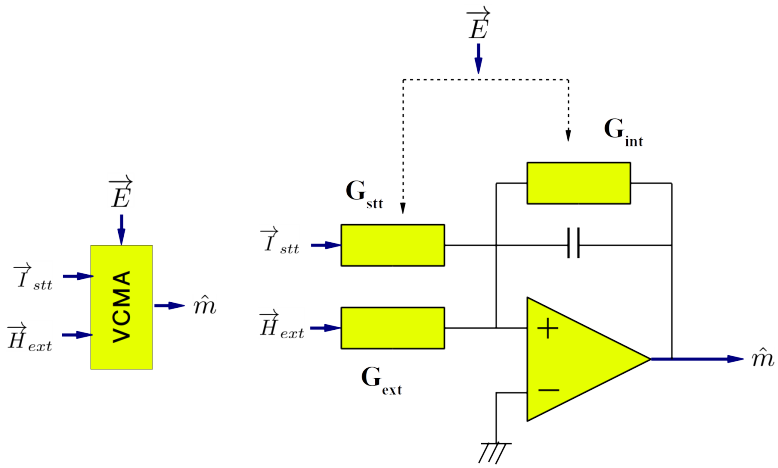

Fig. 8. Circuit model for LLG module

This LLG solver incorporates the VCMA effect by changing the internal anisotropy field strength. Unlike the ME effect, this cannot be supplied as an external field since the variation in the anisotropy field strength changes the solution intimately by changing the normalizing factors and the time scale of the LLG solver. This effect is therefore incorporated through an extra input that provides the electrical field information to the LLG solver which then handles the dynamic update of the anisotropy field strength.

$$H_k(t) = H_{k;0} - \eta E(t) \tag{33}$$

where $E(t)$ is the instantaneous (at time t) electric field applied on the magnet and η is the VCMA effect strength.

For further details on the implementation please see [49]. This module can incorporate thermal effects as well if the thermal noise source is included in the circuit model for the device.

Magneto-Electric Effect (ME)

The magneto-electric effect is given by:

$$\alpha_{ME} = \mu_0 \frac{dM}{dE} \tag{34}$$

$B = \mu_0 M$. Therefore,

$$B_{ME} = \alpha_{ME} E_{ME} \tag{35}$$

where $E_{ME} = V_{ME}/t_{ME}$ is the electric field on the multi-ferroic material, B_{ME} is the generated exchange field on an adjacent magnetic layer, and α_{ME} is the empirically measured coefficient for the effect.

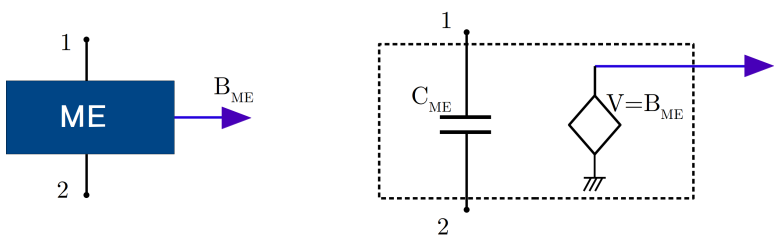

Fig. 9. Circuit model for Magneto-Electric module

The effect is modeled as a parallel plate capacitor and a controlled voltage source whose strength is the magnetic field produced by the ME.

Parameter	**Symbol**	**Units**
Area	A_{ME}	m^2
Thickness	t_{ME}	m
ME Coefficient	α_{ME}	s/m
Relative Permittivity	ϵ_r	$-$

Magnetic Coupling

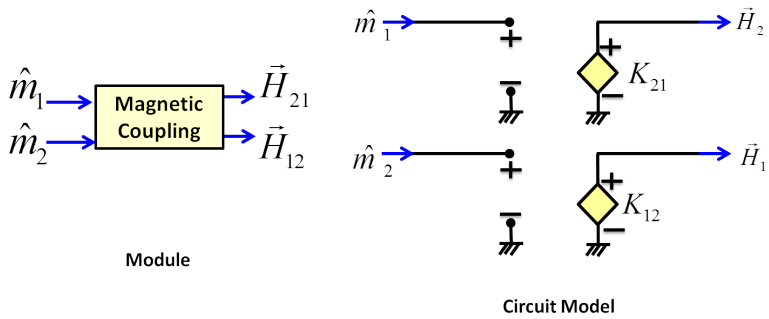

Fig. 10. Circuit model for Magnetic Coupling module

The magnetic coupling between two magnets 1 and 2 are given by:

$$\begin{Bmatrix} H_x \\ H_y \\ H_z \end{Bmatrix}_j = \begin{bmatrix} K_{xx} & K_{xy} & K_{xz} \\ K_{yx} & K_{yy} & K_{yz} \\ K_{zx} & K_{zy} & K_{zz} \end{bmatrix}_{ji} \begin{Bmatrix} m_x \\ m_y \\ m_z \end{Bmatrix} \tag{36}$$

These coefficients can be adjusted to generate a magnetic interaction of certain type, e.g. dipolar, exchange etc. These coefficients can be precomputed for a given geometry using magneto-static equations (Maxwell's equations).

These coefficients are provided as parameters to the modules whose inputs are the magnetization of the two magnets and output are the magnetic fields between the two magnets, implemented using two VCVS as shown in the circuit diagram.

Parameter	**Symbol**	**Units**
Coupling matrix between 1 and 2	K_{12}	Oe
Coupling matrix between 2 and 1	K_{21}	Oe

.3 Software Codes

This appendix contains the software code for spin-circuit models and testbenches that can be used and modified to generate the results in this work.

The recommended software setup for these simulations are:

- HSPICE circuit simulator (v.2012 or later)
- MATLAB
- HSPICE-toolbox for MATLAB
- ASU Predictive Technology Models
- Modular Spintronics Library

It is possible to run most of these examples using a free SPICE simulator, such as ngspice, though it may not be possible to run a few advance analyses, e.g. Transient Noise (*.trannoise*), in a free/open-source version. MATLAB has been used for post-processing and plotting of the data due to its built-in capabilities, even though it is possible to directly use use SPICE to obtain many of these results. It is also possible to use free and open-source software such as Octave (along with gnuplot or fltk) or Python (along with NumPy, SciPy and matplotlib or ggplot2) as a MATLAB replacement.

.3.1 Circuit Model and Testbench for CMOS Inverter

Following are the circuit model for the CMOS inverter built from the PTM models. It is assumed that the PTM models are installed and available.

CMOS Model

```
***CMOS Invertor, Driver/Access Transistor and MOS Capacitor
    Models***
*Using 14nm ASU Perdictive model
```

```
.lib '~/PTM-MG/modeldir/models' ptm14hp
*.lib '~/PTM-MG/modeldir/models' ptm14lstp
.lib '~/PTM-MG/modeldir/param.inc' 14nm

.subckt CMOSINV in out dd ss

** The MOSFETs
Xnmos   out in2 ss 0 nfet
Xpmos   out in1 dd 0 pfet

** Probes for metrology
Vnmos   in in2 0
Vpmos   in in1 0

.ends

.subckt NMOSDRV src gt drn

** A MOS based driver transistor
Xnmos   src gt drn 0 nfet

.ends

.subckt NMOSCAP p n rsd = 100M

** An NMOS based CAP. Can adjust Rsd
Xcap    src p drn n nfet
Rsrc    src 0 'rsd'
```

```
Rdrn     drn 0 'rsd'

.ends

.subckt PMOSCAP p n rsd = 100M

** A PMOS based CAP. Can adjust Rsd
Xcap     src p drn n pfet
Rsrc     src 0 'rsd'
Rdrn     drn 0 'rsd

.ends
```

FO-1 Testbench

```
 ***** FO1 Invertor testbench*********
************************************

.include '/path/to/cmosinvertor.sp'

**** testbench

.param vdrv=0.5
.param vdd=0.5

**The driver invertor
Xdriver drvin intmdt1 dd 0 CMOSINV

**The subsequent fanouts
Xout1    intmdt out1 dd 0 CMOSINV
```

```
Xout2    out1 out2 dd 0 CMOSINV

**Read off the final output stage
Xload1   out1 0 NMOSCAP
 M=2

**Voltage drivers
Vdd1     dd 0 vdd

Vin drvin 0 pulse vdrv 0 20p 5p 5p 50p 200p

**simulation

.option post captab
.option runlvl = 6
*.dc vdrv 0 0.9 0.01
.tran 0.01p 100p
.probe v(*) i(*)
.end
```

.3.2 Spin-Circuit Models for Spin Switches

Following are the spin-circuit models for the spin-switches used in this work:

IMA Spin Switch

```
 *****GSHE based SS*****

.include 'G_FM_NM.sp'
.include 'LLG.sp'
```

```
.include 'G_GSHE.sp'
.include 'G_Fixed.sp'
.include 'Magnetic_Coupling.sp'

**Spin Switch Model
.subckt GSHE_SS w_in r_out r_inp r_inn

.param pi='acos(-1)'

** Dual Reader MTJs - defined in G_Fixed.sp
* G0 is the MTJ conductance when magnets are orthogonal (z
    and x)
* P is the Polarization of interfaces from low TMR data.
XMTJ r_inp r_inn r_out thetaR phiR IszR IsxR IsyR G_Fixed
+ G0='1e-3' P='0.7'

*The two magnets
XLLGW HWx HWy HWz IsxW IsyW IszW thetaW phiW LLG_C
+ alpha='0.01' Hk='130' Area='80e-9*100e-9' tfm='2e-9' Ms='
    800' ima='1'

XLLGR HRx HRy HRz IsxR IsyR IszR thetaR phiR LLG_C
+ alpha='0.01' Hk='130' Area='80e-9*100e-9' tfm='2e-9' Ms='
    800' ima='1'

*The Magnetic Coupling
XMagneticCoupling mxR myR mzR mxW myW mzW HRx HRy HRz HWx HWy
    HWz
Magnetic_Coupling
```

```
+ MsR='800' VolR='80e-9*100e-9*2e-9'
+ MsW='800' VolW='80e-9*100e-9*2e-9'
+ dyy='-0.203' dxx='0.296' dzz='-0.093' dxy='0' dxz='0' dyz='
    0'

*FM|NM Interface for the write FM
XWriteLayer 3c 4c 0 7z 0 7x 0 7y thetaW phiW IsxW IsyW IszW
    G_FM_NM
+ g='5e15*(80*100*1e-18)' a='1' b='0' P='0.7'

*GSHE layer for write
XGSHE w_in 0 3z 0 3x 0 3y 0 G_GSHE
+ theta='-0.3' L='80*1e-9' W='100*1e-9' t='2*1e-9' rho='170*1
    e-8' lsf='2*1e-9'

*For metrology
VGSHEz 7z 3z 0
VGSHEx 7x 3x 0
VGSHEy 7y 3y 0

*Conversion between LLG's spherical to Magnetic Coupling's
    rectilinear
EX1 mxW 0 vol='sin(v(thetaW))*cos(v(phiW))'
EY1 myW 0 vol='sin(v(thetaW))*sin(v(phiW))'
EZ1 mzW 0 vol='cos(v(thetaW))'
EX2 mxR 0 vol='sin(v(thetaR))*cos(v(phiR))'
EY2 myR 0 vol='sin(v(thetaR))*sin(v(phiR))'
EZ2 mzR 0 vol='cos(v(thetaR))'
.ends
```

```
**An equivalent Spin Switch Load
.subckt GSHE_LOAD p n
XGSHE n p 0 0 0 0 0 0 G_GSHE
+ theta='0' L='80*1e-9' W='100*1e-9' t='2*1e-9' rho='170*1e-8
    ' lsf='2*1e-9'
.ends
```

PMA Spin Switch

```
 *****GSHE based SS*****

.include 'G_FM_NM.sp'
.include 'LLG.sp'
.include 'G_GSHE.sp'
.include 'G_Fixed.sp'
.include 'Magnetic_Coupling.sp'

.subckt GSHE_SS w_in r_out r_inp r_inn
.param pi='acos(-1)'

* MTJ
* G0 is the MTJ conductance when magnets are orthogonal (z
    and x)
* P is the Polarization of interfaces from low TMR data.
XMTJ r_inn r_inp r_out thetaR phiR IszR IsxR IsyR G_Fixed
+ G0='1e-3' P='0.99'

* Two LLGs
XLLGW HWx HWy HWz IsxW IsyW IszW thetaW phiW LLG_C
```

```
+ alpha='0.1' Hk='2500' Area='pi*16e-9*16e-9' tfm='2e-9' Ms='
    400' ima='0'
XLLGR HRx HRy HRz IsxR IsyR IszR thetaR phiR LLG_C
+ alpha='0.1' Hk='2500' Area='pi*16e-9*16e-9' tfm='2e-9' Ms='
    400' ima='0'

*Exchange Coupling
XMagneticCoupling mxR myR mzR mxW myW mzW HR1x HR1y HR1z HW1x
    HW1y HW1z
Exchange_Coupling
+ Ms1='400' Vol1='pi*16e-9*16e-9*2e-9'
+ Ms2='400' Vol2='pi*16e-9*16e-9*2e-9'
+ Jex='2.6e6'

*FM|NM Interface
XWriteLayer 3c 4c 0 7z 0 7x 0 7y thetaW phiW IsxW IsyW IszW
    G_FM_NM
+g='5e15*(pi*16*16*1e-18)' a='1' b='0' P='0.7'

*GSHE Layer - spin current is in the "orthogonal direction"
XGSHE w_in 0 3z 0 3x 0 3y 0 G_GSHE
* theta='-1*pi/4' L='32*1e-9' W='32*1e-9' t='2*1e-9' rho
    ='170*1e-8' lsf='2*1e-9'
sx=0 sy=1 sz=0

*For metrology
VGSHEz 7z 3z 0
VGSHEx 7x 3x 0
VGSHEy 7y 3y 0
```

```
*Conversion from spherical to rectilinear
EX1 mXW 0 vol='sin(v(thetaW))*cos(v(phiW))'
EY1 mYW 0 vol='sin(v(thetaW))*sin(v(phiW))'
EZ1 mZW 0 vol='cos(v(thetaW))'
EX2 mXR 0 vol='sin(v(thetaR))*cos(v(phiR))'
EY2 mYR 0 vol='sin(v(thetaR))*sin(v(phiR))'
EZ2 mZR 0 vol='cos(v(thetaR))'

*Add bias H field for switching
Ehwx HWx 0 vol='v(HW1x) + 30'
Ehwy HWy 0 vol='v(HW1y)'
Ehwz HWz 0 vol='v(HW1z)'
Ehrx HRx 0 vol='v(HR1x) + 30'
Ehry HRy 0 vol='v(HR1y)'
Ehrz HRz 0 vol='v(HR1z)'
.ends
```

PMA Spin Switch with Sy-FM

```
 *****GSHE based SS

.include 'G_FM_NM.sp'
.include 'LLG.sp'
.include 'G_GSHE.sp'
.include 'G_Fixed.sp'
.include 'Magnetic_Coupling.sp'

.subckt GSHE_SS w_in r_out r_inp r_inn
.param pi='acos(-1)'
```

```
*MTJ
* G0 is the MTJ conductance when magnets are orthogonal (z
    and x)
* P is the Polarization of interfaces from low TMR data.
XMTJ r_inn r_inp r_out thetaR phiR IszR IsxR IsyR G_Fixed
+ G0='1e-1' P='0.99'

*Write Assist Layer LLG
XLLGWA HWAx HWAy HWAz IsxW IsyW IszW thetaWA phiWA LLG_C
+ alpha='0.1' Hk='10100' Area='pi*8e-9*8e-9' tfm='1.2e-9' Ms=
    '400' ima='0'
*Write Free Layer LLG
XLLGWF HWFx HWFy HWFz IsxW IsyW IszW thetaWF phiWF LLG_C
+ alpha='0.1' Hk='10100' Area='pi*8e-9*8e-9' tfm='0.8e-9' Ms=
    '400' ima='0'
*Read LLG
XLLGR HRx HRy HRz IsxR IsyR IszR thetaR phiR LLG_C
+ alpha='0.1' Hk='10100' Area='pi*8e-9*8e-9' tfm='2e-9' Ms='
    400' ima='0'

*Magnetic Coupling W+R
XMagneticCoupling mxR myR mzR mxWF myWF mzWF HR1x HR1y HR1z
    HW1fx HW1fy HW1fz
Exchange_Coupling
+ Ms1='400' Vol1='pi*8e-9*8e-9*0.8e-9'
+ Ms2='400' Vol2='pi*8e-9*8e-9*2e-9'
+ Jex='2.6e6'
```

```
*Magnetic Coupling A+F
XExCoup mxWF myWF mzWF mxWA myWA mzWA HW2fx HW2fy HW2fz HW1ax
    HW1ay HW1az
Exchange_Coupling
+ Ms1='400' Vol1='pi*8e-9*8e-9*0.8e-9'
+ Ms2='400' Vol2='pi*8e-9*8e-9*1.2e-9'
+ Jex='2.6e6'

*FM|NM Layer
XWriteLayer 3c 4c 0 7z 0 7x 0 7y thetaWA phiWA IsxW IsyW IszW
    G_FM_NM
+ g='5e15*(pi*8*8*1e-18)' a='1' b='0' P='0.7'
XGSHE w_in 0 3z 0 3x 0 3y 0 G_GSHE
+ theta='-1*pi/4' L='16*1e-9' W='16*1e-9' t='2*1e-9' rho='
   170*1e-8' lsf='2*1e-9'
sx=0 sy=1 sz=0

*Matrology
VGSHEz 7z 3z 0
VGSHEx 7x 3x 0
VGSHEy 7y 3y 0

*Conversion Spherical to Rectilinear
EX1F mXWF 0 vol='sin(v(thetaWF))*cos(v(phiWF))'
EY1F mYWF 0 vol='sin(v(thetaWF))*sin(v(phiWF))'
EZ1F mZWF 0 vol='cos(v(thetaWF))'
EX1A mXWA 0 vol='sin(v(thetaWA))*cos(v(phiWA))'
EY1A mYWA 0 vol='sin(v(thetaWA))*sin(v(phiWA))'
EZ1A mZWA 0 vol='cos(v(thetaWA))'
```

```
EX2 mXR 0 vol='sin(v(thetaR))*cos(v(phiR))'
EY2 mYR 0 vol='sin(v(thetaR))*sin(v(phiR))'
EZ2 mZR 0 vol='cos(v(thetaR))'

*bias H field
Ehwxf HWFx 0 vol='v(HW1fx) + v(HW2fx)  + 30'
Ehwyf HWFy 0 vol='v(HW1fy) + v(HW2fy)'
Ehwzf HWFz 0 vol='v(HW1fz) + v(HW2fz)'
Ehwxa HWAx 0 vol='v(HW1ax) + 30'
Ehwya HWAy 0 vol='v(HW1ay)'
Ehwza HWAz 0 vol='v(HW1az)'
Ehrx HRx 0 vol='v(HR1x) + 30'
Ehry HRy 0 vol='v(HR1y)'
Ehrz HRz 0 vol='v(HR1z)'
.ends
```

ME Spin Switch

```
 *****MESO Model*****

.include 'LLG.sp'
.include 'G_Fixed.sp'
.include 'magnetoelectric.sp'

** MESO Module - Simple Model

.subckt MESO_INVERTER win rinp rinn rout
+ Ms = 800 alpha = 0.01 Hk = 1200 Lfm = 15e-9 Wfm = 60e-9 tfm
    = 4e-9
```

```
+ alpha_me = 3e-8 Lme = 15e-9 Wme = 60e-9 tme = 5e-9 eps =
    500
+ gmtj = 1e-3  pmtj = 1

.param pi='acos(-1)'

** The Reader Side is Supply -> Dual MTJ -> output

XMTJ rinn rinp rout theta phi sx sy sz G_Fixed
+ G0 = 'gmtj' P = 'pmtj'

** Writer side is the LLG + controlled field from the ME
    Capacitor

* LLG for magnet's switching dynamics
XLLG hx hy hz sx sy sz theta phi LLG_C
+ alpha = 'alpha' Hk = 'Hk' Area = 'Lfm*Wfm' tfm = 'tfm' Ms =
     'Ms' ima='1'

* ME Capacitor: controlled exchange field
XME win 0 hx hy hz ME_CAP
+ Area = 'Lme*Wme' tins = 'tme' eps = 'eps' alpha_me = '
    alpha_me'

*** Extended FM- See Intel paper ckt diagram
*Rfm c0 c1 0.5k

.ends
```

.3.3 MESH Oscillator Model

Following is the MESH OScillator spin-circuit model along with the testbench and simulation setup.

```
*************Magnetoelectric Spin-Hall Oscillator
    ************


.include 'LLG_CI.sp'
.include 'G_MTJ.sp'
.include 'magnetoelectric.sp'
.include 'G_GSHE.sp'
.include 'G_FM_NM.sp'

.param pi = 3.14159
.param alpha = 0.01
.param Ms = 800
.param Hk = 500
.param Volume = '80*20*2e-21'
.param gmix = 1e15
.param Rmtj = 5k
.param Pmtj = 0.7
.param thetash = 0.3
.param Lgshe = 20n
.param Wgshe = 30n
.param tgshe = 2n
.param lsfgshe = 1.5n
.param rhogshe = 170e-8
.param Lme = 80n
```

```
.param Wme = 20n
.param tme = 10n
.param epsme = 500
.param alphame = 1e-8

** Circuit Model
*MTJ Reader
XMTJ out 0 theta phi mtjz mtjx mtjy G_MTJ
+ G0 = '1/Rmtj' P = 'Pmtj'
*Central LLF for the free layer
XLLG theta phi isx isy isz hx hy hz hpT llg_solver
+ alpha='alpha' Hk='Hk' Vol='Volume' Ms='Ms'
*FM|NM Layer for GSHE
XFN 0 c1 0 z1 0 x1 0 y1 theta phi fmx fmy fmz G_FM_NM
+ G = 'gmix*Lgshe*Wgshe' P = 'Pmtj'
*GSHE Write Layer
XGSHE ini 0 c2 c1 z2 z1 x2 x1 y2 y1 G_GSHE
+ theta = 'thetash' L = 'Lgshe' W = 'Wgshe' t='tgshe' rho = '
    rhogshe'
lsf='lsfgshe'
*ME Write Layer
XME inb 0 hmex hmey hmez ME_CAP
+ Area = 'Lme*Wme' tins = 'tme' eps = 'epsme' alpha_me = '
    alphame'
*Reader resistance
Rread inr out 1k

*Voltage drivers
.param ei = -70m
```

```
.param eh = -100m
Vread inr 0 50m
Vhctr inb 0 0
*Vhctr inb 0  pulse 'eh' '-eh' 1n 0.2u 50p 50p 1u
*Victr ini 0 ei
Victr ini 0  pulse 'ei' '-ei' 1n 500n 50p 50p 1u

*open ckt for GSHE
Rc c2 0 10MEG
Rz z2 0 10MEG
Ry y2 0 10MEG
Rx x2 0 10MEG

*Hd for magnet
Ehp hpT 0 vol='4*pi*Ms/Hk'

* Spin-Current Input
EIx isx 0 vol='v(mtjx)+v(fmx)'
EIy isy 0 vol='v(mtjy)+v(fmy)'
EIz isz 0 vol='v(mtjz)+v(fmz)'

* Magnetic-field Input
EV1 hx 0 vol='v(hmex)+v(hxx)'
EV2 hy 0 vol='v(hmey)+v(hyy)'
EV3 hz 0 vol='v(hmez)+v(hzz)'

** Noise Suppress is used to scale down other noise sources
   in circuit
*** This factor does NOT affect the Thermal Magnetic Noise
```

```
.param noiseSupress='1e-5'
.param gamma='1.76*1e7'
.param kT='0.0259*1.602e-19*1e7'

G1x hxx 0 noise='((4*kT*alpha)/(Ms*Volume*gamma))*(1/
   noiseSupress^2)'
R1x hxx 0 1
G1y hyy 0 noise='((4*kT*alpha)/(Ms*Volume*gamma))*(1/
   noiseSupress^2)'
R1y hyy 0 1
G1z hzz 0 noise='((4*kT*alpha)/(Ms*Volume*gamma))*(1/
   noiseSupress^2)'
R1z hzz 0 1

.nodeset V(theta)='pi-0.01'
.nodeset V(phi)='pi/2'

*EMZ Mz 0 vol='cos(V(theta))'
*EMX Mx 0 vol='sin(V(theta))*cos(V(phi))'
*EMY My 0 vol='sin(V(theta))*sin(V(phi))'


.option post
.option ingold=1
.option delmax=1p
.tran 100p 501n UIC
*.trannoise v(hz) samples=1 seed=19  scale='noiseSupress'
.probe v(*)  i(*)
*.fft v(out) np=32768 start=10n stop=20n
```

```
.end
```

.3.4 Circuit Testbench for Spin Switches

Following are the circuit testbenches for the spin switches.

Testbench to Extract Device Characteristics

```
*** Generating switching characteristics for SS ***

.include '../../gshe/gshe_switch.sp'

.option captab post

.param pi = 'acos(-1)'
.param vdd = -0.8
.param vss = 0.8
.param vgshe = 0.1

** Test setup

Xswitch in out dd ss GSHE_SS

Vin in 0 pulse '1*vgshe' '-1*vgshe' 0 1u 50n 50n 5u
Vdd dd 0 vdd
Vss ss 0 vss

Vout out out1 0
```

```
Xload out1 0 GSHE_LOAD

.ic V(Xswitch.thetaW) = 'pi-0.001'
.ic V(Xswitch.phiW) = '-pi/2'
.ic V(Xswitch.thetaR) = '0.001'
.ic V(Xswitch.phiR) = 'pi/2'

.tran 1p 1u UIC
.probe V(*) I(*)
.end
```

FO-1 testbench

```
 ***** FO1 Invertor testbench*********
*************************************

.include '../../gshe/gshe_switch_pma_exch_high_t.sp'

**** testbench

.param vdrv=-0.035
.param vdd=0.036
.param vss=-0.036
.param vdd1=0.036
.param vss1=-0.036
.param pi='acos(-1)'
**The driver invertor
Xdriver drvin intmdt1 dd1 ss1 GSHE_SS

**The four subsequent fanouts
```

```
Xfo1     intmdt out1int dd2 ss2 GSHE_SS

**Voltage drivers
Vdd1     dd1 0 vdd
Vdd2     dd2 0 vdd1
Vss1     ss1 0 vss
Vss2     ss2 0 vss1
*Vin     drvin 0 vdrv
Vin drvin 0 pulse '-1*vdrv' vdrv 30n 5p 5p 170n 185n

**Read off current at the driver output
Voutp    intmdt1 intmdt 0
Vout1    out1int out1 0
**Read off the output stages
*R1  out1 0 100MEG
Xload    out1 0 GSHE_LOAD

*Initial angle of the driver (close to +z axis)
.ic V(Xdriver.thetaW)='pi-0.001'
.ic V(Xdriver.phiW)='0'
.ic V(Xdriver.thetaR)='0.001'
.ic V(Xdriver.phiR)='0'
*Initial angle of the fanouts
*1
.ic V(Xfo1.thetaW)='0.001'
.ic V(Xfo1.phiW)='0'
.ic V(Xfo1.thetaR)='pi-0.001'
.ic V(Xfo1.phiR)='0'
```

```
**simulation
.option post captab
*.option runlvl = 6
*.dc vdrv 0 0.9 0.01
.tran 1p 100n UIC
*.meas
.probe v(*) i(*)
.end
```

Majority Gate

```
 ***** MGL testbench*********
************************************

.include 'path/to/memtj.sp'

**** testbench

.param edrv1=-0.021
.param edrv2=-0.021
.param edrv3=-0.021
.param edd1=0.07
.param edd2=0.07
.param edd3=0.07
.param edd4=0.021
.param ess1=-0.07
.param ess2=-0.07
.param ess3=-0.07
.param ess4=-0.021
.param pi='3.14159'
```

```
**sel invertor
Xsel sel dd1 ss1 intmdt11 MESO_INVERTER

**driver1 invertor
Xdriver1 drvin1 dd2 ss2 intmdt21 MESO_INVERTER

**driver3 invertor
Xdriver2 drvin2 dd3 ss3 intmdt31 MESO_INVERTER


**The driven device
Xfo1     intmdt dd4 ss4 out1int MESO_INVERTER

** two output stages

Xout1     out1 dd4 ss4 out2 MESO_INVERTER
Xout2     out1 dd4 ss4 out3 MESO_INVERTER

**Voltage drivers
Vdd1     dd1 0 edd1
Vdd2     dd2 0 edd2
Vdd3     dd3 0 edd3
Vdd4     dd4 0 edd4
Vss1     ss1 0 ess1
Vss2     ss2 0 ess2
Vss3     ss3 0 ess3
Vss4     ss4 0 ess4
*Vin     drvin 0 vdrv
```

```
Vin1 sel 0 pulse '-1*edrv1' edrv1 0n 0p 0p 100n 200n
Vin2 drvin1 0 pulse '-1*edrv2' edrv2 0n 0p 0p 50n 100n
Vin3 drvin2 0 pulse '-1*edrv3' edrv3 0n 0p 0p 25n 50n

**Read off current at the driver output
Voutp1   intmdt11 intmdt1 0
Voutp2  intmdt21 intmdt1 0
Voutp3   intmdt31 intmdt1 0
Voutp   intmdt1 intmdt 0
Vout1   out1int out1 0

**Read off the output stage
Rload1  out2 0 100MEG
Rload2  out3 0 100MEG


*Initial angle of the drivers (close to +z axis)
.ic V(Xdriver1.theta)='0.01'
.ic V(Xdriver1.phi)='0'

.ic V(Xdriver2.theta)='0.01'
.ic V(Xdriver2.phi)='0'

.ic V(Xsel.theta)='0.01'
.ic V(Xsel.phi)='0'

*Initial angle of the fanout
.ic V(Xfo1.theta)='pi-0.01'
.ic V(Xfo1.phi)='0'
```

```
.ic V(Xout1.theta)='pi-0.01'
.ic V(Xout1.phi)='0'

.ic V(Xout2.theta)='pi-0.01'
.ic V(Xout2.phi)='0'

**simulation
.option post captab
*.option runlvl = 6
.option ingold=1
*.dc vdrv 0 0.9 0.01
.tran 10p 250n UIC
*.meas
.probe v(*) i(*)
.end
```

.3.5 Example MATLAB Script for Post-Processing and Plotting

FO-1 Post Processor

```
%%%%Post Processor For FO-1%%%%%%%

clear all; clc;
close all;

netlist = 'gshesspmaexchhightfo1testbench.sp';
trans_output = 'gshesspmaexchhightfo1testbench.tr0';

usetr = 0;
```

```
if exist(trans_output,'file') == 2
    reply = input('Use previous .tran result ? (y/n) ','s');
    if(strcmpi(reply,'y') || isempty(reply))
        usetr=1;
    end
end

if usetr == 0
    hscommand = ['hspice -i ' netlist];
    delcommand = ['rm ' trans_output];
    system(delcommand);
    system(hscommand,'-echo');
end

%hbar=1.055e-34;
%q=1.6e-19;
%Ms=800;Vol=80e-9*100e-9*4e-9;Hk=130;alpha=0.01;
%kstt = hbar/(2*q*Ms*Vol*Hk*1e-1);

xx = loadsig(trans_output);

t = evalsig(xx,'TIME');
drivertheta = evalsig(xx,'v_xdriver_thetar');
fo1theta = evalsig(xx,'v_xfo1_thetar');
inp = evalsig(xx,'v_drvin');
intr = evalsig(xx,'v_intmdt');
out1 = evalsig(xx,'v_out1');
iout = evalsig(xx,'i_vout1');
idd1 = evalsig(xx,'i_vdd1');
```

```
idd2 = evalsig(xx,'i_vdd2');
iss1 = evalsig(xx,'i_vss1');
iss2 = evalsig(xx,'i_vss2');
ivin = evalsig(xx,'i_vin');
iintr = evalsig(xx,'i_voutp');
igshez = evalsig(xx,'i_xdriver_vgshez');
vgshez = evalsig(xx,'v_xdriver_3z');
igshex = evalsig(xx,'i_xdriver_vgshex');
vgshex = evalsig(xx,'v_xdriver_3x');
igshey = evalsig(xx,'i_xdriver_vgshey');
vgshey = evalsig(xx,'v_xdriver_3y');
imtj1 = evalsig(xx,'i_xdriver_xmtj_gmtj1');
imtj2 = evalsig(xx,'i_xdriver_xmtj_gmtj2');
%isttz = evalsig(xx,'v_xdriver_iszw');
%isttx = evalsig(xx,'v_xdriver_xllgwa_hsx')/kstt;
%istty = evalsig(xx,'v_xdriver_xllgwa_hsy')/kstt;
vdd1 = evalsig(xx,'v_dd1');
vss1 = evalsig(xx,'v_ss1');
vdd2 = evalsig(xx,'v_dd2');
vss2 = evalsig(xx,'v_ss2');

strt_idx = max(find(t<30e-9))
end_idx = min(find(abs(intr(strt_idx:end)-max(intr(strt_idx:
    end)))<1e-4))-1
%strt_idx = max(find(abs(inp-max(inp))<1e-6))+1
% end_idx =
strt_idx+min(find(abs(intr(strt_idx:end)-max(intr(strt_idx:
    end)))<1e-3))-1
%Energytot =
```

```
trapz(t(strt_idx:end_idx),
abs(vdd1(strt_idx:end_idx).*idd1(strt_idx:end_idx))+abs(vss1(
    strt_idx:end_idx).*
iss1(strt_idx:end_idx)))
% EMTJ =
trapz(t(strt_idx:end_idx),
abs((vdd1(strt_idx:end_idx)-intr(strt_idx:end_idx)).*imtj1(
    strt_idx:end_idx)+(vs
s1(strt_idx:end_idx)-intr(strt_idx:end_idx)).*imtj2(strt_idx:
    end_idx)))
% EGSHE =
trapz(t(strt_idx:end_idx),abs(intr(strt_idx:end_idx).*iintr(
    strt_idx:end_idx)))
% ES =
trapz(t(strt_idx:end_idx),
abs(vgshez(strt_idx:end_idx).*igshez(strt_idx:end_idx)+vgshex
    (strt_idx:end_idx).
*igshex(strt_idx:end_idx)+vgshey(strt_idx:end_idx).*igshey(
    strt_idx:end_idx)))
% Qstt = trapz(t(strt_idx:end_idx),isttz(strt_idx:end_idx))/q
%delay = t(end_idx)-t(strt_idx)

%calculate powers
%power through input
Pinp = abs(ivin.*inp);
%power through dd1
Pdd1 = abs(idd1.*vdd1);
%power through ss1
Pss1 = abs(iss1.*vss1);
```

```
%power through dd2
Pdd2 = abs(idd2.*vdd2);
%power through ss1
Pss2 = abs(iss2.*vss2);
%power to the next stage
Pout = abs(intr.*iintr);
%Power MTJ+
Pmtjp = imtj1.*(vdd1-intr);
Pmtjm = imtj2.*(vss1-intr);
Pgshez = vgshez.*igshez;
Pgshey = vgshey.*igshey;
Pgshex = vgshex.*igshex;
Evin = trapz(t,abs(Pinp));
Edd1 = trapz(t,abs(Pdd1));
Ess1 = trapz(t,abs(Pss1));
Edd2 = trapz(t,abs(Pdd2));
Ess2 = trapz(t,abs(Pss2));
Eout = trapz(t,abs(Pout));
Emtjp = trapz(t,abs(Pmtjp));
Emtjm = trapz(t,abs(Pmtjm));

Pmtjpl = Pmtjp(end)*1e6
Pmtjml = Pmtjm(end)*1e6
Pgshe = Pout(end)*1e6

Ptot = Pmtjpl + Pmtjml + Pgshe
figure;
plot(t*1e9,cos(drivertheta),'r*-',t*1e9,cos(fo1theta),'b^-');
```

```
xlabel('t (ns)');ylabel('m');legend('driver','fo1','Location'
    ,'Best');xlim([0
100]);ylim([-1.1 1.1])


figure;
plot(t*1e9,inp*1e3,'r-',t*1e9,intr*1e3,'b-',t*1e9,out1*1e3,'k
    -');
xlabel('t (ns)');ylabel('V_l_e_v_e_l
(mV)');legend('V1','V2','V3','Location','Best');

figure;
plot(t*1e9,(Pdd1+Pss1)*1e6,'r-',t*1e9,Pmtjp*1e6,'b-',t*1e9,
    Pmtjm*1e6,'g-',t*1e9,
Pout*1e6,'k-');
xlabel('t (ns)');ylabel('P
(\muW)');legend('P_i_n','P_M_T_J_+','P_M_T_J_-','P_G_S_H_E');
```

Post Processor for MESH Oscillator

```
%%%MESH Post Processor%%%%

clear all; clc;
%close all;

netlist = 'MESHOscilator.sp';
trans_output = 'MESHOscilator.tr0';
fft_output = 'MESHOscilator.ft0';

usetr = 0;
```

```
if exist(trans_output,'file') == 2
    reply = input('Use previous .tran result ? (y/n) ','s');
    if(strcmpi(reply,'y') || isempty(reply))
        usetr=1;
    end
end

if usetr == 0
    hscommand = ['hspice -hpp -mt 16 -i ' netlist];
    delcommand = ['rm ' trans_output];
    system(delcommand);
    system(hscommand,'-echo');
end

xx = loadsig(trans_output);
yy = loadsig(fft_output);

t = evalsig(xx,'TIME');
theta = evalsig(xx,'v_theta');
phi = evalsig(xx,'v_phi');
victr = evalsig(xx,'v_ini');
vhctr = evalsig(xx,'v_inb');
vout = evalsig(xx,'v_out');
hmez = evalsig(xx,'v_hz');

mz = cos(theta);
mx = cos(phi).*sin(theta);
my = sin(phi).*sin(theta);
```

```
freq = evalsig(yy,'hertz');
vspectra = evalsig(yy,'v_out');

figure;
plot(t*1e9,mz);
xlabel('t(ns)');ylabel('m_z');ylim([-1.1 1.1]);%xlim([10 15])
    ;

%figure;
%plot(t*1e9,vout*1e3);;
%xlabel('t(ns)');ylabel('V_O_U_T (mV)');;xlim([10 15]);

%figure;
%plot(freq*1e-9,vspectra);
%xlabel('Fequency (GHz)');ylabel('V_O_U_T (dB)');xlim([0.1
    20]);

%figure;
%box on;
%plot3(mz,my,mx);
%xlabel('m_z');ylabel('m_y');zlabel('m_x');

figure;
plot(victr(2:end)*1e3,mz(2:end));
%plot(vhctr(2:end)*1e3,mz(2:end));
xlabel('V_I_-_C_o_n_t_r_o_l (mV)');ylabel('m_z');
%xlabel('V_H_-_C_o_n_t_r_o_l (mV)');ylabel('m_z');

figure;
```

```
plot(-victr(2:end)*1e3,(41.945-vout(2:end)*1e3)+41.945);
%plot(vhctr(2:end)*1e3,vout(2:end)*1e3);
xlabel('V_I_-_C_o_n_t_r_o_l (mV)');ylabel('V_O_U_T');
%xlabel('V_H_-_C_o_n_t_r_o_l  (mV)');ylabel('V_O_U_T');
```

.4 Material Parameters Database

This section is adapted from Samiran Ganguly, Kerem Y. Camsari, Supriyo Datta, "Evaluating Spintronic Devices Using The Modular Approach" [1]

We list the baseline parameters for various modules used in this work below. In simulations of chapter 5 only one parameter is changed at a time, except for magnet design where the area of the magnet or M_s is changed with H_k to maintain an energy barrier of 40 kT. All parametric changes for numerical experiments performed in chapter 5 are monotonic.

Note: The FM-NM interface conductance values in our modules correspond to half the magnitudes reported in the literature, for instance see [51,113]. $g_0 = 5 \times 10^{15}$ corresponds to the $Re(g_{\uparrow\downarrow}) = 2.5 \times 10^{15}$.

Table 1

MTJ Module

Parameter	**Units**	**Value**
Conductance	S	$1m$
Polarization	-	0.7
In-Plane Coeff.	-	1
OOP Coeff.	-	0

Table 2

MTJ Module: Heusler Alloy

Parameter	**Units**	**Value**
Conductance	S	$1m$
Polarization	-	0.99
In-Plane Coeff.	-	1
OOP Coeff.	-	0

Table 3

MTJ Module: Heusler Alloy SV

Parameter	**Units**	**Value**
Conductance	S	0.1
Polarization	-	0.99
In-Plane Coeff.	-	1
OOP Coeff.	-	0

Table 4

GSHE Module: IMA Magnet

Parameter	**Units**	**Value**
Width	m	$100n$
Length	m	$80n$
Thickness	m	$2n$
Spin-flip length	m	$2n$
Resistivity	$\Omega - m$	$170e - 8$
Spin Hall Angle	-	0.3

Table 5
GSHE Module: Low H_k PMA Magnet

Parameter	**Units**	**Value**
Width	m	$100n$
Length	m	$100n$
Thickness	m	$2n$
Spin-flip length	m	$2n$
Resistivity	$\Omega - m$	$170e - 8$
Spin Hall Angle	-	0.3

Table 6
GSHE Module: Medium H_k PMA Magnet

Parameter	**Units**	**Value**
Width	m	$32n$
Length	m	$32n$
Thickness	m	$2n$
Spin-flip length	m	$2n$
Resistivity	$\Omega - m$	$170e - 8$
Spin Hall Angle	-	0.3

Table 7
GSHE Module: High H_k PMA Magnet

Parameter	**Units**	**Value**
Width	m	$16n$
Length	m	$16n$
Thickness	m	$2n$
Spin-flip length	m	$2n$
Resistivity	$\Omega - m$	$170e - 8$
Spin Hall Angle	-	0.3

Table 8
FM-NM Module: IMA Magnet

Parameter	**Units**	**Value**
Conductance	S	$80n \times 100n \times 5 \times 10^{15}$
Polarization	-	0.7
In-Plane Coeff.	-	1
OOP Coeff.	-	0

Table 9
FM-NM Module: Low H_k PMA Magnet

Parameter	**Units**	**Value**
Conductance	S	$\pi \times 50n \times 50n \times 5 \times 10^{15}$
Polarization	-	0.7
In-Plane Coeff.	-	1
OOP Coeff.	-	0

Table 10
FM-NM Module: Medium H_k PMA Magnet

Parameter	**Units**	**Value**
Conductance	S	$\pi \times 16n \times 16n \times 5 \times 10^{15}$
Polarization	-	0.7
In-Plane Coeff.	-	1
OOP Coeff.	-	0

Table 11
FM-NM Module: High H_k PMA Magnet

Parameter	**Units**	**Value**
Conductance	S	$\pi \times 8n \times 8n \times 5 \times 10^{15}$
Polarization	-	0.7
In-Plane Coeff.	-	1
OOP Coeff.	-	0

Table 12
LLG Module: IMA Magnet

Parameter	**Units**	**Value**
Area	m^2	$80n \times 100n$
Thickness	m	$2n$
Damping Coeff.	-	0.01
Sat. Magnetization	emu/cc	800
Aniso. Field Strength	Oe	130

Table 13
LLG Module: Low H_k PMA Magnet

Parameter	**Units**	**Value**
Area	m^2	$\pi \times 50n \times 50n$
Thickness	m	$2n$
Damping Coeff.	-	0.01
Sat. Magnetization	emu/cc	800
Aniso. Field Strength	Oe	130

Table 14
LLG Module: Medium H_k PMA Magnet

Parameter	**Units**	**Value**
Area	m^2	$\pi \times 16n \times 16n$
Thickness	m	$2n$
Damping Coeff.	-	0.1
Sat. Magnetization	emu/cc	400
Aniso. Field Strength	Oe	2500

Table 15
LLG Module: High H_k PMA Magnet

Parameter	**Units**	**Value**
Area	m^2	$\pi \times 8n \times 8n$
Thickness	m	$2n$
Damping Coeff.	-	0.1
Sat. Magnetization	emu/cc	400
Aniso. Field Strength	Oe	10100

Table 16

LLG Module: High H_k PMA Sy−AFM

Parameter	**Units**	**Value**
Area	m^2	$\pi \times 8n \times 8n$
Thickness Assist	m	$1.2n$
Thickness Free	m	$0.8n$
Damping Coeff.	-	0.1
Sat. Magnetization	emu/cc	400
Aniso. Field Strength	Oe	10100

Table 17

LLG Module: High H_k IMA

Parameter	**Units**	**Value**
Area	m^2	$8n \times 20n$
Thickness	m	$2n$
Damping Coeff.	-	0.05
Sat. Magnetization	emu/cc	400
Aniso. Field Strength	Oe	13000

Table 18

ME Module

Parameter	**Units**	**Value**
Area	m^2	$80n \times 100n$
Thickness	m	$10n$
ME Coeff.	-	1×10^{-8}
Rel. Permittivity	-	500

Table 19
Dipolar Coupling Module: IMA Magnet

Parameter	**Units**	**Value**
Sat. Magn. 1	emu/cc	800
Vol. 1	m^3	$100n \times 80n \times 2n$
Sat. Magn. 2	emu/cc	800
Vol. 2	m^3	$100n \times 80n \times 2n$
Dipolar Coeff.	-	$0.0256, -0.0128, -0.0128$

Table 20
Exchange Coupling Module: Low H_k PMA Magnet

Parameter	**Units**	**Value**
Sat. Magn. 1	emu/cc	800
Vol 1	m^3	$\pi \times 50n \times 50n \times 2n$
Sat. Magn. 2	emu/cc	800
Vol 2	m^3	$\pi \times 50n \times 50n \times 2n$
Exchange Field Coeff.	erg/cm^2	5

Table 21
Exchange Coupling Module: Medium H_k PMA Magnet

Parameter	**Units**	**Value**
Sat. Magn. 1	emu/cc	400
Vol 1	m^3	$\pi \times 16n \times 16n \times 2n$
Sat. Magn. 2	emu/cc	400
Vol 2	m^3	$\pi \times 16n \times 16n \times 2n$
Exchange Field Coeff.	erg/cm^2	5

Table 22
Exchange Coupling Module: High H_k PMA Magnet

Parameter	**Units**	**Value**
Sat. Magn. 1	emu/cc	400
Vol 1	m^3	$\pi \times 8n \times 8n \times 2n$
Sat. Magn. 2	emu/cc	400
Vol 2	m^3	$\pi \times 8n \times 8n \times 2n$
Exchange Field Coeff.	erg/cm^2	5

Table 23
Exchange Coupling Module: Sy−AFM

Parameter	**Units**	**Value**
Sat. Magn. 1	emu/cc	400
Vol Assist	m^3	$\pi \times 8n \times 8n \times 1.2n$
Sat. Magn. 2	emu/cc	400
Vol Free	m^3	$\pi \times 8n \times 8n \times 0.8n$
Exchange Field Coeff.	erg/cm^2	5

Table 24
LLG Module: Stochastic Magnet

Parameter	**Units**	**Value**
Area	m^2	$30n \times 15n$
Thickness	m	$0.5n$
Damping Coeff.	-	0.01
Sat. Magn.	emu/cc	500
Aniso. Field Strength	Oe	1000

VITA

VITA

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