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Laser direct written silicon nanowires for electronic and sensing applications

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ABSTRACT

Nam, Woongsik Ph.D., Purdue University, August 2016. Laser Direct Written Silicon Nanowires for Electronic and Sensing Applications. Major Professor: Xianfan Xu, School of Mechanical Engineering.

Silicon nanowires are promising building blocks for high-performance electronics and chemical/biological sensing devices due to their ultra-small body and high surface-to-volume ratios. However, the lack of the ability to assemble and position nanowires in a highly controlled manner still remains an obstacle to fully exploiting the substantial potential of nanowires. Here we demonstrate a one-step method to synthesize intrinsic and doped silicon nanowires for device applications. Sub-diffraction limited nanowires as thin as 60 nm are synthesized using laser direct writing in combination with chemical vapor deposition, which has the advantages of in-situ doping, catalyst-free growth, and precise control of position, orientation, and length. The synthesized nanowires have been fabricated into field effect transistors (FETs) and FET sensors. The FET sensors are employed to detect the proton concentration (pH) of an aqueous solution and highly sensitive pH sensing is demonstrated. Both top- and back-gated silicon nanowire FETs are demonstrated and electrically characterized. In addition, modulation-doped nanowires are synthesized by changing dopant gases during the nanowire growth. The axial p-n junction nanowires are electrically characterized to demonstrate the diode behavior and the transition between dopant levels are measured using Kelvin probe force microscopy.

CHAPTER 1. INTRODUCTION

During the past decades, semiconductor nanowires have attracted a great deal of attention due to their demonstrated potential for high-performance nanoscale devices such as transistors (Cui and Lieber, 2001), sensors (Cui et al., 2001), resonators (Feng et al., 2007), solar cells (Garnett and Yang, 2008) and thermoelectric systems (Hochbaum et al., 2008). The high surface-to-volume ratios of nanowires make them sensitive probes to chemical and biological species. The ultra-thin bodies of nanowires allow excellent electrostatic control which is required for high-performance electronic devices. However, despite their promise, complex procedures for integrating nanowires into a nanoscale device remain an obstacle for widespread applications. The bottom-up approach requires assembly of nanowires grown from chemical vapor deposition (CVD), which not only involves CMOS incompatible processes but also suffers from difficulty in precisely positioning nanowires. The top-down approaches require multiple fabrication steps for nanowire patterning, etching, and doping as well as the use of advanced optical or electron-beam lithography and silicon-on-insulator (SOI) substrates.

In this work, we demonstrate a single-step, laser-direct-write method to fabricate intrinsic and doped silicon nanowires. The synthesized nanowires are used for electronic devices and sensing applications.

1.1 Nanowires

The vapor-liquid-solid (VLS) method has been the most successful route to produce semiconductor nanowires. In the VLS method, vapor phase precursors are dissolved into nanosized liquid droplets of a catalyst material, from which unidirectional nanowire growth proceeds. The produced nanowires have a single-crystalline structure, which is ideal for electronic and optical applications, and high-quality surfaces with fewer surface dangling bonds due to nanowire surface faceting (Garnett et al., 2009). The possible in situ doping by incorporating dopant precursors during nanowire growth eliminates the need for an additional doping procedure. Because the diameter of each nanowire is largely determined by the size of the catalytic particle, the choice of the seed particles allows control over the diameter of the nanowires produced. However, the use of the catalyst also leads to undesirable contamination of nanowires. For Si nanowires, the most commonly used catalyst is Au. Au atoms are highly diffusive in Si and act as deep level acceptors, negatively affecting device performance. There have been significant research efforts to overcome this drawback. Complementary metal-oxide-semiconductor (CMOS) compatible metals such as Al (Wang et al., 2006) and Bi (Heitsch et al., 2008) have been demonstrated as catalysts for Si nanowire growth. Catalyst-free growth of silicon nanowires was also shown to be possible (Kim et al., 2009).

A more crucial drawback of using the bottom-up nanowires for device applications is difficulty in precisely controlling the position and orientation of nanowires. Because these nanowires are produced as entangled mesh, additional fabrication procedures are required to position and align nanowires in placement required for large-scale

semiconductor devices. There have been a number of techniques developed to overcome this obstacle. For example, nanowires were aligned using strong electric fields (Lee et al., 2010), dielectrophoresis (Raychaudhuri et al., 2009; Freer et al., 2010), microfluidic alignment (Huang et al., 2001), lubricant-assisted contact printing (Fan et al., 2008; Yan et al., 2011), and nanocombing (Yao et al., 2013). Some of these techniques achieved a very high yield in the alignment of single nanowires to metallic pads, but none of them has demonstrated the capability to create the high density and precision required for integrated circuit manufacturing. Alternatively, large arrays of accurately placed, high density vertical nanowires were demonstrated using lithographically defined catalyst locations (Mårtensson, 2003; Borgström, 2007). Although these vertical nanowires are available for high-density device applications, a great amount of work is still required to solve fabrication issues and improve device performance.

1.2 Laser Direct Writing

Laser direct writing (LDW) refers to a technique that is able to create 1D to 3D features by laser-induced deposition, modification, or subtraction of materials. LDW has some advantages over conventional patterning methods such as lithography. First, a wide range of materials including metals, ceramics, semiconductors, polymers, composites and biomaterials can be patterned or fabricated. Second, intricate 3D structures which are either impossible or impractical with conventional patterning methods can be easily made by LDW. Moreover, no need for masks or preexisting patterns adds more flexibility to LDW. Consequently, LDW is extensively used for rapid prototyping applications because designs and patterns can be changed and immediately applied to final products.

One of the LDW methods is laser chemical vapor deposition (LCVD). In this process, a laser beam is focused on a substrate and materials are deposited around the laser spot from gas precursors. Since LCVD was first demonstrated for depositing Si and W in the early 1980s (McWilliams et al., 1983), the method was used for direct writing of Al lines on various substrates (Foulon and Stuke, 1993), and also applied to create 3D structures (Lehmann and Stuke, 1994; Wanke et al., 1997). However, minimum feature sizes in these studies were much larger than the laser beam diameter.

There has been much research effort to reduce feature sizes far below the diffraction limit. The approaches to this end include multiphoton polymerization (Kawata et al., 2001; Li et al., 2009), stimulated emission depletion (STED) microscopy (Westphal and Hell, 2005), near field plasmonic approaches (Sun and Leggett, 2004; Srituravanich et al., 2008), and zone plate lithography (Smith et al., 2006). These methods have achieved sub-diffraction limit features down to tens of nanometers, but none of them was able to be directly applied to grow nanoscale materials.

1.3 Nanowire Field Effect Transistor Sensors

Since ion-sensitive field effect transistors (ISFETs) were first demonstrated to measure chemical quantities in 1970 (Bergveld, 1970), there has been considerable attention to use them for chemical and biological applications. The detection principle of ISFETs is based on their configuration as field effect transistors (FETs). In a standard FET, the conductance of the semiconductor channel is modulated by the electric field applied by a gate electrode. The application of a gate voltage depletes or accumulates charge carriers in the channel and thus the FET conductance directly depends on the gate

voltage. In an ISFET, the binding of a charged chemical or biological species has a role analogous to that of a gate voltage. Unlike conventional FETs, the gate oxide surface of an ISFET is exposed to an external electrolyte, allowing a chemical or biological species of interest to interact with the surface. The charges of the surface-bound species create an electric field, which modulates the number of carriers in the channel in the same way as a gate voltage does, and consequently the existence and the concentration of a target species can be detected by measuring the change of the FET conductance.

One advantage of ISFETs is that there is no need for the a priori attachment of fluorescent or any other labels to target molecules. This label-free sensing makes detection quick and on site. The required specific detection can be provided by functionalizing the sensor surface with a receptor for target molecules. The direct, electrical readout of signals is another attractive feature of these sensors. The electrical signals can be directly routed to the outside world, enabling easy integration of the sensors into miniaturized systems. However, the limited sensitivity of ISFETs remained a challenge.

In 2001, the application of nanowires to FET sensors (Cui et al., 2001) demonstrated the potential of significantly improved sensitivity, triggering new research interest. Because of the one-dimensional morphology and high surface-to-volume ratio of a nanowire, a very small amount of surface-bound molecules are needed to change the conductance of the nanowire in the sensors. In subsequent research, sensitivity increased to the point sufficient to detect single particles (Patolsky, 2004). The first nanowire FET sensors were demonstrated for the detection of pH, protein, and calcium ions. Later, nanowire FET sensors were used to detect single-stranded DNA (Hahm and Lieber,

2004). Complementary single-stranded sequences of peptide nucleic acids (PNAs) were used as a receptor, and excellent selectivity between target DNA and mismatched mutant DNA was demonstrated. Cancer marker proteins down to femtomolar concentrations were also detected using nanowire FET sensors (Zheng et al., 2005). In this research, an array of distinct nanowires with different receptors were used to simultaneously detect multiple biomarkers and discriminate false positives, providing high selectivity and the information necessary for robust diagnosis of disease. Gas-phase species, such as NO_2, CO, ethanol and so on, have been sensed via metal oxide nanowires, including ZnO, TiO_2, SnO_2, and others (Comini et al., 2002; Li et al., 2008; Joshi et al., 2009).

A persistent issue encountered in applications of nanowire FET sensors to physiological fluid samples such as blood is that the surface of nanowires can be deactivated by biofouling and non-specific binding. Also, the sensitivity of the sensors depends on solution ionic strength due to charge screening of dissolved solution counterions, that is, the Debye screening (Stern et al., 2007). To overcome these limitations, Stern et al. (2009) used a microfluidic purification chip which captures biomarkers from blood samples and thereafter releases them into a purified buffer for sensing. The approach allowed them to detect two cancer markers, PMSA and CA15.3 in whole blood.

1.4 Nanowire Transistors and Circuits

Using nanowires for FETs offers some advantages over conventional planar devices. First, the ultra-thin body of nanowires allows more efficient control over charge carriers in the semiconductor channel. Moreover, the one-dimensional morphology of

nanowires enables straightforward implementation of semicylindrical gate or gate-all-around architectures, reducing short channel effects and improving device performance. In addition, the single-crystalline structure and smooth surfaces of nanowires reduce carrier scattering in the FET channel and results in high carrier mobility.

One of the most commonly used structures of nanowire FETs is a back gate configuration where a nanowire is deposited on an oxide and the underlying Si substrate acts as a back gate. Metal electrodes are directly deposited on the nanowire without intentional formation of p-n junctions. In this structure, device performance is largely affected by Schottky barriers at the metal-semiconductor interfaces (Guo et al., 2003; Chen et al., 2005). In a conventional FET, metal-semiconductor interfaces are placed away from a channel by highly doped source/drain extensions and thus a gate voltage has little influence on the Schottky barriers. However, in such a nanowire FET, the application of a gate voltage alters the width of the Schottky barriers and the carrier transport through the Schottky barriers is influenced by the gate voltage, making the FET a Schottky barrier device. Schottky barriers at metal-silicon nanowire interfaces are typically positive due to Fermi level pinning by surface states (Sze and Ng, 2007). Therefore, engineering contact properties can significantly improve device performance. For example, a study of nanowire FETs showed that extrinsic field-effect mobility can be significantly improved by thermal annealing (Cui et al., 2003).

Early research on nanowire devices focused on the demonstration of individual transistors and basic devices. Duan et al. (2001) demonstrated indium phosphide nanowire FETs and crossed-wire p-n junctions. Cui and Lieber (2001) also demonstrated silicon nanowire p-n junction diodes and bipolar transistors. Huang et al. (2001)

fabricated logic gates using silicon and gallium nitride nanowires. As nanowire assembly techniques (Lee et al., 2010; Raychaudhuri et al., 2009; Freer et al., 2010; Huang et al., 2001; Fan et al., 2008; Yan et al., 2011; Yao et al., 2013) have developed, nanowire devices have been integrated into larger scale circuits. Address decoders (Zhong et al., 2003) were created using a crossbar structure where active devices were formed at the intersection points of two crossed nanowires. Programmable nanowire circuits were demonstrated using Ge/Si heterostructure nanowires (Yan et al., 2011). However, the lack of the capability to create a high density array of precisely aligned nanowires which are required for very large scale integrated (VLSI) circuit manufacturing still limits an industrial use of nanowire arrays for device applications.

1.5 P-n Junction Nanowires

In order to make full use of the electrical properties of semiconductor nanowires, controlled doping is an important issue. For VLS nanowires, in-situ doping can be realized by adding dopants to the gas mixture used for nanowire deposition. Diborane (Cui et al., 2000) and trimethylboron (Lew et al., 2004; Vallett et al., 2010) have been used for p-type Si nanowires, and phosphine (Wang et al., 2005) and arsenic (Tang et al., 2005) for n-type Si nanowires. The growth mechanism of semiconductor nanowires also offers the possibility of straightforward fabrication of axial heterojunction structures. For example, axial modulation-doped nanowires have been demonstrated by changing the dopant source during nanowire growth (Kempa et al., 2008; Imamura et al., 2008). These axial p-n junction structures are advantageous because they do not require additional junction fabrication processes. In addition, transition lengths as short as 10 nm have been

reported (Christesen et al., 2013). The known difficulty in fabricating axial p-n junction nanowires is the radial deposition or the dopant incorporation through the nanowire surface after changing the growth conditions (Yang et al., 2005). In the case of boron in silicon nanowires, boron atoms are insufficiently incorporated into Si via metal catalysts and the majority of boron atoms come from deposition of high boron concentration layers on the side-wall of a nanowire (Imamura et al., 2008). Therefore, if a doping agent such as B_2H_6 is introduced midway during the growth of a p-n junction nanowire, the entire nanowire is doped with boron, which severely limits the realization of axial p-n junction nanowires. A similar mechanism was also observed for boron-doped Ge nanowires and Tutuc et al. (2006) proposed a new method to synthesize p-n junction Ge nanowires where a thin boron-doped layer is deposited after fabricating a phosphorus-doped and undoped junction structure. On the other hand, when PH_3 is used as an n-type doping source for Si nanowires, a similar n-type overcoating has not been observed (Kempa et al., 2008; Yang et al., 2005). The VLS grown axial p-n junction nanowires have been demonstrated for tunnel field-effect transistors (Vallett et al., 2010), photovoltaics (Kempa et al., 2008) and diodes (Tutuc et al., 2006).

Another way to create p-n junction nanowires is growing a distinct shell on a preexisting nanowire core. The outer shell is epitaxially grown on a nanowire surface and by repeating the shell growth with different reactants, core/shell or core/multi-shell radial structures can be created. The unique geometry of radial nanowire heterostructures makes them excellent candidates for photovoltaic devices (Tian et al., 2007) because a carrier collection distance can be very short and hence bulk recombination can be avoided. The outer shell of a radial nanowire heterostructure can be also used as a surrounding-gate

which provides excellent electrostatic control over the conducting channel. Lauhon et al. (2002) reported the fabrication of high-performance transistors based on core/multi-shell Si-Ge nanowires.

1.6 Summary

Despite the demonstrated potential of nanowires for many applications and intense research for over a decade, nanowires still have few industrial applications. The main challenges include the lack of a reliable nanowire assembly technique which satisfies requirements for VLSI circuit fabrication, and metal contamination from catalysts used during the CVD growth. Although previous research has shown significant progress to overcome each of these drawbacks separately, none of them has achieved the level which can be used for industrial applications.

Laser direct writing has been widely used for research and industrial applications. The combination of laser direct writing and CVD was demonstrated decades ago, but the minimum feature sizes were much larger than the laser beam diameters. Although recent research has decreased feature sizes down to sub 100 nm resolution, these methods generally cannot be used for material synthesis.

In this work, we report a single-step approach to fabricate intrinsic and doped silicon nanowires with excellent control of nanowire position. Laser direct writing in combination with CVD created nanowires with diameters as small as 60 nm which is far below the diffraction limit. The synthesized nanowires are demonstrated for nanowire FETs and sensors. In addition, by changing dopant gases during nanowire growth, p-n junction nanowires were synthesized and characterized.

1.7 Report Outline

This chapter has introduced previous research about nanowires, laser direct writing, nanowire FET sensors, nanowire FETs, and p-n junction nanowires. Chapter 2 discusses laser direct writing of silicon nanowires. Experimental details of the laser direct write CVD method are first provided and the resulting nanowire growth is discussed. Our experiment and HFSS simulation show that the interference between incident laser irradiation and surface scattered radiation creates periodic heating needed for the synthesis of sub-diffraction limited nanowires.

Chapter 3 demonstrates the application of the laser direct written nanowires for chemical sensors. The synthesized nanowires are fabricated into nanowire FET sensors and the sensors are employed to detect the proton concentration (pH) of an aqueous solution.

Chapter 4 focuses on the application of the laser direct written nanowires for FETs. Both top-gated and back-gated nanowire FETs are fabricated using the laser direct synthesized nanowires, and device characteristics are investigated. The effect of doping concentration on device performance is studied.

In Chapter 5, axial p-n junction nanowires are demonstrated. The p-n junction nanowires are fabricated by changing the dopant gases during the laser-assisted nanowire growth. The p-n junction nanowires are electrically tested as diode devices and the surface potential is measured using Kelvin probe force microscopy.

Chapter 6 presents a summary and future plans for synthesis of modulation-doped nanowires as well as to improve the performance of nanowire FETs and sensors.

CHAPTER 2. LASER DIRECT WRITING OF SILICON NANOWIRES

The laser direct writing of silicon nanowires requires a variety of equipment, including lasers, optics, a gas delivery system, and nano-positioning stages. In this chapter, the experimental system for the nanowire synthesis will be described in detail. Then, a Fresnel zone plate (FZP) which is one of the key components in the experiment will be discussed. The focusing performance of our FZPs will be analyzed using the scalar diffraction theory. Finally, we will discuss experimental parameters which critically affect the nanowire growth and provide an explanation for the formation of the nanowires based on experimental results and numerical calculations.

2.1 Experimental Description

Silicon nanowires are synthesized using the combination of laser direct writing and chemical vapor deposition (CVD). Figure 2.1 shows a schematic of the laser direct write CVD method. A laser beam is focused onto a substrate using a focusing element. In our experiment, Fresnel zone plates were used as the focusing element because they give a diffraction limited spot size and are compact. This compactness of zone plates offers the potential of parallel processing by placing an array of multiple zone plates. The focused laser beam locally heats a small area on the substrate. The substrate is a 200 nm-thick silicon dioxide top layer over a 200 nm-thick polycrystalline silicon (poly-Si) layer on

quartz. The silicon dioxide top layer electrically isolates deposited Si nanowires from the substrate, and the poly-Si layer serves as a means for absorbing laser radiation. The substrate is located in a vacuum chamber with precursor gases of silane and dopant gases. Due to the thermal energy of the laser, the reactive precursors decompose on the laser spot and silicon is deposited. The choice of dopant atoms determines the doping polarity of nanowires. In the meantime, movement of the piezoelectric stage holding the substrate creates silicon nanowires in a desired pattern.

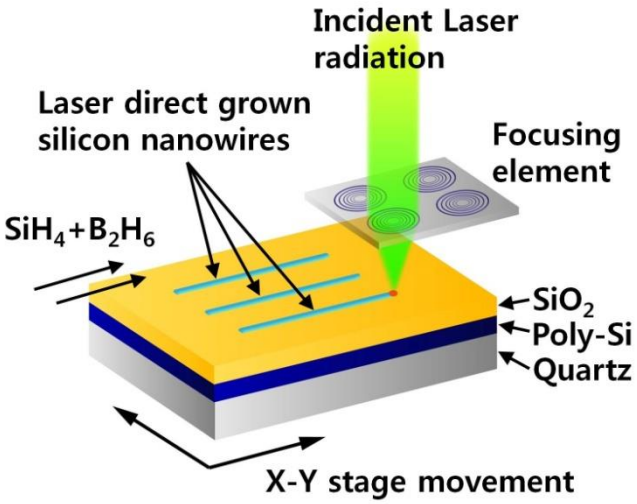

Figure 2.1. Schematic diagram of laser direct writing of silicon nanowires.

2.1.1 Lasers and Optical Components

Two titanium sapphire femtosecond pulsed lasers were used for nanowire growth. The first laser was a Coherent Mira which has a wavelength of 800 nm, 150 fs pulse duration, and 76 megahertz (MHz) repetition rate. The other laser was a Coherent Micra with a wavelength of 800 nm, a minimum pulse duration of 20 femtoseconds, and 80 MHz repetition rate. The reason to choose femtosecond lasers over a continuous wave (CW) laser is the capability of creating a highly confined heated area. Because a CW

laser delivers energy to the focus spot continuously, the heat dissipates around the spot and consequently the surface area with a temperature high enough to decompose silane becomes larger than the laser focus spot. In contrast, the high energy pulses of a femtosecond laser heat up the substrate in a very short time. Because temperature increases up to the point needed for silicon deposition before the heat is dissipated, the highly confined heating necessary to create a narrow silicon nanowire is possible.

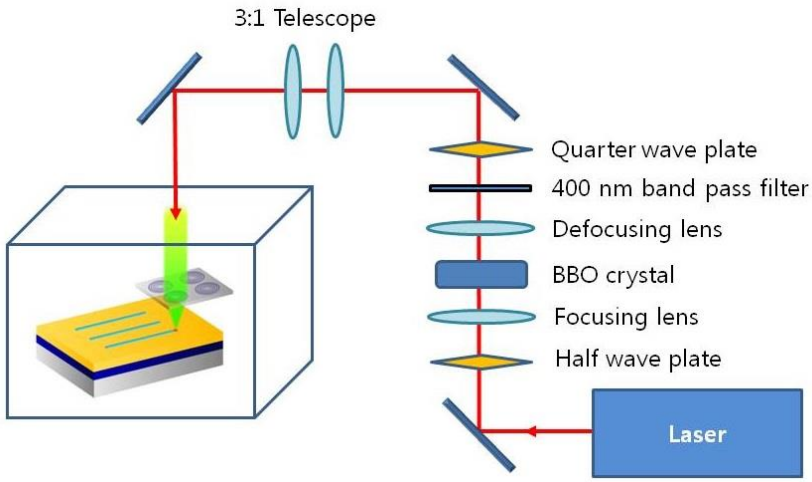

Figure 2.2. Diagram of the optical components in the experimental setup.

The laser beams were tuned to have a wavelength of 790 nm and frequency doubled to 395 nm by using a barium borate (BBO) crystal because silicon or silicon dioxide does not absorb the wavelength of 800 nm easily. Since the pulse widths of the two femtosecond lasers are different, two different thicknesses of the BBO crystal were required. A 1 mm-thick crystal was used for the Mira laser and a 100 μm-thick crystal was used for the Micra. To control the power and the polarization of the incident laser light, a half wave plate was inserted before the BBO crystal. Changes in the polarization angle were made by rotating the crystal and the half wave plate, and a circularly polarized

beam was created by adding a quarter wave plate after the crystal. The frequency doubled beam was filtered using a 400 nm band pass filter. The beam path with the optical components is shown in Figure 2.2. More details on the experimental setup and the laser direct writing method are found in the literature (Mitchell, 2010; Mitchell et al., 2011).

2.1.2 CVD System

The integrated system for the laser CVD method consists of a vacuum chamber, a gas delivery system, and a mechanical positioning system. The vacuum chamber is the place where the actual CVD takes place. The chamber has a viewport on top through which the laser passes and a swinging front door which allows the substrates and other components to be placed. A mechanical roughing pump is used to pump the chamber down to a minimum pressure of less than 100 milliTorr.

In the gas delivery system, there are 6 processing gas lines, which are separately regulated by mass flow controllers (MFCs). The 6 available gases are nitrogen at 2000 standard cubic centimeters per minute (sccm) maximum flow rate, a 9:1 hydrogen silane mixture at 10 sccm, diborane at 10 sccm, silicon tetrachloride in hydrogen at 10 sccm, argon at 200 sccm, and phosphine at 10 sccm. The process gas is delivered to the substrate through a flexible metal nozzle which is positioned close to the substrate. Because silane easily reacts with oxygen in the air to form silicon dioxide, the chamber is pumped to a minimum pressure and filled to 100 Torr with nitrogen to ensure that there is as little oxygen left in the chamber as possible. This pumping and filling process is repeated 8 times before and after the experiment. The entire gas delivery system is controlled by a custom-built software.

In order to write silicon nanowires in a desired pattern, the substrate needs to be moved relative to the laser beam. A Mad City Labs Nano-Align5-200 nanopositioning stage was used for the high precision movement of the substrate. The piezo-electric stage has a spatial resolution of 0.1 nm and the capability of scanning in both the x and y directions. In addition, the stage controls the separation in the z direction between the zone plates and the substrate. A Labview program was custom-written and used to control the stage. Figure 2.3 shows the inside of the CVD chamber including the zone plate holder, the piezo-electric stage, and the substrate holder.

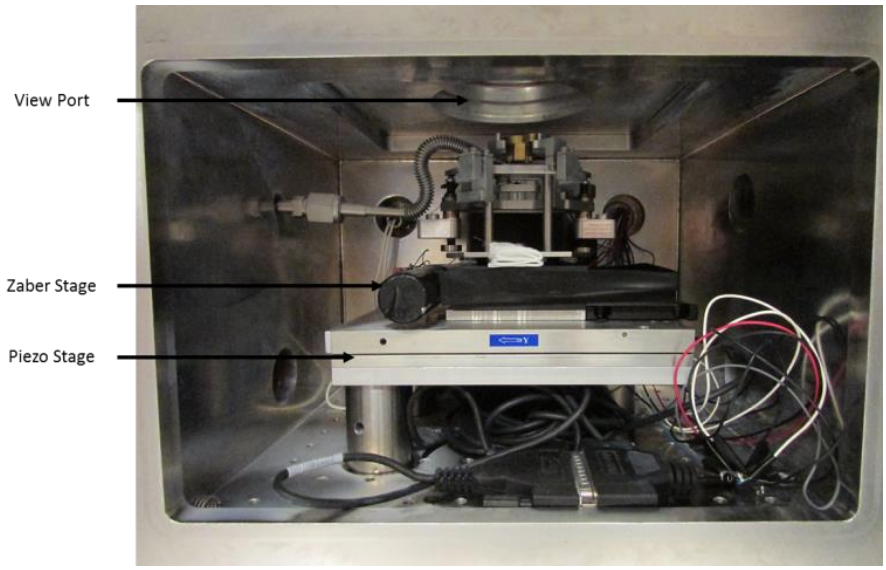

Figure 2.3. Internal image of the vacuum chamber.

2.1.3 Substrate Preparation

The substrate for nanowire growth is a quartz slide with a 200 nm-thick silicon dioxide top layer and a 200 nm-thick poly-Si layer in between. The substrate fabrication starts with standard solvent and piranha cleanings of a quartz slide. Semiconductor grade toluene, acetone, methanol and isopropanol were used for the solvent cleaning, and 96 %

sulfuric acid and 30 % hydrogen peroxide were mixed in a 1:1 ratio for the piranha cleaning. Then, a 350 nm-thick amorphous silicon layer was deposited using low pressure CVD at 545 °C for 260 minutes. In order to utilize the Si layer as a backgate in backgated FET devices, phosphorus was ion-implanted into the amorphous silicon. The used implant energy was 50 keV and the implant dose was 5×10^{14} ions/cm^2. The amorphous silicon was dry-oxidized at 1100 °C in O_2 for 130 minutes to yield 200 nm of thermally grown silicon dioxide. The oxidation consumes some of the Si layer and the thickness of the Si layer is reduced to around 200 nm. The high temperature process also crystallizes the amorphous Si layer, turning it into poly-Si. In addition, the implanted dopant atoms diffuse in the Si layer and are electrically activated during the high temperature process.

The top silicon dioxide layer serves as an insulator which electrically isolates laser-grown nanowires from the underlying poly-Si layer. The 200 nm-thick poly-Si layer has two roles as an efficient light absorber during the nanowire growth and as a backgate in a fabricated FET device. The heat absorbed in the poly-Si layer during nanowire growth locally increases the temperature of the substrate, enabling nanowire growth with a low laser power.

2.2 Fresnel Zone Plates for Light Focusing

A Fresnel zone plate (FZP) is a two dimensional focusing device consisting of a series of concentric circular gratings. Although FZPs have been known for more than 100 years, they had attracted little interest for a long time because of difficulty in fabrication and the existence of other optical elements, such as lenses and mirrors, which have functions similar to those of FZPs. Recent advances in micro-/nanotechnology triggered

FZPs to gain growing interest in various applications. Because FZPs can operate with all electromagnetic waves regardless of wavelength, they have found useful applications with x-rays and extreme ultraviolet (EUV) radiation where a refractive lens cannot be used due to strong absorption (Chao et al., 2005). Not only that, mature silicon technology resolved the difficulty in the fabrication of FZPs. With a planar geometry, FZPs can be conveniently made using standard thin film technology. The compactness of FZPs makes the integration of the optical device with other components easier. FZPs have become important optical devices in a variety of applications such as confocal microscopy, spectroscopy, and high-resolution lithography (Smith, 1996).

In our experiment, FZPs are used to focus the incident laser on the substrate. Because FZPs can be designed to achieve a near diffraction limit spot size at a specific wavelength and are as small as a few hundreds of μm in diameter, they are suitable for our experiment. Arrays of FZPs can be easily fabricated using standard thin film methods and used for parallel writing of nanowires. There are two types of FZPs, amplitude- and phase-zone plates. The former has alternate transparent and opaque rings. In this case, light impinging on the opaque rings is absorbed and the focusing efficiency of the FZP is low. In the case of phase-zone plates, phase-reversal zones are used instead of opaque rings. The incident radiation with the wrong phase is phase-modulated and waves passing through both open and phase-reversal zones interfere constructively at the focal point, allowing a higher efficiency of phase-zone plates. We chose to use phase-zone plates due to their higher efficiency and this allowed us to use very low laser power for nanowire growth. The FZPs were fabricated on a quartz substrate using E-beam lithography and the detailed fabrication procedure has been described previously (Srisungsitthisunti, 2011).

2.2.1 Principle of Fresnel Zone Plates

Fresnel zone plates have concentric alternate transparent and opaque (or phase-reversal) zones as shown in Figure 2.4. The optical path length from the boundary of each zone to the focal spot is a half wavelength different from that of an adjacent zone. In the case of having a plane wave as incident radiation, the radii of zones can be calculated using the following equation (Pedrotti et al., 2007).

$$r_n^2 = (f + \frac{n\lambda}{2})^2 - f^2 = n\lambda f + \frac{n^2\lambda^2}{4} \tag{3.1}$$

where f is the focal length of the zone plate, λ is the wavelength of the incident radiation, and r_n is the radius of the nth zone. The radius of the innermost zone is denoted as r_1. In the far-field, the focal length is much larger than the wavelength ($f >> \lambda$) and the radii of the zones are approximately given by the following expression.

$$r_n = \sqrt{n\lambda f} \tag{3.2}$$

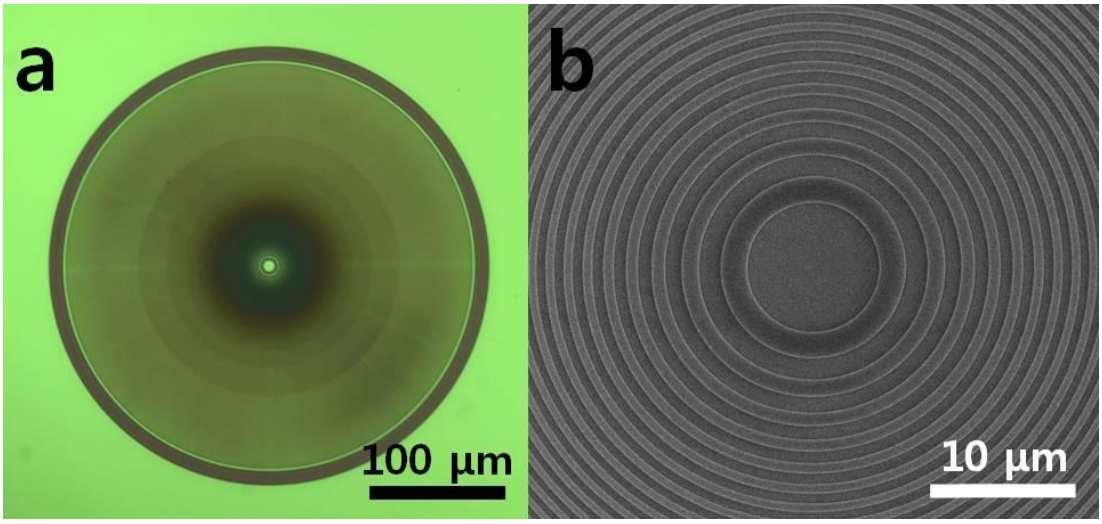

Figure 2.4. (a) Optical image and (b) SEM image of Fresnel zone plate.

The resolution of an FZP is largely determined by the wavelength λ and the outermost zone width, $\Delta r_n = r_n - r_{n-1}$. The Rayleigh's criterion sets the diffraction limited spatial resolution of an FZP as follows:

$$d_{FWHM} = \frac{0.61\lambda}{NA} \tag{3.3}$$

The numerical aperture of an FZP is the ratio of the outermost zone radius to the focal length, and can be expressed using the outer zone width Δr_n by taking the derivative of Eq. (3.2):

$$NA = \frac{r_n}{f} = \frac{\lambda}{2\Delta r_n} \tag{3.4}$$

Thus, the resolution of the zone plate depends on the outermost zone width, Δr_n.

$$d_{FWHM} = 1.22\Delta r_n \tag{3.5}$$

2.2.2 Rayleigh-Sommerfeld Calculation of Fresnel Zone Plates

Because the final size of the focused laser spot in our experiment is ultimately determined by the Fresnel zone plates, it is important to accurately analyze the focusing performance of the FZP. Several numerical methods are available to predict the light diffraction of an FZP, including scalar diffraction theory (Cao and Jahns, 2004), beam propagation method (Srisungsitthisunti, 2009), finite element analysis (Kurokhtin and Popov, 2002), and finite-difference time domain method (Prather and Shi, 1999). Among these methods, the scalar diffraction theory is simple and fast because it includes analytical methods. Although the method is inaccurate for near-field calculation, the far-field diffraction of FZPs, which is the case in our experiment, can be accurately

calculated using the method. Cao and Jahns (2004) recently evaluated the analytical solution for FZP focusing using the far-field approximation ($f >> \lambda$). The Rayleigh-Sommerfeld (RS) diffraction integral modified by Cao and Jahns (2004) is used to calculate the diffraction of FZPs in this chapter.

When the wavelength of a wave field is smaller than the aperture size of an FZP used to control the wave, the Rayleigh-Sommerfeld (RS) diffraction integral can be used to calculate the light diffraction of the FZP:

$$U(R) = \sum_{n=1}^{N} U_n(R) \tag{3.6}$$

$$U_n(R) = \frac{1}{\lambda} \iint_{A_n} \frac{f}{\rho^2} \exp(jk\rho) r dr d\theta \tag{3.7}$$

where *(r, θ)* are the polar coordinates at the FZP plane, *(R, ϕ)* are the polar coordinates at the focal plane, *N* is the number of rings, $U_n(R)$ is the individual diffracted field at the focal plane from the *n*th ring, *U(R)* is the total diffracted field distribution at the focal plane, A_n is the area of the *n*th ring, and $\rho = [f^2 + R^2 + r^2 - 2Rr\cos(\theta - \phi)]^{1/2}$. Although the RS integral is normally difficult to solve analytically, Cao and Jahns (2004) applied the far-field assumption ($f >> \lambda$) and evaluated an analytical solution for an FZP as follows:

$$U_n(R) = \frac{kf}{f_n^2} \exp\left[jk\left(f_n + \frac{R^2}{2f_n} \right) \right] \times \int_{a_n}^{b_n} \exp\left(jk \frac{r^2 - r_n^2}{2f_n} \right) J_0\left(\frac{kRr}{f_n} \right) r dr \tag{3.8}$$

where a_n and b_n are the radii of the lower and the upper edges of the *n*th ring, respectively, $f_n = (f^2 + r_n^2)^{1/2}$, and J_0 is the zero-order Bessel function of the first kind. Equation (3.8) is used to calculate the diffraction of FZPs in this chapter.

2.2.3 Focusing Analysis of Fresnel Zone Plates

The design parameters of the Fresnel zone plates used to grow nanowires are summarized in Table 2.1. The zone plates were designed for the wavelength of 395 nm and the diameter is about 300 μm. The phase-reversal zones were made of hydrogen silsesquioxane (HSQ) and the refractive index of the HSQ layer at around 400 nm wavelength was estimated to be 1.47 (Srisungsitthisunti, 2011). Because the light passing through the HSQ layer must undergo a π phase shift, the thickness of the layer should be 420 nm from the equation, $t = \lambda / 2(n_2 - n_1)$.

Table 2.1. Design parameters of the phase zone plates used in the experiment.

Wavelength	395 nm	# of rings	540
Focal length	50 μm	Zone plate radius	149.88 μm
Outermost zone width	211 nm	Focal spot size (FWHM)	185 nm
N.A.	0.9487	Diffraction efficiency	15.8 %

Figure 2.5 shows the light diffraction of the FZP calculated using the RS diffraction integral method. In Figure 2.5a, the x axis is the axial distance from the center of the FZP and the y axis is the radial distance from the center of the FZP. Strong light focusing is observed at x = 50 μm which is the focal point of the FZP. Figure 2.5b shows the intensity distribution of light at the focal plane. The full width half maximum (FWHM) at the focal spot is calculated to be 185 nm. Because the spot size of the FZP is directly related to the thickness of synthesized nanowires, achieving a small spot size is important in our experiment. The diffraction efficiency of the FZP is calculated to be 15.8 % by dividing the light intensity at the central peak by the total intensity incident on the FZP.

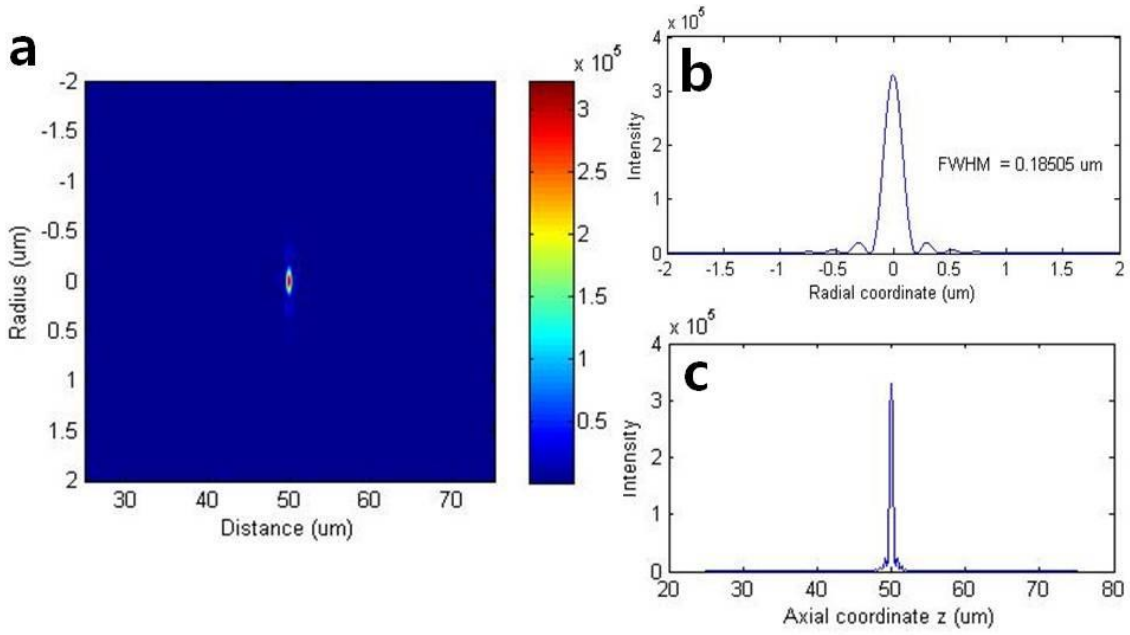

Figure 2.5. RS integral calculation of the FZP used to grow nanowires. (a) The intensity distribution of light diffracted by the FZP, (b) radial intensity at the focal plane, and (c) axial intensity.

The effect of fabrication errors in zone radii was also calculated. Figure 2.6a shows the intensity distribution at the focal plane when random fabrication errors between 10 and 50 nm, which are 5 – 24 % of the outermost zone width, are added to the zone radii. The FWHM increased only 2 nm from that of the ideal zone plate and the peak intensity decreased to 85.4 % of the ideal zone plate. In real fabrication processes, a more common situation is when all of the HSQ zones are either wider or narrower than the ideal zones. For example, when the HSQ layer is under-exposed or over-developed, the widths of the HSQ zones can be narrower than intended. Figure 2.6b shows when the HSQ zones become 60 nm narrower than the ideal widths. In this case, the FWHM increased only 2 nm and the peak intensity decreased to 87 % of the ideal zone plate. This indicates that the FZPs are tolerant of errors in zone widths.

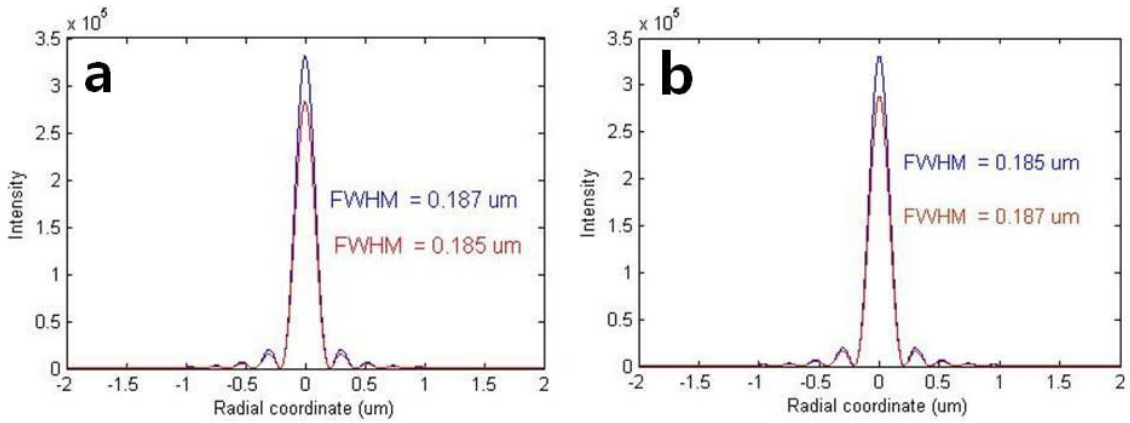

Figure 2.6. Intensity distribution of diffracted light at the focal plane. Blue lines are for ideal zone plates and red lines are for (a) an FZP with random fabrication errors in zone width and (b) an FZP with narrower HSQ zone widths.

Another possible fabrication error can be variation in the thickness of the HSQ layer. Figure 2.7 shows the spot size and the peak intensity of the focused light with different thicknesses of the HSQ layer. The thickness of the phase-reversal zones has no influence on the size of the focal spot. The peak intensity at the focus has its maximum at the phase retardation of π and decreases with an increasing or decreasing amount of phase retardation. However, the change in the peak intensity is gradual and as small as 2.4 % with a thickness error of 43 nm which is 10 % of the ideal thickness.

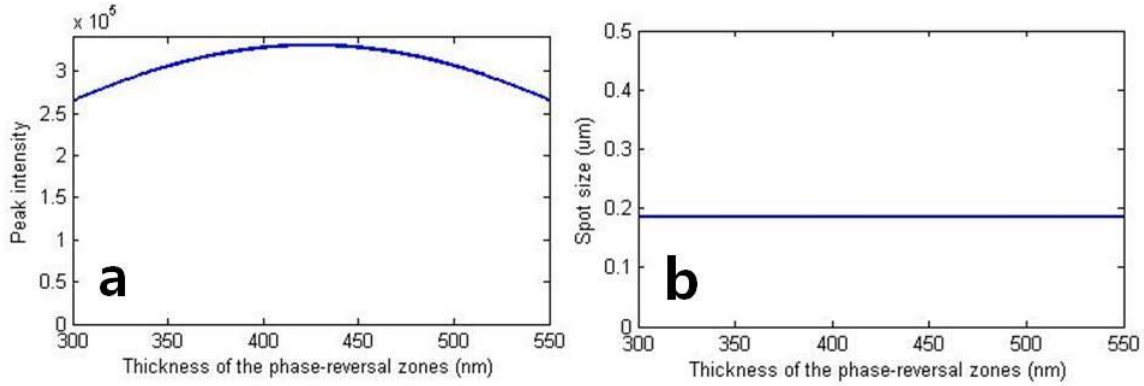

Figure 2.7. (a) Peak intensity at the focal spot and (b) the size of the focal spot as a function of the thickness of the HSQ layer.

Although the FZP is tolerant of errors in zone radii and the thickness of the phase-reversal zones, the FZP is sensitive to variation in the incident wavelength. Figure 2.8 shows the axial and the radial intensity distribution of diffracted light when the incident wavelength is shifted by ±5 nm. The 5 nm wavelength shift decreases the peak intensity to about 25 % and increases the spot size by more than 20 nm. Moreover, the focal length is shifted by about 1.3 μm. This indicates that the laser wavelength needs to be carefully tuned to the correct value to get the best result in the experiment. In addition, considering that the bandwidths of our femtosecond lasers are tens of nm, a non-negligible part of the laser power will be lost in the focusing process, making the actual focusing efficiency of the FZP lower.

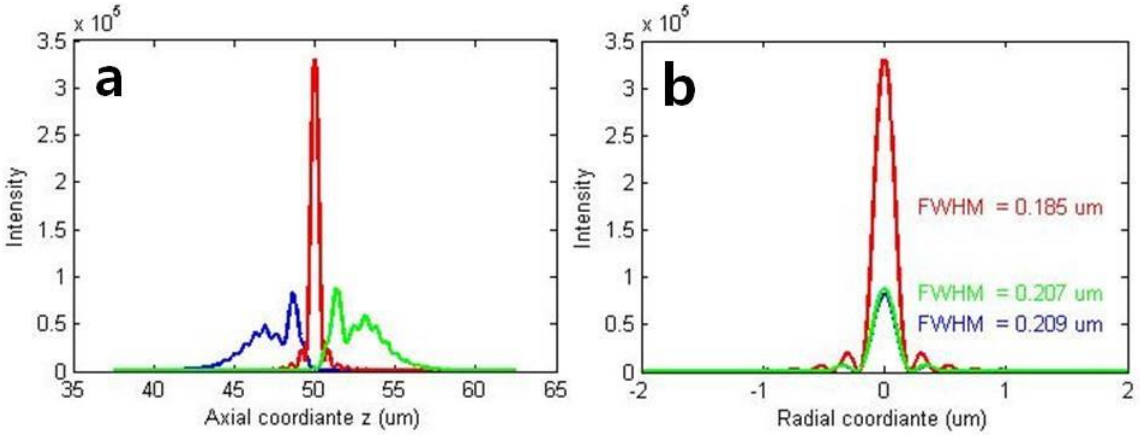

Figure 2.8. (a) Axial and (b) Radial intensity distribution of the light diffracted by the FZP designed for 400 nm and illuminated with 395 nm (green), 400 nm (red), and 405 nm (blue).

2.3 Nanowire Growth

Silicon nanowires with widths as small as 60 nm which is far below the diffraction limit are produced using the laser CVD method. By appropriately controlling experimental parameters, nanowires with different diameters and morphology can be created. Our experimental results and numerical simulation elucidate that the interference between incident laser radiation and surface-scattered radiation plays a key role in forming high-resolution nanowires. The nanowires were synthesized by James Mitchell and the numerical calculation was performed by Nan Zhou.

2.3.1 Effects of Experimental Parameters

One of the key parameters in the formation of nanowires is the polarization of the incident laser. Figure 2.9 shows the dependence of the nanowire shape on the polarization direction. When the laser was horizontally polarized, a continuous, thin nanowire was created as shown in Figure 2.9a. Vertical and 45 degree diagonal polarization directions, on the other hand, resulted in discontinuous segments of nanowires in Figure 2.9b and c, respectively. As a result, nanowires were formed parallel to the polarization direction of the incident laser. All the nanowires in Figure 2.9 were written from left to right and the writing direction had no influence on nanowire shape or orientation. It is also worth noting that the width of the nanowire in Figure 2.9a is about 60 nm which is far below the diffraction limit of the 400 nm laser. A circularly polarized light resulted in a thicker wire in Figure 2.9d. The wire is essentially an agglomerate of thinner nanowires and has a rough surface.

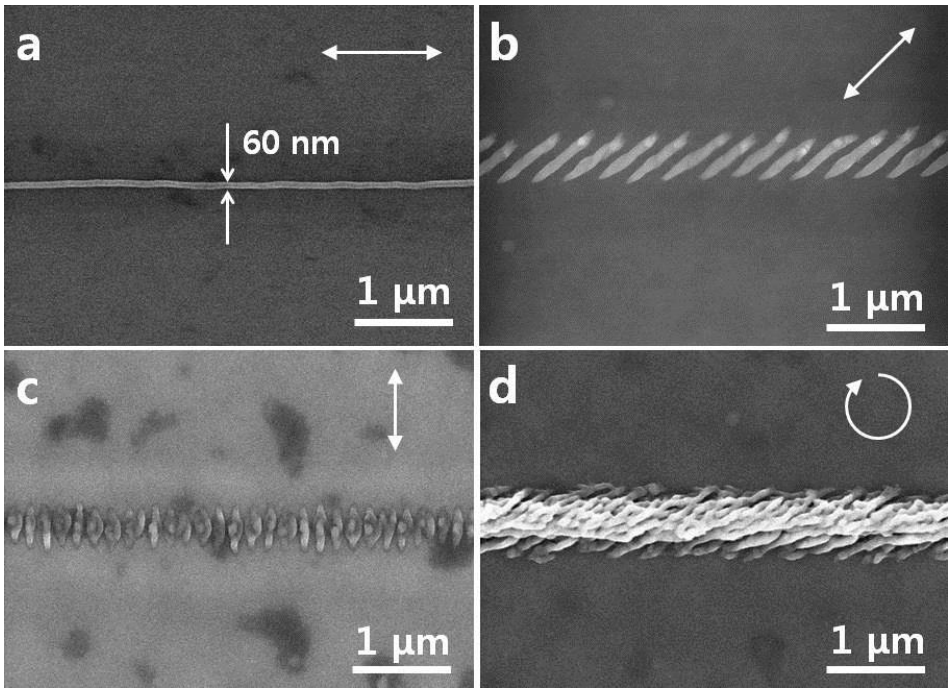

Figure 2.9. Effect of laser polarization on nanowire formation.

Another important parameter in the formation of nanowires is the power of the incident laser. Unlike polarization which affects the shape of nanowires, power determines the number and the thickness of nanowires which are formed simultaneously. For horizontally polarized laser irradiation, the number of simultaneously formed nanowires increases with a higher power as shown in Figure 2.10. A single nanowire is created at a low power (Figure 2.10a) and two or three nanowires are simultaneously formed by increasing the power (Figure 2.10b and c). As many as five nanowires were created in the experiment and the finite size of the laser spot kept the number of simultaneously formed nanowires from further increasing. As the power continues to increase, nanowires become thicker, touch each other, and a thick wire is formed instead of multiple thin nanowires. When multiple nanowires are formed, the gap distance between nanowires is not altered with the laser power. This is because thin nanowires are

created by periodic surface heating in the laser spot and this will be further discussed in Chapter 2.3.2. For circularly polarized laser irradiation, a thick nanowire was formed instead of multiple nanowires and the power controlled the thickness of the nanowires. More discussion on the effects of experimental parameters can be found in the literature (Mitchell et al., 2014).

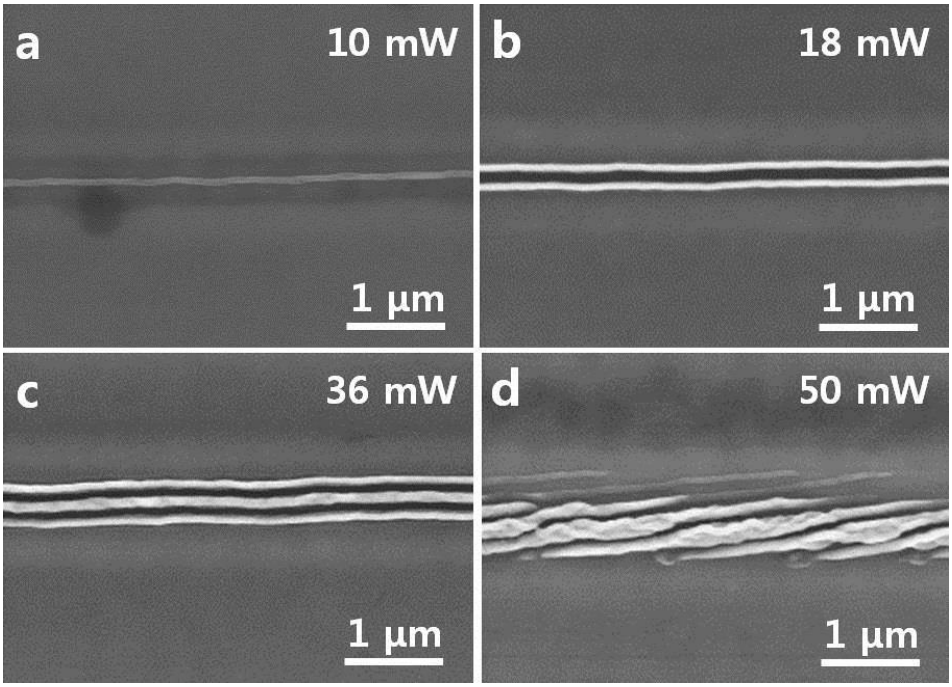

Figure 2.10. Effect of laser power on nanowire formation.

2.3.2 Explanation of Nanowire Formation

The formation of thin nanowires in our experiment has a close relation to laser induced periodic surface structures (LIPSS, ripples) which are often observed when a linearly polarized laser beam ablates a surface of a solid. According to the ratio of the ripple period (Λ) to the laser wavelength (λ), LIPSS can be divided into low spatial frequency ripples ($0.4 < \Lambda/\lambda < 1$) and high spatial frequency ripples ($\Lambda/\lambda < 0.4$) (Huang et al., 2009). For metals and semiconductors, low spatial frequency ripples are

perpendicular to laser polarization in most cases. These ripples are generally explained by interference of an incident laser beam and surface plasmons caused by the incident beam (Brueck and Ehrlich, 1982; Bonse et al., 2012). In dielectrics, low spatial frequency ripples are often parallel to laser polarization. It is widely accepted that these ripples are the result of interference between the incident radiation and surface-scattered radiation (Emmony et al., 1973; Sipe et al., 1983). It has been also reported that dielectric surfaces highly excited by high-power laser irradiation exhibit metallic behavior and formed ripples are perpendicular to the polarization direction (Huang et al, 2009). The ripple formation in this case is explained in the same way as on metal surfaces.

In order to explain the formation of our nanowires, numerical calculations were performed using the frequency-domain finite-element method (FEM). Figure 2.11 shows the $|E_x|^2$ distributions right above the silicon dioxide surface along the dashed lines in the insets. The laser fluences of 0.012 and 0.029 J/cm^2 were calculated using the laser power used in the experiment and the zone plate efficiency of 15.8 % calculated in Chapter 2.2.3. The laser beam diameter in the simulation was 250 nm and the beam center was positioned 125 nm away from the end of the nanowire as shown in the right inset of Figure 2.11b. For all simulations, the electric field polarization of the incident laser was parallel to the nanowires. Figure 2.11a shows that the interference between the incident radiation and nanowire-scattered radiation causes a central peak and two side lobes in electric field intensity. The highest intensity of the electric field was at the end of the nanowire as shown in Figure 2.11b and this indicates that the nanowire grows at the tip. The distances between the central peak and the two side lobes are about 180 nm, which is close to the distance between simultaneously formed nanowires in the experiment. As the

laser fluence increases, the field intensity at the two side lobes increases. Once the field intensity at the two side lobes becomes high enough to heat the silicon dioxide surface to the temperature required for silane decomposition, three nanowires will be simultaneously formed. Figure 2.11c shows the electric field distribution when three nanowires are formed. High intensity areas are found at the ends of the nanowires, illustrating the nanowire growth at the tip of each nanowire. The center nanowire is longer than the two side nanowires and this is also observed in the experiment (Figure 2.12).

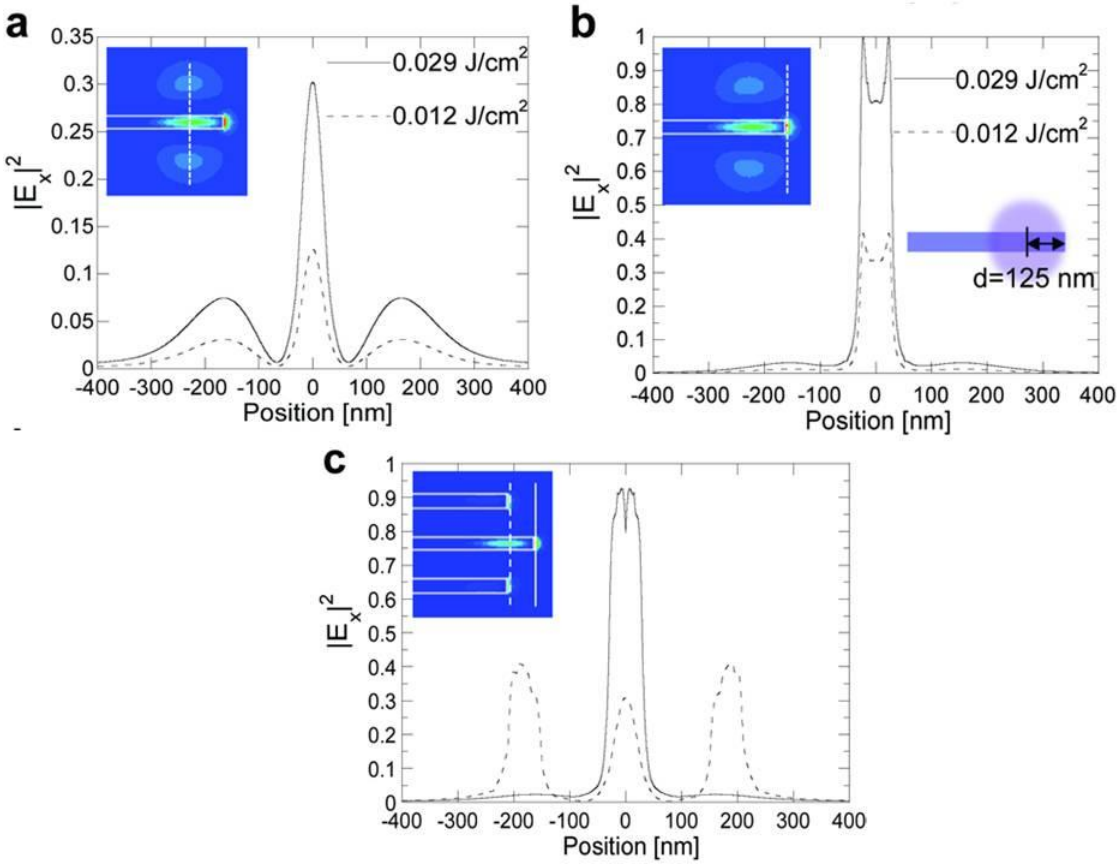

Figure 2.11. Electric field distributions during nanowire growth (Mitchell et al., 2014).

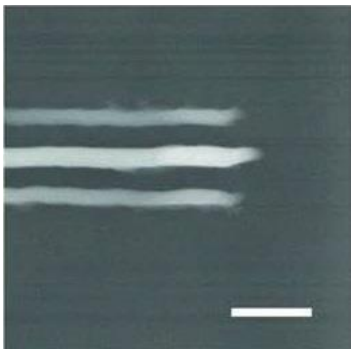

Figure 2.12. SEM image of the ends of triple nanowires. The scale bar is 400 nm (Mitchell et al., 2014).

The simulation illustrates the nanowire formation when a nanowire already exists on the laser spot. However, the beginning of the nanowire formation cannot be explained by the interference effect because there is no scattering center at first. Indeed, a large initial deposition is often observed in the experiment (Figure 2.13a) because the incident radiation heats up the oxide surface without the confinement needed for sub-diffraction limited nanowires. Figure 2.13a also shows that as the scanning continues, the wire diameter quickly decreases due to the aforementioned interference. The end of the nanowire in Figure 2.13b, on the other hand, shows no sign of large deposition because the interference is already stable.

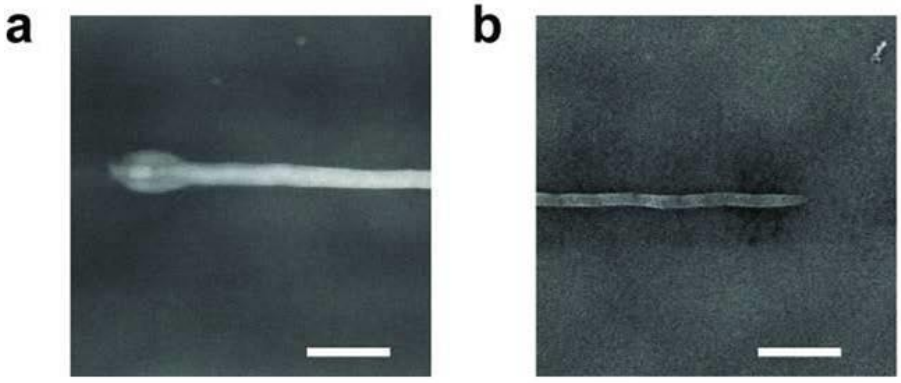

Figure 2.13. SEM images of (a) the start and (b) the end of a nanowire. The scale bars are 400 nm (Mitchell et al., 2014).

To sum up, the direct heating by the incident laser creates an unstable initial deposition of silicon. The initially deposited silicon scatters the incident laser and the interference between the incident laser beam and the scattered irradiation begins to occur. A spatially confined, periodic surface heating is generated due to the interference effect and consequently nanowires with sub-diffraction limited diameters are synthesized. It is also worth noting that the laser fluence in the experiment is far below the ablation threshold of the surface silicon oxide and therefore surface plasmons which are often mentioned as a cause of LIPSS formation plays no role in the formation of our nanowires (Mitchell et al., 2014).

2.3.3 Micro-structure of Silicon Nanowires

The laser direct written silicon nanowires were analyzed using transmission electron microscopy (TEM). Figure 2.14 shows the cross-section TEM images of an as-deposited nanowire. The nanowire has a semi-circular cross-section with a width of about 60 nm and a height of about 30 nm. No periodic atomic structure is observed in Figure 2.14b, indicating that the nanowire is composed of amorphous silicon. Figure 2.14a shows that the silicon oxide layer under the nanowire is completely intact, demonstrating that the laser irradiation during the nanowire formation causes no damage on the oxide surface. The image also shows the structure of the substrate with 200 nm thick silicon dioxide and 200 nm thick poly-Si layers. The platinum layers over the nanowire were deposited for TEM sample preparation.

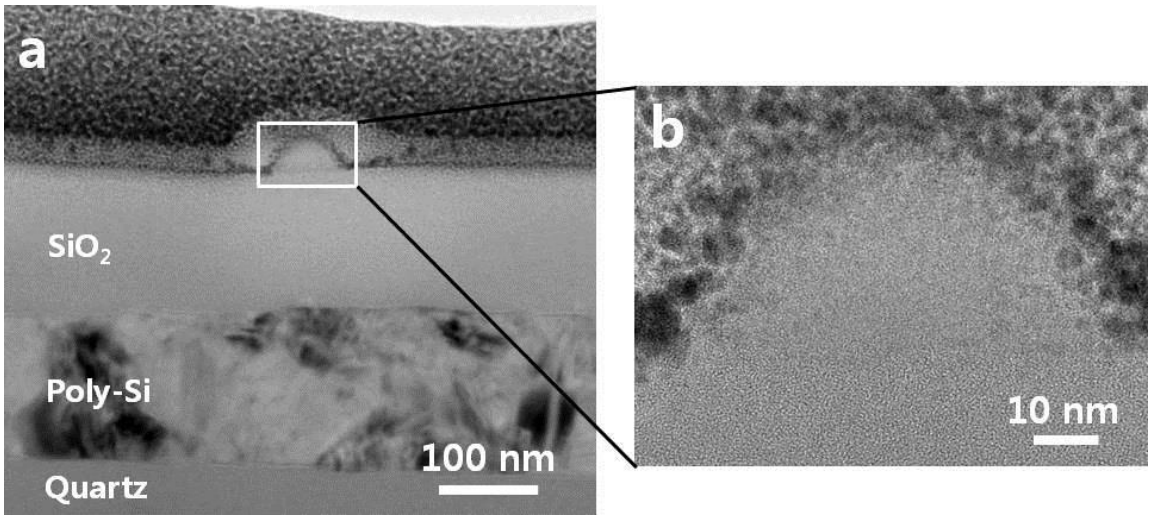

Figure 2.14. Cross-section TEM images of an as-deposited nanowire.

Although the amorphous silicon nanowire has usefulness for some applications such as thin-film transistors (TFTs) for displays, single-crystalline or polycrystalline silicon is preferred in most cases due to its superior electrical properties. In order to crystallize the amorphous nanowires, we annealed the nanowires and examined the micro-structure of the annealed nanowires using TEM. Figure 2.15a and b show the cross-section TEM images of a nanowire annealed at 700 °C for 12 hours. Small grains with diameters of 2-7 nm are observed in Figure 2.15b, indicating that the nanowire crystallized into polycrystalline silicon. Although the annealing was done with N_2 flow, the outside of the nanowire was unintentionally oxidized due to a small amount of O_2 which remained in the annealing chamber. We expect that this oxidation can be minimized by deliberately purging O_2 residue from the chamber. Figure 2.15c and d show the cross-section of a nanowire annealed at 1100 °C for 2 hours. Severe oxidation is observed on the outside of the nanowire and the diameter of the central silicon is reduced to about 20 nm. Note that the diameter of the oxidized nanowire increased and the shape of the nanowire is not

semi-circular any more because silicon expands 2.17 times in thickness when oxidized. The central silicon is single-crystalline in Figure. 2.15d. However, the nanowire is most likely to have multiple grains along the axial direction because the nanowire is tens of micrometers long.

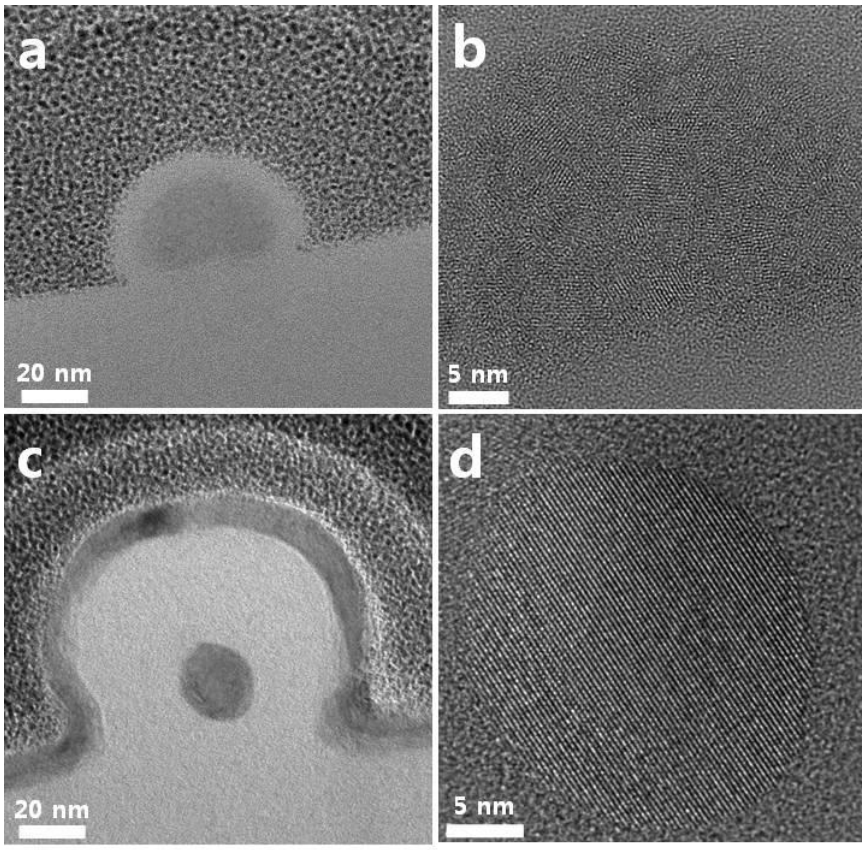

Figure 2.15. TEM cross-section images of silicon nanowires annealed (a-b) at 700 °C for 12 hours and (c-d) at 1100 °C for 2 hours.

2.4 Summary

In this chapter, the laser-direct-writing method to synthesize silicon nanowires has been described. The femtosecond pulsed lasers and optical components including filters, lenses, and frequency-doubling crystals are used to provide a spatially confined heating required for silane decomposition. The CVD system was deliberately designed to deliver

gases, control gas flow rates, and accurately move a substrate. The substrates were prepared to have Si and SiO_2 layers on quartz.

The Fresnel zone plate is one of the most important optics in the experiment which focuses the incident laser beam into a diffraction-limited spot size. In order to analyze the focusing capacity of the zone plates, the modified Rayleigh-Sommerfeld diffraction integral was used and the spot size and the efficiency of the zone plates were calculated. It was also shown that the zone plates are tolerant of fabrication errors, but sensitive to variation in the incident wavelength.

In addition, we have discussed the experimental parameters which affect the nanowire formation. The polarization direction of the incident laser is one of the parameters which determine the shape of synthesized nanowires and the laser power mainly determines the number of simultaneously formed nanowires. The experimental results and numerical calculations have explained that the interference between the incident laser and surface-scattered radiation plays a critical role in producing sub-diffraction limited nanowires. The synthesized nanowires were amorphous silicon and could be crystallized into poly-Si.

CHAPTER 3. SILICON NANOWIRE FIELD EFFECT TRANSISTOR SENSORS

Over the past decades, field effect transistor (FET) sensors, in which the surface potential of the conduction channel is modulated by charged molecules, have garnered significant research interest for chemical and biological applications. Recently, it has been shown that the use of nanoscale materials such as silicon nanowires (SiNWs) can significantly improve the sensitivity of FET sensors, allowing detection of a very low concentration of analytes (Cui et al., 2001; Stern et al., 2007). Due to the large surface-to-volume ratio, nanoscale Si FETs are expected to have excellent sensitivity (Chen et al., 2007). Label-free, direct electrical detection is another advantage of FET sensors. However, complex procedures for integrating nanowires into a nanosensor remain an obstacle for widespread applications. The "bottom up" approach requires assembly of nanowires grown from chemical vapor deposition (CVD) (Patolsky et al., 2006), which not only involves CMOS incompatible processes but also suffers from difficulty in precisely positioning nanowires. Metal contamination from catalysts used during CVD growth is another disadvantage. Alternative "top-down" methods are proposed to overcome these shortcomings, providing CMOS compatibility and precise control of nanowire position (Stern et al., 2007; Hakim et al., 2012). The "top-down" approaches require complex, multiple fabrication steps for nanowire patterning, etching, and doping.

In this chapter, we describe fabricating Si FET sensors with laser direct written silicon wires which have diameters of a few hundred nm. Our laser direct writing method enables one-step nanowire fabrication, eliminating the need for nanowire positioning, etching, and doping. The unique feature of the fabricated Si wires is that they can have very rough surfaces which are beneficial for sensing applications due to their large surface area. In addition, our approach features in situ doping, catalyst-free growth, and excellent control of position, orientation, and length. Laser direct written Si FETs were employed to detect the proton concentration (pH) of an aqueous solution.

3.1 Basic Principles of FET Sensors

Among the different types of FET sensors, ion-sensitive field-effect transistors (ISFETs) are the most fundamental sensor devices. Most of the other FET sensors can be constructed by modifying the gate of an ISFET or coupling the surface of the gate oxide with different receptors, such as antibodies, nucleic acids, and cells. The ISFET bears a close similarity to a MOSFET. The main difference between an ISFET and a MOSFET is that there is no metal gate electrode in the ISFET. Instead, a gate voltage can be applied through a reference electrode (*e.g.*, Ag/AgCl electrode) inserted in an aqueous solution which is in contact with the gate oxide in the ISFET (Figure 3.1b).

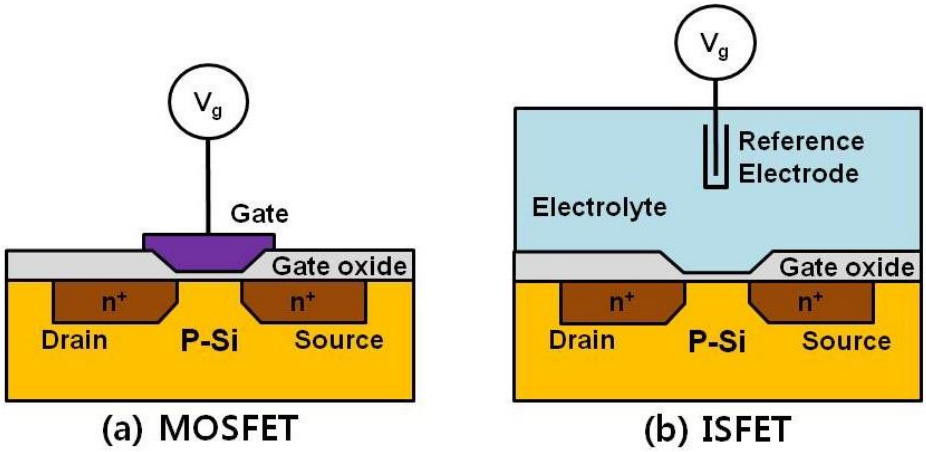

Figure 3.1. Schematic representation of (a) a MOSFET and (b) an ISFET.

Because of the similarities between an ISFET and a MOSFET, the ISFET operational mechanism is commonly described using the theoretical expressions of a MOSFET. The drain current of the MOSFET, I_d, in the non-saturated mode is given by the following equation (Sze and Ng, 2007):

$$I_d = \mu C_{ox} \frac{W}{L}\left(V_g - V_t - \frac{1}{2}V_d\right)V_d \tag{3.1}$$

where μ is the electron mobility in the channel, C_{ox} is the oxide capacitance per unit area, W and L are the width and the length of the channel, V_g is the gate voltage, V_t is the threshold voltage, and V_d is the drain-source voltage. Eq. (3.1) can be also used for an ISFET in spite of the absence of a gate electrode. In the case of an ISFET, the gate voltage, V_g, which is applied to the reference electrode creates an electric field across the electrolyte and the solution/oxide interface, and this electric field induces an inversion layer in the channel when V_g is high enough. The effects of the reference electrode and the solution/oxide interface manifest themselves in the threshold voltage, V_t. For a MOSFET, the threshold voltage, V_t, is given by

$$V_t = \frac{\Phi_M - \Phi_{Si}}{q} - \frac{Q_{ox} + Q_{ss} + Q_B}{C_{ox}} + 2\phi_f \tag{3.2}$$

where the first term means the work-function difference between the gate metal (Φ_M) and the silicon channel (Φ_{Si}), Q_{ox} is the oxide-trapped charge density, Q_{ss} is the charge density at the oxide-silicon interface, Q_B is the depletion charge density in the silicon channel, and ϕ_f is the Fermi level of the silicon from the intrinsic Fermi level which is a function of the doping concentration of the silicon. In an ISFET, the metal work-function, Φ_M, is replaced by the potential of the reference electrode, E_{ref}, the solution/oxide potential, φ, which depends on the activity of ions in the solution, and the surface dipole potential, χ_{sol}, of the solution. Therefore, the threshold voltage of the ISFET is (Bergveld, 2003)

$$V_t = E_{ref} - \varphi + \chi_{sol} - \frac{\Phi_{Si}}{q} - \frac{Q_{ox} + Q_{ss} + Q_B}{C_{ox}} + 2\phi_f \tag{3.3}$$

Finally, the drain current of the ISFET, I_d, becomes (Schöning and Poghossian, 2002)

$$I_d = \mu C_{ox} \frac{W}{L}\left[V_g - \left(E_{ref} - \varphi + \chi_{sol} - \frac{\Phi_{Si}}{q} - \frac{Q_{ox} + Q_{ss} + Q_B}{C_{ox}} + 2\phi_f\right) - \frac{1}{2}V_d\right]V_d \tag{3.4}$$

The interface potential, φ, can be changed chemically, for example, by changing the pH of the solution and this means that the threshold voltage, V_t, and correspondingly the drain current, I_d, can be altered chemically without changing the applied voltages.

In the case of pH sensors, hydroxyl groups (-OH) on the oxide surface act as active sites which are able to bind or release hydrogen ions in an electrolyte. The hydroxyl groups can be neutral, protonized or deprotonized depending on the pH of the solution (Figure 3.2). They are positively charged when protonized to OH_2^+ and negatively

charged when deprotonated to O^-. Therefore, the pH of the surrounding solution changes the amount of the surface charges and consequently the solution/oxide interface potential, φ. The pH dependence of the interface potential, φ, is described by the site-binding theory (Bousse et al., 1983):

$$\varphi = 2.303\frac{kT}{q}\frac{\beta}{\beta+1}(pH_{pzc} - pH) \tag{3.5}$$

with k as the Boltzmann constant, T as the absolute temperature, β as a dimensionless sensitivity parameter which is dependent on the density of surface hydroxyl groups and the surface reactivity, and pH_{pzc} as the pH at the point of zero charge. According to Eq. (3.4) and (3.5), a change in pH induces an alteration in the channel conductance and consequently the drain current, I_d. Thus, the pH value of the test solution can be determined by measuring the drain current of the ISFET.

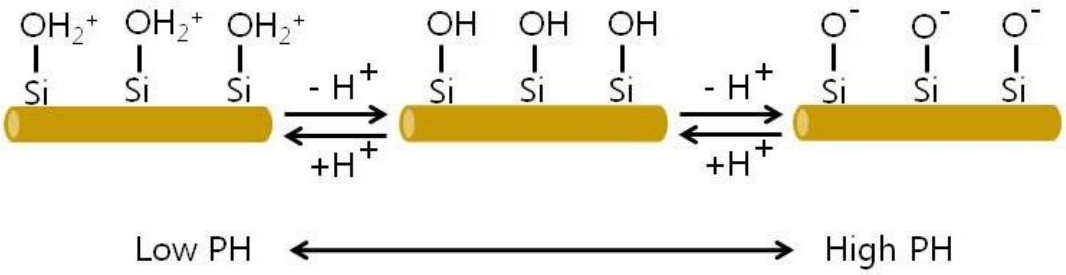

Figure 3.2. Protonation and deprotonation of hydroxyl groups in an aqueous solution.

Since the ISFET is very sensitive to an electrical interaction near the gate insulator surface, the sensor device can be used to detect a chemical or biological reaction leading to a potential change near the gate insulator surface. To this end, the surface of an ISFET is, in general, functionalized with chemical or biological receptors. Depending on the type of receptors used, the mechanism of potential generation is different. For example,

an antigen-antibody affinity reaction or DNA hybridization will cause a surface polarization effect which affects the surface potential, whereas potential changes are caused by a catalytic reaction product on an enzyme-modified surface. However, the basic principles for an ISFET discussed in this chapter can be applied to most FET-based sensors.

3.2 Laser Direct Writing of Silicon Wires for FET Sensors

Silicon nanowires for FET sensors were synthesized using the laser direct writing method discussed in Chapter 2. The silicon nanowires were created using circularly polarized laser light at a pressure between 30 and 40 Torr with flow of 10 % silane in argon and 100 ppm diborane in hydrogen. In order to obtain a low doping concentration desirable for high sensitivity (Nair and Alam, 2007), we lightly doped the Si nanowires with a SiH_4:B_2H_6 mass flow ratio of 6,000:1. Figure 3.3 shows the SEM images of Si nanowires synthesized for FET sensors. The diameters of the nanowires are between 300 and 500 nm and they have rough surfaces which are desirable for high sensitivity due to their large surface areas. The nanowire in Figure 3.3a is an agglomerate of 70 nm-thick nanowires as shown in the upper inset of Figure 3.3a. Using the cross section in the lower inset of Figure 3.3a, we calculated the surface-to-volume ratio of the nanowire to be 1.4 times that of a smooth, cylindrical wire of the same thickness. However, if we consider the 350 nm wire consisting of strands of 70 nm wires, which is closer to what is shown in the upper inset of Figure 3.3a, the surface-to-volume ratio will be about 5 times that of the smooth nanowire. Therefore, the actual surface-to-volume ratio can be between 1.4 and 5 times that of a smooth wire.

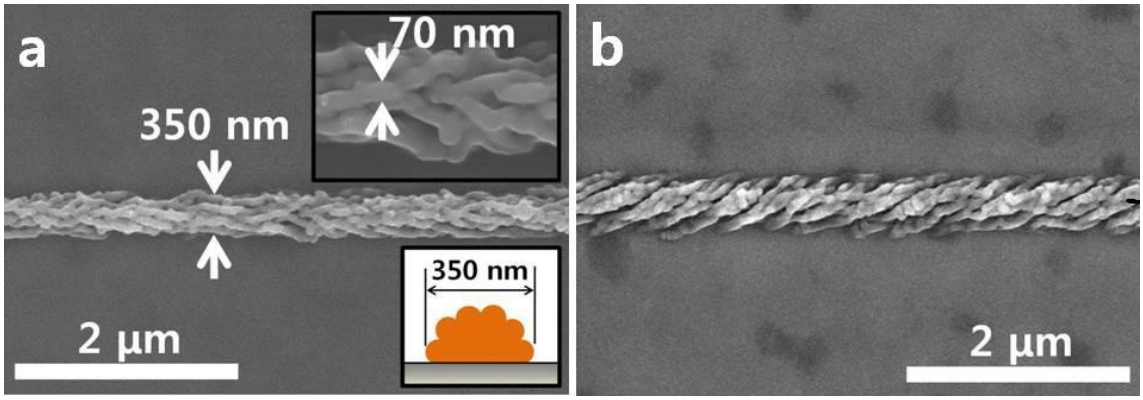

Figure 3.3. SEM images of laser direct written silicon wires (Nam et al., 2013).

3.3 Fabrication of Silicon Nanowire FET Sensors

The laser direct written silicon nanowires were annealed at 1000 °C in argon for 30 minutes to crystallize and activate dopant atoms. Source/drain contacts were then patterned using photolithography. AZ1518 photoresist and a Suss MJB-3 mask aligner were used for the photolithography. The photoresist-patterned device chip was treated with O_2 plasma to remove a photoresist residue in the exposed area and etched in buffered oxide etch for 5 seconds to remove native oxide on the silicon surface. Subsequently, a 100 nm-thick Ni layer was deposited using electron beam evaporation and source/drain contacts were created with a liftoff process. The metalized nanosensors were annealed using rapid thermal annealing at 400 °C in forming gas (4 % H_2/ 96 % N_2) for 2 minutes to form low-resistance NiSi contacts at the interfaces between the Si wires and the Ni electrodes (Patolsky et al., 2006).

Since the sensor devices operate in contact with an aqueous solution, it is essential to have a passivation layer on the device surface which prevents Ni electrodes from undergoing electrochemical corrosion in the solution. A combination of Si_3N_4 and SU8 layers was first tested for the passivation layer. A pattern for a liftoff of Si_3N_4 was created

using AZ1518 photoresist and photolithography. Then, 100-200 nm thick Si_3N_4 was deposited using plasma-enhanced CVD at a low temperature of 95 °C to avoid thermal deformation of the photoresist as well as to facilitate the liftoff. Finally, an SU8 layer was deposited and patterned (Figure 3.4a). Although the passivation layers of Si_3N_4 and SU8 effectively protected most of the Ni electrodes, an electrochemical corrosion was observed near the silicon channel (Figure 3.4b), which is near the open edge of the passivation layers, after an extended operation of the device in a solution. This indicates that the Si_3N_4 coating was not conformal and the aqueous solution leaked into the electrodes because of the poor adhesion between SU8 and the underlying layer.

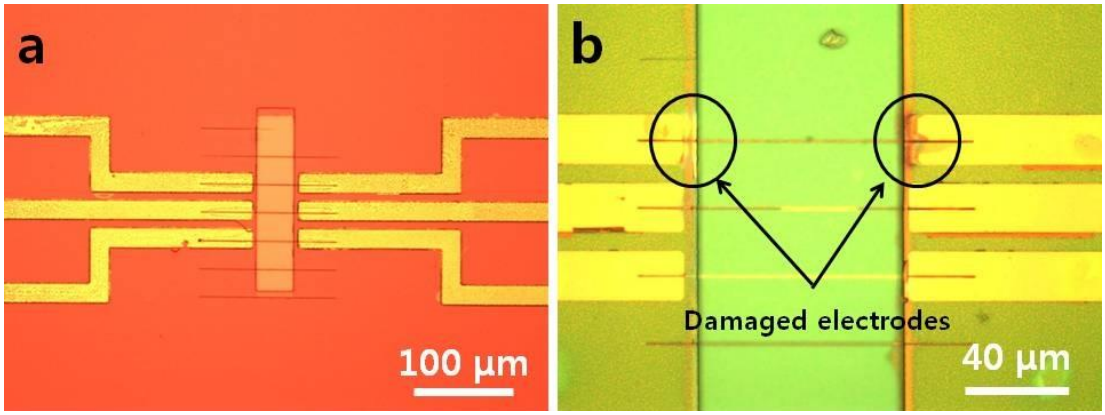

Figure 3.4. Optical images of (a) a Si FET sensor device with Si_3N_4 and SU8 passivation layers and (b) electrochemically damaged electrodes after a pH sensing experiment.

AZ1518 photoresist was also tested for the passivation layer because of its excellent adhesion to the SiO_2 substrate. The AZ1518 photoresist was patterned and baked at 120 °C for 30 minutes. Although an increase in gate leakage current was detected when a high gate voltage was applied to the reference electrode, the AZ1518 passivation layer kept the gate leakage current very small at a low gate voltage and suppressed the corrosion of the Ni electrodes effectively. Therefore, AZ1518 passivation was used for

FET sensors in the following chapters. Figure 3.5a shows an optical image of a typical device with four Si wires aligned horizontally. In the device, the separation between source/drain contacts is 20 μm and the width of the vertical channel exposed to an electrolyte solution in the pH sensing experiment is 10 μm. The device fabrication procedure is illustrated in Figure 3.6.

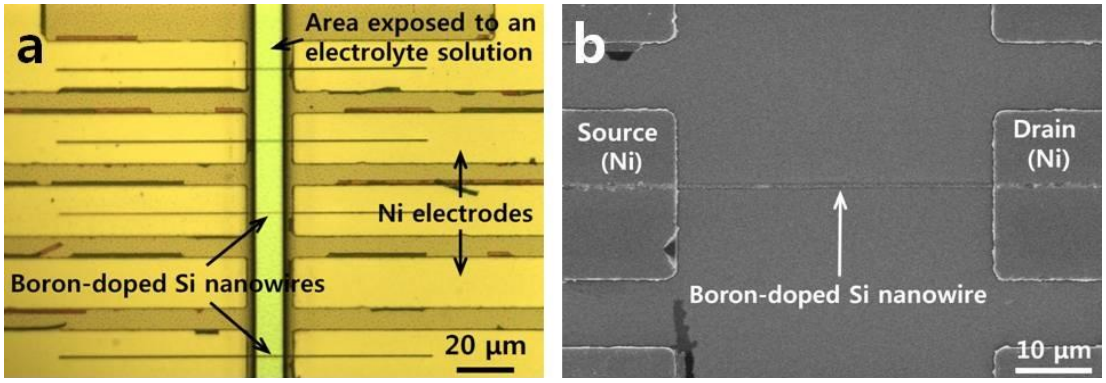

Figure 3.5. (a) Optical image of a laser direct written Si FET sensor. (b) SEM image of a Si FET sensor without a passivation layer.

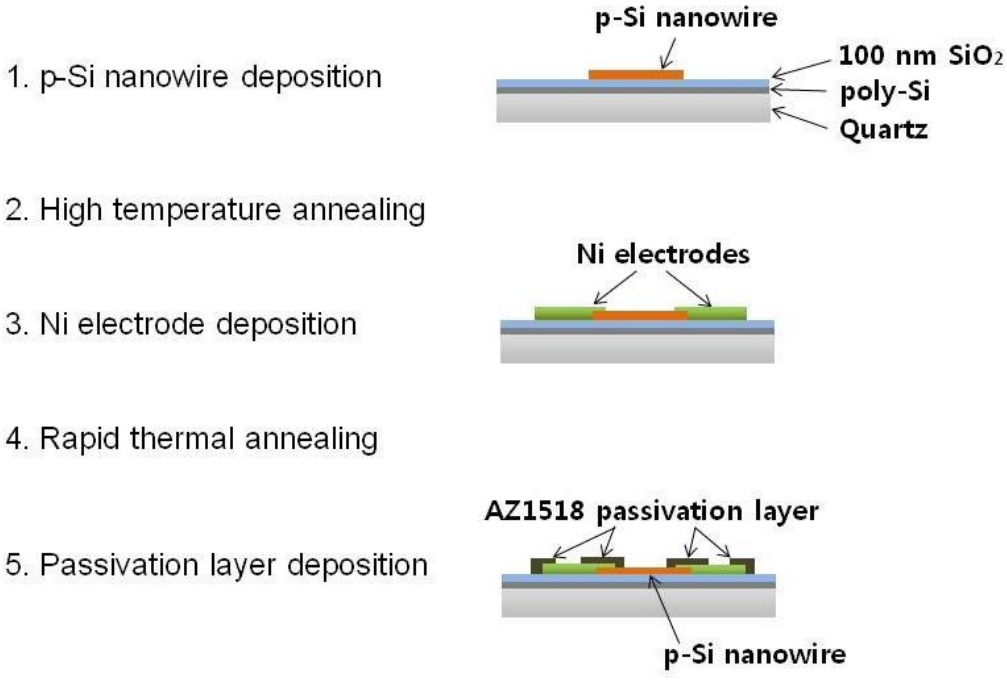

Figure 3.6. Schematic illustration of the device fabrication procedure.

3.4 Experimental Setup for pH Sensing Tests

Two different experimental setups were used for the pH sensing experiment. For the real-time measurement of the drain current, an HP 4140B pA meter was used to apply a drain voltage and measure the consequent drain current. The current meter was connected to a computer and controlled by a custom-written Labview program. Standard pH buffer solutions (pH 3-10) were purchased from EMD Chemicals, Inc. and a syringe pump delivered pH solutions to an FET sensor at a constant flow rate of 50 μL/min. A custom-made PDMS microfluidic channel with a volume of about 2 μL was placed on the sensor surface to hold pH solutions. The measurement setup is shown in Figure 3.7.

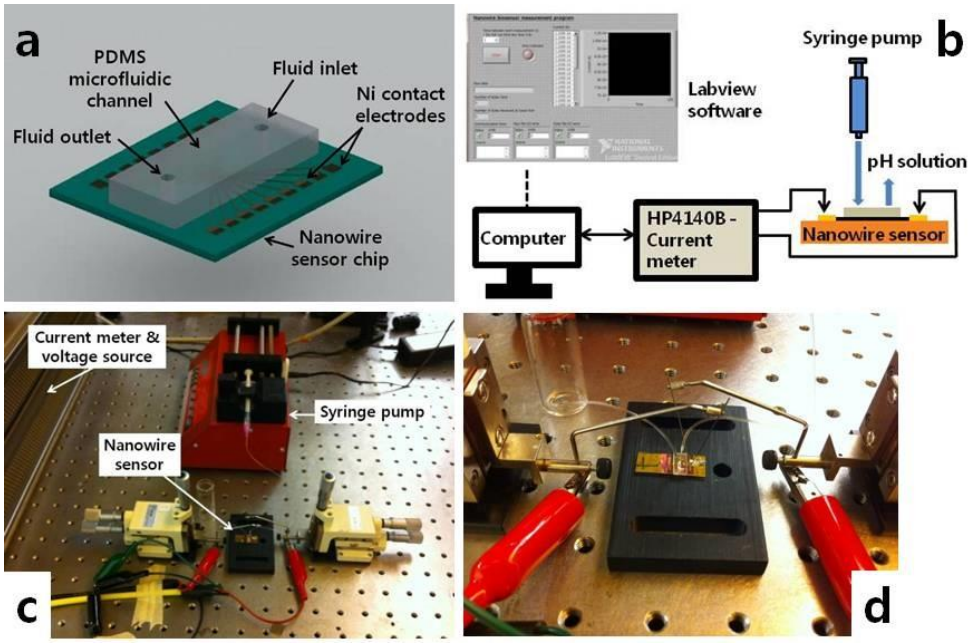

Figure 3.7. (a) Schematic of an FET sensor chip with a microfluidic channel. (b) Schematic of the experimental setup for a real-time pH sensing test. (c-d) Images of the measurement setup with a fabricated sensor device.

To measure a device response to gate voltage, we used the solution-gate approach where a gate voltage is applied by a reference electrode immersed in electrolyte. A

reference electrode is commonly used in electrochemical experiments since it has a stable electrode potential due to the employment of a redox system. Figure 3.8a shows an Ag/AgCl reference electrode (RE-5E, BASi) which is used in our experiment. In the reference electrode, an Ag wire completely covered with AgCl is immersed in a 3 M sodium chloride solution and a porous frit at the bottom separates the salt solution from an analyte solution while it allows ionic conduction between the two solutions. A custom-made solution reservoir made of silicon rubber was placed on the sensor chip to hold pH solutions. Electrical measurement was performed at room temperature on a probe-station with a Kiethley 4200-SCS semiconductor parameter analyzer and the low-frequency noise in our device was measured using an Agilent 35670A spectrum analyzer. Figure 3.8b shows the experimental setup with an FET sensor, the reference electrode, the solution reservoir, and the probe station.

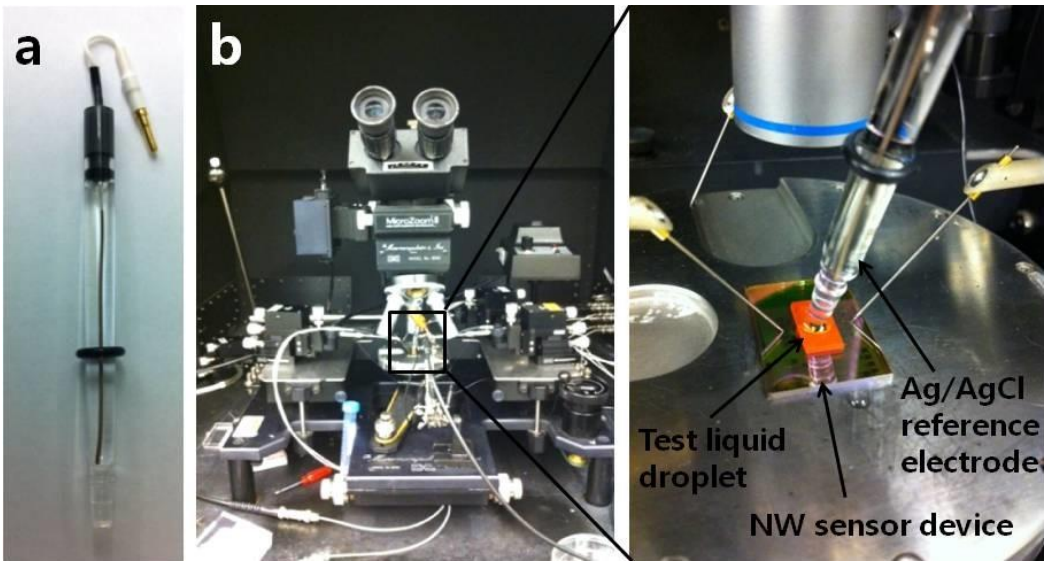

Figure 3.8. (a) Ag/AgCl reference electrode and (b) Images of the experimental setup to measure device response to gate voltage.

3.5 Electrical Characterization of pH Sensors

The transport characteristics of the fabricated FET sensors were studied before and after the rapid thermal annealing. In our devices, Ni was used for source and drain contacts because nickel silicides, which are formed by thermal annealing described in Chapter 3.3, have a low hole Schottky barrier height of ~0.4 eV (Bucher et al., 1986; Sze and Ng, 2007). Figure 3.9 shows the drain current, I_D, versus the source-drain voltage, V_D, behavior of a typical sensor device before and after thermal annealing. The curves become more linear and the conductance is about 2.7 times greater after annealing. This increased conductance is attributed to the Ni-SiNW contacts which were improved with silicide formation.

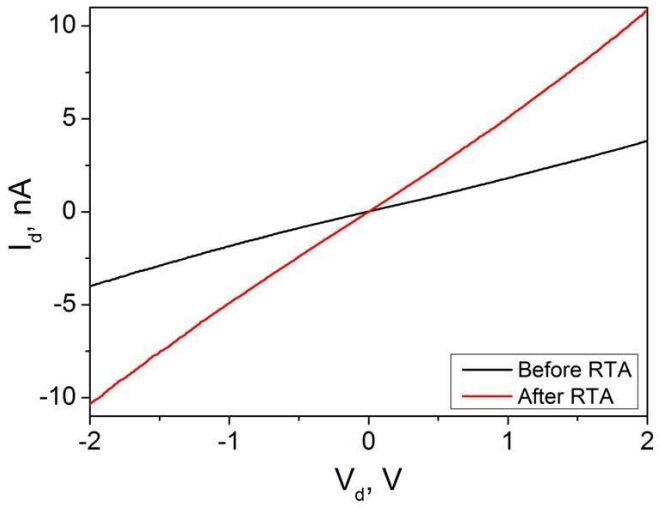

Figure 3.9. I_D-V_D characteristics on the same device before and after thermal annealing.

To demonstrate pH sensing, we tested the FET sensors in pH solutions. Figure 3.10a shows the drain current (I_D) dependence on the gate voltage (V_G) with a constant drain voltage (V_D) of 100 mV in solutions with pH values varying from 3 to 10. Consistent with p-type accumulation behavior, the conductance of the device increases with a

negative gate voltage. As pH increases, the source-drain conduction increases as well. This is the expected behavior of a p-type Si FET. Hydroxyl (-OH) groups on the oxide can be protonated or deprotonated in electrolyte depending on the pH value of the solution, which causes changes in the surface charge. As a result of the additional gating effect from the surface charges, hole carriers in the p-type Si wire are depleted and the conductance of the wire decreases at low pH, and vice versa, at high pH. Figure 3.10b shows the drain current (I_D) versus the drain voltage (V_D) with a constant gate voltage (V_G) of -1 V at different pH values. The I_D value at V_D = 0.5 V increases from 0.6 nA at pH 3 to 4.9 nA at pH 9, demonstrating that our device is highly sensitive to solution pH. The small nonlinearity observed in the I_D-V_D curves is attributed to slightly non-ohmic contacts between the Si wire and the source/drain electrodes. During the measurement, the leakage current in aqueous solution between gate and source/drain electrodes was kept smaller than 0.02 nA, which indicates that the passivation layer over the source/drain electrodes effectively suppressed the gate leakage. However, the leakage current started to increase when V_G became smaller than -1 V.

According to Eq. (3.5) which describes the electrostatic potential drop, φ, at the electrolyte-oxide interface, a change in pH induces an alteration of the surface potential of the Si wire, thus causing a shift in the I_D-V_G curve. The prefactor in Eq. (3.5) is the well-known Nernst value of 59 mV/pH, which usually limits the maximum shift of the I_D-V_G curve (Knopfmacher et al., 2010). In Figure 3.10a, parallel shifts of the I_D-V_G curves are observed. By comparing V_G values of the curves at a constant I_D of 0.2 nA, we roughly estimate the shift of the curves between pH 6 and 10 to be ~48 mV/pH, which is

in good agreement with previously reported values for solution-gated pH sensors (Knopfmacher et al., 2010).

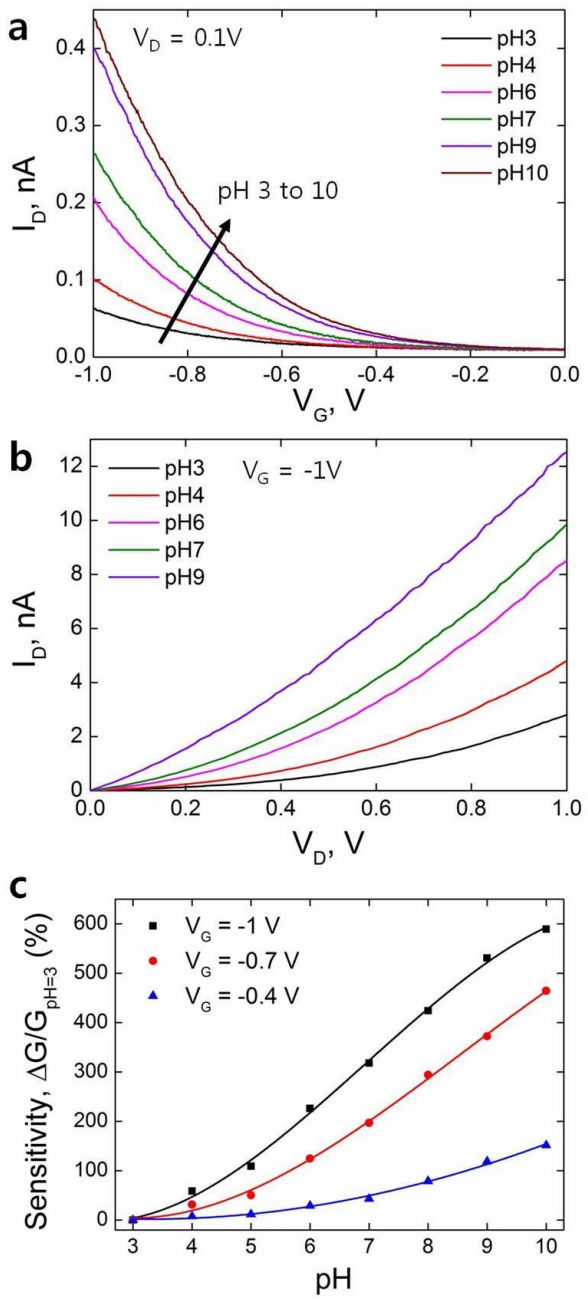

Figure 3.10. Electrical response of a laser direct written Si FET sensor in different pH solutions. (a) I_D-V_G characteristics with a constant V_D of 0.1 V at pH values ranging from 3 to 10. (b) I_D-V_D characteristics with a constant V_G of -1 V at pH values ranging from 3 to 9. (c) Device sensitivity as a function of pH value at V_G = -1, -0.7, and -0.4 V. Solid lines are a guide for the eye.

The sensitivity of a Si FET sensor is defined as the normalized conductance change, $\Delta G/G_0 = (G - G_0)/G_0$ (Stern et al., 2007; Nair and Alam, 2007; Gao et al., 2010). Figure 3.10c shows the sensitivity of our device, $\Delta G/G = (G - G_{pH=3})/G_{pH=3}$, as a function of pH at different V_G values. $\Delta G/G$ is about 150 % at pH 10 with V_G = -0.4 V and increases as V_G becomes more negative. With V_G = -1 V, $\Delta G/G$ is about 600 % at pH 10, which is comparable or superior to those reported for sensors made from CVD grown nanowires. Cui et al. (2001), for example, reported ~100 % of $\Delta G/G$ between pH 2 and 9, while Gao et al. (2010) reported ~600 % between pH 4 and 9. We believe that the high sensitivity of our sensor is due to the rough surface and the low doping concentration of the Si wire. Since the Debye screening length of silicon, $L_D = (\varepsilon_{Si} kT / q^2 N_A)^{1/2}$, is longer as the doping concentration, N_A, is lower (Sze and Ng, 2007), the reduced screening of carriers in the Si wire makes the gating effect of ions on the surface more effective. Considering that FET nanosensors are known to have lower sensitivity in the linear transport regime (Gao et al., 2010), if V_G further decreases to the linear regime, $\Delta G/G$ is expected to decrease. Thus, operating the nanosensor with a proper gate voltage is another important factor for high sensitivity.

Figure 3.11 shows the real-time response of our FET sensor to different pH solutions. The drain current, I_D, increases at pH 8.9 and decreases at pH 4, which is consistent with the results in Figure 3.10. The large noise level in the drain current, which is not observed in Figure 3.10, is believed to be due to external factors, such as a manual switch of the pH solutions during the experiment and poor contacts between the device and the measurement setup. Therefore, we believe that the noise level can be minimized by a

careful modification of the experimental setup. The overall current in Figure 3.11 slowly increases over time. This drift is most likely due to the electrochemical reaction of the Ni contacts of the sensor. We observed electrochemical damage to the Ni contacts after a prolonged period of operation and thus the measurement result can be reproduced for only several hours in our sensors.

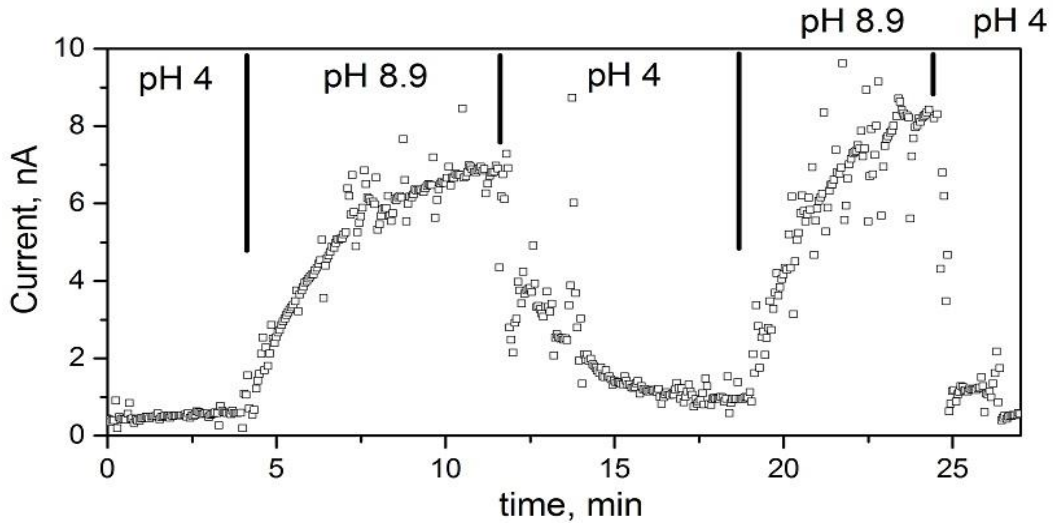

Figure 3.11. Real-time response of a laser direct written Si FET sensor to different pH solutions.

To check the intrinsic detection limit of our sensors, the signal-to-noise ratio (SNR) of the same FET sensor used for Figure 3.10 was obtained by measuring the low-frequency noise of the device. The SNR can be given by (Rajan et al., 2011)

$$SNR = \frac{\Delta\psi_0}{\sqrt{\ln(f_2 / f_1)}} \frac{g_m(V_G)}{\sqrt{S_I(f = 1Hz)}} \tag{3.6}$$

where f_1 and f_2 are two corner frequencies of the measurement bandwidth, $\Delta\psi_0$ is the measured shift of the surface potential on the Si wire, S_I is the current noise power spectral density, and g_m is the transconductance. Since f_1 and f_2 mean the measurement

bandwidth of the sensor, we will consider $\ln(f_2 / f_1)$ to be 1 for the sake of definiteness (Helbling et al., 2010). The voltage noise power spectral density, S_V, was measured with V_D = 0.1 V and V_G = -1 V in a pH 6 solution (titrated using sodium hydroxide from 50 mM potassium hydrogen phthalate, the Debye length (Israelachvili, 2011), λ_D = ~0.85 nm) and is shown in Figure 3.12. S_I at 1 Hz was calculated to be 9.4×10^{-26} A^2/Hz from the relation $S_I = S_V / R^2$ and R = 483 MΩ. Using $\Delta\psi_0 =$ 48 mV/pH and g_m = 1.02 nS, the SNR of our device was determined to be ~160/pH and this corresponds to the noise equivalent pH change of 0.006. Therefore, the detection limit of our sensor is 0.6 % of a pH change. The denominator in Eq. (3.6) is the root-mean-square current noise amplitude (Rajan et al., 2011), which can be used as a direct indication of the error in our device, and is calculated to be 3.1×10^{-13} A at V_D = 0.1 V and V_G = -1 V.

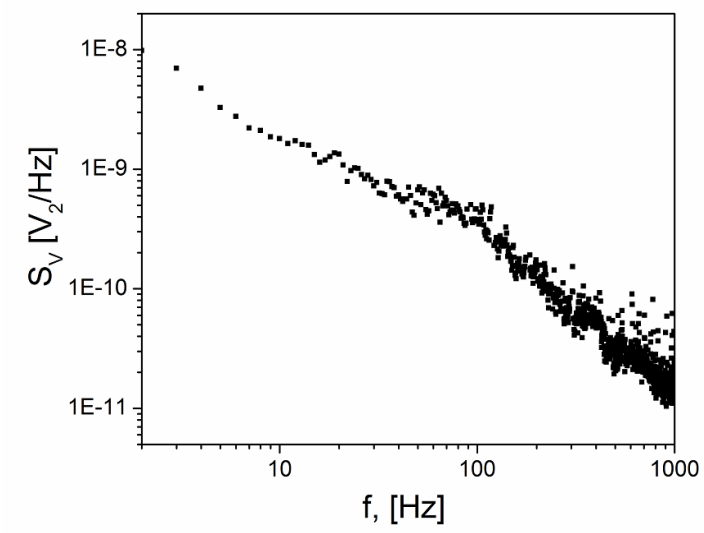

Figure 3.12. Noise power spectral density of the voltage fluctuation S_V obtained with V_D = 0.1 V and V_G = -1 V in a pH 6 solution.

3.6 Summary

In this chapter, we have demonstrated laser direct written Si FET sensors for pH detection. Our approach utilizes a laser to fabricate p-type Si wires at a desired location on an insulating surface, simplifying overall fabrication processes and thus facilitating integration of Si wires into sensor devices. These wires were rough, and therefore even if the diameters of the wires are ~300 nm, they still provide a large surface area for high sensitivity. The laser direct written Si wires were fabricated into FET sensors using standard micro-fabrication techniques. Ni was used for metal contacts and AZ1518 photoresist was used for device passivation. The fabricated Si FET sensors were tested in pH solutions with an Ag/AgCl reference electrode as a gate and shown to have excellent sensitivity to solution pH. We expect that our approach can be easily extended for other sensing applications by proper surface functionalization.

CHAPTER 4. SILICON NANOWIRE FIELD EFFECT TRANSISTORS

Laser-direct-written silicon nanowires can be used as building blocks for nanoscale electronic devices. This chapter will discuss the application of our nanowires to field effect transistors (FETs). Back-gated silicon nanowire (SiNW) FETs which have been fabricated using p- or n-type nanowires will be discussed. Top-gated SiNW FETs have been also fabricated using p-type nanowires and electrically characterized.

4.1 Basic Principles of FETs

Simplified cross sections of a metal-oxide-semiconductor field effect transistor (MOSFET) and a Schottky-barrier field effect transistor (SBFET) are shown in Figure 4.1. A transistor is, in general, a three-terminal device where the conductance of the silicon channel between the source and the drain is controlled by the gate. In many cases, a contact to the substrate is added as a fourth terminal as well. The difference between a conventional MOSFET and a SBFET is the existence of p-n junctions at the ends of the channel. As shown in Figure 4.1a, the source and drain of a MOSFET are highly doped and current flow in the off-state is limited by the p-n junctions at the interfaces between the channel and the source/drain. When the device is turned on, an inversion channel is created at the interface of the channel and the gate oxide and current flows through the inversion channel. On the other hand, a SBFET has metallic source/drain contacts and

therefore no p-n junctions as shown in Figure 4.1b. Current flow in the off-state is limited by the Schottky barriers at the interfaces between the Si channel and the metallic source/drain contacts. When the SBFET is turned on, the Schottky barriers become thinner, an inversion or accumulation channel is formed at the interface of the Si channel and the gate oxide, and therefore current flows between the source and drain contacts.

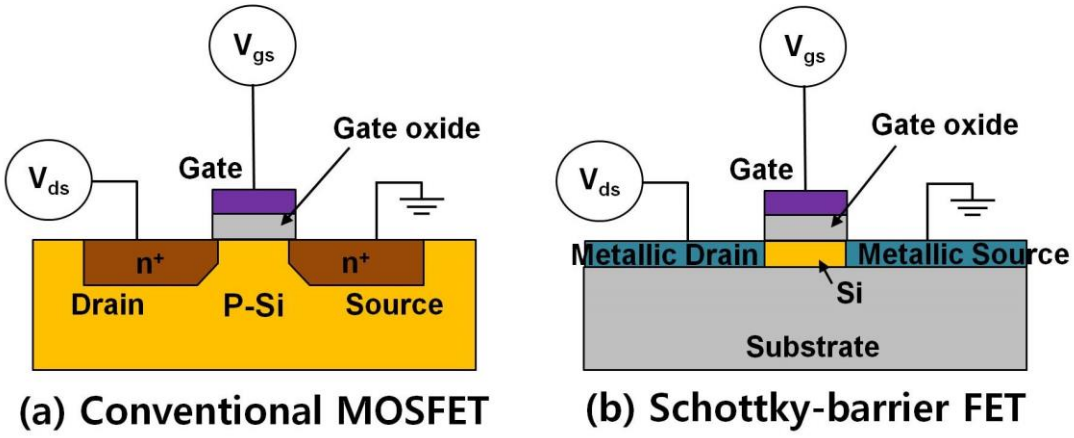

Figure 4.1. Schematic representation of (a) a conventional MOSFET and (b) a Schottky-barrier FET.

The versions of FETs can be categorized using the type of the channel carriers. When the channel carriers in the on-state are electrons, the device is an n-channel device and more conductive with more positive gate bias. If holes are the channel carriers in the on-state, the FET is a p-channel device and more conductive with more negative gate bias. Note that negative drain and gate voltages are applied to make a p-channel device more conductive. In result, negative drain current is measured in a p-channel device. Typical *I-V* characteristics of p- and n-channel devices are summarized in Figure 4.2.

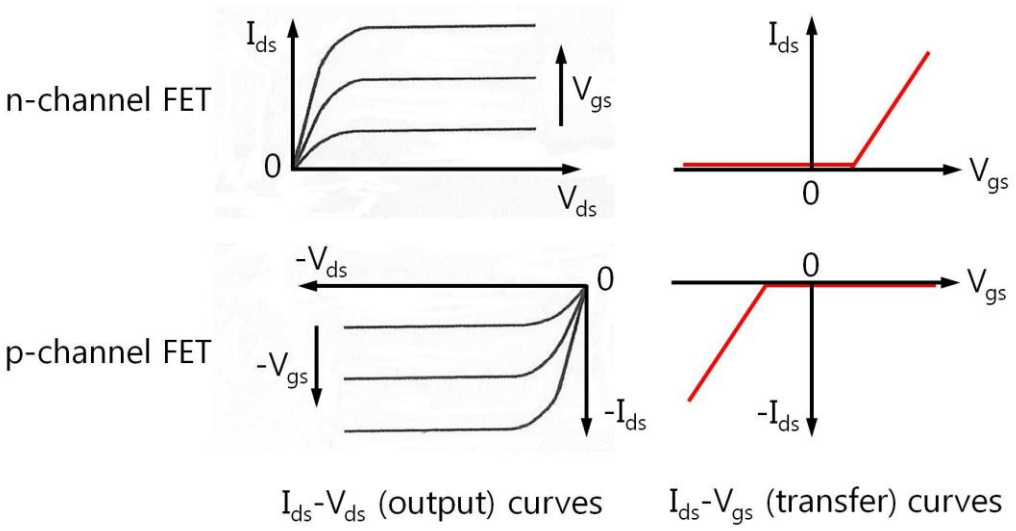

Figure 4.2. Output and transfer characteristics of p- and n-channel FETs (Sze and Ng, 2007).

4.2 Laser Direct Writing of Silicon Nanowires for FETs

Silicon nanowires for FETs were synthesized using the laser direct writing method discussed in Chapter 2. Unlike in Chapter 3 where nanowires with a diameter of a few hundreds of nm were used, nanowires as thin as about 60 nm were used in this chapter. The incident laser was horizontally polarized to enable the formation of the thin nanowires with the interference effect discussed in Chapter 2.3.2. P-type nanowires were synthesized using 500 ppm diborane (B_2H_6) as a dopant gas and the mass flow rate of SiH_4:B_2H_6 was between 1:1 and 500:1, which corresponds to a concentration ratio between 200:1 and 100,000:1. N-type nanowires were created using 100 ppm phosphine (PH_3) with a SiH_4:PH_3 mass flow rate between 2:1 and 50:1, which corresponds to a concentration ratio between 2,000:1 and 50,000:1. The scan speed was 0.5 μm/s. Figures 4.3a and 4.3b show the SEM images of p-type and n-type nanowires, respectively. The

nanowires look similar to each other, indicating that the dopant gases have little effect on the morphology and the diameter of the nanowires.

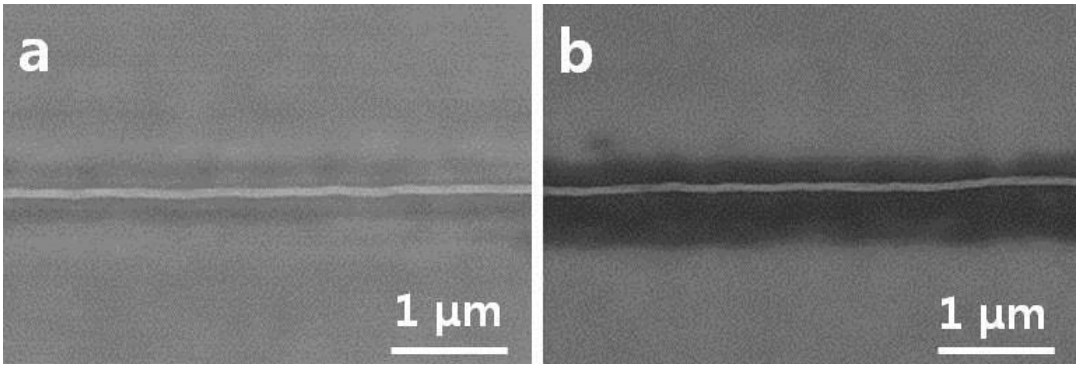

Figure 4.3. SEM images of (a) a boron-doped nanowire and (b) a phosphorus-doped nanowire.

4.3 Fabrication of Silicon Nanowire FETs

Both back-gated and top-gated FETs were constructed with laser-direct-written silicon nanowires. In order to utilize the poly-Si layer under the SiO_2 layer in the substrate as a back gate, we doped the poly-Si layer with phosphorus using ion implantation. The ion implantation was performed at 50 keV with an implant dose of 5 x 10^{14} ions/cm^2 by CuttingEdge Ions, LLC. The final doping concentration of the poly-Si layer will be between 1.4 and 2.5 x 10^{19} cm^{-3} after the high temperature oxidation explained in Chapter 2.1.3. Figure 4.4 shows the schematics of our device structure.

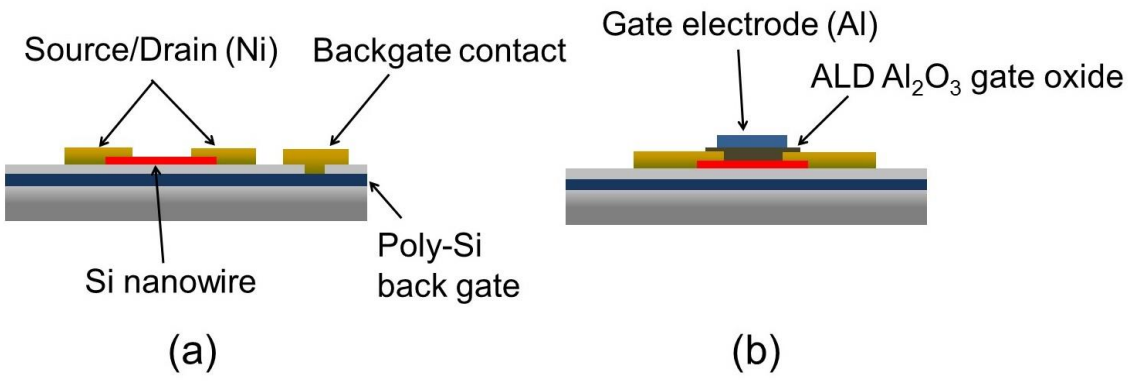

Figure 4.4. Schematics of (a) a back-gated SiNW FET and (b) a top-gated SiNW FET.

The laser-direct-written silicon nanowires were first annealed at a high temperature in N_2 to crystallize and activate dopant atoms. The annealing conditions were 6 hours at 800 °C, 12 hours at 700 °C, or 15 – 20 hours at 650 °C. Different annealing conditions will result in differences in grain sizes and the degree of crystallization. The annealing chamber was purged with N_2 for 1 hour before increasing temperature to avoid thermal oxidation of the nanowires. The annealed nanowires were etched in 10:1 HF for 20 seconds to remove the surface oxide. Alignment marks and a coordinate system, which will be used to locate nanowires, were created using electron beam lithography (EBL) and a liftoff process. The coordinate system consists of a few μm-sized squares which are located every 50 μm and 5 μm-sized squares were used as the alignment marks. Poly(methyl methacrylate) (PMMA) and a Leica VB6 were used for the EBL. Since our substrate is made of quartz which is insulating, we spin-coated the PMMA-coated sample with AquaSave 53za (Mitsubishi Rayon), which is a conducting polymer, to avoid charging effects during the EBL process. Subsequently, 5 nm titanium and 80 nm gold were deposited using an electron beam evaporator. For back-gated devices, contacts to

the underlying poly-Si layer were patterned using EBL and the 200 nm-thick SiO_2 layer was etched in 6:1 buffered oxide etch (BOE) for 3 minutes. Source/drain contacts were then patterned and a 100 nm-thick Ni layer was deposited using electron beam evaporation. Immediately before the Ni deposition, the PMMA-patterned device chip was treated with O_2 plasma to remove a PMMA residue in the exposed area and etched in BOE for 5 seconds to remove native oxide on the silicon surface. The metalized devices were annealed using rapid thermal annealing at 350 °C for 1 minute in forming gas (4% H_2/96 % N_2) to form nickel silicide at the Ni-Si interfaces. In the Ni-Si reaction, Ni is the dominant diffusing species (Tang et al., 2012) and the growth of nickel silicide from S/D Ni electrodes is observed in our devices (Figure 4.5). The diffusion length of Ni into the nanowire channel was between 100 and 110 nm after the rapid thermal annealing.

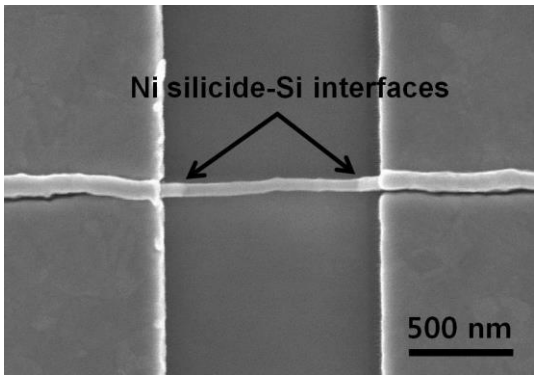

Figure 4.5. SEM image showing the formation of nickel silicide.

For top-gated devices, an Al_2O_3 layer with a thickness of 5 – 25 nm was deposited on the devices using atomic layer deposition (ALD) with trimethylaluminum as a precursor. Since the Al_2O_3 layer is deposited on S/D metal pads as well as the silicon nanowires, the S/D pad areas were patterned and etched in BOE to remove the Al_2O_3 layer on the metal pads. Finally, gate electrodes were patterned using EBL and Al was

deposited for the gate metal. Figure 4.6 shows an SEM image of top-gated SiNW FET devices. The device fabrication procedures are illustrated in Figure 4.7.

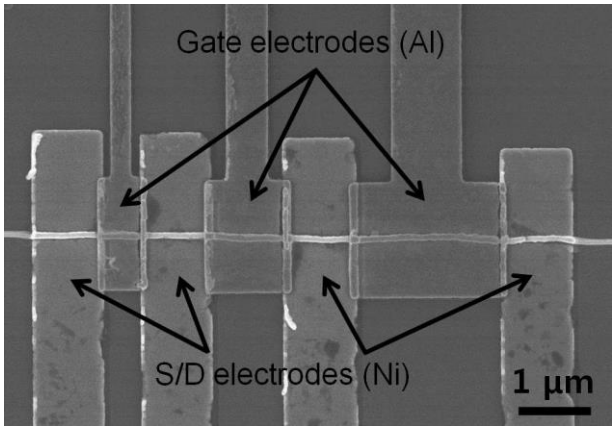

Figure 4.6. SEM image of top-gated SiNW FETs.

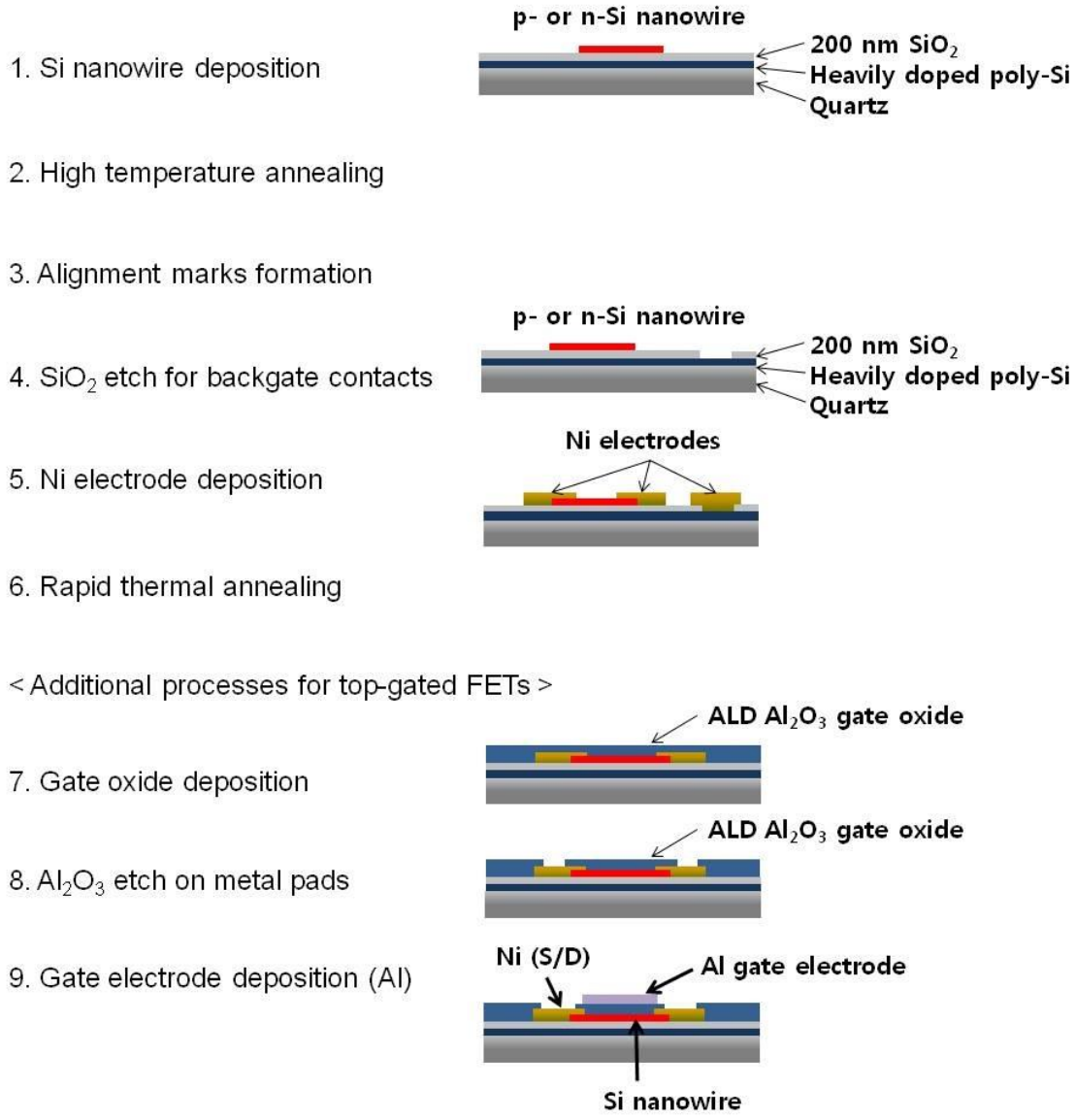

Figure 4.7. Schematic illustration of the device fabrication procedure.

The created SiNW FETs were electrically characterized using a probe station consisting of a Micromanipulator 6000, a vibration isolation table, a Keithley SCS 4200 semiconductor parameter analyzer, and an HP 4284A LCR meter. A Windows PC running Labview program was used to drive the instruments and collect the data.

4.4 Electrical Characterization of Back-Gated Silicon Nanowire FETs

Figure 4.8 shows the I_{ds}-V_{gs} curves of a back-gated SiNW FET with a channel length, L_{ch} = 1.8 μm. The nanowire of the device was doped with Boron and annealed at 800 °C for 6 hours. Unlike traditional MOSFETs with an inversion-mode behavior, the drain current of the p-type device increases as a more negative gate voltage is applied and thus the device shows an accumulation-mode behavior. The on-current reaches 9.7 μA/μm at V_{ds} = -1 V which is normalized by the diameter of the semi-circular nanowire. The maximum transconductance is 81.2 nS (1.35 μS/μm) at V_{ds} = -1 V and 15 nS (0.25 μS/μm) at V_{ds} = -0.1 V. The drain-induced barrier lowering (DIBL), which is defined as $\Delta V_g/\Delta V_d$ at $I_d = 10^{-10}$ A, is measured to be 940 mV/V and the subthreshold swing (SS) is 860 mV/dec. The large DIBL and SS are in part attributed to the 200 nm thick gate dielectric. Note that although the DIBL phenomenon of our device is similar to the DIBL effect in conventional MOSFETs, the mechanism of the increase of drain current in our device involves the thinning of Schottky barrier as well as the lowering of the barrier height (Jang et al., 2003; Koo et al., 2005).

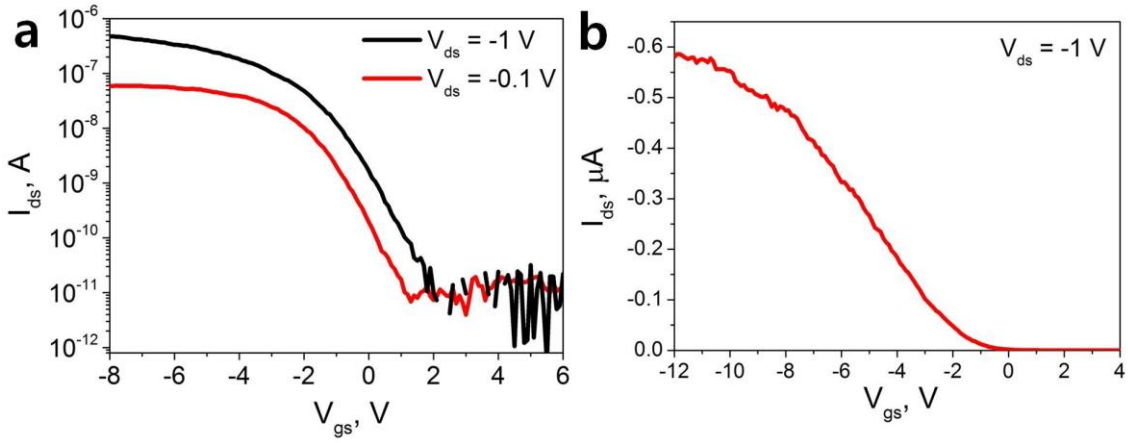

Figure 4.8. I_{ds}-V_{gs} characteristics of a laser-direct-written SiNW FET with a back gate. The nanowire was annealed at 800 °C.

The low-field mobility, μ_p, of the p-type nanowire was calculated to be 51 $cm^2V^{-1}s^{-1}$ at V_{ds} = -0.1 V using the equation $\mu = g_m L_{ch}^2 / C_{ox} V_{ds}$ with C_{ox} being the gate capacitance. The "metallic cylinder on an infinite metal plate model" is often used to calculate the gate capacitance, yielding an analytical equation for the gate capacitance (Khanal and Wu, 2007):

$$C_{ox} = \frac{2\pi\varepsilon_0\varepsilon_{r,eff} L_{ch}}{\ln(2t_{ox}/r)} \tag{4.1}$$

where $\varepsilon_{r,eff}$ is the effective dielectric constant of SiO_2, t_{ox} is the thickness of the gate oxide, and r is the radius of the nanowire. However, Eq. (4.1) is inaccurate with the dielectric constant for SiO_2 of ε_r = 3.9 unless an infinitely long, metallic nanowire is completely surrounded by the gate oxide. Therefore, the effective dielectric constant of $\varepsilon_{r,eff}$ = 2.45, which is calculated for a nanowire on SiO_2 (Wunnicke, 2006), was used and the gate capacitance, C_{ox}, was calculated to be 95 aF. Although the extracted mobility of the device is moderate considering that the nanowire is polycrystalline silicon, the mobility value is not the intrinsic hole mobility of the nanowire because drain current is limited by the Schottky barriers at the silicon/silicide interfaces as well as the channel conductance. We expect that the electrical performance of our nanowire FET can be improved by using low Schottky barrier silicides. For example, platinum silicide provides a low Schottky barrier of 0.23 eV for holes while erbium silicide has a low barrier height of 0.28 eV for electrons (Fritze et al., 2004).

Figure 4.9 shows the drain current I_{ds} versus drain voltage V_{ds} characteristics of the same device used for Figure 4.8. The device shows an enhancement-mode operation and non-saturated drain current is observed. The non-saturation behavior is because the width

of the Schottky barrier at the source contact becomes thinner as the drain voltage increases. The thinner barrier allows more tunneling current and therefore less voltage drop across the barrier. The increased number of holes injected from the source and the increased voltage drop in the channel result in an increasing drain current without saturation. Koo et al. (2005) have experimentally and numerically demonstrated non-saturated drain current for p-type accumulation channels as well as saturation behavior for inversion channels in Schottky barrier SiNW FETs. Non-saturation behavior of drain current in Schottky barrier SiNW FETs has been also observed elsewhere (Tang et al., 2012; Weber et al., 2006).

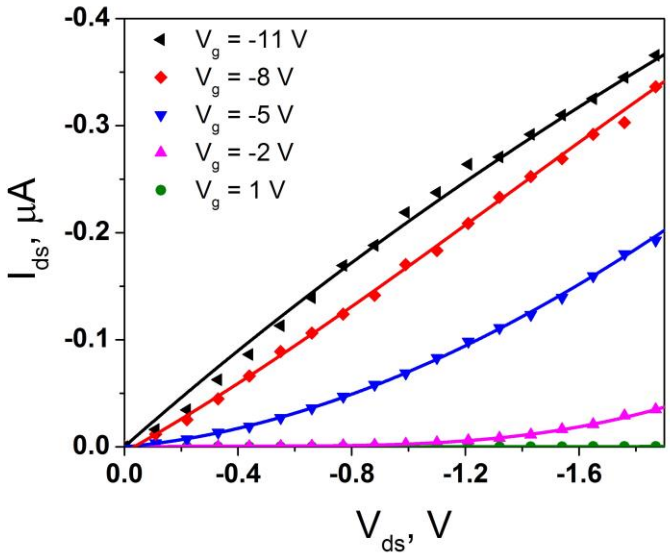

Figure 4.9. I_{ds}-V_{ds} characteristics of a laser-direct-written SiNW FET with a back gate. Solid lines are a guide for the eye.

In order to see the effect of annealing conditions on device performance, back-gated FET devices have been fabricated using nanowires annealed at a lower temperature of 650 °C for 20 hours. The measured drain current I_{ds} versus gate voltage V_{gs} characteristics of the device with a channel length of 1.8 μm are shown in Figure 4.10a. The on-current

is 8.6 nA (0.14 μA/μm) at V_{ds} = -0.1 V and V_{gs} = -10 V and the maximum transconductance is 1.7 nS (28 nS/μm) at V_{ds} = -0.1 V. The low-field mobility μ_p is calculated to be 5.8 $cm^2V^{-1}s^{-1}$ at V_{ds} = -0.1 V, which is much lower than the mobility of the device annealed at 800 °C (Figures 4.8 and 4.9). The lower mobility value is most likely to be due to incomplete crystallization of the amorphous Si nanowire. The crystallization rate of amorphous Si is described by an Arrhenius-type expression (Olson and Roth, 1988), $\upsilon = \upsilon_0 \exp(-E_a / k_B T)$, where υ is the crystallization rate, E_a is the activation energy, k_B is Boltzmann's constant, and T is the temperature in K. Since the crystallization rate is significantly lower at a lower temperature, the annealing time of the nanowires at 650 °C needs to be considerably lengthened for complete crystallization. In general, the slow crystallization of Si results in larger grain sizes and therefore higher mobility values (Olson and Roth, 1988). However, when the annealing period is not long enough for high crystallinity, the remaining amorphous silicon will degrade the electrical properties of the crystallized Si nanowire.

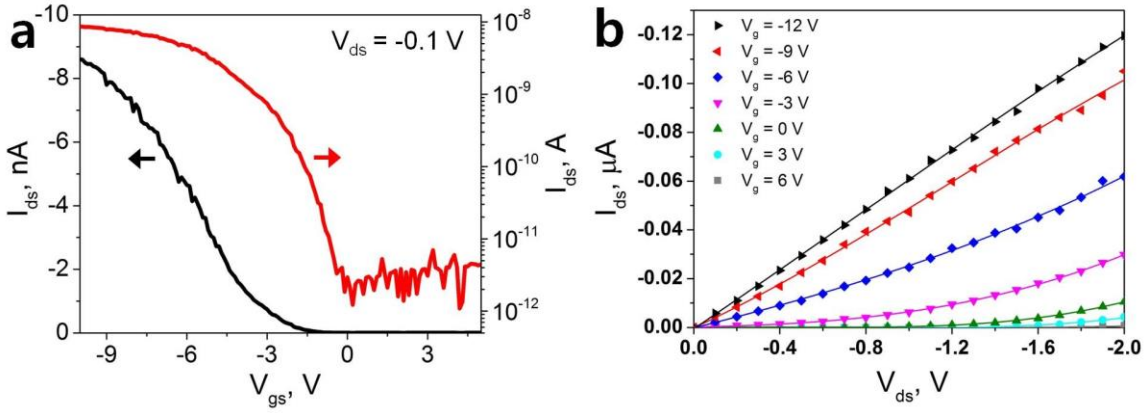

Figure 4.10. (a) I_{ds}-V_{gs} and (b) I_{ds}-V_{ds} characteristics of a laser-direct-written SiNW FET with a back gate. The nanowire was annealed at 650 °C.

We have also fabricated n-channel SiNW FETs using phosphorus-doped, n-type nanowires. The devices have the same back-gate configuration as previous p-channel devices. Figure 4.11a shows the drain current I_{ds} versus gate voltage V_{gs} characteristics of the device with a channel length of 1.8 μm. The on-current of the device is 5.2 nA (87 nA/μm) at V_{ds} = 1 V and V_{gs} = 15 V, and the maximum transconductance is 0.42 nS (7 nS/μm) at V_{ds} = 1 V and 0.036 nS (0.6 nS/μm) at V_{ds} = 0.2 V. The calculated low-field mobility is 0.06 $cm^2V^{-1}s^{-1}$ at V_{ds} = 0.2 V, which is much smaller than that of the p-channel device annealed at the same temperature. This inferior performance was, in fact, anticipated because nickel silicide has a high Schottky barrier of 0.66 – 0.75 eV for electrons (Sze and Ng, 2007; Liehr et al., 1985). Since drain current is mainly limited by the high Schottky barrier rather than the conductance of the channel, the extracted mobility has little relation to the intrinsic value of the channel material. Note that ambipolar behavior is observed in Figure 4.11a due to the relatively low Schottky barrier height for holes. With increasingly negative V_{gs}, there is an increase in drain current.

Another factor affecting the device performance is the crystallinity of the nanowire. Although boron and phosphorus impurities in amorphous Si enhance the crystallization rate, the effect is small unless the impurity concentration is larger than 10^{19} cm^{-3} (Olson and Roth, 1988). The doping concentration of our nanowires is relatively small and we can assume that phosphorus-doped nanowires will be crystallized at the same rate as boron-doped nanowires.

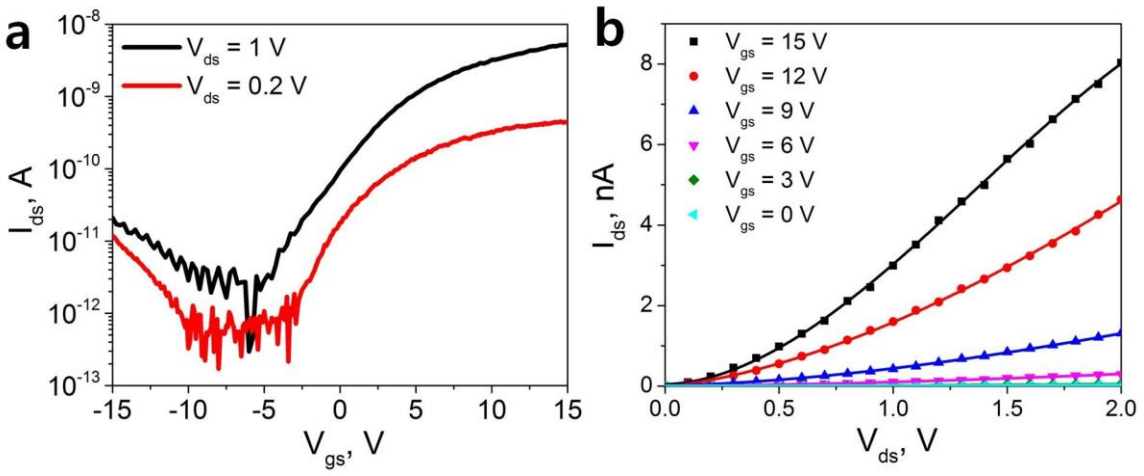

Figure 4.11. (a) I_{ds}-V_{gs} and (b) I_{ds}-V_{ds} characteristics of an n-type SiNW FET with a back gate. The nanowire was annealed at 650 °C.

4.5 Electrical Characterization of Top-Gated Silicon Nanowire FETs

Laser-direct-written SiNW FETs with an Al top gate and an Al_2O_3 gate oxide has been fabricated and tested. The p-type nanowires of the FETs were annealed at 800 °C and the thickness of the gate oxide was 5 nm. Figure 4.12a shows the I_{ds}-V_{gs} characteristics of a top-gated device with a channel length of 800 nm. The on-current is 0.33 μA (5.5 μA/μm) at V_{ds} = -1 V and V_{gs} = -7 V. The maximum transconductance is 0.213 μS (3.55 μS/μm) at V_{ds} = -1 V and 1.82 nS (30 nS/μm) at V_{ds} = -0.01 V. The drain-induced barrier lowering (DIBL) is measured to be ~940 mV/V and the subthreshold swing (SS) is ~680 mV/dec. Using the relation $C_{ox} = \pi\varepsilon_0\varepsilon_r L_{ch} / \ln(1+t_{ox}/r)$ for coaxial, circular cylindrical electrodes (Ramo et al., 1994), the gate capacitance is calculated to be 1.3 fF. Since our nanowire is semi-circular and the fringing capacitance at the gate oxide-substrate interfaces is not included in the equation, the calculated gate capacitance will be an upper limit of the actual capacitance. The low-field mobility of the p-type nanowire is calculated to be 0.9 $cm^2V^{-1}s^{-1}$ at V_{ds} = -0.01 V. Compared to the mobility of 51 $cm^2V^{-1}s^{-1}$

in the back-gated device annealed at 800 °C, the mobility of the top-gated device is significantly lower. In addition, the subthreshold swing of 680 mV/dec was not improved much from 860 mV/dec of the back-gated device despite the aggressive scaling down of the gate oxide thickness from 200 nm to 5 nm. This degraded performance is considered to be due to the incompatibility between Si and Al_2O_3, such as a high density of interface traps (Lee et al., 2002), fixed charges in the thin oxide (Buchanan et al., 2000), and mobility reduction due to soft optical phonons (Saito et al., 2005). The electrical performance of the device can be improved by proper post-annealing (Lee et al., 2002; Moselund et al., 2011) or inserting a SiO_2 layer between the Al_2O_3 layer and the nanowire (Saito et al., 2005). Ultimately, we can choose thermally grown SiO_2 as a gate oxide unless the channel length of our device becomes ultra-short.

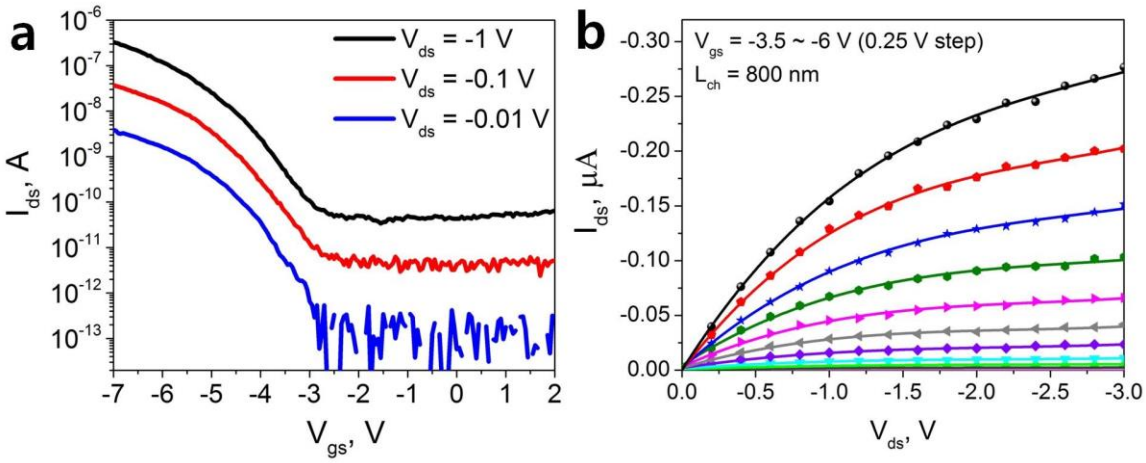

Figure 4.12. (a) I_{ds}-V_{gs} and (b) I_{ds}-V_{ds} characteristics of a top-gated SiNW FET with a channel length of 800 nm.

Figure 4.13 shows the I_{ds}-V_{ds} characteristics of a top-gated device with a channel length of 300 nm. Unlike the 800 nm device which exhibits well-saturated drain conduction in Figure 4.12b, the output characteristics of the 300 nm device have a

pronounced inflection of the curves in the saturation region, which is referred to as kink effect (Sze and Ng, 2007). With shorter channel lengths, the electric field in the channel increases and the channel carriers acquire extra energy from the high electric field. Consequently, impact ionization occurs at the drain end of the channel and some of the generated electrons go to the source, forcing further carrier injection from the source. The kink effect is more often observed in floating body devices (Sze and Ng, 2007; Valdinoci et al., 1997).

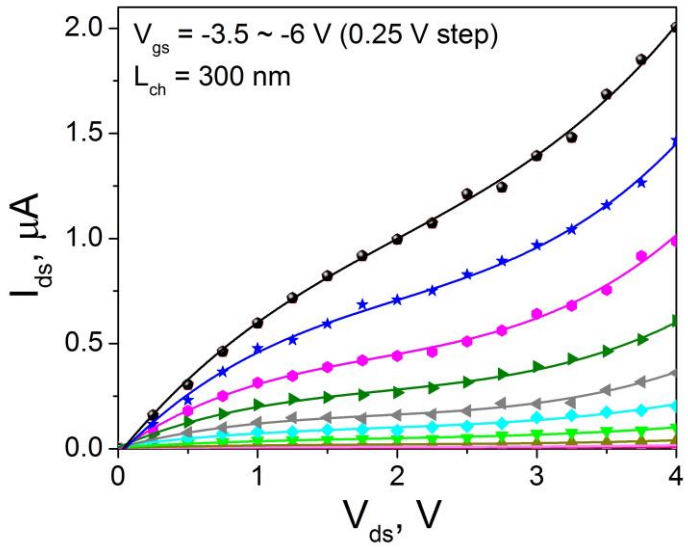

Figure 4.13. I_{ds}-V_{ds} characteristics of a top-gated SiNW FET with a channel length of 300 nm.

4.6 Effect of Doping Concentration on Device Performance

Figure 4.14 shows I_{ds} versus V_{gs} curves of two different SiNW FETs. The nanowire of the device in Figure 4.14a (device A) was synthesized with a high diborane flow rate (SiH_4:B_2H_6 = 1:1) and thus has a higher doping concentration while the nanowire in Figure 4.14b (device B) was synthesized with a lower diborane flow rate (SiH_4:B_2H_6 =

400:1). Both devices have a back gate configuration with a 200 nm thick SiO_2 layer as a gate oxide and a channel length of 4 μm.

The most conspicuous difference between the two devices is their on-off ratios. The device A with a high doping concentration cannot be turned off and therefore the on-off ratio was only about 2.2, whereas the device B with a lower doping concentration is completely turned off with positive gate voltages and the on-off ratio is higher than 10^4. In addition, the drain current in the device A is much larger than that of the device B. The low on-off ratio of the device A is due to the electrostatic screening by charged dopant atoms in the nanowire. Since the doping concentration of the nanowire is too high, the applied positive gate voltage can deplete only the surface layer of the nanowire, allowing current flow in the nanowire core. From the resistivity of the nanowire in the device A, we estimate the doping concentration of the nanowire to be ~4 x 10^{17} cm^{-3} when the nanowire is assumed to be single-crystalline Si. The Debye length, which is a characteristic length for electrostatic screening, is calculated to be ~6 nm using the equation, $L_D = \sqrt{kT\varepsilon_0\varepsilon_{r,Si} / Nq^2}$ where $\varepsilon_{r,Si}$ is the dielectric constant of Si and N is the doping concentration. Since our nanowire is, in fact, polycrystalline Si, the actual doping concentration will be much higher and therefore the actual Debye length will be shorter than 6 nm. The calculated Debye length of 6 nm is already smaller than the radius of the nanowire (~30 nm).

Drain current in the device A will flow in the "bulk" of the Si nanowire while charge carriers in the device B will move on the surface accumulation layer. In addition, the Schottky barriers at the source/drain contacts are thinner in the device A due to the high

doping concentration. The bulk carrier transport and the thin Schottky barrier will result in a higher drain current in the device A as shown in Figure 4.14.

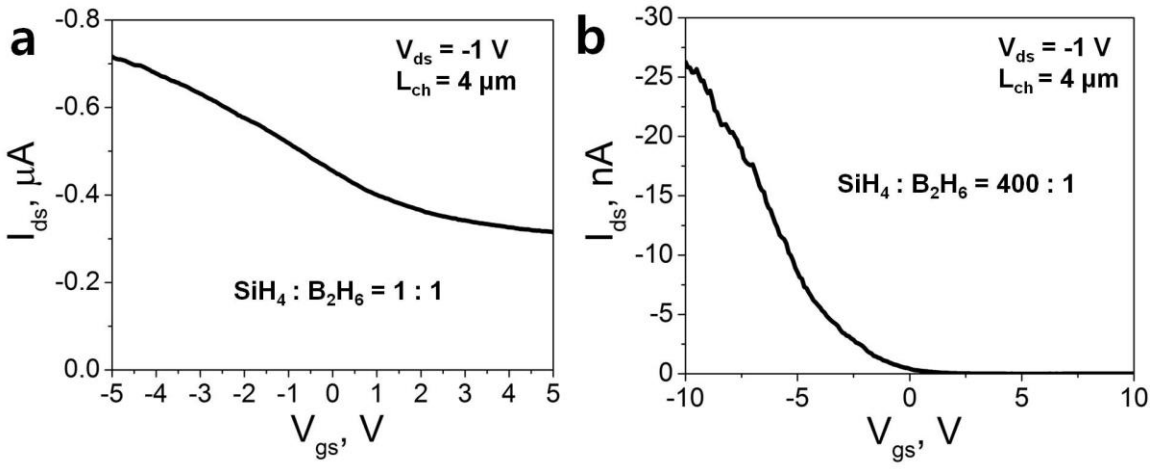

Figure 4.14. I_{ds}-V_{ds} characteristics of back-gated SiNW FETs. The nanowires were synthesized with SiH_4:B_2H_6 mass flow rates of (a) 1:1 and (b) 400:1.

Table 4.1. Summary of device parameters of laser-direct-written SiNW FETs.

Device No.	1	2	3	4	5	6
Gate configuration	Back-gated	Back-gated	Back-gated	Top-gated	Back-gated	Back-gated
Annealing Temperature (°C)	800	650	650	800	600	650
Annealing period (hours)	6	20	20	6	12	20
Dopant atoms	B	B	P	B	B	B
Mass flow rate (SiH_4:B_2H_6 or PH_3)	400:1	400:1	50:1	500:1	1:1	400:1
L_{ch} (μm)	1.8	1.8	1.8	0.8	4	4
t_{ox} (nm)	200	200	200	5	200	200
V_{ds} (V)	-1	-0.1	1	-1	-1	-1
On-current (μA/μm)	9.7	0.14	0.087	5.5	11.9	0.44
Transconductance (μS/μm)	1.35	0.028	0.007	3.55	0.95	0.072
μ ($cm^2V^{-1}s^{-1}$)	51	5.8	0.06	0.9	-	7.3
I_{on}/I_{off}	$> 10^4$	$> 10^3$	$\sim 10^3$	$> 10^3$	~2.2	$> 10^4$

4.7 Summary

In this chapter, we have demonstrated the application of the laser-direct-written silicon nanowires to field effect transistors. The synthesis of p- and n-type nanowires was first described. Nanowires as thin as 60 nm were synthesized using a horizontally polarized laser light. The nanowires were in-situ doped during the synthesis using diborane (B_2H_6) and phosphine (PH_3).

The fabrication procedure of SiNW FETs was also described in detail. Both top- and back-gated FETs were fabricated. For back-gated devices, the 200 nm thick poly-Si layer under the 200 nm SiO_2 on the quartz substrate was doped using ion implantation and used as a back gate. Ni was used for source/drain contacts and nickel silicide was formed using rapid thermal annealing. For top-gated devices, an Al_2O_3 layer was deposited using atomic layer deposition for a gate oxide and a metal gate was created.

The fabricated FET devices have been electrically characterized and the results have been discussed. The low field mobility of 51 $cm^2V^{-1}s^{-1}$ was extracted from a back-gated FET device annealed at 800 °C. The back-gated devices annealed at 650 °C were shown to have reduced mobility most likely due to incomplete crystallization. The device performance of top-gated FETs has been also discussed.

In addition, we have discussed the effect of doping concentration on device performance. When a nanowire was doped with a high concentration of boron, the fabricated FET device could not be turned off due to the electrostatic screening effect.

CHAPTER 5. P-N JUNCTION SILICON NANOWIRES

The silicon p-n junction is one of the fundamental building blocks to construct electronic and optoelectronic devices. However, fabrication of p-n junctions typically requires complex processes of patterning, doping, and etching. In this regard, laser direct writing has significant advantages over conventional "top-down" approaches since it has the capability to adjust parameters in-situ, including dopant gases and concentrations. In this chapter, we demonstrate the fabrication of p-n junction nanowires using the laser-direct-write CVD method. The laser-direct-written p-n junction nanowires were fabricated into multifinger devices with parallel metal contacts using standard microfabrication techniques and electrically characterized. In addition, the doping distribution along the nanowires was measured using Kelvin probe force microscopy.

5.1 Laser Direct Writing of P-n Junction Nanowires

P-n junction nanowires were fabricated using the laser-direct-write method discussed in Chapter 2. The incident laser was horizontally polarized to enable the interference effect discussed in Chapter 2.3.2 and thus formed nanowires as thin as 60 nm. The p-type part of the p-n junction nanowires was synthesized using 500 ppm diborane (B_2H_6) as a dopant gas. The mass flow rate of SiH_4:B_2H_6 was 5:1, 10:1 or 1,000:1, which corresponds to a concentration ratio of 1,000:1, 2,000:1, or 20,000:1, respectively. The n-

type part of the p-n junction nanowires was created using 100 ppm phosphine (PH_3) with a mass flow rate of SiH_4:PH_3 between 5:1 and 10:1, which corresponds to a concentration ratio between 5,000:1 and 10,000:1, respectively.

In order to change the dopant and polarity, we used two different methods. The first one we employed was to stop the nanowire deposition at the position of the p-n junction and switch the dopant to the opposite dopant polarity. In this method, the nanowire deposition started with a flow of one type of dopant and stopped at a position where a p-n junction would be formed. The laser illumination was blocked and the chamber was evacuated below 100 mTorr and refilled with the opposite dopant polarity. Once the chamber was refilled, the nanowire deposition was resumed. Before resuming the nanowire growth, the stage was moved backward 200-400 nm in the x direction to ensure nanowire continuity.

This stop-and-resume method enables easy formation of p-n junctions at a desired location and a sharp transition between dopant levels is expected at the p-n junctions. However, the switch of dopant gases usually caused a shift in the nanowire writing as seen in Figure 5.1. These shifts caused a discontinuity in nanowires as seen in Figure 5.1a and b, or defects as seen in Figure 5.1c. It is assumed that the cause of these shifts is a difference in dopant gas flow rate and pressure. Since the gas nozzle is placed very close to the zone plate in the experiment, a small change in the gas flow from the nozzle can force the zone plate to slightly move, and this movement makes a shift in nanowire writing. These shifts became smaller when the flow rate of dopant gases was smaller, but were still observed with the same flow rate of diborane and phosphine. With 10 sccm silane, 1 sccm diborane and 1 sccm phosphine, the boron-doped parts of nanowires were

hundreds of nm farther in the direction of flow than the phosphorus-doped parts as seen in Figure 5.1a and b. A proper stage movement in the y direction can cancel out these shifts and continuous p-n junction nanowires as shown in Figure 5.2 were created. However, the success rate was still low and only about one or two out of ten runs resulted in continuous single nanowires.

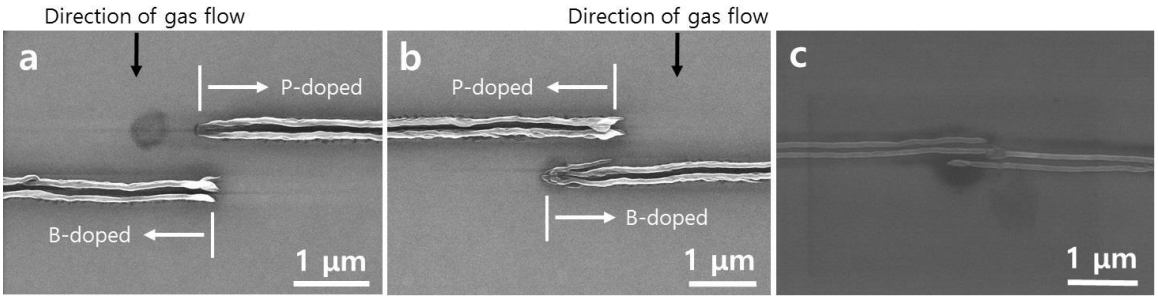

Figure 5.1. SEM images of p-n junction nanowires with (a, b) discontinuity and (c) a defect. The nanowire deposition was stopped at the p-n junction locations and resumed after the chamber was refilled with the opposite dopant polarity.

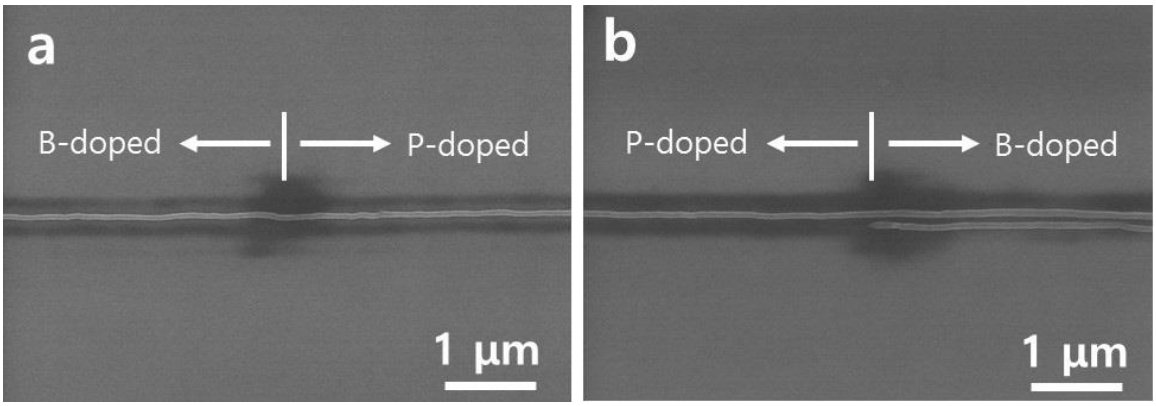

Figure 5.2. SEM images of continuous p-n junction nanowires deposited with the stop-and-resume method. (a) Both p- and n-type sections of the nanowire are single nanowires. (b) The n-type section of the nanowire is a single nanowire, but after changing the dopant type, the nanowire becomes a double nanowire.

We also synthesized p-n junction nanowires without stopping to switch dopants. In this method, the chamber was filled with one type of dopant and the nanowire growth

started with a flow of the same dopant. Then, the dopant was switched to the opposite polarity during the nanowire growth. This method facilitated forming continuous p-n junction nanowires without experiencing the previous shift problem due to the gas change and consequent disjointed nanowires. The overall process was faster than the previous method since there was no need to wait until the gas change was completed. However, it is expected that the transition between dopant levels will not be as sharp as in the previous method. Also, the location of the formed p-n junction was not accurate since there was a delay between the gas switch and the actual transition in nanowire doping. From the electrical measurement which will be discussed in Chapter 5.3, it was confirmed that the p-n junctions formed within 10 μm from the location of the gas change, which corresponds to 20 seconds when considering the scanning speed of 0.5 μm/s. Figure 5.3 shows SEM images of p-n junction nanowires formed with the continuous deposition method.

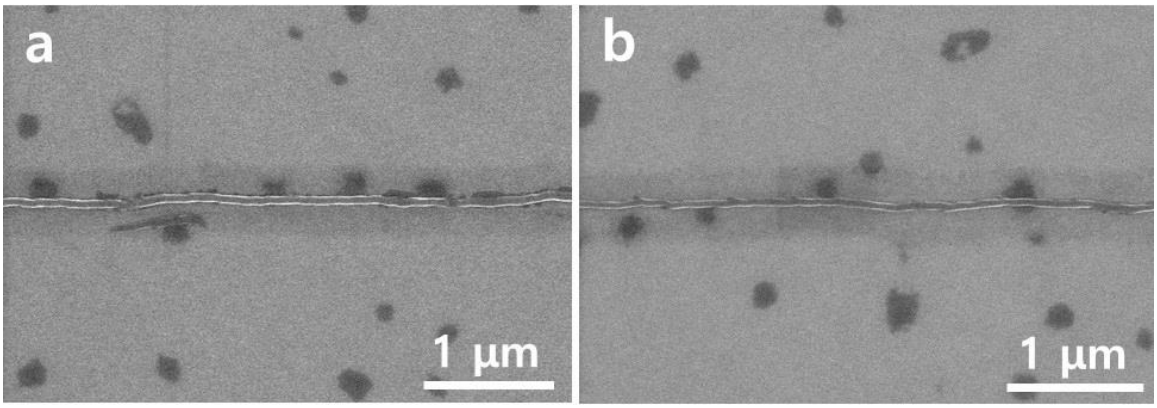

Figure 5.3. SEM images of continuous p-n junction nanowires which were formed using the continuous deposition method.

5.2 Fabrication of P-n Junction Nanowire Devices

In order to electrically characterize our p-n junction nanowires, we fabricated multifinger devices with parallel metal contacts spaced by 5 μm gaps spanning the nanowires. Every two adjacent metal contacts formed a two-terminal device.

The p-n junction nanowires were first annealed either at 700 °C for 20 hours or at 800 °C for 6 hours to crystallize and activate dopant atoms. The annealing chamber was purged with N_2 for 1 hour before increasing temperature to avoid unintentional thermal oxidation of the nanowires. From the TEM analysis in Chapter 2.3.3, the grain size after the annealing is expected to be a few nanometers. The annealing temperature and time were carefully chosen to avoid unnecessary diffusion of dopant atoms and keep the transition length as short as possible. According to Fair's vacancy model, the diffusion coefficient of impurities in silicon can be calculated using the following equation (Campbell, 2008).

$$D = D^0 + \frac{n}{n_i} D^- + \left[\frac{n}{n_i}\right]^2 D^{2-} + \frac{p}{n_i} D^+ + \left[\frac{p}{n_i}\right]^2 D^{2+} \tag{5.1}$$

where D^0, D^-, D^{2-}, D^+ and D^{2+} are the neutral, negative vacancy one, negative vacancy two, positive vacancy one, and positive vacancy two diffusivity, respectively, n_i is the intrinsic carrier concentration, and n and p are the electron and hole concentrations. The vacancy diffusivity is of the form

$$D^i = D_0^i e^{-E_a/kT} \tag{5.2}$$

where E_a is the activation energy of the vacancy and D_0^i is a nearly temperature-independent term. Assuming for the sake of simplicity that the silicon nanowires are

single crystalline, $p = 2.5 \times 10^{19}$ cm^{-3} and $n = 5 \times 10^{18}$ cm^{-3}, the characteristic diffusion length, $\sqrt{Dt}$, is calculated to be 22 nm for boron and 7.6 nm for phosphorus with the annealing conditions of 800 °C and 6 hours. With the annealing conditions of 700 °C and 20 hours, the characteristic diffusion length decreased to 9 nm for boron and 1.9 nm for phosphorus. Hence, we believe that the annealing process had limited effect on the transition length of the p-n junctions in the nanowires. The diffusion coefficients and other numbers used for the calculation are summarized in Table 5.1.

Table 5.1. Summary of the diffusion coefficients, vacancy diffusivities, and activation energies used to estimate the characteristic diffusion lengths (Campbell, 2008). The unit for the diffusion coefficients and vacancy diffusivities is cm^2/s, and eV for the activation energies.

	B in Si		P in Si	
D_o^0	0.037		3.9	
E_a^0	3.46		3.66	
D_0^+	0.41		-	
E_a^+	3.46		-	
D_0^-	-		4.4	
E_a^-	-		4.0	
D_0^{2-}	-		44.0	
E_a^{2-}	-		4.37	
	700 °C	800 °C	700 °C	800 °C
D^0	4.43×10^{-20}	2.07×10^{-18}	4.28×10^{-19}	2.51×10^{-17}
D^+	4.90×10^{-19}	2.30×10^{-17}	-	-
D^-	-	-	8.40×10^{-21}	7.16×10^{-19}
D^{2-}	-	-	1.02×10^{-21}	1.31×10^{-19}
D	1.14×10^{-17}	2.26×10^{-16}	4.89×10^{-19}	3.12×10^{-17}
$\sqrt{Dt}$ (nm)	9.1	22	1.9	8.2
n_i (cm^{-3})	1.08×10^{18}	2.57×10^{18}	1.08×10^{18}	2.57×10^{18}

The annealed nanowires were etched in 10:1 HF for 20 seconds to remove the surface oxide. Little change in nanowire diameter was observed during this etch process and therefore we assume that the N_2 purge before the high temperature annealing for crystallization effectively reduced unintentional thermal oxidation during the annealing process. Alignment markers and a coordinate system were then patterned using electron beam lithography (EBL). 5 nm titanium and 80 nm gold were subsequently deposited using an electron beam evaporator. For source and drain contacts, 100 nm-thick Ni was patterned using EBL and a liftoff process. Ni was chosen since low-resistance NiSi can be formed at a relatively low temperature. Immediately before the Ni deposition, the nanowires were exposed to O_2 plasma to remove residual resist in the exposed area and etched in 6:1 BOE for 5 seconds to remove native oxide on the surface. The metallized devices were finally annealed using rapid thermal annealing at 350 °C for 1 minute in forming gas (4 % H_2/96 % N_2) to form nickel silicide at the Ni-Si interfaces. More details about the EBL process can be found in Chapter 4.3.

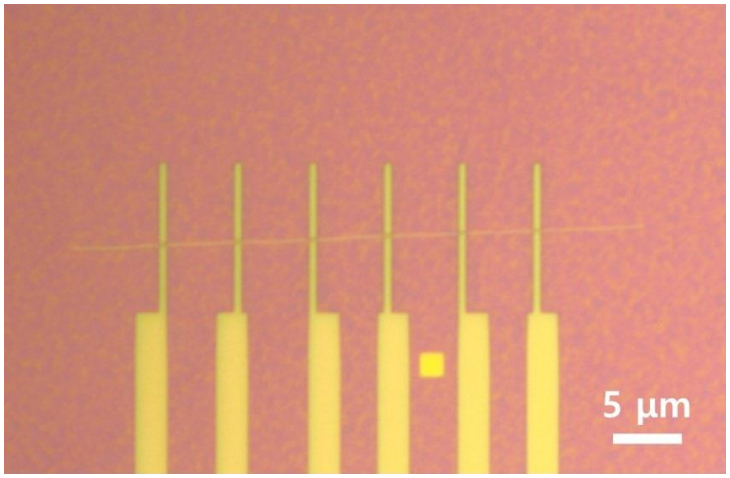

Figure 5.4. Optical image of a multifinger device fabricated from a p-n junction nanowire.

5.3 Electrical Characterization of P-n Junction Nanowire Devices

The p-n junction nanowire devices were electrically characterized using a probe station. We first tested nanowire devices which were fabricated from a p-n junction nanowire deposited using the stop-and-resume method. The concentration ratios of SiH_4:B_2H_6 and SiH_4:PH_3 used for this nanowire were 2,000:1 and 10,000:1, respectively, and the nanowire was annealed at 700 °C for 20 hours. The p-n junction was in the middle of the nanowire which was 25 μm away from the start of the nanowire deposition. Figure 5.5 shows the I-V curves of the two terminal devices. The transition region in the middle of the nanowire demonstrates the desired diode behavior as shown in Figure 5.5a. When positive voltages are applied to the p-side terminal, increased current is observed while very small current is measured at negative voltages. When the voltage is larger than 2 V, the current increases linearly rather than exponentially because the series resistance of the p- and n-type sides dominates. The p-type (Figure 5.5b) and n-type (Figure 5.5c) sections of the nanowire both demonstrate resistive behavior as expected. Using the resistance from the I-V curve along with the nanowire cross sectional area of 1.41×10^{-11} cm^2, the resistivity of the p-type section of the nanowire is 0.30 Ω·cm. which corresponds to a boron doping level of approximately 6×10^{16} cm^{-3} when we assume that the nanowire is single crystalline silicon. The resistance of the n-type section of the nanowire is 0.89 Ω·cm and the corresponding phosphorus doping concentration is 6×10^{15} cm^{-3}. Since our annealed nanowire is poly-crystalline silicon and the resistivity of poly-crystalline silicon is much higher than that of single crystalline silicon especially when the doping concentration is low or moderate, due to the dopant segregation (Fripp, 1975) and the trapping states at grain boundaries (Seto, 1975), the actual doping concentrations

of boron and phosphorus in the p-n junction nanowire are expected to be much higher than the above values. Another way to estimate the doping concentrations of the silicon nanowire is to use the gas ratios of SiH_4:B_2H_6 and SiH_4:PH_3 during the nanowire deposition. In literature, when the gas ratios of SiH_4:B_2H_6 and SiH_4:PH_3 were 2,000:1 and 10,000:1 for CVD-grown poly-crystalline silicon, carrier concentrations of about 2×10^{19} cm^{-3} for holes and about 10^{19} cm^{-3} for electrons were reported (Cowher and Sedgwick, 1972). Therefore, we believe that the actual doping concentrations are between 6×10^{16} and 2×10^{19} cm^{-3} for boron and between 6×10^{15} and 10^{19} cm^{-3} for phosphorus. The nonlinearity observed in Figure 5.5b and c is attributed to the Schottky barrier at the Ni-Si interfaces and can be minimized by optimizing the post-metal annealing process.

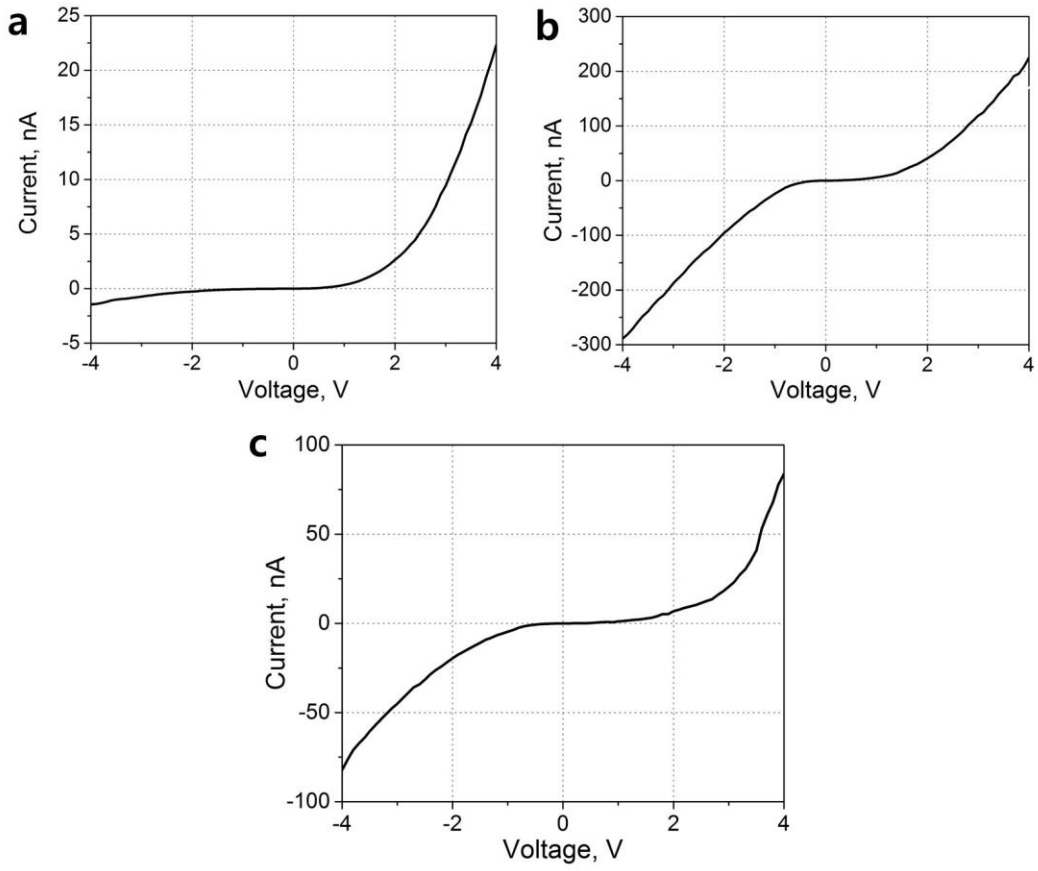

Figure 5.5. I-V characteristics of a laser-direct-written p-n junction SiNW devices. The p-n junction nanowire was deposited by the stop-and-resume method. (a), (b), and (c) correspond to the p-n junction, p-type, and n-type portions of the nanowire, respectively.

Figure 5.6 shows the I-V curves of nanowire devices which were fabricated from a p-n junction nanowire deposited using the continuous deposition method. This nanowire was deposited with the same doping concentrations as the nanowire in Figure 5.5 and it was annealed at 800 °C for 6 hours. The p-n junction was placed about 3 to 4 μm away from the location of dopant gas change and this corresponds to 13 to 14 μm away from the start of the nanowire deposition. In Figure 5.6a, the central p-n junction region shows the expected diode behavior. Compared to Figure 5.5a, the current is larger because of the higher annealing temperature and consequent lower series resistance. When the

voltage is larger than 1 V, the series resistance dominates and the current increases linearly. Figure 5.6b shows the ideality factor, $\eta_{ideality}$, calculated using the following equation (Sze and Ng, 2007).

$$\eta_{ideality} = \frac{q}{kT}\left(\frac{d(\ln I)}{dV}\right)^{-1} \tag{5.3}$$

where q is the elementary charge, k is the Boltzmann constant, and T is the absolute temperature. The ideality factor equals to 2 when the recombination current dominates and it equals to 1 when the diffusion current dominates. However, in real devices, the ideality factor can be higher due to the generation and recombination of carriers, the series resistance, the trap-assisted tunneling, and the surface effects (Sze and Ng, 2007; Zhu et al., 2009). In our p-n junction diode device, the ideality factor is 1.84 at $V = 0.3$ V, but it quickly increases at a higher voltage due to the high series resistance. In addition, since the nanowire is poly-crystalline silicon, the higher generation-recombination rates and traps at grain boundaries result in higher ideality factors. The p-type (Figure 5.6c) and the n-type (Figure 5.6d) sides of the nanowire demonstrate resistive behavior with nonlinearity at a low voltage. The nonlinear I-V curves indicate that the effect of the Schottky barrier between the Si nanowire and Ni contacts is significant. The resistivity of the p-type section of the nanowire is calculated to be 0.16 Ω·cm, which corresponds to a boron doping concentration of 2×10^{17} cm^{-3} when we assume that the nanowire is single crystalline. The resistivity of the n-type section of the nanowire is calculated to be 1.15 Ω·cm, which corresponds to a phosphorus doping concentration of 4×10^{15} cm^{-3}. Note again that the actual doping concentrations of boron and phosphorus are expected to be higher due to the poly-crystallinity of our nanowire. Considering the concentration ratios

of SiH_4:B_2H_6 and SiH_4:PH_3 used for the nanowire, the actual doping concentrations are estimated to be between 2×10^{17} and 2×10^{19} cm^{-3} for boron and between 4×10^{15} and 10^{19} cm^{-3} for phosphorus.

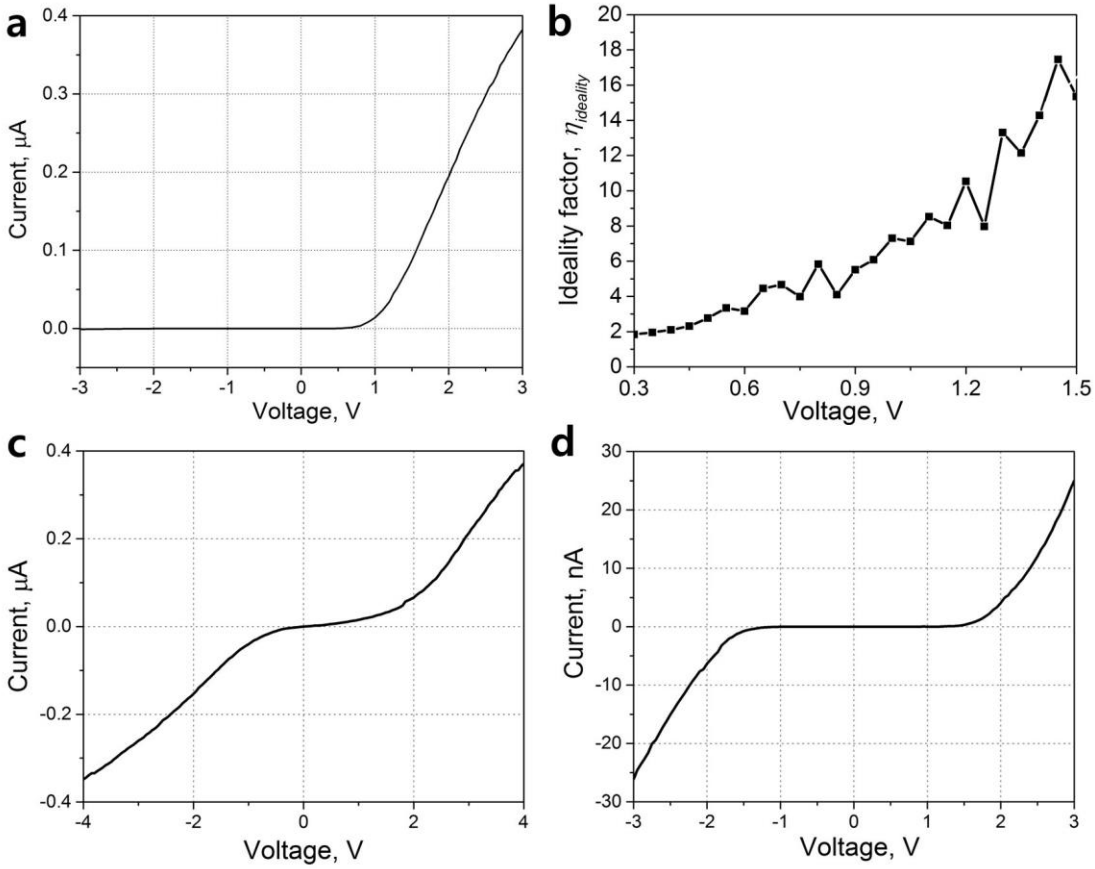

Figure 5.6. I-V characteristics of a laser-direct-written p-n junction SiNW devices. The p-n junction nanowire was deposited by the continuous deposition method. (a), (c), and (d) correspond to the p-n junction, p-type, and n-type portions of the nanowire, respectively. (b) shows the ideality factor calculated from the I-V curve in (a).

5.4 Kelvin Probe Force Microscopy of P-n Junction Nanowires

Kelvin probe force microscopy (KPFM) has been proven as an efficient tool which allows a quantitative determination of surface potentials with high spatial resolution (Nonnenmacher et al., 1992, Loppacher et al., 2005, Koren et al., 2009). In this chapter,

we visualize the transition between dopant levels along our p-n junction nanowires using KPFM.

KPFM measures a contact potential difference (CPD) between a conducting atomic force microscopy (AFM) tip and a sample. The CPD, V_{CPD}, is defined as (Melitz et al., 2011):

$$V_{CPD} = \frac{\phi_{tip} - \phi_{sample}}{q} \tag{5.4}$$

where ϕ_{tip} and ϕ_{sample} are the work functions of the tip and sample and q is the elementary charge. Figure 5.7a shows the energy band diagram of the tip and sample surface when they come close to each other and are electrically connected. The Fermi levels of the tip and sample are aligned and an electric field is generated between the tip and sample. This electric field can be detected by monitoring the oscillation of the tip and can be eliminated by applying an external voltage, V_{DC}, which equals to V_{CPD} with opposite direction (Figure 5.7b). Therefore, the CPD can be measured by finding V_{DC} which nullifies the electrical force between the tip and sample surface.

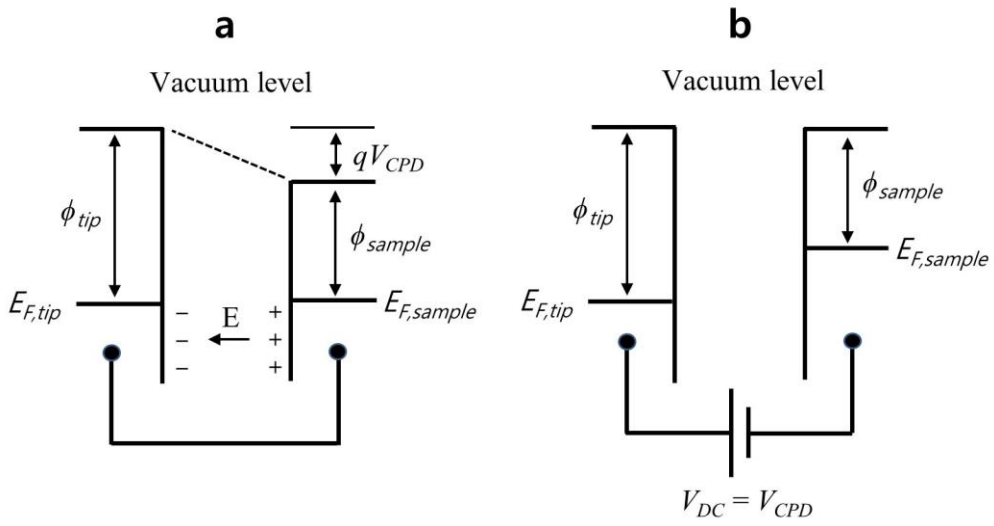

Figure 5.7. Energy band diagram illustrating Kelvin probe physics. (a) The tip and sample with different work functions of ϕ_{tip} and ϕ_{sample} are electrically contacted. The Fermi levels are aligned and there is an electric field between the tip and sample. (b) The electric field can be nullified by applying an external voltage V_{DC} which equals V_{CPD}.

For the actual measurement of the CPD, an additional AC voltage, V_{AC}, is applied between the tip and sample since the electrostatic force between the tip and sample is small without any external bias. For example, Zerweck et al. (2005) calculated an electrostatic force of 1.2×10^{-12} N between an AFM tip and sample with the work function difference of 100 meV, the tip radius of 15 nm, and the tip-sample separation of 3 nm. On the other hand, the magnitude of the van der Waals force which is the dominant attractive force at a noncontact situation is on the order of 10^{-9} N (Weisenhorn et al., 1989). With both DC and AC components, the voltage difference, ΔV, between the tip and sample becomes:

$$\Delta V = (V_{DC} \pm V_{CPD}) + V_{AC} \sin(wt) \tag{5.5}$$

The electrostatic force between the tip and sample is given by:

$$F_{es} = -\frac{1}{2}\Delta V^2 \frac{dC(z)}{dz} = -\frac{1}{2}\frac{\partial C(z)}{\partial z}[(V_{DC} \pm V_{CPD}) + V_{AC}\sin(wt)]^2 \quad (5.6)$$

with components at DC

$$F_{DC} = -\frac{\partial C(z)}{\partial z}[\frac{1}{2}(V_{DC} \pm V_{CPD})^2] \quad (5.7)$$

and at frequencies *w* and *2w*

$$F_w = -\frac{\partial C(z)}{\partial z}(V_{DC} \pm V_{CPD})V_{AC}\sin(wt) \quad (5.8)$$

$$F_{2w} = \frac{\partial C(z)}{\partial z}\frac{1}{4}V_{AC}{}^2[\cos(2wt) - 1] \quad (5.9)$$

where *dC/dz* is the gradient of the capacitance between the tip and sample surface. F_w in Equation (5.8) is used to measure the V_{CPD}. By finding V_{DC} which eliminates the oscillating component with the frequency *w*, the CPD can be accurately measured.

In the KPFM measurement of our p-n junction nanowires, a Pt/Ir-coated Si cantilever with a spring constant of 42 N/m was used. The measurement was performed in the two-pass technique in which the height profile is recorded during the first pass and then the CPD is measured during the second pass. We first tested a p-n junction nanowire deposited using the stop-and-resume method. The concentration ratios of SiH_4:B_2H_6 and SiH_4:PH_3 used for this nanowire were 100,000:1 and 20,000:1, respectively. V_{AC} was 5 V. The Figure 5.8 shows the KPFM image of the nanowire. In Figure 5.8b, a difference in CPD between the p-type and n-type sections of the nanowire is clearly observed and the transition length is about 300 nm. The CPD difference across the p-n junction is about 15 mV, which is much smaller than expected. Assuming that the hole concentration in the p-type side is 2×10^{17} cm^{-3} and the electron concentration in the n-type side is 4×10^{15} cm^{-3}

which were calculated in Chapter 5.3, the ideal potential difference is calculated to be ~750 meV (Sze and Ng, 2007). The discrepancy between the measured CPD and the actual work functions of semiconductor materials was previously reported (Melitz et al, 2011; Loppacher et al., 2005; Robin et al., 2000). In fact, the measured CPD is related to the surface potential, which is different from the work function of the bulk Si due to the space-charge-layer near the surface (Melitz et al., 2011). In addition, KPFM is extremely sensitive to the adsorbates in the air and surface traps (Robin et al., 2000). Therefore, the CPD difference measured across a p-n junction is usually smaller than the ideal potential difference. For example, Loppacher et al. (2005) reported a CPD difference of 120 meV between p-type and n-type Si measured at a dark condition. This discrepancy can be decreased by removing surface contaminants and oxide layers in ultra-high vacuum (UHV) and performing the KPFM measurement in UHV (Melitz et al., 2011).

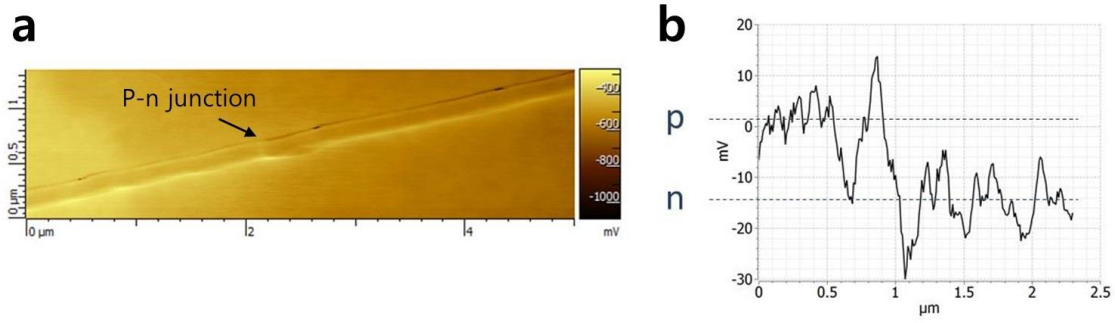

Figure 5.8. (a) Kelvin probe force microscope image of a laser-direct-written p-n junction nanowire. The nanowire was deposited using the stop-and-resume method. (b) CPD profile for a line scan over the transition region along the nanowire.

We also tested a p-n junction nanowire deposited using the continuous deposition method. The concentration ratios of SiH_4:B_2H_6 and SiH_4:PH_3 used for this nanowire were 2,000:1 and 10,000:1, respectively. V_{AC} was 4 V. In Figure 5.9c, the CPD difference over

the p-n junction is clearly observed. The transition length is about 1.5 μm, which is much longer than 300 nm in Figure 5.8c. This indicates that the continuous deposition method results in a longer transition length since the dopant gases are switched without stopping the stage movement. The CPD difference across the p-n junction is about 100 mV. This is smaller than the ideal work function difference of ~750 meV which was calculated above, but close to 120 meV which was reported by Loppacher et al. (2005).

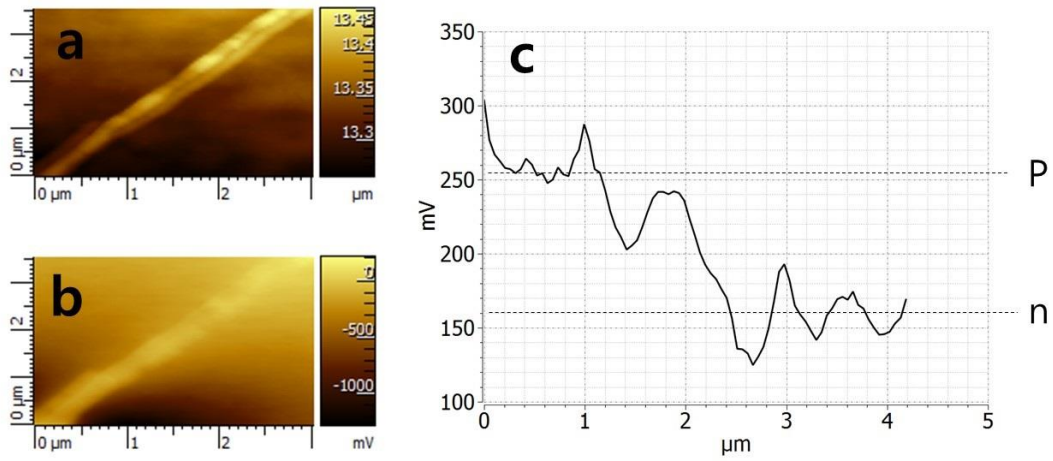

Figure 5.9. (a) Atomic force microscope image and (b) Kelvin probe force microscope image of a laser-direct-written p-n junction nanowire deposited using the continuous deposition method. (c) CPD profile for a line scan over the transition region along the nanowire.

5.5 Summary

In this chapter, we have demonstrated the fabrication of p-n junction nanowires using the laser-direct-write CVD method. The p-n junction nanowires were deposited using two different methods. The first one was vacuuming and refilling the chamber with the opposite dopant polarity while stopping the nanowire deposition at the p-n junction location, and then resuming the nanowire growth once the chamber was completely refilled. This method had an advantage of a sharp transition between dopant levels, but

the shift caused by the change of the dopant gases and consequent discontinuity in nanowires were the major problems. The other method we employed was switching the dopant gases without stopping the nanowire growth. This method resulted in a longer transition length, but the fabrication of continuous, single nanowires was much easier with this method.

The laser-direct-written p-n junction nanowires were then fabricated into multifinger devices for electrical characterization. The central p-n junction sections of the nanowires exhibited desired diode behavior while the p-type and n-type sides of the nanowires showed resistive behavior as expected.

Finally, the p-n junction nanowires were tested using Kelvin probe force microscopy. The contact potential difference (CPD) was measured and a CPD difference across the p-n junction was observed, which confirmed the successful formation of p-n junctions using our laser-direct-write method.

CHAPTER 6. CONCLUSIONS AND FUTURE WORK

6.1 Conclusions

In this work, we have demonstrated a one-step, laser-direct-write method to synthesize silicon nanowires (SiNWs). Sub-diffraction limited nanowires have been produced using only far field optics, and the position, orientation, and length of the nanowires are precisely controlled. The in-situ doping of the nanowires not only enables fabrication of axial p-n junction nanowires, but also simplifies device fabrication processes and thus facilitates integration of the nanowires into sensors and electronic devices. In addition, catalyst-free growth is another advantage of our laser-direct-write method.

The details of the laser-direct-write method have been described. One of the key components in the experiment is the Fresnel zone plates which focus a laser light on a substrate. Numerical calculations show the zone plates create a focal spot with a diameter of 185 nm and they are tolerant of fabrication errors. The morphology and the diameter of nanowires are determined by the laser power and polarization. By using proper experimental parameters, nanowires as thin as 60 nm have been created. In addition, experimental results and numerical calculations show that the interference between incident laser and surface-scattered light plays a key role in creating thin nanowires.

Field-effect-transistor (FET) sensors have been fabricated from laser-direct-written Si wires. The sensors were used to detect the proton concentration (pH) of an aqueous solution and it was shown that the conductance of the nanowire is sensitive to solution pH. The excellent sensitivity of the sensor devices demonstrates that our approach offers a simple and promising way to fabricate highly sensitive Si FET sensors.

Fabrication and electrical characterization of FETs have been discussed. Both back- and top-gated SiNW FETs were fabricated and hole mobility as high as 51 $cm^2V^{-1}s^{-1}$ was demonstrated. Enhanced device performance was observed with nanowires annealed at 800 °C than 650 °C. Top-gated devices exhibited lower mobility due to the incompatibility between Si and Al_2O_3 which was used as a gate oxide.

Finally, laser-direct-written p-n junction nanowires have been demonstrated. The p-n junction nanowires were fabricated by changing dopant gases during the nanowire growth. Multifinger devices with parallel metal contacts were fabricated from the nanowires to electrically characterize the nanowires. The p-n junction sections of the nanowires showed the expected diode behavior and the p- and n-type sections of the nanowires had resistive behavior. The surface potential of the nanowires was also measured using Kelvin probe force microscopy and the results showed transition between dopant levels at the position of the p-n junctions.

6.2 Future work

Although we have demonstrated valuable advances in the laser direct writing of nanowires and their applications to sensors and FETs, further work is still necessary to enhance the results. One possibility is employing thinner nanowires for SiNW FET

sensors. Due to their high surface-to-volume ratio, the use of a thinner nanowire for a sensor device will result in higher sensitivity. In Chapter 3, nanowires as thick as ~300 nm were used for sensor devices. Although these nanowires have rough surfaces, their surface-to-volume ratio is still limited by their large diameter, and therefore we expect that the sensitivity of nanowire sensors can be improved by using nanowires as thin as 60 nm which can be synthesized with our method.

In addition, our SiNW sensors can be easily extended for biosensing applications by functionalizing the sensing surface with bioreceptors. The created biosensors will share the working principles of ion-sensitive field effect transistors, but the analyte will be determined by the receptors attached on the sensor surface. For example, the existence and concentration of streptavidin can be detected by functionalizing SiNWs with biotin (Cui et al., 2001). DNA strands can be sensed with the use of peptide nucleic acids (PNAs) or complementary DNA as a receptor (Hahm and Lieber, 2004; Gao et al., 2011).

Improvement in the performance of the silicon nanowire FETs and sensors can be achieved by enhanced crystallization of the amorphous nanowires. Although the nanowires were annealed and crystallized before device fabrication, the grain size of the crystallized silicon was still in the range of nanometers. It is possible to enlarge the grain size with further investigation into annealing conditions and crystallization methods. We expect that it is also possible to obtain a single grain in the cross section of the nanowire since the diameter of the nanowire is only 60 nm. To this end, the nanowires can be crystallized for a prolonged period of time at a relatively low temperature. Another method for a larger grain size includes nickel induced crystallization of amorphous silicon (Kawazu et al., 1990; Jin et al., 1998).

The performance of the SiNW FETs and sensors can be improved by employing low Schottky barrier silicides for source/drain contacts. Since the Schottky barriers at the interfaces of silicon and metal contacts strongly affect the device properties of a Schottky barrier transistor, lowering the barrier height will result in improved on-current and other electrical characteristics. Different kinds of silicides should be used for p- and n-channel devices. Platinum silicide provides a low Schottky barrier of ~0.23 eV for holes while erbium silicide has a low barrier height of ~0.28 eV for electrons (Fritze et al., 2004). Since the Schottky barrier height of nickel silicide which is used for our devices is ~0.4 eV (Bucher et al., 1986; Sze and Ng, 2007), the use of platinum or erbium silicide will increase the performance of our FETs and sensors.

The synthesis of modulation-doped nanowires offers the potential of significantly extending the applicability of the laser-direct-written nanowires into various electronic and sensing devices. However, the electrical properties of the p-n junction nanowires can be further improved by increasing the doping concentrations of boron and phosphorus and optimizing the annealing conditions. In Chapter 5.3, the series resistances of the p-n junction diodes were still high. Especially, the n-type sections of the nanowires had higher resistance due to their low doping concentration and higher Schottky barrier at the interface of Si and NiSi. Increasing the doping concentrations will lower the resistivity of the nanowire and also reduce the effect of the Schottky barriers. The reduced series resistance will result in a better demonstration of the rectifying behavior of our p-n junction nanowires.

Finally, the surface potential profiles of our p-n junction nanowires which were measured using Kelvin probe force microscopy (KPFM) in Chapter 5.4 need to be

improved since significant dips and bumps were observed in the results. Because KPFM is very sensitive to surface adsorbates and oxides, the surfaces of the nanowires need to be carefully cleaned before KPFM measurement. In addition, any irregularity in the topography of the p-n junction area needs to be avoided in order to make the transition length more clearly distinguishable in the Kelvin probe measurements.

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- Femtosecond-laser-assisted chemical vapor deposition
- Characterization techniques: Electrical device characterization, Scanning electron microscopy,
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Honors & Awards

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- Korean government scholarship to study abroad 8/2010 – 7/2012
- Warren and Judy Stevenson scholarship, School of Mechanical Engineering, Purdue University 9/2010

Publications

Journal Publications

1. **Nam, W.**, Mitchell, J. I., and Xu, X., Laser direct synthesis of silicon nanowire field effect transistors, Nanotechnology, Vol. 26, pp. 055306 (2015).
2. Mitchell, J. I., Zhou, N., **Nam, W.**, Traverso, L. M., and Xu, X., Sub-diffraction laser synthesis of silicon nanowires, Sci. Rep., Vol. 4, pp. 3908-1-4 (2014).
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4. Wei, D., Mitchell, J. I., Tansarawiput, C., **Nam, W.**, Qi, M., Ye, P. D., and Xu, X., Laser direct synthesis of graphene on quartz, Carbon, Vol. 53, pp. 374-379 (2013).
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Patent

1. **Nam, W.**, Bae, Y., and Choi, M., 3-dimensional nanoparticle assembly structure and gas sensor using same, US, China, and South Korea Patent, Publication No US20140193325 A1 (2014).

Conference Presentations

1. **Nam, W.**, He, X., and Xu, X., Sub-diffraction-limit laser lithography assisted by laser-induced periodic surface structures (LIPSS), International Conference on Laser Ablation 2015, Cairns, Australia, August 31-September 4, 2015.
2. **Nam, W.**, Mitchell, J. I., and Xu, X., Laser direct written silicon nanowires for electronic and sensing applications, US-Korea Conference on Science, Technology, and Entrepreneurship 2015, Atlanta, GA, USA, July 29-Aug 1, 2015.
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5. **Nam, W.**, Mitchell, J. I., Wei, D., and Xu, X., Laser direct written silicon nanowires and graphene for chemical sensing applications, 31th International Congress on Applications of Lasers & Electro-Optics, Anaheim, CA, USA, September 23-27, 2012.
6. **Nam, W.**, Mitchell, J. I., Wei, D., Tansarawiput, C., Qi, M., and Xu, X., Laser direct growth of silicon nanowire and graphene for device fabrication, The 13th International Symposium on Laser Precision Microfabrication, Washington DC, USA, June 12-15, 2012.
7. **Nam, W.**, and Choi. M., Nanostructured tin oxide films prepared by spark discharge for gas sensing applications, The 11th Korean Conference on Aerosol and Particle Technology, Busan, South Korea, July 1-3, 2010.
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