TOTAL IONIZING DOSE AND SINGLE EVENT UPSET TESTING OF FLASH BASED FIELD PROGRAMMABLE GATE ARRAYS

By

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Abstract

The effectiveness of implementing field programmable gate arrays (FPGAs) in communication, military, space and high radiation environment applications, coupled with the increased accessibility of private individuals and researchers to launch satellites, has led to an increased interest in commercial off the shelf components. The metal oxide semiconductor (MOS) structures of FPGAs however, are sensitive to radiation effects which can lead to decreased reliability of the device.

In order to successfully implement a FPGA based system in a radiation environment, such as on-board a satellite, the single event upset (SEU) and total ionizing dose (TID) characteristics of the device must first be established. This research experimentally determines a research procedure which could accurately determine the SEU cross sections and TID characteristics of various mitigation techniques as well as control circuits implemented in a ProASIC3 A3P1000 FPGA.

To gain an understanding of the SEU effects of the implemented circuits, the test FPGA was irradiated by a 66MeV proton beam at the iTemba LABS facility. Through means of irradiation, the SEU cross section of various communication, motor control and mitigation schemes circuits, induced by high energy proton strikes was investigated. The implementation of a full global triple modular redundancy (TMR) and a combination of TMR and a AND-OR multiplexer filter was found to most effectively mitigate SEUs in comparison to the other techniques. When comparing the communication and motor control circuits, the high frequency I2C and SPI circuits experienced a higher number of upsets when compared to a low frequency servo motor control circuit.

To gain a better understanding of the absorbed dose effects, experimental TID testing was conducted by irradiating the test FPGA with a cobalt-60 (Co-60) source. An accumulated absorbed dose resulted in the fluctuation of the device supply current and operating voltages as well as resulted in output errors. The TMR and TMR filtering combination mitigation techniques again were found to be the most effective methods of mitigation

Key Words

FPGA - Field Programmable Gate Array

ASIC - Application Specific Integrated Circuit

COTS - Commercial Off The Shelf

SEE - Single Event Effect

SEU - Single Event Upset

TID - Total Ionizing Dose

SET - Single Event Transient

1. Introduction

1.1 Overview

With the designed operational lifespan of modern satellites exceeding 10 years [1], in-field reprogrammability has become requirement in the design. Variations in the objectives, design or operational parameters could result in inadequate performance of the satellite system which may lead to partial or complete failure of the system. The implementation of reliable, long term and fully reprogrammable satellites will allow for adaptations to be made to the system due to developments of the objectives. Satellites will be able to perform both multiple interchangeable tasks and adapt to new requirements, increasing the effective lifespan.

Field programmable gate arrays (FPGAs) have been utilized in space applications for more than 10 years with varying results [2]. Only in recent years, have they gained popularity over the conventional application specific integrated circuits (ASICs). As a result of their high flexibility, together with high performance, complexity and the ability to feature more than one million system gates [2], FPGAs have become an ideal component of space applications.

The implementation of FPGAs in a radiation environment unfortunately poses a number of disadvantages. Total Ionizing Dose (TID) effects, caused by an accumulative dose of radiation, can induce a degradation of performance characteristics in, or result in failure of the FPGA. TID effects in FPGAs lead to the increase in computational times, increased leakage current, shifts in the device threshold voltages and permanent functional failure [3]. In addition to the permanent effects, temporary soft errors can also be experienced, resulting in bit flips in the memory elements of the device propagating through the circuitry and producing an error on the output of the circuit.

FPGAs are also susceptible to single event effects (SEEs) caused by heavy ion or ionized high energy particle strikes, depositing a charge in the device [4]. If the deposited charge surpasses the critical charge of the device, a resulting bit flip could be induced in the form of a single event transient (SET) [4]. This SET propagates throughout the circuitry of the device and, if latched into a memory element, results in a single event upset (SEU). This consequently results in the affected circuitry outputting an error. In addition to SEUs and other soft errors, permanent SEEs can also be induced, resulting in temporary failure, or at worst, permanent failure of the FPGA.

A large amount of research into the effects of space radiation has been conducted in order to better understand and mitigate the effects of an accumulation of dose and high energy particle strikes can be seen in [5, 6, 7, 8]. A large number of advanced radiation hardened devices have been developed by many of the FPGA manufacturing companies for applications in high radiation environments [9, 10]. However, these devices are available at very high costs in terms of capital, computational speeds, physical dimensions and the amount of resources available in the device. In most cases, radiation hardened FPGAs at the available cost, fail to minimize the effects which radiation imposes on the device. As a result, a growing interest in the feasibility of utilizing commercial off the shelf (COTS) FPGAs in these space based applications has emerged [2]. Consequently, numerous tests have been conducted to determine the SEU cross section, TID characteristics and expected operating life span of numerous commercially available FPGAs [7, 11, 12, 13].

In an attempt to mitigate space radiation effects, various mitigation schemes have been invented and patented. An example of a TID mitigation scheme which aims to extend the operational life span of the device can be seen in [11]. A growing number of mitigation schemes, aimed at reducing the effects of SEEs due to high energy particle strikes in FPGAs, been developed as a response to the increased interest in implementing FPGAs in space applications.

The most common of these, triple modular redundancy (TMR), is based on a principle that implements a series of three flip-flops or latches, as oppose to one, followed by a majority voter, which determines the state of the output by considering all three. TMR may be applied locally to memory elements alone or globally to the user logic, global signals and memory elements [14]. Although global TMR has been proven to mitigate SEUs effectively, it requires at least triple the amount of additional overhead resources [15]. An alternative mitigation approach can be seen in [16, 17] where three identical FPGAs have been programmed, with the outputs voted externally, to the devices in order to detect any errors in the device. The FPGA from which the error originates is reprogrammed to restore the internal state of the device's configuration memory (SRAM device). A specialized mitigation technique described in [18] enables the identification and classification of errors as either being due to permanent faults or transients, as well as identifying if the error affects a replicating module, user voter or the mitigation scheme itself [19]. This self-checking capability allows for the origin of the internal fault to be identified and corrected. This mitigation scheme has been implemented in the Xilinx XC4000 FPGA.

SEU protection insertion discussed in [20] utilizes a tool which implements SEU protection mechanisms for both the FPGA memory elements and registers automatically. The protection is implemented in the VHDL code and is based on Hamming coding and two dimensional parity arrays.

The guard-gate mitigation scheme seen in [21] makes use of a SET filter, consisting of an inverter string which delays the signal along a path. All signals with a pulse width shorter than the delay are filtered out, in essence filtering out the transient and preventing it from being latched into memory.

The AND-OR multiplexer SET filter described in [15] mitigates SEUs by filtering out single event transients. The mitigation technique offers two variations for implementation in circuits where single or double input lines are available. The mitigation scheme can be seen to be combined with TMR to ensure effective mitigation.

The main contribution of this thesis was to develop an experimental procedure to experimentally determine the single event upset and total ionizing dose effects of the ProASIC3 A3P1000 flash based FPGA in a space radiation environment. The research presented aimed to examine the SEU cross section and TID effects of various mitigation schemes and control circuits implemented in the A3P1000. It also aimed to determine the effectiveness of the implemented mitigation schemes in order to draw comparisons between them.

1.2 Outline of the thesis

1.2.1 Chapter 2

Chapter 2 covers the theoretical background topics related to the single event upset and total ionizing dose testing. A summary of the space orbits and environment in which satellites operate in presented, followed by the common radiation sources found in space. This chapter also provides a brief description of CMOS, MOSFET, ASIC and FPGA devices and discusses the single event effects and total ionizing dose effects on FPGAs, which forms the basis of testing during this research.

1.2.2 Chapter 3

Chapter 3 discusses the research motivation for this project, as well as the real world effects of radiation. The shortcomings of current solutions to the radiation effects faced in a space based

applications are then discussed, together with a new focus on the use of commercial off the shelf components in these space applications. Radiation hardened FPGAs and current mitigation schemes are then discussed which aim to reduce and even eliminate the effects which radiation plays on the device. This chapter aims to provide an overview of the current issues faced and proposed solutions suggested when considering the implementation of a FPGA in a space based application.

1.2.3 Chapter 4

In chapter 4 the research procedure is described in detail. The primary objectives of the experimental tests conducted are described, together with a description of the ProASIC3 A3P1000 device used during testing. The SPI, I2C, UART communication protocols, in addition to the DC, stepper and servo motor control circuits implemented in the FPGA during testing, are described in detail in order to gain a better understanding of the implemented code which was tested. The various mitigation techniques implemented are also described in this chapter, outlining the structure of each such that a clear comparison can be made between them. The data acquisition device and method of capturing and monitoring data is described together with the experimental set-up for both the SEU and TID testing conducted. Furthermore, the design of the mechanical system implemented at the iTemba LABS facility can be seen in this chapter. This chapter also illustrates the detailed design schematics and strength analyses required to design and implement the mechanical platform. The LabVIEW code written for the control of the mechanical system, as well as for the data monitoring, can be found in this chapter. Photographs of the experimental set up and equipment at both the TID and SEU testing facilities are also included in this chapter.

1.2.4 Chapter 5

Chapter 5 presents the results obtained from both the high energy proton SEU testing and the absorbed dose response TID testing. The SEU results from the two testing sessions, each consisting of multiple tests, will be presented and discussed to describe the error rate observations as well as the SEU cross sections of the test circuits implemented in the FPGA. The TID results obtained from the testing conducted at the FruitFLY facility are also presented in this chapter. The error rate of each of the implemented circuits as well as the device current and voltage characteristics will be presented and discussed.

1.2.5 Chapter 6

Chapter 6 discusses the data presented in chapter 5 and draws conclusions from the experiments conducted. The findings thereof are presented, together with recommendations for related future work and improvements which would prove to be beneficial if similar testing were to be conducted.

2 Theoretical Background

Space is a harsh environment characterised by the presence of various sources and levels of radiation, vast ranges of temperatures, virtually no gravity effects, very low density of matter and an almost perfect vacuum. When implementing an electrical, mechanical or control system in a space environment, it is essential to consider these factors, especially the extreme temperatures and the radiation and vacuum effects of space on the components to be used. Either one of these variables could result in the malfunctioning of components or systems, in turn, resulting in the failure of the mission. The following sections will introduce a basic theoretical background to certain aspects of the space environment and related concepts.

2.1 Fundamental Concepts

2.1.1 Energy

Radiation energy is generally defined in terms of the Electron Volt (eV). The electron volt is not a SI unit, but rather a value that must be experimentally determined. The electron volt is a unit of energy approximately equal to $1.60217657 \text{ X } 10^{-19}$ joules and is defined as the amount of kinetic energy gained by a single unbound electron as it is accelerated through an electric potential difference of one volt [22]. The Electron volt was defined as a standard as a result of the usefulness in electrostatic particle accelerator sciences as a particle with charge q has an energy of E=qV once passed through a potential V [22].

2.1.2 Radiation Dose

Radiation can be measured and described in two units. The first is a measure of the rate of exposure experienced. The second is a measure of the total amount of radiation accumulated over a specific time period. Radiation dose is a measurement of the energy deposited by a source of ionizing radiation per unit mass of a specific material. The SI unit of the absorbed radiation dose is joules per kilogram, named gray (Gy), and the non-SI unit being the rad. The relationship between the rad and gray can be seen in equation 1 [23].

1 rad = 1 Ergs/g

1 Gy = 1 J/kg

$$Dose = \frac{\Delta E}{\Delta m} \text{ and } 1Gy = 1\frac{J}{kg} = 100\, rads = 10^4\, Ergs/g$$

Equation 1

The absorbed dose is defined as the amount of energy (ΔE) deposited by the ionizing radiation per unit mass of material (Δm) [24]:

2.1.3 Flux

The flux can be defined as the number of particles passing through a 1 cm^2 area during a 1 second interval. The unit is thus particle/$cm^{-2}s^{-1}$.

$$\Phi = \frac{\dot{Photons}}{Area\ Time}$$

Equation 2

2.1.4 Fluence

The fluence is obtained by integrating the flux over the time giving the unit particles/cm^{-2}.

$$\Phi = \frac{Photons}{Area}$$

Equation 3

2.1.5 Linear Energy Transfer

The linear energy transfer (LET) is defined as the amount of energy deposited per unit length and is represented in units of eV/cm [24]. The LET of a charged particle is known to be proportional to the square of the charge and inversely proportional to the kinetic energy of the particle defined as: Q^2/E_k. The LET is also a product of specific ionization and the average energy deposited per ion pair [24].

The LET has the unit MeV/(g/cm2) and is defined by the following equation:

$$LET = \frac{1}{\rho}\frac{dE}{dx}$$

Equation 4

Where ρ is the density of the material, E is the energy loss through the material and x is the distance.

2.2 Orbits

The orbit or region of space in which the designed system will operate in will be of great importance when designing the electrical and mechanical subsystems. The orbit in which the space platform will operate will determine the instantaneous energy and total dose of the radiation experienced by the platform. When considering the amount of radiation which will be present in the desired operating region of space, the operating characteristics and expected operating life cycle of the system can be estimated. Satellite orbits can be broadly classified into the low earth orbit, medium earth orbit and high hearth orbit.

2.2.1 High Earth Altitude and ground

The high earth altitudes occupied by commercial and military aircrafts range from of 30 000 feet (9.144km) to 60 000 feet (18.288km) [25, 26, 27]. Sensitive electronics on board these aircrafts will experience high energy particle strikes from galactic cosmic rays, as well as total ionizing dose accumulation. The GCR flux exposure is approximately doubled for each 6000 feet increase in altitude, reaching a maximum at 60 000 feet. SEE are of greater importance at these altitudes than TID. The amount of absorbed radiation in a 20 year life cycle of an avionic system would be in the region of 110 rad, a large factor less than required to induce any errors [25, 26, 27]. Only SEEs are considered at ground level as the amount of absorbed radiation will have no impact on electronics. Figures 1 and 2 show the various flux measurements at varying altitudes and latitudes.

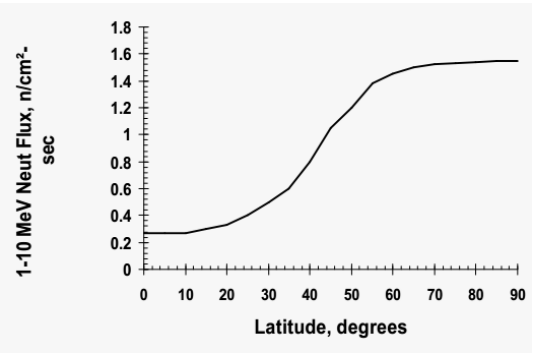

Figure 1: Flux at varying latitudes [26]

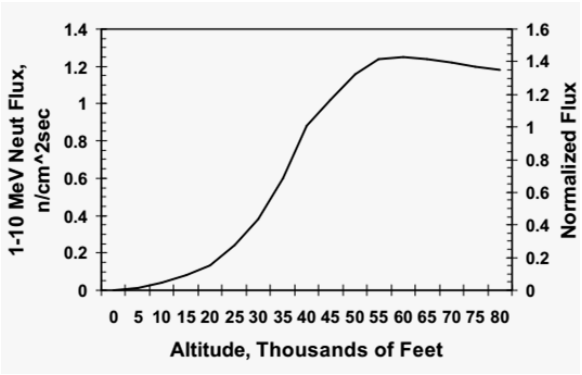

Figure 2: Flux at various altitudes [26]

Figures 3 and 4 [25] illustrates the measured and calculated dose rate on board two different flights.

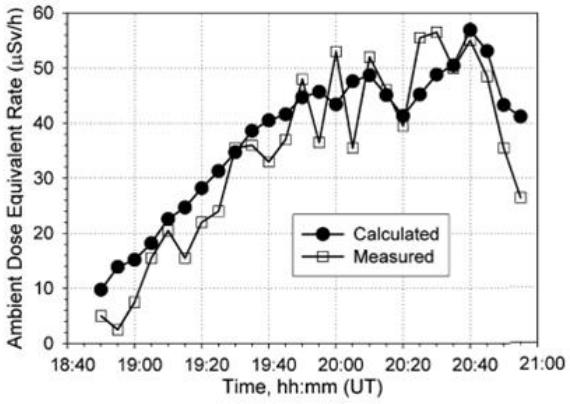

Figure 3: Dose rate on board a Concorde flight [25]

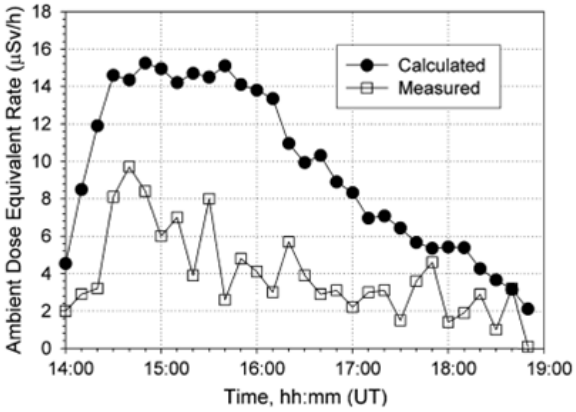

Figure 4: Dose rates on-board an A310-300 flight [25]

2.2.2 Low Earth Orbit

Low earth orbit is characterized by an approximate distance of 160 to 1 400 kilometres away from the surface of the earth [28]. The majority of scientific research, weather monitoring, satellite phone and military satellites are found in this orbit.

Low earth orbit satellites primarily experience ionizing radiation from sources such as galactic cosmic rays (GCRs), energetic electrons and protons trapped in the geomagnetic field and the earth's natural radiation belts and solar particle events (SPEs) [29].

2.2.3 Medium Earth Orbit

Medium earth orbits are classified as being a distance of 6 000 to 27 000 kilometres from the earth's surface and is primarily used by global positioning system (GPS), observation, weather and spy satellites [30]. Medium earth orbits include a semi-synchronous orbit which allows a satellite to constantly cross over the same position on the equator each day. This also includes the Molniya orbit, which allows a satellite to access and communicate with in the far northern and southern areas of the earth's surface as oppose to the geostationary satellites [30].

The primary source of radiation found in the medium earth orbit originates from the Van Allen radiation belts [31]. Additional radiation sources also include galactic cosmic rays and solar particle events.

2.2.4 Geostationary Orbit

This orbit is defined by a distance of approximately 36 000 kilometres from the surface of the earth. The most common satellites found in this orbit include weather, television, long distance communication, internet and GPS satellites. Geostationary satellites at a distance of approximately 36 000 kilometres have a constant velocity of 11080 km/h about the equator and follow the earth's rotation as a result. The geostationary satellites are able to maintain their relative position over a longitude, but may drift north or south. These satellites have little capabilities to monitor the northern or southern areas of the earth. [28, 30].

The primary source of ionizing radiation in the geostationary orbit originates from the outer electron belt of the earth's trapped radiation belts. Additional sources include radiation from solar particle events and galactic cosmic rays.

2.2.5 High Earth Orbit

High earth orbits are classified as being more than 36 000 kilometres above the surface of the earth and are commonly occupied by space observation and weather observation satellites [32]. Space systems found in the high earth orbit have no protection from the earth's magnetic field and thus are vulnerable to galactic cosmic rays and solar particle events. Figure 5 illustrates the basic Earth orbit layout.

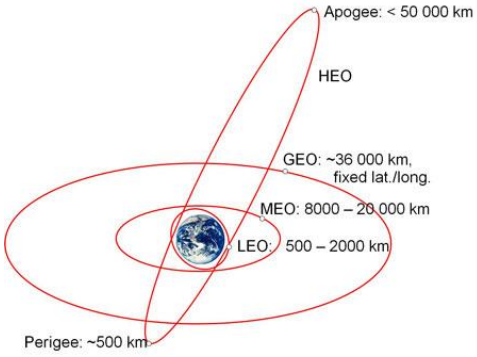

Figure 5: Basic orbit layout [32]

2.3 Space Radiation Environment

2.3.1 Vacuum

In addition to the presence of radiation, the space environment can also be characterized by a lack of matter (vacuum) and atmosphere. Only a few hydrogen and helium atoms can be found per square meter, and additionally, due to the gravitational pull of larger bodies in space such as planets, the atoms are found closer to these bodies [33, 34]. The lack of air in space prevents the transfer of heat from components such as motors or voltage regulators into the atmosphere, preventing the components from being able to dissipate heat at the required rate. Another consideration to take into account when designing the electrical or mechanical system is the physical properties of the component. An electrical component which contains trapped air will result in a pressure difference between the outer space environment, this internal structure will then result in the failure of the component. The pressure difference between, for example, the trapped air and the vacuum will lead to the physical failure of the device.

The same applies to motors and bearings which are manufactured in such a manner that trapped air cannot escape. In addition to the previously stated design considerations, lubrication is not able to function correctly in a vacuum or non-gravity environment. The lubrication substance will leak from its original position and spread to other unintended locations. In applications where lubrication is essential, such as high revolution bearings, it will be required to make the correct design choices when considering components which will experience large amounts of motion [33, 34].

2.3.2 Temperature

The temperature of components in space is determined by the presence or lack of sunlight shining onto the component. A piece of metal exposed to sunlight for example, can reach temperatures of 260 degrees Celsius and, when in shade, can drop to far below -100 degrees Celsius [35]. A special coating may be applied to the surface of exposed metals, resulting in a temperature range of the materials between 120 to -129 degrees Celsius [36]. Precautions must be taken as to the specified operating temperatures of any mechanical or electrical components implemented on board a space platform.

2.3.3 Radiation

The measuring and quantifying of the radiation environment in space has long been an area of interest for many scientists and companies. The space environment typically consists of a large variety of primary particles of varying ranges of energies and secondary particles created by a number of different nuclear interactions [29]. Even though the large numbers of particles have a wide range of energies, their flux is often low. Occurrences such as solar flares are often the only times at which the flux levels are dramatically higher. This variation in energy and flux levels requires the components, which are implemented in a space system, to be robust.

Naturally occurring radiation in space comprises of protons, electrons and heavy ions of elements from the periodic table [37] as well as secondary neutrons created by interactions of solar particles with the atmosphere and materials. Radiation can be defined as energy in motion in the form of high speed particles or electromagnetic waves [38] and can further be classified as being either ionizing or non-ionizing radiation.

Ionizing Radiation has adequate energy to remove electrons from atoms, thus creating charged particles. Due to the high energy of the radiation, electrons from inner orbits are able to be removed creating a highly unstable atom. Sources of high energy ionizing radiation include protons and gamma rays.

Non-ionizing radiation does not have sufficient energy to remove electrons from atoms and thus are not considered to negatively impact any part of electronic space operations. Sources of non-ionizing radiation include radio waves and microwaves [38].

2.4 Radiation Sources

FPGAs in the space environment will mainly be implemented on board satellites and data collecting space craft systems, the more common being satellites. Most satellites are found in low, medium and high earth orbits where radiation source typically include plasma radiation, trapped radiation, cosmic rays and solar flares [39]. Any space system in operation will be exposed to radiation originating from a number of sources characterized by varying energy and magnitudes of flux. The

three principal sources of space radiation are; galactic cosmic rays, trapped radiation and solar particle events. Figure 6 demonstrates the principal space radiation sources.

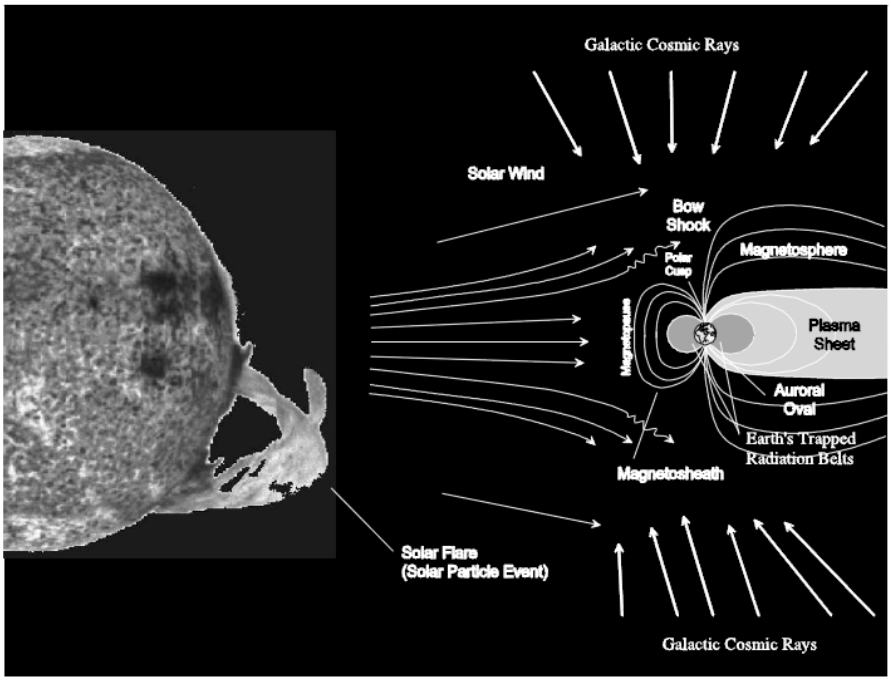

Figure 6: Principal space radiation sources [29]

2.4.1 Galactic Cosmic Rays

Galactic cosmic rays consist of high energy particles, the majority of which are protons, originating from space. The main contributing particles for electronics include neutrons and protons.

2.4.1.1 Ionizing Radiation Dose

The ionizing radiation dose originating from GCRs can be seen as insignificant compared to that of trapped radiation. Flux originating from GCRs are affected and attenuated by the geomagnetic field which prevents penetration of low orbits of low inclinations [39]. The main variable is the inclination of the orbit, as seen in the example of a 500 km 30 degree inclination orbit, there is almost no penetration, but for a 500 km 57 degree inclination orbit, where penetration occurs and for polar orbits the exposure is high at any altitude [39].

Despite the fact that geomagnetic shielding is ineffective for GEO, the average dose for ordinary events with a spherical shielding of 2 gram/square centimetre is approximately 18 rad (Si)/year. For an anomalously large flare and the same shielding as mentioned above, the dose would be as high as 600 rad(Si)/event [39].

Table 1 shows solar flare shielded doses for 1 anomalously large event for the geostationary orbit [39].

Table 1: Solar flare dose with shielding in geostationary orbit

	MAGNETOSPHERICALLY UNATTENUATED		MAGNETOSPHERICALLY ATTENUATED TO 70DEG W		MAGNETOSPHERICALLY ATTENUATED TO 160DEG W	
S (GM/SQCM)	SLAB(4PI) (RADS-SI)	SOLID SPHERE (RADS-SI)	SLAB(4PI) (RADS-SI)	SOLID SPHERE (RADS-SI)	SLAB(4PI) (RADS-SI)	SOLID SPHERE (RADS-SI)
0.01	4.690E+03	4.597E+03	4.796E+02	4.782E+02	2.680E+02	2.675E+02
0.02	4.762E+03	4.645E+03	4.810E+02	4.781E+02	2.686E+02	2.674E+02
0.03	4.812E+03	4.688E+03	4.824E+02	4.782E+02	2.692E+02	2.675E+02
0.04	4.846E+03	4.737E+03	4.838E+02	4.784E+02	2.696E+02	2.675E+02
0.05	4.868E+03	4.788E+03	4.850E+02	4.786E+02	2.702E+02	2.676E+02
0.06	4.878E+03	4.850E+03	4.862E+02	4.788E+02	2.708E+02	2.676E+02
0.08	4.872E+03	4.950E+03	4.886E+02	4.794E+02	2.718E+02	2.678E+02
0.10	4.828E+03	5.221E+03	4.910E+02	4.802E+02	2.728E+02	2.680E+02
0.20	4.004E+03	5.875E+03	5.000E+02	4.849E+02	2.768E+02	2.696E+02
0.30	3.202E+03	5.117E+03	5.062E+02	4.902E+02	2.802E+02	2.716E+02
0.40	2.680E+03	4.429E+03	5.110E+02	4.950E+02	2.826E+02	2.737E+02
0.50	2.298E+03	3.957E+03	5.144E+02	4.998E+02	2.846E+02	2.758E+02
0.60	2.004E+03	3.553E+03	5.168E+02	5.051E+02	2.862E+02	2.776E+02
0.70	1.774E+03	3.216E+03	5.182E+02	5.108E+02	2.874E+02	2.794E+02
0.80	1.587E+03	2.966E+03	5.190E+02	5.168E+02	2.884E+02	2.814E+02
0.90	1.428E+03	2.727E+03	5.188E+02	5.232E+02	2.892E+02	2.836E+02
1.00	1.296E+03	2.512E+03	5.180E+02	5.297E+02	2.898E+02	2.860E+02
1.25	1.038E+03	2.134E+03	5.130E+02	5.488E+02	2.900E+02	2.921E+02
1.50	8.504E+02	1.795E+03	5.038E+02	5.690E+02	2.890E+02	2.988E+02
1.75	7.120E+02	1.592E+03	4.908E+02	6.002E+02	2.868E+02	3.061E+02
2.00	5.978E+02	1.402E+03	4.736E+02	6.153E+02	2.83[illegible]E+02	3.144E+02
2.50	4.430E+02	1.037E+03	4.244E+02	7.829E+02	2.736E+02	3.334E+02
3.00	3.424E+02	8.769E+02	3.406E+02	8.544E+02	2.592E+02	3.626E+02
3.50	2.654E+02	7.021E+02	2.654E+02	6.989E+02	2.394E+02	3.929E+02
4.00	2.136E+02	5.719E+02	2.136E+02	5.725E+02	2.118E+02	4.972E+02
4.50	1.733E+02	4.956E+02	1.733E+02	4.954E+02	1.733E+02	5.004E+02
5.00	1.418E+02	4.160E+02	1.418E+02	4.161E+02	1.418E+02	4.147E+02
6.00	9.860E+01	3.047E+02	9.860E+01	3.047E+02	9.860E+01	3.050E+02
8.00	5.120E+01	1.759E+02	5.120E+01	1.759E+02	5.120E+01	1.759E+02
10.00	2.870E+01	1.094E+02	2.870E+01	1.094E+02	2.870E+01	1.094E+02
15.00	7.984E+00	3.464E+01	7.984E+00	3.464E+01	7.984E+00	3.464E+01
20.00	2.558E+00	1.580E+01	2.558E+00	1.580E+01	2.558E+00	1.580E+01
30.00	1.104E-01	1.250E+00	1.104E-01	1.250E+00	1.104E-01	1.250E+00

2.4.1.2 Single Event Effects

Galactic cosmic rays and anomalously large events for transitioning protons are the most likely sources to cause SEEs. Cosmic ray induced SEEs are much more common than proton induced SEEs at altitudes below 1000 km and above 4000 km for 60 degree circular orbits [39]. The earth's magnetic field shields low inclination orbits from cosmic rays, resulting in a decrease as oppose to the proton upset rates. Higher inclination orbits thus experience higher upset rates due to cosmic radiation.

Galactic cosmic rays (GCRs) originate from outside of our solar system and are speculated to be isotropic throughout space. GCRs particles in our solar system have been measured to have energies of between tens up to 10^{12} MeV (10 GeV) nucleon^{-1} and have the highest penetrating capabilities of

the ionizing radiation types [40]. Sources of GCRs mainly include supernovae and neutron starts within our galaxy and partially from our sun. The magnetic field of the sun, as well as solar winds, modulate the flux of ions with energies of 10 GeV or less and a large attenuation of the flux is experienced during the high activity solar maximum periods. [41].

Table 2: Characteristics of galactic cosmic rays [40]

Hadron Composition [11]	Energies	Flux	Radiation Effects	Metric
87% protons 12% alphas 1% heavier ions	Up to ~10^{11} GeV	1 to 10 $cm^{-2}s^{-1}$	SEE	LET

The GCR spectrum comprises of 98% protons and heavy ions (baryon component) and 2% electrons and positrons (lepton component) and the baryon component consists of 87% protons, 12% helium ions (alpha particles) and 1% heavy ions [40] as seen in Table 2. The high energy heavy ions are of great importance in single event effects (SEE) testing and have high linear energy transfer (LET) and penetrating characteristics. The flux of the GCR is usually in the range of 1 to 10$cm^{-2}s^{-1}$ and dependent on solar cycles [41].

Figure 7 illustrates the typical GCR energy spectrum of a few elements during a solar minimum and maximum [41].

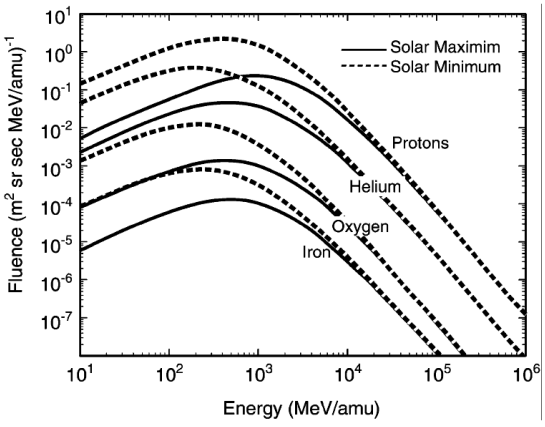

Figure 7: GCR energy spectra for protons, helium, oxygen and iron [41]

Due to the particle composition of GCRs, low energy particles readily lose their energy once they penetrate the magnetosphere and due to the earth's magnetic field as well as are deflected away

from the earth at the equator as a result of the geomagnetic field lines being parallel to the earth's surface, but the protection has no effect in the geosynchronous orbit (36 000km) where the earth's magnetic field is weak. The geomagnetic filed lines at the poles are directed towards the earth at the poles, resulting in GCR particles being funnelled towards the high altitudes [23, 29].

2.4.2 Trapped Radiation

The radiation environment around the earth can be described as a high concentration of energetic ionizing electrons and protons together with small amounts of low energy heavy ions [39] which are trapped within two toroidal shaped radiation belts called the Van Allen Belts, found in the earth's magnetosphere [29, 40]. The inner radiation belt (IRB) is theorized to extend from approximately 0.1 to 2.4 earth radii and comprises of electrons of energies up to 5 to 10MeV and protons of energies up to approximately 700 MeV. The majority of trapped protons have energies of between 150 and 250 MeV and these energies and abundance decrease with the distance from the earth. The outer radiation belt (ORB), which extends from between approximately 2.8 to 4 earth radii, to between approximately 10 to 12 earth radii consists of electrons with energies below a maximum of 10MeV and no significant number of protons [29, 40]. The level flux found in the IRB is much lower than that found in the ORB resulting in higher dose rates for humans and electronics in this belt [41, 42]. Figure 8 illustrates the three types of motion of charged particles in the Earth's radiation bands.

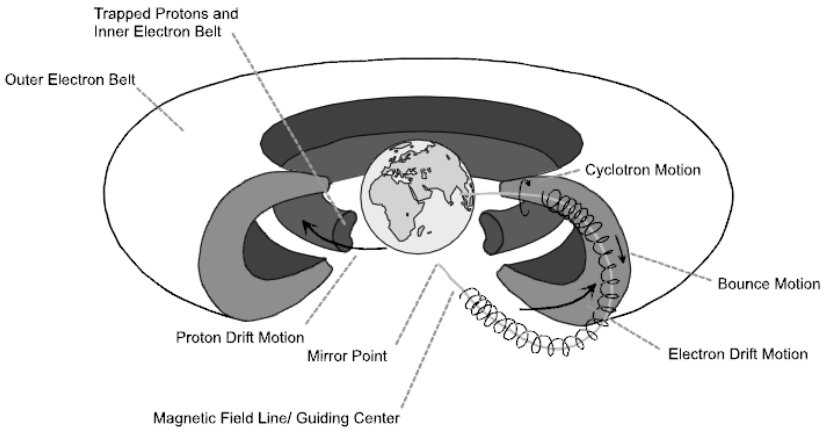

Figure 8: In the Earth's radiation bands, three types of motion can be seen for charged particles, namely; cyclotron motion, bouncing motion and drift motion [29, 39]

Due to the earth's axis of rotation and magnetic field axis being misaligned, a region known as the South Atlantic Anomaly (SAA) has been an important area of research and concern for low orbiting

space crafts. This area experiences high levels of trapped protons due to the intersection of the trapped proton belt with orbiting space crafts. Research has discovered that "for the 51.56^{o} inclination, 400 km altitude orbit of the ISS, about half the ionizing radiation dose is due to trapped protons in the SAA and half originates from GCR at higher altitudes" [29]. Figures 8 and 9 show the flux curves over the SAA.

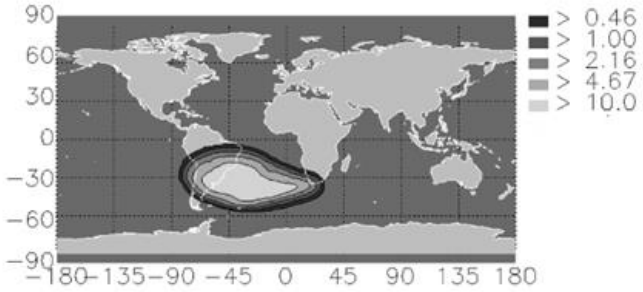

Figure 9: Iso-Flux curves for 9.4MeV protons [29]

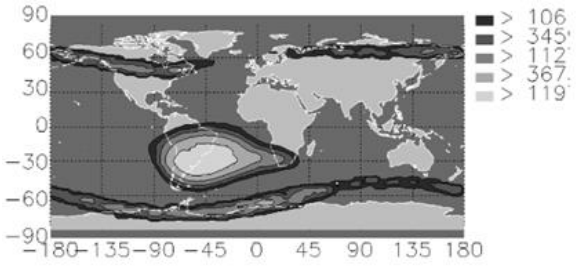

Figure 10: Iso-Flux curves for 560keV electrons [29]

The movement of the trapped particles can be defined as circling around and bouncing along magnetic field lines, while also being reflected back and forth between mirror points in opposite hemispheres, as shown in Figure 8. [29, 39] Additional movement of particles include the longitudinal drift of electrons to the east and protons to the west [23].

At the geostationary orbit protons have energies between 100 keV and 1MeV, while electrons have energies of between 100keV and a few MeV [41].

2.4.2.1 Ionizing Radiation Dose

The calculated daily dose for LEO and GEO for an orbit altitude of 500km and inclination of 60 degrees [39] can be seen in Table 3.

Table 3: Daily dose for 500km/60 degree orbit during solar minimum [39]

S	T	T	ELEC	BREM	PROTON	TOTAL
GM/SQCM	MM	MILS	RADS-AL	RADS-AL	RADS-AL	RADS-AL
0.01	0.04	1.00	4.304E+02	1.679E-01	6.493E+01	4.955E+02
0.02	0.07	3.00	2.406E+02	1.187E-01	2.498E+01	2.657E+02
0.03	0.11	4.00	1.539E+02	9.230E-02	1.545E+01	1.694E+02
0.04	0.15	6.00	1.076E+02	7.633E-02	1.071E+01	1.184E+02
0.05	0.19	7.00	7.992E+01	6.540E-02	7.814E+00	8.780E+01
0.06	0.22	9.00	6.208E+01	5.710E-02	6.268E+00	6.841E+01
0.07	0.26	10.00	4.989E+01	5.060E-02	5.159E+00	5.510E+01
0.08	0.30	12.00	4.115E+01	4.537E-02	4.395E+00	4.559E+01
0.09	0.33	13.00	3.468E+01	4.110E-02	3.844E+00	3.857E+01
0.10	0.37	15.00	2.967E+01	3.756E-02	3.389E+00	3.310E+01
0.20	0.74	29.00	1.090E+01	2.170E-02	1.675E+00	1.260E+01
0.30	1.11	44.00	6.208E+00	1.625E-02	1.164E+00	7.389E+00
0.40	1.48	58.00	4.088E+00	1.316E-02	9.099E-01	5.011E+00
0.50	1.85	73.00	2.833E+00	1.104E-02	7.575E-01	3.601E+00
0.60	2.22	87.00	2.008E+00	9.501E-03	6.737E-01	2.691E+00
0.80	2.96	117.00	1.056E+00	7.438E-03	5.723E-01	1.636E+00
1.00	3.70	146.00	5.778E-01	6.156E-03	5.052E-01	1.089E+00
1.25	4.63	182.00	2.756E-01	5.123E-03	4.589E-01	7.396E-01
1.50	5.56	219.00	1.309E-01	4.425E-03	4.216E-01	5.570E-01
1.75	6.48	255.00	6.178E-02	3.921E-03	3.964E-01	4.621E-01
2.00	7.41	292.00	2.811E-02	3.540E-03	3.764E-01	4.081E-01
2.50	9.26	365.00	4.293E-03	3.016E-03	3.411E-01	3.484E-01
3.00	11.11	437.00	4.175E-04	2.677E-03	3.140E-01	3.171E-01
3.50	12.96	510.00	8.088E-06	2.436E-03	2.882E-01	2.907E-01
4.00	14.81	583.00	0.000E+00	2.251E-03	2.689E-01	2.711E-01
4.50	16.67	656.00	0.000E+00	2.099E-03	2.524E-01	2.545E-01
5.00	18.52	729.00	0.000E+00	1.970E-03	2.364E-01	2.384E-01
6.00	22.22	875.00	0.000E+00	1.756E-03	2.098E-01	2.116E-01
8.00	29.63	1167.00	0.000E+00	1.453E-03	1.706E-01	1.721E-01
10.00	37.04	1458.00	0.000E+00	1.233E-03	1.421E-01	1.433E-01

2.4.2.2 Single Event Effects

The high energy protons trapped in the space environment are able to cause single event effects in semiconductor electronics. At an altitude of 2600 km and inclination of 60 degrees, the maximum upset rate occurs, with a single event upset rate of 0.1 upsets/bit-day for susceptible electronics with typical shielding [39].The upset rate of protons at low altitude orbits and a low inclination are generally determined by the South Atlantic Anomaly.

2.4.3 Solar Particle Events

The main source of solar energetic particles (SEPs) includes solar flares and sporadic eruptions of the sun's chromospheres [40]. The flux emitted contains protons, and heavy charged particles and electrons. The most important of these being protons, due to their abundance and high energy levels. Solar particle events are considered to be rare and are generally limited to the 11 year solar cycle. During this cycle of 11 years, 7 are high activity years and 4 years are of low activity [41].

Two generally accepted indications of the solar cycle include the number of sunspots and solar 10.7cm radio flux (F10.7) [41]. More emphasis has been put on forecasting and predicting solar cycle activity in recent years. It is known that during the declining phase of the solar maximum, the larger

solar particle events are likely to occur more regularly. It is also know that electron flux will be larger during the declining phase and the proton flux will be at a maximum during the solar minimum phase [41].

A solar particle events is defined as an event with a total proton fluence of >30 MeV of 10^6, 3 X10^6 and 10^7 cm^{-2}, which generally has proton energies in the region of 20 to 80 MeV. Approximately 50 of these events can occur during a solar cycle [29, 40].

The manner in which SPEs are produced allows SPEs to be defined as either those which are produced by impulsive flares or those which are produced by coronal mass ejections (CMEs) [29]. SPEs which result from impulsive solar flares have short durations, usually only lasting a few hours. These SPEs also have large fluxes of electrons, with a total fluence of between 10^7 and 10^8 cm^{-2}, which is relatively small. These SPEs are limited to a 30 to 45 degree angle in solar latitude [29]. SPEs as a result of CMEs have a longer duration in the order of days and also have higher proton fluxes of which the total fluence can be larger than 10^9 cm^{-2}. The solar latitude angle extends from 60 to as much as 180 degrees.

Table 4: Characteristics of SPEs [41]

Hadron Composition	Energies	Integral Fluence (>10MeV/nuc.)	Peak Flux (>10MeV/nuc.)	Radiation Effects
96.4% protons 3.5% alphas ~0.1% heavier	Up to ~GeV/nuc.	Up to ~10^{10} cm^{-2}	Up to ~10^5 cm^{-2} s^{-1}	TID DD SEE

2.4.4 Atmospheric ionizing radiation

This secondary form of radiation occurs as a result of the primary GCR particles interacting with the earth's atmosphere. The intensity and energies of the primary GCR and secondary particles are dependent on the altitude, location in the geomagnetic field and the solar cycle stage [40].

2.4.5 Dose Levels in space orbits

The dose rates for various orbits in space are of importance for total ionizing dose effects on microelectronics. The following are the dose rates for specific orbits [23, 24]:

- Low Earth Orbit 0.1 kRads/year
- Medium Earth Orbit 100 kRads/year
- Geostationary Earth Orbit 10 kRads/year

2.4.6 Testing Facility Sources

2.4.6.1 Total ionizing dose

The facility available for the experiment is the Agricultural Council Facilities in Stellenbosch which allows the tests to be performed with a Colbat-60 (Co-60) source. The Co-60 source produces Gamma rays with energies close to 1.3MeV and a radiation dose of 845.08 rad/minute. The source will allow for good long term characterization of exposing a FPGA to a radiation source.

2.4.6.2 Single Event Upset

The SEU testing will be conducted at the iThemba Laboratories in Cape Town. This research facility is able to produce protons with energies of up to 66MeV for regular testing and 200MeV if the request for a higher energy is approved. The dose rate is not of interest for SEE testing.

2.5 Natural shielding

2.5.1 Magnetosphere

A magnetosphere is generated when a constant stream of charged particles interact with, and is deflected by, the intrinsic magnetic field of a planet [43]. The shape of the magnetosphere is characterized by the earth's magnetic field, solar winds and interplanetary magnetic fields (IMF) [44]. The physical shape of the magnetosphere is non-spherical and extends to approximately 70 000km (10-12 Earth radii) on the sun's side. The tail side of the magnetosphere, on the night side of the earth, is shaped like a cylinder with a radius of approximately 20-25 radii with the magnetotail extending to over 200 earth radii [44].

The Earth's magnetosphere deflects solar wind, cosmic rays and high energy charged particles originating from outside of the solar system. The charged particles which enter the magnetosphere spiral around filed lines, moving back and forth between the poles several times per second [45].

The interaction between solar winds and the earth's geomagnetic field produces energy, stored as potential energy in the magneto tail, this causes a magnetic substorm and, as a result, auroral activity in the upper atmosphere occurs. This occurrence can cause the surfaces of spacecraft to

become highly charged, causing a discharge in the form of electrical arching [23, 24]. Figure 11 illustrates the Earth's magnetosphere and radiation sources.

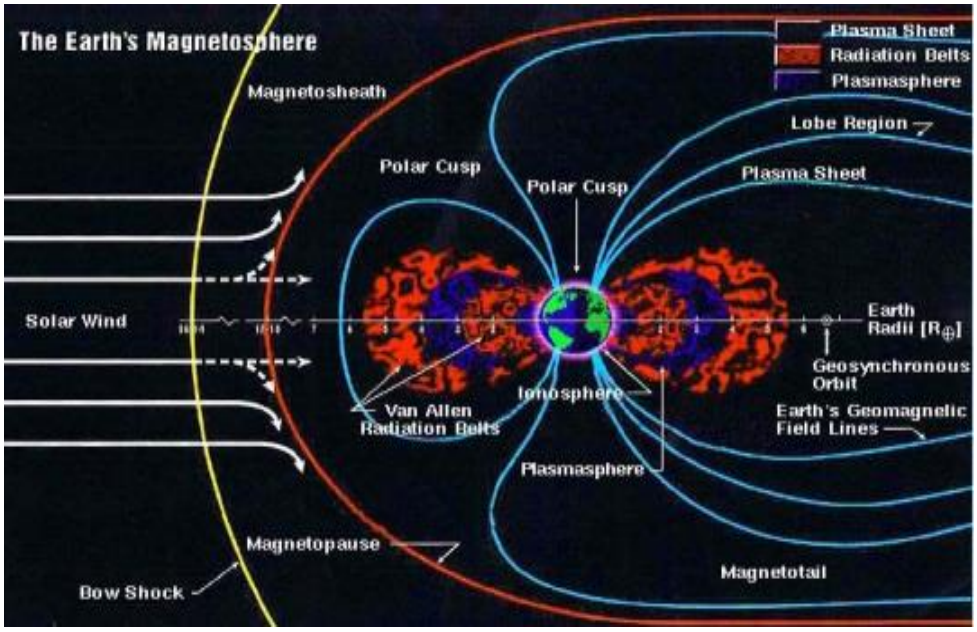

Figure 11: Earth's magnetosphere [46]

2.5.2 Geomagnetic shielding

The earth's magnetosphere deflects most of the charged particles originating from outside of the magnetosphere and prevents the particles from entering. The charged particles are deflected away via the Lorentz force, but this force is opposed by the particles' own momentum. The ability of a charged particle to penetrate a geomagnetic field is dependent on the particle's magnetic rigidity defined in equation 5 [47]:

$$p = \frac{pc}{Ze}$$

Equation 5

Where p = relativistic momentum expressed in units of eV/c, c = velocity of light, 2.998X 10^{8} ms^{-1}, e = elementary charge, 1.602 X 10^{-19} c and Z = atomic number. Figure 12 demonstrates the method of calculating the required energy to penetrate the magnetosphere.

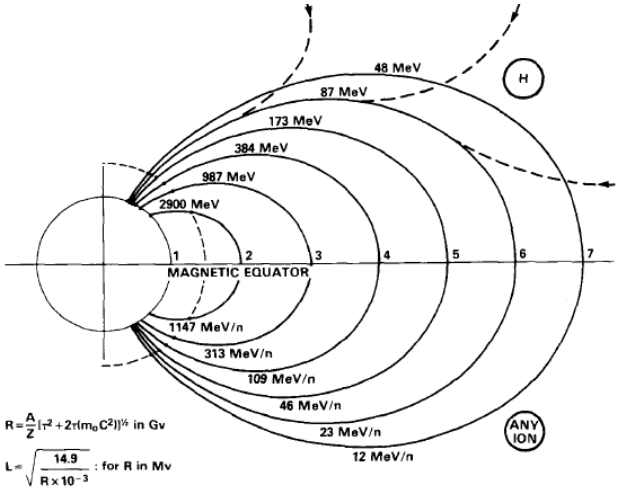

Figure 12: Energy required to penetrate the magnetosphere

2.6 Radiation interactions with matter

The interaction and energy loss of radiation particles can be classified into two categories, namely (direct) ionizing and (indirect ionizing) non-ionizing radiation. The first, ionizing radiation includes; Alpha particles, electrons, protons, positrons and beta particles. The interaction of charged particles with matter is described as electric (coulomb) forces which dispose of their energy as ionization and excitation [23, 24].

The second category, uncharged (indirect ionizing) particles which include neutrons and y-quantums is the radiation of particles with no charge. These particles can transfer energy to the absorbing matter by transferring energy to charge particles, nuclei and atom electrons as a result of nuclear or electromagnetic interactions. [23, 24].

2.6.1 Charged particles (direct ionizing)

2.6.1.1 Alpha particles

Alpha particles have strong interactions with matter due to being relatively heavy in addition to having charge. During an interaction, a large number of ions per unit length are produced, resulting in less penetration. Alpha particles are able to interact with both orbiting electrons and the nuclei in any absorbing material [23, 24]. Alpha particles passing close to a nucleus can be deflected away

with no change in energy (Rutherford scattering), deflected away with a small change in energy or absorbed by the nucleus, resulting in nuclear transformation [23, 24].

The most commonly found process which occurs during the absorption of alpha particles is the excitation and ionization of orbital electrons. During excitement, the incident particle transfers an amount of its energy into the electrons of the absorbing material by pulling (attracting) the electron towards it and out of its belt. This energy “excites” the electron and the gained energy promotes the electron to a further orbit. However, after excitation the transferred energy is not sufficient to surpass the binding energy of the electron, resulting in the electron returning to its original, lower energy, orbit. During the de-excitation phase, the electron will emit the excitation energy in the as electromagnetic radiation [23]. If the amount of energy transferred surpasses the binding energy of the electron, an ion pair will be created during an ionization effect. The ion pair will comprise of an ejected electron and positively charged atom [23, 24].

Alpha particles lose energy each time an electron is excited or when ionization occurs. This causes the Alpha particle’s kinetic energy to decrease and slow down. As the kinetic energy of the alpha particle decreases and the particle reaches the end of its path, ionization becomes more frequent. When this occurs, the kinetic energy peaks close to the end of the path and stops within a very short distance [23, 24].

2.6.1.2 Beta Particles

Beat particles are able to interact with the nuclei and orbiting electrons of the absorbing material. Beta particles passing in close proximity to a nucleus are able to be deflected with no Rutherford scattering, with minimal energy loss, or more importantly, interactions with orbiting electrons [23, 24]. Beta particle interactions with electrons are a result of repulsive electric (columbic) forces between the beta particle and the electrons, often resulting in ionization and excitation. The amount of energy lost by the beta particle during ionization or excitation is equal to the kinetic energy of the atom, together with the energy required to release or excite the electron from the atom. When free electrons fill the vacant position of the internal electron orbit, X-rays are emitted. Ultraviolet photons are produced by the excitation by beta particles of the external orbital electrons [23, 24].

After negatively charged beta particles have transferred all their energy, they will either become a "free electron" or combine with positively charged ions. Positively charged beta particles, after having transferred all of their kinetic energy, are unable to coexist with the surrounding electrons. These beta particles will be attracted to nearby electrons, and after collision, they are both annihilated. This annihilation results in two photons being released with the amount of energy equal to that of the two particle masses. These photons called "annihilation radiation" both have energies up to 0.512MeV [23, 24].

Charged particle paths

The path length of a heavy charged particle is defined by the actual distance travelled by the particle, whereas the range of the particle is defined by the depth of penetration. Figure 13 shows the typical penetration of a 7.69 MeV alpha particle from polonium 214 travelling in air. It is possible to see the Bragg ionization peak which occurs very close to the end of the range of travel [23, 24].

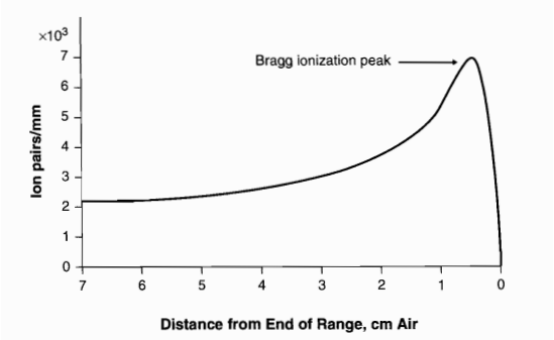

Figure 13: Path of charged particle in air [23]

2.6.1.3 Gamma and X- rays

When gamma and x-ray photons interact with a material they will either by absorbed, penetrated or scattered. These interactions can be further distinguished by the amount of energy of that photon harbours, and the density and atomic number of the absorbing material. The following processes can be described for the general case of photon attenuation: [23, 24].

- Rayleigh scattering
- Compton Effect

- Photoelectric Absorption
- Pair Production

2.6.1.4 Neutrons

Neutron interactions with the atoms of the absorbing material occur due to nuclear and electromagnetic forces. Neutrons do not directly cause excitation or ionization, but rather release or 'free' charged particles or nuclear fragments, which in turn are able to directly cause ionization and excitation. Neutrons cause collisions in light atomic nuclei. This produces 'recoil' nuclei which lead to excitation, ionization and loss of energy. Neutrons are also able to be captured and kept by atomic nuclei, producing a stable and radioactive nuclide. Or they may be reemitted to be captured by another nuclei, resulting in the binding energy being released in the form of gamma-ray emission [23, 24].

2.7 Common Space Radiation Effects on Microelectronics

The effects which radiation has on electronics can be classified as being due to either accumulation or single high energy particles. Accumulated dose effetcs, including total ionizing dose effects, result in a gradual deterioration of device performance togehter with an increased supply current to the device. Single particle effects include sinle event effects which result in instantanious effects in the device. Effects can vary from bit flips to the burning out of the device. Both of these catagories of radiation effects will be discussed in more detail in the following sections.

2.8 Complementary Metal Oxide Semiconductor (CMOS)

Metal oxide semiconductor (MOS) transistors are constructed on a semiconductor (silicone) substrate. Dopants are added to the silicone to increase conductivity (both additional electrons and holes). The structure of the MOS is constructed by superimposing a number of layers of insulating, conducting and transistor materials. Two variations of MOS transistors are thus possible to be constructed. The first, nMOS, is a negatively doped silicone with an abundance of electrons. The second, pMOS, is a positively doped silicone with an abundance of holes [48, 49].

A complementary metal oxide semiconductor (CMOS) chip is one in which both types of transistors are utilized to create any gate. COMS chips have the advantage of requiring less power than chips making use of a single type of transistor, making them suitable for tasks which utilize batteries as well as having a high level of immunity to noise. Figure 14 illustrates an n-type and p-type CMOS.

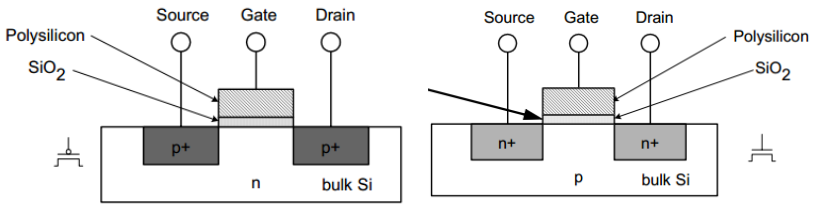

Figure 14: N and P type CMOS

2.9 Metal Oxide Semiconductors Field Effect Transistor

Metal oxide semiconductor field effect transistors (MOSFETs) form the basis of modern semiconductor technology. The general structure of the MOSFET consists of a lightly doped p-type substrate with the source and drain, both heavily doped n-type embedded in. [50, 51]. Figure 15 illustrates the symbol and cross section of an n-type MOSFET.

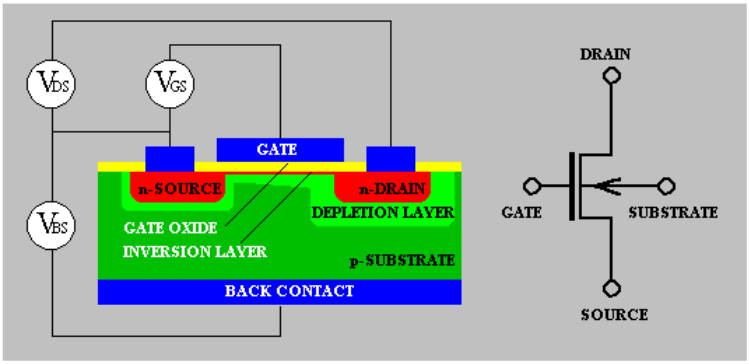

Figure 15: Cross section and circuit symbol of n-type MOSFET [52]

Current is prevented from passing from the source to the drain while the gate voltage is zero by the lightly doped p-type substrate, which has a high electrical resistance. A strong electric field across the p-type substrate material is created by applying a positive voltage to the gate [48, 49, 50, 51]. The electric field strength is determined by dividing the potential difference by the separation

distance between the gate and the body electrodes. This small distance allows for a large electric field to be created, even for small voltages [48, 49, 50, 51].

In a normally off or n-type MOSFET the positively charged gate electrode repels the holes in the p-type substrate resulting in the deformation of the band of the p-type region once the electrical field is high enough. This allows the population of electrons to accumulate in the conduction band between the source and the drain allowing current to flow though the device. Since the population of the conduction band only occurs above the critical voltage, there is no conduction or current flow below this level. This allows for the switching characteristic of the MOSFET. A normally on or p-type MOSFET is constructed of a lightly doped n-type substrate between the source and drain electrodes and requires a negative voltage applied to the gate electrode to close the device [48, 49, 50].

The voltage applied to the gate of the electrode determines the amount of current flowing between the source and drain within the FET. The MOSSFET is able to be controller with very little power and thus able to be switched on or off with a very small gate voltage and almost no current [49, 50].

2.10 Application Specific Integrated Circuits

Application specific integrated circuits (ASICs) are integrated circuits designed for a single application by a single design team. The specifically designed ASIC and all of the intellectual property and design databases remain the property of the customer and is not available to the public [51]. Improvements in technology has allowed the size of ASICs to drastically decrease as the design complexity has increased, from 5 000 gates to over 100 million gates while also including 32-bit processors and memory blocks on a chip [53].

The turn over time and cost to produce ASICs can become extremely large, as a great deal of design and manufacturing work is required. Any mistakes in the design will result in failure to carry out the intended task. As ASICs are solely designed for a specific task, they are not reprogrammable, but still carry a number of benefits. ASICs are able to handle more complex code, have faster computational times and are resistant to SEEs [54, 55]. The permanent and non-volatile nature, together with reliability and high computational speeds, make ASICs a very popular solution to almost any micro processing problem. Because of this, ASICs can be found in almost all electronic circuits.

2.11 Field Programmable Gate Arrays

A field programmable gate array can be described as a pre-packaged semiconductor device which is based around a matrix of configurable logic blocks, connected by programmable interconnects [56]. FPGAs are able to be electrically programmed and reprogrammed into almost any type of digital circuit by the user after manufacturing to suit the application at hand. FPGAs differ from application specific integrated circuits (ASICs) as ASICs are designed by the customer and manufactured with predesigned circuitry to serve a predetermined purpose. FPGAs, unlike ASICs are available off the shelf with a short lead time, are less expensive and able to be reprogrammed in-field to account for design errors or adapt to new requirements. This in field reprogram ability feature of the FPGA makes it ideal for space based applications where access to the device is not available and constant adjustments and updates are required to be made to the system. It is possible to partially reconfigure a FPGA while the rest of the device is in operation, allowing for additional flexibility.

This flexibility of FPGAs results in a number of disadvantages. These include having a 20 to 35 times larger physical size, 3 to 4 times slower operating frequencies and up to 10 times increased power consumption when compared to ASICs [57]. These disadvantages are due to the reprogram ability of the FPGA, which results in almost 90 percent of the total area of the FPGA comprising of programmable routing interconnects [57].

Despite these disadvantages, FPGAs hold the greater advantages in digital system designs because of its low volume cost, high flexibility and fast turnaround times, resulting in FPGAs being more suitable for space applications than ASICs. However, implemented in a space environment, the FPGAs greatest disadvantage becomes its susceptibility to total ionizing dose and single event upset effects [7]. FPGAs perform exceptionally well in any situation where any design changes could be expected, a cheaper and small number of specialized products are required and where prototyping or experimental tests are to be conducted.

Figure 16 illustrates a generalised example of an FPGA, showing the configurable logic blocks (CLBs) arranged in a two dimensional grid, surrounded by routing, which allows the CLBs to be programmably interconnected [57]. The "programmable" aspect of the FPGA refers to the ability to program and reprogram the chip after the silicone fabrication process has been completed. An

underlying programming technology which allows changes in the behaviour of a pre-fabricated chip after it has been fabricated allows for this reconfigurable/programmable feature [57]. I/O blocks which are also connected to the programmable routing interconnects can be seen on the outside of the grid.

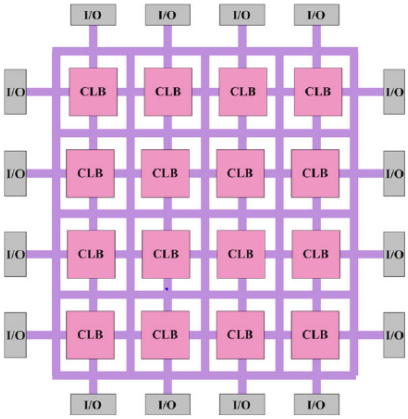

Figure 16: FPGA architecture

2.11.1 Architecture

2.11.1.1 SRAM based

Logic cell configuration data is stored in static memory. Due to this volatile memory, the SRAM FPGA is not able to store data while no power is connected and requires reprogramming upon start up. SRAM FPGAs can be programmed in either master mode, where the FPGA configuration data is read from an external source, or in slave mode, where the FPGA is configured by an external master device such as a JTAG interface [58]. Additionally, SRAM based FPGAs with internal flash memory are also available. These FPGAs contain internal based flash memory, making the use of external non-volatile memory unnecessary. The in-chip flash memory can be interfaced with via SPI and can be capable of storing up to two configuration bitstreams [58].

2.11.1.2 Flash based

Flash based FPGAs have non-volatile flash memory built into the FPGA as oppose to SRAM and utilize the flash memory as a primary resource for the configuration storage of the device. Flash based memory stores information in an array of floating gate transistors which, when in the presence of an

applied voltage, is able to store a bit value. Floating gate transistors differ from MOSFETs by having an additional electrode, known as the floating gate electrode, between the control gate and the semiconductor material. The floating gate transistor acts in the same manner as a normal MOSFET when no charge is applied to the floating gate electrode, such that when a positive charge is applied to the control gate, a channel carrying current between the source and drain is created [59, 60].

Applying a negative charge to the floating gate prevents the channel from allowing current to flow between the source and drain, thus reducing the effect of the control gate. The threshold voltage is adjusted to be more positive or negative by either applying or not applying charge to the floating gate [59]. Electrons are able to pass through the insulation layer and remain in the floating gate allowing the transistor to operate as a normal MOSFET by applying a large enough current. The floating gate retains the charge and thus retains the high state which was applied when the power is disconnected [60, 25]. Figure 17 illustrates the cross section of a floating gate transistor.

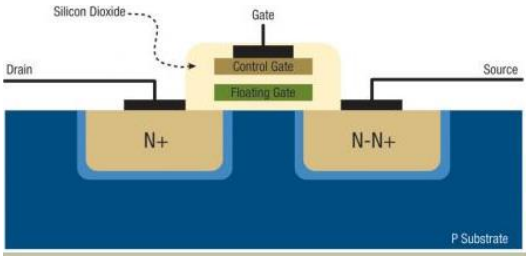

Figure 17: Floating gate flash structure [25]

Flash and SRAM FPGAs differ by the structure of the logic modules and the method in which the logic modules are interconnected. The effects of radiation in different FPGA based technologies will mainly be determined by the type of transistor implemented. SRAM FPGAs, unlike Flash based FPGAs, have configuration memories which consist of SRAM memory cells as well as logic modules which are very susceptible to TID and SEEs. The configuration memory of flash based FPGAs consisting of flash transistors, are not sensitive to SEEs and thus the most susceptible aspect of Flash based FPGAs will be the logic and memory modules. The floating gate transistors of flashed based FPGAs will be sensitive to TID effects [7, 11, 25, 59]

2.12 Single Event Effects

The interaction of single high energy particles with electronic devices may result in ionization. The resulting deposited charge may lead to a number of effects which are broadly classified as non-

destructive (soft errors) or destructive (hard errors). Soft errors usually manifest as bit flips in memory cells or transient pulses in support circuitry or logic. Hard errors usually result in the temporary malfunctioning of a device, requiring the device to be reset, or as a permanent failure of the device [61]. Lists of classifications of SEE's are [34, 62, 63, 64]:

Soft errors

- Single Event Transient (SET) – Impacting particle which induce asynchronous voltage pulses in the combinational circuitry of the FPGA. When this induced voltage exceeds the switching threshold with a large enough pulse width, the resulting signal propagating through the circuit can either be filtered out or be latched into memory elements. The effects are non-destructive in nature.
- Single Event Functional Interrupt (SEFI) – SEU altering the control circuit of the FPGA resulting in the change of the device state.
- Single Event Upset (SEU) – change of logic state of a memory cell due to the latching of a SET into a memory element or when a volatile memory element is struck by a high energy particle.
- Multiple Bit Upset (MBU) – change of logic state of multiple memory cells (multiple SEUs at the same instance)

Hard Errors

- Single Event Latchup (SEL) – SELs result in higher operating current, as a result of the ionizing track in parasitic pnpn turning on both internal transistors, exceeding the device specifications. Threshold for latchup decreases at high temperatures, both high and low current SELs can occur.
- Single Event Gate Rupture (SEGR) and Burnout (SEB) – permanent damaging of power transistor or any other high voltage devices

2.12.1 Single Event Latchup

Single event latchups (SELs) result in a high supply currents well above the maximum rated values and have the potential to result in complete failure of the implemented space system, and thus

considered to be a critical effect. Because of this, components sensitive to SEL are not generally utilized in space based applications. SEL are triggered by heavy ions, protons and neutrons and are heavily dependent on the temperature of the FPGA. It has been found that at higher temperatures the latchup cross section increases together with the decrease of the threshold for latchup. In modern devices, both high current and low current SELs are able to occur, making the characterization of SELs a challenging obstacle in larger and more complex circuits [34, 62, 63, 64]. Figure 18 demonstrates the temperature dependence of the latchup cross section versus the LET.

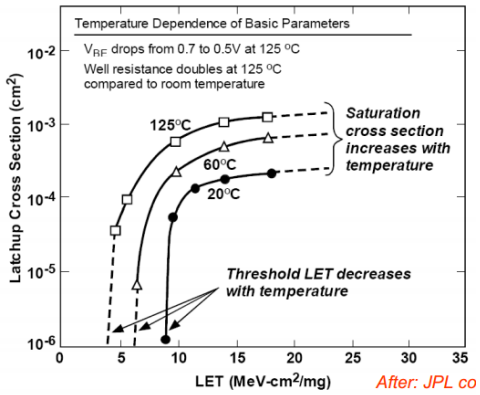

Figure 18: Temperature dependence of latchup cross section vs. LET [62]

2.12.2 Single Event Functional Interrupt

Single event functional interrupts (SEFIs) casue corruption of the data path, resulting in a temporary filure of the device's functionality. This is restored by resetting the device, or after a power cycle of the device has completed. SEFIs commonly arise from SEUs which have occured in the control register of the device [62].

2.12.3 Single Event Transient

The effects of single event transients (SETs) can result in transients on either external signals, such as comparators, or internal signals in the CMOS resulting in errors in the outputted data. SETs are able to result in errors in subsequent circuits if the transients are not filtered in a number of stages in the circuit. SETs may result in SEUs if they are latched into memory elements [62]. Figure 19 illustrate the pulse width and pulse amplitude of a SET.

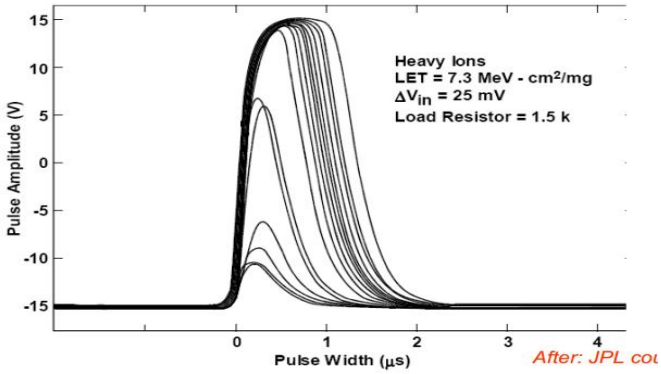

Figure 19: SET pulse width and amplitude [62]

2.12.4 Single Event Upsets

Single event upsets (SEUs) are caused by ionizing due to the impact of heavy ions or high energy particles at the depletion region of an N-P junction transistor. Small charges in this region are collected, which in turn creates voltage and current transients [63]. The Linear Energy Transfer (LET) which results from the high energy particle impacts are possible to increase to above the critical charge (Q_{crit}) required to cause the junction to change state causing a bit flip of the memory element, resulting in an error [63]. The error will propagate though the circuitry and later be shifted out. The amount of energy transfer required to cause a bit flip in a memory element is referred to as $LET_{THRESHOLD}$ measured in units of MeV-cm^2/mg. Another important measure of a device's sensitivity to radiation exposure is the cross section of the device. The cross section of the device can be calculated by Equation 1 [63]. The cross section gives an indication of the probability that a SEU will occur in the device [62].

Figure 20 illustrates the relationship between a number of particle energies and the resulting SEE cross section.

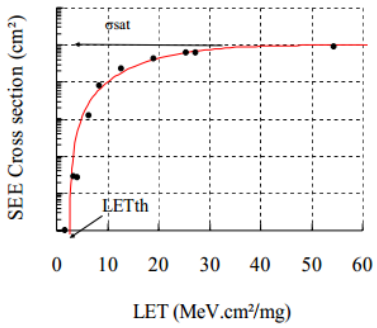

Figure 20: Cross section vs. LET

The cross section of the SEE is a direct function of the LET.

$$A = \frac{Numberof Errors}{Fluence \times \cos(\theta)}$$

Equation 6

Where the fluence is calculated by the given parameters of testing and theta is the angle of incidence of the device to the beam. Figure 21 demonstrates the effects of a high energy neutron impacting with a MOS transistor [63].

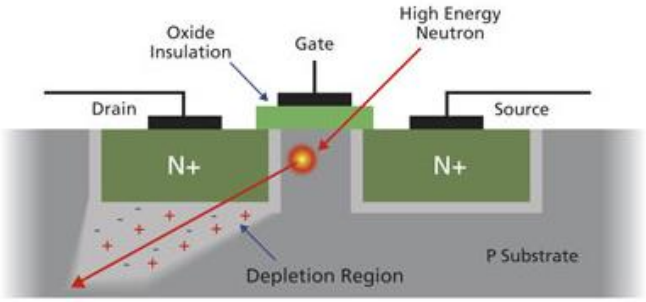

Figure 21: High energy particle collision with MOS

SEUs generally only change the state of storage elements, namely the memory cells and registers. SEU effects are non-destructive in nature and result in errors propagating through the circuitry [63]. Any device with an implemented circuit with a LET threshold in excess of 120MeV-cm^2/mg is considered to be immune to SEUs [63].

2.13 Total Ionizing Dose

An accumulated dose of radiation can induce a degradation of sensitive electrical components which can lead to the malfunctioning or failure of the device. This effect is known as total ionizing dose (TID) [65, 66]. TID effects can be vary depending on the device and the amount of exposure, but can include [11, 67, 68, 69]

- Increased supply current to the device resulting in failure of the device (destructive)
- Result in incorrect outputs of the device (bit flips similar to that of SEU effects)
- Increased propagation (computational) time through the circuitry
- Have annealing effects which remain in the device

Ionizing effects in FPGAs occur due to the high and low energy charged particles striking the crystal lattice. This interaction results in the addition or subtraction of electrons from a neutral or partially ionized atom. The altering of the number of electrons leads to the bond between atoms breaking down, in turn changing the chemical composition of the material [11, 8].

In the MOS structure, the accumulation of trapped charges within the silicone dioxide insulating layer escapes through tunnelling effects. This occurs when ions escape the insulation layer, producing a very small current.

In CMOS structures, the TID exposure causes electron-hole pairs in the insulation layer, inducing a very small current when these pairs recombine [11, 8].

TID effects in MOS devices are dependent on the following factors [11]:

- Total dose
- Dose rate
- Method of construction
- Operating and post operating temperatures
- Annealing effects
- Source of radiation
- Physical device properties
- Device dielectric

Figure 22 illustrates the trapped charges are responsible for the threshold voltage shifts and leakage current [11].

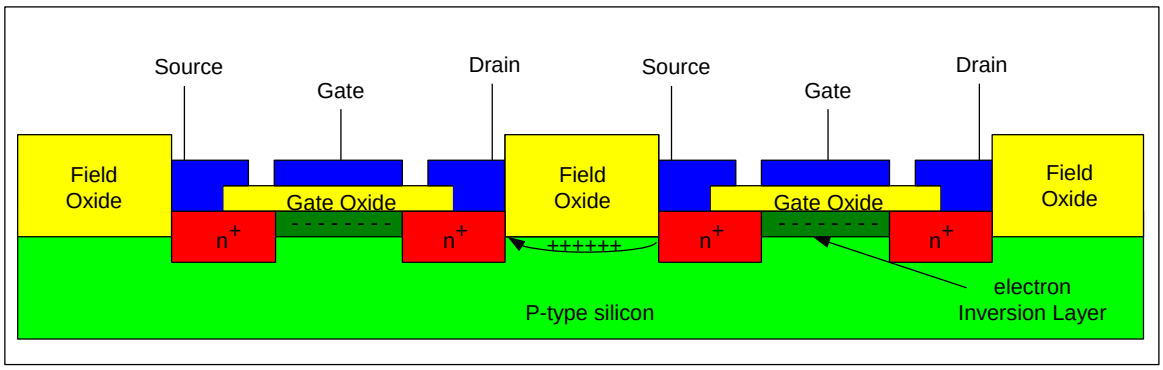

Figure 22: TID

2.14 SRAM vs. FLASH testing

Only FLASH based FPGAs will be used in the experiments due to the non-volatile memory and immunity to SEL. The SRAM and flash architectures can be distinguished by the exact structure of the logic modules, as well as the interconnection of these logic modules.

2.14.1 Effects on SRAM cells:

If an ion with sufficient energy strikes near to any of the four transistors of which the cross-coupled inverter of a typical SRAM is constructed, a bit flip of the bit values currently stored can be induced. The critical energy to cause a bit flip in the SRAM cell is also dependant on the switching frequency of the cell due to the active feedback of the cross-coupled transistors [63]. The critical energy is also decreased due to the decrease of process node sizes. It is estimated that the critical energy has decreased by an order of 30% when comparing a 65nm to a 45nm process [63].

2.14.2 Effects on FLASH cells:

The critical energy for flash cells are notably larger compared to SRAM cells. However, an ion strike near to or in the depletion region of the transistor will result in a charge being deposited in the area.

The configuration memory flash cells are constructed more robustly than the flash cells used in bulk memory and results in a much higher critical energy for these cells. The charge created due to an ion strike with a linear energy transfer of 37 MeV-cm^2/mg is less than 1% of the critical energy of a programmed floating gate configuration switch (250nm PROASIC) [63]. The non-volatile memory of Microsemi's 130nm Flash architecture has a LET threshold value of 60MeV-CM^2/mg and a configuration memory which is 7.6 times larger and has an estimated LET threshold in excess of 120MeV-cm^2/mg, ensuring immunity [63].

3 Research Rationale

3.1 Research Motivation

The research project is motivated by the single event upset and total ionizing dose effects, caused by space radiation in commercial off the shelf (COTS) flash based FPGAs. FPGAs are able to be utilized on-board satellites, as well as exploration platforms in a number of applications, including, but not limited to: image and video capturing and transmission, data acquisition from sensors, data transmission and receiving, motor control and propulsion control. Only flash based FPGAs were considered during this research as these devices are able to retain the data programmed in the configuration memory after power has been disconnected from the device. This allows the device to operate without requiring reprogramming after a power failure, such as when the solar panels are not able to charge the on-board batteries of the system. The FPGA is also able to be initially programmed before launch and will not require reprogramming once it is in the area of operation. The most important benefit of flash based FPGAs as oppose to the SRAM counterparts is the radiation hardened configuration memory which is able to withstand radiation energies in excess of 120 MeV. This advantage makes the implementation of flash based FPGAs the ideal choice.

The low cost, small size, low power consumption, large computing power and versatility of the FPGA allow any number of these devices to be implemented into the designed system to operate as the main controller of the platform. To ensure continuous operation of space based systems, such as satellites, which make use of commercially available FPGAs, it is of great importance to experimentally determine the performance characteristics of the FPGA during irradiation. Once it is experimentally determined how the FPGA will operate when exposed to a radiation source of known energies and dose rate, the performance and life span of the device can be estimated for a specified space radiation environment. Both the SEU and TID characteristics will not only be useful for space based applications, but for any application where the FPGA must operate in a radioactive or nuclear environment.

3.2 Real World Radiation Effects

The effects radiation has on electronics both in space, high altitudes and on ground level is often underestimated or not completely understood by designers. A number of examples of critical errors due to SEEs will be mentioned below [26, 34, 70, 71, 72, 72, 73, 74].

- 1992 PERFORM system utilized by aircrafts to perform take-off manoeuvres required replacing after SEUs occurred in the SRAMs [34, 70].
- 1998 Study found that each day 1 out of 10 000 SRAMs in pacemakers had bitflips. This number would increase by 300 times for transoceanic flights [34, 71].
- 2000 Sun Unix server system crashed in several locations in the USA due to SEUs in cache memory [72].
- 2005 ASC Q Cluster supercomputer showed 7170 errors in the 81 GB memory cache after 102 days. 243 of these led to a crash of the programs or operating system.[72]
- The CREME program detected an upset rate of between 0.00012/hour to 0.00084/hour for several single chip microprocessors at a 784km 98 degree orbit with a 1g/cm^{2}aluminium shielding during a solar minimum. During a solar maximum, the error rate increased to between 3 and 18 upsets per hour.
- 1998 the TOMS-EP experienced radio interference and SEUs which interfered with the Earth sensor, resulting in being forced into safe-mode [73].
- 2003 the small mission for advanced research and technology (SMART) experienced high levels of radiation and during exceptionally large solar flares, the star tracker malfunctioned resulting in difficulties to maintain orientation. SEUs in the opto-coupler in the power processing unit resulted in eight uncommented shutdowns of the engines. [73]
- The Mars Odyssey experienced failure in its Marie system as a result of SEUs in the instrument's memory. The instrument ceased scientific operations and proceeded to initiate an error detection and correction procedure, after which the instrument lost communication with the spacecraft's control computer [23, 73]

3.3 Current Shortcomings

There is currently minimal amount of research being conducted in the field of radiation effects on electronics. Radiation effects such as TID and SEUs are not always considered when designing the electrical systems for space based platforms and vehicles. FPGAs are a common type of controller implemented in satellites and other platforms operating in space. Failure of the controller could thus lead to possible failure of subsystems or even the project.

The maximum amount of absorbed radiation dose as well as the magnitude of the energy of excited particles strikes in the FPGA, resulting in a loss of device functionality, has not been experimentally determined for all FPGAs. The device characteristics are not known to the extent where a designer can accurately predict how the FPGA will function after certain periods of time during radiation exposure of a specific level.

The effects of long term exposure to gamma rays can lead to the total ionizing dose effects in FPGAs, one of which includes an increased supply current draw of the device. This could possibly lead to the failure of the device, or errors in the outputs of the device. Single event effects induced in FPGAs as a result of high energy particles, for the purposes of this research are limited to soft errors due to a single or multiple bit upsets in the FPGA.

TID and SEU induced errors are able to be reduced by various mitigation schemes including double modular redundancy (DMR), triple modular redundancy (TMR) and Mitigation by means of Reconfigurable FPGA computing developed in [7]. These schemes aim to reduce and possibly prevent output errors of the FPGA from occurring. Although the mitigation schemes are aimed at preventing output errors, they are only able to prevent single bit upsets and in some cases, even multiple bit upsets effectively. They are however not able to eliminate all occurring errors and as a result, errors still propagate through the circuitry. Mitigation schemes aimed at protecting the device do not prevent the device from failing after a certain period of time as a result of TID effects or other destructive SEEs.

Another factor to take into account when implementing these mitigation schemes is the increase of the amount of recourses required to implement these mitigation methods. A relationship between the effectiveness of the mitigation and the amount of additional overhead recourses required should

be taken into account when considering an integrated design. It is important to determine the TID and SEU characteristics of a FPGA with and without mitigation schemes. It is necessary to devise an experiment which will realistically characterize the behaviours and performance of a number of given FPGAs with various parameters, such as aluminium protection, code complexity, mitigation schemes and other relevant parameters.

Several radiation hardened FPGA devices can currently be found in the market, but at a much higher cost. These radiation hardened FPGAs are priced anywhere between R 50000.00 to R600 000.00, as opposed to commercial of the shelf (COTs) products which can be purchased from less than R300.00 [104]. The focus of this paper is thus to determine the viability of implementing these COTs FPGAs in the space environment and how to improve the performance of these FPGAs by means of implementing mitigation schemes.

3.4 Commercial off the Shelf Components

Commercial off the shelf (COTS) components are readily available and are generally cost effective. The varieties of components available make the use of COTS FPGAs at attractive choice to be implemented in space applications. FPGA variations range from different architecture technologies, physical size, number of input and output pins, number of logic elements available and the cost of the device. As a result, the designer is able to select an appropriate FPGA for the task and able to receive and replace this device in a short amount of time, at a low cost.

It is important to be able to determine the SEE and TID characteristics of these COTS FPGAs such that a device can confidently be chosen for a specific task under per determined conditions and be expected to have a known operational lifespan. COTS electronics are generally able to withstand 3-10 krad (si) of total dose without experiencing any performance degradation. These electronic components are usually able to continue functioning with amounts of degradation in the ranges of 10 to 30 krad (Si) [7]. COTS FPGAs operating in a space environment will be subjected to high energy particles with energies in the MeV to GeV ranges together with high dose rates.

It is important to determine the SEU cross section of the required circuits and TID characteristics of these devices in order to estimate an error rate and life span. Furthermore a comparison between

the radiation hardened devices and COTS FPGAs can be made if desired, both with and without mitigation. A comparison between the COTS and radiation hardened FPGAs will provide an indication of the benefit of implementing these hardened devices.

3.5 Radiation Hardened Devices

Radiation hardening is a process of design considerations and techniques made to reduce the effects of radiation on the device. Methods of hardening may include applying physical protection to the circuit or implementing circuit redundancy [8].

3.5.1 Physical hardening

To create a hardened IC, insulating silicone dioxide or sapphire substrates are used as oppose to the standard silicon wafer. This process increases the radiation tolerance of ICs by several factors. An alternative method of radiation hardening involves coating the IC in depleted boron, reducing the effects of radiation on the internal components. Constructing the substrate with high band gap material results in more energy being required to move electrons from the valance band to the conduction band. When a high energy particle collides with this substrate the induced conducting path can be prevented [8].

An example of a radiation hardened FPGA is the Xilinx Q-PRoVirtex II device. The Q-Pro is able to operate up to a total absorbed dose of 1.2MRad. The following results were recorded for the device by [75]

- At a TID of 300 kRad, the device no longer meets all timing specifications. While the device will still continue to operate properly, it may not be able to handle higher clock speeds (on the order of 250 MHz or more).
- At a TID of 400 kRad, the SEU cross-section of the device starts to noticeably rise.
- At a TID of 800 kRad, the ICC leakage current begins to increase.
- At a TID of 1.2 MRad, the ICC leakage current is now double the manufacturer's nominal specified value.

3.5.2 Mitigation Schemes

3.5.2.1 Single Event Upset

A number of well-known mitigation schemes have been designed to mitigate the effects of SEEs, mainly focused on SEUs. These mitigation schemes are aimed at reducing the rate of bit flips in data streams. Several mitigation schemes are well known and have been tested in experiments and have been implemented in real world circuits.

The most common mitigation schemes are the Dual Modular Redundancy (DMR) and Triple Modular Redundancy (TMR). Both of these mitigation schemes are readily available to use in a design without limitations. A number of alternative methods of mitigation exist, such as the AND-OR multiplexer SET filtering circuit designed [15].

Dual Modular Redundancy

DMR is implemented into the circuitry by duplicating the components of a system. The duplicated components operate in parallel and provide redundancy to allow for comparisons between the two outputs. In FPGAs, DMR can be applied locally to only the memory elements of the circuit, or globally to each component in the circuit. DMR is not an effective solution to SEUs in a radiation environment and requires at least double the amount of power and components to implement.

Triple Modular Redundancy

Triple modular redundancy is possibly the most commonly known and used mitigation method. TMR requires the circuitry to be tripled, creating three outputs which are then entered into a majority voting circuit. This outputs only one signal, which is the majority or the three input signals. Any errors occurring in one of the three circuits will, as a result, be eliminated. The drawback of TMR is the requirement of at least three times the power and area as the circuit must be tripled. The additional TMR overhead could result in an even higher amount [15]. Another disadvantage of TMR is not having the ability to account for multiple bit upsets (MBUs). MBUs occur when a bit flip occurs in two of the redundancy circuits, resulting in the correct circuit being outvoted by the two incorrect ones. TMR protects the sequential components of the circuit from single bit flips. Local TMR will not provide immunity against errors when the SET occurs in the unprotected combination logic, when SETs occur in the global clock, enable or clear signals. In addition to this, a strike in the voter circuits

will also result in a SEU [15]. A high level of immunity to all SEUs can be ensured at the cost of higher power requirements and area usage, by implementing full global TMR protection, tripling all sequential, user logic, global signals and voting circuits.

Figure 23 illustrates an example of local Triple Module Redundancy (TMR) [68] and Figure 24 illustrates an example of global TMR.

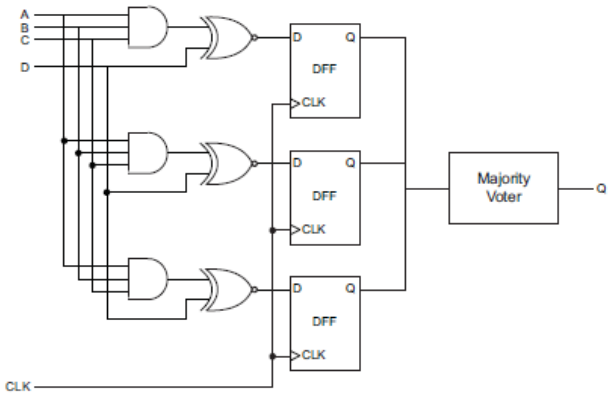

Figure 23: TMR Mitigation

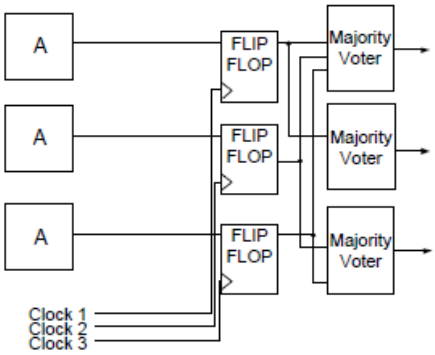

Figure 24: Full global TMR

SET Suppressor

The SET filtering circuit consists of a AND - OR gate circuits in parallel, which is connected to the inputs of a two input multiplexer. This filtering circuit mitigates SETs, preventing any memory elements from latching these SETs and resulting in SEUs [15]. Simulated results indicate that the SET filter method provides SET immunity with an area saving of 11.6% to 62.2%, compared to TMR when the SET delay element filter method was implemented [15].

Figure 25 illustrates the two input AND-OR multiplexer SET filter circuit. Figure 26 demonstrates the one input delay element AND-OR multiplexer SET filter circuit [15].

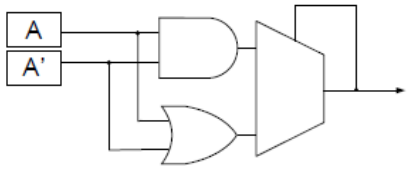

Figure 25: DMR SET filter [15]

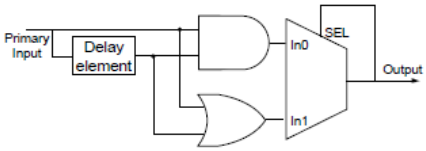

Figure 26: Delay element SET filter [15]

An advanced SET filter not only provides protection for the occurrence of SEUs, but additionally provides MBU protection. This development in mitigation ensures that the circuitry is protected against MBUs which, in other mitigation schemes, would result in an output error.

3.5.2.2 Total Ionizing Dose

Mitigation for total ionizing dose focuses on prolonging the operational life of the FPGA, as oppose to reducing the number of errors. The switched modular redundancy (SMR) method seen in [45, 76] significantly prolongs the life of MOS devices in a space radiation environment by "adding redundancy and applying a resting policy" [11, 45, 47]. This amount, which the threshold voltage shifts in a MOS device while irradiated, is influenced by the bias voltage applied to the gate during and after irradiation [11, 76]. While the gate of the MOS device is unbiased, the threshold voltage shift will be smaller. As a result, the maximum dosage tolerated by a device is much higher for during gate bias cycling than constantly applying a bias during irradiation [11, 76]. Figure 27 [11] demonstrated the performance comparison between an unmitigated and mitigated FPGA during irradiation.

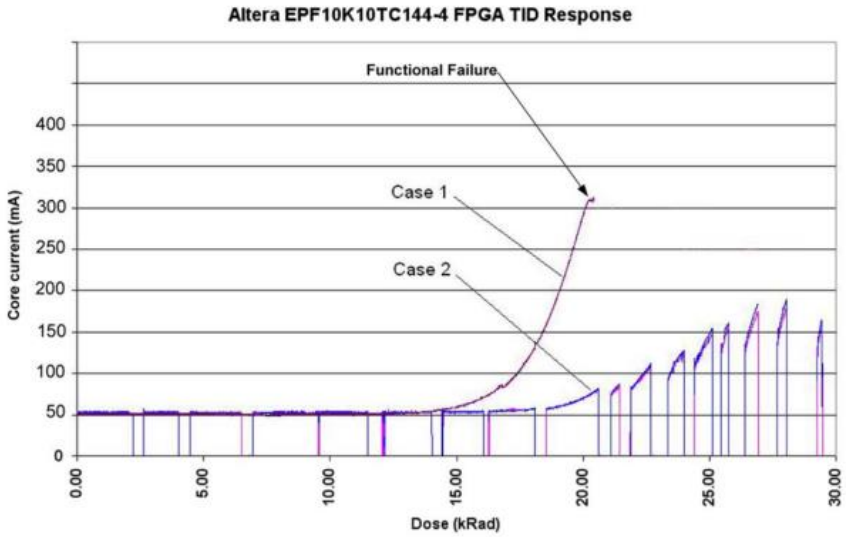

Figure 27: TID mitigation comparison between unmitigated (Case 1) and mitigated (case 2) methods for the Altera SRAM FPGA [11]

4 Research Set-up and Procedure

4.1 Primary Objectives

The primary objectives of the research includes the design and implementation of a mechanical control testing platform, which allows for the experimental testing of electronic components in the existing vacuum chamber at the iThemba LABS cyclotron. In addition to this, it was critical to experimentally determine the SEU and TID characteristics of the MicroSemi ProASIC3 A3P 1000 flash based FPGA.

The experimental tests required to determine the SEU and TID characteristics of ProASIC3 flash FPGA were performed separately in two separate testing facilities. Each facility provides the appropriate required radiation source. The FPGA was programmed with a number of specific circuits which are commonly used in a space environment. The FPGA was then irradiated while powered on and operating.

The SEU characteristics were determined by irradiating the A3P1000 FPGA with a proton "beam" with an energy of 66MeV at various beam currents. The outputs of various circuit implementations were monitored to detect the amount of errors occurring over a known time period, given the proton beam energy and current. The number of errors captured was used in the Bendel 1 parameter equation to determine the SEU cross section per proton\ cm^2 per bit. A Bendel graph was then able to be plotted to indicate the estimated cross section for any of the implemented circuits at various proton energy levels. The viability of using COTs components with and without mitigation schemes rather than radiation hardened components for space based applications was verified during these tests.

For TID testing, the output errors were monitored, as well as the supply voltages and current to the FPGA. This provided an indication of the particle energy or radiation dose which the FPGA is subjected to. This allowed accurate predictions of the expected error rate due to absorbed dose, and operating characteristics for TID, such as the increase or decrease of supply current and relevant voltages.

A mechanical platform was designed and implemented which allows a number of DUTs with a physical size of up to 100mm by 100mm to be mounted simultaneously. Each DUT is able to be

individually selected such that the specified DUT is in the path of the proton beam. Furthermore, any specified section of the DUT board is able to be irradiated if required as well as vary the angle of inclination between the beam and board. The testing platform implemented will be utilized by the Nelson Mandela Metropolitan University (NMMU) and outside organizations for the testing of their specific electrical and electronic components. This will promote the increase of radiation testing performed on devices to be utilized in space applications.

An electrical system was implemented to allow for communication between the computer running the LabVIEW software and the control and monitoring FPGA board, and the mechanical system's motors. Communication between the control FPGA and the motors within the vacuum chamber was achieved with the FGG.2B.319 and FGJ.2B.319 connectors which are able to create a link between the contents of the vacuum chamber and the outside world while retaining a perfect vacuum. All variables were continuously monitored and recorded by the computer running LabVIEW software.

4.2 ProASIC3 A3P 1000 PQ208 Architecture

The ProASIC3 FPGA was chosen as the device to be tested. This flash based FPGA was chosen above the SRAM types as the ProASIC3 requires no boot PROM [103]. This prevents configuration errors from occurring during boot up. The ProASIC3 has a dedicated non-volatile 1024 bit FlashROM memory. The non-volatile nature of the memory prevents Single Event Latchups (SEL) from occurring during tests which could result in the failure of the test. Read and write communications are performed using the JTAG interface. The FlashROM memory is arranged into 8X128 bits organized as 8 pages of 16 bytes [103]. Figure 28 illustrates the layout of the ProASIC3 architecture [103].

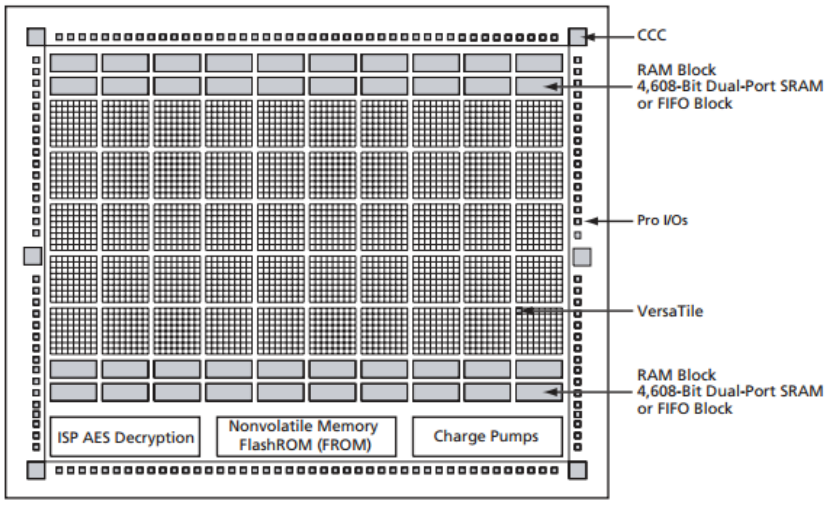

Figure 28: ProASIC3E architecture

The ProASIC3 A3P1000's reprogrammable flash technology is based on a 130nm, 7 layer metal flash based CMOS with a 1 million gate capacity. The A3P1000 operates with a core supply voltage of 1.5V at an average current of 8mA, functions with a wide range of I/O voltages (1.5V, 1.8V, 2.5V and 3.3V mixed voltage operation) and allows 300 user IOs [77]. The high flexibility, low power requirements and high level of computational power makes the A3P1000 a suitable controller to be implemented in a space application. The device will be able to connect to a large number of secondary or additional primary components and have access to ample processing recourses. The ProASIC3 datasheet can be found on the attached disk.

4.3 Testing Circuits

Implemented in the test FPGA were a number of motor control, communication methods and mitigation technique circuits which were tested at the same time. This is done as only one DUT and two sessions of SEU and one session of TID testing was available to obtain experimental results. All of the test FPGA and control FPGA VHDL code can be found on the attached disk.

Each of the communication and motor control circuits implemented for testing were first coded in VHDL to function with the required sensor, RF transmitter/ receiver or motor. Each circuit functioned correctly with an input or output device described in the sections below. This ensured that the testing circuits were actual circuits which had real world relevance for space applications.

Figure 29 illustrates a number of the sensors and one of the motors used to validate the circuit implementations. All of the device datasheets can be found on the attached disk.

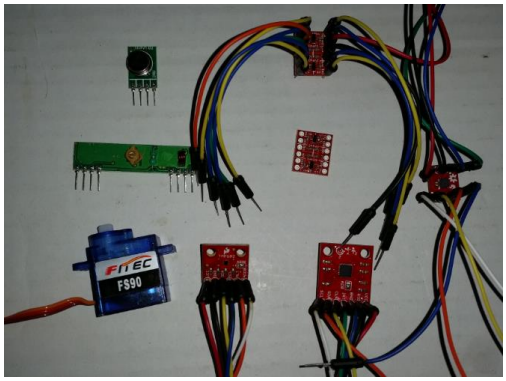

Figure 29: A number of the sensors and motors tested with the circuits

4.3.1 Single Event Upsets

During the testing of the implemented circuits, continuous monitoring for the occurrence of SEUs was performed. The single event transients which resulted in single event upsets originated from a number of possible areas in the circuit. For the mitigation testing conducted, the SETs were able to have originated from the sequential or memory sections of the circuit. The SETs may have been induced in the user logic, clock and clear signals or in the memory elements (latch or flip-flop) and majority voters. Additional SEUs were able to have occurred in the IO banks themselves, resulting in output errors, regardless of the mitigation applied to the circuitry inside the FPGA. For the control circuits tested, the SETs were able to originate in either the combination or sequential parts of the circuit in addition to the IO banks.

4.3.2 Circuit Comparing and Duplication

For the mitigation implementations, each circuit output should be that of the input. A logic high input should result in a logic high output. Each mitigation circuit with a single output was compared to the input pattern applied to the circuit. An SEU was determined to have occurred once the output of the circuit did not match the state that was applied to the input. For multiple output circuits, the outputs were ANDed and the result of the AND was compared to the signal applied to the input in the same manner.

For the communication and motor control circuits, each circuit was duplicated a calculated number of times in parallel to one another. The number of duplications was determined by the percentage of the chip which each circuit's duplications was required to fill. The parallel duplication ensured that each implemented circuit type occupied the same amount of the chip resources.

Each of the parallel duplicated circuits of a specific type of circuit, such as for SPI, was divided into two groups. All of the circuits in each group were ANDed and the resulting output of the two groups was a representation of all of the parallel circuits. A single upset in any of the circuits in either of the two groups would result in an error in the output of the combined circuits. The two resulting outputs were then compared and a SEU was detected when the outputs did not match.

Initially, the outputs of each of the parallel circuits did not match the others identically due to the Nano second clock delays in the FPGA due to physical mapping of the circuits in the device. This resulted in a number of the signals being out of sync with one another by a few nano seconds. The resulting ANDing of the outputs of the parallel circuits always outputted a logic zero, indicating an error. The problem was overcome using the global clock buffer function built into the Libero software. This buffer applied the clock signal to each of the duplicated circuits simultaneously.

Duplication of the both the mitigation and control circuits was achieved by coding a program in C#. This program created a VHDL file for each test circuit containing a number of duplicated circuits indicated by the user. The VHDL file produced by the C# program made the duplication of any test circuit possible for any number of desired duplications. The C# duplication code can be found on the attached disk.

4.3.3 Standard mitigation techniques

A number of memory elements, specifically latches, were connected in series and repeated a set number of times as a benchmark. This captured any single event upsets occurring in the circuit. This circuit provided an indication of the amount of errors occurring for the cross-section of the memory elements of the FPGA. Latches were implemented as oppose to flip-flops, as each SET will be latched into a memory element, ensuring that most of the occurring errors will be counted. Various mitigation techniques were implemented together with the latches to determine the effectiveness of implementing each mitigation technique. The results provided an accurate indication of the

effectiveness of the technique and the resulting number of errors of the memory elements implemented.

The implementations can be seen below:

4.3.3.1 Implementation 1

Implementation 1 consists of a set number of memory elements, namely latches, connected in series with the output of the last connected to the input of the next. A single clock and clear line is connected to each of the latches. Any SETs occurring will be latched and result in a SEU. This implementation tested the number of errors occurring for a set number of memory elements, allowing for a baseline error rate and SEU cross section from which to compare the mitigation techniques.

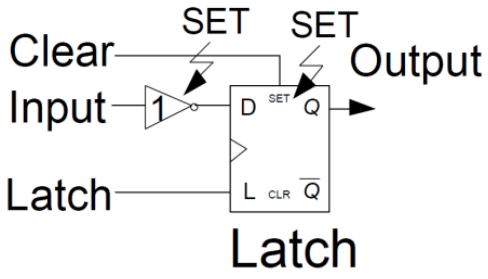

Figure 30: Implementation 1

4.3.3.2 Implementation 2

Implementation 2 consists of a series of memory elements protected with local TMR and a majority gate. This implementation tested the effectiveness of preventing SEUs in memory elements using this local TMR mitigation method. No protection is provided for the input, clock and clear signals.

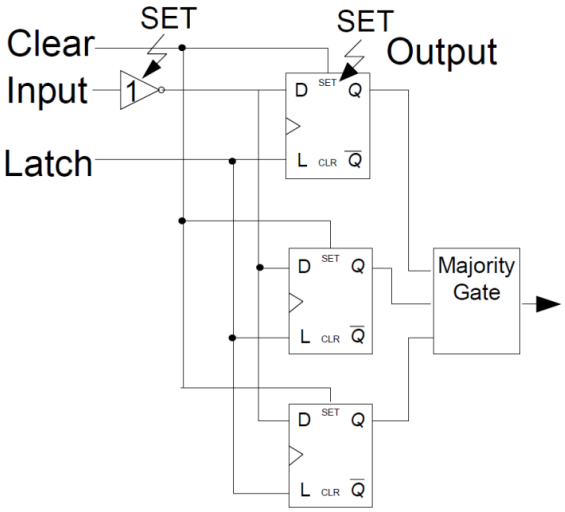

Figure 31: Implementation 2

4.3.3.3 Implementation 3

Implementation 3 incorporates DMR protection of the user logic with a single SET filter before the latches. The latches are protected by local TMR and a single majority gate. No protection is provided for the input, clock and clear signals.

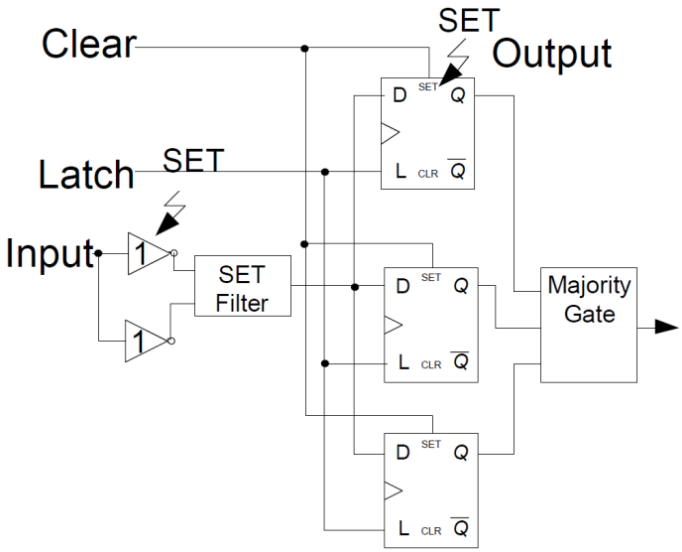

Figure 32: Implementation 3

4.3.3.4 Implementation 4

Implementation 4 provides DMR protection for the user logic and is followed by TMR SET filters, one for each input to the latches. The latches are protected with local TMR and two majority gates which input to the next set of DMR user logic. No protection is provided for the clock and clear signals.

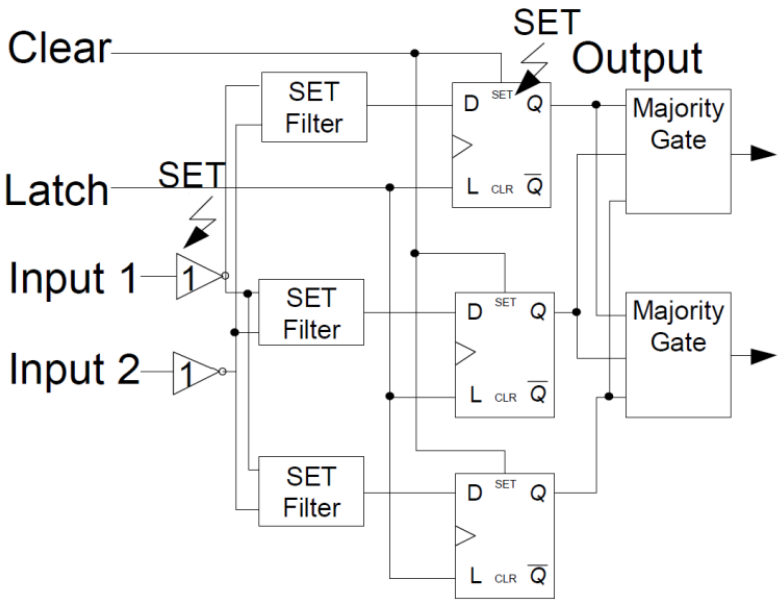

Figure 33: Implementation 4

4.3.3.5 Implementation 5

Implementation 5 provides DMR protection for the user logic and followed by three SET filters, one for each input to the latches. The latches are protected with local TMR and two majority gates which input to the next set of DMR user logic. Implementation 5 is identical to 4, except that the clock and clear signals are tripled for protection.

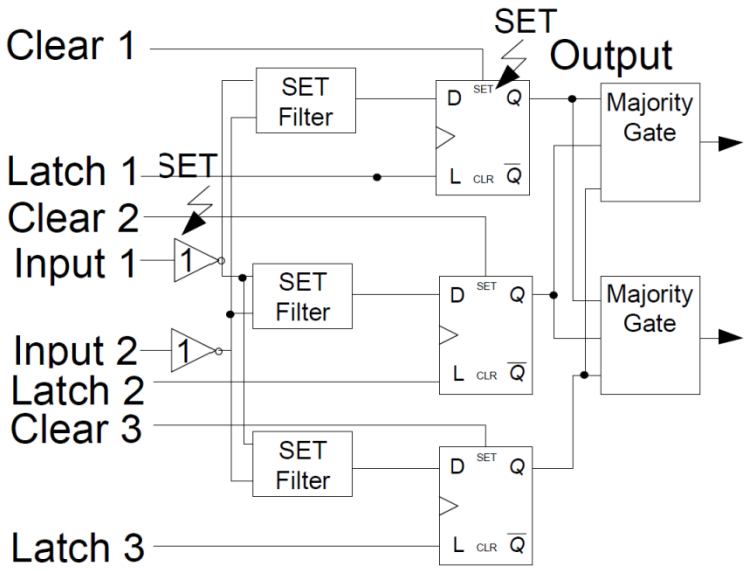

Figure 34: Implementation 5

4.3.3.6 Implementation 6

Implementation 6 provides full TMR protection of the user logic as well as TMR for the latches and three majority gates. TMR protection is provided for the clock and clear signals.

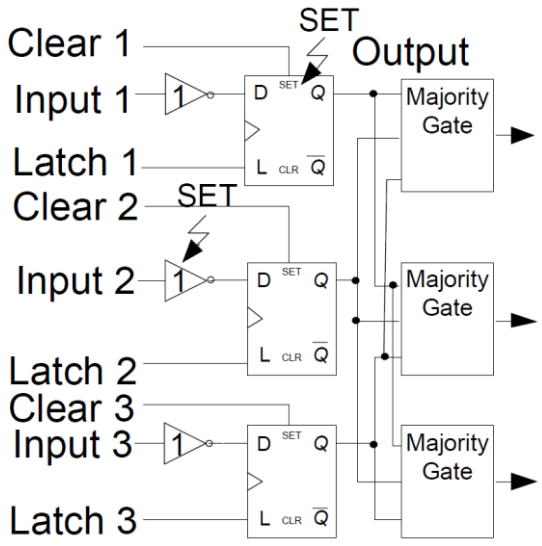

Figure 35: Implementation 6

4.3.3.7 Implementation 7

Implementation 7 makes use of DMR protection of the user logic and two SET filters before the latches. There is however no protection of the clock and clear signal as well as no protection for the latches against SEUs and no majority gates.

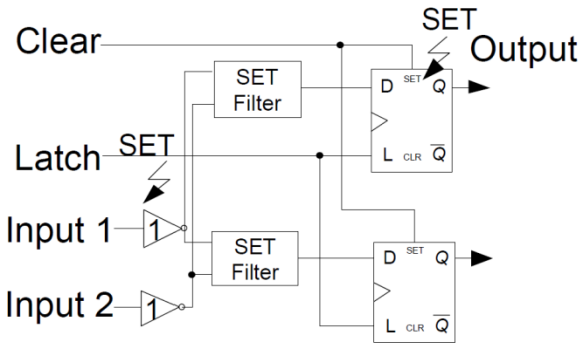

Figure 36: Implementation 7

4.3.3.8 Implementation 8

Implementation 8 makes use of a series of AND gates to filter two input signals. The single resulting user logic signal is then sent to three SET filters using the delay element. The latches are protected from SEUs by TMR and a single majority gate. The clock and reset signals are unprotected.

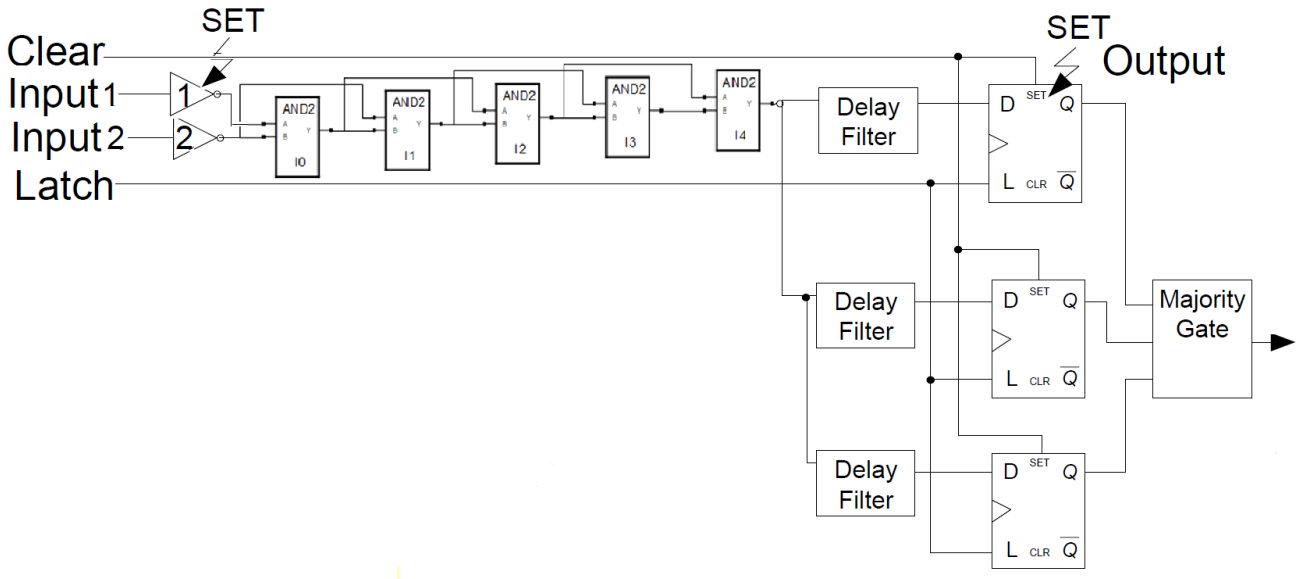

Figure 37: Implementation8

4.3.3.9 Implementation 9

Implementation 9 provides TMR protection of the user logic in addition to the use of SET filters with the delay element. The latches are protected with TMR and a single majority gate with MBU protection. TMR protection is provided for the clock and clear signals.

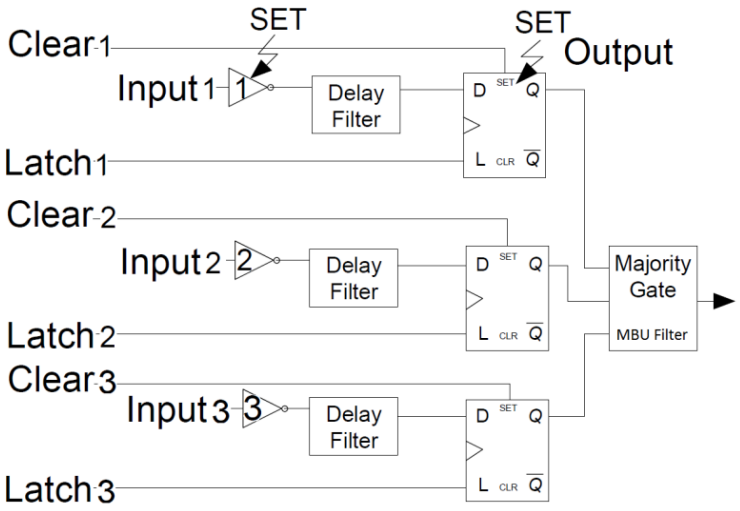

Figure 38: Implementation 9

4.3.3.10 Implementation 9 forced multiple bit upset

This implementation is identical to implementation 9, but forces multiple bit upsets to occur.

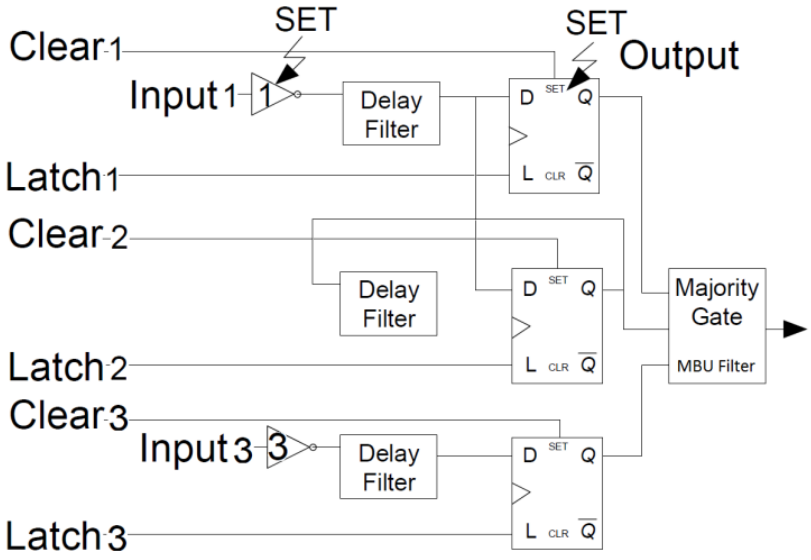

Figure 39: Implementation 9 MBU

4.3.3.11 Implementation 10 forced multiple bit upset

Implementation 10 is identical to implementation 6 with the inclusion of MBU filters, however it forces multiple bit upsets to occur for every SEU to test the effectiveness of these MBU filters.

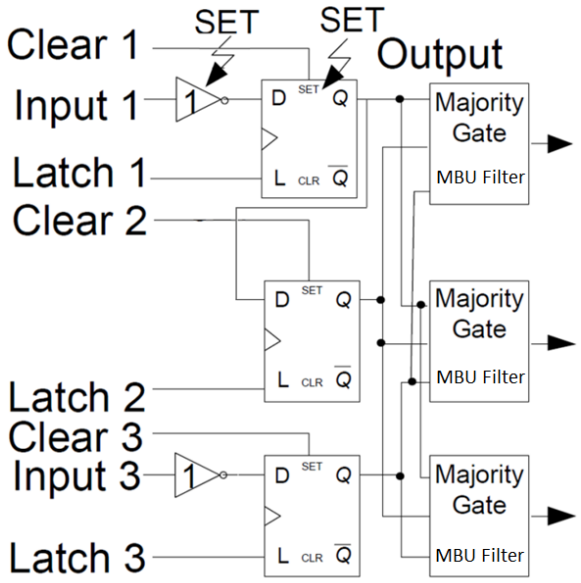

Figure 40: Implementation 10 MBU

4.3.4 Serial Peripheral Interface

The synchronous SPI protocol was developed as an improvement of the asynchronous serial communication methods. The SPI protocol is a high speed short distance communication method which is able to transmit and receive data of almost any format or length. SPI controllers have been implemented in most 32 bit processors including the ARM, MIPS and PowerPC, FPGAs as well as microcontrollers such as the PIC, AVR and MSP430 [85, 86]. SPI is utilized in a large number of secondary devices as shown below:

- temperature sensors, pressure sensors, analogue to digital converters, touch screens
- audio codecs, digital potentiometers, digital to analogue converters
- Camera lens mounts
- Ethernet, USB, USART, CAN, IEEE 802.15.4, IEEE 802.11
- flash and EEPROM memory

- LCD displays
- MMC or SD cards

The SPI protocol allows a master device to accurately and easily communicate with a number of slave devices using shared data signals (MISO and MOSI), a shared clock signal (SCLK) generated by the master device and a slave select signal (SS) to initiate the desired slave. The inclusion of this clock line eliminates the stringent timing requirements and ensures that the data is transmitted and received by both the master and slave on the same rising or falling edge of a clock pulse. The synchronous nature of this communicating also allows the clock rate to be varied without interrupting the data transmission, within limits, by the master device to allow for user requirements. [78, 81]

The SPI protocol functions as a shift register between the master and salve device(s), as data is transmitted, data is also received. Data is never only transmitted or received by a master or slave, but is always sent and received by both devices. Data received, but not read will be lost once the next bit is transmitted.

Timing considerations of SPI include, both ensuring the clock signal is within limits for the slave device(s) and ensuring that the master and slave device have the same mode of operation. The mode of operation is determined by the clock polarity and clock phase parameters. A clock polarity of zero indicates that the first clock edge is the rising edge. A clock phase of zero indicates that the first data bit is written on the salve select falling edge and read on the first SCLK edge [79]. A summarised graphic representation of the modes of operation can be seen in Figure 41 [79]. Figure 42 shows a multiple slave set up.

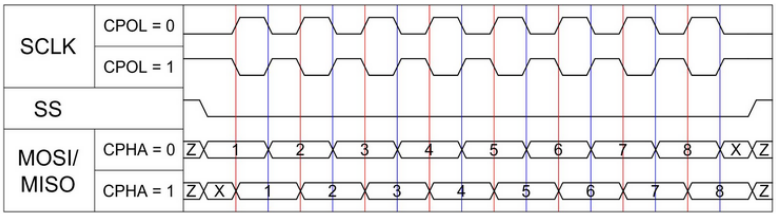

Figure 41: Typical SPI operating modes [79]

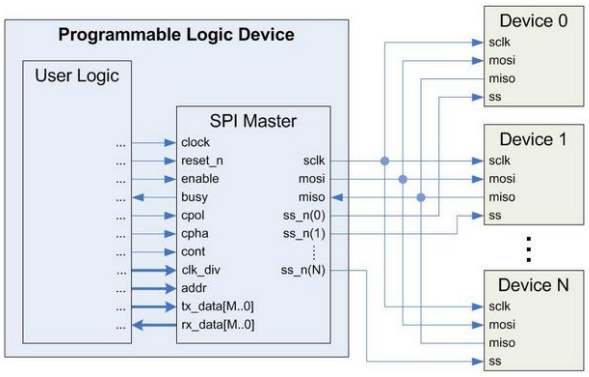

Figure 42: Multiple slave SPI mode [79]

Multiple slave set up is possible with the inclusion of a salve select line for each salve. The SS line is active low, thus selecting the desired slave for communication is done by setting the SS line for the target device to low.

- The typical communication procedure comprises of:
- setting the SS line of the target device low
- Sending the instruction data byte (receiving a byte at the same time, which is usually ignored)
- Sending the address byte for the specific register to read
- Read the 8 or 16 bit data from the slave device
- Pull the SS line high

4.3.4.1 ADXL362 three axis accelerometer

The ADXL362 three axis accelerometer is an ultra-low power device capable of operating with an accuracy of 550 µg/√Hz in the x and y axes and 920 µg/√Hz in the z axis while requiring only 1.8uA during normal operational mode. Two additional modes of higher noise immunity are available in the device which increases accuracy to 175 µg/√Hz in the x and x axes and 250 in the z [80]. This ultra-low noise mode of operation requires 13uA at the rated 3.5V supply. The device is further able to decrease the power requirements by having the ability to enter a standby mode drawing 0.01uA current. This mode is automatically, or manually exited when activated by motion or a command. The device is available in a 3mm x 3.25mm x 1.06mm package. The ADXL362 has three possible measurement ranges, including ±2 g, ±4 g, and ±8 g, with a resolution of 1 mg/LSB, 2 mg/LSB and 4 mg/LSB for the ranges respectively. The physical dimensions, low power requirements, high accuracy

and range make this device suitable to be implemented on board satellites or any other space based platform [80].

The accelerometer was used to determine the rate of acceleration and position of the platform or components of the space platform, in order to ensure correct positioning, orientation and alignment. Such implementations may include the correct alignment of solar panels, alignment of cameras or other sensors and the tracking of the rotation or movement of any components.

Figure 43 demonstrates the required communication sequence for the correct transmission of a single byte of data from a specific register of the device.

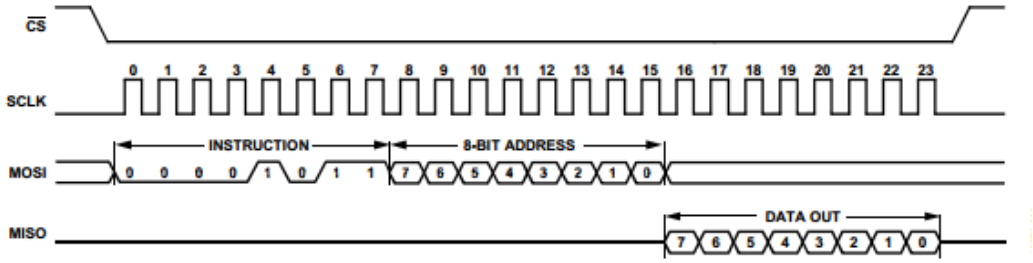

Figure 43: Required Communication procedure [80]

Figure 44 shows an example of a MISO input signal sent from the control board simulating the output of a sensor. This signal was used to test the SPI receiving circuit during irradiation. The input signal as well as the frequency of the singal is determined by the control board. A series of alternating 1s and 0s were sent to the test FPGA at a frequency of 6.25 KHz (160 µs period).

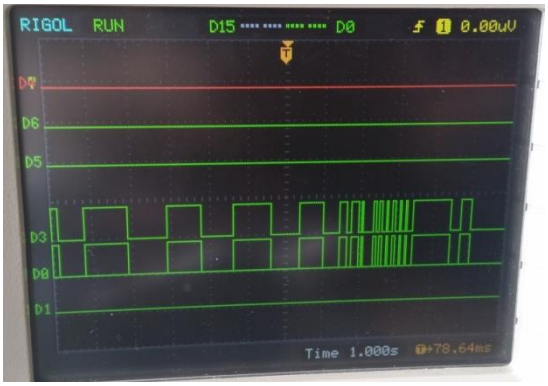

Figure 44: SPI MISO test signal

Figure 45 illustrates the MOSI signal sent from the test FPGA to the control board, simulating a sensor. This signal was tested during irradiation to determine the number of upsets occurring in the transmitting circuitry of the SPI code. The binary values of “000010111 000010111” was sent to the control board to simulate the requesting of receiving data in the given address. This signal was sent at a frequency of 0.6 kHz.

Figure 45: SPI MOSI test signal

Figure 46 shows the clock signal output for the SPI implementation. The frequency of the SPI clock was set to 1 kHz (1ms period).

Figure 46: SPI clock signal

4.3.5 Inter Integrated Circuit (I2C)

Inter Integrated circuit (I^2C) is a multi-master, multi-slave serial protocol two wire interface to connect two devices of low speed over a short distance. The I^2C bus comprises of a bi-directional serial data (SDA) and clock (SCL) line [87, 88]. I2C has the advantage over other communication methods of allowing a number of master devices to communicate with a network of slave devices

requiring only two wires due to the built in addressing capability [87, 88]. I2C can be used as a control interface to signal processing devices which comprise of separate application specific data interfaces [81]. Other applications include [84]:

- RF tuners, video decoders and encoders, audio processors.
- Reading configuration data of SPD EEPROMs on SDRAM, DDR SDRAM, DDR2 SDRAM memory
- Accessing NVRAM chips
- DACs and ADCs.
- Changing contrast, hue, and colour balance settings in monitors
- Changing sound volume in intelligent speakers.
- Controlling OLED/LCD displays
- Reading hardware monitors and diagnostic sensors, CPU thermostat and fan speed.
- Turning on and turning off the power supply of system components.

As with asynchronous serial communication, I2C requires only two wires for communication. Additionally I2C can accommodate any number of master devices and up to 1008 slave devices [87, 88]. Allowing multiple master devices further increases the flexibility of the system to allow multiple master devices such as microcontrollers and microprocessors to access each compatible I2C device. I2C communication data rates fall between SPI and asynchronous serial. I2C devices generally operate at either standard data rates of up to 100 kHz or fast mode data rates of up to 400 kHz. A later revision of the I2C protocol was developed supporting data rates of up to 5 MHz, but devices generally operate at the 400 kHz data rates [87, 88]. I2C is more complex to implement in software than that of SPI and UART, as it requires adhering to specific communication protocols.

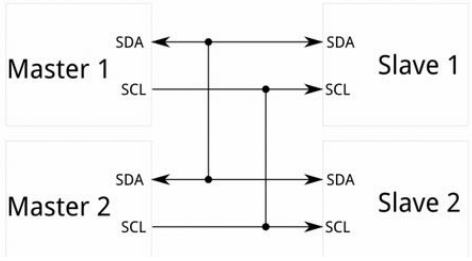

Figure 47: Multi master and slave I2C set up

4.3.5.1 TMP102

The TMP102 is a low power digital temperature sensor with an operating range of -40degrees Celsius to +125degrees Celsius, with an accuracy of 0.5degc and resolution of 0.0625 degrees Celsius. The TMP102 operates with a supply voltage range of 1.4V to 3.6V and requires 10uA maximum current during operation [89]. The TMP102 is available in a package size of 1.5mm x 1.5mm x 0.5mm and operates in the fast (1 kHz to 400 kHz) and high-speed (1 kHz to 3.4 MHz) modes. The device includes features such as a shutdown mode to save power, a thermostat more to operate as a comparator, extended more to read values below and above the indicated range and variable data conversion rates to allow for optimal power usage and data output rate combinations [89].

Communication with the TMP102 requires a set sequence of transmitting and receiving data to operate as a data transmitter, as outlined below [89]:

- Communication is initiated by addressing the appropriate salve TMP102 by transmitting the required 7 address bits followed by a direction bit, indicating the intent to write or read data.
- The TMP102 acknowledges the reception of the correct addressing byte
- The TMP102 salve device transmits the most significant byte of the temperature value
- The master transmits a acknowledge bit to the salve to continue transmission
- The TMP102 slave transmits the least significant byte of the temperature data to the master
- The master transmits a acknowledge bit to the salve to acknowledge the reception of the data

Figure 48 illustrates the TMP102 sensor communication protocol.

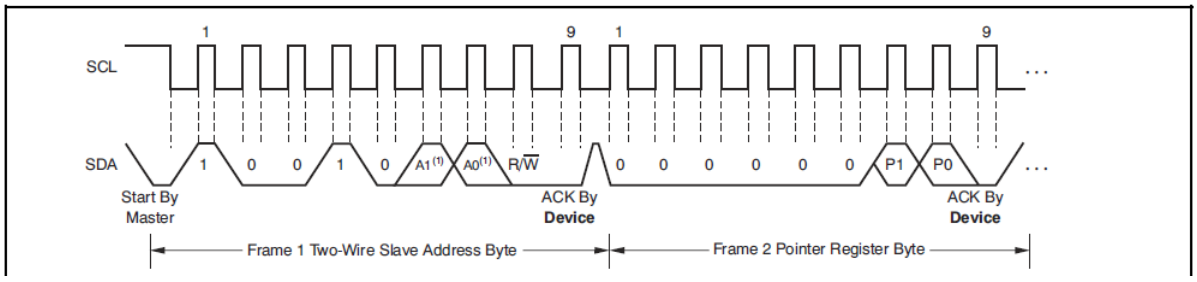

Figure 48: TMP102 communication protocol [89]

The high temperature range, high resolution and accuracy combined with the low power requirements and physical dimensions of the TMP102 enables this device to be a suitable temperature sensor to be implemented in a space environment. The sensor can be utilized to determine the temperature of battery packs in the space platform, measure the temperature of motors and motor drivers, solar panel temperatures, shielding temperature and general equipment monitoring.

Figure 49 illustrates the SDA signal of the I2C circuit. The 7 bit address and command is sent to the salve, in this case the control FPGA, followed by the two byte pointer register address. The frequency of the signal was sent set to 400 kHz (2.5µs period) according to the device specifications. The bit sequence sent included pulling the output signal low followed by the "10010001" instruction and address data.

Figure 49: I2C SDA signal

Figure 50 shows the I2C clock signal with a frequency of 4MHz (250ns period) used during testing of the I2C error rate.

Figure 50: I2C SCL signal

4.3.6 Universal Asynchronous Receiver/Transmitted

A universal asynchronous receiver/transmitter (UART) is a section of circuitry which is required to transmit and/ or receive parallel data over a serial interface. Parallel data is able to be transmitted and received serially and recombined into parallel data [90]. UART is a form of asynchronous serial communication, requiring predetermined timing parameters (baud rate) and start, stop and parity bits combined with each byte of data to ensure that the transmission and receiving of data is synchronized [90, 91].

UARTs are commonly found in microcontrollers, as software in a processor and as standalone ICs and are generally classified as functioning as either a transmitter or receiver. The transmitter is responsible for creating a serial data packet from parallel data, adding synchronization and parity bits and transmitting this data packet within the specified timing limits. The receiver is responsible for reading data from the incoming line at specified timing intervals, interpreting the sync and parity bits and then outputs this data to the microcontroller or other components [90, 91, 92].

The communication procedure can be described in the following steps [90, 91, 92]:

- The transmitter sends a start bit to the receiver to indicate that data is about to be sent
- The data bits starting with the least significant bit are sent one at a time, each after a time period specified by the baud rate.
- The receiver reads the data bit on the incoming line at exactly halfway through the specified period
- After the transmission of the data byte, a parity bit may be added by the transmitter to allow for error detection by the receiver
- The transmitter then sends a stop bit to signify the end of the data transmission, which must be detected by the receiver or else an error signal, will be sent by the receiver to the host.

Figure 51 demonstrates the basic UART TX and RX protocols.

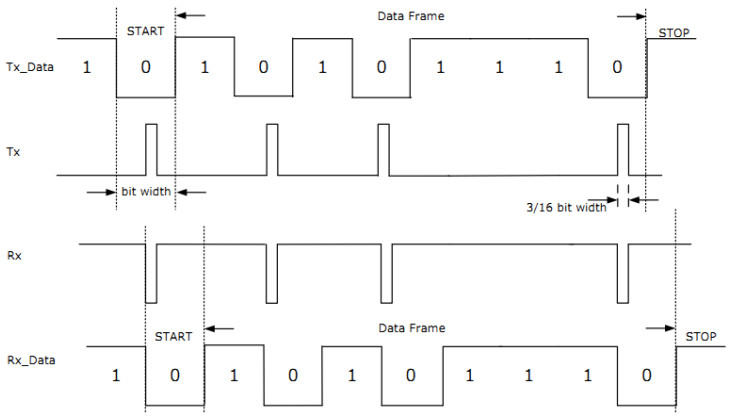

Figure 51: UART communication protocol [92]

UART is generally used in any form of communication where parallel data is required to be sent over a serial connection. The connections vary from serial wired connections to wireless radio frequency connections. Commonly used data rates for UARTs vary in fixed values from a baud rate of 1200 to 921600 bps.

4.3.6.1 RWS-371-6receiver and TWS-BS transmitter RF modules

A radio frequency (RF) transmitter and receiver pair was chosen for UART testing. The TWS-BS RF transmitter operates at a frequency of 433.92MHz and transmits data up to a baud rate of 8000 bps [94]. The TWS requires a supply voltage of 3 to 12V and current of 8mA, and has a transmission range of 500feet, making this transmitter unsuitable for space based applications [94]. This device was chosen as an inexpensive alternative for the high power RF transmitters available which require the same operation UART control code to transmit data. As only the control code will be tested and not the device, the device range is not of significance.

The RWS-371-6 RF receiver operates at a frequency of 433.92MHz, a 5V supply and 4800 bps baud rate [93]. This transmitter receives data from the TWS transmitter and will be used as an inexpensive substitute as opposed to the long range RF receivers implemented on-board space based systems [93]. The operational UART code again remains the same for these devices with only changes in the data rates.

Figure 52 illustrates the UART TX signal sent to the control FPGA. The signal consisted of an “11100011” bit sequence in addition to a start and stop bit, sent at a frequency of 2.5 kHz (400µs period).

Figure 52: UART TX signal

Figure 53 shows an example of the UART TX input signal. The bit values of the input signal was stored and sent to the control FPGA. The input signal was controlled by the control FPGA as in the MISO signal. This signal was sent at 6.25 kHz.

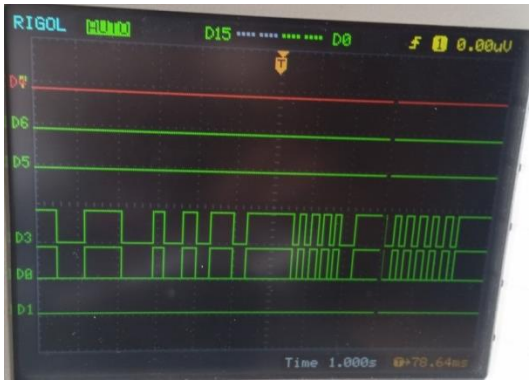

Figure 53: UART TX signal

4.3.7 DC Motor

Direct Current (DC) motors are the most common motors found in the majority of electro-mechanical actuation applications. DC motors are based on the principal of placing a coiled current carrying conductor within a magnetic field, causing attraction and repulsion of opposing fields which

results in a mechanical force [95, 96, 97]. A brushless DC motor consists of a rotating, permanent magnet in the rotor surrounded by stationary electromagnetic magnets in the housing called the stator. The supply voltage is applied in pulses of a specified pulse width, called pulse width modulation which determines the resulting shaft speed of the motor. The direction of the shaft rotation is determined by the direction of current applied. The desired motor position is determined by the amount of time the motor rotates at a specific speed. A shaft encoder may be used to accurately determine the position of the shaft [95, 96, 97].

A DC motor control circuit was chosen as a test circuit for the purpose of this research, as DC motors are commonly used in many applications in space. DC motors can serve various functions such as to drive land based vehicles, rotate components of vehicles or platforms or to actuate components to perform tasks. DC motors are able to rotate through 360 degrees for long continuous periods of time, either at high speeds and low torque or lower speeds and high torque when combined with a gearing system. To function with operational accuracy, DC motors require a feedback system.

Figure 54 illustrates the high speed DC motor control output signal. This PWM signal simulates the output signal to drive a DC motor at high speeds. The signal frequency can be seen to be in the 5 kHz range.

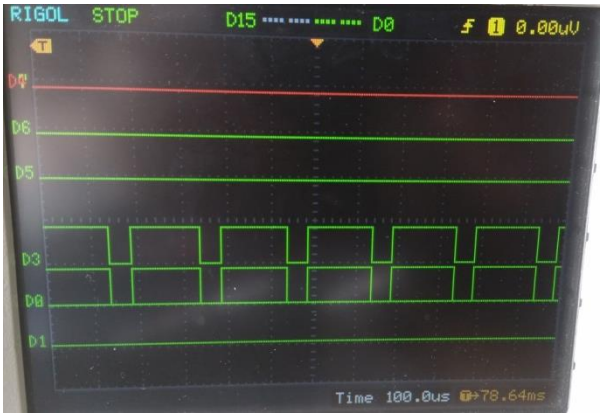

Figure 54: High speed DC output signal

Figure 55 illustrates the PWM signal to drive a DC motor at a low speed. This signal can be seen to have a high output frequency pulsing in the range of 5 kHz.

Figure 55: Low speed DC output signal

4.3.8 Servo Motor

Servo motors are rotational actuators which allow for precise control of an angular position. Servo motors are able to rotate to a very accurate position at a highly accurate angular velocity and acceleration within a given rotation limit of the motor [98, 99]. The motor receives a pulse width indicating the desired position to rotate to and once completed, remains at this position without having to remove the power supply. Servo motors are combined with a rotary encoder to calculate the exact position of the motor for a closed loop control of the motor system [98, 99].

Servo motors fundamentally consist of a DC motors connected to a speed reduction gear system, increasing the output torque. The servo motor also has an electronic system which calculates and monitors the position of the shaft according to the input position. Servo motors form part of almost all precision actuating devices which are required to accurately position a member [98, 99]. These applications in space may include the positioning of solar panels, movement of extremities of robots and positioning of sensors. Servo motors require less power than stepper motors, and require no switching of power as in DC motors.

Figure 56 illustrates the servo motor PWM control signal required to drive the motor. The lower frequency of the output signal can be noted to pulse at an approximate frequency of 200 Hz.

Figure 56: Servo motor PWM signal

4.3.9 Stepper Motor

Stepper motors comprise of a rotor, a permanent magnet rotating shaft, and stationary electromagnets, referred to as the stator, surrounding the motor [100, 101]. Stepper motors reduce one revolution into a number of steps energised by pulses. Stepper motors require four wires as inputs to the four electromagnets, which when energised, result in a step of the motor shaft. The motor is only able to rotate one step at a time and each step must be either before or after the previous [83, 100]. Since the motor operates in discrete steps, the shaft position of the motor can easily be determined by the input signals without a feedback system. The speed of a stepper motor is determined by the speed of the input signals to the motor magnets and the position of the shaft is proportional to the number of pulses, allowing for reliable and simple control over speed and position. Stepper motors have the advantage over DC and servo motors as it maintains a high holding torque at standstill if a winding is energised. Further resolution of steps and an increase in output torque is possible by half stepping the motor [83, 100].

Stepper motors are inexpensive, reliable, robust and accurate rotary actuators. Therefore these motors are able to be utilized in space based applications to drive wheels on land based systems, actuate any members or equipment or rotate and move sensors.

Figure 57 shows a single stepper motor output signal for one of the four motor windings. The output signal can be seen to pulse at an approximate frequency of 1.562 kHz. Since four of these signals are sent to the motor, the effective output frequency is 6.25 kHz.

Figure 57: Stepper motor output signal

Figure 58 shows the stepper motor output signals for two of the windings, illustrating the difference in phase of the signals.

Figure 58: Stepper motor winding outputs

4.3.10 Control Board Circuit

The control and monitoring board was responsible for the sending of the input signals to the test FPGA, as was well as detecting errors in the output of the test FPGA. The output signals required to be sent to the test FPGA included the MISO, UART RX, DC speed, DC direction, servo speed up and

sped down signals. The control FPGA sent alternating 1s and 0s as inputs to each of these signals. This served as simulated data received from the slave sensors in the case of SPI and UART and the motor control signals to adjust the speed and direction of the test motors.

The input signals from the outputs of the testing FPGA was compared to determine if an SEU had occurred in any of the circuits. If an SEU was detected by the control board, an output was sent to the DAQ to indicate that an error had occurred for a specific circuit. The VHDL code for this control FPGA can be found on the attached disk.

4.4 Data Acquisition

The variables required to be monitored during this test varied for TID and SEU testing. During SEU testing, the outputs from the DAQ for each implemented circuit were monitored by the control FPGA to detect errors. The control FPGA outputted a logic high on the specific pin allocated for the circuit in which the error occurred. This signal, indicating an error for the specific circuit, was counted by the NI9403 DAQ and accumulated the number of errors for each circuit implemented in the DUT. For TID testing, the outputs of the DUT were monitored and counted in the same manner as for SEU testing. Additionally, the supply current to the board and the VCC, VCCPLF and VCCIB voltages were captured by the NI9205 DAQ and be monitored to record the current and voltage changes of the board as the total absorbed dose increased. The duration of each test was recorded to calculate the SEU and TID characteristics.

As no open connection were available on the board itself to allow for current measurements, a shunt resistor was required to measure the supply current of the DUT.

4.5 Experimental Setup - Total Ionizing Dose

The physical setup of the test performed can be seen in Figure 59. The figure illustrates the setup at the facility in which the basic location of the Co-60 source and the DUT can be seen. The wiring was installed in the provided areas at the facility as directed by the supervisors. The monitoring of the DUT was performed outside of the room on a laptop running LabVIEW. The test board FPGA as well as the DAQ and the control FPGA were kept within the test room as an Ethernet cable was able to fit through the provided wiring hole. The monitoring equipment was protected with lead blocks.

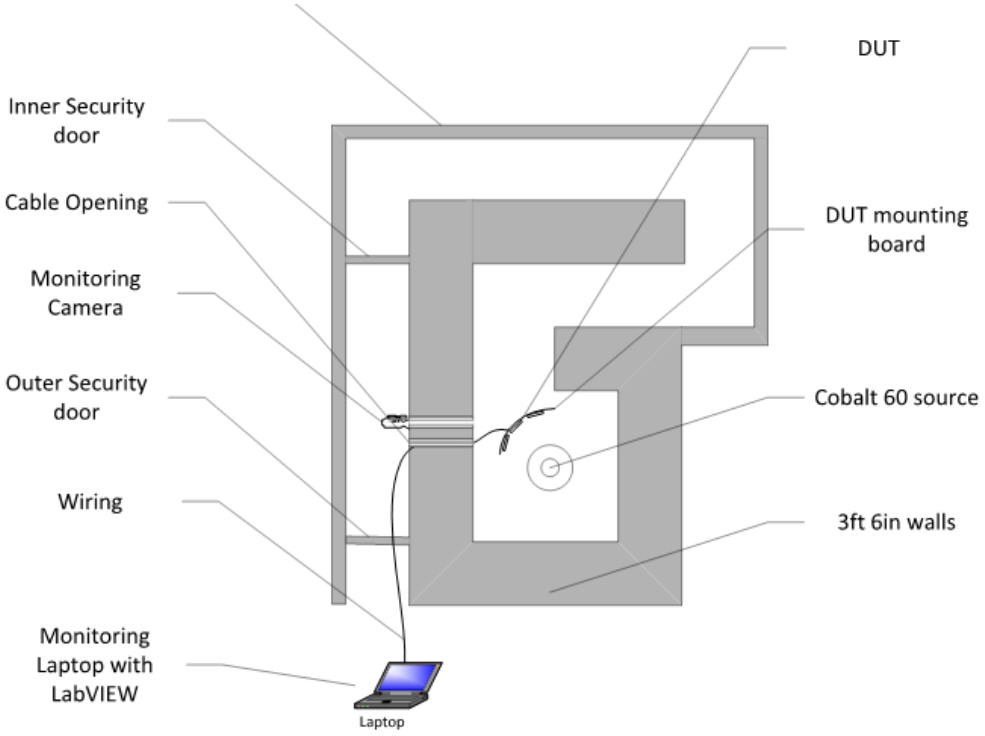

Figure 59: Facility Layout

4.5.1 Electrical Design

The electrical set up for the TID testing was simple as all of the components operated in open air conditions. The DUT, DAQ card and control board was in the test room during irradiation and only an Ethernet cable was able to connect the computer to the test room.

Figure 60 illustrates the electrical setup for the testing procedure. The computer running LabVIEW communicated with the DAQ chassis and cards via an Ethernet cable. The control board was connected to the inputs and outputs of the DUT with 1.6 metre ribbon cables. The length of the ribbon cables was kept below 2 metres to reduce noise in the cabling. The DAQ card was connected to the control board via ribbon cables of the same length. The DAQ card monitored the outputs from the control board, allowing the monitoring of the errors on the outputs of the DUT. Power was required to be supplied to the DAQ chassis, the control board and the DUT board individually, as the operating voltages of the devices varied. The supply current and relevant voltages of the DUT board was monitored and logged by the analogue ports on the NI 9403DAQ card. All digital input and

outputs were captured by the NI9205 and then recorded and displayed on by the computer running LabVIEW.

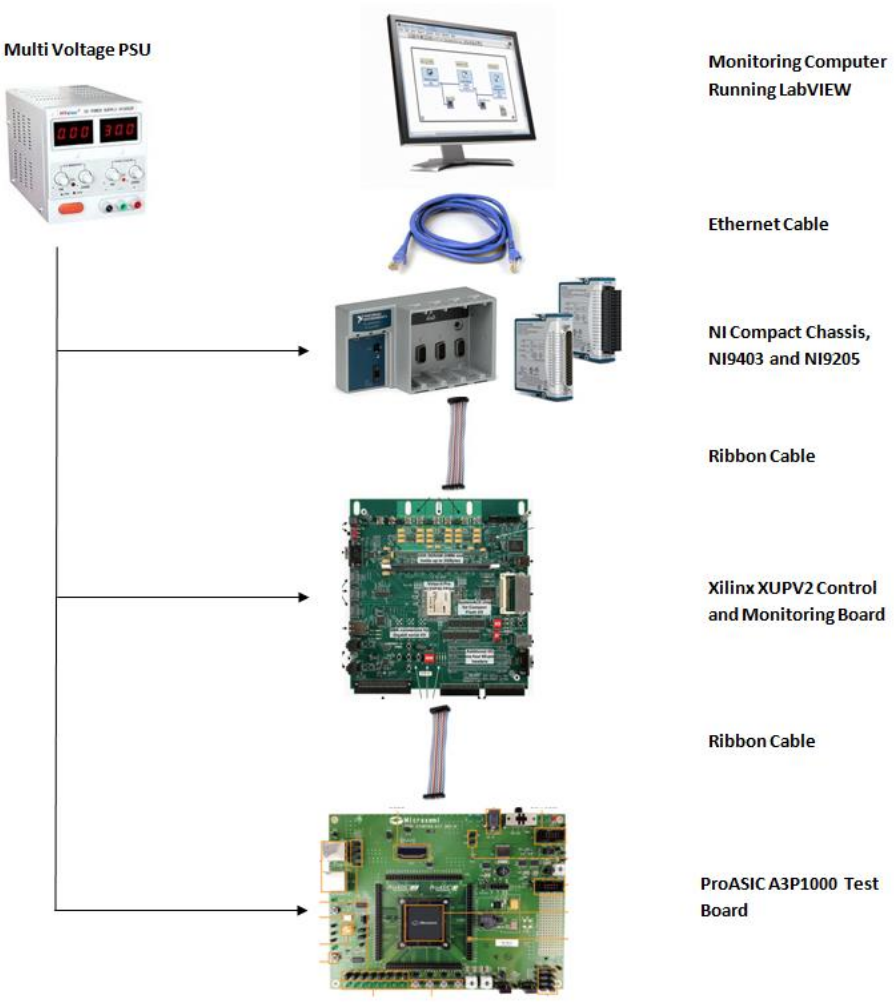

Figure 60: TID test configuration

4.5.2 Mechanical Design

The proposed mechanical concept for the TID testing can be seen in Figure 61. It was decided that a mechanical system would not be required, as only one FPGA was irradiated. The FPGA was simply placed on an elevated position in the line of sight of the CO-60 source and the control equipment was protected from the source with lead blocks.

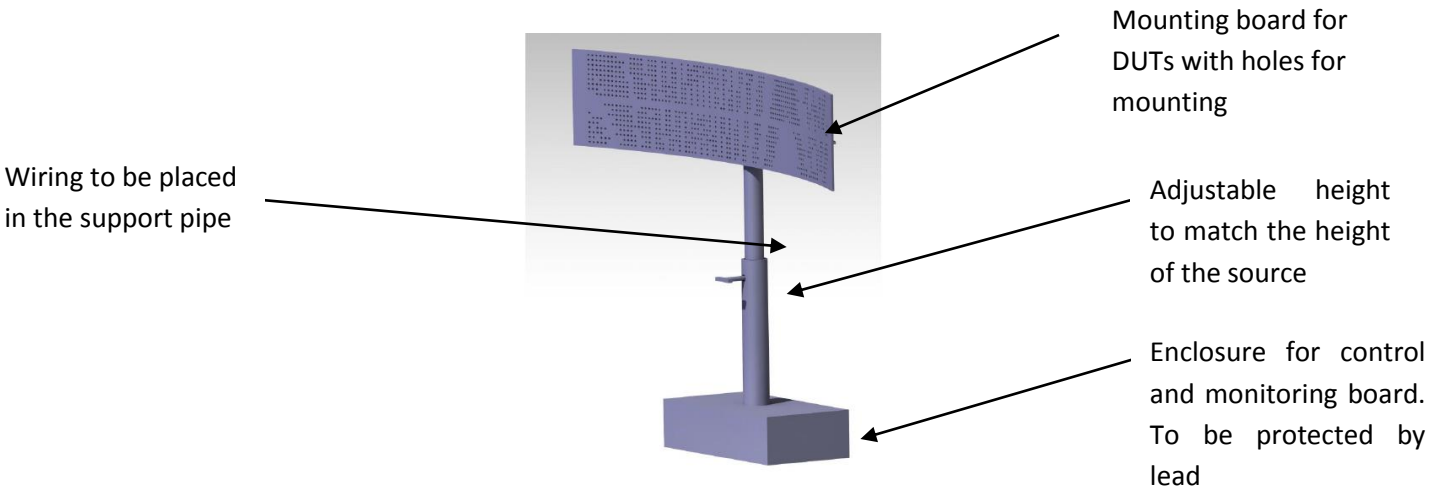

Figure 61: Proposed mechanical set up

4.5.3 Test Procedure

Each FPGA was programmed in advance to the experiment. Once the test setup was complete a test run was performed to check and account for any errors. Any persisting errors were accounted for in the results. This test provided the basic benchmark operating conditions of the FPGA

During irradiation, the testing time was recorded and displayed together with the required test variables. The parameters monitored included the supply current to the board, various voltages on the board and the number of errors of each implemented circuit. This data was saved and analysed at a later stage once the testing was completed.

4.5.4 Monitoring and Recording of Data

A program interface written in LabVIEW for the monitoring of the test variables can be seen in Figure 62. Since no inputs to the monitoring board or any control system was required, only the output errors were monitored by the NI9403 and the supply current and voltages by the NI9205. All of the monitoring LabVIEW programs written can be found on the attached disk.

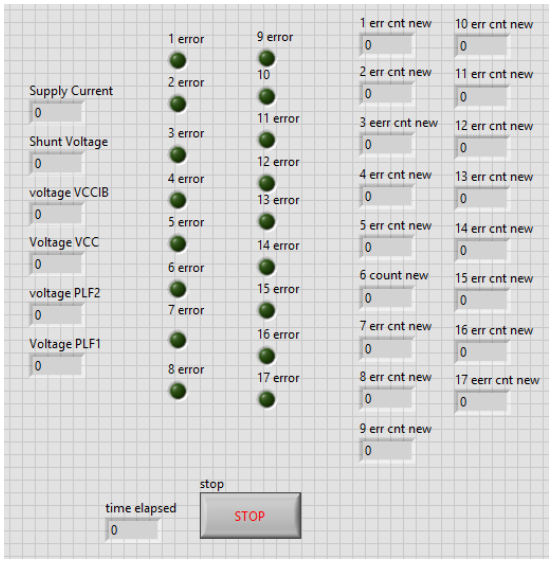

Figure 62: LabVIEW user interface

Figure 63 illustrates the LabVIEW code used to measure the current and voltage values inputted to the NI9205. As seen in Figure 63, the top section of the code calculates the supply current. The resistance across the shunt resistor was measured to be 14.5 Ohms, by which the voltage across the resistor is divided to calculate the supply current. The supply voltage was measured using the analogue input of the NI9205, an example of this can be seen in the lower section of Figure 63.

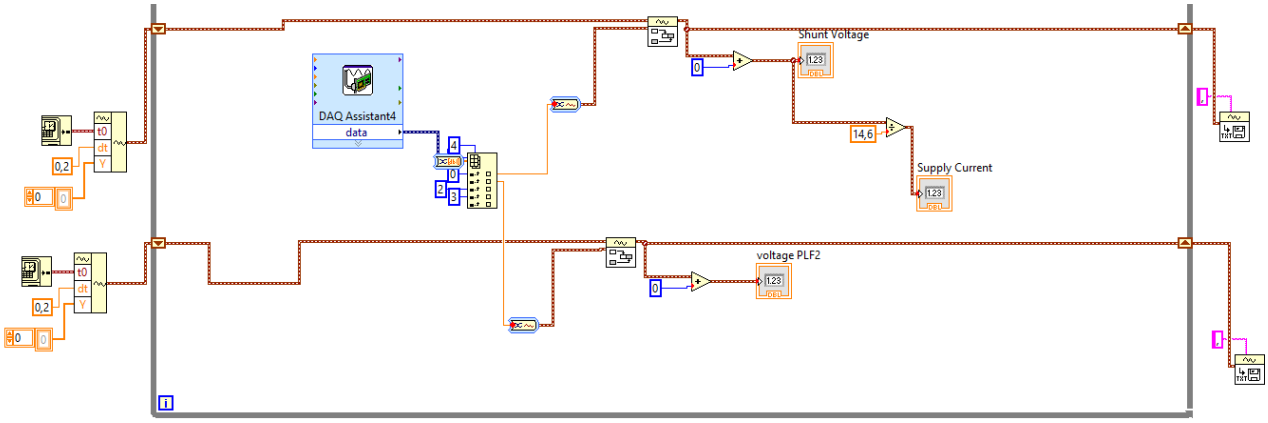

Figure 63: Current and voltage measurement method

Figure 64 shows the LabVIEW code for capturing and counting the errors which have occurred in each implemented circuit. The errors signal pin was connected from a specific pin on the control FPGA board to a specified pin on the NI9403. Each error signal outputted for a specific circuit by the control board was accumulated by the LabVIEW program.

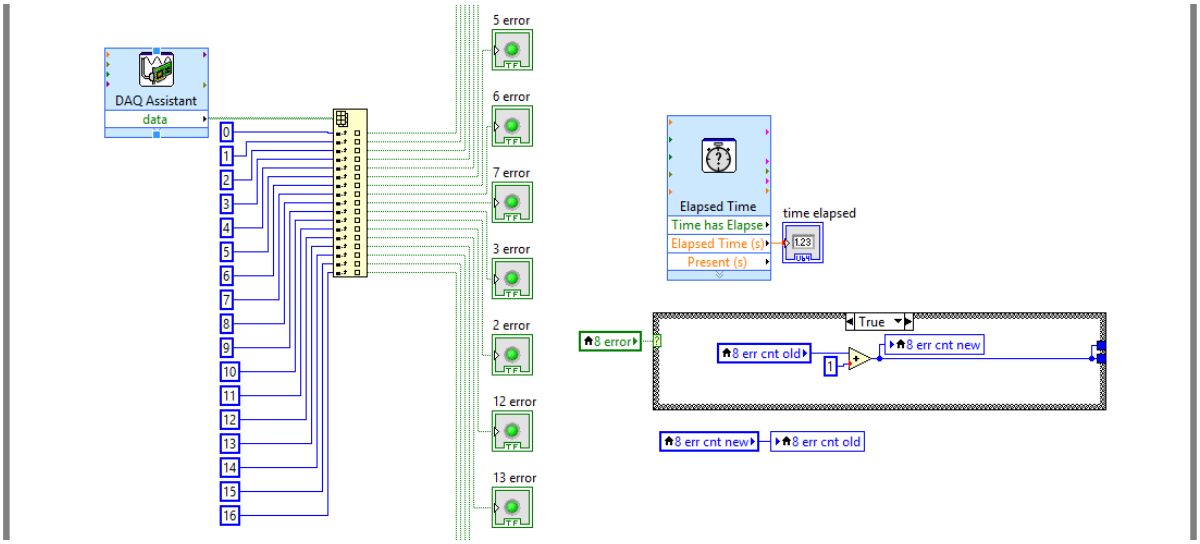

Figure 64: Section of LabVIEW code counting errors

4.5.5 Data Analysis

The data analysis for the TID testing included the plotting of the number of errors counted for each implemented circuit over the test duration, which was represented as the total absorbed dose. Additionally, the supply current and board voltages was graphically displayed for the test duration. From these graphs, the TID characteristics, such as A3P1000 operating voltage and supply current and the number of expected output errors, can be estimated for implementation within a radiation environment.

4.6 Experimental Setup - Single Event Upset

In addition to the TID testing conducted in the experimental procedure, the single event upset (SEU) characteristics were required to be determined for the ProASIC A3P1000. A number of test circuits, including SPI, I2C, UART, DC motor, servo motor and stepper motor control circuits were tested to determine the SEU characteristics of each. Additionally a number of mitigation schemes were implemented in the A3P1000 and the effectiveness of mitigating SEUs of each implementation was determined.

A SEU mechanical testing platform was implemented in a vacuum chamber in the iThemba cyclotron Laboratories in Cape Town. The mechanical set up allows multiple test boards to be positioned in the path of a proton beam, produced by a cyclotron. The test board are able to be individually selected for irradiation, as well as allow the angle of incidence of the board to be adjusted. All of the above can be performed under vacuum which allows for more testing to be conducted. Before the implementation of the mechanical system, only a single device was able to be tested after an approximate 5 hour time period, required to vent and then create the vacuum.

The requirements for the SEU experimental procedure included the designing and constructing of a mechanical system which was implemented to be used by the facility for future testing as well as irradiating an A3P1000 FPGA with a 66MeV Proton beam, used in determining the SEU cross section for various circuits implemented in the device. The mechanical set up allowed for the irradiation of FPGAs and will allow for other electrical and electronic devices tested at the facility. These tests will allow researchers and designers to test the desired components in a simulated space environment (radiation and vacuum). Initial testing determined the SEU characteristics of FPGAs in a space environment, such that the error rate of the device, when exposed to a certain level of energy, could be estimated by experimental results.

4.6.1 Testing Configuration

The test configuration for the SEU experiment can be seen in Figure 65. The test equipment was placed in the A-Line scattering room. The NI compact Chassis and DAQ modules was placed on the outside of the vacuum chamber and communicate with the control and test FPGAs inside the chamber via a male (FGG.2B.319) and female (FGJ.2B.319) vacuum connector. These specialised connectors allowed the vacuum to remain at an optimal pressure while connecting the components in the inside to those outside the chamber. The connectors were wired with a 20 core shielded cable and the control and test FPGAs were connected via 1.6 metre ribbon cables. The DAQ chassis was connected to a network switch with a 80 metre Ethernet cable, which in turn was connected to the computer running the LabVIEW software.

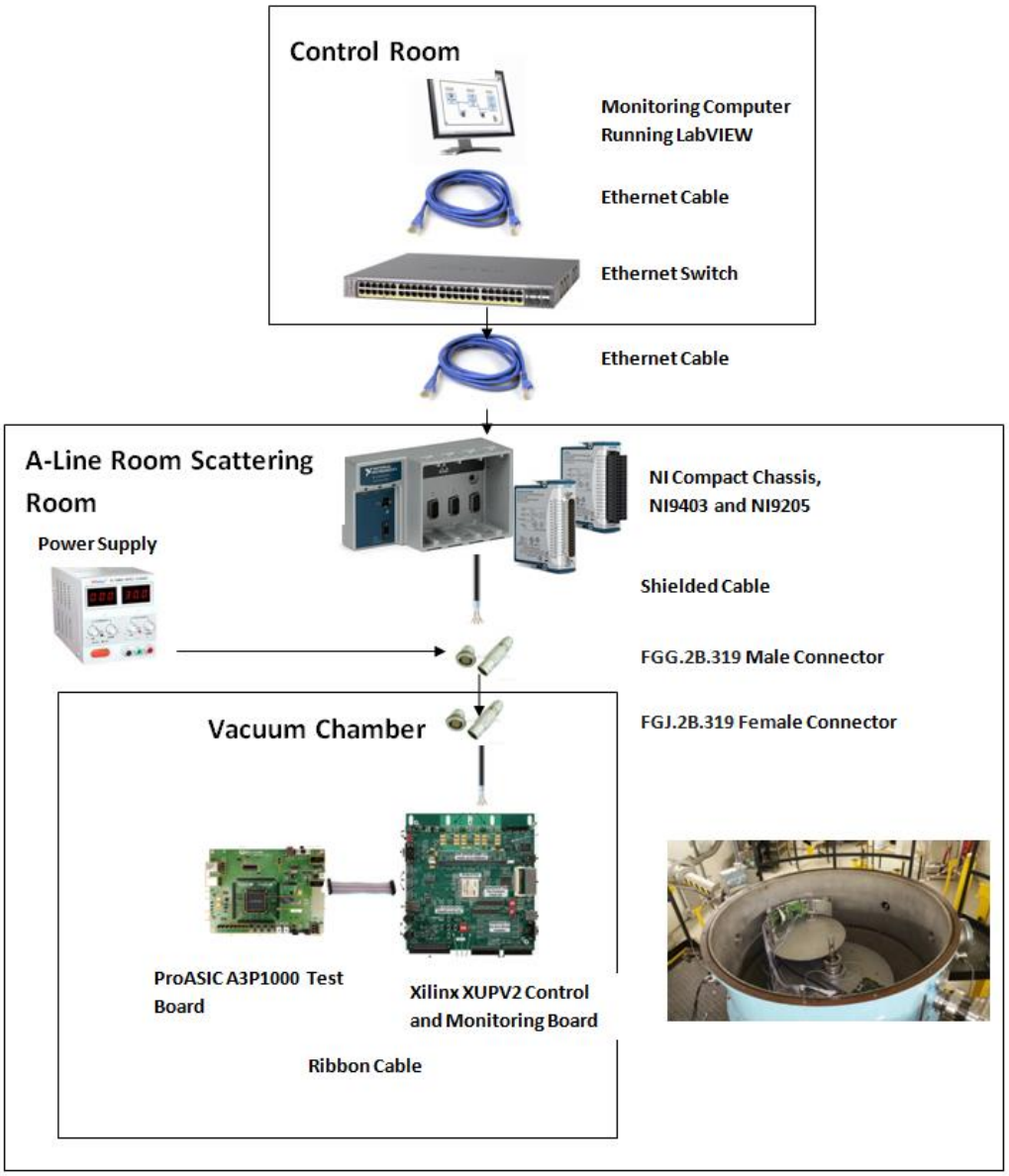

Figure 65: SEU test configuration

4.6.2 Mechanical

The requirements of the mechanical system design include the following:

1. Ability to test multiple test boards in a vacuum environment
2. Individual test board must be able to be selected for irradiation
3. Angle of incidence of the selected test board must be able to be varied

4. Position of the test boards must be able to be adjusted vertically to test multiple components on the DUT board
5. All of the chosen components both mechanical and electrical must be able to operate in the vacuum environment

4.6.2.1 Concept 1

The first concept designed to operate as the testing platform can be seen in Figures 66 to 68. This concept allows for the placement of five DUT boards, which together follow the curvature of the vacuum chamber. This allows for the DUT to be placed as close to the detector as possible, thus allowing for accurate radiation measurements at the position of the DUT. All of the DUT boards would be rotated together allowing for less motors and controls to be implemented. Each DUT is also able to be selected by moving the mounting board containing all of the DUT boards into the path of the beam. This concept does not however, allow for vertical adjustments to be made to the position of the board and would have proven to be too costly to manufacture.

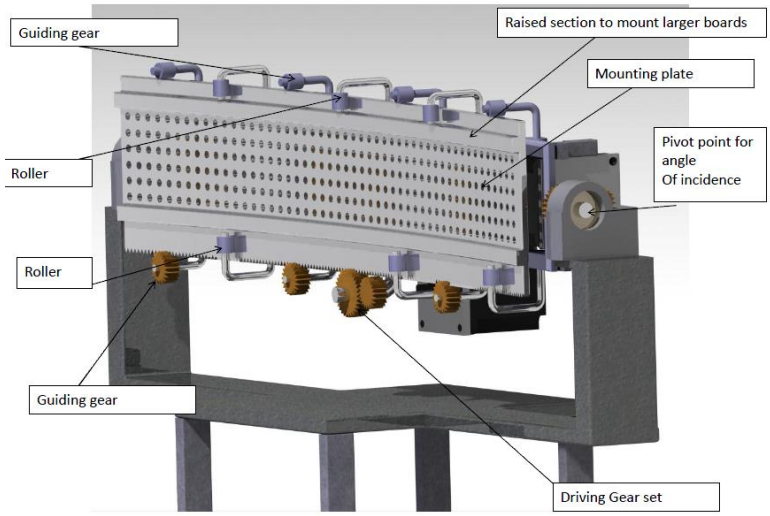

Figure 66: Concept Front

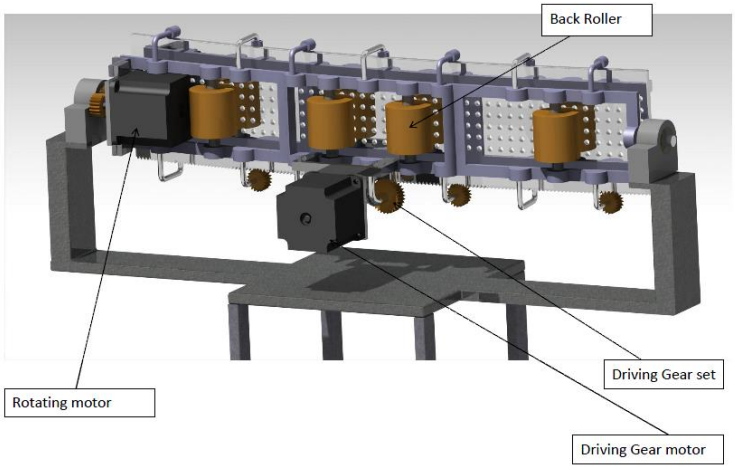

Figure 67: Concept Rear

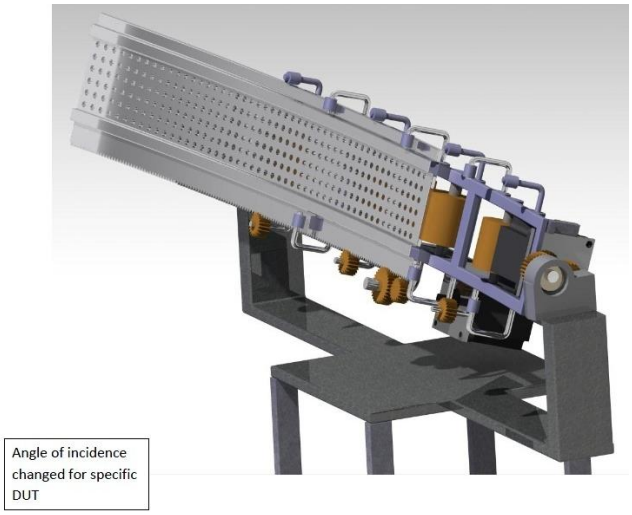

Figure 68: Concept DUT Selected Position

4.6.2.2 Final Design

The chosen concept can be seen in Figure 69. This concept allowed for vertical adjustments of the DUT boards in which multiple components on the DUT board can be tested. The system allowed each DUT board to be individually adjusted, but required more control. The whole system rotates about the base and allows each individual DUT to be selected for irradiation.

The vertical adjustments to the system are made by two stepper motors (FL57ST56-0606A) driving two anti-backlash lead screws. The lead screw assists in supporting the weight of the system and provides very high accuracy in the positioning of the system. Two shafts, guided by linear bushes, guide each lead screw and ensure that no moment is created on the screw resulting in bending and

misalignment. The DUT mounts are rotated by smaller stepper motors (FL39ST44-0304A) with the assistance of a bearing housing.

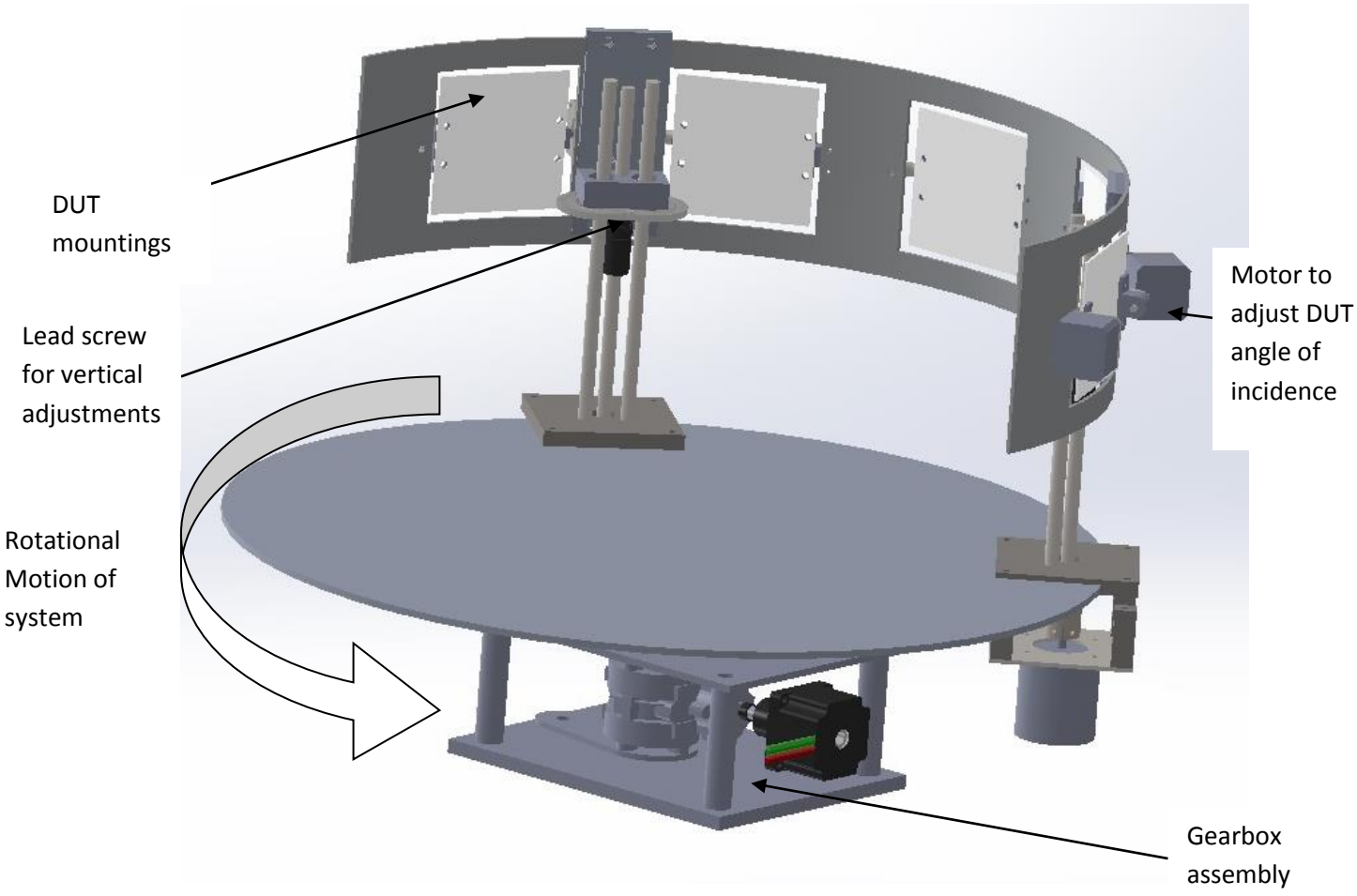

Figure 69: Final design

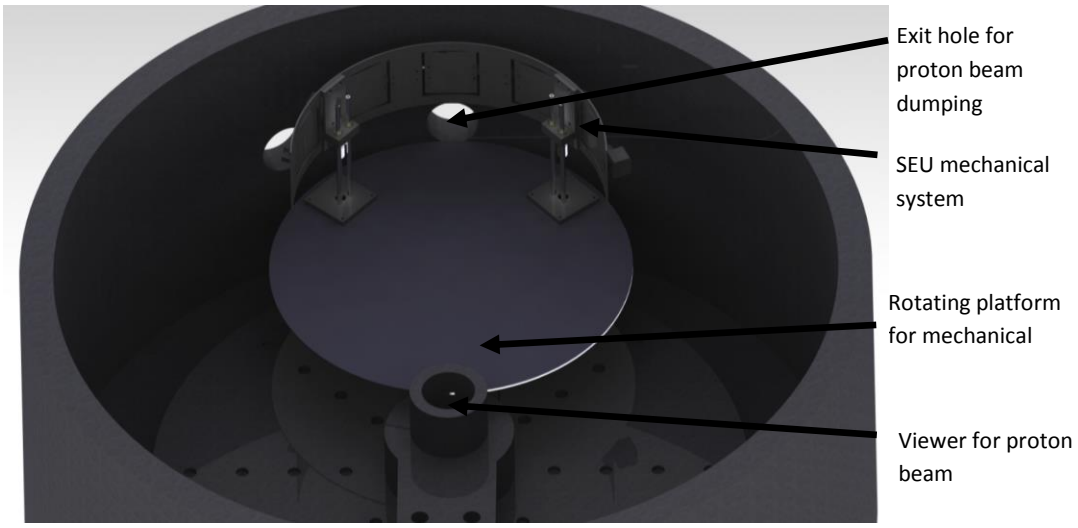

Figure 70: SEU mechanical in vacuum chamber

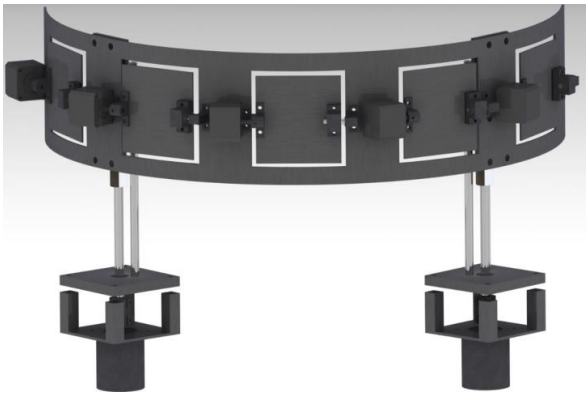

Figure 71: Reverse of SEU mechanical

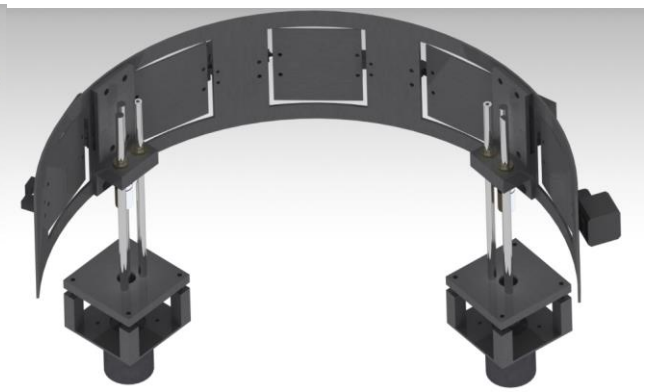

Figure 72: Front of SEU mechanical system

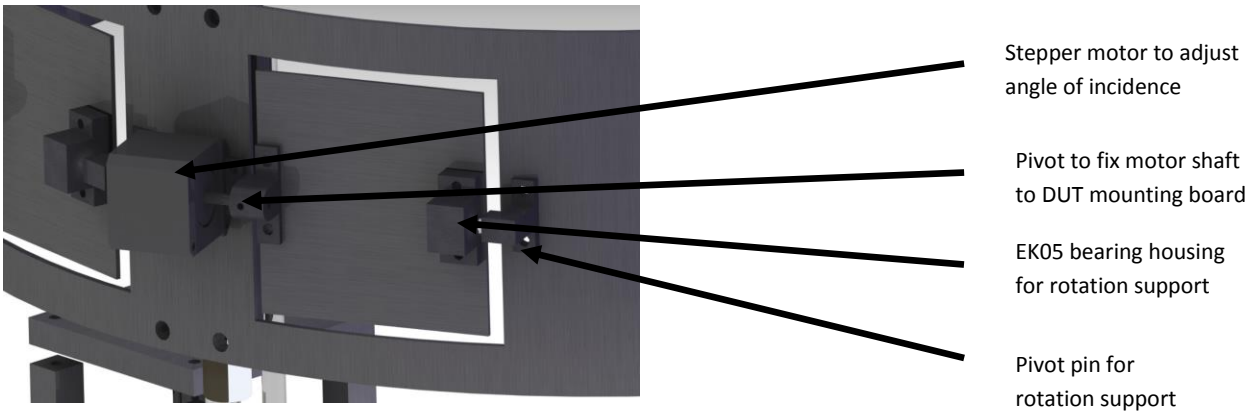

Figure 73: Reverse DUT mounting plate

Figure 74: SEU mechanical system

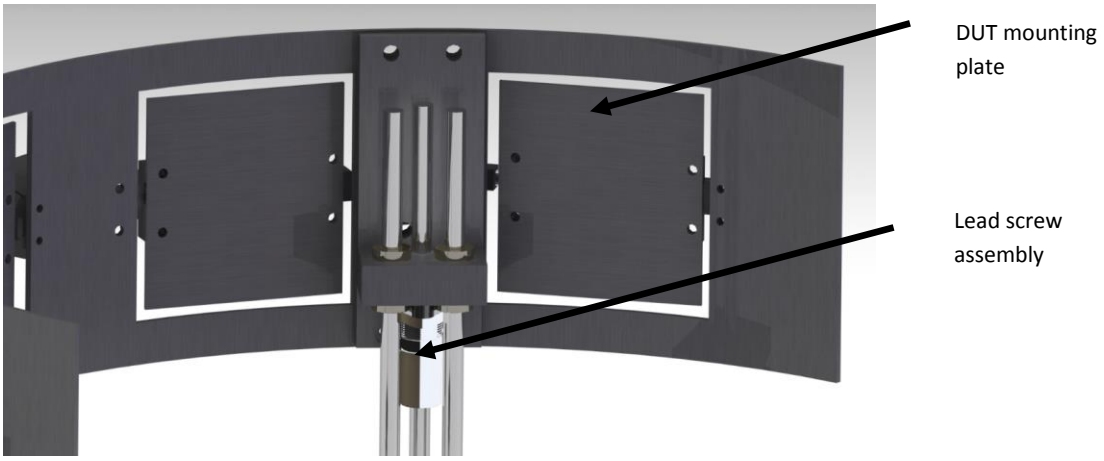

Figure 75: Front of SEU mechanical DUT plates

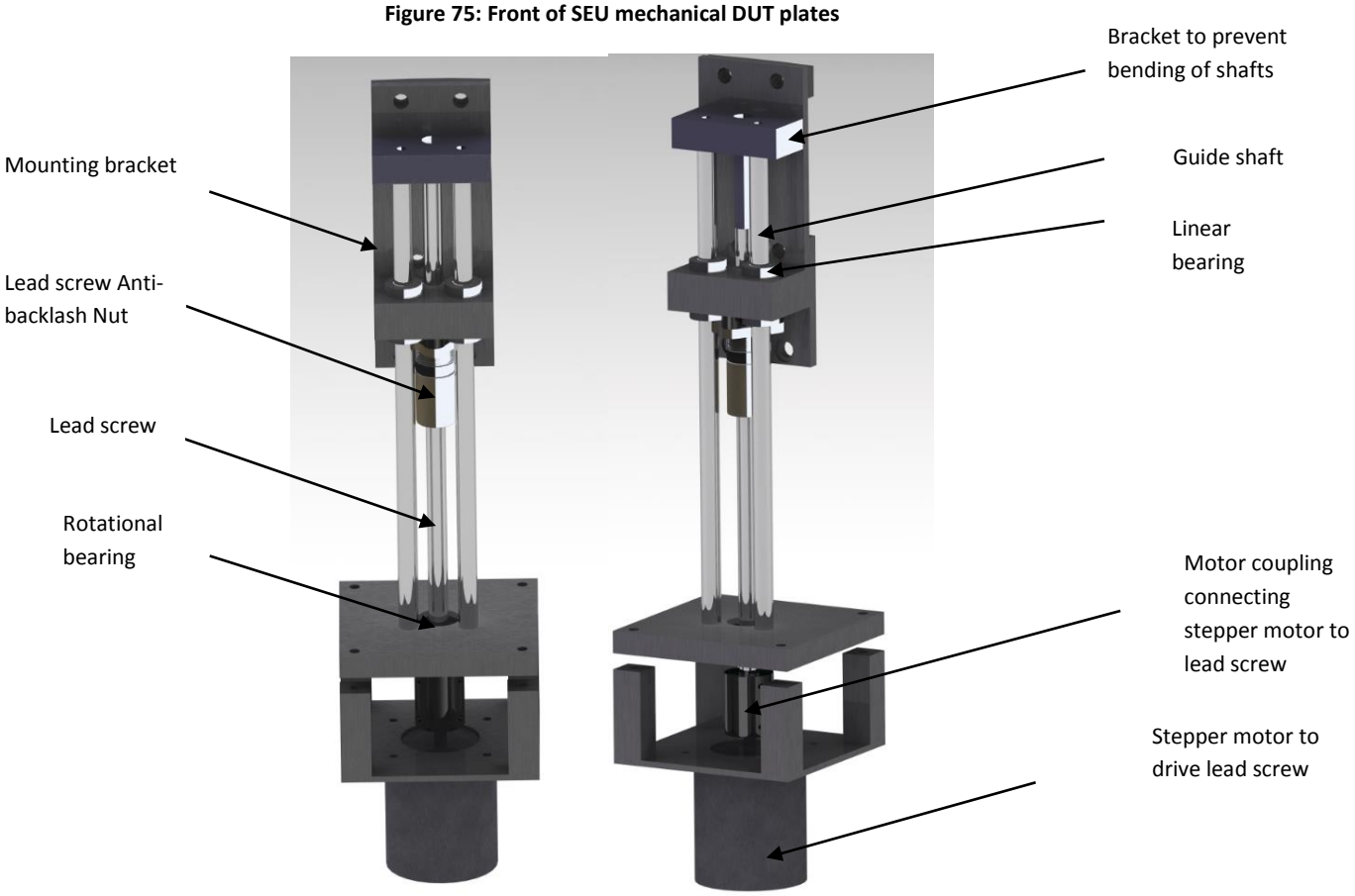

Figure 76: Lead screw assembly

The mechanical system was designed to be constructed from robust and long lasting materials, such as aluminium and stainless steel, which do not oxidise over time. This ensures that the system remains fully functional for the longest period of time. Figure 74 shows the rear of the DUT mounting plates, which are rotated by the stepper motor shown. The EK05 bearing housing and pivot pin

provide ease of rotation and support, such that there is no moment on the motor shaft due to the weight of the DUT and plate. Figure 76 shows the front of the DUT mounting plate where the test electronics are mounted. The mounting plates were manufactured from aluminium to ensure higher levels of scattering and secondary particles when the proton beam strikes the plate. Aluminium was chosen as the increase in scattering and secondary particles causes lower energy particles to interact with the FPGA, depositing more energy than the high level particles which pass through the chip. In addition to the above, aluminium is the material commonly used for satellite construction and shielding.

The lead screw assembly, seen in Figure 76 and 77, provides the vertical movement of the system. The lead screw is driven via a motor coupling connected to a stepper motor. Rotation of the lead screw is assisted by the use of a bearing shown in Figure 77. Rotating the lead screw adjusts the position of the lead screw nut which in turn vertically adjusts the position of the mechanical structure holding the test boards. The lead screws are each guided by two guide shafts which prevent a moment occurring on the screw and stabilises the mechanical system in all axes. Smooth motion of the guide shafts are ensured by including linear bearings. A final bracket seen, in Figure 65, ensures that the guide shafts and the lead screw are held in position, allowing only vertical motion of the curved plate housing the test boards. All of the design files of the mechanical system can be found on the attached disk.

Since the purpose of the lead screws are to carry the weight of the upper section of the platform and allowing for the adjustment of the vertical position of the test boards, the specifications of the lead screw, together with the driving stepper motor, were required to be accurately determined with the use of the following equations [101].

Percentage of surface contact required:

$$A_e = \frac{F_{axial}}{P_{zul}[mm^2]} = \frac{45N}{35\ MPa} = 1.2857 \times 10^{-6}\ m^2$$

Equation 7

The actual contact surface area of 563 X10^{-6} m^2 is more than sufficient for safe operation.

Selection of thread size and determination of actual surface pressure:

$$P_{real} = \frac{F_{axial}}{A_e\ real\ [MPa]} = \frac{45N}{563 \times 10^{-6}} = 0.07993\ MPa$$

Equation 8

Pv-Value:

$$pv = p_{real} \cdot v = 0.34$$

Equation 9

Surface speed:

$$v = \frac{n \cdot d1 \cdot \pi}{60\,000[\frac{m}{s}]} = \frac{3 \times 0.01 \times \pi}{60000} = 1.571 \times 10^{-6} m/s$$

Equation 10

RPM:

$$n = \frac{v \cdot 1000 \cdot 60}{\pi \cdot d1\,[\frac{1}{min}]}$$

Equation 11

Feed rate:

$$s = \frac{n \cdot p}{60000[\frac{m}{s}]} = \frac{3 \times 0.012}{60\,000} = 600 \times 10^{-9} m/s$$

Equation 12

Drive Torque:

$$M_{ta} = \frac{F_{axial} \cdot p}{2000 \cdot \pi} = \frac{45N \times 0.012}{2000 \times \pi} = 8.594 \times 10^{-5} Nm$$

Equation 13

$$M_{te} = \frac{F_{axial} \cdot p \cdot \eta}{2000 \cdot \pi} = \frac{45N \times 0.012 \times 0.8}{2000\pi} = 6.875 \times 10^{-5} Nm$$

Equation 14

Where:

P_{zul} -is the maximum permitted surface pressure

$A_e\ real$ - is the percentage of surface contact area of the trapezoidal lead screw nut

p -is the lead

M_{ta} -is the drive torque (Nm) when converting rotating motion to linear motion

M_{te} -is the drive torque (Nm) when converting linear motion to rotating motion

v -is the surface speed (m/s)

s -is the feed rate (m/s)

n -is the RPM (min^-1)

η - is the efficiency

The FL57ST56-0606A stepper motor was chosen to drive the lead screw system. This motor produces a holding torque of 0.59Nm, exceeding the required driving torque. The 12V 0.6A bipolar motor provides a high driving torque at an accurate 200 steps per revolution.

Table 5: Material specifications [101, 105]

iglidur® J - Material data

Materials table

Genera l features	Unit	iglidur® J	test method
Density	g/cm³	1,49	
Colour		yellow	
Max. humidity absorption at 23°C/50% R. H.	% weight	0,3	DIN 53495
Max. water absorption	% weight	1,3	
Coefficient of surface friction, dynamic, against steel	µ	0,06 - 0,18	
pv values (dry)	MPa x m/s	0,34	
Mechanical properties			
Bending E-module	MPa	2.400	DIN 53457
Tensile strength at +20 °C	MPa	73	DIN 53452
compressive strength	MPa	60	
Maximum recommended surface pressure (20° C)	MPa	35	
Shore D-hardness		74	DIN 53505
Physical and thermal properties			
Max. long term application temperature	°C	+90	
Max. short term application temperature	°C	+120	
Minimum application temperature	°C	-50	
thermal / heat conductivity	[W/m x K]	0,25	ASTM C 177
Coefficient of thermal expansion (at 23° C)	[K-1 x 10-5]	10	DIN 53752
Electrical properties			
Specific forward resistance	Ωcm	> 10^{13}	DIN IEC 93
surface resistance	Ω	> 10^{12}	DIN 53482

iglidur®-Material	Surface pressure
iglidur® J	4 MPa
iglidur® W300	5 MPa
iglidur® A180	3.5 MPa
iglidur® J350	2 MPa

Table 01: Permitted continuous surface pressure in the threads

Further mechanical analysis was performed on all components supporting critical sections of the mechanical system and experiencing high levels of stress due to loading. Displacement, principle and von Mises stress analysis was performed using CATIA V5 software to provide accurate computer generated calculations based on the material specified for each component and user inputted forces and moments acting upon the test component. The resulting analysis gives an accurate indication of how the component will function under the influence of the applied forces and moments.

Figure 77 illustrates the centre of gravity for the mechanical system above the rotating disk. The weight and distribution of weight of this section of the system will determine the forces acting on the supporting components which require analysis.

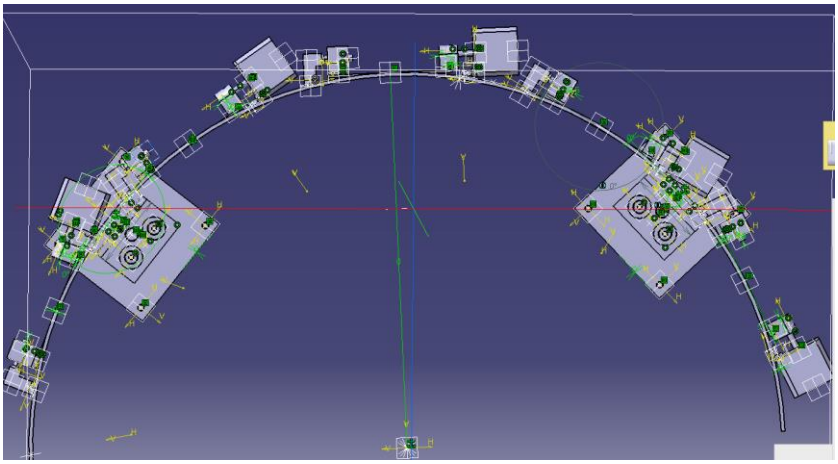

Figure 77: Centre of gravity

The analysis of the lead screw nut, which supports the weight of the entire mounting section of the mechanical design, can be seen in Figures 65 and 66.

The input force used to calculate the displacement and stress analysis of the nut was chosen to be the half of the total weight of the components which it supports, multiplied by a safety factor of 2. The resulting maximum displacement of the nut can be seen to be 0.0134 mm, which will result in perfectly safe operation of the nut. From Table 5 [103] the specified maximum surface pressure for the material of the nut is 4MPa and the calculated maximum resulting principle stress calculated is 0.649MPa as seen in Figures 78 and 79.

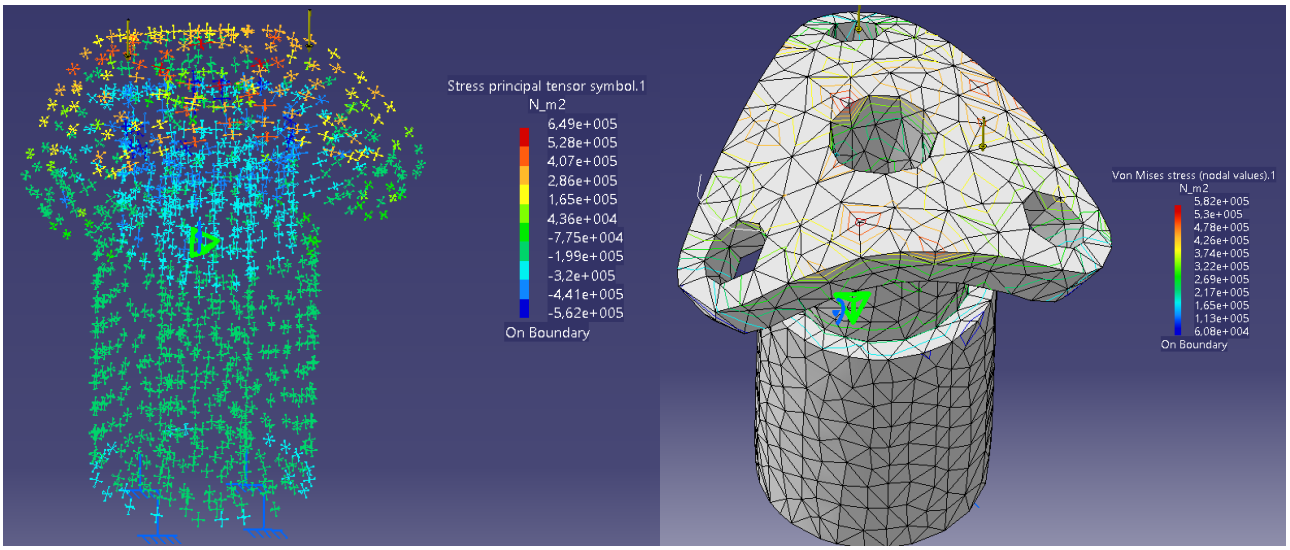

Figure 78: Lead screw nut analysis

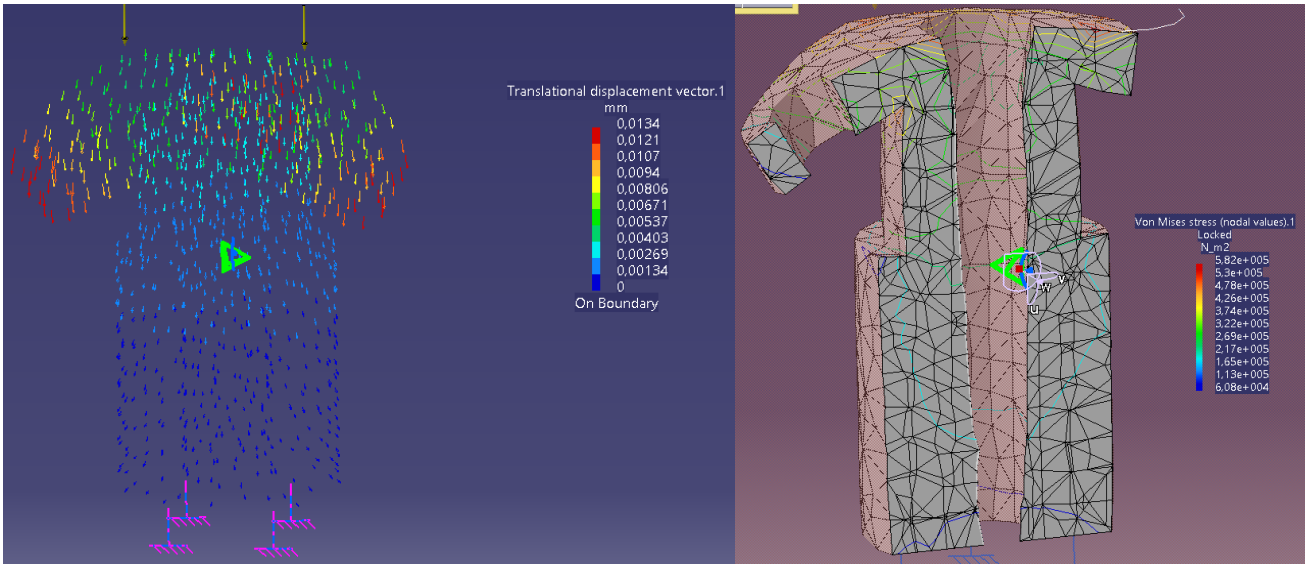

Figure 79: Lead screw nut analysis

The stress and displacement analysis of the bolt experiencing the highest moment due to the weight of the mechanical system can be seen in Figures 80 and 81. This analysis was based on the force acting upon the bolt head in the direction of the centre of gravity of the mechanical structure. The force used in the analysis was the weight of the entire mechanical system (if all 7 supporting bolts had to be removed). The maximum resulting displacement can be seen to be $5.24X10^{-5}$ mm and the maximum stress 3.14MPa. Both of these values are within the safety limit for the stainless steel material used in the construction of the bolt, resulting in a yield stress of between 280 and 700MPa.

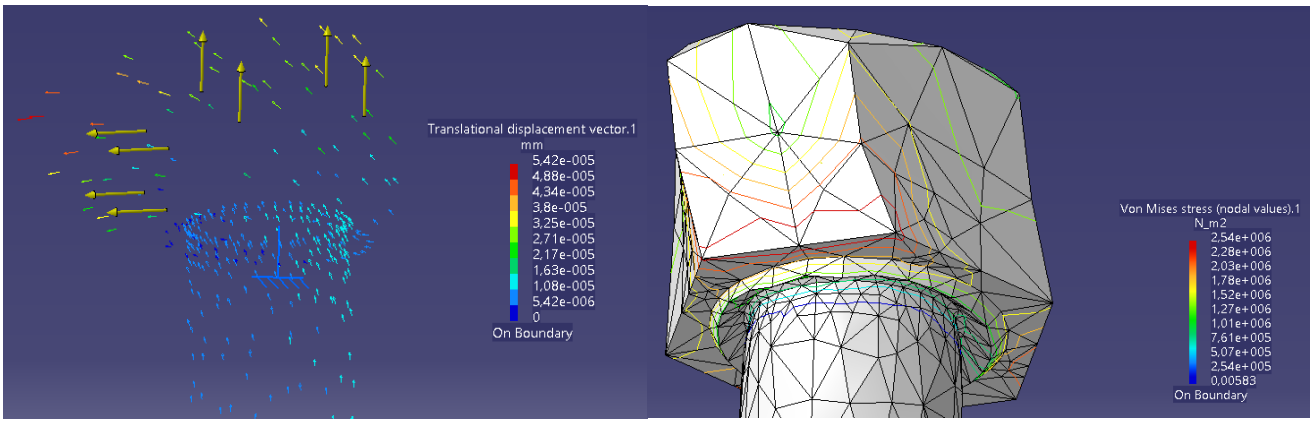

Figure 80: Bolt head analysis

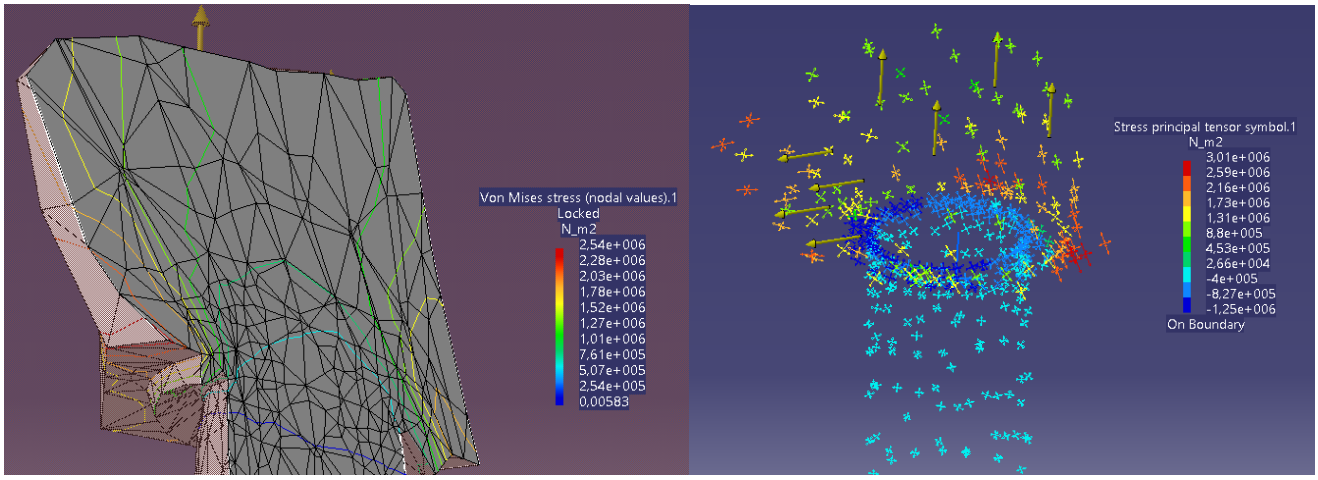

Figure 81: Bolt head analysis

Figures 82 and 83 illustrate the stress analysis of a moment of 10Nm acting upon the bolt head, together with a force of the weight of the whole mechanical system (43N) acting upon the bolt head. Higher stress and displacement values were calculated than in the analysis before, however, the maximum calculated stress of 267MPa with an included safety factor is still less than the yield stress of stainless steel.

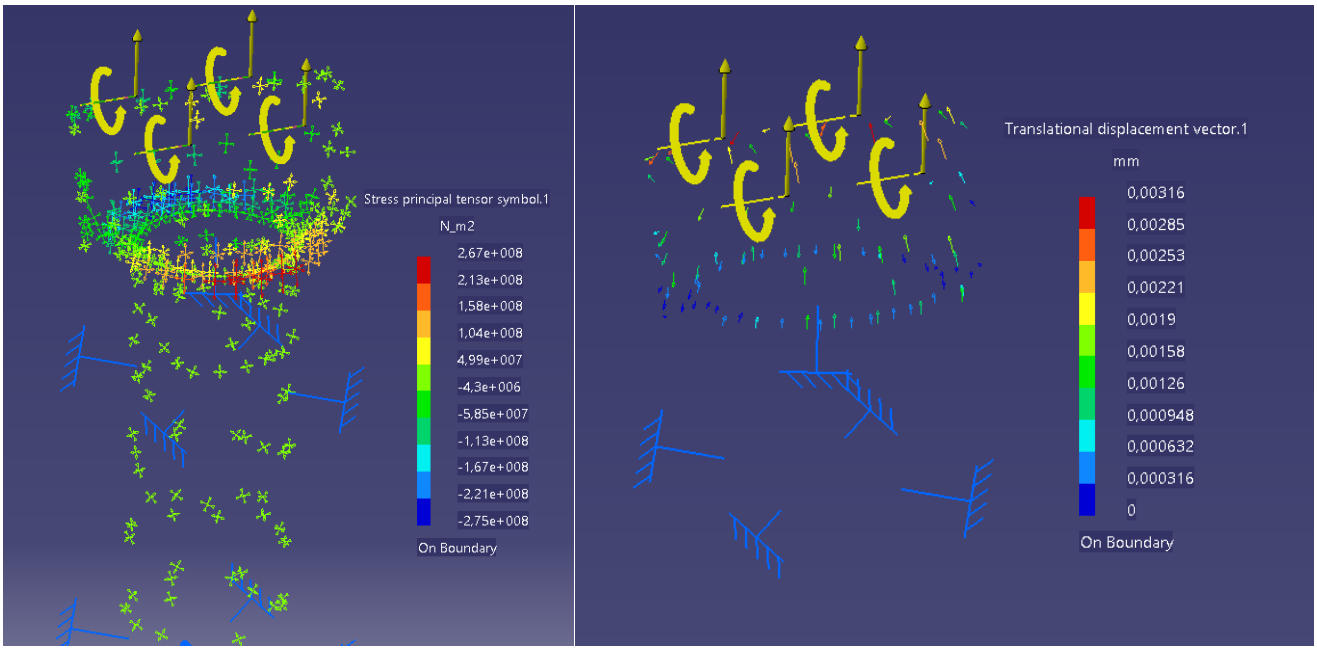

Figure 82: Bolt head analysis

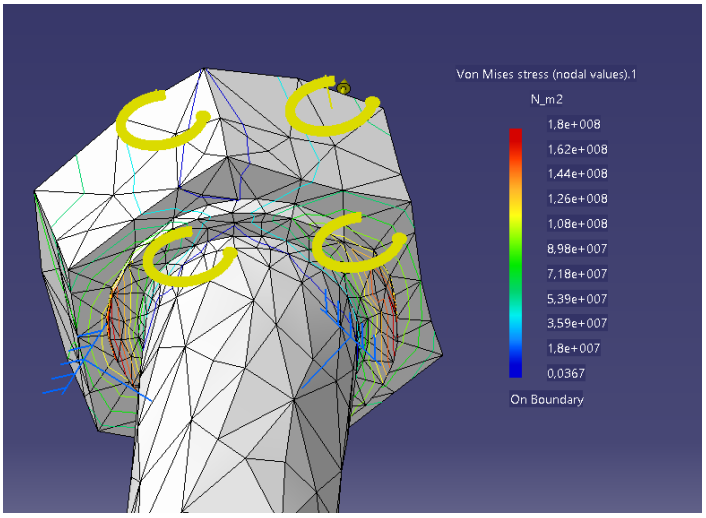

Figure 83: Bolt head analysis

Figures 84 and 85 illustrates the displacement and stress analysis of the guide shafts supporting the lead screw. The guide shafts are responsible for ensuring that no moment is exerted on the lead screw due to the centre of gravity of the system. The guide shaft is fixed at the bottom and top with a moment acting upon the shaft at the position of the linear bearings. The worst case stresses will be present when the resulting moment and forces are acting upon the centre of the shaft. Figure 86 illustrates the resulting stress analysis of applying a moment of 15Nm (weight of system multiplied by distance to centroid) to the centre of the shaft. The maximum resulting displacement was calculated to be 0.0242 mm and the stress was 6.76MPa. The stress is far below the minimum yield stress of 280MPa of stales steel.

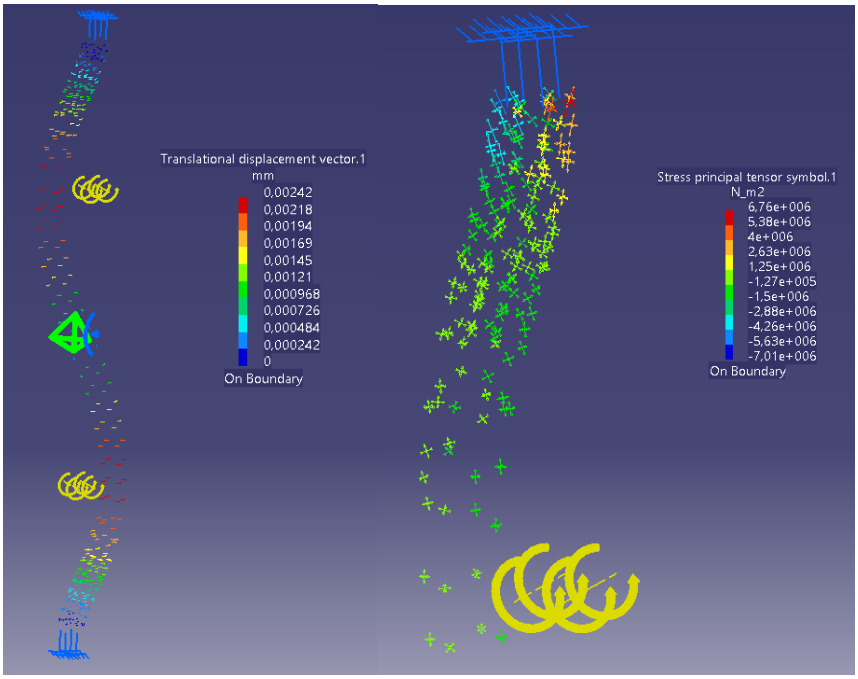

Figure 84: Guide shaft analysis

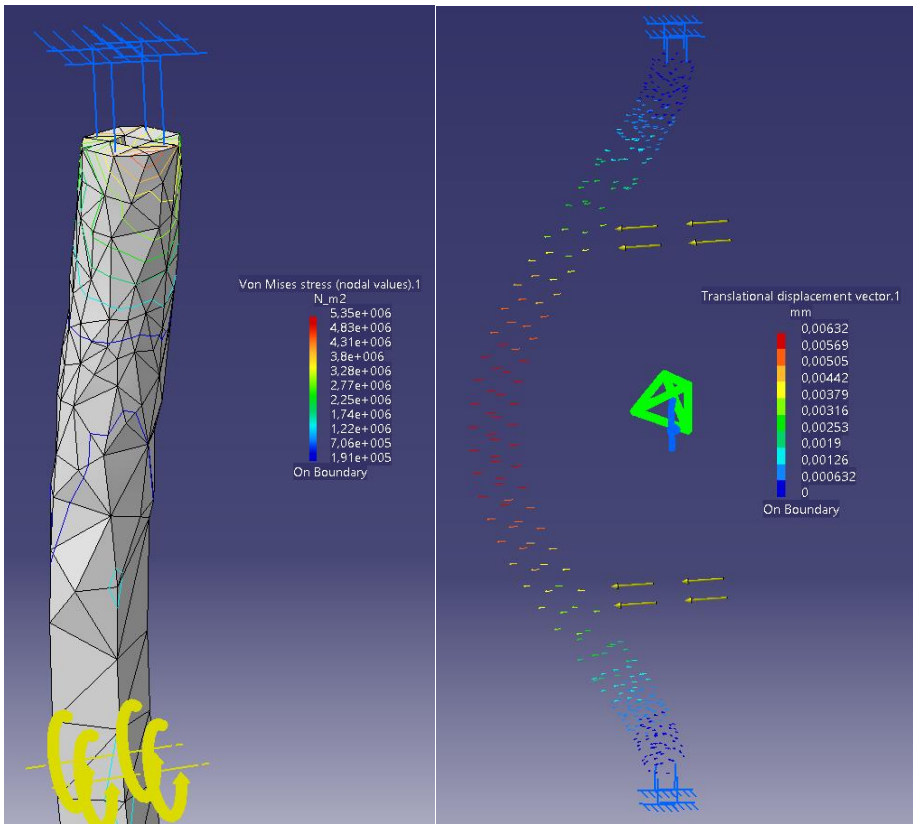

Figure 85: Guide shaft analysis

Figures 86 and 87 show the resulting stress and displacement results of applying a force equal to the weight of the system to the shaft. The resulting stress can be seen to be greatly less than the yield stress of stainless steel.

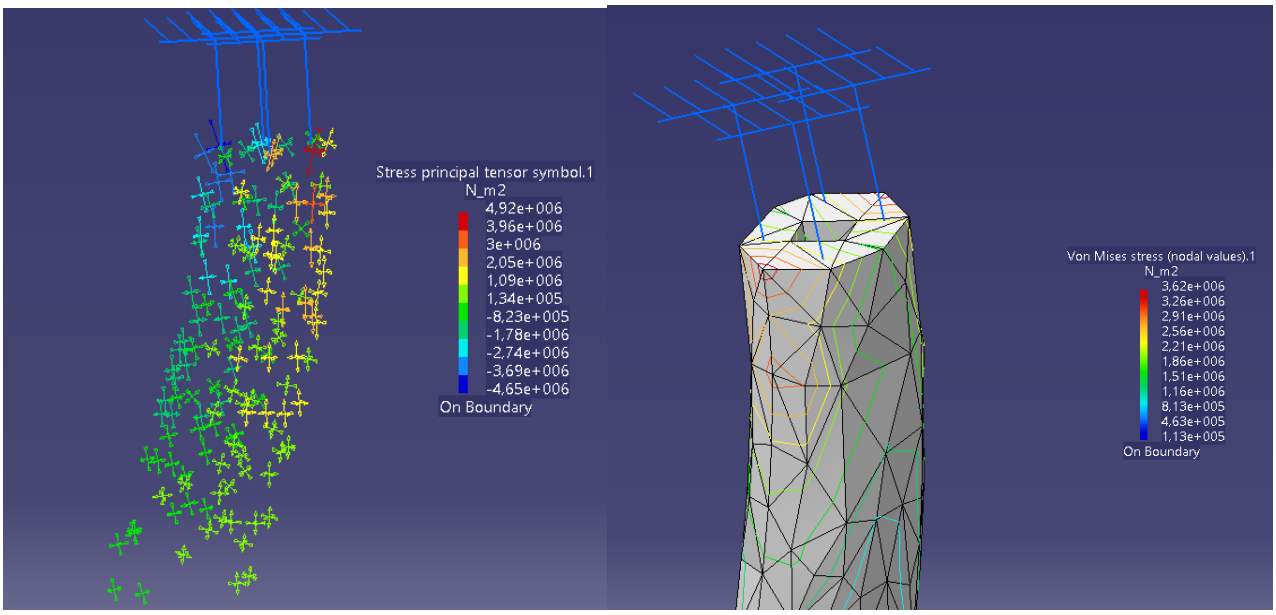

Figure 86: Guide shaft analysis

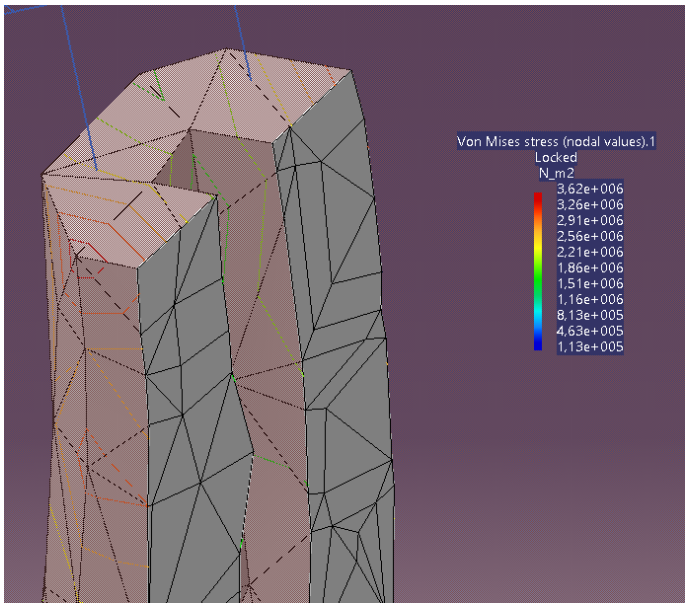

Figure 87: Guide shaft analysis

The motor required for the rotation of the test boards were required to be as small as possible and output enough torque on the output shaft to rotate the test board and mounting plate. The required torque was calculated was found to be 0.026Nm.

$$Torque = Force \times Distance = 2N \times 0.013m = 0.026Nm$$

Equation 15

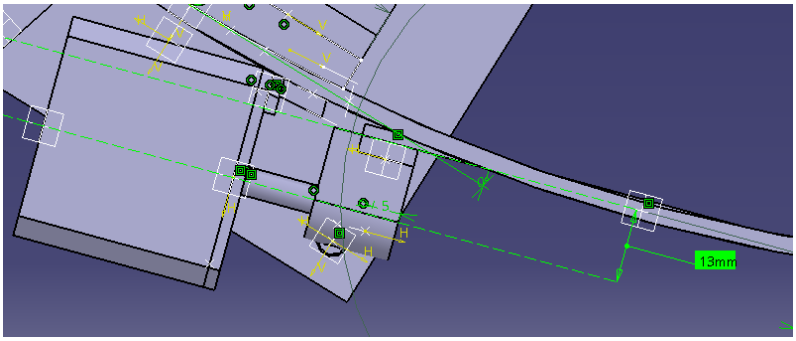

Figure 88: Mounting plate torque

The FL39ST34-0404B stepper motor was chosen to rotate the mounting boards. The 12V 0.4A motor produces an output torque of 0.21Nm with an accuracy of 200 steps per revolution. These motors will provide a highly accurate solution to adjust the angle of incidence of the test boards.

4.6.3 Control

The control of the system designed, includes the vertical height adjustment of the test boards and the angle of incidence of each of the test boards. The vertical adjustment of the system allows for multiple devices on a single test board to be irradiated and controlled by two lead screws driven by two stepper motors. These stepper motors were controlled by the LabVIEW software on the computer which sends signals to the DAQ card. The DAQ card turn sends the signals to the LM298 H-Bridge motor drivers which power the stepper motors. An open loop control system was implemented for the stepper motors, due to the high reliability and small step size of the motors. The control of the angle of incidence of the DUT mounting plates was able adjusted with the use of smaller stepper motors. The motors was powered and controller in the same manner as those described above. All of the LabVIEW monitoring and mechanical control program files written can be found on the attached disk.

Figure 89 shows the LabVIEW designed interface of the system. The angle of incidence of each DUT is able to be adjusted while the current angle is displayed in real time. The vertical height of the system

is able to be imputed while the current position is displayed. Emergency stop buttons are implemented into the design and physically on the system.

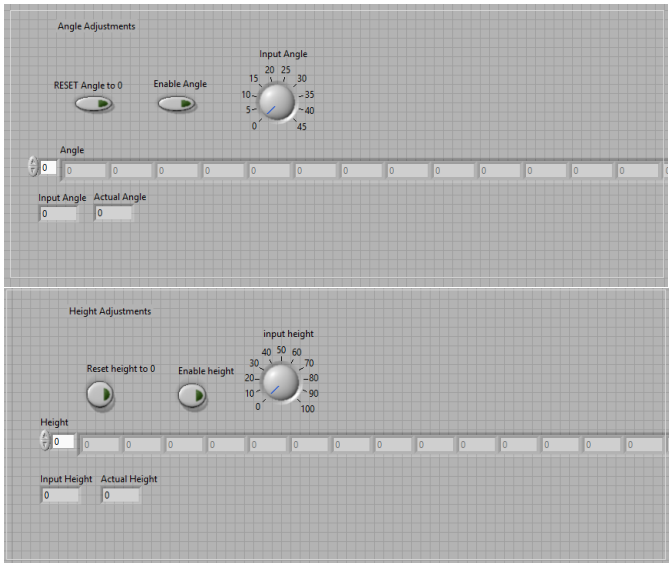

Figure 89: LabVIEW interface for angle of incidence and height control

Figure 90 shows the LabVIEW code implemented to adjust the height of the mounting plates. The code for adjusting the angle of incidence and all other cases to those shown in Figure 90 can be found on the attached disk.

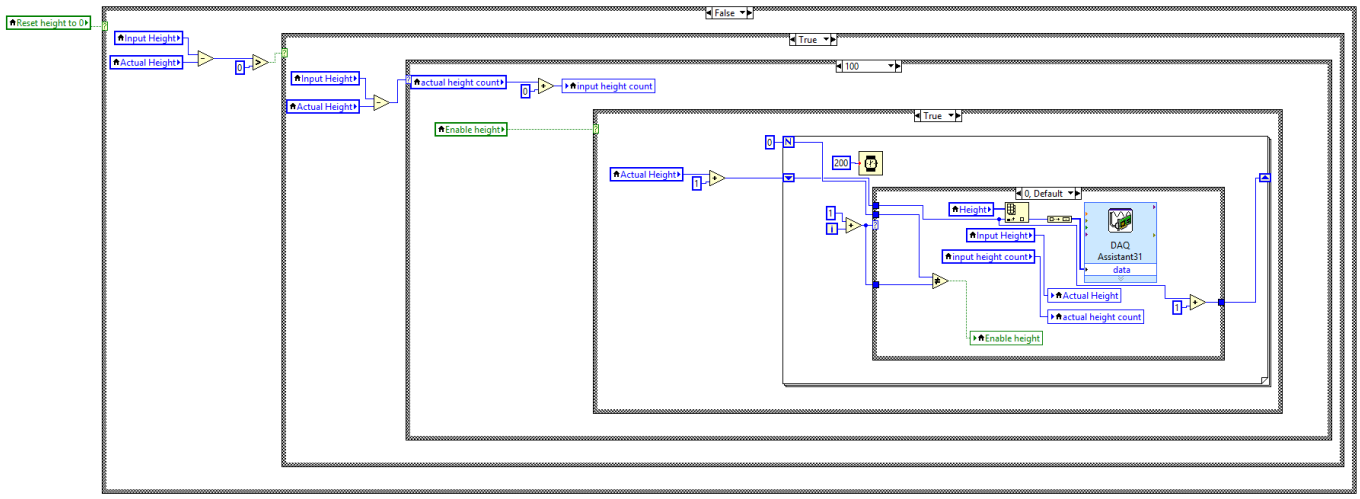

Figure 90: LabVIEW code for motor control for height

4.6.4 Electrical Design

The electrical design of the SEU testing set-up includes the wiring of all of the connections between the A3P1000 test board, Xilinx Xup2, NI DAQs, motors and motor drivers and additional components.

A PCB board seen in Figure 91, was designed to be used during both the TID and SEU testing. Unfortunately, due to the limited number of IO pins available connecting the inside and outside of the vacuum chamber, no control of the mechanical system would be possible. This limits the number of boards able to be irradiated during testing. In addition to this, the A3P1000 socket was not readily available to implement on the PCB design. Without a socket, the entire PCB would have to be discarded after each test when the FPGA failed. The use of a development board with the socket was found to be the more viable option, as this allowed the FPGA chip to be interchangeably replaced.

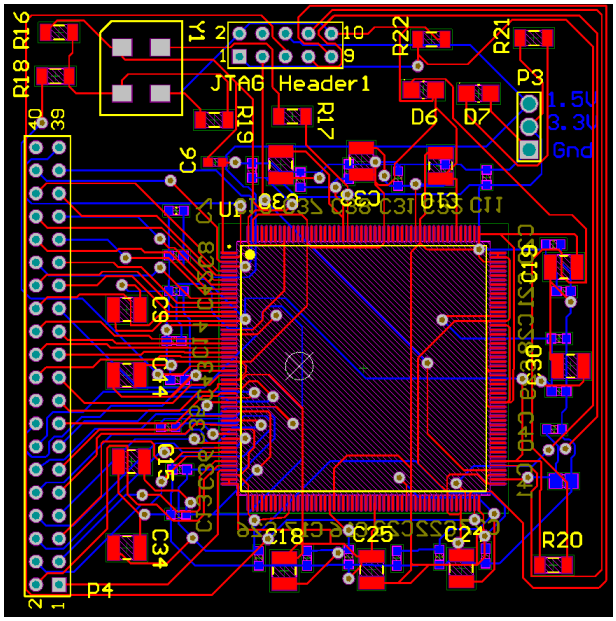

Figure 91: Designed PCB intended to test

4.6.5 Test Procedure

The initial set-up, before the testing procedure could commence, involved the installation of the mechanical system inside the vacuum chamber, the installation of the test and control board as well as the wiring of these boards, all inside of the chamber. The DAQ and motor drivers were then set up on the outside of the chamber and connections between the inside and outside of the chamber were formed. Once all of the electrical and mechanical components were in place, an open position out of the line of site of the beam, and closed position in the beam's path was determined.

The test procedure for the SEU testing involved the following steps:

- Test board moved to the open position
- The beam was tested on the viewer in the chamber to be calibrated and to determine the spread of the beam.
- The beam was redirected and the test board moved to the closed position
- Irradiation of the test board commenced for a specific period of time while monitoring the outputs from the control board to the DAQ
- After a set period of time, the beam was redirected away

The last two steps were repeated for each test run to be completed.

4.6.6 Data Analysis

The data analysis of the SEU testing consisted of recording the number of SEUs detected on the outputs of the various implemented circuits. Further analysis of this data could predict the characteristics of the circuits when exposed to varying levels of proton energies. The first part of the data analysis included graphically plotting the number of SEUs which were detected for each circuit over the test duration. This provided an indication of the SEU rate which the circuit experienced for a given time period during the tests. Using the total number of SEUs which have been detected for each circuit, the circuit information and the Bendel 1 parameter equation, the SEU cross section per bit (cm^2/bit) was determined for each of the implemented circuits [104].

$$s = \left(\frac{24}{A}\right)^{14} \left(1 - e^{-0.18Y^{0.5}}\right)^4$$

Equation 16

Where $Y = \left(\frac{18}{A}\right)^{0.5} [E - A]$ and E and A are energies in MeV.

Initial solving of the value "A" was completed to allow for the graphical plotting of the SEU cross section per bit for any desired proton energy. The Bendel 1 parameter equation is not commonly used in modern SEU analysis, as a more accurate analysis is possible with the use of the Bendel 2 parameter equation. However, analysis using the Bendel 2 parameter equation was not possible as only one test energy was available.

4.7 Testing Installation

Figure 92 shows the MicroSemi ProASIC3 A3P1000 FPGA and development board used as the test board during the experiment. Figure 93 shows the Xilinx XUP2 development board with the Virtex 2 Pro FPGA used as the control and monitoring board during the experiment.

Figure 92: MicroSemi ProASIC3 A3P1000 chip and development board

Figure 93: XIlinx Xup2 development board

4.7.1 Total Ionizing Dose

The total ionizing dose set up required no mechanical fixtures, as required for the SEU testing. The test board was required to be placed at a position within the facility such that the Co-60 source had a clear line of sight to the FPGA. The remaining monitoring equipment, such as the Xilinx monitoring board and NI DAQ cards, was required to be placed within 2 meters of the test FPGA to reduce noise in the cabling which would be misinterpreted as errors in the output signals. The monitoring equipment was protected from the source by the inclusion of lead blocks, which prevents errors in or damage to the monitoring equipment. The remaining installation involved the installation of an Ethernet cable from the inside of the test room to the outside where the laptop was placed.

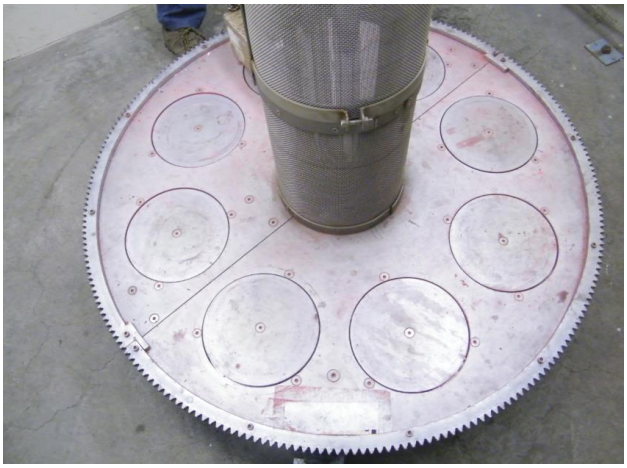

Figure 94: FruitFly Africa Co-60 source

Figure 95: TID pre testing set up.

4.7.2 Single Event Upset

The single event upset testing required a more complex mechanical and electrical set up, due to the nature of the testing and facility. The testing facility at the iTemba LABS enables high energy proton testing in the A-line scattering chamber. The mechanical structure of the scattering chamber, where the beam exits the guiding section and enters the testing environment, was designed in such a manner that the beam requires constant vacuum. This requires the test components to be placed within a vacuum chamber in order to be irradiated. This resulted in a number of limitations to the test set up to be overcome. The first task included the design and construction of a mechanical

platform which would allow for the mounting of the test FPGA. It was decided to design a system which would allow for multiple test boards of any nature to be mounted at a single time as well as adjusting the vertical position and angle of incidence of the board. The mechanical platform is not only designed for the purposes of this experiment, but rather for the future tests to be conducted by any researchers interested in conducting experiments at the facility.

The electrical set up at the testing facility involved the electrical wiring between the test and monitoring board in the chamber as well as allowing a connection between the inside and outside of the chamber without affecting the vacuum.

Figure 96: A-Line scattering chamber

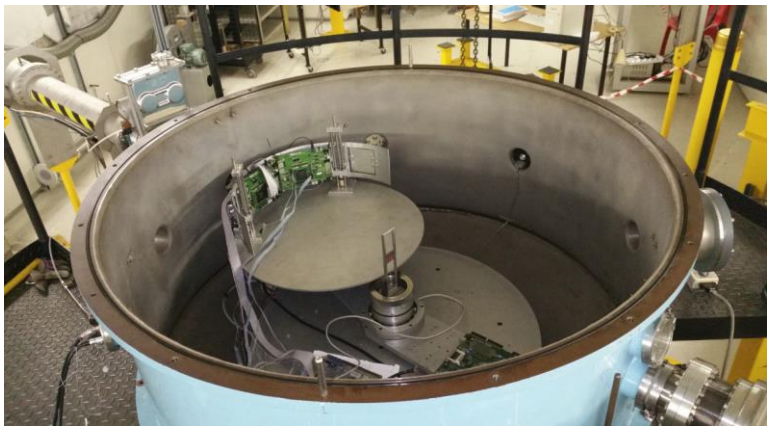

Figure 97: Vacuum chamber with test equipment installed

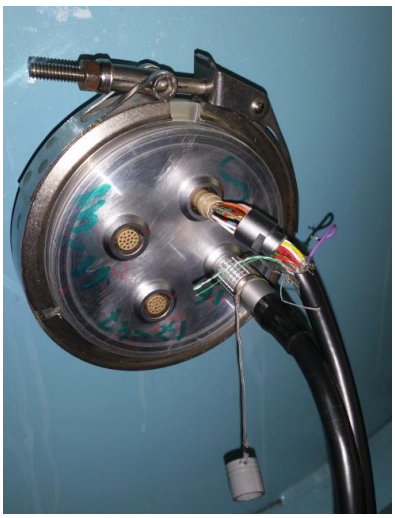

Figure 98: FGG.2B.319 male vacuum connectors

Figure 99: FGJ.2B.319 female vacuum connectors

Figure 100 :A3P1000 test board and Xilinx control board in chamber

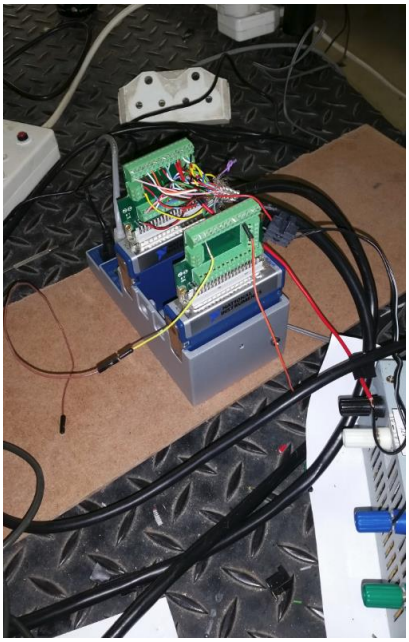

Figure 101: NI DAQ and chassis

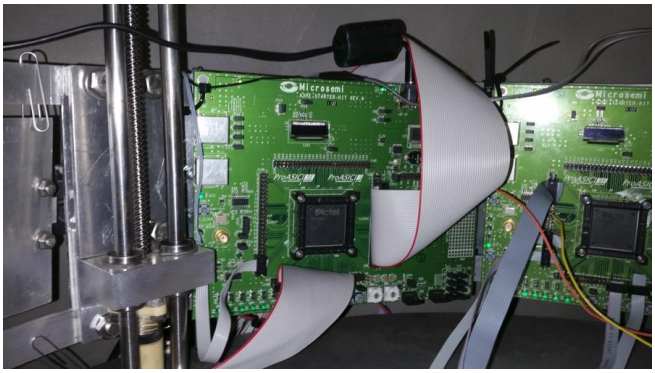

Figure 102: A3P1000 test board

Figure 103: Control room at iTemba LABS facility

Figure 104: Image of proton beam striking the viewer

Figure 105: SEU mechanical fixture

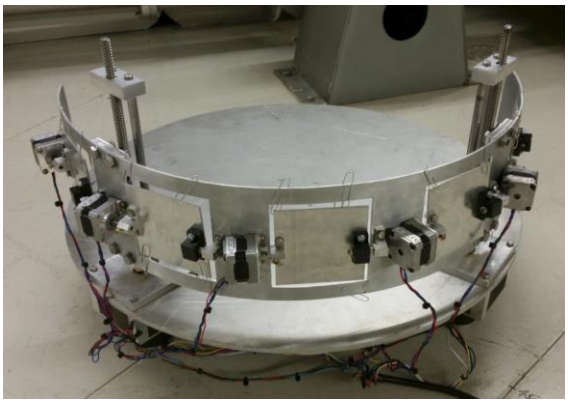

Figure 106: SEU mechanical fixture

Figure 107: Rotating motor and gearbox

4.8 Decapsulation

Decapulation of the A3P1000 FPGA was performed to allow the measuring of the size of the actual Die. Decapsulation was performed by carful removal of the outer casing with the use of a high speed rotary tool. The die size of the A3P1000 PQ208 was found to be 6mm by 6mm. This measurement of the die was used when calculating the number of protons interacting with the die during testing. Figure 108 illustrates the decapsulated A3P1000 FPGA, exposing the die.

Figure 108: ProASIC A3P1000 PQ208 FPGA with exposed die

5 Experimental Results and Discussion

5.1 Single Event Upset

During the first SEU test, the test board was irradiated by a proton beam with energy of 66MeV and current of 2nA as well as 3nA. During this initial test, no SEUs were detected in any of the circuitry. By moving the “viewer” or “ruby” into the path of the proton beam, the particles depositing energy in the chip resulted in SEUs occurring.

The reason for only detecting SEUs when the viewer was placed in the path of the beam can be explained by considering the interactions of the proton beam with the Al_2O_3 material of the viewer. The die material of the A3P1000 is not thick enough to stop or slow down the protons enough, allowing the depositing of sufficient energy to induce SEUs. The amount of energy deposited in the target material, in this case the chip, increases as energy decreases. Placing the viewer in the path of the beam reduces the energy of the beam, resulting in more energy being deposited in the chip. Additionally, neutrons, deuterons, tritons, alphas, lower energy protons and gamma-rays are produced by the proton beam hitting the viewer, which results in a higher amount of energy being deposited in the chip. All of the SEU data and graphs can be found on the attached disk.

5.1.1 Test 1

The SEU testing conducted consisted of two test sessions. The first test conducted focused on the implementation of the servo motor, UART, SPI and I2C control circuits. The number of connections between the control board inside of the vacuum chamber and the DAQ on the outside was limited to only one FGG.2B.319 and FGJ.2B.319 connector pairs. This pair was to be shared between the testing conducted in this paper in addition to the testing conducted by another student conducting experiments. As a result, the first test would aim to determine the number of errors occurring in the four circuits as well as the number of errors occurring within the various sections of each circuit. All of the data from the test can be found on the attached disk.

Figure 109 shows the error rate for the various outputs of the implemented circuits for a 120 second test with beam energy of 66MeV and current of 2nA. The servo motor control circuit experienced only a single upset, possibly due to the low 200Hz frequency and simplicity of the circuitry. The MOSI

(SPI) circuits can be seen to have been minimally affected by SEUs as the only error occurring in this circuit was detected in the last 20 seconds of testing. This circuit performed well despite the complex circuitry, but the lower frequency resulted in fewer errors occurring in the frequency dependant combinational circuitry. The transmitting portion of the UART circuit (UART TXD) can be seen to have outputted no errors and thus not affected by SEUs during this test. This circuit experienced no as a result of the simple circuitry, despite having an output frequency of 2.5kHz. The UART receiver however circuit performed slightly worse than the transmitter during testing as it experienced a total of 5 SEUs. The higher number of upsets can be attributed to the increased circuit frequency of 6.25kHz.

The I2C and SPI clock signals experienced more errors than the circuits described before. The number of SPI clock errors can be explained by the complexity of the SPI circuit and high number of combination and memory elements, while the I2C error rate resulted due to the 4MHz output frequency and having a very small number of combinational and memory elements. The MISO (SPI) signal performed well up to approximately 90 seconds of testing, after which a larger number of output errors were counted. The high number of errors occurred due to the high 6.25kHz signal frequency and high number of combination and memory elements. The I2C data circuit experienced the overall highest error rate of the test duration with a total number of SEUs of 27 together with the MISO controller. The high number of I2C data upsets was not expected due to the small number of memory elements, however the output frequency of 400kHz did attribute to the upset rate. It can be noted that for each of the test circuits that SEUs were only detected after 30 seconds of testing and, with exception to the I2C data signal, follow a general trend of error rates as seen by the plot.

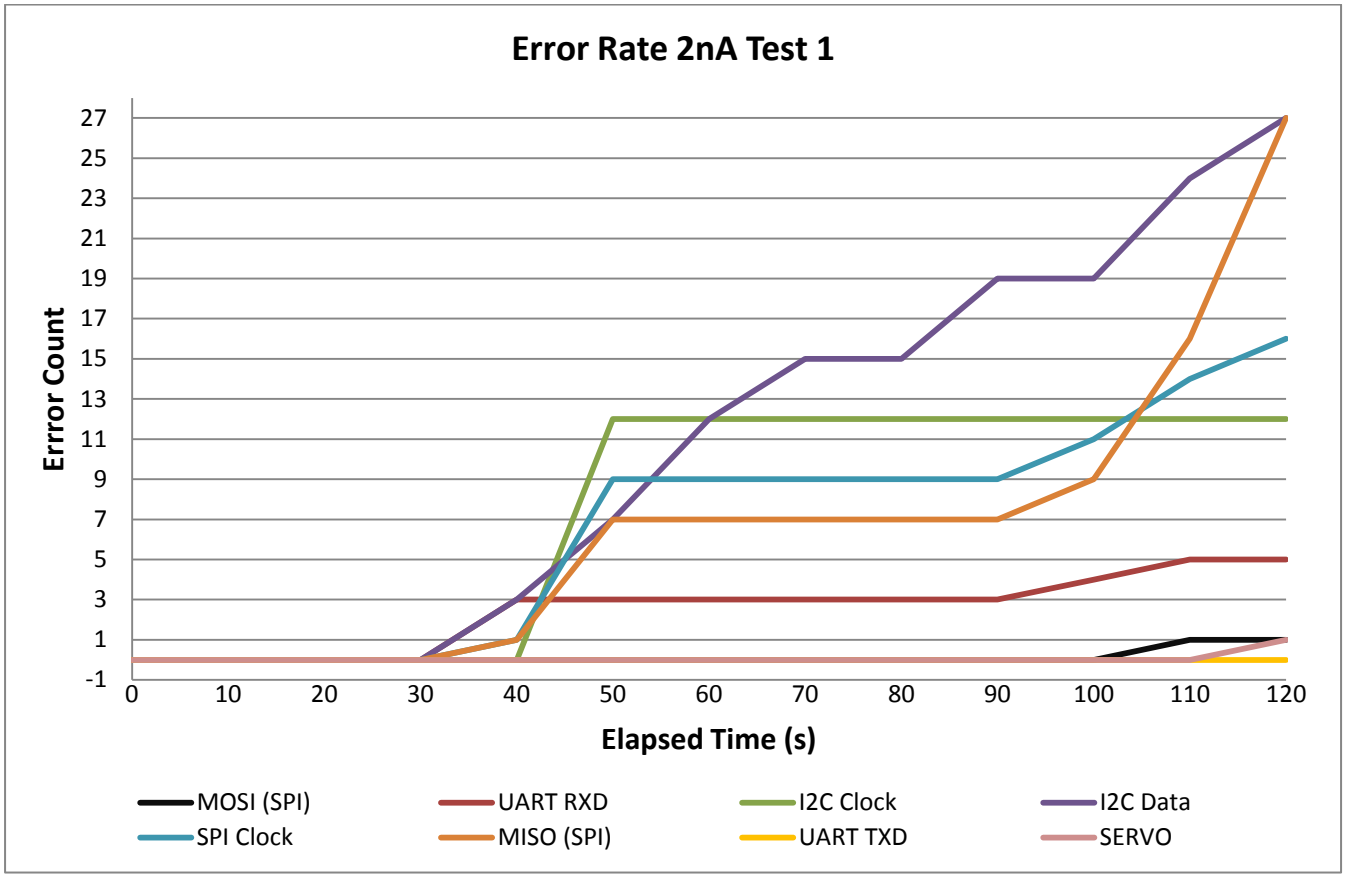

Figure 109: Test 1 error rate results at 2nA

Figure 110 illustrates the combined SEU rate for the implemented circuits. The servo motor control circuit performed the best overall with only a single SEU over the 120 second test period. This circuit also had the lowest frequency output, 200Hz, of all the circuits. The second least number of SEUs occurred in the UART circuit despite having a moderately high output frequency, with a total of only 5 SEUs over the test duration. The I2C and SPI circuits performed the least favourable, with 39 and 44 SEUs respectively. However a difference between the two be seen in the error rate of the I2C and SPI circuits, where the error rate of the I2C implementation appears to be larger over the whole test duration. The higher number of combinational and memory elements of the SPI implementation contributed to the higher number of upsets. The I2C circuit performed worse than was expected. Despite having a very small number of combinational and memory elements, the high very frequency output circuit experienced the second highest number of upsets.

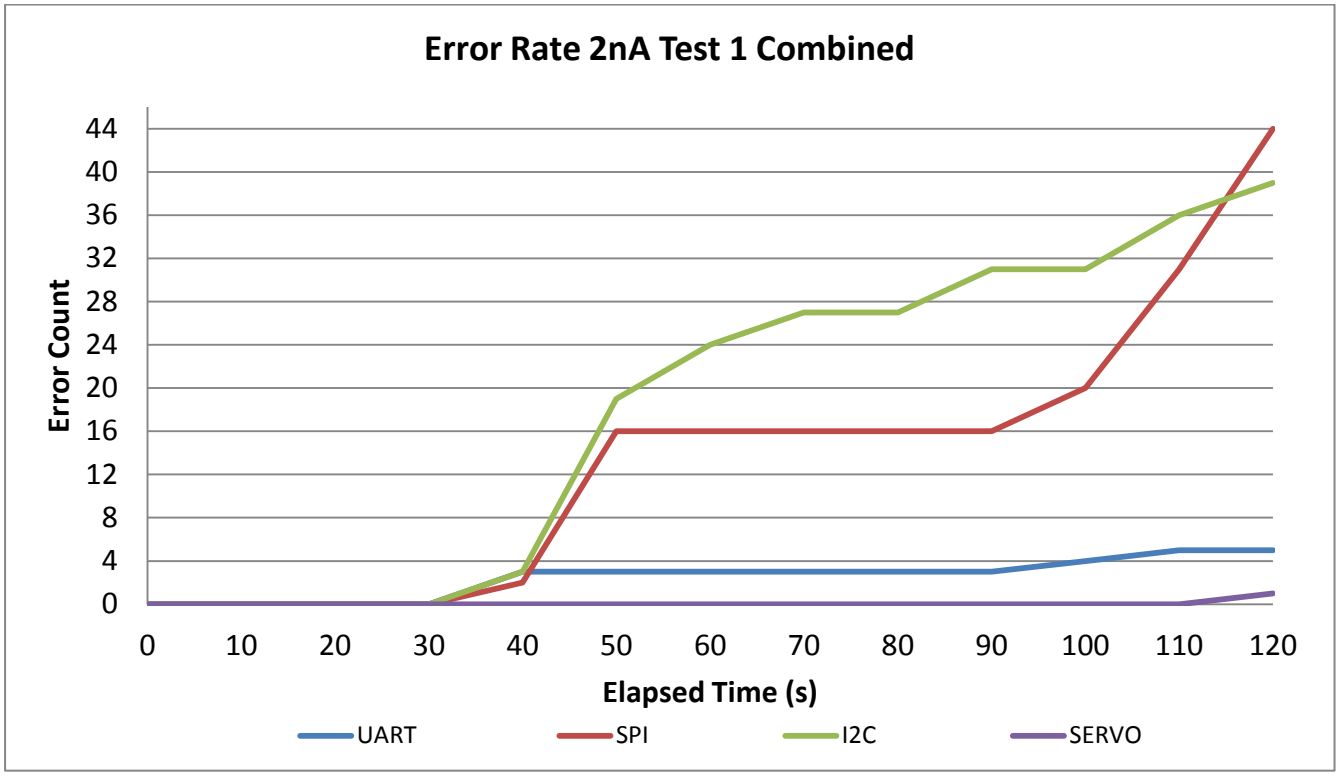

Figure 110: Test 1 combined error rate results at 2nA

Table 6 illustrates the characteristics of the test conducted with a beam energy of 66MeV and current of 2nA, including the flux, particles per time period and the number of protons striking the die area of the chip, assuming a uniform beam dispersion over the target area.

Table 6 : Beam and target parameters at 2nA

Time (s)	120
Current (A)	2×10^{-9}
Total number particle Flux (s^{-1})	1.2483×10^{10}
Total number particles in given seconds	1.49794×10^{12}
Beam area (cm^2)	3.14159
A3P1000 die area (cm^2)	0.36
Number of protons interacting with die	1.71651×10^{11}

The number of various memory elements (flip-flops) together with the number of combinational elements for each of the implemented circuits can be seen in Table 7. The total number of memory elements and the percentage of the total chip which the circuit comprises must be noted for the calculations to follow.

Table 7: Circuit mapping of A3P1000

Mitigation Technique	Total Core Cells	Combinational	DFN1E0	DFN1E1	DFN1	DFN0E0	DFN1C1	DFN1E1P1	DFN1P1	Percentage of Chip
UART	4829	3889	380	40	520	0	0	0	0	19.65
SPI	5106	3771	210	270	855	0	0	0	0	20.78
I2C	1579	1216	38	0	26	1	220	13	65	6.52
SERVO	4471	3211	60	720	480	0	0	0	0	18.19
Total	15985	12386	688	1030	1881	1	220	13	65	65.04

Table 8 shows the calculated proton fluence, a product of the protons striking the die and the percentage of the chip occupied by the circuit, for each circuit. The SEU cross section for each circuit is calculated by dividing the number of SEUs by the proton fluency for the circuit. The SEU cross section (cm^2/ bit) is in turn calculated by dividing the SEU cross section per circuit by the total number of memory elements. The SEU cross section per bit is then used in Equation 16 to solve for the Bendel 1 parameter values, from which a predicted cross section for each circuit can be plotted for a wide range of proton energies.

Table 8: Cross section results for implemented circuits at 2nA

Implemented Circuit	Proton fluence	SEU count	SEU cross section per circuit	SEU cross section (cm^2/bit)	Bendel Parameter A
UART	3.3728×10^{10}	5	1.4824×10^{-10}	1.5771×10^{-13}	24.3161
SPI	3.5663×10^{10}	44	1.2337×10^{-9}	9.2418×10^{-13}	21.6337
I2C	1.1029×10^{10}	39	3.5363×10^{-9}	9.7418×10^{-12}	18.4852
SERVO	3.1228×10^{10}	11	3.2023×10^{-11}	2.5415×10^{-14}	29.3976

Using the Bendel parameter calculated in Table 8, the SEU cross section per bit for any desired proton energy can be plotted, as seen in Figure 111. From Figure 111 it can be seen that the I2C has the highest SEU cross section per bit, resulting in the highest number of SEUs for any given proton energy. The very large SEU cross section in comparison to the other circuits is a result of the high number of upsets together with the small number of circuit elements. The SPI circuit performs the second worst, with close to 5×10^{-12} upsets per proton /cm^2 per bit for all proton energies, due to the high number of upsets. The UART and servo motor control performed well with a very small SEU cross section due to the small number of upsets and large number of circuit elements. The test results indicated that the I2C implementation would be the least reliable of the test circuits and

result in the highest number of SEUs for a proton strike of any energy. Each proton with an energy in excess of 50MeV would result in more than 5 $x10^{-12}$ SEUs in the I2C circuitry, whereas the number of SEUs in the other implementations would never exceed $4x10^{-12}$ SEUs per proton strike for any energy. The low frequency UART and servo circuits have a very low SEU cross section and would result in a minimal amount of SEUs in a space application. The Bendel plot provides an estimated performance characteristic for the implemented circuits.

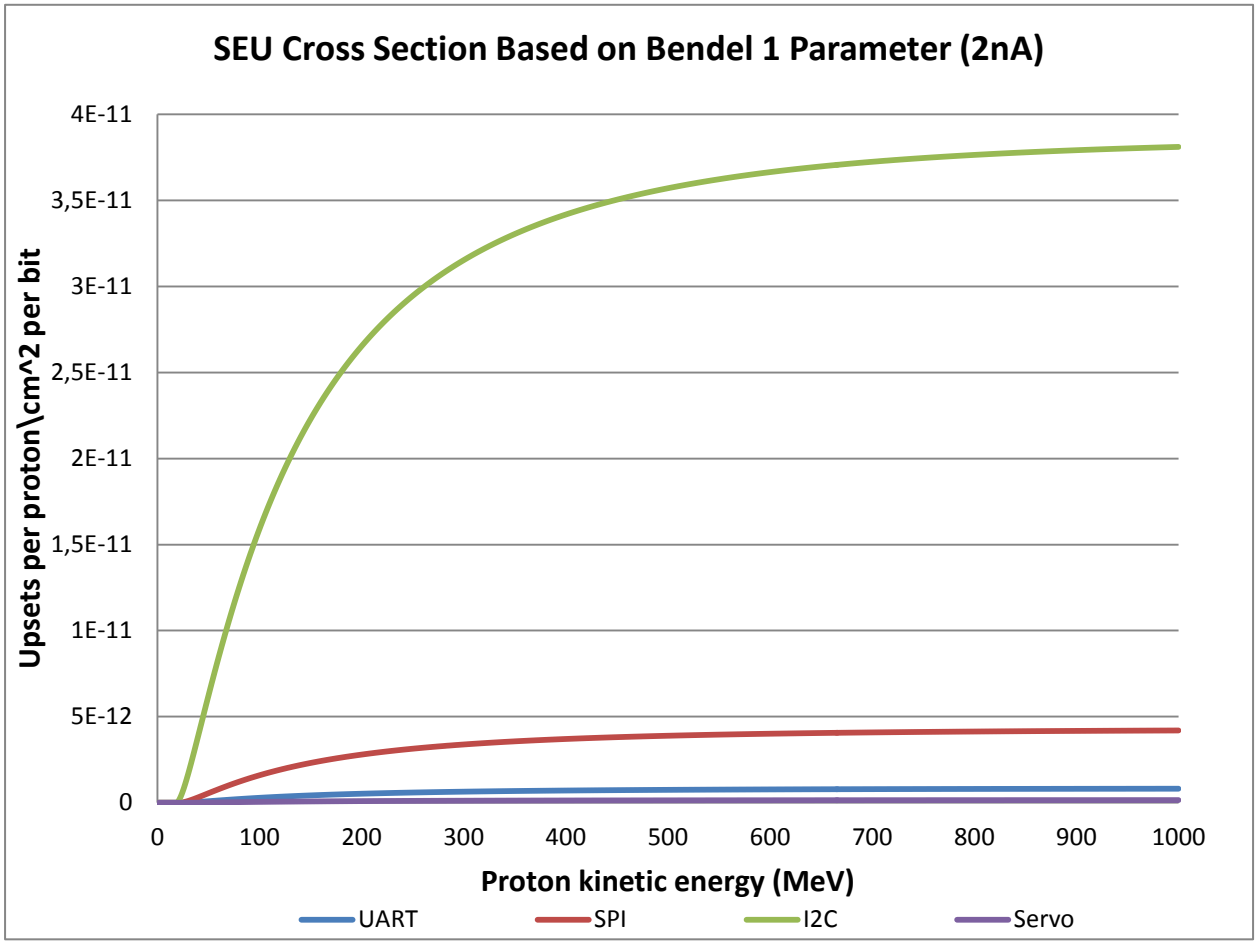

Figure 111: SEU cross section for test circuits at 2nA from, Bendel 1 parameter equation

Figure 112 shows the number of SEUs occurring during a 120 second test period, with a proton beam energy of 66MeV and current of 3nA. As in the previous test, the I2C data circuitry experienced the highest number of SEUs, at a similar SEU rate than before. The high upset rate can be attributed to the high 400kHz frequency output of the signal, despite the low number of circuit elements. The MISO (SPI) signal experienced the second highest number of SEUs for the duration of the second test

due to both the high number of circuit elements and moderate output frequency. The I2C clock and SPI clock signals experienced the same amount of errors at a similar error rate. Although the number of circuit elements for the I2C clock was substantially lower than that of the SPI clock circuit, the output frequency was very high in comparison. The remainder of the signals all experienced less than 10 SEUs during the test period. The UART RX signal experienced a slightly larger number of upsets when compared to the UART TX singal, due to the slightly higher output frequency of the circuit. The very low speed servo motor control circuit experienced only a small number of upsets together with the MOSI signal which performed the best. It can be noted how the circuits all experienced SEUs at similar times during the test period, due to high energy proton strikes. The increase in beam current resulted in an increased number of SEUs occurring in each of the circuits. This increased number of SEUs can be attributed to the increased number of high energy particle strikes as a direct result of the increased current.

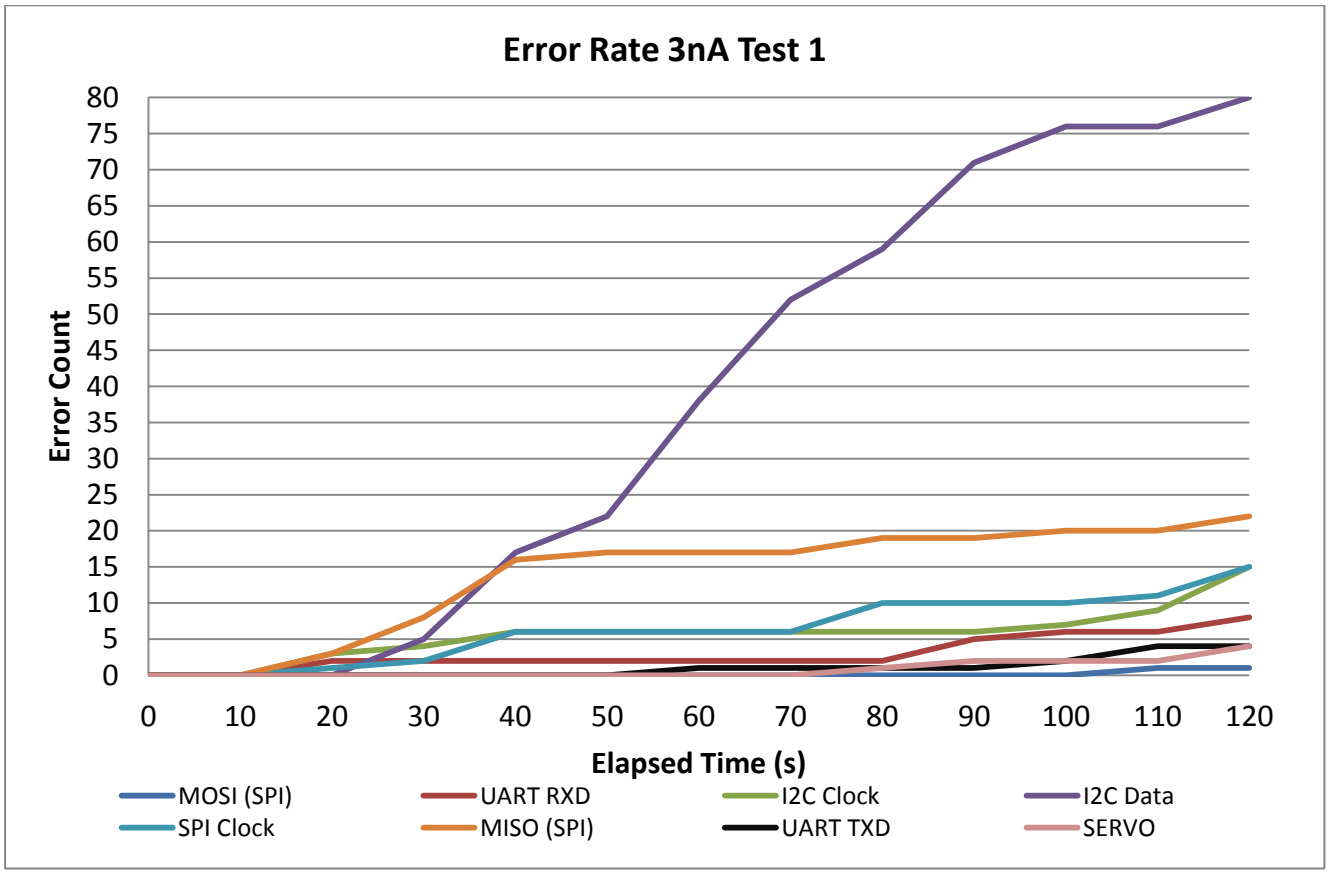

Figure 112: Test 1 error rate results 3nA

Figure 113 shows the total number of SEUs for each of the four implemented circuits. The I2C implementation can be seen to have the highest number of SEUs (95) followed by SPI (39). As with the previous test, the SPI and I2C circuits have very similar SEU rates, up until a period of approximately 40 to 50 seconds into the test. After this time the I2C error rate continues to increase at a higher rate due to the errors occurring in the I2C clock signal. The UART and servo circuits functioned well during irradiation and experienced only 11 and 4 SEUs respectively. Both the servo and UART circuits were very simple with moderately low output frequencies.

Figure 113: Test 1 error rate results combined 3nA

Table 9 illustrates the beam and test characteristics for the test conducted at 3nA The flux, number of particles and number of protons interacting with the die can be seen.

Table 9: Beam and target parameters at 3nA

Time	120
Current (A)	3×10^{-9}
Total number particle Flux (s^{-1})	1.8724×10^{10}
Total number particles in given seconds	2.2469×10^{12}

Beam area (cm^2)	3.14159
A3P1000 die area (cm^2)	0.36
Number of protons interacting with die	$2.5748 X10^{11}$

Table 10 illustrates the cross section calculation results for the implemented circuits.

Table 10: Cross section results for implemented circuits test 1 at 3nA

Mitigation Technique	Proton fluence	SEU count	SEU cross section per circuit	SEU cross section (cm^2/bit)	Bendel Parameter A
UART	$5.0592 x10^{10}$	12	$2.3719 x10^{-10}$	$2.5233 x10^{-13}$	23.5749
SPI	$5.3494 x10^{10}$	38	$7.1036 x10^{-10}$	$5.3210 x10^{-13}$	22.4406
I2C	$1.6543 x10^{10}$	95	$5.7427 x10^{-9}$	$1.5820 x10^{-11}$	17.8929
SERVO	$4.6842 x10^{10}$	4	$8.5394 x10^{-11}$	$6.7773 x10^{-14}$	25.7011

Using the calculated values in Table 10, the resulting SEU cross section per bit can be plotted and seen in Figure 114. Figure 114 shows the I2C circuit having the highest SEU cross section per bit by a large margin, followed by the SPI, UART and servo circuits which have low SEU cross sections, below $5x10^{-12}$ upsets per proton strike for all energies. Even though the number of errors detected for the I2C implementation was not extremely larger, the smaller percentage of the chip which this implementation filled resulted in the high cross section. The I2C circuit will result in the highest number of SEUs, up to $6x10^{-11}$, occurring due to a high energy proton strike.

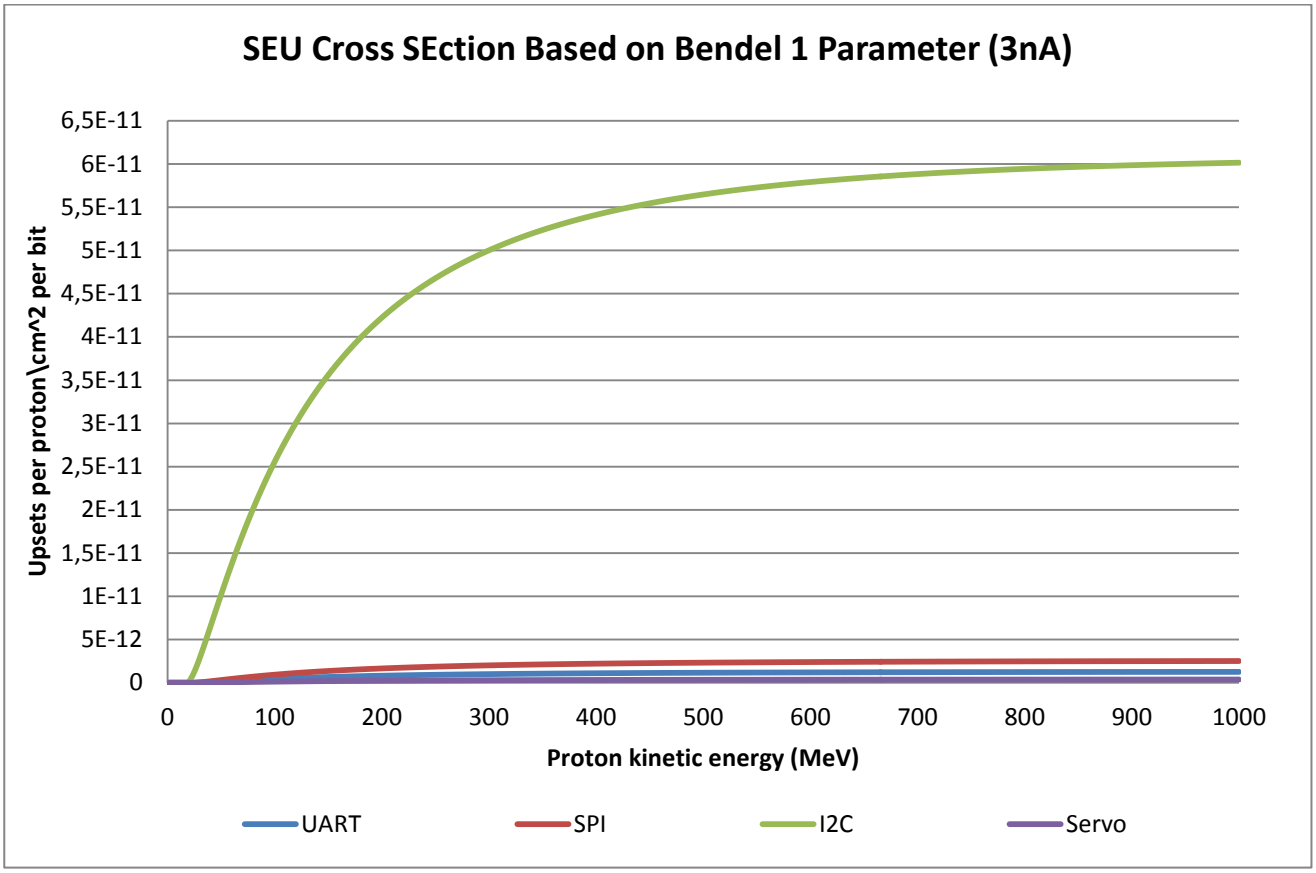

Figure 114: SEU cross section for test circuits at 3nA, from Bendel 1 parameter equation

Table 11 shows the cross section calculations when combining the testing at 2nA and 3nA seen above. This gives the SEU cross section results for the first test period.

Table 11 : Cross section results for implemented circuits of combined runs

Implemented Circuit	Proton fluence	SEU count	SEU cross section per circuit	SEU cross section (cm^2/bit)	Bendel Parameter A
UART	9.8374×10^{10}	19	1.9314×10^{-10}	2.0547×10^{-13}	23.8963
SPI	1.0402×10^{11}	84	8.0756×10^{-10}	6.0492×10^{-13}	22.2507
I2C	3.2167×10^{10}	139	4.3213×10^{-9}	1.1904×10^{-11}	18.2381
SERVO	9.1081×10^{10}	12	1.3175×10^{-10}	1.0456×10^{-13}	24.9814

Figure 115 shows the resulting SEU cross section based on the Bendel 1 parameter equation for the combined testing of the 2nA and 3nA experiments. The resulting graph follows the same behaviour as the individual tests for each of the implemented circuits. The I2C circuit can be seen to have the largest SEU cross section per bit of 4.5×10^{-11} upsets per proton for all energies. The SEU cross sections of the SPI, UART and servo circuits can be seen to be much lower, all remaining below $5 \times 10^{-}$

^{12} upsets per proton/cm^2 per bit, for all energy values. A possible reason for the high I2C SEU cross section could be the high frequency data signal or the sequence of bits which were outputted. Further testing and analysis would be required to ensure that the errors detected in the I2C data signal were indeed due to SEUs and not due to a faulty signal or noise. The SPI, UART and servo implementations are estimated to function with a small number of SEUs in a space environment.

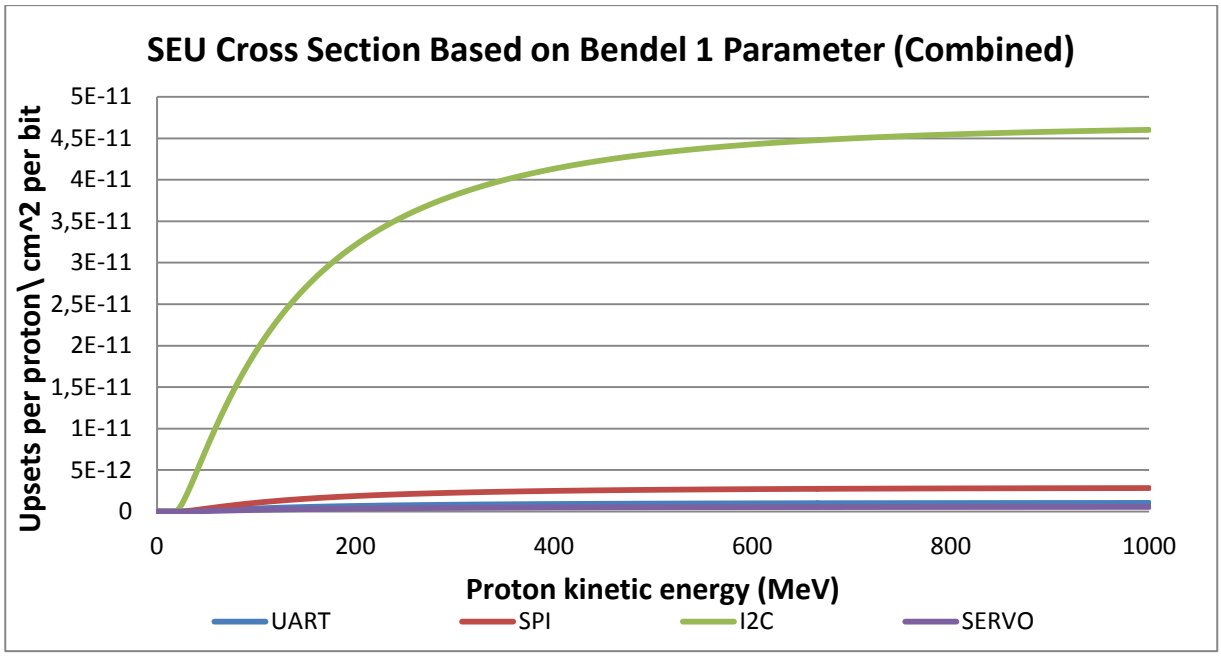

Figure 115 : SEU cross section for test circuits at 3nA, from Bendel 1 parameter equation for combined runs

5.1.2 Test 2

For the second test an additional FGG.2B.319 and FGJ.2B.319 vacuum connector pairs was acquired and soldered to allow for 19 additional IO pins which enables the testing of more circuits. The additional pins allowed the testing of a SPI, I2C, UART, servo motor, stepper motor, dc motor as well as 11 mitigation schemes. All of the data from the test 2 can be found on the attached disk.

The error rates for the various implementation methods tested at 2nA can be seen in Figure 116. The implementation 8 can be seen to have failed after approximately 30 seconds, resulting in the data from this implementation being discarded. Implementation 1 can be seen to have a high SEU rate and number of SEUs detected when compared to the other implementations. This is to be expected, as this implementation consisted of memory elements with no mitigation to protect the latches.

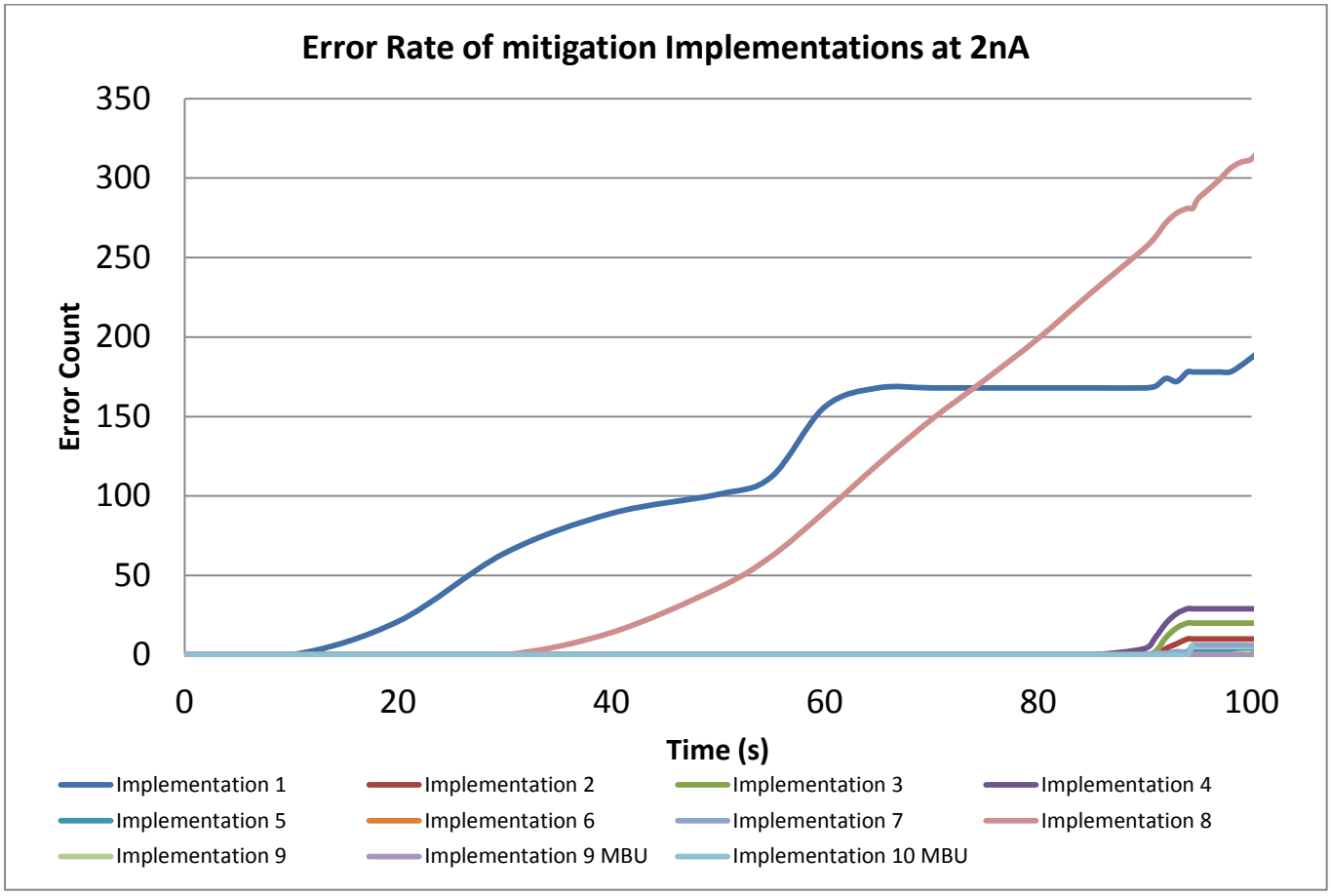

Figure 116: Error rate for implemented mitigation schemes at 2nA

Figure 117 illustrates a scaled representation of Figure 116. The number of SEUs detected in each implementation can be seen, allowing the number of SEUs occurring in each implementation to be viewed and compared. Implementation 1 consisting of a number of unmitigated memory elements (latches) connected in series experienced the highest number of upsets (182) as would be expected. Implementation 2 consisting of local TMR protection, experienced a total of 10 SEUs. The resulting transients occurred either directly in the user logic, clock, and clear signals or in the majority voter. Multiple errors could also have occurred in the memory elements in addition to upsets occurring in the IO banks of the device, which has no protection.

Implementation 3 performed the second worst out of all of the mitigated circuits, even though it was expect to mitigate a higher number of the SEUs and perform better than implementation 2. This mitigation method did not perform well in spite of having DMR protection provided for the user logic together with a SET filter protecting the TMR memory elements. Although mitigation was added for

the user logic, the detected transients occurred in the unmitigated global clock and clear signals, the majority gate, in the IO banks of the device or as multiple upsets in the latches resulting in SEUs.

Implementation 4 was expected to perform very well due to providing DMR protection for the user logic and TMR protected SET filters. Additionally TMR protection was included for the memory elements as well as DMR majority gates. However, Implementation 4 unexpectedly performed the worst out of all of the mitigation methods. Possible sources of SEUs could include transients occurring on the global clock and clear signals, directly in multiple of the memory elements or in the IO banks or due to multiple bit upsets. Transients occurring in a majority voter would also lead to an increase in SEUs.

Implementation 5 is identical to implementation 4, with the addition of TMR being applied to the global clock and clear signals. The resulting number of SEUs can be seen to drastically decrease over the test period when compared to implementations 3 and 4, and performed the third best overall. The resulting SEUs detected could be attributed to SETs occurring in the majority voters or SEUs occurring in the IO banks of the FPGA. Additional sources include SETs occurring in multiple of the signals or memory elements.

Implementation 6, which consists of full global TMR provided for all of the user logic, global signals, latches and majority voters, performed the best overall mitigating the highest number of upsets, together with implementation 9. SEUs occurring in implementation 6 can be attributed to SEUs occurring in the IO banks of the FPGA or due to multiple upsets occurring in the memory elements or majority voters. The importance of providing protection for all of the global signals and user logic can be seen in this implementation.

Implementation 7 performed relatively well when compared to the various mitigation methods, despite only providing DMR SET filter protection for the user logic before each memory element. No protection was provided for the memory elements or the global clock or clear signals, which contributed to the number of SEUs. Implementation 8 did not function as expected during the test conducted and the resulting data was considered as void. The reason for considering implementation 8 as void is the linear increase in the number of errors, indicating that a permanent error has occurred in the circuit.

Implementation 9 provides TMR protection for the user logic, global signals and memory elements together with TMR SET delay element filters and a single MBU filtering majority gate. The effectiveness of this mitigation scheme with the MBU protection and SET delay element filters can be seen in Figure 103, where only a single SEU was detected during testing. The mitigation scheme offers no DMR or TMR protection for the majority voters as well as the IO banks.

Implementation 9 MBU is identical to implementation 9, however, the effectiveness of the MBU filter and SET filters are tested by forcing MBUs to occur for each SEU. The implementation scheme performed well at filtering the MBUs during testing and performed fourth best out of the implementations while experiencing MBUs. Implementation 10 was a copy of implementation 6 with TMR majority gate MBU filters incorporated into the circuit. MBUs were also forced in the occurrence of a SBU. The MBU filters implemented performed well at reducing the number of errors occurring in the circuit as only 6 errors were detected.

The effectiveness of implementations 5, 9 MBU, 9 and 6 can clearly be seen in Figure 103. Each of these implementations experience less than 5 upsets during the test period.

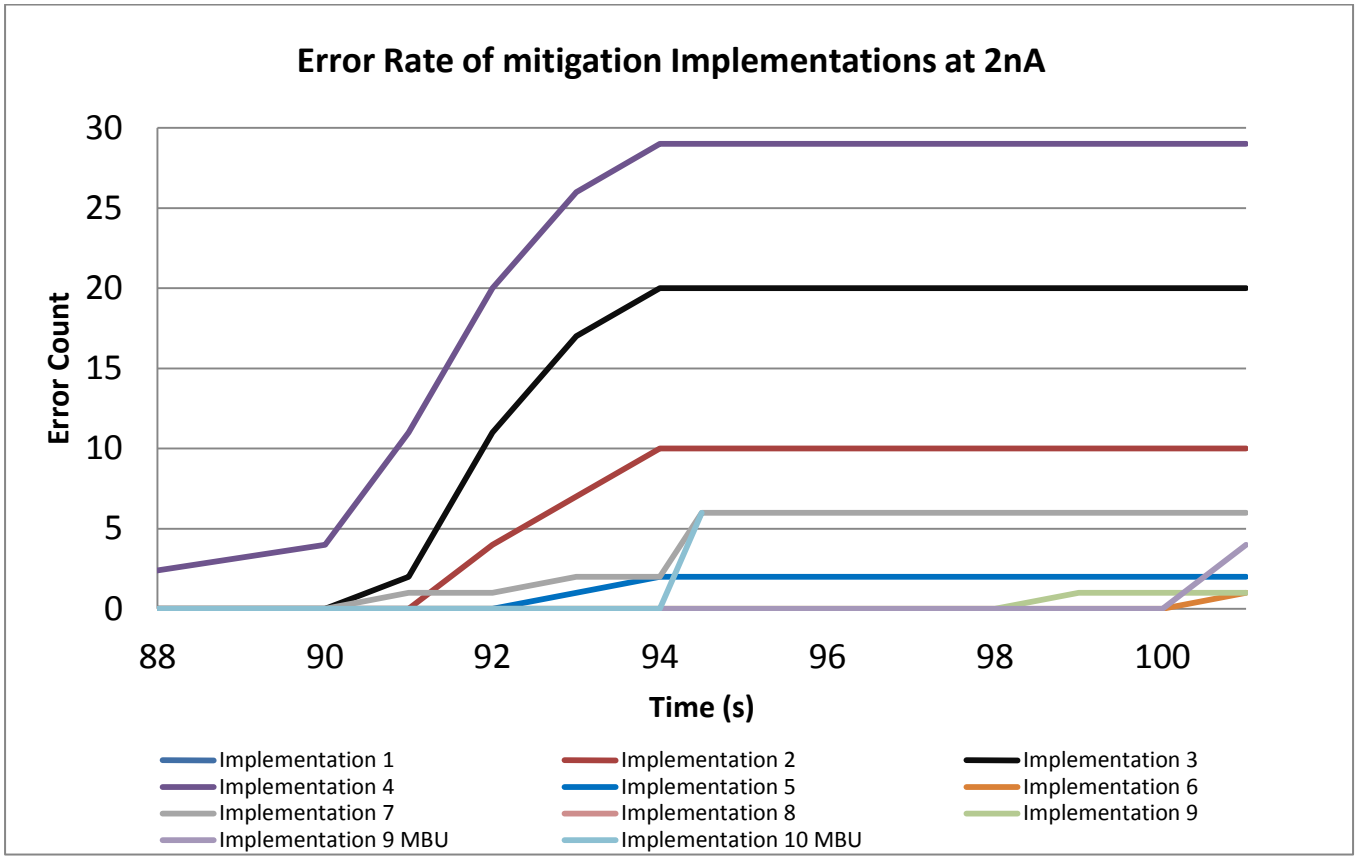

Figure 117: Scaled SEU error rate of Figure 116

Table 12 illustrates the circuit mapping of the mitigation implementations tested.

Table 12: Circuit mapping of various implementation methods in A3P1000

Mitigation Technique	Total Core Cells	Combinational	DLN1C1 (Latches)	MAJ Gate	INV	AND2	OR2	MX2	AND3	OR3	Percentage of Chip
Implementation 1	1208	604	604	0	604	0	0	0	0	0	4.92
Implementation 2	1656	948	708	236	236	0	0	0	0	0	4.80
Implementation 3	1140	798	342	114	342	114	114	114	0	0	4.64
Implementation 4	1336	1069	267	178	89	267	267	267	0	0	5.44
Implementation 5	1106	911	195	130	195	195	195	195	0	0	4.50
Implementation 6	1144	763	381	381	381	0	0	0	0	0	4.65
Implementation 7	1135	883	252	0	126	252	252	252	0	0	4.62
Implementation 8	2225	1958	267	89	623	712	267	267	0	0	9.05
Implementation 9	1152	1008	144	0	432	144	144	192	48	48	4.69
Implementation 9 MBU	1140	960	180	0	420	120	120	180	60	60	4.64
Implementation 10 MBU	1180	886	294	0	294	0	0	197	197	197	4.80
Total	14422	10788	3634	1128	3742	1804	1359	1664	305	305	56.75

Table 13 shows the beam parameters and resulting protons interacting with the A3P1000 die.

Table 13: Beam and test parameters at 2nA

Time	94	99	101
Current (A)	2×10^{-9}	2×10^{-9}	2×10^{-9}
Total number particle Flux (s^{-1})	1.2483×10^{10}	1.2483×10^{10}	1.2483×10^{10}
Total number particles in given seconds	1.17339×10^{12}	1.2358×10^{12}	1.2608×10^{12}
Beam area (cm^2)	3.14159	3.14159	3.14159
A3P1000 die area (cm^2)	0.36	0.36	0.36
Number of protons interacting with die	1.3446×10^{11}	1.41612×10^{11}	1.44473×10^{11}

Table 14 illustrates the SEU cross section calculations for each implemented test circuit using the proton fluence, number of SEUs and number of memory elements. The resulting Bendel "A" value can be calculated which will be required to plot Figure 104.

Table 14: SEU cross section results for implemented mitigation schemes at 2nA

Mitigation Technique	Proton fluence	SEU count	SEU cross section per circuit	SEU cross section (cm^2/bit)	Bendel Parameter A
Implementation 1	6.9608×10^{9}	182	2.6147×10^{-8}	4.3289×10^{-11}	16.7201
Implementation 2	6.4560×10^{9}	10	1.5489×10^{-9}	2.1878×10^{-12}	20.4278
Implementation 3	6.2372×10^{9}	20	3.2066×10^{-9}	9.3759×10^{-12}	18.5328
Implementation 4	7.3095×10^{9}	29	3.9674×10^{-9}	1.4859×10^{-11}	17.9685
Implementation 5	6.0511×10^{9}	2	3.3052×10^{-10}	1.6950×10^{-12}	20.7783
Implementation 6	6.7252×10^{9}	1	1.4870×10^{-10}	3.9028×10^{-13}	22.9057
Implementation 7	6.2098×10^{9}	6	9.6621×10^{-10}	3.8342×10^{-12}	19.6766
Implementation 8	1.2193×10^{9}	281	2.3083×10^{-8}	8.6453×10^{-11}	15.9571
Implementation 9	6.7722×10^{9}	1	1.4766×10^{-10}	1.0254×10^{-12}	21.4848
Implementation 9 MBU	6.7016×10^{9}	4	5.9687×10^{-10}	3.3159×10^{-12}	19.8685
Implementation 10 MBU	6.4560×10^{9}	6	9.2937×10^{-10}	3.1611×10^{-12}	19.9321

Figures 118 and 119 illustrate the resulting calculated upsets predicted per proton\cm^2 per bit. This allows the various implemented mitigation schemes to be compared to one another as all values are scaled according to the percentage of the chip which was occupied by the circuit, the number of memory elements and the period of irradiation. Implementation 1 can be seen to have the highest SEU cross section, as would be expected for an unmitigated circuit. Unexpectedly, implementation 4 had the second highest SEU cross section, even though this circuit incorporated DMR protection of the user logic and a SET filter before each TMR protection for memory elements. Implementation 3 resulted in the third worst SEU cross section followed by implementation 7. Implementation 9 MBU and 10 MBU had similar SEU cross section, with implementation 10 MBU performing slightly better.

Unexpectedly, implementation 2 had a small SEU cross section and performed the fourth best overall. The third best mitigation scheme was found to be implementation 5. Implementation 9 had the second lowest SEU cross section, and implementation 6 was found to be the most effective technique, resulting in the in lowest cross section. With exception to implementation 3 and 4, the mitigation schemes implemented all performed well, mitigating the majority of the errors caused by SEUs. The SEU cross section of these mitigation schemes were all found to be less that $2x10^{-11}$ upsets per proton/ cm^2 per bit.

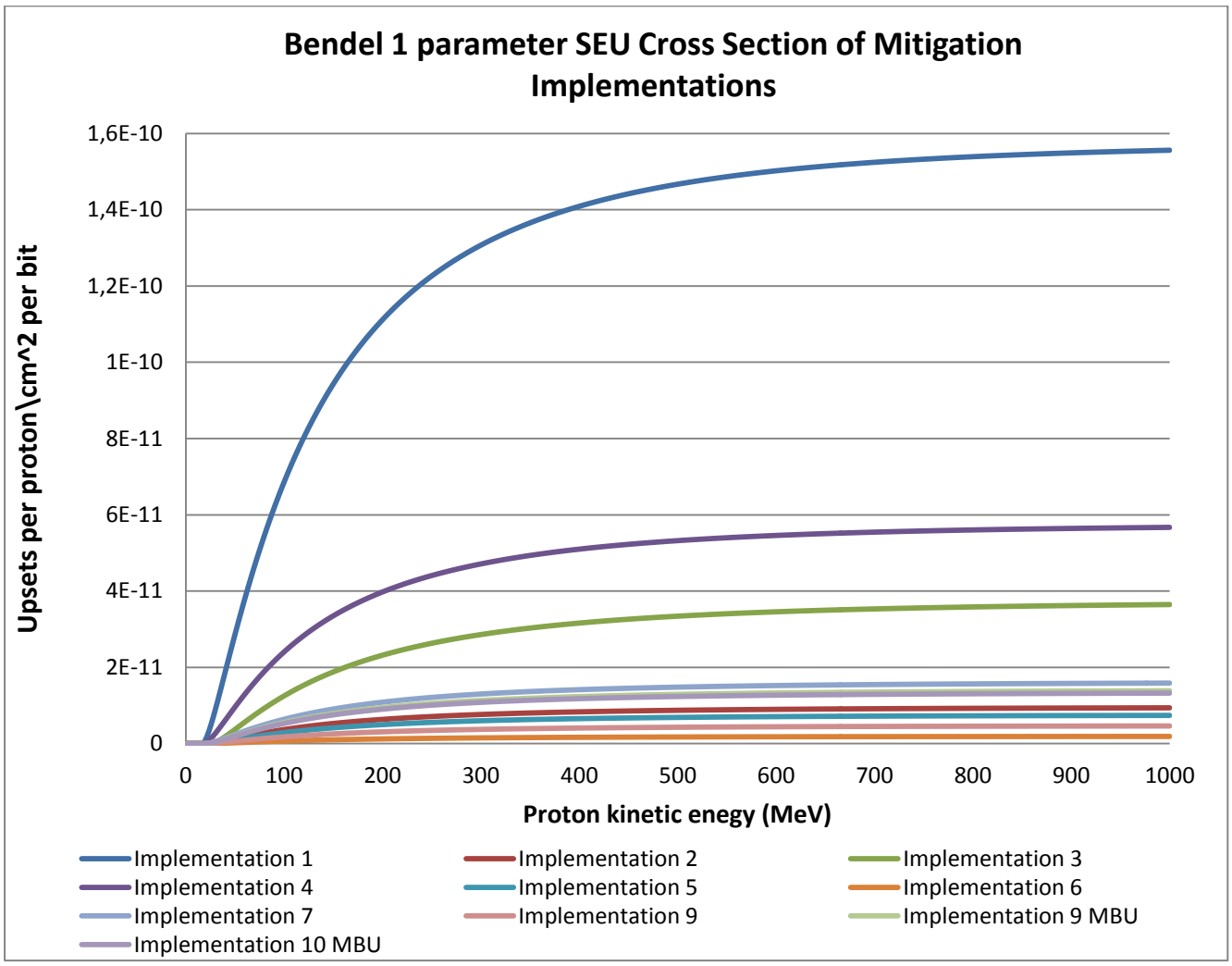

Figure 118: SEU cross section for mitigation circuits at 2nA, from Bendel 1 parameter equation

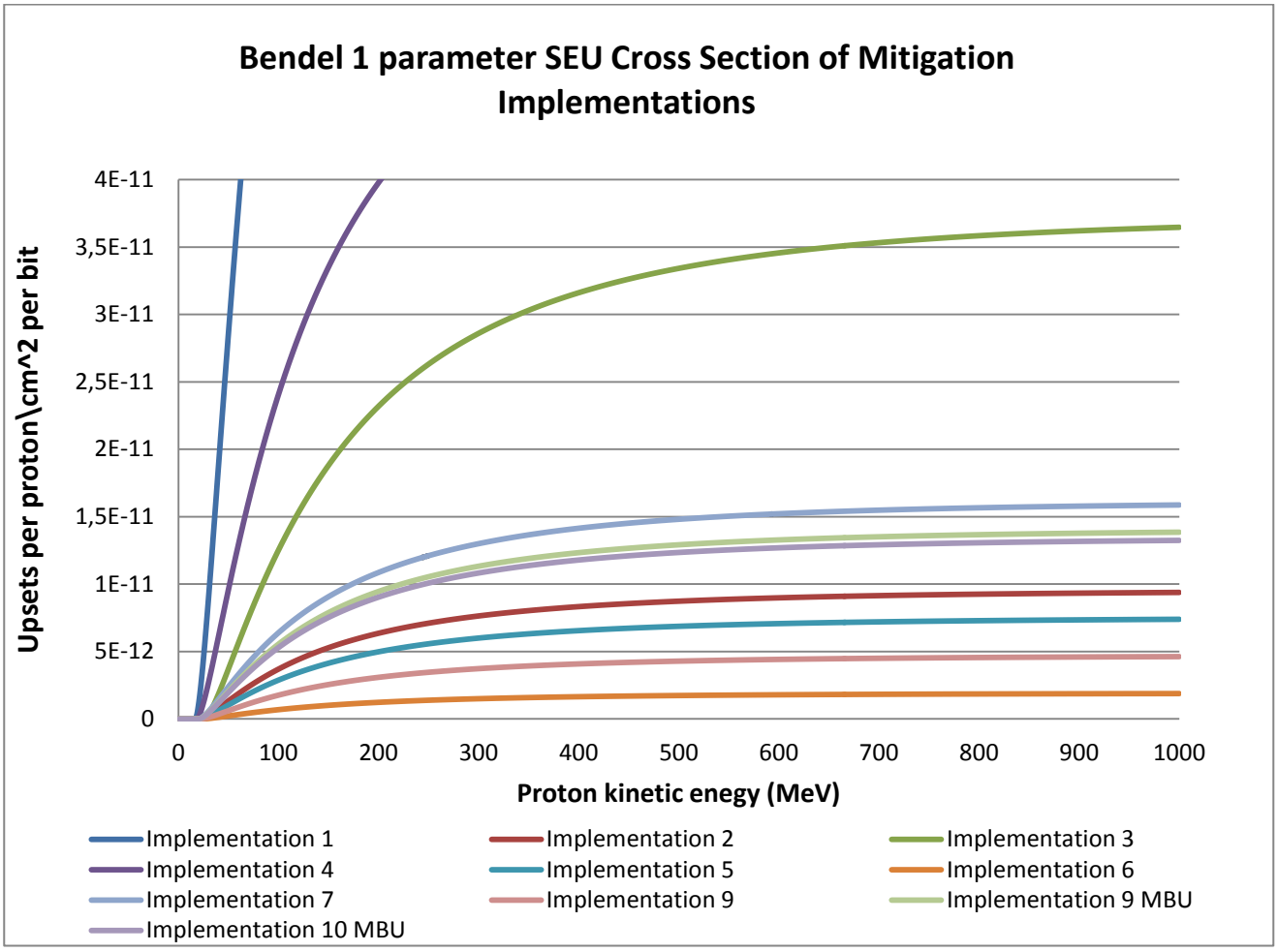

Figure 119: rescaled SEU cross section for mitigation circuits at 2nA, from Bendel 1 parameter equation

The second section of the second test conducted involved the testing of I2C, SPI, UART, servo motor control, DC motor control and stepper motor control circuits to provide an indication of the experimental SEU cross sections of these circuits.

Figure 120 illustrates the SEU rates for the six implemented circuits over a 48 second test period at 1nA. The highest number of errors occurred in the SPI circuit, due to being the most complex circuit, having the highest number of combination and memory elements and a moderately high frequency MISO signal. The I2C signal experienced the second highest number of upsets due to the high number of circuit elements and very high frequency. The I2C implementation experienced a lower number of errors than it should have, due to that the SDA output signal was only monitored during this test, and not the input. Monitoring of both signals would have shown a greater upset rate. The DC and stepper motor control circuits performed average with 15 and 11 SEUs detected respectively.

The stepper motor experienced a lower number of errors due to the small number of memory elements in the circuit. The error rate of the DC motor circuit was low, but higher than expected for the total number of circuit elements, but the error rate increased due to the 5 kHz signal frequency. The UART and servo motor control circuits performed the best overall during this test with only a few errors detected. The low number of servo errors could be attributed to the low frequency of the servo motor signal. The UART signal performed better than would have been expected, possibly due to the lower number of circuit elements, but this must be observed over more tests.

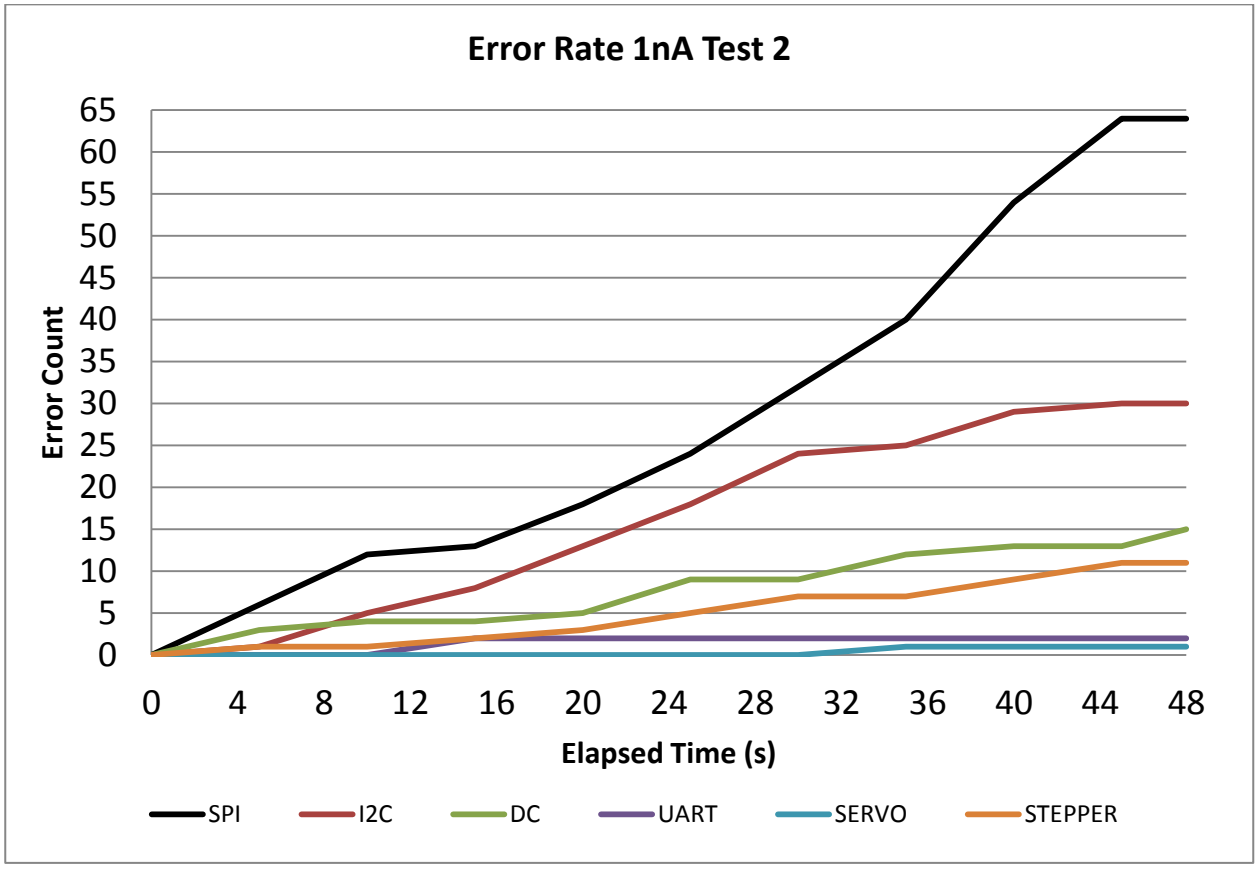

Figure 120: Test 2 error rate results 1nA (run 1)

Figure 121 illustrates the SEU rates for various circuits during a 120 second period of irradiation at 1nA. The SPI circuitry again experienced the highest number of SEUs during this test period as seen in the previous test. The reason can be explained by the high number of combination and memory elements in the circuit together with a moderate output frequency. The UART performed substantially worse than the previous test and accumulated the second highest number of errors. The errors could have occurred due to the high signal frequencies and moderate number of memory

elements. The signal upset rate must be closely monitored for the following tests to observe this increase in errors. The DC motor circuit experience a higher number of SEUs than the first test, but relatively low overall. The low number of upsets can be attributed to the small number of combinational and memory elements tested. The I2C circuit performed better than expected during this with approximately 40 SEUs occurring despite the very high signal frequency. The stepper motor circuits performed similarly to the I2C circuit, having a small number of memory elements. The very low frequency servo motor circuitry performed the best overall with only 1 error being detected over the test period.

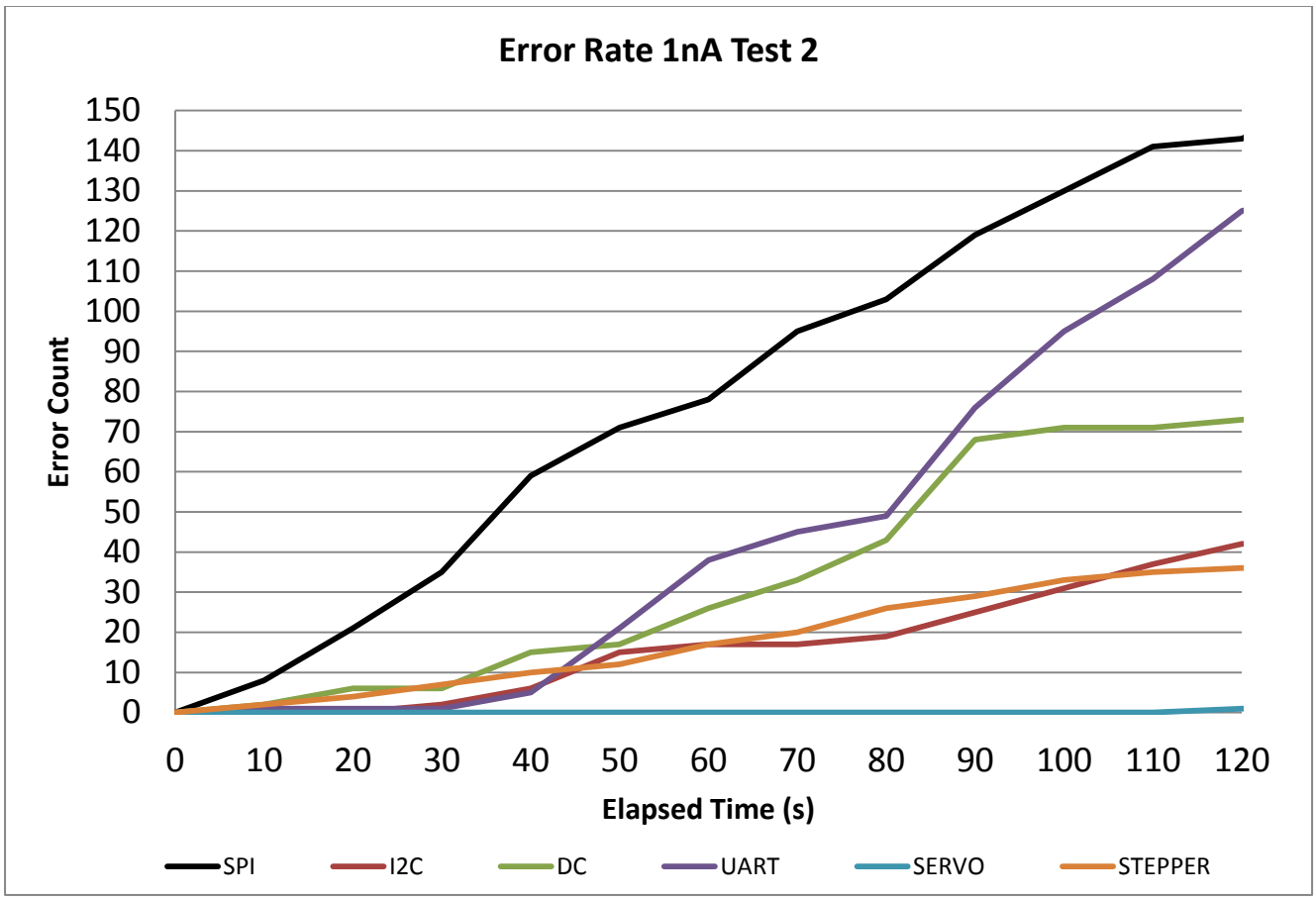

Figure 121: Test 2 error rate results 1nA (run 2)

Table 15 illustrates the circuit mapping of the test circuits. Only the memory elements are shown due to the large number of components utilized in the circuits.

Table 15: Circuit mapping of various implementation methods in A3P1000

Mitigation Technique	Total Core Cells	Combinational	DFN1E0	DFN1E1	DFN1	DFN1C1	DFN1E1P1	DFN1P1	Percentage of Chip
UART	1457	1175	114	12	156	0	0	0	5.93
SPI	2032	1428	84	180	340	0	0	0	8.27
I2C	1876	1428	48	0	32	272	16	80	7.63
SERVO	1324	946	18	216	144	0	0	0	5.39
DC	937	745	168	0	0	24	0	0	3.81
STEPPER	1522	1446	0	0	76	0	0	0	6.19
Total	9148	7168	432	408	748	296	16	80	37.22

Table 16 shows the various beam parameters such as the flux, number of protons interacting with the die.

Table 16: Beam and test parameters at 1nA

Time	122
Current (A)	1×10^{-9}
Total number particle Flux (s^{-1})	6.2414×10^{9}
Total number particles in given seconds	7.6145×10^{11}
Beam area (cm^2)	3.14159
A3P1000 die area (cm^2)	0.36
Number of protons interacting with die	8.7256×10^{10}

Table 17: SEU cross section results for implemented circuits at 1nA

Mitigation Technique	Proton fluence	SEU count	SEU cross section per circuit	SEU cross section (cm^2/bit)	Bendel Parameter A
UART	5.1730×10^{9}	126	2.4357×10^{-8}	8.6373×10^{-11}	15.9581
SPI	7.2145×10^{9}	145	2.0098×10^{-8}	3.3275×10^{-11}	17.0194
I2C	6.6607×10^{9}	42	6.3057×10^{-9}	1.4075×10^{-11}	18.0340
SERVO	4.7008×10^{9}	1	2.1273×10^{-10}	5.6278×10^{-13}	22.3574
DC	3.3268×10^{9}	73	2.1943×10^{-8}	1.1429×10^{-10}	15.6587
STEPPER	5.4038×10^{9}	36	6.6620×10^{-9}	8.7658×10^{-11}	15.9422

Figure 122 shows the SEU cross section of the test circuits for a 1nA beam current and 120 second test duration. The DC motor circuit resulted in the highest SEU cross section of 3.8x10-10 upsets per proton/ cm^2 per bit, although it did not experience the highest number of SEUs. This is due to the number of SEUs detected and the small percentage of the chip occupied by this circuit compared to the other circuits. The UART and stepper motor control circuits resulted in the second and third highest SEU cross sections due to the smaller chip size occupied and relative number of SEUs. Both of these had a SEU cross section of 3×10^{-10} upsets per proton/cm^2 per bit. Despite having the highest

number of errors, the SPI circuit resulted in the third lowest SEU cross section due to the large number of circuit elements. The I2C circuit had the second smallest SEU cross section, followed by the servo motor circuit which performed the best, resulting in the lowest SEU cross section.

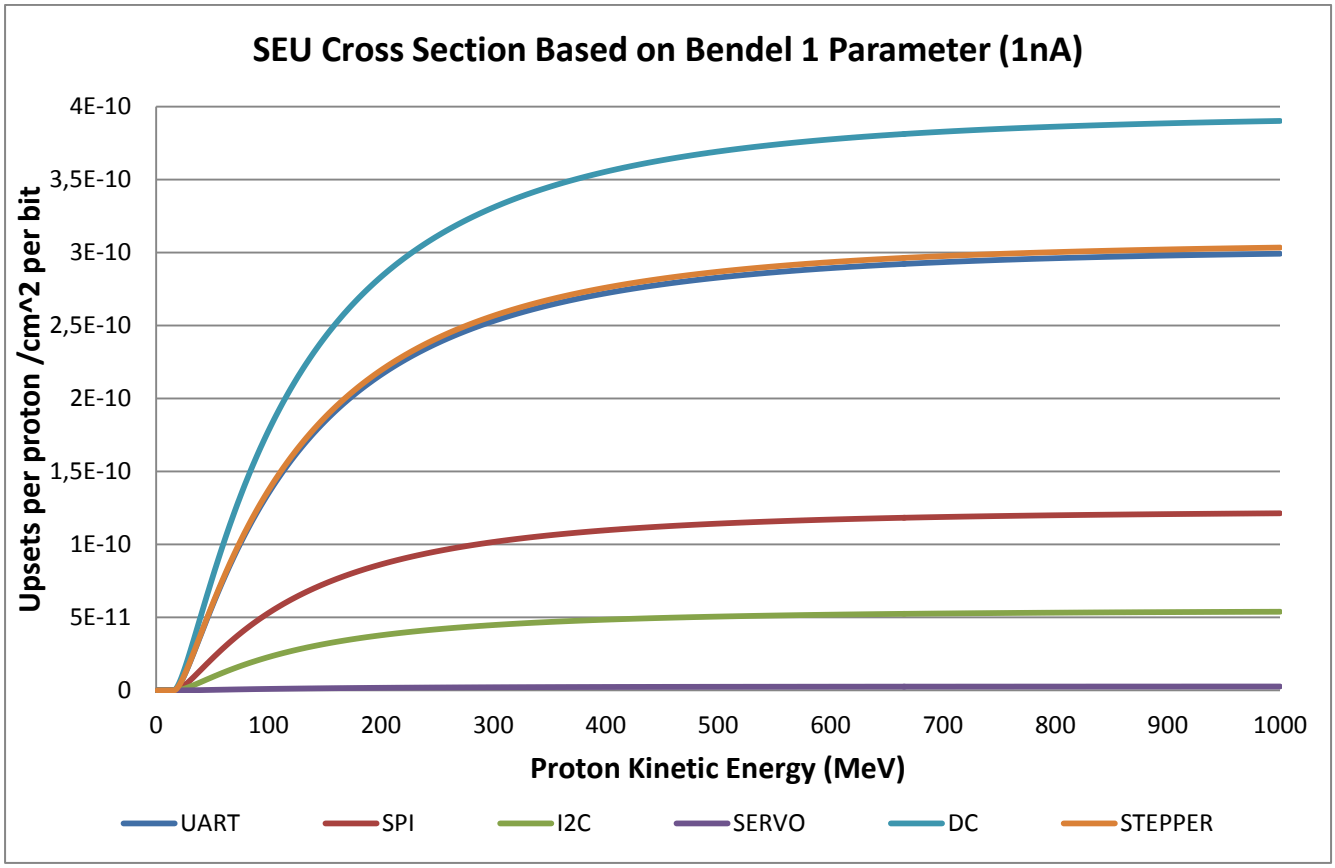

Figure 122: SEU cross section for mitigation circuits at 1nA, from Bendel 1 parameter equation

Figure 123 shows the error rate for the test circuits during a 2nA test. The UART circuit can be seen to have experienced a large number of errors at a high rate. It is unsure whether this was due to SEUs or failure of the device circuitry for the UART code. The linear increase in errors gives a possible indication that the circuitry for the UART code had perhaps failed during irradiation, without causing the device to fail. The SPI implementation experienced more errors than the remaining circuits, followed by the I2C implementation, which experienced an increase in SEUs when compared to the previous test. This increased number of errors is more expected than the lower number in the previous test. The DC motor circuit experienced the third least amount of errors, followed by the stepper motor and servo motor circuits as in the previous tests.

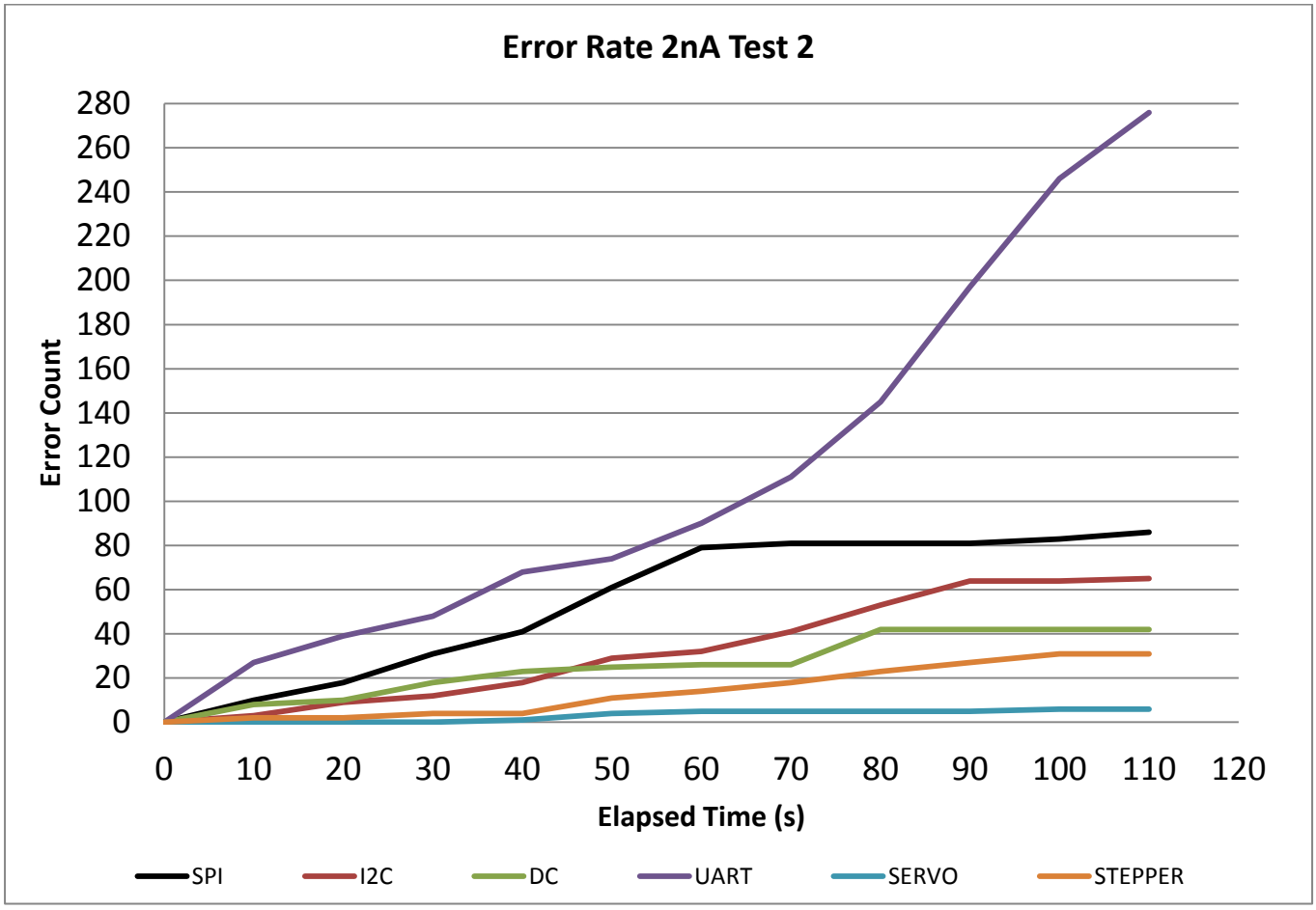

Figure 123: Test 2 error rate results 2nA

Table 18: Beam and test parameters at 2nA

Time	110
Current (A)	2×10^{-9}
Total number particle Flux (s^{-1})	1.2483×10^{10}
Total number particles in given seconds	1.3731×10^{12}
Beam area (cm^2)	3.14159
A3P1000 die area (cm^2)	0.36
Number of protons interacting with die	1.5735×10^{11}

Table 19: SEU cross section results for implemented circuits at 2nA

Mitigation Technique	Proton fluence	SEU count	SEU cross section per circuit	SEU cross section (cm^2/bit)	Bendel Parameter A
UART	9.3284×10^{9}	276	2.9587×10^{-8}	1.0492×10^{-10}	15.7496
SPI	1.3010×10^{10}	86	6.6104×10^{-9}	1.0944×10^{-11}	18.3414
I2C	1.2011×10^{10}	65	5.4117×10^{-9}	1.2080×10^{-11}	18.2202
SERVO	8.4769×10^{9}	6	7.0781×10^{-10}	1.8725×10^{-12}	20.6408
DC	5.9991×10^{9}	42	7.0010×10^{-9}	3.6464×10^{-11}	16.9148
STEPPER	9.7446×10^{9}	31	3.1813×10^{-9}	4.1859×10^{-11}	16.7581

The SEU cross section for the test circuits tested at 66MeV and 2nA can be seen in Figure 110. The UART control code can be seen to have the biggest SEU cross section for this test with more than 350 upsets per proton\ cm^2 per bit. The stepper motor circuit can be seen to have the second highest SEU cross section, followed closely by the DC motor control circuit. The SPI and I2C communication circuits, being similar in nature and operating frequencies, have similar SEU cross sections of almost 50 upsets per proton/ cm^2 per bit. The best performing circuit with the lowest SEU cross section can be seen to be the servo control circuit.

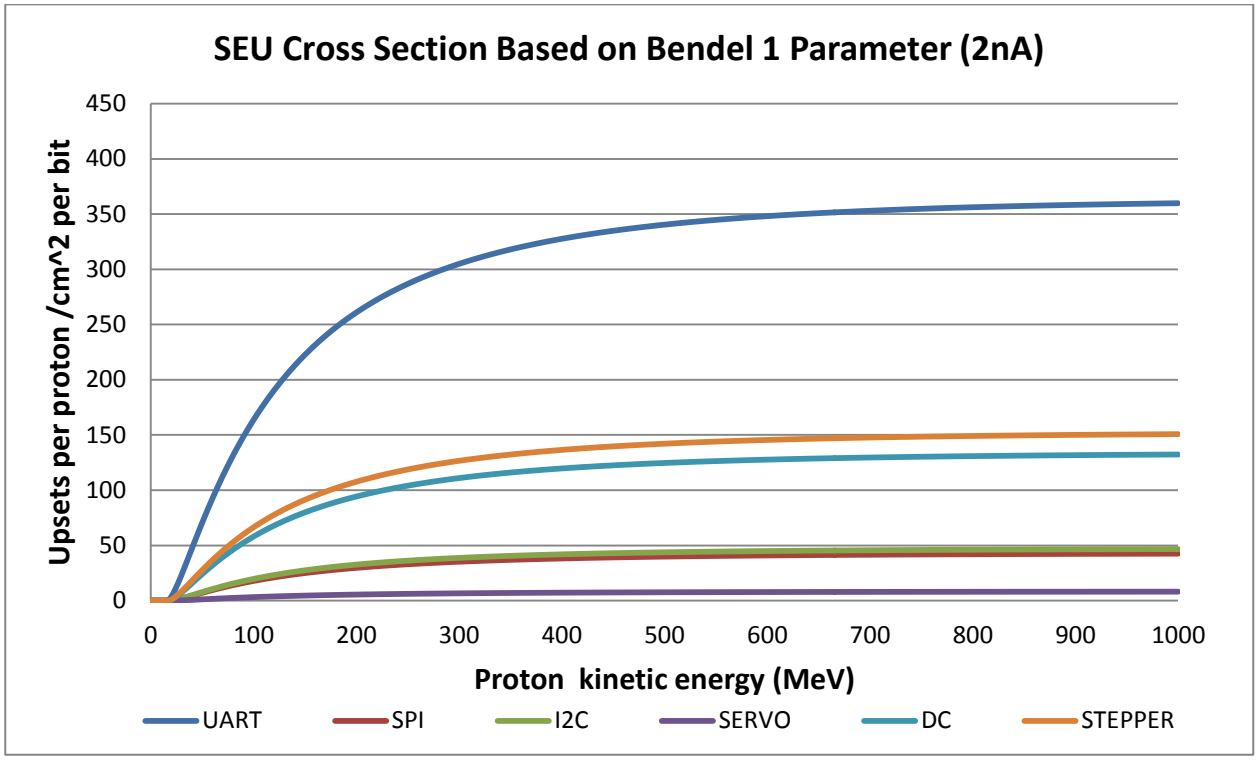

Figure 124: SEU cross section for mitigation circuits at 2nA, from Bendel 1 parameter equation

Table 20: SEU cross section results for implemented circuits for combined runs

Mitigation Technique	Proton fluence	SEU count	SEU cross section per circuit	SEU cross section (cm^2/bit)	Bendel Parameter A
UART	$1.6537 X10^{10}$	404	$2.4431 X10^{-8}$	$8.6633 X10^{-11}$	15.9548
SPI	$2.3063 X10^{10}$	295	$1.2791 X10^{-8}$	$2.1177 X10^{-11}$	17.5454
I2C	$2.1292 X10^{10}$	137	$6.4343 X10^{-9}$	$1.4362 X10^{-11}$	18.0096
SERVO	$1.5027 X10^{10}$	8	$5.3237 X10^{-10}$	$1.4084 X10^{-12}$	21.0361
DC	$1.0635 X10^{10}$	130	$1.2224 X10^{-8}$	$6.3667 X10^{-11}$	16.2904
STEPPER	$1.7274 X10^{10}$	78	$4.5153 X10^{-9}$	$5.9412 X10^{-11}$	16.3667

Figure 125 illustrates the SEU cross section curves for the test circuits for the three tests conducted during the second testing stage combined. The resulting curves shows the UART circuit having the highest overall SEU cross section by a large margin. This result should be further tested to confirm this finding due to the possibility of an internal error having occurred in the FPGA. The DC motor circuit resulted in the second highest SEU cross section due to the small number of circuit elements tested and the moderate number of SEUs detected.

The stepper motor control circuit can be seen to have the third highest SEU cross sections, also due to the moderate number of SEUs detected and having the lowest number of memory elements tested. The SPI and I2C communication circuits can be seen to have the third and second lowest SEU cross sections even though both had experienced high numbers of SEUs. The resulting cross section was low due to the large number of combinational and memory elements tested during irradiation. The very low frequency servo motor control circuit performed the best overall as in the previous tests. The low number of SEUs and moderately high number of circuit elements resulted in a low SEU cross section.

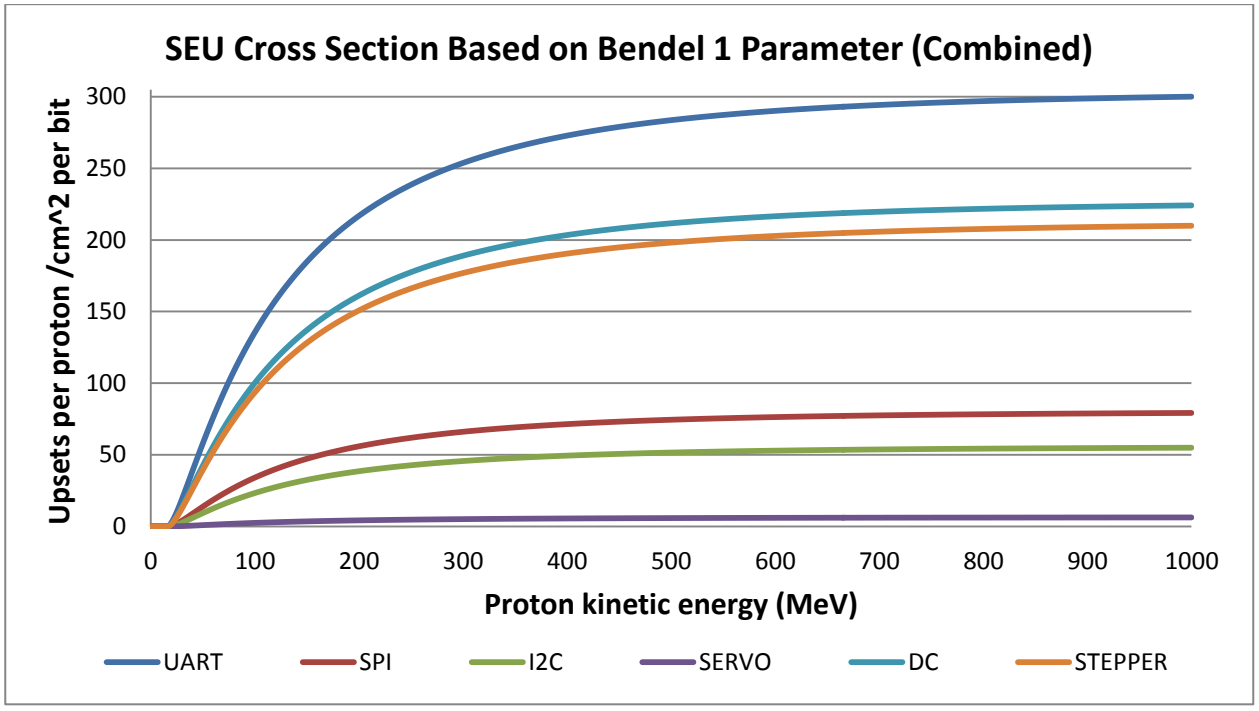

Figure 125: SEU cross section for mitigation circuits for combined runs, from Bendel 1 parameter equation

5.1.3 Post Radiation Tests

After the confirmed failure of the FPGA, the testing was terminated and the FPGA and radiation level of the testing environment was allowed to decrease. After a safe radiation level was reached the FPGA was removed from the test position and testing was conducted to determine if the FPGA could be reprogrammed. Firstly the FPGA was connected to power and the outputs of the test circuits were monitored for any outputs. After no outputs were detected, the attempt to reprogram the FPGA resulted in the failure of the erasing of the device.

5.1.4 Mechanical Design

Prior to conducting the single event upset testing, the mechanical platform was shipped to the iTemba LABS beforehand and assembled there. The mechanical design, together with the control motors, was then mounted in place within the vacuum chamber and tested for operational reliability under vacuum. Once it was confirmed that the control of the rotational position, vertical adjustments and angle of incidence of the design was functional and operated under vacuum, the mechanical structure was proven to function as designed.

The control of the angle of incidence of the test board mounting plates, as well as the vertical position of the system controlled by the lead screws, operated as intended. This allowed full control of the parameters. The structure of the mechanical design functioned as planned and structural rigidity and integrity was maintained when applying test loads several times higher than the designed loads.

Unfortunately, due to the limited number of vacuum (FGG.2B.319 and FGJ.2B.319) connectors available, the number of available IO pins between the inside and outside of the chamber was limited to 17. Since the test circuits alone required all 17 of the IO pins, the control motors of the mechanical design were as a result not able to be implemented during the testing of the FPGA. Due to this, the ProASIC3 development board was to be mounted onto the mechanical platform without the ability to rotate the board.

5.2 Total Ionizing Dose

The total ionizing dose tests were conducted at the FruitFly Africa facility. The A3P1000 test board was programmed and irradiated for a period of 429 minutes (7:09 hours) at a dose rate of 845.08 rad/minute, resulting in a total absorbed dose of 362.45 Krad. The desired outcomes of the experiment was to monitor the error rate of the various circuits as well as the operating characteristics, such as the supply current and voltages, of the device to determine how the absorbed dose would affect the normal operation of the A3P1000. All of the TID data and graphs can be found on the attached disk.

5.2.1 Output Error Rate

Table 21 shows the total number of errors counted by the control board during the duration of irradiation. The test circuits include the various communication circuits including SPI, I2C and UART and motor control circuits for DC, servo and stepper motors.

Table 21: TID test summary

Elapsed Time (s)	24745	
Absorbed Dose (Krad)	348.53	
Implemented Circuit:	**Error Count:**	**Scaled percentage (WTR filled amount)**
SPI	4109	100
I2C	2680	66
DC	529	6
UART	581	10
SERVO	308	5
STEPPER	3363	65

Figure 126 illustrates the number of errors occurring for the various implemented circuits during the 429 minute test period. The numbers of errors for all of the circuits follow the same linear trend with a very low gradient, experiencing almost no errors. With exception to SPI, the number of errors only increases after an absorbed dose of approximately 240 Krad. After the radiation dose reaches a specific point for each circuit, the errors outputted by the circuit increase at a high rate. The highest number of errors (4109) was detected by the SPI circuit which had the highest number of

combination and memory elements as well as moderately high signal frequencies. The second highest number of errors was outputted by the stepper motor circuit (3363) which was not expected. Although the number of memory elements was low, the output frequency was moderately high. The third highest number of errors was detected in the I2C circuit (2680). The extremely high single frequencies and moderately high number of combination and memory elements contributed to the large number of errors. Due to the high signal frequencies and relatively high number of combination and memory elements, a higher number of errors were expected, however the SDA input signal was not monitored, resulting in the lower error rate.

The three remaining circuits performed well in comparison with UART experiencing 581 errors, DC 529 errors and the servo motor circuit experiencing 308 errors. The URAT circuit performed relatively well due to the moderately high signal frequencies and the simple circuitry with a lower number of combinational and memory elements. The DC motor circuit also performed well due to rather low numbers of circuit combinational and memory elements as well as only having a moderately high signal frequency. The servo motor control circuit performed the best out of the test circuits partially due to the ultra-low output frequency and moderately low number of circuit elements.

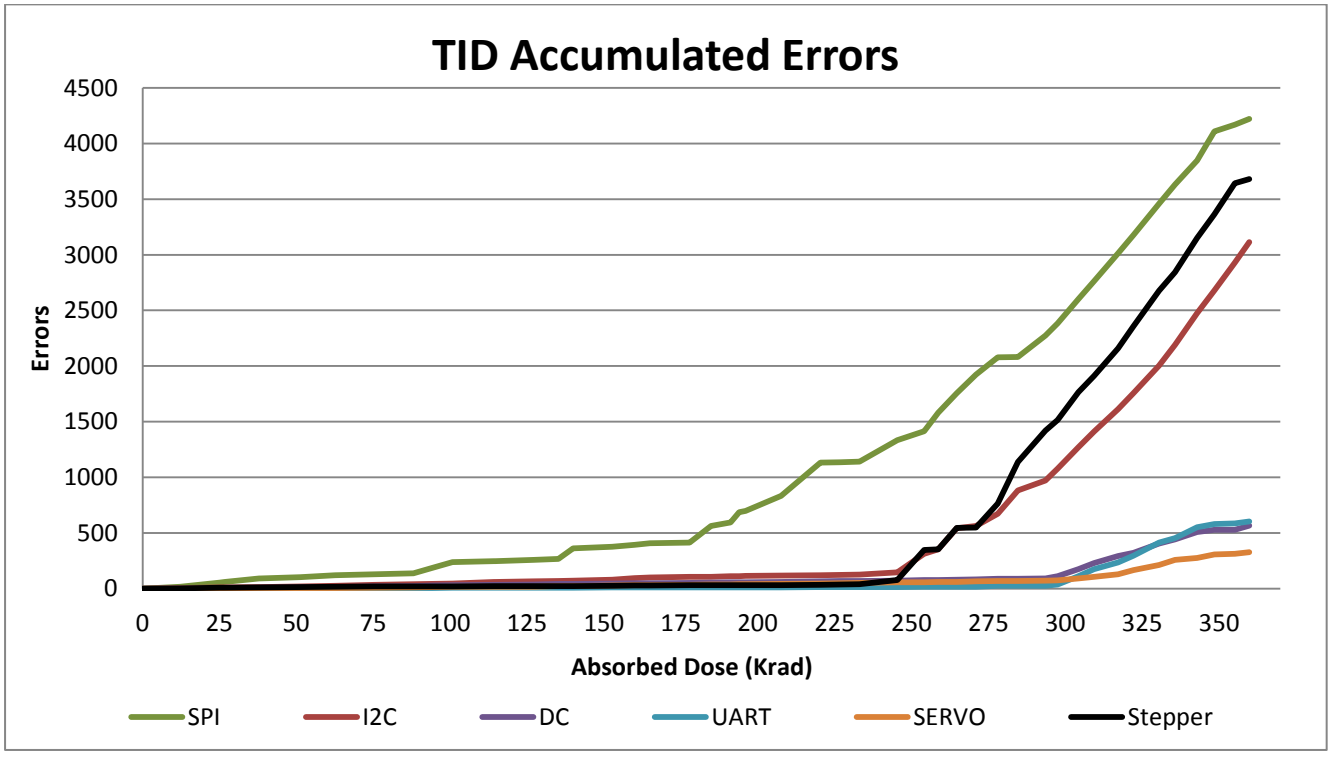

Figure 126: TID error rate for test circuits

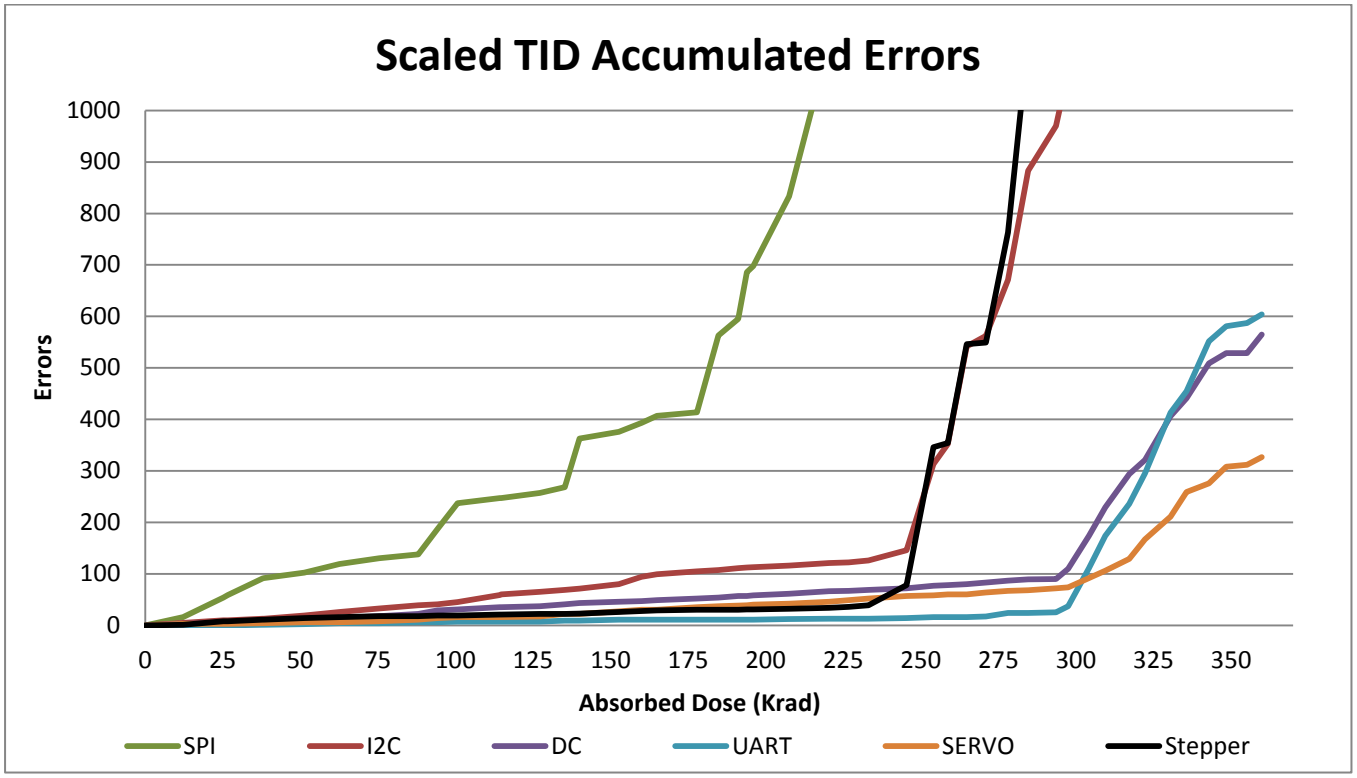

Figure 127: Rescaled TID error rate for test circuits

Figure 128 illustrates the scaled TID error rate according to the number of errors occurring in the circuit, the percentage the circuit fills the FPGA and the number of memory elements present in the circuit. The resulting plot shows the same error order as in Figure 127.

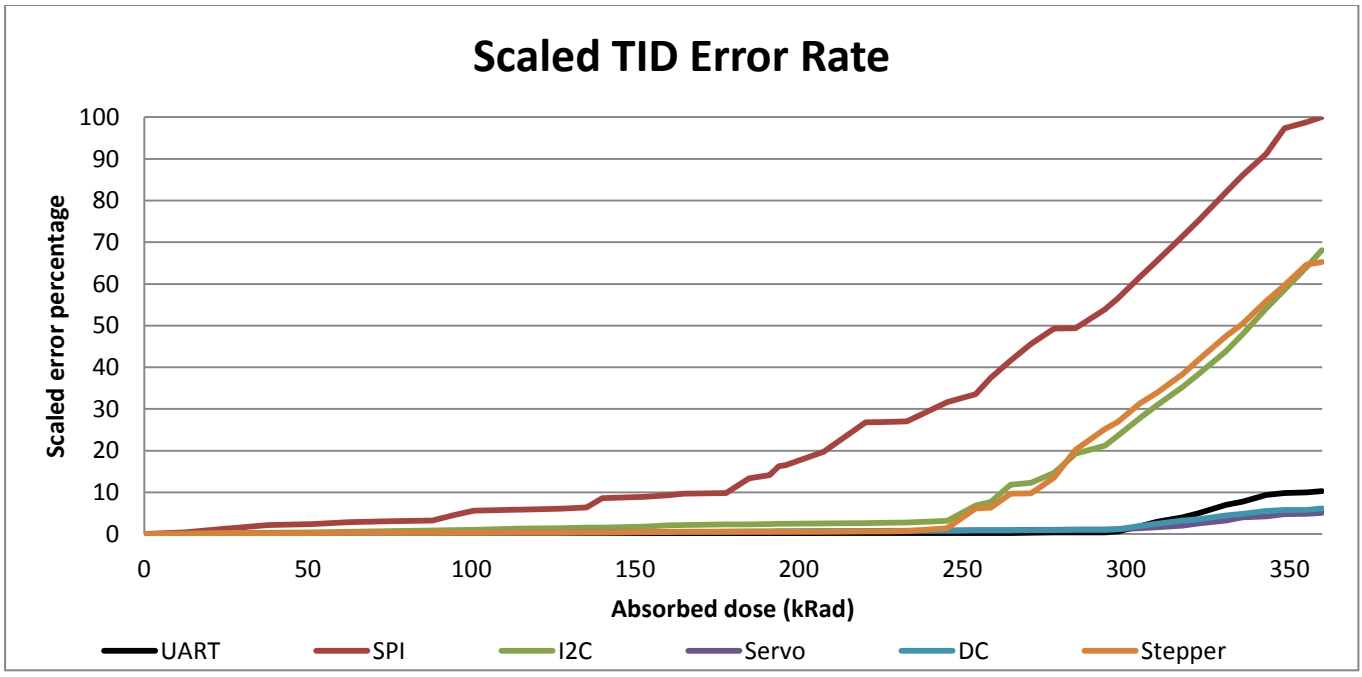

Figure 128: TID error rate scaled according to circuit size

In addition to the previously described test circuits, a number of mitigation methods were tested during the TID testing procedure. The resulting number of errors detected in each of the mitigation schemes can be seen in Table 22.

Table 22: TID test summary for mitigation methods

Absorbed Dose (Krad)	359.91	
Elapsed Time (s)	25553	
Mitigation Technique:	**Error Count:**	**Scaled percentage (WTR filled amount)**
Implementation 6	31	12.5
Implementation 5	43	17.9
Implementation 9 MBU	141	56.9
Implementation 10 MBU	203	79.1
Implementation 1	263	100
Implementation 7	89	36
Implementation 8	186	38.5
Implementation 9	26	10.4
Implementation 4	56	19.3
Implementation 2	96	37.4
Implementation 3	135	54.4

Figure 129 illustrates the number of errors occurring in each of the mitigation schemes during the testing period. The number of errors for each of the test circuits can be seen to increase with the increase in absorbed dose. A detail description of the areas in each circuit where any errors could have occurred can be seen in the second SEU test session for the tested mitigation schemes. The highest number of errors was detected in implementation 1 as expected for an unmitigated circuit with no protection for the memory elements. The second highest number of errors was detected in implementation 10 MBU, closely followed by implementation 8. The implementation 9 MBU had the fourth highest number of errors, followed by implementation 3. Implementation 2 performed better than expected, performing the 6^{th} best followed by implementation 7 which experienced the 5^{th} least number of errors. The four implementations with the least number of errors accumulated over the test period include implementation 4, followed by implementation 5 and implementation 6 and the best being implementation 9.

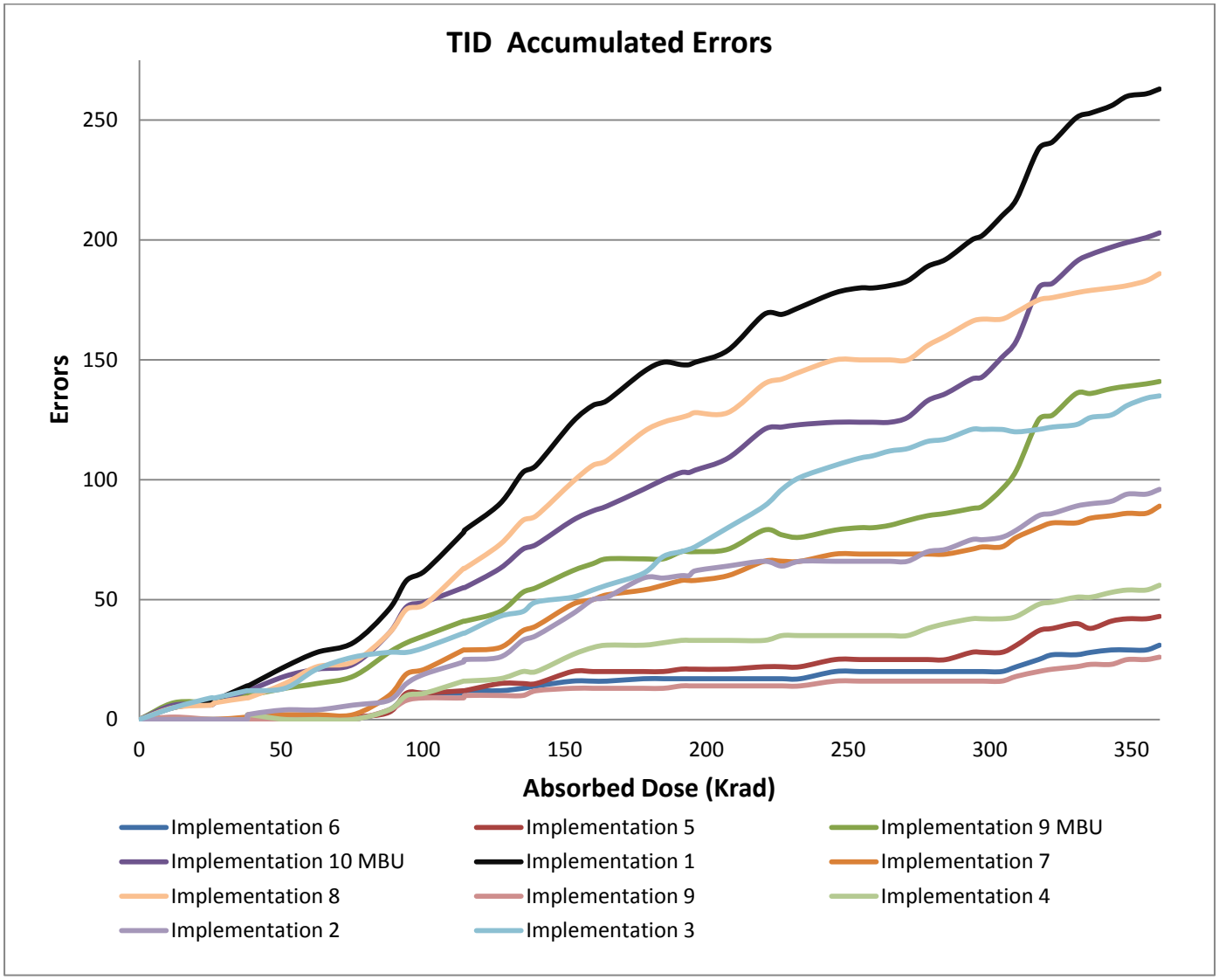

Figure 129: TID error rate for mitigation circuits

Figure 130 illustrates a scaled plot of the TID mitigation error rates for the implemented circuits. The error rates of each mitigation scheme were scaled according to the number of memory elements in the circuit as well as the total percentage of the FPGA which the implementation filled. According to this scaling method, implementation 1 performed the worst, as before. Implementation 10 MBU performed the second worst, by a greater margin than in the previous results. With the scaled results, implementation 9 MBU performed the third worst, from the fourth worst for the pre-scaled results. Implementation 3 performed the fourth best in this scaled plot, followed by implementation 8 which when scaled, performed the fifth worst, as oppose to the 3rd as before. Implementation 2, 7, 4 remained in the same positions as the 6th, 5th and 4th best implementations followed by implementation 5, 9 and 6 which were the 3rd, 2nd and best effective implementations.

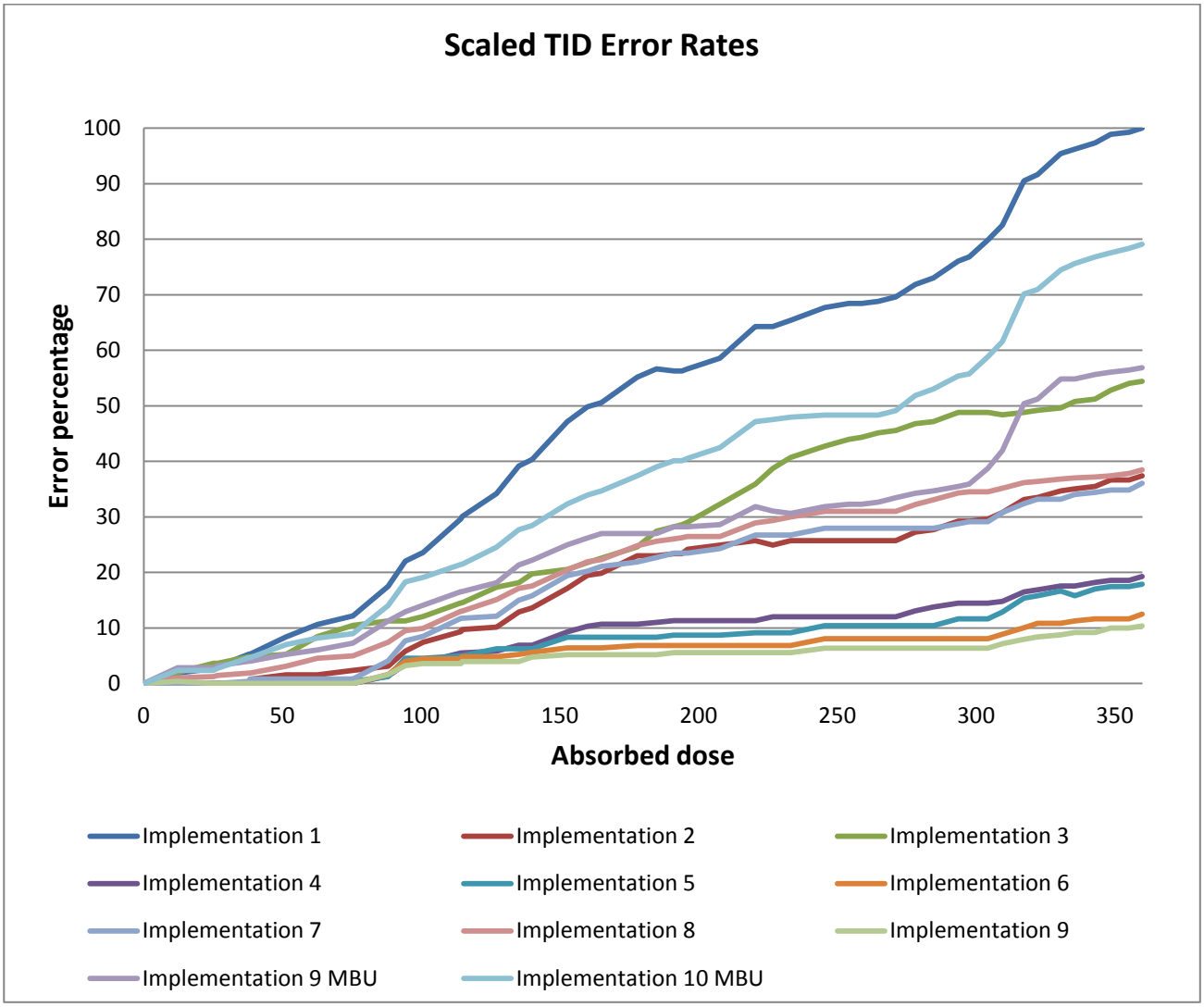

Figure 130: Scaled TID error rates

5.2.2 Supply Current

Figure 131 shows the per second fluctuation of the FPGA board supply current over the duration of the experiment. The majority of the measured current values remain constant with the first fluctuations of the supply current seen from as early as an absorbed dose of 10Krad. The current deviation remains constant, within a range of 62mA to 85mA, during the testing for an absorbed dose of up to 230Krad. After an absorbed dose of 230Krad, a sudden increase in the current fluctuation can be seen with ranges of 27mA to 120mA. The effects of this sudden fluctuation of current, as a result of the absorbed dose, can be seen in the number of errors detected in the

outputs as well in Figure 126. The number of output errors increase exponentially together with the varying supply current fluctuations after an absorbed dose of 230 kRad.

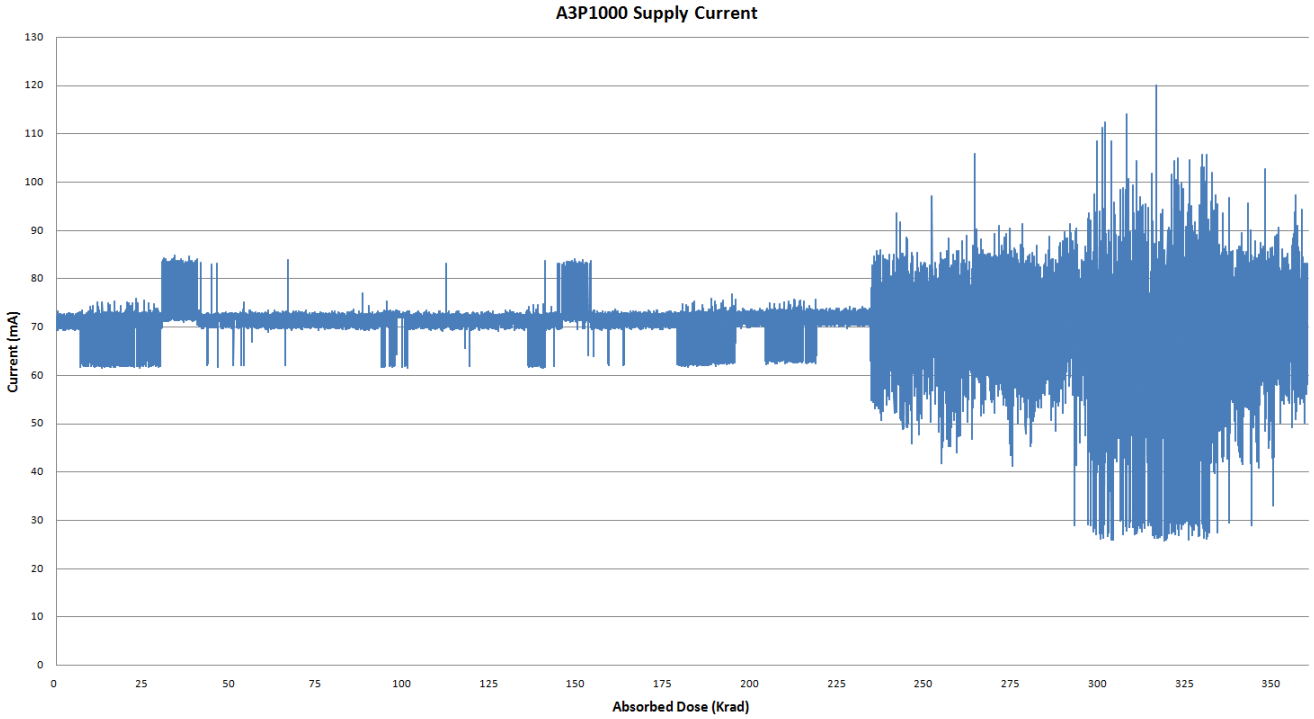

Figure 131: Supply current vs. absorbed dose

Figure 132 shows the measured supply current of the test board for 100 second intervals. This allows for more accurate analysis of the relationship between the absorbed dose and supply current. It can be seen that the average supply current remained relatively constant with slight variances for an absorbed dose up to approximately 230Krad. After 230Krad, the supply current fluctuated more sporadically with large decreases in the current being measured around 300Krad. This current fluctuation occurs at the same absorbed dose as the increase in output errors as seen in Figure 125.

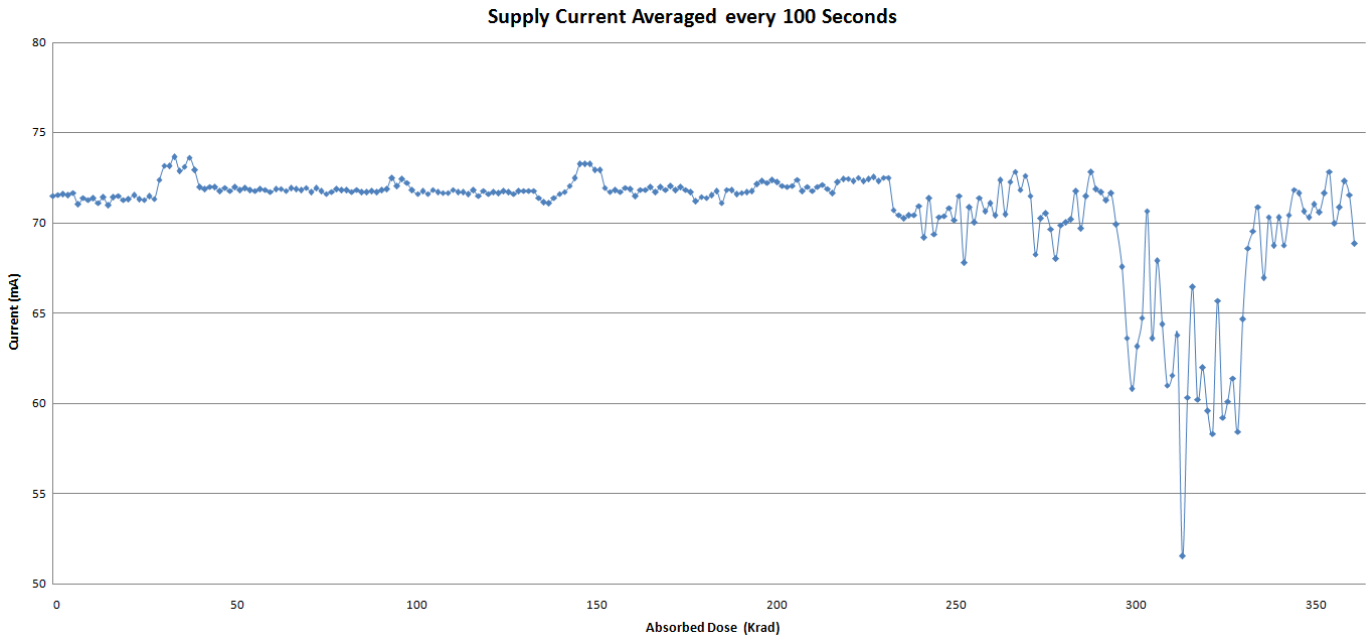

Figure 132: Averaged supply current over 100 second periods

5.2.3 Voltage

Figure 133 shows the relationship between the shunt resistor values and the VCCPLF measured voltage of the FPGA. A clear relationship can be seen when comparing the two voltages over the test duration. The majority of the voltage fluctuations occurred in both of the measured voltages during the test, although the magnitude of the fluctuations varied.

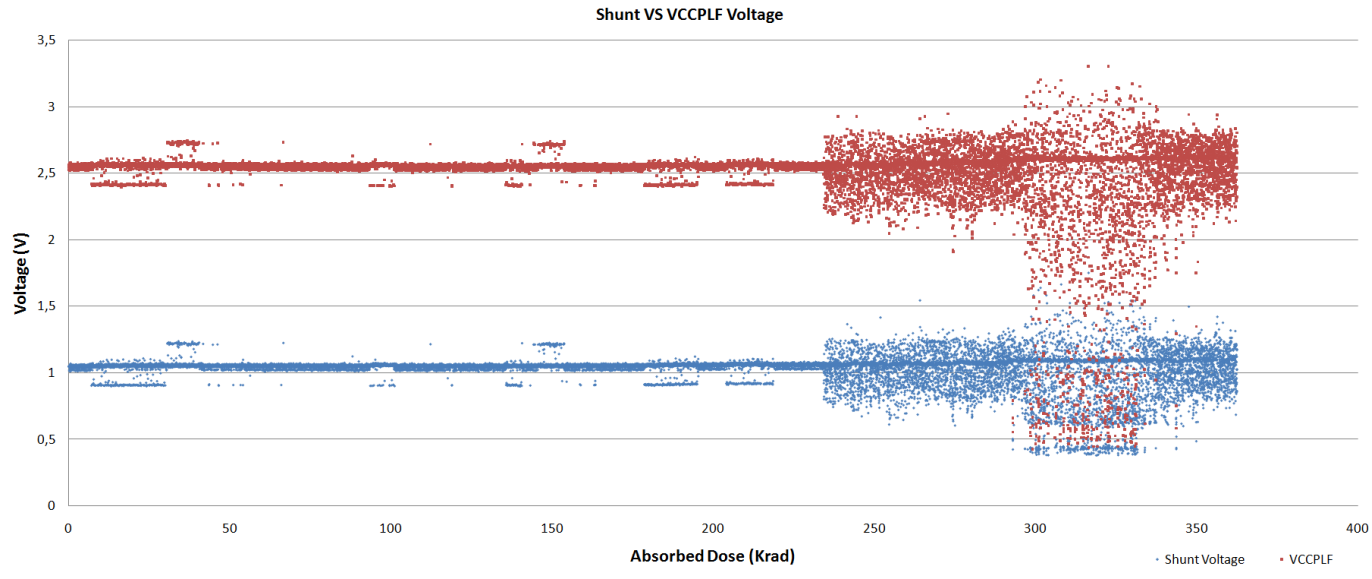

Figure 133: Shunt and VCCPLF voltage vs. absorbed dose

Figure 134 illustrates the averaged measured voltage of the shunt resistor and the VCCPLF measured voltage over 100 second intervals. A clear relationship between the two voltages can be seen, showing voltage fluctuations occurring at the same amount of absorbed dose with varying magnitudes.

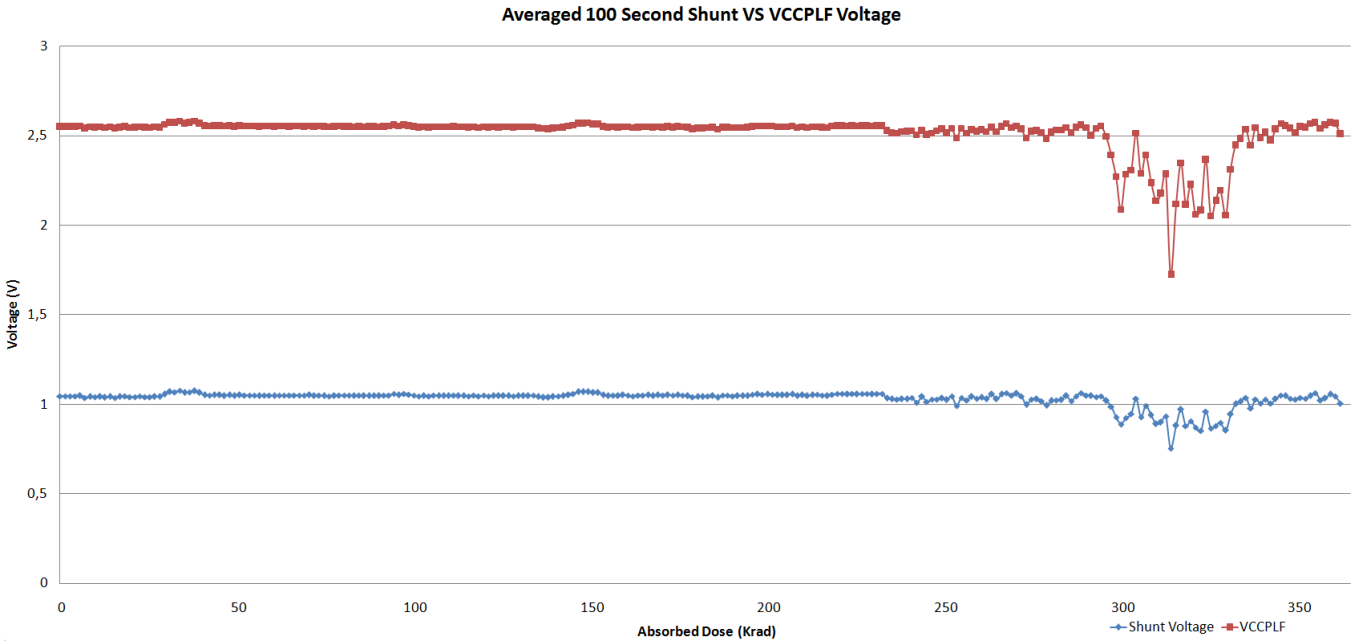

Figure 134: Averaged shunt resistor and VCCPLF voltages

From the supply current, output error and voltage analysis, reliable functionality of the A3P1000 device can be considered to be lost after an absorbed dose of 230 kRad. After a total absorbed dose of 230 kRad, large fluctuations in the supply current and operating voltages in addition to an exponential increase in the output errors can be observed. This relationship between the absorbed dose and the operating characteristics indicates that the reliable functionality of the device was lost after this amount of absorbed dose.

6 Conclusion

6.1 Overview

With the recent increased number of privately owned and long term commercial and military satellites currently being launched into orbit, the implementation of reconfigurable commercial off the shelf FPGAs have become an area of interest. Reconfigurable FPGAs appear as the more attractive option for space applications, as the number of programmable gates have increased.

These FPGAs are however are susceptible to radiation effects such as SEUs and TID, which often make FPGAs unsuitable for space applications. In an attempt to solve this problem, radiation hardened components providing SEU protection and an increased tolerance to an absorbed dose mitigate the radiation effects. However, the availability of these devices are at a higher capital cost, decreased computation speeds, increased physical dimensions and reduced available resources.

As an alternative, various mitigation schemes have been created to mitigate the effects of space radiation on COTS FPGAs. The mitigation schemes provide error mitigation for SEUs and mitigate TID effects, prolonging the operational lifespan of the FPGA.

The main purpose of this research thesis was to determine an experimental procedure in which the SEU and TID characteristics of various test circuits implemented in a flash based FPGA could be determined. It was proposed that the SEU cross section and TID error rates of UART, DC, servo, stepper, SPI and I2C control circuits were to be determined to better understand the radiation effects on these circuits. It was also proposed that various SEU mitigation schemes, comprising of variations of TMR and the AND-OR multiplexer SET filter, would be implemented such that the performance of each method could be evaluated and that comparisons between the implementations could be made. The SEU testing was to be conducted by irradiating the test FPGA with a 66MeV proton beam of varying current. The TID testing was to be carried out by exposing the test FPGA to a Co-60 source with a dose rate of 845.08 rad per minute. Additionally, it was proposed that a mechanical platform would be designed and implemented at the iTemba LABS testing facility to facilitate both this experiment as well as future testing to be conducted at the facility.

The SEU experimental results presented in this thesis illustrate the error rates, SEU cross section and calculated SEU cross section for additional proton energies for each implemented circuit. The testing

was conducted over two test sessions, each lasting for an average duration of 20 minutes. The first test session aimed to detect the number of SEUs occurring in each of the four implemented circuits, as well as the subsection of the code in which the SEU was detected. A successful experimental procedure for detecting SEUs induced in an FPGA by a high energy proton beam was developed as the first test yielded results. The UART, SPI, I2C and servo motor circuits were tested during irradiation to determine the SEU cross section of each circuit. The recorded error rates show the accumulation of errors for the subsections of each circuit as a function of elapsed time. The MISO, MOSI and clock signals of the SPI circuit could be monitored individually to determine the section in which an error had occurred. Similarly, the I2C data and I2C clock signals and UART RX and UART TX were monitored individually, providing an indication as to in which part of the circuits the most errors occurred. From the total number of accumulated errors of each circuit, the SEU characteristics and number of upsets per proton/ cm^2 per bit can be determined for any given proton energy. This provides an indication of the performance characteristics of the circuit when exposed to a proton of a given energy level.

The resulting SEU cross section for the combined results of the first testing session indicated that the worst performing circuit was that of the I2C implementation. The high number of upsets detected could result due to the very high output frequency of the I2C signals. This together with the low number of combination and memory elements resulted in the high SEU cross section of the I2C implementation. The three remaining circuits performed relatively similarly, with the SPI circuit performing the third worst. The high number of errors in the SPI implementation were as a result of the moderately high signal frequencies as well as the high number of combinational and memory elements in the circuitry. This high number of circuit elements ensured that the SPI implementation had a relatively low SEU cross section. The UART circuit performed the second best due to the combination of a lower number of errors and high number of circuit elements. The best performing circuit was found to be the servo motor control circuit which experienced the lowest number of upsets, possibly due to the extremely low signal frequency. The low number of SEUs and high number of circuit elements resulted in the lowest SEU cross section.

The second test session focused on the SEU testing of the implemented mitigation schemes. Each of the mitigation schemes were implemented in the FPGA and tested during irradiation, monitoring the number of errors detected. The results obtained from this experiment indicated the error rate of

each implementation and the resulting SEU cross sections. The unmitigated implementation experience the highest number of SEUs (182) as would be expected.

Implementation 4 consisting of local TMR mitigation unexpectedly performed poorly, with the highest number of errors for all of the mitigated circuits. Implementation 3 comprising of DMR protected user logic and a SET filter protecting the TMR memory elements, performed the second worst out of the mitigated circuits followed by Implementation 7, consisting of DMR SET filters for the user logic placed before the memory elements.

Implementation 9 MBU, which tests the effectiveness of the MBU filter together with SET filters, performed well up until the last few seconds of testing where 4 errors were detected. This implementation was found to be the 6th most effective while forcing MBUs to occur for every SEU. Implementation 10 MBU, testing the effectiveness of the MBU filter, performed well experiencing only 10 SEUs and performing the 5th best overall while MBUs were forced in the circuit. This circuit resulted in a lower SEU cross section compared to implementation 9 MBU despite experiencing a higher number of SEUs.

Implementation 2, consisting of a simple local TMR implementation experienced the third highest number of errors for the mitigated circuits, but performed surprisingly well when considering the SEU cross section of the circuit, ending as the 4th best implementation scheme. Implementation 5, consisting of TMR global signals and providing DMR protection for the user logic as well as TMR protected SET filters performed exceptionally well by only experiencing 2 SEUs during testing. Implementation 9 consisting of TMR protected user logic, global signals and memory elements together with SET delay filters and a single MBU filtering majority voter experienced the lowest number of SEUs together with implementation 6.

Implementation 6 however performed the best overall when considering the SEU cross section of the circuit. This is as a result of both the single SEU detected and the higher number of memory elements present in the circuit during testing. This implementation was as a result in this test found to be the most effective to implement for high energy proton testing.

In addition to the mitigation schemes, the SEU characteristics of various test circuits were determined. Sporadic behaviour of the UART circuit resulted in an unclear identification of SEUs, but

it was presumed that the circuit functioned correctly. Assuming that all of the errors detected were as a result of SEUs, the UART circuit performed the worst during this test.

The DC motor control circuit was found to have the second highest cross section, however the DC motor circuit did not experience the highest number of upsets. The moderate number of upsets together with the small number of circuit elements resulted in the high cross section of the circuit. The stepper motor circuits had the third highest cross section, even though the circuit experienced the second lowest number of upsets on average. The low number of latches in the circuit resulted in the high cross section. The SPI control circuit, despite experiencing the second highest number of upsets, resulted in the third smallest SEU cross section. This can again be attributed to the large number of combination and memory elements in the test circuit. The I2C circuit resulted in the second smallest cross section. The extremely high frequency signals of the I2C circuit produced a moderately high number of errors. The best performing circuit was found to be the servo motor control implementation. This circuit implementation experienced the lowest number of errors during each test while containing a large number of combinational and memory elements. The low circuit frequency was an important factor in the number of errors detected.

In order to establish the TID characteristics of the FPGA and implemented circuits, the error rate and device parameters were recorded during irradiation. A single test was conducted with duration of 429 minutes, in which all the test parameters were monitored. The resulting supply current of the FPGA can be seen to have a direct relationship to the total absorbed dose. An increase in the absorbed dose leads to the sporadic fluctuation of the supply current, but surprisingly, not failure. The supply current fluctuated between values of 28 and 120nA during the irradiation testing, with greater fluctuations experienced after an approximate 230 kRad absorbed dose. The relationship between the VCC voltage, shunt voltage and the absorbed dose was noted to be dependant. The increases in the absorbed dose lead to an increase in the fluctuation and magnitude of fluctuation of the VCC voltage and the shunt resistor voltage. The VCC voltage fluctuates at the same amount of absorbed dose as the supply current, but at different magnitudes. The averaged current and voltage plots provide a clearer illustration of the current and voltage fluctuations of the device due to the absorbed dose.

In addition to the device parameters, the error rates of the various circuits were recorded. When considering the error rates of these circuits, a relationship between the error rate and the absorbed dose, as in the supply current can be noted. As the total absorbed dose increases, the error rate increases and leads to an exponential growth in the error rate of each of the test circuits. The highest number of errors was detected in the SPI circuit, followed by the stepper motor and I2 circuits. The UART, DC and servo motor circuits all experienced a low number of errors in comparison. The TID effects on the number of errors detected for the various mitigation schemes provide an indication of the expected effectiveness of each implementation. The unmitigated scheme, implementation 1, performed the worst. The difference in errors between the mitigation schemes during the TID testing resulted in interesting findings. Implementation 10 MBU performed the second worst during TID testing, followed by implementation 8. Implementation 9 MBU performed the fourth worst, followed by implementation 3. Surprisingly, implementation 2 experienced the 6^{th} least amount of errors, followed closely by implementation 7. Implementation 4, 5, 6 and 9 formed the four top performing methods of mitigation during the TID testing. The most effective mitigation scheme was found to be implementation 9, consisting of TMR protected user logic, global signals and memory elements together with SET delay filters and a single MBU filtering majority voter, resulted in the lowest number of errors detected in the circuit outputs.

In addition to the SEU and TID testing conducted, the mechanical design implemented to facilitate SEU testing at the iTemba LABS functioned as intended in the vacuum testing environment. The mechanical platform enables full control of the horizontal and vertical position of the beam on the test board, as well as the angle of incidence between the beam and the board. The mechanical system and all of its components performs accurately and reliably within the radioactive vacuum environment.

From the experiments conducted, comparisons between the various mitigation schemes can be made to determine the effectiveness of each in comparison to the other techniques. From this, it was found that implementation 6 and 9 performed the best for both the SEU tests as well as the TID testing. The communication and motor control circuits tested provided insight into the number of experienced upsets in each circuit due to high energy proton strikes. The relationship between the number of upsets and the circuit frequency as well as the number of combination and memory elements in the circuit was observed. An indication of the number of errors expected in each of the

circuits was determined during testing, providing an indication of the cross sections of each circuit. It must be noted that these tests conducted only serve as an indication of the expected behaviours of both the control circuits and the mitigation schemes. To fully understand and make accurate predictions of the number of expected errors and effectiveness of each circuit, more testing is required to allow for the analysis of more data. Final conclusions can only be made when the data set is larger.

From the findings of the tests conducted, the preliminary SEU cross sections due to high energy proton strikes as well as the TID characteristics of the implemented circuits implemented in the A3P1000 can be estimated for a space application in a given radiation environment. The testing conducted also provides a basis for the further testing of various FPGAs and additional circuit implementations.

6.2 Recommendations

A number of recommendations can be made to the experimental procedure described in this thesis, allowing for more in depth and further detailed experimental results to be obtained. These recommendations include:

1. The design and fabrication of specialised PCB boards. The use of PCB boards specifically designed for the experimental testing of SEU and TID effects would be of a great advantage during testing. Designed boards would allow for current and voltage monitoring to all inputs of the FPGA chip, not only the entire board. This allows for in-depth current monitoring of the test FPGA. As only the required components will be design for the PCB board, no additional redundant components will be present during testing, minimizing the chance of noise and interference due to components.
2. It would be advisable, if possible, to obtain as much testing time as possible. Multiple testing sessions will allow for more results to be obtained which would in turn, give a better indication of the true SEU and TID characteristics of the testing circuits and test FPGA. The tests conducted in this thesis are limited to two test sessions, thus only providing an indication of the expected radiation characteristics to be. Further prolonged testing will

provide a basis on which to build accurate predictions of the SEU and TID behaviour of the test device and various mitigation schemes.

3. It is recommended for SEU testing at the iTemba LABS to source as many vacuum connectors as possible, allowing for the maximum number of IO pins available. The increased number of pins will allow for an increased number of boards to be tested during one session. This would increase the number of test circuits which can be tested. Since testing time at the iTemba LABS is limited, this will speed up the testing process and allow for more results to be obtained, resulting in more accurate estimations and conclusions. Additionally, the pins will allow for the control of the mechanical platform which increases testing time.
4. In addition to flash based FPGAs, SRAM FPGAs should be tested simultaneously. The testing of both flash and SRAM based FPGAs will provide an indication of the space radiation environment operating characteristics of each, allowing accurate comparisons between the two to be made. The available mitigation schemes for SRAM based FPGAs should also be tested to determine the effectiveness of these.
5. During testing, the maximum number of test boards should be used. The additional test boards will allow for more experimental results to be recorded and provide backup boards in the case a test board malfunctions. Multiple test boards can determine if anomalies in the output data are caused by the device or are as a result of the radiation.
6. For SEU testing, the angle of incidence can be adjusted to increase the effective thickness of the chip. This will result in a higher amount of deposited energy in the device and increase the number of SEUs during testing. Conducting SEU testing at various angles will provide additional data.
7. For TID testing, after initial testing the FPGA can be left to anneal at a predetermined temperature. The resulting performance characteristics of the FPGA after the annealing period should be recorded and compared to the testing characteristics. This provides valuable information of the annealing effects of TID testing and radiation exposure.
8. During SEU testing, it is advised to monitor the supply current of the FPGA. The current as a function of time during the testing will provide useful data when examining the behaviour of the device during irradiation and before failure.
9. Additional TID testing should be conducted with the use of a NI DAQ device with build in counters. With the use of this DAQ device, the percentage degradation of maximum

frequency as well as the percentage degradation of propagation delay can be determined. These results will allow for the analysis of the performance degradation due to the total absorbed dose.

7 References

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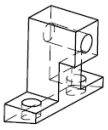
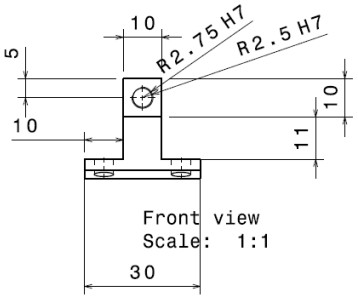
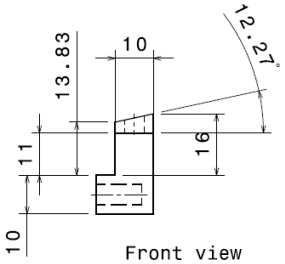
Appendix A



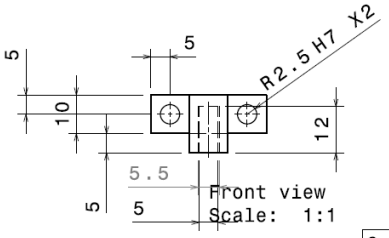
Isometric view
Scale: 1:1



Front view
Scale: 1:1

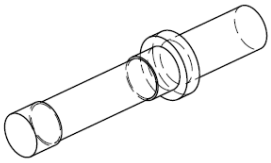


Front view
Scale: 1:1



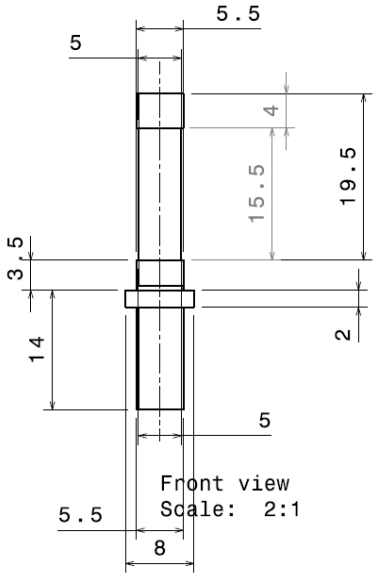
Front view
Scale: 1:1

Quantity	5
Material	Alu



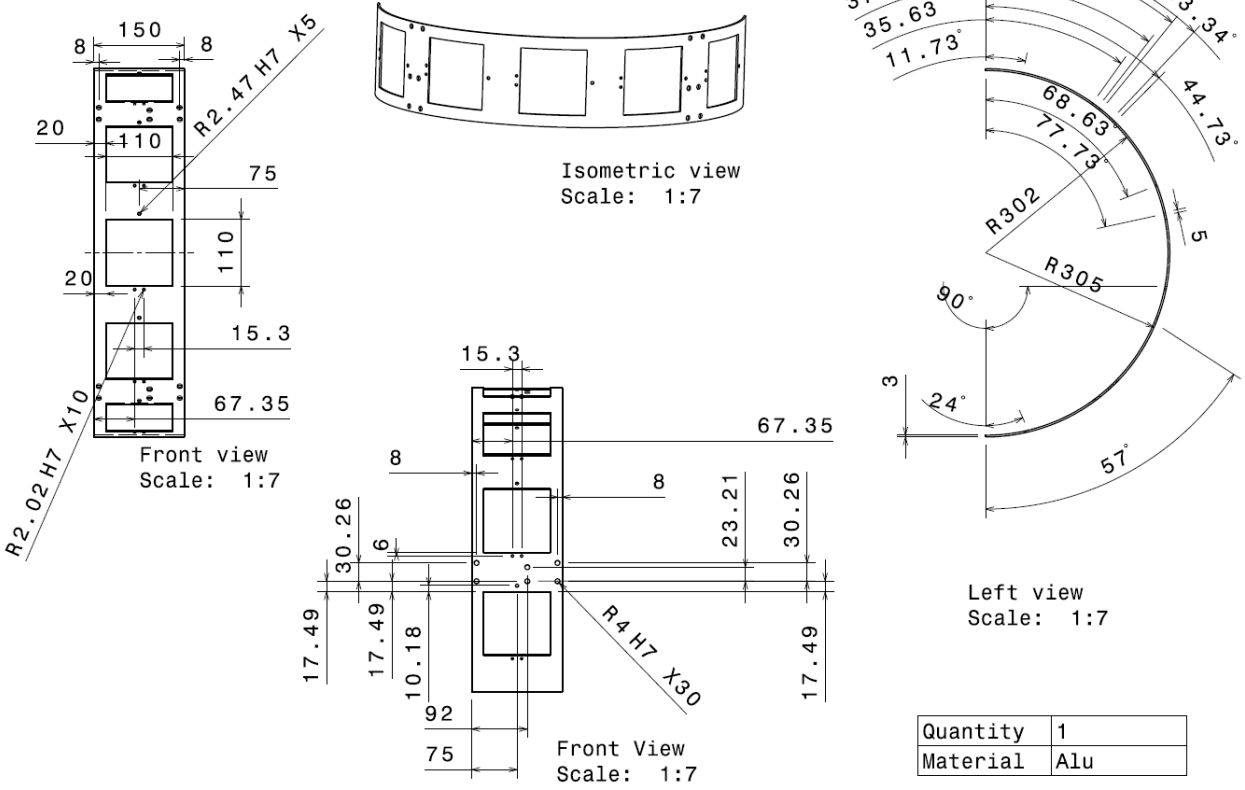
Isometric view
Scale: 2:1

Front view
Scale: 2:1

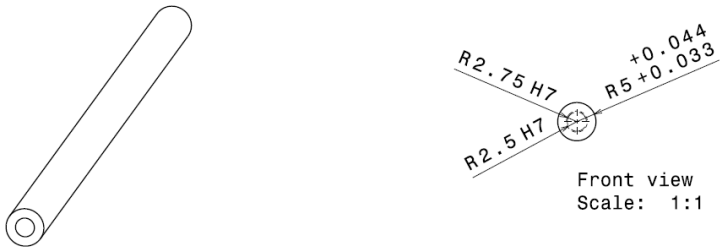


Front view
Scale: 2:1

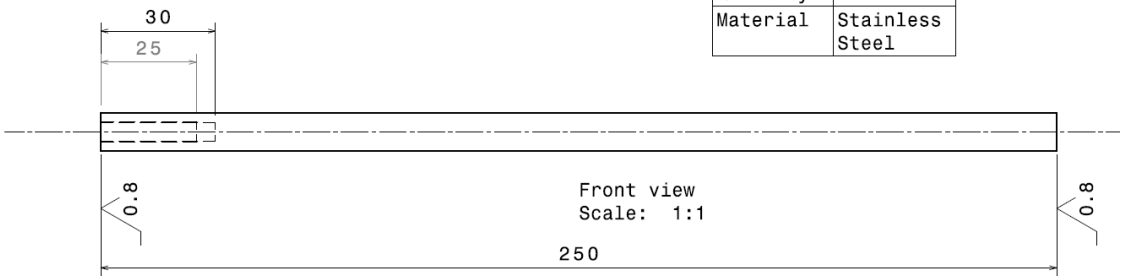
Quantity	5
Material	Stainless Steel

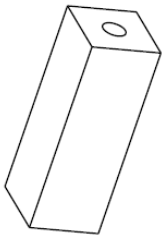


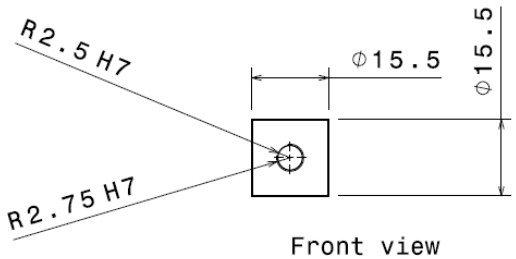
Quantity	1
Material	Alu



Quantity	4
Material	Stainless Steel

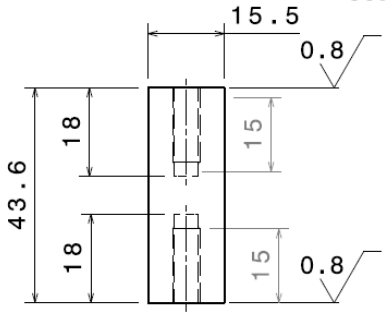






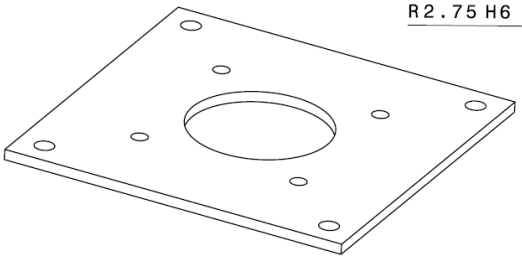
Front view
Scale: 1:1

Isometric view
Scale: 1:1

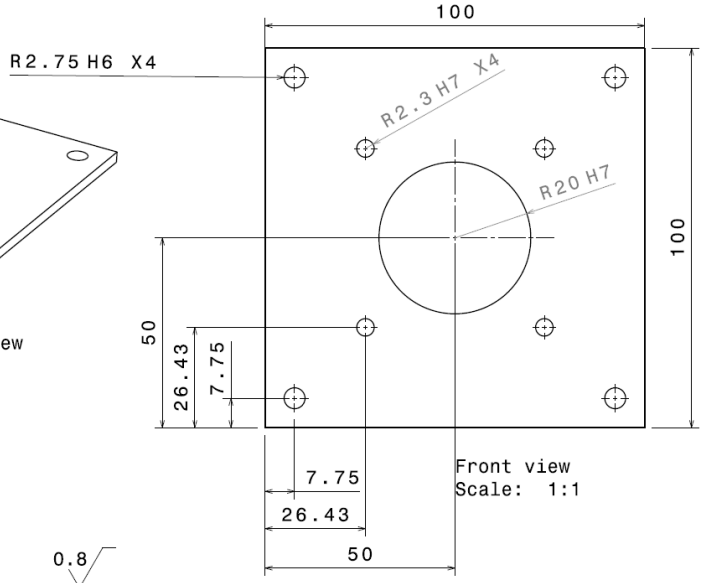


Front view
Scale: 1:1

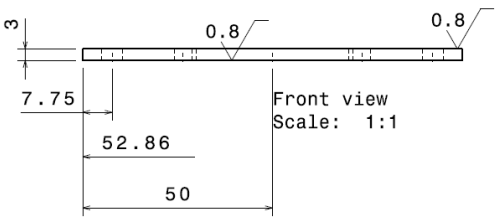
Quantity	8
Material	Alu



Isometric view
Scale: 1:1

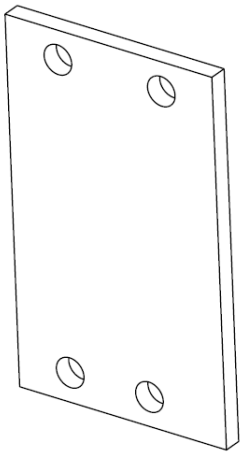


Front view
Scale: 1:1



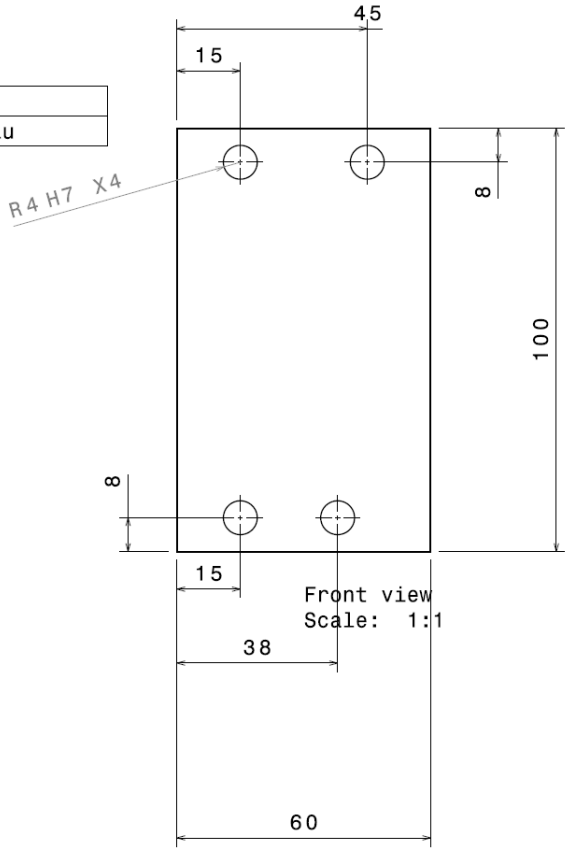
Front view
Scale: 1:1

Quantity	2
Material	Alu

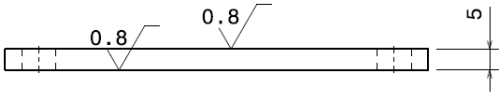


Isometric view
Scale: 1:1

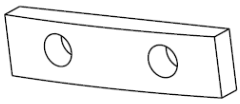
Quantity	2
Material	Alu



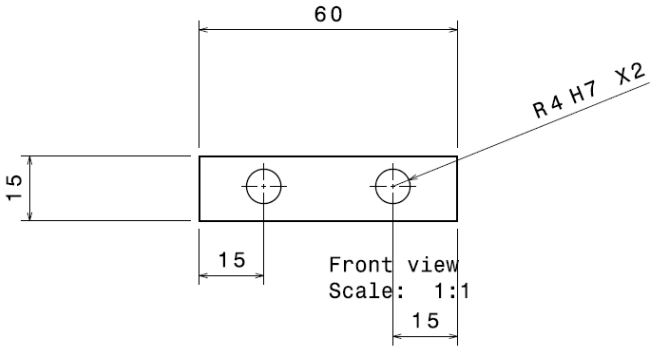
Front view
Scale: 1:1



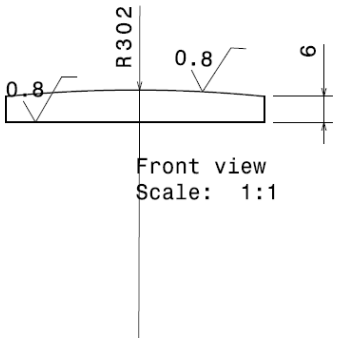
Front view
Scale: 1:1



Isometric view
Scale: 1:1

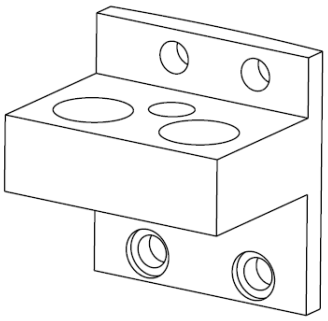


Front view
Scale: 1:1

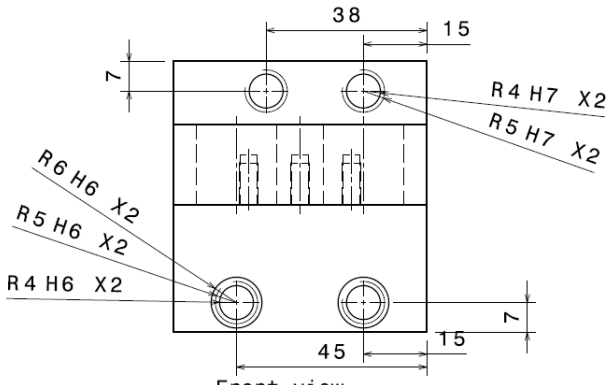


Front view
Scale: 1:1

Quantity	2
Material	Alu

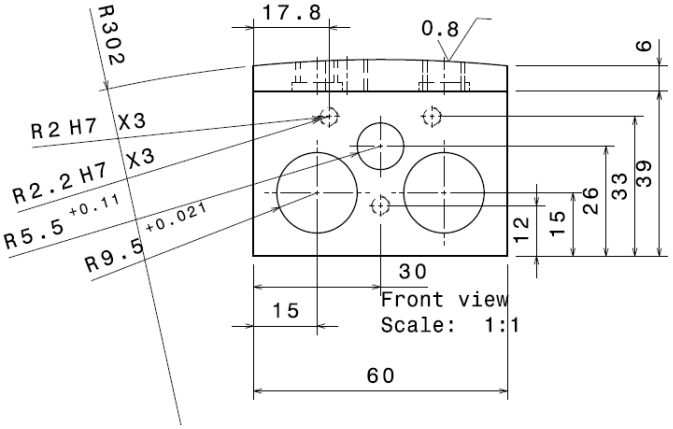


Isometric view
Scale: 1:1

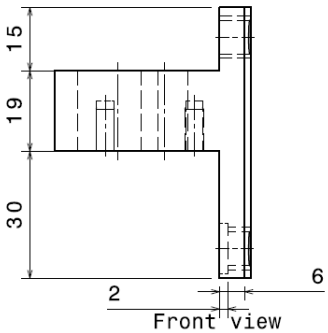


Front view
Scale: 1:1

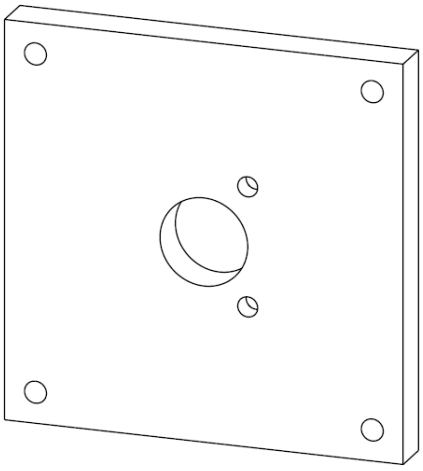
Quantity	2
Material	Alu



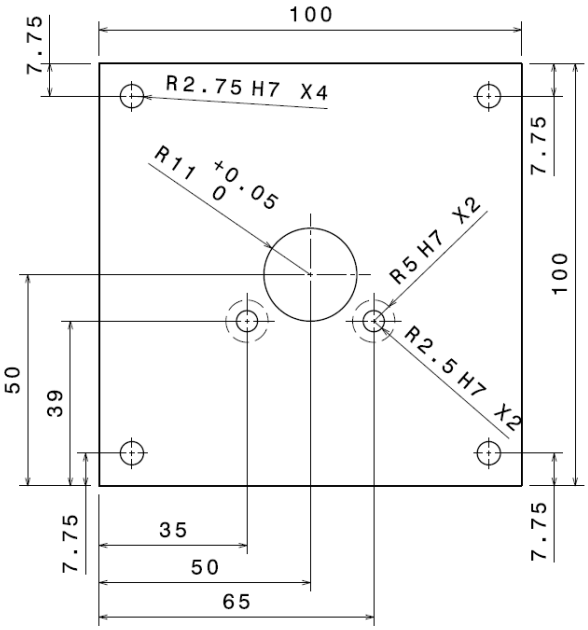
Front view
Scale: 1:1



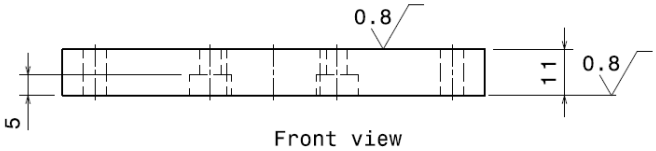
Front view
Scale: 1:1



Isometric view
Scale: 1:1

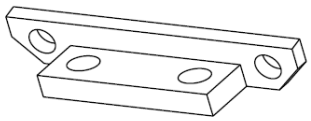


Front view
Scale: 1:1

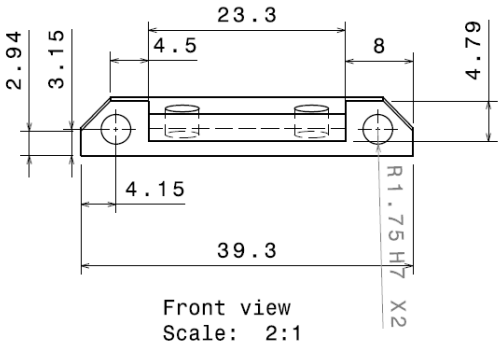


Front view
Scale: 1:1

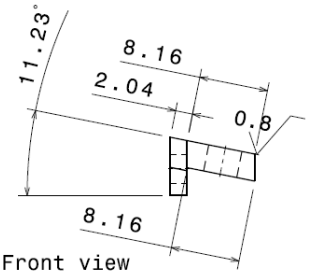
Quantity	2
Material	Alu



Isometric view
Scale: 2:1

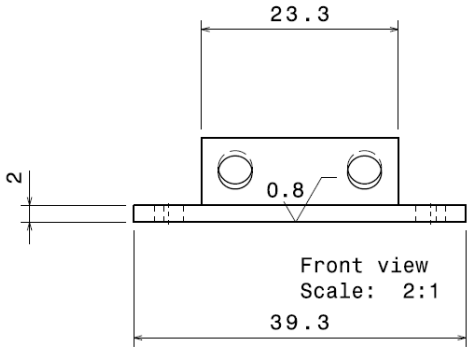


Front view
Scale: 2:1

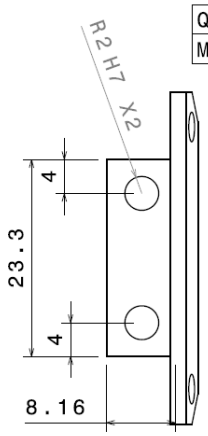


Front view
Scale: 2:1

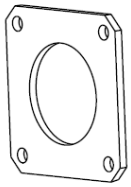
Quantity	5
Material	Alu



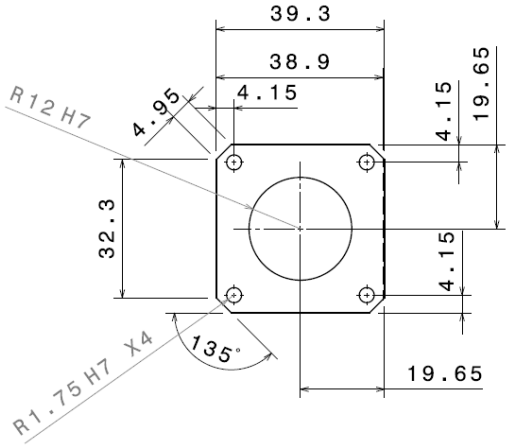
Front view
Scale: 2:1



Front view
Scale: 2:1

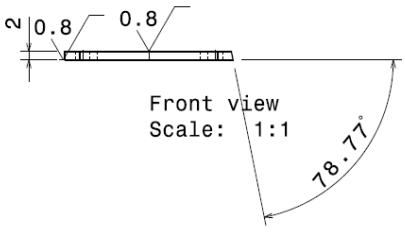


Isometric view
Scale: 1:1

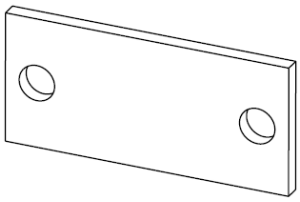


Front view
Scale: 1:1

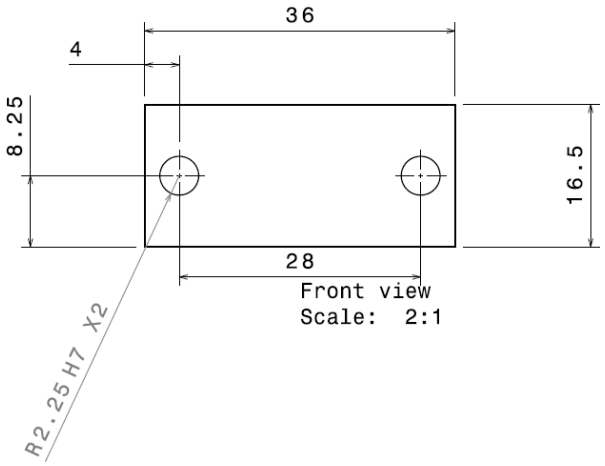
Quantity	5
Material	Alu



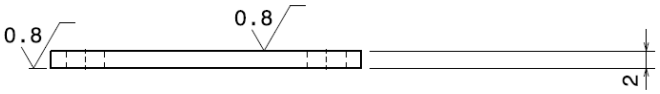
Front view
Scale: 1:1



Isometric view
Scale: 2:1

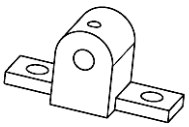


Front view
Scale: 2:1

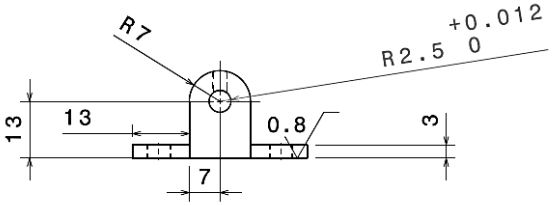


Front view
Scale: 2:1

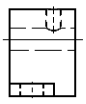
Quantity	5
Material	Alu



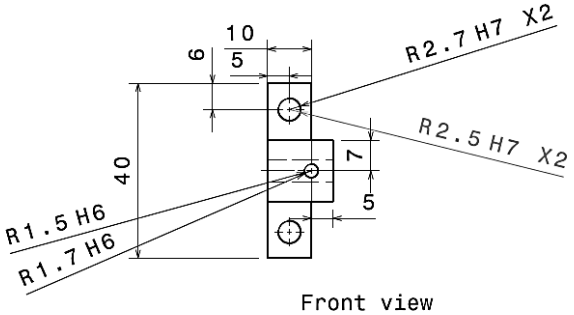
Isometric view
Scale: 1:1



Front view
Scale: 1:1

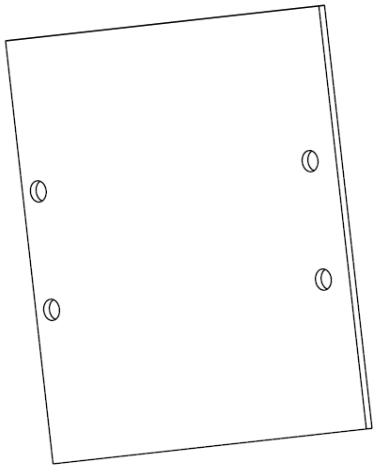


Front view
Scale: 1:1

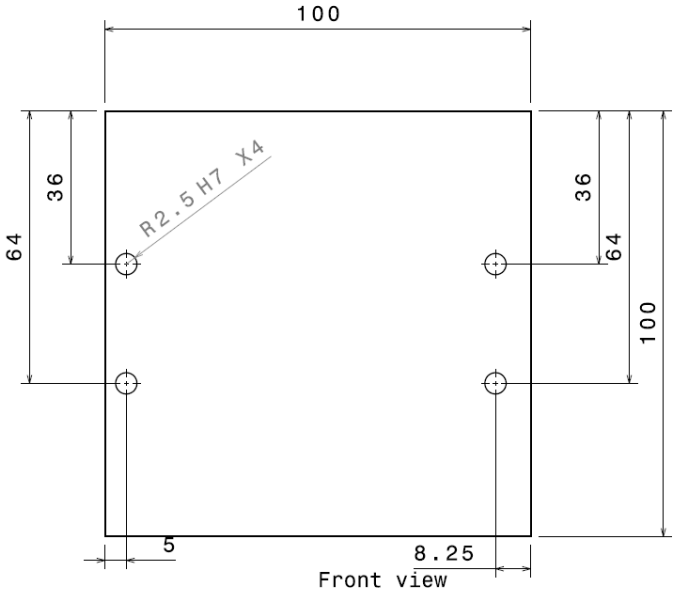


Front view
Scale: 1:1

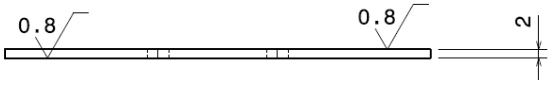
Quantity	5
Material	Alu



Isometric view
Scale: 1:1

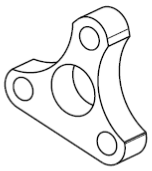


Front view
Scale: 1:1

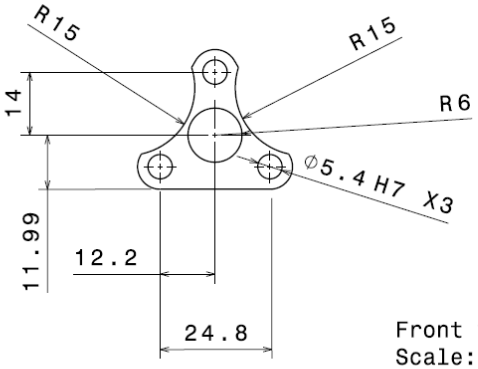


Front view
Scale: 1:1

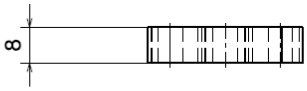
Quantity	5
Material	Alu



Isometric view
Scale: 1:1

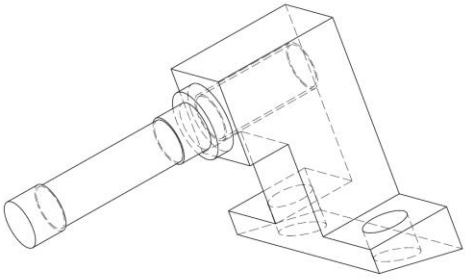


Front view
Scale: 1:1

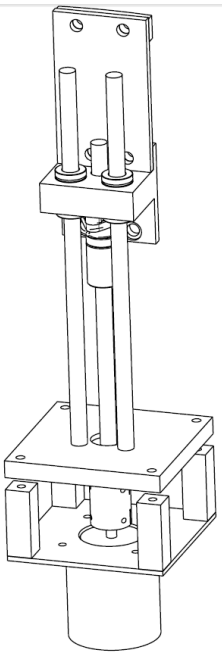


Front view
Scale: 1:1

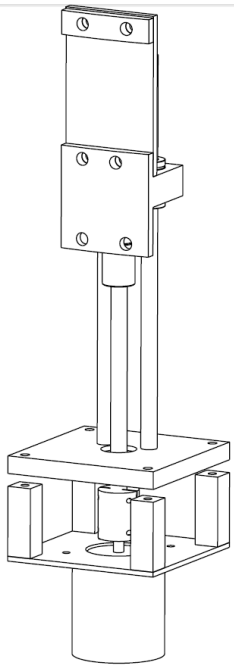
Quantity	2
Material	Al



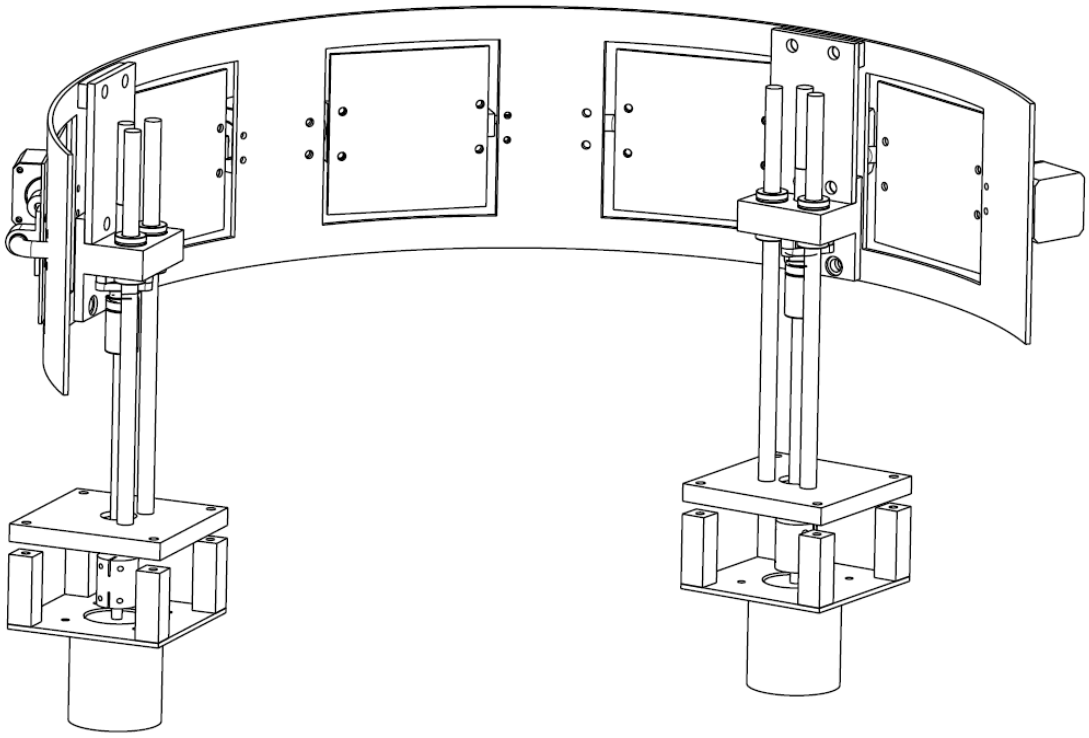
Isometric view
Scale: 4:1



Isometric view
Scale: 1:2



Isometric view
Scale: 1:2



Isometric view
Scale: 1:3

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EXAMINATION SECTION
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Nelson Mandela Metropolitan University
Port Elizabeth
6013

Enquiries: Postgraduate Examination Officer

Nelson Mandela Metropolitan University

for tomorrow

DECLARATION BY CANDIDATE

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STUDENT NUMBER: _____

QUALIFICATION: _____

TITLE OF PROJECT: _____

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DECLARATION:

In accordance with Rule G4.6.3, I hereby declare that the above-mentioned treatise/ dissertation/ thesis is my own work and that it has not previously been submitted for assessment to another University or for another qualification.

SIGNATURE: _____

DATE: _____