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ESTCUBE-1 ELECTRICAL POWER SYSTEM – DESIGN, IMPLEMENTATION AND TESTING

Bachelor's Thesis

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Tartu 2013

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Acronyms and abbreviations

ADC – analog-to-digital converter

ADCS – Attitude Determination and Control System

CAM – Camera subsystem

CDHS – Command and Data Handling System

COM – Communication subsystem

CPU – central processing unit

CSV – comma separated values

CTL – Subsystem Control Circuit

DAC – digital-to-analog converter

DC – direct current

DET – direct energy transfer

EEPROM – electrically erasable programmable read-only memory

EMI – electromagnetic interference

EPS – Electrical Power System

FRAM – ferroelectric random-access memory

GND - ground

GPIO – general purpose input output

GS – Ground Station

ICP – Internal Communication Protocol

JTAG – Joint Action Test Group

LDO – linear dropout

LEO – low earth orbit

MCU – Microcontroller Unit

MLCC – multilayer ceramic capacitor

MOSFET – metal-oxide-semiconductor field-effect transistor

MPB – Main Power Bus

MPP – maximum power point

MPPT – maximum power point tracking

NA – not available

NASA – National Aerospace Administration

PWM – pulse-width modulation

1. Introduction

ESTCube-1 is a 1 kg nanosatellite designed and built to test the electric solar wind sailing technology or E-sail. This thesis focuses on the development of the Electrical Power System (EPS) hardware for this satellite.

The EPS is the only source of electricity for the satellite while operating in space, therefore this system has to be reliable and robust. Designing hardware for space environment sets many constraints that are not relevant for instruments used on ground. Furthermore, the system has to meet the power needs of all other subsystems, fit into the tight-packed satellite structure and – due to limited communication windows – work autonomously most of the time, relying purely on sensor data when making decisions. All these requirements and operating conditions set very strict constraints on the system, making the design a nontrivial task.

Many people have contributed to the development of the EPS over the years; the author's task in the EPS team was to integrate all of the previous developments and finalize them into one functional module. This task also included testing the functionality of and characterizing the system.

The system described in this work features innovative solutions that have never been used onboard CubeSats before; for example, fully hardware based maximum power point tracking system. The design and preliminary results have been published [1] and presented at the 63rd International Astronautical Congress [2]. An article based on the testing results of the final hardware has been submitted for review for a special edition of Acta Astronautica that focuses on small spacecraft [3]. Future publications about the in-orbit performance of the system are currently being planned.

The main goals of this work were stated as follows:

- List the requirements for the electrical power supply of ESTCube-1 satellite;
- Design and build the subsystem hardware;
- Test and verify the functionality of the module.

Work presented in this thesis was conducted over a period of two years and will be continued in the future. During this period three revisions of the hardware were developed and tested. The result of the work was a flight-ready power system.

2. Overview

2.1. Overview of the ESTCube-1 mission

The Estonian Student Satellite project started at the University of Tartu in 2008. The main aim is to promote space technology and give students hands-on experience in researching and developing technologies and solutions for space use. Additionally, a scientific experiment was planned: a demonstration of an ambitious solar wind sailing technology (E-sail). To achieve these goals a spacecraft was built and launched into high inclination low-Earth orbit (LEO) with altitude of ~650 km. Over the past 5 years the project has grown into a full scale international cooperation involving students and institutes from several countries. [4]

The satellite (ESTCube-1) is a single unit (1 U) CubeSat: measuring 100 x 100 x 113 mm and weighing no more than 1.33 kg. The CubeSat standard was developed by California Polytechnic State University and Stanford University's Space Systems Development Laboratory in 1999. Their aim was and is to increase accessibility to space by providing a standardized picosatellite design. [5] It is estimated that about 70 CubeSats ranging from 1 U to 3 U have been launched since the development of the standard in 1999 [6].

During the E-sail technology demonstration, the satellite will be spun up to 1 rotation per second, and with the use of centrifugal force a 10 m long Heytether will be reeled out. Afterwards, the tether will be charged to high potential and according to theory, the generated electric field interacting with the Earth's ionospheric plasma should have a measurable effect on the satellite's angular velocity. This novel technology could enable faster and more affordable interplanetary and deep space travel. [7]

ESTCube-1 was launched on 6th of May 2013 from the Guiana Space Centre onboard the Vega rocket [8]. This was Vega's second flight and everything went according to plan: deployment of ESTCube-1 took place two hours after lift-off. Radio beacon was received during the first pass and two-way communication was established 48 hours after deployment as planned. As of May 14 the subsystems are being tested and the preparations for the scientific mission are on-going. [9]

2.2. Overview of previous Electrical Power Systems

To give an overview of previous power systems, a selection of successfully launched EPSs was chosen. Unfortunately many of the satellite teams have not published their designs; consequently the selection of satellites is limited. Power systems from the following satellites' were analysed: QuakeSat (Stanford University, 2003) [10] [11] [12], AAUSAT-1 (Aalborg University, 2003) [13] [14], Compass-1 (Aachen University, 2008) [15] [16], SwissCube-1 (École Polytechnique Fédérale de Lausanne, 2009) [17] [18], RAX-1 (University of Michigan, 2010) [19], and a commercial plug-and-play EPS from Clyde-Space [20].

The overall topology of the power systems has remained the same since the first CubeSats: systems are composed of solar panels for energy harvesting, batteries for energy storage, DC-DC converters for voltage regulation, and a distribution system to control the power flow to the consumers. Although the overall design has remained the same, different approaches have been taken to implement the aforementioned sections of the system.

Using photovoltaics is the most widely spread method of powering satellites in space. Different solar cell technologies are available, but onboard CubeSats GaAs-based cells are the most common. Survey conducted on pico- and nanosatellites (about half of which are CubeSats) in 2010 showed that if solar panels were used, 79% of them were GaAs-based [21]. Most importantly, these cells are highly efficient (up to 30%) [22]. Due to the limited area available on the sides of the CubeSat, some satellites use deployable solar arrays to increase energy production. The survey showed that 16% of the pico- and nanosatellites have used deployable panels [21].

To convert the energy collected by the solar panels into usable voltages, an energy conversion system has to be used. Most CubeSats use one of the three following systems: direct energy transfer (DET), fixed point controller or maximum power point tracking (MPPT) [23].

DET systems are the simplest; they interface the solar cells directly to the consumers and the energy storage system. Very little additional components are required, increasing the system's robustness. While being very simple, these systems force solar cells to operate in non-optimal conditions, which results in loss of efficiency [24]. DET-based systems have been used onboard QuakeSat and Compass-1.

Fixed point controllers monitor one point, usually set by voltage, on the solar panels' current-voltage-curve. These systems are more difficult to implement than DET-based systems, but

still much simpler than MPPT solutions. These kinds of solutions have been used on SwissCube-1 and RAX-1.

The MPPT-based systems utilise various algorithms to determine the maximum power point (MPP) and control the switching regulators between the cells and the load. This approach traditionally requires a microprocessor to acquire measurements, determine the MPP and adjust the conversion parameters accordingly, and a switching regulator to do the voltage conversion. These kinds of systems are more complicated to implement, but they also take into account the various environmental effects: temperature, incidence angle of the light, and radiation damage. [23] MPPT-based systems have been used on AAUSAT-1 and ClydeSpace's EPS.

The harvested energy is stored in rechargeable batteries to provide power during energy-negative operations or the eclipse phase of the orbit. Various configurations of lithium-ion (Li-ion) and lithium-polymer (Li-Po) batteries are used onboard CubeSats. These types of batteries are very widely used due to their high energy density and compact size; according to the survey 82% of pico- and nanosatellites have used lithium-based batteries [21]. The only known CubeSat to have flown without any batteries is Delft C³ [25]. Since Li batteries are sensitive to over- and undercharging, various protection systems have been implemented onboard CubeSats; dedicated chips are often used, but software-based solutions have also been used [15].

Voltage conversion is generally solved by using buck and/or boost switching regulators for larger loads and linear dropout (LDO) regulators or charge pumps for smaller loads. Switching converters can be very efficient (>80%) over a wide range of output currents and can be integrated into the system as a stand-alone solution. LDO regulators and charge pumps do not offer that high efficiency, but are simple to design in and take up very little board space. All compared satellites use similar switching regulator based solutions.

Energy harvesting, storage and distribution systems have been interfaced together using two different topologies: a regulated or an unregulated power bus [26]. A regulated bus can be directly used to power loads, but it suffers from reduced efficiency when charging and discharging batteries due to requiring separate regulators. An unregulated bus allows for higher efficiencies when storing energy, but requires additional voltage conversion to provide subsystems with stable voltages [26]. Unregulated buses have been used onboard QuakeSat, AAUSAT-1 and Compass-1. SwissCube-1 is an example of a regulated bus solution.

Power distribution is typically implemented by using a simple switching circuit. While plain MOSFETs can be and have been used for power switches [15], most systems use current-limited power switches. The latch-up triggers the current limit and the switch is turned off. After a period of time, the system is turned on again and normal operation is resumed. [27] A similar system is implemented on AAUSAT-1.

3. System requirements

3.1. Satellite architecture

The satellite is divided into subsystems based on their functionality:

- Attitude Determination and Control System (ADCS): contains magnetometers, gyroscopes and sun sensors for determining the satellite's attitude, and magnetic actuators for adjusting it.
- Camera subsystem (CAM): onboard camera system for Earth and tether endmass imaging [28].
- Command and Data Handling System (CDHS): the flight computer of the satellite.
- Communication subsystem (COM): provides two-way communication with the ground station.
- Electrical Power System (EPS): responsible for power harvesting, storage and distribution. Also controls the beacon of the satellite.
- Payload (PL): the E-sail technology demonstration package. Contains the unreeling mechanism, high voltage supply and electron emitters.
- Structure (STR): provides the mechanical structure of the satellite.

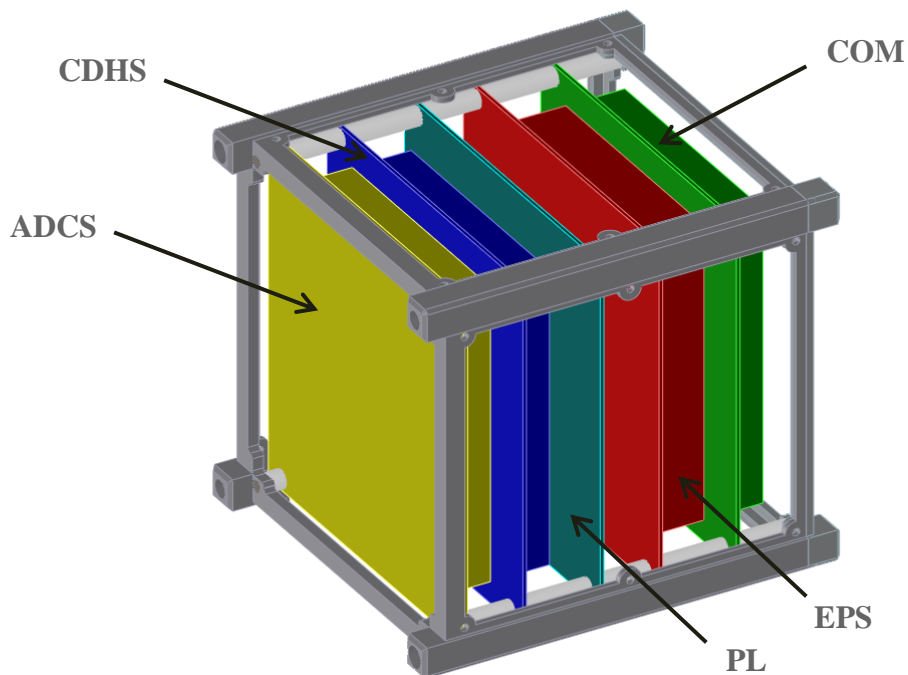


Figure 1. Satellite stack structure (ESTCube-1 STR team, 2010).

3.2. System requirements

During the early phases of satellite planning, the following tasks were assigned to the EPS:

- Energy generation and harvesting;
- Energy storage;
- Energy distribution within the satellite;
- Post deployment operations of the satellite;
- Controlling the beacon hardware on COM board;
- Driving the ADCS magnetic actuators;
- Protection of other subsystems from single event latch-ups (SEL) (section 3.3).

Additionally, the following requirements were posed by the CubeSat standard:

- No electronics or subsystems shall be active during the launch to prevent any interference with the launch vehicle or other payloads.
- CubeSat shall include at least one deployment switch to turn off satellite power completely.
- After satellite deployment there will be a delay period of 30 minutes before any deployable systems are activated.

Post deployment start-up sequence:

1. Satellite is powered on by the Sun.
2. Delay of 30 minutes before antennas are deployed.
3. Delay of 15 minutes before beacon transmissions start.
4. Delay of 48 hours before uplink is powered on.
5. Normal mode is activated on command from the ground station (GS).

Satellite operation modes:

- Normal mode – CDHS controls the satellite operations and composes normal mode beacon containing various information about satellite systems. Transition from normal mode to safe mode occurs on critical fault or on command from the ground station.
- Safe mode – only EPS and COM are powered on and normal mode is resumed on command from the ground station. Safe mode beacon, which contains EPS diagnostic data, is transmitted.

Figure 2 shows the subsystem voltage requirements and Table 1 shows the power requirements of the subsystems. This data was the basis for the EPS development.

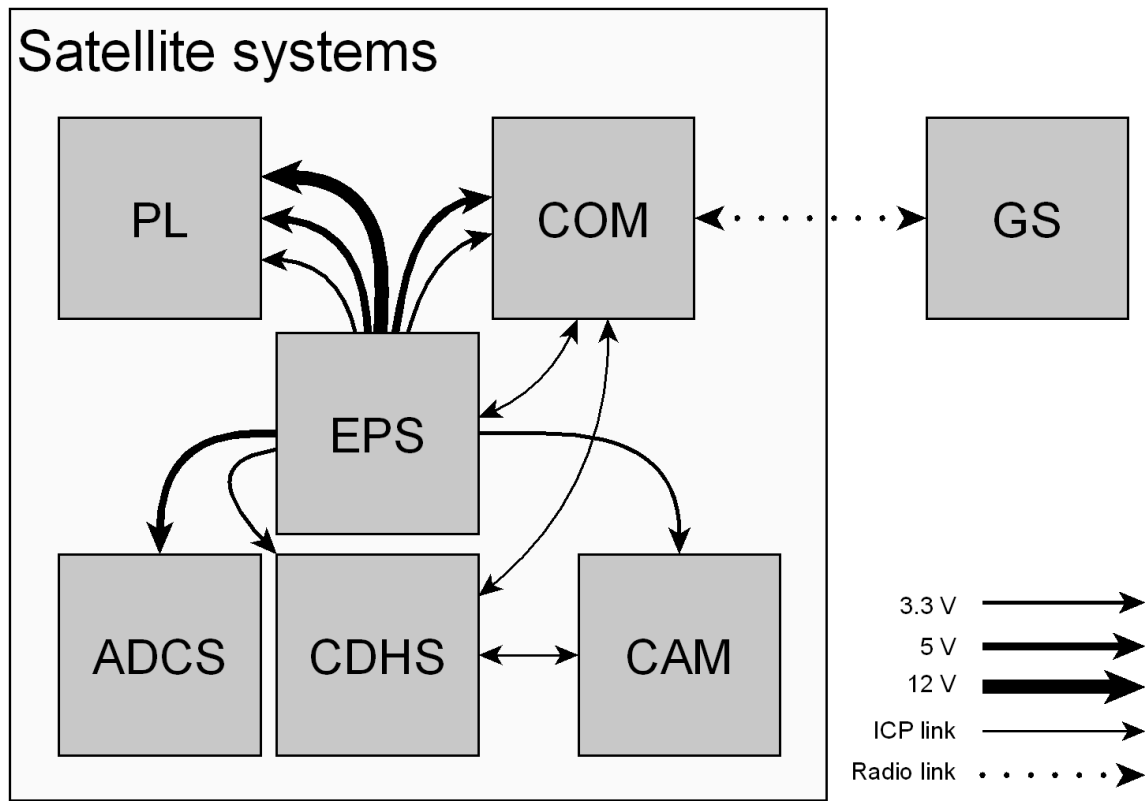


Figure 2. Satellite system diagram¹.

Table 1. Power requirements of the subsystems

| Satellite subsystem | Peak power (early estimate ² / final), mW | Orbit average power (early estimate ¹ / final), mW |
|---------------------------|---|--|
| ADCS sensors | 150 / 300 | * ³ |
| ADCS magnetic actuators | 700 / 840 | * |
| CAM | 300 / 300 | * |
| CDHS | 200 / 300 | 20 / 200 |
| COM | 2600 / 2000 | 310 / 550 |
| EPS control systems | NA / 200 | NA / 200 |
| PL | 6000 / 4200 | * |
| Antenna deployment system | 4200 / 4200 | * |

¹ Internal communication protocol (ICP)

² Based on ESTCube-1 phase B reports [53] [54].

³ Systems used only during specific mission phases, therefore do not have direct impact on the power budget.

3.3. Space environment hazards

Designing an instrument for use in space is not a trivial task. The device has to tolerate heavy mechanical loads during launch, only to end up in a hostile environment. These conditions can lead to progressive degradation of the onboard electrical and mechanical systems. The system has to endure vacuum, periodic thermal fluctuations, and cosmic radiation.

In vacuum, thermal convection is eliminated, and since heat radiation is inadequate for cooling devices, the only practical way to dissipate heat is through conduction. This reduces the amount of thermal energy that individual chips can dissipate and therefore may lead to overheating and thermal damage.

Periodic thermal fluctuations (thermal cycles) cause expansion and contraction of the various details used onboard the satellite; this can have effects on the mechanical integrity of the system, for example cracks in solder joints [29]. Proper equipment and methods have to be used to produce high quality solder joints that would withstand this kind of stress [30].

Radiation can have degrading or damaging effects on electronics. Parameters of electronic parts may drift due to long term radiation exposure – as the total ionizing dose (TID) increases, the performance of the device decreases. The degraded performance may present itself in many different ways, ranging from increase in power consumption to shift in logic levels. Yearly TID is highly dependent on orbit parameters and is very difficult to estimate beforehand. [31] [32] By adding shielding to the system, the yearly TID can be lowered. [33]

While TID has only degrading effects, the single event upsets (SEU), single event latch-ups (SEL) and single event burnouts (SEB) can cause permanent damage to the system. These effects are caused by heavy ions, protons and neutrons. SEUs and SELs can cause flipped bits or excessive current consumption, but can be recovered from by power-cycling the affected device. SEB effects are caused by high current state and are not recoverable. While shielding may be effective for mitigating TID effects, it has minimal impact on reducing single event rates. The effects can only be lessened by making the system more redundant, robust and adding latch-up protection systems. [31] [32] [34]

4. Measuring methods

To evaluate the performance of the EPS many sensors were designed into the system. Information about voltage, current and temperature can be collected from various parts of the system, giving a good overview of the performance. This section covers the problems and solutions related to the onboard measurement systems.

4.1. PC-based EPS module control and monitoring software

To improve the efficiency and workflow of the on-ground testing process, a software package had to be developed. The software has to perform the following tasks:

- Gather telemetry data from the hardware module.
- Display the data on screen.
- Log the gathered data in a file.
- Plot charts of the data gathered.
- Send commands to the hardware module.
- Operate in real-time.

Two solutions were considered: a LabVIEW-based solution and a dedicated application written in Java. LabView has built-in serial drivers, graph plotting functionality and a wide range of other ready-to-use features that would have to be implemented separately in the dedicated program. On the other hand, separate solution would have more flexibility (important, because many of the future requirements were unknown at that time), could be modified and recompiled with free software and the code could be reused in the future, for example in the mission control software. A Java-based application was chosen, because there were ready-made, easy to use packages for the functionalities that were missing: serial communication and graph plotting.

Telemetry data was composed into packets and transferred to the computer over a standard serial converter (UART to USB). The data was parsed by the program and then displayed onto the screen, giving an overview of the state of the system.

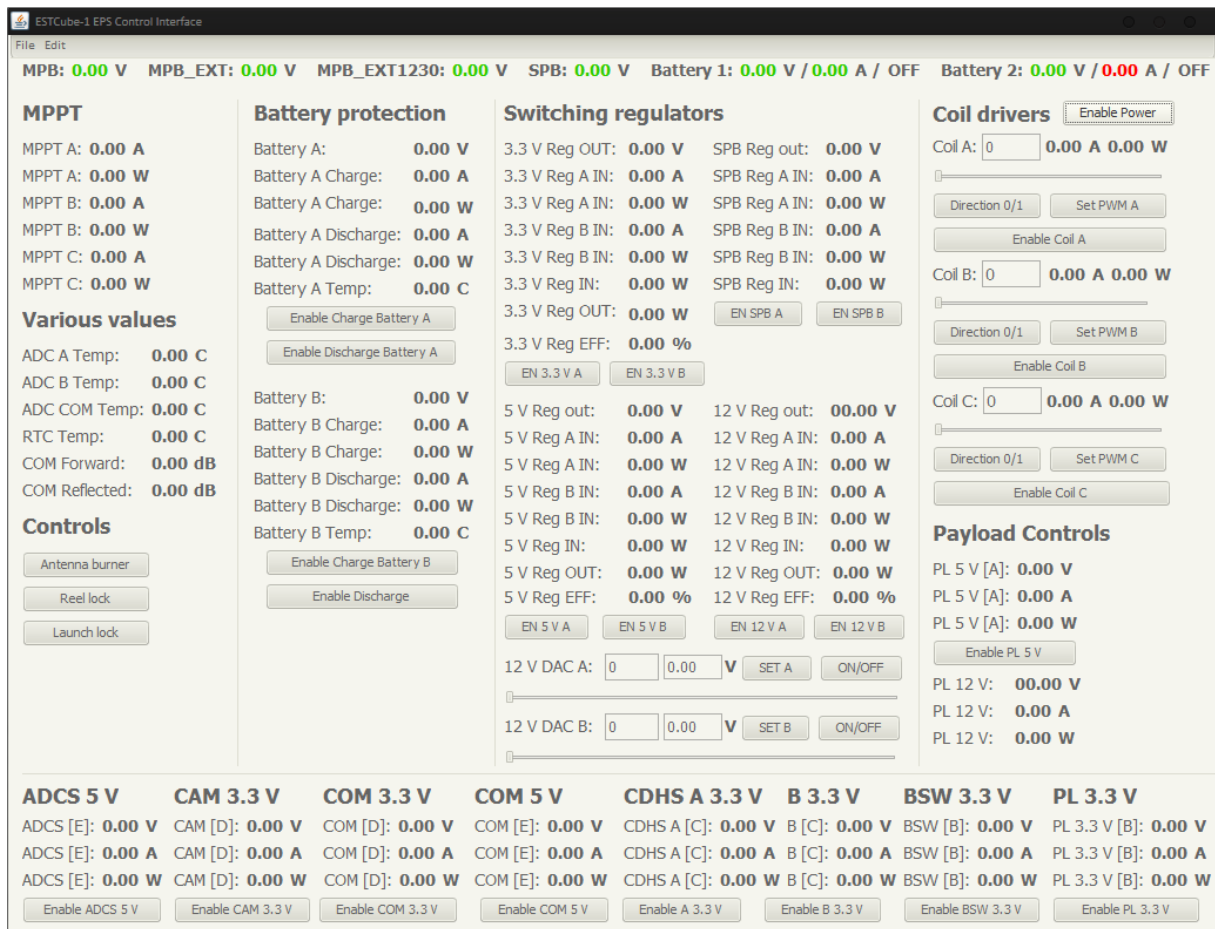


Figure 3. Screenshot of the EPS control and monitoring interface.

The program is capable of logging all the gathered data into a comma separated values (CSV) type file, making the data easily sharable and processable by third-party software. The time of taking the measurements is recorded and all the measurements receive a standardized UNIX timestamp.

The computer to subsystem communication is solved using standardized commands that utilise the same communication link. Functionality includes switching various devices on and off and changing operating parameters where possible.

To be able to convert the raw data gathered from the subsystem into human-readable format, a conversion system was added. There were two ways this could have been accomplished: one option was to do it purely mathematically based on the information in the datasheets and saving time, second option was to calibrate all measurement points against a precision measurement device, giving the best result. The calibration method was chosen, because this gave us more confidence in the results and also enabled us to test all measurement channels over their specified range, ensuring full functionality.

This specialized software was constantly improved throughout the module development process and proved to be a vital tool. Debugging and gathering data about the state of the hardware and software was effortless and enabled much higher productivity; purely writing down the measurement data manually would have consumed many more hours than it did with the automated measurement collection and conversion system.

4.2. Measurement and calibration devices

The EPS contains various measurement devices that were calibrated using precision instruments. The devices and the used equipment are listed below.

Measurement devices onboard:

- Linear Technology LT6105 precision current-sense chip;
- Maxim MAX1119 dual-channel 8-bit ADC with internal 4.096 V reference;
- Maxim MAX1230 16-channel 12-bit ADC with Analog Devices ADR3450ARJZ 5 V reference;
- Atmel AVR ATmega1280 internal 10-bit ADC with Maxim MAX6145 4.5 V reference.

Devices used for calibration and measurement process:

- Agilent 3458A 8.5 digit benchtop multimeter;
- Amprobe 37XR-A true RMS digital multimeter;
- Rhopoint M210 4-wire low resistance meter;
- Keithley 2303 power supply;
- Rohde-Schwarz RTO1014 oscilloscope;

4.3. Calibration of the measurement points

To be able to take precise measurements during the on-ground testing and in-orbit operations the measurement channels (these consist of analog-digital converters (ADCs) and current sense amplifiers for measuring currents) had to be calibrated. Calibrations were done using an 8½ digit Agilent 3458A multimeter and Keithley 2303 precision power supply. If the current exceeded 1.2 A, which is the current limit for the Agilent multimeter, Amprobe 37XR-A multimeter was used to measure the upper range. The calibration process resulted in slope

and intercept data for all the measurement points. The slope and intercept were determined using linear regression.

Calibration of the voltage measurement points was conducted according to this algorithm:

1. Solder in an external wire into the measurement point.
2. Connect a power supply and calibration multimeter to this wire.
3. Set starting voltage and write down ADC and multimeter values.
4. Increase / decrease voltage in steps and write down results until final voltage value is reached.
5. Estimate nonlinearity, calculate slope and intercept.

Calibration of the current measurement points was more complicated and to get correct results, the current was introduced into the shunt resistor in differential mode and it was ensured that no other current passed through the shunt. The current sense amplifier was powered from a separate source (see Figure 4).

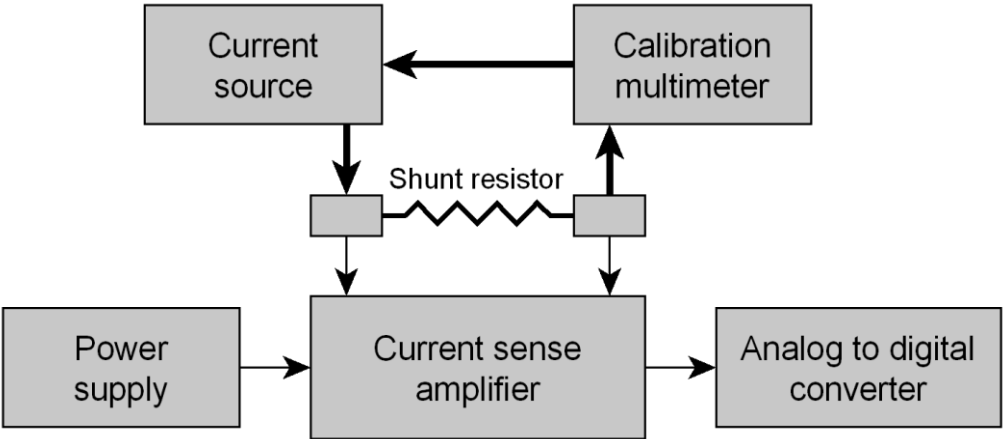


Figure 4. Current measurement setup.

Calibration of the current measurement points was conducted according to this algorithm:

1. Solder in wires to the shunt resistor contacts and current sense amplifier supply pin.
2. Connect the power supply, current source and calibration multimeter to the wires.
3. Set the current to zero and write down ADC and multimeter values.
4. Increase current in steps and write down results until final current value is reached.
5. Calculate nonlinearity, slope and intercept.

These operations were conducted on all 18 voltage and 27 current measurement points.

5. System implementation and testing

5.1. EPS block diagram

The system is composed of several components:

- Power harvesting system – contains the solar cells and circuitry to boost the voltage to usable levels, including MPPTs.
- Power storage system – contains the batteries and battery protection circuits; a dedicated protection circuit for both cells.
- Power distribution system – contains the regulators and individual subsystem switches.
- Second Power Bus (SPB) – a dedicated power rail for the microcontroller and its peripherals.
- Third power bus (TPB) – a dedicated power supply for state savers and digital-analog converters (DAC).
- Various release switches – switches for deploying the antennas and unlocking the payload systems.
- Magnetic actuator drivers – driver circuitry for controlling the magnetic torquers.

All these systems are connected together through the Main Power Bus (MPB), through which all of the satellite's power flows. The MPB is a battery-stabilized, but unregulated power bus.

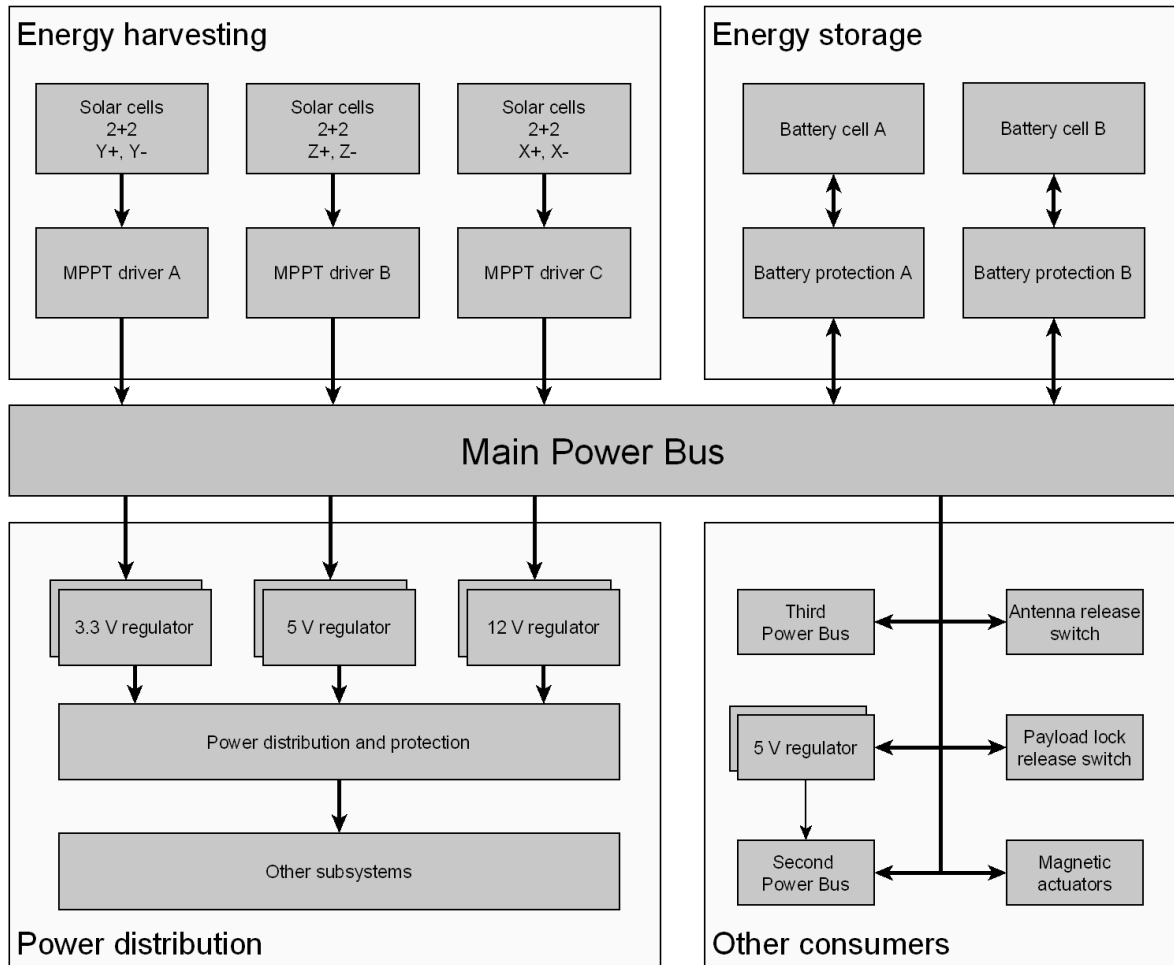


Figure 5. EPS system diagram (X, Y and Z denote axes).

5.2. Implementation overview

The satellite's structural design required that the overall height of the EPS must not exceed 21.5 mm. Main height defining components are the cylindrical batteries which are 18.6 mm in diameter [35]. Due to the high number of components involved, a two board solution was chosen. The batteries were placed in the middle of the system, so that the mass of the batteries would be as close to the real mass centre of the satellite as possible. This meant that one of the PCBs would have a rectangular slot in the middle, and on the other board, the area occupied by the batteries could not be used for components.

Next the functionalities were divided between the two boards. It was decided that all of the high current circuitry would go to one of the boards, and other power rails and the microprocessor with its peripherals would go the other board. Given that the power distribution board (PDU) board has about 3.5 times as many components as the

Microcontroller Unit (MCU) board, it was obvious that the MCU board would have the slot cut into it and the PDU board would stay intact.

Due to the space environment hazards discussed in paragraph 3.3 components used in the module were carefully picked. Automotive grade multilayer ceramic capacitors (MLCC) were chosen for all the power rails to ensure highest reliability. All integrated circuits used are either industrial or automotive grade, to ensure highest reliability possible. Most of the high power semiconductors used have integrated thermal protection circuits to protect the device from thermal damage.

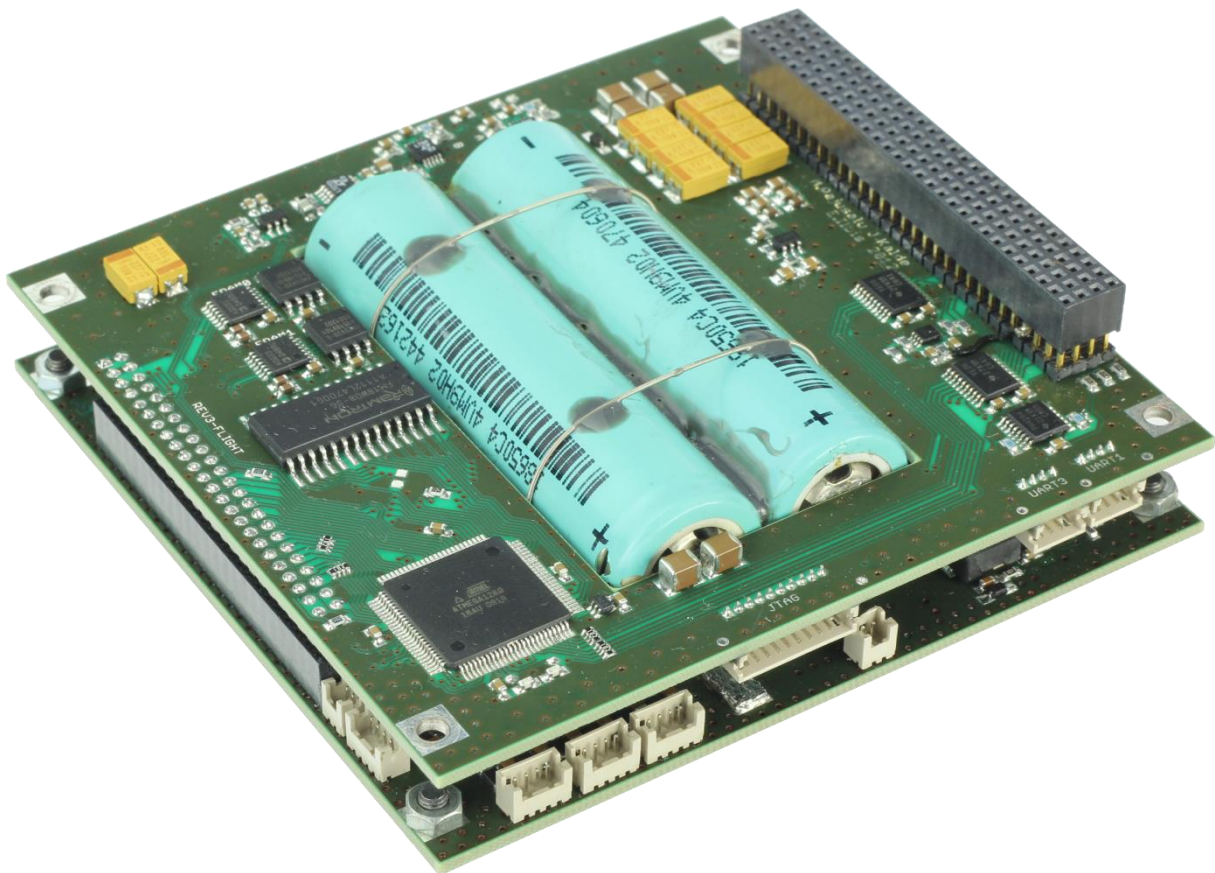


Figure 6. A photograph of the EPS module.

5.3. Power Distribution Unit (PDU)

Power Distribution unit is responsible for following functionalities in the EPS:

- Energy harvesting
- Energy storage including batteries
- Voltage regulation for other subsystems
- Subsystem management

- Driving magnetic actuators
- Antenna deployment switch

All this is composed onto the PDU PCB, making it the most complicated board in the satellite. The PCB is composed of 6 layers and contains 850-odd components. The functionality implemented on each layer is described below:

1. Top side - stack connector (A), CTL circuits (B), Switching regulator inductors (C), TPB connector (D), two Li-ion batteries (E), magnetic actuator connectors (F), the energy harvesting system and connectors (G), and EPS system bus connector (H). See Figure 7 below for a photograph, Figure 44 for Gerber view and Figure 52 for layout.

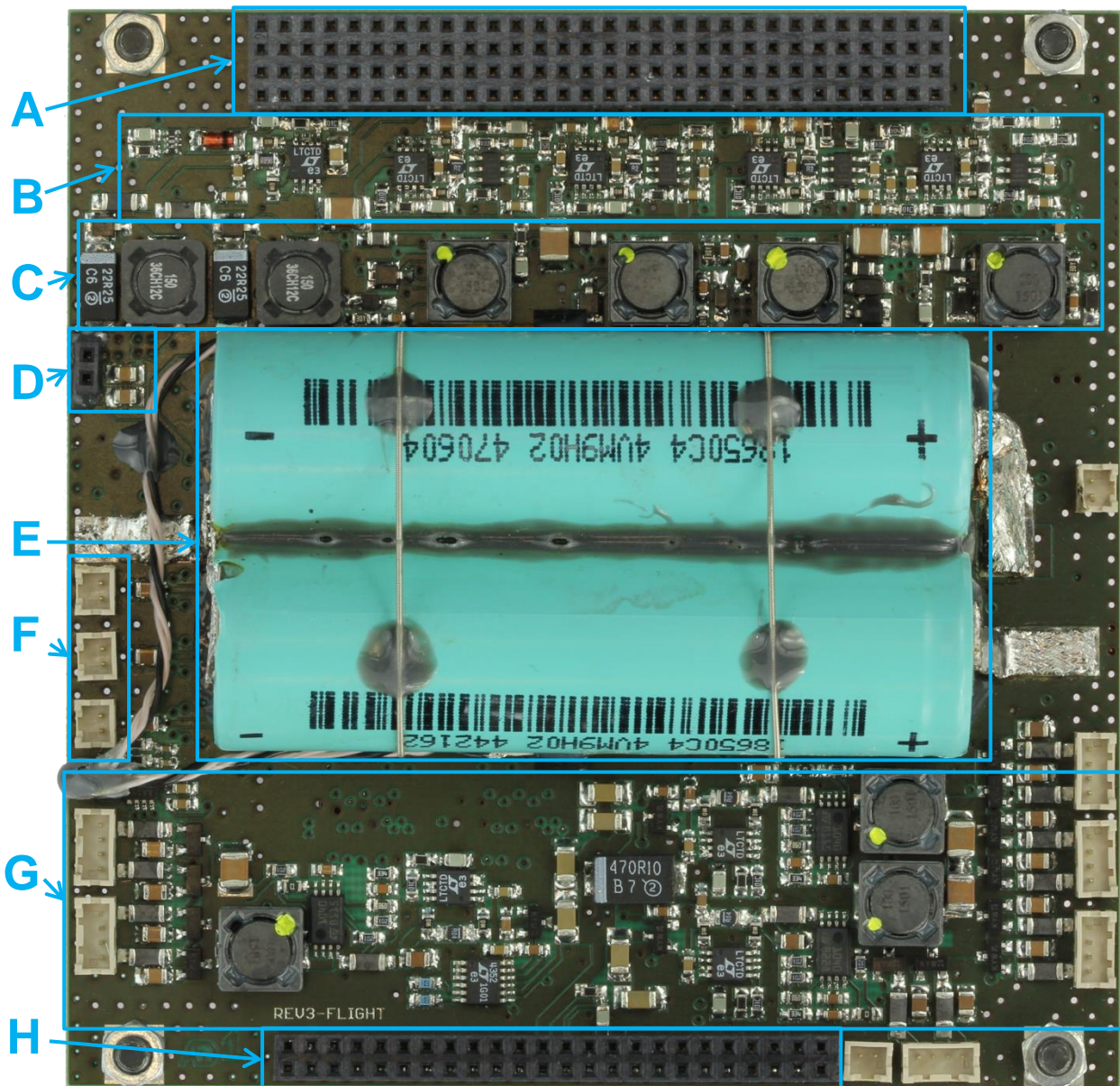


Figure 7. A photograph of the EPS PDU PCB top side.

- Bottom side - CTL circuits (A), switching regulator circuits (B), the MPB (C), battery protection circuits (D), energy harvesting support circuitry (E, G), external ADCs (F) and magnetic actuator driver circuits (H). See Figure 8 below for a photograph, Figure 45 for Gerber view and Figure 52 for layout.

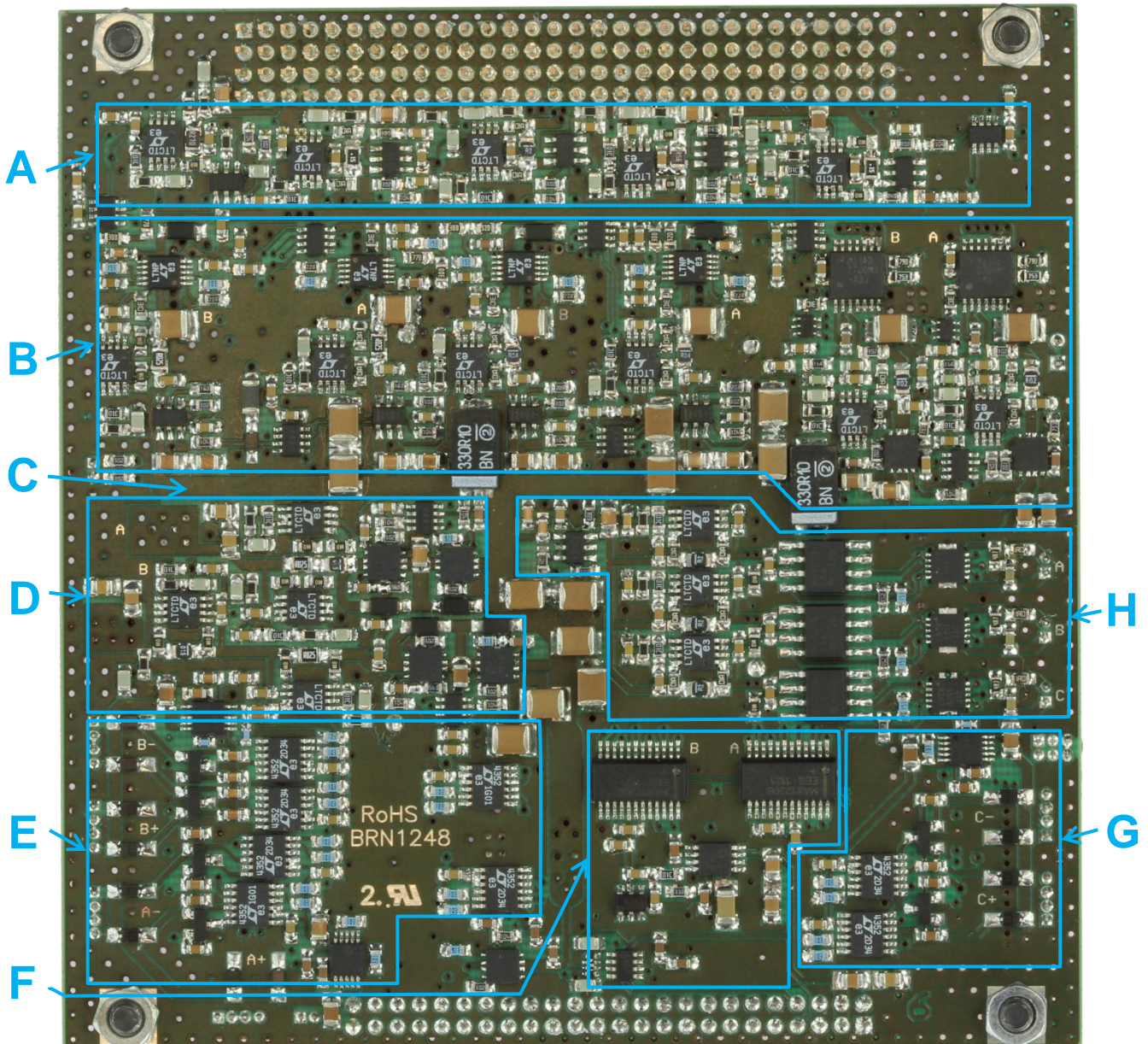


Figure 8. A photograph of the EPS PDU PCB bottom side.

- Internal layer 1 – dedicated ground (GND) layer (see Figure 46 for Gerber view).
- Internal layer 2 – GND and analog signals for ADCs (mostly vertical) (see Figure 47 for Gerber view).
- Internal layer 3 – GND and various digital signals (mostly horizontal) (see Figure 48 for Gerber view).

6. Internal layer 4 – GND and various digital signals (mostly vertical) (see Figure 49 for Gerber view).

To provide low impedance ground connections throughout the board, all of the layers contain a ground polygon where possible; most of the ground is inside the board due to component density on the outer layers. To further improve the ground plane, via stitching was used where possible. The ground plane resistance between opposing corners was measured and resulted in less than 10 mΩ. In addition, via stitching makes the board more resistant to external noise and reduces the electromagnetic noise emitted by the board itself due to via fencing. Due to the lack of space on outer layers and better noise immunity in the central layers, all of the measurement and controls signals were routed onto the internal layers. To reduce the crosstalk between the signals on adjacent layers the traces were routed in perpendicular directions.

To improve the mechanical robustness of the system and reduce the probability of a failure during launch, the batteries were tightly secured to the PCB using high-strength nickel plated steel wire. Special through-board holes were designed in to secure the wire by soldering. Furthermore the batteries were glued down using Scotch-Weld 2216 epoxy from 3M.

Many cables run into and out of the PDU board, therefore miniature connectors had to be used. DF13-series from Hirose was chosen; these connectors have low height profile, just 5.3 mm when mounted (vertical space between the two boards is 11 mm) and feature 1.25 mm pitch spacing, enabling high density connections. Same series connectors have been used in space before [36].

5.3.1. Main Power Bus (MPB)

The MPB is one of the most important power buses in the satellite and requires an adequate implementation to avoid critical failures. To achieve this, all consumers on the bus were separated from the power rail with current-limited power switches. Two exceptions were made: SPB supply through a diode and Third Power Bus charge pump input. These do not increase the risk factor, because even if one of the buses is lost, the satellite will cease to function anyway. For block diagram of the MPB, refer to Figure 5.

The MPB is designed to be as stable as possible; three different types of capacitance were connected to the rail: Li-ion batteries (through the battery protection system), solid tantalum capacitors and MLCCs. Combination of these three give a better frequency response over the whole range. Different capacitance values were used to further improve the noise filtering

performance. The capacitance banks are distributed strategically on the MPB to maximize the noise reduction and to minimize voltage fluctuations caused by current spikes. Ceramic capacitors were connected in series to improve reliability (this way two capacitors in series have to short out to cause a catastrophic failure); their combined capacitance adds around 200 μF to the bus capacitance. Solid tantalum capacitors were added mainly because of their bulk capacitance (total 1.13 mF with 3 capacitors). Due to space constraints, tantalum capacitors couldn't be connected in series; tantalum capacitors are proven to be very reliable, therefore the risk factory of this kind of design remains low [37].

5.3.2. Power harvesting system

The power harvesting system collects energy from 12 solar cells mounted on the 6 sides of the satellite and converts the voltage into usable levels by the satellite. The most effective way to collect solar power from the cells is by using a MPPT system [38]. Classically this system is implemented in the microcontroller software, but due to very complicated operations required, the calculations take up a lot of CPU time. These types of systems were also investigated [39], but an innovative alternative was chosen.

Our system uses a commercially available single-chip hardware solution – this device combines the power point tracking and conversion. This way the power harvesting doesn't depend on the processor, making the system more robust and freeing up valuable microcontroller resources. To further improve the redundancy and reliability of the system, there is a dedicated stand-alone circuit for each pair of cells on the opposing sides. Should one of these circuits fail, the other two will be unaffected and the power collection will not halt.

All the satellite's sides are covered with triple-junction GaAs based photovoltaic cells (3G30C from Azur Space) (two per side). These cells feature up to 30% efficiency and can provide maximum of 1.2 W of energy at reference conditions [22]. Each cell is connected to a driven MOSFET (aka. ideal diode) through a filtering circuit. This minimizes the unwanted noise, both captured and radiated by the solar panels. The diodes sum the solar cell outputs together and prevent the cells from becoming consumers when in the dark. Because the cells are wired in parallel and only produce 2.3 V on the output, ideal diodes (LTC4352 from Linear Technology) had to be used to minimize the power loss. The measured voltage drop on the ideal diode is only 20 mV at 0.5 A. Because the controller drives an external N-channel MOSFET and the input voltage is too low for the internal charge pump, a stand-alone charge

pump had to be used to power the driver. The charge pump is directly powered by the solar cells through regular low-dropout diodes.

After ideal diodes the power goes into a hardware MPPT driver (SPV1040 from ST). This chip provides a single chip solution for MPPT and step-up regulation to required voltage levels. The voltage is stepped to 4.17 V (determined by feedback circuit) from about 2.3 V and the measured efficiency from the solar cells to the MPB is 90%. Output current of the driver is measured for diagnostic purposes with resolution of 4.3 mA per bit. An additional ideal diode is connected to the output to prevent any reverse current problems when the regulator is not working.

To our knowledge, this kind of system has not been used in space before. A similar solution based on the same SPV1040 chips will be used on the FOX-1 satellite, due to launch in second half of 2013 [40].

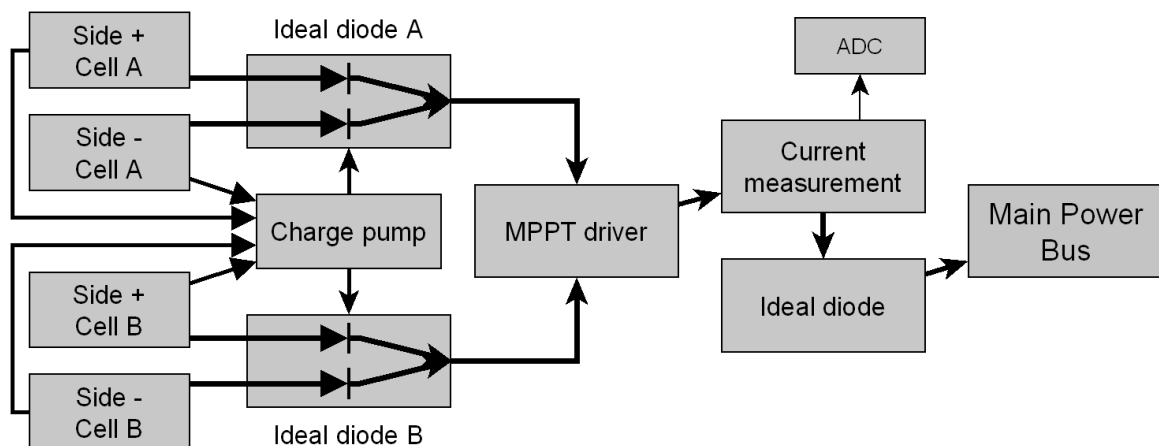


Figure 9. Power harvesting system topology.

5.3.3. Energy storage and battery protection

The energy storage system is composed of the batteries and the circuits to protect them. The system is designed to protect the batteries from the consumers and *vice versa*. Each cell has a dedicated protection circuit. This adds an additional layer of redundancy and robustness; should one cell fail, the other will be unaffected and normal operation is still possible.

The energy is stored in cylindrical high-capacity lithium-ion battery cells (CGR18650C form Panasonic) [35]. These cells have been flight proven onboard the AAUSAT-II and have been functioning for 5 years [41] [42]. They were also extensively tested in-house along with alternatives [43]. These cells can provide up to 12 Wh of energy storage at temperatures

between -5 to +5 °C [43]. Both cells have dedicated temperature sensors for monitoring and diagnostic purposes.

Telemetry data from the cells is constantly collected. Cell voltages, charge and discharge currents are monitored by the EPS microcontroller to provide under- and overvoltage as well as overcurrent protection in software. Software implementation enables us to adjust the thresholds in-orbit, thus making the system very flexible. The voltages are measured with a resolution of 18 mV per bit, giving a precise overview of the cell voltage at all times. This provides the input for power balance calculations. From this we can see whether the satellite is in power-positive or power-negative mode during different mission phases. This could also provide input for future missions, making it a very important feature. Battery related measurements are done by the microcontrollers internal ADC to not be dependent on external devices for the information.

A main switching block separates the batteries from the MPB. TPS2557 switches from Texas Instruments are used for this purpose because of their high current throughput. Switches' hardware current limits are programmed to 1.7 A for discharge and 1 A for charge. The voltage drop of the whole system is only 20 mV during normal operations; therefore the power loss is negligible. Figure 10 below shows the block diagram of the battery protection system.

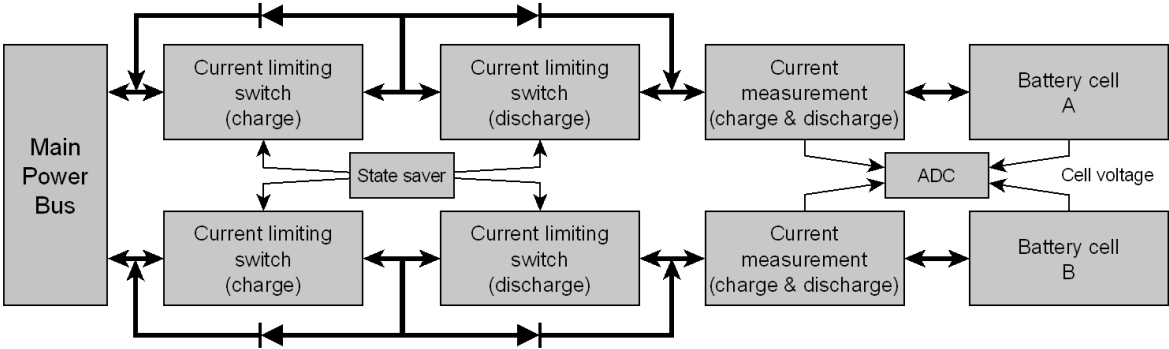


Figure 10. Battery protection system topology.

5.3.4. Regulators and power distribution

To be able to distribute the energy within satellite, a power regulation and distribution system had to be implemented. Subsystems onboard require three different voltage lines for operation: 3.3 V, 5 V and 12 V. For the block diagram of the regulators refer to Figure 12. Schematic drawings are provided in the Appendix 1.

All the regulator circuits are connected to the MPB through power switches (TPS2551 or TPS2557 from Texas Instruments) which feature current limiting and auto-reset functionality [44] [45]. The main purpose of these switches is to protect the MPB from non-functional regulators shorting it out. Additionally this gives the circuit a degree of protection from single-event latch-ups – should the circuit reach the current limit during operation, the power is shortly interrupted by the switch and then restored, effectively restarting the regulator. Overcurrent shutoff activates within few milliseconds, minimizing the possibility of the shorted out component suffering from permanent damage. The current tripping point is adjustable by a resistor and the values have been optimized according to the maximum current required by the regulator at any time during normal operation. Table 2 below shows the current limits and selected resistors for different regulator circuits.

Table 2. Regulator input current limiting resistors

| Switch location | Current limit (A) | Resistor (k Ω) |
|------------------|-------------------|------------------------|
| REG 3.3 V A/B IN | 0.6 | 22 |
| REG 5 V A/B IN | 0.9 | 16 |
| REG 12 V A/B IN | 1.3 | 75 |

The current flowing into the regulator is measured using a specialized high precision current sense amplifier (LT6105 from Linear Technology) and because the gain of the amplifier can be adjusted up to 100, a low value shunt resistor can be used. This minimizes the power loss and voltage drop on the resistor. The output of the current sense amplifier has an RC low-pass filter (the cut-off frequency is set to 0.75 KHz) on it to remove any unwanted noise before passing to signal to the ADC. For every circuit, a shunt resistor with specific value was chosen according to the maximum current passing through at any time during the normal operation – utilising as much of the ADC range as possible. The LT6105 chips are powered from the MPB and this limits their maximum output voltage to 2.6V in the worst case (the MPB being 3.5 V) due to saturation voltage [46]. Requiring full measurement range even in the worst case, the shunt resistor selection was mostly limited by this factor. Table 6 shows the selected resistor values, required maximum current, maximum measureable current at worst case conditions and the resolution of the measurements for different regulator circuits.

The DC-DC regulators chosen for the system have been previously tested separately from the whole system [47]. The 3.3 V and 5 V regulators use the same high efficiency buck-boost switching regulator controller (LTC3440 from Linear Technology). Because the LTC3440 is

not capable of delivering a 12 V output, an alternative boost-only switching regulator was chosen (LM2700 from National Semiconductor). The LTC3440 operates on 300 KHz and the LM2700 on 600 KHz, due to high operating frequencies smaller power inductors could be used thus making the PCB footprint smaller. To minimize the electromagnetic interference (EMI) coming from the inductors, all regulators use magnetically shielded inductors.

To improve the redundancy of the whole system, each regulator circuit (with current limiting and sensing) was duplicated and the outputs connected together to allow for a hot-redundant system. Both regulators are on at the same time and should one of the regulators fail: the other will immediately take over (see Figure 11). This way the downtime of subsystems is avoided. To implement this system, a set of additional diodes had to be added into the outputs of the regulators due to regulator controller design. To compensate the voltage drop on the diodes, the feedback voltage for the regulators was taken from the diode output. To minimize the power loss, low voltage drop diodes (CRS06 from Toshiba) were selected. During normal operation the load on 3.3 V rail is around 90 mA (300 mW) and the power loss on the diode around 22 mW, resulting in power loss about 7%. 5 V rail is usually turned off, but during beacon downlink (2 W, 25% of orbit) the loss on the beacon is around 120 mW, contributing 6% to total loss. Alternatively this system could have been solved with specialized power summing chips, but these were not available during the system design phase and they would have required further testing to ensure their robustness and reliability.

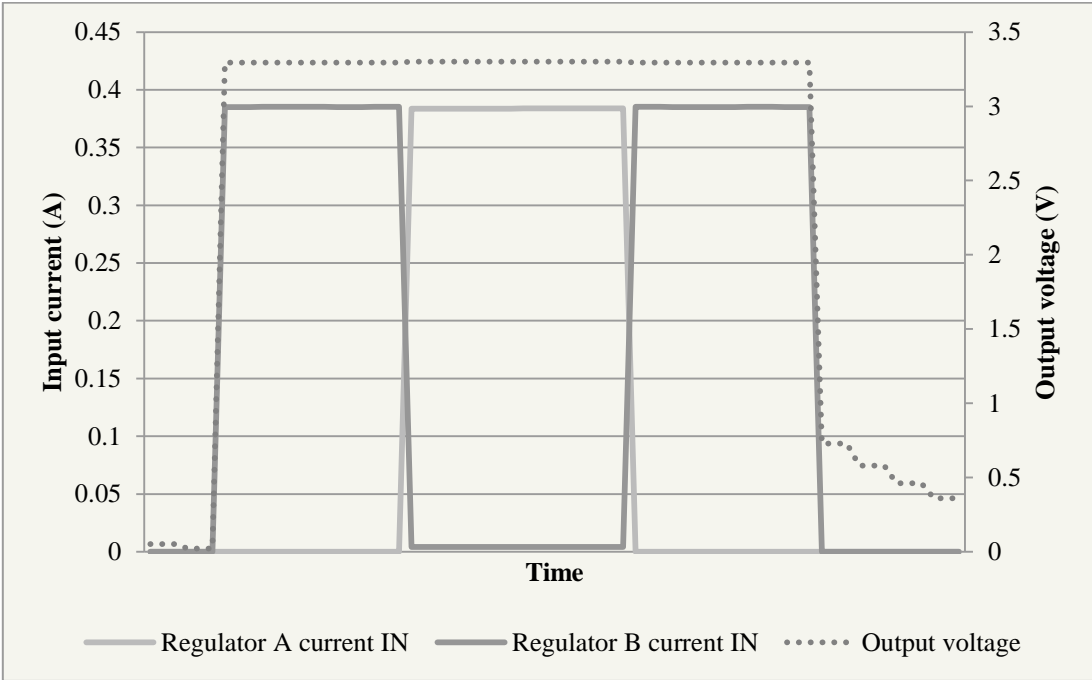


Figure 11. Hot-redundancy of the regulators (3.3 V regulator output).

The regulator outputs are measured and monitored by the microcontroller to ensure that the output voltage is correct all times. Because the input and output voltages and currents are measured, the efficiency of the regulator can be calculated on-the-fly.

The regulator efficiency curves were measured again to have more accurate power model of the satellite and to ensure that the regulators and the measurement system properly functions over the full required range. Table 3 summarizes the efficiencies and full efficiency graphs are available in the Appendix 4.

Table 3. Measured regulator efficiencies

| Regulator and load | Efficiency A/B (4.2 V IN) (%) | Efficiency A/B (4 V IN) (%) | Efficiency A/B (3.7 V IN) (%) |
|--------------------|----------------------------------|--------------------------------|----------------------------------|
| 3.3 V @ 100 mA | 91/90 | 91/91 | 92/91 |
| 3.3 V @ 200 mA | 88/89 | 89/89 | 89/88 |
| 3.3 V @ 300 mA | 87/86 | 87/86 | 86/86 |
| 5 V @ 150 mA | 88/88 | 87/88 | 86/86 |
| 5 V @ 300 mA | 85/85 | 84/84 | 82/82 |
| 5 V @ 450 mA | 82/81 | 80/80 | 77/77 |
| 12 V @ 150 mA | 86/91 | 86/91 | 85/90 |
| 12 V @ 300 mA | 83/85 | 82/84 | 81/83 |

From the table and the graphs we can see that the overall average regulation efficiency is 85%. If the hot-redundancy feature with additional diodes were to be removed, the efficiency of 3.3 V and 5 V regulation could be increased by further few per cent. When decreasing the input voltage from 4.2 V to 3.7 V, the efficiency of the 3.3 V regulators did not change notably, but the efficiency of the 5 V regulator decreased 2-5%. We can see that all of the LTC3440-based regulators are quite similar efficiency-wise; thus one regulator doesn't have to be preferred over the other. Due to 12 V regulators' different conversion efficiencies and the rail not being used in hot-redundant configuration, the more efficient regulator will be preferred and the other one will be kept as a backup. In addition, the 12 V regulators have external DAC converters tied into the feedback pin. This enables regulation of the output voltage within $\pm 10\%$. This feature was requested by the E-sail experiment.

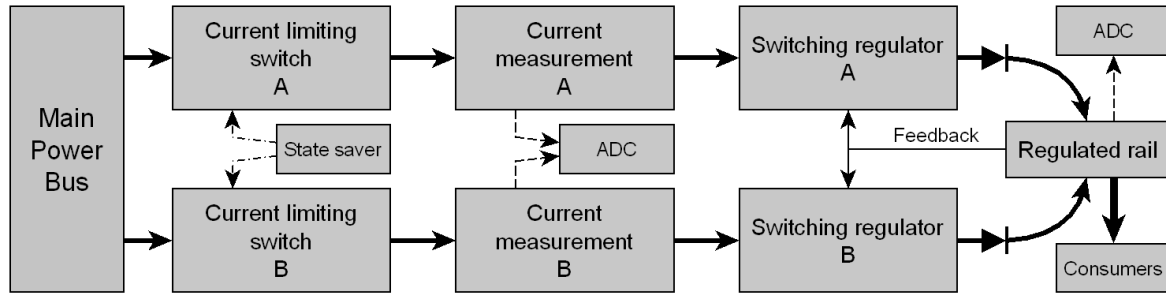


Figure 12. Regulator circuit topology.

5.3.5. Subsystem Control Circuits (CTL)

The CTLs have the task of isolating the subsystems from the regulator outputs. If one of the subsystems were to fail and cause a short, this would not have catastrophic effect on the regulated converter output and the other subsystems powered from the same rail. Similarly to the regulator circuits, the circuits are implemented using TPS 2551 power switches. Each subsystem's CTL(s) current limit was set considering the peak consumption and safety margin. This system also provides protection from the SEL effects by recycling power in case of overcurrent. Table 4 illustrates the current limits and resistors used.

Table 4. CTL current limiting resistors⁴

| Subsystem power rail | Resistor (k Ω) | Current limit (A) |
|----------------------|------------------------|-------------------|
| ADCS | 75 | 0.12 |
| CAM | 75 | 0.12 |
| CDHS A, B, BSW | 75 | 0.12 |
| COM 3.3 V | 62 | 0.15 |
| COM 5 V | 24 | 0.5 |
| PL 3.3 V | 75 | 0.12 |
| PL 5 V | 43 | 0.25 |

The passing current and the output voltage of each CTL can be measured independently. This gives us a very wide range of diagnostic data and enables us to do regulator efficiency calculations, monitor each subsystem independently and identify faults, i.e. high current consumption, output voltage drops, changes in power consumption over time etc. The output

⁴ 12 V rail has only one consumer on it, therefore current limiting is done by the regulator input TPS2557

voltage is measured with a resolution of 1.2 mV per bit and current measurement resolutions and values are shown in the.

Very low value shunt resistors could be used, thus minimizing the power loss on sensing resistors. The degree of measurement accuracy enables us to keep very fine track over the power consumption and may also enable us to see system aging over time.

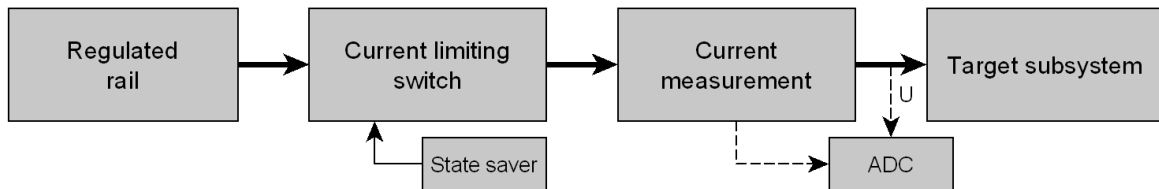


Figure 13. CTL circuit topology.

5.3.6. The magnetic actuators' drivers

The magnetic actuators' drivers are part of the ADCS, but implemented on the EPS board so that the MPB could be used to power them. This implementation allows the satellite to use energy more effectively and reduces the current requirements for the regulators. The driving system is separated from the MPB by a TPS2551 switch. Current going into every driver is measured to give feedback to the ADCS system. An Allegro A3901 motor driver is used to drive the magnetic actuators. Control signals for the driver originate from the EPS processor and duty cycle data originates from CDHS processors which is responsible for the ADCS calculations. Driving frequency is fixed to 32 kHz; low value was selected to reduce EMI problems. Figure 14 below shows the coil driver design.

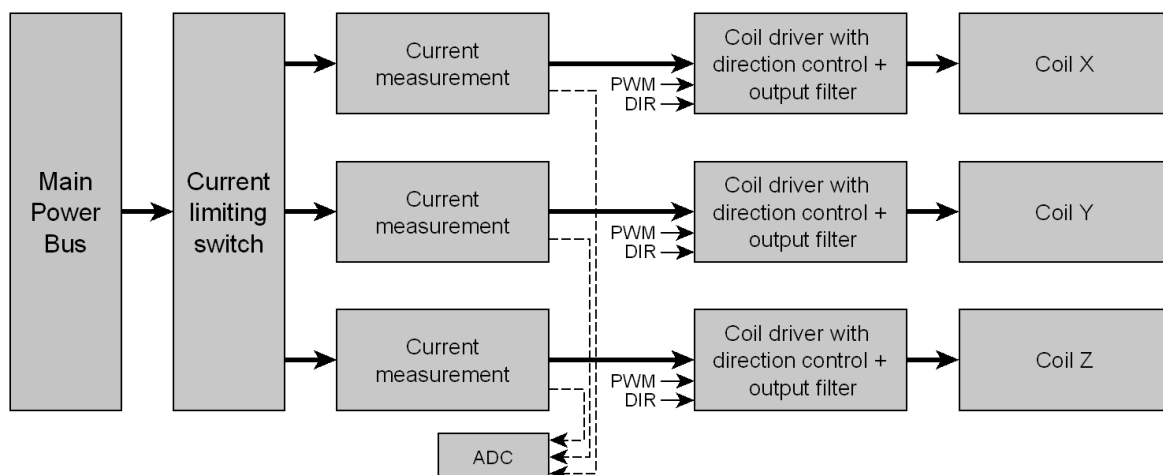


Figure 14. Magnetic torquer driver topology.

5.3.7. Antenna release switch

The EPS was the first system to be powered on when the satellite reached the orbit, therefore the EPS was also responsible for releasing the antennas. The release mechanism is based on resistance wire melting a nylon thread that secures the antennas in place during the launch and deployment. This electrical implementation has to be very simple and robust to ensure success on every try. The final solution involved only one TPS2557 with the current limit set to 1 A. Release tests showed that the system works very well and antennas were released within seconds from the turn-on of the switch.

5.4. Microcontroller Unit (MCU)

The Microcontroller Unit is responsible for the following functionalities in the EPS:

- The PDU management
- Telemetry collection and logging
- Providing the Second and Third Power Bus
- Managing bacon operations

The PCB is composed of 4 layers and contains 225-odd components. The functionality implemented on each layer is described below:

1. Top side - SPB capacitor bank (A), switching regulator circuits (B), serial FRAM memories with logic level conversion (C), parallel FRAM memory (D), the EPS main processor (E), level conversion devices and IO extender (F) and the stack connector (G). See Figure 15 below for a photograph, Figure 37 for Gerber view and Figure 42 for layout.

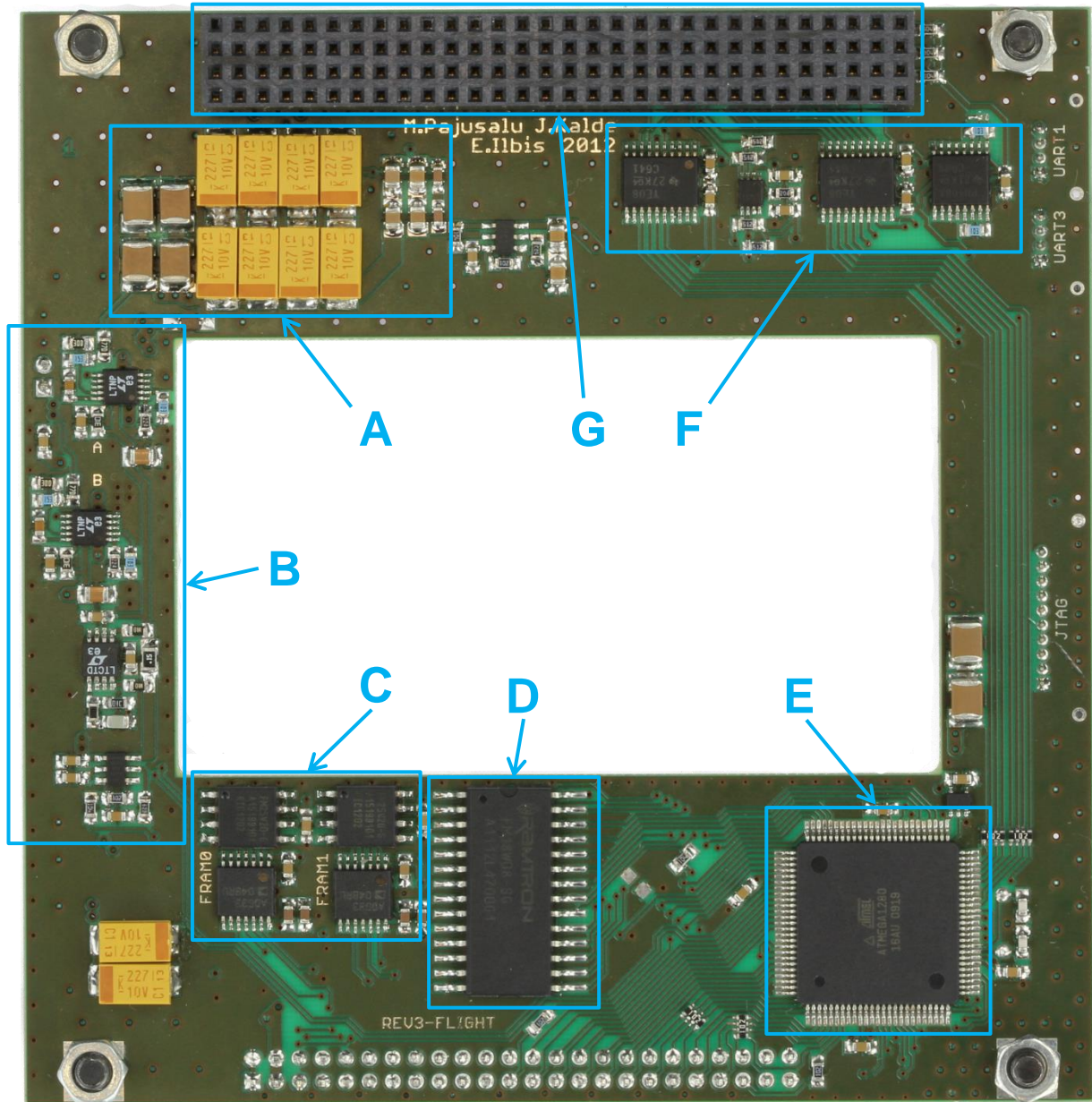


Figure 15. A photograph of the EPS MCU PCB top side.

2. Bottom side – programming and debugging connectors (A), crystal, external watchdog and voltage reference for the processor (B), the real time clock (C), TPB charge pump (D), switching regulator circuits and inductors (E) and payload release mechanism

switches (F). See Figure 16 below for a photograph, Figure 38 for Gerber view and Figure 43 for layout.

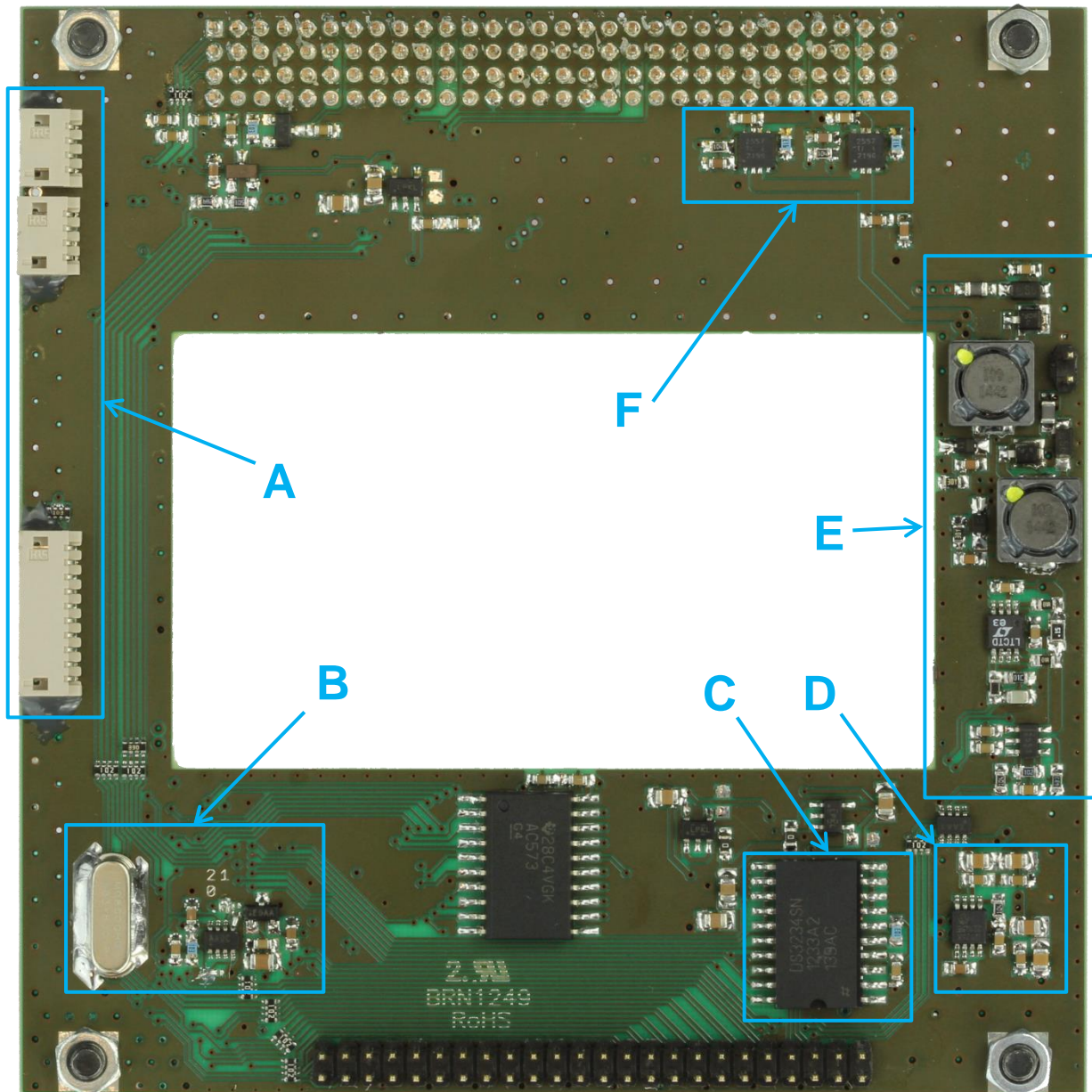


Figure 16. A photograph of the EPS MCU PCB bottom side.

3. Inner layer 1 – dedicated GND layer (see Figure 39 for Gerber view)
4. Inner layer 2 – GND and power traces (see Figure 40 for Gerber view)

Same ground improvement methods were used while designing the MCU board as were used on the PDU board. The measured resistance between the opposing corners is 12 m Ω . Due to there being conductive spacers in the corners and several ground connections in the two system connectors, the ground impedance is very low throughout the module.

5.4.1. EPS system bus

The EPS system bus connects the two EPS boards together and enables communication between them. The hardware interface is implemented with a 48-pin 2.0 mm board-to-board connector. Following signal groups run through the bus:

- Main Power Bus
- Second Power Bus
- AVR ADC lines
- State saver clock and data signals
- Serial Peripheral Interface (SPI) with chip selects for ADCs and DACs
- Coil drivers' enable, PWM and direction signals
- Enable signal for the antenna release switch

5.4.2. Second Power Bus (SPB)

The SPB is a dedicated power rail for the processor and its peripherals. This bus is connected to the MPB in two ways: through two parallel 5 V boost regulators and through a low-dropout diode for failsafe operation. The regulators are based on the LTC3440 buck-boost switching regulator controller and the implementation is identical to the regulators on the PDU board. The SPB regulator has to constantly provide around 200 mW of power at 5 V. Efficiency of the regulators can be compared to the other 5 V regulators on the PDU board given the identical implementation; the efficiency can be estimated to be around 88% during normal operation. Diode connection ensures that the MCU will be powered on, even if the regulators are turned off or malfunctioning. Because of the low operating voltage (around 3.3 V in worst case) the EPS functionality will be limited. ADC block (see Figure 19) will not be functional, but rest of the peripherals will be fully operational.

A capacitor bank, measuring around 500 μF and consisting of solid tantalum and ceramic capacitors was implemented on the SPB. The main purpose of this bank is to keep the processor with its peripherals functioning for a period of time after the MPB loses voltage. This enables the processor to gather data about the power outage and execute necessary procedures before the whole system shuts down. To demonstrate this functionality and determine the time available for the processor to take action, the following test was conducted. The MPB (Ch1), SPB (Ch3), TPB (Ch2) and a processor IO pin (Ch4) were monitored with an oscilloscope. The MPB was shorted out and the time between that event

and the processor stopping was measured. The Figure 17 below demonstrates the behaviour of the system and it can be concluded that the processor is capable of operating up to 80 ms after the loss of MPB.

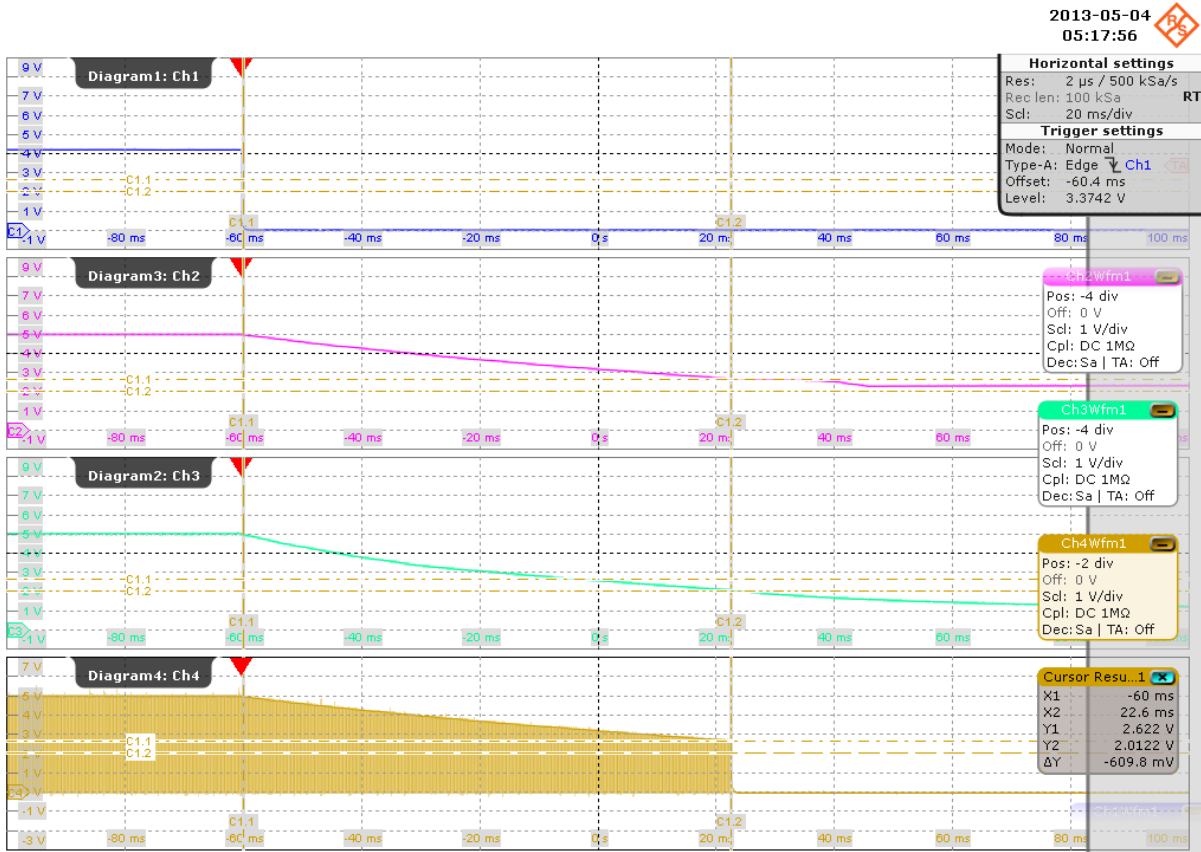


Figure 17. Processor function after MPB short.

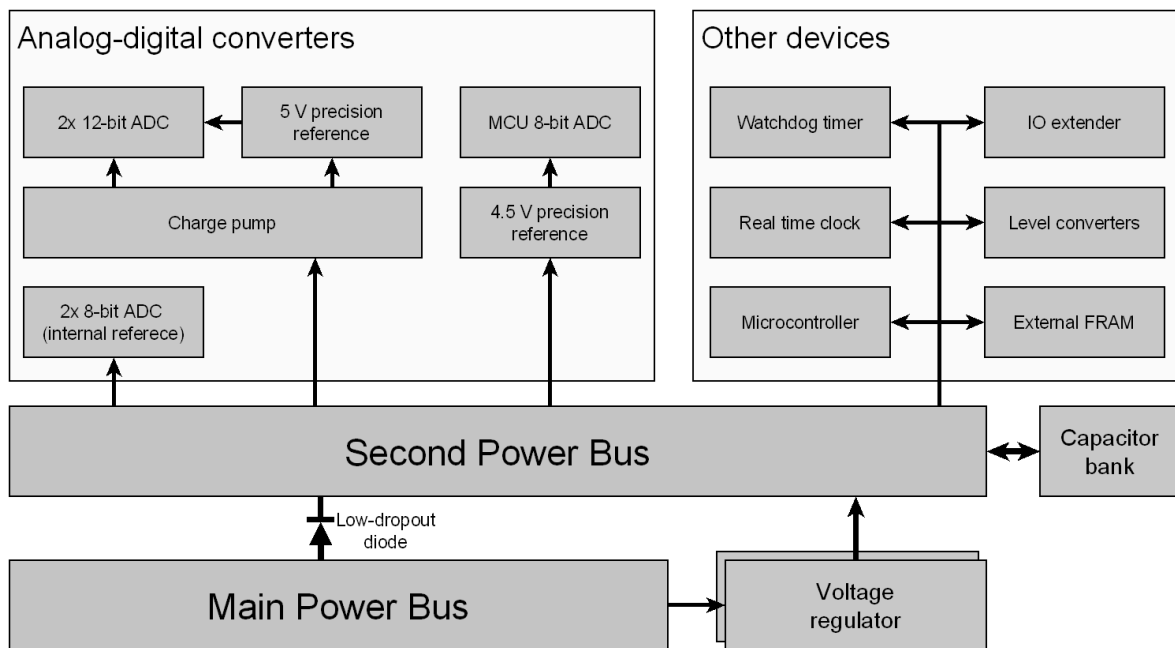


Figure 18. Second power bus topology.

5.4.3. Third Power Bus (TPB)

The Third Power Bus is a dedicated supply rail for state savers and digital-to-analogue converters (these DACs are only used during the experiment and powered down otherwise). This bus is very critical because losing it means losing control over all the regulators, battery switches and subsystem protection circuits. Requirements for the power bus are following:

- Bus voltage must be 5 V.
- Input must come from the MPB.
- <10mW of power is required.
- Dedicated power converter must be used.
- Has to be as reliably and simple as possible.

The input power has to come from the unregulated MPB which has lower maximum voltage than the required TPB voltage; therefore voltage has to be boosted. This problem is usually solved by using a step-up switching regulator, but this application needs so little power that a separate regulator would be unreasonable. The other alternative to boost voltage is with a charge pump. These devices are very simple: internal design usually consists of 4 MOSFETs and some control logic and the only external components needed are 3 capacitors [48]. This device meets all the requirements and takes up very little space, compared to switching regulators.

5.4.4. Microcontroller, ferroelectric RAM (FRAM) and peripherals

The Electrical Power System has its own dedicated microcontroller to manage the power distribution system, collect telemetry data, send beacon, and perform other tasks. Because the EPS is the first subsystem that will be powered on at any time, it has to be able to read the remove before flight pins and determine whether the satellite is in ground servicing mode or deployed in space. After being powered up for the first time in space, the first task for the EPS is to release the antennas and start transmitting the Safe Mode beacon which contains critical parameters about the EPS.

To perform these tasks, an 8-bit ATmega1280 microcontroller from Atmel was chosen. This controller has a wide range of features, very many GPIO pins, low power consumption, and has been tested in ionizing radiation [49]. The features include hardware support for various serial and parallel communication protocols:

- Joint Test Action Group (JTAG) interface – is used to program and debug the microcontroller. JTAG interface in combination with the AVR Dragon tool enables advanced on-the-fly debugging to ease the software development process.
- Serial Peripheral Interface (SPI) – a high speed serial interface, used to communicate with external ADCs (MAX1230 and MAX1119 from Maxim Integrated), DACs (LTC2630 from Linear Technology), FRAM memories (FM25V20 from Ramtron), and the real time clock (MAX3234 from Maxim Integrated).
- Universal Synchronous Asynchronous Receiver/Transmitter (USART) – used to communicate with other subsystems. The EPS has direct connections to CDHS and COM subsystems.
- Two Wire Interface (TWI) – a serial communication line, used to communicate with the beacon frequency generator chip (Si571 from Silicon Labs) and the IO expander⁵ (TCA6408PWR from Texas Instruments).
- Parallel external memory interface – used to connect the parallel FRAM memory module (FM18W08 from Ramtron) to the AVR microcontroller and extend the RAM memory.

Ferroelectric memories have many qualities that make them very appealing for space applications. They are byte-accessible, non-volatile, have virtually unlimited read/write cycles ($>10^{10}$), consume very little power, are faster when compared to EEPROM or Flash memories, and have high radiation tolerance [50] [51]. Given that very high speed (SRAM memories) or high capacity (Flash memories) is not required, the FRAM is perfect for our application. Two different types of FRAMs were used: 256 Kbit parallel memory for extending the microcontroller's internal RAM memory used for storing constants and other non-volatile data, and 2 Mbit serial memories for storing firmware images and log data.

An external watchdog timer (MAX6369 from Maxim Integrated) was chosen over the AVR internal one to ensure reliable stand-alone watchdog functionality and to reduce the software complexity – configuration of the device is done in hardware with pull-up/down resistors and only one GPIO pin from the processor is required to reset the watchdog.

To communicate with the other subsystems, UART interface is used. Because of different logic-levels (EPS operates on 5 V logic, but CDHS and COM have 3.3 V logic), logic-level

⁵ This devices has a number of GPIO pins which are controllable over TWI bus

converters are used. TXB0108 8-bit bi-directional logic-level converters from Texas Instruments were chosen. They operate on very low current and are very simple to integrate into the system. These chips have been tested in radiation and have proven to be tolerant [49].

The beacon of the satellite is designed to be under direct EPS control. This implementation enables the satellite to operate in EPS-only mode; for example, the first 48 hours after deployment only the EPS was powered on and transmitted vital information about the state of the satellite. This gave critical input to planning the first actions when the communications system was powered on and also improved the odds of receiving a signal from the satellite. EPS configures the beacon frequency (frequency is generated by Si570 from Silicon Labs) over a TWI interface through a specialized TWI logic-level conversion chip (PCA9306 from Texas Instruments).

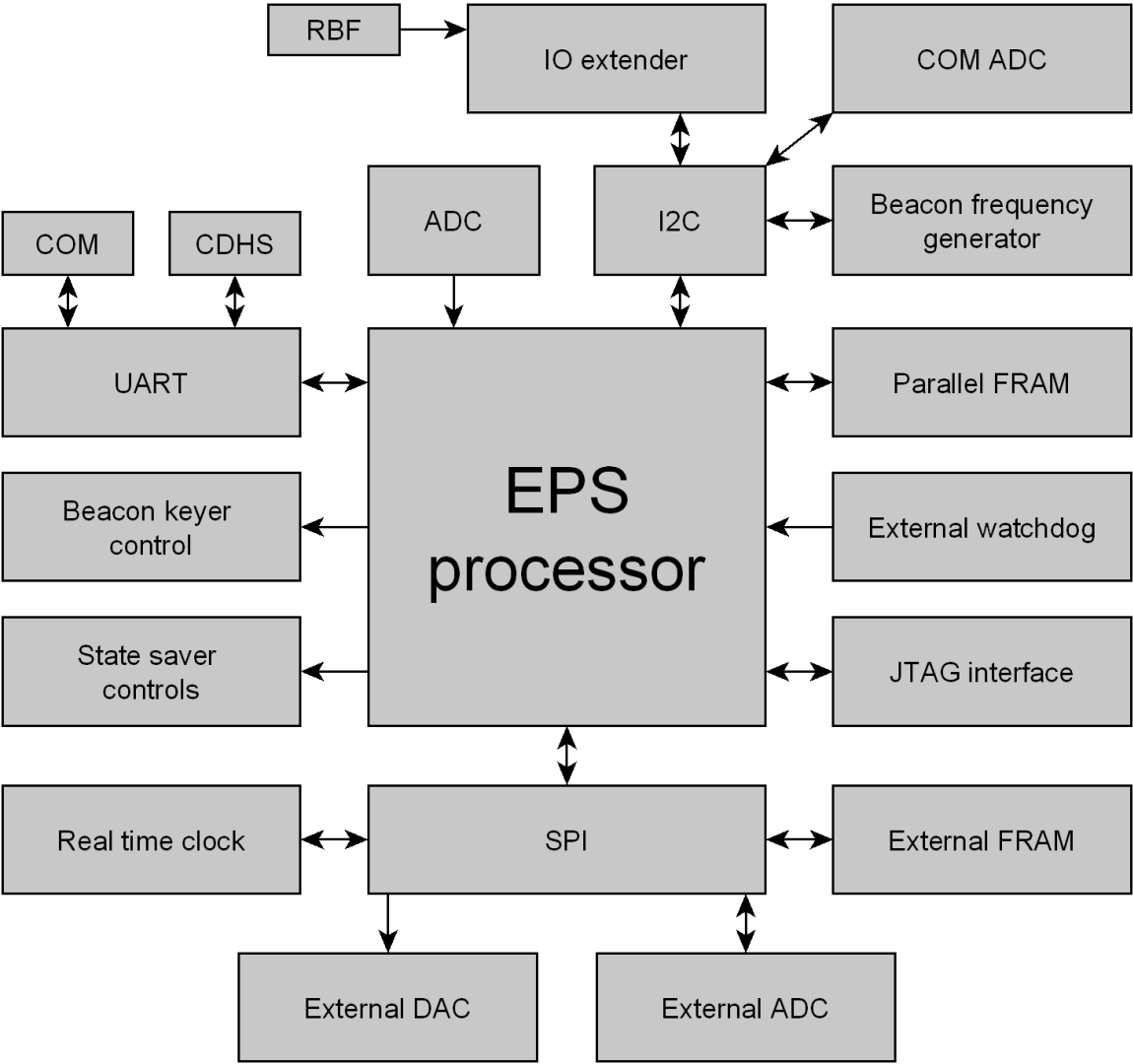


Figure 19. EPS processor topology.

5.4.5. Payload lock release switch

The Payload has two locks in place to prevent the system from moving during the pre-launch and launch period. One of the locks is meant for the reel (reel lock), and the other one to hold the end mass (launch lock) in place. They are very similar to the antenna locking system – both have nylon wires that have to be melted in order to release the locking mechanism. Implementation of this system is identical to the antenna release system – one TPS2557 for each lock with a 1 A current limit. These were implemented on the EPS board, because of the direct access to the MPB.

6.Environmental testing

To qualify the satellite for the launch, various endurance tests had to be conducted to ensure that the satellite withstands the lift off loads and is capable of working in the space environment. These tests included different vibration profiles, shock tests, thermal cycles, and thermal vacuum tests. The tests were performed on the whole satellite assembly.

During the sine sweep vibration testing, satellite had to endure loads up to 22.5 g at 30 – 200 Hz and 10 g at 200 – 2000 Hz in every axis. Random vibration tests were also conducted in all axes with loads up to 18 g at 20-2000 Hz. The sine vibration tests lasted for 15 minutes and the random vibration tests for 4 minutes each. Finally, shocks were conducted: shocks up to 1410 g had to be endured. [52] All these tests were successful and EPS did not suffer any observable damage.

The thermal tests cycled the satellite from -10 to 60 °C and kept it at those levels for two hours. Vacuum tests were conducted in similar order and the satellite was heated up to 70 °C and kept at it for two hours, after that the satellite was cooled for two hours and was heated up again. [52] Two cycles were conducted during both tests. During these tests the EPS was working and collected telemetry data. No failures were observed and test was concluded to be successful.

7. Summary

During the course of this work an Electrical Power System (EPS) was designed, assembled and tested for the ESTCube-1 satellite. The system design was based on functional requirements, individual power needs of the other subsystems, and constraints set by the overall system design and operational environment. The final design meets or exceeds all set requirements.

Most important results of this thesis are:

- A triple-redundant energy harvesting system based on an innovative hardware MPPT solution (measured efficiency up to 90%) was developed and integrated into the system.
- Both batteries have independent protection circuitry, making the energy storage system double-redundant.
- The battery protection circuit voltage drop measured only 20 mV, making the system losses minimal.
- A double-redundant centralized power regulation system with average efficiency of 85% was implemented.
- Each subsystem is independently protected from latch-up events by a hardware protection circuitry.
- The system endured all of the qualification tests, the launch and is currently operational in space.

This system was developed as a stand-alone module and therefore variations of this system or its elements can be used in future projects. Outside interest about the solutions used has been expressed by the Finnish Aalto-1 satellite team and NASA's PhoneSat team.

8. Kokkuvõte

Eesti Tudengisatelliidi projekt algas 2008. aastal Tartu Ülikoolis. Tänapäevaks on programmi käigus arendatud välja Eesti esimene satelliit ESTCube-1, mis viidi edukalt maalähedasele orbiidile mais 2013. aastal. Tegemist on kuupsatelliidi standardile vastava [5] 1-ühikulise nanosatelliidiga. Satelliidi teaduslikuks missiooniks on testida ambitsioonikat elektrilise päikesepurje tehnoloogiat (*E-sail*). Eksperimendi käigus keritakse satelliidist tsentrifugaaljõu abil välja 10 m pikkune mikrojuhe ning laetakse see kõrge potentsiaalini. Maa ionosfääriline plasma peaks teooriakohaselt avaldama tekkinud elektriväljale vastasmõju ning seeläbi satelliidi pöörlemiskiirust aeglustama. Elektrilise päikesepurje tehnoloogia abil võivad saada reaalsuseks kiired ning kulutõhusad reisirid Päikesesüsteemis ning sellest väljaspool. [7]

Käesoleva bakalaureusetöö käigus arendati välja satelliidi tööks vajaliku toitemooduli riistvara. See moodul on satelliidi ainukeseks toiteallikaks orbiidil opereerimise ajal, seega peab olema tegemist töökindla lahendusega. Toitesüsteemi kavandamisel lähtuti toitesüsteemile seatud funktsionaalsetest nõuetest, erinevate alamsüsteemide vooluvajadustest ning töökeskkonna eripäradest (radiatsioon, vaakum, varieeruv temperatuur). Lisaks pidi moodul sobima ka satelliidi mehaanilise struktuuriga ning olema võimeline töötama autonoomselt, lähtudes ainult sensoritelt kogutud infost.

Paljud inimesed on aastate jooksul panustanud ESTCube-1 toitesüsteemi arendusse; autori ülesanne oli kogu eelneva töö baasil ehitada valmis täisfunktsionaalne toitesüsteem. Töö hulka kuulus ka ehitatud mooduli funktsionaalsuse testimine ning omaduste kirjeldamine.

Käesoleva töö raames arendatud süsteem kasutab mitmeid uuenduslikke lahendusi, mida ei ole varem kuupsatelliitide peal testitud: näiteks riistvaral põhinev maksimaalse võimsuspunkti jälgimissüsteem. Uuenduslikest lahendustest tulenevalt on süsteemi ülesehituse kohta peetud rahvusvahelisel astronautika kongressil ettekanne [2] ning avaldatud ka artikkel [1]. Lõplike testimistulemusi sisaldav artikkel on arvustuseks saadetud Acta Astronautica [3].

Töö peamisteks eesmärkideks olid:

- tuua välja nõuded ESTCube-1 toitesüsteemi jaoks;
- kavandada ning ehitada süsteemi riistvara ja
- testida mooduli funktsionaalsust ning kindlaks teha süsteemi omadused.

Kirjeldatud töö viidi läbi kahe aasta jooksul. Selle aja jooksul valmistati kolm versiooni riistvarast ning riistvara lennuversioon täitis või ületas kõiki esitatud nõudeid. Kõige olulisemad tulemused on loetletud allpool.

- Arendati välja ning integreeriti 90% mõõdetud efektiivsusega riistvaralisel võimsuspunkti jälgimisel põhinev energia kogumissüsteem. Süsteem sisaldab kolme identset ahelat, mis on üksteisest sõltumatud.
- Energia hoiustamissüsteem koosneb kahest eraldiseisvast akust koos kaitsesüsteemiga. Kaitsesüsteemi pingelang on 20 mV, mistõttu on efektiivsuskaod süsteemis minimaalsed.
- Pinge reguleerimissüsteemis on iga väljundpinge jaoks kasutusel kaks paralleelset, kuid eraldiseisvat regulaatorit. Regulaatorite keskmine efektiivsus on 85%.
- Igal alamsüsteemil on eraldiseisev kaitse iseenesliku lühistumise (*single event latch-up*) eest, mida võib tekitada radiatsioon.
- Süsteem pidas vastu kõik koormustestid, kanderaketi stardi ning on 2013. aasta mai seisuga kosmoses töökorras.

Süsteem töötati välja eraldiseisva moodulina, seega on võimalik süsteemi või selle osi kasutada tulevastes projektides. ESTCube-1 toitesüsteemi lahenduste vastu on huvi tundnud ka Soome Aalto-1 satelliidi ning NASA PhoneSati meeskonnad.

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Appendices

Appendix 1 – Schematic diagrams (typical implementations)

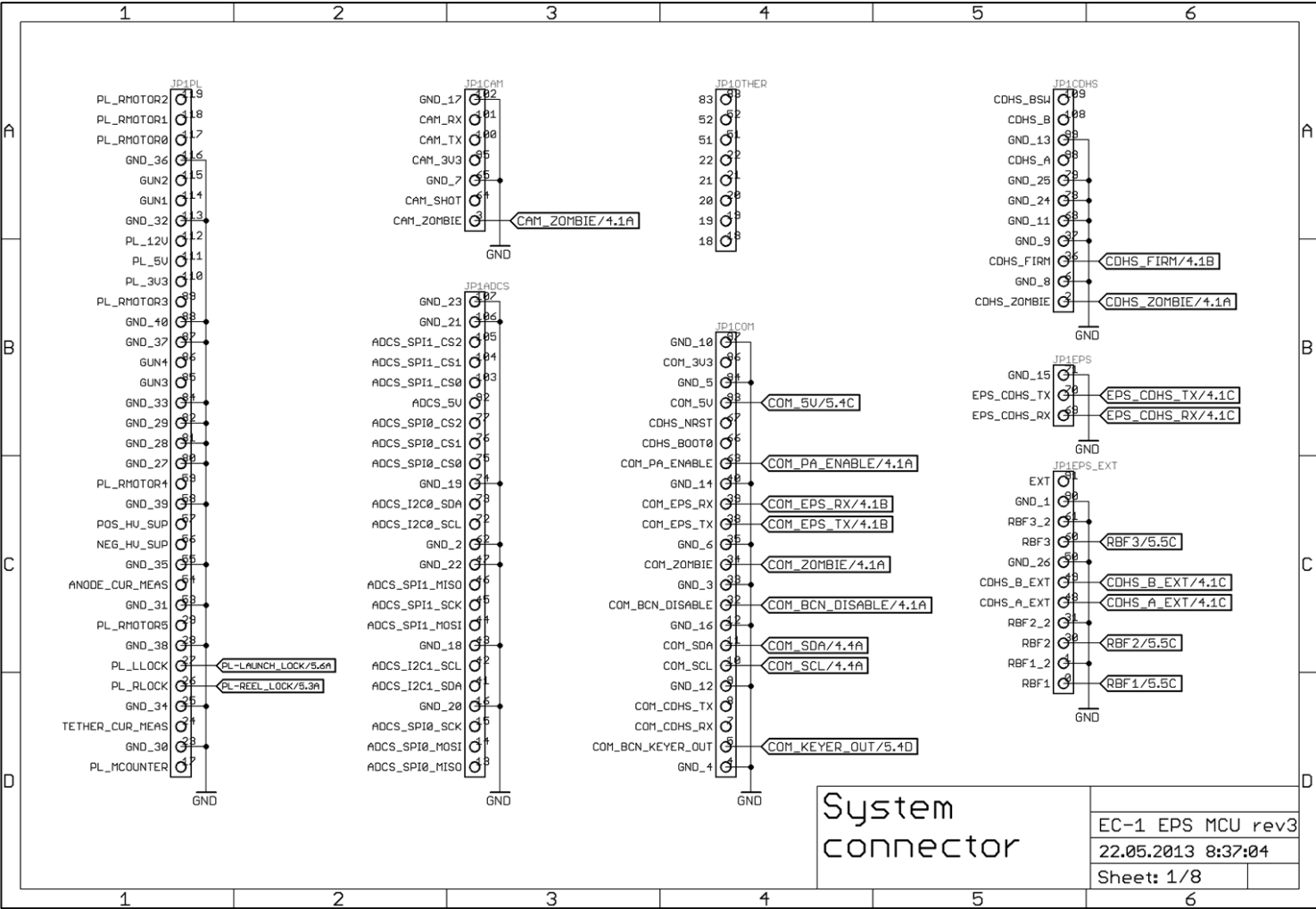


Figure 20. System bus connections on MCU.

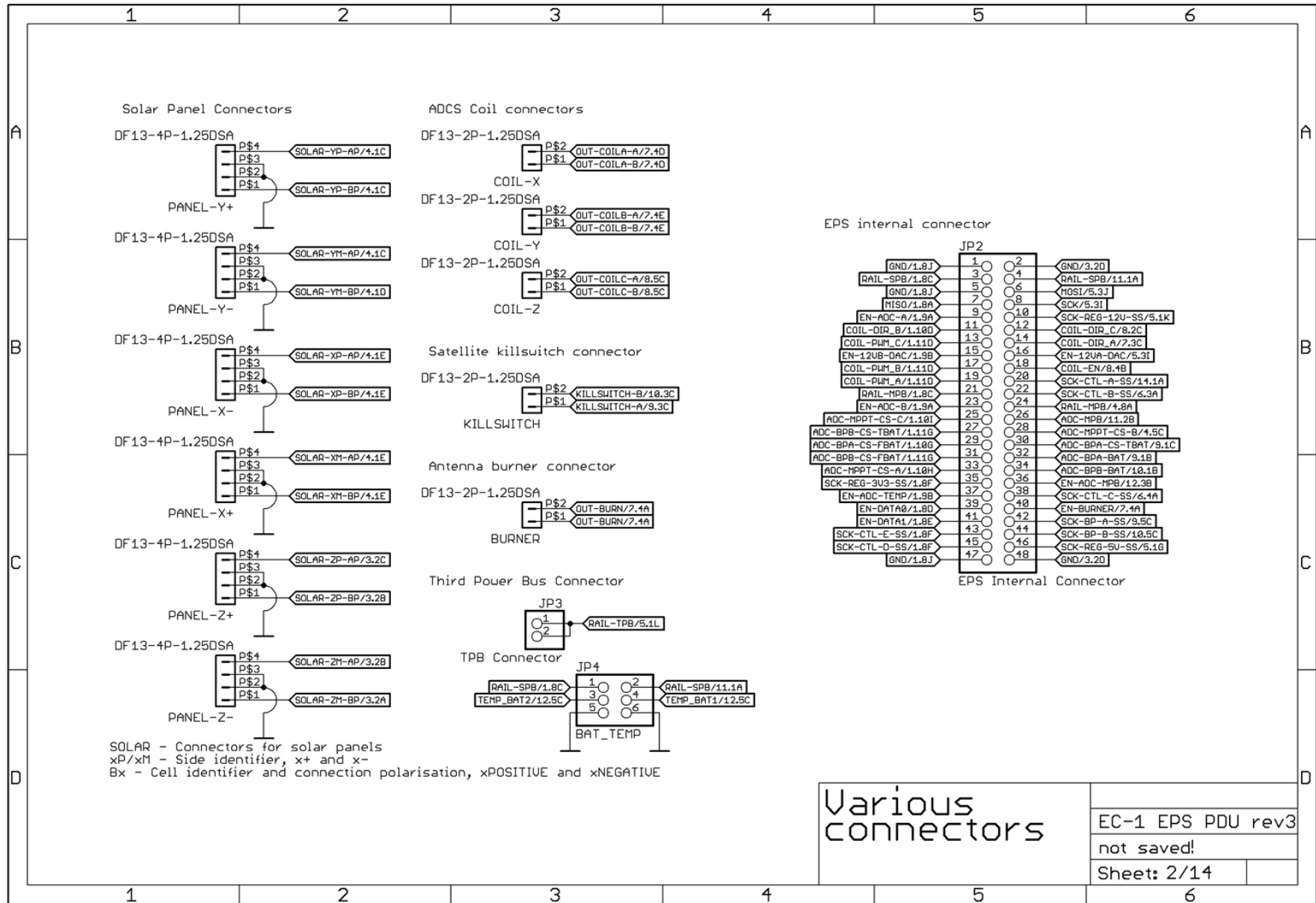


Figure 21. Various connectors on the PDU board (EPS system bus, solar panel connectors, magnetic actuators' connectors, TBP connector etc).

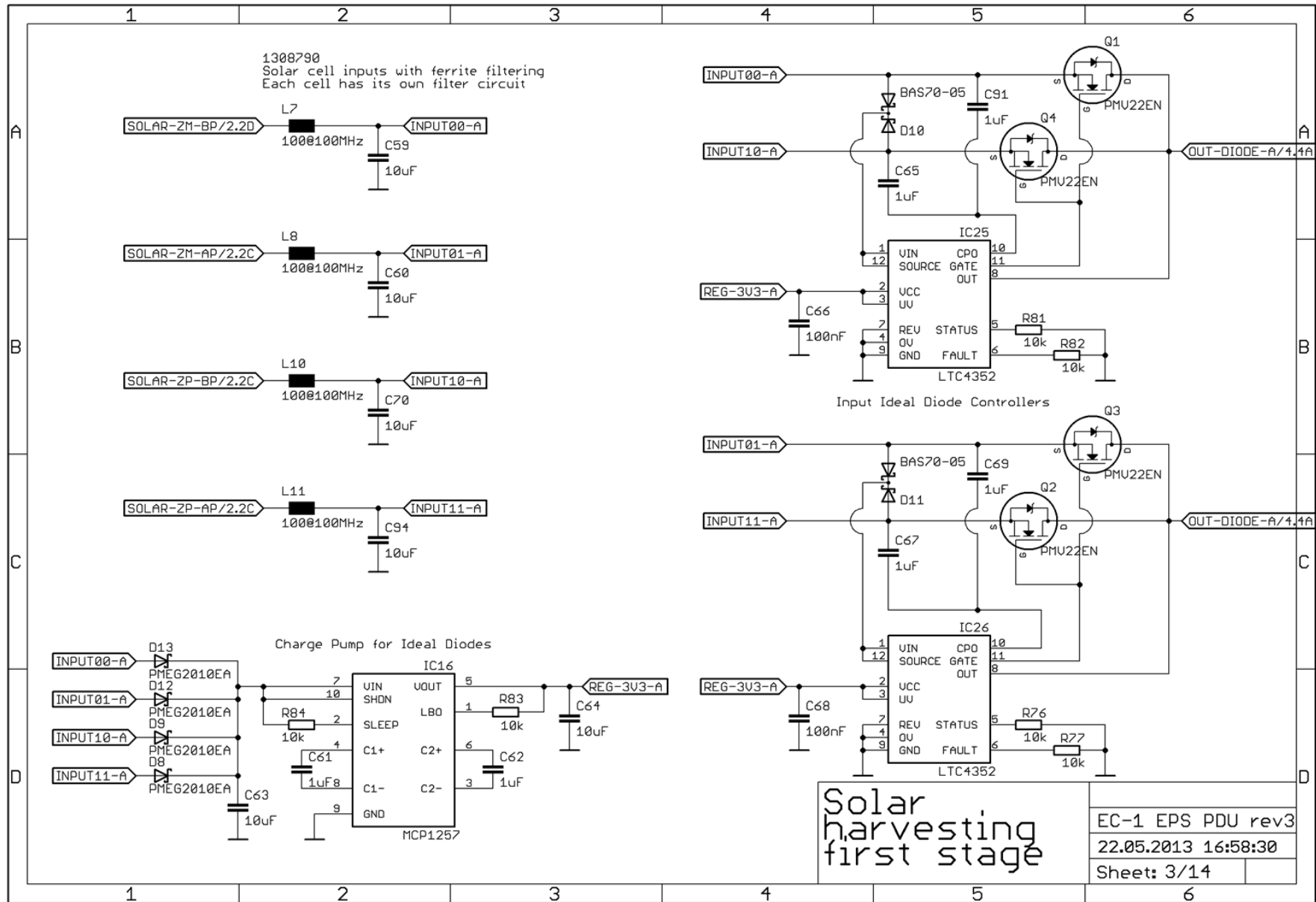


Figure 22. PDU energy harvesting: first stage (input filtering, charge pump, cell ideal diodes).

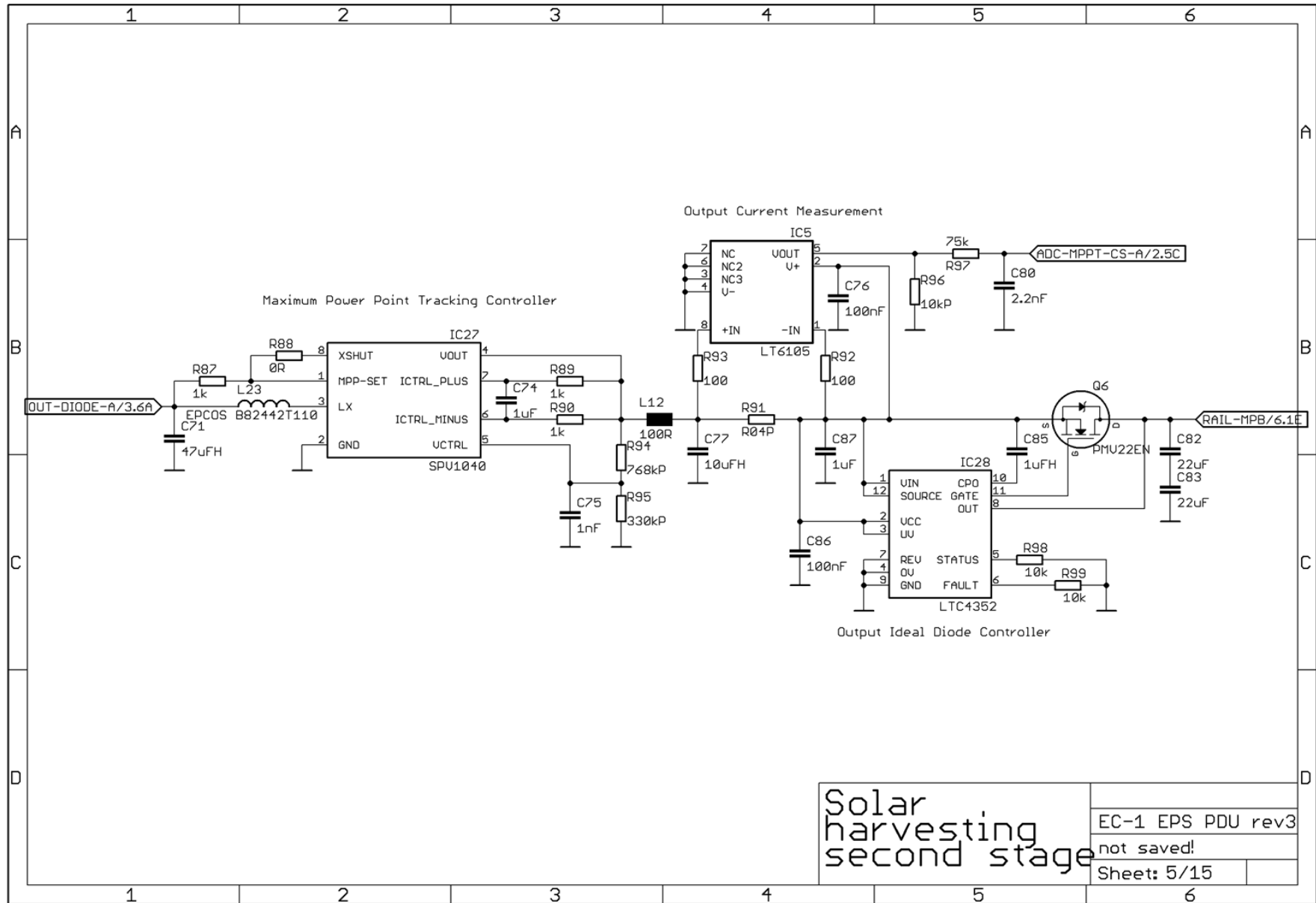


Figure 23. PDU energy harvesting: second stage (MPPT driver, current measurement and ideal diode).

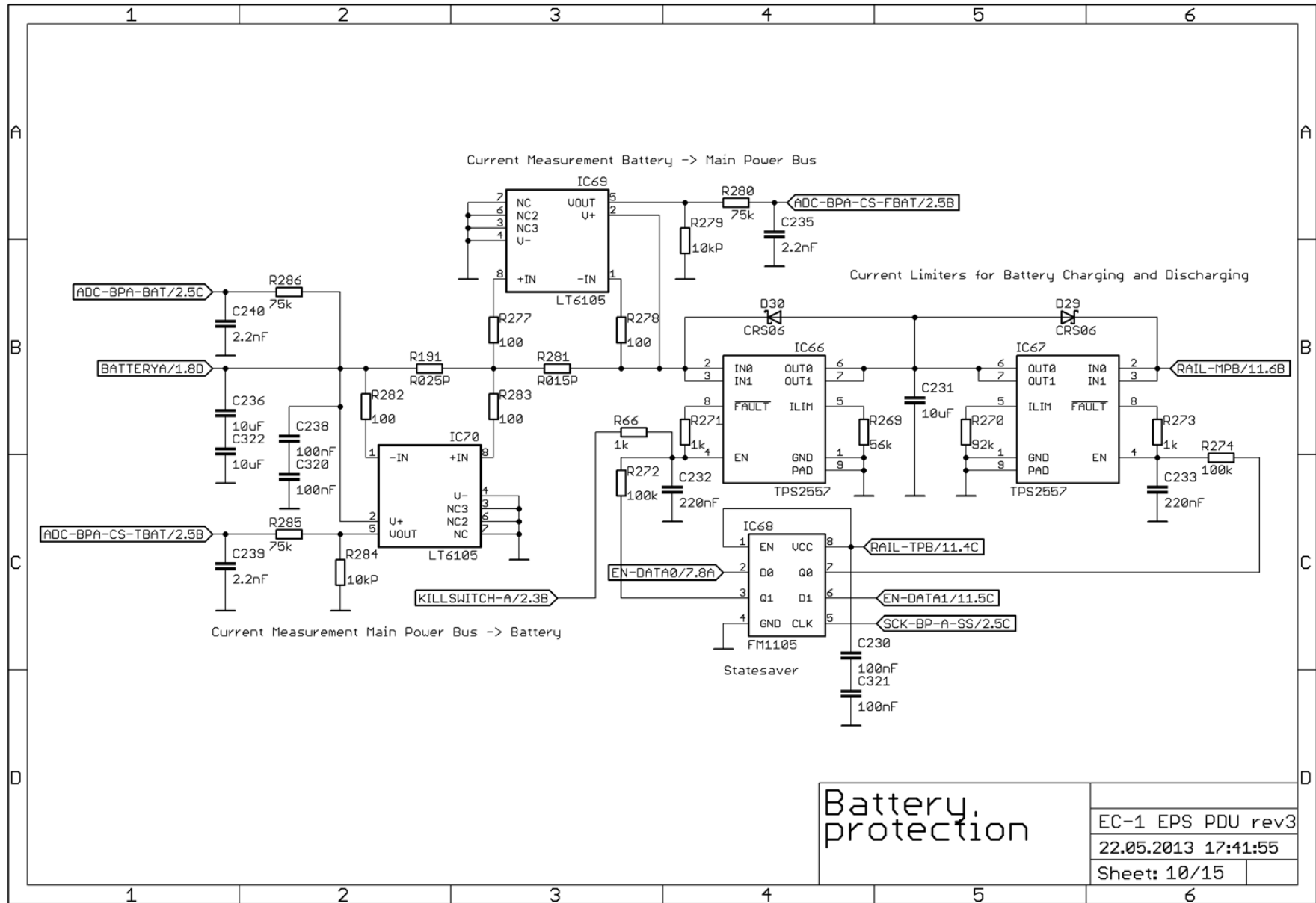


Figure 24. PDU battery protection circuit for a single battery.

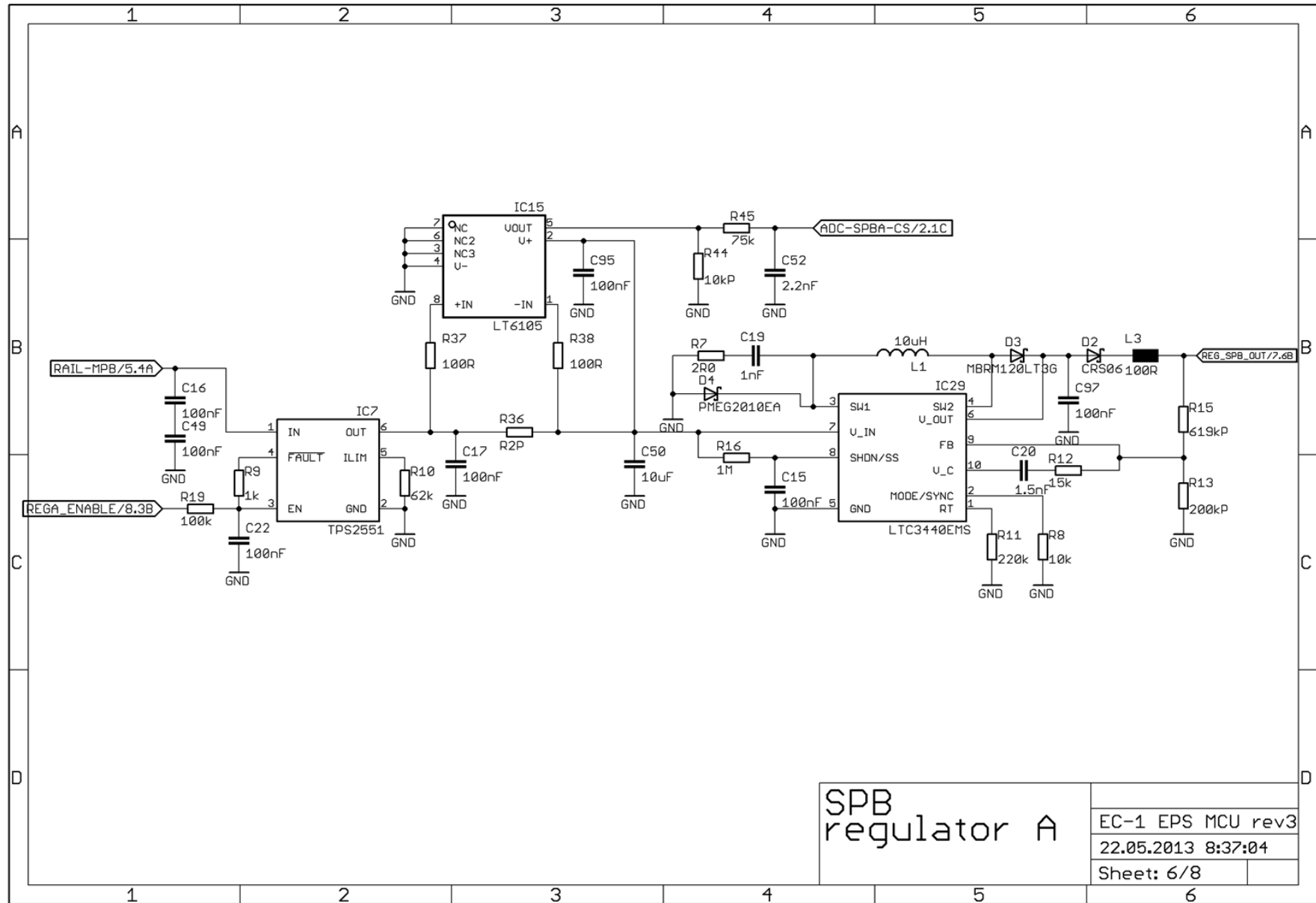


Figure 25. LTC3440-based regulator implementation example.

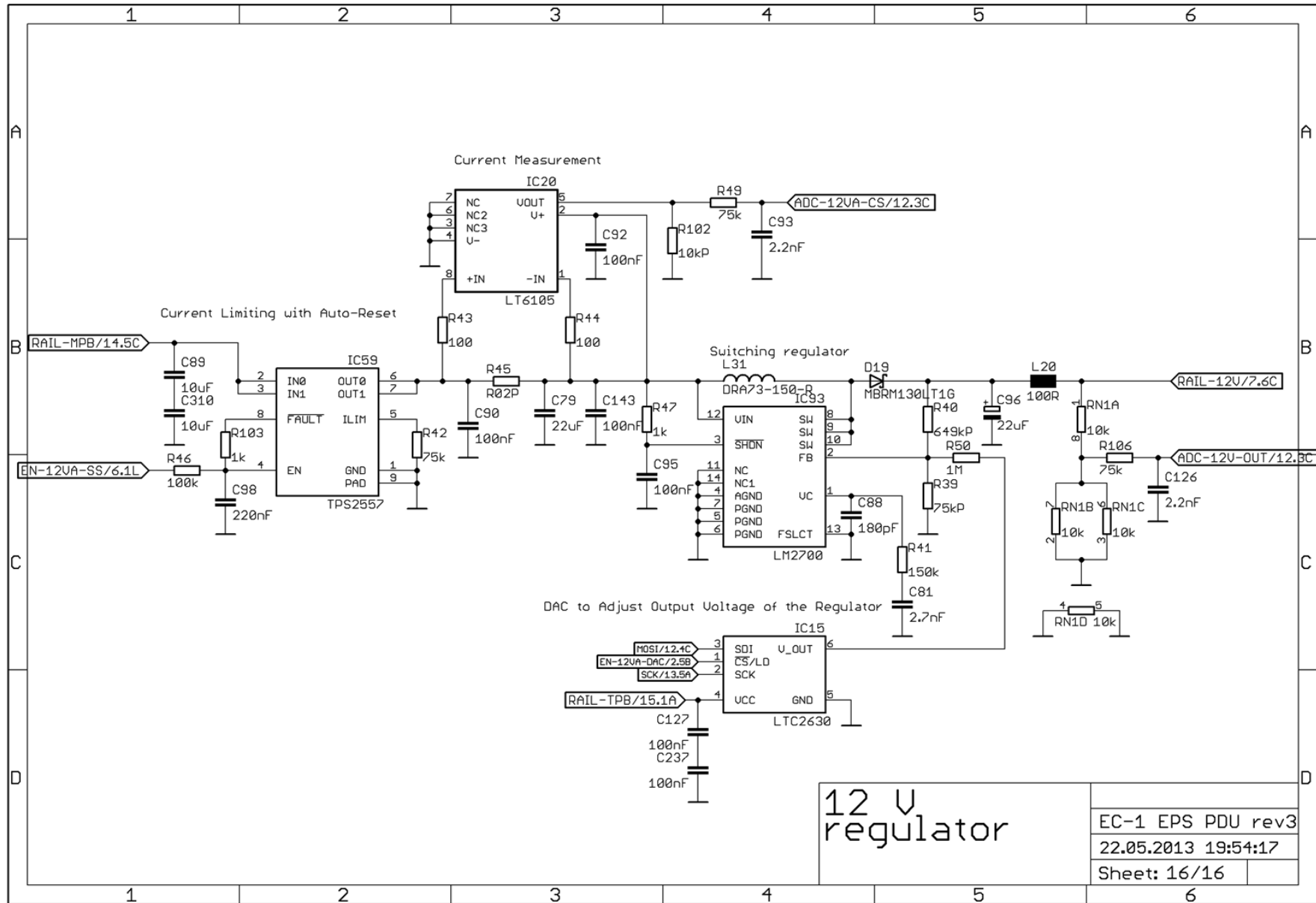


Figure 26. LM2700-based regulator implementation example.

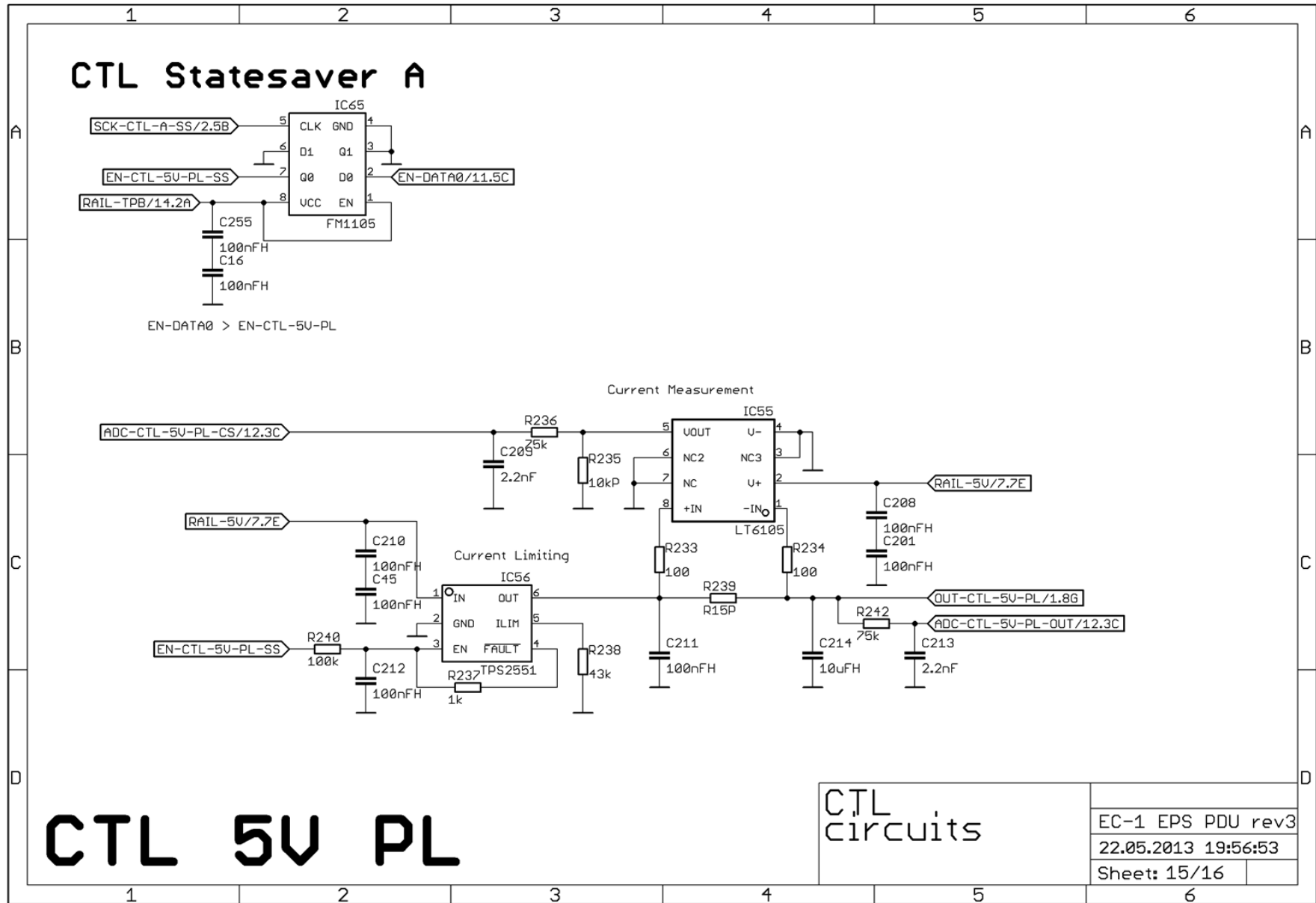


Figure 27. CTL circuit example.

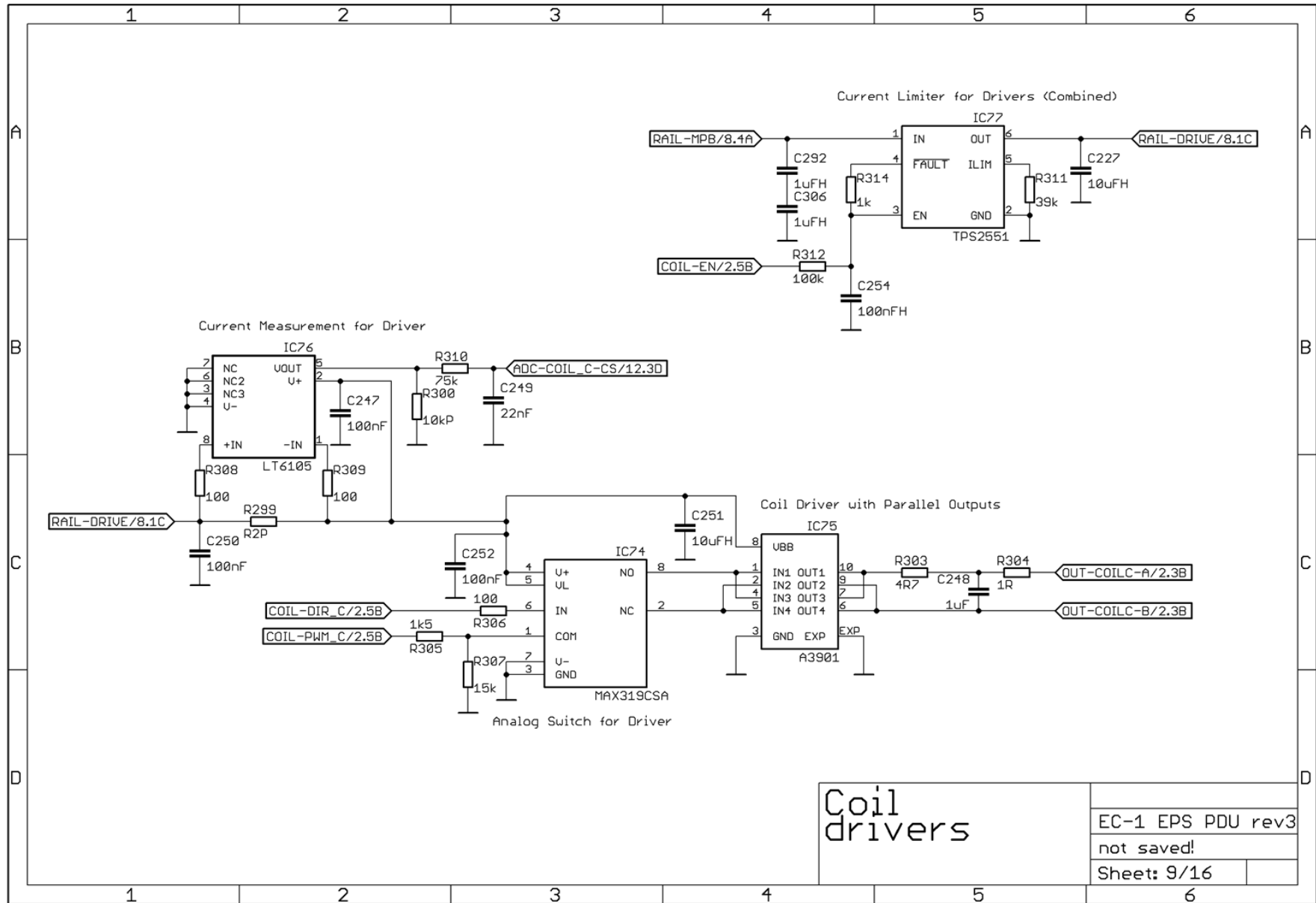


Figure 28. Magnetic actuators' driver example (the switch for all the drivers and one driver circuit).

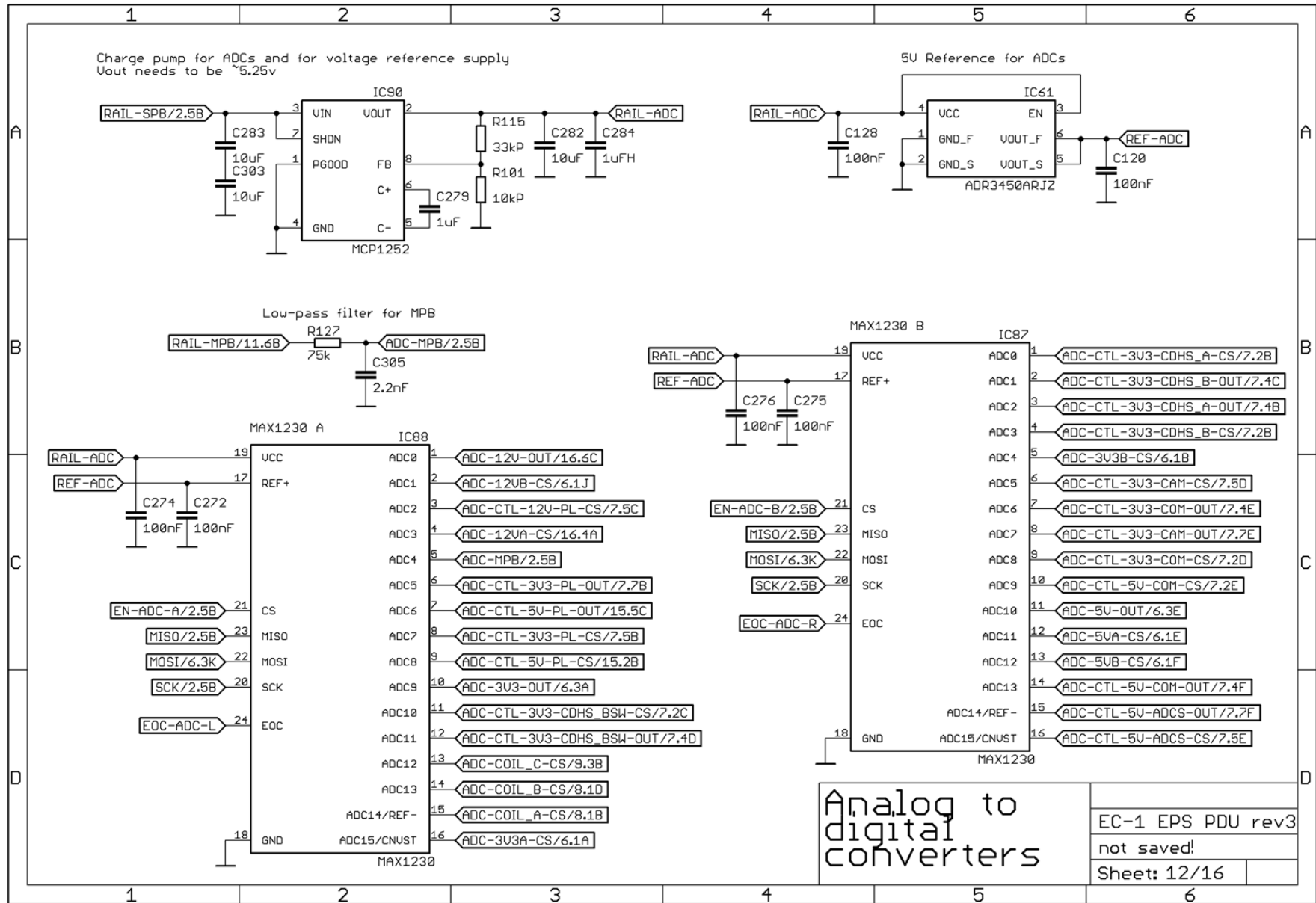


Figure 29. PDU MAX1230 ADC implementation.

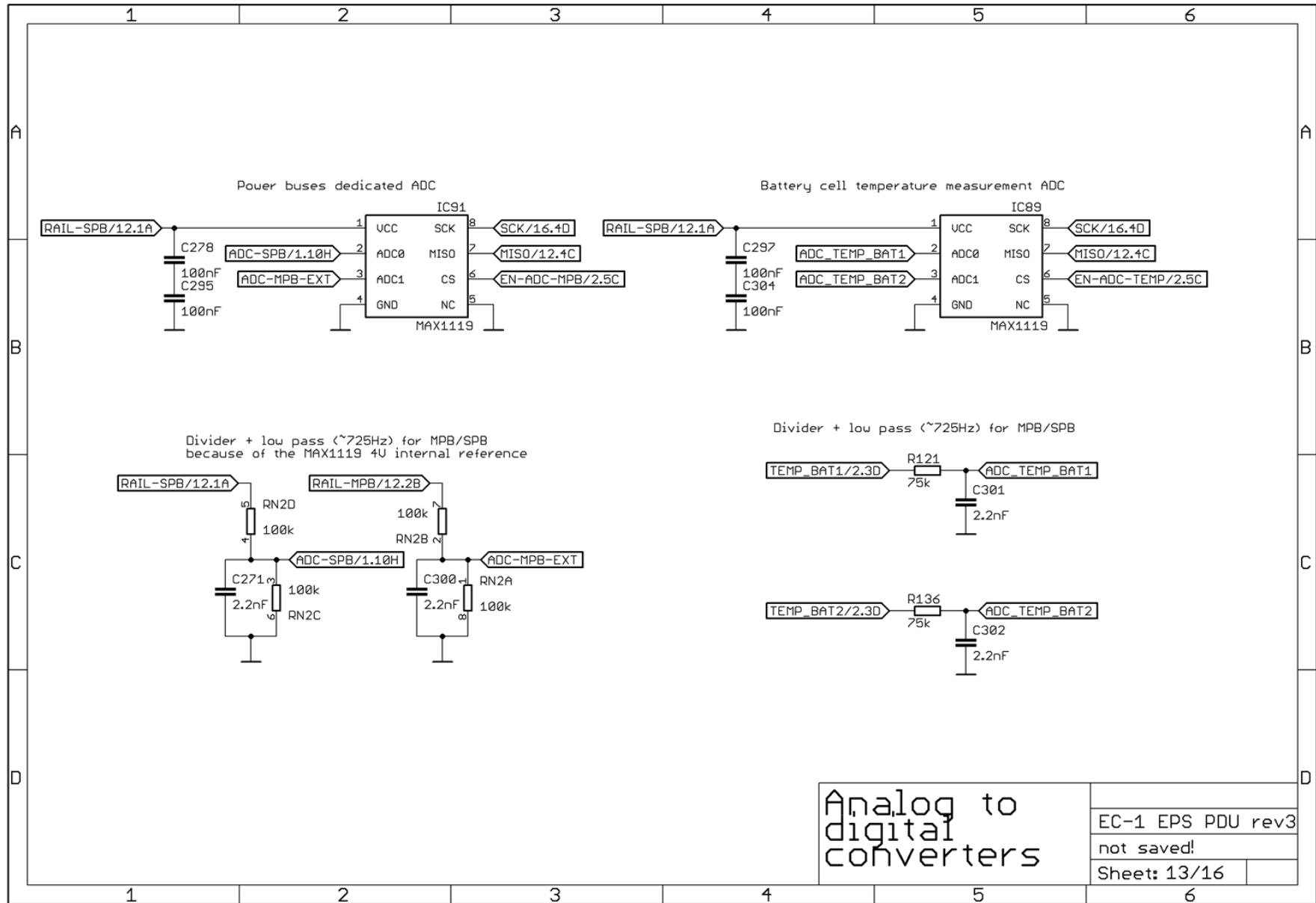


Figure 30. PDU MAX1119 ADC implementation.

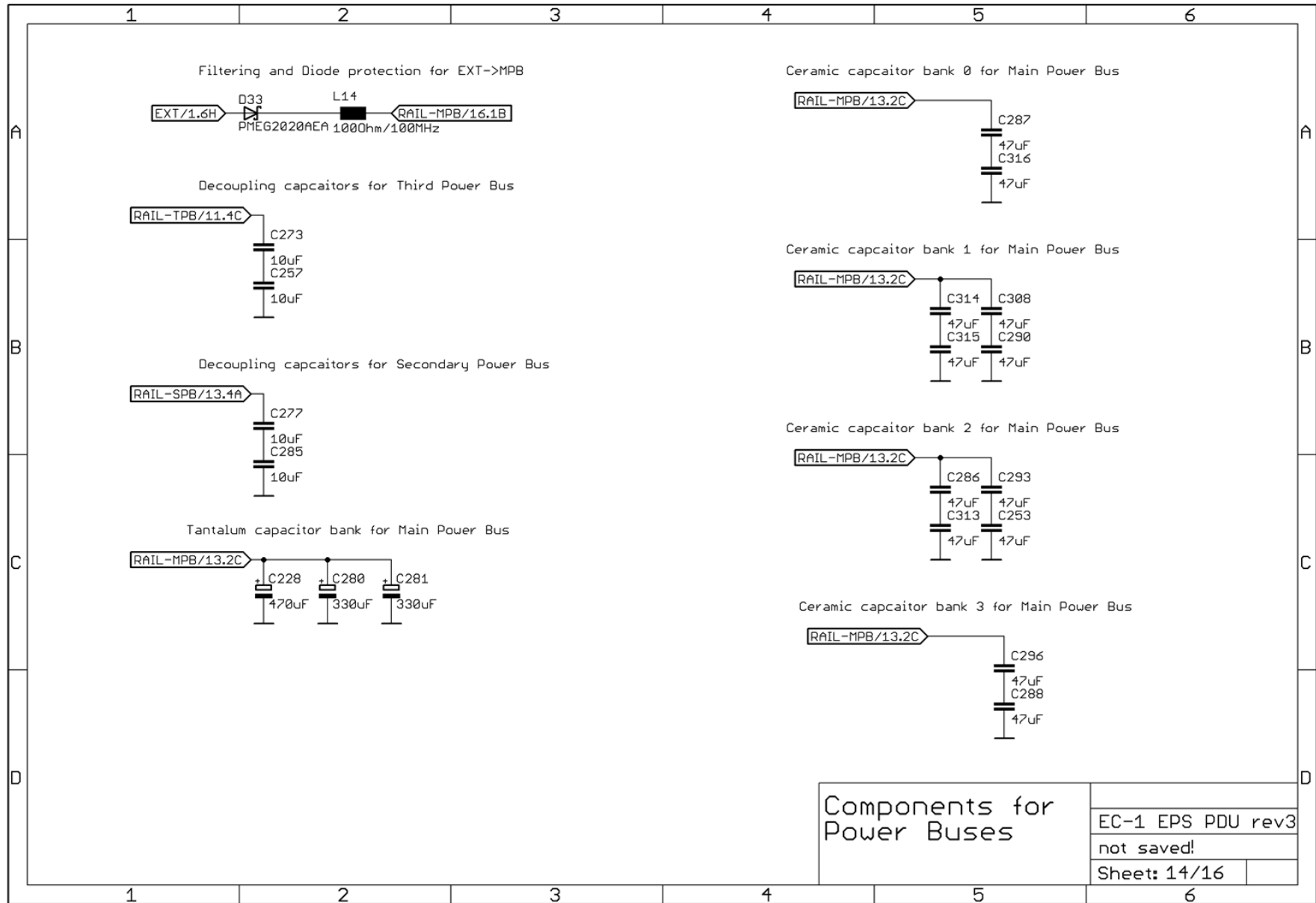


Figure 31. PDU MPB capacitance banks.

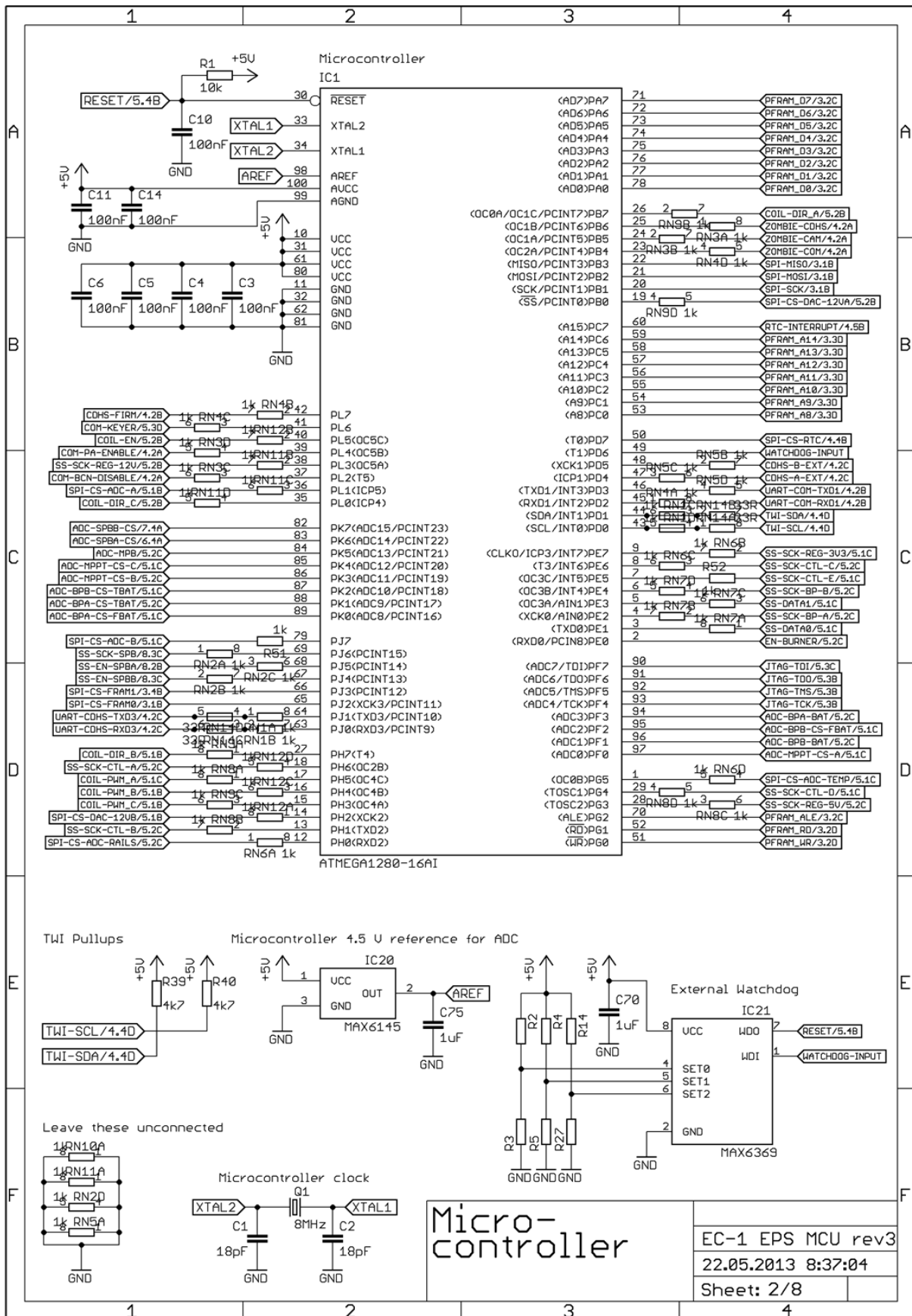


Figure 32. MCU microcontroller implementation with external watchdog and voltage reference.

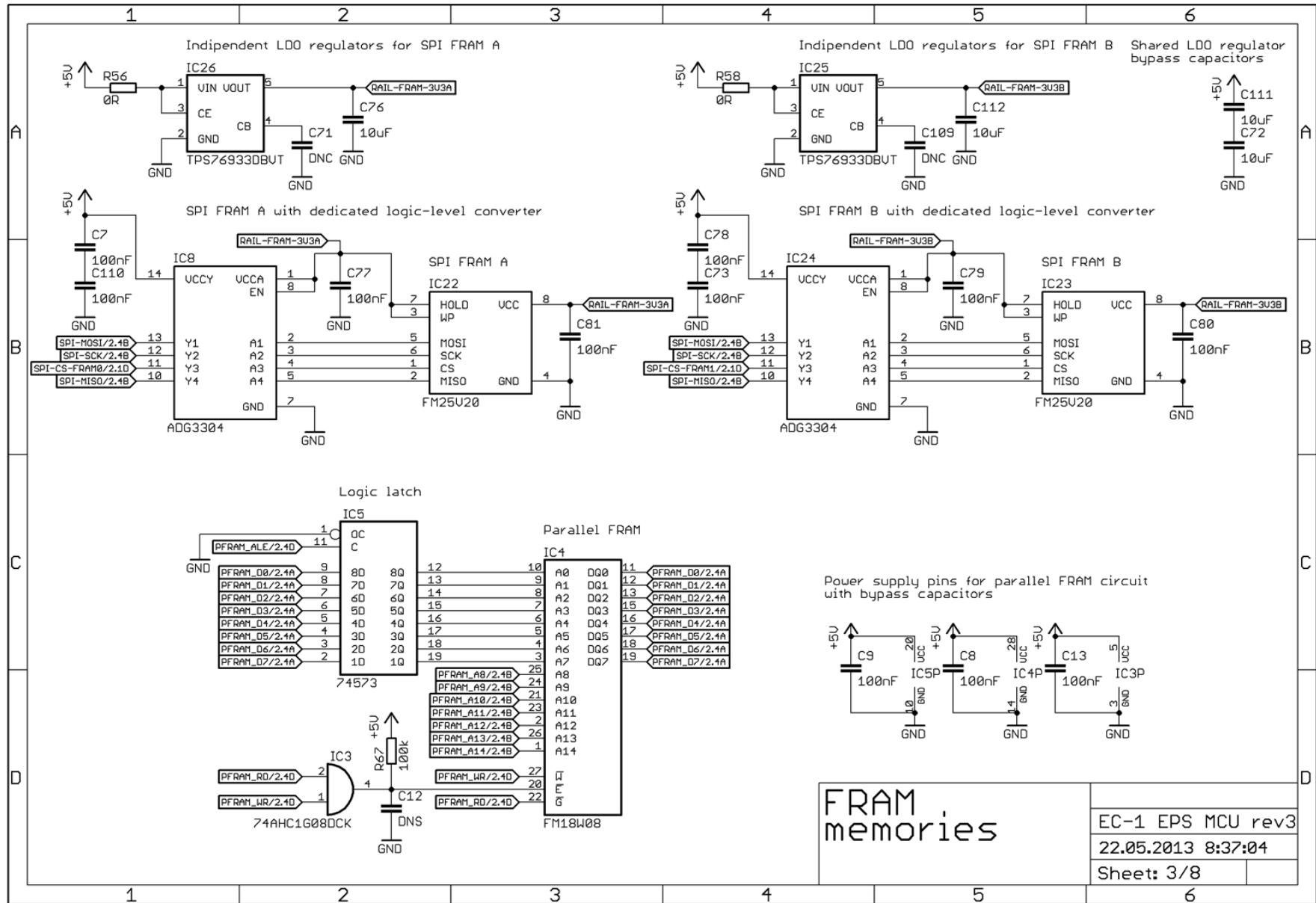


Figure 33. MCU FRAM memory implementations.

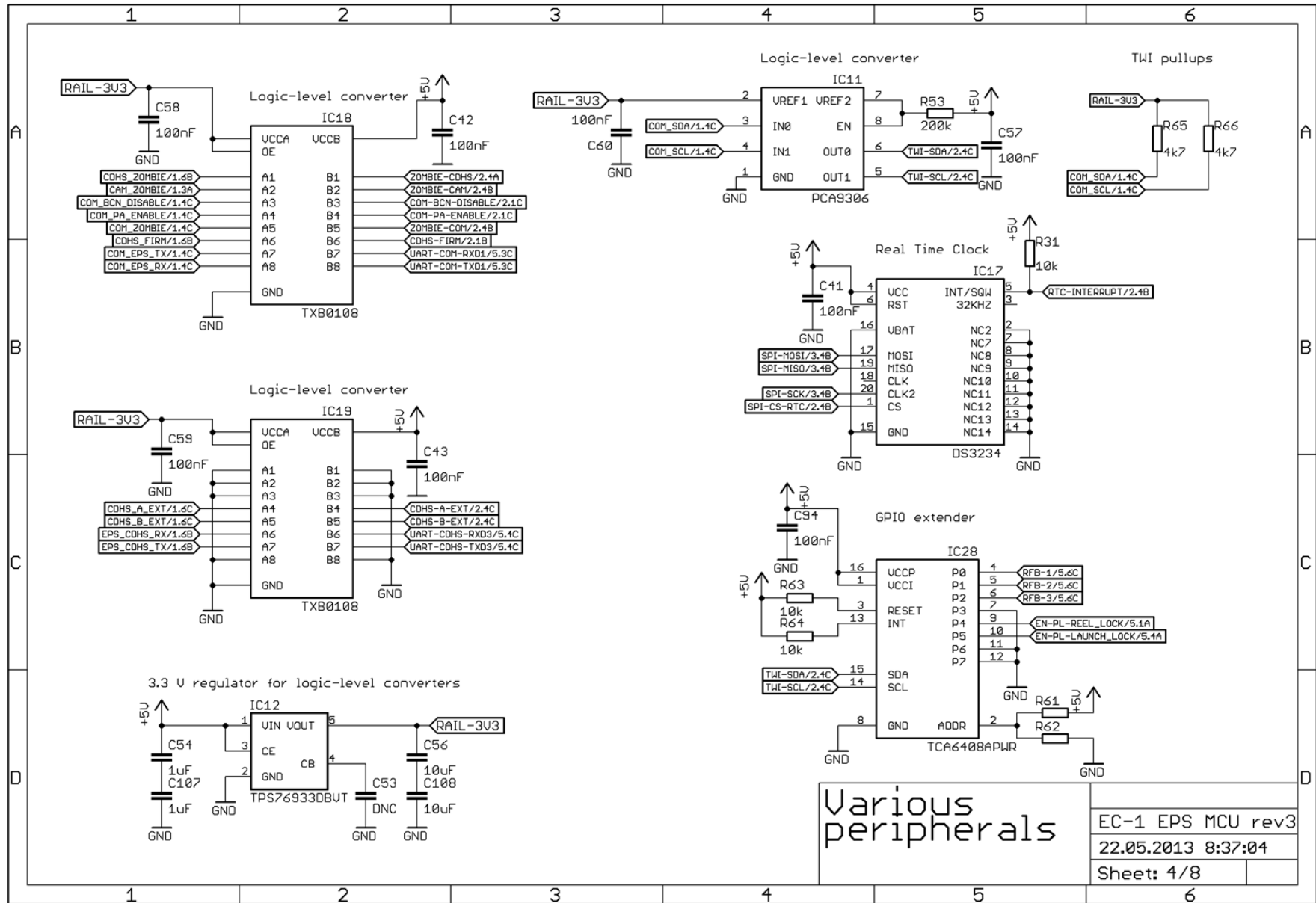


Figure 34. MCU various peripherals (logic-level conversion, real time clock and GPIO extender).

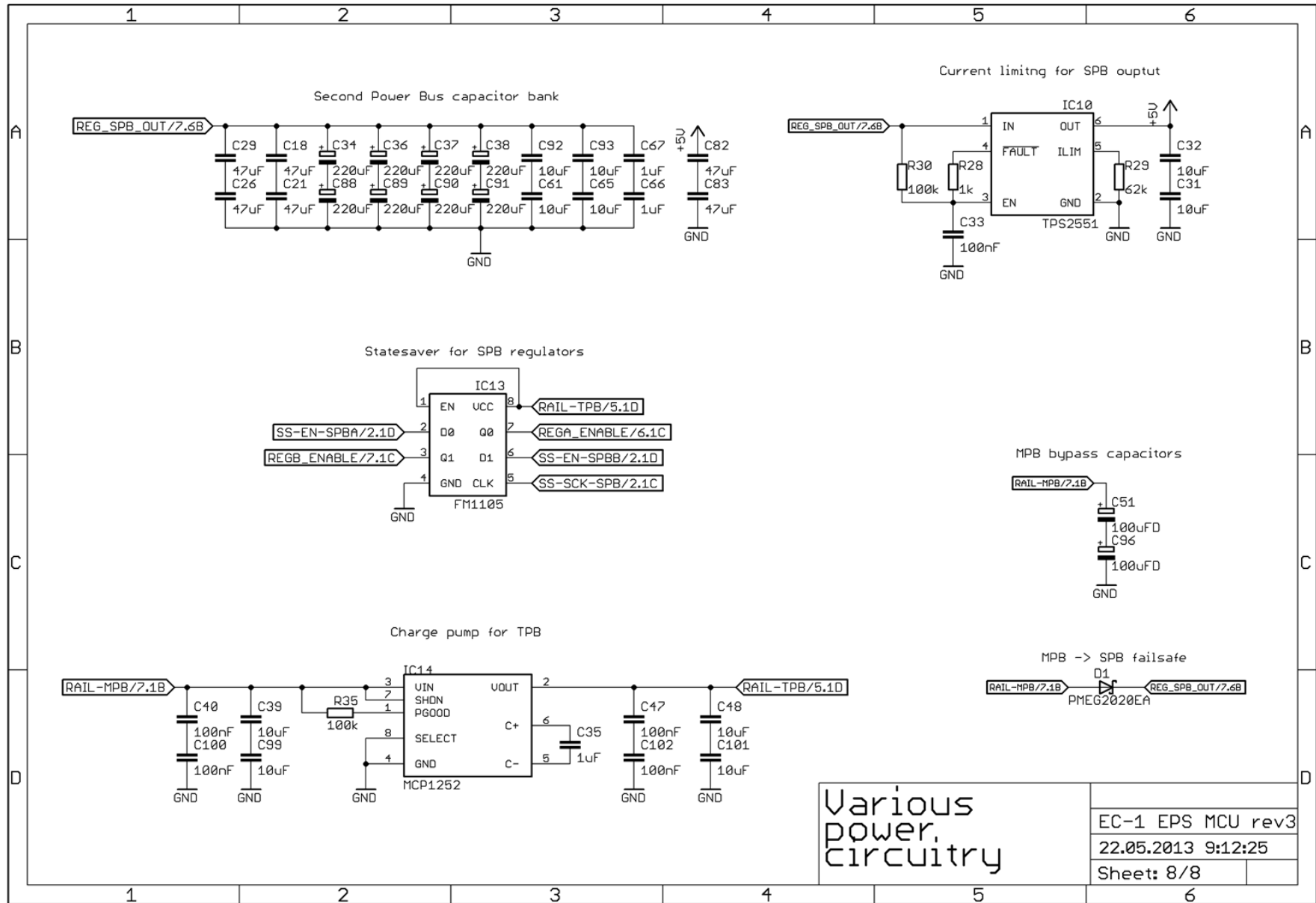


Figure 35. MCU power circuitry (TPB supply, SPB capacitance bank, SPB regulator state saver, SPB output current limiter and MPB to SPB failsafe interface).

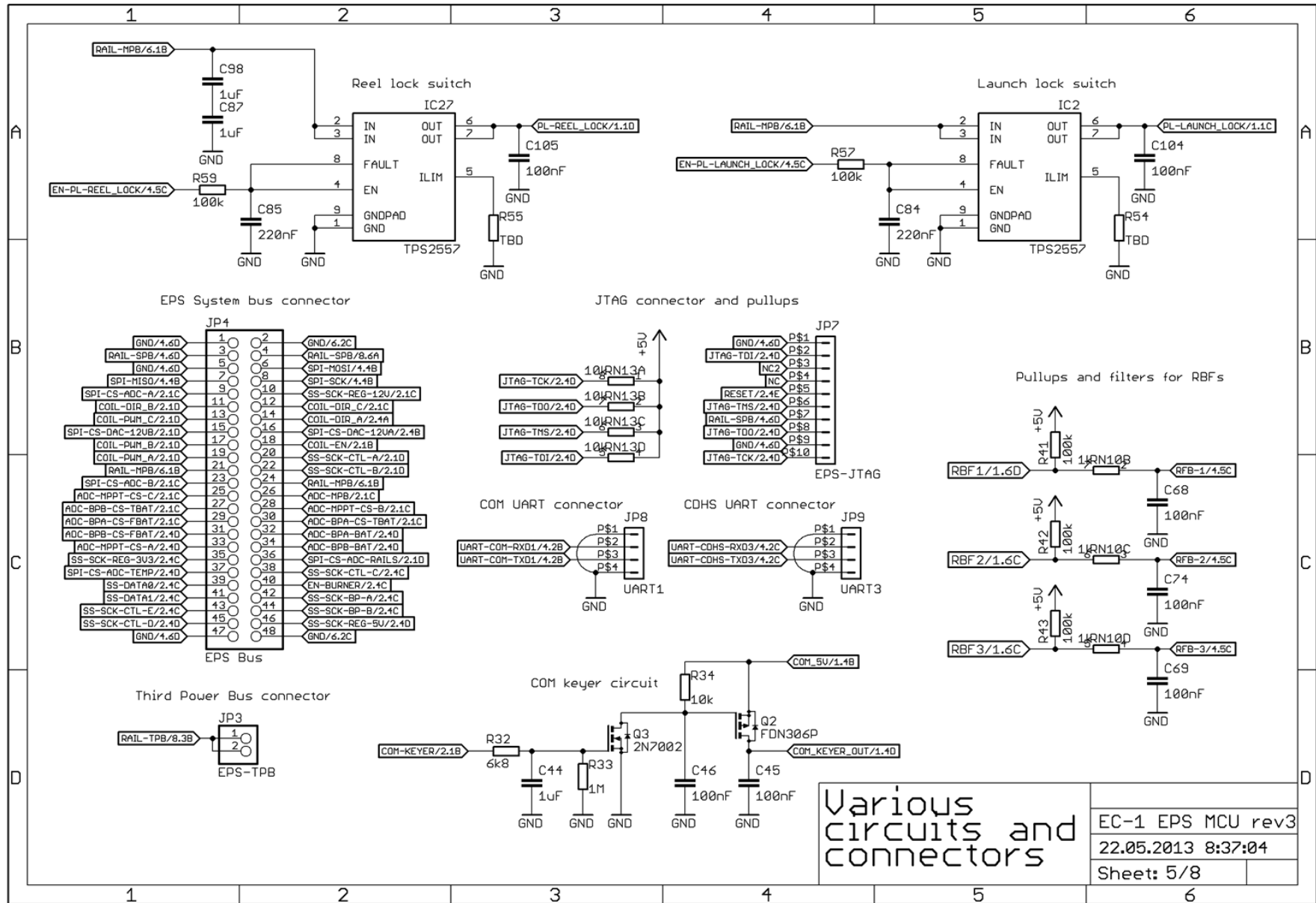


Figure 36. MCU various connectors (EPS system bus, TPB, JTAG and UART) and circuitry (PL lock switches, COM keyer, RBF frontend).

Appendix 2 – Board design

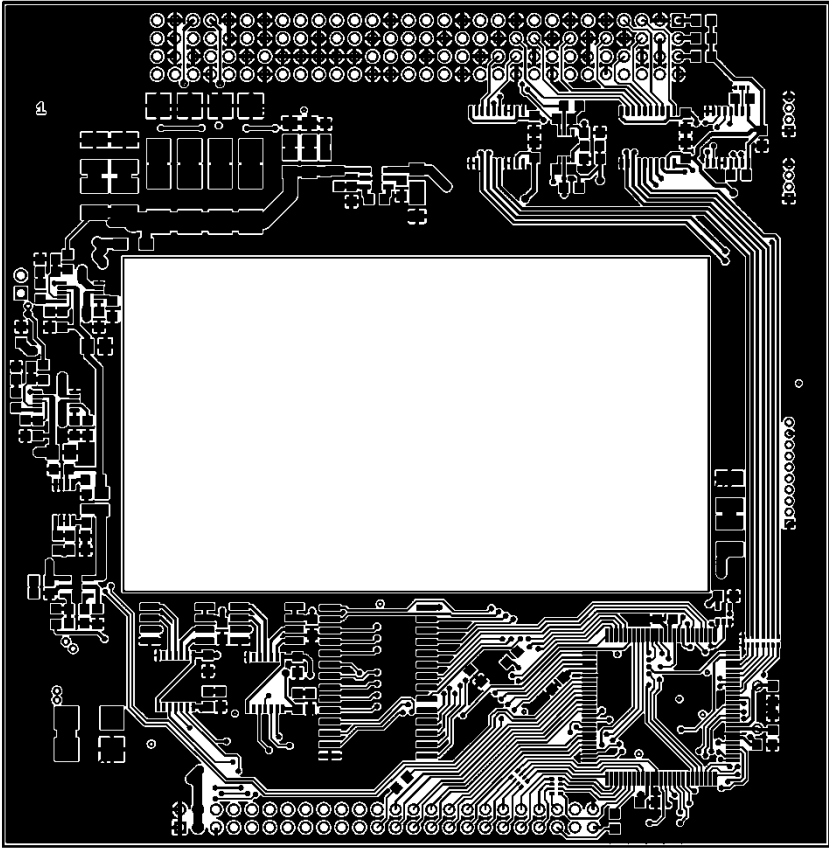


Figure 37. EPS MCU top layer (1.2 scale)

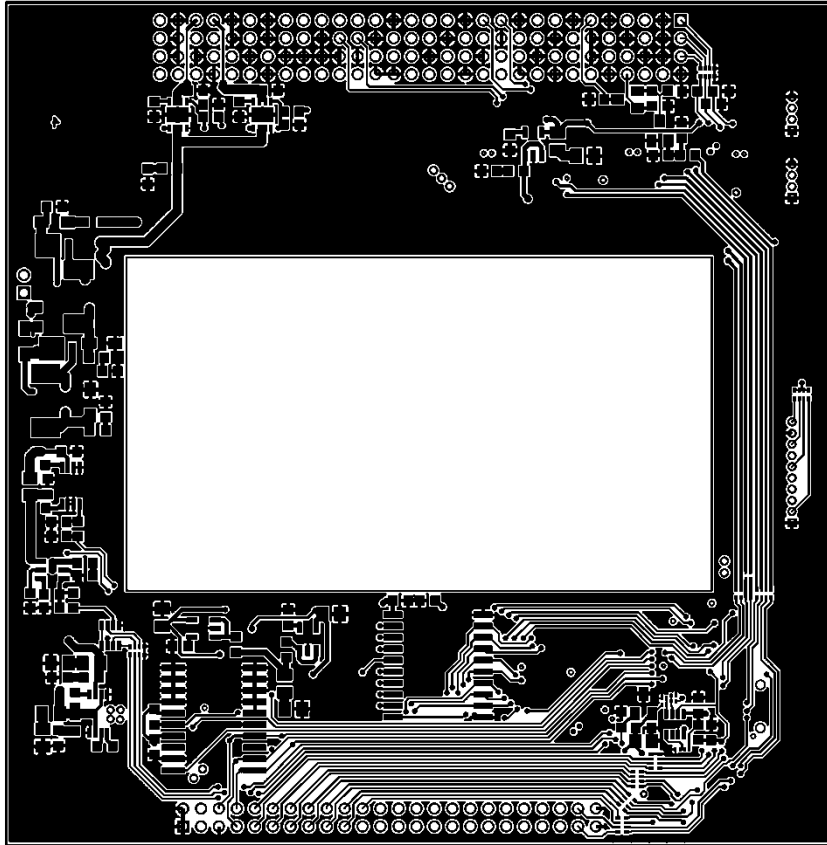


Figure 38. EPS MCU bottom layer (1.2 scale)

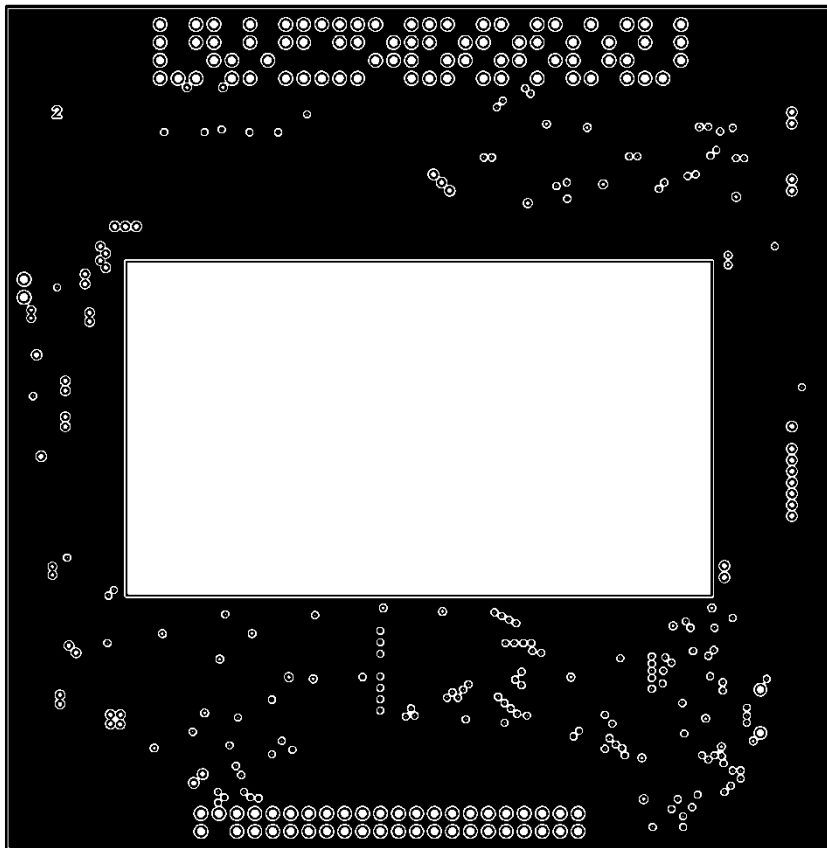


Figure 39. EPS MCU 1. inner layer (1.2 scale)

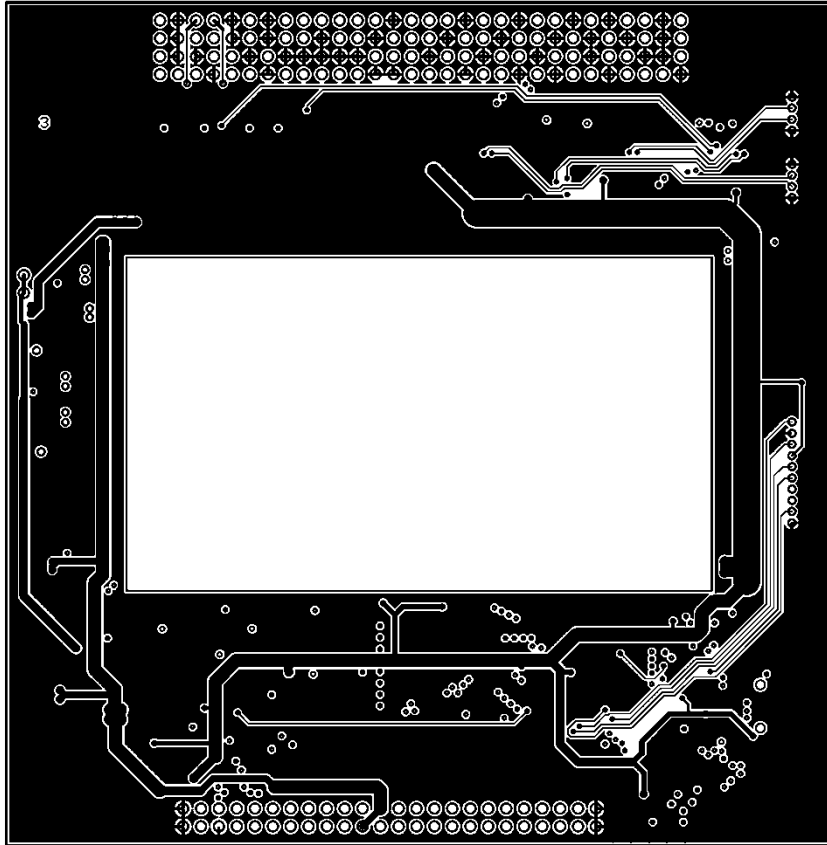


Figure 40. EPS MCU 2. inner layer (1.2 scale)

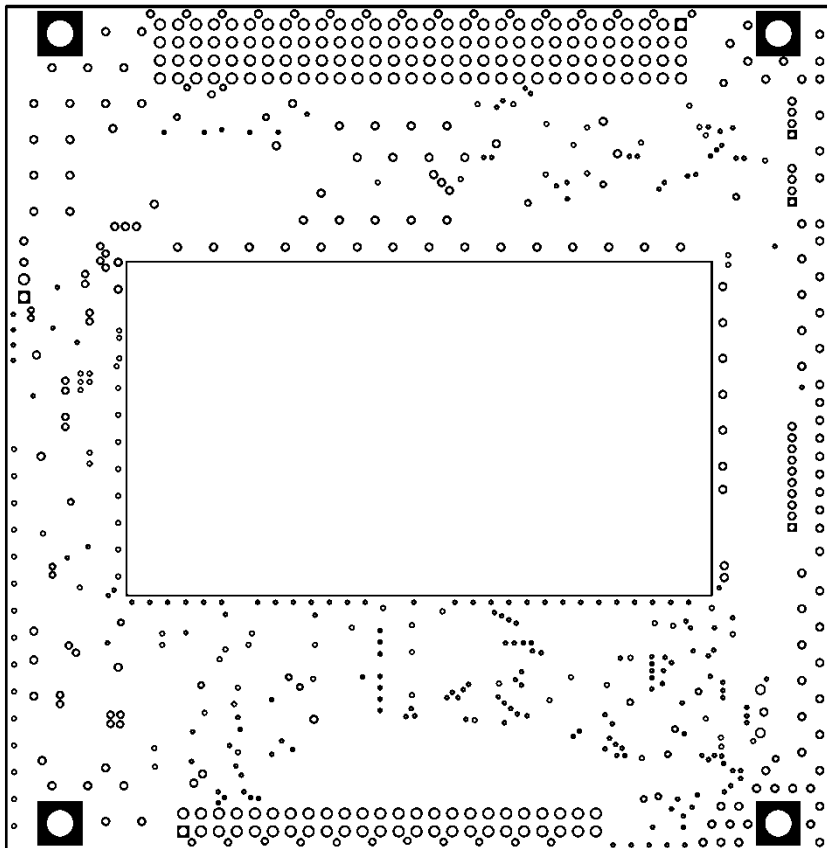


Figure 41. EPS MCU drills (1.2 scale)

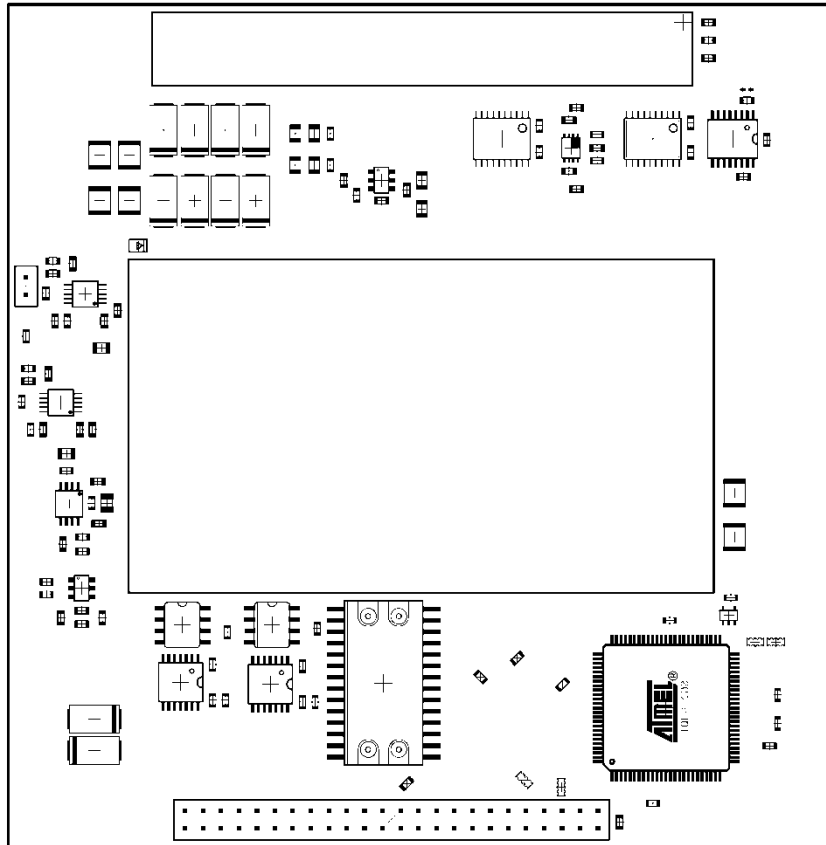


Figure 42. EPS MCU layout top layer (1.2 scale)

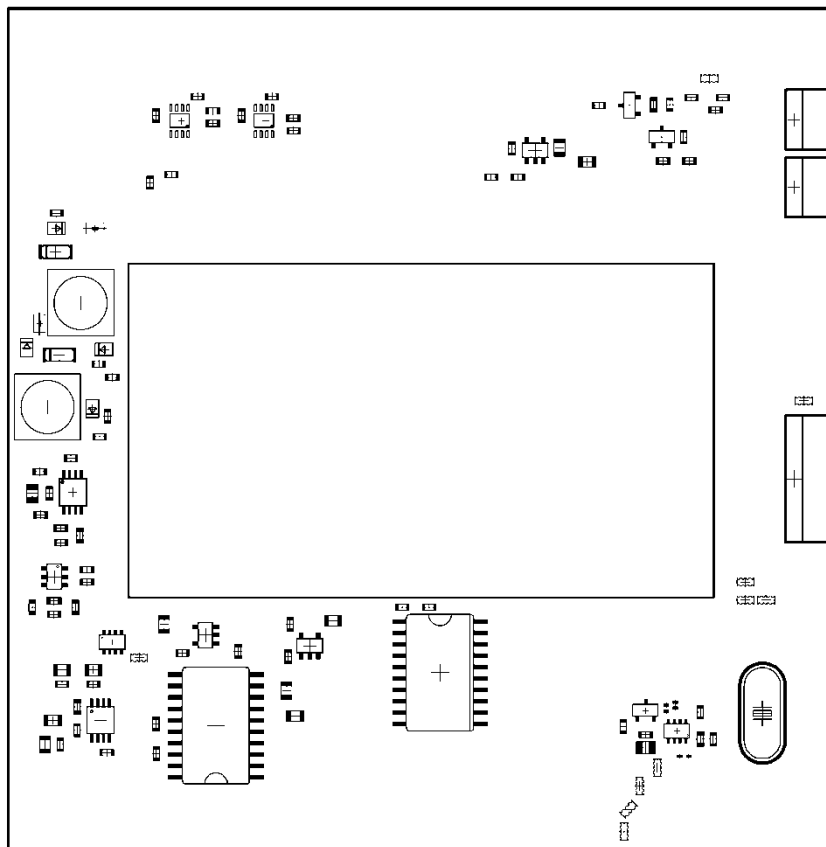


Figure 43. EPS MCU layout bottom layer (1.2 scale)

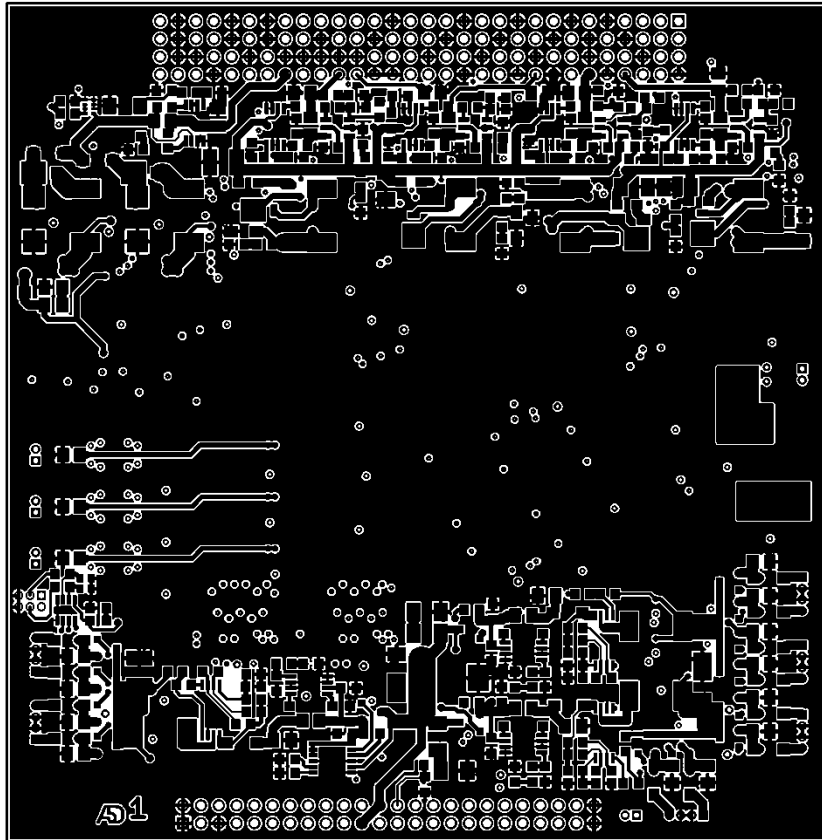


Figure 44. EPS PDU top layer (1.2 scale)

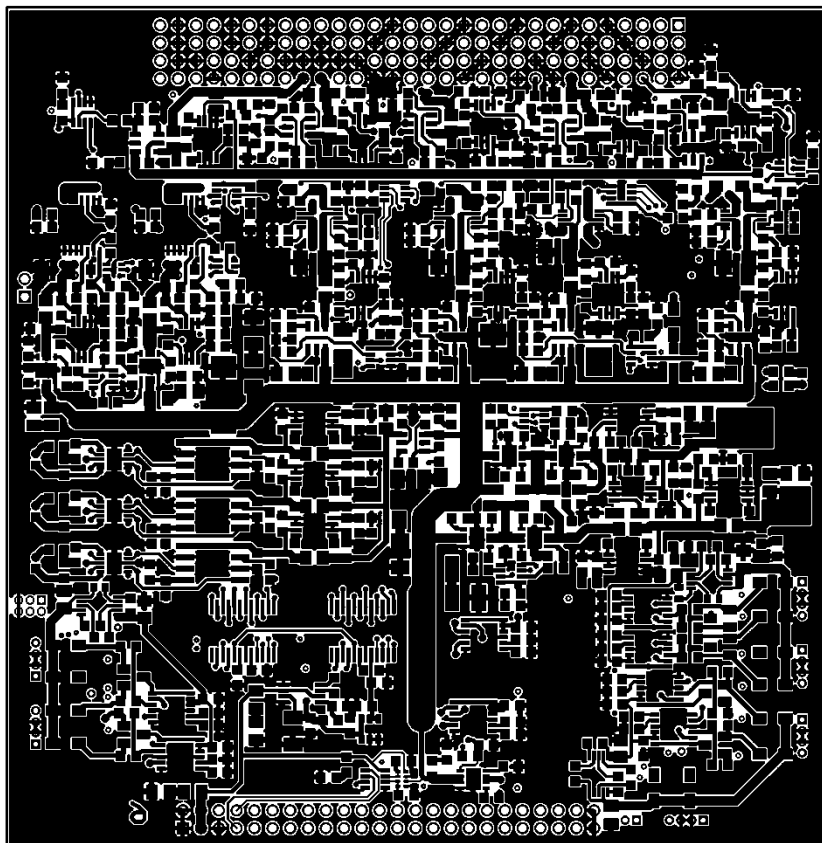


Figure 45. EPS PDU bottom layer (1.2 scale)

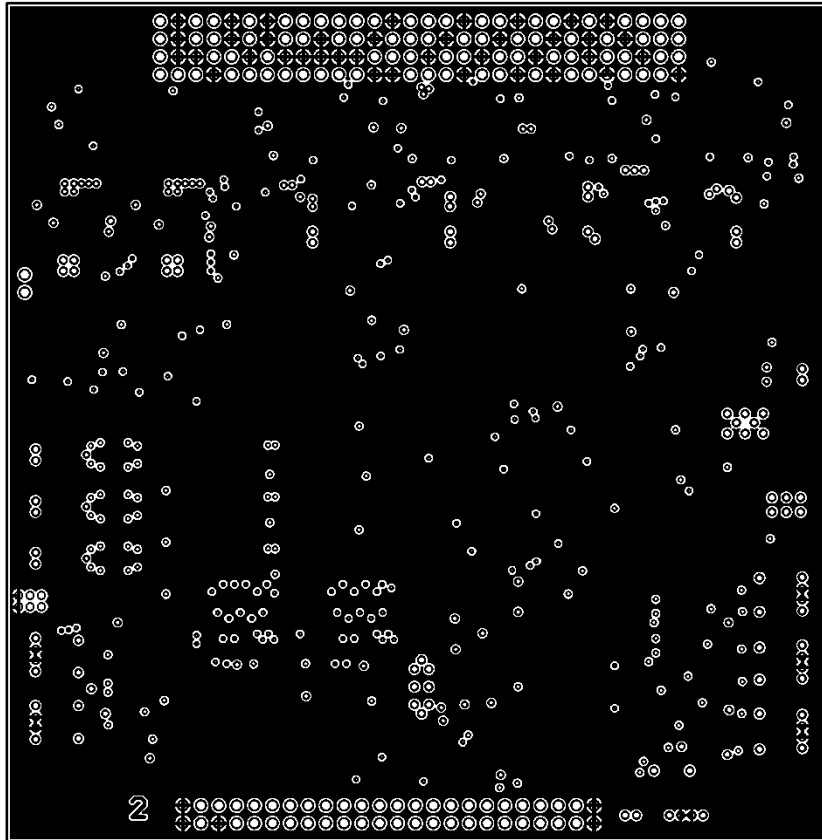


Figure 46. EPS PDU 1, inner layer (1.2 scale)

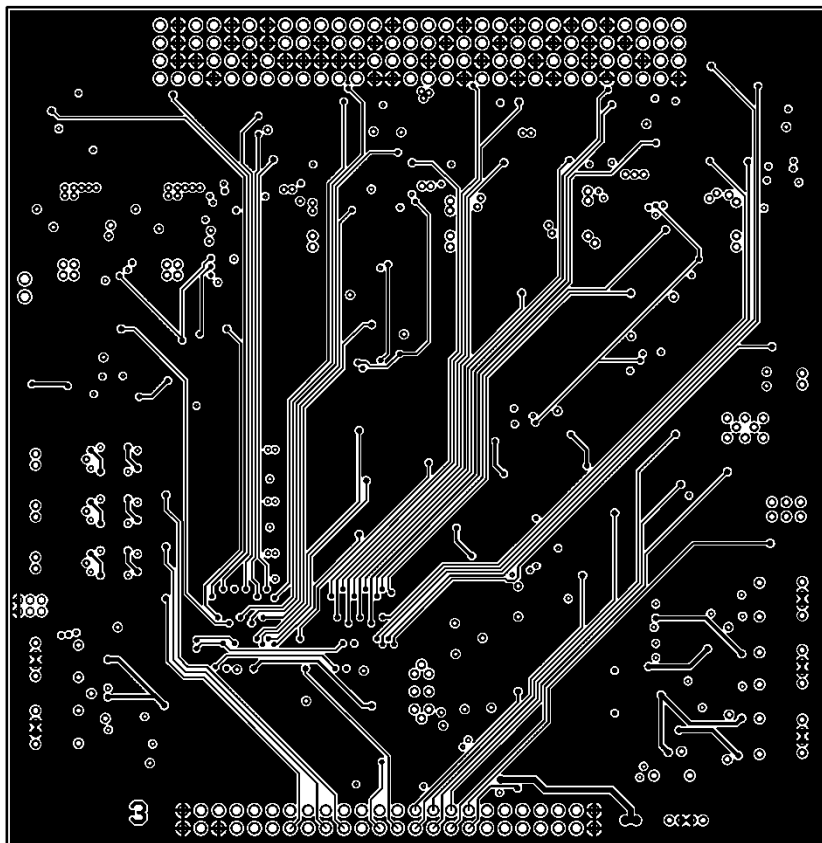


Figure 47. EPS PDU 2, inner layer (1.2 scale)

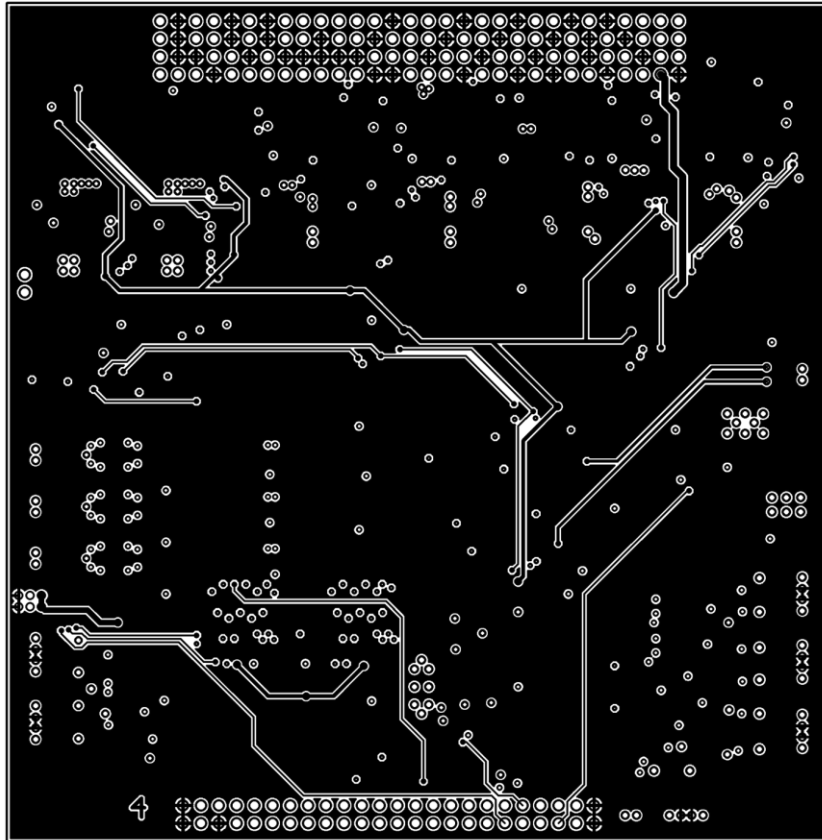


Figure 48. EPS PDU 3. inner layer (1.2 scale)

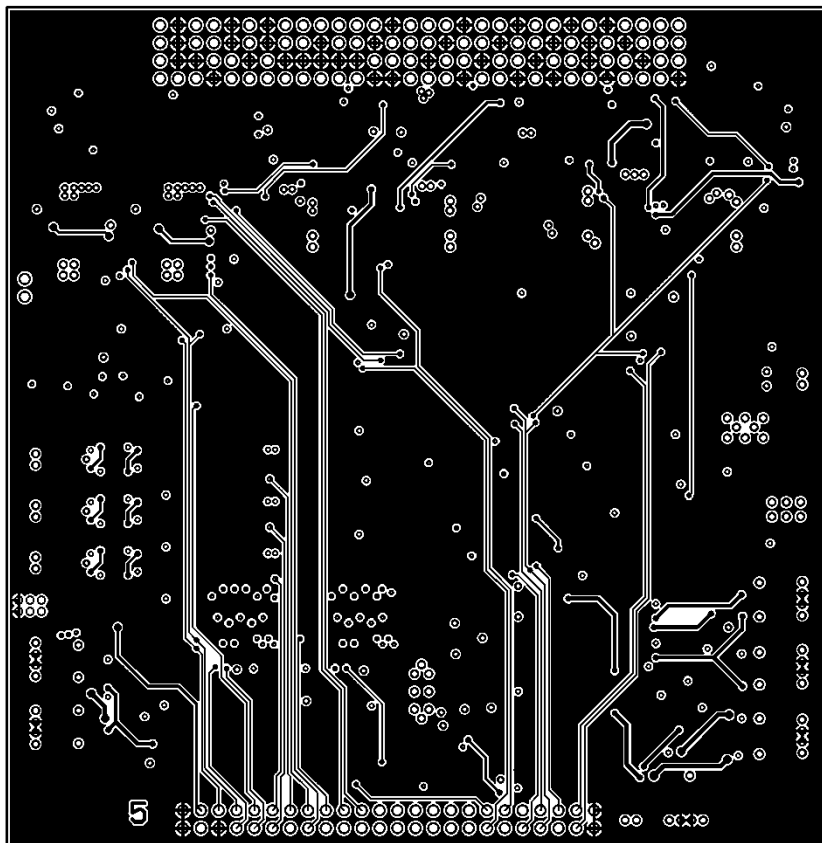


Figure 49. EPS PDU 4. inner layer (1.2 scale)

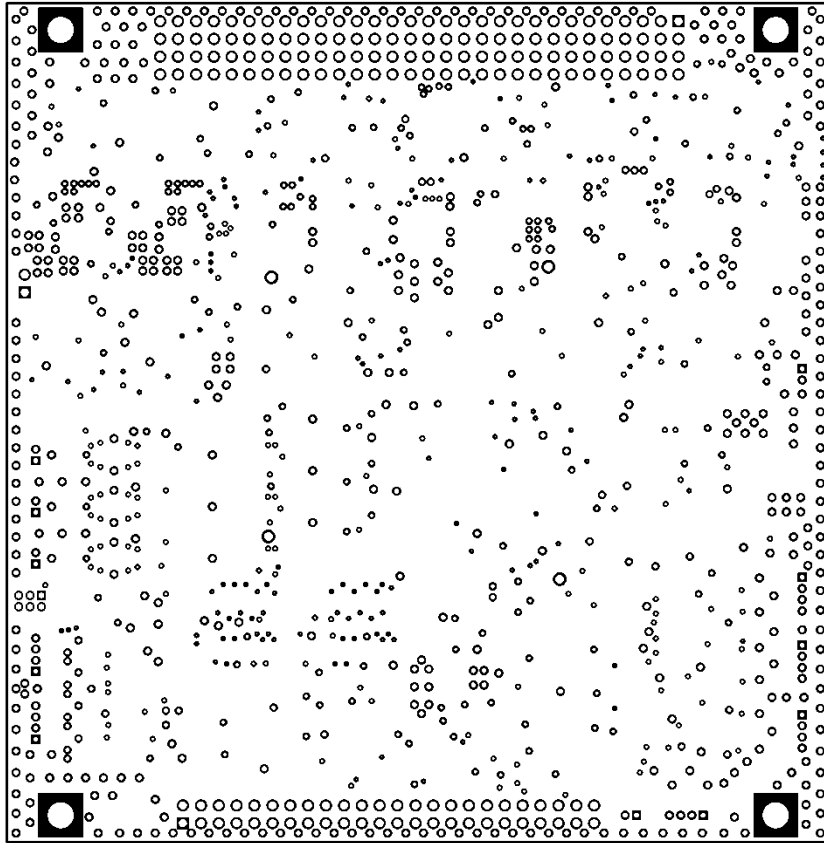


Figure 50. EPS PDU drills (1.2 scale)

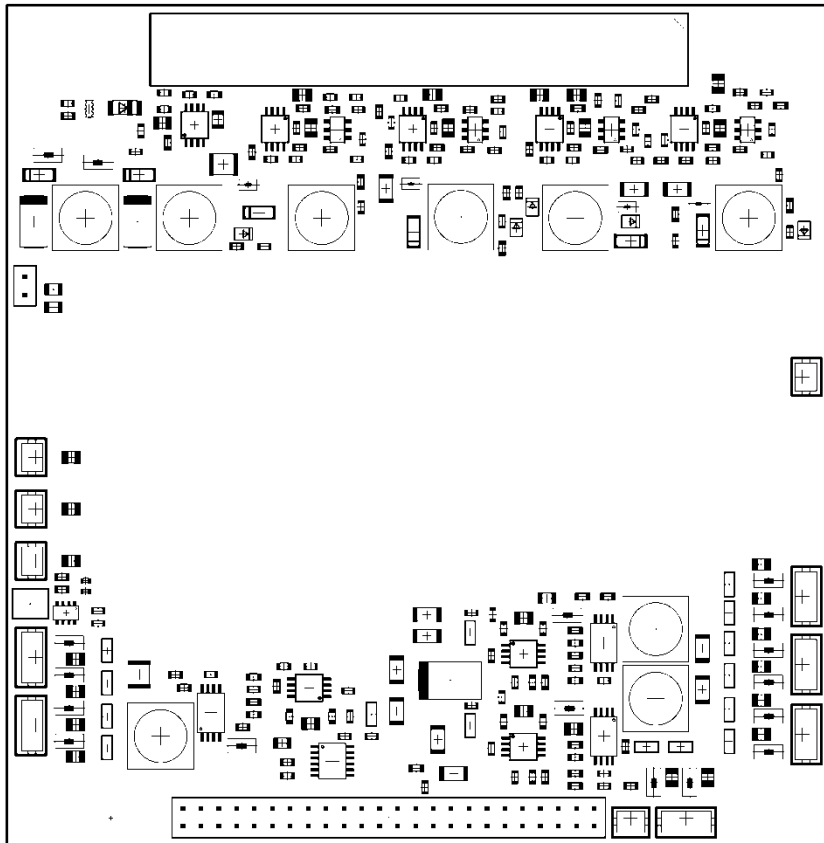


Figure 51. EPS PDU layout top layer (1.2 scale)

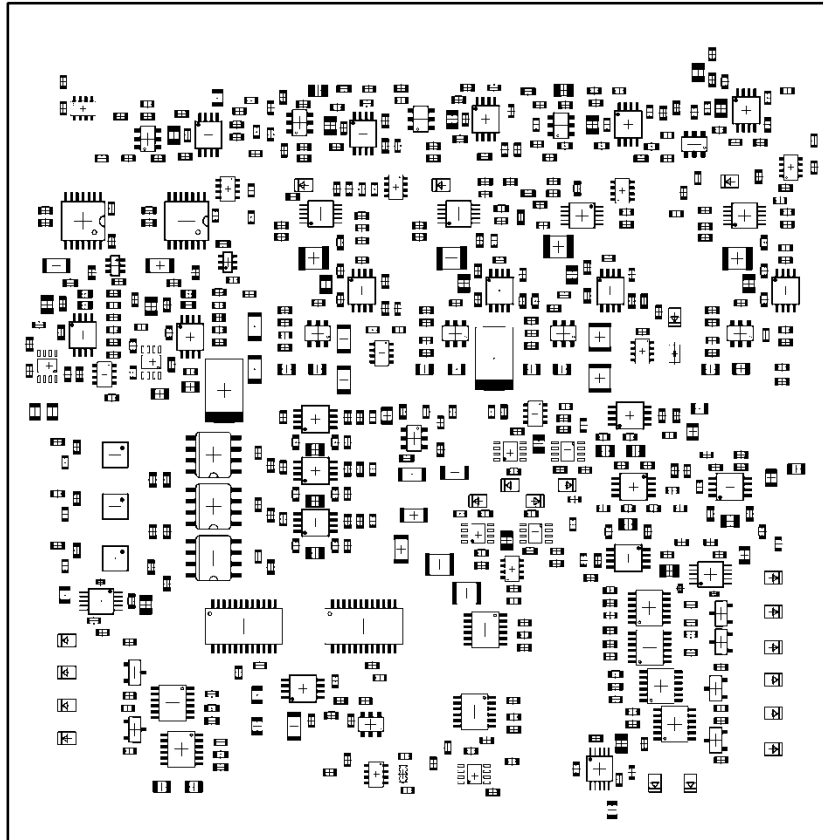


Figure 52. EPS PDU layout bottom layer (1.2 scale)

Appendix 3 – Bill of Materials

| Total | MCU | PDU | Name | Pack | Farnell ID | EU Mouser ID | Arrow ID |
|---------------------|-----|-----|--------------|----------|------------|---------------------|---------------------|
| Integrated Circuits | | | | | | | |
| 3 | 0 | 3 | A3901 | DFN-10 | 1651947 | | A3901SEJTR-T |
| 1 | 0 | 1 | ADR3450ARJZ | SOT23-6 | 1843665 | | ADR3450ARJZ-R2 |
| 3 | 0 | 3 | SPV1040 | TSSOP-8 | | 511-SPV1040T | |
| 2 | 0 | 2 | LM2700MT | TSSOP-14 | 9778993 | | LM2700MT-ADJ/NOPB |
| 2 | 0 | 2 | LTC2630 | SC70-6 | 1432739 | | LTC2630ISC6LZ12#PBF |
| 9 | 0 | 9 | LTC4352 | MSOP-12 | 1647760 | | LTC4352IMS#PBF |
| 3 | 0 | 3 | MAX319ESA | SOIC-8 | 1379913 | 700-MAX319ESA | |
| 2 | 0 | 2 | MAX1119 | SOT23-8 | | 700-MAX1119EKAT | |
| 2 | 0 | 2 | MAX1230 | QSOP-24 | | 700-MAX1230BEEG | |
| 1 | 0 | 1 | MCP1252ADJ | MSOP-8 | 1332066 | | |
| 3 | 0 | 3 | MCP1257 | MSOP-8 | 1851914 | | |
| 9 | 2 | 7 | TPS2557 | QFN-8 | 1782842 | 595-TPS2557DRBT | TPS2557DRBT |
| 2 | 0 | 2 | AD22100KTZ | TO-92 | 9605320 | | |
| 17 | 3 | 14 | TPS2551 | SOT23-6 | 1755631 | | TPS2551DBVT |
| 6 | 2 | 4 | LTC3440EMS | MSOP-10 | 1273938 | | LTC3440EMS#PBF |
| 28 | 2 | 26 | LT6105 | MSOP-8 | | | LT6105HMS8#PBF |
| 11 | 1 | 10 | FM1105 | SOT23-8 | | 877-FM1105 | |
| 1 | 1 | | 74AHC1G08DCK | SC70-5 | 1470829 | | SN74AHC1G08DCKR |
| 1 | 1 | | ATMEGA1280 | TQFP-100 | 1455090 | 556-ATMEGA1280-16AU | |
| 1 | 1 | | FM18W08 | SOIC-28 | 2077744 | | |
| 2 | 2 | | FM25V20 | SOIC-8 | | 877-FM25V20-G | |
| 1 | 1 | | MCP1252 | MSOP-8 | 1332064 | | |
| 2 | 2 | | TXB0108 | TSSOP-20 | 1494945 | | TXB0108PWR |
| 2 | 2 | | ADG3304 | TSSOP-14 | 1078228 | | |

| Total | MCU | PDU | Name | Pack | Farnell ID | EU Mouser ID | Arrow ID |
|---------------------|-----|-----|-------------|----------|------------|----------------------|----------|
| 1 | 1 | | DS3234 | TSSOP-20 | | 700-DS3234SN# | |
| 1 | 1 | | PCA9306 | TSSOP-8 | 1053573 | | |
| 1 | 1 | | SN74AC573 | SOIC-20 | 9590285 | | |
| 2 | 2 | | LP2985A | SOT23-5 | 1053660 | | |
| 1 | 1 | | TCA6408APWR | TSSOP-16 | 1903303 | | |
| 1 | 1 | | MAX6145 | SOT23 | 1673172 | | |
| 1 | 1 | | MAX6369 | SOT23-8 | 2085159 | | |
| Ceramic capacitors | | | | | | | |
| 2 | 2 | 0 | 18pF | NP0 0603 | | | |
| 2 | 0 | 2 | 180pF | NP0 0603 | | | |
| 9 | 2 | 7 | 1nF | NP0 0603 | | | |
| 6 | 2 | 4 | 1.5nF | NP0 0603 | | | |
| 45 | 2 | 43 | 2.2nF | NP0 0603 | | | |
| 2 | 0 | 2 | 2.2nF | NP0 0402 | | | |
| 2 | 0 | 2 | 2.7nF | NP0 0603 | | | |
| 181 | 50 | 131 | 100nF HR | X7R 0603 | | 810-CGA3E2X7R1H104K | |
| 9 | 2 | 7 | 220nF HR | X7R 0603 | | 810-CGA3E1X7R1E224K | |
| 43 | 10 | 33 | 1uF HR | X7R 0603 | | 810-CGA3E1X7R1E105K | |
| 40 | 5 | 35 | 10uF HR | X5R 0805 | | 810-CGA4J3X5R1A106K | |
| 28 | 12 | 16 | 10uF | X5R 0805 | 1845747 | | |
| 1 | 0 | 1 | 10uF 25V | X5R 0805 | 1735530 | | |
| 6 | 0 | 6 | 22uF | X5R 1206 | 1833823 | | |
| 10 | 0 | 10 | 22uF HR | X7R 1210 | | 81-GCM32ER71C226K19L | |
| 3 | 0 | 3 | 47uF HR | X7R 1210 | | 81-GCM32ER70J476KE9L | |
| 20 | 6 | 14 | 47uF | X5R 1210 | 2112721 | | |
| 4 | 1 | 3 | TBD | XxR 0603 | | | |
| Tantalum capacitors | | | | | | | |
| 2 | 0 | 2 | 22uF | C | 1754111 | | |

| Total | MCU | PDU | Name | Pack | Farnell ID | EU Mouser ID | Arrow ID |
|-----------|-----|-----|---------------------|-----------|------------|--------------|----------|
| 10 | 10 | 0 | 220uF | C | 1793879 | | |
| 2 | 0 | 2 | 330uF | D | 1754080 | | |
| 1 | 0 | 1 | 470uF | E | 1754081 | | |
| Resistors | | | | | | | |
| 4 | 1 | 3 | 0R | 5% 0603 | | | |
| 2 | 0 | 2 | R015 | 1% 0805 | | | |
| 2 | 0 | 2 | R02 | 1% 0805 | 1107333 | | |
| 4 | 0 | 4 | R025 | 1% 0805 | | | |
| 5 | 0 | 5 | R04 | 1% 0805 | 1107336 | | |
| 1 | 0 | 1 | R075 | 1% 0805 | | | |
| 1 | 0 | 1 | R09 | 1% 0805 | 1865235 | | |
| 2 | 2 | 0 | R15 | 1% 0805 | 1717814 | | |
| 7 | 0 | 7 | R2 | 1% 0805 | 1107345 | | |
| 1 | 0 | 1 | R27 (ADCS) | 1% 0805 | 1838640 | | |
| 1 | 0 | 1 | R56 (PL3V3) | 1% 0805 | | | |
| 3 | | 3 | 1R | 1% 0603 | | | |
| 6 | 2 | 4 | 2R | 1% 0603 | | | |
| 3 | | 3 | 10R | 1% 0603 | | | |
| 1 | 1 | 0 | 33R resistor array | 5% 0804 | | | |
| 62 | 4 | 58 | 100R | 1% 0603 | 2008332 | | |
| 10 | | 10 | 1k | 5% 0402 | | | |
| 30 | 6 | 24 | 1k | 5% 0603 | | | |
| 12 | 12 | 0 | 1k resistor array | 5% 0804 | 9235361 | | |
| 4 | 4 | 0 | 4k7 | 5% 0603 | | | |
| 2 | 1 | 1 | 10k resistor array | 5% 0804 | 1770152 | | |
| 1 | | 1 | 100k resistor array | 5% 0804 | 9235469 | | |
| 3 | | 3 | 10k | 5% 0402 | | | |
| 33 | 8 | 25 | 10k | 5% 0603 | | | |
| 29 | 2 | 27 | 10k (LT6105 GAIN) | 0.5% 0603 | 1840588 | | |

| Total | MCU | PDU | Name | Pack | Farnell ID | EU Mouser ID | Arrow ID |
|-------------|-----|-----|-------------------|-----------|------------|----------------------|----------|
| 6 | 2 | 4 | 15k | 1% 0603 | | | |
| 1 | | 1 | 33k | 1% 0603 | | | |
| 45 | 2 | 43 | 75k (Low Pass) | 1% 0603 | 2059486 | | |
| 2 | | 2 | 75k (12V FB) | 0.1% 0603 | 1670201 | | |
| 25 | 10 | 15 | 100k | 5% 0603 | | | |
| 9 | | 9 | 100k | 5% 0402 | | | |
| 2 | | 2 | 150k | 1% 0603 | | | |
| 1 | 1 | 0 | 200k | 5% 0603 | | | |
| 6 | 2 | 4 | 200k (3V3, 5V FB) | 0.1% 0603 | 1160402 | | |
| 6 | 2 | 4 | 220k | 1% 0603 | | | |
| 3 | | 3 | 330k (MPPT FB) | 0.1% 0603 | 1577639 | | |
| 2 | | 2 | 340k (3V3 FB) | 1% 0603 | 1171038 | | |
| 4 | 2 | 2 | 619k (5V FB) | 1% 0603 | 1171065 | | |
| 2 | | 2 | 649k (12V FB) | 1% 0603 | 1171067 | | |
| 3 | | 3 | 768k (MPPT FB) | 1% 0603 | 1171075 | | |
| 8 | 2 | 6 | 1M | 1% 0603 | | | |
| 32 | 5 | 27 | TBD | 1% 0603 | | | |
| Diodes | | | | | | | |
| 6 | 0 | 6 | BAS70-05 | SOT23 | 1797836 | | |
| 2 | 0 | 2 | MBRM130LT1G | POWERMITE | 1651128 | 863-MBRM130LT1G | |
| 6 | 2 | 4 | MBRM120LT3G | POWERMITE | 1459064 | 863-MBRM120LT3G | |
| 18 | 2 | 16 | PMEG2010EA | SOD-323 | 8737908 | 771-PMEG2010EA-T/R | |
| 1 | 0 | 1 | PMEG2020AEA | SOD-323 | 8737940 | | |
| 11 | 3 | 8 | CRS06 | SOD-323 | 1300795 | 757-CRS06(TE85L,Q,M) | |
| 1 | 0 | 1 | Zener 5.1V | SOD-80C | | | |
| Transistors | | | | | | | |
| 1 | 1 | 0 | 2N7002K | SOT23 | 1758065 | | |
| 15 | 0 | 15 | PMV22EN | SOT23 | 1894625 | 771-PMV22EN215 | |
| 1 | 1 | 0 | FDN306P | SOT23 | 1471047 | | |

| Total | MCU | PDU | Name | Pack | Farnell ID | EU Mouser ID | Arrow ID |
|------------------------|-----|-----|--------------------|-------------|------------|----------------------|----------|
| Inductors and ferrites | | | | | | | |
| 6 | 2 | 4 | B82472G6103M | 7.3x7.3 max | 1644569 | | |
| 2 | 0 | 2 | DRA73-150-R | 7.3x7.3 max | 2145221 | | |
| 17 | 0 | 17 | Ferrite bead | 1206 | 1651732 | | |
| 7 | 2 | 5 | Ferrite bead | 0805 | 1669751 | | |
| Connectors | | | | | | | |
| 4 | 0 | 4 | 2P-Wire-Side | DF13-1.25 | | 798-DF13-2S-1.25C | |
| 4 | 0 | 4 | 2P-PCB-Side | DF13-1.25 | 1324877 | | |
| 8 | 2 | 6 | 4P-Wire-Side | DF13-1.25 | 1324864 | | |
| 6 | 0 | 6 | 4P-PCB-Side | DF13-1.25 | 1324879 | | |
| 2 | 2 | 0 | 4P-PCB-Side-Angle | DF13-1.25 | | | |
| 1 | 1 | 0 | 10P-Wire-Side | DF13-1.25 | | 798-DF13-10S-1.25C | |
| 1 | 1 | 0 | 10P-PCB-Side-Angle | DF13-1.25 | | 798-DF13-10P1.25DS20 | |
| 50 | 18 | 32 | Crimp | DF13 | 1324945 | 798-DF13-2630SCFA | |
| 1 | 1 | 0 | 2.0p M | 2x40, long | | | |
| 1 | 0 | 1 | 2.0p F | 2x50 | 1668196 | | |
| 1 | 0 | 1 | 1.27 F | 2x8 | 1865315 | | |
| 1 | 0 | 1 | 2.0p F | 1x2 | 1668161 | | |
| Crystals | | | | | | | |
| 1 | 1 | 0 | 8MHz crystal | | 1703597 | | |

Appendix 4 – Measurement results

Table 5. Battery protection shunt resistor values.

| Measurement point | Maximum rated current (A) | Shunt resistor value (Ω) | Max measurable current (A) | 1 bit resolution (μA) |
|-------------------|---------------------------|-----------------------------------|----------------------------|------------------------------------|
| Charge | 1 | 0.025 | 1.04 | 6900 |
| Discharge | 1.7 | 0.015 | 1.73 | 11000 |

Table 6. Regulator shunt resistor values.

| Measurement point | Maximum rated current (A) | Shunt resistor value (Ω) | Max measurable current @ 2.6 V (A) | 1 bit resolution (μA) |
|-------------------|---------------------------|-----------------------------------|------------------------------------|------------------------------------|
| REG 3.3 V IN | 0.6 | 0.04 | 0.65 | 300 |
| REG 5 V IN | 0.9 | 0.025 | 1.04 | 480 |
| REG 12 V IN | 1.3 | 0.02 | 1.3 | 620 |

Table 7. Regulator output measurement resolution.

| Measurement point | 1 bit resolution (mV) |
|------------------------------------|-----------------------|
| 3.3 V regulator output | 1.2 |
| 5 V regulator output | 1.2 |
| 12 V regulator output ⁶ | 3.7 |

⁶ Has 3:1 voltage divider in the output

Table 8. CTL shunt resistor values.

| Measurement point | Maximum rated current (A) | Shunt resistor value (Ω) | Max measurable current ⁷ (A) | 1 bit resolution (μ A) |
|-------------------|---------------------------|-----------------------------------|---|-----------------------------|
| ADCS | 0.1 | 0.27 | 0.14 | 40 |
| CAM | 0.1 | 0.2 | 0.11 | 61 |
| CDHS A, B, BSW | 0.1 | 0.2 | 0.11 | 62 |
| COM 3.3 V | 0.15 | 0.15 | 0.15 | 83 |
| COM 5 V | 0.5 | 0.075 | 0.52 | 166 |
| PL 3.3 V | 0.04 | 0.56 | 0.04 | 22 |
| PL 5 V | 0.25 | 0.15 | 0.26 | 82 |
| PL 12 V | 0.35 | 0.09 | 0.56 | 140 |

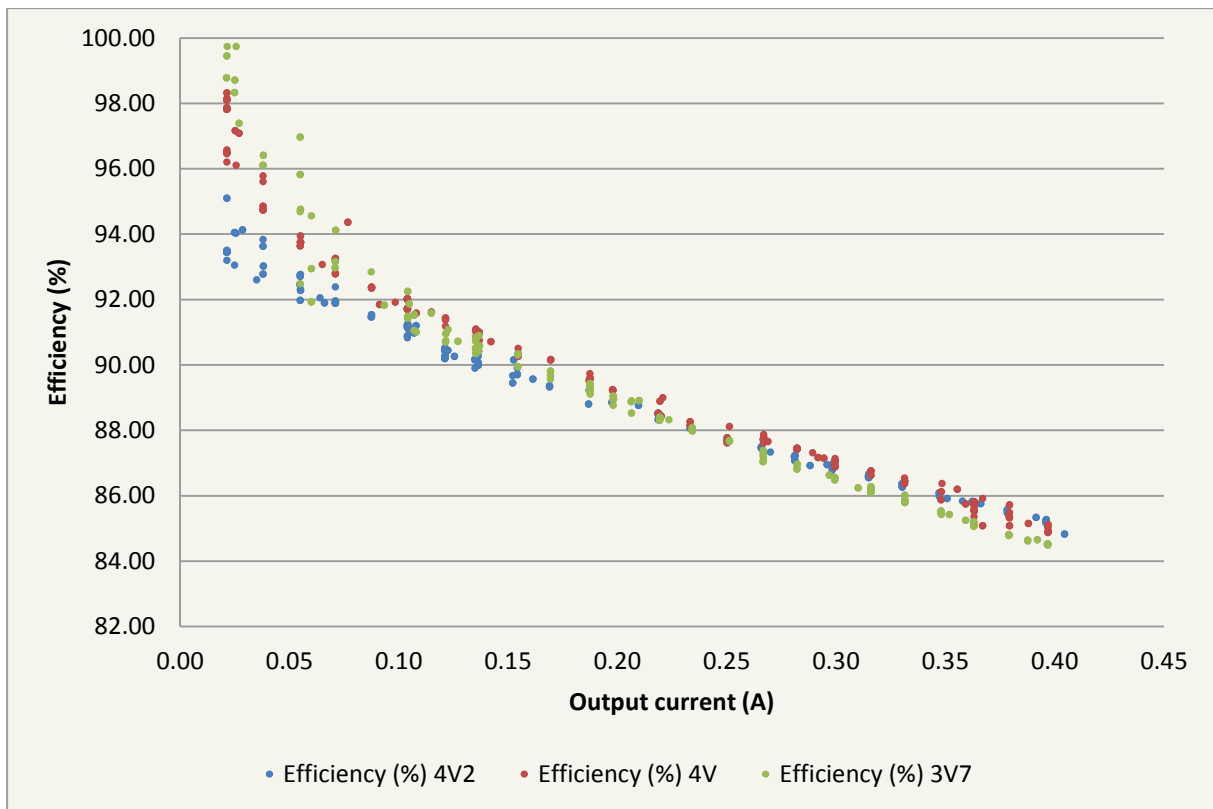


Figure 53. 3.3 V regulator A output efficiencies.

⁷ 2.2 V @ 3.3 V circuits, 3.9 V @ 5 V circuits, 5 V @ 12 V circuits

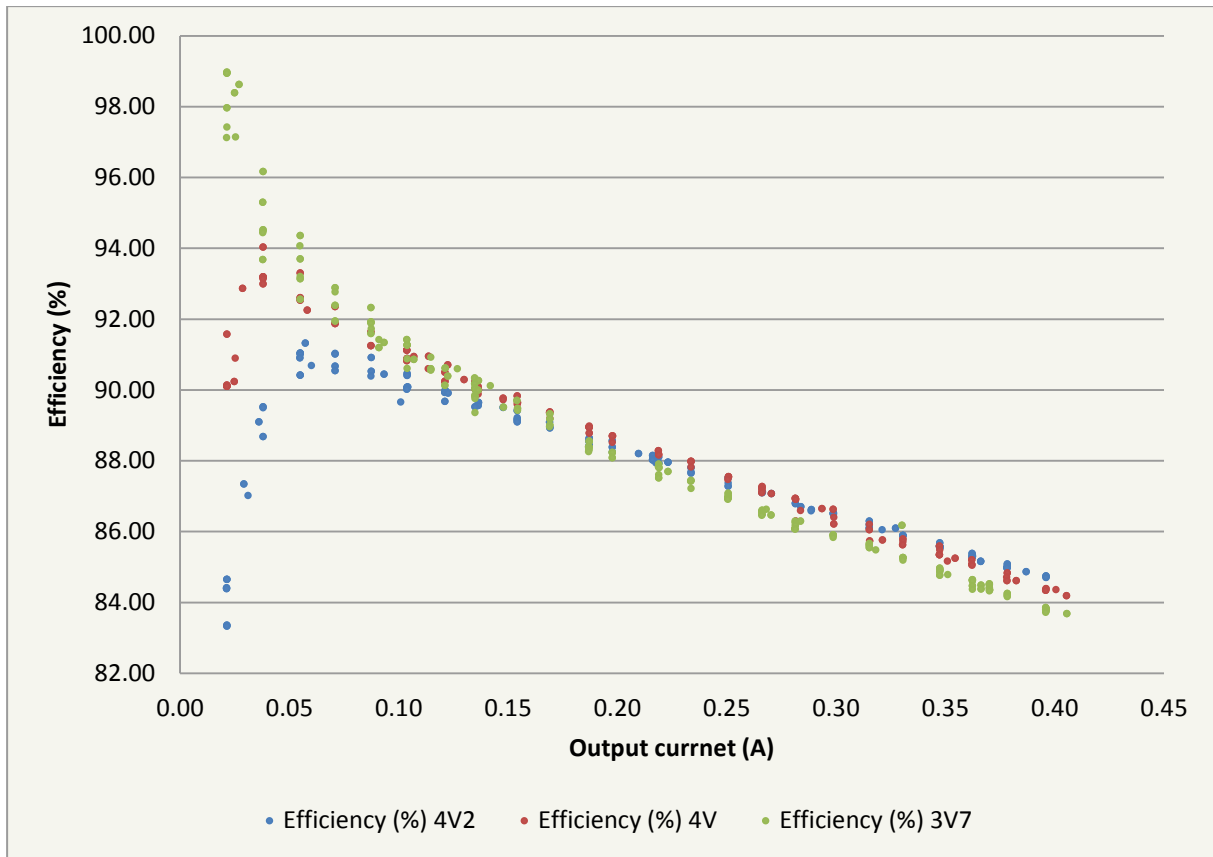


Figure 54. 3.3 V regulator B output efficiencies.

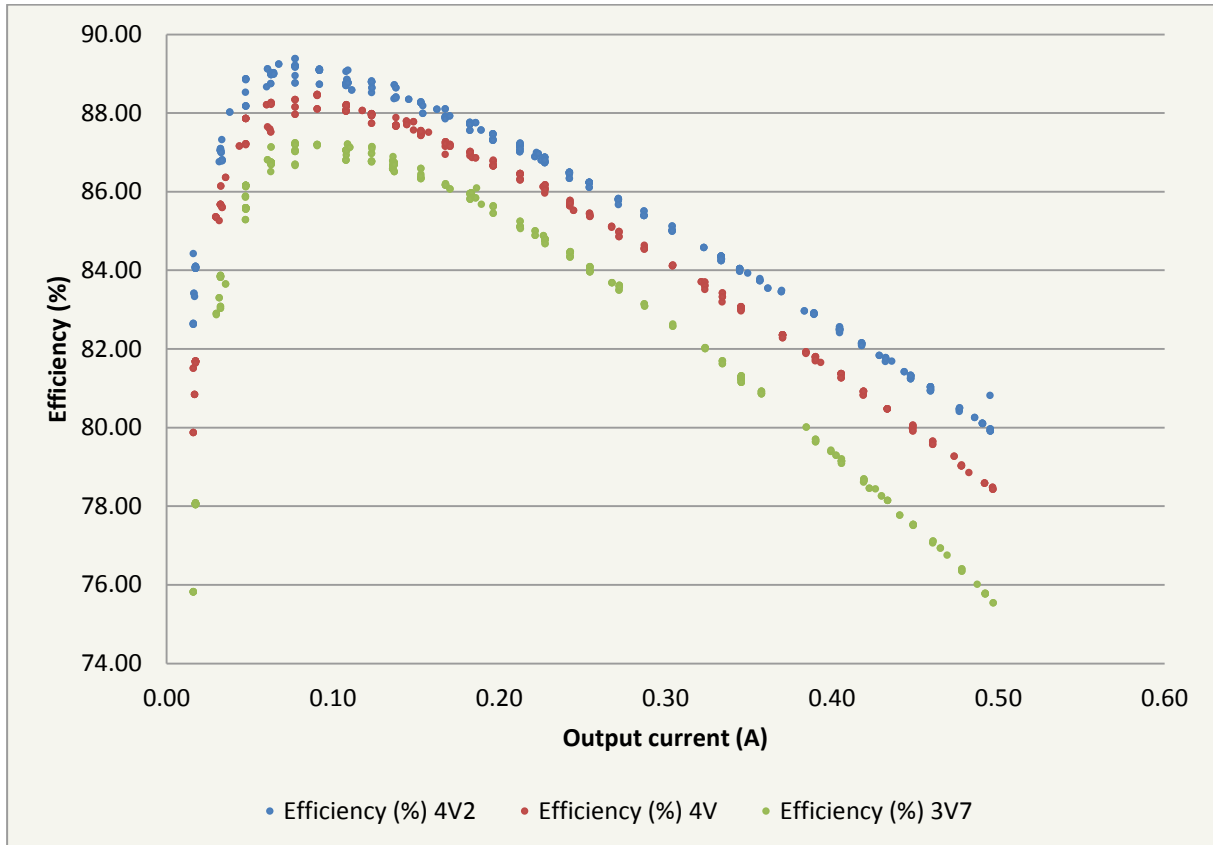


Figure 55. 5 V regulator A output efficiencies.

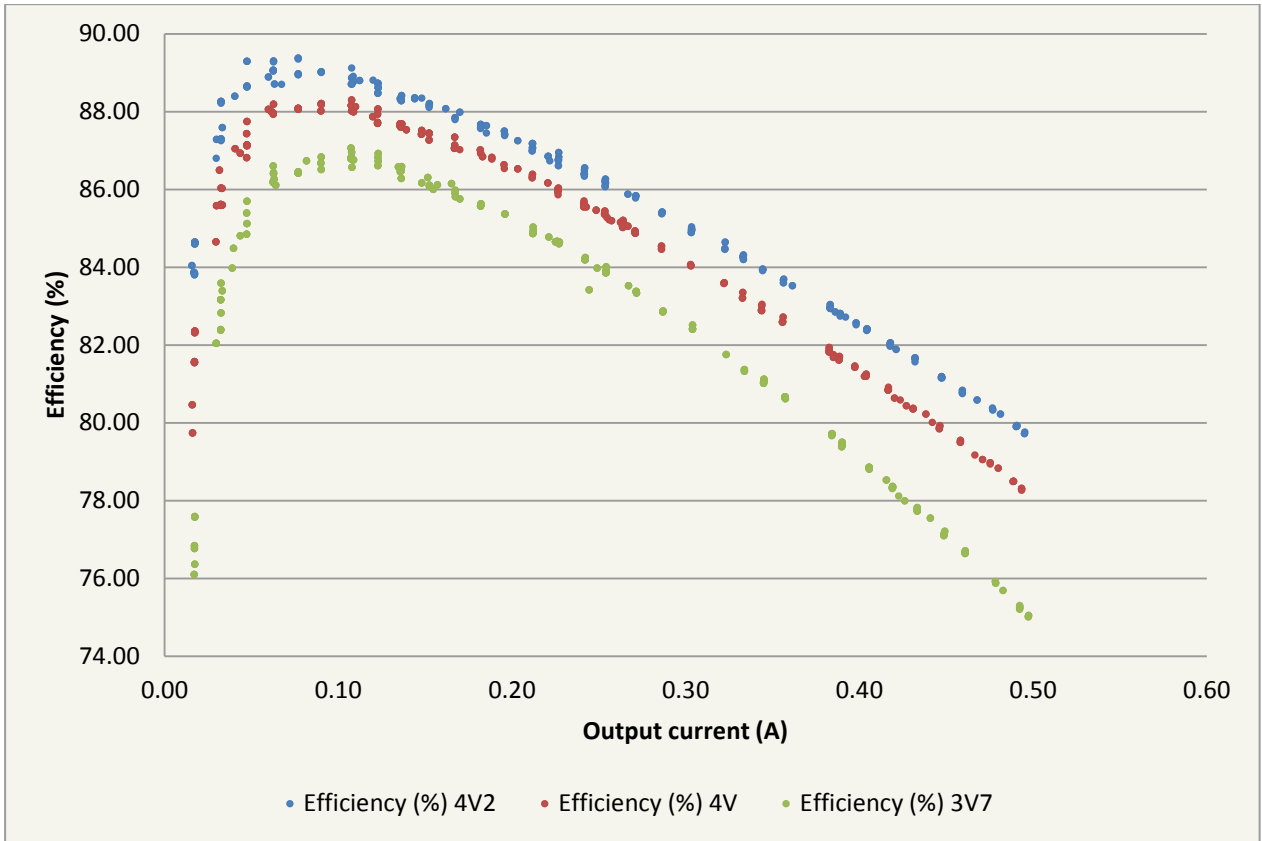


Figure 56. 5 V regulator B output efficiencies.

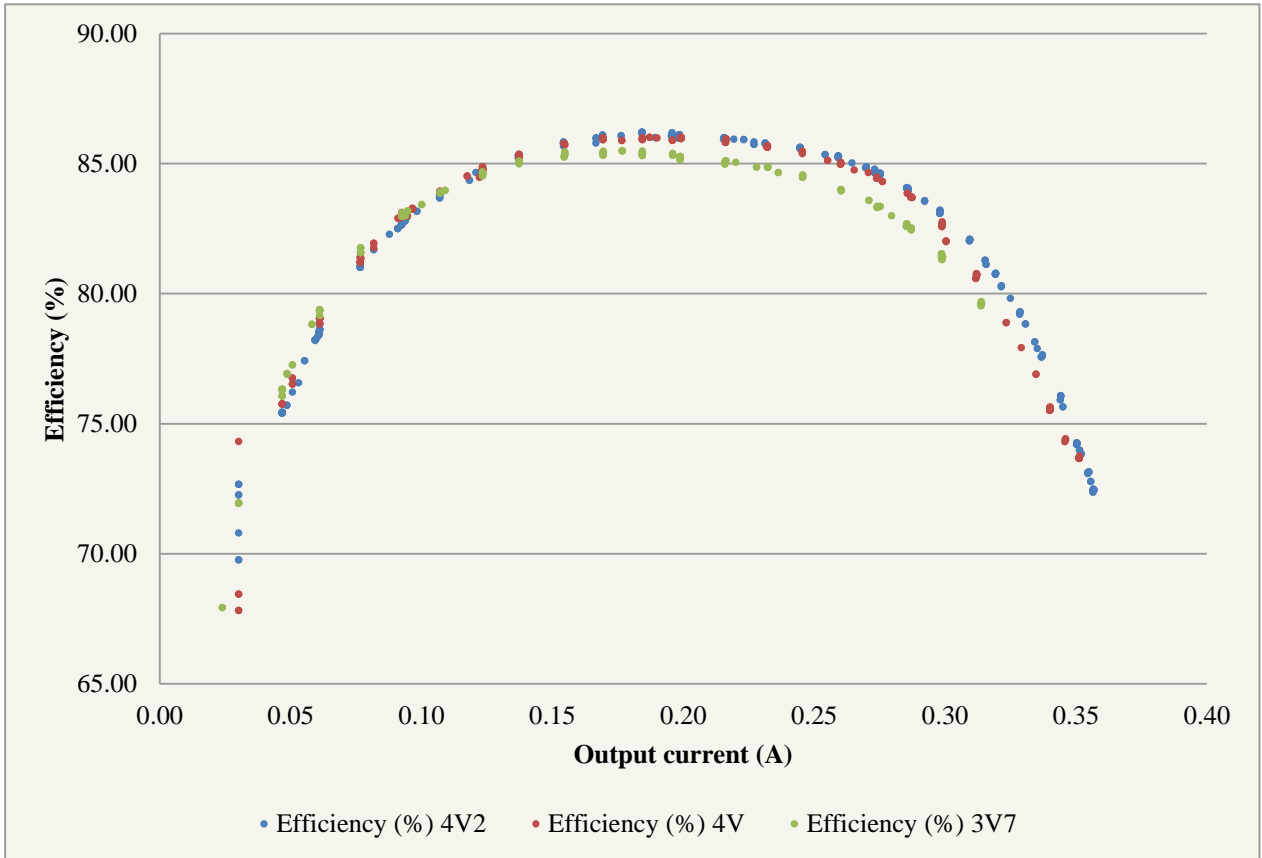


Figure 57. 12 V regulator A output efficiencies.

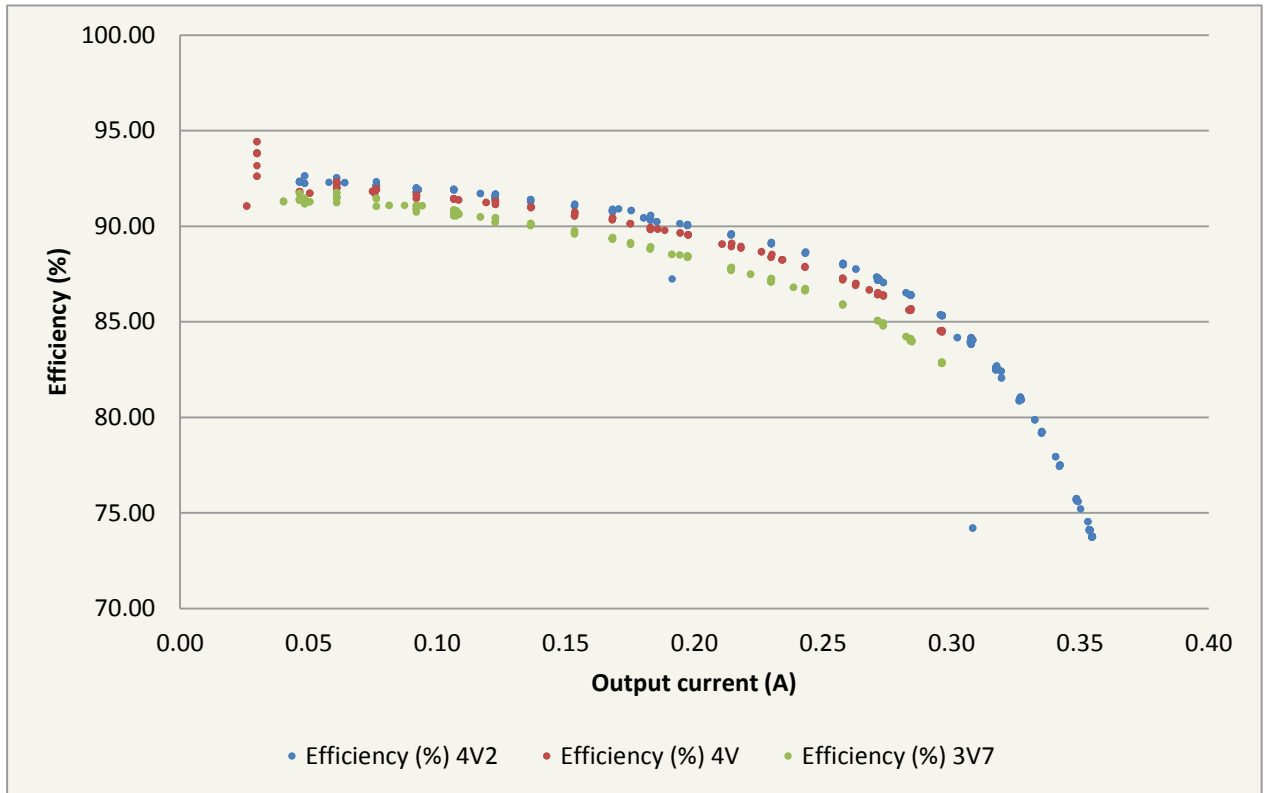


Figure 58. 12 V regulator B efficiencies.

Acknowledgements

I would like to thank my supervisor and EPS team coordinator Mihkel Pajusalu for the support and advice given throughout the course of the work. Without his commitment and relentlessness, the EPS team would have not been as effective as it was and is now. Many thanks to current and previous EPS members, who have contributed to the hardware development of the module: Jaanus Kalde for developing the first revision of the MCU board, Martynas Pelakauskas for choosing and testing the batteries, Ahto Leitu for testing the regulators used onboard, and Ramon Rantsus for investigating the MPPT solutions.

I would also like to thank Mart Noorma and Silver Lätt for granting us such an amazing opportunity to build a spacecraft, Viljo Allik for providing many of the critical supplies needed for the system and sharing his expert knowledge in electronics and assembly, and all of the other instructors and members of the satellite team for their contributions and support.

Additionally, I would like to thank my parents for their support and my girlfriend for tolerating the long working hours, which went into satellite development.

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