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High Power Soft–switching IGBT DC–DC Converter

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Original scientific paper

A soft-switching topology for high power buck converter is proposed. Zero-current turn-on and zero-voltage turn-off is achieved without auxiliary switches. All active switches in the converter transmit power to the load equally. Converter control is simple despite four active switches. Converter operation is described and DC analysis is carried out. All operation modes are identified. The condition for soft-switching is derived. A full-scale 38 kW laboratory prototype with 1700 V IGBT modules is built for railway application. Switching frequency is fixed at 20 kHz. Experimental results are shown. The results confirm the analysis. A high efficiency of 97 % is achieved.

Key words: buck converter, IGBT switch, soft-switching, static characteristic

IGBT pretvarač za velike snage s mekim sklapanjem. Predstavljena je nova topologija silaznog istosmjernog pretvarača s mekim sklapanjem pogodna za velike snage. Isklapanje pri nuli napona i uklapanje pri nuli struje ostvareno je bez pomoćnih sklopki. Sve aktivne sklopke u pretvaraču prenose snagu u teret podjednako. Upravljanje pretvaračem je jednostavno unatoč većem broju aktivnih sklopki. Opisan je i analiziran rad pretvarača. Identificirani su svi načini rada. Izvedeni su uvjeti za meko sklapanje. Izrađen je laboratorijski model pretvarača u punoj snazi od 38 kW. Model je izveden s 1700 V-tnim IGBT modulima, a za primjenu na tračničkim vozilima. Sklopna frekvencija je konstantna i iznosi 20 kHz. Prikazani su rezultati mjerenja. Potvrđena je provedena analiza. Postignut je visoki stupanj korisnog djelovanja od 97 %.

Ključne riječi: istosmjerni silazni pretvarač, IGBT sklopka, meko sklapanje, statička karakteristika

1 INTRODUCTION

In high frequency and high power IGBT converters soft-switching techniques are necessary to achieve acceptable efficiency and compact design. This is especially true when high voltage IGBTs ($\geq$ 1700 V) with high switching losses are needed to build the converter. SiC components with adequate voltage and current ratings for high power and high voltage applications are yet not available.

Soft-switching techniques were first investigated in earlier bipolar switching transistor designs [1, 2] and also with IGBTs with their appearance in practical converter designs [3,4]. Numerous soft-switching DC-DC converter topologies with different approaches were reported. On one hand there are resonant, quasi-resonant and multi-resonant converters [5–7], mainly with variable switching frequency, while on the other are soft-switch PWM converters with constant switching frequency [8]. If a constant switching frequency is preferable for the application, a PWM converter is the right choice, although it is possible to operate a resonant converter with PWM at constant switching frequency [9]. Commonly, soft-switch PWM converter is derived from a classical hard-switch converter with the addition of a snubber cell consisting of an auxiliary switch and reactive components [8, 10]. The snubber cell is active during switch transitions and the auxiliary switch makes little to no contribution to the transfer of power. The auxiliary switch requires a separate driving signal that is synchronized with the signal of the main switch and usually with defined and precise timing.

Some soft-switching topologies achieve soft-switching with two or more active switches, but without auxiliary switches. The best known are phase shifted full bridge converter and its dual, current fed full bridge converter [8, 11, 12]. Soft-switching topologies without galvanic separation and without auxiliary switches are also presented. A two switch chopper topology is briefly presented in [13] and analyzed in discontinuous current conduction mode (DCCM) in [14]. This topology achieves zero-voltage (ZV) turn-off and zero-current (ZC) turn-on. Soft-switching is lost for low output power. Both switches equally transmit power to the load and therefore are equally stressed. The control circuit needs to generate only one PWM output since both switches are driven si-

multaneously. The main drawback is high voltage stress of the main diode, varying from two to three times the output voltage (for a boost topology), depending on design parameters. A two switch topology that maintains all positive benefits of hard-switching topologies i.e. simplicity and no additional voltage and current stress of the switches is described in [15]. Again, both switches equally transmit power to the load. The switches turn-on with ZC from zero to full load, but are turned-off with classical hard switching. A soft-switching bidirectional DC-DC converter with no auxiliary switches with only the addition of snubber capacitors across the switches is described in [16]. To achieve ZC turn-on and ZV turn-off of all switches, the converter needs to operate in DCCM. This is not always possible, especially in the case of wide input voltage variations, when the value of the input voltage becomes close to the value of the output voltage.

The topologies described in [13–16], similar to the topologies with auxiliary switch, have limitations such as lack of soft-switching over the whole operation range and higher switch peak current or voltage stress, but have a distinct advantage of simpler control since no additional output for the auxiliary switch is needed. With little or no change, classical PWM control can be used. Compared to the converters with one main switch, these converters can transfer more power, taking in consideration only the switch limitations, since the switches share the total current and switching stress. The thermal design is simpler and therefore such converters are advantageous for high power applications.

In this paper, a soft-switching high power converter with no auxiliary switches that overcome some of the limitations of converters in [13–16] is derived and analyzed. Experimental results measured on a laboratory prototype are presented.

2 TOPOLOGY DERIVATION

The aim was to build a converter without galvanic separation as a front-end converter in auxiliary power supply for a railway application. The main converter characteristics are:

- input voltage 400 V to 1000 V, DC
- output voltage 380 V, DC
- output power 38 kW
- switching frequency 20 kHz.

In the target application, the use of simple PWM control with existing control circuits was preferred. Also, a compact mechanical design was desired. A simple hard-switched buck converter with one 1700 V IGBT cannot be implemented. Switching losses of one IGBT at 100 A and 20 kHz would be too high for a standard package, greater than 1 kW. Another possibility is to parallel several hard-switching buck converters. That would facilitate thermal design, but with no substantial reduction of the total loses. A soft-switching converter topology was evaluated as better solution.

The soft-switching high power converter described in [16] has very good efficiency and relatively simple control, but has to be operated in DCCM. With the required input voltage variations of 1:2,5 and with close values of output and input voltage, DCCM is not practically achievable due to excessively high peak currents in worst-case conditions. A soft-switching converter which is well suited for continuous current mode (CCM) operation, is presented in [15], Fig. 1. The converter is based on buck interleaved topology. During conduction of the diode D_1, switch S_2 is switched on. Soft commutation of the current from diode D_1 to switch S_2 takes place. The rate of rise of switch current is limited by the small commutation inductances L_{k1} and L_{k2}. When switch S_2 is switched off, a hard commutation of the current to the diode D_2 takes place. In next interval, switch S_1 is switched on resulting again in soft commutation from D_2 to S_1. The switches turn-on with ZC and turn-off in hard switching. When 1700 V IGBTs are used in such a converter, hard turn-off switching loses still present major share of the losses, and therefore it is worth considering a modification of the topology that would also enable a soft turn-off.

In the topology on Fig. 2, both turn-on and turn-off are soft. The switches turn-on with ZC and turn-off with ZV [13]. As the topology in Fig. 1, this topology has a simple control and no auxiliary switches. The switches are driven simultaneously with one PWM signal. The commutating capacitor C_k limits the rate of rise of switch voltage after turn-off. During turn-on process, the commutating capacitor is discharged in the load. If the converter is to be operated in CCM, a small commutation inductor L_k is necessary to achieve soft commutation of the current from the main diode to the switches and consequently ZC turn-on of the switches. The main drawback is the high voltage stress of the switches and especially of the main diode.

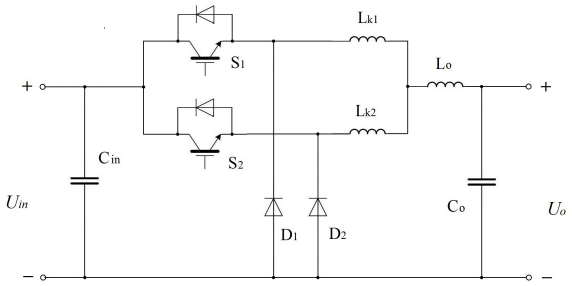


Fig. 1. Buck interleaved topology with ZC turn-on

Peak switch voltage is equal to the capacitor C_k voltage. The capacitor will be charged to the value of input voltage plus voltage corresponding to the energy stored in L_k that is transferred to C_k at the end of turn-off interval. The peak diode voltage is equal to the input voltage plus the capacitor voltage resulting in a value greater than twice the input voltage [14].

Merging the topologies from Fig. 1 and Fig. 2 gives the proposed topology, shown in Fig. 3. The switches turn-on with ZC, similar as in the interleaved converter, Fig. 1. Turn-off is ZV switched as is in the converter in Fig. 2. Despite the large number of active switches, the control is simple. The converter can be driven with basically one PWM signal that is split in two phase shifted signals with 180° phase shift and with max. duty cycle (D) of 0,5 each. One signal is applied to S_{11} and S_{12}, and the other to S_{21} and S_{22} (signal diagrams on Fig. 5). In CCM, the commutating inductor is no longer needed in series with the switch-capacitor connection as is in the topology in Fig. 2. The small commutating inductors L_{k1} and L_{k2} are placed in series with the main inductor L_o. This results in lower voltage stress of semiconductors than in the converter in Fig. 2. As it is shown in the analysis in the next section, the voltage stress of the IGBT switches is equal to the input voltage U_{in} neglecting parasitic inductances. The voltage stress of diodes D_1 and D_2 is load independent and is equal to twice the input voltage. In a real converter design, high diode voltage stress can be resolved with a combination of two series diodes. The resulting higher conduction loses are expected to be largely outweighed by the reduction in switching loses.

The large number of active switches is a drawback of this topology when applied to lower power range. For high power converters, switch multiplication is inevitable as the transferred power is rising due to series and/or parallel connections of converters or switches needed to overcame switch limitations. The proposed topology is a way to effectively parallel the switches and assure soft-switching at the same time. With regard to these considerations, the proposed converter is well suited for high power applications.

3 CONVERTER OPERATION

In order to simplify the analysis, following assumptions are made:
- the converter is fed by an ideal voltage source at the input,
- circuit operation is in steady state,
- all components are ideal, switching transition times of the IGBTs are neglected,
- output capacitance C_o is large enough to be considered as an ideal voltage source,

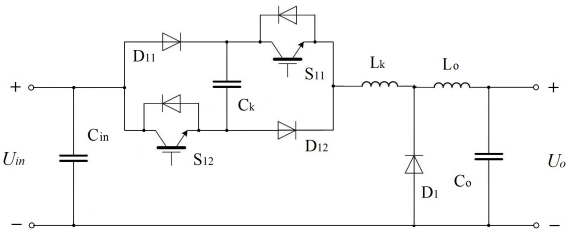


Fig. 2. Two switch buck topology with ZC turn-on and ZV turn-off

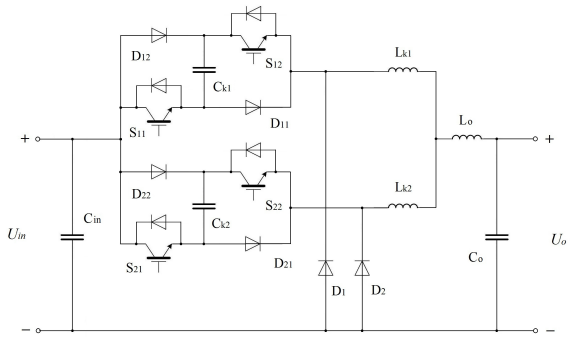


Fig. 3. Proposed buck converter soft-switching topology

- main inductance L_o is large enough to be considered as an ideal current source during switching intervals,
- parasitic inductances and capacitances are neglected, except when mentioned in the analysis.

Input and output DC voltages U_{in} and U_o are defined on Fig. 3. The following are also defined:

$$\begin{aligned} 2L_{k1} = 2L_{k2} = L_k, \\ C_{k1} = C_{k2} = C_k. \end{aligned} \tag{1}$$

3.1 Basic Operation Mode

The basic operation mode will be analyzed in detail. In basic operation mode, the converter is in CCM. The switching function is defined in Fig. 5. The duty cycle lies between D_m and 0,5. For lower values of D_m, the converter cannot achieve soft-switching. The limit for soft-switching will be derived in the next section. Fig. 4. shows equivalent circuits for the first five time intervals that constitute the first half of the switching cycle. The other five intervals form the second half of the switching cycle. These are the same as the first five intervals, except that the roles of the elements with designation 1 are changed by elements with designation 2 and vice versa. The analysis starts at the beginning of full conduction of S_{11} and S_{12}.

S_{11}, S_{12} conduction, t_0 – t_1: During conduction interval the energy is transferred to the load as it is in a sim-

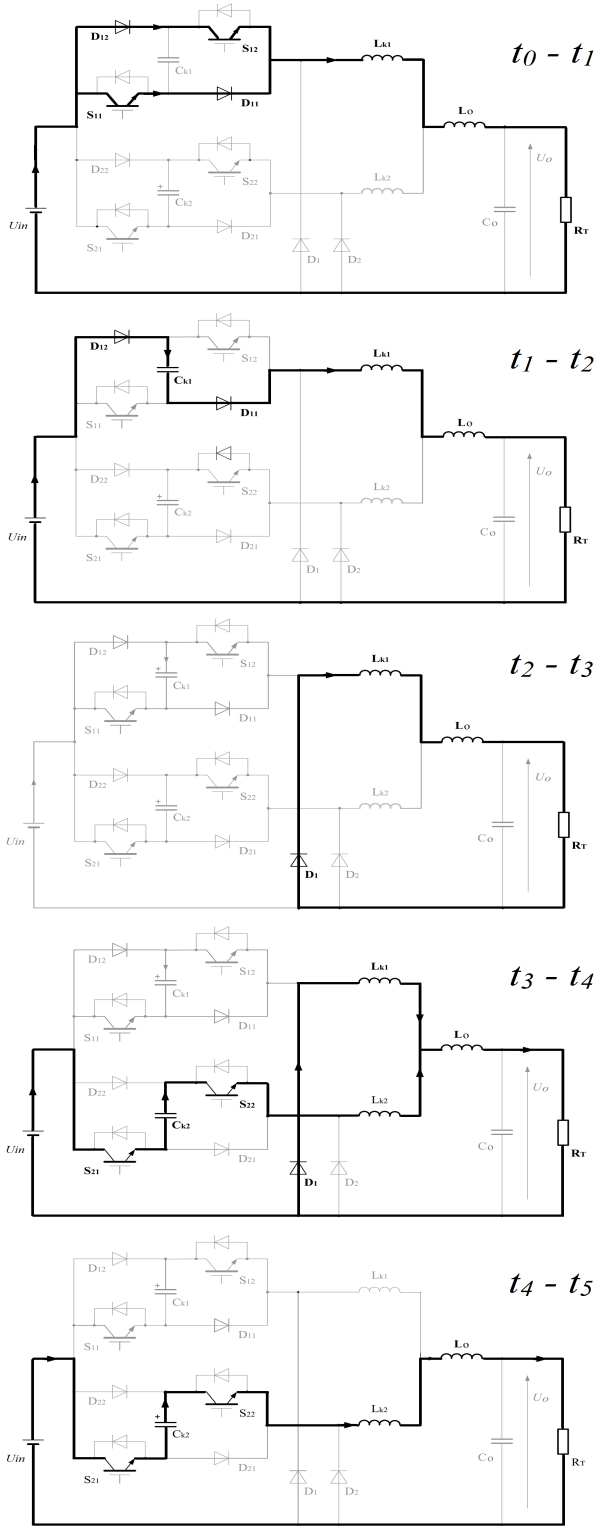


Fig. 4. Equivalent circuits for the first five time intervals. Positive current directions are indicated with arrows.

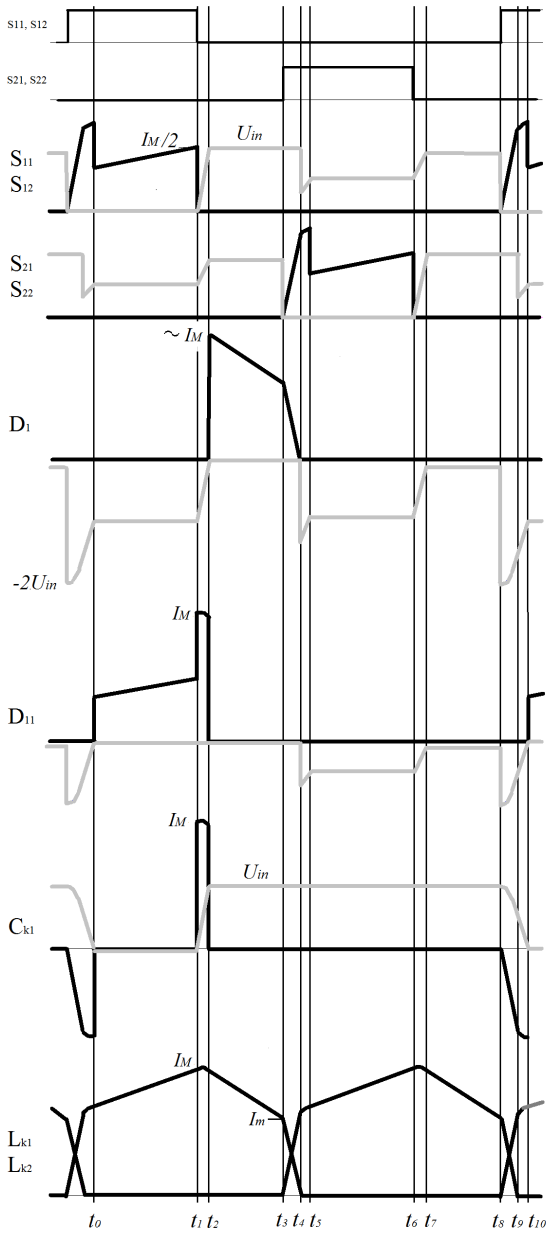


Fig. 5. Principal waveforms of the proposed converter. Black: currents, grey: voltages.

ple hard-switching buck converter. Ideally, the main inductor current i_{Lo} is equally divided between S_{11} and S_{12}. The capacitor C_{k1} is not charged and the capacitor C_{k2} is charged to the input voltage U_{in}. Blocking and reverse voltages of non-conducting semiconductors are equal or less than the input voltage U_{in}.

Turn-off interval, $t_1 - t_2$: Switches S_{11} and S_{12} are turning-off at the same instant. Each switch is switching half of the full inductor current I_M. After switch turn-

off, the inductor current i_{Lo} continues to flow through the diodes D_{12}, D_{11} and the capacitor C_{k1}. The voltage on C_{k1} and simultaneously on the IGBTs S_{11} and S_{12} rises from zero with nearly linear slope defined with capacitance C_k and value I_M. The switches turn-off with ZV. D_1 is still not conducting. The reverse voltage on D_1 drops from the value of U_{in} to zero as the voltage on C_{k1} rises from zero to U_{in}. If the leakage inductance L_σ of the loop formed by input voltage source, C_{k1}, D_{12}, D_{11} and D_1 is neglected, when D_1 voltage falls to zero, the inductor current, from the input voltage source will commutate instantly to the diode D_1 and the turn-off interval is terminated.

Now, the leakage inductance L_σ is introduced only in this point because of its influence on voltage stress of the IGBTs. When the voltage on C_{k1} has reached U_{in}, diode D_1 will start to conduct. The input voltage source, C_{k1} and L_σ form an oscillatory circuit with initial voltage of U_{in} at C_{k1} and initial current I_M through L_σ. The voltage at C_{k1} will raise above U_{in} for an amount of ΔU:

$$\Delta U = I_M \sqrt{L_\sigma / C_k}. \tag{2}$$

In this interval, the voltage on C_{k1} is the same as the switch S_{11} and S_{12} voltage. The value $U_{in} + \Delta U$ is the highest voltage stress of the IGBTs. For simplicity this is not shown in Fig. 5. The waveforms are drawn with the assumption of $L_\sigma = 0$. A good design should minimize L_σ in order to lower the voltage stress of the switches.

D_1 conduction, $t_2 - t_3$: All active switches are closed. Diode D_1 conducts as in a free-wheeling interval of a classical buck converter. C_{k1} and C_{k2} are charged to U_{in} (neglecting the effect of parasitic inductance L_σ). Blocking and reverse voltages of semiconductors are equal to or less than the input voltage U_{in}. At the end of the interval, current i_{Lo} falls to I_m.

Turn-on interval, $t_3 - t_4$: Turning-on the switches S_{21} and S_{22} at t_3 connects the series combination of input voltage source and capacitor C_{k2} to the diode D_2. This raises the reverse voltage of D_2 to the value of $2U_{in}$ which represents the highest voltage stress of the main diodes. At the same time, this will force the current to commutate from D_1 to the branch containing the input voltage source and C_{k2}. The rate of rise of the switch current at the initial instant t_3 is limited and is defined with U_{in} and L_k. The switches turn-on with ZC. Indeed, from the equivalent circuit for the turn-on interval $t_3 - t_4$ on Fig. 6, solving for switch current $i_{S21} = i_{S22} = i_{S2}$:

$$i_{S2}(t) = 2U_{in}\sqrt{\frac{C_k}{L_k}} \sin \frac{t - t_3}{\sqrt{L_k C_k}}, \tag{3}$$

$$\left(\frac{di_{S2}}{dt}\right)_{t=t_3} = \frac{2U_{in}}{L_k}. \tag{4}$$

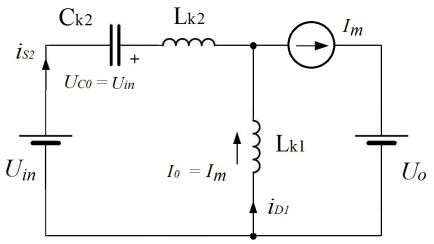


Fig. 6. Equivalent circuit for the turn-on interval $t_3 - t_4$.

At the same time C_{k2} discharges with the input current.

The turn-on interval will terminate when C_{k2} is discharged completely or diode current D_1 falls to zero, whichever occurs first. From Fig. 6 and from (3), we derive the expression for the diode current:

$$i_{D1}(t) = I_m - 2U_{in}\sqrt{\frac{C_k}{L_k}} \sin \frac{t - t_3}{\sqrt{L_k C_k}}. \tag{5}$$

From (5), if the condition

$$I_m < 2U_{in}\sqrt{\frac{C_k}{L_k}} \tag{6}$$

is satisfied, the oscillatory input current will turn-off the diode and the capacitor C_{k2} will still be not discharged completely. This condition is not valid only for a higher load current, in practice above nominal load. For that reason, the case when (6) is not satisfied will no longer be analyzed in detail.

C_{k2} full discharge, $t_4 - t_5$: Capacitor C_{k2} continues to discharge, now with approximately constant current defined by the main inductance L_o. When the capacitor is completely discharged, the diodes D_{21} and D_{22} will turn-on and another conduction interval begins, now with S_{21} and S_{22}.

3.2 Other Operation Modes

It is possible to operate the converter with duty cycle greater than 0,5. In the overlapping portion of the switching cycle, one pair of switches conducts a fraction of the full main inductor current i_{Lo}, while the remainder of the current is carried by the other pair of switches. In the rest of the switching cycle, the current is carried only by one switch pair. In the transition between these two characteristic intervals, the diodes D_1 and D_2 are also conducting. Due to space constraints these operation modes will not be analyzed, but only shown in the section with experimental results. Soft switching is preserved in this mode.

Operation in DCCM is another possible operation mode though there is little sense in designing the converter to operate in DCCM at a nominal current, since a simpler two switch topology [14] can accomplish similar operation with soft turn-on and soft turn-off in DCCM.

4 DC ANALYSIS

4.1 DC Characteristics in Basic Operation Mode

For an ideal converter without losses, the input power is equal to the output power. Therefore:

$$\frac{U_o}{U_{in}} = \frac{I_{in}}{I_o}, \tag{7}$$

where I_{in} and I_o are the average values of input and output currents respectively. Current I_{in} is equal to:

$$I_{in} = \frac{2}{T_S}\left(\int_{t_0}^{t_1} 2i_{S11}\,(t)\,dt + \int_{t_1}^{t_2} i_{D11}\,(t)\,dt + \int_{t_3}^{t_5} i_{S21}\,(t)\,dt\right) \tag{8}$$

where T_S is the switching period. Current i_{S21} in the interval $t_3 - t_4$ is given by (3) and from Fig. 5:

$$2i_{S11}\,(t) = i_{Lo}(t),\ t_0 < t < t_1, \tag{9}$$

$$i_{D11}\,(t) = I_M,\ t_1 < t < t_2, \tag{10}$$

$$i_{S21}\,(t) = I_m,\ t_4 < t < t_5. \tag{11}$$

The durations of the intervals $t_0 - t_1$, $t_1 - t_2$, $t_3 - t_4$ and $t_4 - t_5$ are calculated from equivalent circuits in Fig. 4 and 6, with regard to the conditions that govern the transitions from one interval to another:

$$T_1 = t_1 - t_0 = DT_S - T_4 - T_5, \tag{12}$$

$$T_2 = t_2 - t_1 = \frac{U_{in}C_k}{I_M}, \tag{13}$$

$$T_4 = t_4 - t_3 = \sqrt{L_kC_k}\sin^{-1}\frac{I_m}{2U_{in}\sqrt{C_k/L_k}}, \tag{14}$$

$$T_5 = t_5 - t_4 = \sqrt{\left(U_{in}\frac{C_k}{I_m}\right)^2 - \frac{1}{4}L_kC_k}. \tag{15}$$

When calculating the average input current, the following simplification can be made:

$$I_m = I_M = I_o. \tag{16}$$

This is equivalent to $L_o \gg$ and allows for simpler and more easily understandable equations.

In order to obtain normalized values for currents, voltages and time variables, we introduce:

$$U_B = U_{in}, \tag{17}$$

$$R_B = \frac{1}{2}\sqrt{\frac{L_k}{C_k}}, \tag{18}$$

$$I_B = \frac{U_B}{R_B} = 2U_{in}\sqrt{\frac{C_k}{L_k}}, \tag{19}$$

$$T_B = T_S. \tag{20}$$

Normalized values are denoted with the subscript N. The characteristic values in normalized form are:

$$U_{oN} = \frac{U_o}{U_B} = \frac{U_o}{U_{in}}, \tag{21}$$

$$I_{oN} = \frac{I_o}{I_B} = \frac{I_o}{2U_{in}}\sqrt{\frac{L_k}{C_k}}, \tag{22}$$

$$T_{kN} = \frac{T_k}{T_B} = \frac{\sqrt{L_kC_k}}{T_S}. \tag{23}$$

Finally, from (3) and (7) to (23), the expression for the DC output characteristic in basic operation mode is:

$$U_{oN} = 2D - 2T_{kN}\sin^{-1}I_{oN} + \frac{T_{kN}}{I_{oN}}\left(3 - 2\sqrt{1 - I_{oN}^2}\right) \tag{24}$$

with the condition

$$I_{oN} \le 1 \tag{25}$$

which is condition (6) in normalized form.

Figure 7 shows a plot of the normalized DC output characteristic of the proposed converter with D and T_{kN} as parameters. T_{kN} is an important design parameter that governs the main characteristics of the converter. Curves that delimit the areas of soft- and hard-switching operation are also plotted. The condition for soft-switching is explained latter.

First term in (24) is the same as for the output characteristic of the hard-switching buck converter. Factor 2 arises due to the interleaved operation of the two pair of

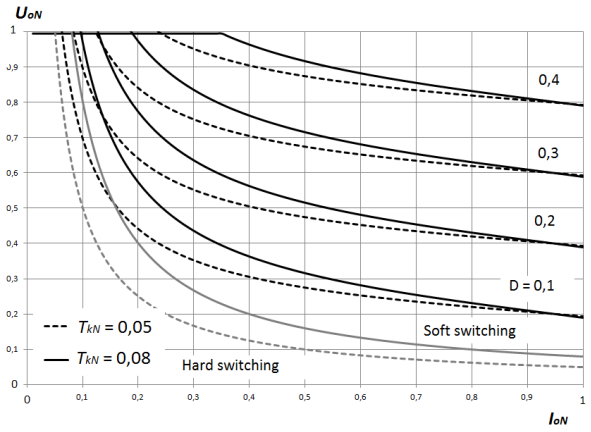


Fig. 7. DC output characteristics. The curves that delimit the hard-switching and soft-switching regions are in grey.

switches. The third term becomes dominant for low output currents and is responsible for the increase of output voltage for lower output currents. This can be explained by the fact that in each switching period, the commutation capacitors C_{k1} and C_{k2} are charged to the input voltage and discharged to the load. In each period there is a constant amount of energy delivered to the load in addition to the energy that depends on the value of the load resistor R_T. When the output current is low, this capacitor energy is dominant and raises the output voltage. By lowering the output current further, the output voltage becomes equal to the input voltage and stays at that value. The converter enters in the low output current region.

4.2 Low Output Current Region

If the value of main inductor peak current I_M is too low, the voltage value of the charged commutation capacitor C_k will not reach the input voltage in the turn-off interval after instant t_1. No commutation from the input to the main diode takes place. In this mode, the main diodes D_1 and D_2 do not conduct. For that reason, the average input and output currents are equal and therefore, input and output voltages are also equal. The energy stored in inductance $L_o + L_k/2$ at instant t_1 is insufficient to charge the commutation capacitor to U_{in}:

$$U_{in}^2 C_k \leq I_M^2 \left(L_o + L_k/2\right). \tag{26}$$

Approximation (16) does not hold anymore because the inductor current varies between 0 A and I_M. The relation for the output current as the average value of the inductor current will be used. From (26), the condition for operation in the low output current region in normalized form is:

$$I_{oN} \leq D\sqrt{\frac{2L_k}{2L_o + L_k}} + T_{kN}\left(\sqrt{2} - \frac{\pi}{2\sqrt{2}}\right). \tag{27}$$

The complete waveform analysis of this mode of operation will be no longer carried out. The converter will work in this mode only during transitions as at start-up. Soft switching is also preserved in this mode. The main experimental waveforms of this mode are shown in Section 5.

4.3 Soft-switching Condition

In order to maintain the output voltage constant, if the output current decreases, the duty cycle must also be decreased. With decreasing duty cycle, the conduction time intervals $t_0 - t_1$ and $t_5 - t_6$, Fig. 5, will disappear. With further reduction of the duty cycle, commutating capacitors do not have enough time to discharge to zero voltage and no turn-off at ZV is possible since the commutating capacitors are not discharged completely.

When the conducting intervals are exactly zero, the commutating capacitors are still charged to U_{in} and discharged to zero in one switching cycle. In this case, the energy delivered from the input voltage source to the circuit in one half of the switching period is:

$$\begin{aligned} W_{in1/2} &= U_{in}\int_{t_0}^{t_5} i_{in}\left(t\right)dt = \\ &= U_{in}\left[\int_{t_1}^{t_2} i_{Ck1}\left(t\right)dt + \int_{t_3}^{t_5} i_{Ck2}\left(t\right)dt\right] \end{aligned} \tag{28}$$

Each of the terms in brackets is equal to one commutating capacitor charge Q_{Ck} required to charge C_k to input voltage U_{in}:

$$W_{in1/2} = U_{in}\left(Q_{Ck1} + Q_{Ck2}\right) = 2U_{in}Q_{Ck} = 2U_{in}^2 C_k. \tag{29}$$

All the energy delivered to the circuit is transferred to the load. The minimal load power P_o at which soft switching is maintained is equal to twice the energy $W_{in1/2}$ multiplied by the switching frequency f_S. Therefore, the condition for soft-switching to be maintained is:

$$P_o \geq 4U_{in}^2 C_k f_S. \tag{30}$$

To represent condition (30) in Fig. 7, P_o must be in normalized form:

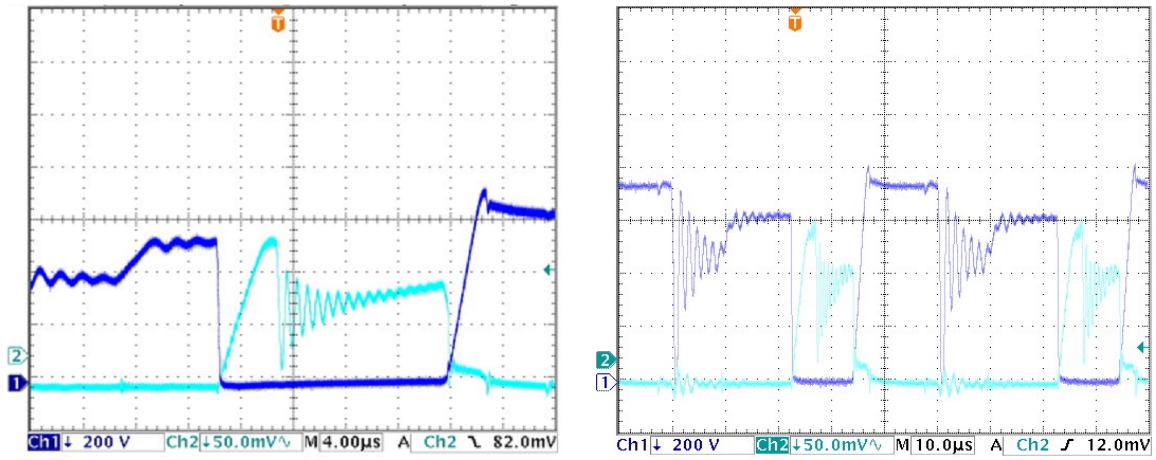
$$P_{oN} \geq \frac{4U_{in}^2 C_k f_S}{I_B U_B} = 2T_{kN}. \tag{31}$$

In Fig. 7, the limit between hard-switching and soft-switching region is represented in grey for two values of T_{kN}.

5 EXPERIMENTAL RESULTS

A full-scale 38 kW laboratory prototype was built with the characteristics listed in Section 2. Four 200 A, 1700 V IGBT modules SKM200GB176D from "SEMIKRON" were used, one module for a switch and a diode in parallel branch i.e. S_{11}, D_{12}, another module for S_{12}, D_{11} and so on. Two diodes 200 A, 1700 V in series, BYM200B170DN2 from "Infineon" were used for each main diode.

Commutation capacitors with capacitance of $C_k = 300$ nF were selected. The first criteria in the selection of capacitance was turn-off loses. Previously, a set of measurements of switching loses were made on a single switch with 1700 V IGBT [17]. Parallel commutation capacitance was varied in ZV turn-off and equivalent series commutation inductance in ZC turn-on. A capacitance of 300 nF was judged as optimal regarding loses since further increase in capacitance does not contribute greatly to the reduction of turn-off loses. Similar results were obtained in [16]. In ZC turn-on, as was measured, if the value of commutation inductance is greater than 10 μH, turn-on loses can be neglected. Experiments on the converter were made



(a) (b)

Fig. 8. IGBT current and voltage waveforms. a) turn-on, conduction and turn-off intervals showing ZC turn-on and ZV turn-off, U_{in} = 600 V, I_o = 80 A. Ch2: (light) 25 A/div. b) two switching periods with U_{in} = 750 V, I_o = 90 A. Ch2 (light): 25 A/div.

with two values of inductance L_k of 25 µH and 50 µH in order to evaluate the influence of the design parameter T_{kN}, (23).

Figures 8 and 9 show oscillograms of voltage and current of one IGBT switch and of the series combination of two diodes that stands for one main diode. The main differences that can be seen in the waveforms in comparison to the idealized waveforms in Fig. 5 are the high-frequency oscillations in IGBT current during conduction interval and high-frequency oscillations in voltage waveforms caused by the main diode recovery. The current in the conduction interval oscillates because of the parasitic *LC* combination in the loop of the commutation capacitor formed by two switches and two diodes.

In the analysis, main diode recovery current is neglected. In the measured waveforms, the influence of diode recovery is clearly visible. When the diode recovery current is cut-off, it will continue to flow for a short time, driven by the commutation inductance, through the commutation capacitor and antiparallel IGBT diodes in the input voltage source. This is the cause of a reverse voltage of -2U_{in} on the main diode at the instant of diode turn-off that is not present on the idealized waveforms with neglected diode recovery. The oscillations caused by the reverse current cut-off are also visible in the IGBT voltage waveforms.

Figures 10 and 11 illustrate operation modes with $D > 0{,}5$ and operation in low output current region with $U_{in} = U_o$. It can be seen that soft switching is preserved in both cases.

The static DC output characteristic is measured and the results shown in Fig. 12. are compared to the characteristics given by (24). In the region of nominal output current, the measured and computed values do not differ significantly, though low output currents show a greater difference. The main reason is that for low currents the AC component of the main inductor current is not negligible as stated in (16). Despite the difference, the measured characteristics show the increase and finally the limitation of output voltage to U_{in} in the low output current region.

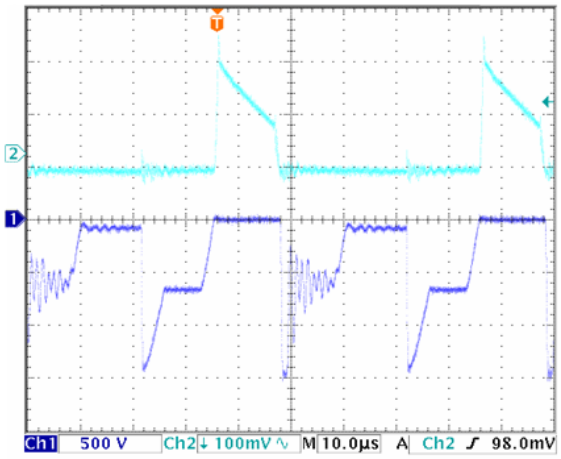


Fig. 9. Main diode D_1 (consisting of two series diodes) current and voltage waveforms. Two switching periods are shown for U_{in} = 750 V, I_o = 80 A. Ch2 (upper trace): 50 A/div.

Efficiency was measured with standard class DC instruments for input and output voltages and currents. The relative error of current measurements was 0,5% and the

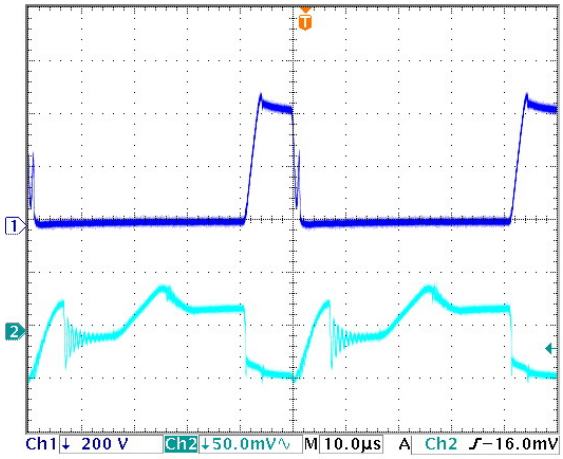


Fig. 10. IGBT current and voltage waveforms, D = 0,8. The converter operates with U_{in} = 400 V, U_o = 370 V and I_o = 95 A. Ch2 (lower trace): 25 A/div.

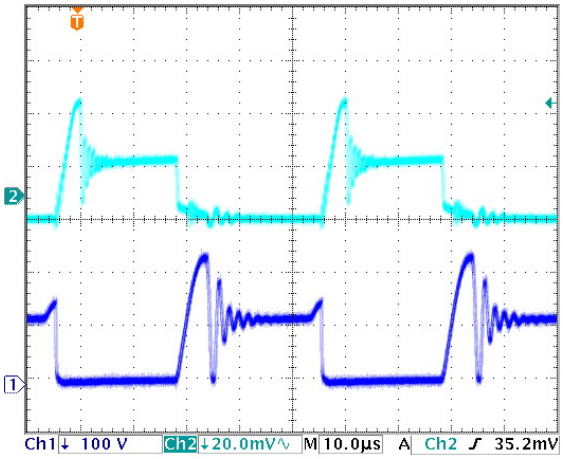


Fig. 11. IGBT current and voltage waveforms in the low current region. U_{in} = U_o = 600 V, I_o = 21 A. Ch2 (upper trace): 10 A/div.

relative error of voltage measurements was 0,1%. The obtained results are shown in Fig. 13. Dispersion of the results are evident. For better evaluation of semiconductor loses, the temperatures of the heat sink in nominal converter operation were measured. Nominal operation is: U_{in}= 600 V, U_o= 380 V and I_o= 100 A. After that, semiconductors were loaded with DC currents adjusted in such a way that the temperatures were the same as obtained in the nominal converter operation. Semiconductor DC loses are easily measured. A total of 1180 W converter semiconductor loses were measured for nominal operation. With added inductor loses of 100 W, total loses were 1280 W, which confirms high efficiency of nearly 97%.

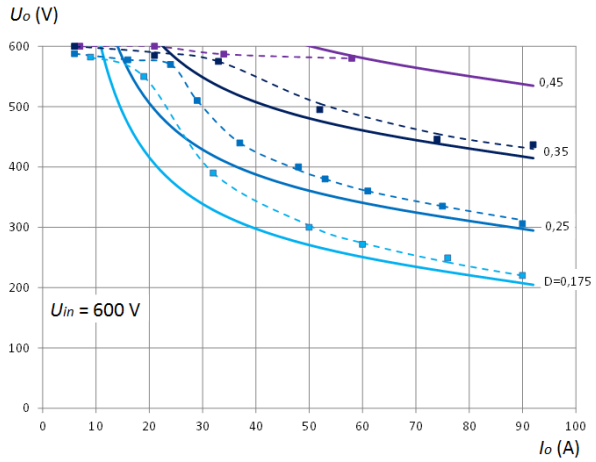


Fig. 12. Measured static DC output characteristics.

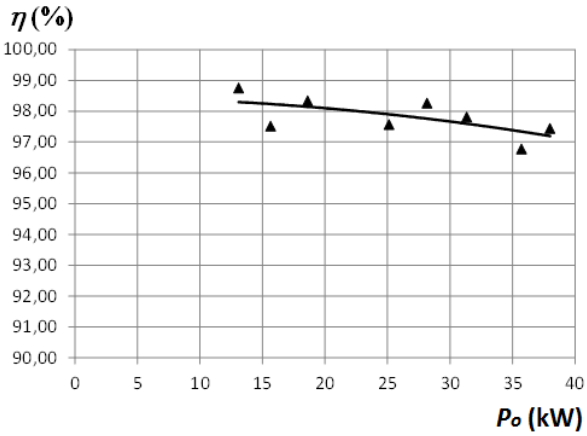


Fig. 13. Measured efficiency.

6 CONCLUSION

The proposed converter, despite four active switches has a simple control based on one PWM signal. All the switches transfer power to the load equally. This makes the converter suitable for high power applications. Switch loses are equally divided between switches facilitating the thermal design. Switches turn-on with ZC and turn-off with ZV in a wide load range. Analytical results are confirmed by experiment. High efficiency of 97% can be reached with 1700 V IGBTs at 20 kHz switching frequency and at output power of 38 kW.

REFERENCES

[1] E. T. Calkin, B. H. Hamilton, F. C. LaPorta, "Switching regulator with network to reduce turnon power losses in the switching transistor", U.S. patent 3 745 444, July 1973.

[2] E. Buchanan, E.J. Miller, "Resonant Switching Power Conversion Technique", *PESC '75 Conf. rec.*, Culver City, USA, pp. 188-193, June 1975.

[3] K. Heumann, C. Keller, R. Sommer, "Behaviour of IGBT modules in zero-voltage-switch applications", *PESC '92 Conf. rec.*, vol. 1, Toledo, Spain, pp. 19 - 25, 1992.

[4] K. Wang, F. C. Lee, G. Hua, D. Borojevic, "A comparative study of switching losses of IGBTs under hard-switching, zero-voltage-switching and zero-current-switching", *PESC '94 Conf. rec.*, vol. 2, Taipei, Taiwan, pp. 1196 - 1204, June 1994.

[5] R. L. Steigerwald, "High-Frequency Resonant Transistor DC-DC Converters", *IEEE Transactions on Industrial Electronics*, vol. IE-31, no. 2, pp. 181-191, May 1984.

[6] F. C. Lee, "High-Frequency Quasi-Resonant Converter Technologies", *Proceedings of the IEEE*, vol. 26, no. 4, pp. 377-390, April 1988.

[7] W. A. Tabisz, F. C. Lee, "Zero-voltage-switching multi-resonant technique – a novel approach to improve performance of high- frequency quasi-resonant converters", *PESC '88 Conf. rec.*, vol. 1, Kyoto, Japan, pp. 9-17, 1988.

[8] G. Hua, *Soft-Switching Techniques for Pulse-Width-Modulated Converters*, Ph.D. Dissertation, Virginia Polytechnic Institute and State University, Blacksburg, Virginia, April 1994.

[9] J.-P. Vandelac, P. D. Ziogas, "A DC to DC PWM Series Resonant Converter Operated at Resonant Frequency", *IEEE Transactions on Industrial Electronics*, vol. 35, no. 3, pp. 451-460, August 1988.

[10] T. W. Ching, K. U. Chan, "Review of soft-switching techniques for high-frequency switched-mode power converters", *VPPC '08. IEEE Conf. rec.*, Macau, China, pp. 1-6, Sept. 2008.

[11] R. L. Steigerwald, K. D. T. Ngo, "Full bridge lossless switching converter", U.S. Patent 4 864 479, Sept. 1989.

[12] C. Iannello, S. Luo, I. Batarseh, "Full bridge ZCS PWM converter for high-voltage high-power applications", *IEEE Transactions on Aerospace and Electronic Systems*, vol. 38 , no. 2, pp. 515 - 526, April 2002.

[13] Y. Tsuruta, A. Kawamura, "A High Efficiency and High Power Chopper Circuit QRAS using Soft Switching under Test Evaluation at 8kW", *Journal of Power Electronics*, vol. 6, no. 1, pp. 1-7, Jan. 2006.

[14] T. Mishima, Y. Takeuchi, M. Nakaoka, "A New High Step-Up Voltage Ratio Soft Switching PWM Boost DC–DC Power Converter with Edge Resonant Switched Capacitor Modular", *EPE 2011 Conf. rec.*, Birmingham, U.K., pp. 1-10, Aug./Sept. 2011.

[15] M. Ilić, D. Maksimović, "Interleaved Zero-Current-Transition Buck Converter", *IEEE Transactions on Industy Applications*, vol. 43, no. 6, pp. 1619-1627, Nov./Dec. 2007.

[16] J. Zhang, J.-S. Lai, R.-Y. Kim, W. Yu, "High-Power Density Design of a Soft-Switching High-Power Bidirectional dc-dc Converter", *IEEE Transactions on Power Electronics*, vol. 22, no. 4, pp. 1145-1153, July 2007.

[17] N. Čobanov, *Mass reduction of auxiliary power supply converters for railway applications by soft-switching* (in Croatian), Ph.D. Dissertation, Faculty of electrical engineering and computing, University of Zagreb, Croatia, July 2012.

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