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理學碩士 學位論文

n-ZnO/p-Si 이종접합구조 다이오드 특성 연구

n-ZnO/p-Si Diode characteristics of Hetero junction structure

指導教授 金 泓 承



2010年 2月

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本 論文을 李鍾勳의 理學碩士 學位論文으로 認准함.

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2010年 12月 28日

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Contents

	page
List of Figures····	i
List of Tables	ix
Abstract	· vi
Chapter 1. Introduction·····	• 1
Reference·····	. 3
Chapter 2. Literature Survey	
2.1 Introduction to ZnO material	
2.1.1 Physical properties of ZnO······	. 5
2.1.2 Application of ZnO······	8
Reference	9
2.2 Introduction to Silicon material	
2.2.1 Physical properties of Si·····	…10
Reference·····	13
2.3 Heterojunction of n-ZnO/p-Si	
2.3.1 Concept·····	…14
2.3.2 diode current-voltage characteristics·····	17
Reference·····	24
Chapter 3. Thermal-annealing Effect on the Diode Characteristics	of
n-ZnO/p-Si (111)	

3.1 Experimental Details······26
3.2 Results and Discussion ————————————————————————————————————
3.3 Conclusion
Reference 39
Chapter 4. Dependence of the Diode Characteristics of n-ZnO/p-Si (111) or
the Si Substrate Doping
4.1 Experimental Details······42
4.2 Results and Discussion 43
4.3 Conclusion
Reference54
Chapter 5. Effect of Indium doped-ZnO/p-Si(111) on Diode Characteristics
5.1 Experimental Details······57
5.2 Results and Discussion 60
5.3 Conclusion·····70
Reference·····71
Chapter 6. Summary and Conclusions······73
Acknowledgement 75
Curriculum Vitae······77
Publication List 78
Appendix86

List of Figures

Chapter 2. Literature Survey

- Figure 2.1 Hexagonal wurtzite structure of ZnO.
- **Figure 2.2** The bandgap energy and the lattice constant of II-VI and III-V compound semiconductor.
- Figure 2.3 Application of ZnO material.
- Figure 2.4 Resistivity vs. impurity concentration in Si and GaAs at 300 K.
- **Figure 2.5** The band diagram of n-ZnO/p-Si (111) heterostructure diode and concept for lighting mechanism.
- **Figure 2.6** The schematic of (a) n-ZnO atoms and (b) p-Si atoms of <111> direction from the top-view.
- Figure 2.7 Current-voltage characteristics of a practical Si diode.
- **Figure 2.8** Current-voltage characteristics of GaAS diode with R_p (parasitic resistance) and R_s (series resistance).
- Chapter 3. Thermal-annealing Effect on the Diode Characteristics of n-ZnO/p-Si (111)
- **Figure 3.1** (a) Schematic diagram of the fabrication process for a n-ZnO/p-Si heterojunction diode and (b) the patterns of the metal mask.
- **Figure 3.2** XRD spectra of ZnO films with different annealing temperatures in a N₂ ambient (*:Diffraction peaks of the Si substrate).
- **Figure 3.3** FWHM of the ZnO (002) peak of the as-grown ZnO and post thermally annealed ZnO.

Figure 3.4 AFM surface images of the ZnO films with different annealing temperatures in a N_2 ambient: (a)as-grown ZnO and ZnO annealed at (b) 600 °C, (c) 700 °C, and (d) 800 °C.

Figure 3.5 Variations of the grain size and the surface roughness of ZnO films annealed in a N_2 ambient at different annealing temperatures from the AFM results. **Figure 3.6** Current-voltage characteristics of the n-ZnO/p-Si heterojunction diodes at room temperature. The inset shows a schematic diagram of the heterojunction diode.

Figure 3.7 Semi-log plots of the current-voltage characteristics of n-ZnO/p-Si(111) heterojunction diodes and the diode ideality fact (n) of ZnO annealed at 700 °C. The values show the forward current (I_F) and reverse current (I_R) ratio at \pm 5 V.

Figure 3.8 I/(dI/dV) – current characteristics of the n–ZnO/p–Si (111) heterojunction diodes and the series resistances at different annealing temperatures.

Figure 3.9 (a) Electroluminescence image of a n-ZnO/p-Si heterojunction diode at forward bias (13 \sim 15 V). (b) The inset shows the patterns of a n-ZnO/p-Si heterojunction diode.

Chapter 4. Dependence of the Diode Characteristics of n-ZnO/p-Si (111) on the Si Substrate Doping

Figure 4.1 Device annealed in N_2 exhibits ohmic I-V behavior with Ti/Au on the p and p^+-Si substrates.

Figure 4.2 I-V characteristics of n-ZnO/p and p^+-Si heterojunction diodes at room temperature subjected to post-thermal annealing in (a) N_2 and (b) air. The inset shows a semi-log plot of the I-V characteristics of n-ZnO/p and p^+-Si heterojunction diodes. The values show the forward current (I_F) and reverse

current (I_R) ratios at ± 4 V.

Figure 4.3 Log(I) - log(V) plots of current-voltage characteristics of n-ZnO/p and p⁺-Si heterojunction diodes subjected to post-thermal annealing in (a) N₂ and (b) air. Also shown are I/(dI/dV) plots of n-ZnO/p and p⁺-Si heterojunction diodes subjected to post-thermal annealing in (c) N₂ and (d) air, together with the series resistances.

Figure 4.4 (a) Electroluminescence image of an n-ZnO/p⁺-Si heterojunction diode at forward bias (over10 V). (b) Inset shows the patterns of an n-ZnO/p⁺-Si heterojunction diode.

Chapter 5. Effect of Indium doped-ZnO/p-Si(111) on Diode Characteristics

Figure 5.1 (a) The n-ZnO/p-Si (111) diode pattern image viewing top, measuring optical microscope and (b) schematic diagram of n-ZnO/p-Si diode, viewing cross section.

Figure 5.2 XRD θ -2 θ scan of un-doped ZnO film and In (5 at.%)-doped ZnO film.

Figure 5.3 I-V characteristics of un-doped ZnO/p-Si diode and In (0.6~10 at.%)-doped ZnO/p-Si diode with turn-onvoltage, The insets show the ln(I)-V plots of I-V curves with the ideality factors.

Figure 5.4 The Semi-log plots of the I-V curves. The insert values are on-off ratio at ± 5 V.

Figure 5.5 Relationship between the indium doping concentration and the (a) turn-on voltage, (b) series resistance, (c) reverse current at -5 V.

Figure 5.6 The cross-sectional TEM image of the (a) un-doped ZnO and (b) In (5 at. %) / p-Si(111).

List of Tables

Chapter 2. Literature Survey

Table 2.1 Properties of ZnO.

Table 2.2 Properties of Si at 300 K.

Table 2.3 The lattice mismatch and the lattice constant between the n-ZnO and the other substrate materials.

Table 2.4 The summarized notation of the diode equation.

Table 2.5 The diode ideality factor at the recombination type.

Chapter 4. Dependence of the Diode Characteristics of n-ZnO/p-Si (111) on the Si Substrate Dopingg

Table 4.1 Carrier concentration, mobility, and resistivity of ZnO annealed in N_2 and air ambients, and p and p⁺-silicon substrates having different resistivities.

Chapter 5. Effect of Indium doped-ZnO/p-Si(111) on Diode Characteristics

Table 5.1 Carrier concentration, mobility and resistivity of un-doped ZnO, In (0.6, 1, 5, and 10 at. %)-doped ZnO and p-Sisubstrate.

Table 5.2 Summary of the diode characteristics with saturation current density, turn-on voltage, series resistance, ideality factor, forward current/reverse current ratio at ± 5 V and barrier height.

Chapter 6. Summary and Conclusions

Table 6.1 Summary of the diode characteristics with saturation current density,

turn-on voltage, series resistance, ideality factor, forward current/reverse current ratio at \pm 5 V and barrier height.



n-ZnO/p-Si 이종접합구조 다이오드 특성 연구

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Abstract

차세대 광원으로 주목받는 LED (light-emitting diode)에 대한 관심과 수요는 꾸준히 증가하였고, 현재 많은 연구가 활발히 진행되고 있다. 이러한 가장 큰 이유는 기존의 광원보다 에너지 절감 효과가 크며, 수명이 우수한 장점이 있기 때문이다. 기존의 청색 LED 기술은 GaN를 기반으로 하고 있다. 하지만 GaN를 기반으로 하는 LED는 특정국가에 원천기술이 묶여 있으며, 이를 해결하기 위해 차세대 물질로의 대체를 하기 위한 노력이 시도되고 있다. 이러한 GaN를 대체하기 위한 물질로는 SiC, ZnSe, ZnS, ZnO 등의 화합물 반도체가 대표적이다. 그 중 가장 유력한 대체 물질로 주목받는 ZnO는 2-6 족 화합물 반도체로서 3.27 eV의 광대역 밴드갭을 가지는 직접 천이형 반도체이며, 상온에서 60 meV의 큰 엑시톤 결합 에너지를 가진다. 이런 큰 엑시톤 특성 때문에 ZnO는 단파장 및 방출 다이오드(light emitting diode)와 엑시톤 기반의 레이저 다이오드(laser diodes)의 적용에 큰 주목을 받고 있다.

ZnO 박막을 제조하려는 방법에는 스퍼터링, 화학기상 증착 (CVD), 분자 빔에피택시 (MBE), 원자층 증착법 (ALD), 펄스 레이저 증착 (PLD) 등 매우 다양

한 방법들이 사용되고 있다. 증착된 ZnO 박막은 산소 결핍형 산화물이기 때문에 구조적, 광학적 특성이 좋지 못하다. 그래서 아일랜드 크기를 증가시키고 격자 응력을 완화해 박막의 결정성과 발광 특성을 향상시키기 위해 성장 후 후속 열처리 과정이 필요로 하다. 증착된 ZnO 박막은 산소의 공공과 Zn의 침입때문에 쉽게 n형 반도체 특성이 있는 것으로 알려졌다. 반면 ZnO는 p형 형성을 위한 도핑과정에서 억셉터 불순물의 낮은 용해도와 높은 자체 보상 효과에의해 특성이 좋고 재현성 있는 p형 ZnO 구현이 어려워 p-GaN, SiC, p-다이아몬드 기판을 이용한 헤테로 접합을 많이 시도하고 있다. 하지만 위 기판들은 고가격이라는 문제가 있다. 이를 해결하기 위해 본 연구에서는 가격이 저렴한 p-Si(111)기판을 이용하여 이종 접합을 시도하였다. 특히 Si 기판은 ZnO와 열팽창 계수가 비슷하고, 기존의 실리콘 기반의 소자 제작 기술을 그대로 활용할수 있는 장점을 가지고 있다. 다만 Si(111)기판에서 (111) 면간 거리가 a=0.384 nm로서 ZnO 결정의 a=0.325 nm 와 격자 불일치가 15.4 %의 다소 큰 차이를 보인다.

Si 기판을 이용하여 이종 접합 다이오드 제작 시 p 타입의 Si(111) 기판의 구조적 안정성을 확보하고 ZnO 박막의 전자농도 및 전기적 특성의 조절이 쉬워야 하며 이를 통해 간접 천이 밴드갭을 가진 Si 이 아닌 직접 천이 밴드갭을 가진 ZnO 쪽에 Si 쪽의 홀이 유입되어 재결합을 통한 발광이 일어나도록 하여야 한다. 이러한 재결합 과정이 일어나려면 캐리어 농도 차이에 의한 캐리어흐름을 고려할 필요가 있다. 특히, 광대역 반도체 물질을 이용한 p-n 접합 소자에서 캐리어 농도가 높은 쪽이 낮은 쪽으로 공간전하 영역을 넘어 이동하는 단일 캐리어에 의한 주된 전류 특성이 나타난다고 보고되고 있다.

정공 농도를 변화시키기 위해서 기판의 비저항이 다른 두 개의 p형 Si(111) 기판을 사용하여 소자를 제작하였다. 전자의 농도 변화를 시키려는 방법에는 도핑에 의한 방법과 후속 열처리를 통한 캐리어 조절 방법 2가지 방법

이 있다. 전자는 ZnO 박막에 In을 0.6 ~ 10 at. %를 도핑 하면 Zn2+자리에 In3+를 치환이 되어 자유 전자를 증가시켜 캐리어 농도를 변화시킬 수 있다. 후자의 방법으로는 N2 분위기와 air 분위기에서 열처리 하여 ZnO 박막 내의 캐리어 농도를 변화 시키는 방법을 사용하였다. ZnO 박막의 구조적 특성은 XRD 측정과 AFM 측정을 통하여 분석하였으며, 캐리어 농도는 Hall 측정을 통해 조사하였다. 마지막으로 포토리소그래픽 공정과 lift-off 방법을 이용하여 다이오드 소자를 제작하고 I-V 측정을 하였다.

ZnO의 캐리어 농도변화는 I-V 특성에 영향을 주는 것을 확인할 수 있었으며, 또한 구조적 특성 때문에 I-V 결과에 영향을 미치는 것을 확인하였다. 문턱 전압은 1.8 ~ 4.6 V까지 다양한 값을 가졌으며 가장 낮은 on-off 비 (± 5 V)는 1.0 x 106 인 것을 확인을 하였다. 높은 전압일 때 가장 낮은 시리즈 저항 값은 37 Ω인 것을 확인하였다. 높은 전압일 때 단일 캐리어에 의한 주된전류 특성 흐름은 p+-Si 기판(~ 1019 /cm3)과 대기 분위기에서 열 처리된 ZnO 박막(~ 1016 /cm3)의 이종접합 다이오드의 I-V 결과에서 명확하게 나타난 것을 확인하였다. 제작된 모든 소자는 순방향 전압 인가 시 황색 발광을 하는 것을 확인하였다.

Chapter 1. Introduction

In recent years, Zinc oxide (ZnO) has been regarded as a promising material for ultraviolet light-emitting device applications because of its wide direct band-gap of 3.27 eV and large exciton binding energy of 60 meV (cf. 25 meV for GaN) [1-3]. In addition, ZnO is a candidate material for next high performance devices such as blue/UV optoelectronics, light-emitting diodes, lasers, detectors, window material for flat panel displays, solar cell, and gas sensors [4-7]. In addition, the applications of the ZnO film can be used from insulator and metal to change the carrier concentration. A study of the ZnO about the carrier concentration is to obtain high carrier concentration (over 10^{20} /cm³) for substitution of indium tin oxide (ITO) [8-9]. The high carrier concentration of n-type ZnO can be obtained as high doping in the ZnO with group III donor impurities such as Ga, Al and In [10-12]. Thin films of ZnO have been grown by using a variety of deposition techniques, such as sol-gel process, spray pyrolysis, chemical vapor deposition (CVD), pulsed laser deposition, and sputtering [13-16]. High-quality ZnO films are essential to fabricate the ZnO-based devices. Therefore, several growth techniques have been employed to improve the film quality. Among them, post-thermal annealing can modify the grain size, the lattice strain, and the extent of orientation in the films, leading to enhanced luminescent properties of ZnO and enhanced [17, 18].

Usually, un-doped ZnO shows n-type conductivity because of deviations from stoichiometry due to the presence or intrinsic defects such as oxygen vacancies (\underline{V}_o) and zinc interstitials (Zn_i) [19]. Several experiments have shown that p-type ZnO is achievable with V elements, such as P (phosphorus) and N (nitrogen), or

with post thermally annealed ZnO film in an NH₃ ambient [20–22]. However, to realize p-type ZnO for applications is difficult due to the low solubility of the dopant and the highly self-compensating process upon doping [19]. For this reason, some p-type materials, such as p-GaN, p-diamond, and 6H-SiC, were reported to fabricate heterojunction diodes with n-ZnO [23–25], but, those substrates have the problem of high cost. Thus, we used p-type Si(111) substrate as a large area substrate with low cost. Moreover, the silicon substrate has thermal expansion coefficient similar to that of ZnO [26], and the Si(111) substrate (lattice mismatch ~15.4%) has a better lattice mismatch compared to the Al₂O₃ (lattice mismatch ~18%) substrate on which ZnO was generally deposited.

In this paper, we focused on to investigate heterojunction diode characteristic of n–ZnO/p–Si (111) structure. A review of the literature is presented in Chapter 2 that describes the general properties of Si materials, concept of hetrojucntion structure of n–ZnO/p–Si, the characteristics of p–n junction diode, the deposition mechanisms using the rf–sputter and PLD systems, and the measurement systems. The optimum temperature of post thermal annealing condition and the structural properties of ZnO film via using a rf–sputter system are described in Chapter 3. The n–ZnO/p–Si heterojunction diode characteristics depend on the post thermal annealing and the different p–type silicon resistivity were reported in the Chapter 4. Also, the effects of indium mole fraction on the ZnO film/p–Si heterojunction structure diode is investigated using pulsed laser deposition in Chapter 5. Finally, the summary and the conclusion in given in Chapter 6.

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Chapter 2. Literature Survey

2.1 Introduction to ZnO material

2.1.1 Physical properties of ZnO

Zno has a hexagonal wurtzite structure with a = 3.25 A and c= 5.12A [1, 2]. The chemical bonds in ZnO with a wurtzite structure are largely ionic in nature because of a significant difference in the electron negativity between Zn (1.65) and 0 (3.44) [3]. The ionic radius of the Zn²⁺ ion is 0.60 angstroms and that of the oxygen ion is 1.40 angstroms. The ratio of radii for the cation and anion is thus rjr. = 0.60/1.40 = 0.428. The Zn²⁺ ions occupy tetrahedral holes. The oxygen ions form a hexagonal closest-packed structure (atoms or ions are stacked ABABAB).

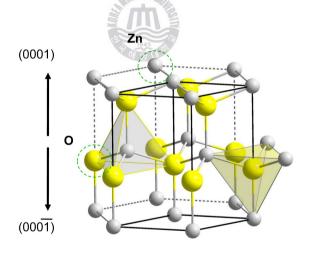


Figure 2.1 Hexagonal wurtzite structure of ZnO.

Wurtzite (Hexagonal)

Table 1 shows properties of ZnO. It should be noted that ZnO have wide bandgap (3.37 eV) and high exciton binding energy (60 meV verse 26 meV for GaN). It is able to fabricate more effective LED and LD device, there still exists uncertainty in some of these values. For example, there have few reports of p-type ZnO and therefore the hole mobility and effective mass are still in debate. ZnO can also be chemically etched which is important for device fabrication [4].

Table 2.1 Properties of ZnO [2].

D	77.1
Property	Value
Lattice parameters at 300 K	
a ₀	0.32495 nm
c_{0}	0.52069 nm
a o/ c o	1.602 (ideal hexagonal structutre shows 1.633)
u	0.345
Density	5.606 g/cm^3
Stable phase at 300 K	Wurtzite
Melting point	1975 °C
Boiling point	2360 °C
Thermal conductivity	0.6, 1-1.2
I : (/°C)	$a_0: 6.5 \times 10^{-6}$
Linear expansion coefficient (/°C)	$c_0: 3.0 \times 10^{-6}$
Static dielectric constant	8.656
Refractive index	2.008, 2.029
Energy gap	3.37 eV, direct
Intrinsic carrier concentration	$<10^6 \text{cm}^{-3}$ (max n-type doping $> 10^{20} \text{cm}^{-3}$ electrons; max p-type doping $< 10^{17} \text{cm}^{-3}$ holes)
Exciton binding energy	60 meV
Electron effective mass	0.24
	0.24
Electron Hall mobility at 300 K	$200 \text{ cm}^2/\text{Vs}$
for low n-type conductivity	
Hole effective mass	0.59
Hole Hall mobility at 300 K	$5 - 50 \text{ cm}^2/\text{Vs}$
for low p-type conductivity	

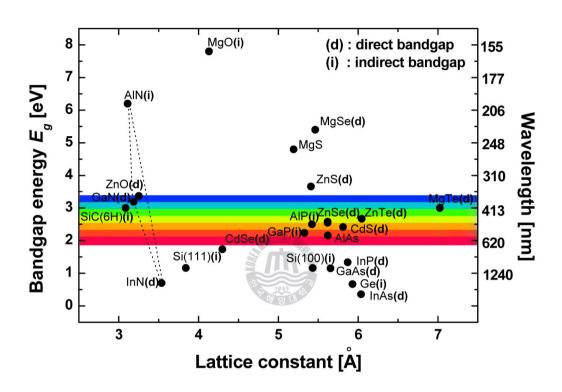


Figure 2.2 The bandgap energy and the lattice constant of II-VI and III-V compound semiconductor.

2.1.2 Application of ZnO

Many researchers have extensively studied Wurtzite structured ZnO thin films because ZnO films have potential in many applications, such as transparent conducting oxide electrodes, thin-film gas sensors, solar cells, luminescence materials, and hetero-junction laser diodes [5–7]

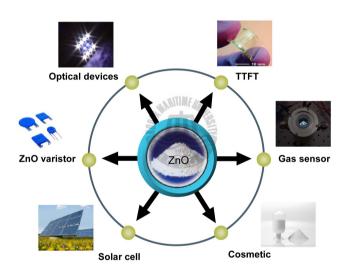


Figure 2.3 Application of ZnO material

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2.2 Introduction to Silicon material

2.2.1 Physical properties of Si

Silicon has many industrial uses [1–3]. It is the principal component of most semiconductor devices, most importantly integrated circuits or microchips. Silicon is widely used in semiconductors because its native oxide is easily grown in a furnace and forms a better semiconductor – dielectric interface than any other material [4]. Table 2.2 show the properties of Si material. The crystal structure is diamond structure and the band gap is 1.12 eV. As indirect band structure and narrow band gap energy, it is can not applied on the visible light device. But it has many advantage such as existing the large area substrate and low cost, good crystal quality. If it could be applied by using silicon material on optical device, the optical device has vert low cost. Figure 2.4 is relation of resistivity–impurity concentration in Si. The carrier concentration of silicon material is changing by dopant concentration [5].

Table 2.2 Properties of Si at 300 K [5].

Property	Value
Atoms or molecules /cm ³	5.0×10^{22}
Atomic or molecular weight	28.08
Density, g/cm ³	2.33
Breakdown field, V/cm	$\sim 3 \times 10^5$
Crystal structure	Diamond
Dielectric constant	11.8
Effective density of states Conduction	
band N_c cm ⁻³	2.8×10^{19}
Valence band $N_{\rm v}$, cm ⁻³	1.02×10^{19}
Electron affinity χ, V	4.01
Energy gap, eV	1.12
Intrinsic carrier	1.5×10^{10}
concentration n _i , cm ⁻³	1,3 X 10
Lattice constant, Å	5.431
Effective mass:	5
Electron, cm ² /V·s	$m_e = 0.33m, m_e^* = 0.26m$
Holes, cm ² /V·s	$m_h = 0.56m, m_h^* = 0.38m$
Intrinsic mobility:	
Electron, cm ² /V·s	1350
Holes, cm ² /V·s	480
Temperature coefficient of expansion	2.5×10^{-6}
Thermal conductivity, W/cm·°C	1.5

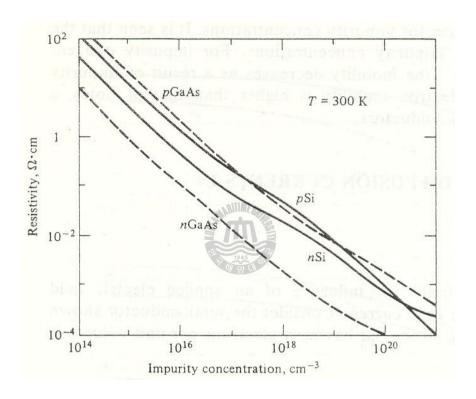


Figure 2.4 Resistivity vs. impurity concentration in Si and GaAs at 300 K [5].

Reference

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2.3 Heterojunction of n-ZnO/p-Si

2.3.1 Concept

Figure 2.5 shows a band diagram of n-ZnO/p-Si (111) heterostructure. To achieve efficient emission in a light-emitting device based on an n-ZnO/p-Si heterojunction diode, the hole-electron pairs have to recombine in the ZnO region of the wide band gap due to the carrier concentration difference in forward bias. The *pn*-junction diode using the wild band gap material reported dominant single carrier injection characteristics with limited space charge region at high voltage [1-3]. We considered that the concentration of electrons in the n-type ZnO film or of holes in the p-type Si substrate can be varied by the method proposed below. A ZnO film annealed in N₂ ambient was found to have higher carrier concentrations and a lower resistivity than a ZnO film annealed in air ambient [4]. Other method is cationic doping of group III (B, Al, In, Ga) elements in the ZnO film for changed electron concentration. When the hole concentration was changed, differently doped Si substrates could be used for the p-type Si substrate.

Figure 2.6 shows a schematic of (a) n–ZnO atoms and (b) p–Si atoms of <111> direction from the top–view. A lattice array of si (100) direction at top–view differ with hexagonal ZnO structure (0001) direction. It has large lattice mismatch that value is 40.1 %. While, the si (111) substrate (lattice mismatch with ZnO \sim 15.4 %) has a small lattice mismatch compared to the Al₂O₃ (mismatch with ZnO \sim 18%) and si (100) substrate [5]. The lattice mismatch and the lattice constant between the n–ZnO and the other substrate materials is shown in table 2.3. Also, the silicon substrate (\sim 3 \times 10⁻⁶ / $^{\circ}$ C) has thermal expansion coefficient similar to that of ZnO

 $(a_0: 6.5 \times 10^{-6}; c_0: 3.0 \times 10^{-6})$ [6].

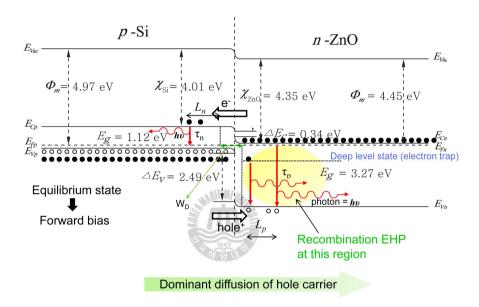


Figure 2.5 The band diagram of n-ZnO/p-Si (111) heterostructure diode and concept for lighting mechanism.

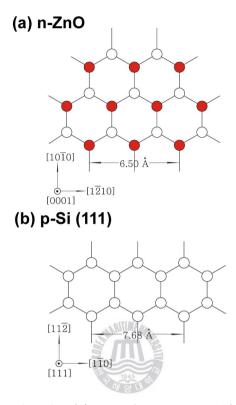


Figure 2.6 The schematic of (a) n-ZnO atoms and (b) p-Si atoms of <111> direction from the top-view.

Table 2.3 The lattice mismatch and the lattice constant between the n-ZnO and the other substrate materials.

Substrate	Lattice constant(Å)	Lattice mismatch(%)
Si(111)	a= 3.84	15.4
Si(100)	a= 5.43	40.1
α -Al ₂ O ₃	a= 4.785	18
GaN	a=3.189	1.9
SiC	a=3.086	5.3

2.3.2 diode current-voltage characteristics

Table 2.4 The summarized notation of the diode equation.

<u>Table 2.4</u>	The summarized notation of the diode equation.
A	cross sectional are of device
D_h	hole diffusion coefficient (m ² s ⁻¹) in the n-side
e	electronic charge (1.6 $ imes$ 10 $^{-19}$ C)
e	(subscript) electron
EHP	electron hole pair
I	diode current
I'	new diode current (different temperature)
J	total current density
I_{so}	reverse saturation current in the Shockley model (minority carrier diffusion)
I_{gen}	reverse current due to thermal generation in the SCL
I_{rev}	total reverse current
k	Boltzmann constant ($k = 1.3807 \times 10^{-23} \text{ JK}^{-1}$)
kT/e	0.0259 V at ~300 K
L_h	hole diffusion length (m) in the <i>n</i> -side
N_d , N_a	donor and acceptor concentration (m ⁻³)
n_i	intrinsic concentration
n_{no} , p_{po}	equilibrium majority carrier concentrations: $n_{no} = N_d$ and $p_{po} = N_a$
n_{po} , p_{no}	equilibrium minority carrier concentrations
SCL	space charge layer or depletion layer: region aroung the metallurgical junction that
JCL	has been depleted of its normal concentration of carriers
T	absolute temperature (K)

V	applied voltage	
V_{O}	built-in voltage	
V_r	reverse bias voltage, $V = -V_r$	
W	width of depletion layer with applied voltage	
9	permittivity of a medium; $\varepsilon = \varepsilon_0 \varepsilon_r$ where ε_0 and ε_r are the absolute and relative	
\mathcal{E}	permittivities	
μ_h	drift mobility of holes in the <i>n</i> -side	
$ au_h$	hole recombination life time (s) in the n -side	
$ au_g$	mean thermal generation time in the SCL	

The basic theory of current-voltage characteristics of p-n junction was established by Shockley [7]. This theory was then extended by Sah, Noyce and Shockley, and by Moll [8]. Here, we summarized the diode current-voltage characteristics at the ideal case for Shockley equation [9].

At $x = W_{dn}$, the hole diffusion current is

$$J_p = -qD_p \frac{dp_n}{dx}|_{W_{D_n}} = \frac{qD_p p_{no}}{L_p} \left[\exp(\frac{q\,V}{k\,T}) - 1\right] \eqno(1)$$

$$J_{n} = qD_{n} \frac{dn_{p}}{dx} |_{-W_{D_{p}}} = \frac{qD_{n}n_{po}}{L_{n}} \left[\exp(\frac{qV}{kT}) - 1 \right]$$
 (2)

where

$$L_p (\equiv \sqrt{D_p \tau_p}) \tag{3}$$

The total current is given by

$$J = J_n + J_p = \left(q \frac{D_n n_{po}}{L_n} + q \frac{D_p p_{no}}{L_p}\right) \left[\exp(\frac{q V}{k T}) - 1\right]$$

$$=(\frac{qD_{n}}{L_{n}N_{A}}+\frac{qD_{p}}{L_{n}N_{D}})n_{i}^{2}[\exp(\frac{qV}{kT})-1]=J_{o}[\exp(\frac{qV}{kT})-1] \tag{4}$$

Equation 4 is the celebrated Shockley equation. The current-voltage characteristics of p-n diode could be understood by using the Shockley equation. To describe experimentally measured characteristics, its equation has to the diode ideality factor and series resistance and given by

$$I = I_o \exp\left[\frac{q(V - Ir_s)}{nkT} - 1\right] \tag{5}$$

where the I_0 is the saturation current at V=0, q is the electronic charge, r_s is series resistance of the diode, k is the Boltzmann constant, n is diode'sideality factor and T is the absolute temperature.

According to the Sah-Noyce-Shockley theory [8], the diode's ideality fact is 1.0 at low voltage and 2.0 at high voltage [10]. But, at the wide band gap material, the diode ideality factors were reported more higher [11-13]. The ideal diode equation assumes that all the recombination occurs via band to band or recombination via traps in the bulk areas from the device. However recombination does occur in other ways and in other areas of the device. These recombinations produce ideality factors that deviate from the ideal. Deriving the ideal diode equation by considering the number of carriers the need to come together during the process produces the results in the table 2.5

Table 2.5 The diode ideality factor at the recombination type.

Recombination type Ideality factor Description
--

Band to band (low level injection)	1	Recombination limited by minority
band to band (low lever injection)		carrier
Dand to hand (high lavel injection)	2	Recombination limited by both carrier
Band to band (high level injection)		types
Auger	2/3	Two majority and on minority carriers
		required for recombination
Depletion region (junction)	2	two carriers limit recombination.

For diode ideality factor (n), the current in a forward biased pn junction is generally described by the Shockley equation which is not affected by series resistance at the low voltage.

$$I = I_o \left[\exp\left(\frac{qV}{nkT} - 1\right) \right] \tag{6}$$

At room temperature (300 K), $\frac{kT}{q}$ is 0.0259 V. For the applied voltage greater than

a few kT/q volt, the -1 can be removed for simplify diode equation

$$I = I_o \left[\exp\left(\frac{qV}{nkT}\right) \right] \tag{7}$$

Taking the logarithms of both sides of the equation,

$$\ln(I) = \ln(I_0) + \frac{qV}{nkT} \tag{8}$$

Thus a plot of the natural logarithm of diode curret versus voltage should be straight line with slope $\frac{q}{nkT}$ (= 38.61 V⁻¹ for n = 1) and a y-axis intercept of $\ln(I_o)$.

The current-voltage characteristics is shown in Fig. 2.7 [9].

- (a) Generation-recombination current region
- (b) Diffusion-current region
- (c) High-injection region
- (d) Series-resistance effect
- (e) Reverse leakga current due to generation-recombination and surface effects

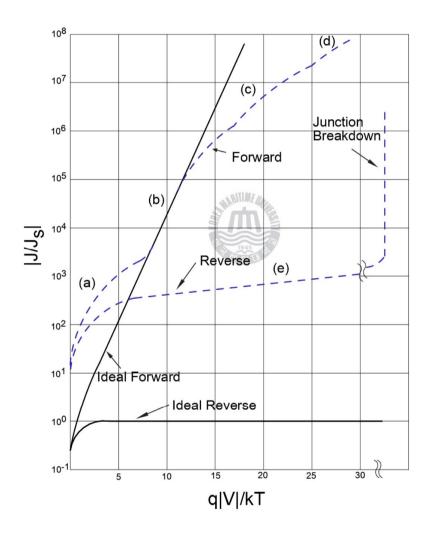


Figure 2.7 Current-voltage characteristics of a practical Si diode [9].

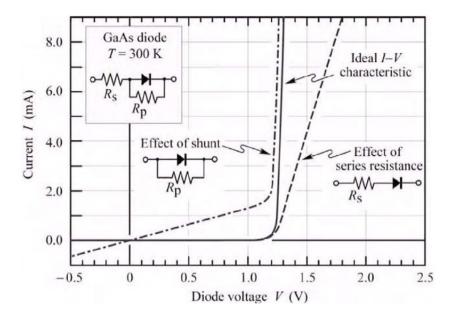


Figure 2.8 Current-voltage characteristics of GaAS diode with R_p (parasitic resistance) and R_s (series resistance) [15],

Frequently a diode has unwanted or parasitic resistance which is shown in Fig. 2.8 [15]. At low forward voltage, a parallel resistance could be effected on current-voltage characteristics, while a series resistance effect on current-voltage characteristics at high forward voltage. A series resistance can be caused by excessive contact resistance or by the resistance of the neutral regions. A parallel resistance can be caused by any channel that bypasses the p-n junction. This bypass can be caused by damaged regions of the p-n junction or by surface imperfections. Consequently, the Shockley equation need to be modified in order take into parasitic resistance and is given by [15]

$$I - \frac{(V - Ir_s)}{R_n} = I_o \exp\left[\frac{q(V - Ir_s)}{nkT} - 1\right]$$
(9)

The series resistance can be evaluated at high voltage where $V > \frac{E_g}{e}$. For sufficiently large voltage, the diode I-V characteristics becomes linear and the series resistance is given by the tangent to the I-V curve

$$R_s = \frac{dV}{dI}|_{at\ V > \ turn-on\ voltage} \tag{10}$$

Equation (5) can be re-written as taking the logarithms of both sides of the equation,

$$\ln(I) = \ln(I_o) + \frac{q(V - IR_s)}{nkT}$$
(11)

The $\ln(I_0)$ values is so small than $\ln(I_0)$ that $\ln(I_0)$ can be neglected. Solving the equation for V and then differentiating V with respect to I yields

$$\frac{dV}{dI} = R_s + \frac{nkT}{q} \frac{1}{I} \tag{12}$$

This equation can be re-written as

$$I\frac{dV}{dI} = IR_s + \frac{nkT}{q} \tag{13}$$

Thus a plot of $I\frac{dV}{dI}$ versus forward current at high voltage is straight line and slope means the series resistance.

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Chapter 3. Thermal-annealing Effect on the Diode

Characteristics of n-ZnO/p-Si (111)

In recent years, Zinc oxide (ZnO) has been regarded as a promising material for ultraviolet light-emitting device applications because of its wide direct band-gap of 3.37 eV and large exciton binding energy of 60 meV. Thin films of ZnO have been grown by using a variety of deposition techniques, such as sol-gel process, spray pyrolysis, chemical vapor deposition (CVD), pulsed laser deposition, and sputtering [1-5]. High-quality ZnO films are essential to fabricate the ZnO-based devices. Therefore, several growth techniques have been employed to improve the film quality. Among them, post-thermal annealing can modify the grain size, the lattice strain, and the extent of orientation in the films, leading to enhanced luminescent properties of ZnO and enhanced [6].

Usually, un-doped ZnO shows n-type conductivity because of the native defects such as oxygen vacancies (V_o) and zinc interstitials (Z_{ni}) [7]. Several experiments have shown that p-type ZnO is achievable with Velements, such as P (phosphorus) and N (nitrogen), or with post thermally annealed ZnO film in an NH₃ ambient [8-10]. However, to realize p-type ZnO for applications is difficult due to the low solubility of the dopant and the highly self-compensating process upon doping [11]. For this reason, some p-type materials, such as p-GaN, p-diamond, and 6H-SiC, were reported to fabricate heterojunction diodes with n-ZnO [12-14], but, those substrates have the problem of high cost. Thus, we used p-type Si(111) substrate as a large area substrate with low cost. Moreover, the silicon substrate has thermal expansion coefficient similar to that of ZnO [15], and the Si(111)

substrate (lattice mismatch ~15.4%) has a better lattice mismatch compared to the Al₂O₃ (mismatch ~18%) substrate on which ZnO was generally deposited.

In this work, our aim is to investigate the effect of annealing temperature on the diode characteristics of n-ZnO and p-Si(111). The n-ZnO/p-Si(111) heterojunction diodes were fabricated by using photolithography. Here, we report the effect of annealing temperature on the current and voltage characteristics, and we discuss about the relationship between the structural and the electrical properties of the ZnO film.

3.1 Experimental Details

p-type Si (111) wafers with a resistivity of 1-50 Ω·cm were used as substrates for the n-ZnO/p-Si heterojunction diodes. Before the deposition, the wafers were ultrasonically cleaned with acetone, methanol, and de-ionized water for 5 min. Then, the samples were etched for 1 min in buffered HF (HF: H₂O = 1: 1) to remove native oxides. Finally, the wafers were rinsed with de-ionized water and blow - dried with a nitrogen gun. Undoped ZnO films were deposited on the p-Si substrates at room temperature by using a RF-sputtering system. The chamber was evacuated to a base pressure of 10⁻⁶ Torr; then, Ar (50 sccm) gas was introduced through mass flow controllers. The working pressure and the RF power were 5 mTorr and 200 W, respectively. The thickness of the deposited ZnO films was approximately 280 nm. After deposition, the ZnO films were annealed at 600, 700, and 800 °C in a N₂ ambient for 1hr. As shown in Fig. 3.1(a), n-ZnO/p-Si

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heterojunction diodes were fabricated using a photolithography process. A metal mask was used Fig. 3.1(b), and the inside circular diameter size was 200 um. For the n-ZnO/p-Si(111) diode structure, the n-ZnO layer was etched selectly by using a BOE (buffered oxide etch) solution until the p-Si substrate was exposed for the p-type electrode pad to be formed. Cr/Ni/Au (15 nm/15 nm/50 nm) was deposited as the n-type contact metal, and Ti/Au (15 nm/50 nm) was deposited as the p-type contact metal by using electron-beam evaporation, respectively. For the Ohmic contacts, the diodes of the formed electrode pad were annealed by using a thermal furnace in a N₂ ambient for 5 min.

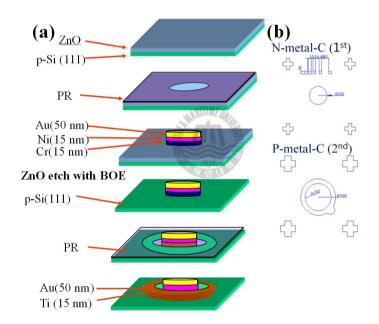


Figure 3.1 (a) Schematic diagram of the fabrication process for a n-ZnO/p-Si heterojunction diode and (b) the patterns of the metal mask.

The structure properties of annealed ZnO films were investigated by XRD and AFM. The diode characteristics of n-ZnO/p-Si were measured by using a

semiconductor parameter analyzer (HP4145B). For a convenient explanation, we numbered each diode sample. The ZnO films annealed at 600, 700, and 800 °C were designated as #D1, #D2, and #D3, respectively.

3.2 Results and Discussion

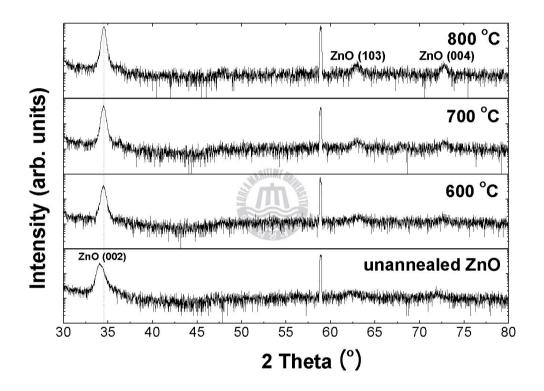


Figure 3.2 XRD spectra of ZnO films with different annealing temperatures in a N_2 ambient (*:Diffraction peaks of the Si substrate).

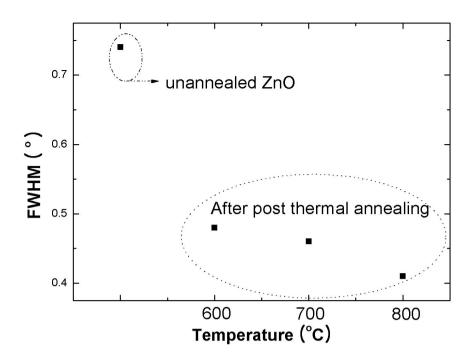


Figure 3.3 FWHM of the ZnO (002) peak of the as-grown ZnO and post thermally annealed ZnO.

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Figure 3.2 shows XRD spectra obtained from ZnO films annealed in a N_2 ambient at different annealing temperatures. Theas-grown ZnO film shows the ZnO (002) peak at $2\Theta = 34.0^{\circ}$. After annealing, the ZnO (002) peaks are observed at $2\Theta = 34.4^{\circ}$ and 34.5° , which correspond to the (002) plane of the hexagonal ZnO. Therefore, the annealed ZnO films are highly oriented with their c-axes perpendicular to the plane of the Si (111) substrate. According to Bragg equation, while the plane spacing of an as-grown ZnO (002) film is 5.26 Å, that of the annealed ZnO film is 5.18 Å which is the known plane spacing in the ZnO (002) direction. Figure 3.3 shows the full width at half maximum (FWHM) of the ZnO

(002) peak for all samples. A smaller FWHM means a larger grain size and a higher film crystallinity. While the FWHM of the as-grown ZnO film was 0.74°, that of the annealed ZnO films was around 0.45°. These phenomena may be explained by re-crystallization and re-growth during the high-temperature annealing [16].

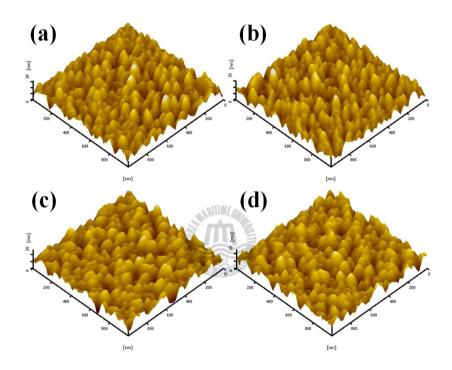


Figure 3.4 AFM surface images of the ZnO films with different annealing temperatures in a N_2 ambient: (a)as-grown ZnO and ZnO annealed at (b) 600 °C, (c) 700 °C, and (d) 800 °C.

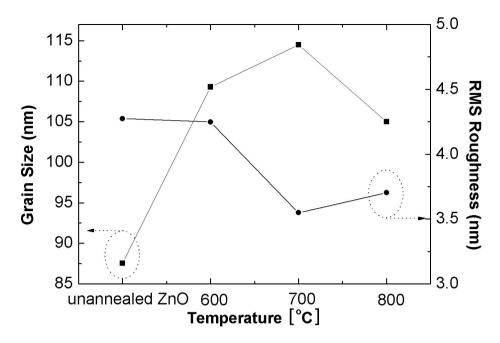


Figure 3.5 Variations of the grain size and the surface roughness of ZnO films annealed in a N_2 ambient at different annealing temperatures from the AFM results.

Figure 3.4 shows the AFM images of the ZnO surface, and Fig. 3.5 shows the grain size and the root-mean-square (RMS) roughness. After annealing, while the grain sizes were increased from 87.5 nm to 114.5 nm, the RMS roughness was decreased from 4.27 nm to 3.53 nm. This implies that the grains went through recovery and re-growth and that the crystal quality of ZnO film was improved by strain release during high-temperature annealing [16].

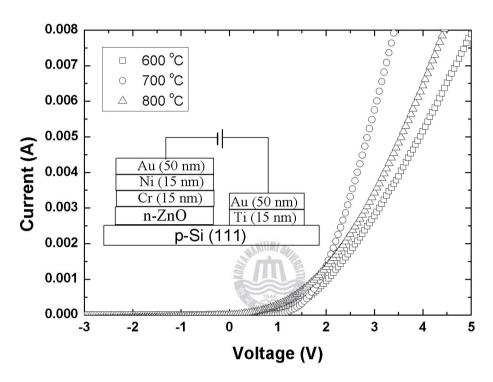


Figure 3.6 Current-voltage characteristics of the n-ZnO/p-Si heterojunction diodes at room temperature. The inset shows a schematic diagram of the heterojunction diode.

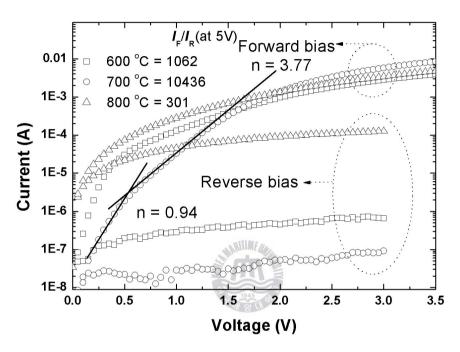


Figure 3.7 Semi-log plots of the current-voltage characteristics of n-ZnO/p-Si(111) heterojunction diodes and the diode ideality fact (n) of ZnO annealed at 700 °C. The values show the forward current (I_F) and reverse current (I_R) ratio at \pm 5 V.

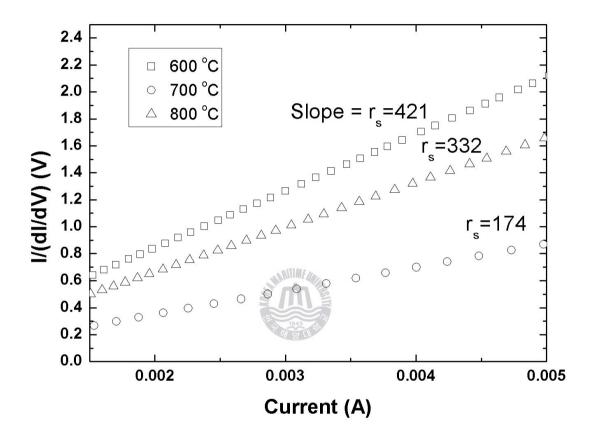


Figure 3.8 I/(dI/dV) – current characteristics of the n-ZnO/p-Si (111) heterojunction diodes and the series resistances at different annealing temperatures.

The current-voltage (I-V) characteristics obtained from n-ZnO/p-Si(111) heterojunction diodes are shown in Fig. 3.6. Regardless of the annealing temperature conditions, the device shows clear rectification. The turn-on voltages of all of

devices ranged from 1.4 to 1.7 V. The insert of Fig. 3.6 shows the schematic structure of the n-ZnO/p-Si(111) heterojunction diode. A semi-log plot of the current versus bias in Fig. 3.6 is shown in Fig. 3.7. According to the I-V characteristics of the standard diode equation [17],

$$I = I_0 \{ \exp[q(V - Irs)/nkT] - 1 \}$$
(1)

$$n = q/kT(dV/dlnI) (2)$$

where the I_0 is the saturation current at V = 0, q is the electronic charge, r_s is series resistance of the diode, k is the Boltzmann constant, n is diode's ideality factor and T is the absolute temperature. According to Eq.(1), we calculated the series resistance, which is shown in Fig. 3.8 at high voltage. The series resistance ranged from 174 to 421 Ω, and #D2 has the lowest series resistance. Compared with the structural and the diode characteristics, the diode characteristics were changed by the crystallinity and the surface state of the thin films [18]. According to the AFM results, the ZnO film annealed at 700 °C had the largest grain size and the smallest RMS roughness. Better crystal quality was shown to be related to a lower series resistance. In addition, the semi-log plots of the current-voltage curves at forward bias and reverse bias are show in Fig. 3.7. Thus, we calculated the diode's ideality factor of #D2 through Eq.(2). According to the Sah-Noyce-Shockley theory [19], the diode's ideality fact is 1.0 at low voltage and 2.0 at high voltage. However, while the value of the diode's ideality fact was about 0.94 at voltages from 0.2 to 0.5 V, the ideality value at high voltages from 0.7 to 1.2 V was n =3.77. Interestingly, we could not apply the high voltage the result

Sah-Novce-Shockley theory. Wang et al. [20] reported that deviations of the diode's ideality fact at high voltage could be inferred from the nonlinear metal-semiconductor contact. Meanwhile, under reverse voltage, the breakdown voltage of all the ZnO/Si heterojunction diodes was over 10 V. In addition, we examined the I_F (forward current) to I_R (reverse current) ratio at \pm 5 V. The value of I_F/I_R of #D2 was over ten times higher than those of the other samples. Finally, the radiation from the n-ZnO/p-Si diodes was investigated for under forward bias at room temperature. Regardless of the annealing temperature, the n-ZnO/p-Si (111) diodes exhibited weak vellow light at 13-15 V, as shown in Fig. 3.9(a). Figure 3.9(b) shows the fabricated diode patterns. The emitted light was considerably vellow for two reasons. First, a dislocation occurred due to the lattice mismatch at the interface of the ZnO layer on the Si substrate and functioned as a non-recombination center, such as a defect affecting the irradiation in the n-ZnO/p-Si diodes [21]. The other reason is that in our experiment, the p-Si (111) substrate has a much lower hole concentration ($^{\sim}10^{15}~\mathrm{cm}^{-3}$) than the electron concentration (~1018 cm-3) of all annealed ZnO films. Because of the low hole concentration, recombination may dominantly occur in the depletion region on the Si side.

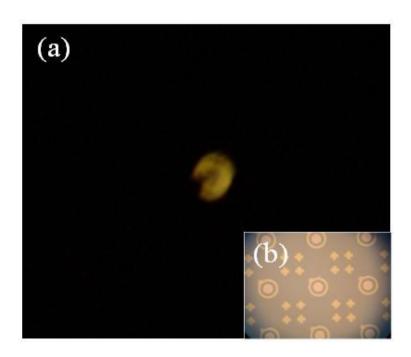


Figure 3.9 (a) Electroluminescence image of a n-ZnO/p-Si heterojunction diode at forward bias (13 $^{\sim}$ 15 V). (b) The inset shows the patterns of a n-ZnO/p-Si heterojunction diode.

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3.3 Conclusion

ZnO films were deposited on p-type Si (111) substrates by using a RF-sputtering system at room temperature and were annealed at 600, 700 and 800 $^{\circ}$ C in a nitrogen ambient for 1 hr. Annealed n-ZnO/p-Si (111) heterojunction diodes were formed by using a photolithographic method. All the annealed ZnO films had a better crystal quality than the as-grown films. The results of the diode characteristics investigated by using current-voltage measurements showed diode characteristics that varied with the annealing temperature. The turn-on voltage of the diodes was about 1.4 $^{\sim}$ 1.7 V, and the series resistances were about 174 $^{\sim}$ 421 $^{\circ}$ Q, and the current-voltage curves show a clear rectification. Moreover, we observed a yellow radiation at a forward bias (13 $^{\sim}$ 15 V).



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Chapter 4. Dependence of the Diode Characteristics of

n-ZnO/p-Si (111) on the Si Substrate Doping

In recent years, zinc oxide (ZnO) has attracted interest for its use in next-generation light-emitting diodes because of its wide direct band gap (~3.37 eV), high exciton binding energy (~60 meV), and high transparency (>80%) at visible wavelengths [1]. It is generally difficult to obtain p-type ZnO because undoped ZnO exhibits n-type conductivity due to native defects, such as zinc interstitials (Zn_i) and oxygen vacancies (V_o) [2]. Some research groups have succeeded in producing p-type ZnO, but it is difficult to use p-type ZnO in low solubility the dopant applications the of self-compensating process that occurs on doping [2]. For these reasons, other research groups have attempted to produce hetero junctions with n-type ZnO on p-type substrates, such as p-GaN, p-SiC, p-diamond, and p-Si [3-6]. Silicon substrates have several advantages, including a large area and low cost.

If efficient emission is to be achieved in a light-emitting device based on an n-ZnO/p-Si heterojunction diode, hole-electron pairs have to recombine in the ZnO region of the wide band gap due to the carrier concentration difference at forward bias. We considered that the concentration of electrons in the n-type ZnO film or of holes in the p-type Si substrate can be varied by using the method proposed below. A ZnO film annealed in a N₂ ambient was found to have a higher carrier concentrations and a lower resistivity than a ZnO film annealed in an air ambient [7]. When the hole concentration was changed, differently doped Si substrates could be used for the p-type Si substrate.

The aim of this study is to investigate the effect of doping concentration in the Si substrate on the diode characteristics of n-ZnO/p and $p^+\text{-}Si$ substrates. ZnO films were deposited on a low-resistivity (p^+) (~0.004 - 0.0055 $\Omega\cdot cm$) silicon substrate and a high-resistivity (p) (~1 - 20 $\Omega\cdot cm$) silicon substrate by using a radio-frequency (RF) sputter system. The effect of carrier concentration on the current and voltage characteristics was investigated, and the relationship between carrier concentration and the emission properties of an $n\text{-}ZnO/p^+\text{-}Si$ diode is discussed.

4.1 Experimental Details

Undoped ZnO films were deposited by RF-sputtering at room temperature on p-type Si (111) substrates having resistivities of $1-20~\Omega\cdot\text{cm}$ (p) and $0.004-0.0055~\Omega\cdot\text{cm}$ (p⁺) for 1 hr by using a ZnO (4N) target. Prior to deposition, the wafers were ultrasonically cleaned for 5 min each in acetone, methanol, and deionized water. The samples were dipped for 2 min into buffered HF (HF: H $_{2}$ O = 1:1) to remove the native oxide. Finally, the samples were rinsed with deionized water and dblow-dried with a nitrogen gun. Prior to deposition, the Si substrate was placed in a vacuum chamber evacuated to a base pressure of $^{\sim}$ 10⁶ Torr. Ar gas (50 sccm) was used as the reaction gas, and was introduced through mass flow controllers. The working pressure was 5 mTorr and the RF power was 200 W. The deposited ZnO films were approximately 280 nm thick.

After deposition, the ZnO films were annealed in a horizontal thermal oxidation furnace at 800 °C in N_2 and air ambients. After thermal annealing,

n–ZnO/p–Si heterojunction diodes were fabricated by using photolithography. A metal contact was formed by using electron–beam evaporation. Then–metal and p–metal were Ni/Au(15/50 nm) and Ti/Au(15/50 nm), respectively. To achieve an Ohmic contact between the metal and the semiconductor, we annealed the devices in an N_2 ambient at 350 °C for 5 min in a horizontal thermal furnace. The electrical properties were evaluated by using Hall measurements (Ecopia, HMS–3000) with the Van der Pauw method. The diode characteristics of n–ZnO/p–Si were measured using a semiconductor parameter analyzer (Hewlett–Packard, HP4145B).

4.2 Results and Discussion

Table 4.1 Carrier concentration, mobility, and resistivity of ZnO annealed in N_2 and air ambients, for p and p⁺-silicon substrates having different resistivities.

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Material	Туре	Carrier concentration	Mobility	Resistivity [Ω·cm]
		$[/cm^3]$	$[cm^2/V \cdot s]$	
p ⁺ -Si(111)[0.005	P	3.1×10 ¹⁹	44.3	4.5×10^{-3}
Ω·cm] p-Si (111)	P	1.9×10 ¹⁵	308.1	1.0×10 ¹
[10 Ω·cm] ZnO annealed	n	4.3×10 ¹⁸	9.87	1.5×10^{-1}
$\begin{array}{c} \text{in} \ N_2 \\ \text{ZnO annealed} \end{array}$	n	9.1×10 ¹⁶	10.28	7.8×10^{0}
in air				

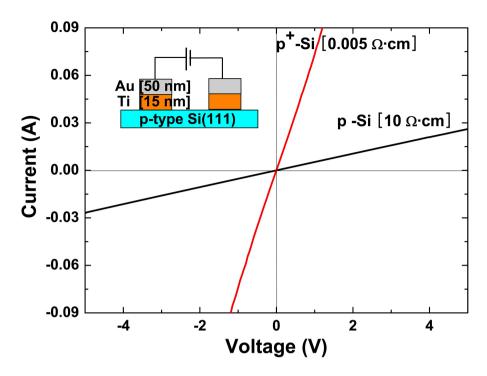


Figure 4.1 Device annealed in N_2 exhibits ohmic I-V behavior with Ti/Au on the p and the p⁺-Si substrates.

Table 1 shows the Hall measurement results for the ZnO films annealed in N_2 and air ambients at 800 °C and for high-resistivity (p) and low-resistivity (p⁺) commercial p-type substrates. The resistivities of the p⁺ and the p-Si substrates were 4.5×10^{-3} and 1.0×10^{1} $\Omega \cdot cm$, corresponding to hole concentrations of 3.1×10^{19} and 1.9×10^{15} /cm³, respectively. The hole mobilities in the p⁺ and the p-Si substrates were 44.3 and 308.1 cm²/V·cm, respectively. The hole mobility in the p-Si substrate is about seven times higher than that in the p⁺-Si substrate due to its lower hole concentration as a lower carrier scattering. The electron concentrations for the ZnO films annealed in N_2 and air were 4.3×10^{18} and 9.1×10^{16} /cm³, respectively. This result agrees with the finding that the oxygen

concentration in the ZnO films, which depends on the employed annealing ambient, affects the electrical properties of the films [7]. Figure 4.1 shows the I-V characteristics for the Ti/Au contacts on the p^+ and the p-Si substrates after annealing at 350 °C for 5 min in N_2 ambient. These values were measured using the TLM method with an outer pad-to-pad connector. Theas-deposited Ti/Au on the silicon exhibited a non-linear I-V behavior, although after thermal annealing it showed a clear linear I-V behavior in the voltage range from -5 to 5 V. The p^+ -Si substrate has a higher current flux than the p-Si substrate due to its low resistivity; however, Ohmic behavior was confirmed in both the p^+ and the p-Si substrates with Ti-Au metal, as evidenced by their linear I-V characteristics.



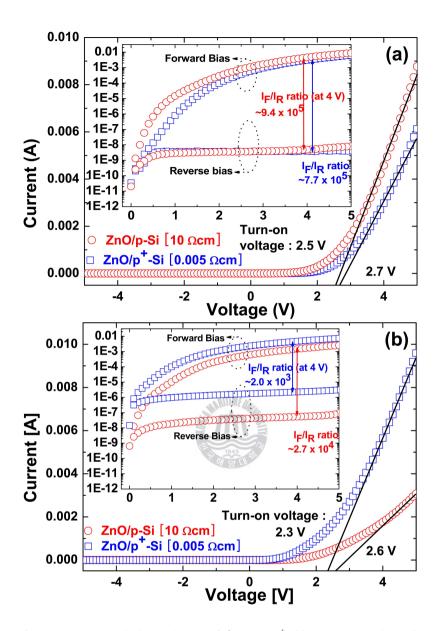


Figure 4.2 I-V characteristics of n-ZnO/p and p^+-Si heterojunction diodes at room temperature subjected to post-thermal annealing in (a) N_2 and (b) air. The inset shows a semi-log plot of the I-V characteristics of n-ZnO/p and p^+-Si heterojunction diodes. The values show the forward current (I_F) and reverse current (I_R) ratios at ± 4 V.

Figure 4.2(a) shows the I-V characteristics of ZnO annealed in N₂ on the p⁺ and the p-Si substrates, which have similar turn-on voltages of 2.7 and 2.5 V, respectively; other research groups have attempted to achieve similar turn-on voltages in an n-ZnO/p-Si structure [8,9]. The inset in Fig. 4.2 (a) shows a plot of log(I) vs. voltage; when the reverse bias reaches 5 V, both p⁺ and p-Si have a small reverse leakage current of about 10^{-9} A. In contrast, other research groups have reported reverse leakage currents of $10^{-4} \sim 10^{-5}$ A [10]. Moreover, the ratio of the forward current to the reverse current (I_F/I_R) at \pm 4 V is high, being approximately 10^5 .

Figure 4.2(b) shows the I-V characteristics of the ZnO films annealed in air on p⁺ and p-Si substrates; they have turn-on voltages of 2.3 and 2.6 V, respectively. The values of I_E/I_R at 4 V for the ZnO films annealed in air on p⁺ and p-Si substrates are 10^3 and 10^4 , respectively. For a reverse bias of 5 V, the leakage current of the ZnO films annealed in air on p⁺ and p-Si substrates are 10⁻⁶ and 10^{-8} A, respectively. Of the two ZnO films annealed in air, the one on the p⁺-Si substrate has a higher leakage current. These results indicate that heavy doping of p⁺-Si makes a tunneling current more probable [10]. In addition, under reverse bias, the ZnO film annealed in N_2 has a lower leakage current than does the non-annealed ZnO films on p and p⁺-Si substrates. This finding indicates that non-annealed ZnO films on p and p⁺-Si substrates place considerable strain on the ZnO layer, generating defects, such as dislocations and grain boundaries, and generating a leakage current path. In contrast, ZnO films annealed in N2 result in reduced strain on the ZnO lattice due to relaxation and regrowth of the ZnO layer. Thus, the heterojunction diode fabricated from ZnO annealed in N2 exhibited more stable rectification characteristics and higher values of I_F/I_R .

To reveal the injection current characteristics at forward bias, we plot the I-V curves on a log-log scale for samples annealed in N_2 (Fig. 4.3(a)) and in air (Fig. 4.3(b)). These plots have three different regions. At a low forward bias (Fig. 4.3(a)), the current injection in region I of the p^+ -Si device increases linearly from 0 to about 0.5 V whereas this region extends only to about 0.25 V for the p-Si device. In particular, at a low forward bias, the injection currents of the devices annealed in air increase more linearly and to a higher current up to voltages of 0.55 V (p+) and 0.6 V (p).

This limiting current can be explained by using the leakage current path at low voltage [11]. Ye et al. [8] applied the Anderson model to n-ZnO/p-Si and found that the conduction band offset was $\Delta E_C = \chi_{ZnO} - \chi_{Si} = 0.4\,e\,V$ and that the valence band offset was $\Delta E_V = E_{g,ZnO} - E_{g,Si} + \Delta E_C = 2.55 \, eV$. The energy band diagram exhibits a similar narrow neck on the band interface between the Si band and the ZnO band. At a low forward bias, injected hole carriers accumulate in the ZnO/p-Si interface due to the high valence band offset, and they recombine across the narrow neck of the band interface. This recombination mechanism is presumably associated with threading dislocations (TDs) in the ZnO layer. These dislocations form a leakage current path [11]. The current in region I is higher for the ZnO film annealed in air than for the ZnO film annealed in N2; this is especially true for the ZnO film on the p⁺-Si substrate annealed in air due to its high hole concentration. This current could be due to a higher concentration of TDs in the ZnO layer because of a new phase of mixed Si-O at the ZnO/p-Si interface and/or the poor state of the junction surface [12]. In a previous study [13], the Auger depth profile of ZnO/p-Si annealed in air revealed that annealing in an ambient containing oxygen produced oxygen-rich ZnO

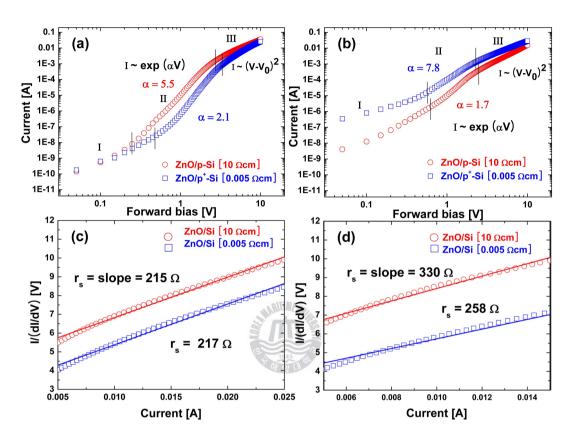


Figure 4.3 Log(I) - log(V) plots of current-voltage characteristics of n-ZnO/p and p⁺-Si heterojunction diodes subjected to post-thermal annealing in (a) N₂ and (b) air. Also shown are I/(dI/dV) plots of n-ZnO/p and p⁺-Si heterojunction diodes subjected to post-thermal annealing in (c) N₂ and (d) air, together with the series resistances.

films and that the ZnO/Si interface had a wide range of concentrations of O and Si atoms. In region II in the present study (Figs. 4.3(a) and (b)), the current increases exponentially in accordance with the equation $I \sim exp(aV)$ because of the recombination-tunneling mechanism, which is usually observed in wide-band-gap p-n diodes [14]. The constant awas evaluated by curve fitting the exponential data in Figs. 4.3(a) and (b). For devices annealed in N₂, awas 2.1 and 5.5 V⁻¹ for p⁺ and p-Si substrates, respectively, while for devices annealed in air, a was 7.8 and 1.7 V⁻¹ for p⁺ and p-Si substrates, respectively. In the recombination-tunneling mechanism, the constant a can be expressed as [8, 14]

$$a = (8\pi/3h)(m_h * \varepsilon_s)^{1/2} N_D / [N_A^{1/2} (N_A + N_D)], \tag{1}$$

where h is Planck's constant, m_h^* is the effective mass of holes (0.69 m_0), ε_s is the dielectric constant of ZnO (= 8.5), N_D is the donor concentration, and N_A is the acceptor concentration. According to Eq. (1), a increases if N_D is increased whereas α decreases if N_A is increased. ZnO films on p-Si substrates having different N_D were produced by post-thermal annealing, and Hall measurements were used to estimate N_D . The results revealed that the ZnO film annealed in N_2 had a higher N_D than the ZnO film annealed in air, as the former had a higher α value. This result could be explained by the lattice mismatch between ZnO and Si (111), which is as large as 15.4 %. Consequently, a dislocated n-type region is usually generated by the strain on the ZnO/Si interface, and more donor-liked efects (e.g., oxygen vacancies) remain in the ZnO film annealed in N_2 than in the ZnO film annealed in air. These defects provide are combination-tunneling path and produce a higher electron density in the ZnO film annealed in N_2 [8].

Surprisingly, for the different values of N_A in the p⁺ and the p-Si substrates, the avalue of ZnO/p⁺-Si annealed in air is higher than that of ZnO/p-Si. This may be explained by the more highly doped p⁺-Si having a much higher acceptor carrier density than the electron carrier density of ZnO annealed in air; these high acceptor carriers play a major role informing the tunneling path. When V > 3.0 (region III), the I-V characteristics follow a power law, $I \sim (V-V_0)^2$, which is attributed to space-charge-limited current (SCLC) conduction. This SCLC mechanism has been reported to be due to single-carrier injection in wide-band-gap semiconductors [15]. This phenomenon is clearly observed in the ZnO film annealed in air. In the ZnO film on the p⁺-Si substrate annealed in air, single carrier injection (holes) produces a much higher hole concentration and mobility in Si than it does in ZnO.

The I-V curves start to deviate from linearity at high forward biases due to the series resistance (r_s). The current of a semiconductor diode with a series resistance can be expressed by [15]

$$I = I_0 \left(\exp[q(V - Ir_s)/nkT] - 1 \right), \tag{2}$$

where I_0 is the saturation current at V = 0, q is the electronic charge, r_s is the series resistance of the diode, k is Boltzmann's constant, n is the diode's ideality factor, and T is the absolute temperature. When I/(dI/dV) is plotted against I, as shown in Fig. 4.3(a) for N_2 annealing and in Fig. 4.3(b) for air annealing, the slope is r_s . Diode series resistances in the range from 215 to 330 show a good fit to the experimental curve. ZnO films annealed in air have higher series resistances than do ZnO films annealed in N_2 because of the higher sheet resistance of ZnO annealed in air and the lower electron carrier density, which could produce a high

contact resistance between n-ZnO and n-metal.

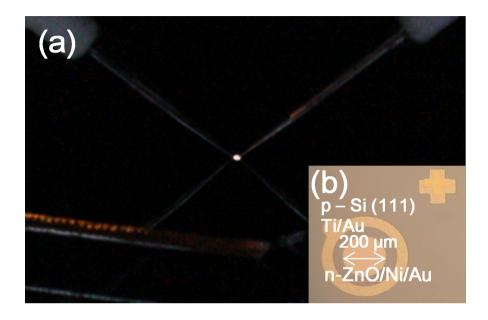


Figure 4.4 (a) Electroluminescence image of an $n-ZnO/p^+-Si$ heterojunction diode at forward bias (over10 V). (b) Inset shows the patterns of an $n-ZnO/p^+-Si$ heterojunction diode.

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Finally, the radiation emitted from the n-ZnO/p⁺-Si diodes was investigated under forward bias at room temperature, as shown in Fig. 4.4. The emission of n-ZnO/p-Si was described in our previous paper[16]. The inset in Fig. 4.4 shows the diode pattern; the radiation is detected in an inner circle having a diameter of 200 mm on the interface between n-ZnO and p⁺-Si. The n-ZnO/p⁺-Si(111) diodes emitted yellow light at voltages over 10 V; this emission is superior to that from n-ZnO/p-Si diodes. This finding is thought to be due to hole injection being dominant in the ZnO region of the wide band gap due to the hole concentration

being higher than the electron concentration in the present case. The emitted light was noticeably yellow for deep-level emission. Photoluminescence spectra (not shown here) had a broad peak at around 565 nm in the yellow region. This yellow emission is associated with a deep-level emission from the ZnO region.

4.3 Conclusion

ZnO films were deposited on p-type Si (111) substrates by using an RF-sputtering system at room temperature and were annealed at 800 °C in nitrogen and air ambients for 1 hr. The devices exhibited excellent rectification behaviors and diode characteristics, having turn-on voltages in the range from 2.3 to 2.7 V and series resistance from 215 to 330 Ω . The diode characteristics could be varied by using different annealing ambients and different doping concentrations in p-type silicon. The n-ZnO/p⁺-Si(111) heterojunction diodes exhibited an enhanced yellow emission for forward biases of over 10 V.

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Chapter 5. Effect of Indium doped-ZnO/p-Si(111) on

Diode Characteristics

ZnO material is attractive for using optical devices, solar cells, transparent conducting oxide electrodes, and transparent thin film transitors because of its wide band gap (3.37 eV) energy and large exciton binding energy (60 meV) [1,2]. Recently, although the results of p-type ZnO film have been reported [3-5], it is still difficulty to growth of reliable p-type ZnO material due to the low solubility of the dopant and the highly self-compensating process upon doing [6]. For these reasons, the p-n junction structure have attempted with other p-type materials such as p-GaN, p-SiC and p-Si [7-9]. Especially, the p-type silicon substrate has various advantages such as large area substrate, low cost and excellent Si-based technology. An un-doped ZnO material has dominant n-type conductivity at room temperature due to the native defects such as zinc interstitials (Zn_i) and oxygen vacancies (V_o) , or present of hydrogen [6]. In addition, the applications of the ZnO film can be used from insulator and metal to change the carrier concentration. A study of the ZnO about the carrier concentration is to obtain high carrier concentration (over 10²⁰/cm³) for substitution of indium tin oxide. The high carrier concentration of n-type ZnO can be obtained as high doping (over 1 at. %) in the ZnO with group III donor impurities such as Ga, Al and In [10-12]. As the p-n junction diode need to the properties of semi-conductor, we attempted doping in the ZnO with indium (0.6, 1, 5, and 10 at. %) for a stable n-type properties on diode characteristics.

In this work, our aim is to investigate relationship between changed dido characteristics and effect of In-doping in the ZnO. The In-doped ZnO films were deposited on the commercial p-Si substrate by using a PLD system. The In-doped ZnO/p-Si hetero junction diodes were fabricated by using a photolithography. Here, we report current-voltage characteristics of In-doped ZnO/p-Si hetero junction diode and we discuss about the relationship between changed the diode characteristics and changed physical properties by the In-doping in the ZnO.

5.1 Experimental Details

The Indium-doped ZnO films and un-doped ZnO were deposited on the p-Si(111) with resistivity of 10 Ω ·cm and carrier concentration of 1.9 × 10¹⁵/cm³ by using a pulse laser deposition system with In-doped ZnO targets which have In (0.6, 1, 5, and 10 at. %) content. A detail description of In-doped ZnO targets can be found elsewhere [13]. Prior to the deposition, the wafers were ultrasonically cleaned with acetone, methanol and de-ionized water for 5 min. Then the samples were dipped for 2 min into buffered HF (HF: $H_2O = 1:10$) to remove SiO₂ layer. Finally, the samples were rinsed with de-ionized water and blow-dried with a nitrogen gun. The Si substrate had been put into the chamber that was evacuated to a base pressure of ~10⁶ Torr before deposition. In this experiment, a KrF excimer laser ($\lambda = 248$ nm, $\tau = 25$ ns) was used for the ablation of the In-doped ZnO target at the energy density of ~2 J/cm². The In-doped ZnO was deposited for 60 min below conditions which were the oxygen pressure of 130 mTorr and deposition temperature of 600 °C in the chamber. The result of α -step, the thickness of the In-doped ZnO film was ~250 nm.

deposition, the hetero diodes tructure was made by using photolithography process. Its detail description can be found elsewhere [14]. For the n-ZnO/p-Si(111) hetero diode structure, In-doped ZnO and un-doped ZnO were selectively etched by using a buffered oxide etch solution until the p-Si surface. As shown in fig. 5.1(a), after the n-metal and the p-metal were deposited by using an e-beam evaporation system, the electrodes were annealed at 350°C in N₂ ambient for 5 min using a horizontal thermal furnace to obtain the ohmic behavior, Figure 5. 1(a) shows the hetero junction diode with diameter of 200 µm. The structure characteristics of deposited ZnO films were investigated by XRD (D/MAX 2100H) and Transmission Electron Microscope while the electrical properties were estimated by Hall measurement (Ecopia, HMS-3000) using Vander Paw method. In addition, current-voltage characteristics were measured by a semiconductor parameter analyzer (Hewlett-Packard, HP4145B).

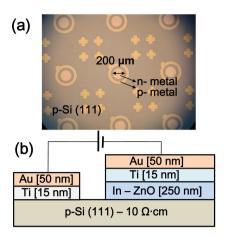


Figure 5.1 (a) The n-ZnO/p-Si(111) diode pattern image viewing top, measuring optical microscope and (b) schematic diagram of n-ZnO/p-Si diode, viewing cross section.



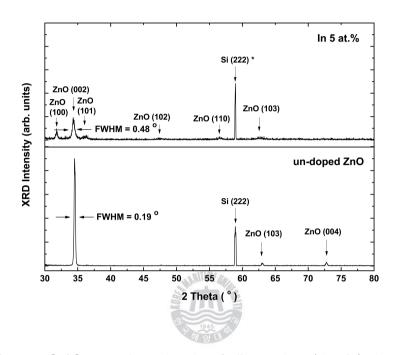


Figure 5.2 XRD θ -2 θ scan of un-doped ZnO film and In (5 at.%)-doped ZnO film.

Figure 5.2 shows Θ - 2Θ x-ray diffraction (XRD) pattern of un-doped ZnO and In (5 at.%)-doped ZnO films. Un-doped ZnO film and In-doped ZnO films show the preponderant peak at the 2Θ =34.4°, which is corresponding to the (002) plane of the hexagonal ZnO. The 2Θ values at 31.8°, 36.3°, 47.7°, 62.9° and 72.8° are corresponding to the (100) (101), (102), (103) and (004) diffraction peaks of ZnO films, respectively. The phases corresponding to indium oxide or other zinc-indium compound were not observed. As compared with un-doped ZnO film, the ZnO (002) peak intensity of In (5 at. %)-doped ZnO films were decreased, while the intensity

of the $(10 \, \ell)$ ZnO peak was increased by In-doping. Caglar et al. [15] reported that Indium incorporation in to the compounds caused reorientation which exhibited itself as $(10 \, \ell)$ preferred orientation. The full width of half maximum (FWHM) of ZnO (002) peak of un-doped ZnO and of the In $(5 \, \text{at.} \%)$ -doped ZnO were $0.19 \, ^{\circ}$, and $0.48 \, ^{\circ}$, respectively.

Table 5.1 Carrier concentration, mobility and resistivity of un-doped ZnO, In (0.6, 1, 5, and 10 at. %)-doped ZnO and p-Sisubstrate.

	Carrier concentration	[/cm ³] N	Iobility [cm ² V·s]	Resistivity [Ω·cm]
un-doped ZnO	-3.8×10^{17}		20.4	8.7×10^{-1}
In 0.6 at. %	-3.1×10^{18}		24.4	8.7×10^{-2}
In 1 at. %	-5.7×10^{18}	STATE OF THE STATE	18.3	5.9×10^{-2}
In 5 at. %	-2.2×10^{19}	1945	11.4	2.4×10^{-2}
In 10 at. %	-3.0×10^{19}	W S LIV	13.8	1.5×10^{-2}
p-Si (111)	1.90×10^{15}		308.1	1.0×10^1

The table 5.1 shows the result of Hall measurement of un-doped ZnO film and of In $(0.6^{\sim}10$ at. %)doped-ZnO films at room temperature. The electron concentration of In (10 at. %)-doped ZnO film increased up to 3.0×10^{19} /cm³ and the resistivity decreased up to the 1.5×10^{-2} Ω ·cm. Caglar et al. [15] was reported that this phenomenon is caused by the interstitials indium atoms or replacing Zn²+ atoms with the In³+atoms to make excess electron. We obtained more improved n-type conductivity to the ZnO films with increased carrier density $(^{\sim}10^{19}$ /cm³) and

with little changed mobility by In-doping.

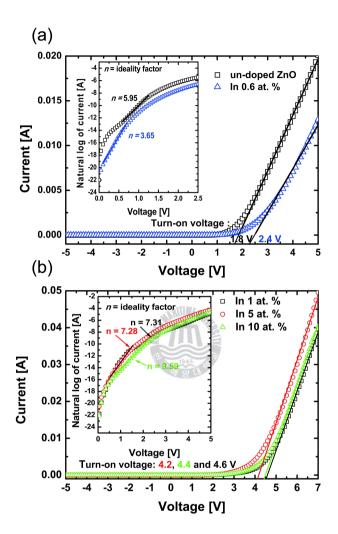


Figure 5.3 I-V characteristics of un-doped ZnO/p-Si diode and In (0.6~10 at.%)-doped ZnO/p-Si diode with turn-onvoltage, The insets show the ln(I)-V plots of I-V curves with the ideality factors.

Figure 5.3 shows the current-voltage (I-V) characteristics of the ZnO/p-Si and In (0.6~10 at.%)-doped ZnO/p-Si (111) heterojunction diodes at the room temperature. The devices show clear rectification with turn on voltage of 1.8, 2.4, 4.2, 4.4 and 4.6 V, respectively. The turn-on voltage of general un-doped ZnO/p-Si diode was reported about ~2V [16,17]. The turn-on voltage was increased as increasing In-doping concentration. This result was thought by changed ZnO phase. Moreover, In (10 at.%)-doped ZnO/p-Si diodes show the lowest reverse leakage current about 3.5×10^{-9} A (2.8×10^{-6} A/cm²) at -5 V. These values are very low compared to un-doped ZnO (6.2×10^{-6} A, 4.9×10^{-3} A/cm²). At the n-ZnO/p-Si hetero junction diode, Mridha et al. [18] reported the low leakage current density value of 7.6×10^{-5} A/cm² at -5V, but we obtained more low its value using an In (10 at%)-doped ZnO/p-Si diode.



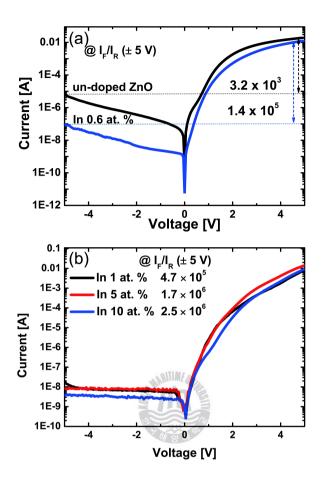


Figure 5.4 The Semi-log plots of the I-V curves. The insert values are on-off ratio at ± 5 V.

Figure 5.4 shows $\log (I)$ -V plots from the I-V results. At forward current and reverse current ratio at ±5 V, its value of un-doped ZnO is 3.2×10^3 , while In (10 at.%)-doped ZnO/p-Si diodes show high I_F/I_R ratio of 2.5×10^6 , respectively. These results may be thought by a low leakage current at the reverse bias due to the changed structures of the ZnO films which make more stable current transport characteristics without leakage current path at reverse bias by In-doping. For

obvious diode characteristics, we derived the diode factors such as ideality factor, series resistance, barrier height from the I-V curve. The standard diode equation can be written as [18, 20],

$$I = I_s \exp\left[\frac{qV}{nkT} - 1\right] \tag{1}$$

where I_s is the saturation current, q is the electron charge, n is ideality factor, k is the Boltzmann constant $(1.38 \times 10^{-23} \text{ J/K})$, T is absolute temperature. At this eq.(1), because under forward bias is greater than a few kT/q volt, the -1 can be removed for simplify diodeequation [18]. To obtain the ideality factor in low forward bias, I-V curves were plotted on an $\ln(I)$ -V scale and it was shown in inset of Fig. 5.3. The ideality factors were obtained from the slope of $\ln(I)$ -V curves and the J_s obtained from the straight line intercept of $\ln(I)$ -V curvesat V = 0. An ideality factor of un-doped ZnO/p-Si diode is 5.95, while its values of $\ln(0.6^{\sim}10 \text{ at. }\%)$ -doped ZnO/p-Si diodes have from 3.65 and 9.59, respectively. The ideality factors of un-doped ZnO/p-Sidiodes were variously reported about 3.91, 5.47 and 4.15 [18, 19]. According to Sah-Noyce-Shockley theory [21], the ideality fact is 1.0 at low voltage and 2.0 at high voltage. The reason of high ideality factor has presumed due to the presence of SiO₂ layer at interface and/or the poor junction state [18,20]. The saturation current density of un-doped ZnO is 5.59×10^{-5} A/cm² while In $(0.6^{\sim}10 \text{ at.}\%)$ -doped ZnO/p-Si are $9.15 \times 10^{-7} \sim 8.52 \times 10^{-6}$.

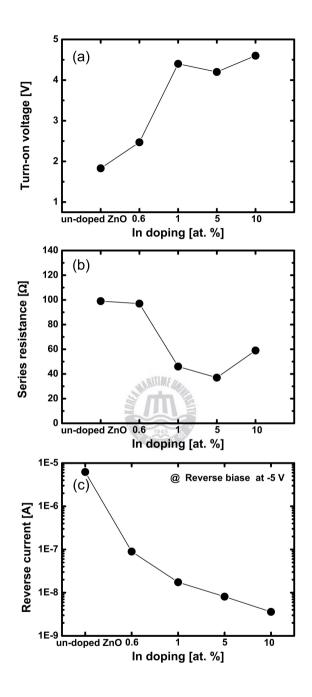


Figure 5.5 Relationship between the indium doping concentration and the (a) turn-on voltage, (b) series resistance, (c) reverse current at -5 V.

When I/(dI/dV) is plot against I, slope is series resistance (r_s) . It was obtain by fitting method from I-V curve at high forward voltage. The series resistances show dominant I-V characteristics at a high voltage. The series resistances of un-doped ZnO/p-Si is 99 Ω and In $(0.6^{\sim}10 \text{ at.\%})$ -doped ZnO/p-Si are 97, 46, 37, 59 Ω , respectively. The decrease of the series resistance was thought by decreasing specific resistivity in the ZnO film. The barrier height Φ_b is calculated from [18,19],

$$\phi_b = \frac{KT}{q} \ln(\frac{A^* A T^2}{I_s}) \tag{2}$$

where Φ_b is barrier height, A is area of the diode and A^* is effective Richardson constant (32/cm²k²) for ZnO. The barrier height of un-doped ZnO/p-Si diode is 0.63 eV and In (0.6~10 at.%)-doped ZnO/p-Si diode is from 0.68 ~ 0.73., respectively. The barrier heights of un-doped ZnO/p-Si have reported about 0.82, 0.77 and 0.65 eV [18, 19]. We summarize the I-V characteristics in table 5.2 and relationship between the indium doping concentration and the I-V characteristics ((a) turn-on voltage, (b) series resistance, (c) reverse current at -5 V) is shown in Fig. 5.5.

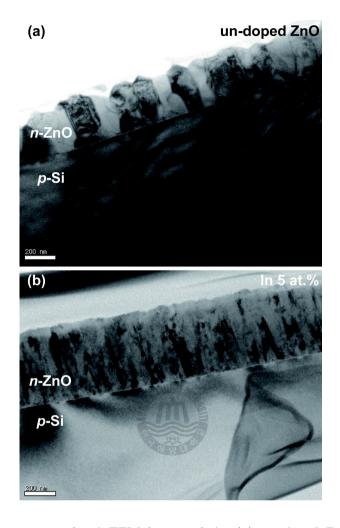


Figure 5.6 The cross-sectional TEM image of the (a) un-doped ZnO and (b) In (5 at. %) / p-Si(111).

Figure 5.6 shows a cross-sectional TEM image of un-doped ZnO and In (5 at. %)-doped ZnO on the p-Si (111) substrate. The TEM image shows the random textured ZnO films because of incorporated indium atoms. The grain is decreased at AFM results (not shown here) and the surface is smooth [13]. This changed structure is thought to affect on turn-on voltage and diode characteristics.

Table 5.2. Summary of the diode characteristics with saturation current density, turn-on voltage, series resistance, ideality factor, forward current/reverse current ratio at \pm 5 V and barrier height.

	$J_s~({ m A/cm}^2)$	Turn-on	$r_s(\Omega)$	n	I_F/I_R [± 5 V]	Φ_b (eV)
		voltage (V)				
un-doped	5.59×10^{-5}	1.8	99	5.95	3.2×10^3	0.63
ZnO						
In 0.6 at. %	9.15×10^{-7}	2.4	97	3.65	1.4×10^{5}	0.73
In 1 at. %	8.58×10^{-6}	4.6	46	7.31	4.7×10^5	0.68
In 5 at. %	7.45×10^{-6}	4.2	37	7.28	1.7×10^{6}	0.69
In 10 at. %	8.52×10^{-6}	4.4	59	9.59	2.5×10^6	0.68

5.3 Conclusion

We study the effect of indium (In) doping (0.6, 1, 5, and 10 at. %) on diode characteristics with hetero structure of indium doped–ZnO films on the p–Si (111) substrate. The In–doped ZnO was deposited by using applicable and hetero junction diode was made by using a photolithography method with a lift–off method. The electrical properties of In–doped ZnO films were changed to increase the carrier concentration up to 3.0 × 10^{19} and to decrease resistivity up to the 1.5×10^{-2} Ω ·cm. Also, the diode characteristics were considerably change by the effect of In–doping. Especially, In–doped ZnO/p–Si diodes show very low reverse current density about 2.8×10^{-6} A/cm² (In10 at.%) at –5 V and high on–off ratio (In 10 at.%) about 2.5×10^{-6} at ±5 V. The hetero structure diode exhibited typical current–voltage behaviors with turn–on voltages of 1.8×4.6 V and with series resistance of 37×99 Ω .

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Chapter 6. Summary and Conclusions

ZnO films were deposited on the p–Si(111) substrate by using a sputter system and a PLD system. First result is controlled electron and hole concentration. As ZnO annealed in the Air and N_2 ambient, the electron carrier concentration has different concentration and its values are high 10^{16} and low 10^{18} /cm³, respectively. It was also found that electron concentration of the In–doped ZnO film was increased from $^{\sim}10^{17}$ to $^{\sim}10^{19}$ /cm³ by increased indium dopant concentration. We verified the different hole carrier concentration by using a differently doping silicon substrate (p $^{+}$ –Si and p–Si) and its values were $^{\sim}10^{15}$ and $^{\sim}10^{19}$ /cm³, respectively. Second result is clear ohmic contact characteristics at n–ZnO and p–Si materials by using Ti [15 nm]/Au [50 nm] materials. Third result is diode characteristics of n–ZnO/p–Si hetero junction structure. The diode parameter is shown in table 6.1. The turn on voltage is from 1.8 $^{\sim}$ 4.6 V and the series resitance is from 37 $^{\sim}$ 330 $^{\circ}$ 2. The lowest on–off ratio at $^{\pm}$ 5 V is 1.0 x $^{\circ}10^{19}$.

Table 6.1 Summary of the diode characteristics with saturation current density, turn-on voltage, series resistance, ideality factor, forward current/reverse current ratio at \pm 5 V and barrier height.

Annealing	Substrate	Js (A/cm ²)	$r_s(\Omega)$	n	Φ_b (eV)	Turn on	I_F/I_R (at \pm
	(Ω·cm)					voltage (V)	5 V)
N ₂	p-Si (0.005)	2.7 x 10 ⁻⁸	217	4.91	0.82	2.7	1.4 x 10 ⁶
	p-Si (10)	1.5 x 10 ⁻⁸	215	1.37	0.83	2.5	1.0 x 10 ⁶
Air	p-Si (0.005)	1.1 x 10 ⁻⁵	258	4.91	0.66	2.3	3.3×10^5
	p-Si (10)	5.1 x 10 ⁻⁷	330	7.99	0.74	2.6	3.4×10^3

In doping concentration	Js (A/cm ²)	A THANK	William Control of the Control of th	Ф («V)	Turn on	I_F/I_R (at \pm
(at. %)	JS (A/cm)	$\dot{r}_{s}(\Omega)$	n	Φ_{b} (eV)	voltage (V)	5 V)
as dep.	5.59 × 10 ⁻⁵	99	5.95	0.63	1.8	3.2×10^{3}
0.6	9.15×10^{-7}	97	3.65	0.73	24	1.4×10^5
1	8.58×10^{-6}	46	7.31	0.68	4.6	4.7×10^5
5	7.45×10^{-6}	37	7.28	0.69	4.2	$1.7~\times~10^6$
10	8.52×10^{-6}	59	9.59	0.68	4.4	$2.5~\times~10^6$

Fourth result is emission characteristics of n-ZnO/p-Si heterojunction diode. All devices was shown yellowish light at forward bias. However, a intensity of emitting light is so weak that we can't measure optical characteristics.

감사의 글

어느 듯 시간은 흘러 석사생활 2년을 마무리하는 이 순간까지 오게 되었습니다. 이 교정과 함께 한지 벌써 6년이라는 긴 시간 동안 많은 사람과 함께 하였고, 때로는 어려운 일, 때로는 즐거운 일, 다 같이 고생한 일, 함께 기뻐했던 일들을 가슴 깊숙이 추억으로 남게 되었습니다. 이 순간까지 많은 사람에게 도움을 받아왔기에, 부족한 저를 지금까지 있게 해주신 많은 분께 감사의 글을 남기고 싶습니다.

불현듯 다가온 행운이라는 표현이 어울리듯이, 좀 더 공부를 갈망하던 시기에 혼쾌히 부족한 저를 받아 주시고, 연구할 수 있게 해주신 김홍승 교수님께 감사드립니다. 항상 연구에 열정적인 모습, 다른 사람들을 편하게 대해 주시는 모습, 어떤 태도로 문제에 접근하시며 해결해 가시는 모습들을 보면서 많은 점을 배울 수 있었고, 제 인생에 새로운 가치관을 심어 주셔서 너무나 감사드립니다. 또한, 논문지도 및 연구방향에 대해 너무나 잘지도 해 주셔서 감사드립니다. 사랑합니다. 교수님. 또한, 학과 공부에 열의를 갖게 해주신 이삼녕 교수님, 안형수 교수님, 장지호 교수님께 감사드립니다. 바쁜신 와중에도 저의 부족한 논문을 심사해주신 양민 교수님, 장낙원 교수님 감사드립니다. 같은 프로젝트를 하면서 많은 도움을 주신 성균관대 조형균 교수님, 경북대 이호성교수님, 전남대 김진혁 교수님께 감사드립니다. 부산대 조채룡 교수님, 인제대 류혁현교수님께 감사드립니다. 또한, 동의대 이원재 교수님께 감사드립니다.

3년이라는 긴 시간 동안 함께 동고동락 한 저희 DMD Lab. 연구실 구성원들에게 고마움을 표합니다. 3년이라는 긴 시간 동안 많이 부족한 저를 도와주시고, 챙겨 주신이주영 선배에게 감사드립니다. 너무나 다르지만 서로 하나씩 맞춰 가면서 서로 도움이된 준제야 고맙다. 항상 부족한 선배지만 많이 도와준 보라, 준용, 아라, 다정아 고마워. 연구실 선배로서 많이 격려 주신 명훈 선배, 은수, 재현 선배에게도 감사드립니다. 같이

공동연구하면서 측정 많이 도와준 성균관대 보현 형, 원석 형, 영이 누나, 동찬 형에게 감사드립니다. 항상 유쾌하신 경북대 준호 형, 진영 씨, 형훈이에게 감사드립니다. 또한, 전자과 효성, 지훈이에게 감사드립니다.

같은 석사 생활하면서 많은 추억을 쌓은 동기들에게 감사드립니다. 석사 생활 외롭지 않게 함께 보내준 진영이, 영훈이, 시영이, 승준이, 해용이, 은주에게 감사드립니다. 또한, 연구생활 하면서 많은 도움 준 헌수형, 아름이, 민정이 에게 감사드립니다.

지금까지 저를 있게 해 주신 너무나 사랑하는 가족. 항상 저를 믿어 주시고, 도움 주신 아버지, 어머니께 이 논문을 받칩니다. 사랑하는 누나 너무나 고마워.

언급하지 못한 많은 너무나 많은 사람이 있습니다. 그분들께도 감사드립니다. 지나온 시간 동안 함께한 많은 사람이 있었습니다. 항상 건강하시고 행복하시길 바랍니다. 이제 어느덧 09년 마지막 12월입니다. 하지만, 다가올 새해가 있기에 마지막에만 머무를 수는 없는 듯합니다. 제 인생에 또 다른 시작을 위해 다시 시작하는 마음으로 처음에 가졌던 가슴 뜨거운 마음으로 다시 나아가도록 하겠습니다.

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A. International Journal Publication (SCI)

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C. International Conference Presentations

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D. Domestic Conference Presentations

- 1. **J. H. Lee**, J. Y. Lee, J. J. Kim, B. L. Jang, H. S. Kim, N. W. Chang, H. K. Cho, H. S. Lee, "Thermal annealing effect on diode characteristics of n-ZnO/p-Si(111)", The 4th Symposium on Ferroelectricity, Muju Korea 17-19 February (2008).
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Appendix

This appendix excerpted from S. M. Sze, Kwok K. Ng, "Physice of Semiconductor Devices 3ed", (Wiley-Interscience, New Jersey, 2007), p. 90–95.

At thermal equilibrium this relation is given by

$$n = n_i \exp(\frac{E_F - E_i}{kT}) \tag{1}$$

$$p = n_i \exp\left(\frac{E_i - E_F}{kT}\right) \tag{2}$$

We consider an abrupt p-n junction with a donor concentration of N_d and an accepter concentration of N_A . All dopants are assumed to be fully ionized so that the free electron and free hole concentration are given by

$$n_{no} = N_D = N_C \exp\left(-\frac{E_C - E_F}{kT}\right) = n_i \exp\left(\frac{E_F - E_i}{kT}\right)$$
(3)

$$p_{po} = N_A = N_V \exp(-\frac{E_F - E_V}{kT}) = n_i \exp(\frac{E_i - E_F}{kT})$$
 (4)

Obviously, at thermal equilibrium, the pn product from the above equation is equal to n_i^2 . When voltage is applied, the minority-carrier densities on both sides of the junction are changed, and the pn product is no longer equal to n_i^2 . We shall now define the quasi-Fermi levels as follows

$$n = n_i \exp(\frac{E_{Fn} - E_i}{kT}),\tag{5}$$

$$p = n_i \exp(\frac{E_i - E_{Fp}}{kT}),\tag{6}$$

where E_{Fn} and E_{Fp} are the quasi-Fermi levels. From Eqs. (5) and (6) we obtain

$$E_{Fn} \equiv E_i + kT \ln(\frac{n}{n_i}) \tag{7}$$

$$E_{Fp} \equiv E_i - kT \ln(\frac{p}{n_i}) \tag{8}$$

From Eqs. (5) and (6), pn is given by

$$pn = n_i^2 \exp\left(\frac{E_{Fn} - E_{Fp}}{kT}\right) \tag{9}$$

For a forward bias, $(E_{Fn}-E_{Fp})>0$ and $pn>n_i^2$; For a reverse bias, $(E_{Fn}-E_{Fp})<0$ and $pn< n_i^2$

Here we have to know the current-density equation and it is given by

$$J_n = q\mu_n nE + qD_n \nabla n, \tag{10}$$

$$J_p = q\mu_p p E - q D_p \nabla p, \tag{11}$$

The values of total current density is

$$J = J_n + J_p \tag{12}$$

where μ_n and μ_p are the electron mobilities and hole mobilities. The D_n and D_p are carrier diffusion constant. Eqs. (10) and (11) reduced by the Einstein relation Eq. (13), (14), (5), and (6). It is shown Eq. (15) and (16).

$$D_n = (\frac{kT}{g})\mu_n$$
; Einstein relation, (13)

$$E \equiv \frac{\nabla E_i}{q} \tag{14}$$

$$J_n = q\mu_n nE + qD_n \nabla n = \mu_n n \nabla E_i + \mu_n kT \nabla n$$

$$= \mu_n n \nabla E_i + \mu_n k T \left[\frac{n}{kT} (\nabla E_{Fn} - \nabla E_i) \right] = \mu_n n \nabla E_{Fn}$$
(15)

$$J_p = q\mu_p pE - qD_p \nabla p = \mu_p p \nabla E_i - \mu_p k \, T \nabla p$$

$$=\mu_{p}p\nabla E_{i}-\mu_{p}kT[\frac{p}{kT}(\nabla E_{i}-\nabla E_{Fp})]=\mu_{p}p\nabla E_{Fp} \tag{16}$$

It follows that within the depletion region,

$$qV = E_{Fn} - E_{Fp} \tag{17}$$

Equation (9) and (17) can be combined to give electron density and hole density at the boundary of the depletion-layer region on the p-side ($x = -W_{Dp}$) and n-side ($x = W_{Dn}$); where $p_p \approx p_{po}$ for low-level injection, and n_{po} is the equilibrium electron density on the p-side

$$n_p(-W_{Dp}) = \frac{n_i^2}{p_p} \exp(\frac{qV}{kT}) \approx n_{po} \exp(\frac{qV}{kT})$$
(18)

$$p_n(-W_{Dn}) \approx p_{no} \exp(\frac{qV}{kT})$$
 (19)

at $x = W_{Dn}$ for the n-type boundart. The preceding equation are the most-important boundary conditions for the ideal current-voltage equation. Form the continuity equation we obtain for the steady-state condition in the n-side of the junction

$$-U + \mu_n E \frac{dn_n}{dx} + \mu_p n_n \frac{dE}{dx} + D_n \frac{d^2 n_n}{dx^2} = 0$$
 (20)

$$-U + \mu_p E \frac{dp_n}{dx} + \mu_p p_n \frac{dE}{dx} + D_p \frac{d^2 p_n}{dx^2} = 0$$
 (21)

In these equation, U is the net recombination rate. Note that due to charge neutrality, majority carriers need to adjust their concentrations suck that

 $(n_n - n_{no}) = (p_{n-p_{no}})$. It also follows that $\frac{dn_n}{dx} = \frac{dp_n}{dx}$. Multiplying Eq. (20) by $\mu_p p_n$

and Eq. (21) by $\mu_n n_n$ and combining with the Einstein relation $D = \frac{kT}{q} \mu$, we obtain

$$-\frac{p_n - p_{no}}{\tau_n} - \frac{n_n - p_n}{(n_n/\mu_n) + (p_n/\mu_n)} \frac{Edp_n}{dx} + D_a \frac{d^2p_n}{dx^2} = 0$$
 (22)

where
$$D_a = \frac{n_n + p_n}{n_n/D_p + p_n/D_n}$$
 (23)

is the ambipolar diffusion coefficient, and

$$\tau_p \equiv \frac{p_n - p_{no}}{U} \tag{24}$$

From the low-injection assumption $[p_n \ll (n_n \approx n_{no})]$ in the *n*-type semiconductor, Eq. (22) reduces to

$$-\frac{p_n - p_{no}}{\tau_n} - \mu_p E \frac{dp_n}{dx} + D_p \frac{d^2 p_n}{dx^2} = 0$$
 (25)

which is Eq. (21) except that the term $\frac{\mu_p p_n dE}{dx}$ is ignored under low-injection assumption. In the neutral region where there is no electric field, Eq. (25) further reduces to

$$\frac{d^2 p_n}{dx^2} - \frac{p_n - p_{no}}{D_p \tau_p} = 0 {26}$$

The solution of Eq. (26), with the boundary conditions of Eq. (19) and $p_n(x=\infty)=p_{no}, \mbox{ gives}$

$$p_n(x) - p_{no} = p_{no} \left[\exp\left(\frac{qV}{kT}\right) - 1 \right] \exp\left(-\frac{x - W_{Dn}}{L_p}\right)$$
 (27)

where

$$L_p (\equiv \sqrt{D_p \tau_p}) \tag{28}$$

At $x = W_{dn}$, the hole diffusion current is

$$J_{p} = -qD_{p}\frac{dp_{n}}{dx}|_{W_{D_{n}}} = \frac{qD_{p}p_{no}}{L_{p}}[\exp(\frac{qV}{kT}) - 1]$$
(29)

$$J_{n} = qD_{n}\frac{dn_{p}}{dx}|_{-W_{D_{p}}} = \frac{qD_{n}n_{po}}{L_{n}}[\exp(\frac{qV}{kT}) - 1] \tag{30}$$

The total current is given by

$$J\!=J_n+J_p=(q\frac{D_nn_{po}}{L_n}\!+q\frac{D_pp_{no}}{L_p})[\exp(\frac{q\,V}{k\,T})\!-\!1]$$

$$=(\frac{qD_{n}}{L_{n}N_{A}}+\frac{qD_{p}}{L_{n}N_{D}})n_{i}^{2}[\exp(\frac{qV}{kT})-1]=J_{o}[\exp(\frac{qV}{kT})-1] \tag{31}$$