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Modeling, Control and Experimental Investigation of a Novel DSTATCOM Based on Cascaded H-bridge Multilevel Inverter

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Original scientific paper

A novel static synchronous compensator for reactive power compensation of distribution system (DSTATCOM) is proposed, based on the cascaded H-bridge multilevel inverter configuration. The mathematical formulation of the multilevel DSTATCOM is presented using state-space representations. A new software phase-locked loop (SPLL) is presented for grid synchronization and the obtained phase angle of the fundamental component of the grid voltage is utilized for deriving the active and reactive power balancing equations of the multilevel DSTATCOM. The proportional-resonant (PR) controller scheme is adopted for the current tracking control of the inverter, and the average dc-link voltage is controlled using a proportional-integral (PI) controller to regulate the active power flow of the DSTATCOM. Besides, the voltage balancing (VB) control among individual H-bridges is achieved by using separate PI regulators to control the difference voltage between the individual dc-link voltage and the average dc-link voltage. The validity of the proposed multilevel DSTATCOM and its control strategies is substantially confirmed by the extensive simulation results and the experimental results from the prototype system.

Key words: Multilevel, Cascaded H-bridge, DSTATCOM, Phase-locked loop (PLL), Voltage balancing

Modeliranje, upravljanje i eksperimentalno istraživanje novoga raspodijeljenog statičkog kompenzatora jalove snage zasnovanog na višestupanjskom pretvaraču s ulančenim H-mostovima. Predložen je novi statički sinkroni kompenzator za kompenzaciju jalove snage distribucijskog sustava (DSTATCOM) zasnovan na konfiguraciji višestupanjskog pretvarača s ulančenim H-mostovima. Matematički model višerazinskog DSTATCOM-a prikazan je u prostoru stanja. Predstavljena je nova programski izvedena petlja sa zaključanom fazom namijenjena sinkronizaciji s mrežom, a dobiveni fazni kut osnovne komponente mrežnog napona koristi se za izvod jednadžbi ravnoteže aktivne i jalove snage višerazinskog DSTATCOM-a. Usvojen je koncept proporcionalno-rezonantnog regulatora za slijeđenje trajektorije struje pretvarača, a srednji napon istosmjernog međukruga upravlja se korištenjem proporcionalno-integracijskog (PI) regulatora u svrhu regulacije toka radne snage DSTATCOM-a. Osim toga, upravljanje uravnoteženjem napona među pojedinim H-mostovima ostvareno je korištenjem odvojenih PI regulatora za upravljanje razlikom napona među pojedinim istosmjernim međukrugovima te srednjim naponom istosmjernih međukrugova. Valjanost predloženog višestupanjskog DSTATCOM-a i primijenjenih upravljačkih strategija potvrđena je brojnim simulacijskim i eksperimentalnim rezultatima na prototipskoj izvedbi ovog sustava.

Ključne riječi: višestupanjski, ulančeni H-most, DSTATCOM, petlja sa zaključanom fazom (PLL), uravnoteženje napona

1 INTRODUCTION

In recent decades, the electric distribution systems are suffering from significant power quality (PQ) problems, which are characterized by low power factor, poor voltage profile, voltage fluctuations, voltage sag/swell, load unbalancing, and supply interruptions. These power quality issues have attracted attention to the researchers from both academy and industry. As a result, many power quality standards were proposed, such as the IEEE 519-1992, IEEE Std.141-1993, IEEE Std.1159-1995 and IEC 1000-3-2, etc. [1–4]. Among all forms of the power quality issues, the voltage fluctuations or sag/swell problems were recognized as the most costly events in the modern assembly lines and commercial offices [5–8]. On the other hand, the increasing power quality problems have stimulated a great potential for the industry to devise the power quality mitigation and compensation devices. For instance, the static synchronous compensator for the distribution system (DSTATCOM) was proposed in [5] to solve the voltage sag and flicker problems. In [6–8], new compensation schemes for the voltage flicker problem were presented and the combined compensation scheme based on the active power filter (APF) and switching capacitors was implemented in

a typical electrical distribution system for the automobile industry.

The DSTATCOMs and APFs share the same power-stage topologies, but differ in the control strategies and reference current generation schemes, as reported in [8–12]. Generally, the DSTATCOMs are designed to compensate fundamental frequency reactive power while the APFs compensate a wider spectrum which contains both fundamental reactive power and the harmonic components. Moreover, DSTATCOMs also have the capability for voltage regulation for the grid voltage at the common coupling point (PCC) by injecting or absorbing a certain amount of reactive power. Hence the DSTATCOMs received considerable attention due to the urgent requirement for tackling the voltage fluctuation problems [9–11].

To meet the requirement of the reactive compensation for high-power, medium-voltage electric distributions systems, the conventional three-phase three-wire or four-wire DSTATCOM topologies have evolved into the multilevel and multi-cell topologies [13–16]. In [13], the dc-link voltage equalization for the diode-clamped multilevel DSTATCOM was reported. The diode-clamped multilevel topology, however, shows poor capability for modular fabrication and the capacitor voltage balancing is rating complex. Moreover, it has deficiency for redundant operation of the power electronic switches. The cascaded H-bridge multilevel topology, on the other hand, shows much better modular capability, simple layout, excellent redundant operation ability and it can be extended to higher voltage levels by adding new H-bridge modules [14–16]. However, the dc-link voltage stabilization across the dc-link capacitors is not trivial due to the unequal power losses for the individual H-bridges and the limited precision for the gating signals. Therefore, this paper is aiming to present a detailed elaboration of the DSTATCOM based on the cascaded H-bridge multilevel inverter, which includes the mathematical formulation, grid-synchronization, current tracking and the dc-link voltage balancing schemes.

This paper is organized as follows: The mathematical formulation of the multilevel DSTATCOM is presented in Section 2. The control strategies are presented in Section 3, where a novel software phase-locked loop (SPLL), the current tracking schemes and the dc-link voltage balancing scheme will be discussed in detail. In Section 4 the simulation results are presented to test the performance of the proposed system. In Section 5 the extensive experimental results obtained from the laboratory prototype system are presented to validate the theoretical analysis and the simulation results. Finally, Section 6 concludes this paper.

2 MATHEMATICAL MODELLING

Figure 1 shows the circuit diagram of the seven-level cascaded multilevel DSTATCOM based on three H-bridge

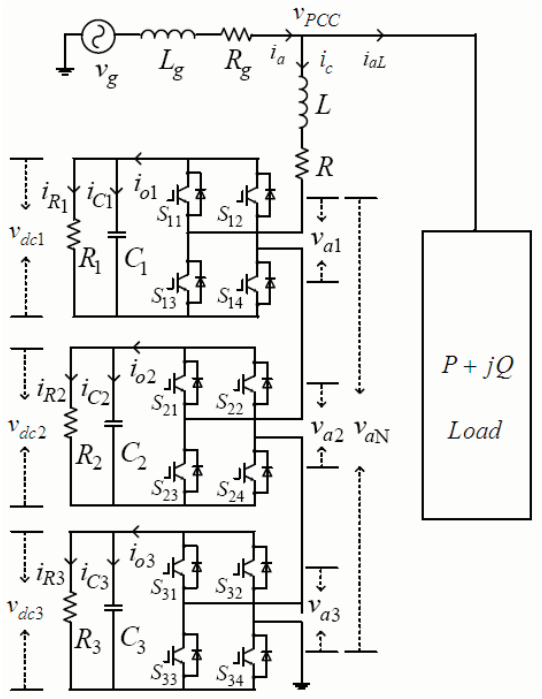


Fig. 1. The schematic of the proposed DSTATCOM based on cascaded H-bridge multilevel inverter

modules. It can be observed that each H-bridge includes four IGBT switches with anti-parallel diodes and a dc-link capacitor. The output voltages of the cascaded H-bridge inverter can be derived as [12]:

$$v_{aN} = v_{a1} + v_{a2} + v_{a3}. \tag{1}$$

Assuming $v_{dc1} = v_{dc2} = v_{dc3} = V_{dc}$ in the steady state conditions and the unipolar modulation scheme is adopted in the PWM process, then each H-bridge module can produce three different voltage levels: $-V_{dc}$, 0, V_{dc}. With reference to the upper bridge, it is possible to set $v_{a1} = +V_{dc}$ by turning on power switches S_{11} and S_{14} and $v_{a1} = -V_{dc}$ by turning on power switches S_{12} and S_{13}. Moreover, it is possible to set $v_{a1} = 0$ by turning on either S_{11} and S_{12} or S_{13} and S_{14}, the lower bridge operates in a similar manner. Therefore, seven distinct voltage levels can be synthesized at the ac terminals. It should be noted that the switching states of S_{x1}, S_{x2} $(x = 1, 2, 3)$ must be complementary to those of S_{x3}, S_{x4} $(x = 1, 2, 3)$ in order to avoid short circuit of the H-bridge. To derive the state-space equations for the multilevel DSTATCOM, the switching functions are defined for individual H-bridges, as denoted by:

$$\begin{cases} f_1 = S_{11} \cdot S_{14} - S_{12} \cdot S_{13}, \\ f_2 = S_{21} \cdot S_{24} - S_{22} \cdot S_{23}, \\ f_3 = S_{31} \cdot S_{34} - S_{32} \cdot S_{33}. \end{cases} \quad (2)$$

The value of f_x ($x = 1, 2, 3$) indicates the dynamic process of charging and discharging between the dc-link capacitors C_1, C_2 and C_3. Supposing the DSTATCOM current i_c is positive, then the capacitor C_x ($x = 1, 2, 3$) is charging if $f_x = 1$, discharging if $f_x = -1$, and not undergoing any of these processes if $f_x = 0$. Complementary phenomenon appears if the inverter current is negative. The following assumptions are made for deriving the mathematical model of the cascaded H-bridge inverters.

a) The grid is assumed to be AC current source;

b) The power losses of the whole system are categorized as series loss and parallel loss. The series loss and interfacing inductor loss are represented as equivalent series resistance (ESR). Parallel losses are represented as shunt connected resistances across the dc-link capacitors, corresponding to the active power loss of the H-bridge, including blocking loss, capacitor loss and absorbing circuit loss, etc.

The differential equation describing the dynamics of the coupling inductor between the cascaded H-bridge inverter and the grid can be derived as:

$$v_{PCC} = Ri_c + L\frac{di_c}{dt} + f_1 v_{dc1} + f_2 v_{dc2} + f_3 v_{dc3}, \quad (3)$$

where the variable v_{PCC} represents grid voltage at the point of common coupling (PCC), L represents the inductance of the coupling inductor and R represents the equivalent series resistance (ESR). The variables v_{dc1}, v_{dc2} and v_{dc3} are actual voltages across the dc-link capacitors of the cascaded H-bridge inverter, which may not equal to the reference voltage V_{dc} during dynamic process. According to the Kirchhoff's law, the currents flowing into the dc-link capacitors C_1, C_2 and C_3 can be expressed as:

$$\begin{cases} i_{c1} = C_1\frac{dv_{dc1}}{dt} = i_{o1} - i_{R1} = f_1 i_c - \frac{v_{dc1}}{R_1}, \\ i_{c2} = C_2\frac{dv_{dc2}}{dt} = i_{o2} - i_{R2} = f_2 i_c - \frac{v_{dc2}}{R_2}, \\ i_{c3} = C_3\frac{dv_{dc3}}{dt} = i_{o3} - i_{R3} = f_3 i_c - \frac{v_{dc3}}{R_3}, \end{cases} \quad (4)$$

where R_1, R_2 and R_3 are the equivalent resistance of each H-bridges, representing the parallel losses. The variables i_{o1}, i_{o2} and i_{o3} represent the total dc-link current and i_{R1}, i_{R2} and i_{R3} represent the current in the dc-link resistance of the individual H-bridge module. The Eqs.(3)-(4) can be rearranged as:

$$\begin{cases} \frac{di_c}{dt} = \frac{v_{PCC}}{L} - \frac{R}{L}i_c - \frac{f_1 v_{dc1}}{L} - \frac{f_2 v_{dc2}}{L} - \frac{f_3 v_{dc3}}{L}, \\ \frac{dv_{dc1}}{dt} = \frac{f_1 i_c}{C_1} - \frac{v_{dc1}}{R_1 C_1}, \\ \frac{dv_{dc2}}{dt} = \frac{f_2 i_c}{C_2} - \frac{v_{dc2}}{R_2 C_2}, \\ \frac{dv_{dc3}}{dt} = \frac{f_3 i_c}{C_3} - \frac{v_{dc3}}{R_3 C_3}. \end{cases} \quad (5)$$

Let the vector of state variables be denoted with $X_3 = [i_c \ v_{dc1} \ v_{dc2} \ v_{dc3}]^\top$ and the input vector with $U_3 = [v_{PCC} \ 0 \ 0 \ 0]^\top$. Then (5) can be expressed in compact matrix form:

$$\dot{X}_3 = A_3 X_3 + B_3 U_3. \quad (6)$$

The matrices A_3 and B_3 can be simply derived as:

$$A_3 = \begin{bmatrix} -\frac{R}{L} & -\frac{f_1}{L} & -\frac{f_2}{L} & -\frac{f_3}{L} \\ \frac{f_1}{C_1} & -\frac{1}{R_1 C_1} & 0 & 0 \\ \frac{f_2}{C_2} & 0 & -\frac{1}{R_2 C_2} & 0 \\ \frac{f_3}{C_3} & 0 & 0 & -\frac{1}{R_3 C_3} \end{bmatrix},$$

$$B_3 = \begin{bmatrix} \frac{1}{L} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}.$$

3 CONTROL STRATEGIES

Figure 2 shows the controller architecture for the proposed multilevel DSTATCOM, which is based on the floating-point digital signal processor (DSP) and the field programmable gate array (FPGA) hardware platforms. A detailed discussion of this hardware architecture will be delivered in Section 5. This section briefly outlines the control strategies of the multilevel DSTATCOM, which includes the grid-synchronization using the software phase-locked loop (SPLL), the current tracking scheme and the voltage balancing (VB) control strategies, as illustrated in Fig. 3.

3.1 Software phase-locked loop (SPLL)

Accurate synchronization of the multilevel DSTATCOM to the grid is of vital importance to ensure its stable operation since the phase angle of the grid voltage is used to derive the active and reactive power balancing equations for the DSTATCOM. Figure 4 shows the schematic of the proposed software phase-locked loop (SPLL) for grid synchronization based on the least-mean square (LMS) estimation algorithm [17]. Here the mathematical formulation of the SPLL is briefly outlined. An arbitrary grid voltage can be represented as:

$$v_{sa}(t) = V_1 \sin(\omega_0 t + \phi_1) + \sum_{n=2}^{N} V_n \sin(n\omega_0 t + \phi_n), \quad (7)$$

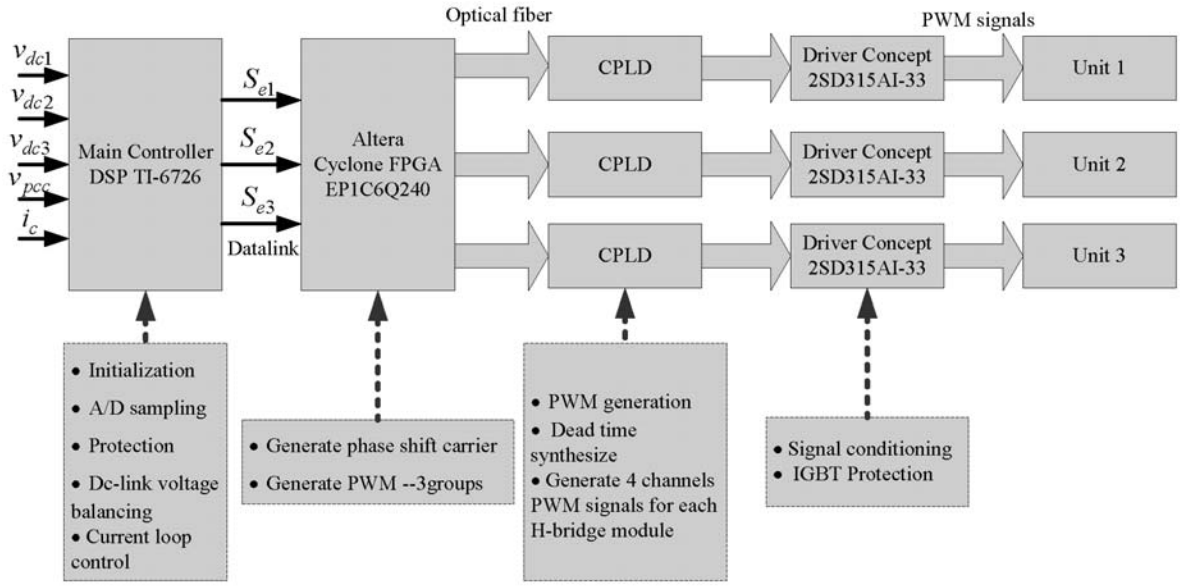


Fig. 2. Proposed controller architecture for the multilevel DSTATCOM

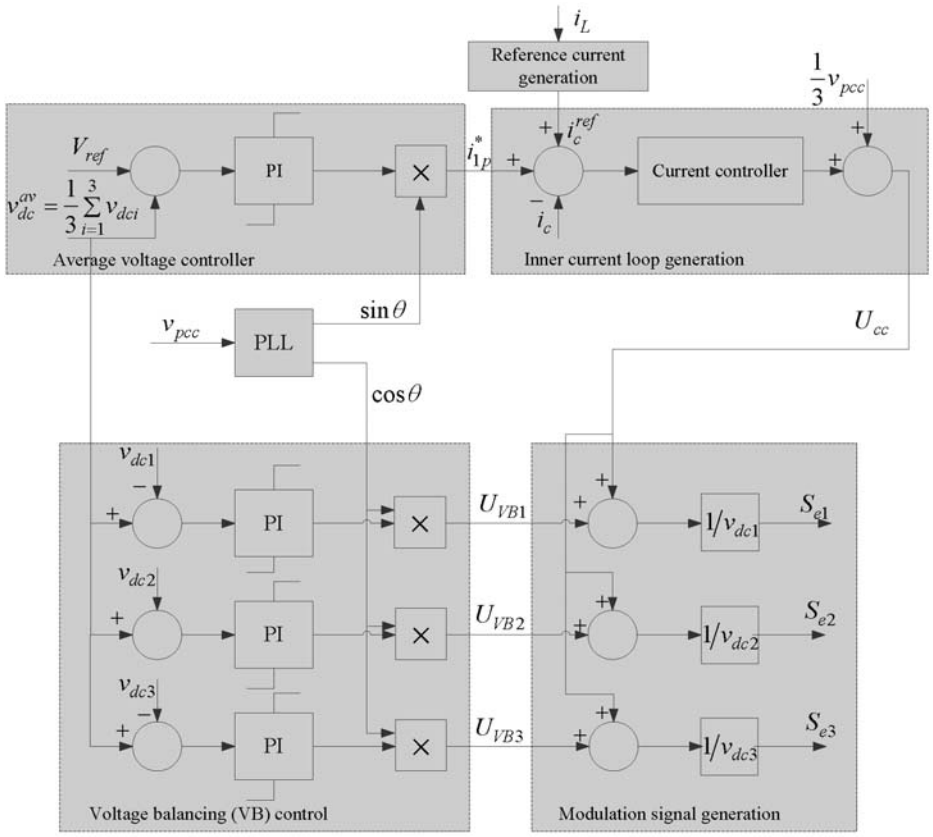


Fig. 3. Control strategies for the DSTATCOM implemented in the digital signal processor (DSP)

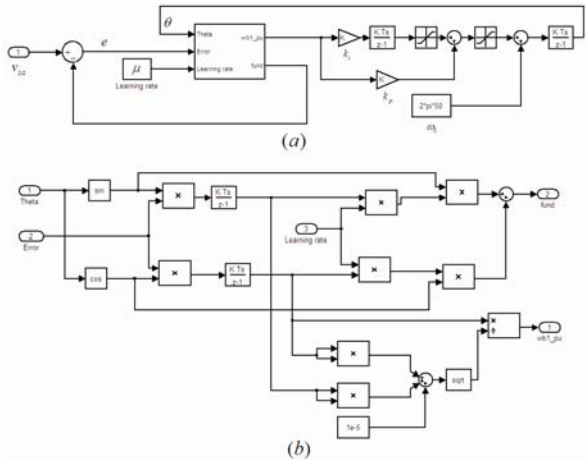


Fig. 4. Diagram of the single-phase software phase-locked loop (SPLL) for grid synchronization

where φ_1 and φ_n are the initial phase angle of the fundamental and the nth order harmonic component, respectively. Here the DC offset is neglected for the sake of brevity. The phase angle of the fundamental component voltage can be expressed as:

$$\phi_1 = \Delta\theta_1 + \theta_1, \tag{8}$$

where θ_1 and $\Delta\theta_1$ represent the estimated phase angle of the fundamental grid voltage and the estimation error, respectively, obtained from the SPLL. Therefore, substituting (8) back to (7), we get:

$$\begin{aligned} &v_{sa}(t) = V_1\cos(\Delta\theta_1)\sin(\omega_0 t + \theta_1) + \\ &V_1\sin(\Delta\theta_1)\cos(\omega_0 t + \theta_1) + \textstyle\sum_{n=2}^{N} V_n \sin(n\omega_0 t + \phi_n). \end{aligned} \tag{9}$$

From Equation (9), it can be deduced that the fundamental component of the original signal can be regenerated by adjusting coefficients $V_1\cos(\Delta\theta_1)$, $V_1\sin(\Delta\theta_1)$, even though the phase angle of the original signal is unknown. The objective of the proposed SPLL is to reconstruct the phase angle of the fundamental grid voltage φ_1 using the least mean square (LMS) algorithm [17–19]. Therefore, the fundamental grid voltage can be expressed by the inner product of two vectors, namely, the vector of trigonometric functions and the vector of weights in the LMS-based weights updating algorithm [17, 19]. The weight vector W denotes the coefficients of the corresponding trigonometric functions. From the aforementioned definition, the fundamental grid voltage can be expressed as:

$$\hat{Y} = W^T X, \tag{10}$$

where $\hat{Y}$ is the estimated output of the fundamental grid voltage by using the LMS-based weights estimation scheme. The vector W and X corresponding to the weight vector and the input vector, respectively, are represented as:

$$\begin{cases} W = [V_1\cos(\Delta\theta_1),\ V_1\sin(\Delta\theta_1)] = [\omega_{a1},\ \omega_{b1}], \\ X = [\sin(\omega_0 t + \theta_1),\ \cos(\omega_0 t + \theta_1)]^T. \end{cases} \tag{11}$$

The weights updating process of the proposed SPLL is similar to the adaptive linear neural network (ADALINE) in [18, 19], which was based on the recursively searching the optimal point of the quadratic cost function, defined by the least-mean square (LMS) error of the harmonic estimation algorithm. It is worth noting that the salient difference between the ADALINE scheme and the proposed SPLL algorithm is that, the frequency and phase angle signals utilized in the LMS weights updating process were assumed to be constant. However, in case of the SPLL, the frequency and phase angle of the fundamental grid voltage is recursively updated by the loop filter (LF) and voltage controlled oscillator (VCO) of the PLL, denoted by the proportional-integral (PI) controller and the discrete integrator in Fig. 4a, respectively. In other words, the LMS-based weights updating procedure is utilized as the phase detector (PD) for the PLL, denoted in Fig. 4b, which generate the error signal to drive the loop filter (LF) and voltage controlled oscillator (VCO), according to the initial definition of PLL. The graphical interpretation of the proposed SPLL is shown in Fig. 4. It can be observed that the proposed SPLL resembles the existing PLLs in terms of loop filter (LF) and voltage controlled oscillator (VCO) structures. However, the phase detector (PD) section of the conventional PLL is replaced by the LMS recursive weights updating algorithm of the grid voltage, as shown in Fig. 4b.

3.2 Current-loop control scheme

The system equation across the coupling inductance can be derived as:

$$v_{PCC} = v_{aN} + R\cdot i_c + L\cdot\frac{di_c}{dt}. \tag{12}$$

Applying Laplace transformation (s-domain transform) to (12), assuming $v_{dr} = v_{PCC} - v_{aN}$, the following equation can be obtained:

$$\frac{I_c(s)}{V_{dr}(s)} = \frac{1}{R + L\cdot s}. \tag{13}$$

Similar to the analysis adopted in [17], the inner current loop is depicted in Fig. 5. The open-loop transfer function for the current loop controller can be represented as:

$$G_{open}(s) = G_{cc}(s)\cdot\frac{1}{1 + T_d\cdot s}\cdot\frac{1}{R + L\cdot s}, \tag{14}$$

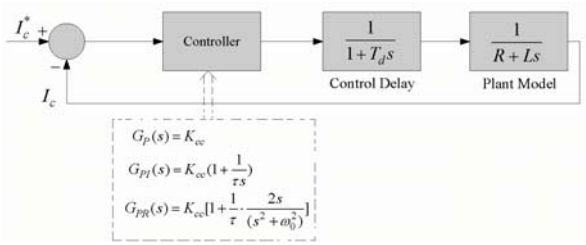


Fig. 5. Simplified block diagram for the current loop controller

where T_d denotes the control delay, and $G_{cc}(s)$ represents the transfer function of the current controller, which can be a proportional controller, proportional-integral (PI) controller, or proportional-resonant controller. The closed-loop transfer function for the current tracking control can be denoted as:

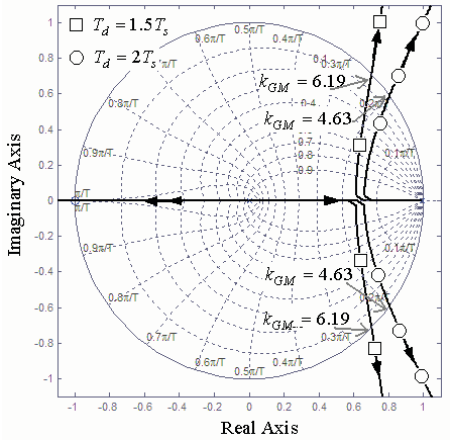
$$G_{close}(s) = \frac{G_{open}(s)}{1 + G_{open}(s)}. \tag{15}$$

Next, the current tracking performance is studied for the different regulators, namely, the P, PI and PR regulators.

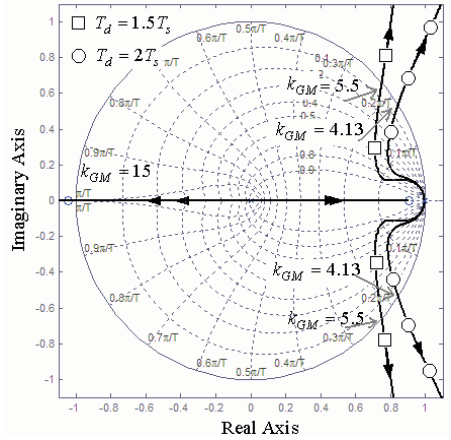
The proportional controller provides a simple solution for current tracking, assuming the control gain is K_{cc}, then the closed-loop transfer function for the P controller is derived as:

$$G^{P}_{close}(s) = \frac{K_{cc}}{(T_d \cdot L) \cdot s + (T_d \cdot R + L) + (R + K_{cc})}. \tag{16}$$

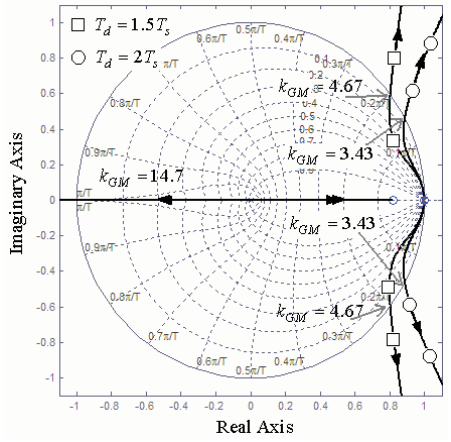
Figure 6 shows the closed-loop root locus of the current-loop controller under different regulators, namely, the P, PI and PR controllers. It can be observed from Fig. 6a that, when the proportional controller is used for current reference tracking, the maximum controller gains k_{GM} are 6.19 and 4.63 when $T_d = 1.5T_s$ and $T_d = 2T_s$, respectively. The critical gains in Fig. 6a impose the upper limit for the current loop regulator to ensure the closed-loop stability. Normally, a higher controller gain implies a faster dynamic response under transient disturbance of the current reference, but at the tradeoff of reduced stability margin. Therefore, if the P controller is selected for the multilevel DSTATCOM, a tradeoff must be reached between the dynamic response and closed-loop stability. For instance, the controller gain corresponding to the damping ratio $\xi = 0.707$ can be used for the practical system. It can also be observed from Fig. 6a that the control delay deteriorates the stability margin. Hence the delay due to the A/D sampling, computation of the control algorithm and PWM generation should be minimized to enhance the stability margin.



(a) With proportional (P) controller



(b) With proportional-integral (PI) controller



(c) With proportional-resonant (PR) controller

Fig. 6. Root locus analysis of the current-loop control scheme

The proportional-integral (PI) is a well-known regulator which is widely utilized for error tracking in grid-tie converter applications. Similar to the analysis of the P controller, the closed-loop transfer function for the current tracking control under the proportional-integral (PI) control is derived as:

$$G_{close}^{PI}(s) = \frac{K_{cc}(\tau s+1)}{\{(\tau T_d L)s^3 + (T_d R + L)\tau s^2 + \\ +(R+K_{cc})\tau s + K_{cc}\}}. \quad (17)$$

where the transfer function of the proportional-integral (PI) is represented as:

$$G_{PI}(s) = K_{cc}(1+\frac{1}{\tau s}). \quad (18)$$

The parameter τ represents time constant for the integrator of the PI regulator. Fig. 6b shows the root locus plot of the closed-loop current tracking scheme using PI regulator when the time constant is selected as $\tau = 10T_s$. It can be observed that the critical controller gains are 5.5 and 4.13, when the control delays are $T_d = 1.5T_s$ and $T_d = 2T_s$, respectively. Similar to the case of the P controller, the control delay also deteriorates the stability margin. The time constant (τ) of the PI regulator also shows a significant impact on the critical gains, smaller time constant implies faster integration, but at the tradeoff of reduced stability margin. On the other hand, higher time constant would result in sluggish integration, which relaxes the gain margin. The critical gains of the PI regulator under different time constants are listed in Table 1. It is worth noting that with the increase of the integration time constant, the critical gain also increases. Moreover, for the same integration time constant, longer control delays implies smaller stability margin.

The PI regulator shows unsatisfactory performance for current tracking in case of alternating reference signal, which results in remarkable phase and amplitude tracking errors. The proportional resonant (PR) current controller, on the other hand, achieves perfect tracking performance for the alternating reference signal, which mimics the PI regulator implemented in the synchronous rotating reference frame with the following transfer function:

$$G_{PR}(s) = K_{cc}[1 + \frac{1}{\tau}\cdot\frac{2s}{(s^2+\omega_0^2)}], \quad (19)$$

where the parameter τ is also defined as the time constant for the resonant controller, and ω_0 denotes the angular frequency of fundamental grid voltage. Hence the PR regulator achieves zero steady-state error for the alternating signal at ω_0 due to the infinite open-loop gain introduced by the PR current regulator. Substituting the equation (19) into the transfer function of the closed-loop current tracking scheme, we get:

$$G_{close}^{PR}(s) = \\ \frac{\tau K_{cc}s^2 + 2K_{cc}s + \tau K_{cc}\omega_0^2}{\{(\tau T_d L)s^4 + (T_d R+L)\tau s^3 + [(R+K_{cc})\tau + T_d L\omega_0]s^2 \\ +[(T_d R + L)\tau\omega_0^2 + 2K_{cc}]s + \tau\omega_0^2(R+K_{cc})\}}. \quad (20)$$

Fig. 6c shows the root locus plot of the closed-loop current tracking scheme using PR regulator when the time constant is selected as $\tau = 10T_s$. It can be observed that the critical controller gains are 4.67 and 3.43, when the control delays are $T_d = 1.5T_s$ and $T_d = 2T_s$, respectively. The same effect of the reduced stability margin to control delay can be noticed for the PR regulator, as shown in Table 1. Moreover, it is found that the time constant τ also shows similar impact on the stability margin as compared to the case of PI regulator.

Table 1. The critical gains (K_{GM}) obtained from the root locus analysis for the proportional-integral (PI) controller and proportional-resonant (PR) controller under different control delays (T_d)

Time constant (τ)	PI Controller		PR Controller	
	T_d=1.5T_s	T_d=2T_s	T_d=1.5T_s	T_d=2T_s
5T_s	4.77	3.37	2.19	0.68
8T_s	5.42	3.96	4.35	2.83
10T_s	5.5	4.13	4.67	3.43
20T_s	5.97	4.39	5.54	4.03
30T_s	6.05	4.69	6.03	4.41
50T_s	6.22	4.58	6.04	4.46
100T_s	6.23	4.56	6.05	4.55

Note: T_s represents the sampling time of the A/D channels.

3.3 Dc-link voltage balancing (VB) control strategy

In the previous section, the current tracking control scheme has been analyzed using root locus plots of the closed-loop transfer function. Another importance aspect for ensuring stable operation of the proposed multilevel DSTATCOM is the dc-link voltage balancing control strategy. It is well-know that the active and reactive power flow between the inverter and the grid depends on the magnitude and phase of the synthesized multilevel voltage v_{aN} with respect to the grid voltage v_{PCC}. The multilevel voltage v_{aN} is the sum of the output voltage of the individual H-bridge modules (Fig. 1). To better illustrate power flow of the multilevel inverter, the average output voltage for each H-bridge modules is denoted as:

$$v_{av} = \frac{1}{3}\sum_{i=1}^{3} v_{ai} = \frac{1}{3}v_{aN}. \quad (21)$$

Figure 7 shows the phasor representation of the output voltage waveform of each H-bridge module. The phase

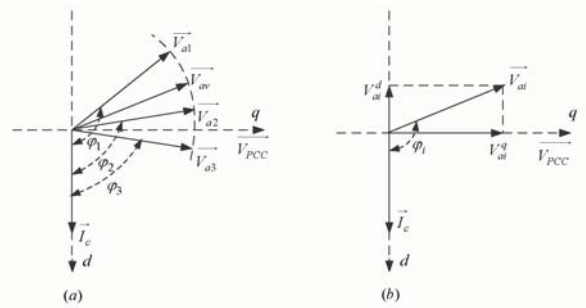


Fig. 7. Phasor representation of the individual H-bridge voltage with respect to its injection current

displacement of the grid voltage and the reactive current i_c is also illustrated. The active and reactive power delivered by the ith H-bridge to the grid can be represented as:

$$\begin{cases} P_i = V_{ai} \cdot I_c \cdot \cos\phi_i, \\ Q_i = V_{ai} \cdot I_c \cdot \sin\phi_i, \end{cases} \tag{22}$$

where φ_i represents the phase angle between the multilevel DSTATCOM current and the output voltage of each H-bridge module. It can be observed from the phasor diagram in Fig. 7a that the active and reactive power delivered by each module is proportional to the in-phase and orthogonal component of its output voltage with respect to the current. Fig. 7b shows the fictitious *d*-*q* reference frame which depicts the active and reactive component of the output voltage, denoted by the *d*- and *q*-axis component, respectively, which is a projection of the individual output voltage to the two axes. Hence the active and reactive powers loaded by the ith H-bridge module can be derived by:

$$\begin{cases} P_i = V_{ai}^d \cdot I_c, \\ Q_i = V_{ai}^q \cdot I_c. \end{cases} \tag{23}$$

It can be noticed from the above equation, that in order to equally distribute the reactive power among each H-bridge modules, the *q*-axis component of the output voltage v_{ai} $(i = 1, 2, 3)$ should be same. Nevertheless, the active power absorption by each H-bridge modules may not be identical to each other due to non-ideal dc-link parameters, such as IGBT or diodes conduction losses, which is reflected by the unequal *d*-axis projection of the output voltage v_{ai}. Therefore, the actual active power absorption by the ith H-bridge module can be rewritten in terms of the average output voltage v_{av}, as:

$$P_i = V_{ai}^d \cdot I_c = (V_{av}^d + \Delta V_{av}^d) \cdot I_c = P_{av} + \Delta P_i, \tag{24}$$

where P_{av} represents the average active power absorption of the H-bridge modules, and ΔP_i represents the difference between the individual active power and the average active power absorption. In order to achieve active power balance among the modules, the summation of the *d*-axis projections of output voltage of each H-bridge modules should be zero. In other words, once the total active power absorption of the multilevel DSTATCOM is obtained, the dc-link voltage balancing control scheme serves the purpose of equally distributing the reactive power among individual H-bridge modules by dynamically interchanging the active power among each modules. Followed by this principle, the control scheme is devised as shown in Fig. 3. It shows that the total active power absorption of the DSTATCOM is balanced by regulating the average dc-link voltage using a proportional-integral (PI) controller, and the output of the PI regulator is multiplied by a sine function synchronized with the grid using software phase-locked loop (SPLL), which is completely same as that of the conventional grid-connected converters. The voltage balancing (VB), on the other hand, is achieved by regulating individual dc-link voltage with respect to the average dc-link voltage in order to regulate the active power distribution among the H-bridge modules. The proportional-integral (PI) regulators are also used and the output of the PI regulators are multiplied with a cosine function synchronized with the grid voltage, which projects the control error to the orthogonal axis with respect to the grid voltage, i.e., the *d*-axis denoted by Fig. 7.

Once again referring to Fig. 3, it is worth noting that the PI regulators for the voltage balancing signals, denoted by U_{VB1}, U_{VB2}, U_{VB3}, can be simplified by substituting $U_{VB3} = -(U_{VB1} + U_{VB2})$ to reduce the computational load. After the voltage balancing signals are obtained, the total synthesized modulation signals can be derived as:

$$S_{ei} = \frac{1}{v_{dci}}(U_{VBi} + U_{cc}), \quad i = 1, 2, 3, \tag{25}$$

where U_{cc} represents the output signal of the current loop controller.

4 SIMULATION RESULTS

This section reports the simulation results of the proposed multilevel DSTATCOM under various operating conditions. The parameters of the power-stage and the controllers are listed in Tables 2 and 3, respectively. The sim-

Table 2. The specifications of the multilevel DSTATCOM

Coupling inductor (*L*)	500 μH
Dc-link Capacitor (*Cdc*)	2000 μF
Switching frequency of IGBT (f_{sw})	2.5 kHz
Sampling frequency (*fsample*)	15 kHz
Grid voltage at PCC (*vPCC*)	100 V (RMS)
Dc-link voltage reference (*Vdc*)	50 V

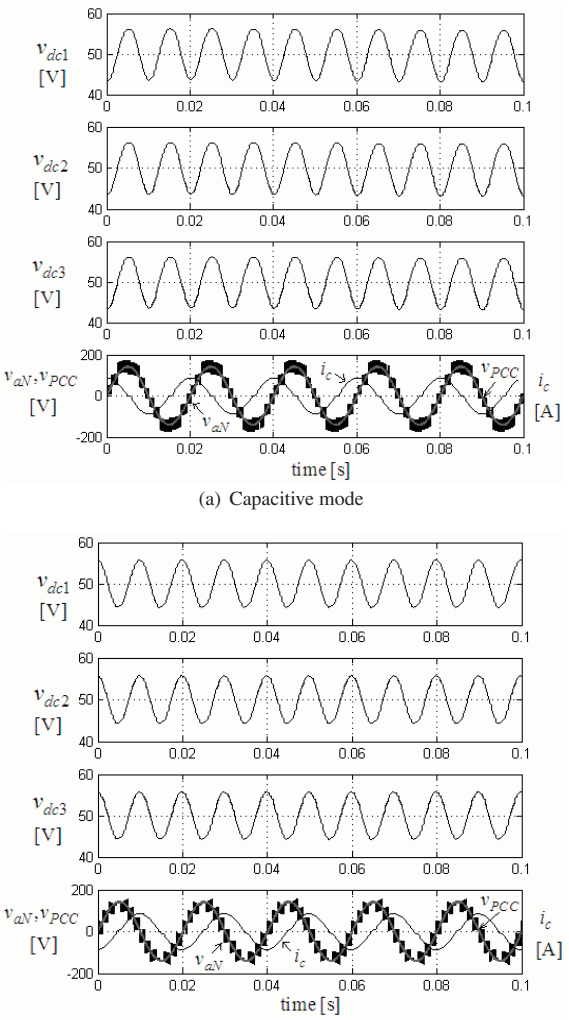
Table 3. The controller parameters for the multilevel DSTATCOM

Proportional gain of PR current regulator (K_{pcc})	2.5
Time constant of PR current regulator (τ_{cc})	$10T_s$
Proportional gain of average dc-voltage controller (K_{pdc1})	0.6
Time constant of average dc-voltage controller (τ_{dc1})	$1000T_s$
Proportional gain of voltage-balancing controller (K_{pdc2})	0.2
Time constant of voltage-balancing controller (τ_{dc2})	$2000T_s$

ulation results under ideal H-bridge modules and non-ideal modules are investigated. In case of the ideal H-bridge module scenarios, the same dc-link capacitors and equivalent power losses are assumed across the individual H-bridges. Besides, in case of non-ideal H-bridge modules, the 20% difference is considered for the dc-link capacitors and equivalent power losses are considered, i.e., the dc-link capacitors are 2000 μF, 2400 μF and 1600 μF for each module, respectively. In order to further investigate the performance of the multilevel DSTATCOM, the simulation results under different modulation indices are also provided.

Figure 8 shows the simulation results of the DSTATCOM for the capacitive and inductive operational modes under ideal H-bridge scenarios. Fig. 8a shows the simulation results of capacitive operation mode, i.e., the DSTATCOM generates leading reactive current with respect to the grid voltage at the point of common coupling. The individual dc-link voltages, the synthesized multilevel output voltage and the injection current of the DSTATOM are depicted in Fig. 8a.

It can be observed that the dc-link voltages are controlled to track the reference voltage, with a ripple of double fundamental frequency due to the reactive current generated by the system. The amplitude of the voltage ripples can be reduced if the higher value dc-link capacitors are adopted, or if the reference dc-link voltage is increased to higher voltage levels. Moreover, the synthesized output voltage v_{aN} shows excellent seven-level wave shape, as predicted in the theoretical analysis. The PCC voltage v_{PCC}, as denoted by the gray color in Fig. 8a, is almost in phase with the synthesized multilevel output voltage. Since the active power exchange between the multilevel DSTATCOM with the grid is determined by the phase angle difference between v_{PCC} and the fundamental component of the multilevel voltage, hence it can be noticed from Fig. 8a that the active power consumption of the DSTATCOM is very small. The compensating current i_c, is amplified by a factor of 5 for better illustration, and it shows an 90 degree leading the phase angle of the PCC voltage v_{PCC}.



(a) Capacitive mode

(b) Inductive mode

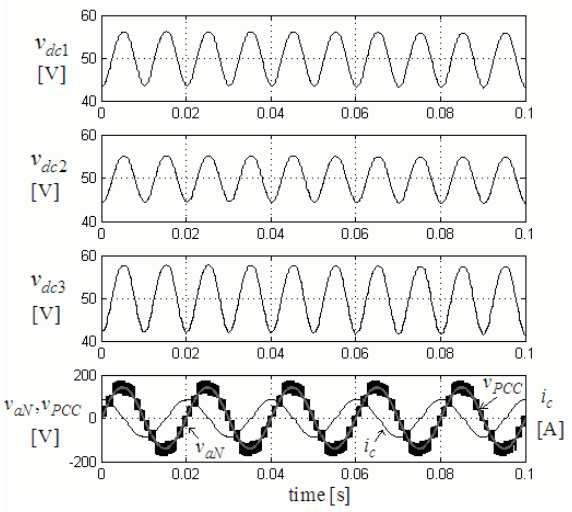
Fig. 8. Simulation results of the multilevel DSTATCOM under ideal H-bridge modules

Figure 8b shows the simulation results when the multilevel DSTATCOM generates lagging reactive current. The dc-link voltages are almost same as the case of generating leading reactive current (Fig. 8a). Whereas, it can be observed that the voltage ripples across the dc-link capacitors in Fig. 8b show opposite phase angles compared to Fig. 8a, which result in a different wave shape for the synthesized multilevel voltage. It is worth noting that the fundamental component of the multilevel output voltage is almost in phase with the grid voltage (v_{PCC}). Therefore, it

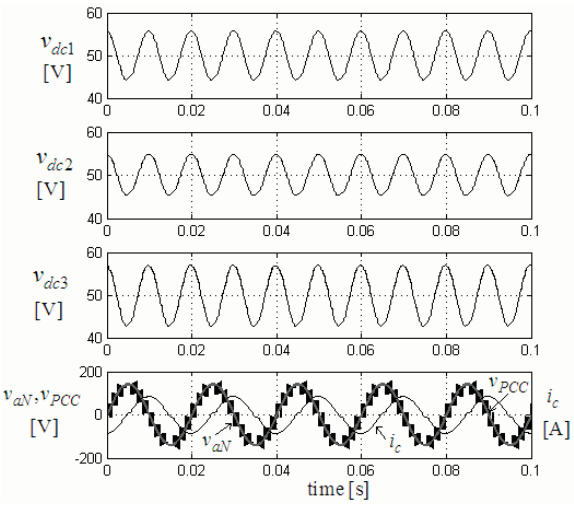
can be concluded from Fig. 8 that the proposed multilevel DSTATCOM can be used to generate leading or lagging reactive current, and the dc-link stabilization can be easily achieved.

Figure 9 shows the simulation results of the DSTATCOM under non-ideal H-bridge module scenarios by changing the dc-link capacitors of the second and third modules to 2400 μF and 1600 μF, respectively. The dc-link capacitor across the first H-bridge remains to be 2000 μF. It is depicted in Fig. 9 that the dc-link with a higher value capacitance shows lower voltage ripple in magnitude, and the third unit shows the largest voltage fluctuations among the three H-bridges. The dc-link voltage waveforms under capacitive and inductive operation mode show similar characteristics compared to Fig. 8. It is verified that the dc-link voltage stabilization can also be achieved under non-ideal H-bridge module scenarios.

To further test the performance of the DSTATCOM, the effect of the modulation index is studied by changing the grid voltage v_{PCC}. Figure 10 shows the simulation results of the system when the modulation index (m) is changed to 0.56, and both the capacitive and inductive operation modes are reported. It can be noticed from Fig. 10 that the dc-link voltages shows similar waveforms compared to the case in Fig. 8. Nevertheless, the synthesized multilevel

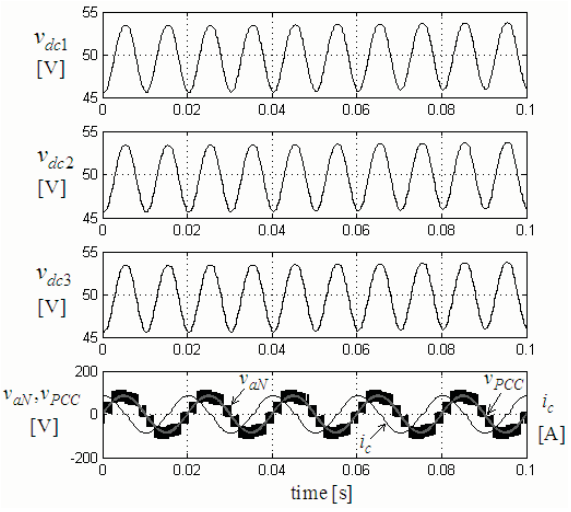


(a) Capacitive mode

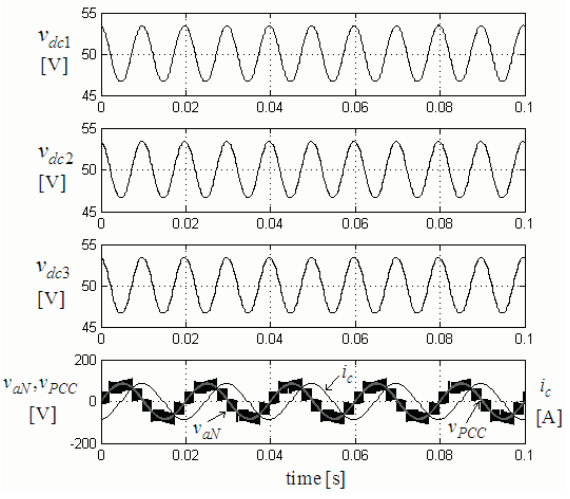


(b) Inductive mode

Fig. 9. Simulation results of the multilevel DSTATCOM under non-ideal H-bridge modules



(a) Capacitive mode



(b) Inductive mode

Fig. 10. Simulation results of the multilevel DSTATCOM when the modulation index m=0.56

voltage v_{aN} reduced to five levels, which implies that the quality of the synthesized voltage degrades. Moreover, the simulation results in Fig. 10 also imply that, for the practical applications, the modulation index (m) should be properly selected to ensure the quality of the output multilevel voltage.

In other words, when the grid voltage is determined, the selection of dc-link voltage is directly associated with the modulation index (m), which influences the output multilevel voltage. For the N-block multilevel inverter with equal dc-link voltages, $2N + 1$ level output voltage can be synthesized [14, 15]. Hence the filtering inductance would be minimized to reduce the cost, weight and volume of the system. Excessive small modulation index (Fig. 10), would not violate the closed-loop stability, but the performance of the multilevel DSTATCOM degrades.

5 EXPERIMENTAL RESULTS

To verify the validity and effectiveness of the proposed multilevel DSTATCOM and its control strategies, a prototype system is built as shown in Fig. 11. The parameters of the power stage and the controller parameters are listed in Tables 2 and 3, which is consistent with the simulation section.

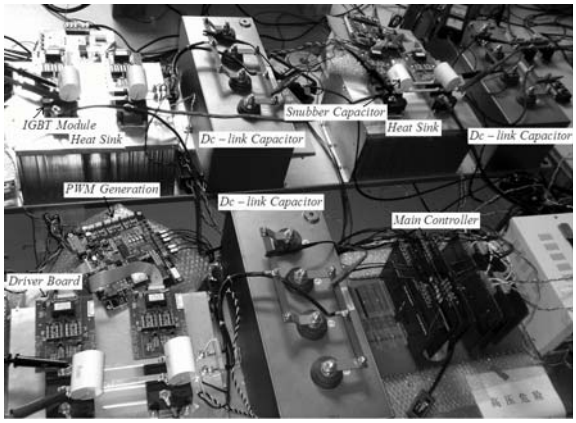


Fig. 11. A photo of the experimental setup

As depicted in Fig. 2, the proposed multilevel DSTATCOM is implemented using the digital signal processor (DSP) from Texas Instruments, where the sampled dc-link voltages, the grid voltage and the inverter current are processed using the devised control algorithm. The DSP is responsible for initialization, A/D sampling, overcurrent/voltage protection, dc-link voltage balancing control as well as the current loop tracking control algorithms. The obtained modulation signals, denoted by S_{e1}, S_{e2} and S_{e3} in Fig. 2 are sent to the field programmable gate array (FPGA), which is utilized to generate phase-shifted carriers of 2.5 kHz, and these carriers are compared with the modulation signal S_{e1}, S_{e2} and S_{e3} to generate switching signals for each H-bridge modules.

It is worth noting that the unipolar PWM scheme is adopted for each H-bridge hence only two switching signals, or gating signals, are generated by the comparison logic, which denote the PWM signals for the left-side and right-side arm of the individual H-bridge unit. The generated gating signals are sent to the bottom level controller, denoted by "PWM Generation" in Fig. 11, to synthesize four channel PWM signals for each H-bridge. Moreover, to avoid direct conducting between the upper and lower IGBTs across each H-bridge, the dead-time of 4 μs is added in the bottom controller. Then these gating signals are sent to the driver circuit (2SD315AI-33) to drive the IGBTs. A detailed flowchart of the function blocks of the hardware is also illustrated in Fig. 2.

Figure 12 shows the gating signals for the left-side arm of the first H-bridge module. It can be observed that the

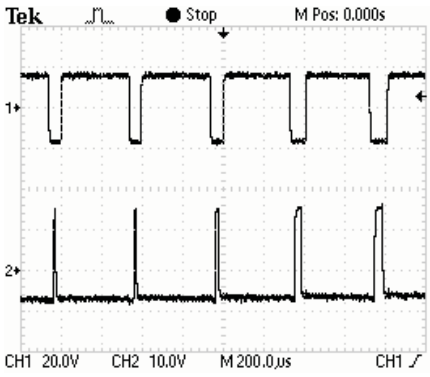


Fig. 12. The gating signals for the left-side arm of the first H-bridge module

upper and lower IGBTs conduct interchangeably and the dead-time can also be observed. Figure 13 shows the experimental results of the multilevel DSTACOM when it generates leading reactive current. It is worth noting that the circuit parameters and the controller parameters are consistent with simulation section. The excellent dc-link voltage waveforms are obtained, which perfectly matches the theoretical analysis and the simulation results. Besides, the synthesized multilevel output voltage v_{aN} and the inverter current i_c are also depicted in Fig. 13. It shows that the seven level output voltage waveform is obtained and the inverter injection current is almost 90 degrees leading the synthesized multilevel voltage.

Figure 14 shows the experimental results of the multilevel DSTATCOM when it generates lagging reactive current. The dc-link voltage stabilization is also achieved and

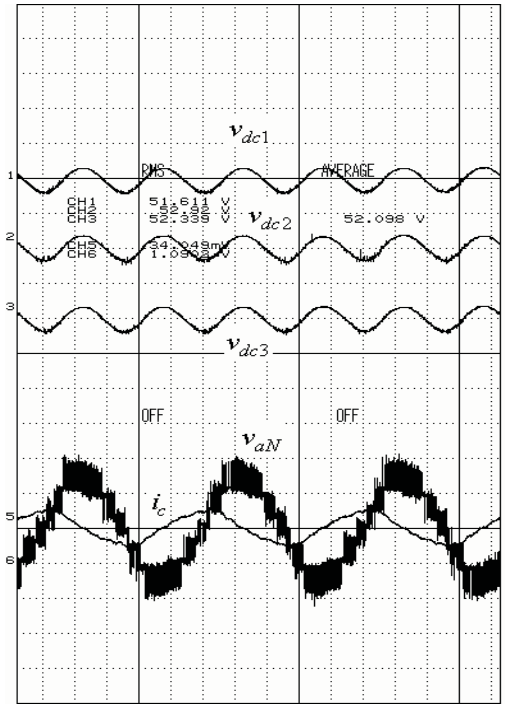


Fig. 13. Experimental results of the multilevel DSTATCOM for the leading reactive current

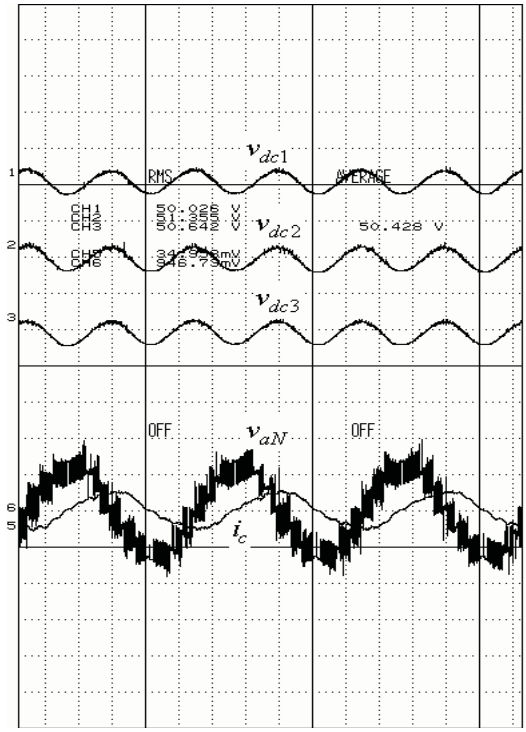


Fig. 14. Experimental results of the multilevel DSTATCOM for the lagging reactive current

the direction of the voltage fluctuation is out of the phase compared to the case of leading reactive current generation in Fig. 13. The synthesized multilevel output voltage and the injection current depicted in Fig. 14 matches the simulation results perfectly.

To test the performance of the multilevel DSTACOM under low modulation index scenario, the grid voltage at PCC is reduced to 75 V (RMS) while the reference voltage for the dc-link is also set as 50 V. As shown in Fig. 15, the lower modulation index indeed shows remarkable influence on the synthesized output voltage, which verifies the simulation results in the previous section. It can also be noticed that the dc-link voltage stabilization and reactive current generation is also achieved. Nevertheless, the synthesized multilevel voltage reduces to five levels, which is consistent with the theoretical analysis. One should be noted that for the practical multilevel DSTATCOM applications, the modulation index should be selected higher than 0.85 to ensure preferred multilevel voltage profile, i.e., the $2N + 1$ level voltage for the N-block multilevel inverter system.

6 CONCLUSIONS

This paper proposes a novel static synchronous compensator for distribution system applications (DSTATCOM) based on the cascaded H-bridge multilevel inverter, which can be used for dynamic reactive power compensation for medium voltage electric power systems. The mathematical formulation of the DSTATCOM is presented using state-space representations. The control strategies are presented, which includes a new software phase-locked loop (SPLL) for grid synchronization, the proportional-resonant current controller and the voltage balancing algorithm. Extensive simulation results are provided to study the performance of the multilevel DSTACOM and a laboratory prototype system is also built for verification. The experimental results match the theoretical analysis and the simulation results perfectly, which validated the validity and effectiveness of the proposed system and its control strategies.

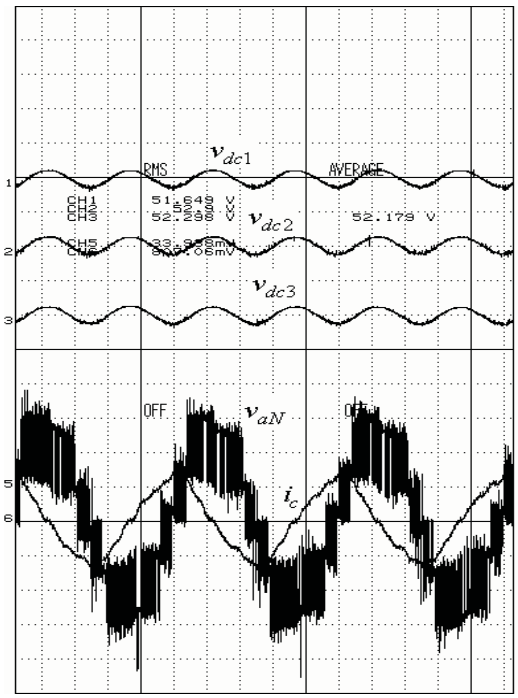


Fig. 15. Experimental results of the multilevel DSTATCOM when the modulation index m=0.56

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