Development of Tunable RF Integrated Passive Devices

by

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

Radio frequency (RF) lumped elements are crucial building blocks for designing any type of passives circuits for RF front-end applications in mobile devices. In particular, high-quality (Q) factor lumped elements are desirable for improving both insertion loss and noise performance. Integrated passive devices (IPD) technology is a platform that can provide miniature inductors, and capacitors with high-Q values that are unattainable with traditional CMOS technologies. Over the past several years, IPD technology has been used to implement devices such as filters, couplers and impedance-matching networks for a wide range of system-in-package applications. However, most of the IPD circuits do not yet have any tunable/reconfigurable functions for use in frequency agile applications.

The objective of this research is to develop tunable integrated passive devices (IPDs) using barium strontium titanate (BST) and micro-electrical-mechanical-systems (MEMS) technologies. Another objective is to develop a fabrication process for monolithic integration of MEMS switches and IPD devices. A 4-mask IPD glass/alumina-based fabrication process is developed at the University of Waterloo for the first time. Details of the modeling and characterization of high-Q lumped elements, L and C, are investigated. The RF performance of these elements is compared with that of similar designs fabricated in a commercial IPD foundry. To highlight the benefits of the IPD process, lumped element bandpass filters are designed, fabricated, and tested.

BST varactors are integrated with IPD circuits to demonstrate a highly miniaturized tunable impedance matching network featuring a wide impedance coverage from 2-3 GHz and an insertion loss of approximately 1 dB. The network promises to be useful in a broad range of wireless applications. A high performance tunable IPD/BST bandstop filter with a wideband balun as a multi-chip module is also proposed. Reconfigurable IPD/BST bandpass filters with tunable transmission zeros are presented and investigated experimentally for operation under high power levels. Intermodulation test results are presented for the integrated IPD/BST devices.

Making use of the fact that the IPD fabrication process is amenable to the realization of MEMS devices, the IPD process originally developed for realizing passive circuits is further expanded to accommodate monolithic integration of MEMS switches with IPD circuits. Contact-type MEMS switches are developed, fabricated and tested. Also, a monolithically integrated IPD/MEMS 3-bit high resolution true-time delay network and high-Q switched-capacitor bank are fabricated and tested to demonstrate the benefits of integrating MEMS technology with the IPD technology.

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Oliver Ka Wai WONG, Waterloo, NOV 2016.

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CHAPTER 1

INTRODUCTION

1.1 Motivations

There has been a strong market-driven demand recently to increase the amount of functionality in compact wireless devices and combine it with low production cost. Multifunctional handheld devices, such as cellular phones, laptops and Internet of things (IoTs) are the main driving forces that require high performance and small-scale passive chipsets. Passive components are indispensable elements in RF communication systems. For example, in a typical cellular phone, passive components account for almost 40% of the size [1], as shown in Figure 1.1. They are used for filtering, decoupling or dividing energy, and are crucial for building L-C tanks and matching networks.

In order to fulfill the requirements of multi-wireless systems such as LTE, GSM, GPS and CDMA in small portable devices, small-form factor multi-band passive components are needed. With the help of advanced technologies, this need can be satisfied with passive surface mount devices (SMDs) or components. However, off-chip inductors, capacitors,

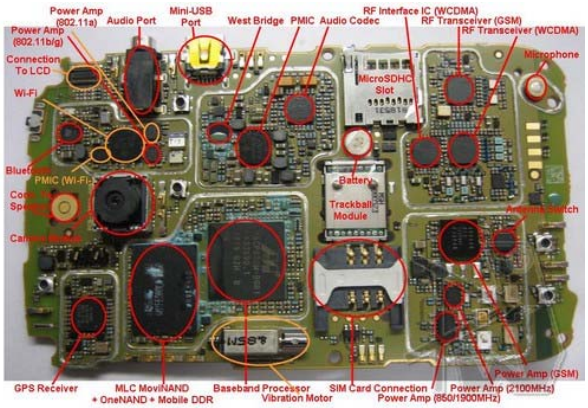


Figure 1.1 Circuit board of the Blackberry Bold

varactor diodes and ceramic filters still suffer performance degradation and increase overall device size.

There has been intensive research on investigating system-on-chip (SOC) passive components that would enable active RFIC devices can be built with passive devices on the same wafer. It may help reduce the cost and offer further size reductions. While it may help in reducing the cost and size, the typical quality factor (Q-factor) of an on-chip inductor for CMOS technologies is around 10 [2]-[3]. Such a low Q-factor inductor results in significantly poor performance in RF building blocks, such as low gain/power ratio of the low-noise amplifier (LNA) [4], high phase noise of the voltage-controlled oscillator (VCO) [5]-[6], and poor matching and degradation of noise figure [7].

Some techniques are proposed to boost the Q-factor of the on-chip inductors, such as using proton implantation [8] and ground shielding [9]-[10], which mainly alter the substrate impedance or diminish the substrate capacitance under the inductor so that the eddy current in the substrate can be minimized. Releasing the inductors on the back-side etching can eliminate the substrate loss and increase the Q-factor, but problems could arise during

packaging, since these inductors are relatively fragile. Also, some of the techniques cannot be easily implemented.

LTCC (low-temperature co-fired ceramic) is a popular technology for designing passive components because it provides a reasonable-cost, low-loss solution for RF applications. L and C elements can be built using aligned and laminated sheets and co-fired around 900 °C. LTCC tape thickness can be made as thin as 12.5 μm, but it is difficult to achieve an accurate thickness resolution. Although it is possible to have several layers interconnecting the L and C elements, there are several disadvantages of using LTCC technology in such applications. Since the ceramic tape film is quite thick, it results in very low density capacitors (<50 pF/mm^2). Furthermore, to achieve high capacitance, these capacitors are usually very large in size which significantly increases the overall costs of the circuits. A high dielectric constant of the thick ceramic tape can be used in LTCC, but it induces a large underpass capacitance in the inductors and limits the operating frequency range of the inductors to below 4 GHz.

Over the past decade, researchers have started to develop a high-Q thin film integrated passive device (IPD) technology for realizing passive components including different transmission lines, R, L and C [11]-[12].

TABLE 1.1 PERFORMANCE COMPARISONS OF DIFFERENT TECHNOLOGIES

	Inductor	Capacitor	MEMS Integration	Form Factor/Device Precision
LTCC	Moderate Q-Factor Low SRF*	Medium Q-factor Low Density (<50pF/mm^2)	No	Medium/Moderate
Standard CMOS	Poor Q-Factor	Low Q-Factor Medium Density	Yes	Small/Good
IPD	Moderate to High Q-Factor High SRF*	High Q-Factor High Density >600pF/ mm^2	Yes	Small/Good

*SRF-self resonating frequency

Table 1.1 summarizes the benefits of IPD compared with LTCC and CMOS technologies in RF performance. One of the highlights of this technology is the metal layer (thick copper) which can be used to realize the high-Q values. Another highlight is that a high resistivity substrate is used so that the eddy current can be reduced and less power is dissipated in the substrate effects [13]. Also capacitor density and its Q-factor can be greatly enhanced with very thin high-dielectric constant material and thick copper, respectively.

In addition to these, the electrical performance and overall size of the circuit can be improved since it is easy to integrate several passive components to design a reconfigurable passive device, such as a differential duplexer with the L-C network. This helps reduce the extra number of passive components in the RF front-end, for instance, the balun. Furthermore, building all high-Q passive components on a single chip can, when compared to the discrete off-chip passive components, greatly reduce the unpredictable parasitic inductance of the leads and soldering. This passive loss reduction can greatly increase the battery life of a wireless device.

More importantly, the IPD thin film fabrication involves processes with sputtering, chemical vapor deposition (CVD) and e-beam evaporation, all of which are similar to the current IC technology and, the thermal budget is much lower compared with the ceramic

technology. As a result, it is advantageous to combine IPD and radio frequency micro-electromechanical systems (RF MEMS) process monolithically, as well as IPD with BST technology in a hybrid fashion to obtain the goal of tunable IPD.

Research on RF MEMS began in the early 1990's. Since then, many companies and research groups have tried to employ MEMS in the RF front-end modules (FEMs) because of their excellent linearity performance, low insertion loss, low dc power consumption and high isolation [14]. Tunability in RF MEMS circuits is one of the major features in creating various tunable devices such as varactors, switching networks, phased arrays and impedance matching networks for different active and passive devices.

RF filter is one of the most crucial elements in microwave communication systems. These communication systems are multi-band and require a large number of filters. Figure 1.2 shows a block diagram of a multiband transceiver. A large area is occupied when individual fixed bandpass filters are employed. The problem can be circumvented by using reconfigurable/tunable devices.

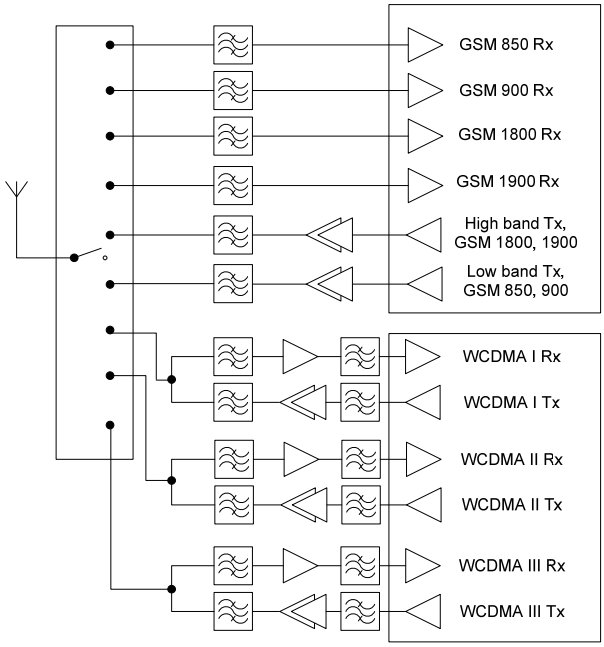


Figure 1.2 A typical multi-band transceiver configuration.

1.2 Objectives

The motivation for this research is to develop a tunable/reconfigurable IPD platform for designing bandpass and bandstop filters, as well as other passive components, using the BST-based, MEMS integrated with the high-Q integrated passive device (IPD) platform. The MEMS integration is of particular interest since the same the IPD process, with some modifications, can be employed to realize MEMS-based tunable IPD devices. The IPD process on its own has a huge market volume, and will be in a widespread use in RF applications and, can be applied in the system in package (SiP) technologies or multi-chip modules (MCMs) integration to help develop passive devices for the next generation of communication systems.

The main objectives of this proposed project are:

- Development of a glass-based, and alumina-based integrated passive device (A/G-IPD) fabrication process, at the University of Waterloo, that can be used to fabricate high-Q RF passive lumped elements such as inductors and capacitors
- Development and demonstration of several tunable IPD devices through hybrid integration with BST technology, such as tunable impedance matching networks and tunable bandstop, and reconfigurable bandpass filters.
- Development of a monolithic IPD-MEMS process that is a compact, low-loss and reconfigurable/tunable such as high-Q switched capacitor banks and high-resolution low-loss true-time delay networks.

1.3 Thesis Outline

In Chapter 1, the motivation and objectives of the overall research project are described. Chapter 2 presents a literature review of IPD devices and tunable devices using MEMS technology. Chapter 3 covers the development efforts of the new glass-based IPD process at

the University of Waterloo. Some fabrication challenges for thick metal and the corresponding solutions are addressed in detail. Measured results and modeling characterizations of high-Q passive elements such as inductors, capacitors and bandpass filters are also presented in this chapter. Chapter 3 also illustrates the design and performance of a tunable impedance network using BST varactors in an alumina-based IPD process. Chapter 4 elaborates on the reconfigurable/tunable bandstop and bandpass filter with wideband balun using the commercial IPD technology offered by ON Semiconductor for frequency agile applications. Results comparisons between the proposed process and the commercial process are presented. Chapter 5 presents a novel monolithic IPD-MEMS process, which features a low loss and high resolution true-time delay network. A high-Q IPD-MEMS digital capacitor bank is also presented. Finally, Chapter 6 provides a brief summary of the contributions of the thesis, along with possible future proposed research directions.

CHAPTER 2

LITERATURE REVIEW

2.1 Thin-film Integrated Passive Device (IPD) Platform

A thin film integrated passive device (IPD) is a general term for multiple thin-film passive elements such as resistors, capacitors and inductors that share the same substrate and packaging. Thick metal is one of the key features in this technology. Because of its small form factor and high-quality, this platform is well-suited for the future trend of the RF system-in-package (SiP) which is an excellent alternative to system-on-chip (SoC). SoC has several performance constraints in designing passive devices, so the loss of the RF systems is quite high, which is unfavorable to the future wireless systems. In contrast, SiP provides a platform to place multiple chips without performance trade-off, thus satisfying the overall requirements of the system design.

Figure 2.1 shows a typical IPD process geometry consisting of three main parts - resistor, capacitor and inductor – which are interconnected by metal via holes. A passivation layer is deposited to protect the components from air and acts as an isolation dielectric

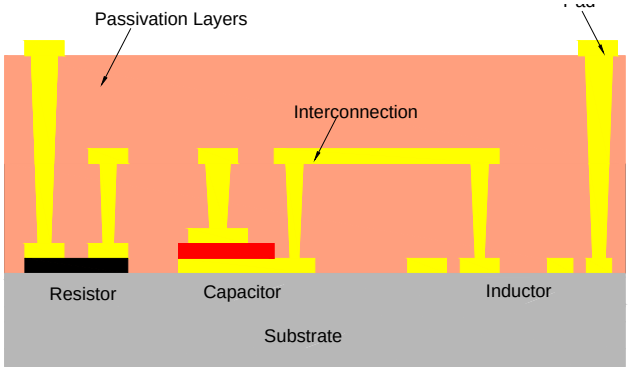


Figure 2.1 A typical geometry of IPD process

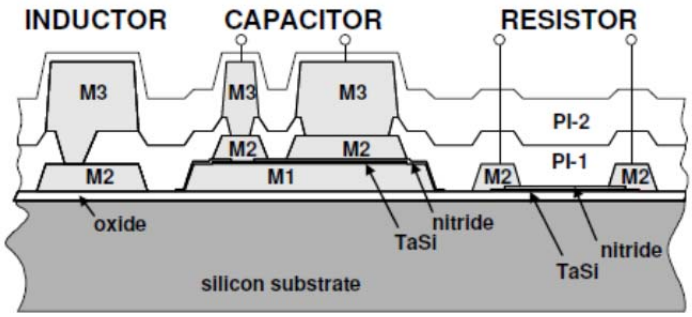
among all the interlayer components. Pads are usually placed on top of the geometry to provide access between the IPD and the circuits outside.

2.1.1 IPD RF Bandpass Filter

RF bandpass filters are one of the most crucial components in the RF-front end for a variety of wireless applications such as WiMax, WLAN and cellular phone networks. These filters can help enhance wanted signal reception, reduce harmonic effects among different active devices and improve the linearity and noise figure of the overall RF system. By using the IPD process, a low-loss and small-scale band-pass filter can be achieved. Furthermore, its flexibility is a great advantage, enabling integration of the IPD chip with other active CMOS chips by stacking.

Figure 2.2 (a) shows the IPD structure by STATS ChipPAC Inc. The schematic and layout of a miniaturized ultra-wideband (UWB) bandpass filter using the silicon IPD technology is shown in Figure 2.2 (b) and (c) [15]. Three metals layers and two dielectric layers are used. The thicknesses of metal 1 (M1) to metal 3 (M3) are 1 µm, 3 µm and 8 µm respectively. The capacitance density of this process is 330pF/mm^2 and the quality factor of the inductor is between 25 and 45, depending on the operating frequency and inductance value. As shown

in Figure 2.2(d), the passband frequency of the filter is from 7 GHz to 9 GHz, and its insertion loss is within 2.5 dB. A similar approach can also be found in [16].



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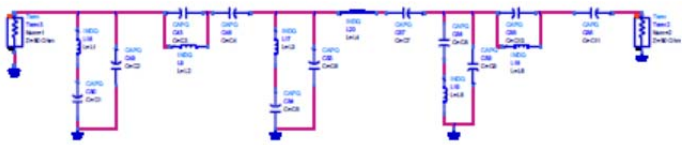

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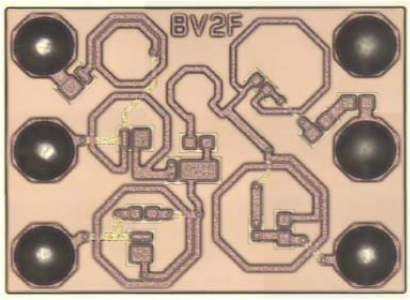

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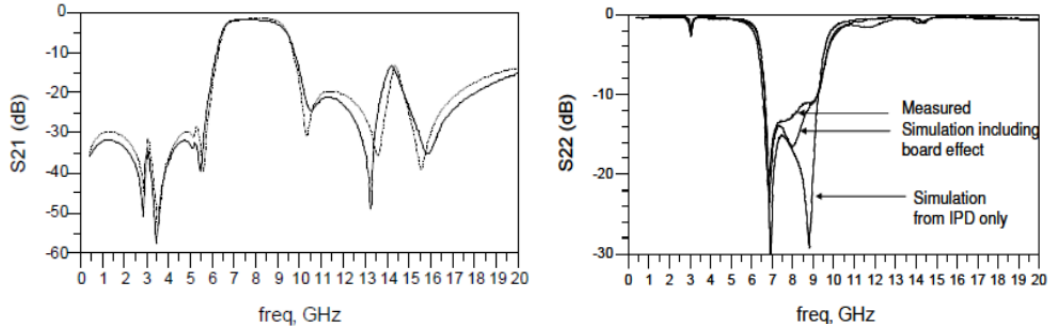
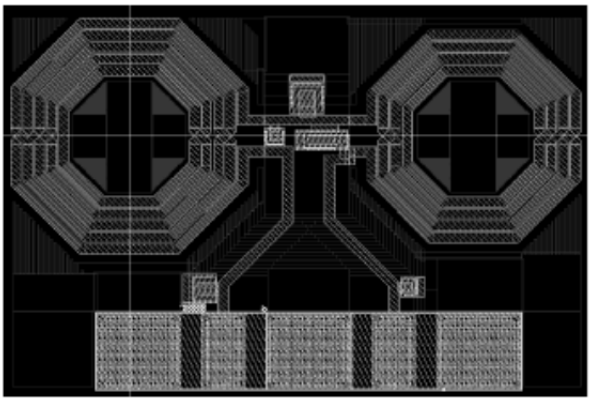


(d)

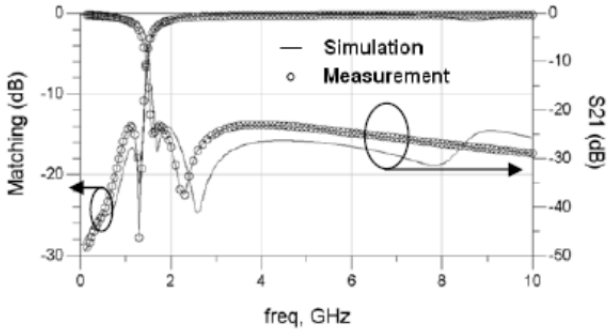
Figure 2.2 Ultra-wideband (UWB) bandpass filter using silicon IPD technology by STATS ChipPAC Inc. (a) Thin-film IPD structure. (b) Schematic of the filter. (c) Layout of the UWB filter and (d) frequency response of the UWB bandpass filter [15].

2.1.2 IPD RF Lowpass Filter

Lowpass filters are useful for suppressing harmonics, oscillation feedback signals towards the main desired signal, and spurious responses from the active devices such as voltage-controlled oscillators (VCOs), amplifiers and mixers. The filters also help lower the possibility of receiving other frequency band signals. In [17], STMicroelectronics demonstrates the IPD lowpass filter in silicon-on-insulator (SOI) CMOS technology for GSM applications. The chip size is around 450 μm × 700 μm. Its layout and the frequency responses are shown in Figure 2.3 (a) and (b), respectively. It can be shown that the insertion loss is around 1.5 dB and a wideband rejection is achieved.



(a)

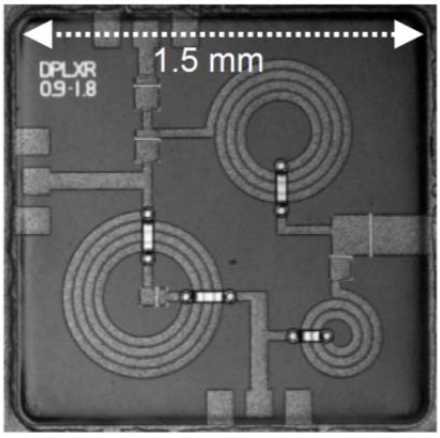


(b)

Figure 2.3 IPD GSM lowpass filter. (a) Layout of the lowpass filter and (b) frequency response of the lowpass filter [17].

2.1.3 RF Diplexer

A diplexer is one of the important devices in a multi-band system. It consists of two filters coupled to a common output which has a lowpass and a highpass stage, respectively. Figure 2.4 (a) shows a 900/1800 MHz diplexer by KAIST, Korea [18]. In this design, an alumina substrate is used to replace a popular high-resistivity silicon substrate to decrease costs. Also, it brings a better thermal conductivity. The process and frequency response of the filter are shown in Figure 2.4 (b) and (c). The overall insertion loss is around 0.5 dB and the isolation is between 20-40 dB.



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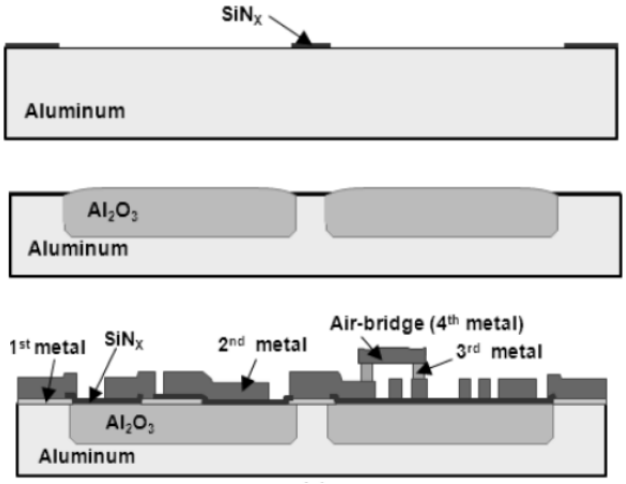

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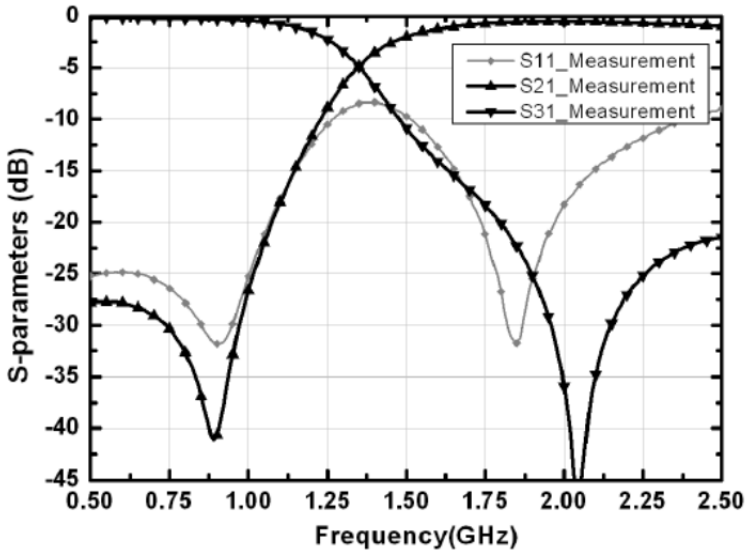


(c)

Figure 2.4 900/1800 MHz diplexer by KAIST. (a) Layout of the filter. (b) IPD structure from KAIST on aluminum substrate and (c) frequency response of the duplexer [18].

2.2 RF MEMS Tunable Filters

Different wireless applications are allocated to different ISM frequency bands. The latest portable handheld devices even have to operate at multi-frequency bands, but many devices still have multiple single-band filters installed to function at the corresponding frequency. Tunable filters can change the cutoff frequency of the passband/stopband adaptively. It not only reduces the complexity of the systems, but also minimizes the size of the overall circuit resulting in low-cost production. Tuning methods can be generally divided into three main groups: (i) electronic, (ii) mechanical, and (iii) material. Table I shows the most popular method for the current tunable filter technology.

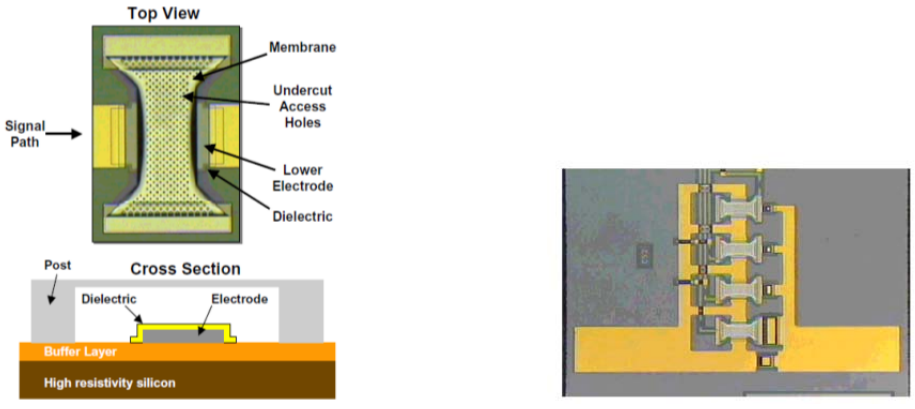
TABLE 2.1 COMPARISONS OF DIFFERENT TUNING METHODS FOR RF TUNABLE FILTER

Tuning Technology	Electronic Tuning			Mechanical Tuning		Material Property Tuning	
	PIN Diode	Varactor	Active Device	MEMS	Piezoelectric	YIG	BST
Tuning Speed	ns	ns	ns	μs to ns	ms	ms	ns
Power Handling	High	Low	Low	High	High	Medium	Medium
Power Consumption	Medium	0	Medium	0	Low	Very High	0
Q-factor	R_s=1Ω	Low	Low	High	High	Very High	Low
Size	Small	Medium	Small	Small	Small	Big	Small

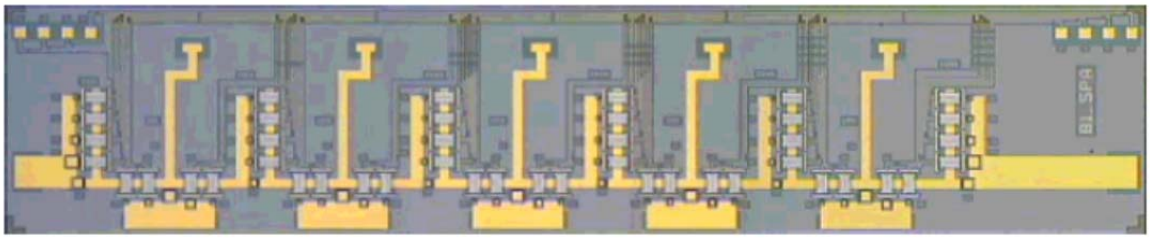
By comparing all the aspects in terms of tuning speed, power handling, power consumption, Q-factor and size, MEMS has the highest potential to develop a good quality tunable filter with a small size and low loss. Hence, in the following sections, various RF MEMS tunable filters are discussed.

2.2.1 Tunable Filter with MEMS Capacitive Membrane Switch

Figure 2.5 shows one of the first tunable filters in the UHF band by Raytheon Systems Company [19]. As shown in Figure 2.5 (a) and (b), a capacitive membrane switch is used to construct the variable capacitor which is the main element for the tunable bandpass filter. The whole 5-pole filter is shown in Figure 2.5 (c). Figure 2.5(d) shows five capacitive-



(a) (b)



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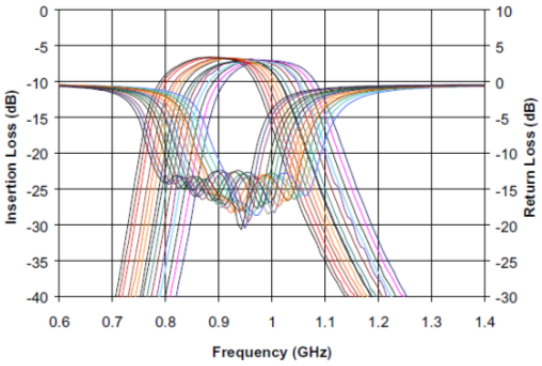


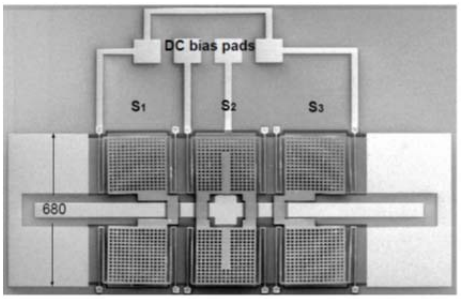
(d)

Figure 2.5 Tunable bandpass filter by using capacitive membrane switch. (a) RF MEMS capacitive membrane switch. (b) 4-bit variable capacitor. (c) Tunable capacitor with inductor network (size: 3.5 mm×14 mm) and (d) 5-pole frequency response [19].

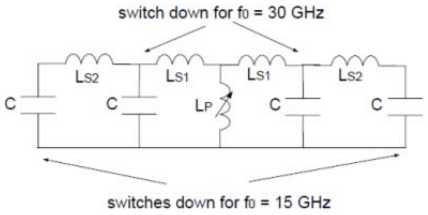
coupled L-C filter is shown in Figure 2.5 (c). Figure 2.5 (d) shows five capacitive-coupled L-C resonators are put together and the frequency response of the filter. The tunable passband is between 880-992 MHz, with an insertion loss of around 7 dB.

2.2.2 Tunable Filter with MEMS Capacitive Membrane Switch on an Inductor

Another tunable filter using some capacitive switches with capacitors is shown in Figure 2.6 [20]. It uses a short-circuit stub connected to the ground to behave as an inductor. By changing the height of the movable plate, the effective inductance is changed. The insertion loss is about 3-5 dB at 15 GHz and 30 GHz, respectively. However, the tunability of an inductor designed this way is very limited.



(a)



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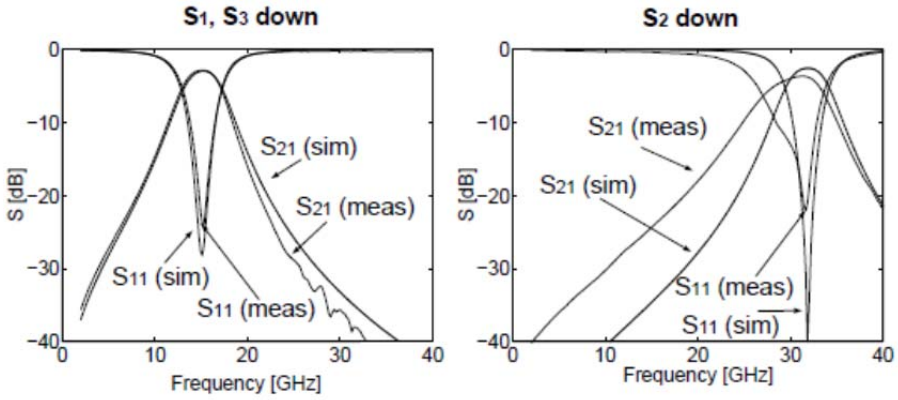
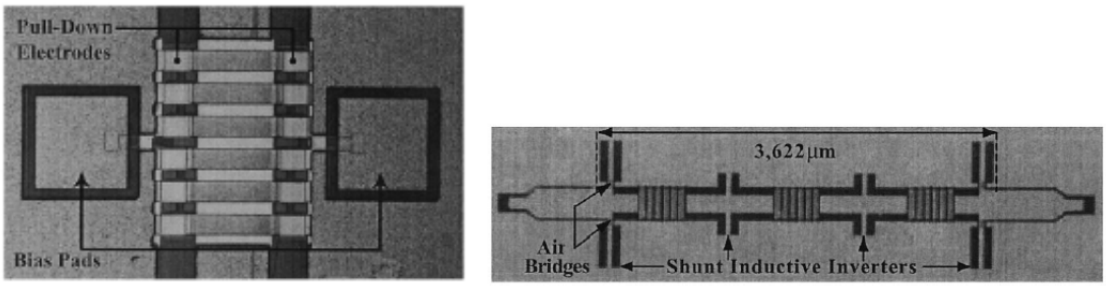


(c)

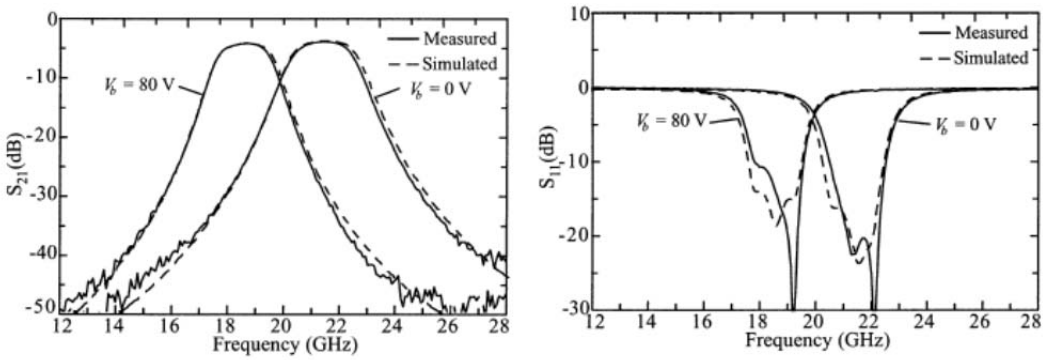
Figure 2.6 Bandpass filter using the tunable short-circuit inductor (a) Layout of the tunable bandpass filter. (b) Schematic of the bandpass filter and (c) the frequency response for different actuation of the switch [20].

2.2.3 Tunable Filter with MEMS Varactor

Figure 2.7 shows a tunable bandpass filter using a set of varactors to constitute a slow-wave resonator unit. Figure 2.7 (a) and (b) show the structure of the varactors and the layout of the filter. It can be seen that a miniature filter is achieved by the slow-wave structure with the shunt inductive inverters. The passband is between 18.6 GHz to 21.4 GHz, with an insertion of around 4-5 dB.



(a) (b)



(c)

Figure 2.7 Bandpass filter using the MEMS varactor (a) Layout of MEMS varactors. (b) Layout of the bandpass filter and (c) the frequency response for different actuations of the switch [21].

In most of the literature publications, MEMS is mainly used for microwave or millimeter wave frequencies. In fact, most of the RF MEMS filters use transmission lines as the inductor part. Hence, when it comes to lower frequency applications (e.g. 1 GHz), the circuit size is always bulky due to the longer inductive line. Alternatively, off-chip inductors may replace the transmission lines, however, it is difficult to make them small and apply them to a micro-scale chip. All in all, there is notable potential in integrating the IPD platform and RF MEMS technologies since it is a trade-off among all the current technologies.

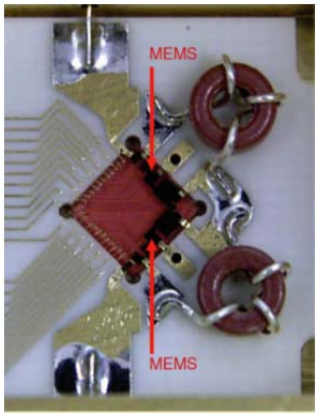


Figure 2.8 A two-pole, 850-1750 MHz tunable filter built using the off-chip air coil inductor.

CHAPTER 3

DEVELOPMENT OF THE INTEGRATED PASSIVE DEVICE (IPD) FABRICATION PROCESS AND ITS COMPONENTS

3.1 Introduction

High performance passive devices are always needed in the RF front-end and wireless systems. Particularly in demand are high quality (high-Q) factor-passive elements, inductors (L) and capacitors (C), which are the building blocks of most of the compact passive devices. On the other hand, owing to the stringent requirements of the modern communication systems, some high-Q fixed and tunable passive components are preferable in the RF-front ends. As discussed earlier, the loss of the on-chip filter can be very high, mainly because the Q-factor of the on-chip lumped inductor on the CMOS silicon substrate is very low (i.e., around 10) which leads to a poor quality factor of the L-C resonator. As a result, the in-band insertion loss is high, which may increase the noise figure in the overall RF system performance.

In this chapter, the proposed glass-based IPD fabrication process built at the University of Waterloo is first presented. Details of the modeling and characterization of the high-Q lumped elements, L and C, are also investigated. To highlight our low-loss IPD process, a modified three-pole Chebyshev bandpass filter at 1.5 GHz is designed, fabricated and tested, and its RF performance is also compared with a similar design fabricated in a commercial IPD process offered by ON Semiconductor. In addition, a repeated measurement of our 3-year-old wafer is obtained, which verifies the reliability of our proposed IPD process. Finally, an impedance tuner using barium strontium titanate (BST) varactors on our proposed alumina-based IPD process is presented.

3.2 Integrated Passive Device (IPD) Fabrication Considerations

Metal Layer

To achieve the high-Q passive elements, the choice of metal is of great importance. Table 3.1 shows a general comparison of different metals. Based on cost, compatibility of current and available foundry technology, and the fabrication complexity, copper is chosen, even though silver has a slightly higher conductivity.

TABLE 3.1 COMPARISONS OF ELECTRICAL AND MECHANICAL PROPERTIES OF DIFFERENT METALS

Metal	Conductivity (MS/m)	Young's Modulus(GPa)	Thermal Conductivity $Wm^{-1}K^{-1}$	Cost
Copper	58	110	401	Low
Silver	62	83	429	High
Aluminum	35	69	237	Low
Gold	45.2	83	318	Very High

Thick Photoresist

For planar inductors, the smaller the size (i.e., shorter current path), the less the loss. In other words, the Q-factor is higher at low inductance. In order to boost the Q-factor without increasing the size, a smaller gap is sometimes desirable. However, this comes with the difficulty of high aspect ratio thin-film fabrication, so a good choice of photoresist would be the key to enhancing the Q-factor of the inductor.

In the open literature, SU-8 is popular for micro-molding in MEMS applications, since it is able to achieve high-aspect ratio structure (>20:1) [22]. However, SU-8 has poor adhesion with copper or gold seed layer as well as stress problems in the dense winding inductors, which leads to delamination during development. Moreover, SU-8 is very difficult to be removed after the copper electroplating. A wet etch in N-methyl-2-pyrrolidone (NMP) and oxygen plasma may be needed to remove all the SU-8 residues [23]. Because of the good copper compatibility, AZ-P4000 (AZ-4562) and AZ-9260 are the better choices for making micro-moldings as they both have very similar process steps and characteristics. Owing to the higher aspect ratio, AZ-9260 is chosen for the thick photoresist mold. Its characterization picture is shown in Figure 3.1.

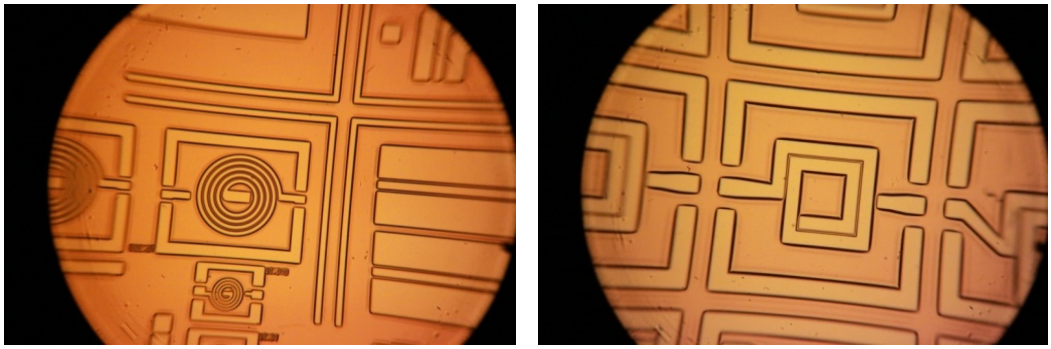


Figure 3.1 Characterization of the 10 μm thick positive photoresist AZ-9260.

Difficulties in using thick photoresist

In thin-film fabrication, it is assumed that the resist film is homogeneously exposed, and therefore, the time for development and exposure are easily controlled and optimized. However, there are many fabrication challenges with the use of thick photoresist. First, underexposure is a common problem. With thick photoresist, UV energy going to the base of the resist can be slightly different between the top and the bottom, which may affect the linearity of the development rate and exposure time. Another difficulty of applying thick photoresist is edge bead, which induces an undesired gap during exposure. It is common to have this when spin-coating thick photo resists, since they have lower viscosity which increases the tension across the surface. A procedure of edge-bead removal has to be applied in order to achieve an accurate distance between the mask and the sample.

Another challenge is to characterize the rehydration time for the AZ 9260 series thick photoresist. To obtain a reliable development time, a rehydration period of around 30 minutes @ 50%/22 °C for 10 μm photoresist after soft bake is required. The reason for this is that water is one of requirements to help the photoreaction from transforming DiazoNaphtoQuinone- (DNQ-) sulfonate into indene carboxylic acid. This rehydration step helps some water from the air to diffuse into the resist film. However, if the air humidity is too low, even a long rehydration will not provide sufficient water content [24]-[25].

Substrate

Table 3.2 shows the electrical characteristics for different substrates. A glass is chosen because its low cost and very high resistivity, which help reduce the eddy current and the loss in the substrate. This will be discussed further in the inductor design section.

TABLE 3.2 COMPARISONS OF DIFFERENT SUBSTRATE MATERIAL

	Electrical			Cost
	Relative Dielectric Constant (ϵr)	Loss Tangent ($\times 10^{-3}$)	Resistivity (Ω-cm)	
Quartz	3.8	0.02	$>10^{15}$	Medium
Glass	4-5	1-5	$>10^{13}$	Low
Si	11.9	50	10-100	Low
HR-Si	12	1-10	1000-5000	Medium
HR-GaAs	12.9	0.6	10^{7}-10^{9}	High

3.3 Integrated Passive Devices Process

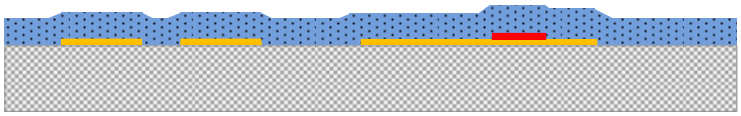
Our proposed 4-mask IPD process developed in the University of Waterloo has two metal layers (1st: Gold and 2nd Copper), as shown in Figure 3.2. In (a), a layer of chromium/gold (Cr/Au: 30 nm/50 nm) is deposited on the boro-aluminosilicate glass substrate as a seed layer, and a gold layer of 1.5 μm is electroplated, which serves as the first metal layer. Then, a 20 nm of chromium (Cr) is deposited on top of the gold and a lift-off process is followed by wet etching of gold and chromium. In (b), a 20 nm of TiW is deposited to serve as a seed layer for nitride, and thereafter, a 0.5 μm of silicon nitride (Si_xN_y) is deposited by PECVD. In (c), photoresist is used to help pattern the (Si_xN_y) which serves as a dielectric layer for the capacitor with RIE. In (d), after that, a polyimide layer- PI-2611 (4 μm) is spun and patterned using (RIE) to make some via holes. Aluminum is used as a hard mask for patterning the polyimide, and it is etched in the PAN etchant afterwards. In (e), after etching the polyimide, a thin layer Ti (e-beam: 20 nm)/Au (sputtering: 100 nm)/Ti (e-beam: 20 nm) is deposited as a seed layer and the adhesion layer for the thick copper. After that, in (f), a layer of thick

photoresist is spun and patterned, and, in (g), an 8 μm thick copper layer (2nd metal layer) is electroplated. Finally, in (h), the seed layer is removed by RIE.

(a)

(b)

(c)



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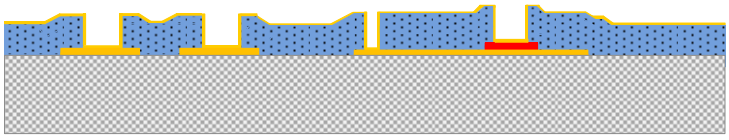

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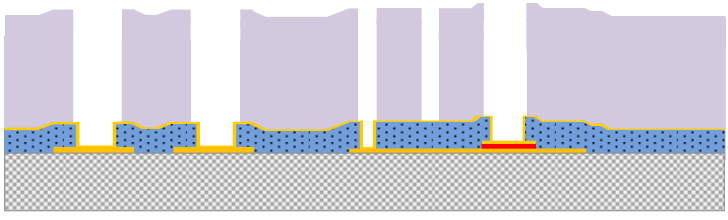


(f)

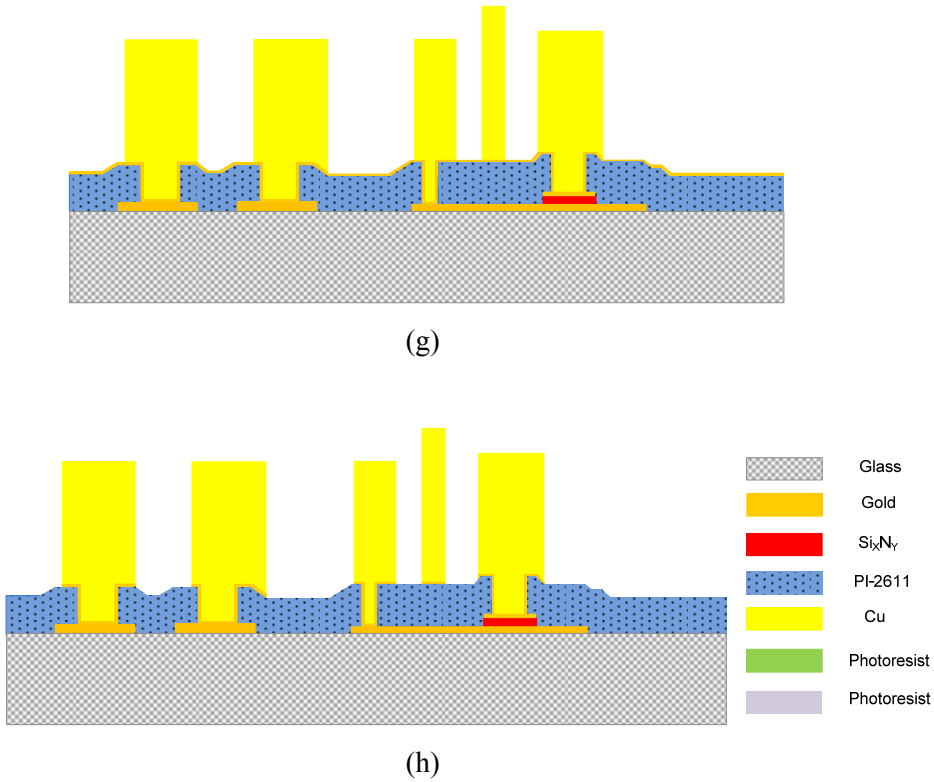


Figure 3.2 Proposed 4-mask IPD fabrication process flow.

In order to characterize the electrical parameters such as loss tangent and dielectric constant for all layers (including the actual dielectric constant of the Si_xN_y, glass substrate, and polyimide), devices for instance RF filters, inductors, capacitors and CPW transmission lines are designed in the electromagnetic software (HFSS) and the circuit simulator (ADS). Figure 3.3 shows a fabrication picture in steps (e) and (f) in Figure 3.2. The inner square is the first metal layer covered by SiN dielectric and Cr/Au, and the entire place is covered by polyimide, which is denoted in amber color. Figure 3.4 shows the via holes by etching the polyimide using anisotropic dry etching in RIE to obtain vertical sidewalls.

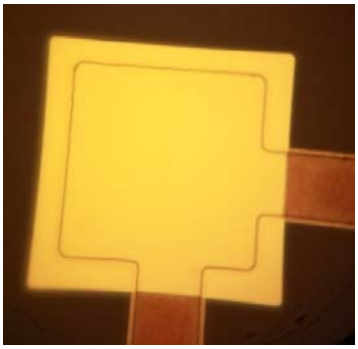


Figure 3.3 Fabrication picture in steps (e) and (f) in Figure 3.2.

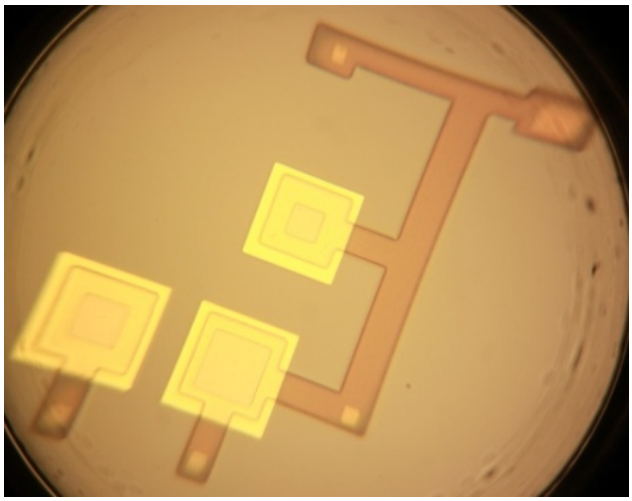
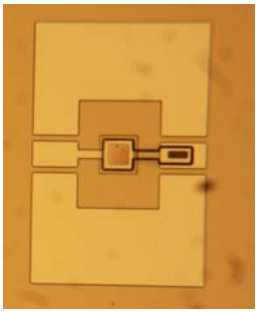
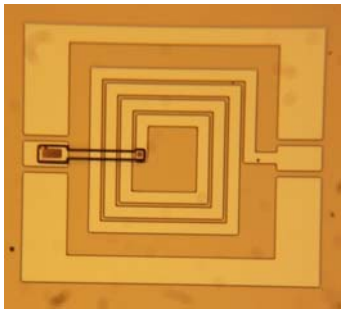


Figure 3.4 Fabrication picture in step (g) in Figure 3.2 before depositing the seed layer.

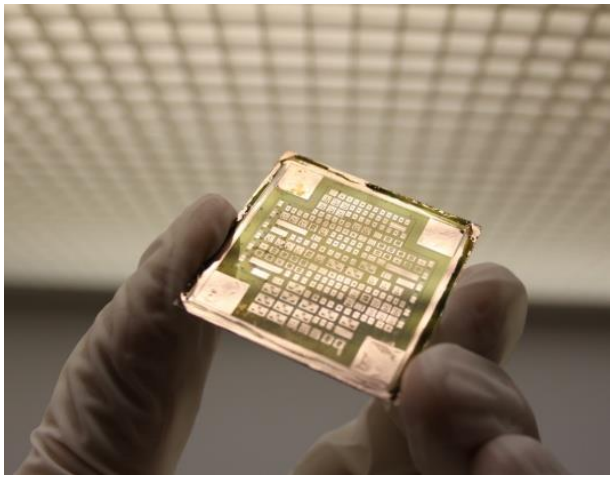
Figure 3.5 (a) - (c) shows one of the IPD capacitor, inductor designs, and, the first preliminary wafer, respectively. It should be mentioned that some of the metals are short-circuited, since the cracking of the thick photoresist in some areas, as shown in Figure 3.5 (c). As a result, the yield of the first preliminary wafer is not very satisfactory. The main reason for this is that a weak alkaline copper electroplating solution was first used to electroplate the thick copper. However, it is found out that there is a possibility that the thick photoresist is attacked by the alkaline solution and resulting in cracking of the photoresist



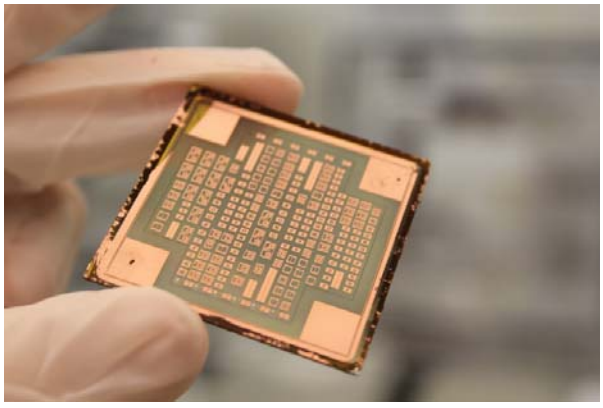
(a)



(b)



(c)



(d)

Figure 3.5 Final fabrication: (a) Capacitor, (b) Inductor and (c) 1st preliminary wafer and (d) completely successful IPD wafer.

structure. Optimized post-bake times and temperatures were also investigated in order to increase the durability of the photoresist in the plating bath. After several trials of recipe and solution changes, the proposed process is successfully implemented and developed at the University of Waterloo. The final wafer picture is shown in Figure 3.5 (d).

3.4 Modeling and Characteristics of IPD Inductor

In designing an RF inductor, there are several important considerations that affect its Q-factor and self-resonant frequency. These factors include: metal thickness, line width, gap distance between metal traces, inductor size, and number of turns. A good understanding of the inductor model is needed to achieve optimum inductance with high-Q factor. They will be discussed below:

A typical geometry and physical lumped model parameters of a planar spiral inductor are shown in Figure 3.6 and 3.7, respectively.

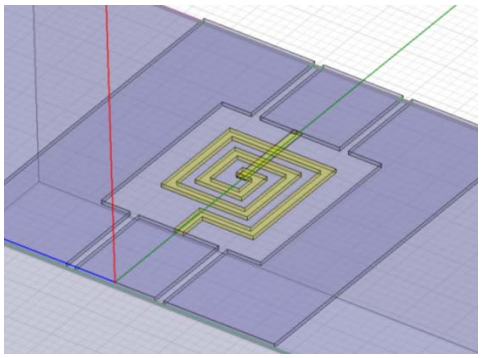


Figure 3.6 Geometry of the thick copper inductor.

L_s: Inductance of the spiral including the underpass structure

R_s: Resistance of the spiral including underpass structure

C_s: Series capacitance by the capacitive coupling of the overlap between the spiral and the underpass

$C_{isolation}$: Capacitance from the metal to the isolation layer which is polyimide

C_{glass}: Capacitance of the substrate

R_{glass}: Resistance of the substrate

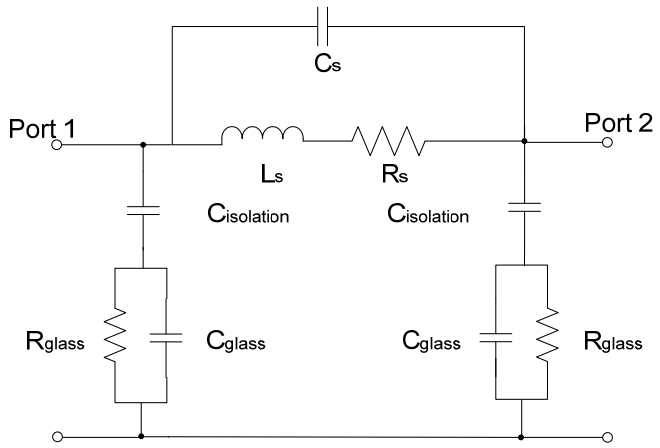


Figure 3.7 Physical lumped model of a spiral inductor on glass substrate [13].

Series Inductance

By using the Greenhouse model [26], the equation for the inductance is:

$$L_T = L_0 + \Sigma M \tag{3.1}$$

where L_T is the total inductance, L_0 is the sum of the self-inductances of all the straight segments, and the summation, M, is the sum of all the mutual inductances, including positive (same current direction) and negative (opposite current direction). This equation can be demonstrated with the help of Figure 3.8 and the equations below:

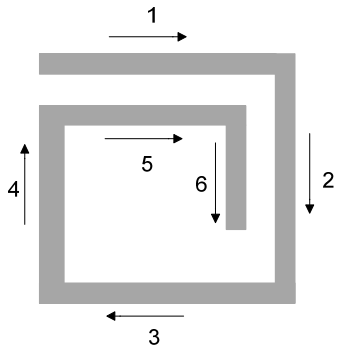


Figure 3.8 Current flow in the inductor.

$$L_T = L_1 + L_2 + L_3 + L_4 + L_5 + L_6 + 2(M_{15} + M_{26}) - 2(M_{13} + M_{24} + M_{35} + M_{46}) \quad (3.2)$$

$$L_x = 2l_x\{\ln[\frac{2l_x}{w+t} + 0.50049 + [\frac{w+t}{3l_x}]]\} \quad (3.3)$$

$$M = 2lk \quad (3.4)$$

$$k = \ln\left\{\frac{l}{GMD} + [1 + (\frac{l^2}{GMD^2})]^2\right\} - [1 + (\frac{GMD^2}{l^2})]^2 + \frac{GMD}{l} \quad (3.5)$$

$$\ln GMD = \ln d - \left\{\left[\frac{1}{12(d/w)^2}\right] + \left[\frac{1}{60(d/w)^4}\right] + \left[\frac{1}{168(d/w)^6}\right] + \cdots\right\} \quad (3.6)$$

where *l* is the length (in cm) of the conductor, k is mutual-inductance-parameter, w and t are the width of the thickness (in cm) of the conductor and *GMD* is the geometric mean distance between the two conductors which is approximately equal to the distance, *d,* between the track centers. This model gives a good physical sense and relatively accurate results in calculating the inductance. However, it is not easy to design the desired inductance according to the specifications required, and, it is only applicable to the square shape. Furthermore, it cannot deal with other forms, such as in circular, hexagonal and octagonal shapes, as shown in Figure 3.9.

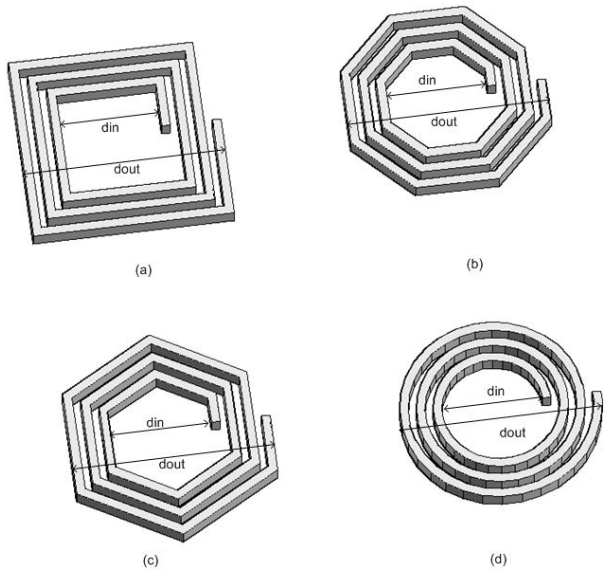


Figure 3.9 Different implementations of inductor (a) square, (b) octagonal, (c) hexagonal and (d) circular.

A simple model based on data fitting (least-square fit) with the experimental results is reported in [27]. This model is verified with more than 10000 inductors in the library,

$$L(nH) = \beta\, {d_{out}}^{\alpha 1} w^{\alpha 2} {d_{avg}}^{\alpha 3} n^{\alpha 4} s^{\alpha 5} \tag{3.7}$$

therefore, it has a relatively low percentage error. In this model, the inductance is given by Equation (3.7) where coefficients β and α are layout-dependent, as given in Table 3.3.

TABLE 3.3 COEFFICIENTS FOR DATA-FITTED MONOMIAL EXPRESSION

Layout	β	α_1	α_2	α_3	α_4	α_5
Square	1.62×10^{-3}	**-1.21**	**-0.147**	**2.4**	**1.78**	**-0.03**
Hexagonal	1.28×10^{-3}	**-1.24**	**-0.174**	**2.47**	**1.77**	**-0.049**
Octagonal	1.33×10^{-3}	**-1.21**	**-0.163**	**2.43**	**1.75**	**-0.049**

Using the simulation software of HFSS and MATLAB, some values are verified and the model is found to have a maximum error percentage of less than 10% for inductances is between 1 nH-8 nH.

Series Resistance

For a transmission line, at DC, the current density is uniform. However, when the frequency becomes higher, the induced eddy current makes the current density non-uniform. This eddy current effect produces its own magnetic field to oppose the original field. As a result, it reduces the net current flow in the conductor and hence increases the ac resistance. The severity of the eddy current effect is determined by the ratio of skin depth to the conductor thickness. The equation for depth of penetration (also known as skin depth) in a good conductor is $\delta = 1/\sqrt{\pi f \mu \sigma}$ where f is the operating frequency, μ is the permeability and σ is the conductivity of the metal conductor [13]. Assume the current density attenuates as a function of distance *x* away from the bottom surface of a transmission line (i.e. microstrip line) on the substrate [28], which can be represented by the equation below:

$$J = J_0 \cdot e^{-x/\delta} \tag{3.8}$$

$$I = \int J \cdot dA = \int_0^t J_0 \cdot e^{-x/\delta} \cdot w \cdot dx \tag{3.9}$$

$$= J_0 \cdot w \cdot \delta \cdot (1 - e^{-t/\delta}) \tag{3.10}$$

where t is the thickness of the conductor.

The last term in the equation can be defined as an effective thickness:

$$t_{eff} = \delta \cdot (1 - e^{-t/\delta}) \tag{3.11}$$

$$R_s = \frac{\rho \cdot l}{w \cdot t_{eff}} \tag{3.12}$$

where l is the total length of line segments and ρ is the resistivity. It can be shown that as δ decreases with high frequency, R_s also increases. Figure 3.10 shows that as the copper thickness increases, the effective thickness increases accordingly, since it lowers the series resistance of the inductor and results in a higher quality factor of inductor. However, as the thickness increases, the RF resistance does not decrease monotonically with the thickness. As the thickness grows, the reduction in RF resistance is negligible. The RF resistance is low enough for copper thickness between 5-10 um in the frequency from 0.5 GHz or above.

Another curve-fitted numerical approach that takes the ground plane into consideration also combines the R_{dc} and R_{hf}, which gives a general solution of the R_{ac} [28]-[29] in terms of film thickness (t),

$$R_{ac} = R_s = \sqrt{[(R_{dc})^2 + (kR_{hf})^2]} \tag{3.13}$$

$$R_{ac} = R_s = \sqrt{[\left(\frac{1}{\sigma w t}\right)^2 + (k\frac{l}{2\sigma\delta(w+t)})^2]} \tag{3.14}$$

where R_{hf} is the ac resistance of the strip conductor at high frequency with equal circumference carrying a uniform current across its skin depth, and k is a correction factor.

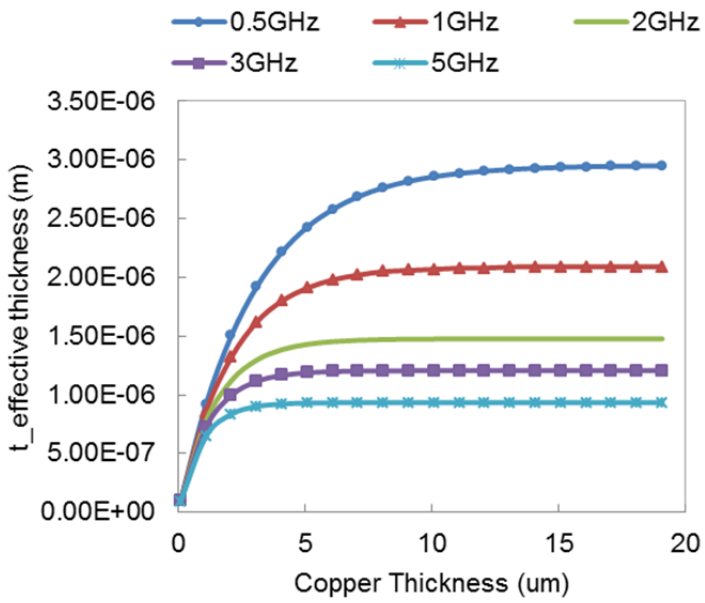


Figure 3.10 Effective metal thickness for different frequencies.

Series Capacitance

The series capacitance is the feed-through capacitive coupling between the input and output port of the inductor without passing through the spiral inductor. It is attributed to the crosstalk between the adjacent turns, and the overlap between the spiral and the underpass. Nonetheless, the potential of the adjacent turns is almost the same and is always neglected. On the other hand, because of the larger potential difference, the overlap capacitance between the spiral and the underpass is more significant. It is sufficient to model this series capacitance, C_s, as the sum of the overall capacitance [13], [30],

$$C_s = n \cdot w^2 \cdot \frac{\varepsilon_{\text{iso}}}{t_{\text{isoM1-M2}}}, \tag{3.15}$$

where n is the number of overlap, w is the width of the spiral line and t_{isoM1M2} is the isolation layer (polyimide) thickness between the spiral coil and the underpass.

Q-factor of an Inductor

In an ideal inductor, the energy is only stored in the magnetic field, and therefore the extra capacitance can be regarded as parasitic elements. Hence, the overall Q of an inductor can be simplified to [31]:

$$Q = 2\pi \left| \frac{\text{energy stored}}{\text{energy loss per one oscillatio n cycle}} \right| \tag{3.16}$$

$$Q = \frac{\omega L_s}{R_s} \times \underbrace{\frac{R_p}{R_p + \left[\left(\frac{\omega L_s}{R_s} \right)^2 + 1 \right] R_s}}_{\text{Substrate Loss Factor}} \times \underbrace{\left[1 - \frac{{R_s}^2 (C_s + C_p)}{L_s} - \omega^2 L_s (C_s + C_p) \right]}_{\text{Self-resonance Factor}} \tag{3.17}$$

where

$$R_p = \frac{1}{\omega^2 {C_{iso}}^2 R_{glass}} + \frac{R_{glass} (C_{iso} + C_{glass})^2}{{C_{iso}}^2} \tag{3.18}$$

$$C_p = C_{iso} \cdot \frac{1 + \omega^2 (C_{iso} + C_{glass}) C_{glass} {R_{glass}}^2}{1 + \omega^2 (C_{iso} + C_{glass})^2 {R_{glass}}^2} \tag{3.19}$$

and

$$C_{iso} = \frac{1}{2} \cdot l \cdot w \cdot \frac{\varepsilon_{iso}}{t_{iso}}, C_{glass} = \frac{1}{2} \cdot l \cdot w \cdot C_{sub} \text{ and } \mathrm{R}_{\text{glass}} = \frac{2}{l \cdot w \cdot G_{\text{sub}}}$$

R_{glass} and C_{glass} are the parasitic resistance and capacitance, respectively. Equation (3.17) shows that the Q-factor consists of three parts which are the intrinsic Q of the inductor, the substrate loss and the self-resonance factor. It can be observed that R_p is equal to zero if R_{glass} is infinity. Normally, R_{glass} is quite large compared with the silicon substrate, hence, it does not affect the overall Q-factor very much [9], [26] and [32].

3.5 Inductor Design Considerations

In order to optimize the IPD fabrication process for a high-Q inductor, some parameters have to be considered. Initially, the following parameters were initially selected: a copper (M2) thickness of 8 µm, an M1 of 1 µm, and an isolation layer of 4 µm. The results using those parameters give some insights on the experimental and simulated results obtained from the electromagnetic (EM) simulation software such as Sonnet and HFSS. Figure 3.11 shows a physical example for one-turn thick copper inductor whereas Figure 3.12 shows its simulated and experimental performance.

The Q and L extracted from the network are defined as:

$$Q = \left| \frac{\mathrm{Im}(1/Y_{11})}{\mathrm{Re}(1/Y_{11})} \right| \tag{3.20}$$

$$L_s = \frac{1}{2\pi f} \mathrm{Im}(\frac{1}{Y_{11}}) \tag{3.21}$$

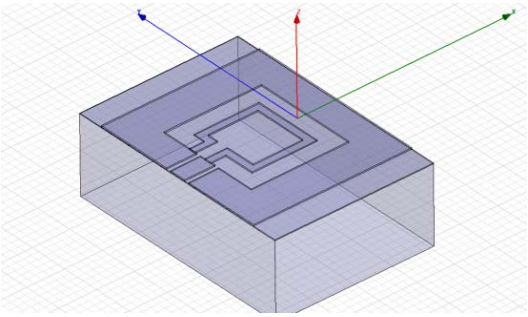
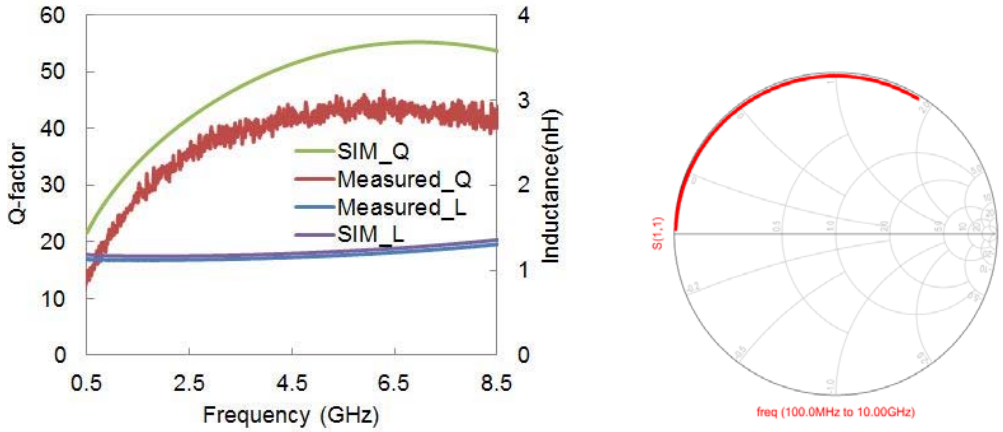


Figure 3.11 One-turn inductor (w: 50 µm and din=500 µm)



(a) (b)

Figure 3.12 (a) Measured and simulated Q-factor and inductance vs. frequency (5um thick copper) and (b) its Smith chart.

The equipment used for the on-wafer measurement is Agilent-N5242A PNA-X with Picoprobe GSG 150. In order to accurately measure the quality factor, a careful calibration is needed. Figure 3.12 shows that the measured inductance is well matched with the simulation, which is around 1.2 nH. However, the measured quality factor is not in agreement with the initial results. One of the main reasons for this discrepancy is the contact resistance (~0.04 ohm extracted from the modeling) between the probe and the transmission line. This induces of a higher series resistance in the inductor, which contributes to a variation of approximately 20% from the simulation results. The quality factor maintains above 25 from 1.3 GHz to 10 GHz and its maximum Q is around 45 at 6.2 GHz. It should be noted that, the probe pad is not deembedded in order to avoid overestimating the quality factor, which will be useful for designing passive circuits in the future.

Metal Width (W)

As discussed earlier, the wider the width of the transmission line, the lower the series resistance (especially for low frequency), which results in a higher quality factor, as shown in Figure 3.13. However, this does not mean that a larger metal width is always desirable, since it induces a larger area of the parasitic capacitance under the substrate, thereby resulting in a lower self-resonant frequency, as shown in Figure 3.14.

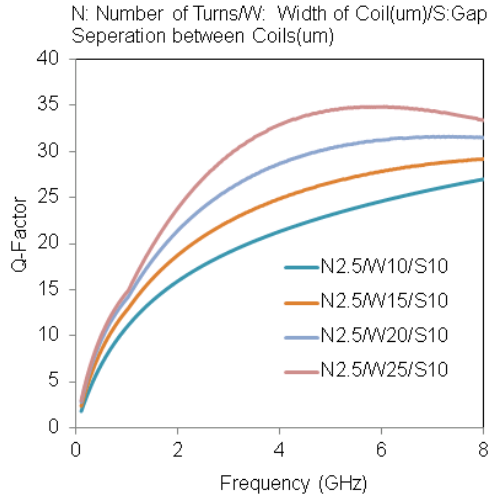


Figure 3.13 Simulated Q-factor vs width of the coil.

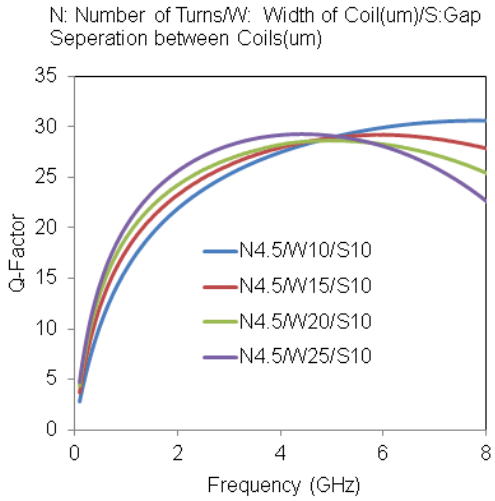


Figure 3.14 The self-resonant frequency decreases as the of the width of the coil increases.

The average distance of the inductor, $d_{avg,}$ = (din+dout)/2 (shown in Figure 3.11) increases as the metal width increases, and it brings a stronger magnetic coupling effect, therefore the inductance increases, as shown in Figure 3.15. The rate of change of the inductance is higher when the number of turns is higher, as shown in Figure 3.16.

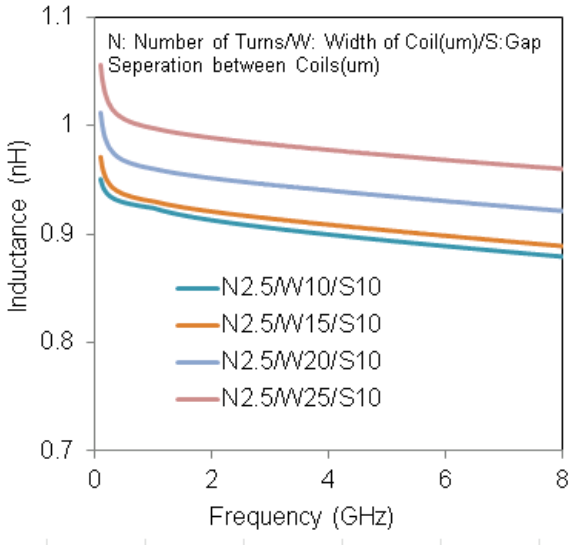


Figure 3.15 Change in inductance as the width of the coil increases for 2.5 turns.

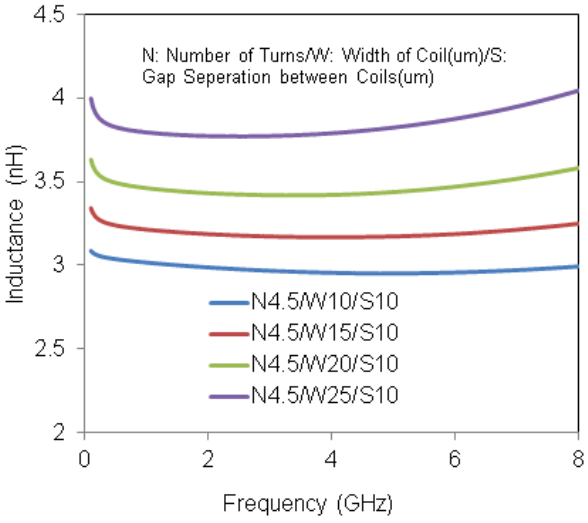


Figure 3.16 Change in inductance as the width of the coil increases for 4.5 turns.

Number of Turns (N)

As the number of turns increases, the inductance likewise increases because more magnetic energy is stored together in the coil. This is illustrated in Figure 3.17. However, if the number of turns reaches a saturation point, the Q-factor usually drops accordingly. This matches with the modeling for the series resistance, which induces higher energy loss and degrades the quality factor.

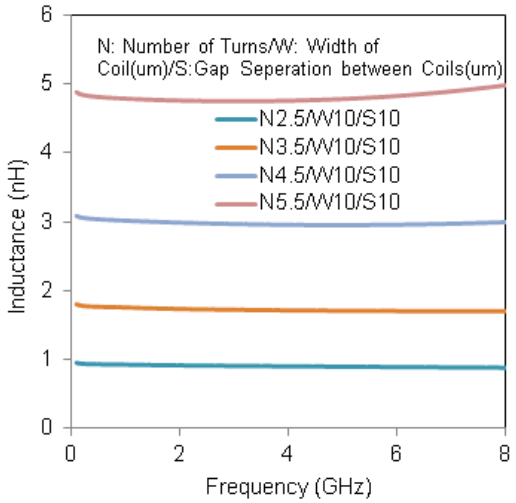


Figure 3.17 Inductance versus number of turns.

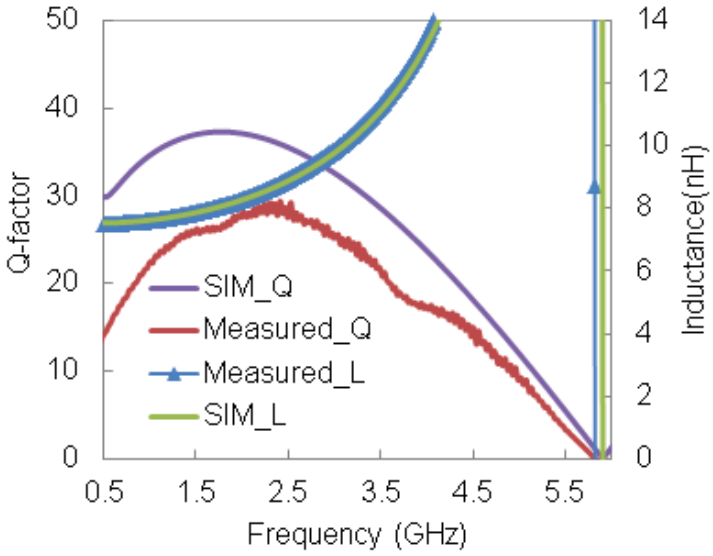


Figure 3.18 Measured and simulated Q-factor and inductance vs frequency (3.5 turns).

Figure 3.18 shows the simulated and measured results of the 3.5-turn inductor. The measured inductance value is well-matched with the simulation results. The maximum Q-factor is around 30 at 2.3 GHz, which is much higher than that of a similar inductor fabricated using a CMOS technology inductor. The contact resistance is not deembedded, which partly explains the discrepancy between simulated and measured results.

Thickness of Copper (t)

As discussed earlier, increasing the copper thickness helps boost the Q-factor of the inductor since it can lower the series resistance of the coil. To demonstrate this, several inductors with different thicknesses are simulated in HFSS. However, to make a fair comparison, the inductance and its area have to be approximately the same. The copper thickness and width is set to a constant (t+W=53 µm), and the aspect ratio of the separation and the copper thickness is constantly equal to 1. Figure 3.19 shows the variations between the simulated Q-factor and the copper thickness. As can be observed, that the Q-factor boost is increased significantly from t = 3 µm to 5 µm, but when t further increases to 10 µm or above, the Q-factor increase starts to slow. Therefore, 8-10 µm of copper is chosen as the target of our proposed process.

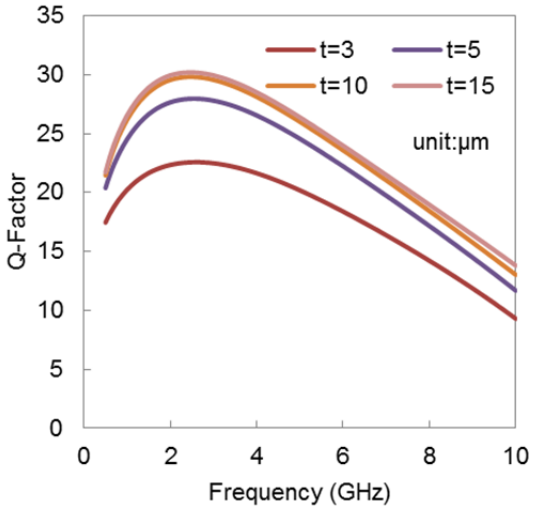


Figure 3.19 Simulated Q-factor vs copper thickness (N=2.5, din =160 µm).

3.6 Modeling and the Characteristics of the IPD Capacitor

To design an IPD capacitor, for simplicity, the thickness of the dielectric (Si_xN_y) is unchanged. The only variable is area, so the equation is $C=\varepsilon_0\ \varepsilon_r A_{overlap}/d$. In fact, the area is not directly proportional to the capacitance in the EM-simulation, because this equation does not account for the stray capacitance, especially for small value of capacitance (i.e., around 1 pF). Figure 3.20 and 3.21 show the geometry of the capacitor and its equivalent model.

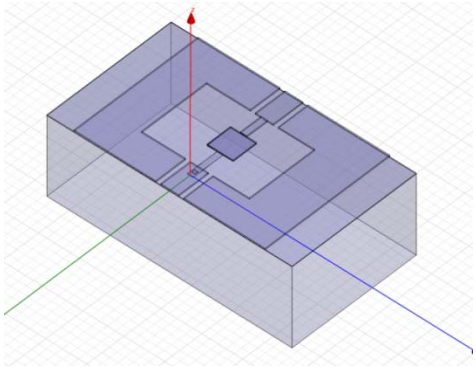


Figure 3.20 Geometry of the capacitor with an area of 120 μm^2.

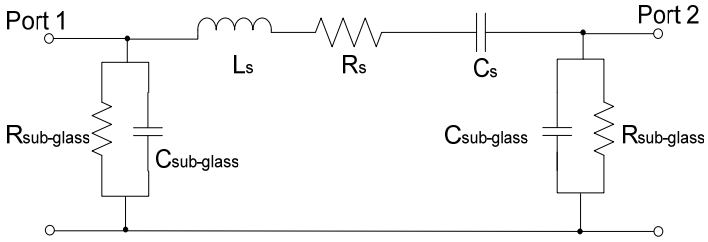


Figure 3.21 Equivalent model of the capacitor.

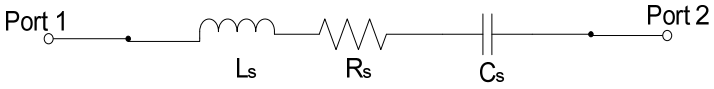


Figure 3.22 Simplified model of the IPD capacitor (ignoring the loss in the glass substrate).

L_s: Small inductance from the transmission line (with the conductor plates)

R_s: Loss from the upper and lower plates and part of the transmission line around the cap

C_s: Intrinsic capacitance from storing electric energy in the dielectric (Si_xN_y)

Since glass wafer is used for the IPD process instead of Si-wafer, the loss of the substrate is small enough that it can be neglected [33]. Hence, a simplified model, shown in Figure 3.22 can be used. Generally, the operating frequency is far away from the resonant frequency, therefore, it is assumed to be $\omega L_s << Z_{serie.}$, where Z_{series} is the overall impedance and port 2 is connected to ground, as shown below:

$$Z_{series} = R_s + j(\omega L_s - \frac{1}{\omega C}) \approx 1/Y_{11} \tag{3.22}$$

To extract the model parameters, the following equations can be used:

$$C_s = \frac{-1}{2\pi f \cdot \mathrm{Im}(\frac{1}{Y_{11}})} \tag{3.23}$$

$$L_s = \frac{1}{\omega C_s} = \frac{1}{2\pi f C_s} \tag{3.24}$$

$$R_s = \mathrm{Re}(\frac{1}{Y_{11}}) \tag{3.25}$$

$$Q = \left| \frac{\mathrm{Im}(Y_{11})}{\mathrm{Re}(Y_{11})} \right| \tag{3.26}$$

In order to characterize the dielectric constant of the capacitor, it is assumed to be 7.5 in the design. As the designed capacitance is around 1.8 pF, the measurements of the fabricated unit value are almost double what was expected. There are two reasons for this: the thickness is 0.2 μm thinner than the designed value, and the corrected dielectric constant for the silicon nitride is around 6.8. Figure 3.23 shows the frequency response of the corrected MIM capacitor from Figure 3.20. As its area is 120 μm^2, the measured capacitance and Q-factor are 3.57 pF and 70 at 1.8 GHz, respectively. To explain the Q degradation of the capacitor, the measured series resistance of this capacitance is extracted from the model, which is around 0.2 ohm. And after adding this parameter into the EM-simulation, the simulated and measured results are matched very well, as shown in Figure 3.24. The contact resistance

(copper oxide) can be as ascribed the major reason for this Q-factor degradation. The same method can also be used for explaining the degradation of the inductor.

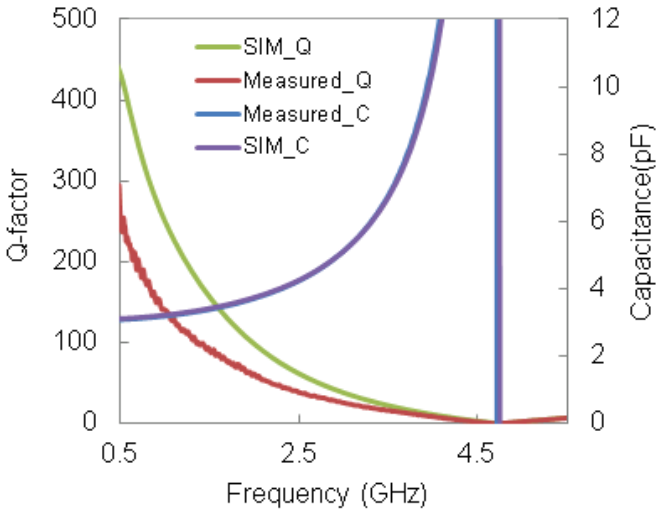


Figure 3.23 Frequency response of a 120 μm^2 capacitor (after correcting the dielectric constant).

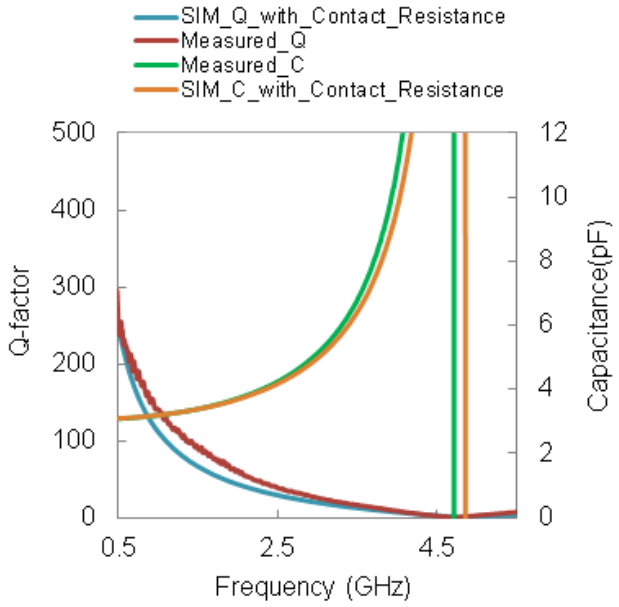


Figure 3.24 Corrected frequency response of a 120 μm^2 capacitor (with consideration of the copper oxide)

3.7 Modified Third-order Chebyshev Bandpass Filter

To show a substantial insertion loss difference between the IPD and regular CMOS process, a third-order Chebyshev filter operating at 1.8 GHz is designed. Its schematic is shown in Figure 3.25. The g values for third-order with passband ripple (L_{Ar} = 0.04321 dB) are determined as g_0=g4=1, g_1=g_3=0.8516 and g_2=1.1032. After the impedance scaling transformation for the bandpass filter, the values of L_{series}, C_{series}, $L_{parallel}$ and $C_{parallel}$ can be calculated.

The circuit is simulated by ADS, with consideration of the Q-factor of the lumped element. Figure 3.26 shows the frequency response comparisons among all the configurations, such as using ideal, IPD, and CMOS lumped elements at the center frequency 1.8 GHz. Compared with the SOI CMOS 65nm technology [34], the standard Q of the inductor is approximately 10 at 1 nH. In order to compare the IPD and CMOS process, the Qs of the passive elements provided in [35] are used. The circuit simulation shows that the in-band insertion loss of our proposed IPD BPF (with Q-factor consideration) is around 1 dB whereas the one in the CMOS technology is around 4 dB, as shown in Figure 3.27. A smaller insertion loss of bandpass filter at the early stage in the RF system is always desirable, since it can improve the overall system noise figure and obtain better sensitivity in the receiver.

To demonstrate our proposed IPD process, this third-order Chebyshev filter is modified by adding an optimized value of inductor (L_a) at the shunt resonator so that a transmission zero is obtained. The schematic is shown in Figure 3.28. This transmission zero not only enhances the roll-off effect, but also can be tuned to increase the rejection at a particular frequency (e.g. the 2nd harmonic of the bandpass filter), as shown in Figure 3.29. More importantly, this inductor does not consume any extra area of the overall filter, as it is only a short transmission line between the L_2-C_2 shunt resonator.

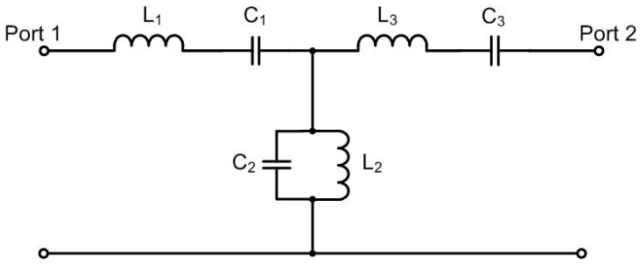


Figure 3.25 Schematic diagram of the third-order Chebyshev bandpass filter.

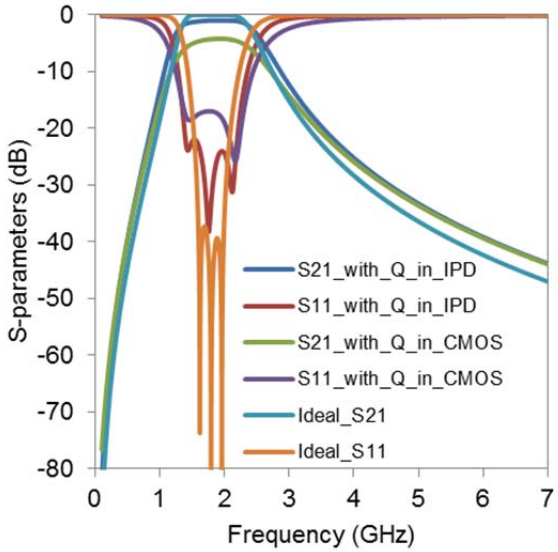


Figure 3.26 Frequency response of the third-order Chebyshev filter, with comparisons of the lumped elements in ideal, IPD and CMOS platforms.

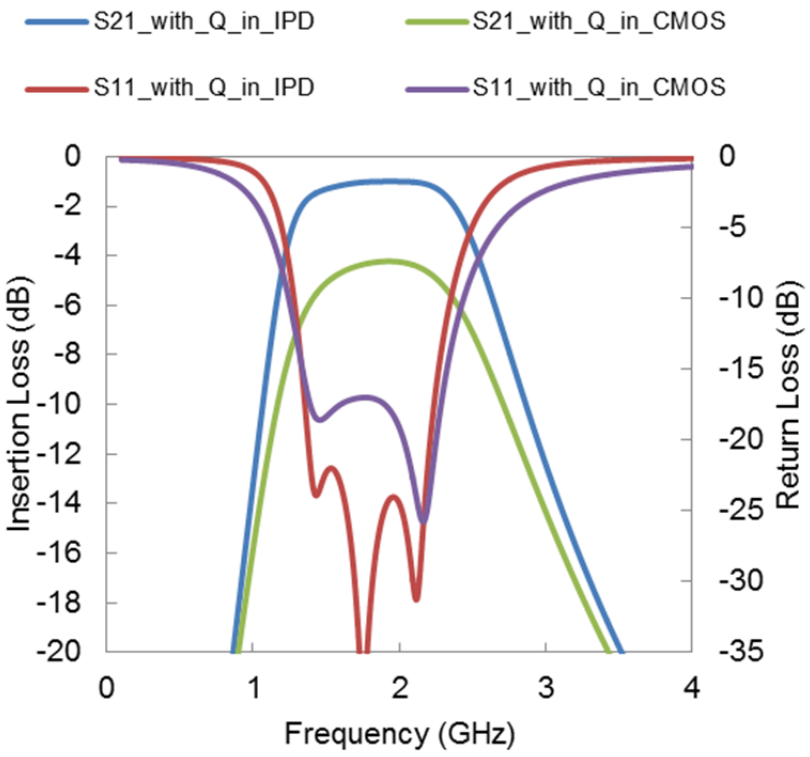


Figure 3.27 Comparison of the insertion loss between high-Q L-C elements in IPD (blue) and SOI CMOS 65nm process (green)

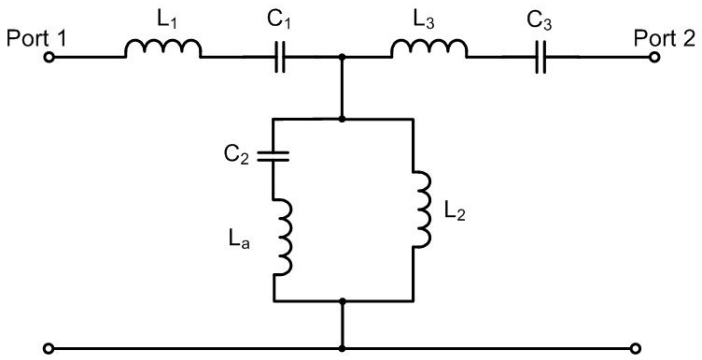


Figure 3.28 Schematic of the modified third-order Chebyshev bandpass filter, with an extra inductor (La) at the shunt resonator.

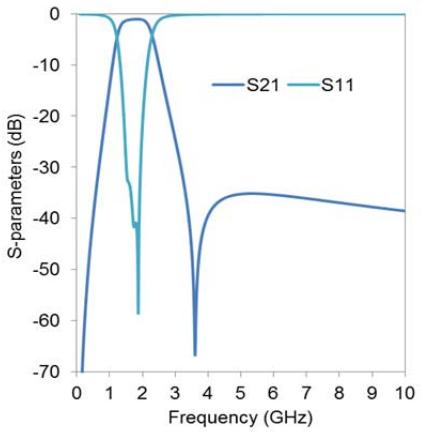
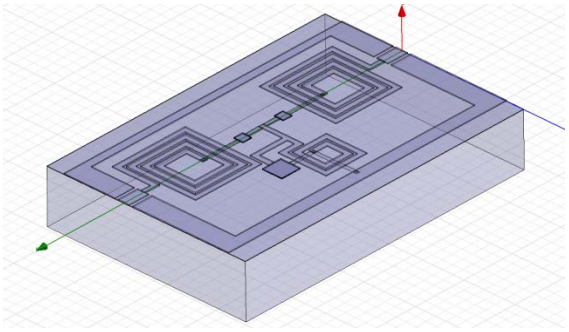
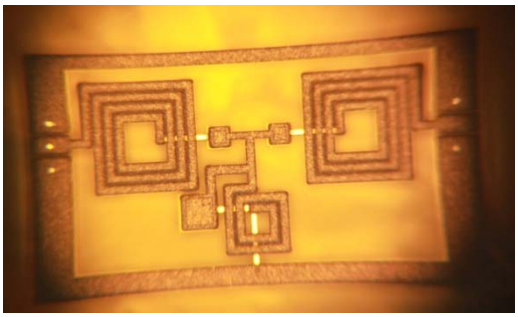


Figure 3.29 Frequency response after adding the small inductor.

Figure 3.30 shows the layout of the BPF in our proposed IPD process. The EM-simulated results indicate that the insertion loss for the in-band response is around 1 dB, with a wide 15-dB rejection from 1.5 GHz to 8 GHz, as shown in Figure 3.31. The EM-simulated and measured results are shown Figure 3.32. As can be seen, both results agree very well with each other across a wide frequency range. The measured insertion loss is between 1.2 - 1.4 dB, while a 20-dB return loss can be achieved from 1.45 GHz - 1.9 GHz. Furthermore, the transmission zero is at around 2.3 GHz, with a 25-dB rejection level. A wideband 20-dB rejection is achieved from 3 GHz to 8 GHz.



(a)



(b)

Figure 3.30 Layout of proposed IPD bandpass filter. (a) 3D structure in EM simulation. (b) Final modified third-order Chebyshev bandpass filter developed in CIRFE at the University of Waterloo.

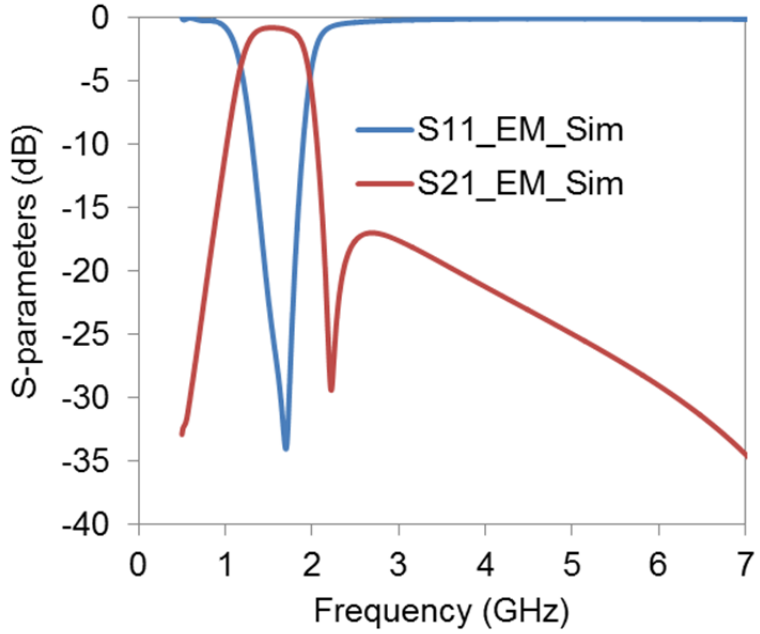


Figure 3.31 EM-simulated frequency response of bandpass filter (S21: ~ -1dB).

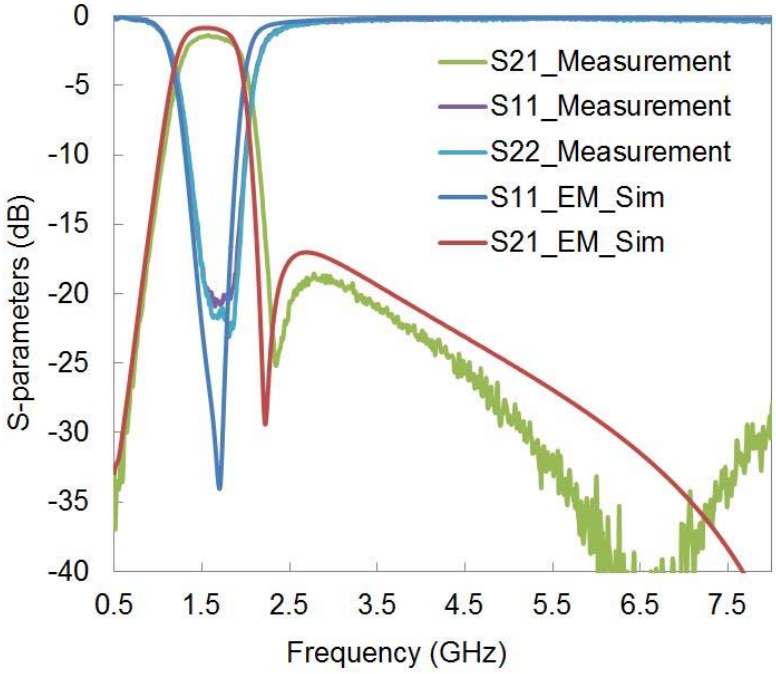


Figure 3.32 Measured and simulated results of modified third-order Chebyshev bandpass filter.

In the IC development process, it is important to lower the possibility of electromigration failure which is a momentum of the conduction electron flows to the metal atoms in the interconnections. As a result, there may be voids or open/short circuits around the metal layer [36]. In order to test the failure rate/simplified reliability of our proposed IPD circuit, an RF measurement is performed on the same 3-year old wafer at room temperature. An almost identical RF performance of the IPD bandpass filter is obtained without any sign of electromigration, which validates the reliability of our proposed IPD process, as shown in Figure 3.33.

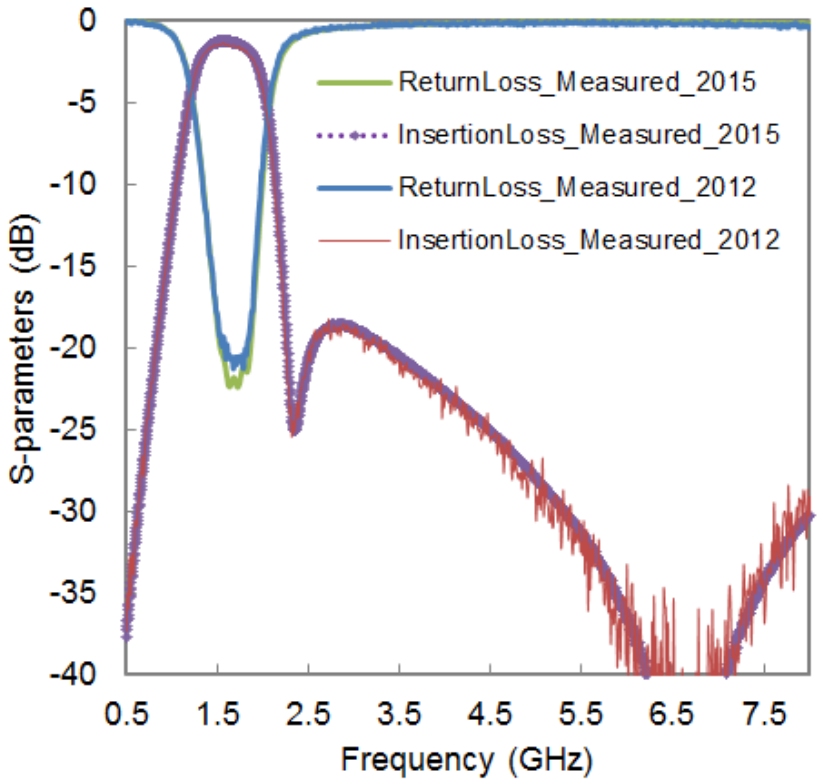


Figure 3.33 Measured results comparison of our proposed IPD bandpass filter between the year of 2012 and 2015.

By using a similar configuration to the modified third-order Chebyshev bandpass filter, an IPD bandpass filter with two transmission zeros operating at 1.6 GHz is designed. Its

schematic diagram is shown in Figure 3.34. C_p and C_2 are the main values to control the location of the transmission zero so that a wide rejection band can be achieved. This circuit is fabricated by a commercial foundry ON Semiconductor, as shown in Figure 3.3, while a photo of an 8" wafer that includes all of the designed circuits is shown in Figure 3.36. In the IPD process diagram illustrated in Figure 3.37, a maximum of three metal layers can be used. The top two metal layers are 5 μm thick copper, whereas

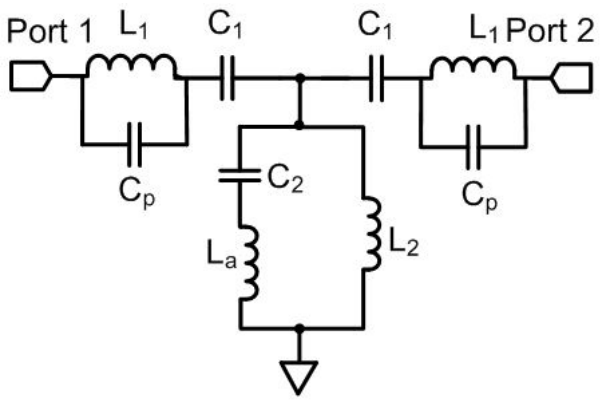


Figure 3.34 Schematic of third-order bandpass filter with an extra inductor at the shunt resonator.

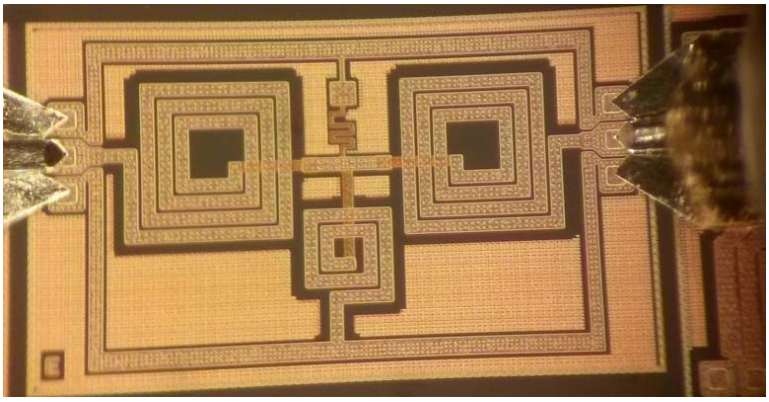


Figure 3.35 Picture of modified third-order Chebyshev bandpass filter fabricated by ON Semiconductor.

the bottom one is a regular 2 μm aluminum metal. Titanium nitride (TiN) and silicon nitride (SiN) are used as their resistor layer and capacitor layer, respectively. The frequency performance is plotted in Figure 3.38, indicating that the overall RF performances between the EM-simulated and measured results match relatively well.

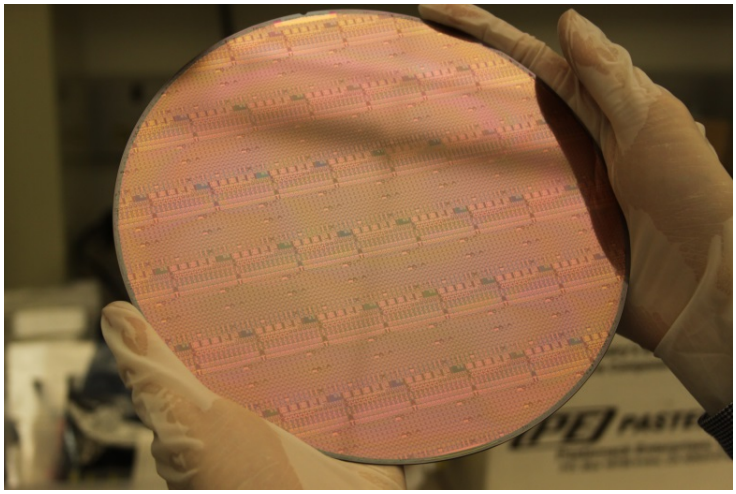


Figure 3.36 Picture of an 8-inch IPD wafer fabricated by ON Semiconductor.

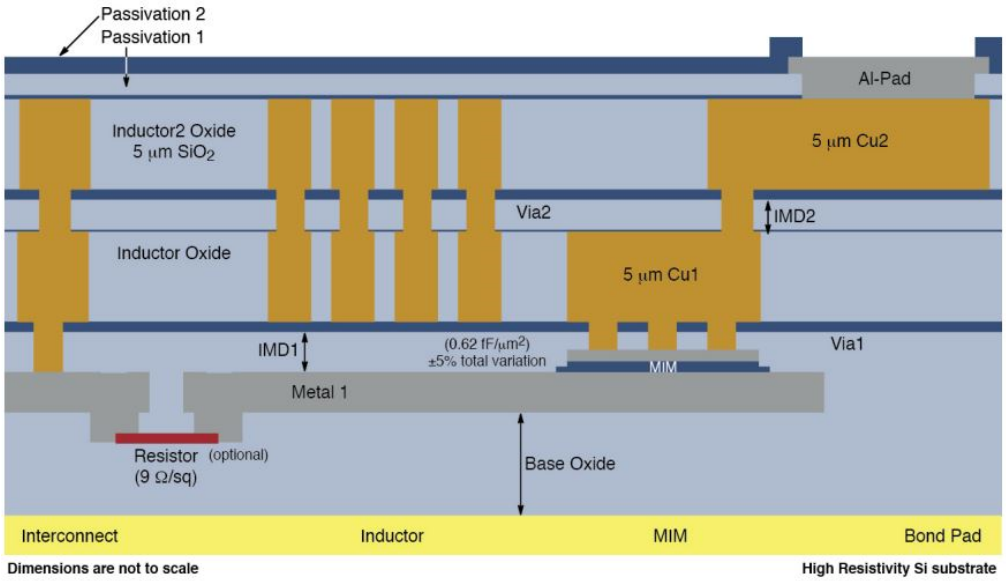


Figure 3.37 IPD layer process diagram from ON Semiconductor.

The measured insertion loss is around 2.5 dB and the 10-dB impedance bandwidth is 20%. The small discrepancy comes from a slight change in C_2 from the fabrication. This pushes the transmission zero from around 3 GHz to 2.7 GHz, whereas the other transmission zero is located around 4.6 GHz. In general, a good 20-dB wideband rejection is achieved from approximately 2.3 GHz to 8 GHz. A reconfigurable bandpass filter with tunable transmission zero can be developed based on this filter configuration. This will be discussed in detail in Chapter 4.

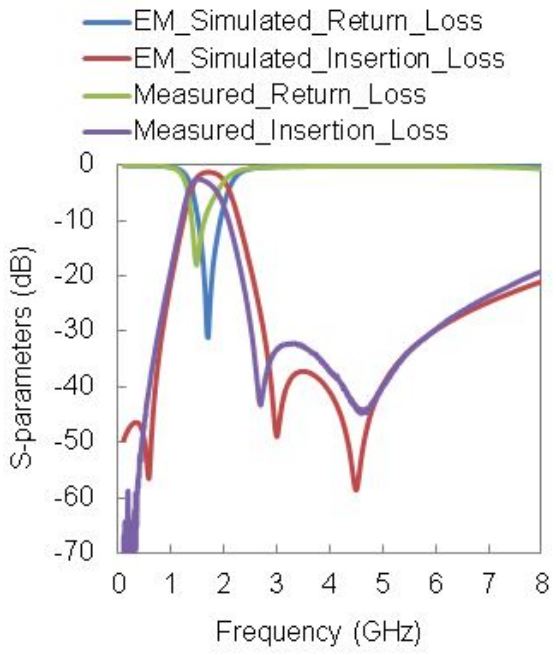


Figure 3.38 Frequency performance of EM simulated and measured results.

3.8 Impedance Tuner

Impedance matching networks (IMNs) are attractive to many RF applications, such as source/load-pull characterization [37], and rapid impedance matching between an antenna and the front end circuits in an unknown environment [38], as shown in Figure 3.39. Having a continuously tunable impedance-matching for an antenna is especially important in modern

communication systems (3G/4G+/LTE), since it can adaptively change the impedance according to the surrounding environment. In so doing, the radiation efficiency of the antenna can be enhanced while the bandwidth can still be maintained under the stringent requirements of the wireless standards. One of the challenges for antenna-tuning in modern communication systems is the wide operating frequency band with continuously changing of impedance. For instance, the LTE scheme has more than 30 frequency bands that are

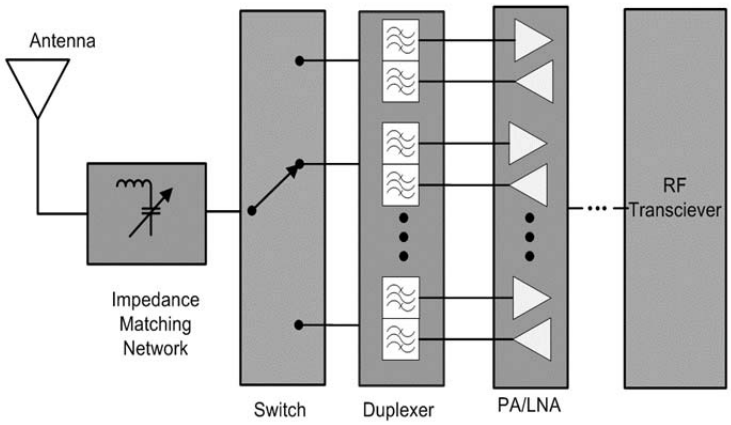


Figure 3.39 Possible RF front-end configuration.

allocated for data transmission. Moreover, a wide and continuous impedance coverage with a small form factor is always desirable, as this may enhance the chance of matching an unknown load so as to minimize any losses due to impedance mismatch.

Different impedance tuning approaches have been proposed to achieve impedance tuners. In [39]-[40], good impedance coverage is obtained using transmission line-based resonators to replace lumped inductors. However, the size becomes very large when frequency is below 4 GHz. In [41]-[42], CMOS-SOI technology is used to reduce the dielectric loss of the impedance tuner. Nonetheless, in order to have a relatively high-Q inductor to reduce the insertion loss, the thin metal loss still remains an issue when metal thickness is comparable to scales of skin-depth. Off-chip discrete lumped elements are good candidates for implementing IMN since the Q can be higher than in those implemented in regular CMOS

processes. However, the size and the parasitics that can adversely affect the circuit performance are always a concern.

On the other hand, the integrated passive device (IPD) is a compact thin-film technology that uses thick metal to provide high-Q lumped elements, which leads to low-loss RF performance. This feature of the IPD is important in many system-in-packages (SIPs) and RF multi-chip modules (MCMs) for the latest mobile devices. Hence, in the following section, a continuous impedance tuner using BST varactors is proposed with our in-house developed alumina-based IPD process. Some high-Q lumped elements such as capacitors and inductors are also tested and demonstrated experimentally.

3.8.1 Design of Impedance Tuner Using Alumina-based IPD Process

A similar fabrication process, mentioned in section 3.3, is used for implementing this impedance tuner. However, an alumina wafer is used, since a low-loss performance is always preferred in designing an impedance tuner.

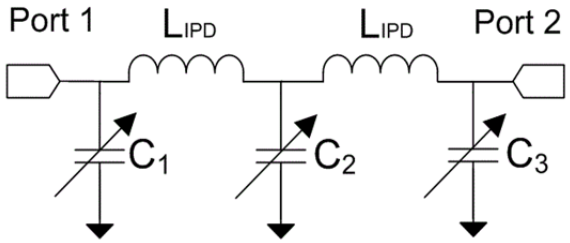


Figure 3.40 Schematic of the proposed impedance tuner with our developed IPD process and BST varactors.

The schematic of our proposed IPD impedance tuner using the BST varactors as tuning elements is shown in Figure 3.40. It consists of three capacitors (C_1, C_2 and C_3) connected in a shunt configuration with series IPD inductors (L_{IPD}) placed between the capacitor branches. In order to achieve a low loss and wider impedance coverage, a two-stage low-pass configuration is chosen in our design. A BST varactor offers a good continuous step tuning such that a finer capacitance choice for impedance matching can be achieved. The BST

varactors (TCP-3027H from ON Semiconductor [43], with an approximate measured capacitance range of 1.3-5 pF at 2 GHz), are used with an AIPD inductor of 3.5 nH to realize an impedance tuner over the frequency range of 2-3 GHz. Electromagnetic (EM) simulations are performed in SONNET [44], with considerations of the inductor, the capacitor pads and the bias circuits. The 3D diagram of the structure is shown in Figure 3.41. The photos of our proposed IPD impedance tuner with and without the flip-chip BST varactors are shown in Figure 3.42 (a) and (b) respectively. In order to reduce the loss, the top metal is mainly used for most of the signal routing. The BST varactors are mounted on the copper pads using a flip-chip machine. Compared with semiconductor varactors and MEMS switched-capacitor, BST varactors require no complicated DC bias networks, and therefore, the overall circuit size can be minimized.

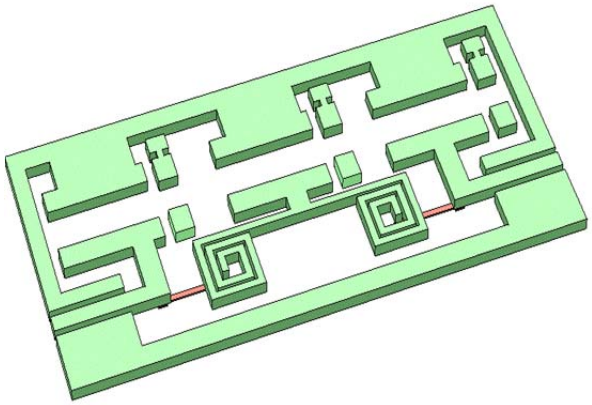
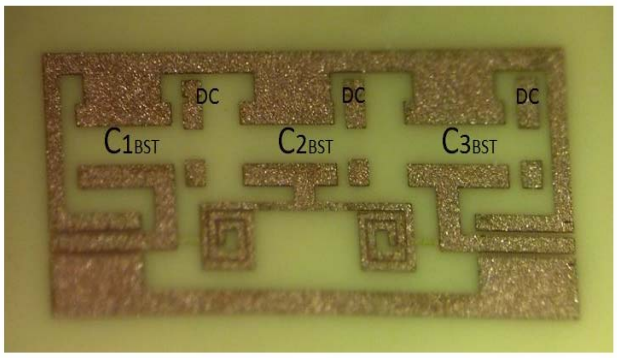


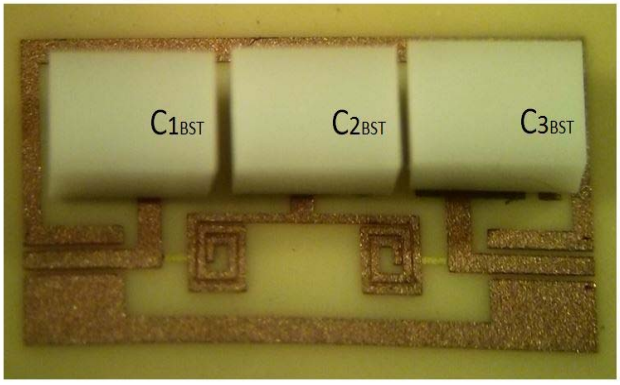
Figure 3.41 3-D diagram for EM simulation. *z-dimension not to scale.

3.8.2 Measurement Results

The impedance tuner is measured using the N5242A PNA-X network analyzer. On-wafer measurements are performed with varactor Picoprobe (150 μm-pitch GSG probes). The Q-



(a)



(b)

Figure 3.42 Proposed IPD impedance tuner (a) without BST varactors and (b) with BST varactors. *size: 3.8 mm x 1.88 mm (with DC pads).

factor is at least 30 within that frequency range. The EM simulated and the corresponding measured impedance coverages on the Smith chart at 2, 2.7 and 3 GHz are plotted in Figure 3.43 (a)-(f). The 40 measured data points agree very well with the simulated results and indicate that very good coverage is achieved. In order to evaluate the insertion loss of the impedance tuner, the unit is tested at three different frequencies. Figure 3.44 shows the measured insertion and return loss from 2 to 3 GHz. A 1-1.3 dB insertion loss is obtained with at least a 35-dB return loss over a 50 MHz bandwidth at any frequency within this wide frequency range.

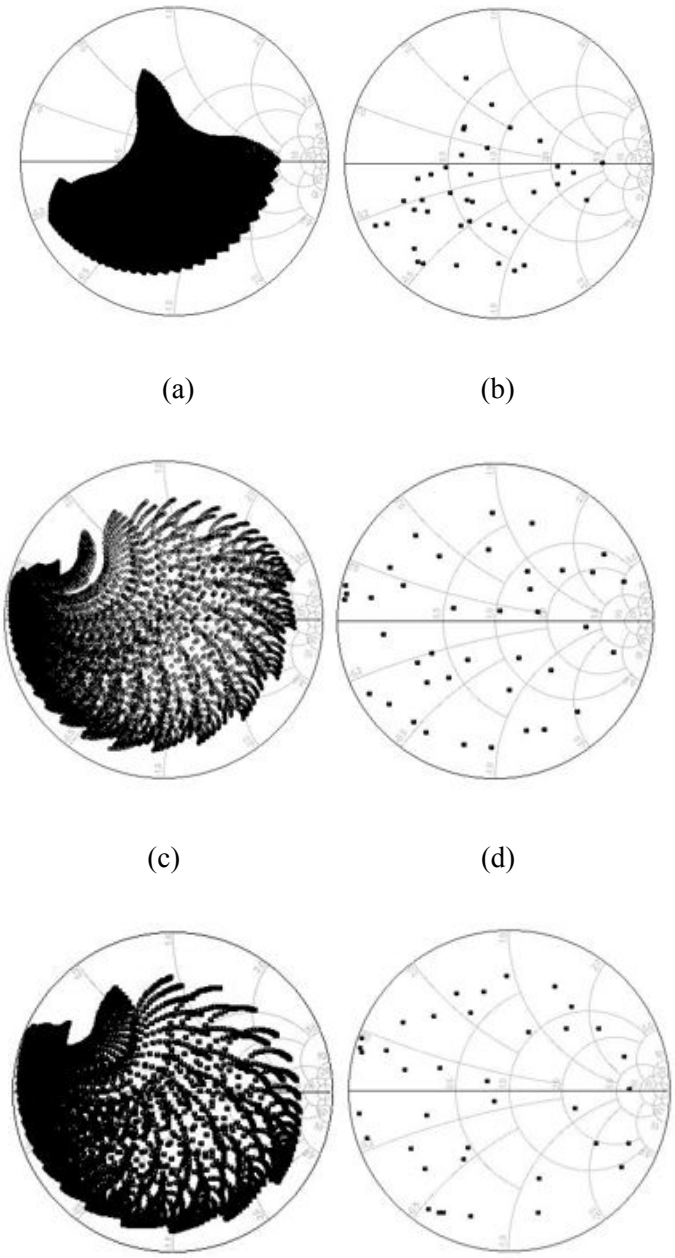


Figure 3.43 Simulated and measured impedance coverage at different frequencies. (a) Simulated and (b) measured results at 2 GHz. (c) Simulated and (d) measured results at 2.7 GHz. (e) Simulated and (f) measured results at 3 GHz.

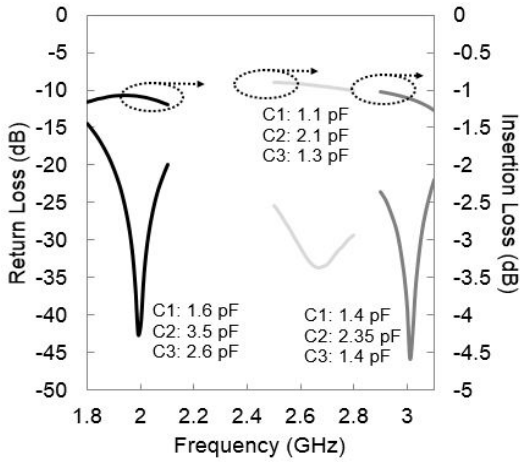


Figure 3.44 Measured insertion loss and return loss when it is terminated at 50-ohm at both ports at different frequencies.

3.9 Summary

In this chapter, the design of our proposed 4-mask IPD glass/alumina process fabricated at the University of Waterloo, and its lumped-elements modeling consideration including inductor and capacitor are described in this chapter. The measured results of the characterizations are also discussed, and a modified third-order Chebyshev bandpass filter using our proposed IPD process is also designed and tested. A repeated on-probe measurement shows an almost identical RF performance with our filter, which strongly verifies the reliability of our proposed IPD process. A similar configuration of the bandpass filter is also designed and later fabricated by the commercial company, ON Semiconductor. The measurement results show that a 1-dB improvement for the in-band insertion loss is achieved for our IPD process.

Additionally, a highly miniaturized impedance tuner using BST varactors has been designed, fabricated, and tested. This small- sized impedance tuner has demonstrated a wide impedance coverage over a frequency of 2-3 GHz while achieving an insertion loss of approximately 1-dB. Because of the combined unique features of wide-range coverage, miniaturization and insertion loss, the proposed IPD impedance tuner promises to be useful in across a broad range of wireless applications.

CHAPTER 4

RECONFIGURABLE/TUNABLE INTEGRATED PASSIVE DEVICES (IPD) BANDSTOP AND BANDPASS FILTER WITH WIDEBAND BALUN USING BARIUM STRONTIUM TITANATE (BST) VARACTORS

4.1 Introduction

Reconfigurable RF filters are attractive for use in advanced and emerging RF applications [45]-[46]. In particular, there is an increasing interest for employing tunable/reconfigurable bandstop filters (BSF) in systems that use carrier aggregation [47] and [48] or multiband systems [49]-[52]. In comparison with tunable bandpass filters, BSF usually provides a good passband insertion loss and thus offers a better front-end noise figure. BSF can also be potentially employed to suppress intermodulation products generated by nonlinearities in the system or by interference generated by other systems operating in a nearby band.

Over the past years, different approaches of achieving tunable BSF (< 4 GHz) have been proposed using PIN diodes [53], BST varactors [54], GaAs-based varactors [55]-[56] and MEMS [57]. A bandstop filter with defected ground structure (DGS) using BST varactors is

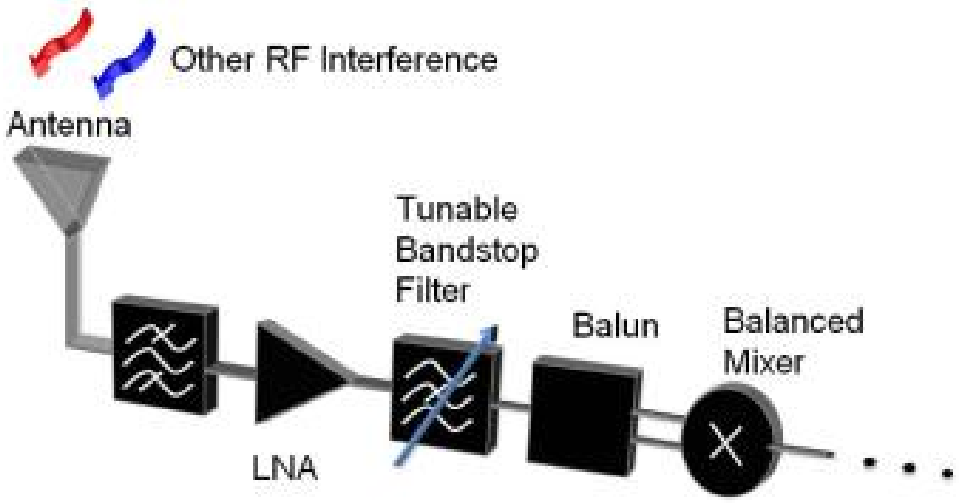


Figure 4.1 Block diagram of a possible RF front-end configuration.

reported in [54]. However, it is bulky and the filter demonstrated a limited tuning range. Most of the results reported in the literature on tunable bandstop filters use microstrip transmission-line resonators with sizes that preclude their use in many applications that demand highly miniature front-end components. Figure 4.1 shows a block diagram for a possible RF front-end configuration. In a balanced system, a balun is a crucial device in a balanced system and its main function is to transfer a signal from single-ended to differential ports. Sufficient operating bandwidth is needed for some applications, for instance, maintaining a balanced mixer with a good noise figure and low level of spurious output [58]. To design a wideband balun, one popular approach is to change the field direction from a single-ended/unbalanced transmission line to a balanced transmission line [59]. A wideband performance can undoubtedly be accomplished by having long transitions. However, the size constraints may limit their low frequency (<4 GHz) applications in RFIC. Some configurations are proposed using highpass and lowpass lumped-element structure or multiple units in a lattice balun [60]-[61]. Nevertheless, they exhibit high loss and a relatively narrow bandwidth. Integrated passive device (IPD) technology is a good platform that provides a compact and relatively high-Q lumped element solution. One of the main advantages is the thick copper metal that exceeds the skin depth at low frequency. Also, a

high resistivity substrate is usually used in IPD, which minimizes the induced parasitic capacitances. The compatibility of integrating IPD into the system-in-package (SIP) or system-on-chip (SOC) environment using multi-chip modules (MCMs) is also a desired feature in applications that have stringent size requirements [62]-[63].

Figure 4.2 illustrates the ON Semiconductor IPD process which is used to fabricate the devices reported in this chapter. The multilayer process includes one aluminum layer and two thick copper layers which can be used to build lumped element L, C and R. Silicon nitride (0.62 fF/μm^2) and titanium nitride (9 Ω/sq) are used as the dielectric layer for metal-insulator-metal capacitor and resistor, respectively. Details on this process can be found at [64].

In this chapter, a multi-chip module (MCM) tunable bandstop filter with a wideband balun is presented with a detailed analysis and EM simulations for the proposed tunable bandstop filter [65]. High power tests are carried out and are included here in this chapter to determine the high linearity performance of the BST-based tunable filter. The wideband IPD phase inverter in the balun is discussed in detail, along with its equivalent circuit. Designs and test results are also presented in this chapter for a fixed IPD bandpass filters, and for an IPD bandpass filter with a tunable transmission zero to demonstrate the reconfigurability. Two approaches for realizing tunable notches, with and without a balun, are discussed and compared for frequency agile applications.

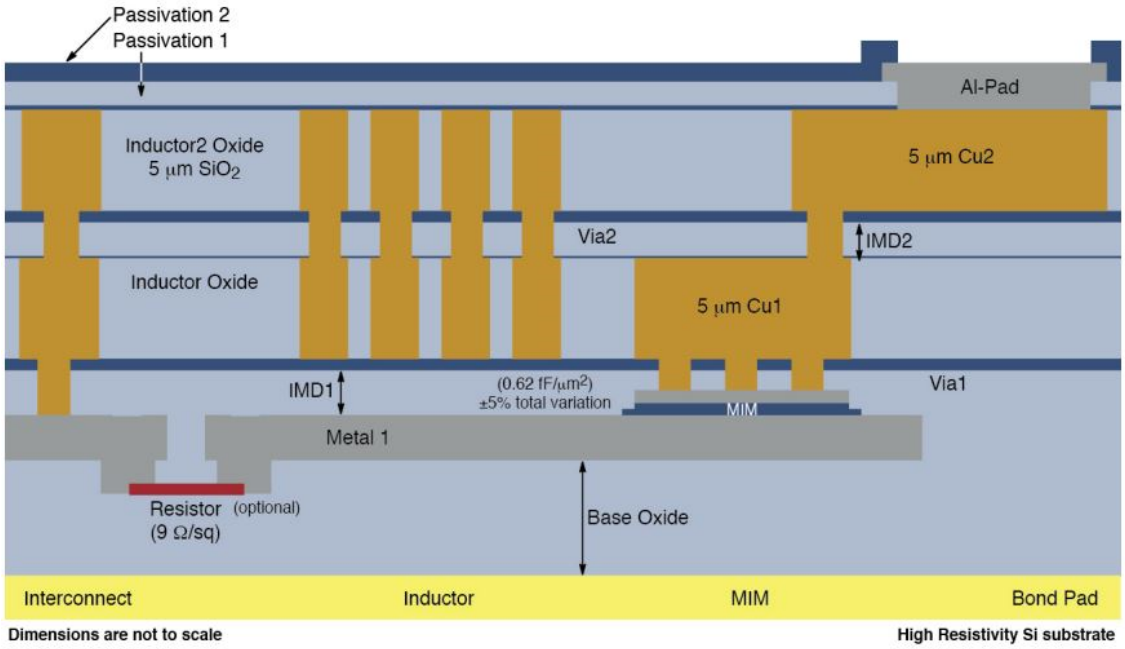


Figure 4.2 ON Semiconductor IPD process.

4.2 Barium Strontium Titanate (BST) Varactor

Barium Strontium Titanate (BST) material has become increasingly over the past few years, both in the research community and in industry. One of the reasons is that it has a very high dielectric constant (thin film >100) which can be tuned by applying different electric field with the corresponding input voltage. Furthermore, BST-based varactor offers a relatively low RF loss and requires a small area for bias network. It also has very small current leakage and high tuning speed, and features a truly tunable capacitance compared with other types of digitally-tunable capacitors (DTC). Table 4.1 shows a comparison of tunable elements. Figure 4.3 shows the picture of a BST varactor from ON Semiconductor.

TABLE 4.1 COMPARISON OF TUNABLE RF ELEMENTS

	GaAs	MEMS	BST
RF Loss	High	Low	Low
Power Handling	Poor	Excellent	Excellent
Tunability	High	Low	Moderate
Tuning Speed	Fast	Slow	Fast
Control Voltage	Low	High	Low
Size (incl. bias network)	Moderate	Moderate	Smallest
Reliability	High	Moderate	High
Cost	Moderate	Low/Moderate	Moderate/High

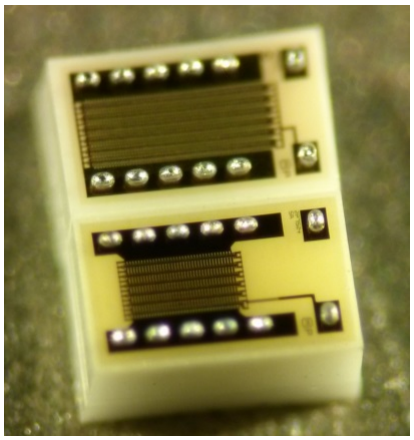
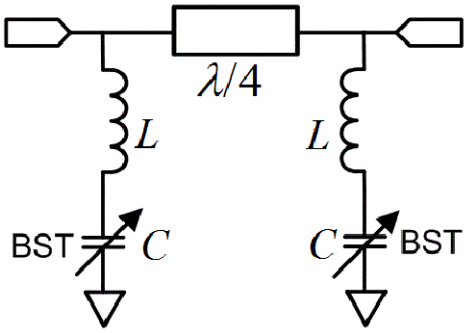


Figure 4.3 BST varactor from ON Semiconductor.

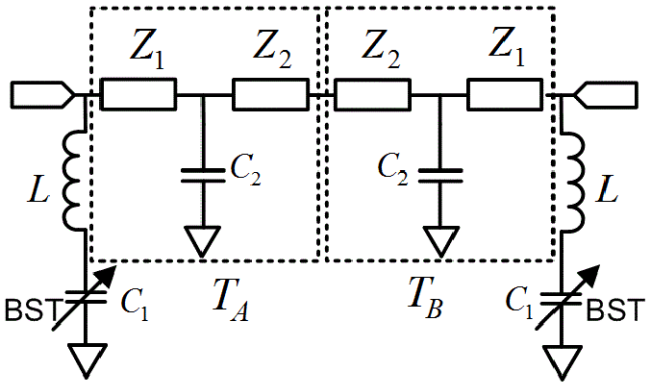
4.3 Compact Tunable Bandstop Filter Using BST Varactors

4.3.1 Design Structure and Operation

Figure 4.4 (a) illustrates a traditional circuit design for a bandstop filter which consists of two resonators connected by a $\lambda/4$ transmission line. The schematic of the proposed tunable filter is shown in Figure 4.4 (b). Instead of using a $\lambda/4$ transmission line, shorter transmission lines loaded with high-Q capacitor are used to miniaturize the circuit size. To analyze the circuit, networks (T_A and T_B) are used to replace the $\lambda/4$ transmission line. Each T-network consists of two short transmission lines centered at 2 GHz and a capacitor, and evaluated to simulate a $\lambda/8$ transmission line. To obtain the initial values, the ABCD matrix of the



(a)



(b)

Figure 4.4 Tunable bandstop filter. (a) A traditional tunable BSF using 90-degree transmission line. (b) Proposed miniaturized IPD BSF using distributed and lumped elements.

network T_A can be modeled as a $\lambda/8$ long transmission line:

$$\begin{pmatrix} A & B \\ C & D \end{pmatrix}_{T_A} = \begin{pmatrix} \cos\theta & jZ_1 \sin\theta \\ jY_1 \sin\theta & \cos\theta \end{pmatrix}$$

$$\begin{pmatrix} 1 & 0 \\ Y & 1 \end{pmatrix} \begin{pmatrix} \cos\theta & jZ_2 \sin\theta \\ jY_2 \sin\theta & \cos\theta \end{pmatrix} = 1/\sqrt{2} \begin{pmatrix} 1 & jZ_o \\ jY_o & 1 \end{pmatrix} \quad (4.1)$$

After some manipulation, Equation (4.2) and (4.3) can then be obtained as follows:

$$\cos^2\theta - \omega C_2 Z_1 \sin\theta \cos\theta - Z_1 Y_2 \sin^2\theta = 1/\sqrt{2} \quad (4.2)$$

$$\sin\theta \cos\theta [Z_1 + Z_2] - Z_1 Z_2 \omega C_2 \sin^2\theta = Z_o/\sqrt{2} \quad (4.3)$$

The elements of the T-network are obtained by forcing the |S21| of the BSF to be zero along with Equations 4.2 and 4.3. Optimization is carried out to obtain the physically realizable values that meet the RF performance requirements. It should also be mentioned that the goals of this BSF configuration are optimized so that a wide tuning range, good pass-band and rejection level performance, and compact chip-size can be realized. Table 4.2 shows all of the design parameters of the BSF, including the impedance (Z_1 and Z_2) and the electrical length (θ) of each transmission line, the inductor (L), the fixed capacitance (C_2) and the capacitance range of the BST varactor (C_1). Figure 4.5 shows the simulated phase response between a section of a 90-degree transmission line and the two cascaded T-networks. As can be seen, the phase response is well-matched over a wide frequency range from 0.1-5 GHz.

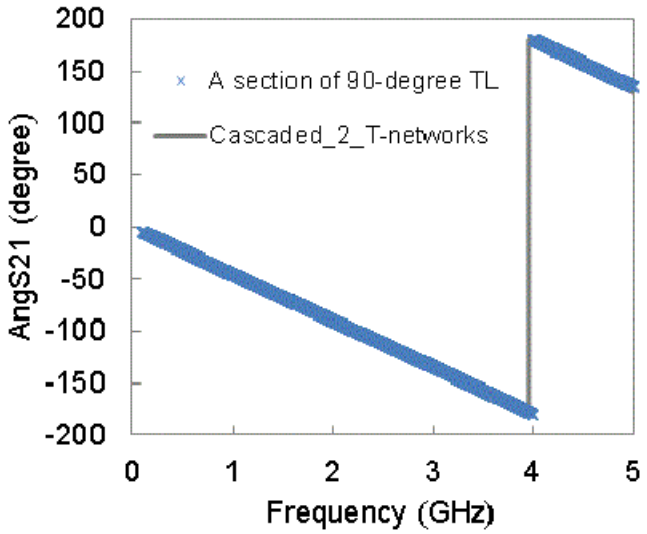
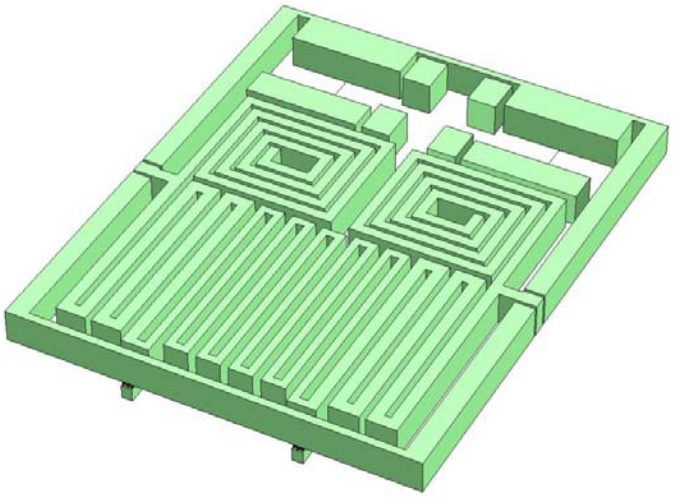


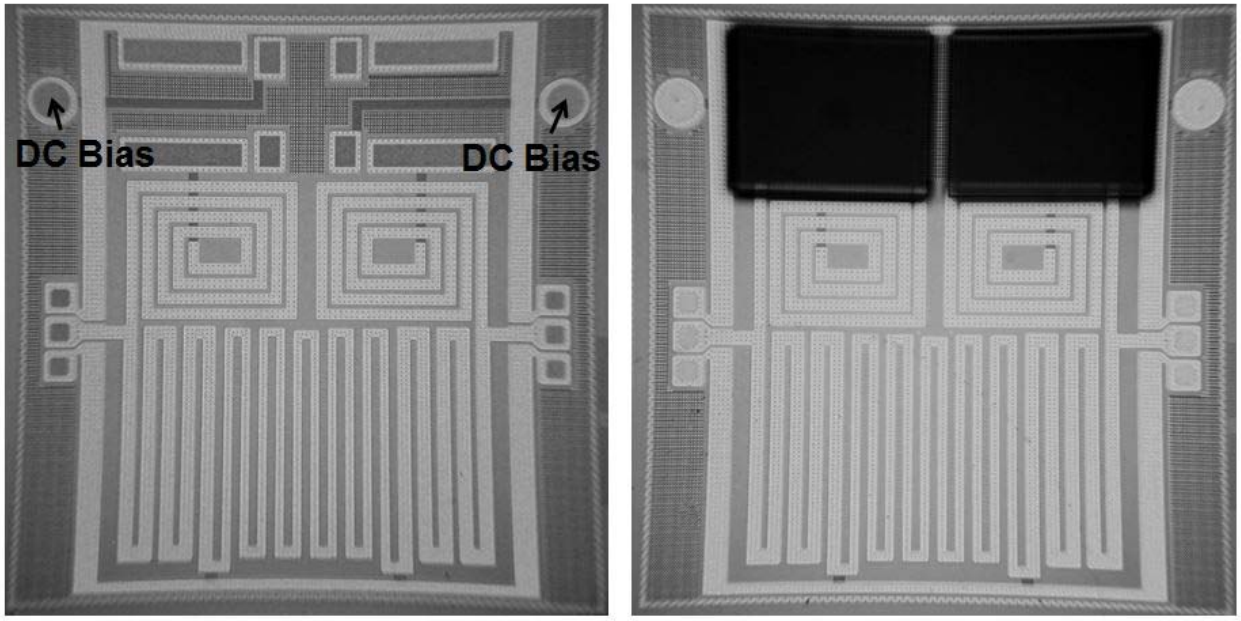
Figure 4.5 Simulated phase response between the two cascaded T-networks and one section of a 90-degree transmission line.

TABLE 4.2 DESIGN PARAMETERS FOR IPD TUNABLE BANDSTOP FILTER

Z_1	Z_2	C_2	L	C_1	θ
60 Ω	90 Ω	0.5 pF	9.35 nH	0.4-1.4 pF	16^o



(a)



(b) (c)

Figure 4.6 Picture of tunable IPD bandstop filter. (a) 3D- structure* (b) layout without BST (c) layout with flip-chip BST (size: 2.6 mm x 2.6 mm). **not to scale in z-direction.*

4.3.2 Simulated and Measurement Results

To verify the design, the tunable IPD BSF using BST varactors is simulated and measured. The 3-D structure of the filter, and layout pictures of the BSF with and without the flip-chip BST varactors are shown in Figure 4.6 (a)-(c). The model of the BST varactor is TCP-3012H, with Q of 70-90, and the capacitance ranges from 0.4-1.5 pF at 1.5 GHz. The chip size is 2.6 mm x 2.6 mm. The use of a flip-chip package can greatly reduce the circuit size as there is no complicated bias network involved, and the induced parasitic can be significantly reduced as well. Figure 4.7 compares the EM-simulated (dotted line) and measured results (solid line), of a continuously tunable bandstop over a frequency range from 1.4 GHz to 2.4 GHz. The two BSTs in the tunable BSF filters are biased synchronously in this case, with a voltage of 2-20 V (0.4 pF - 1.3 pF). As can be seen, both the simulated and measured results agree very well.

Figure 4.8 shows the measured return loss and insertion loss of the BSF in the whole

continuous tunable range from 1.3 GHz to 2.3 GHz. It can be seen that the out-of-band insertion loss is maintained very low from 0.1 GHz to 4 GHz (i.e., less than 1-dB in 3-4 GHz), indicating that a reasonably good rejection level is achieved. A small passband offset is observed at both end of the bias voltage, since the designed center frequency is around 1.8 GHz. To improve the performance of the tunable BSF filter, asynchronous tuning is used where different DC bias voltages are applied to the BST varactors. The measured insertion losses of the tunable BSF with synchronous and asynchronous DC bias are plotted in Figure 4.9 (a) and (b). As can be seen, the rejection level is optimized with the use of asynchronous tuning. The tuning bandwidth below the 40-dB rejection level is improved from 190 MHz (1.76-1.95 GHz) to 300 MHz (1.6 GHz-1.9 GHz). In addition, Figure 4.10 shows that the 20-dB fractional bandwidth changes only slightly (8-12 %) over the entire voltage swing.

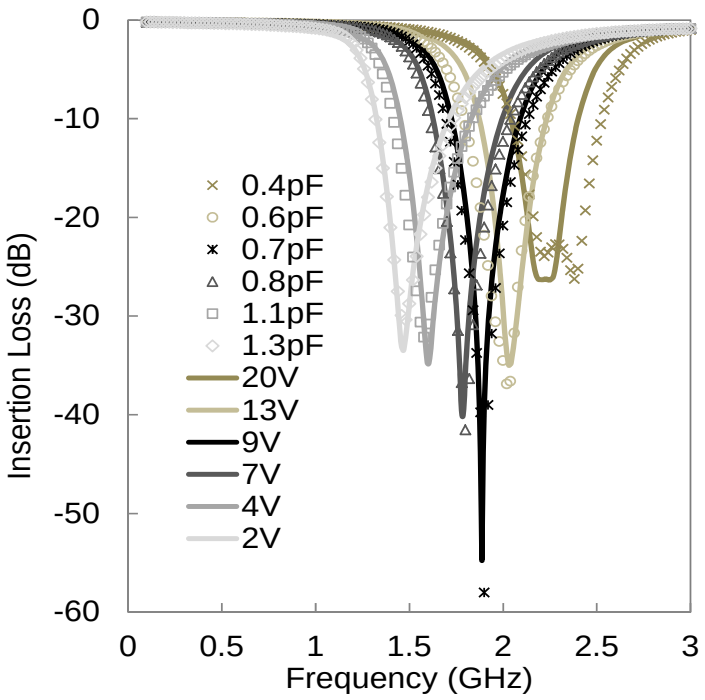


Figure 4.7 The EM-simulated (dots) and measured (solid lines) results.

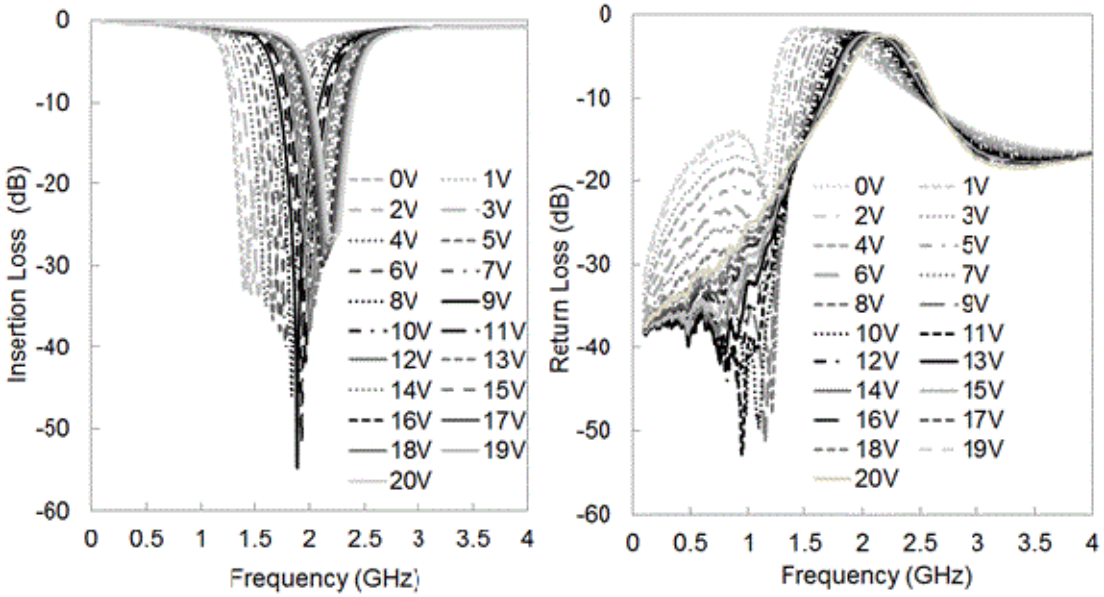
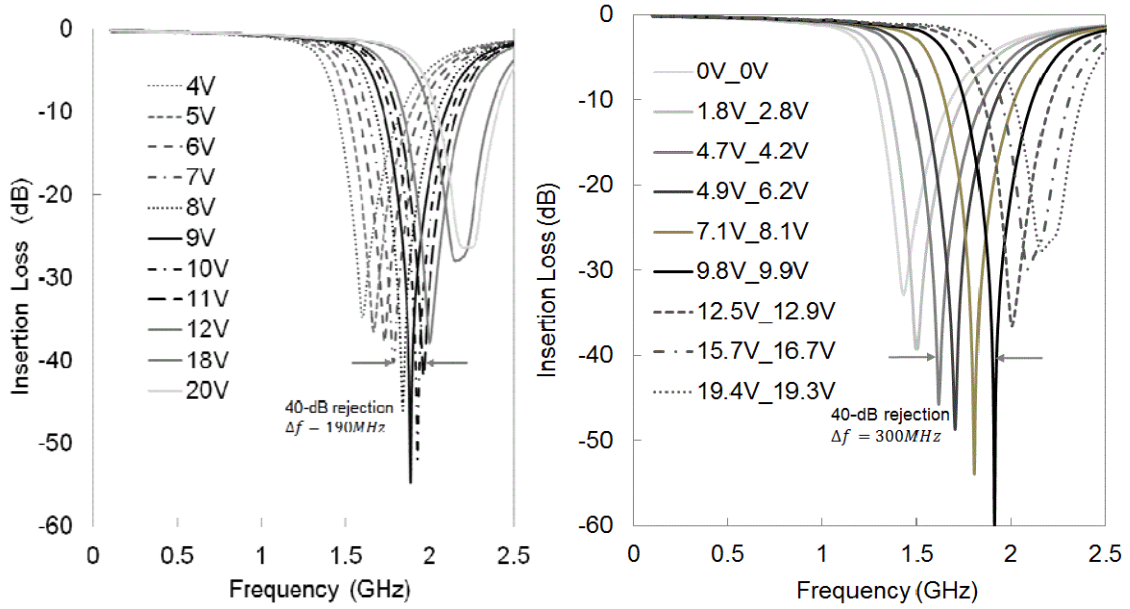


Figure 4.8 Measured insertion loss and return loss of the continuously tunable IPD bandstop filter with synchronous DC bias.



(a) (b)

Figure 4.9 Measured tuning bandwidth with 40-dB rejection of the continuously tunable IPD bandstop filter with (a) synchronous DC bias and (b) asynchronous DC bias.

4.3.3 Linearity of the Tunable Bandstop Filter and its Performance with the IPD Wideband Balun

In order to improve the linearity of the tunable BSF, high linearity tunable BST varactors are used. The varactors are built from a stack of series capacitors (C_{TOP} and C_{BOT}) and a biasing network (R_{FEED} and R_{BIAS}), combined inside the device, as shown in Figure 4.11. This series stack configuration reduces the voltage swing across each capacitor, similar to the technique reported in [66]. The number of devices used in the stack can be selected based on linearity requirements and available physical space. A 24-capacitor stacked model (S24) is used to demonstrate our tunable BSF, and other models such as S36, S40 and S48 devices are available from ON Semiconductor as well. The 3rd harmonic performance of the capacitor

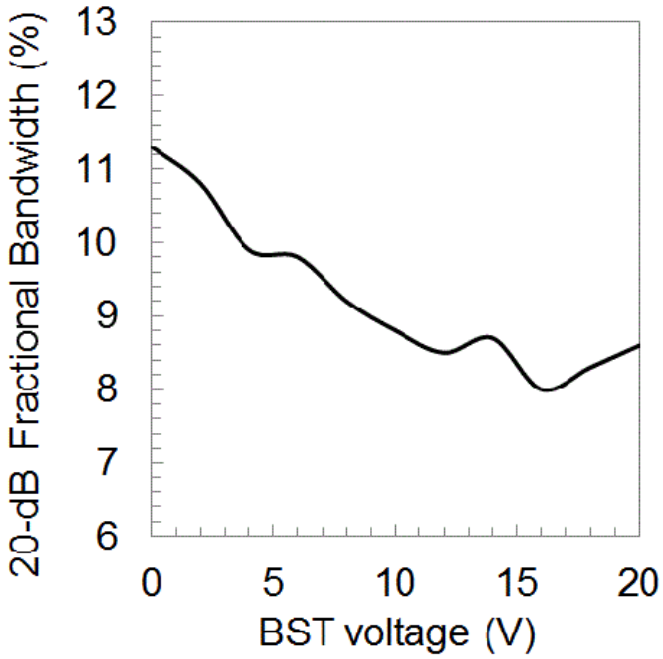


Figure 4.10 Measured 20-dB fractional bandwidth.

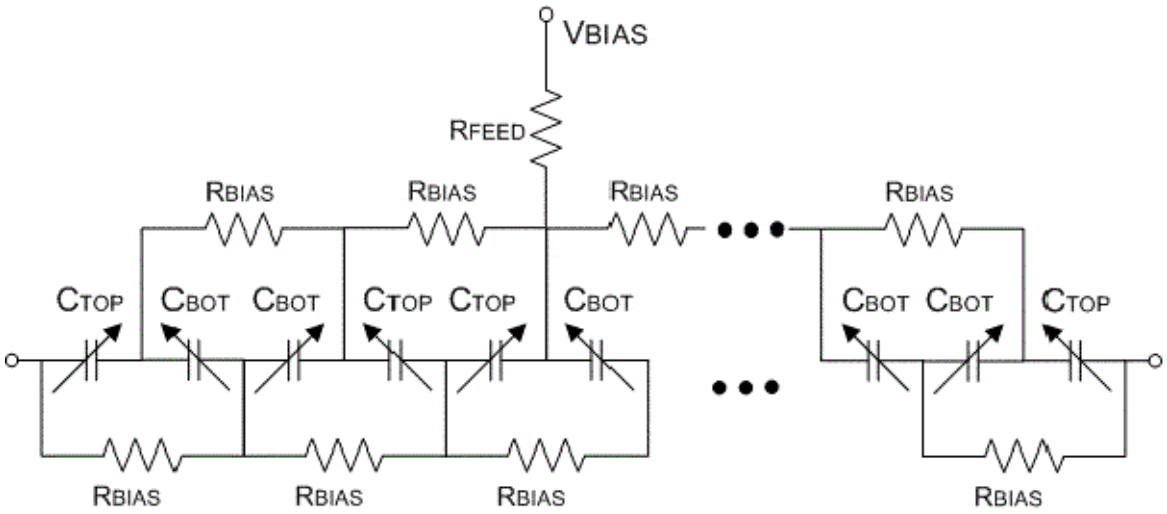
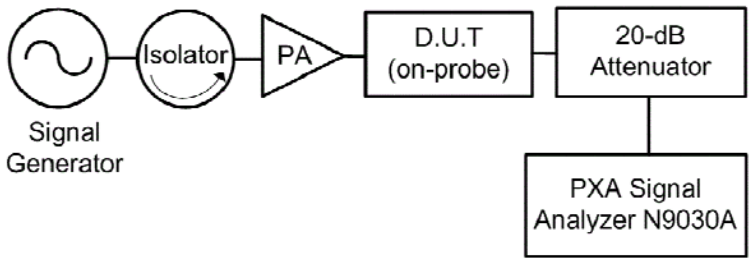


Figure 4.11 Internal structure of S24 tunable BST varactor.

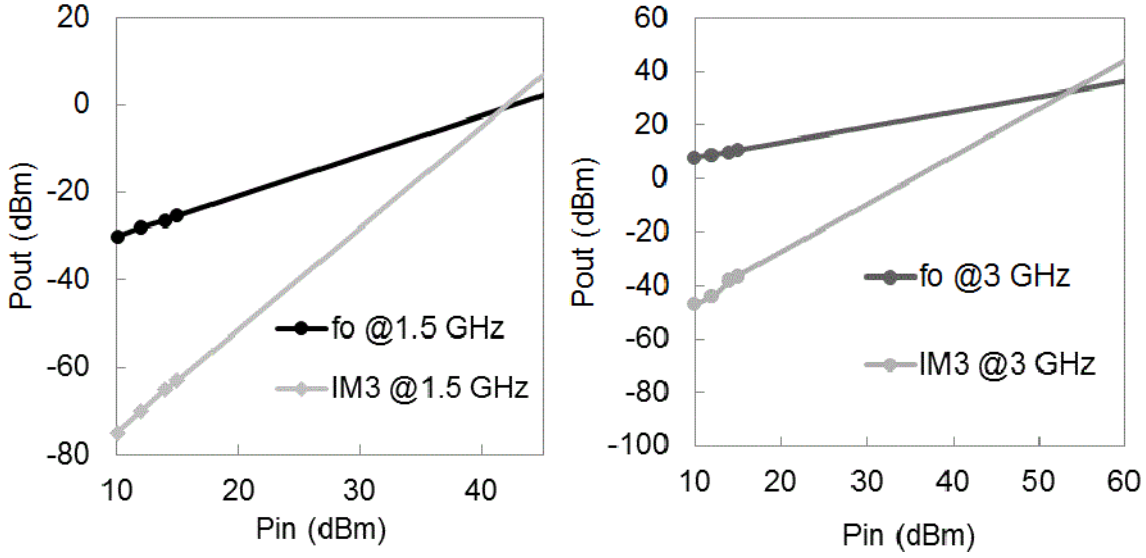
alone is improved by 12 dB going from an S24 to an S48 design. A standard on-wafer two-tone test is used to measure the linearity of the IPD tunable BST-based bandstop filter. The pictures of the measurement set-up and wafer measurement are shown in Figure 4.12 (a) and 4.12 (b), respectively.



(a)

(b)

Figure 4.12 Experiment set-up for IP_3 measurement.



(a) (b)

Figure 4.13 IP_3 test performance for the tunable BSF (a) stopband and (b) passband.

TABLE 4.3 COMPARISON OF TUNABLE BANDSTOP FILTER BELOW 4 GHZ

	Size (mm^2)	Tuning Method	Max. Rejection Level (dBm)	IIP_3 (dBm)	Tuning Range
[49]	>25×37	Varactor	20	26	43%[1]
[51]	>10×20	Varactor	> 64	N/A	52%[2]
[54]	16.2×22.7	BST	24	N/A	7%[3]
[57]	8 × 11	MEMS	80	>50	55%[4]
This work	**2.6 ×2.6**	**BST**	**60**	**>50**	**55%[5]**

1: 40-dB (0.47-0.73 GHz)

2: 20-dB (77-128 MHz)

3: 15-dB (1.2-1.4 GHz)

4: 40-dB (1.1-2.7 GHz)

5: 20-dB (1.3-2.3 GHz)

For the BSF, the maximum voltage swing occurs at the stopband frequency, and in order to verify the linearity performance within the tunable range, high-power testing was carried out at two frequencies 1.5 GHz (within the stop-band) and 3 GHz (in the pass band) with a tone spacing of 10 MHz. An extrapolated third-order intercept point (IIP_3) of 42 dBm (stopband), and 53 dBm (passband) are obtained, as shown in Figure 4.13. Table 4.3 shows the comparisons between our tunable BSF and others for frequency below 4 GHz.

4.4 IPD Wideband Balun

4.4.1 Design Structure and Operation

The proposed wideband balun consists of a Wilkinson power divider using high-Q lumped elements and a wideband phase inverter, as shown in Figure 4.14. One of the advantages of using the Wilkinson power divider is that it provides a good isolation between the output ports. By placing the wideband phase inverter at one of the outputs of the power divider (i.e. port-2), a 180° frequency-independent out-of-phase signal can then be obtained between ports 2 and 3. To describe the operation of the structure, the operation of the IPD Wilkinson power divider is explained in part A, while the structure of the phase inverter and its model using the theory of all-pass filter is discussed in part B.

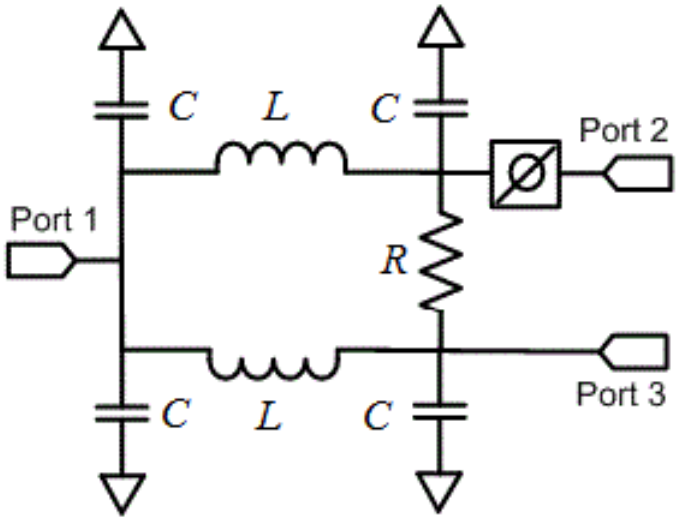


Figure 4.14 Schematic of the IPD wideband balun for RF front ends.

A) IPD Wilkinson Power Divider

As can be seen in Figure 4.14, the IPD Wilkinson power divider consists of a pi-network that uses high-Q lumped-elements to replace the quarter-wave transformers. The pi-network is basically a low-pass structure that is designed to provide low loss and a 90° phase at the center frequency (i.e. 2 GHz). This divider has all three ports matched to 50 Ω, which makes

it very convenient to combine with the wideband phase inverter. To calculate the *L* and *C*, the pi-network can be converted into ABCD matrix Equation (4.4), after which the corresponding values can be obtained as given in Equation (4.5).

$$\begin{pmatrix} A & B \\ C & D \end{pmatrix} = \begin{pmatrix} 1-\omega^2 LC & j\omega L \\ j\omega C(2-\omega^2 LC) & 1-\omega^2 LC \end{pmatrix} \tag{4.4}$$

$$C = \frac{1}{\sqrt{2}Z_o\omega}\tan\left(\frac{\theta}{2}\right), \mathrm{L} = \frac{\sqrt{2}Z_o \sin\theta}{\omega} \tag{4.5}$$

where θ is the electrical length of the quarter wavelength transmission line. Table 4.4 shows all the values of the IPD power divider.

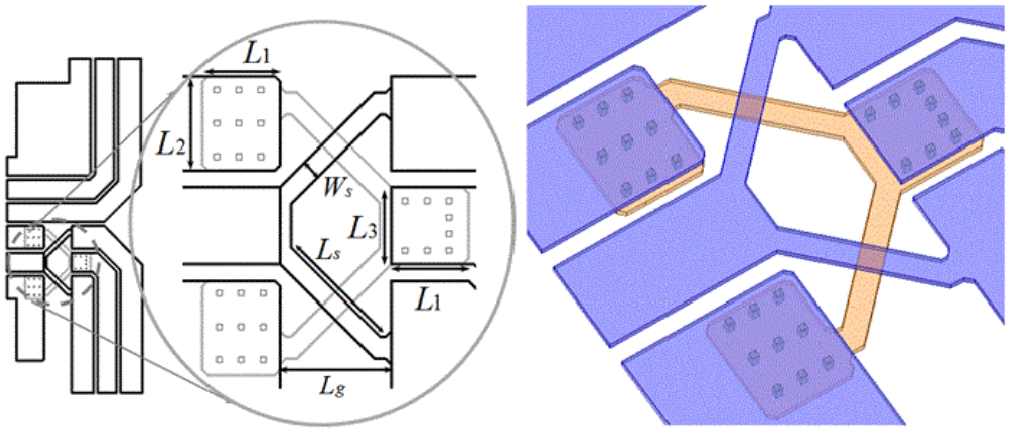
TABLE 4.4 EQUIVALENT LUMPED ELEMENT VALUE FOR IPD WILKINSON POWER DIVIDER

L	C	R
5.65 nH	1.1 pF	100 Ω

B) IPD Wideband Phase Inverter

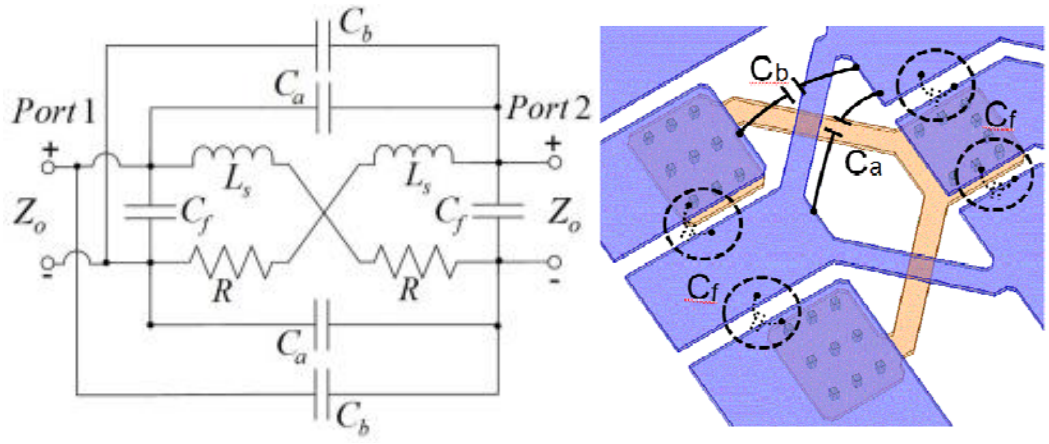
The IPD phase inverter is shown in Figure 4.15. It consists of a pair of strip lines which are connected from one end (signal/ground) to the other end (ground/signal) for both the top and bottom layer, respectively. The 3D structure is illustrated in Figure 4.15 (b). As can be seen, there are three metal patches connecting to the top metal with some vias and the strip lines are symmetrical to one another. Theoretically speaking, the phase of the RF signal can be reversed by having this structure, and thus a frequency independent 180^o phase change can be performed. A similar design was proposed in [67] using silicon technology. The equivalent circuit shown in Figure 4.16, which we devise for the inverter, has helped significantly to optimize the inverter performance, considering the limitations imposed by the

commercial thick metal IPD process on the dielectric layers thickness we can use. The insertion loss and phase balance can be critically affected in the cross-over area due to the mutual coupling. In the model shown in Figure 4.16 (a), the overlapping two strip lines can be modeled as a series connection of an inductor L_s, and a resistor R. The coupling capacitance between the signal/ground (port-1) to signal/ground (port-2) is represented by C_a. The small parasitic capacitance between the signal/ground (port-1) to ground/signal (port-2) is modeled as C_b. Also, the fringing capacitance for the coplanar waveguide transmission (CPW) line from the signal to the ground is modeled as C_f, as shown in Figure 4.16 (a) and (b). In order to illustrate the need for optimizing these parameters, Figure 4.17 (a) - (d) show the simulated return loss, insertion loss and phase response of the phase inverter for various values of L_s and C_a. According to Figure 4.17 (a)-(c), a shorter strip line gives a better return loss and phase response. Furthermore, a larger value of C_a affects the wideband phase response, as shown in Figure 4.17 (d).



(a) (b)

Figure 4.15 Structure of the IPD phase inverter terminated by 50-ohm CPW line. (a) Dimensions of the phase inverter from top view in Table 4.5. (b) 3-D view including the via locations (not to scale in z-direction).

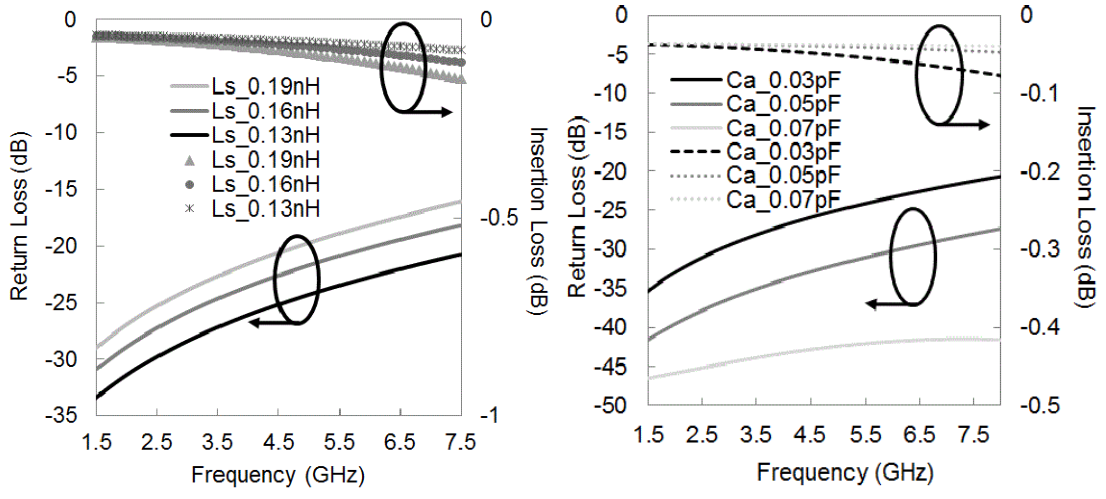


(a) (b)

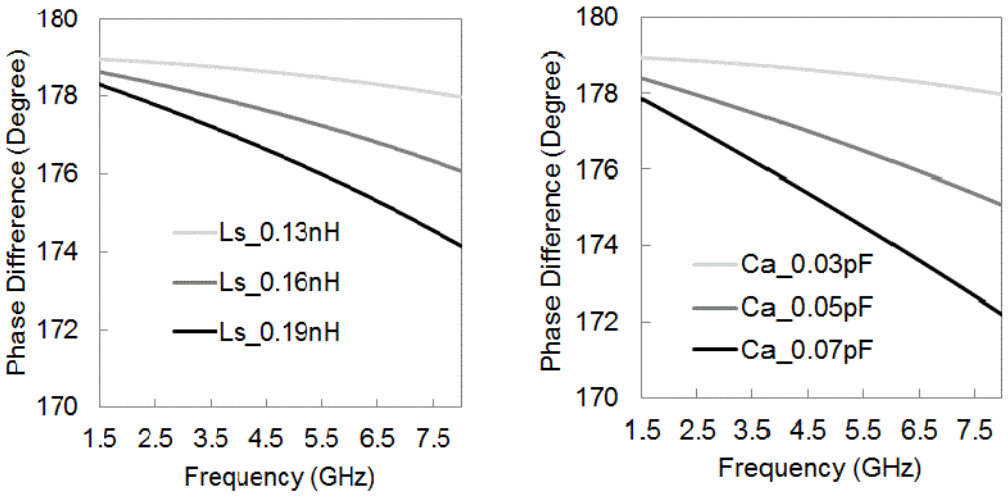
Figure 4.16 (a) Equivalent circuit model of the IPD phase inverter. (b)Parasitics in 3D diagram (not to scale in z-direction).

TABLE 4.5 PHYSICAL DIMENSIONS FOR PHASE INVERTER

L_1	L_2	L_3	W_s	L_g	L_s
70 µm	85 µm	40 µm	18 µm	100 µm	115 µm



(a) (b)



(c) (d)

Figure 4.17 The effect of strip line inductance (L_s) and coupling capacitance (C_a) of the phase inverter. (a) L_s vs. insertion/return Loss. (b) C_a vs. insertion/return Loss. (c) L_s vs. phase difference. (d) C_a vs. phase difference.

TABLE 4.6 EQUIVALENT LUMPED ELEMENT VALUE FOR PHASE INVERTER

C_a	C_b	L_s	C_f	R
0.03 pF	0.2 pF	0.13 nH	0.02 pF	0.21 Ω

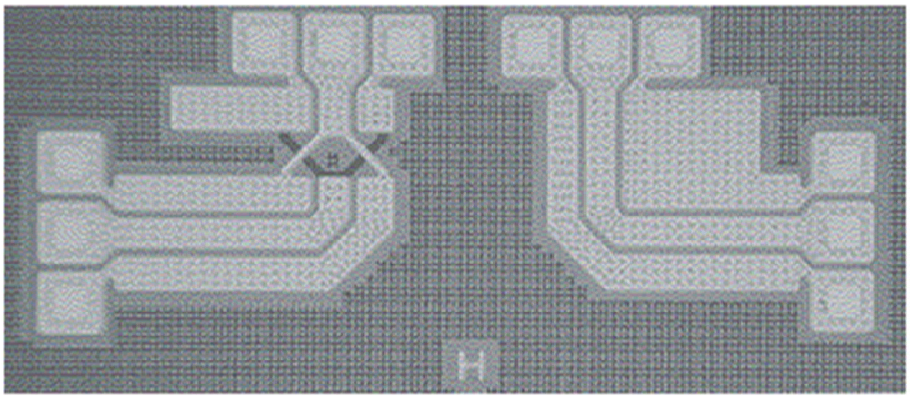


Figure 4.18 Picture of the phase inverter (left) and a section of transmission line (right).

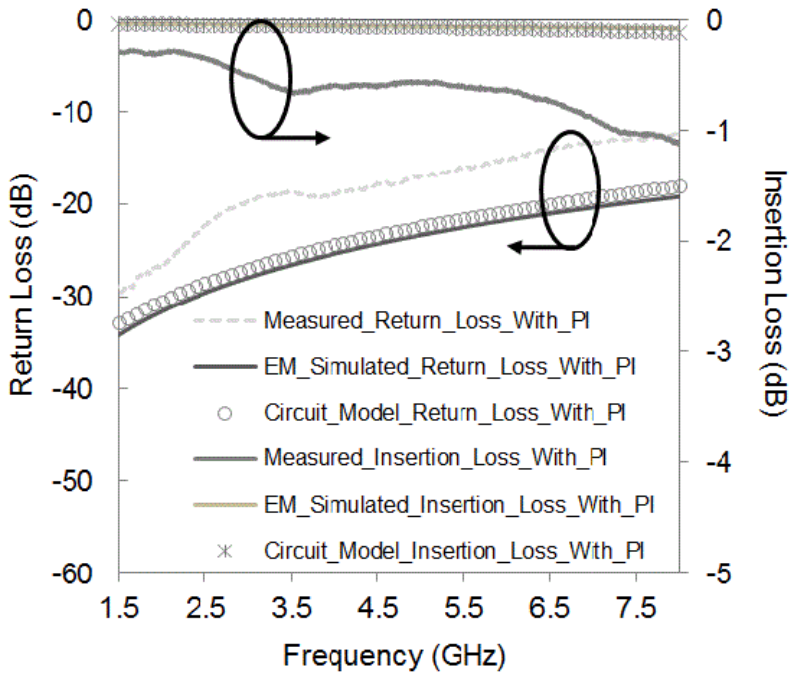


Figure 4.19 The circuit-simulated, EM-simulated and measured results of the phase inverter.

Table 4.6 shows all lumped-model values for the wideband phase inverter. In order to characterize the performance of the phase inverter by measurement, two transmission lines: one with no phase inversion and one with phase inversion are built in IPD, as shown in Figure 4.18. The measured performance of the transmission line with inversion is shown in Figure 4.19. A comparison with circuit model simulation and EM simulation is also given in the same figure. The EM-simulated and the lumped model insertion and return loss results match very well. A very wideband impedance bandwidth of the phase inverter is achieved from 1.5 GHz to 8 GHz. The discrepancy in the loss between simulation and measured results is attributed to the fact that all via holes are assumed ideal in the EM simulation, and zero surface roughness is used for the electroplated copper (Cu conductivity is assumed: 5.8×10^{7} S/m) used to fabricate these IPD devices.

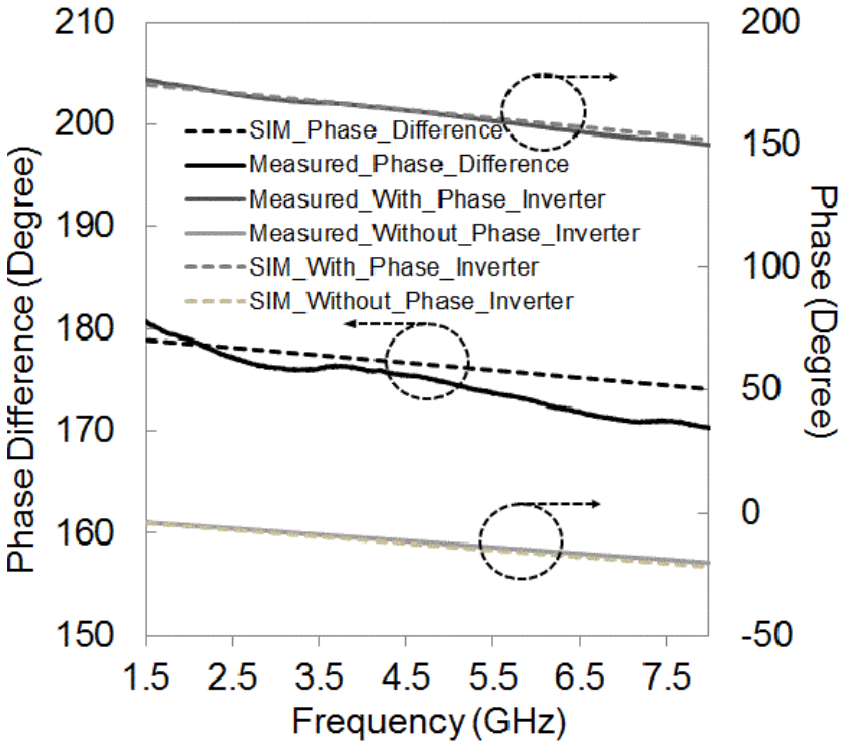
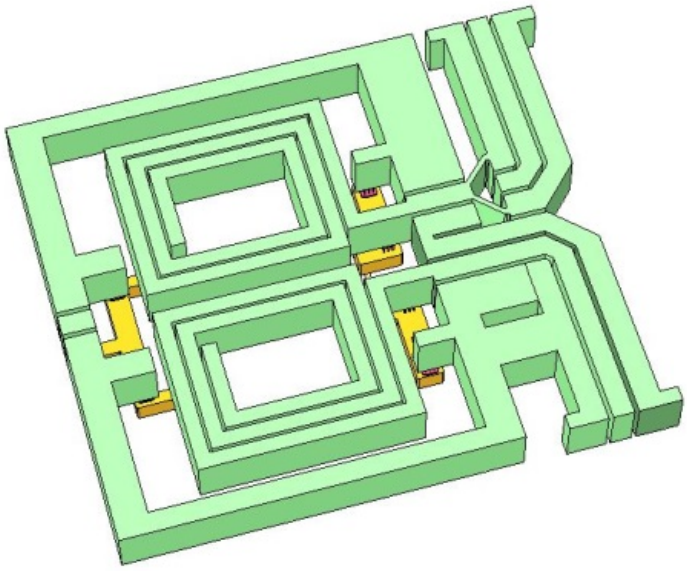
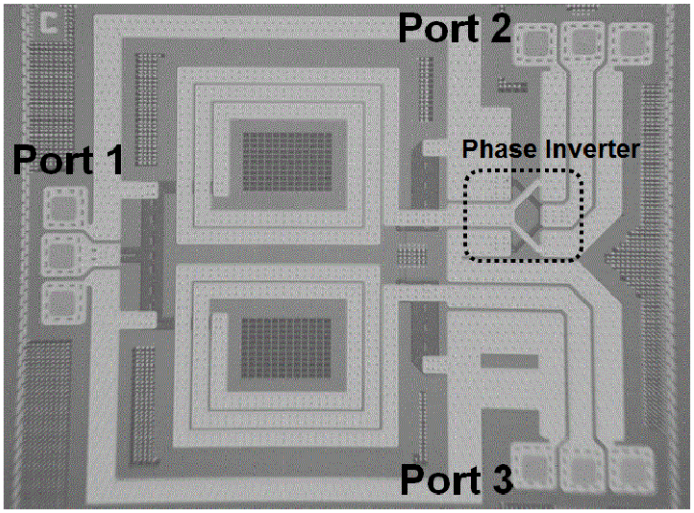


Figure 4.20 Simulated and measured phase differences with and without phase inverter.

The measured phase response is plotted in Figure 4.20, which shows that the simulation and measurement agree very well with one another. A comparison between the phase of the transmission line without the phase inverter and that with the phase inverter is also shown in this figure. It can be seen that a phase difference of 175° ± 5° can be achieved at least from 1.5 GHz to 8 GHz. Figure 4.21 shows the picture of the IPD wideband balun. The maximum measured insertion loss is 1.5 dB from 0.5 GHz to 2.63 GHz. The return loss (< -10 dB) for the balanced port (S_{22}) is from 0.5 GHz to 2.56 GHz whereas the other balanced port (S_{33}) and unbalanced port (S_{11}) is from 0.5 GHz to 2.48 GHz, as shown in Figure 4.22. Furthermore, a measured fractional bandwidth of at least 50 % (1.5-2.5 GHz) with phase imbalance (180°± 10°) and amplitude imbalance of (< ±1 dB) is achieved, as depicted in Figure 4.23, and it can be easily enhanced with the use of a multi-stage power divider.

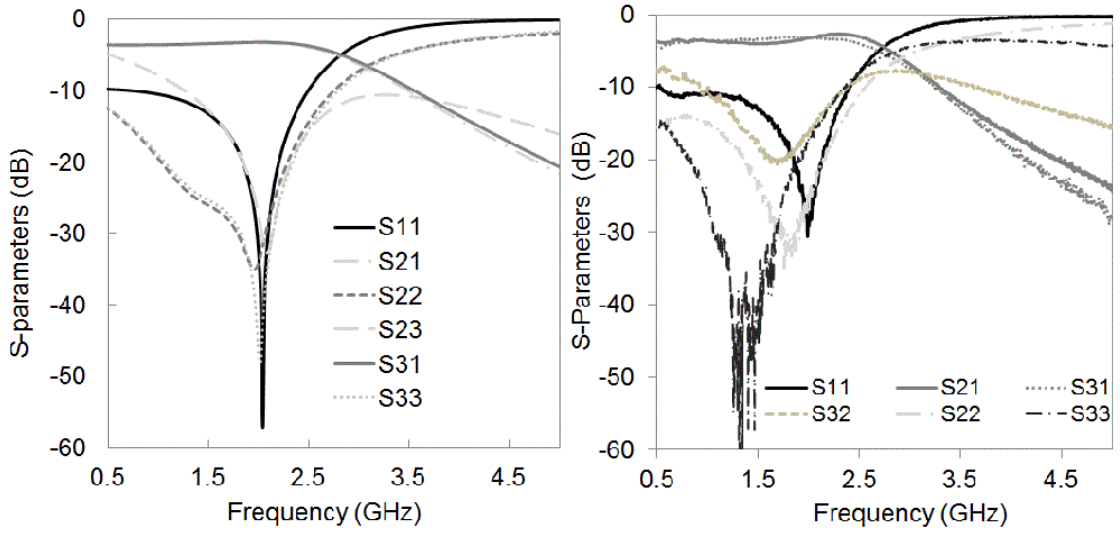


(a)



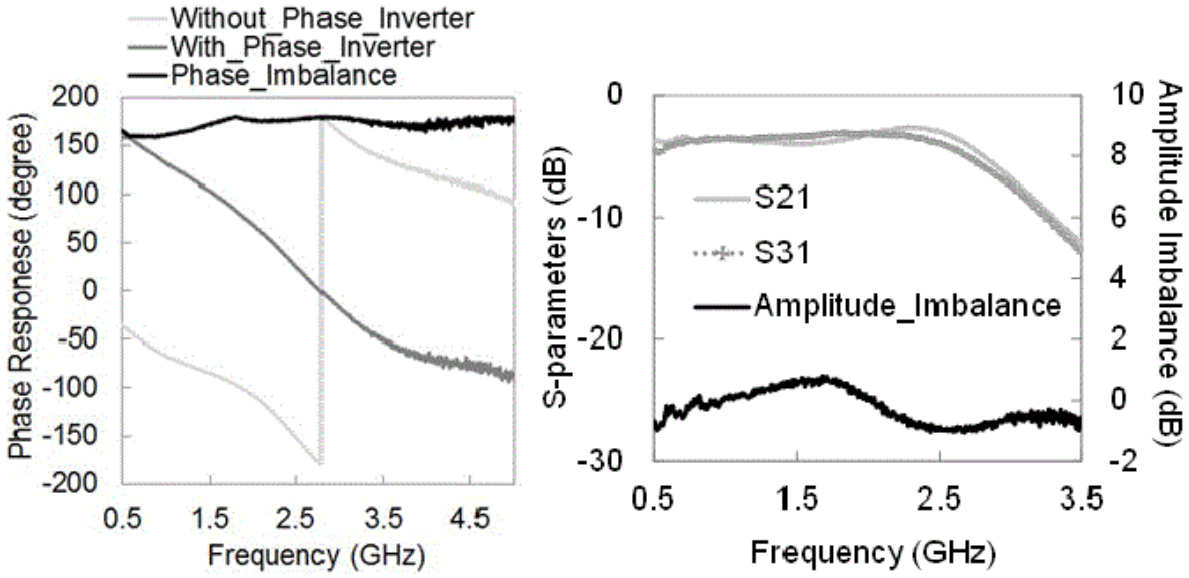
(b)

Figure 4.21 Picture of wideband balun. (a) 3D structure* (b) circuit layout (size: 2 mm x 1.9 mm).
**not to scale in z-direction.*



(a) (b)

Figure 4.22 (a) EM-Simulated and (b) measured S-parameters of the wideband IPD balun.

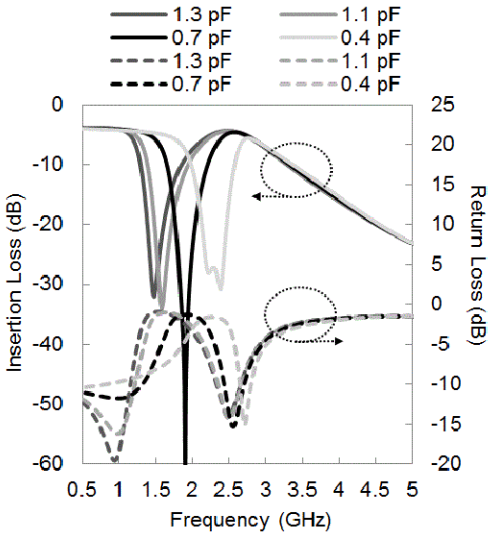


(a) (b)

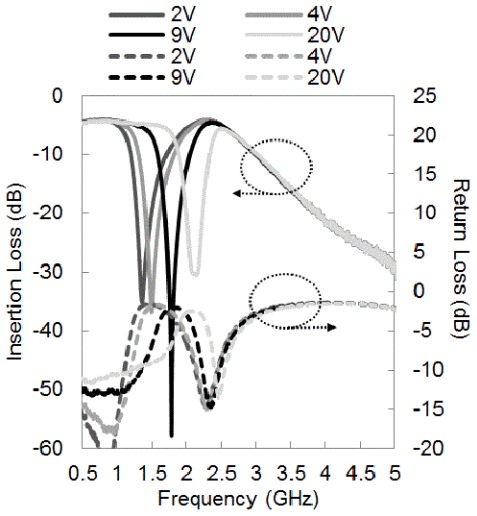
Figure 4.23 Measured (a) phase and (b) amplitude imbalance of the wideband IPD balun.

Furthermore, the simulated and measured results of the cascaded IPD tunable BSF and wideband balun are shown in Figure 4.24 (a) and (b). Four voltage states are plotted with

respect to their corresponding BST capacitances, the capacitors are continuously variable and therefore, all points in between are attainable. The measured maximum rejection (58-dB) is achieved at around 1.8 GHz, while the rejection level is still maintained at least 30-dB for the whole tuning range (1.3-2.2 GHz).



(a)

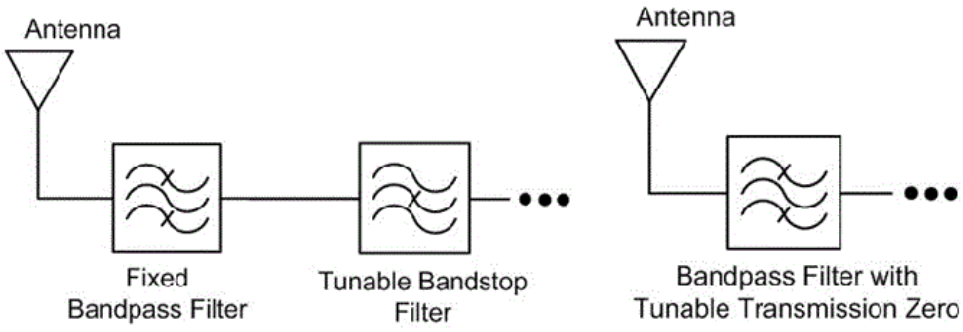


(b)

Figure 4.24 (a) Simulated and (b) measured tunable BSF cascaded with the IPD balun.

4.5 Reconfigurable IPD-based Bandpass Filters

Rather than using a standalone bandstop filter to provide the rejection, a bandpass filter with a tunable transmission zero can be potentially used in some frequency agile system applications that need to reject a particular interference signal. Figure 4.25 shows the block diagrams of two possible configurations: A) a bandpass filter cascaded with bandstop filter and B) a bandpass filter with a built-in tunable notch filter.

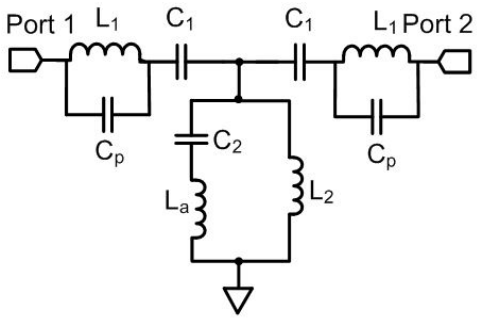


(a) (b)

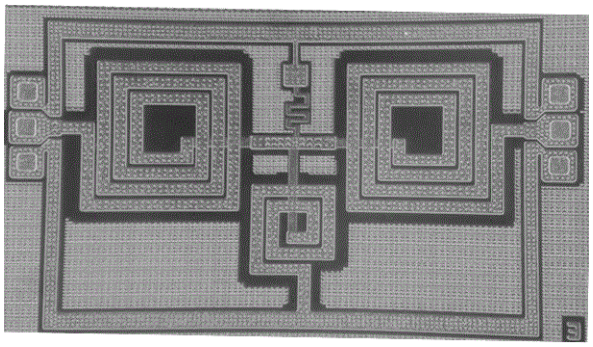
Figure 4.25 Possible configuration of a bandpass filter with tunable zero functionality. (a) A fixed bandpass filter cascaded with a tunable bandstop filter. (b) A bandpass filter with transmission zero function.

A) Bandpass Filter Cascaded with Tunable Bandstop Filter and Balun

To realize the first approach, a three-pole fixed Chebyshev IPD bandpass filter centered at 1.5 GHz is designed with two added transmission zeros. It is then cascaded with the tunable bandstop filter and balun discussed in section 4.4. One of the advantages of this approach is that a wide tuning range of the transmission zero can be achieved since it is solely based on the tunable bandstop filter. Figure 4.26 illustrates the filter schematic and a picture of the fabricated IPD chip. A ripple level of 0.01 dB of low pass prototype is used, and the values of g1, g2, g3, g4 are 0.6291, 0.9702, 0.6291 and 1.0, respectively [68]. The IPD bandpass filter is designed with extra transmission zeros to have a shaper roll-off near the in-band



(a)



(b)

Figure 4.26 Third-order modified Chebyshev IPD bandpass filter with two transmission zeros. (a) Schematic of the bandpass filter. (b) Picture of the bandpass filter (size: 2.6 mm × 1.5 mm).

TABLE 4.7 DESIGN PARAMETERS FOR IPD BANDPASS FILTER WITH TWO TRANSMISSION ZERO

L_1	L_2	C_1	C_2	L_a	C_p
7.35 nH	2.56 nH	1.24 pF	2.5 pF	1.46 nH	0.16 pF

response and to help the out-of-band rejection. To achieve this, parasitic elements-C_p (underpass capacitance) and L_a (meandered inductor), are added and optimized in the circuit as shown in Figure 4.26 (a). The value of C_p can be estimated with the equation found in [13]. Table 4.7 shows all the parameters of the IPD bandpass filter cascaded with the tunable BSF. Figure 4.27 (a)-(d) show the measured results of the cascaded configuration with, and without the balun. Two fixed transmission zeros, more than 40-dB rejection, are observed at 2.6 GHz and 4.6 GHz because of the shunt series-resonant branch (C_2 and L_a), and the series

parallel-resonant branch (L_1 and C_p). The location of the transmission zeros can be easily changed by altering the length of the meandered inductor and the width of the underpass (wider width leads to higher underpass capacitance). Also, it can be seen this approach offers a 500 MHz tuning bandwidth which varies from 1.8 to 2.3 GHz. Furthermore, an out-of-band 30-dB rejection is observed from at least 2 to 5 GHz for both cases. The insertion loss at 1.5 GHz is around 3.5 dB (without balun) and 6.8 dB (with balun), respectively. In addition, the fractional 10-dB impedance bandwidth is approximately 10-15%, and the bandwidth of the transmission zero tuning can confidently be extended, based on the choice of BST varactor.

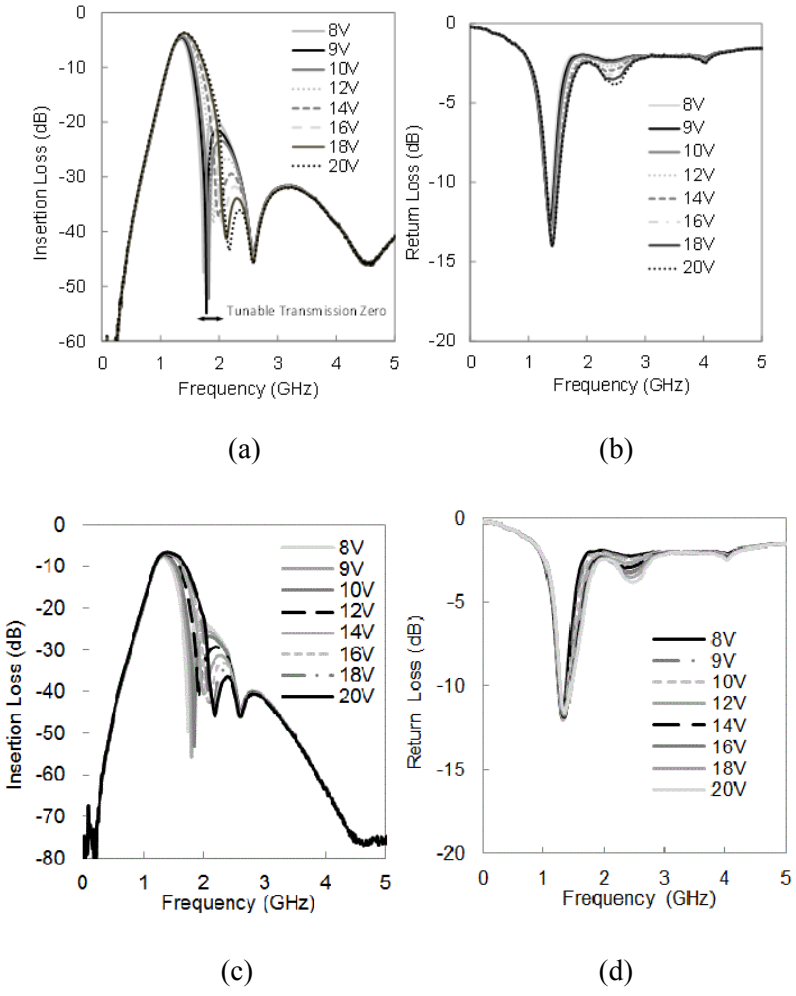
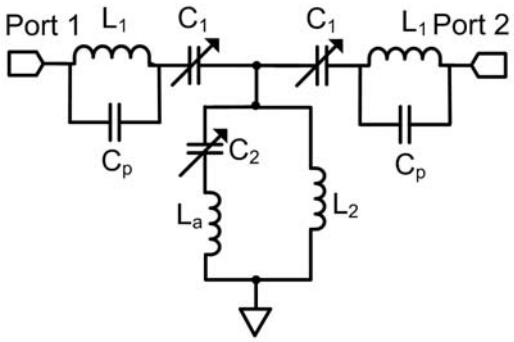
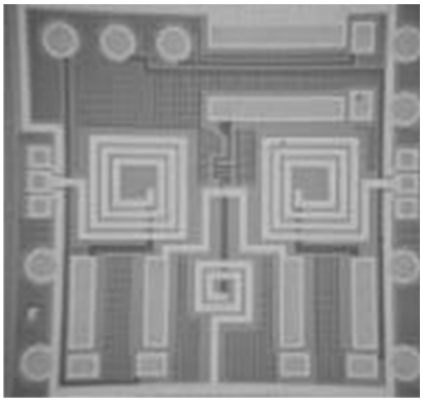


Figure 4.27 Measured insertion loss and return loss of the IPD bandpass filter cascaded with the tunable IPD bandstop filter using synchronous DC bias, without balun (a) and (b), and with balun (c) and (d).



(a)



(b)

(c)

Figure 4.28 IPD bandpass filter with built-in tunable transmission zero. (a) Schematic (b) Layout without BST and (c) layout with BST (size: 2.6 mm× 2.5 mm).

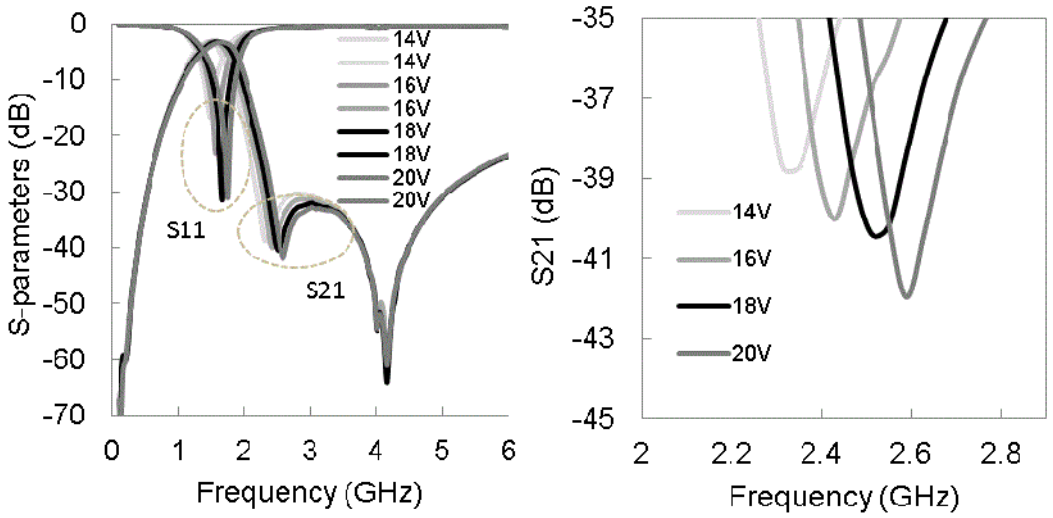
B) Bandpass Filter with Built-in Tunable Notch Cascaded with Balun

Figure 4.28 (a) shows the schematic of the IPD bandpass filter with the built-in tunable transmission zero. Three BST varactors are employed. The layouts of the circuit without, and with BST varactors are shown in Figure 4.28 (b) and (c), respectively. The DC bias pads are also included in the IPD circuit as shown in Figure 4.28 (b). The operation and design are similar to the bandpass filter discussed in part (A), however, the difference is that the tunable transmission zero is now mainly tuned by BST varactor in the shunt series parallel-resonant branch (C_2 and L_a), and therefore the circuit size is a lot smaller than the cascaded version. In

order to keep the center frequency unchanged, C_1 is held constant after it is tuned for a good return loss at the desired operating frequency. Table 4.8 shows the design parameters of the design shown in Figure 4.25 (a) and the BST varactors being used for C_1 is TCP-3027H (ON Semiconductor) [69]. At 1.5 GHz, the Q is approximately 50-80 and its capacitance range is from 1-3.5 pF. On the other hand, the model used for C_2 is TCP-3082H (ON Semiconductor) [70], with Qs of 30-50 and a capacitance range from 2.5-12.6 pF at 1.5 GHz. The operating V_{bias} is varied from 0-20 V for both models. Figure 4.29 (a)-(d) show the measured performance of the IPD bandpass filter with two transmission zeros. The filter is designed at 1.5 GHz. As can be seen, that the maximum insertion loss at the center frequency is around 3.6 dB (without balun) and 7 dB (with balun), and the transmission zero can be tuned from 2.3 GHz to 2.6 GHz (tuning bandwidth: 300 MHz) with a 39 - 44 dB rejection level when C_2 is biased from 14-20V while C_1 is kept at 12 V. The 40-dB rejection tuning range is from at least 2.43-2.64 GHz. Also, a wide stop-band rejection of 30-dB is achieved from 2.3 GHz to 5 GHz. A two-tone high power is also carried for this reconfigurable bandpass filter. Input power from 10 dBm to 20 dBm is applied to the device, and the set-up is the same as the bandstop filter. Figure 4.30 indicates that the IIP_3 is around 36 dBm and the 2^{nd} harmonic distortion is at least 60 dBc. Comparing the two approaches: A and B, a slightly higher insertion loss of 0.2 dB is observed in approach B because of the low Q value of the BST varactor models used in this approach. However, the bandpass filter in approach B has a built-in function of tunable transmission zeros, which saves a significant amount area in circuit size.

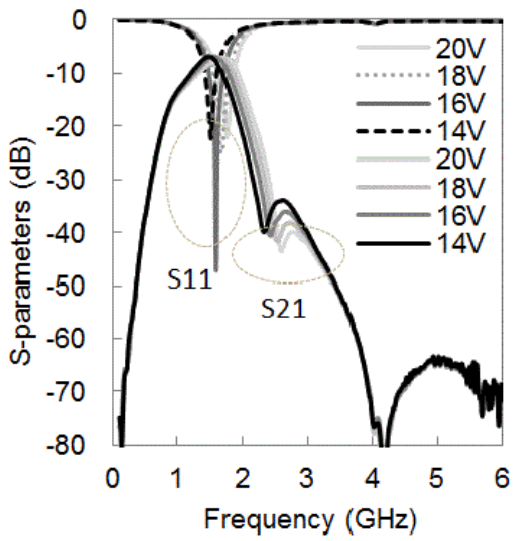
TABLE 4.8 DESIGN PARAMETERS FOR IPD BANDPASS FILTER WITH BUILT-IN TUNABLE TRANSMISSION ZERO

L_1	L_2	C_1	C_2	L_a	C_p
7.2 nH	2.05 nH	1.1 pF	2.7-3.3 pF	1.4 nH	0.22 pF

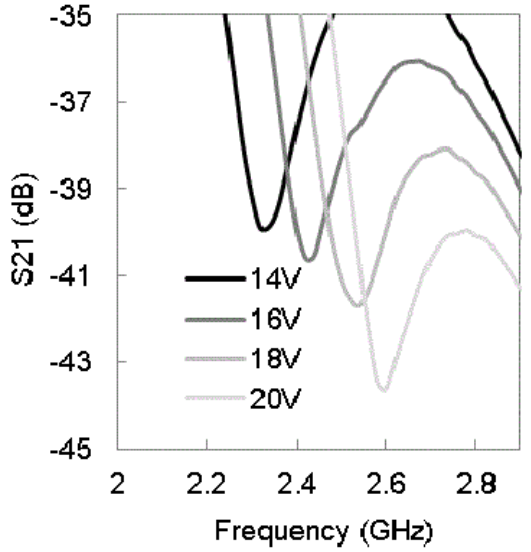


(a)

(b)

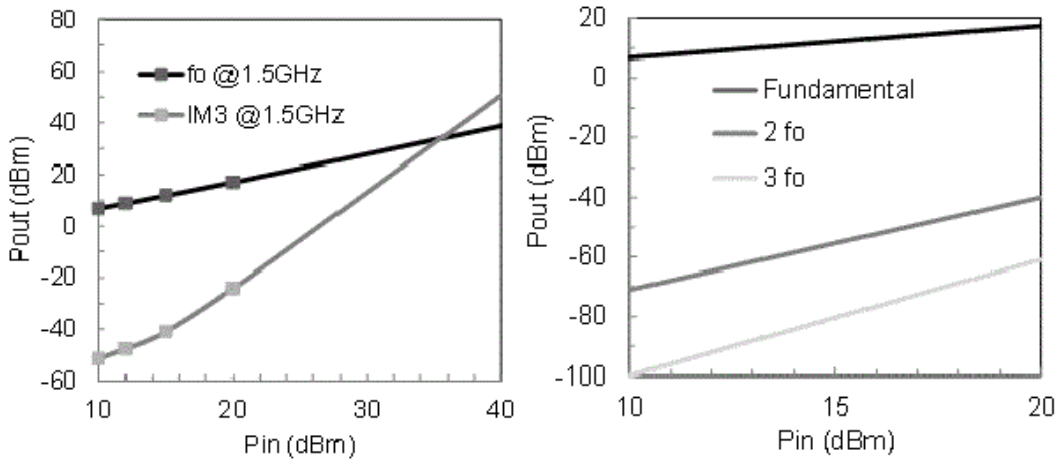


(c)



(d)

Figure 4.29 Measured response of the IPD bandpass filter with built-in tunable transmission zeros. Without balun: (a) insertion and return loss (b) rejection level at around 2.4 GHz. With balun: (c) insertion and return loss (d) rejection level at around 2.4 GHz.



(a) (b)

Figure 4.30 Measured (a) IP_3 performance: 10 MHz tone spacing and (b) harmonics performance of the IPD bandpass filter with built-in transmission zero without balun.

4.6 Summary

A high performance reconfigurable/tunable IPD bandstop filter with a wideband balun as a multi-chip module is proposed. The IPD phase inverter in the balun has been successfully modeled and demonstrated. Moreover, a compact, IPD-based fixed bandpass filter and a bandpass filter with a tunable transmission zero have been demonstrated experimentally. High power nonlinearity test results have been carried out for both the tunable bandstop filter and the bandpass filter with tunable transmission zero. The integration of IPD technology with BST technology can potentially lead to the realization of highly miniature filters with good RF performance for frequency agile applications [71].

CHAPTER 5

MONOLITHIC IPD-MEMS TECHNOLOGY AND ITS APPLICATIONS TO DELAY-LINE NETWORKS AND SWITCHED CAPACITOR BANKS

5.1 Introduction

RF MEMS switch technology has been a popular candidate for the last 15 years, mainly because it can be used as a fundamental block for some tunable RF/microwave devices such as switch matrices [72], tunable filters [73]-[75] and reconfigurable antenna [76]-[77]. There are many advantages in using RF MEMS switches, such as excellent linearity, low insertion loss, near-zero power consumption and high isolation. In addition, it can be employed for frequency applications up to 40 GHz or higher [78].

In particular, the phase shifter is a crucial element in the phased array applications, as it can change the phase of each radiating element electrically so as to steer the antenna beam in the desired direction. In order to achieve a better resolution for tracking, a wideband phased array is always desirable. However, the problem of beam squint as a function of frequency in those traditional wideband phased arrays with a phase shifter can potentially lead to faulty

steering of the target. As a result, a true-time delay (TTD) network is required for accurate beam-steering systems [79]. Different MEMS-based TTD networks with distributed transmission lines are proposed [80]-[82]. One of the drawbacks is that they require a large number of switches integrated with different distributed transmission lines. Furthermore, all these distributed transmission lines increase the size of the entire circuit especially when the operating frequency goes down below 4 GHz. In addition, most of the MEMS-based TTD networks are usually designed in the high frequency regime (>5 GHz), and therefore, the problem of the skin-depth effect is not as significant for low frequency applications. As a result, thin-film fabrication (metal thickness including membrane < 3 μm) is commonly used, and is sufficient for achieving a reasonable insertion loss.

One of the distinct advantages of adopting the IPD technology is that it uses the thick metal to reduce the skin-depth effect loss in a standard thin-film IC process. Thick metal can also be used to enhance the power handling as well as reliability in RF switches [83]-[84]. However, there is not been much research in the literature discussing the monolithic integration of RF MEMS and IPD technology, which is highly desirable since all the advantages of those two technologies can be combined in a single platform. In [85], a thick metal surface micromaching process is proposed to build a varactor, and different sacrificial layers are used to provide different layer of metals to improve the varactors as well as the inductors, which highly increases the complexity and cost of the whole process.

In this chapter, a new and simple monolithic integration process of IPD-MEMS, developed at the University of Waterloo, is proposed. In using this process, two applications are demonstrated with its low-loss and tunable performance: (ii) a 3-bit MEMS TTD network and (ii) a switched capacitor bank. For the first application, a compact, 3-bit low loss IPD-MEMS digital TTD network is first presented, followed by a continuous TTD network using a BST varactor. The second application is a high-Q switched capacitor bank using DC-contact MEMS switches monolithically integrated with IPD capacitors.

5.2 Proposed Alumina-based IPD-MEMS Technology

The proposed alumina-based IPD-MEMS process is illustrated in Figure 5.1. This process, which mainly consists of two metal layers (including a thick metal layer on the top) and a dielectric layer, monolithically integrates the features of the high-Q passive elements and MEMS tunability, thus enhancing the performance of the RF devices. The fabrication steps are as follows. In (a), a 50-nm thick of sputtered TiW (bias line) is followed by 0.5-μm of Si_xN_y deposited by PECVD. In (b), a Cr/Au (30 nm/60 nm) seed layer is first deposited, after which a 1.5-μm of gold is electroplated as the first metal layer. In (c), a 0.5-μm of Si_xN_y is deposited by plasma-enhanced chemical vapor deposition (PECVD) as the dielectric layer for the capacitor and the DC isolation layer for the bottom electrode. In (d), a 3-μm sacrificial layer of polyimide (PI-2555) is spun and partially cured at 160 °C, and anchors and dimples are defined using reactive ion etching (RIE) respectively. In (e), with the help of photoresist AZ 9260, a thick gold metal (5-6 μm) is electroplated as the movable MEMS structure and the suspended bridge in the inductor. In order to have low stress plating, some conditions are optimized, such as low current density and temperature (2-3 mA/cm^2, 140 °F). Apart from that, a good agitation of the solution is applied for uniform plating [86]. It should be noted that most of the signal routing and inductors are on this thick metal layer so as to reduce the RF path loss. Finally, in (f), the sacrificial layer is removed by using the Dupont EKC 265 post-etch residue remover, and the bridges are then released using a critical point dryer (CPD) process to avoid any stiction problems. Compared with our IPD fabrication process reported in Chapter 3 [87], it not only has the tunable features from the MEMS structure, but can also increase the self-resonating frequency of the inductor due to the fact that there is no dielectric between the suspended bridge and the underpass which leads to lower underpass capacitance.

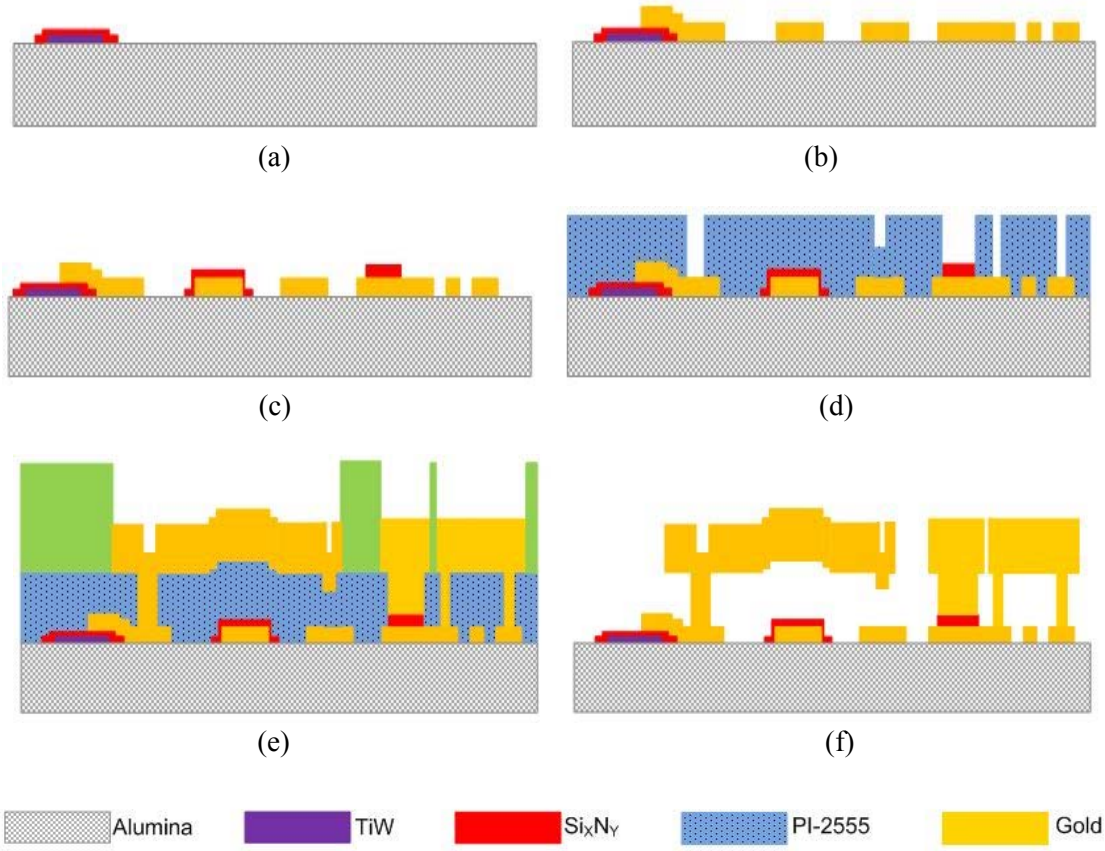


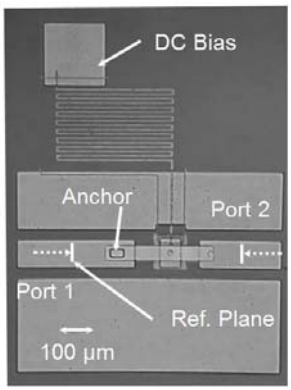
Figure 5.1 Proposed alumina-based IPD-MEMS fabrication process.

5.3 DC-contact MEMS Switch Using IPD-MEMS Technology

DC-contact MEMS switches are built in our developed IPD-MEMS fabrication process. Figure 5.2 (a) shows the side-view simulation picture of an actuated inline dc-contact cantilever MEMS switch in CoventorWare [88]. Some considerations are made to deicide the suspended bridge gap to the bottom electrode. First, it is small enough to actuate the switch within a good range of electrostatic force, which results in a good pull-in voltage. Secondly, the RF isolation level can be better, since the MEMS switch has a bigger bridge gap in the OFF-state. More importantly, a reasonable thickness of polyimide results in a

clean release process, and it has to be optimized with a good temperature and time such that the EKC solution does not attack any materials. Hence, a 3 μm of suspended bridge gap to the bottom electrode is chosen, with a dimple thickness of 0.5 μm. The width and length of the MEMS bridge are 30 μm and 280 μm, respectively. The switch is terminated by a 50-ohm coplanar waveguide (40/70/40 μm) transmission line on both input and output, as shown in Figure 5.2 (b). The upper gold metal is used for the MEMS membranes, and, anchors and

(a)

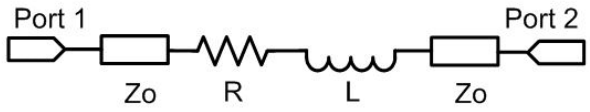


(b)

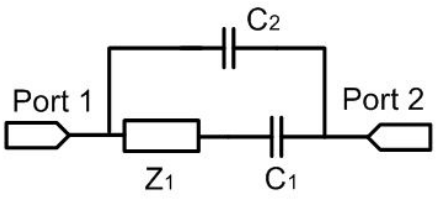
Figure 5.2 DC-contact cantilever MEMS switch (a) side view of the membrane * not to scale (b) MEMS switch terminated by a 50-ohm CPW line.

dimples (10×10 μm^2) are also defined. The simulated pull-in voltage is approximately 110 V whereas the measured voltage is around 120 V. One of the reason for the voltage discrepancy is that it is relatively difficult to maintain a good uniformity in thick electroplated gold. As a result, the electrostatic force required is slightly larger than that calculated by the simulation which assumes an evenness of metal thickness for the entire bridge. Figure 5.3 (a) and (b) are the simplified circuit models for the ON/OFF mode of the cantilever switches [89]. When it is ON, the switch can be modeled as a series configuration of resistance (R=0.6 Ω) and inductance (L = 0.077 nH) terminated by Z_o (50-ohm). On the

other hand, when it is OFF, the switch can be modeled using three elements: (i) a short transmission line (Z_1 = 72 Ω), (ii) a series capacitance (C_1 = 4.55 fF) between the switch metal and the transmission line, and (iii) a parasitic capacitance (C_2 = 3 fF) between the open ends of the transmission line through the substrate. Table I shows lumped element values for the MEMS switch in the ON- and OFF-state. Figure 5.4 shows the simulated and measured insertion/isolation loss as well as return insertion loss in the ON-state, and those simulated values are extracted from the electromagnetic simulation to fit the measurement results. It can be seen that both simulated and measured results have a good agreement over a wide frequency range. For the OFF-state, the measured insertion loss is less than 0.2 dB, while a minimum 20-dB isolation for OFF state is achieved up to 20 GHz, as shown in Figure 5.5.



(a)



(b)

Figure 5.3 Simplified circuit model when the series MEMS switch is (a) ON and (b) OFF.

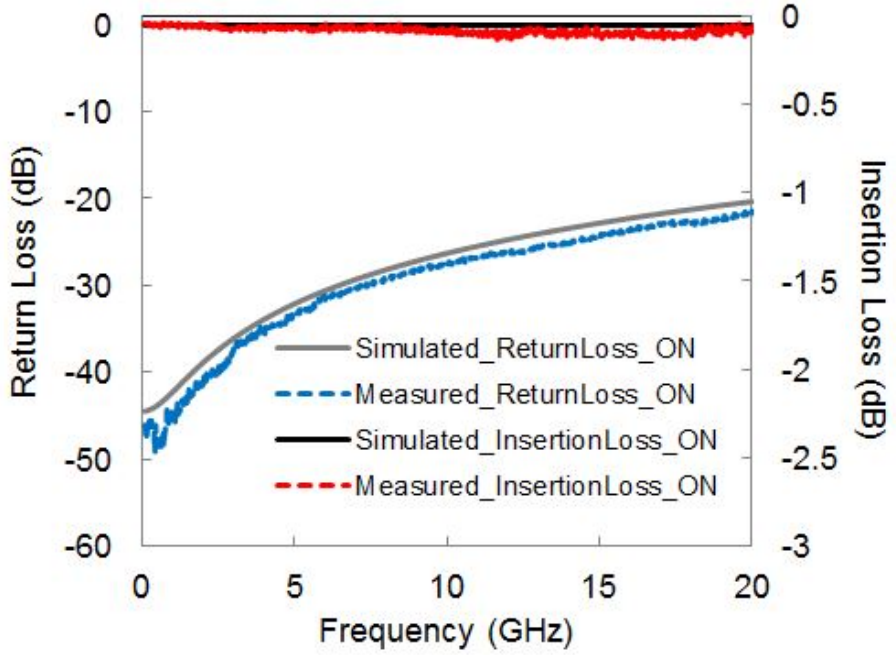


Figure 5.4 Simulated (fitted model) and measured results for MEMS switch in the ON-state.

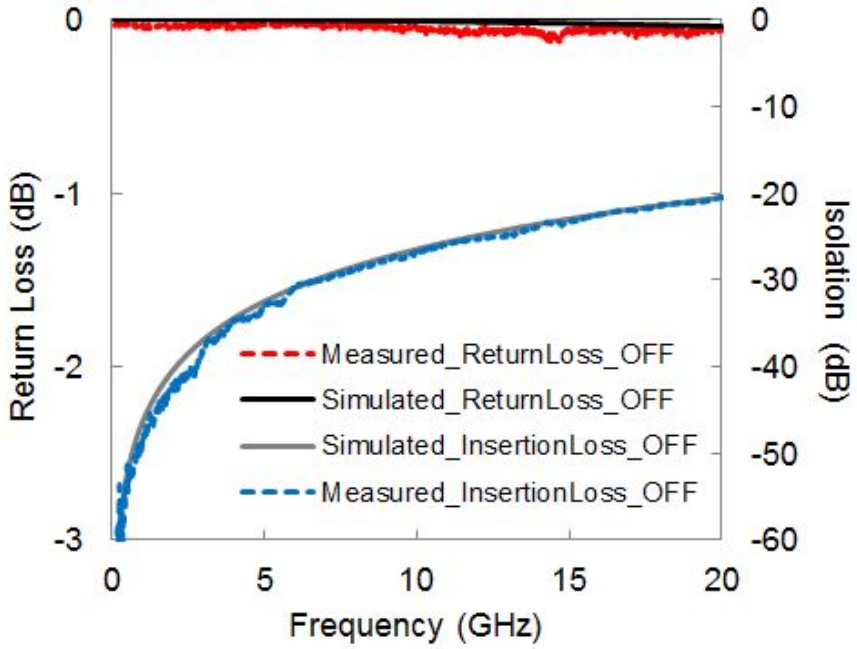


Figure 5.5 Simulated (fitted model) and measured results for MEMS switch in the OFF-state.

5.4 True-time Delay Network Design

In full duplex systems where the receiver and transmitter operate at the same frequency, interference cancellation can be potentially realized through the use of balun transformer for phase inversion, a variable delay line and a variable attenuator. It is always challenging to use this RF cancellation technique since a high-resolution of true time-delay (TTD) 10-30 ps is usually required to fully cancel the interference generated from the transmitting antenna to the receiving antenna [90]-[91].

Furthermore, in phased array, when signals are received at the receiving antenna array, there is always a small time difference. This mainly depends on the spacing of the antenna elements as well as the angle of the incidence. Having a fine control of the time delay setting can help compensate the signal delay at the receiver end so that a receiving signal coming from a certain direction can be combined coherently. As a result, the signal level can be enhanced [92].

Hence, one of the important criteria in the design of a TTD network is the achievable minimum time-delay step. This is particularly important for those systems that have been mentioned above to achieve an effective signal cancellation or signal adjustment. We present in this Chapter with two IPD-based delay line circuits with a focus on minimizing the time delay steps. The first circuit focuses on the 3-bit digital TTD by using MEMS switches, while in the second circuit, a BST is added to the MEMS-based delay circuit for further fine tuning of the delay steps.

5.4.1 Multi-bit Lumped-element Delay-line Network

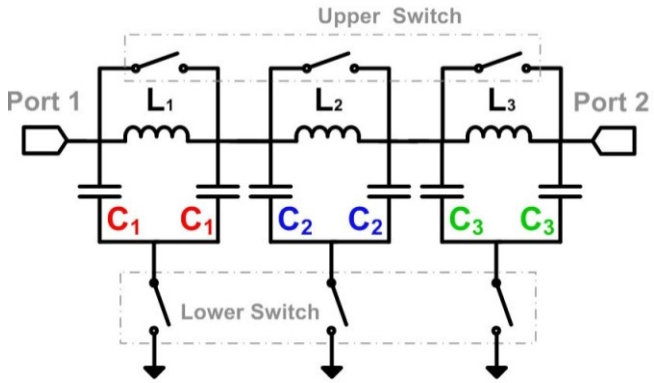


Figure 5.6 Ideal lumped element 3-bit delay-line network using ideal switches.

Figure 5.6 illustrates the configuration for the lumped element true-time delay network and Table 5.1 shows its switch combinations. The upper and lower switches complement each other for the same bit, (e.g. @ state 010, the upper switches are 010 whereas the lower switches are 101). To demonstrate this TTD network, the 1st, 2nd and 3rd phase units are designed to have 11°, 22° and 33° of phase shift when the upper switch is in the OFF-state and the lower switch is in the ON state for each unit. By using ABCD matrix for the pi-network, Equation (5.1) is obtained, which then gives the values of the elements for a specific phase (θ):

$$L_i = \frac{Z_o}{\omega_0}\sin\theta_i, C_i = \frac{1}{Z_o\omega_o}\left(\frac{1-\cos\theta_i}{\sin\theta_i}\right) \tag{5.1}$$

where L_i, C_i, and θ_i are the inductance, capacitance and electrical length for each unit respectively. Table 5.2 shows all the lumped element values for this 3-bit TTD network. The simulated phase change, group delay and S-parameters using ideal switches are shown in Figure 5.7-5.9, respectively. The data show that the phase change at 2 GHz is from 0° to 66° and its group delay is approximately from 0 to 90 ps with a minimum resolution of 15 ps. In [93], a CMOS version of the circuit shown in Fig. 5.6 was demonstrated at 30 GHz. While it is true that CMOS switches can help miniaturize the overall size circuit, the insertion loss and

DC power consumption are still the big concerns in designing a time delay network. In addition, at low frequency, the inductors and capacitors occupy a relatively large area which makes CMOS technology prohibitively expensive.

TABLE 5.1 SWITCH CONFIGURATIONS FOR LUMPED ELEMENT PHASE SHIFTER AS SHOWN IN FIGURE 5.6

State	Switch Configuration			
000	Lower Switch	0	0	0
	Upper Switch	1	1	1
001	Lower Switch	0	0	1
	Upper Switch	1	1	0
010	Lower Switch	0	1	0
	Upper Switch	1	0	1
011	Lower Switch	0	1	1
	Upper Switch	1	0	0
100	Lower Switch	1	0	0
	Upper Switch	0	1	1
101	Lower Switch	1	0	1
	Upper Switch	0	1	0
110	Lower Switch	1	1	0
	Upper Switch	0	0	1
111	Lower Switch	1	1	1
	Upper Switch	0	0	0

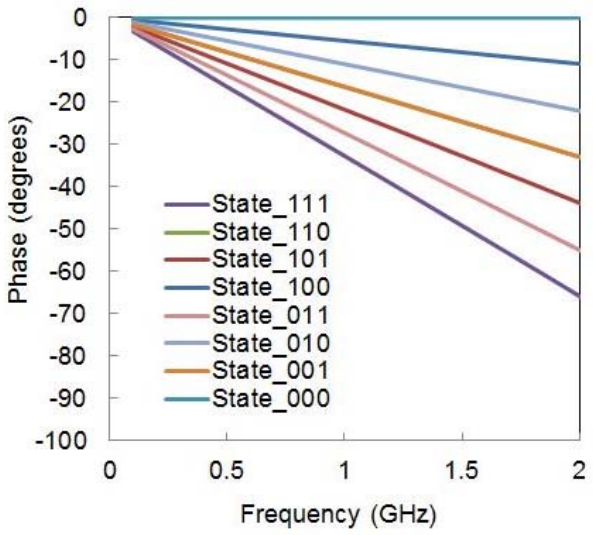


Figure 5.7 Phase change for the ideal 3-bit delay-line network shown in Figure 5.6.

TABLE 5.2 LUMPED ELEMENTS FOR 3-BIT TTD NETWORK

L_1	L_2	L_3	C_1	C_2	C_3
0.76 nH	1.49 nH	2.16 nH	0.15pF	0.31 pF	0.47 pF

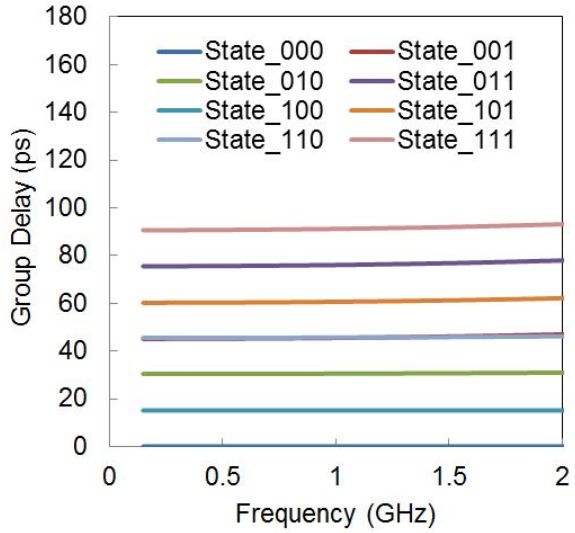


Figure 5.8 Group delay for the ideal 3-bit delay-line network shown in Figure 5.6.

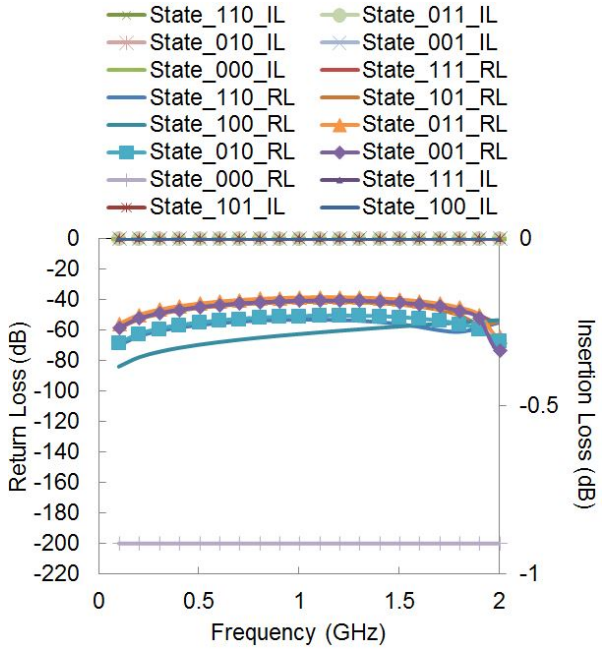


Figure 5.9 S-parameters for the ideal 3-bit delay-line network shown in Figure 5.6.

5.4.2 Three-bit Digital True Time Delay (TTD) Network Using MEMS Switches

In order to simplify the circuit by reducing the number of switches, a modified version of the circuit shown in Figure 5.6 is proposed in Figure 5.10. It consists of three of the phase units, each of which has a π-network that includes an inductor and two capacitors connecting in shunt configuration and loaded with a switch to ground. This 3-bit TTD network employs only 3 switches. It should be noted that eliminating the upper switches

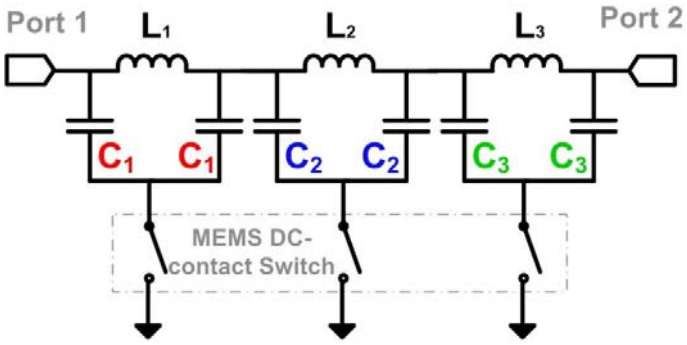
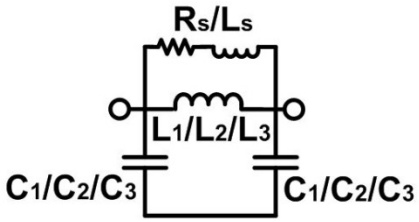


Figure 5.10 Schematic diagram of the proposed 3-bit IPD-MEMS true-time delay network.

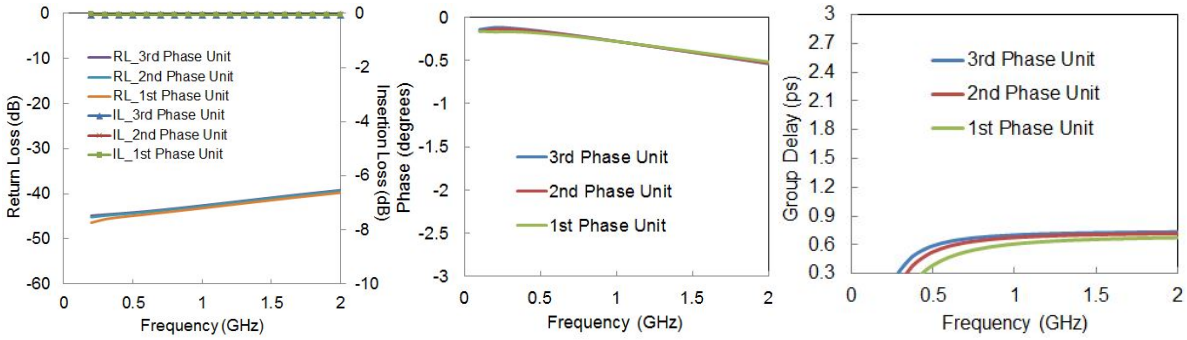
would slightly degrade on the return loss of the TTD network, since the ideal short circuit that is realized by the upper switch is now replaced by a shunt resonator (an inductor and a resistor). For instance, in state 011, the first unit in the ideal circuit shown in Figure 5.6 contributes a very low impedance (i.e., zero, if an idea switch is used). On the other hand, in the first unit shown in Figure 5.10, L_1 and $C_1/2$ contribute to a shunt resonator. To have a better explanation, simulations on one-bit configuration with (case I) the upper switch, and without (case II) the upper switch shown in Figure 5.6, are plotted as follows:

Case I

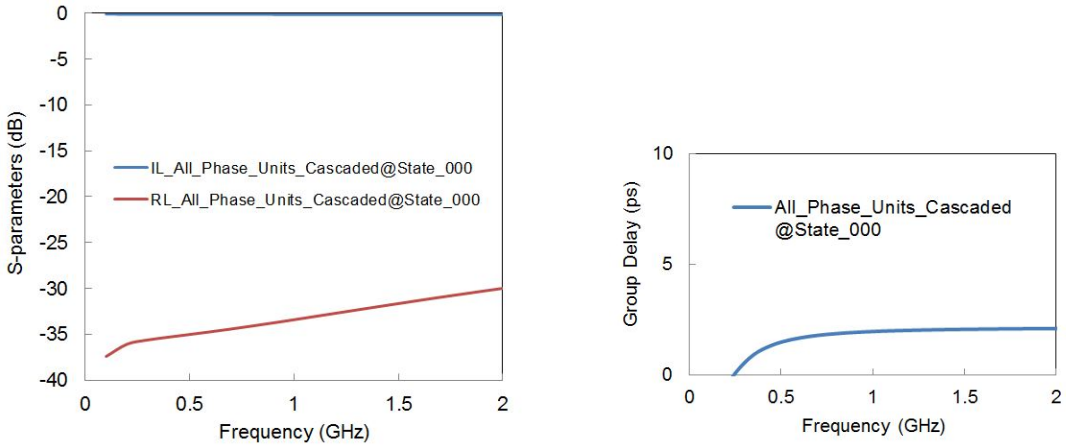
Figure 5.11 (a)-(d) show the simulated results of a one-bit configuration with the upper switch ON at state 000 for Figure 5.6 (lower switch OFF), with the corresponding lumped element values from Table 5.2. Since The series switch loaded in parallel with the resonator provides a very low impedance path, most of the RF signal passes through from one port to the other without changing the phases. Figure 5.11 (e) and (f) shows the S-parameters



(a)



(b) (c) (d)



(e) (f)

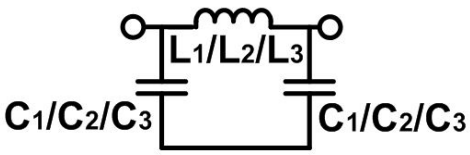
Figure 5.11 Simulated results with upper switch when lower switch is OFF. (a) Schematic of a one-bit configuration without the lower switch (b) S-parameters of the individual unit. (c) Phase shift of the individual unit. (d) Group delay of the individual unit. *Rs= 0.6 Ω, Ls=0.077 nH. (e) S-parameters of

the cascaded three phase units at state 000. (f) Group delay of the cascaded three phase units at state 000.

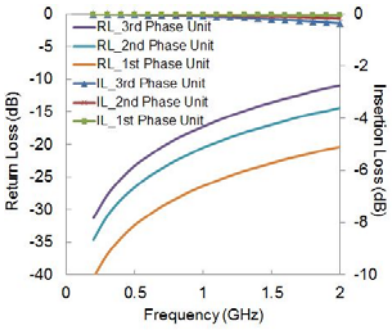
and group delay of the 3 cascaded phase units at state 000. As it can be seen that the return loss is below 30 dB up to 2 GHz while the group delay remains a very small value since the RF signal still goes to a low impedance path from the input to the output port.

Case II

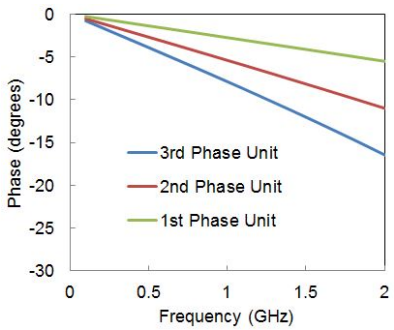
On the other hand, similarly, the simulated results in the circuit (state 000), given in Figure 5.10 for each individual phase unit without the upper switch, and lower switch is OFF, are shown in Figure 5.12 (a)-(d). Furthermore, the S-parameters and group delay of the 3 cascaded phase units are shown in Figure 5.12 (e)-(f). It can be observed that, although the return loss is not as good as in case I, there is a significant phase change on different phase units. Thus, we can make use of this fine change of group delay to design a fine resolution of TTD network when it is cascaded to more sections and switch combinations.



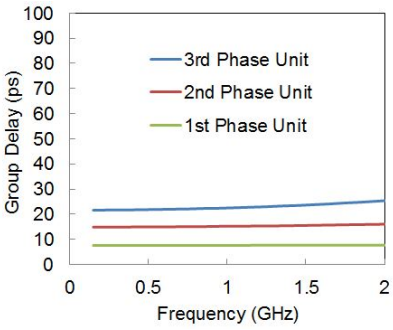
(a)



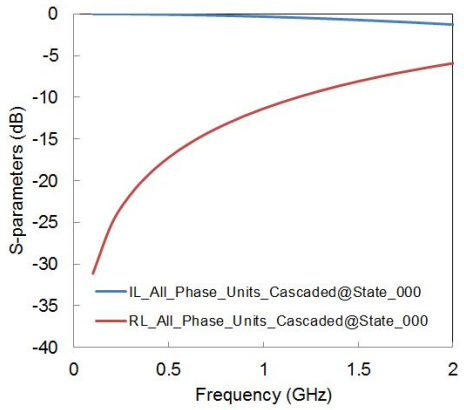
(b)



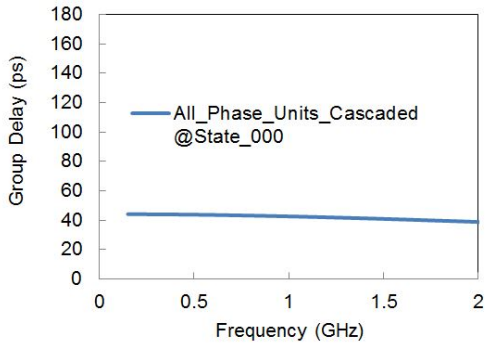
(c)



(d)



(e)

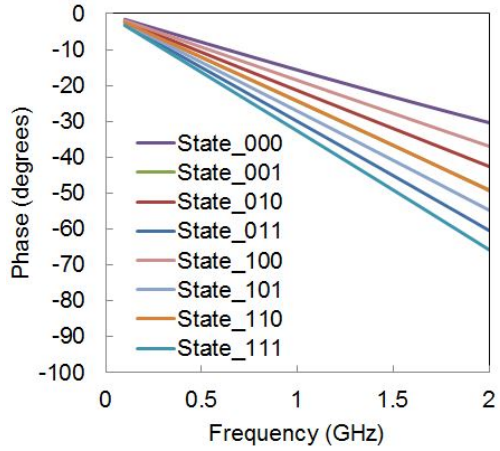


(f)

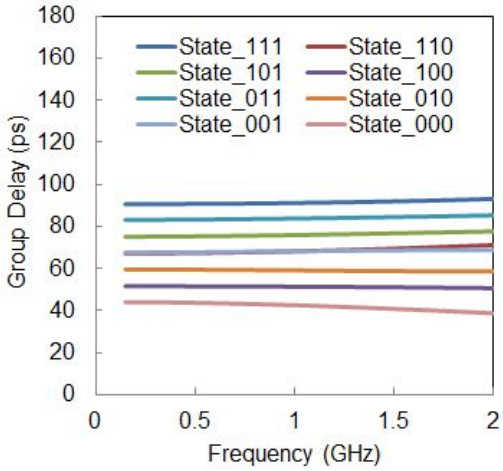
Figure 5.12 Simulated results without upper switch when lower switch is OFF. (a) S-parameters of the individual unit. (b) Phase shift of the individual unit. (c) Group delay of the individual unit. (e) S-parameters of the cascaded three phase units at state 000. (f) Group delay of the cascaded three phase units at state 000.

The circuit simulated phase shifts and S-parameters for the circuit given in Figure 5.10 with 3-bit ideal switches are shown in Figure 5.13. It can be seen that its group delay is from 38 to 93 ps with a minimum step resolution of 8 ps. Compared with the schematic shown in Figure 5.6, the group delay (Figure 5.8) ranges from 0-90 ps with steps of 15 ps. The maximum insertion loss is around 0.5 dB up to 2 GHz.

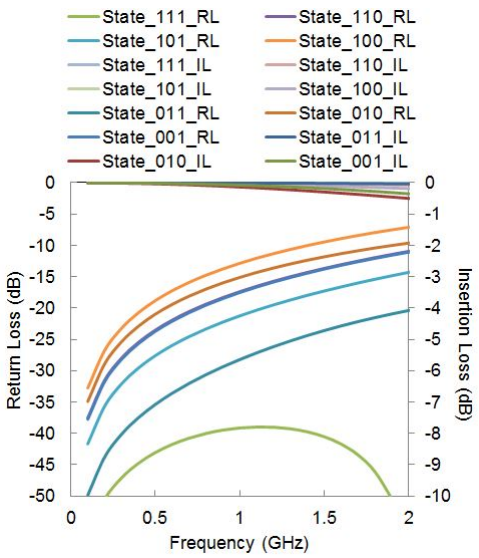
A comparison between the RF performance of the two circuits shown in Figure 5.6 and Figure 5.10 shows that, the price paid in reducing the number of switches and in realizing a finer delay step of 8 ps rather than 15 ps is the return loss degradation. However, operating the circuit up to 1 GHz can yield a return loss larger than approximately 13 dB.


0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
Phase (degrees)
State_000
State_001
State_010
State_011
State_100
State_101
State_110
State_111
0
0.5
1
1.5
2
Frequency (GHz)

(a)


180
160
140
120
100
80
60
40
20
0
Group Delay (ps)
State_111
State_110
State_101
State_100
State_011
State_010
State_001
State_000
0
0.5
1
1.5
2
Frequency (GHz)

(b)



(c)

Figure 5.13 Circuit simulations for the schematic shown in Figure 5.8. (a) Phase shift with 3-bit ideal switches. (b) Group delay with 3-bit ideal switches. (c) S-parameters with 3-bit ideal switches.

Figure 5.14 shows the fabricated picture of the proposed IPD-MEMS TTD network. A cantilever DC-contact switch is used since it can provide a low insertion loss performance as well as it performs very well in the low RF frequency regime. It should be noted that an optimization of the inductor and capacitor values is carried in order to have a better insertion loss and small form factor.

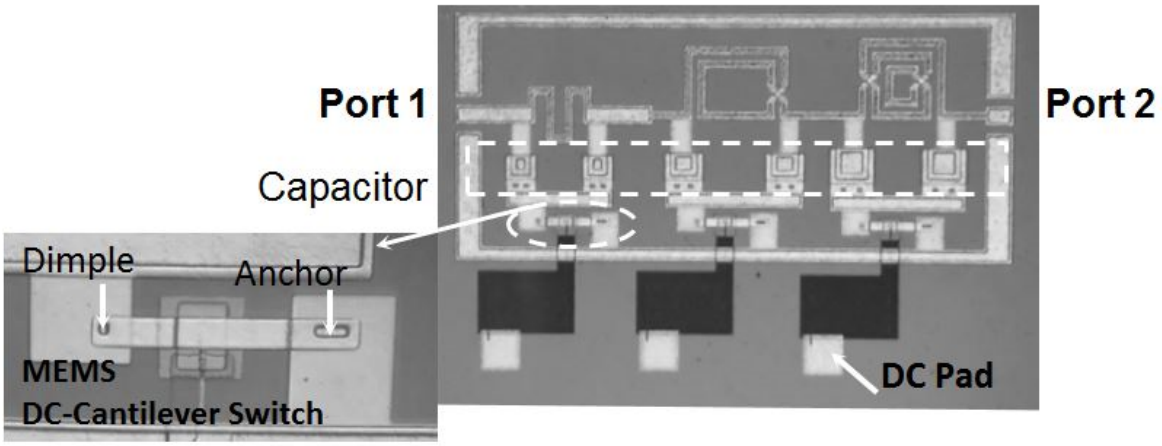
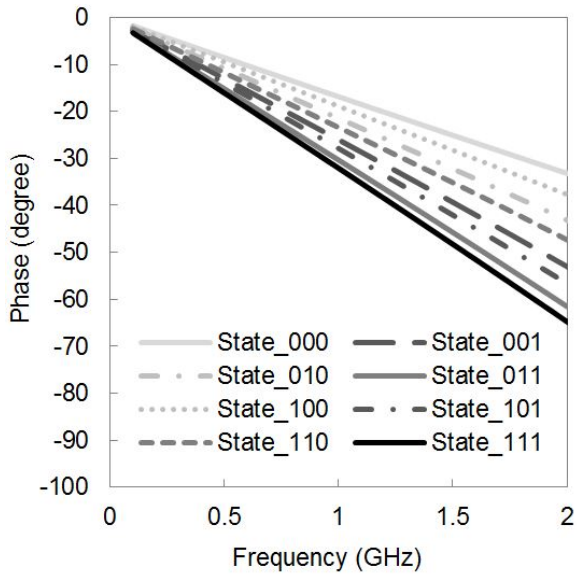
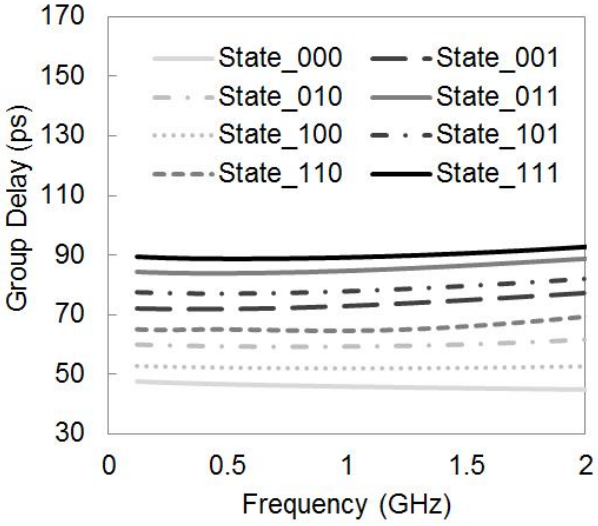


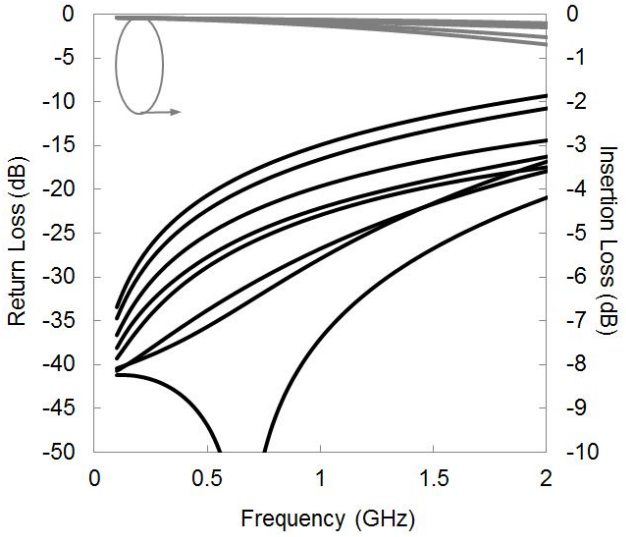
Figure 5.14 Picture of the proposed IPD-MEMS TTD network (right)* and DC cantilever contact switch (left). *chip size: 2 mm × 1.3 mm.



(a)



(b)



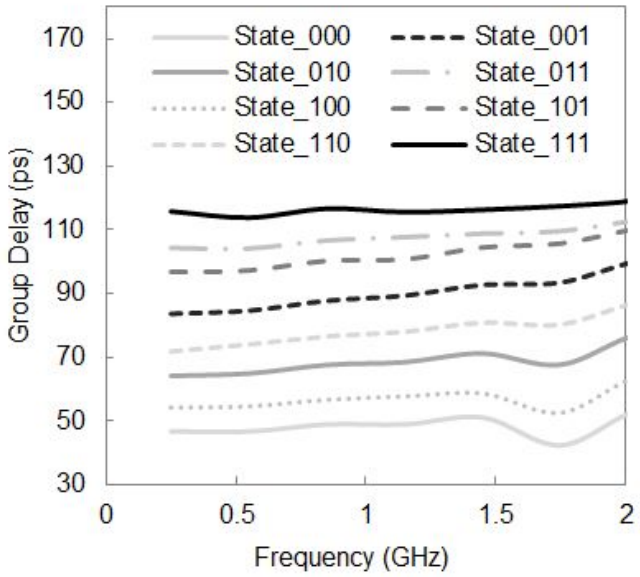
(c)

Figure 5.15 EM-simulated performance for all 8 states. (a) Phase shift. (b) Group delay. (c) Return loss and insertion loss.

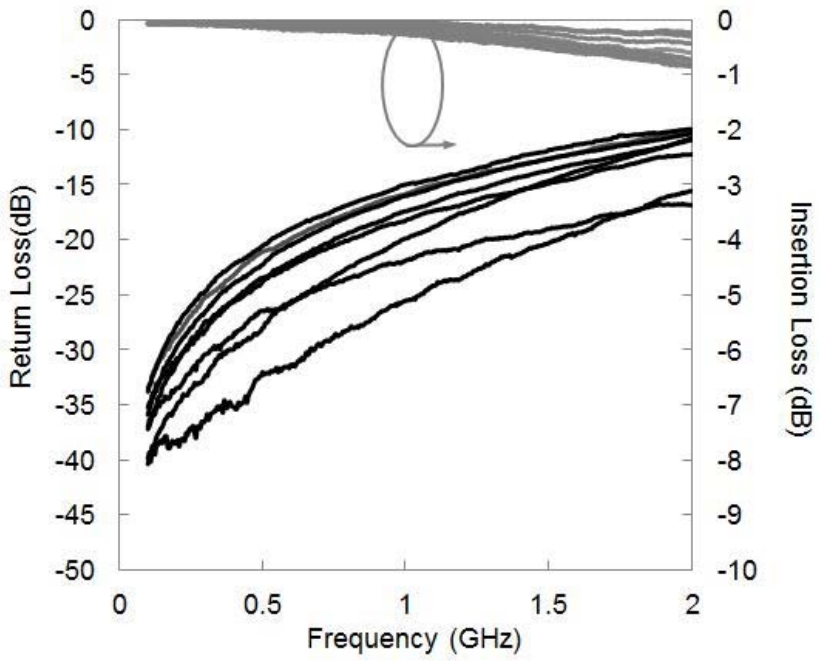
The EM-simulated phase response, group delay and S-parameters are shown in Figure 5.16. Figure 5.15 (a) illustrates a linear phase performance for all states up to 2 GHz. Besides, it can be seen that the group delay is from 44-93 ps, and the 10-dB impedance bandwidth is

approximately up to 2 GHz for all 8 states, and the maximum insertion loss is around 0.7 dB, as shown in Figure 5.15 (b) and (c).

Network analyzer (N5242A PNA-X) and 150 μm-pitch GSG probes are used to perform all the on-wafer TTD measurements. Figure 5.16 (a) shows that the measured group delay for the TTD network can be tuned between 42 ps (min) to 120 ps (max) with a delay step of approximately 10 ps. Furthermore, the measured return loss and insertion loss show that they have a good agreement with the simulated results, as shown in Figure 5.16 (b). A 15-dB return loss is nearly maintained for all the states up to 1 GHz, and its max insertion loss is approximately 0.5 dB. One of the possible reasons for the discrepancy between the simulation and measurement is that the thickness of the dielectric for the capacitor is not the same across the wafer which results in a larger group delay.



(a)



(b)

Figure 5.16 Measured performance for all 8-state pull-in voltage: 120 V. (a) Group delay of the TTD network. (b) Return loss and insertion loss.

5.4.3 Three-bit Continuous Tuning TTD Network Using MEMS and BST Technology

The proposed schematic of the TTD network with continuous tuning is shown in Figure 5.17. The structure is based on the TTD network using MEMS switches from section 5.4.2, and is then cascaded with a BST varactor in a shunt configuration. One of the key advantages of using this compact flip-chip BST varactor is that it can continuously vary the time delay on each singe state of the TTD network so that a wider/finer range of the TTD can be obtained. Furthermore, it can help fine tune the time delay, which could deviate from the designed value due to fabrication errors. Figure 5.18 shows the simulated results of the circuit shown in Figure 5.17, with consideration of the lumped-model for MEMS switches given in Figure

5.3. A maximum 0.5-dB difference in insertion loss at 2 GHz is observed compared with the standalone MEMS TTD network in section 5.4.2. This is due to the varactor capacitive loading to the whole network, as shown in Figure 5.19 (a). On the other hand, the relatively linear and continuous phase change at 2 GHz is observed from 52° to 89°, as shown in Figure 5.19 (b), where the approach in section 5.4.2 can only be used in a discrete configuration.

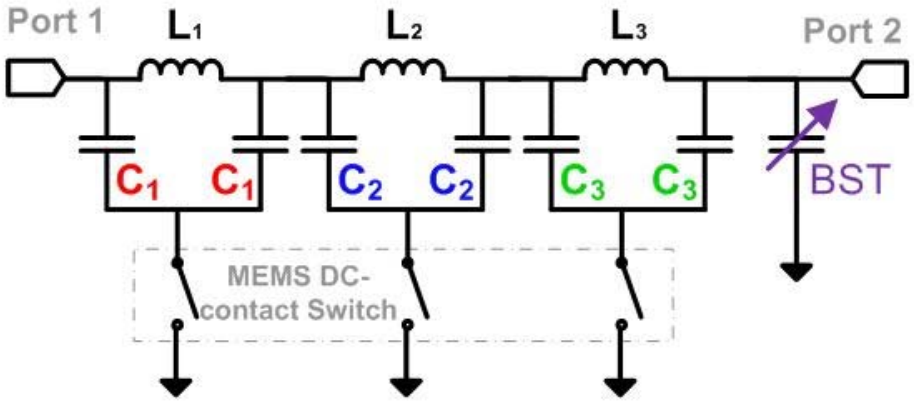
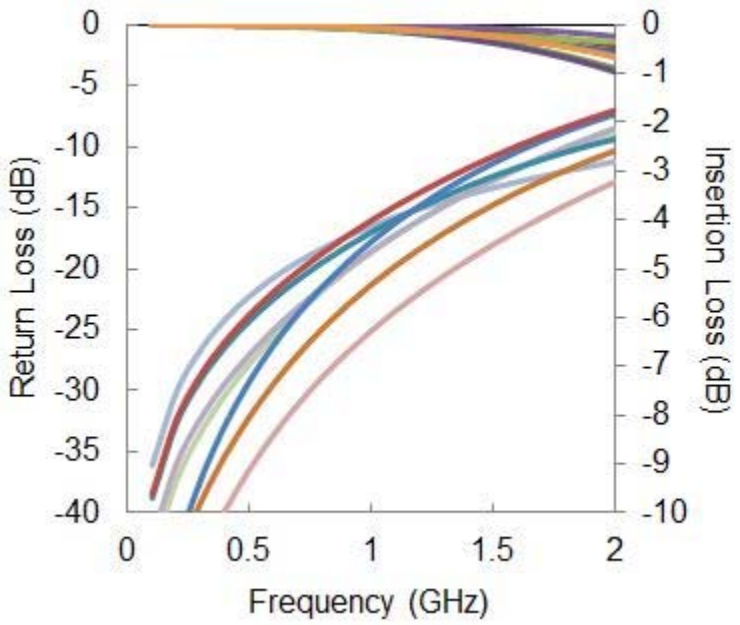
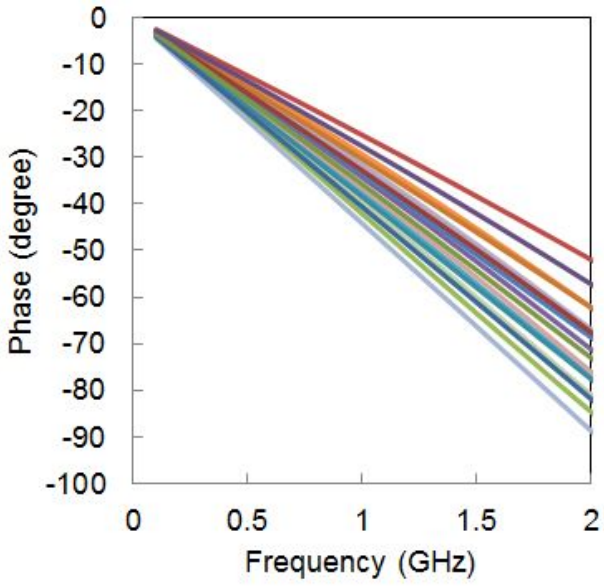


Figure 5.17 Schematic diagram of the proposed IPD-MEMS phase shifter loaded with BST for phase correction.



(a)



(b)

Figure 5.18 Simulated performance for 16 states* with the lumped model for MEMS switches (a) return loss and insertion loss. (b) Phase shift. *Only 0.5 pF (lower boundary) and 0.9 pF (upper boundary) are plotted.

Figure 5.19 and 5.20 show the layout and a photo of the IPD-MEMS/BST TTD network. In order to have a more reasonable return loss, the capacitance range is optimized between 0.5 pF- 0.9 pF for the ON Semiconductor BST varactor TCP-3012H, with an approximate Q of 70-90 at 1.5 GHz. Strictly speaking, the capacitance resolution for BST varactors can be smaller than 0.02 pF (group delay resolution: < 0.6 ps) since it mainly depends on the accuracy of the applied voltage. However, the range of the group delay at each state is of our interests, and therefore, only the measured S-parameters of the corresponding capacitance of 0.5 (lower boundary) and 0.9 pF (upper boundary) at each state are plotted, as shown in Figure 5.21 (a). The maximum insertion loss is around 1.5 dB, and the overall trend is very similar to the digital approach. Figure 5.21 (b) shows the measured group delay for all 16 states. By varying the bias of the BST varactor from 4-10 V, a maximum of continuous group

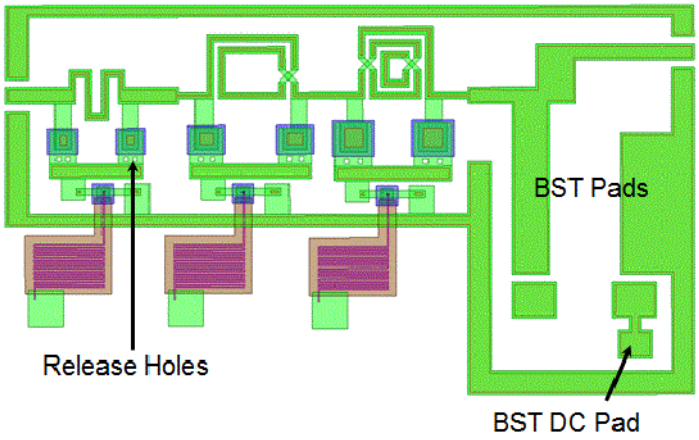


Figure 5.19 Layout of the IPD-MEMS phase shifter loaded with a BST varactor.

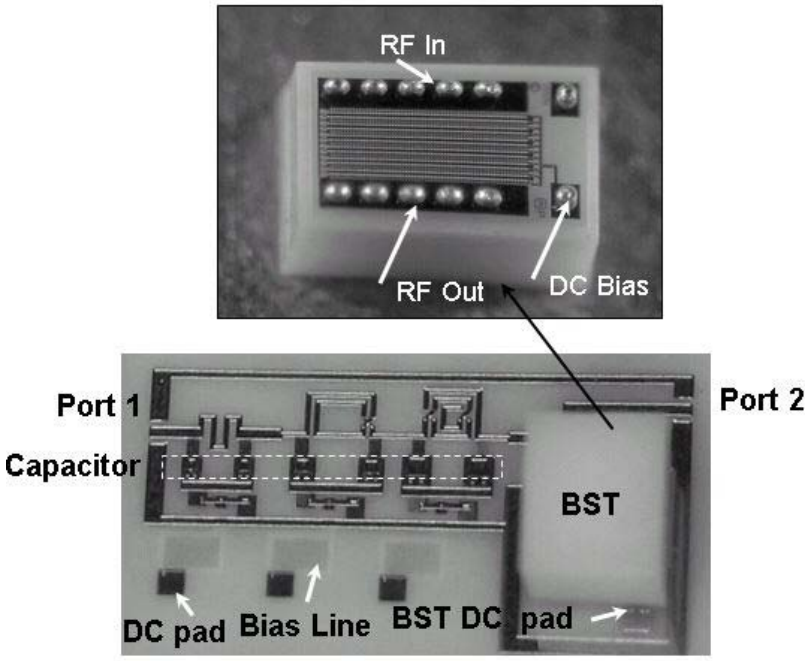
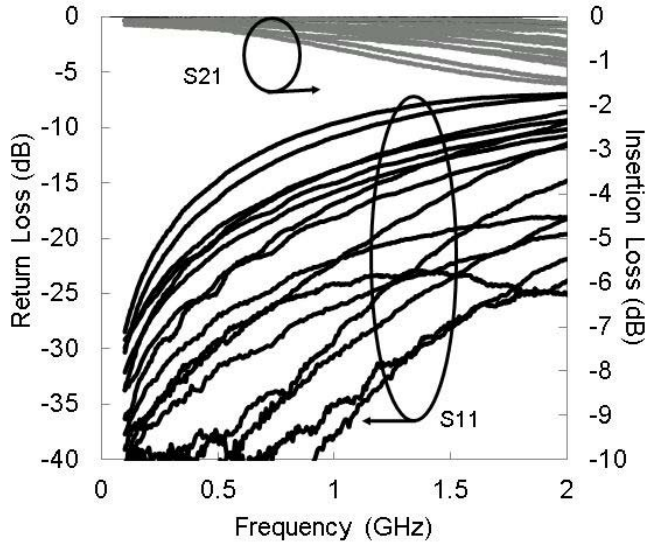
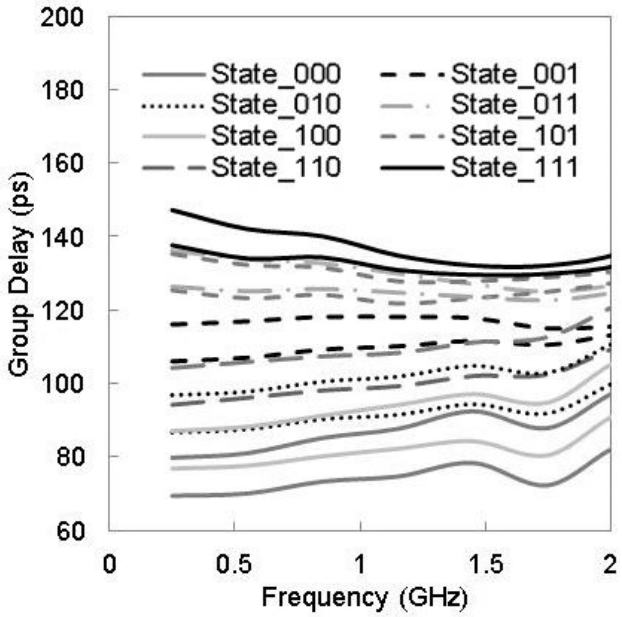


Figure 5.20 Photo of the proposed IPD-MEMS true-time-delay network loaded with a BST varactor. *chip size: 2.9 mm × 1.6 mm, with the back side picture of the BST varactor in WLCSP package.

delay can be achieved between 70-148 pF. Also, a good coverage ranging between 79-138 ps can be obtained. Furthermore, a small TTD resolution of less than 1 ps can also be obtained, which is especially useful for applications that require a fine change of TTD.



(a)



(b)

Figure 5.21 Measured performance for 16 states* (a) return loss and insertion loss. (b) True-time group delay. *Only 0.5 pF (lower boundary) and 0.9 pF (upper boundary) are plotted at each single state using the same color and pattern of the line.

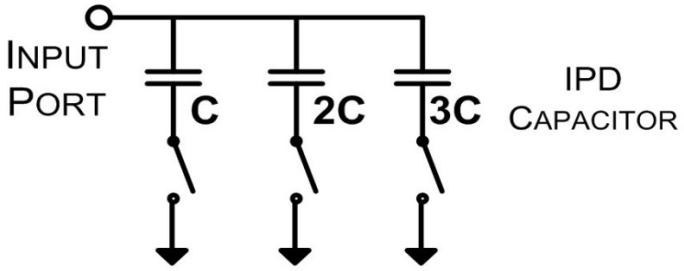
TABLE 5.3 COMPARISONS OF DIFFERENT TTD NETWORKS AT 1GHZ

Return Loss (dB)	Insertion Loss (dB)	Resolution (ps)	Size (mm x mm)	Power Consumption (mW)	Technology	Ref.
13-15	4-10	35	1.5 x 0.75	2-6.2	CMOS	[94]
14	13	2.8	1.6 x 2.5	2.6-6	CMOS	[95]
20-25	0.4-1.8	6.25	27 x 14	Zero	MEMS	[82]
22-27	0.5-0.7	5	3.5 x 2.6	Zero	MEMS	[96]
10-25	< 0.5	10	2 x 1.3	zero	MEMS	Ours
10-38	< 0.9	<1	2.9 x 1.6	zero	MEMS/BST	Ours

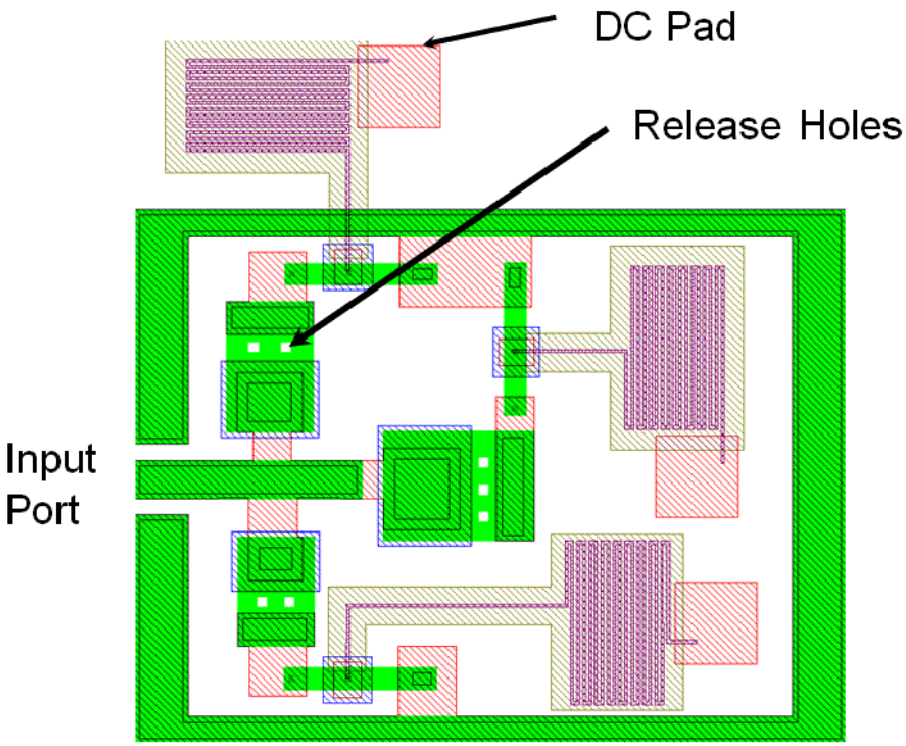
Table 5.3 shows a comparison of different TTD-networks implemented using different technologies at 1 GHz. In terms of achievable resolution and size, our IPD-based circuits that are proposed in this Chapter offer a superior performance to that obtained by other approaches [94]-[95],[82] and [96], particularly at low frequency applications. It can also be seen that our IPD circuit sizes are almost comparable to the CMOS designs with the advantage of having a relatively much lower insertion loss and no dc power consumption.

5.5 IPD-MEMS Digital Capacitor Bank

Figure 5.22 (a) shows the schematic of a 3-bit digital capacitor bank with three parallel connected branches. Each branch consists of an IPD capacitor monolithically integrated with a MEMS switch. In order to demonstrate the tunability, capacitance values from *C, 2C* and *3C* are designed where *C* is approximately 0.6 pF. To demonstrate the process, a capacitance density of 0.3-0.4 fF/ μm^2 is used. Figure 5.22 (b) and Figure 5.23 show the layout, and a photo of the 3-bit capacitor bank, respectively. As can be seen from Figure 5.22 (b), some release holes (10-15 μm) are designed to help an effective wet release for all the suspended structures. Furthermore, the bias line is mostly covered by silicon nitride (except the two protected far ends connected to the bias pads) to avoid any chemical attacks by other etchants during the process. Apart from that, the green area is where the first and second metal (thick) are used to minimize the RF signal loss.



(a)



(b)

Figure 5.22 3-bit IPD-MEMS digital capacitor bank. (a) Schematic diagram and (b) layout *chip size: 1.3 mm × 1.3 mm (including DC bias pads).

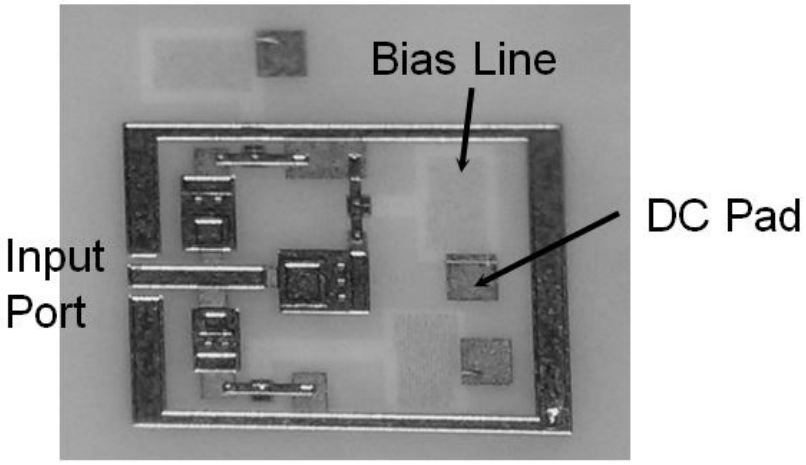
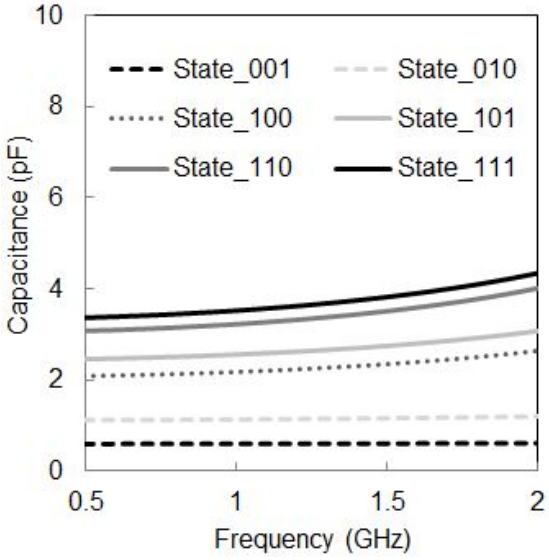
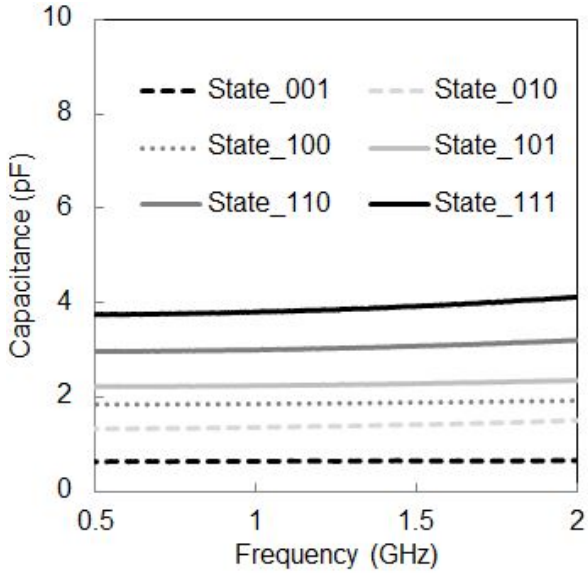


Figure 5.23 Photo of the proposed IPD-MEMS digital capacitor bank.



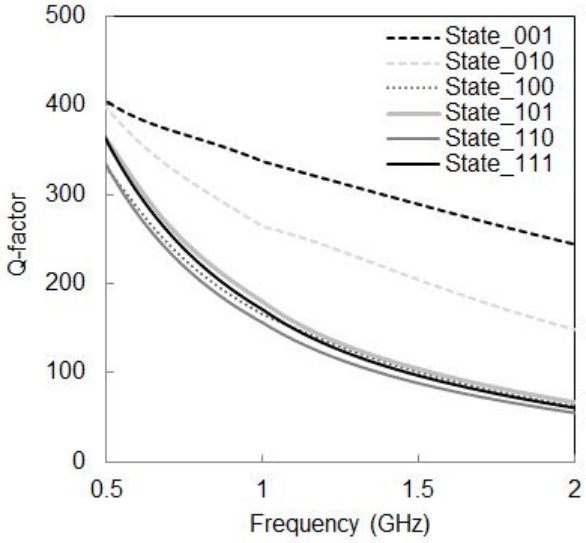
(a)



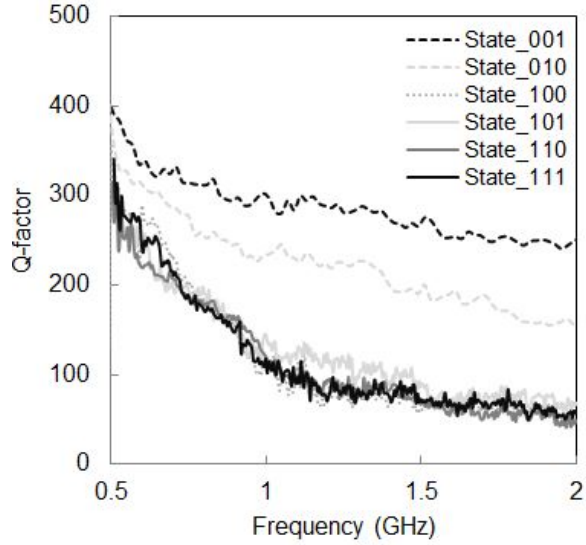
(b)

Figure 5.24 Capacitance change for the IPD-MEMS capacitor bank. (a) Simulated capacitance. (b) Measured capacitance.

The simulated and measured capacitance from 0.5 to 2 GHz, are shown in Figure 5.24 (a) and (b). At 1 GHz, a simulated capacitance between 0.6- 3.52 pF is obtained whereas the measured values ranges from 0.63 to 3.8 pF. As for the Q-factor, from the state 001 to state 111, the simulated results show a range of 150-330 whereas the measured results are approximately from 100 to 300, as shown in Figure 5.25 (a) and (b). It should be noted that it is very difficult to measure the quality factor accurately when it is above 100, since the resistive part of the capacitor is highly sensitive. However, the overall trend can be observed with good agreement between the simulations and measurements.



(a)



(b)

Figure 5.25 Simulated and measured quality factor for the IPD-MEMS capacitor bank.

5.6 Possible Applications for High-Q Varactors

A third-order coupled resonator bandpass filter is designed to demonstrate the importance of the IPD-MEMS high-Q capacitor bank [68], as shown in Figure 5.26. For commercial semiconductor varactors (~2 mm^2), Q-factors are approximately below 50 at around 1 GHz. In order to see the effects of the Q-factor of the capacitor towards the bandpass filter, the frequency response with different Q-factors is plotted, as shown in Figure 5.27 (a) and (b). As seen in Figure 5.27 (b), the

insertion loss at 1.9 GHz ranges from 0.07 dB to 1 dB when the Q-factor of the varactors changes from 5 to 50, while keeping all other elements unchanged. Based on the measured results from the previous section, the Q-factor is at least 50 at 2 GHz under 2 pF, and thus the effects from the IPD-MEMS capacitor bank are significantly less compared to the commercial varactors. More importantly, if a discrete varactor is used, such as a surface mount technology varactor, extra insertion loss and area due to the soldering and complicated bias network (resistor and by-pass capacitor) will be added. As a result, it may degrade the performance of the entire RF systems. With our IPD-MEMS technology, passive devices can be built monolithically with high-Q tunable capacitors as well as inductors. This tunable IPD solution can create more miniaturized passives components to some RF front-end modules, which will be very useful in future reconfigurable communication systems.

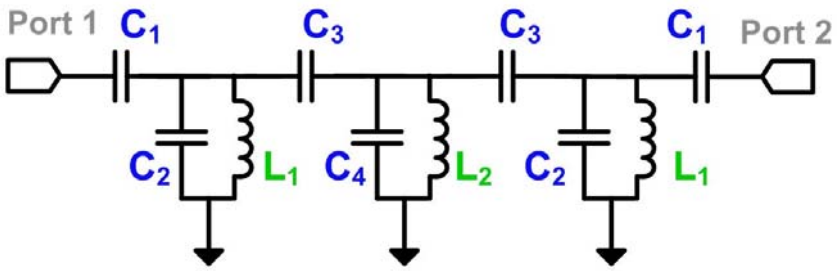
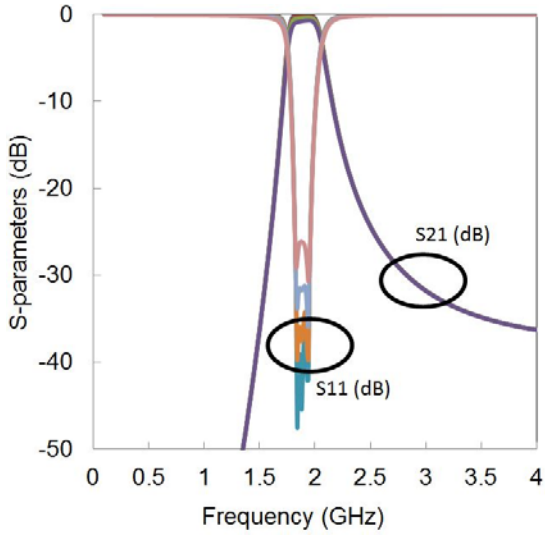


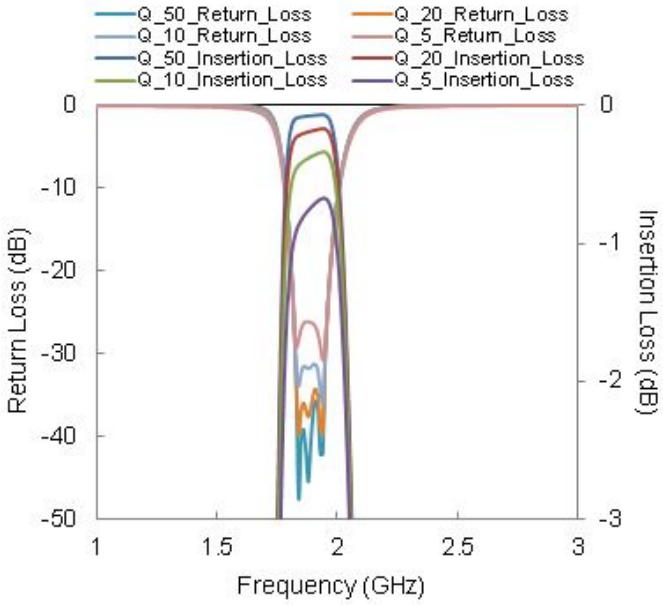
Figure 5.26 Schematic diagram of the third-order coupled resonator bandpass filter with values shown in Table 5.4.

TABLE 5.4 LUMPED ELEMENTS FOR THIRD-ORDER COUPLED RESONATOR BANDPASS FILTER

L_1	L_2	C_1	C_2	C_3	C_4
6.57 nH	6.5 nH	0.54 pF	0.47 pF	0.12 pF	0.85 pF



(a)



(b)

Figure 5.27 Simulated third-order coupled resonator bandpass filter with different Q-factor of varactors.

5.7 Summary

A monolithic alumina-based IPD-MEMS technology process is successfully demonstrated with two tunable applications. In the first application, a compact 3-bit IPD-MEMS TTD network, with both digital and continuous tuning are presented. A fine group delay varying from 79-138 ps is achieved, which can easily be extended to a wider tuning with difference choices of IPD inductors and capacitors. The MEMS and BST varactor approach is ideal for systems that require fine delay resolution. In the second tunable application, a switched capacitor bank with high-Q performance and tunability is demonstrated. Capacitance density can be further increased with a thinner silicon nitride. This proposed IPD-MEMS fabrication offers a simple platform to design components that require low-loss performance, tunability and small form factor for both hybrid and monolithic fashion.

CHAPTER 6

CONCLUSIONS

6.1 Contributions

An integrated passive device (IPD) fabrication process has been developed for the first time at the University of Waterloo. The process has been further expanded to allow monolithic integration of RF MEMS switches with IPD circuits. The main thesis contributions are as follows:

- High-Q lumped-elements L and C components have been fabricated and characterized. IPD miniature bandpass filters were fabricated using the process developed at the University of Waterloo and the commercial IPD fabrication process offered by ON Semiconductor. The measured results of the IPD filters were used to compare the performance of our in-house fabrication process with the commercial fabrication process [87].
- A high performance reconfigurable/tunable IPD bandstop filter with a wideband balun as a multi-chip module has been demonstrated. In particular, the tunable IPD bandstop filter is the smallest among the open literature with the same specifications including loss, tunability, and rejection level. The IPD phase inverter in the balun has been successfully modeled and demonstrated. Moreover, a compact bandpass filter

with a tunable transmission zero has been demonstrated experimentally. High power nonlinearity test results have been carried out for both the tunable bandstop filter and the bandpass filter with tunable transmission zero. The integration of IPD as well as BST technology can potentially lead to the realization of highly miniature filters with good RF performance for frequency agile applications [65], [71].

- RF MEMS switches fabricated using the IPD process have been fabricated and tested. The RF MEMS switches were monolithically integrated with IPD circuitry to demonstrate: (I) a compact 3-bit IPD-MEMS TTD network capable of realizing a delay circuit with a minimum step of 8 ps. A BST varactor was integrated with the 3-bit IPD-MEMS TDD circuit to demonstrate a delay network with a minimum step of 1ps. (II) A switched capacitor bank with high-Q performance and tunability. This proposed IPD-MEMS fabrication offers a simple platform to design components that require low-loss performance, tunability and small form factor [97].

6.2 Future Work

In this thesis, both fixed and tunable IPD platform are investigated, and more importantly, the monolithically-integrated IPD-MEMS fabrication is proposed in this thesis. However, there are several related areas that can be explored in the future:

- Investigation of the reliability of the IPD-MEMS devices.
- Investigation of power handling capability of IPD devices.
- Development of slow-wave structures in IPD to allow further miniaturization of RF circuits.
- Investigation the use of IPD distributed circuits in millimeter-wave applications [98].

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Appendix A

Fabrication of IPD Process on Glass Wafer

1. Substrate Cleaning

- Glass Wafer RCA 1 cleaning
- Soak wafers for 15 mins and rinse with DI water

2. Intlvac E-beam Evaporation (Cr/Au)

- Thickness 30 nm/50 nm

3. Mold for Electroplating

- Photoresist: AZ nLof 2035
- Spinning Speed: 3000 rpm
- Soft Bake: 1 min @ 110 °C
- Exposure Time: 16 s (Oriel Mask Aligner)
- Post Exposure Bake: 1 min at 110 °C
- Development Time1: 1 min
- Development Time2 (rotate wafer for 90 degrees): 1 min
- Hard Bake: 1 min at 110 °C

4. RIE Descum

- Pressure: 20 mTorr
- Gases and Flow Rates: O2, 20 SCCM
- RIE Power: 30 W
- ICP Power: 0 W
- Etching Time: 30 s

5. Au Electroplating

- Plating Current: 30 mA
- Plating time:15 mins

6. Intlvac E-beam Evaporation (Cr)

- Thickness 20 nm

7. Lift-off Kwik Strip (Electroplating mold removal)

Temp/Time: 70°C/40 mins

8. RIE Descum

- Pressure: 20 mTorr
- Gases and Flow Rates: O2, 20 SCCM
- RIE Power: 30 W
- ICP Power: 0 W
- Etching Time: 30 s

9. Electroplating Seed Layer Removal

- Au Etchant/Time: 30 s
- Cr Etchant/Time: 20 s

10. Intlvac Sputtering (TiW)

- Thickness 20 nm

11. PECVD SixNy Deposition

- Time:1500 s
- Thickness: 0.5 µm

12. Mold for Patterning SixNy

- Photoresist: AZ 3330
- Spinning Speed: 4000 rpm
- Soft Bake: 3 min @ 90 °C
- Exposure Time: 13 s (Oriel Mask Aligner)
- Post Exposure Bake: 2 min at 110 °C
- Development Time1: 50 s
- Hard Bake: 1 min at 110 °C

13. RIE Descum

- Pressure: 20 mTorr
- Gases and Flow Rates: O2, 20 SCCM
- RIE Power: 30 W
- ICP Power: 0 W
- Etching Time: 100 s

14. RIE SixNy and TiW

- Pressure: 250 mTorr
- Gases and Flow Rates: CF4, 20 SCCM
- RIE Power: 100 W

- ICP Power: 100 W
- Etching Time: 270 s

15. Kwik Strip (Mold removal)
    - Temp/Time: 70°C/40 mins
16. RIE Descum
    - Pressure: 20 mTorr
    - Gases and Flow Rates: O2, 20 SCCM
    - RIE Power: 30 W
    - ICP Power: 0 W
    - Etching Time: 65 s
17. Mold for Via
    - Photoresist: PI-2611
    - Spinning Speed: 4000 rpm
    - Bake1: 2 mins @ 90 °C
    - Bake2: 2 mins at 150 °C
18. Curing Furnace (with nitrogen flow)
    - 60 mins @ 350 °C
19. Intlvac Sputtering (Al: hard mask)
    - Thickness 0.2 μm
20. Mold for Patterning PI-2611
    - Photoresist: AZ 3330
    - Spinning Speed: 4000 rpm
    - Soft Bake: 3 min @ 90 °C
    - Exposure Time: 13 s (Oriel Mask Aligner)
    - Post Exposure Bake: 2 min at 110 °C
    - Development Time1: 50 s
    - Hard Bake: 1 min at 110 °C
21. RIE Descum
    - Pressure: 20 mTorr
    - Gases and Flow Rates: O2, 20 SCCM

- RIE Power: 30 W
- ICP Power: 0 W
- Etching Time: 60 s

22. Patterning Hard Mask (Al) Removal
    - PAN Etchant/Time: 60 s at 40 °C
23. RIE PI-2611
    - Pressure: 13 mTorr
    - Gases and Flow Rates: O2, 20 SCCM
    - RIE Power: 100 W
    - ICP Power: 200 W
    - Etching Time: 400 s
24. Residue Remover EKC-265
    - 2 mins @ 50 °C
25. Hard Mask (Al) Removal
    - PAN Etchant/Time: 7 mins at 45-50 °C
26. Intlvac E-beam Evaporation/Sputtering/E-beam Evaporation (Ti/Au/Ti)
    - Thickness 20 nm/100 nm/20 nm
27. Mold for Copper Electroplating
    - Photoresist: AZ 9260
    - Spinning Speed1: 500 rpm/15s (acl:10)
    - Spinning Speed2: 3000 rpm/45s
    - Soft Bake: 3 mins @ 110 °C
    - Rehydration: 30 mins
    - Exposure Time: 2 mins 15 s (Oriel Mask Aligner)
    - Development Time1: 6 mins
    - Hard Bake: 1 min at 110 °C
28. RIE Descum
    - Pressure: 20 mTorr
    - Gases and Flow Rates: O2, 20 SCCM

- RIE Power: 30 W
- ICP Power: 0 W
- Etching Time: 60 s

29. RIE Ti

- Pressure: 22 mTorr
- Gases and Flow Rates: CF4, 20 SCCM
- RIE Power: 250 W
- ICP Power: 0 W
- Etching Time: 70 s

30. Copper Electroplating

- Plating Current: 70 mA
- Plating time: 30 mins

31. Kwik Strip (Mold removal)

- Temp/Time: 80°C/60 mins

32. RIE Descum

- Pressure: 20 mTorr
- Gases and Flow Rates: O2, 20 SCCM
- RIE Power: 30 W
- ICP Power: 0 W
- Etching Time: 9 mins

33. RIE Ti/Au/Ti

- Pressure: 22 mTorr
- Gases and Flow Rates: CF4, 20 SCCM
- RIE Power: 250 W
- ICP Power: 0 W
- Etching Time: 10 mins

Appendix B

Fabrication of IPD Process on Alumina Wafer

1. Substrate Cleaning

- Alumina Wafer RCA 1 cleaning
- Soak wafers for 15 mins and rinse with DI water

2. Intlvac E-beam Evaporation (Cr/Au)

- Thickness 30 nm/50 nm

3. Mold for Electroplating

- Photoresist: AZ nLof 2035
- Spinning Speed: 3000 rpm
- Soft Bake: 1 min @ 110 °C
- Exposure Time: 3 s (Mask Aligner: MJB4)
- Post Exposure Bake: 1 min at 110 °C
- Development Time1: 1 min
- Development Time2 (rotate wafer for 90 degrees): 1 min
- Hard Bake: 1 min at 110 °C

4. RIE Descum

- Pressure: 20 mTorr
- Gases and Flow Rates: O2, 20 SCCM
- RIE Power: 30 W
- ICP Power: 0 W
- Etching Time: 30 s

5. Au Electroplating

- Plating Current: 30 mA
- Plating time:22 mins

6. Intlvac E-beam Evaporation (Cr)

- Thickness 20 nm

7. Lift-off Kwik Strip (Electroplating mold removal)

Temp/Time: 70°C/60 mins

8. RIE Descum

- Pressure: 20 mTorr
- Gases and Flow Rates: O2, 20 SCCM
- RIE Power: 30 W
- ICP Power: 0 W
- Etching Time: 30 s

9. Electroplating Seed Layer Removal

- Au Etchant/Time: 30 s
- Cr Etchant/Time: 55 s

10. Intlvac E-beam Evaporation (Ti)

- Thickness 20 nm

11. PECVD SixNy Deposition

- Time:20 mins
- Thickness: 0.5 μm

12. Mold for Patterning SixNy

- Photoresist: AZ 3330
- Spinning Speed: 4000 rpm
- Soft Bake: 3 min @ 90 °C
- Exposure Time: 3 s (Mask Aligner: MJB4)
- Post Exposure Bake: 2 min at 110 °C
- Development Time: 2 mins 20s
- Hard Bake: 1 min at 110 °C

13. RIE Descum

- Pressure: 20 mTorr
- Gases and Flow Rates: O2, 20 SCCM
- RIE Power: 30 W
- ICP Power: 0 W
- Etching Time: 100 s

14. RIE SixNy and Ti

- Pressure: 100 mTorr
- Gases and Flow Rates: CF4, 40 SCCM

- RIE Power: 100 W
- ICP Power: 0 W
- Etching Time: 280 s
- Pressure: 20 mTorr
- Gases and Flow Rates: CF4, 20 SCCM
- RIE Power: 250 W
- ICP Power: 0 W
- Etching Time: 350 s

15. Kwik Strip (Mold removal)
    - Temp/Time: 70°C/70 mins
16. RIE Descum
    - Pressure: 20 mTorr
    - Gases and Flow Rates: O2, 20 SCCM
    - RIE Power: 30 W
    - ICP Power: 0 W
    - Etching Time: 65 s
17. Mold for Via
    - Photoresist: PI-2611
    - Spinning Speed: 4000 rpm
    - Bake1: 2 mins @ 90 °C
    - Bake2: 2 mins at 150 °C
18. Curing Furnace (with nitrogen flow)
    - 60 mins @ 350 °C
19. Intlvac Sputtering Evaporation (Al: hard mask)
    - Thickness 0.2 μm
20. Mold for Patterning PI-2611
    - Photoresist: AZ 3330
    - Spinning Speed: 4000 rpm
    - Soft Bake: 3 min @ 90 °C
    - Exposure Time: 2.5 s (Oriel Mask Aligner)
    - Post Exposure Bake: 2 min at 110 °C

- Development Time1: 60 s
- Hard Bake: 1 min at 110 °C

21. RIE Descum

- Pressure: 20 mTorr
- Gases and Flow Rates: O2, 20 SCCM
- RIE Power: 30 W
- ICP Power: 0 W
- Etching Time: 60 s

22. Patterning Hard Mask (Al) Removal

- PAN Etchant/Time: 180 s at 40 °C

23. RIE PI-2611

- Pressure: 13 mTorr
- Gases and Flow Rates: O2, 20 SCCM
- RIE Power: 100 W
- ICP Power: 200 W
- Etching Time: 400 s

24. Residue Remover EKC-265

- 1 min @ 50 °C

25. Hard Mask (Al) Removal

- PAN Etchant/Time: 7 mins at 45-50 °C

26. Intlvac E-beam Evaporation/Sputtering/E-beam Evaporation (Ti/Au/Ti)

- Thickness 20 nm/100 nm/20 nm

27. Mold for Copper Electroplating

- Photoresist: AZ 9260
- Spinning Speed1 : 500 rpm/15s (acl:10)
- Spinning Speed1 : 3000 rpm/45s
- Soft Bake: 3 mins @ 110 °C
- Rehydration: 60 mins
- Exposure Time: 25 s (Mask Aligner: MJB4)
- Development Time1: 7 mins

- Hard Bake: 1 min at 110 °C

28. RIE Descum
    - Pressure: 20 mTorr
    - Gases and Flow Rates: O2, 20 SCCM
    - RIE Power: 30 W
    - ICP Power: 0 W
    - Etching Time: 60 s
29. RIE Ti
    - Pressure: 22 mTorr
    - Gases and Flow Rates: CF4, 20 SCCM
    - RIE Power: 250 W
    - ICP Power: 0 W
    - Etching Time: 70 s
30. Copper Electroplating
    - Plating Current: 100 mA
    - Plating time: 20 mins
31. Kwik Strip (Mold removal)
    - Temp/Time: 80°C/60 mins
32. RIE Descum
    - Pressure: 20 mTorr
    - Gases and Flow Rates: O2, 20 SCCM
    - RIE Power: 30 W
    - ICP Power: 0 W
    - Etching Time: 9 mins
33. RIE Ti/Au/Ti
    - Pressure: 22 mTorr
    - Gases and Flow Rates: CF4, 20 SCCM
    - RIE Power: 250 W
    - ICP Power: 0 W
    - Etching Time: 10 mins

Appendix C

Fabrication of IPD-MEMS Process on Alumina Wafer

1. Substrate Cleaning
    - Alumina Wafer RCA 1 cleaning
    - Soak wafers for 15 mins and rinse with DI water
2. Intlvac Sputtering (TiW) Thickness 20 nm
3. Mold for Patterning TiW
    - Photoresist: AZ 3330
    - Spinning Speed: 2000 rpm
    - Soft Bake: 3 mins @ 90 °C
    - Exposure Time: 3 s (Mask Aligner: MJB4)
    - Post Exposure Bake: 2 mins at 110 °C
    - Development Time: 2 mins 30 s
    - Hard Bake: 1 min at 110 °C
4. RIE Descum
    - Pressure: 20 mTorr
    - Gases and Flow Rates: O2, 20 SCCM
    - RIE Power: 30 W
    - ICP Power: 0 W
    - Etching Time: 60 s
5. Lift-off Kwik Strip (mold removal)
    - Temp/Time: 75°C/120 mins
6. RIE Descum
    - Pressure: 20 mTorr
    - Gases and Flow Rates: O2, 20 SCCM
    - RIE Power: 30 W
    - ICP Power: 0 W
    - Etching Time: 180 s
7. PECVD SixNy Deposition
    - Time:50 mins
    - Thickness: 1 μm

8. Mold for Patterning SixNy

- Photoresist: AZ 3330
- Spinning Speed: 4000 rpm
- Soft Bake: 3 min @ 90 °C
- Exposure Time: 2.5 s (Mask Aligner: MJB4)
- Post Exposure Bake: 2 min at 110 °C
- Development Time: 70s
- Hard Bake: 1 min at 110 °C

9. RIE Descum

- Pressure: 20 mTorr
- Gases and Flow Rates: O2, 20 SCCM
- RIE Power: 30 W
- ICP Power: 0 W
- Etching Time: 60 s

10. Buffered HF Etching

- Time: 40s

11. Lift-off Kwik Strip (mold removal)

- Temp/Time: 75°C/120 mins

12. Intlvac E-beam Evaporation (Cr/Au)

- Thickness 30 nm/60 nm

13. Mold for Electroplating

- Photoresist: AZ nLof 2035
- Spinning Speed: 3000 rpm
- Soft Bake: 2 mins @ 110 °C
- Exposure Time: 3 s (Mask Aligner: MJB4)
- Post Exposure Bake: 1 min at 110 °C
- Development Time1: 3 min
- Hard Bake: 1 min at 110 °C

14. RIE Descum

- Pressure: 20 mTorr
- Gases and Flow Rates: O2, 20 SCCM

- RIE Power: 30 W
- ICP Power: 0 W
- Etching Time: 60 s

15. Au Electroplating

- Plating Current: 70 mA
- Plating time: 12 mins

14. Intlvac E-beam Evaporation (Cr)

- Thickness 20 nm

15. Lift-off Kwik Strip (Electroplating mold removal)

Temp/Time: 70°C/60 mins

16. RIE Descum

- Pressure: 20 mTorr
- Gases and Flow Rates: O2, 20 SCCM
- RIE Power: 30 W
- ICP Power: 0 W
- Etching Time: 30 s

17. Electroplating Seed Layer Removal

- Au Etchant/Time: 30 s
- Cr Etchant/Time: 55 s

18. Intlvac E-beam Evaporation (Ti)

- Thickness 20 nm

19. PECVD SixNy Deposition

- Time:20 mins
- Thickness: 0.5 μm

20. Mold for Patterning SixNy

- Photoresist: AZ 3330
- Spinning Speed: 4000 rpm
- Soft Bake: 3 min @ 90 °C
- Exposure Time: 3 s (Mask Aligner: MJB4)
- Post Exposure Bake: 2 min at 110 °C

- Development Time: 2 mins 20s
- Hard Bake: 1 min at 110 °C

21. RIE Descum

- Pressure: 20 mTorr
- Gases and Flow Rates: O2, 20 SCCM
- RIE Power: 30 W
- ICP Power: 0 W
- Etching Time: 100 s

22. Mold for 2nd metal

- Photoresist: PI-2555
- Spinning Speed: 3500 rpm
- Bake1: 2 mins @ 90 °C
- Bake2: 160 mins at 160 °C

23. Intlvac Sputtering (Al: hard mask)

- Thickness 0.2 μm

24. Mold for Patterning Al

- Photoresist: AZ 3330
- Spinning Speed: 4000 rpm
- Soft Bake: 3 min @ 90 °C
- Exposure Time: 3 s (Mask Aligner: MJB4)
- Post Exposure Bake: 2 min at 110 °C
- Development Time: 2 mins 20s
- Hard Bake: 1 min at 110 °C

25. RIE Descum

- Pressure: 20 mTorr
- Gases and Flow Rates: O2, 20 SCCM
- RIE Power: 30 W
- ICP Power: 0 W
- Etching Time: 60 s

26. Patterning Hard Mask (Al)

- PAN Etchant/Time: 6 mins at 40 °C

27. Wash Photoresist with Acetone
28. RIE PI-2555
    - Pressure: 13 mTorr
    - Gases and Flow Rates: O2, 20 SCCM
    - RIE Power: 100 W
    - ICP Power: 200 W
    - Etching Time: 150 s
29. Mold
    - Photoresist: AZ 3330
    - Spinning Speed: 4000 rpm
    - Soft Bake: 3 min @ 90 °C
    - Exposure Time: 3 s (Mask Aligner: MJB4)
    - Post Exposure Bake: 3 min at 110 °C
    - Development Time: 2 mins 20s
30. RIE Descum
    - Pressure: 20 mTorr
    - Gases and Flow Rates: O2, 20 SCCM
    - RIE Power: 30 W
    - ICP Power: 0 W
    - Etching Time: 180 s
31. Patterning Hard Mask (Al) Removal
    - PAN Etchant/Time: 6 mins at 40 °C
32. Wash Photoresist with Acetone
33. RIE PI-2555
    - Pressure: 13 mTorr
    - Gases and Flow Rates: O2, 20 SCCM
    - RIE Power: 100 W
    - ICP Power: 200 W
    - Etching Time: 60 s
34. Hard Mask Removal (Al)
    - PAN Etchant/Time: 6 mins at 40 °C

35. Intlvac Sputtering (Au)

- Thickness 0.2 μm

36. Mold for Patterning Electroplated Thick Metal

- Photoresist: AZ 9260
- Spinning Speed: 2000 rpm
- Soft Bake: 3 min @ 110 °C
- Exposure Time: 25 s (Mask Aligner: MJB4)
- Development Time: 7 mins
- Hard Bake: 1 min at 110 °C

37. RIE Descum

- Pressure: 20 mTorr
- Gases and Flow Rates: O2, 20 SCCM
- RIE Power: 30 W
- ICP Power: 0 W
- Etching Time: 60 s

38. Au Electroplating

- Plating Current: 110 mA
- Plating time: 21 mins

39. Intlvac E-beam Evaporation (Cr)

- Thickness 30 nm

40. Kwik Strip (Thick Mold Removal)

- Temp/Time: 75°C/45 mins

41. RIE Descum

- Pressure: 20 mTorr
- Gases and Flow Rates: O2, 20 SCCM
- RIE Power: 30 W
- ICP Power: 0 W
- Etching Time: 120 s

42. Electroplating Seed Layer Removal

- Au Etchant/Time: 4 mins 45s

- Cr Etchant/Time: 55 s

43. Dicing with Photoresist
44. EKC Release
    - 65°C/20 mins
45. Release with Critical Point Dryer (CO_2)