Broadband Doherty Power Amplifier using Symmetrical GaN Transistors

by

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AUTHOR'S DECLARATION

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Abstract

The wireless industry has seen a tremendous growth in its users over the last decade. This has led the industry to adapt a number of new standards allowing for better use of the scarce and often very fragmented frequency spectrum. [1] The new standards have brought with them the use of OFDM signaling to allow for higher data rates and better robustness against frequency selective channel interference. The OFDM protocols combined with multi-standard radios however have provided many challenges to the radio frequency, RF, industry with the largest challenge presented to the power amplifier design. The OFDM signals are well known for their high peak to average power ratio which forces the RF equipment to work at significant back-off compared to peak power. This unfortunately leads to rather low system efficiencies.

To address the problem the Doherty power amplifier has been brought back into the design community as it directly solves the issues related to average power efficiency. To date however many of the Doherty designs have focused on the narrowband application of the power amplifier often targeting a single standard with bandwidths directly tied to the operational band which at best is usually only couple hundred MHz wide. With the recent changes in the standards and the ever growing desire to provide several standards on one radio the Doherty has to be redesigned to allow for broadband communications.

This thesis examines the major sources of bandwidth limitation in the Doherty power amplifier and provides a review of the current approaches to solving the problem. It then goes on to propose several changes in the Doherty architecture to allow for the use of complex impedance to provide both higher efficiency at back-off and wider operational bandwidth.

The proposed technique was then used to design a symmetrical Doherty power amplifier targeted to operate in the 1.8 – 2.8 GHz frequency range with 42 dBm of output power and back-off efficiency above 50%.

Acknowledgements

This thesis contains the results of my research related to high efficiency power amplifiers and in particular the Doherty power amplifier. The knowledge contained within is the result of years of learning from lectures, books, literature and countless hours of simulations. This thesis however is also the result of some guidance from several colleagues whom I deem very knowledgeable in the field. Special thanks go out to Hassan Sarbishaei, Hamed Golestaneh and Mehdi Naseri Ali Abadi who have supported me along the way.

I would also like to thank my readers Professor Lan Wei and Professor Peter Levine.

Last but not least I would also like to thank my supervisor Professor Boumaiza for supporting me on this journey and encouraging me along the way.

Dedication

I would like to dedicate this work to my family. I would not be where I am today if it wasn't for all the great support that I have received from them throughout the years. Their love has kept me going during the highs and lows of this work.

Specifically I would like to thank my husband, my mom and my children for always supporting me in my pursuit of higher learning. They have always been and always will be my corner stone.

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List of Acronyms

3GPP	3rd Generation Partnership Project
Aux	Auxiliary
DC	Direct current
DE	Drain efficiency
DPA	Doherty power amplifier
EM	Electromagnetic
FET	Field effect transistor
IB	Impedance buffer
IIN	Impedance inverting network
ITN	Impedance transformation network
ME	Matching element
LTE	Long Term Evolution
LTE-A	LTE advanced
OFDM	Orthogonal Frequency Division Multiplexing
PA	Power amplifier
PAE	Power added efficiency
PAPR	Peak to average power ratio
Pout	Output power
RF	Radio frequency
WiMAX	Worldwide Interoperability for Microwave Access

Chapter 1 Introduction

1.1 Motivation

The Orthogonal Frequency Division Multiplexing technique, or OFDM for short, has been around for over 40 years with earliest work dating back to 1971 by Weinstein and Ebert. [2] In recent years however it has become more popular due to the increasing demand for low cost high bandwidth solutions needed both for short and long range applications. The lower subcarrier networks such as 802.11a have been around for quite some time providing customers with up to 54 Mb/s wireless connectivity. To increase bandwidth and adaptability as well as to provide mobility solutions 802.16d and 802.16e, also known as WiMAX, have been introduced to the market. Their success however has been marked as marginal in comparison to the full potential that the Long Term Evolution, LTE, standard has brought to the market. In the last couple of years the LTE standard has further evolved to allow for carrier aggregation and signal transmission over contiguous and non-contiguous frequency bands. This however although very beneficial to both the customer and the network provider has created several major problems for the radio hardware designer. On top of that the ability to provide service over multiple standards has long been desired in wireless communications.

The LTE and LTE-Advanced standards rely heavily on the use of OFDM signaling to provide the necessary data throughput. The major drawback of OFDM and combined standard communications however is related to the high peak to average power ratio, PAPR, of the time domain signal. [1] This type of signal is unlike anything that the radio designers had to face in the past. Signals with excess of 12 dB PAPR are now the norm. Such large PAPR signals are detrimental to the cost efficiency across the entire hardware design spectrum. To ease up the hardware requirements many high PAPR signals will go through clipping and filtering before reaching the RF hardware. Often such signals will be reduced to 6-8 dB PAPR. Although this is an improvement over the original 12 dB it is still very challenging to handle from the design perspective.

One of the most important components in any wireless system is the power amplifier. To date most power amplifiers have been designed for peak power at which they were optimized for highest efficiency. For a single carrier system that is not subjected to envelope varying signals that is perfectly fine. For signals with at least 6 dB PAPR power amplifier optimized for peak power no longer provides best efficiency at the required back-off.

This renders the classical power amplifier designs to efficiency well below 40% and that is in the ideal case where things such as knee voltage, package parasitics and harmonics have not been accounted for.

There have been few attempts in the literature to provide designs that focus on high efficiency at the average power, one of the most common ones is the Doherty power amplifier. Unfortunately to date the DPA has been used for narrowband applications. The focus of this thesis is to provide a workable solution for the Doherty power amplifier such that it can not only provide high efficiency at back-off but also maintain this efficiency across the 1.8 GHz – 2.8 GHz frequency band.

1.2 Thesis organization

This thesis provides detailed design of high efficiency power amplifier tailored specifically for the 3GPP market. The focus of the following chapters is to introduce the reader to the intricacies of the power amplifier design for high peak to average power ratio signals consistent with today's market.

Chapter 2 provides the background theory on power amplifier design. It includes the analysis of the current source with respect to conventional operating classes A, AB, B and C. It also includes the basic concepts of the Doherty power amplifier.

Chapter 3 focuses on the bandwidth analysis of the Doherty power amplifier. It summarizes current approaches to bandwidth enhancement through a literature review. It then goes on to explain the primary sources of bandwidth limitation and explores possible solutions.

Chapter 4 builds on the developed theory and uses the concept of complex terminating impedance as well as harmonic tuning to extend the operational bandwidth of the conventional Doherty power amplifier. It then proceeds to show the simulation results obtained at both schematic and EM levels.

Chapter 5 concludes the thesis with a summary of the simulation results against current known works. It also summarizes the overall approach taken to achieve high efficiency across wide bandwidth.

Chapter 2 Power amplifier design

2.1 Power amplifier basics

Every power amplifier design no matter how complicated begins with an analysis based on a simplified device model. In this thesis the device model used to evaluate the preliminary design parameters will be based on the simplified FET device model shown Figure 2-1: Simplified equivalent circuit for FET devices Figure 2-1 in which the package as well as most other parasitics have been ignored and only the voltage controlled current source is modelled as nonlinear. [3].

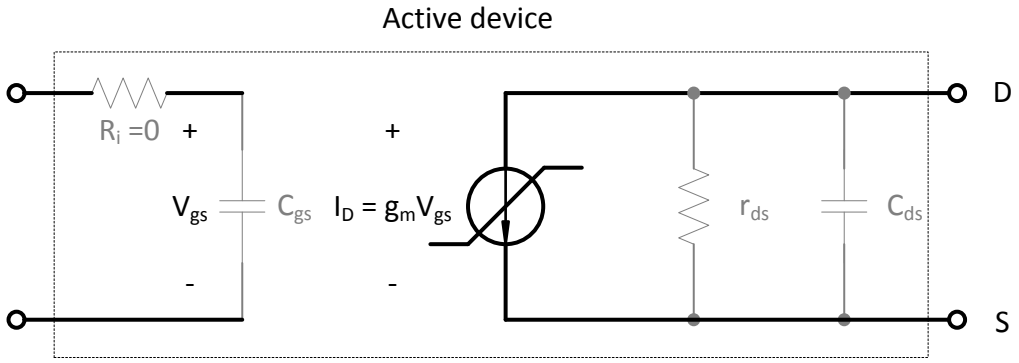

Figure 2-1: Simplified equivalent circuit for FET devices [3]

2.1.1 Output current and harmonic content

In the simplified model the voltage controlled current source is the only element that requires detailed analysis and this section will focus on developing a comprehensive understanding of its function in the amplifier design.

The current in the active device can be described as a sum of the DC current, the fundamental and an infinite number of harmonics.

$$i_D(t) = I_{DC} + I_1 \cos(\omega t) + I_2 \cos(2\omega t) + I_3 \cos(3\omega t) + \cdots \quad (2.1)$$

Under the truncated sinusoid assumption the current coefficients can be found using the conduction angle, θ, and the equations derived in reference [3]. The drain current can be described using equation (2.2) which has been graphically represented in Figure 2-2.

$$I_a(t) = \begin{cases} \frac{I_{max}}{1-\cos\left(\frac{\theta}{2}\right)} * \left[\cos(\omega t) - \cos\left(\frac{\theta}{2}\right)\right] & if\ |\omega t| \leq \frac{\theta}{2} \\ 0 & otherwise \end{cases} \quad (2.2)$$

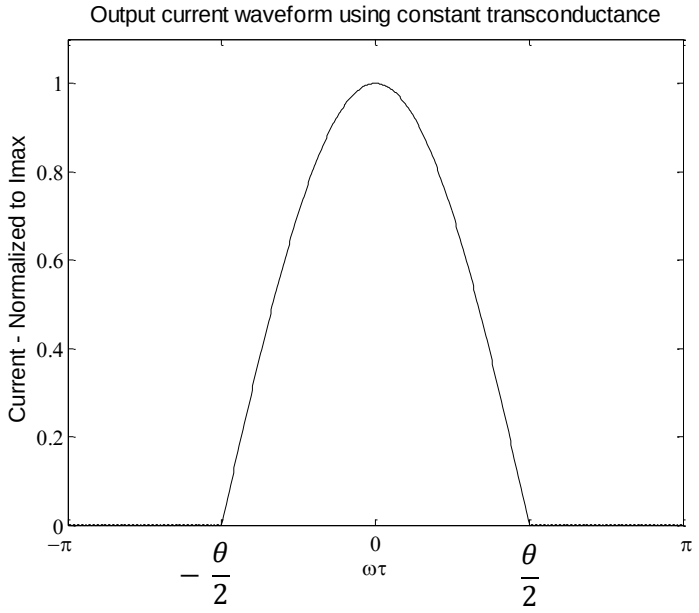

Figure 2-2: Drain current waveform using constant g_m

Using Fourier series the individual current components at dc, fundamental and harmonics can be found using equations (2.3) - (2.5).

$$I_{DC} = \frac{I_{max}}{2*\pi} * \frac{2*\sin\left(\frac{\theta}{2}\right) - \theta*\cos(\frac{\theta}{2})}{1-\cos(\frac{\theta}{2})} \quad (2.3)$$

$$I_1 = \frac{I_{max}}{2*\pi} * \frac{\theta - \sin(\theta)}{1-\cos(\frac{\theta}{2})} \quad (2.4)$$

$$I_n = \frac{2*I_{max}}{\pi} * \frac{\sin\left(n*\frac{\theta}{2}\right)*\cos\left(\frac{\theta}{2}\right) - n*\sin\left(\frac{\theta}{2}\right)*\cos\left(n*\frac{\theta}{2}\right)}{n*(n^2-1)\left(1-\cos\left(\frac{\theta}{2}\right)\right)} \quad (2.5)$$

$$for\ n > 2$$

The values of the individual current components can again be graphed to give the reader a visual representation of the current source's behavior as shown in Figure 2-3. There are several interesting points that can be observed while looking at the current graph as a function of the conduction angle.

a) The output power is approximately constant between the conduction angle of 180 – 360 degrees
b) The harmonic levels decrease with increasing harmonic order
c) The dominating current harmonics while the conduction angle varies from 180-360 degrees are the 2nd and the 3rd harmonics
d) The 2nd harmonic current content is in-phase with the fundamental while the 3rd harmonic component is out-of-phase
e) If conduction angle falls below 180 degrees both the 2nd and the 3rd harmonics are in phase with the fundamental
f) If conduction angle falls below 180 degrees but drops no lower than 135 degrees then the 4th and 5th harmonics will also contribute to the overall current. This is important for Class C power amplifiers and Harmonic Balance simulation setup which must use at least 5th harmonic order setup to achieve accurate results.

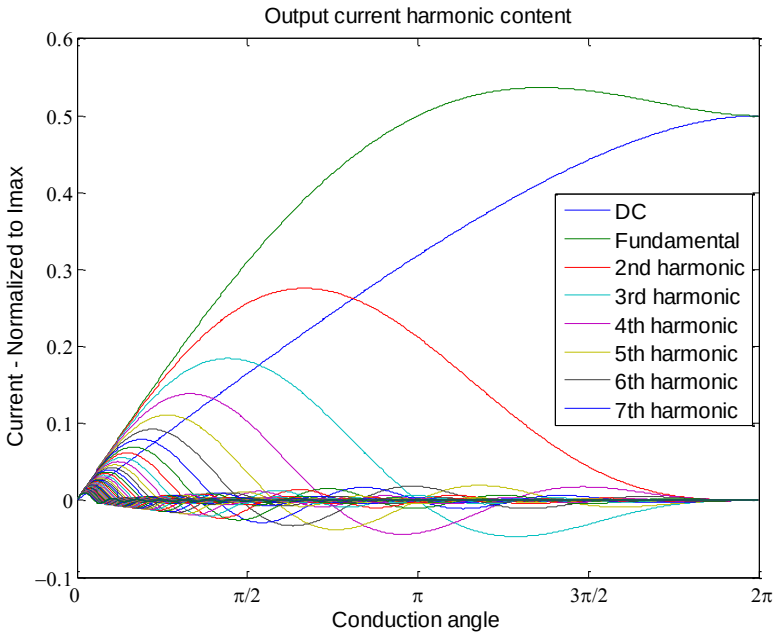

Figure 2-3: Current components of a truncated sinusoidal waveform

2.1.2 Class of operation

The conduction angle of the current source dictates which specific class of operation the PA is working in. If the power amplifier is always on its conduction angle is 360 degrees. If the current source is only on half the time on then the amplifier is operating in Class B. Anything above class B is known as class AB and anything below is Class C. The performance of each class can be described by output power and efficiency both determined by the conduction angle.

$$P_{out,f_o} = \frac{I_{f_o} * V_{f_o}}{2} = \frac{I_1 V_1}{2} = \frac{V_1}{2} * \frac{I_{max}}{2 * \pi} * \frac{\theta - \sin(\theta)}{1 - \cos(\frac{\theta}{2})} \quad (2.6)$$

$$\eta = \frac{P_{out,f_o}}{P_{DC}} = \frac{1}{2} * \frac{\theta - \sin(\theta)}{2 * \sin\left(\frac{\theta}{2}\right) - \varphi * \cos(\frac{\theta}{2})} \quad (2.7)$$

Table 2-1 shows performance summary as well as some other interesting characteristics of each of the operating classes. It can be seen that as the conduction angle decreases from 360 degrees in class A to below 180 degrees in class C the dc component of the current drops off to zero. It is this drop off that increases the drain efficiency. A conduction angle below 180 degrees however also sees a reduction in the fundamental power and an increase in harmonic content. So although the efficiency continues to climb towards the 100% mark the power drop in the fundamental makes the device less desirable for wireless power amplifier applications due to the lower power utilization factor.

Table 2-1 Characteristics of PA operational classes

Class	A	AB	B	C
Conduction angle	360	220	180	135
IDC	0.5* Imax	0.3786* Imax	0.318 * Imax	0.244* Imax
I1	0.5 * Imax	0.5316 * Imax	0.5 * Imax	0.425 * Imax
I2	0	0.1312* Imax	0.212*Imax	0.2711* Imax
I3	0	-0.0449* Imax	0	0.1037 * Imax
Vdc-Vk	24	24	24	24
Imax, A	1.67	1.67	1.67	1.67
RL, ohms	28.8	27	28.8	33.8
PDC, W	23.38	17.7	14.86	11.4
P1, W	10	10.65	10	8.5
Drain Efficiency	43%	60%	67%	74%

In Table 2-1 power and efficiency calculations assume that the load is purely resistive and that the harmonics that do occur in the current waveform are properly shorted and thus do not add to the fundamental voltage. There are however several classes of operation where harmonic contents can be utilized through proper loading to further enhance the efficiency of the overall system.

In general when switching between classes of operation the following can be observed [3]

a) The output power decreases with a decrease in conduction angle.
b) DC power decreases with a decrease in conduction angle.
c) Efficiency increases with a decrease in conduction angle.
d) Output load increases with a decrease in conduction angle.

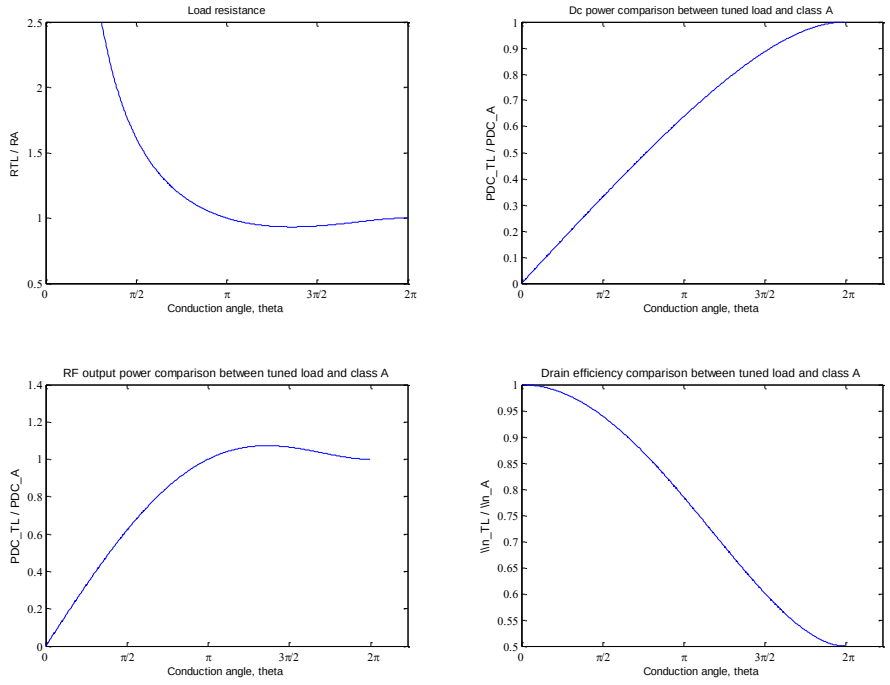

Figure 2-4: Amplifier characteristics as a function of conduction angle [3]

2.1.3 Harmonic tuning and high efficiency power amplifiers design

In high frequency power amplifier design the effectiveness of controlling higher harmonics is inversely proportional to the center frequency, i.e. the higher the frequency of operation the lower the number of harmonics that can be effectively controlled. In fact in most designs only the second and

third harmonic are usually considered. The circuit complexity of trying to control harmonics above the third results in negligible benefits. [3] Also at some point the output capacitance will effectively short the higher harmonics not allowing them to be used for waveform shaping. [3]

In general the efficiency of the power amplifier utilizing harmonic terminations can be described using equation (2.8) found in reference [3].

$$\eta = \frac{P_{out,f_o}}{P_{dissipated} + P_{out,f_o} + P_{out,2f_o + P_{out,3f_o}}} \tag{2.8}$$

From the equation it becomes very obvious that efficiency can be optimized by minimizing the sum of the dissipated power and the power delivered to the second and third harmonics or by maximizing the fundamental power. [3]

While assuming a truncated sinusoid for the output current and only the first two harmonics the output voltage at the load can be written as in reference [3]

$$v_{DS}(t) = V_{DD} - V_1 \cos(\omega t + \theta_1) - V_2 \cos(2\omega t + \theta_2) - V_3 \cos(3\omega t + \theta_3) \tag{2.9}$$

which when normalized with respect to the fundamental voltage will result in

$$v_{DS}(t) = V_{DD} - V_1[\cos(\omega t + \theta_1) - k_2 \cos(2\omega t + \theta_2) - k_3 \cos(3\omega t + \theta_3)] \tag{2.10}$$

where

$$k_2 = \frac{V_2}{V_1} \; and \; k_3 = \frac{V_3}{V_1}$$
$$V_n = |Z_n| * I_n \tag{2.11}$$
$$\theta_n = phase(Z_n)$$

The main goal of harmonic tuning is to provide proper wave shaping (proper k_2 and k_3) such that the overlap between the output voltage and output current is minimized while trying to deliver the maximum possible fundamental power. In many cases harmonic tuning is performed using impedance buffers. The concept of impedance buffers, IB , has been described by Colantonio et al in [4]. The IB unit is responsible for the introduction of either a short or an open circuit in a specific part of the matching network. This ensures that any impedance following the insertion point is not

contributing to the overall impedance at the specific frequency. To ensure that the impedance seen by the transistor at the desired frequency is the optimal one a matching element, ME, has to be inserted between the buffer and the transistor. Thus for most designs requiring control up to the third harmonic the output matching network will look as shown in Figure 2-5.

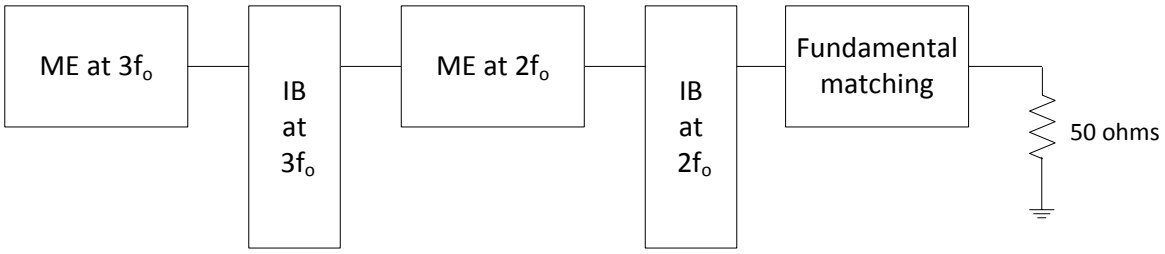

Figure 2-5: Harmonic control circuit setup [4].

2.2 Doherty power amplifier

The above section covered the fundamentals of single ended power amplifiers. This section will focus on the application of already gained knowledge to the design of higher efficiency power amplifiers. The main problem with a single ended power amplifier, as discussed before, is the fact that it is designed for optimal efficiency at peak power and thus will suffer significant degradation at any power other than peak. For example a class B power amplifier although able to theoretically achieve 78.5% efficiency at peak power will not be able to achieve even 40% at 6 dB back-off. The problem in single ended power amplifiers is related to a fixed load impedance that is unable to compensate for a variation in the input signal. This section of the thesis will examine the application of power amplifiers that are capable of achieving high efficiencies at the average power.

2.2.1 Basic concepts

The Doherty power amplifier depends on the active modulation concept which allows the amplifier to operate at maximum efficiency for a specified output power range while varying the output load. [3] The Doherty amplifier is composed of a Main device which operates across the entire input power range and an Auxiliary amplifier that only turns on at a specified back-off power when the Main device has reached its maximum voltage swing. To avoid voltage variation across the load an impedance inverting network has to be added in the Main path of the amplifier. This ensures that while the impedance is changing at the output of the Main the current at the output inverter is held

constant and the overall voltage swing at the load is dependent on the Auxiliary current. [3] To ensure that the two signal paths are added in phase at the output of the Doherty amplifier a phase compensating network has to be included at the input to the Auxiliary amplifier. The entire system level Doherty power amplifier, DPA, is shown in Figure 2-6.

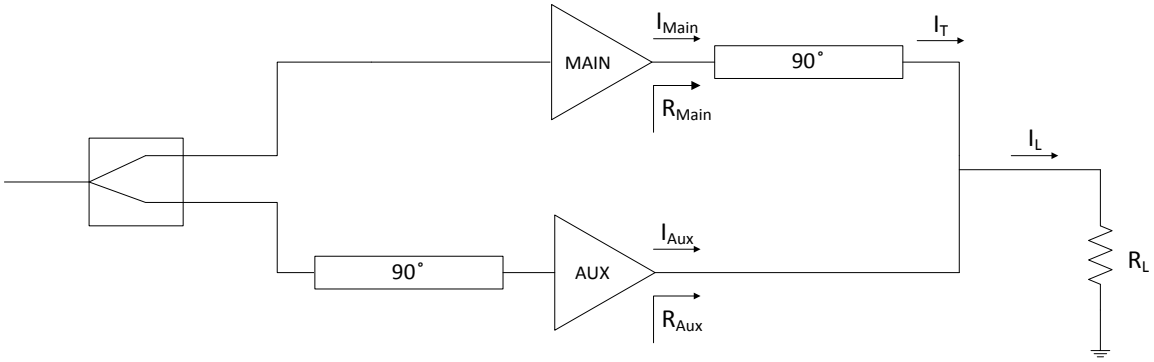

Figure 2-6: Doherty power amplifier [3]

Since the efficiency of a tuned load power amplifier depends strictly on its ratio of output voltage to bias voltage the efficiency of the Doherty power amplifier can be maintained at maximum regardless of the output power level if the output load is properly modulated such that $V_{DD} - V_{knee}$ is maintained over the required region [3]

$$\eta = \frac{\pi}{4} * \frac{V_{output}}{V_{DD}} = \frac{\pi}{4} * \frac{V_{DD} - V_{knee}}{V_{DD}} \tag{2.12}$$

2.2.1.1 Load modulation

To ensure highest efficiency even when the signal is amplitude modulated Doherty proposed the amplifier shown in Figure 2-6. A simpler version illustrating the desired impedance modulation concept and the specifics of the Doherty amplifier operation is shown in Figure 2-7 .

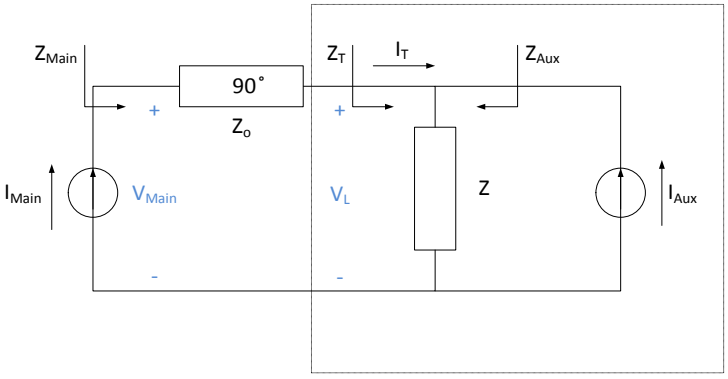

Figure 2-7: Simplified Doherty power amplifier [3]

It can be seen from the above that the impedance that each current source sees is controlled by the current level of the other. It can also be seen that while the Auxiliary amplifier is turned off the Auxiliary impedance becomes infinite while the Main amplifier at the output of the transmission line sees the optimum load of Z.

$$Z_T = Z\frac{I_T + I_{Aux}}{I_T} = Z\left(1 + \frac{I_{Aux}}{I_T}\right) \tag{2.13}$$

$$Z_{Aux} = Z\frac{I_T + I_{Aux}}{I_{Aux}} = Z\left(1 + \frac{I_T}{I_{Aux}}\right) \tag{2.14}$$

2.2.1.2 Inverter

It can be seen that if the inverter network was not included in the main path the output voltage would not be held constant during impedance modulation at the Main amplifier. [3] This of course would result in an operating region that is not desired by the Doherty setup. To avoid this problem the quarter-wavelength line has been inserted between the Main amplifier output and the load. This ensures the consistency of current I_T while the output voltage of the Main amplifier reaches its maximum swing $V_{DD} - V_k$ in the Doherty power region which can be illustrated using the ABCD parameters.

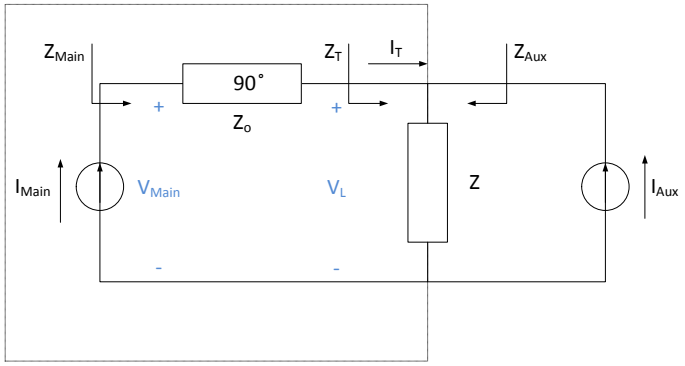

Figure 2-8: Simplified Doherty power amplifier highlighting the inverter section [3]

$$\begin{bmatrix} V_{Main} \\ I_{Main} \end{bmatrix} = \begin{bmatrix} 0 & jZ_0 \\ \frac{j}{Z_0} & 0 \end{bmatrix} * \begin{bmatrix} V_L \\ I_T \end{bmatrix} \tag{2.15}$$

If the above equations are properly expended it can be seen that none of the voltages or currents actually depend on the terminating impedance but only on the characteristic impedance of the quarter-wavelength line. [3]

2.2.2 Doherty power amplifier behavior

The Doherty power amplifier has two distinct operating regions. The first region is fully defined by the operation of the Main device only while the Auxiliary is completely turned off. This is known as the *low power region* and can be illustrated using the following:

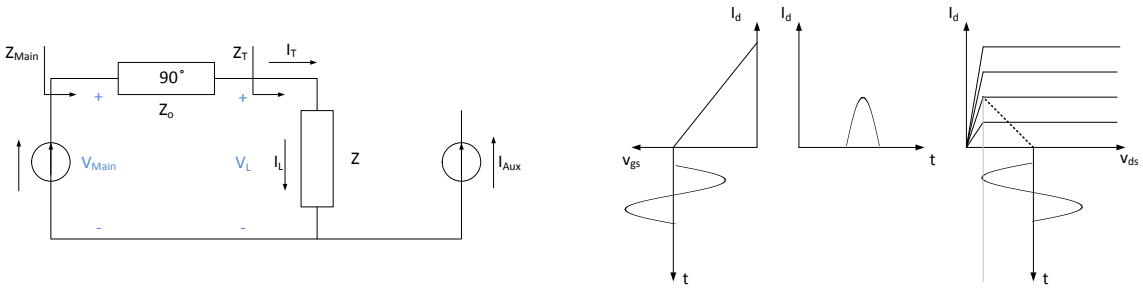

Figure 2-9: Doherty power amplifier in back-off [3]

In this region the power amplifier operates in the class of operation chosen for the Main amplifier which is often selected to be class AB. From the impedance equations it can bee see that the amplifier sees the impedance Z which is transformed by the inverter to

$$Z_{Main} = \frac{{Z_0}^2}{Z_T} = \frac{{Z_0}^2}{Z} \tag{2.16}$$

The second region is known as the *medium power region* and it is defined by the simultaneous operation of the two amplifiers. In this region the Auxiliary amplifier is turned on as soon as the Main device reaches its full voltage swing and the critical current level, $I_{critical}$. When this desired back-off point is reached the Auxiliary amplifier starts to contribute to the overall load current and thus modulates the impedance seen by both amplifiers. Looking from the load node both impedances reach 2Z when both amplifiers have reached its full fundamental currents assuming a 6 dB back-off. However due to the inverter the Main impedance is actually decreased as the output node impedance is increased thus providing the proper loading of the Main amplifier and resulting in continual increase of current and power while the output voltage of the main amplifier remains constant.

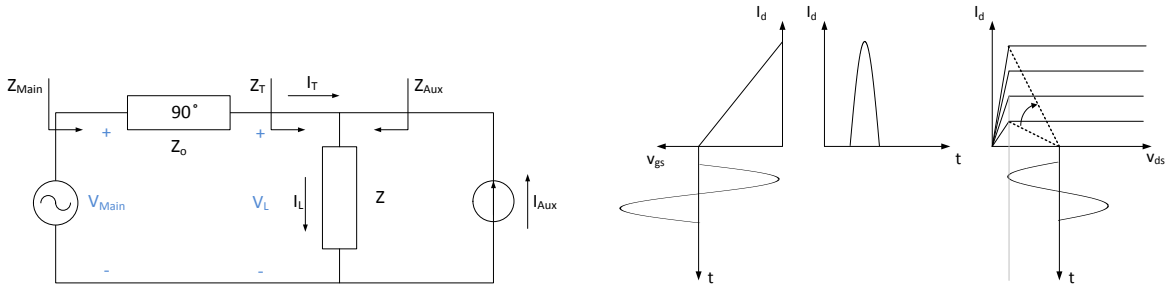

Figure 2-10: Doherty power amplifier at full power [3]

$$Z_{Main} = \frac{{Z_0}^2}{Z_T} = \frac{{Z_0}^2}{Z\left(1 + \frac{I_{Aux}}{I_T}\right)} \tag{2.17}$$

2.2.3 Drain current analysis in the Doherty power amplifier

2.2.3.1 Main amplifier

As with tuned load single ended power amplifiers the analysis of the Doherty amplifier has to start with the current waveform analysis. Again a simplified model will be used with the constant transconductance profile which will result in a truncated sinusoid at the output of the current source. The currents as they are dependent on the input power level will be analyzed using a parameter x which describes the signal drive level from DC (x=0) to maximum value of I_M (x=1). [3]

The drain current itself is a function of the bias current and a sinusoidal drive with a specific peak level. The analysis shown in this section has been expended from the derivations found in reference [3].

Starting at full power the current waveform of the main amplifier can be derived using Figure 2-11.

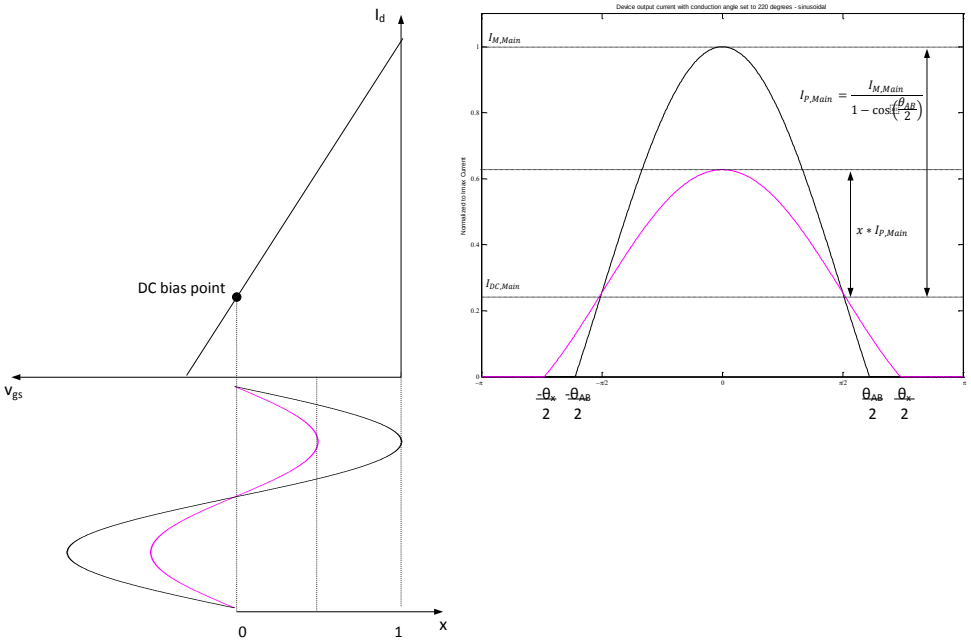

Figure 2-11: Main amplifier output current at full power and back-off (expended from [3])

$$i_d = \begin{cases} I_{DC,Main} + I_{P,Main} * \cos(\theta) & for \quad -\frac{\theta_{AB}}{2} \leq \theta \leq \frac{\theta_{AB}}{2} \\ 0 & otherwise \end{cases} \tag{2.18}$$

Using zero crossings of Figure 2-11 the value of the conduction angle can be determined with equation (2.20)

$$I_{DC,Main} + I_{P,Main} * \cos\left(\frac{\theta_{AB}}{2}\right) = 0 \tag{2.19}$$

or

$$cos\left(\frac{\theta_{AB}}{2}\right) = -\frac{I_{DC,Main}}{I_{p,Main}} \tag{2.20}$$

Substituting equation (2.20) into equation (2.19)

$$i_d = I_{P,Main} * (\cos(\theta) - \cos\left(\frac{\theta_{AB}}{2}\right) \tag{2.21}$$

but

$$I_{P,Main} = I_{M,Main} - I_{DC,Main} = I_{M,Main} + I_{P,Main} * \cos\left(\frac{\theta_{AB}}{2}\right) \tag{2.22}$$

which results in

$$I_{P,Main} = \frac{I_{M,Main}}{1 - \cos\left(\frac{\theta_{AB}}{2}\right)} \tag{2.23}$$

and thus the overall Main amplifier drain current of

$$i_d = \begin{cases} \frac{I_{M,Main}}{1 - \cos\left(\frac{\theta_{AB}}{2}\right)} * (\cos(\theta) - \cos\left(\frac{\theta_{AB}}{2}\right) \; for \; -\frac{\theta_{AB}}{2} \le \theta \le \frac{\theta_{AB}}{2} \\ 0 \qquad\qquad otherwise \end{cases} \tag{2.24}$$

The above is clearly the description of drain current under full input voltage swing conditions. The above equation has to be modified to account for the actual drive level.

$$i_d = I_{DC,Main} + I_{Px,Main} * \cos(\theta) \quad for \; -\frac{\theta_x}{2} \le \theta \le \frac{\theta_x}{2} \tag{2.25}$$

Using zero crossings again

$$I_{DC,Main} + I_{Px,Main} * \cos\left(\frac{\theta_x}{2}\right) = 0 \tag{2.26}$$

or

$$cos\left(\frac{\theta_x}{2}\right) = -\frac{I_{DC,Main}}{I_{Px,Main}} \tag{2.27}$$

Substituting equation (2.27) into (2.25)

$$i_d = I_{Px,Main} * (\cos(\theta) - \cos\left(\frac{\theta_x}{2}\right) \tag{2.28}$$

but

$$I_{Px,Main} = x * I_{P,Main} \tag{2.29}$$

which results in

$$I_{Px,Main} = \frac{x * I_{M,Main}}{1 - \cos\left(\frac{\theta_{AB}}{2}\right)} \tag{2.30}$$

and thus the overall drain current which is written as a function of drive level and instantaneous conduction angle θ_x

$$i_d = \frac{x * I_{M,Main}}{1 - \cos\left(\frac{\theta_{AB}}{2}\right)} * (\cos(\theta) - \cos\left(\frac{\theta_x}{2}\right) for \quad -\frac{\theta_x}{2} \leq \theta \leq \frac{\theta_x}{2} \tag{2.31}$$

Since

$$cos\left(\frac{\theta_x}{2}\right) = -\frac{I_{DC,Main}}{I_{Px,Main}} = -\frac{I_{DC,Main}}{x * I_{P,Main}} \tag{2.32}$$

and

$$cos\left(\frac{\theta_{AB}}{2}\right) = -\frac{I_{DC,Main}}{I_{p,Main}} \tag{2.33}$$

then

$$cos\left(\frac{\theta_{AB}}{2}\right) = x * cos\left(\frac{\theta_x}{2}\right) \tag{2.34}$$

and therefore

$$i_d = \begin{cases} \dfrac{I_{M,Main}}{1 - \cos\left(\frac{\theta_{AB}}{2}\right)} * \left(x * \cos(\theta) - \cos\left(\frac{\theta_{AB}}{2}\right)\right) & for \ -\frac{\theta_x}{2} \leq \theta \leq \frac{\theta_x}{2} \\ 0 & otherwise \end{cases} \tag{2.35}$$

It should be noted however that the above expression is valid only when θ_x actually exists which is when

$$0 = \frac{I_{M,Main}}{1 - \cos\left(\frac{\theta_{AB}}{2}\right)} * \left(x_A * \cos(\pi) - \cos\left(\frac{\theta_{AB}}{2}\right)\right)$$
$$x_A \geq -\cos\left(\frac{\theta_{AB}}{2}\right) \tag{2.36}$$

If the input drive parameter x is below the x_A value then the output current becomes a pure sinusoid as shown in Figure 2-12.

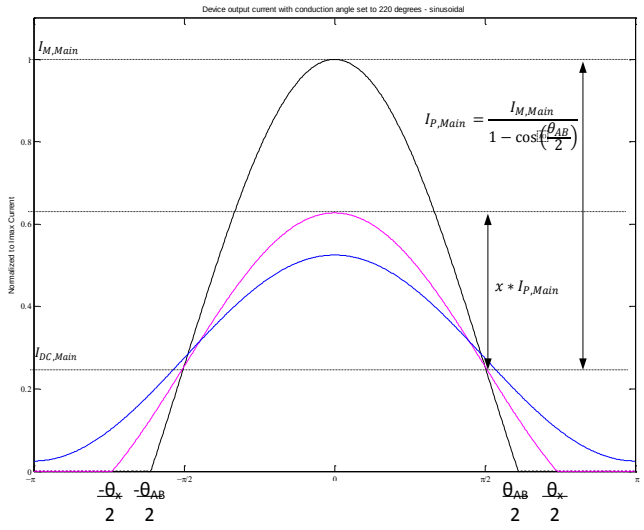

Figure 2-12: Output current as a function of drive parameter x (expended from [3])

2.2.3.2 Auxiliary amplifier

With the definition of a 'virtual negative bias' similar analysis can be performed for the Auxiliary amplifier. [3]

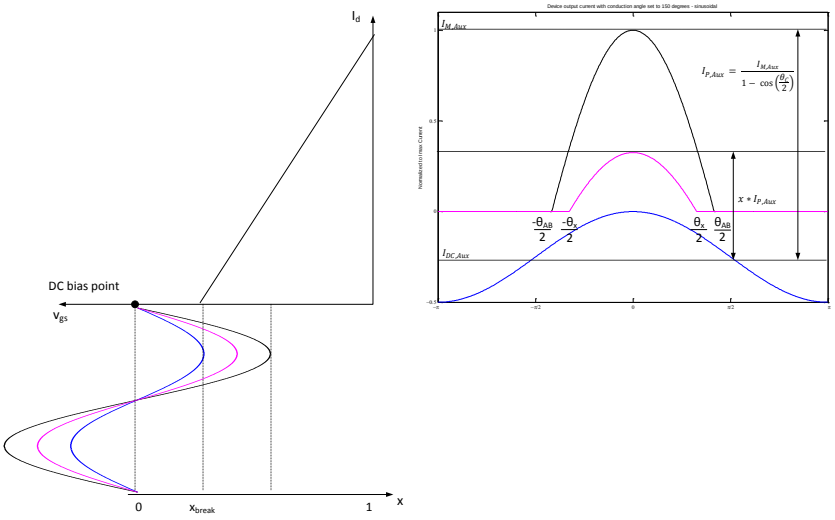

Figure 2-13: Auxiliary amplifier output current waveforms (expended from [3])

$$i_{d,Aux} = \begin{cases} \dfrac{I_{M,Aux}}{1 - \cos\left(\frac{\theta_C}{2}\right)} * \left(x * \cos(\theta) - \cos\left(\frac{\theta_C}{2}\right)\right) for \ -\dfrac{\theta_x}{2} \leq \theta \leq \dfrac{\theta_x}{2} \\ 0 \qquad\qquad otherwise \end{cases} \tag{2.37}$$

and x $\geq x_{break}$

2.2.3.3 Fourier components

Having obtained the required current equations the individual current contributors for dc, fundamental and harmonics can now be obtained as in reference [3] for both the Main and Auxiliary amplifiers.

Class AB

$$I_o(x) = \begin{cases} I_{DC,Main} & if\ x < x_A \\ \dfrac{x * I_{M,Main}}{2\pi} * \dfrac{2 * sin\left(\frac{\theta_x}{2}\right) - cos\left(\frac{\theta_x}{2}\right) * \theta_x}{1 - cos\left(\frac{\theta_{AB}}{2}\right)} & otherwise \end{cases} \tag{2.38}$$

$$I_1(x) = \frac{x * I_{M,Main}}{2\pi} * \frac{\theta_x - sin(\theta_x)}{1 - cos\left(\frac{\theta_{AB}}{2}\right)} \qquad if\ x < x_A\ then\ \theta_x = 2\pi \tag{2.39}$$

$$I_n(x) = \begin{cases} 0 & if\ x < x_A \\ \dfrac{2 * x * I_{M,Main}}{\pi(n^2-1)n} * \dfrac{sin\left(\frac{n\theta_x}{2}\right) * cos\left(\frac{\theta_x}{2}\right) - n * cos\left(\frac{n\theta_x}{2}\right) * sin\left(\frac{\theta_x}{2}\right)}{1 - cos\left(\frac{\theta_{AB}}{2}\right)} & for\ n > 1 \end{cases} \quad (2.40)$$

Class C

$$I_o(x) = \begin{cases} 0 & if\ x < x_{break} \\ \dfrac{x * I_{M,Aux}}{2\pi} * \dfrac{2 * sin\left(\frac{\theta_{x,Aux}}{2}\right) - cos\left(\frac{\theta_{x,Aux}}{2}\right) * \theta_{x,Aux}}{1 - cos\left(\frac{\theta_C}{2}\right)} & otherwise \end{cases} \quad (2.41)$$

$$I_1(x) = \begin{cases} 0 & if\ x < x_{break} \\ \dfrac{x * I_{M,Aux}}{2\pi} * \dfrac{\theta_{x,Aux} - sin(\theta_{x,Aux})}{1 - cos\left(\frac{\theta_C}{2}\right)} \end{cases} \quad (2.42)$$

$$I_n(x) = \begin{cases} 0 & if\ x < x_{break} \\ \dfrac{2 * x * I_{M,Aux}}{\pi(n^2-1)n} * \dfrac{sin\left(\frac{n\theta_{x,Aux}}{2}\right) * cos\left(\frac{\theta_{x,Aux}}{2}\right) - n * cos\left(\frac{n\theta_{x,Aux}}{2}\right) * sin\left(\frac{\theta_{x,Aux}}{2}\right)}{1 - cos\left(\frac{\theta_C}{2}\right)} & for\ \mathrm{n} > 1 \end{cases} \quad (2.43)$$

2.2.4 Detailed analysis of the Doherty power amplifier

2.2.4.1 Low power region

The low power region analysis is rather straight forward. The Doherty amplifier behaves as a classical Class AB power amplifier with a quarter-wavelength transmission line between the load at the output of the current source.

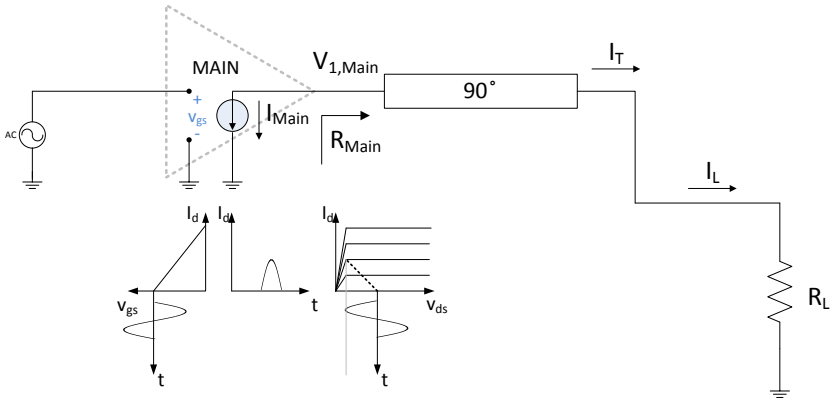

Figure 2-14: Doherty in low power region [3]

To maximize efficiency in this region the voltage at the Main amplifier has to swing up to its maximum of $V_{DD} - V_k$ when the current reaches a level of, $I_{critical}$ related to the desired back-off. For that to happen the impedance seen by the Main amplifier has to be

$$R_{Main}(x_{break}) = \frac{V_{1,Main}}{I_{1,Main}} = \frac{V_{DD} - V_k}{I_{1,Main}(\theta_{x,break})} = \frac{Z_o^2}{R_L} \tag{2.44}$$

where the fundamental component of the current can be found using Equation (2.39).

The requirement for this section is to find the optimum impedance such that maximum voltage swing can be achieved at the required back-off. Assuming that the voltage swing stays the same the output power at back-off can be related to the maximum output power of the Main amplifier using equations found in [3] and listed for reference below.

$$\alpha = \frac{P_{out,Main,break}}{P_{out,Main,Max}} = \frac{I_{1,Main}(\theta_{x,break})}{I_{1,Main}(\theta_{AB})} \tag{2.45}$$

$$I_{1,Main}(\theta_{x,break}) = \alpha * I_{1,Main}(\theta_{AB}) \tag{2.46}$$

which with proper substitutions for Class AB behavior becomes

$$I_{1,Main}(\theta_{x,break}) = \frac{\alpha * I_{M,Main}}{2\pi} * \frac{\theta_{AB} - sin(\theta_{AB})}{1 - cos\left(\frac{\theta_{AB}}{2}\right)} \tag{2.47}$$

$$R_{Main}(x_{break}) = \frac{V_{DD} - V_k}{\frac{\alpha * I_{M,Main}}{2\pi} * \frac{\theta_{AB} - sin(\theta_{AB})}{1 - cos\left(\frac{\theta_{AB}}{2}\right)}} = \frac{2 * \pi}{\alpha} * \frac{V_{DD} - V_k}{I_{M,Main}} * \frac{1 - cos\left(\frac{\theta_{AB}}{2}\right)}{\theta_{AB} - sin(\theta_{AB})} \quad (2.48)$$

Having defined both the current and the impedance in this region one can obtain the voltage across the output current source

$$V_{1,Main}(x) = R_{Main}(x) * I_{1,Main}(x) = \frac{x * (V_{DD} - V_k)}{\alpha} * \frac{\theta_x - sin(\theta_x)}{\theta_{AB} - sin(\theta_{AB})} \quad (2.49)$$

Going back to Equation (2.45) it is important to note that due to Class AB implementation the input and output back-off will not be the same which is unlike in the classical class B Doherty power amplifier.

$$\frac{x * I_{M,Main}}{2\pi} * \frac{\theta_x - sin\left(\frac{\theta_x}{2}\right)}{1 - cos\left(\frac{\theta_{AB}}{2}\right)} = \frac{1 * \alpha * I_{M,Main}}{2\pi} * \frac{\theta_{AB} - sin(\theta_{AB})}{1 - cos\left(\frac{\theta_{AB}}{2}\right)} \quad (2.50)$$

$$x_{break} * [\theta_x - sin(\theta_x)] = \alpha * [\theta_{AB} - sin(\theta_{AB})]$$

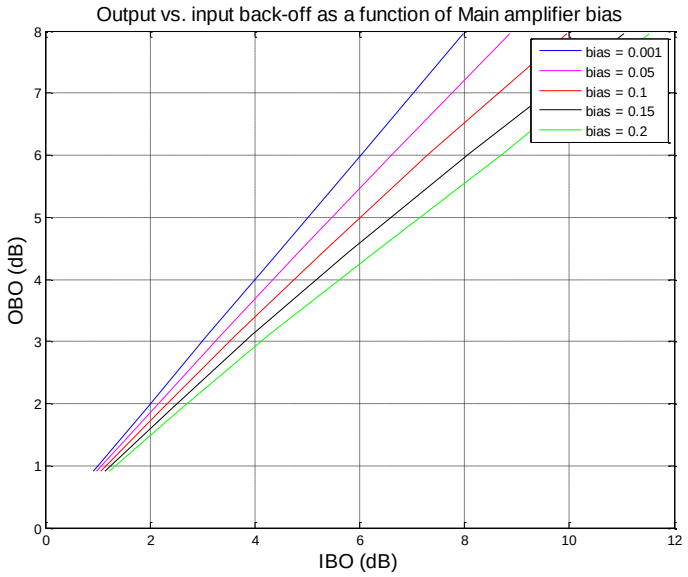

Figure 2-15: Input back-off vs. output back-off for Main amplifier [3]

The above figure illustrates the differences between class B and class AB as a function of bias. The deviation from classical is already observed for bias curve as low as 5%. [3] Thus if biased in class AB x_{break} will not be expected to be at the half mark of the input voltage for a 6 dB back-off.

Having the voltage and current response defined one can now calculate the output and dc powers which can be used to evaluate the efficiency. As per reference [3]

$$P_{out}(x) = \frac{V_{1,Main}(x)}{\sqrt{2}} * \frac{I_{1,Main}(x)}{\sqrt{2}}$$

$$= \frac{x * (V_{DD} - V_k)}{2\alpha} * \frac{\theta_{x,Main} - sin\left(\frac{\theta_{x,Main}}{2}\right)}{\theta_{AB} - sin\left(\frac{\theta_{AB}}{2}\right)} * \frac{x * I_{M,Main}}{2\pi} * \frac{\theta_{x,Main} - sin(\theta_{x,Main})}{1 - cos\left(\frac{\theta_{AB}}{2}\right)} \quad (2.51)$$

$$= \frac{x^2 * I_{M,Main} * (V_{DD} - V_k)}{4 * \pi * \alpha} * \frac{\left(\theta_{x,Main} - sin(\theta_{x,Main})\right)^2}{(\theta_{AB} - sin(\theta_{AB})) * \left(1 - cos\left(\frac{\theta_{AB}}{2}\right)\right)}$$

$$P_{DC}(x) = \frac{x * V_{DD} * I_{M,Main}}{2\pi} * \frac{2 * sin\left(\frac{\theta_{x,Main}}{2}\right) - cos\left(\frac{\theta_{x,Main}}{2}\right) * \theta_{x,Main}}{1 - cos\left(\frac{\theta_{AB}}{2}\right)} \quad (2.52)$$

$$\eta(x) = \frac{P_o(x)}{P_{DC}(x)} \quad (2.53)$$

2.2.4.2 Doherty power region

This region is defined from the break point at back-off until the Main amplifier reaches its maximum power, in case of symmetrical devices the maximum power will not be the device maximum power. In this region although the current of the Main amplifier will be controlled by the input signal x the voltage will remain unchanged due to the load modulation. The current source will behave like a voltage source with $V_{1,Main}$ set to V_{DD}-V_k.

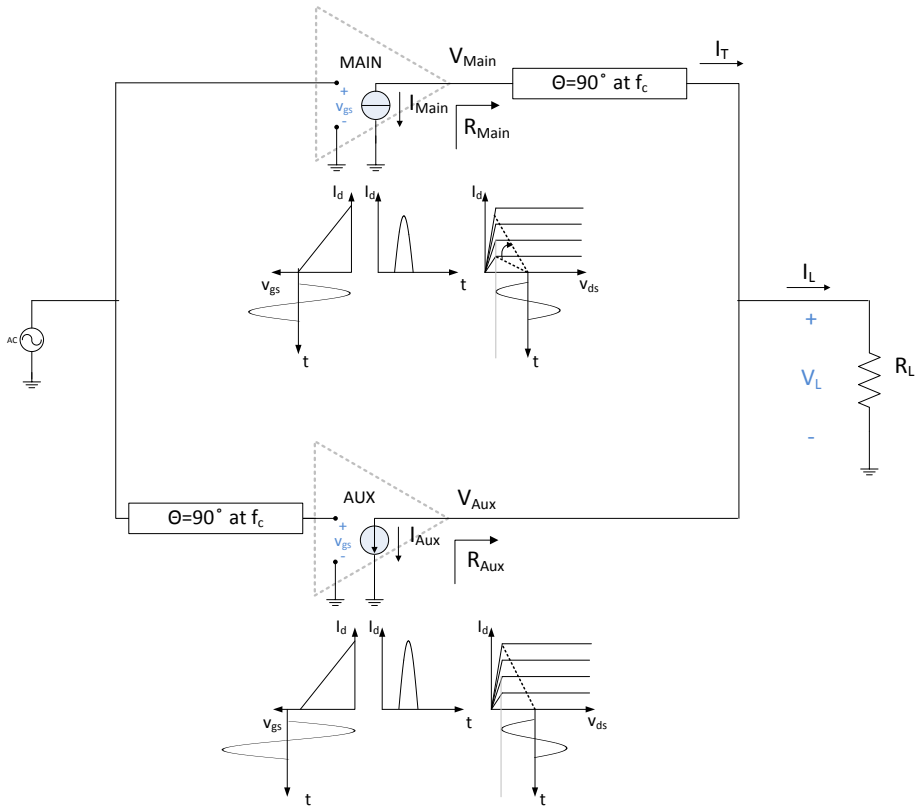

Figure 2-16: Doherty power amplifier at full power [3]

To investigate the behavior of the Doherty power amplifier when both transistors are on Equations (2.13), (2.14) and (2.15) have to be re-visited as in reference [3].

If a lossless quarter-wavelength line is used then it can be seen that

$$V_{1,Main} * I_{1,Main} = V_L * I_T \tag{2.54}$$

If at full power the Doherty power amplifier is required to provide the $I_{1,Main}(\theta_{AB})$ current then

$$I_{T|x=1} = I_{1,Main}(\theta_{AB}) \tag{2.55}$$

which with Equation (2.15) suggests that at back-off the upper branch current must also be $I_{1,Main}(\theta_{AB})$ thus fixing the transformer current over the entire Doherty range.

One can also now find the voltage across the load at the break point using (2.45) and (2.54)

$$V_L(x_{break}) = \frac{V_{1,Main} * I_{1,Main}(x_{break})}{I_{1,Main}(\theta_{AB})} = \alpha * V_{1,Main} = \alpha * (V_{DD} - V_k) \tag{2.56}$$

which can be used with Equation (2.44) to define the characteristic impedance of the quarter-wavelength transmission line given that

$$R_L(x_{break}) = \frac{\alpha * (V_{DD} - V_k)}{I_{1,Main}(\theta_{AB})} \tag{2.57}$$

and

$$R_{Main}(x_{break}) = \frac{V_{DD} - V_k}{I_{1,Main}(\theta_{x,break})} = \frac{V_{DD} - V_k}{\alpha * I_{1,Main}(\theta_{AB})} \tag{2.58}$$

$$Z_o = \frac{V_{DD} - V_k}{I_{1,Main}(\theta_{AB})} \tag{2.59}$$

The final step that needs to be solved in the Doherty amplifier design is the determination of the relationship between the Main and Auxiliary amplifier max current values. Given identical transistors it has been shown in Figure 2-3 that the fundamental current in Class AB will never be the same as that in Class C thus either the Main Amplifier has to be operated at a lower maximum point or the Auxiliary transistor has to be properly sized.

When both transistors have achieved their respective maximum currents of $I_{M,Main}$ and $I_{M,Aux}$ then at the output node the following will be observed

$$\begin{aligned} V_{L|x=1} &= R_L * [I_{1,T} + I_{1,Aux}(\theta_C)] = R_L * [I_{1,Main}(\theta_{AB}) + I_{1,Aux}(\theta_C)] \\ &= R_L * I_{1,Main}(\theta_{AB}) * \left[1 + \frac{I_{1,Aux}(\theta_C)}{I_{1,Main}(\theta_{AB})}\right] \\ &= \alpha * [V_{DD} - V_k] * \left[1 + \frac{I_{1,Aux}(\theta_C)}{I_{1,Main}(\theta_{AB})}\right] \end{aligned} \tag{2.60}$$

and since $V_{L|x=1} = V_{DD} - V_k$ then

$$1 = \alpha * \left[1 + \frac{I_{1,Aux}(\theta_C)}{I_{1,Main}(\theta_{AB})}\right] \tag{2.61}$$

resulting in

$$I_{M,Aux} = I_{M,Main} * \frac{1-\alpha}{\alpha} * \frac{1-cos\left(\frac{\theta_C}{2}\right)}{\theta_C - \sin(\theta_C)} * \frac{\theta_{AB} - \sin(\theta_{AB})}{1-cos\left(\frac{\theta_{AB}}{2}\right)} \quad (2.62)$$

Going back to (2.13) and (2.14)

$$Z_T = Z\frac{I_T + I_{Aux}}{I_T} = Z\left(1 + \frac{I_{Aux}}{I_{1,Main}(\theta_{AB})}\right) \quad x \in [0, x_{break}] \quad (2.63)$$

$$Z_{Aux} = Z\frac{I_T + I_{Aux}}{I_{Aux}} = Z\left(1 + \frac{I_{1,Main}(\theta_{AB})}{I_{Aux}}\right) \quad x \in [0, x_{break}] \quad (2.64)$$

2.2.5 Detailed calculation procedure

Based on the above theory a procedure similar to that applied in [3] will be used to find the starting parameter values for the Doherty power amplifier design:

Step 1: Select the device and determine the I-V characteristics

Set the maximum device current to $I_{M,Aux}$

Step 2: Given the Class AB bias ratio evaluate the conduction angle when in full power and set to DC Main device current

$$cos\left(\frac{\theta_{AB}}{2}\right) = -\frac{I_{DC,Main}}{I_{M,Main} - I_{DC,Main}} = -\frac{\frac{I_{DC,Main}}{I_{M,Main}}}{\left(1 - \frac{I_{DC,Main}}{I_{M,Main}}\right)} = -\frac{\xi}{1-\xi} \quad (2.65)$$

$where\ \xi\ is\ the\ Class\ AB\ bias\ ratio$

$$\xi = \frac{I_{DC,Main}}{I_{M,Main}}$$

Step 3: For a given output back-off point find input back off

$$\alpha = \frac{P_{out,Main,break}}{P_{out,Main,MAx}} = \frac{I_{1,Main}(\theta_{x,break})}{I_{1,Main}(\theta_{AB})} = 10^{\frac{-OBO}{20}} \quad (2.66)$$

Step 4: Based on given bias and thus Main device conduction angle as well as output-back-off determine the input back-off point using equation (2.50) and a numerical solver

Step 5: Determine the auxiliary power amplifier conduction angle using Equation (2.37)

$$i_{d,Aux} = \frac{I_{M,Aux}}{1 - \cos\left(\frac{\theta_C}{2}\right)} * \left(x_{break} * \cos(0) - \cos\left(\frac{\theta_C}{2}\right)\right) = 0$$

$$x_{break} = \cos\left(\frac{\theta_C}{2}\right) \tag{2.67}$$

$$\theta_C = 2 * \cos(x_{break})$$

Step 6: Determine the maximum Main device current using Equation (2.62) and dc current using

$$I_{DC,Main} = \xi * I_{M,Main} \tag{2.68}$$

Step 7: Find the Main device gate voltage

$$V_{GG,Main} = (V_{bi} - V_p) * \xi * \frac{I_{M,Main}}{I_M} + V_p \tag{2.69}$$

Step 8: Find bias current and voltage for the Auxiliary device using

$$I_{DC,Aux} = -\frac{cos\left(\frac{\theta_C}{2}\right)}{1 - cos\left(\frac{\theta_C}{2}\right)} * I_{M,Aux} \tag{2.70}$$

$$V_{GG,Aux} = (V_{bi} - V_p) * \frac{I_{DC,AUx}}{I_M} + V_p \tag{2.71}$$

Step 9: Evaluate load resistance and characteristic impedance of quarter-wave transmission line using Equations (2.57) and (2.59)

Chapter 3 Doherty power amplifier bandwidth analysis

3.1 Introduction

Although the DPA does solve the problem of efficiency at back-off it does so over a very narrow bandwidth. A well-known fact of the Doherty power amplifier is its inability to provide high efficiency across a wide bandwidth. While this was not a concern several years ago with the recent changes in wireless standards and the evolution towards wideband transmission it has been found that the Doherty is no longer able to provide the required performance. In fact in typical designs the bandwidth is usually less than 10%. [5]

To improve the bandwidth performance several publications have focused on extending the bandwidth of the output and input matching networks. In [6] Sun has used the scattering matrix to optimize the output efficiency and power at saturation. Unlike most other publications he has considered the negative effects that parasitics as well as biasing circuits will have on the overall design and has included it in his analysis. He was able to achieve efficiency greater that 40% in the frequency range of 2.2-2.9 GHz or over a fractional bandwidth of 27%. In [7] Giofre et al. have proposed the use of three quarter-wave lines as the combining network of the DPA each with different characteristic impedance. The output power targeted was 40 dBm over a 1.05 – 2.55 GHz frequency range or 83% fractional bandwidth. The achieved efficiency at back-off was in the 35-57% range. The performance was actually impressive however the lower end of the efficiency curve extends over a 400 MHz range in the middle of the targeted frequency range. The design also utilizes high impedance lines which tend to be harder to manufacture. In [8] Bathich and his colleagues have provided a detailed frequency response analysis of the classical DPA. They have shown that the output combining network of the DPA is the main bottleneck to achieving maximum performance. They have used the quarter-wavelength transmission line bandwidth equation to illustrate the dependency of bandwidth on the ratio between Zo and ZL. By increasing the common load impedance they have increased the efficiency at back-off ranging from 41-55% at back-off over 1.7-2.6 GHz frequency range. In [9] Rubio explores wideband compensator networks and second harmonic tuning to achieve high efficiency, 38% and greater, in the 3-3.6 GHz frequency range

The use of offset lines has also shown to benefit the bandwidth of the DPA. In [10] Shao replaces the two quarter wavelength line in the traditional DPA with offset lines and matched the PAs to 70 ohms.

He was unfortunately only able to achieve power added efficiency greater than 30% at back-off over a fractional bandwidth of 40%.

The final approach of enhancing efficiency at back–off looks at the bias voltages along with wideband matching. In [11] Wu used symmetrical devices with asymmetrical bias and modified characteristic impedance to enhance the efficiency in the 0.7-1 GHz range. In his work he was able to achieve 35.3% fractional bandwidth at efficiency of greater than 50% at 6 dB back-off.

A detailed summary of findings is shown in Table 3-1 Literature review summary

Table 3-1 Literature review summary

Author	Year	Approach	BW %	DE %	PAPR	$P_{out\ back\text{-}off}$
Bathich	2011	modified λ/4 offset lines VDD Class C @ 36 V	40.91	41-55	6 dB	38-39 dBm
Sun	2012	real frequency technique considered parasitics etc… optimized at back-off or peak	26.92	38-48	6 dB	36 dBm
Bathich	2012	harmonic tuning	27.85	50-65	6.2 dB	42.2-43.6 dBm
Rubio	2012	wideband compensators 2nd harmonic tuning	18.18	38-56	6 dB	37-38 dBm
Wu*	2012	asymmetrical bias Klopfenstein taper matching	35.29	40-70	6 dB	43-45 dBm
Gustafsson	2013	asymmetrical bias Chebyshev transformer matching	46.15	40-60	6 dB	36 dBm
Nghiem	2013	modified λ/4 offset lines	13.95	20-70	10 dB	30.6 dBm
Shao	2014	broadband matching networks offset lines output impedance mismatch eliminates λ/4 line	40	30.3-40.1	6 dB	30-36 dBm
Giofre	2014	novel output combiner	78.95	35-57	6 dB	34-35.9 dBm

3.2 Bandwidth analysis

The first step to solving the problem of average efficiency over wide bandwidth is to understand where the restrictions are coming from. In previous analysis, [5] and [12] , it was shown that at full power the impedance inverting network, IIN, had the same characteristic impedance as the termination. This implies that its impact across the frequency will be far less significant than when the amplifier is in back-off. Thus the analysis in this section will begin with the Doherty amplifier operating in back-off such that only the Main device is contributing to the output power.

Looking at the setup in Figure 3-1 it becomes very obvious that the only frequency dependent component is the quarter-wave line between the device output and the termination. Using the ABCD matrix of the quarter-wave transmission line one can easily verify the original assumption and show the frequency performance of the amplifier and the bandwidth limitations of the inverter.

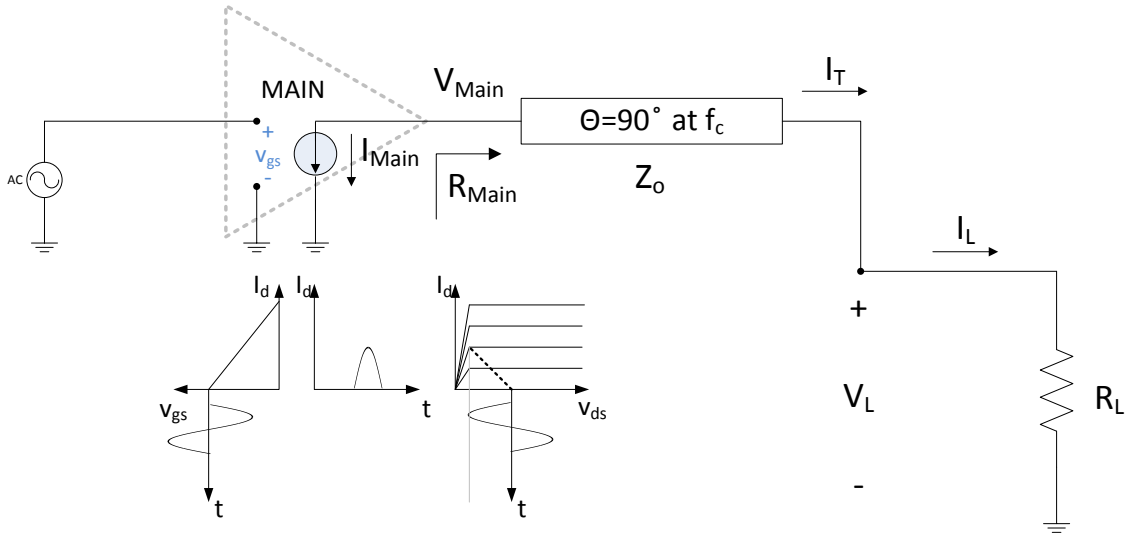

Figure 3-1: Doherty power amplifier in back-off

$$\begin{bmatrix} \boldsymbol{V_{Main}} \\ \boldsymbol{I_{Main}} \end{bmatrix} = \begin{bmatrix} cos\theta & jZ_o sin\theta \\ j\frac{1}{Z_o} sin\theta & cos\theta \end{bmatrix} * \begin{bmatrix} \boldsymbol{V_L} \\ \boldsymbol{I_T} \end{bmatrix} \quad (3.1)$$

$$\text{where } \boldsymbol{V_L} = R_L * \boldsymbol{I_T}$$

Solving the above equation for the voltage seen at the device output clearly demonstrates its dependency on frequency as seen in equation (3.2). It also shows that the voltage is a function of the ratio between the characteristic impedance of the transmission line and the output termination.

$$\boldsymbol{V_{Main}} = \frac{\boldsymbol{I_{Main}} * (R_L cos\theta + j * Z_o sin\theta)}{j * \frac{R_L}{Z_o} sin\theta + cos\theta} \tag{3.2}$$

It is then easily seen that if voltage is a function of frequency then so will be power, efficiency and impedance.

To look at the negative impact of the quarter-wavelength transmission line on bandwidth one can examine the efficiency curve.

$$\eta = \frac{0.5 * Real(\boldsymbol{V_{Main}} * \boldsymbol{I^*_{Main}})}{V_{DC} * I_{DC}} \tag{3.3}$$

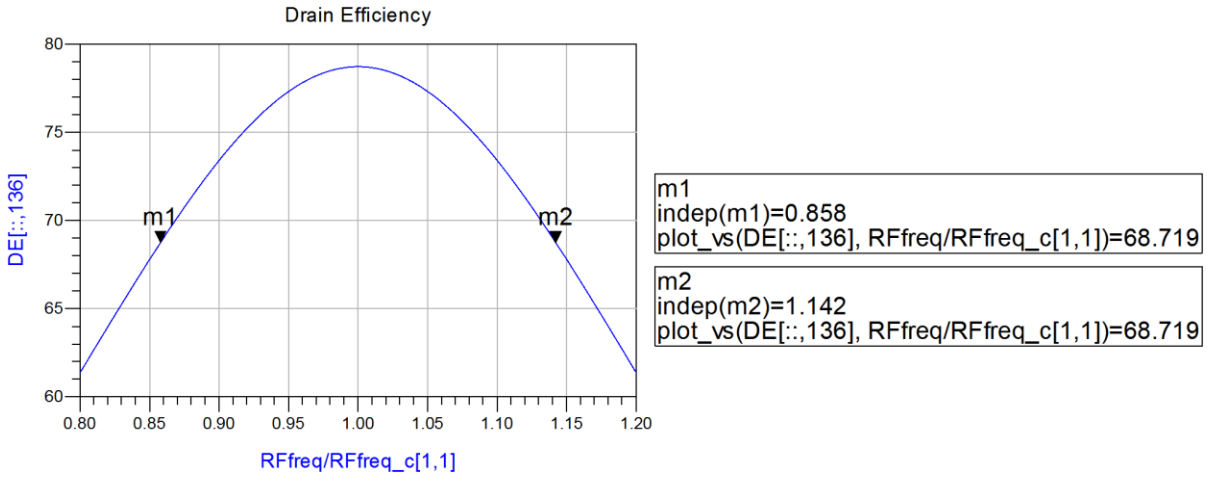

Figure 3-2: Efficiency curve at back-off for ideal Doherty power amplifier

It can be observed that while in back-off there is a significant efficiency degradation due to the inverter. At best the achievable efficiency within 10% of maximum results in 28% fractional bandwidth.

Although the bandwidth restriction dominates in back-off which implies during Main amplifier operation it is important to examine the DPA structure when both the Main and Auxiliary amplifiers are turned on. This is performed to establish the optimal vector relationship between the Main and Auxiliary currents.

Going back to [12] one can expand the previous analysis to include the Auxiliary amplifier.

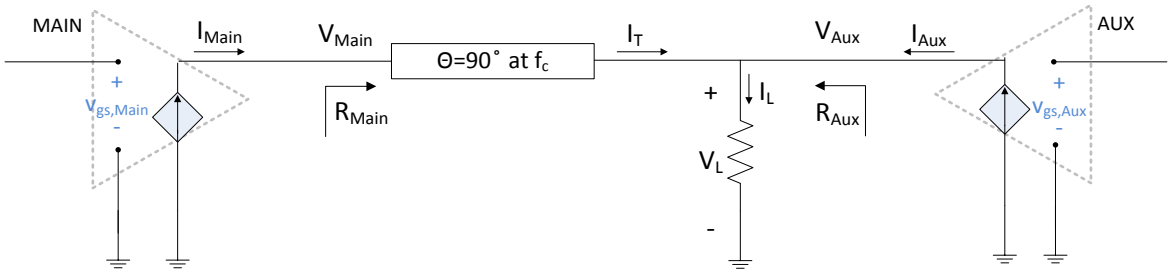

Figure 3-3: Doherty power amplifier

$$\begin{bmatrix} \boldsymbol{V_{Main}} \\ \boldsymbol{I_{Main}} \end{bmatrix} = \begin{bmatrix} cos\theta & jZ_o sin\theta \\ j\frac{1}{Z_o} sin\theta & cos\theta \end{bmatrix} * \begin{bmatrix} \boldsymbol{V_L} \\ \boldsymbol{I_T} \end{bmatrix} \tag{3.4}$$

where $\boldsymbol{V_L} = R_L * (\boldsymbol{I_T} + \boldsymbol{I_{Aux}})$

which leads to

$$\boldsymbol{I_T} = \frac{\boldsymbol{I_{Main}} - j * \boldsymbol{I_{Aux}} * \frac{R_L}{Z_o} sin\theta}{j * \frac{R_L}{Z_o} sin\theta + cos\theta} \tag{3.5}$$

$$\boldsymbol{V_{Main}} = \frac{I_{Main} * (R_L cos\theta + j * Z_o sin\theta) + I_{Aux} R_L (cos\theta_I + j * sin\theta_I)}{j * \frac{R_L}{Z_o} sin\theta + cos\theta} \tag{3.6}$$

where $\angle \boldsymbol{I_{Main}} - \angle \boldsymbol{I_{Aux}} = \theta_I$

3.2.1 Current relationship between main and auxiliary

The first thing that has to get established in equation (3.6) is the relation of the auxiliary current with respect to the main. The usual approach is to either provide a 90 phase shift at the input or one that follows the output combiner as in a quarter wave line.

If $\theta_I = 90°$ Ideal Doherty using Class B for Main and Class C for Auxiliary

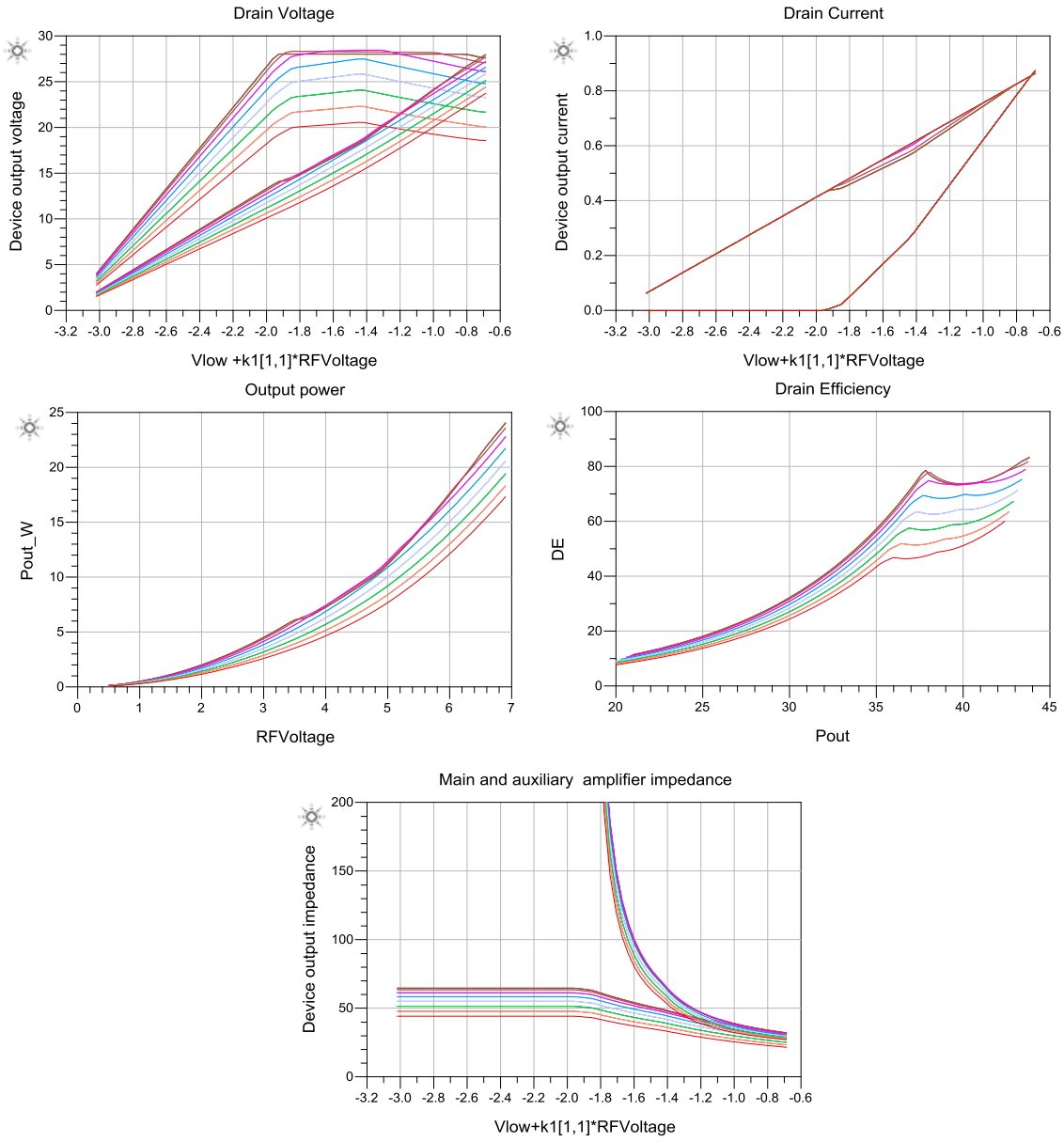

Figure 3-4: Ideal Doherty performance curves with a hybrid 90 degree input splitter

If $\theta_I = \theta$ Ideal Doherty using Class B for Main and Class C for Auxiliary

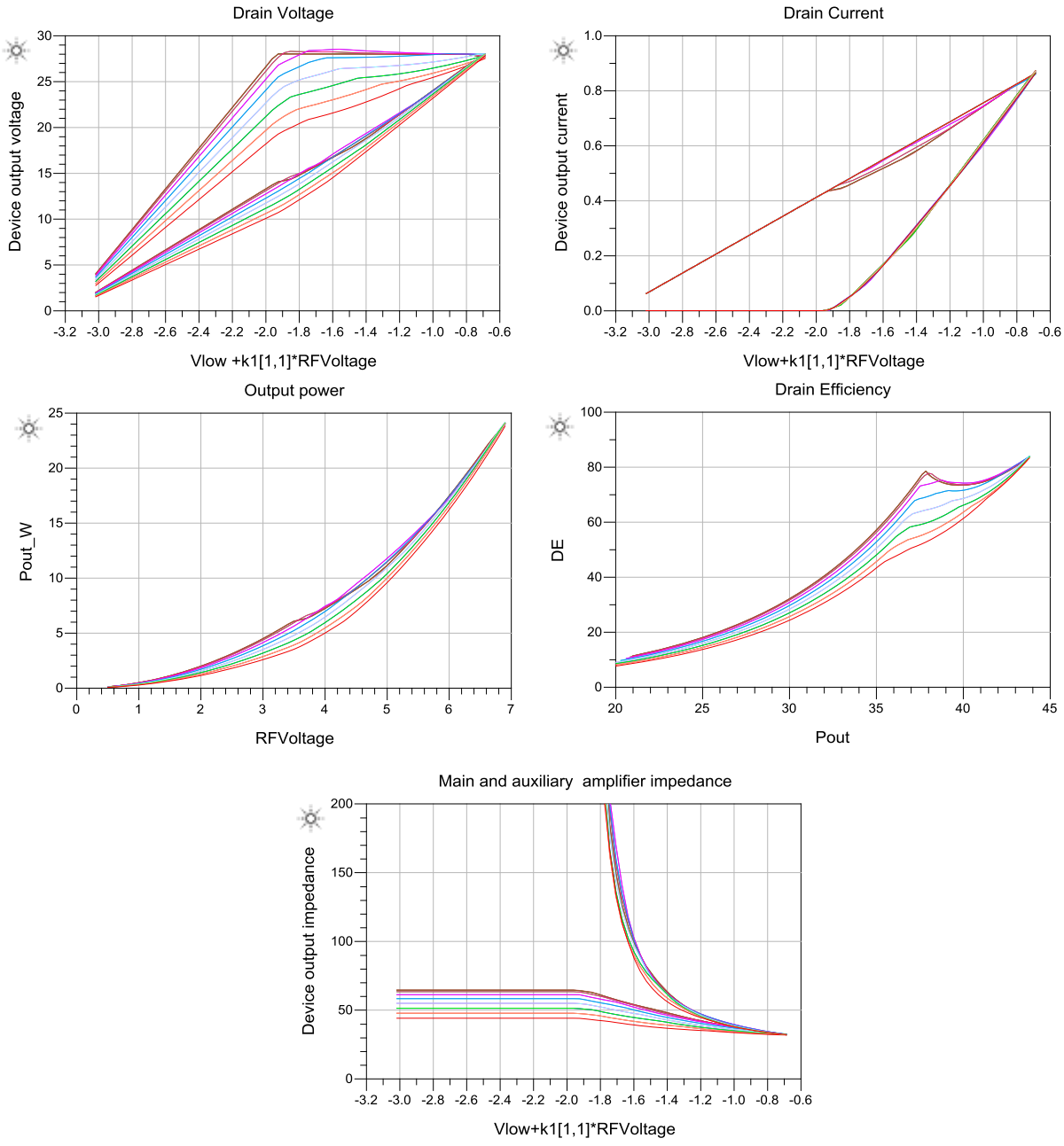

Figure 3-5: Ideal Doherty performance curves with a 90 degree input offset line

Examining Figure 3-4 and Figure 3-5 several points must be mentioned. In either of the cases it can be seen that the voltage seen across the Main amplifier decreases as a function of frequency. This suggest that the amplifier will not see proper load modulation across the frequency band not only at

back-off but also between back-off and full power. It can also be seen that while both choices of current relationship will experience identical degradation at back-off the one that follows the output combiner has actually a better performance at peak power compared to the 90 degree hybrid combiner. This is also illustrated in Figure 3-6.

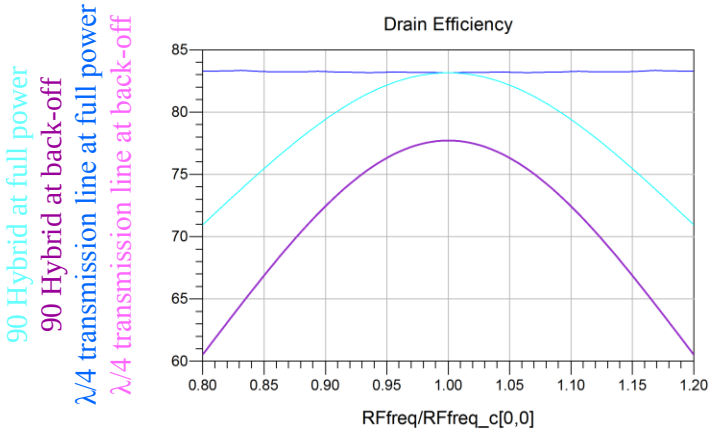

Figure 3-6: Performance with different current phase relationships

3.2.2 Doherty power amplifier with complex terminating impedance

Going back to the analysis it can now be extended to include an arbitrary impedance as the terminating load. It is of course assumed that although I_{Main} can contain several harmonics the short circuit condition will allow only the fundamental component to get through and as such I_{Main} here refers to the linear fundamental current.

The idea of a Doherty power amplifier has always been based on the concept of real terminating impedance. The goal of this thesis is to prove that in fact the design space is far wider than previously anticipated.

Going back to the setup it can be modified such that the terminating impedance contains both real and imaginary parts as shown in Figure 3-7.

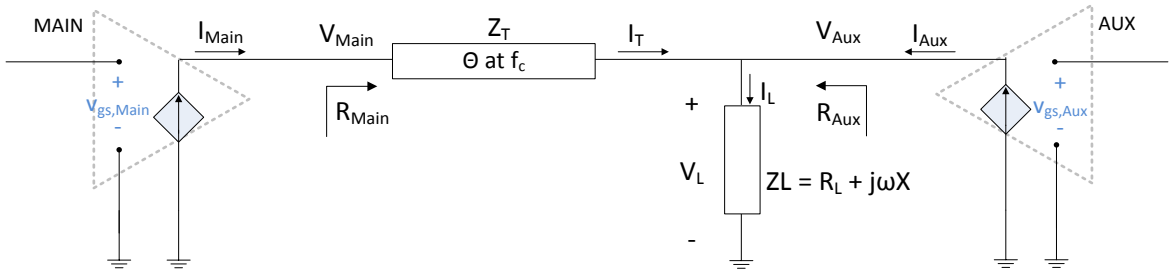

Figure 3-7: Doherty power amplifier with complex terminating impedance

With that in mind a new equation can be developed showing the dependence of Main voltage on the real and imaginary parts of the terminating impedance.

$$Z_L = R_L + jX_L \tag{3.7}$$

Then

$$\boldsymbol{I_T} = \frac{\boldsymbol{I_{Main}} - j * \boldsymbol{I_{Aux}} * \frac{R_L + jX_L}{Z_o} sin\theta}{cos\theta + j * \frac{R_L + jX_L}{Z_o} sin\theta} \tag{3.8}$$

$$\begin{aligned} \boldsymbol{V_{Main}} &= \frac{\boldsymbol{I_{Main}} * \left[R_L + j * \left\{X_L \cos(2\theta) + \left(Z_o - \left(\frac{X_L^2}{Z_o}\right) - \left(\frac{R_L^2}{Z_o}\right)\right) cos\theta\, sin\theta\right\}\right]}{\left(cos\,\theta - \frac{X_L}{Z_o} sin\,\theta\right)^2 + \left(\frac{R_L}{Z_o}\right)^2 sin^2\theta} \\ &+ \frac{\boldsymbol{I_{Aux}} * \left[R_L\, cos\theta + j * \left(X_L \cos(\theta) - \left(\frac{X_L^2}{Z_o} + \frac{R_L^2}{Z_o}\right) \sin\theta\right)\right]}{\left(cos\,\theta - \frac{X_L}{Z_o} sin\,\theta\right)^2 + \left(\frac{R_L}{Z_o}\right)^2 sin^2\theta} \end{aligned} \tag{3.9}$$

3.2.2.1 Analysis in back-off

At back off since only the main amplifier is working the equations simplify to

$$\boldsymbol{V_{Main}} = \frac{\boldsymbol{I_{Main}} * \left[R_L + j * \left\{X_L \cos(2\theta) + \left(Z_o - \left(\frac{X_L^2}{Z_o}\right) - \left(\frac{R_L^2}{Z_o}\right)\right) cos\theta\ sin\theta\right\}\right]}{\left(cos\ \theta - \frac{X_L}{Z_o} sin\ \theta\right)^2 + \left(\frac{R_L}{Z_o}\right)^2 sin^2\theta} \tag{3.10}$$

$$\boldsymbol{Z_{Main}} = \frac{\left[R_L + j * \left\{X_L \cos(2\theta) + \left(Z_o - \left(\frac{X_L^2}{Z_o}\right) - \left(\frac{R_L^2}{Z_o}\right)\right) cos\theta\ sin\theta\right\}\right]}{\left(cos\ \theta - \frac{X_L}{Z_o} sin\ \theta\right)^2 + \left(\frac{R_L}{Z_o}\right)^2 sin^2\theta} \tag{3.11}$$

$$\eta = \frac{0.5 * Real(\boldsymbol{V_{Main}} * \boldsymbol{I_{Main}^*})}{V_{DC} * I_{DC}}$$

$$= \frac{0.5 * \boldsymbol{I_{Main}}^2}{V_{DC} * I_{DC}} * \frac{Z_o^2}{R_L} * \frac{1}{sin^2\theta} * \frac{1}{\left(\frac{Z_o}{R_L}\right)^2 cot^2\theta - 2\frac{X_L Z_o}{R_L^2} cot\theta + \left(\frac{X_L}{R_L}\right)^2 + 1} \tag{3.12}$$

$$P_{out} = 0.5 * Real(\boldsymbol{V_{Main}} * \boldsymbol{I_{Main}^*})$$

$$= 0.5 * \boldsymbol{I_{Main}}^2 * \frac{Z_o^2}{R_L} * \frac{1}{sin^2\theta} * \frac{1}{\left(\frac{Z_o}{R_L}\right)^2 cot^2\theta - 2\frac{X_L Z_o}{R_L^2} cot\theta + \left(\frac{X_L}{R_L}\right)^2 + 1} \tag{3.13}$$

The influence of the real and imaginary parts of the terminating impedance can be quickly investigated by setting up an ideal Doherty test bench where the termination is varied over a fixed region.

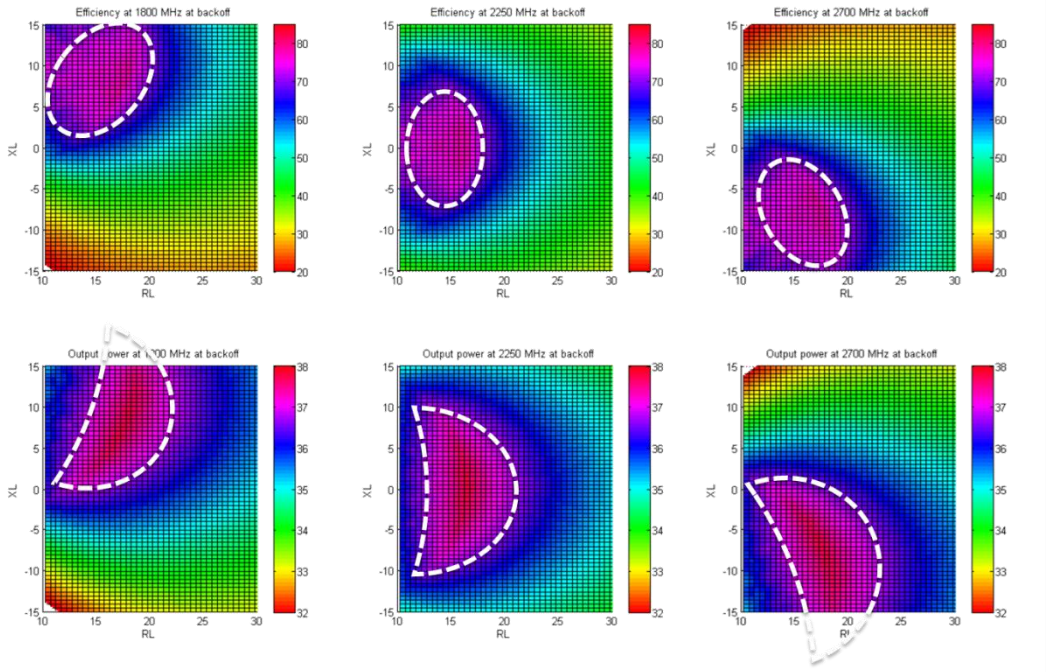

Figure 3-8: Ideal Doherty power amplifier termination sweep results at back-off

The results shown in Figure 3-8 illustrate that in back-off there are distinct regions which will provide the required power and required efficiency. This suggests that the original assumption of real impedance at the common node may not be the optimal one when considering wideband applications. In general the imaginary parts will be positive for frequencies below fc and negative for frequencies above fc.

3.2.2.2 Analysis at full power

A similar analysis can be performed at full power.

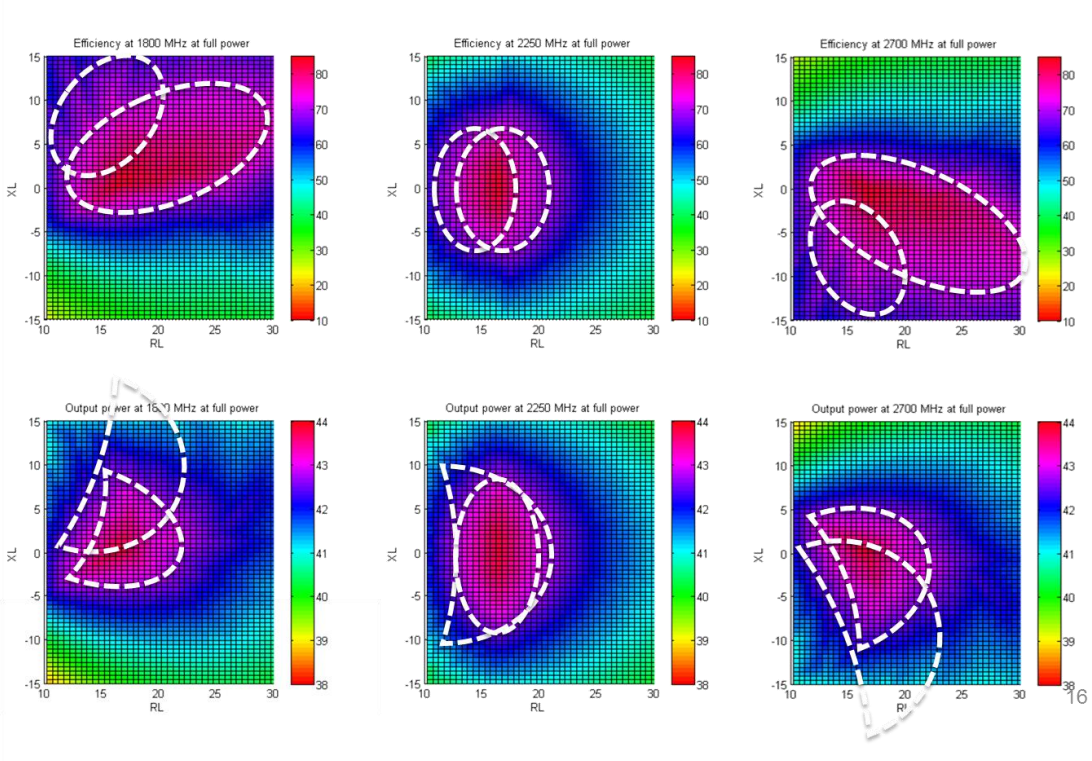

Figure 3-9: Ideal Doherty power amplifier termination sweep results at full power

Looking at Figure 3-8 and Figure 3-9 it becomes obvious that there are regions that overlap for both back-off and full power that produce the optimum performance for both (as shown by the dashed contours). Thus instead of lengthy mathematical derivations a load pull can be performed as long as the regions of best performance are analyzed with respect to back-off and full power at the same time. This means that the optimal impedances must be selected to satisfy the following goals:

a) Back-off power must be within 0.5 dB of 37 dBm
b) Back-off efficiency should be greater than 70%
c) Full power should be within 0.5 dB of 43 dBm
d) Full power efficiency should be greater than 60%

With those goals in mind the optimal impedances were selected from a number of possible solutions and a quick simulation was performed to confirm the findings. The results are shown in Figure 3-10.

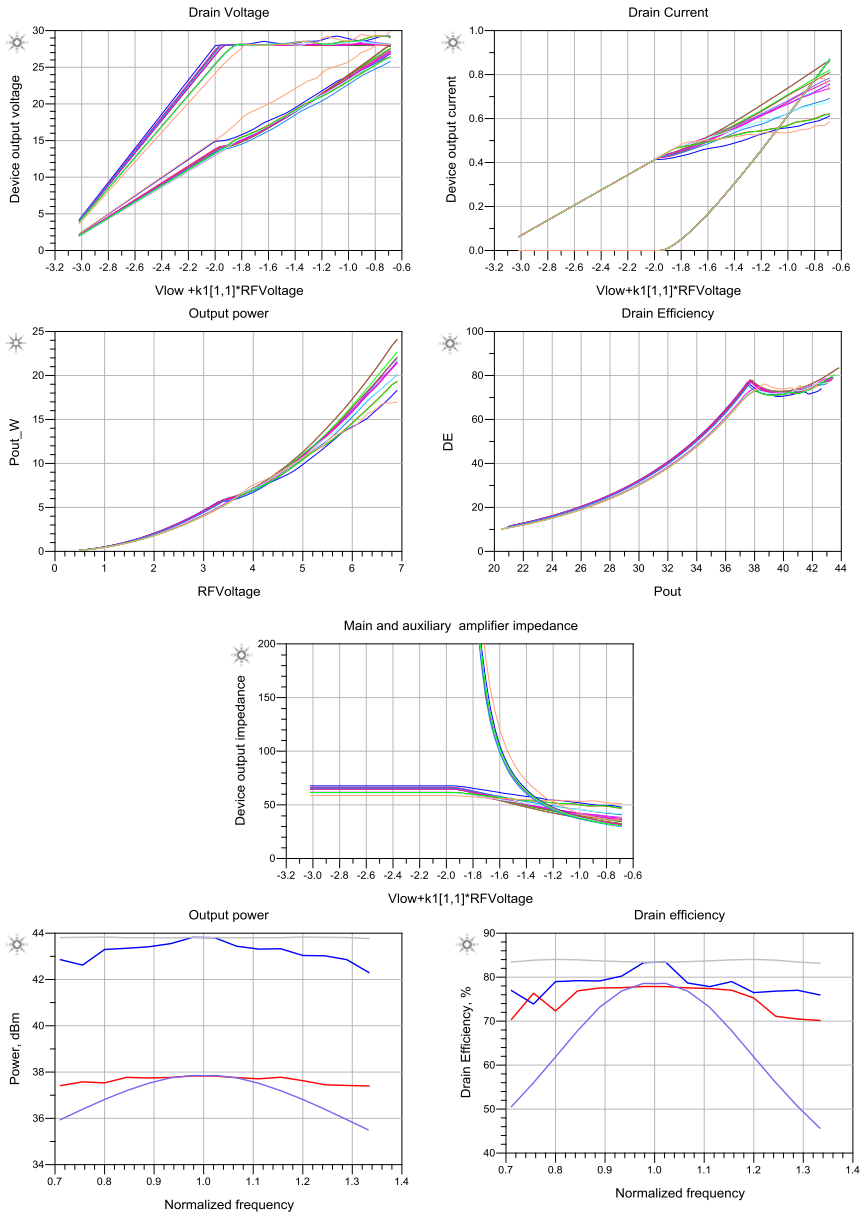

Figure 3-10: Doherty amplifier performance with complex impedance

One can right away note the 20% improvement in back off efficiency at band edges compared to Figure 3-5. (dashed lines in the figure represent ideal Class ABC DPA)

3.3 Output capacitance compensation

As pointed out in [5] most designs have an efficiency of 10% or less and as such current analysis does not provide enough background as to the true frequency limitation of the DPA power amplifier.

Another component that impacts the frequency response is the device output capacitance. If not properly dealt with the output capacitance can significantly impact the overall performance.

If one now assumes that an output capacitor is connected across the current source before the quarter-wave transmission line then the following setup can be obtained:

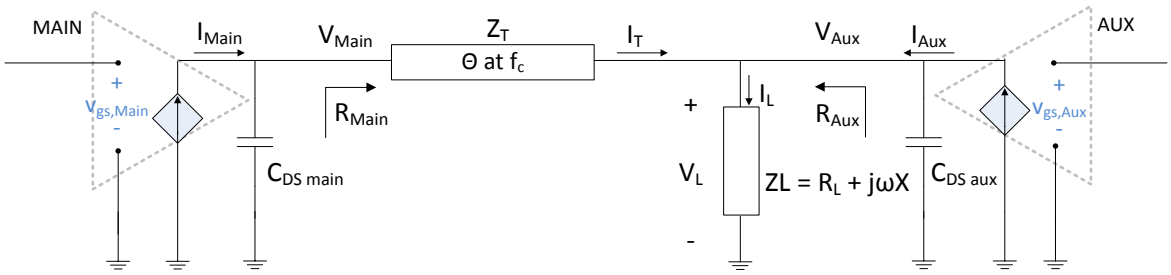

Figure 3-11: Simplified Doherty power amplifier with device capacitance

3.3.1 Capacitance absorption using transmission line

The most common bandwidth friendly way of absorbing the output capacitance of an active device is to use a transmission line. In this case the quarter wavelength line already present in the Doherty setup can be used for that purpose. To establish the necessary changes to the transmission line shown in Figure 3-11 the ABCD matrix has to be used to extract the inductive and capacitive values of the equivalent Pi transmission line model.

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} cos\theta & jZ_o sin\theta \\ j\frac{1}{Z_o} sin\theta & cos\theta \end{bmatrix} = \begin{bmatrix} 1-\omega^2 C_T L_T & j\omega L_T \\ j\omega L_T & 1-\omega^2 C_T L_T \end{bmatrix} \tag{3.14}$$

$$L_T = \frac{Z_o sin\,\theta}{\omega_o}$$

$$C_T = \frac{1-cos\theta}{Z_o sin\theta * \omega_o} = \frac{tan\,\theta}{Z_o \omega_o} \tag{3.15}$$

Once these values have been obtained the model and the transmission line parameters can be adjusted to compensate for the output capacitance of the device.

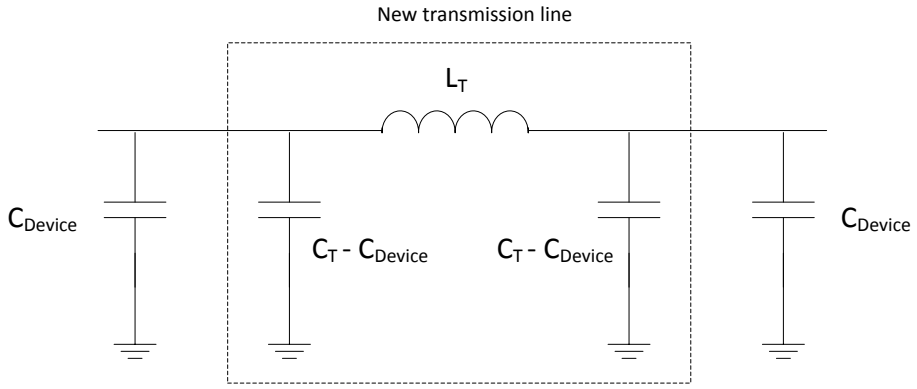

Figure 3-12: Output capacitance compensation network

The new length of the line and the new characteristic impedance can be then set to

$$Z_o' = \frac{1 - cos\theta}{C_T' sin\theta * \omega_o} \tag{3.16}$$

$$\theta' = cos^{-1}(1 - L_T * C_T' * \omega_o^2) \tag{3.17}$$

3.3.2 Regions of high performance

Now that the absorption parameters have been evaluated another load-pull was performed to visualize the impact of the device capacitance on the overall high performance regions. As before it was found that there was enough overlap between the regions that for each frequency point an impedance could be select that satisfied the requirements at both back-off and full power

Chapter 4 Power amplifier design

4.1 Initial DPA design parameters

The preliminary DPA design was performed using the procedure developed in Section 2.2.5 and the summary of the design parameters is shown below.

Table 4-1: Main amplifier design summary

Design parameter Main	Symbol	Value	Unit
Back-off	α	0.5	
Bias ratio	ξ	0.1	
Conduction angle	θ_{AB}	192.76	degrees
Maximum allowed current	$I_{M,Main}$	1.77	A
DC bias current	$I_{DC,Main}$	177	mA
DC gate voltage	$V_{GG,Main}$	-2.942	V
Drain current at back-off	$I_{Critical}$	0.8661	A
Resistance at back-off	$R_{Main}(x=x_{break})$	50.44	Ω
Resistance at saturation	$R_{Main}(x=1)$	25.28	Ω
DC power at back-off	$P_{DC,Main}(x=x_{break})$	8.8245	W
Output power at back-off	$P_{out,Main}(x=x_{break})$	5.2438	W
Efficiency at back-off	$\eta_{Main}(x=x_{break})$	59.42	%
DC power at saturation	$P_{DC,Main}(x=1)$	16.78	W
Fundamental current at saturation	$I_{1Main}(x=1)$	0.9	A
Output power at saturation	$P_{out,Main}(x=1)$	10.46	W
Output power at saturation (dBm)	$P_{out,Main}(x=1)$	40.2	dBm
Efficiency at saturation	$\eta_{Main}(x=1)$	62.35	%
Gain at saturation	$G_{Main}(x=1)$	17.65	dB

Table 4-2: Auxiliary amplifier design summary

Design parameter Aux	Symbol	Value	Unit
Conduction angle	θ_C	128.8	degrees
Maximum allowed current	$I_{M,Aux}$	2.2	A
DC bias current	$I_{DC,Aux}$	-1.67	mA
DC gate voltage	$V_{GG,Aux}$	-5.63	V
Resistance at saturation	$R_{Aux}(x=1)$	25.4	Ω
DC power at saturation	$P_{DC,Aux}(x=1)$	14.37	W
Fundamental current at saturation	$I_{1\_Aux}(x=1)$	0.9	A
Output power at saturation	$P_{out,Aux}(x=1)$	10.41	W
Output power at saturation (dBm)	$P_{out,Aux}(x=1)$	40.17	dBm
Efficiency at saturation	$\eta_{Aux}(x=1)$	72.47	%
Gain at saturation	$G_{Aux}(x=1)$	9.92	dB

Table 4-3: Doherty amplifier design summary

Design parameter DPA	Symbol	Value	Unit
Back-off	α	0.501	
Output Back-off	α	6.00	dB
Load	R_L	12.67	Ω
Output λ/4 impedance	Z_o	25.28	Ω
Power splitter ratio Main	Λ_C	0.855	
Power splitter ratio Aux	Λ_{AB}	0.145	
Output power at back-off	$P_{out,DPA}(x=x_{break})$	5.2438	W
		37.20	dBm
Efficiency at back-off	$\eta_{DPA}(x=x_{break})$	59.42	%
DC power at saturation	$P_{DC,DPA}(x=1)$	31.15	W
Output power at saturation	$P_{out,DPA}(x=1)$	20.87	W
		43.20	dBm
Efficiency at saturation	$\eta_{DPA}(x=1)$	67.00	%
Gain at saturation	$G_{DPA}(x=1)$	12.26	dB
Input break point	x_{break}	0.43	
Input back-off	IBO	7.33	dB

4.2 Doherty power amplifier design using CGH600015D

4.2.1 Device parameter extraction

The ability to monitor the device voltages and currents has brought forth significant improvements in wideband power amplifier designs as was shown by Cripps in his Class J power amplifier development. For this thesis access to internal gate and drain nodes can be used to ensure that the power amplifier is indeed exhibiting the expected behavior. To get access to the gate and drain nodes of the device ColdFET extraction has been performed to identify the values of the parasitics in the die as per reference [13].

4.2.2 Preliminary design

The Doherty power amplifier design consisted of several preliminary steps that were able to confirm the behavior of the amplifier with respect to the theory developed in previous sections. First the parasitics as well as Cds were eliminated from the actual device and harmonic shorts were provided at the internal gate and drain nodes. The results in Figure 4-1were obtained highlighting once again the influence of the quarter-wavelength transmission line and providing a baseline for the bandwidth improvement techniques. As can be seen the drain efficiency, DE, curve at the bottom of the figure follows that obtained in section 3.2 One can also note that although the trend is very similar the actual values are offset by roughly 15-20% due to device knee voltage and Class AB operation of the Main device when compared to ideal Class ABC Doherty power amplifier.

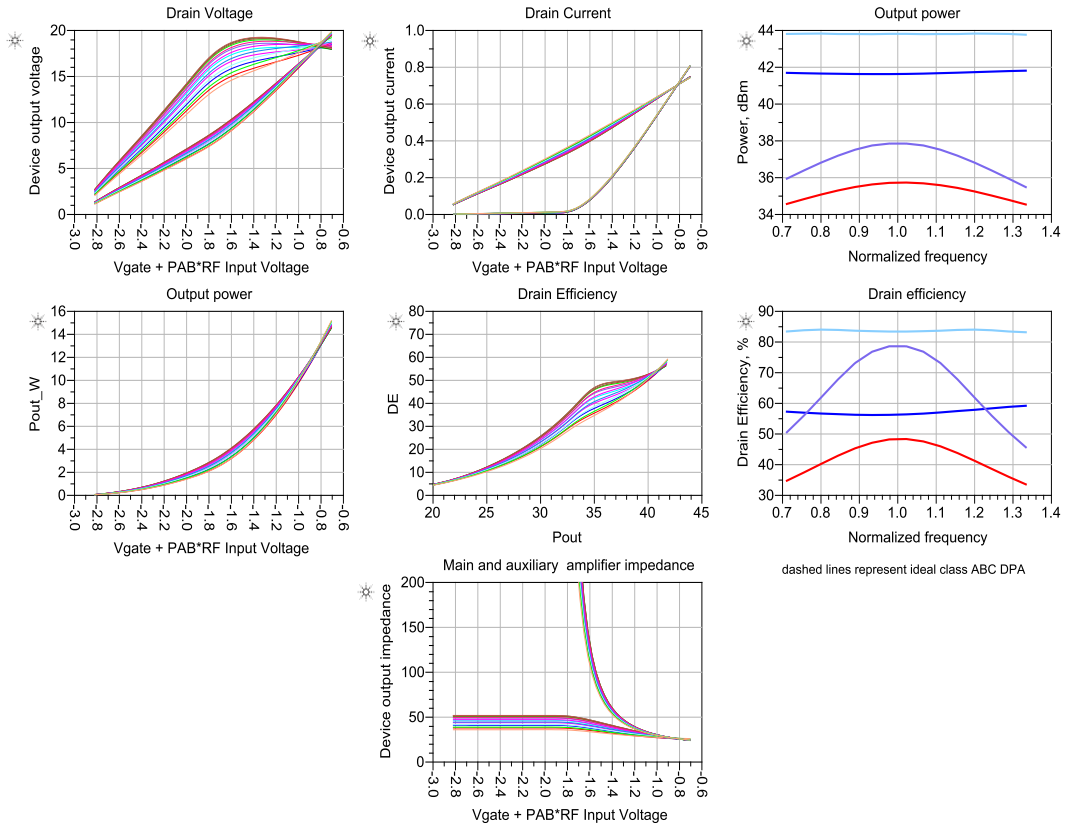

Figure 4-1: Baseline performance of Doherty power amplifier

4.2.3 Optimal terminations

The next step was to add the output capacitance, adjust the quarter-wavelength transmission line accordingly and perform a load-pull at the common node of the DPA simultaneously at back-off and full power and identify the impedance necessary to provide optimal performance not only at both powers but also across the frequency band. An example of the Smith Chart is shown below. The ideal point would be selected in a region where all four contours would overlap as shown in Figure 4-2 and would satisfy the following goals.

a) Back-off power must be within 0.5 dB of 36 dBm
b) Back-off efficiency should be greater than 50%
c) Full power should be within 0.5 dB of 42 dBm
d) Full power efficiency should be greater than 60%

The obtained impedances were then plugged into the common node terminating impedance and the results are shown in Figure 4-3

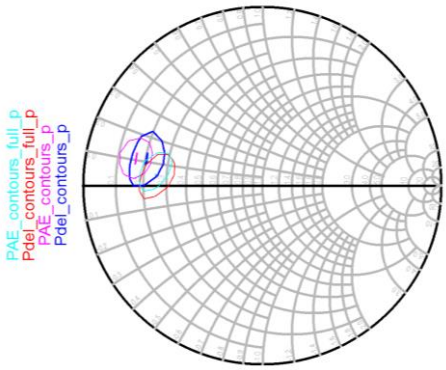

Figure 4-2: Optimum impedance selection example

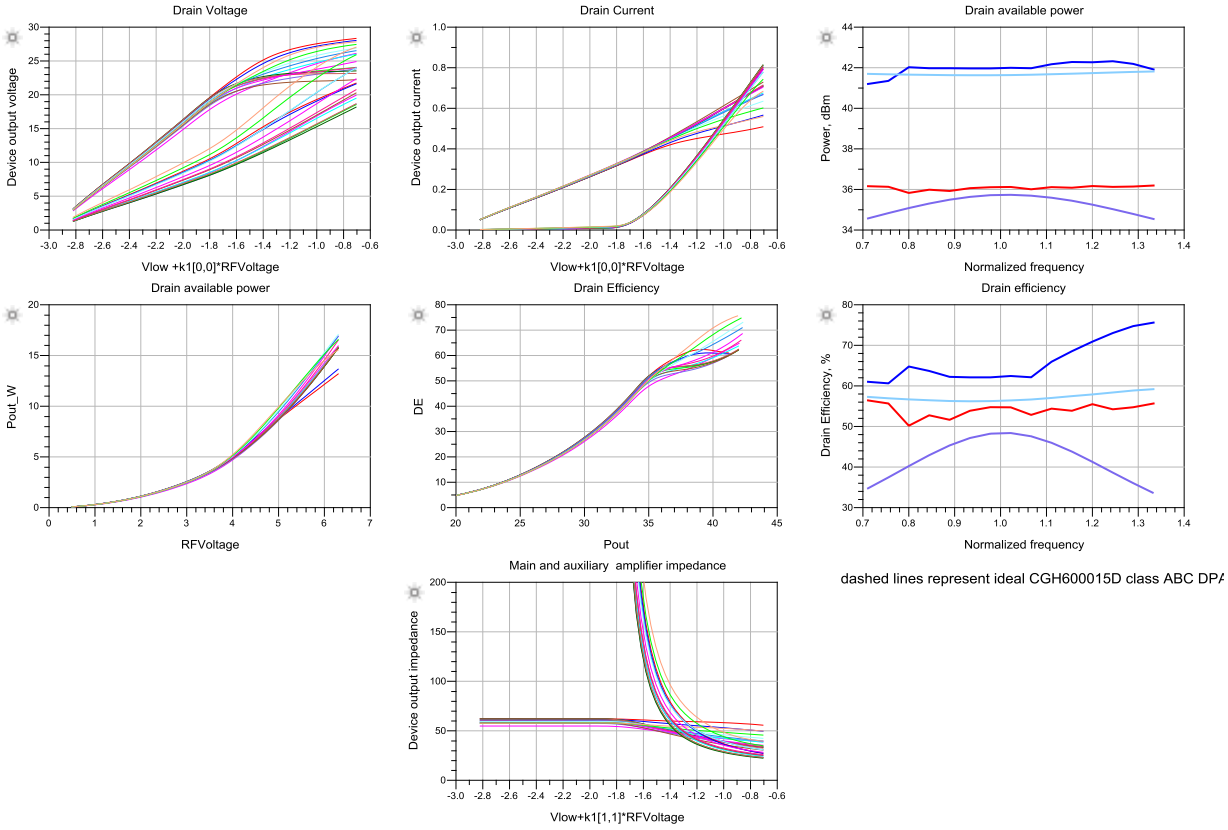

Figure 4-3: Doherty power amplifier performance with optimal impedance terminations

The results shown in Figure 4-3 show a clear improvement over bandwidth compared to those found in Figure 4-1. Looking again at the drain efficiency curve one can again see the large improvement of

efficiency at the band edges. In this case the efficiency improvement is roughly 15% at the upper frequencies and 20% at the lower ones over the baseline Class ABC Doherty power amplifier. Overall with this approach the fractional bandwidth has been improved to 60%

4.2.4 Complete design

After confirming the soundness of the theoretical approach the final steps focused on working with the real unedited device. The parasitics were accounted for and no longer omitted and the harmonics were eventually no longer shorted. Also in this setup unlike before an actual cross junction was inserted at the common node. This of course complicated the design and proper procedures had to be put in place to account for its influence on the design.

In the first pass of the design it was very obvious that something must be added to properly control the harmonics at the output of the device to achieve the desired power and efficiency. A similar approach to that summarized in Section 2.1.3 was utilized.

An ME/IB element was placed at the output of the Main device to help control the performance there. And another ME/IB pair was placed at the output of the auxiliary device at the cross junction of the common node. The IB elements were set to high impedance to minimize their effect on the fundamental matching. Their length was then optimized to recover near maximum performance for both power and efficiency. It was found that the optimal performance across the bandwidth could be achieved with a line length of 435 mils. At this setting the output contours were still overlapping. To allow for inclusion of recent findings with respect to half-wavelength transmission lines and bandwidth extensions, a $\lambda/2$ line was inserted as the ME at the output of the auxiliary device before the cross junction. At that point the load-pull of the new architecture was performed at the fundamental frequency range. At first the second harmonic and third harmonics were shorted to find the appropriate fundamental load at the output of the amplifier. The input at this stage also consisted of a harmonic shorted gate and a voltage source as the input drive. The performance with the newly obtained impedance values was then verified. As before high efficiencies were obtained across the entire design frequency band. At this point it was noted that the fractional bandwidth has shrunk to 44% due to the addition of the above mentioned items.

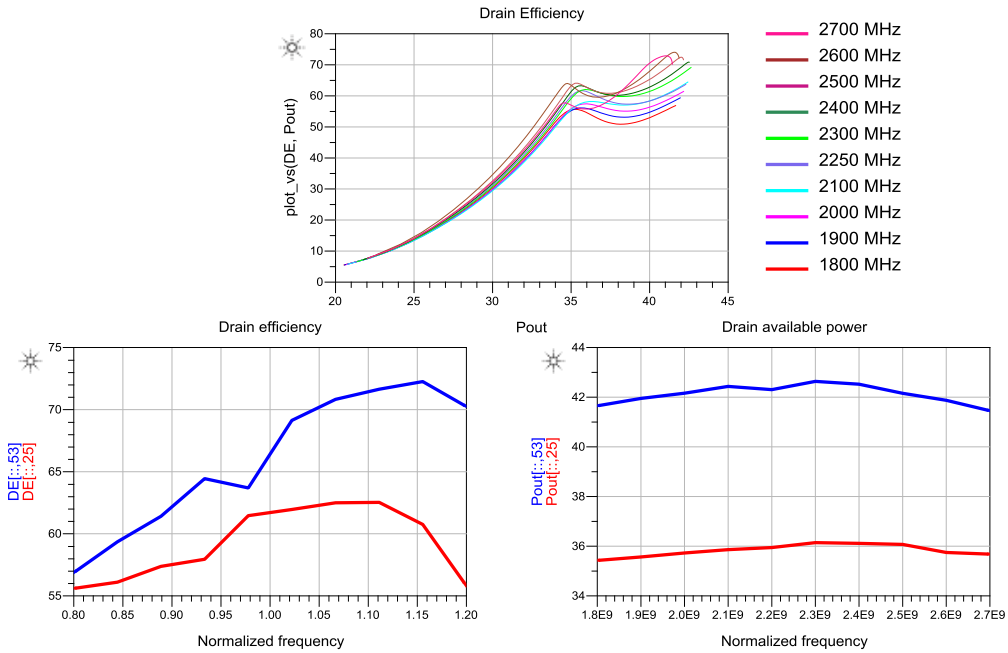

Figure 4-4: Proposed Doherty power amplifier performance with shorted harmonics

The next step was to focus on the design of the third harmonic terminations. Once the third harmonic control was released at the internal drains of the amplifiers the simulation confirmed that 435 mil lines did indeed perform the required job. They have improved the efficiency performance slightly at back-off but significantly at full power. Releasing all harmonic control resulted however in significant deterioration of performance at full power.

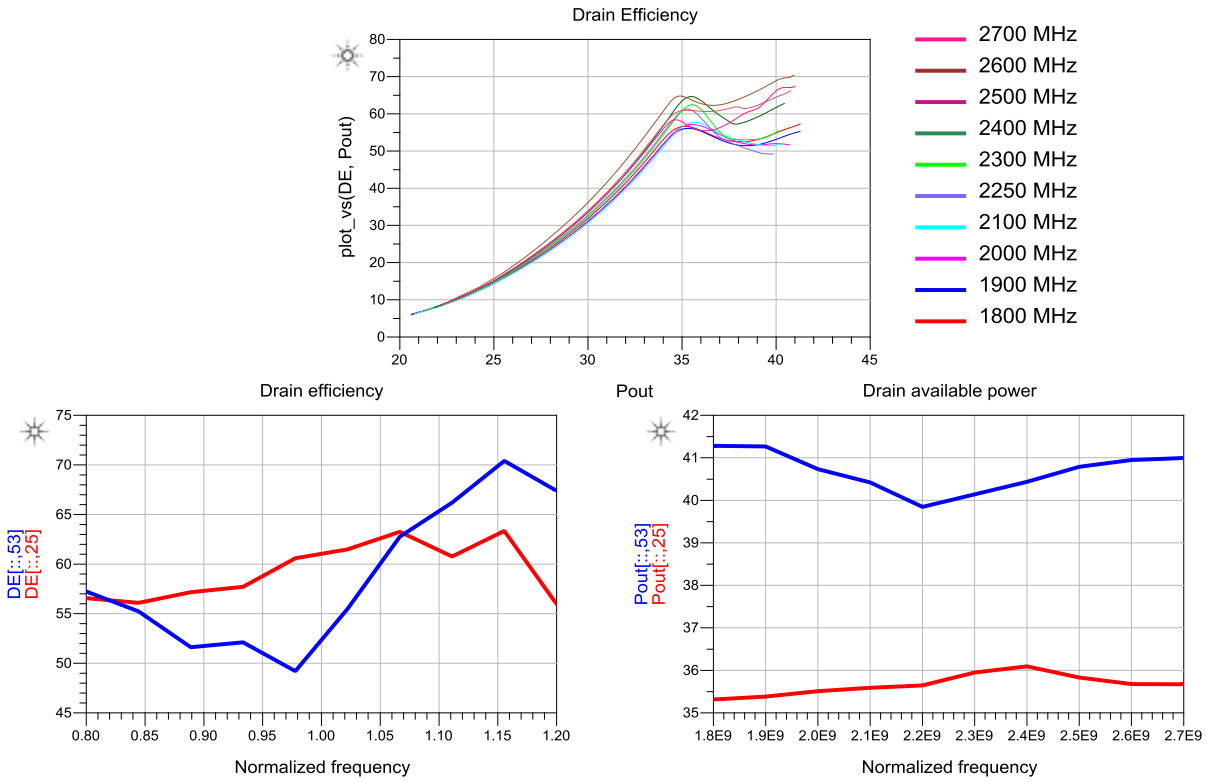

Figure 4-5: Proposed Doherty power amplifier performance without proper harmonic control

At this point to minimize the design time a topology has been selected for the output matching network that would allow for proper second harmonic control as well as proper transformation of the low impedance output to 50 ohm termination. The entire design was re-optimized for both output efficiency and output power across the frequency range.

After that the harmonic shorts at the gate side of the transistors were removed and the stability circuits were added along with input matching networks. During the optimization the input impedance transformation network , ITN, was used to provide the proper power division to the Main and Aux devices making the Wilkinson divider and even split. After several cycles of optimization drain efficiencies near or above 50% were once again obtained at back-off across the entire bandwidth.

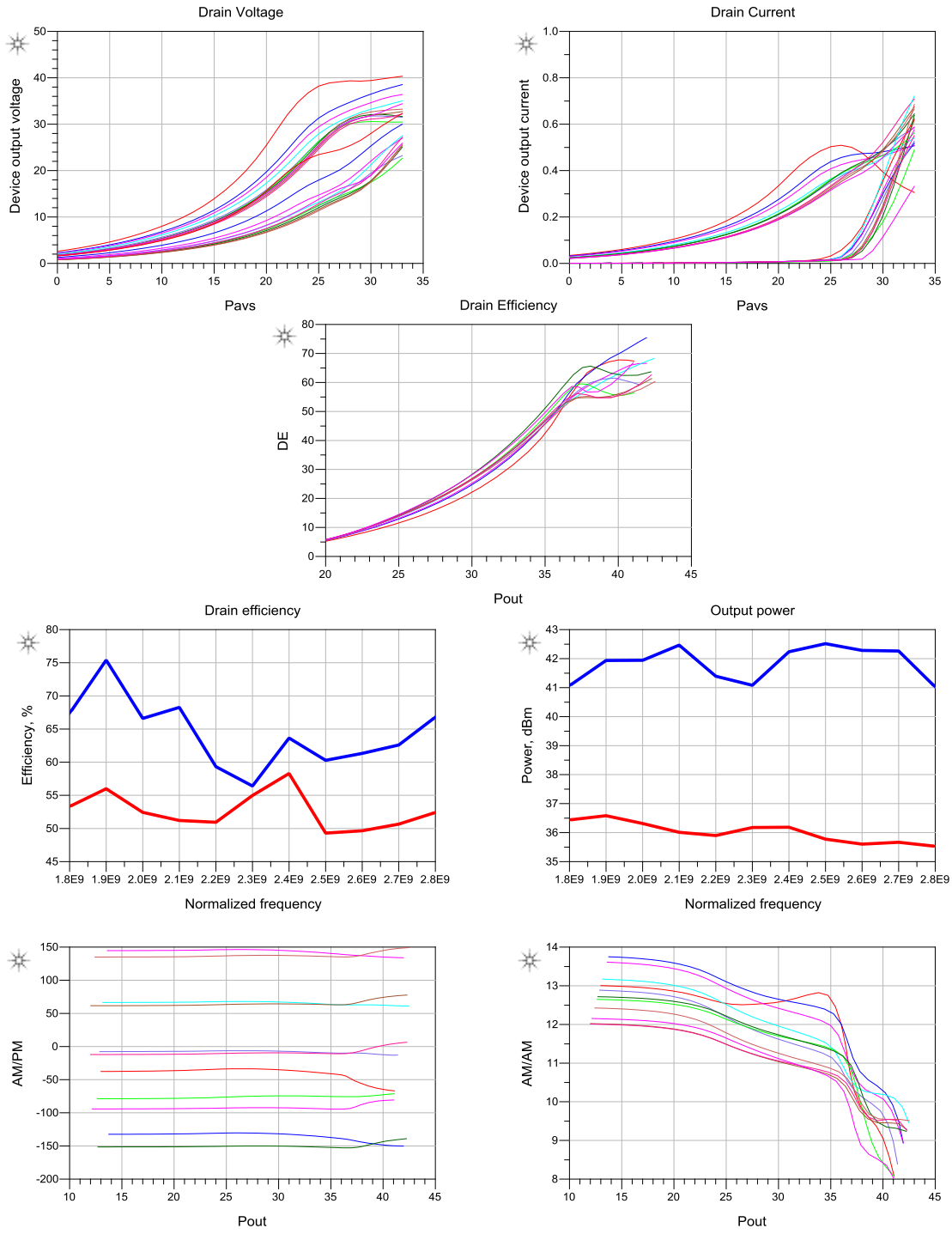

Figure 4-6: Schematic level performance of the proposed Doherty power amplifier architecture

The next step was to transfer the schematic into layout. EM simulations were performed to once again optimize the overall performance. Some software issues have been encountered during this step and it

is believed that the circuit has not been optimally translated into the layout. Nonetheless the overall performance was still fairly good with drain efficiencies near and above 45% recorded across the bandwidth. The final design also indicated 36 dBm output power at back off and 41-42 dBm at peak power.

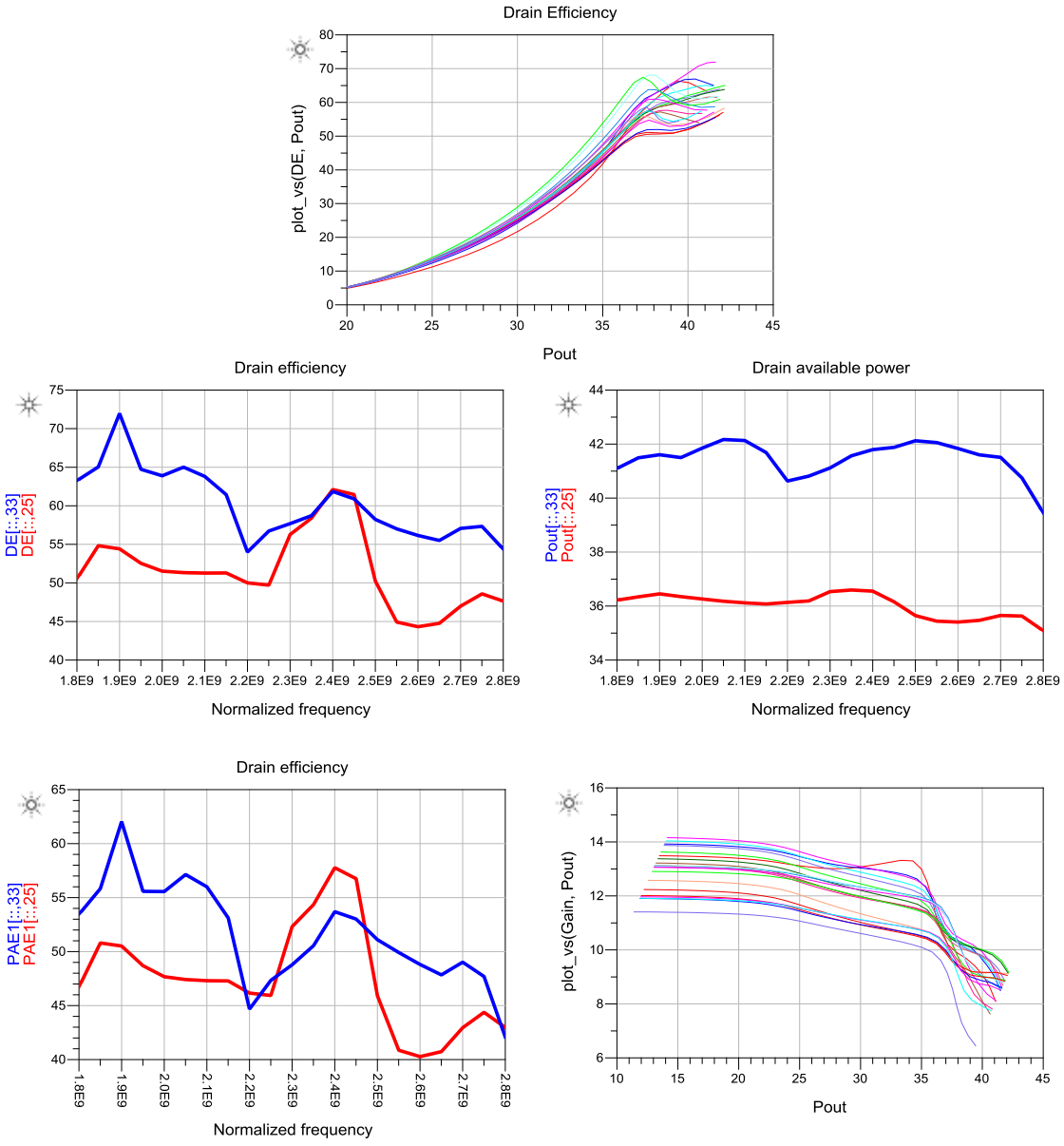

Figure 4-7: EM level performance of the proposed Doherty power amplifier architecture

Chapter 5 Conclusion

5.1 Summary of contribution

This research has presented a novel approach to enhancing the bandwidth of the classical Doherty power amplifier through complex impedance terminations and harmonic tuning.

The thesis started with a review of current wireless standards and their application in broadband communications. It then followed with a detailed review of single ended power amplifiers and their limitations with respect to efficiency performance at back-off for high PAPR signals.

After that a detailed analysis of the classical Doherty power amplifier showed how the amplifier can be used to solve the average power efficiency problem.

The focus of the research was to go beyond that and look at the common sources of bandwidth restrictions in the Doherty power amplifier. This part of the thesis looked to prior art for a deeper understanding of the problem as well as for currently used solutions. It was noted that there are three approaches to trying to solve the bandwidth restrictions: provide wideband matching, provide offset lines and reconfigure the bias voltages. Some designs were more successful than others.

To the author's knowledge this thesis presents one of the top performances on the market. The drain efficiency achieved is above 50% from 1.8 – 2.5 GHz and above 44% from 2.5 – 2.7 GHz at 5-6 dB back-off. This results in 40% fractional bandwidth with output power varying from roughly 41-42 dBm.

5.2 Future work

It is believed that the circuit can be further optimized to achieve higher performance. There are several areas that would benefit from further investigation. The common sources of bandwidth restriction of the Doherty power amplifier were examined in detail. The analysis should however be expended to include the influence of the cross junction of the common node and its interaction with proper fundamental and harmonic terminations. This was a major source of power drop when compared to the more ideal setup. It is due to this cross that the device had to be pushed much harder to achieve the required performance.

The second area that could be explored more fully is related to the mathematical equations in this thesis. Those when properly expended should provide the true solution space to the bandwidth restriction.

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