

Specification Based Bug Detection for Embedded Software

by

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Abstract

Traditional compilers do not automatically analyze processor specifications, thousands of pages of which are available for modern processors. The specifications describe constraints and requirements for processors, and therefore, are useful for software development for these processors. To bridge this gap, our tool em-SPADE analyzes processor specifications and creates processor-specific rules to detect low-level programming errors. This work shows the potential of automatically analyzing processor specifications to detect low-level programming errors at compile time.

em-SPADE is a compiler extension to automatically detect software bugs in low-level programs. From processor specifications, em-SPADE preprocessor extracts target-specific rules such as register use and read-only or reserved registers. A special LLVM pass in em-SPADE then uses these rules to detect incorrect register assignments. Our experiments with em-SPADE have correctly extracted 652 rules from 15 specifications and consequently found 20 bugs in ten software projects. In addition, we explore the use of data mining techniques to learn more about the nature and type of complex checkable rules other than access and reserved bit rules. After applying the frequent itemset mining technique on three specifications, we found that the mining can report complex checkable rules from the specifications with a precision of 53.53% to 82.22% and recall of 36.88% to 75.18%. Thus, the data mining approach is useful for learning complex type of rules in large specifications. These techniques help us identify complex rules. In addition, insights gained from the mining results can be used to improve and standardize specifications. The work is generalizable to other types of specifications and shows the clear prospects of using processor specifications to enhance compilers.

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Dedication

To my parents for their unconditional love, support and motivation.

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Chapter 1

Introduction

Building embedded systems is time-consuming and it is hard to fix bugs in embedded systems after deployment. Therefore, helping developers build such systems is key to the development process. Because of this reason, automated techniques for bug detection are of great use for embedded software.

Embedded system developers have to write software at low level. This means that they directly program different types of hardware, such as registers, memory, timers, interrupt controllers, I/O controllers, and other peripheral controllers. Developers have to initialize hardware and have to work at the register level. Knowing what to do depends on the processor specification and varies between processors. This variability between processors becomes a likely source of bugs. Bugs might occur for a variety of reasons such as—developers' unawareness of such constraints, insufficient knowledge, human errors, etc. Compilers are unable to catch such bugs, because these bugs are not syntactical issues.

Embedded system devices usually come with specifications that state constraints and requirements for these devices. Developers should strictly adhere to the rules and constraints mentioned in the specification describing how to use the device and associated hardware. Because of often only minor variation between devices, developers often rely on knowledge from similar devices and consequently often introduce bugs that incorrectly modify registers.

Thus, it is imperative to utilize specifications to detect bugs in embedded software. Our analysis demonstrates that it is possible to extract invariant rules from specifications and use the extracted rules to automatically check for bugs in embedded software.

Thousands of microcontrollers are currently available and each microcontroller has its own specification. Specifications are large and can extend over one thousand pages. Read-

ing the specification before programming a microcontroller is a laborious and tiresome activity. Large volume of information in specifications can cause unintentional mistakes. While analyzing 15 ATMEL AVR specifications, we found 72 registers on average in each specification. With this many registers, one can expect register-related constraints to be many-folds the number of registers.

We manually studied processor specifications to understand what rules are available in processor specifications and how to extract these rules. The focus of this study was on the processor specifications for the AVR family of microcontrollers, which are embedded devices manufactured by ATMEL corporation. To understand the generality of extracting rules from processor specifications, we also studied a specification for NXP semiconductors qualitatively. This qualitatively study demonstrated that rules across different line of devices remain generic to a good extent; thus, it is possible to build a general rule extractor.

The main focus of this project is to extract and check two common types of constraints: (1) access to “read/write only” registers, and (2) reserved registers. Register bits can be read-only, write-only, or read/write bits. Some bits in registers can be reserved which requires that users do not set reserved bits to one. The implemented rule extractor automatically extracts such rules from processor specifications.

In addition, we explore the use of data mining techniques to facilitate the extraction more complex rules. We demonstrate that it is possible to group sentences that contain rules using frequent itemset mining [4] technique. This grouping is particularly helpful in identifying similar types of rules. Our experiments show that the grouping of sentences closely matches with a list of manually created templates. Developers can use the insights gained from the mining results to quickly extract information from specifications. Specification writers can use the grouping of sentences to improve specifications. Many sentences in specifications have the same or similar meanings but use different words or different word orders. Specification writers can use the data mining results to standardize specifications by choosing the most appropriate sentence from the grouping. They can also create a conciser dataset by removing synonyms.

Our tool, em-SPADE, is a static analysis based checker which compares the source code against the extracted rules to automatically detect bugs. Currently em-SPADE checks the validity of register assignments in underlying source code.

The novelty of this work is that em-SPADE is able to automatically make use of information present in specifications to perform static analysis. This thesis demonstrates that the large volume of the information in specifications can be leveraged for bug detection.

The rule extractor of em-SPADE currently uses simple heuristics to automatically deduce rules from specifications. In the future, we plan to incorporate natural language

processing techniques to extract more complex rules from, for instance, English sentences. This will increase the utility of em-SPADE.

We performed experiments for the family of AVR microcontrollers from ATMEL. To test em-SPADE, we collected code from two sources: (1) application notes from ATMEL for their AVR microcontrollers, and (2) github repository.

em-SPADE found inconsistencies for several AVR microcontrollers. We evaluated em-SPADE on 15 specifications and ten open source embedded software projects. em-SPADE extracted a total of 409 read-write only rules with an accuracy of 99.20% and a total of 243 reserved bit rules with an accuracy of 94.88%. We used em-SPADE to check these rules against the source code of the projects, and found 16 warnings related to read-only rules and 4 errors related to reserved bit rules. These bugs are important because writing to a read-only bit or reserved bits might lead to unintended side effects. While such actions might be fine with one revision of the chip, future revisions might alter the use of, for instance, the reserved bits and consequently introduce subtle bugs in previously functionally correct code.

Using Frequent Itemset Mining [5] on three AVR specifications, we demonstrate that it is possible to automatically identify specification sentences that contain rules and group these sentences by the types of rules. The sentences matching the templates can be used for extracting concrete information.

Organization of the rest of the thesis is as follows. Section 2 describes the problem statement in detail. Section 3 discusses related work. In Section 4, we provide background knowledge on Frequent Itemset Mining [5] and Supervised classification [15]. Section 5 describes the idea and approach of em-SPADE in detail. Section 6 describes the approaches used for identifying complex types of rules. Section 7 discusses experimental methods. Section 8 discusses the bugs detected by the LLVM [13] checker and the rules extracted by the rule extractor. In Section 9, we describe the performance of em-SPADE. Section 10 discusses the limitation, effectiveness and generality of the tool. Finally, in Section 11, we make concluding remarks and discuss future work.

Chapter 2

Problem Statement

em-SPADE bridges the gap between device specifications and the source code that executes on the device. As described in Section 1, specifications detail requirements and constraints that developers need to follow. However, since the volume of this information is vast, it is probable that developers unknowingly violate some constraints. For example, the specification for ATUC128L3U [34] has 964 pages. If developers want to write some code for the ATUC128L3U, they will need to read the entire document. This tedious task creates a likely scenario of making mistakes.

The goal of em-SPADE is to provide reliability by doing cross-validation of embedded software with the corresponding specification. To demonstrate the usefulness of em-SPADE at a basic prototype level, we are only looking at two types of constraints specified in documents. These constraints are related to value assignment to a different register bits. The first type is about register bits designated as read-only or write-only. If a register bit is read-only and developers write to it, then em-SPADE will issue a warning for this because writing to a read-only register bit might change register behavior. We will use *RO-Writes* to refer to writes to read-only register bits.

The other type is related to reserved bits in registers. If some bit is designated as a reserved bit, developers should not write one to it. If it is present in the source code, then em-SPADE will report an error for this violation. Reserved bits might get some functionality in future versions of the device, so incorrectly writing to them might disrupt some intended future functionality. We will use *Reserved-Writes* to refer to writes to reserved register bits.

In specifications, it is standard to use ‘:’ between two register bits to represent a range. For example, “Bits 4:0” represents five bits i.e., 4, 3, 2, 1 and 0. We will use this notation

throughout the thesis.

In the following, we present one example of each type of rule for the ATmega640/V microcontroller:

1. *“TCCR5C—Timer/Counter 5 Control Register C
Bit 4:0—Reserved Bits
These bits are reserved for future use. For ensuring compatibility with future devices, these bits must be written to zero when TCCRnC is written.”* [31]
2. *Bits 7, 6, 4 are read-only bits in the Timer/Counter 1 Interrupt Mask Register (TIMSK1).* [31]

Therefore, em-SPADE is addressing the problem of improper value assignment to register bits. The goal of em-SPADE is to provide reliability with respect to two types of probable issues: (1) RO-Writes, and (2) Reserved-Writes. RO-Writes and Reserved-Writes are likely scenarios in the context of microcontroller code. em-SPADE achieves this goal by cross-checking microcontroller code with corresponding rules in the specification. Since specifications are prose in English language, em-SPADE needs to employ heuristics to automatically extract rules of interest. We discuss the heuristics in detail in Section 5. Our aim is to automate the entire toolchain including the rule extractor. Though, several natural language processing techniques are available for extracting rules, em-SPADE is using simple heuristics for now.

The second issue that we address in this thesis is to learn and extract more complex checkable rules about different entities in microprocessors. Examples of such type of complex rules are the following:

1. *“The WDR (Watchdog Reset) instruction should always be executed before the Watchdog Timer is enabled.”*
2. *“When changing the ACIS1/ACIS0 bits, the Analog Comparator Interrupt must be disabled by clearing its Interrupt Enable bit in the ACSR Register.”*
3. *“Bit 5 SE: Sleep Enable The SE bit must be set (one) to make the MCU enter the sleep mode when the SLEEP instruction is executed.”*
4. *“The Stack Pointer must be set to point above 0x60.”*

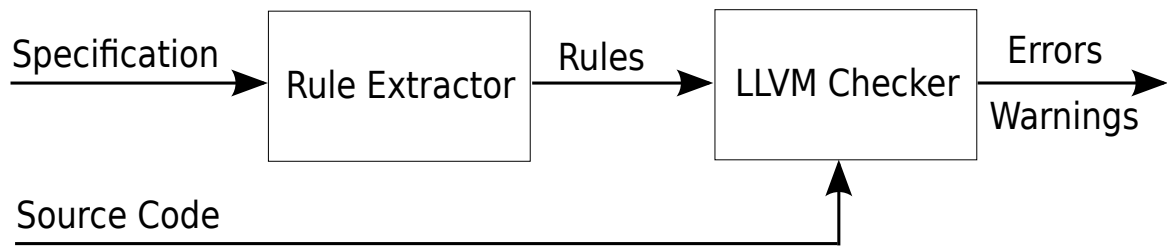


Figure 2.1: General framework of em-SPADE

Chapter 3

Related Work

To the best of our knowledge, em-SPADE is the first to automatically analyze processor specifications for automatic bug detection.

Our work consists of two parts: (1) extracting invariants from device specifications, and (2) applying the invariant rules to find bugs in embedded software. Therefore, we discuss work related to rule extraction from natural language documents, and work related to static analysis based bug detection in embedded software.

Fehnker et al. [10] present an automatic bug detection tool which uses static analysis to find bugs in microcontroller software. They examine three types of issues: (1) incorrect-interrupt-handling check; (2) incorrect-timer-service check; and (3) register-to-reserved-bits check. The last check detects similar bugs as em-SPADE. However, the idea of their paper is different from em-SPADE. They manually create rules in the form of CTL formulae for these three types, and their static analysis tool detects bugs based on the rules. Although the bug detection process is partially automatic, automating the rule extraction process is unaddressed, which is exactly the main contribution of em-SPADE.

Dinesh et al. [8] present techniques to extract formal specifications from legal documents, which, are in natural language. They derive CTL specifications from the document which model checking tools can use for verification of models. The specifications are obtained with the use of intermediate semantic representation of different sentences. On the similar line of work, Pandita et al. [23] discuss about extracting formal method specification from natural language text of API documents.

iComment [36] proposes to detect bugs by analyzing comments in the code. They use NLP, statistical and machine learning techniques to analyze comments in source code. The

paper presents the novel idea of automatically analyzing comments to extract programming rules. iComment uses the extracted rules to automatically detect inconsistencies between comments and source code. Based on the analysis, the tool indicates either bugs or bad comments. On the similar line of work, Padioleau et al. [22] discuss the taxonomies and characteristics of comments in operating system (OS) codes. Empirical data presented in the paper shows that comments in OS code are not merely explanations and it is possible to exploit comments for software bug detection.

PR-Miner [17] extracts general programming rules from large software projects and uses them to automatically detect violations in the code. It uses a data mining technique called frequent itemset mining to extract implicit programming rules. AccMon [44] presents automatic detection of memory related bugs using program counter based invariants. Alattin [37] is an alternative pattern mining technique for detecting neglected conditions. RRFinder [39] automatically mines resource-releasing specifications for API libraries. Xie et al. [41, 40] discuss mining techniques for software engineering and program source code data.

Our implementation of rule checker is static which uses LLVM to issue warnings or errors at compile time. The rule checker can be implemented at run-time as well. Csallner and Xi [7], and Smaragdakis and Csallner [28] discuss about combined static and run-time approaches. Engler et al. [9] discuss concepts that lay the foundation of static analysis. The originality of their paper is that they extract the checking information from the code itself and use them to find inconsistencies in the code. The tool can be used to find bugs in source code without any prior knowledge of the system. Hallem et al. [12] describe a framework for performing system specific static analysis.

Chapter 4

Background

In this section, we present the background about frequent itemset mining and supervised classification. The classification model for complex rules is based on the knowledge gained from frequent itemset mining, and is a supervised classification model.

4.0.1 Frequent Itemset Mining

Frequent Itemset Mining [5] is a data mining technique that generates frequently appearing sets of variables in a transactional database. Frequent itemset mining technique analyzes the transactions to find frequently appearing variables. In its simplest form, this mining technique can produce the set of variables that often appear in transactions. The technique can be applied based on the desired support [16] of the sets. The support of an itemset is the percentage of sets that contain all of the items listed in that itemset. The frequent itemset mining can also be used for association rule learning which help discover interesting relationship between variables. Freely available tools such as apriori package [6] perform frequent itemset mining as well as association rule learning.

We treat each sentence as a transaction and the words in it as transaction items. The frequent itemset mining perform the grouping of words based on their frequency in the transactions. The resulting groups help us understand the association of keywords in sentences, which is essential in discovering new type of rules. We present an example of two sentences from ATmega169 specification to explain the use of frequent itemset mining in our work.

1. *When changing the ACD bit, the Analog Comparator Interrupt must be disabled by clearing the ACIE bit in ACSR.*

2. *When changing the ACIS1/ACIS0 bits, the Analog Comparator Interrupt must be disabled by clearing its Interrupt Enable bit in the ACSR Register.*
3. *Bit 4 - WDCE: Watchdog Change Enable - This bit must be set when the WDE bit is written to logic zero.*
4. *The SE bit must be written to logic one to make the MCU enter the sleep mode when the SLEEP instruction is executed.*
5. *When entering ADC Noise Reduction mode, the Analog Comparator should be disabled.*

If we set the minimum support to 50%, the frequent itemset mining algorithm generated the itemset <When, Analog, Comparator, disabled> from the sentences above. One can observe that these keywords belong to the first two sentences which means that there is a good level of similarity between the first two sentences. In this case, they represent the same type of rule. Such grouping of sentences can help users find large number of sentences belonging to the same type, which is much more efficient than users examining all sentences one by one. Note that we applied stopwords filtering to exclude generic common and meaningless words.

Chapter 5

The Framework

This section describes the two components of em-SPADE: (1) Rule extractor, and (2) LLVM checker. The idea of em-SPADE is to extract invariant rules from specifications and use them to detect bugs in embedded software. Therefore, these are related to the two components of em-SPADE respectively. em-SPADE follows the static analysis approach by issuing warnings or errors at compile time to indicate bugs. The automatic approach of extracting rules from specifications is based on heuristics and does not involve any natural language processing.

Figure 2.1 presents a schematic view of em-SPADE. The first component of em-SPADE, i.e., the rule extractor, takes a microcontroller specification as input and gives the extracted rules in XML format as output. The second component of em-SPADE, i.e., the LLVM checker, takes the XML rules and software code as input and produces errors and warnings as output. We discuss the two components in detail in following subsections.

5.1 Rule Extractor

To gather preliminary data, we first performed an extensive study of four specifications to understand the types of rules. Three of the specifications are for AVR microcontrollers (i.e., ATtiny4 [32], ATmega640/V [31], and ATUC256L3U [34]) and one is for the ARM-M3 based microcontrollers (i.e., UM10360 [35]). The ATtiny4 and ATmega640/V are 8-bit AVR microcontrollers with different sizes of in-system programmable flash. ATUC256L3U is 32-bit Atmel AVR Microcontroller. LPC17xx family are ARM Cortex-M3 based microcontrollers. Section 4.1.1 presents examples of manually extracted rules for ATmega640/V [31] and ARM-M3 processors.

Bit	7	6	5	4	3	2	1	0	
(0x65)	–	–	PRTIM5	PRTIM4	PRTIM3	PRUSART3	PRUSART2	PRUSART1	PRR1
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Figure 5.1: Layout of PRR1 register in ATmega640/V

5.1.1 Rules to Extract

While this thesis, for now, focuses only on the two mentioned types of rules, the initial study investigated more types of constraints. Consequently, some rules listed below fall outside the category of access type and reserved bit type of rules. These rules show the great potential of generalizing our approach to other types of rules. Some rules from ATmega640/V [31] are:

1. “XMCRB—External Memory Control Register B; Bit 6:3—Res: Reserved Bits; These bits are reserved and will always read as zero. When writing to this address location, write these bits to zero for compatibility with future devices.”
2. “ACSR—Analog Comparator Control and Status Register; When changing the ACD bit (i.e., bit 7), the Analog Comparator Interrupt must be disabled by clearing the ACIE bit in ACSR. Otherwise an interrupt can occur when the bit is changed.”
3. Bits 6:4 in the Clock Prescale Register (CLKPR) are read-only bits.
4. “ADCSRB—ADC Control and Status Register B: Bit 7—Res: Reserved Bit; This bit is reserved for future use. To ensure compatibility with future devices, this bit must be written to zero when ADCSRB is written.”
5. “Bit 0—EERE: EEPROM Read Enable; When the correct address is set up in the EEAR Register, the EERE bit must be written to a logic one to trigger the EEPROM read.”

Some rules from the NXP UM10360 [35] are as follows:

1. “Reset Source Identification Register (RSID—0x400F C180); 31:4—Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.”

2. Bit *PLL0STAT* in the *PLL0* register is read-only and Bit *PLL0FEED* in the *PLL0* register is write-only.
3. “*PLL1 Status register (PLL1STAT—0x400F C0A8); 31:7—Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.*”
4. “*PLL1 Feed register (PLL1FEED—0x400F C0AC); 31:8 —Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.*”
5. “*External Interrupt Flag register (EXTINT - address 0x400F C140); 31:4—Reserved, user software should not write ones to reserved bits. The value NA read from a reserved bit is not defined.*”

Processor specifications follow similar structure and content across chip vendors. The first specification is for an ATMEL based microcontroller whereas the second specification is for microcontrollers from NXP semiconductors. Although these specifications are from different vendors, yet the extracted rules are substantially analogous. Therefore, if it is possible to build a tool to extract rules from AVR microcontrollers, the tool should be able to extract rules from other lines of microcontrollers with small or no modifications.

5.1.2 How to Extract the Rules

After this study showed that processor specifications are similar in structure and content, we started creating the automatic rule extractor primarily for the AVR family of microcontrollers. The rule extractor is based on the following observations:

1. The register description layout allows us to get information about the specific bits. Figure 5.1 shows one such example for Power Control Register 1 (PRR1). Bits 7 and 6 in this register are designated as read-only bits while the rest of the bits are all read and write bits.
2. Register names are in uppercase letters with few numeric characters. Lowercase letters, if any, appear after the first three characters in the name. Also, register names are acronyms with a given acronym description. Timer/Counter Control Register A (TCCR0A) is an example from the ATmega640/V specification. USARTn Control and Status Register B (UCSRnB) is another example from ATmega128 specification.

3. Reserved bits in registers have descriptions. We are able to look up these with keyword searches. For example, EECR register in the ATmega640/V specification has the following description about some reserved bits: “Bits 7:6 — Res: Reserved Bits. These bits are reserved bits and will always read as zero.” We have observed this kind of description in all AVR specifications and the NXP UM10360 specification.

Based on these observations, the rule extractor applies the following heuristics to extract the reserved bit and read- and write-only rules:

Heuristics for Reserved Bit Rules – The extraction of reserved bit type of rules starts with identifying the sentences that describe the reserved bits in registers. For this, the rule extractor goes through the sentences and looks for related words such as ‘reserved’ and ‘unused’. Sentences of this type are converted to concrete checkable rules if reserved bit numbers and the register name can both be found. Since the sentence describing the bits is placed as per the bit numbers, it is easy to find the bit numbers given the sentence. The extractor needs only look at the beginning of the sentence, and find the bit number or range of bits. For an example, “Bits 5..0 Res: Reserved Bits - These bits are reserved bits in the ATmega103(L) and will always read as zero.” is a description for reserved bit range 5 to 0 in ‘SPSR’ register in ATmega103. Note that the extractor uses regular expression such as “`\\Bit[\\s+s][\\s0-9:.,]*`” for matching the bit numbers. This is a ‘Boost’ [27] based regular expression which requires an extra backslash before any escape sequence involving a backslash such as ‘`\\s`’.

Extraction of the register name is simple. Unlike bit numbers, the register name might not be available at the beginning of the sentence. However, the name is present in close vicinity of the bit description. Based on our observation, the rule extractor looks at the preceding 100 sentences for the register name. Register names are alphanumeric with all letters in capital. Also, the name is based on the acronym of words which are also available along with the name. For example, “ADC Control and Status Register - ADCSR” in ATmega103. One can observe that the register name ‘ADCSR’ is an acronym of ‘ADC Control and Status Register’. One can use this observation to confirm the validity of the extracted register name.

Heuristics for Read- and Write-only Rules – Extraction of read- and write-only rules is based on the register description layout such as the layout shown in Figure 5.1. One can observe that each bit in this register is designated as ‘R’, ‘W’ or ‘R/W’. ‘R’ represents a read-only bit, ‘W’ represents a write-only bit and ‘R/W’ represents a read-write bit. For read-only and write-only rules, we need the bit numbers which are read-only or write-only along with the register name.

The rule extractor uses regular expression matching technique for identifying the register description. It looks for the bit description pattern in the document, and then uses this pattern to find the read-only or write-only category of each bit. The regular expression used is - “[R/W]*\\s[R/W]*\\s[R/W]*\\s[R/W]*\\s[R/W]*\\s[R/W]*\\s[R/W]*\\s[R/W]*”. This is again a ‘Boost’ [27] based regex with the an extra backslash before the escape sequence ‘\s’. The eight occurrences of ‘R/W’ in the above regular expression correspond to the eight register bits which are marked as either ‘R’ or ‘W’. This regex identifies register bits from register layouts such as the one in Figure 5.1. Note that extraction of the register name is the same as it is for reserved bit rules.

The tool applies a combination of above mentioned heuristics and uses some stop words, such as MCU and AVR, to extract the rules. Specifications of processors are generally in PDF format. em-SPADE first converts it into text format using a free PDF-to-text tool called `pdftotext` [25]. For comparison, we also tried other available tools such as `pdftxt`, `ebook-convert`, `pdf2ps`, `ps2ascii` and `ps2txt`. `pdftotext` is better than all of these in terms of preserving format and information. Once em-SPADE gets the text form of the specification, it reshapes the text by getting rid of empty lines and merging some lines to get the original register description layout. The tool relies on the Boost regular expression libraries [27] to search for patterns and uses C++ containers available in Standard Template Library (STL) to manipulate the intermediate data during rule extraction. The rule extractor writes the rules into a simple text file, which the next module of the tool converts to rules in XML format. The LLVM checker in em-SPADE leverages these extracted rules directly to detect bugs.

5.1.3 Conversion of Rules to XML Format

em-SPADE uses XML to store extracted rules from specifications. The rules XML file is an input to the LLVM checker along with the software code. Figure 5.2 shows an example of a reserved bit rule in XML. The rule corresponds to bit 6 in External Memory Control Register B (XMCRB) of ATmega640/V [31] microcontroller. In this example, the register name is present in line 6 in Figure 5.2. The next line lists the location of the reserved bit in the register. Figure 5.2 shows only the XML expression for the 6th bit of the XMCRB register. Similar expressions can be written for other bits, i.e., 5:3.


```

1  <?xml version = '1.0'?>
   <!DOCTYPE rules SYSTEM 'rules.dtd'>
3  <rules>
   <equals>
5     <l>
       <bit_id = 'XMCRB'
7         location = '6' />
   </l>
9     <r>
       0
11    </r>
   </equals>
13 </rules>

```

Figure 5.2: An example of reserved bit rule in XML

5.2 LLVM Checker

This subsection describes the static checker implemented in LLVM [13]. LLVM stands for Low Level Virtual Machine. It is a compiler infrastructure that allows users to perform a variety of optimizations on the source code with the help of LLVM passes. Building a pass creates a shared object, which users can load using the LLVM optimizer tool *opt* [13]. *Opt* can load LLVM specific bitcode files and perform optimizations written in the pass. Using LLVM passes, we can also do static analysis of the source code. The checker of em-SPADE is an implementation of an LLVM pass.

The pass implemented for em-SPADE performs static analysis based on the XML rules file. Since, the rules of interest only have reserved bits and access type of rules, the pass looks at assembly statements, which are assignments to some registers. The pass parses the XML rules using *libxml2* and verifies the validity of assignments. Assignments become store instructions in LLVM intermediate representation (IR) of the program, so the LLVM checker specifically looks at store instructions in the LLVM IR. The LLVM pass works on a subclass of the `FunctionPass` [11] class. `FunctionPass` executes on all functions, and is useful for inspecting the statements in various functions in a program. The pass works by overriding an abstract virtual method inherited from `FunctionPass`. All the processing in the pass happens within this function. The subclass created in the pass is registered with a name and description. The LLVM optimizer requires this name to invoke the pass. Note that the compilation of the pass creates a shared object file which is loaded using the LLVM optimizer tool.

If the checker finds inconsistencies in assignments based on the rules file, it will produce warnings and/or errors. Since, writing one to a reserved bit can cause problems for a future versions of the device, em-SPADE reports reserved bit violations as errors. However,

violations of access type of rules produce warnings. It is important to mention that register names in *avr-libc* are present as macros. Therefore, the tool does not find the register names in the IR of the program. This necessitates another small module in em-SPADE which creates a mapping of register names and corresponding macro values. It does the mapping by parsing the specification header file in the library. Header files for all AVR microcontrollers are available in *avr-libc*, which is a part of the *avr-gcc* toolchain. This small module creates this mapping in an simple text file which the LLVM pass reads while going through the IR of the program. These changes do not affect LLVM binaries as the changes are only limited to mapping register name macros from headers files to text files.

em-SPADE compiles the program under test with debug options to get more information about the instructions. Thus, em-SPADE is able to provide sufficient information about the warnings and errors that it reports. This helps developers in locating bugs in the program. Currently, em-SPADE only examines one-line instructions in LLVM intermediate representation, and does not handles cases where writes to reserved or read-only bits are data-dependent or conditional.

In summary, we have implemented em-SPADE in C++ that uses LLVM as back-end for performing static analysis. em-SPADE uses `pdftotext` to parse specification PDF documents in text form. Additionally, it uses C++ standard template library, Boost regex library and *libxml2* library. em-SPADE uses Clang as a front end to get the LLVM bitcode from the source.

Chapter 6

Techniques for Complex Rules

In this section, we discuss the use of data mining technique in identifying and grouping complex types of rules.

6.1 Data Mining

To gather knowledge about the complex type of rules from the specifications, we explored the use of data mining technique on the textual data in specifications. Since the corpus of text is large, we extracted modal verb sentences because sentences that contain modal verbs, such as must and should, tend to contain rules. Modal verb sentences are key to finding relevant sentences stating constraints or rules. To gain information from the corpus of modal verb sentences from a set of specifications, we perform frequent itemset mining to learn the most frequent words and their associations. We use the apriori algorithm [6] for performing the frequent itemset mining. The apriori algorithm operates on a database containing transactions. Each transaction is a set of items. For our purpose, the transactions correspond to sentences, and itemsets are words in the sentences. Note that these sentences do not contain any stopwords. This algorithm provides options for setting parameters such as type of itemset, minimum/maximum number of items per set, minimum/maximum support for a set, type of sorting on items, etc. Our technique selects the closed itemset type and sets a value for minimum number of items. It also sets a value for minimum support for a set, and chooses decreasing order for sorting.

To prepare the data for analysis, we perform punctuation correction such as forming one word from hyphenated words by removing the hyphen. We then remove stop words

from the data by running a script. The data is now ready for apriori algorithm to perform frequent itemset mining.

Insights gained from the mining results can be used to quickly extract information from specifications and improve specification writing as following:

1. **Reuse for other specifications.** The grouping of sentences based on the frequent itemsets will make it possible for developers to examine thousands of or more specifications. Developers can examine groups of sentences and decide whether a group of sentences contains rules or not. This would be less time consuming than examining the entire specifications.
2. **Improve specification writing.** The frequent itemset based grouping will help specification writers standardize specifications and write better specifications. Many sentences in specifications have the same or similar meanings but use different words or different word orders. We can use our results to help people use the same format to standardize specifications.
3. **Recommend the most appropriate sentence.** Grouping produced by the frequent itemset mining results can be used to recommend the most appropriate sentences. In addition, specification writers can examine the groups and choose the most appropriate sentence.
4. **More concise datasets.** It will enable finding synonyms from similar sentences, e.g., write and set, logical one and one, etc. Synonyms are semantically related, and therefore finding them helps developers quickly search for sentences with similar meaning [42]. Specification writers can examine the synonyms and use the most appropriate one to reduce unique keywords in specifications.

6.1.1 Manually Defined Rule Templates

Having manually identified a set of “checkable rules”, we propose Linear Temporal Logic (LTL) formula [26] templates that represent these rules. Developers can use these templates to identify rules of same type. A LTL formula shows the logical validity of conditions over time. The following highlights the two LTL templates with example sentences for each template.

1. **Template:** $G(A \Rightarrow B)$
Description: This LTL formula template states that globally, ‘A’ implies ‘B’, where

‘A’ and ‘B’ are boolean expressions.

Examples:

- (a) To save power, the ADC should be disabled before entering any sleep mode.
Explanation: In this, ‘A’ corresponds to ‘any sleep mode’ and ‘B’ corresponds to the ‘ADC disable event’.
- (b) When entering Idle mode, the Analog Comparator should be disabled if not used.
Explanation: Here ‘A’ refers to the ‘idle mode’ and ‘B’ refers to ‘analog comparator disable event’.
- (c) This bit must be set (one) when the WDE bit is cleared, otherwise, the Watchdog will not be disabled.
Explanation: ‘A’ corresponds to “WDE == 0” and ‘B’ corresponds to “this_bit == 1”.
- (d) The WDR (Watchdog Reset) instruction should always be executed before the Watchdog Timer is enabled.
Explanation: In this example, ‘A’ is ‘watchdog timer enable event’ and ‘B’ is ‘WDR instruction execution event’.
- (e) When writing ADCSR, a logical “0” must be written to this bit.
Explanation: ‘A’ here corresponds to ‘ADCSR write event’ and ‘B’ corresponds to “this_bit == 0”.
- (f) To make the comparator trigger the Timer/Counter1 Input Capture interrupt, the ICIE1 bit in the Timer Interrupt Mask Register (TIMSK1) must be set.
Explanation: ‘A’ is “Timer/Counter1 Input Capture interrupt event” and ‘B’ is “ICIE1 == 0”.
- (g) The SE bit must be set (one) to make the MCU enter the sleep mode when the SLEEP instruction is executed.
Explanation: ‘A’ is “sleep instruction execution event” and ‘B’ is “SE == 1”.
- (h) The EEMWE bit must be written to one before a logical one is written to EEWE, otherwise no EEPROM write takes place.
Explanation: ‘A’ corresponds to “EEWE == 1” and ‘B’ corresponds to “EEMWE == 1”.
- (i) When waking up the SPI again, the SPI should be reinitialized to ensure proper operation.
Explanation: Here ‘A’ is ‘SPI wakeup event’ and ‘B’ is ‘SPI reinitialization’.

2. **Template:** $G(A)$

Description: This formula states that globally, boolean expression ‘A’ holds true.

Examples:

- (a) This bit should never be programmed.

Explanation: Here ‘A’ is the boolean expression corresponding to ‘not programming the bit’.

- (b) The Stack Pointer must be set to point above 0x60.

Explanation: In this case, ‘A’ is the boolean expression for ‘stack pointer being set above 0x60’.

- (c) These bits are reserved and should be left unprogrammed.

Explanation: In this case, ‘A’ is the boolean expression corresponding to ‘unprogramming of the bits’.

Note that these templates can involve other LTL operators as well. For example, the LTL representation of the second part of “It is recommended to write the Sleep Enable (SE) bit to one just before the execution of the SLEEP instruction and to clear it immediately after waking up” would be :

$$G((SLEEP\ INSTR) \Rightarrow X(SE == 0))$$

Where ‘X’ represents the LTL operator called ‘next’. This LTL formula states that it is globally the case that the ‘SE’ bit needs to be set to zero just after (i.e. in the next state) the sleep instruction is executed.

Chapter 7

Experimental Method

This section discusses the experimental method under the following four subsections:

7.1 Subjects & Design

To test technical feasibility and understand how em-SPADE works in practice, we experimented with several AVR processors from ATMEL. To experiment with the rule extractor of em-SPADE, we randomly selected ten specifications for training. After training the rule extractor, we randomly selected another set of five specifications for evaluating the rule extractor of em-SPADE.

For evaluating em-SPADE’s capabilities of finding bugs, we looked at application notes [20] and source from ATMEL. Application notes are general application programs for ATMEL based microcontrollers. The application notes span over different domains such as automotive, home appliances, industrial automation, mobile electronics, PC peripherals. em-SPADE analyzed 81 application notes downloaded from ATMEL website. Source code of these application notes contain 50 to 500 lines of code. Apart from this, em-SPADE also analyzed projects for ATMEL AVR microcontrollers available at github.

The 15 specifications in the training and evaluation set cover a wide variety of microcontrollers. They represent three subfamilies: (1) ATmega, (2) ATtiny, and (3) AT90S. These 15 specifications dictate requirements and constraints for 39 AVR microcontrollers. With 39 microcontrollers spanning over three subfamilies, the training and evaluation set becomes representative of AVR microcontrollers. Therefore, the selected set of 15 spec-

ifications representing 39 AVR microcontrollers provides a good variability and scale for testing em-SPADE. The 15 specifications are the following:

1. AT90S2313 – 8-bit AVR Microcontroller with 2K Bytes of In-System Programmable Flash (Rev. 0839IAVR06/02)
2. AT90S8515 – 8-bit AVR Microcontroller with 8K Bytes In-System Programmable Flash (Rev. 0841G09/01)
3. ATmega169, ATmega169V – 8-bit AVR Microcontroller with 16K Bytes In-System Programmable Flash (Rev. 2514PAVR07/06)
4. ATtiny25/V, ATtiny45/V, ATtiny85/V – 8-bit AVR Microcontroller with 2/4/8K Bytes In-System Programmable Flash (Rev. 2586NAVR04/11)
5. ATtiny24, ATtiny44, ATtiny84 – 8-bit AVR Microcontroller with 2/4/8K Bytes In-System Programmable Flash (Rev. 8006KAVR10/10)
6. ATmega103, ATmega103L – 8-bit AVR Microcontroller with 128K Bytes In-System Programmable Flash (Rev. 0945IAVR02/07)
7. ATmega8, ATmega8L – 8-bit AVR Microcontroller with 8K Bytes In-System Programmable Flash (Rev. 2486ZAVR02/11)
8. ATmega128, ATmega128L – 8-bit Atmel Microcontroller with 128KBytes In-System Programmable Flash (Rev. 2467XAVR06/11)
9. ATtiny13, ATtiny13V – 8-bit AVR Microcontroller with 1K Bytes In-System Programmable Flash (Rev. 2535JAVR08/10)
10. ATmega48/V, ATmega88/V, ATmega168/V – 8-bit Atmel Microcontroller with 4/8/16K Bytes In-System Programmable Flash (Rev. 2545TAVR05/11)
11. ATmega640/V, ATmega1280/V, ATmega1281/V, ATmega2560/V, ATmega2561/V – 8-bit Atmel Microcontroller with 64K/128K/256K Bytes In-System Programmable Flash (Rev. 2549PAVR10/2012)
12. ATtiny4, ATtiny5, ATtiny9, ATtiny10 – 8-bit AVR Microcontroller with 512/1024 Bytes In-System Programmable Flash (Rev. 8127EAVR11/11)
13. ATmega48PA, ATmega88PA, ATmega168PA, ATmega328P – 8-bit AVR Microcontroller with 4/8/16/32K Bytes In-System Programmable Flash (Rev. 8161DAVR10/09)

Table 7.1: Summary of detected bugs

Project	Total	Reserved-Writes	RO-Writes
Optiboot	1	1	0
Libpolulu	3	3	0
AVR064	2	0	2
AVR130	3	0	3
AVR132	3	0	3
AVR312	2	0	2
AVR314	2	0	2
AVR318	1	0	1
AVR319	1	0	1
AVR441	2	0	2
Aggregate	20	4	16

14. AT90S8535, AT90SL8535 – 8-bit AVR Microcontroller with 8K Bytes In-System Programmable Flash (Rev. 1041H11/01)
15. ATtiny261/V, ATtiny461/V, ATtiny861/V – 8-bit AVR Microcontroller with 2/4/8K Bytes In-System Programmable Flash (Rev. 2588EAVR08/10)

For data mining experiments, we randomly selected the following three AVR specifications from ATMEL:

1. ATmega103, ATmega103L – 8-bit AVR Microcontroller with 128K Bytes In-System Programmable Flash (Rev. 0945IAVR02/07)
2. ATmega169, ATmega169V – 8-bit AVR Microcontroller with 16K Bytes In-System Programmable Flash (Rev. 2514PAVR07/06)
3. ATtiny13, ATtiny13V – 8-bit AVR Microcontroller with 1K Bytes In-System Programmable Flash (Rev. 2535JAVR08/10)

7.2 Apparatus

We performed the experiments on a Lenovo T420 machine which has an Intel Core i5-2520M processor running at 2.50 GHz. It has 4.0 GB RAM memory and is running Ubuntu 12.10 which has 3.5.0-26-generic version of the Linux kernel.

We manually collected the data about the rule extractor by inspecting the generated rules file for each specification. Then, we compared these rules with the manually extracted rules to calculate different metrics. Source codes of AVR based software were downloaded from ATMEL AVR and github websites.

7.3 Measures

We use the following metrics about the extracted rules from different specifications in the training and evaluation set: (1) Actual Total Rule, (2) True Positives (TP), (3) False Positives, (4) False Negatives, (5) Precision, (6) Recall, and (7) F_1 score. Actual Total Rule gives the number of manually extracted rules from the specifications. True positives (TP) are the correct rules reported by em-SPADE. False positives (FP) are the incorrect rules reported by em-SPADE which are not actual rules. False negatives (FN) are the rules that em-SPADE missed to report.

Precision (P) is the fraction of extracted rules that are correct. Precision is defined as:

$$P = \frac{TP}{TP + FP}$$

Recall (R) is the fraction of correct rules that em-SPADE extracts. It is defined as:

$$R = \frac{TP}{TP + FN}$$

F_1 score is a measure of accuracy which takes both precision and recall into account:

$$F_1 = 2 * \frac{P * R}{P + R}$$

F_1 score reaches its best value at one and worst value at zero.

7.4 Procedure

We performed the testing by categorizing the software code according to the specifications in the training and evaluation set. For example, to test microcontroller software for bugs

Table 7.2: Data about extracted reserved-bit rules from training specifications

Specification	Actual	Tool	FP	FN	P (%)	R (%)	F_1
AT90S2313	15	12	0	3	100.00	80.00	0.89
AT90S8515	12	12	0	0	100.00	100.00	1.00
ATmega169 ATmega169V	12	11	1	1	91.67	91.67	0.92
ATtiny25/V ATtiny45/V ATtiny85/V	16	15	1	1	93.75	93.75	0.94
ATtiny24 ATtiny44 ATtiny84	18	18	0	0	100.00	100.00	1.00
ATmega103 ATmega103L	14	12	1	2	92.31	85.71	0.89
ATmega8 ATmega8L	10	8	1	2	88.89	80.00	0.84
ATmega128 ATmega128L	14	13	3	1	81.25	92.86	0.87
ATtiny13 ATtiny13V	17	15	0	2	100.00	88.24	0.94
ATmega48/V ATmega88/V ATmega168/V	33	28	1	5	96.55	84.85	0.90
Aggregate	161	144	8	17	94.74	89.44	0.92

against the ATtiny13 specification, we first extracted the rules from this specification. em-SPADE took the same rules file as input to perform bug detection test on the set of all ATtiny13 software. Therefore, we needed to vary the specification and the LLVM specific bitcode file of the microcontroller software for testing em-SPADE. We generated the LLVM specific bitcode file using the LLVM front-end tool *Clang*.

Table 7.3: Data about extracted read-write only rules from training specifications

Specification	Actual	Tool	FP	FN	P (%)	R (%)	F_1
AT90S2313	18	15	0	3	100.00	83.33	0.91
AT90S8515	16	13	0	3	100.00	81.25	0.90
ATmega169 ATmega169V	46	39	0	7	100.00	84.78	0.92
ATtiny25/V ATtiny45/V ATtiny85/V	29	27	1	2	96.43	93.10	0.95
ATtiny24 ATtiny44 ATtiny84	29	25	0	4	100.00	86.21	0.93
ATmega103 ATmega103L	21	14	2	7	87.50	66.66	0.76
ATmega8 ATmega8L	29	20	0	9	100.00	68.96	0.82
ATmega128 ATmega128L	30	23	0	7	100.00	76.67	0.87
ATtiny13 ATtiny13V	23	22	0	1	100.00	95.65	0.98
ATmega48/V ATmega88/V ATmega168/V	45	44	0	1	100.00	97.78	0.99
Aggregate	286	242	3	44	98.78	84.61	0.91

Table 7.4: Data about extracted reserved-bit rules from evaluation specifications

Specification	Actual	Tool	FP	FN	P (%)	R (%)	F_1
ATmega640/V ATmega1280/V ATmega1281/V ATmega2560/V ATmega2561/V	20	19	1	1	95.00	95.00	0.95
ATtiny4 ATtiny5 ATtiny9 ATtiny10	24	24	2	0	92.31	100.00	0.96
ATmega48PA ATmega88PA ATmega168PA ATmega328P	33	27	1	6	96.43	81.82	0.88
AT90S8535 AT90SL8535	17	16	0	1	100.00	94.12	0.97
ATtiny261/V ATtiny461/V ATtiny861/V	16	13	1	3	92.86	81.25	0.87
Aggregate	110	99	5	11	95.19	90.00	0.92

Table 7.5: Data about extracted write-read only rules from evaluation specifications

Specification	Actual	Tool	FP	FN	P (%)	R (%)	F_1
ATmega640/V ATmega1280/V ATmega1281/V ATmega2560/V ATmega2561/V	54	53	0	1	100.00	98.15	0.99
ATtiny4 ATtiny5 ATtiny9 ATtiny10	34	31	0	3	100.00	91.18	0.95
ATmega48PA ATmega88PA ATmega168PA ATmega328P	46	42	0	4	100.00	91.30	0.95
AT90S8535 AT90SL8535	23	18	0	5	100.00	78.26	0.88
ATtiny261/V ATtiny461/V ATtiny861/V	28	23	0	5	100.00	82.14	0.90
Aggregate	185	167	0	18	100.00	90.27	0.95

Chapter 8

Results

This section discusses the bugs, i.e., errors and warnings, that em-SPADE reported, and the rules that rule extractor of em-SPADE extracted from the AVR family of microcontroller specifications. In the first subsection, we provide a detail description of the errors and warnings that em-SPADE found for some application note projects and github projects.

8.1 Errors and Warnings Detected

em-SPADE found a total of 20 errors and warnings in ten projects. An overall summary of these bugs is available in Table 7.1. Table 7.1 lists four columns: (1) Project, (2) Total, (3) Reserved-Writes, and (4) RO-Writes. The first column lists the name of the project. The second column tells the total bugs (errors and warnings) found in the particular project. Third and fourth columns tell the number of Reserved-Writes and RO-Writes bugs found in the project respectively. An elaborate discussion on these two type of bugs is available as follows:

8.1.1 RO-Writes

em-SPADE found 16 RO-Writes type of bugs in eight projects which are application notes published by ATMEL. Although writing to read-only bits might not cause a program to fail, it is bad programming practice and can cause new bugs in future revisions. Therefore, we consider RO-Writes as bugs. These bugs correspond to three specifications, i.e., ATmega169, ATtiny13 and ATtiny24. In all these cases, specifications dictate that the

registers have read-only bits that are initialized with 0 but developers incorrectly write 1 to those register bits. The next two paragraphs provide two examples of RO-Writes bugs which em-SPADE found.

Assignment “TIFR1 = 0xFF;” in Main.c in AVR064 project sets all eight bits in TIFR1 register to one. Project AVR064 is intended for the ATmega169 microcontroller and the corresponding specification dictates that bits 7:6 and 4:3 in Timer/Counter1 Interrupt Flag Register (TIFR1) are read-only bits. Hence, setting bits 7:6 and 4:3 to one in TIFR1 register is a violation of the read-only rule and, therefore, the assignment is a bug.

Another example is the assignment “PORTB = 0xFF;” in WakeupTimer/main.c in AVR132. This assignment sets all eight bits in PORTB register to one. The project is intended for the ATtiny13 microcontroller. The ATtiny13 specification dictates that bits 7:6 in Port B Data Direction Register (PORTB) are read-only bits. Hence, setting bits 7:6 to one in PORTB register is a violation of the read-only rule and, therefore, the assignment is a bug.

8.1.2 Reserved-Writes

em-SPADE found one Reserved-Writes type of bug in Optiboot [21]. Optiboot is an optimized bootloader for Arduino [2], and is a quarter of the size of the default bootloader. It allows larger Arduino programs and makes Arduino programs upload faster. Therefore, it plays an important part as Arduino bootloader. Optiboot has two target MCUs, i.e., ATtiny84 [33] and ATmega168/V [30]. In both these specifications, bits 7:6 and 4:3 in Timer/Counter1 interrupt flag register (TIFR1) are reserved. However, `bynase.c` in Optiboot sets all these bits in TIFR1 register to one. This is a violation of the above mentioned reserved bit rule for ATtiny84 and ATmega168/V microcontrollers.

em-SPADE found three Reserved-Writes type of bugs in a library called `libpolulu0-avr` [18]. The Pololu AVR Library is a collection of support functions for programming AVR-based Pololu products or for using Pololu products with AVRs. It is designed for use with the free `avr-gcc` compiler. Most of the library can also be used together with the Arduino environment. This project targets the following microcontrollers—ATmega48pa [29], ATmega88pa [29], ATmega168pa [29], ATmega328p [29], ATmega48/V [30], ATmega88/V [30] and ATmega168/V [30].

For all these microcontrollers, bits 7:3 in Pin Change Interrupt Flag Register (PCIFR) are reserved. However, in two files in libpolulu project i.e., `PololuWheelEncoders.cpp` and `OrangutanPulseIn.cpp`, these bits are set to one as “PCICR = 0xFF;”. This is a violation of the reserved bits rule for all seven microcontrollers. Therefore, the mentioned

assignment is a bug for libpolulu-avr project. In these specifications, bits 7:6 and 4:3 in Timer/Counter1 interrupt flag register (TIFR1) are reserved. However, in OrangutanServos.cpp, the assignment “TIFR1 = 0xFF;” sets all the register bits to one which violates the requirement of reserved bits 7:6 and 4:3 in TIFR1 register. Therefore, this statement is also buggy.

The reported 20 bugs in Reserved-Writes and RO-Writes category span across ten AVR projects and 13 different AVR microcontrollers. It is evident that such bugs are prevalent in microcontrollers codes. Therefore, em-SPADE is useful in detecting register assignment bugs in microcontroller software.

8.2 Specification Analysis Results

Table 7.2 and 7.3 show the data about extracted rules for the ten specifications in the training set. Similarly, Table 7.4 and 7.5 show the data about extracted rules for the five specifications in the evaluation set. Table 7.2, 7.3, 7.4 and 7.5 list the same metrics for access and reserved-bits types of rules.

Reserved bit rules and read-write only rules are present separately in both tables. Each row in these tables starts with the specification name followed by data about reserved bit rules and read-write only rules. Within reserved bit rules and read-write only rules, the tables list seven entries. Within *reserved bit rules* and *read-write only rules* multicolumns, column “Actual” reports the number of manually extracted rules. Column “Tool” reports the number of correct rules that em-SPADE extracted. In the next two columns, the tables show the number of false positives (FP) and the number of false negatives (FN). The next two columns report precision (P) and recall (R) in percentage. The last column lists the F_1 score which is a collective measure of precision and recall. The range of F_1 score in the tables is from zero to one.

Table 7.2 and 7.3 show that the overall precision is 94.74% and 98.78% for reserved bit rules and the read-write only rules in the training set. Also, the overall recall is 89.44% and 84.61% for reserved bit rules and the read-write only rules in the training set. Table 7.4 and 7.5 show that the overall precision is 95.19% and 100.00% for reserved bit rules and read-write only rules in the evaluation set. And the overall recall is 90.00% and 90.27% for reserved bit rules and read-write only rules in the evaluation set.

The F_1 score of reserved bit rules is 0.92 for both training and evaluation set. The F_1 score of read-write only rules is 0.91 for the training set and 0.95 for the evaluation set. The F_1 score of higher than 0.9 for training and evaluation set indicates that the rule

Table 8.1: Summary of Frequent Itemset Mining Result

Itemsets	Support	Total Reported	TP	FP	FN	P (%)	R (%)	F_1
4	1	164	101	63	40	61.58	71.63	0.66
5	1	69	52	17	89	75.36	36.88	0.50
3	2	198	106	92	35	53.53	75.18	0.62
4	1.3	90	74	16	67	82.22	52.48	0.64
5	0.8	102	78	24	63	76.47	55.32	0.64

extractor of em-SPADE is accurate, precise, and effective. In addition, it indicates that the rule extractor works accurately for specifications outside of the training set.

Table 7.2, 7.3, 7.4 and 7.5 show the number of false positives and false negatives for rules extracted from all the specifications. The main reason attributed to both, the false positives and false negatives, is the failure of the heuristics in some cases. In majority of the observed cases, the heuristics fail due to conversion of PDF specifications to text form by `pdftotext`. While converting, `pdftotext` sometimes produces unordered lines or misaligned text for register description layouts. This type of incorrect conversion negatively affects the rule extractor heuristics, which results in false positives and false negatives. In the future, we can use advanced conversion tools or analyze the manufacturers’ source files of specifications to reduce false positives and false negatives.

8.3 Data Mining Results

We used frequent itemset mining to identify checkable rules from the set of modal verb sentences. We conducted experiments with different values of minimum support and minimum number of items in the itemset. The dataset contains modal verb sentences from three ATMEL AVR specifications mentioned in the previous section. We report the number of true positives, false positives, false negatives along with precision and recall. Table 8.1 presents these values for five sets of minimum support and minimum number of items in itemsets. Note that the three specifications contain a total of 141 checkable rules. In the table, the first column reports the ‘minimum number of items’ parameter for the frequent itemset mining algorithm, and the next column reports the ‘minimum support’ parameter. The next column presents the ‘total reported sentences based on the itemsets’. The next three columns report the true positives, false positives and false negatives. The remaining three columns report the metrics precision, recall and F_1 score.

We also present the grouping of sentences for five itemsets that contain four or five words. The five groupings are:

Itemset: must when disabled changing

All the sentences containing this itemset follow the first LTL template.

1. When changing the ACD bit, the analog comparator interrupt must be disabled by clearing the ACIE bit in ACSR. (ATmega169)
2. When changing the ACIS1/ACIS0 bits, the analog comparator interrupt must be disabled by clearing its interrupt enable bit in the ACSR register. (ATmega169)
3. Interrupts must be disabled when changing prescaler setting to make sure the write procedure is not interrupted. (ATmega169)
4. When changing the ACD bit the analog comparator interrupt must be disabled by clearing the ACIE bit in ACSR. (ATmega103)
5. When changing the ACIS1/ACIS0 bits, the analog comparator interrupt must be disabled by clearing its interrupt enable bit in the ACSR register. (ATmega103)
6. Interrupts must be disabled when changing prescaler setting to make sure the write procedure is not interrupted. (ATtiny13)
7. When changing the ACD bit, the analog comparator interrupt must be disabled by clearing the ACIE bit in ACSR. (ATtiny13)
8. When changing the ACIS1/ACIS0 bits, the analog comparator interrupt must be disabled by clearing its interrupt enable bit in the ACSR register. (ATtiny13)

Itemset: must when bit written

Again, all the sentences containing this itemset follow the first LTL template.

1. The SE bit must be written to logic one to make the MCU enter the sleep mode when the SLEEP instruction is executed. (ATmega169)
2. This bit must be set when the WDE bit is written to logic zero. (ATmega169)
3. The EEMWE bit must be set when the logical “1” is written to EEWE otherwise no EEPROM write takes place. (ATmega103)

4. When writing ADCSR, a logical “0” must be written to this bit. (ATmega103)
5. When address and data are correctly set up, the EEWE bit must be written to one to write the value into the EEPROM. (ATmega169)
6. When the correct address is set up in the EEAR register, the EERE bit must be written to a logic one to trigger the EEPROM read. (ATmega169)
7. For ensuring compatibility with future devices, this bit must be written to zero when TCCR1B is written. (ATmega169)
8. For compatibility with future devices, these bit must be written to zero when UBRRH is written. (ATmega169)
9. To ensure compatibility with future devices, this bit must be written to zero when ADCSRB is written. (ATmega169)
10. When the correct address is set up in the EEARL register, the EERE bit must be written to one to trigger the EEPROM read. (ATtiny13)
11. The SE bit must be written to logic one to make the MCU enter the sleep mode when the SLEEP instruction is executed. (ATtiny13)

Itemset: must bit written register

In the sentences containing this itemset, eight sentences follow the first LTL template, and two non-rule modal-verb sentences.

1. Consequently the high byte OCR1AH or OCR1BH must be written first for a full 16 bit register write operation. (ATmega103)
2. All interrupts are assigned individual enable bits which must be written logic one together with the global interrupt enable bit in the status register in order to enable the interrupt. (ATmega169)
3. When the correct address is set up in the EEAR register, the EERE bit must be written to a logic one to trigger the EEPROM read. (ATmega169)
4. In these cases the waveform generation mode (wgm13:0) bits must be set before the top value can be written to the ICR1 register. (ATmega169)

5. The PRSPI bit in “Power Reduction Register PRR” on page 34 must be written to zero to enable SPI module. (ATmega169)
6. The PRUSART0 bit in “Power Reduction Register PRR” on page 34 must be written to zero to enable USART module. (ATmega169)
7. The power reduction ADC bit PRADC in “Power Reduction Register PRR” on page 34 must be written to zero to enable the ADC module. (ATmega169)
8. The PRLCD bit in “Power Reduction Register PRR” on page 34 must be written to zero to enable the LCD module. (ATmega169)
9. All interrupts are assigned individual enable bits which must be written logic one together with the global interrupt enable bit in the status register in order to enable the interrupt. (ATtiny13)
10. When the correct address is set up in the EEARL register, the EERE bit must be written to one to trigger the EEPROM read. (ATtiny13)

Itemset: must bit written one logic

Again, all the sentences containing this itemset follow the first LTL template.

1. All interrupts are assigned individual enable bits which must be written logic one together with the Global Interrupt Enable bit in the Status Register in order to enable the interrupt. (ATmega169)
2. The EEMPE bit must be written to one before a logical one is written to EEPE otherwise no EEPROM write takes place. (ATtiny13)
3. When the correct address is set up in the EEAR register, the EERE bit must be written to a logic one to trigger the EEPROM read. (ATmega169)
4. The CLKPCE bit must be written to logic one to enable change of the CLKPS bits. (ATmega169)
5. To enter any of the five sleep modes, the SE bit in SMCR must be written to logic one and a sleep instruction must be executed. (ATmega169)
6. The SE bit must be written to logic one to make the MCU enter the sleep mode when the SLEEP instruction is executed. (ATmega169)

7. The IVCE bit must be written to logic one to enable change of the IVSEL bit. (ATmega169)
8. All interrupts are assigned individual enable bits which must be written logic one together with the Global Interrupt Enable bit in the Status Register in order to enable the interrupt. (ATtiny13)
9. The CLKPCE bit must be written to logic one to enable change of the CLKPS bits. (ATtiny13)
10. To enter any of the three sleep modes the SE bit in MCUCR must be written to logic one and a SLEEP instruction must be executed. (ATtiny13)
11. The SE bit must be written to logic one to make the MCU enter the sleep mode when the SLEEP instruction is executed. (ATtiny13)
12. A logic one must be written to WDE regardless of the previous value of the WDE bit. (ATtiny13)

Itemset: must bit written enable

In the sentences containing this itemset, all follow the first LTL template.

1. All interrupts are assigned individual enable bits which must be written logic one together with the Global Interrupt Enable bit in the Status Register in order to enable the interrupt. (ATmega169)
2. The CLKPCE bit must be written to logic one to enable change of the CLKPS bits. (ATmega169)
3. The IVCE bit must be written to logic one to enable change of the IVSEL bit. (ATmega169)
4. The PRTIM1 bit in “Power Reduction Register PRR” on page 34 must be written to zero to enable timer/counter1 module. (ATmega169)
5. The PRSPI bit in “Power Reduction Register PRR” on page 34 must be written to zero to enable SPI module. (ATmega169)
6. The PRUSART0 bit in “Power Reduction Register PRR” on page 34 must be written to zero to enable USART module. (ATmega169)

7. The power reduction ADC bit PRADC in “Power Reduction Register PRR” on page 34 must be written to zero to enable the ADC module. (ATmega169)
8. The PRLCD bit in “Power Reduction Register PRR” on page 34 must be written to zero to enable the LCD module. (ATmega169)
9. All interrupts are assigned individual enable bits which must be written logic one together with the Global Interrupt Enable bit in the Status Register in order to enable the interrupt. (ATtiny13)
10. The CLKPCE bit must be written to logic one to enable change of the CLKPS bits. (ATtiny13)

Chapter 9

Performance

We discuss the performance of em-SPADE in terms of overhead caused by the LLVM pass and overhead caused by the rule extractor. We also discuss the scalability of em-SPADE with respect to large concatenated specifications.

9.0.1 Rule Extractor Overhead

Overhead caused by the rule extractor of em-SPADE is not important because rule extraction is a one time task for each processor specification. Once em-SPADE extracts the rules from a particular specification, the LLVM checker can use the same rules file to detect bugs in any software intended for the processor. For each of the 15 specifications in the training and evaluation set, we measured the overhead caused by the rule extractor individually. From the data about the individual overhead for each specification, we calculated the mean overhead. The mean overhead is 4.41 seconds of CPU time which accounts for the amount of CPU time spent in user-mode and kernel mode within the rule extractor process. Note that the rule extractor process can be run individually to record its overhead.

9.0.2 LLVM Checker Overhead

To gather data about overhead produced by the LLVM pass implementation, we ran em-SPADE on four randomly chosen projects using rules from the 15 specifications individually. To calculate the overhead caused by the LLVM checker, we run the LLVM compilation step with and without the LLVM checker. The difference between the CPU time of compilation

with the LLVM checker and the CPU time of compilation without the LLVM checker accounts for the overhead caused by the LLVM checker. Based on the data from the 60 runs, we calculated the mean overhead caused by the LLVM checker. The mean overhead caused by the checker is 1.79 seconds of CPU time.

9.0.3 Scalability of em-SPADE

We tested the scalability of em-SPADE with respect to large specification. To test the scalability of the rule extractor, we combined 15 specs using pdftk [24] to get one large combined PDF file of 3857 pages. The rule extractor completed the extraction in 24.25 seconds which included 24.10 seconds of CPU time. The mean overhead caused by LLVM checker of em-SPADE in this case was 2.22 seconds of CPU time.

9.0.4 Frequent Itemset Mining Overhead

The apriori algorithm to perform frequent itemset mining needs to run for modal verb sentences in each specification. To get a sense of overhead caused by the apriori algorithm, we performed experiments on the three specifications. Since the run time of the apriori algorithm depends on parameters such as ‘support’ and ‘number of items in the itemset’, we conducted the experiments for a particular set of parameters. We set the values of support and number of items as 1% and 4. By conducting five runs of the apriori algorithm on each specification, we measured the CPU time for each run. We calculated the mean of all the 15 runs, and got a mean overhead of 0.017 seconds of CPU time.

Chapter 10

Discussion

In this section, we discuss four important points about em-SPADE which provide details about the limitation, effectiveness and generality of em-SPADE. In below subsections, we discuss the following specific points:

10.1 The Need to Modify the Source Code to Get LLVM Bitcode

As mentioned earlier, we have implemented the checker as a LLVM pass. Building the pass creates a shared object which the LLVM optimizer tool can load. The pass works on the LLVM specific binary bitcode file of the source code under inspection. em-SPADE needs to compile the source code using clang to get the LLVM binary. Clang is the front end for LLVM compiler infrastructure. Clang needs ‘emit-llvm’ option to generate the LLVM specific bitcode output. Most of the projects em-SPADE analyzed were for *avr-gcc* [3] compiler. *Avr-gcc* is a port of GCC which creates binaries for AVR [20] processors. To compile such source codes using clang, we manually need to make some changes such as adding the required header files in the code, providing the path to the include directory of avr library and commenting out a few lines if required. However, in doing so we make sure that none of the changes made put em-SPADE at an advantage in any way as far as finding errors and warnings are concerned.

10.2 False Positives & False Negatives

em-SPADE did not find any false positives while analyzing the embedded software projects. However, since the rule extractor reports false positives, it is probable that em-SPADE may report false positive bugs if the register corresponding to the false rule is assigned some value in the software.

Since the rule extractor is based on heuristics, em-SPADE does not guarantee that it extracts all the rules from specifications. Low recall, specially for ATmega103/ATmega103L and ATmega8/ATmega8L, in Table [1] suggests that em-SPADE misses some actual rules. Inspecting these specifications and the tool heuristics, we found that the limitation comes from `pdftotext` [25]. `Pdftotext` fails to preserve the register description layout in the text format which negatively affects the heuristics. Following the current line of work such as [1], [14], [19], [38] and [43], em-SPADE seeks a balance between false positives and false negatives.

10.3 Incorrect Data in Specifications

The underlying assumption in the context of em-SPADE is that specifications contain correct rules. If there is incorrect data in the specification, then em-SPADE might report false bugs or miss bugs. If developers reference the specification to develop a project, then em-SPADE will not report any bugs because of the consistency between the project code and specification, even though the data in specification is incorrect. However, if developers write projects with the help of their prior knowledge or experience about the device, then em-SPADE will report the bug caused by the inconsistency between project code and the specification. Since specifications act as standard reference guide for developers, it is reasonable to assume their correctness.

10.4 Generality of em-SPADE to other Specifications

Since the rule extractor in em-SPADE makes no specific assumption about ATMEL AVR specifications, em-SPADE should be generalizable to other type of specifications. The heuristics used to extract rules from specifications are applicable to other families of microcontrollers. Our study of NXP LPC17xx microcontrollers gives credence to this belief. Some example rules from these microcontrollers are present in Section 5. One can observe

that these rules are similar to the extracted rules from ATmega640/V [31] which have been listed earlier.

10.5 Practical Use of Data Mining Techniques

We have shown that the frequent itemset mining can be used to know whether a group of sentences contains rules. Such grouping can also help people standardize specifications. Sentences that have the same meaning can be written in a fixed and defined way without any ambiguity.

Chapter 11

Conclusion and Future Work

In this thesis, we propose a new approach to extract rules from processor specifications automatically and check source code against these rules to detect bugs in embedded systems automatically. We build the prototype em-SPADE, which automatically extracts 652 rules correctly from 15 specifications with precisions of 81.25–100.00% and recalls of 80.00–100.00%. em-SPADE detects 20 bugs in ten ATMEL and AVR software projects automatically, which demonstrates the effectiveness of the approach.

We also demonstrate the use of data mining techniques for learning about complex rules from processor specifications automatically. Our experiments with three AVR specifications using frequent itemset mining show that the learning provided closely matches with manually identified rule templates. Data mining techniques can also be used to standardize the processor specifications.

As part of future work, we can use em-SPADE to analyze specifications for processors from other manufacturers. The rules extracted from these specifications can be used to check consistency in corresponding programs. As mentioned earlier, our study of NXP LPC17xx specification demonstrates that em-SPADE would be applicable to other families of microprocessors with little or no modification. Conducting experiments with em-SPADE on other microprocessor specification would prove this explicitly.

In addition to this, the tool can be enhanced to extract information from other types of specifications such as ethernet chips, PCI bus, SCSI bus, SPI bus, SPI chips, UART bus, UART chips, etc. Rules extracted from such types of specifications will be useful for writing firmwares and drivers.

Additionally, the rule extractor can also be enhanced to extract other type of rules from processor specifications such as rules from timing diagrams and rules about electrical

properties of the processor. To further improve the precision and recall of the rule extractor, we can use advanced PDF-to-text conversion tools or analyze the manufacturers' source files of PDF specifications. In addition, we plan to port em-SPADE to gcc framework to avoid the issues of generating LLVM IR e.g., mapping of register names and corresponding macro values for generating IR. Another possible future extension is detecting assignment violations involving function calls.

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