A Low Jitter Analog Circuit for Precisely Correcting Timing Skews in Time-Interleaved Analog-to-Digital Converters

by

Adam Bray

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I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners

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Abstract

Time-interleaved analog-to-digital converters are an attractive architecture for achieving a high speed, high resolution ADC in a power efficient manner. However, due to process and manufacturing variations, timing skews occur between the sampling clocks of the sub ADCs within the TI-ADC. These timing skews compromise the spurious free dynamic range of the converter. In addition, jitter on the sampling clocks, degrades the signal-to-noise ratio of the TI-ADC. Therefore, in order to maintain an acceptable spurious free dynamic range and signal-to-noise ratio, it is necessary to correct the timing skews while adding minimal jitter.

Two analog-based architectures for correcting timing skews were investigated, with one being selected for implementation. The selected architecture and additional test circuitry were designed and fabricated in a 0.18µm CMOS process and tested using a 125 MSPS 16-bit ADC. The circuit achieves a correction precision on the order of 10's of femtoseconds for timing skews as large as approximately 180 picoseconds, while adding less than 200 femtoseconds of rms jitter.

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Chapter 1

Introduction

Speed, magnitude and efficiency; for better or for worse, the world demands that the boundaries be pushed for how fast, how many and how efficiently things can be done. Within the realm of analog-to-digital converters (ADCs) this means pushing the boundaries to obtain: higher analog input bandwidths (to handle RF carrier frequencies), faster sample rates (to accommodate wider bandwidths), higher resolutions (to meet the linearity requirements of the advanced coding schemes) and an energy efficient architecture. One technique that is used to help ADCs achieve these requirements is time-interleaving [1].

The theory and operational details behind time interleaving and time-interleaved analog-to-digital converters (TI-ADCs) is left to Chapter 2 to be discussed. For now the technique of time-interleaving can be viewed as paralleling multiple ADCs, not unlike the trend in microprocessors to use multiple cores to accomplish processing tasks. Like multi-core processors, the idea and necessity behind using TI-ADCs is that it is more energy efficient and practical (in terms of heat dissipation) to use multiple, slower, high resolution ADCs in parallel than to design a single very high speed, high resolution ADC [1]. However, implementing a

TI-ADC such that it achieves all of the previously mentioned requirements is non-trivial.

One challenging aspect of implementing a TI-ADC is achieving the correct clock timing between each of the sub ADCs within the TI-ADC [1]. If there is a skew in the clock timing, here-in referred to as timing skew, of one or more of the interleaved ADCs then the resolution of the TI-ADC will be degraded in proportion to the magnitude of the skew relative to the other interleaved ADCs and the frequency of the input signal to the TI-ADC [1]. Correcting the timing skews requires adjustment of the clocks (analog domain) or the digital output data (digital domain) to an accuracy and precision on the order of femtoseconds or better [1]. In addition the method of correction is required to add as little jitter to the clock as possible in order to minimize the impact on the TI-ADC's noise performance [1]. This thesis presents an option to address the challenge and requirements of correcting timing skews in TI-ADCs. It details the design and implementation of a low jitter analog circuit/method which can correct timing skews to the femtosecond level.

1.1 Thesis Outline

This thesis is divided into 5 main chapters dealing with the background theory, potential architectures, design and implementation, measured results and the major conclusions. Chapter 2 presents relevant background concepts on ADCs and TI-ADCs as well as the pertinent performance specifications. In addition the theory on timing skews and their impact on the TI-ADCs performance specifications are presented as well as the performance impact of clock jitter on ADCs. Lastly, Chapter 2 concludes with a definition of the performance requirements for a timing skew correction system/circuit. Chapter 3 begins with a comparison of analog and digital methods of correcting timing skew. It then presents analog circuit techniques that can be used to adjust the timing skew of a clock. Chapter 3 then continues by

comparing two circuit architectures that can introduce timing skews and their relative performance in terms of jitter and precision. Lastly, Chapter 3 concludes with a recommendation for which circuit structure to implement and the necessary system-level architecture in order to test the structure's performance. Chapter 4 presents the design, layout and fabrication of the various circuits required to implement the system described in Chapter 3 in TSMC's 0.18µm CMOS. Chapter 5 discusses the implementation details of the fabricated chip, including the accompanying printed circuit board (PCB) design and test setup details. In addition the measured results of the fabricated chip are presented, with relevant comparisons to post-layout simulations. Finally, Chapter 6 presents the major conclusions within the thesis as well as future considerations and directions for this research.

Chapter 2

Time-Interleaved Analog-to-Digital Converters

As discussed in Chapter 1, time-interleaving is one technique that can be used to increase the sample rate of an ADC without requiring excessive power dissipation [1]. However, issues arise when designing TI-ADCs beyond those already present in the design of a typical ADC. The issue that this thesis focuses on is timing skews. In order to understand the impact and source of timing skews in a TI-ADC, it is useful to understand the concepts surrounding a TI-ADCs operation and the ADC performance metrics the timing skews affect. It is important to note that although the focus is on timing skews, other issues that can impact or limit the ability to measure or correct timing skews are covered as well.

This chapter begins with an overview of how the performance of an ADC is measured and a description of the fundamental performance metrics and limits that are useful when evaluating a TI-ADC's operation subject to timing skews. Next, the basic operation of a TI-ADC is shown along with an explanation of timing skews and other related issues that occur when the operation is non-ideal. The issue of timing skews is then expanded on with a mathematical analysis showing their impact and the

degree to which timing skews need to be corrected. After this, the concept of jitter is presented, along with the desired limits to which jitter needs to be controlled. Lastly, a summary of the desired performance for a system to correct timing skews is discussed, setting two of the key design goals of this thesis.

2.1 ADC Concepts

The important ADC concepts, beyond those dealing with the operation of the ADC, have to do with understanding the performance specifications and the fundamental limits of an ADC. In most cases the performance specifications of an ADC are measured using a single-tone sinusoidal input, which can be represented as:

$$V_{IN} = \frac{V_{FS}}{2}\cos(2\pi F_{IN} t) \tag{2.1}$$

where V_{FS} is the full-scale input voltage and F_{IN} is the frequency of the sinusoidal tone. Note that within this thesis, unless otherwise noted, when there is an input to an ADC or TI-ADC it is assumed to be a single-tone represented by Equation (2.1). For evaluation purposes, the digital output of the ADC is converted to the frequency domain via a Fast Fourier Transform (FFT). The performance specifications can then be measured and/or calculated from the FFT plot. In short, the FFT converts a discretized (digital) signal of a specific length, L, into a magnitude versus frequency spectrum which contains $L/2$ discrete frequency bins, each spaced apart by F_{SAMPLE}/L, over a bandwidth of $DC \rightarrow F_{SAMPLE}/2$, where F_{SAMPLE} is the sampling frequency. One very important assumption buried within the FFT operation is that the discretized signal is sampled uniformly, meaning all the samples have exactly the same spacing in time between one another. Knowledge of this assumption is important when analyzing timing skews in TI-ADCs, as is shown in Section 2.3.

2.1.1 Sampling Rate, Aliasing and Analog Input Bandwidth

As previously mentioned, F_{SAMPLE} is the frequency the analog input signal to an ADC is sampled at. Alternatively, this frequency is commonly referred to as the sample rate of the ADC and is usually expressed as the number of samples per second (SPS). The sample rate sets the limit for the widest bandwidth, F_{BW}, the ADC can accurately convert, which is determined by the Nyquist rate as:

$$F_{BW} < \frac{F_{SAMPLE}}{2} \tag{2.2}$$

However, it is very important to note that this is not the limit for the highest frequency the ADC can convert, which is roughly determined by the ADC's analog input bandwidth [2].

Knowing that the FFT only recognizes frequencies between DC and $F_{SAMPLE}/2$, aliasing together with Nyquist zones describe how a frequency higher than $F_{SAMPLE}/2$ is represented in an FFT plot. Aliasing is the phenomenon of a higher than Nyquist rate signal being reflected back to the $(DC \rightarrow F_{SAMPLE}/2)$ range or first Nyquist zone. A Nyquist zone is a region of width $F_{SAMPLE}/2$, whose zone number and frequency range is determined by [2]:

$$i^{th} Nyquist\ Zone = \frac{(i-1)F_{SAMPLE}}{2} \rightarrow \frac{iF_{SAMPLE}}{2} \tag{2.3}$$

$$i = 1, 2, 3, \ldots \infty$$

The Nyquist zone in which the input frequency falls, determines the frequency of the reflected (aliased) signal, F_{ALIAS} and is given by:

$$Odd\ Nyquist\ Zone: F_{ALIAS} = F_{IN} - \frac{(i-1)F_{SAMPLE}}{2}$$
$$i = 1, 3, 5, \ldots \infty \tag{2.4}$$

$$Even\ Nyquist\ Zone: F_{ALIAS} = \frac{iF_{SAMPLE}}{2} - F_{IN}$$
$$i = 2, 4, 6, \ldots \infty \tag{2.5}$$

To illustrate how all of these concepts tie together, Figure 2.1 shows an ideal FFT plot over 5 Nyquist zones of two discrete signals and their aliases along with an overlay of a typical analog bandwidth profile. For simplicity, the images that also appear with aliasing are ignored.

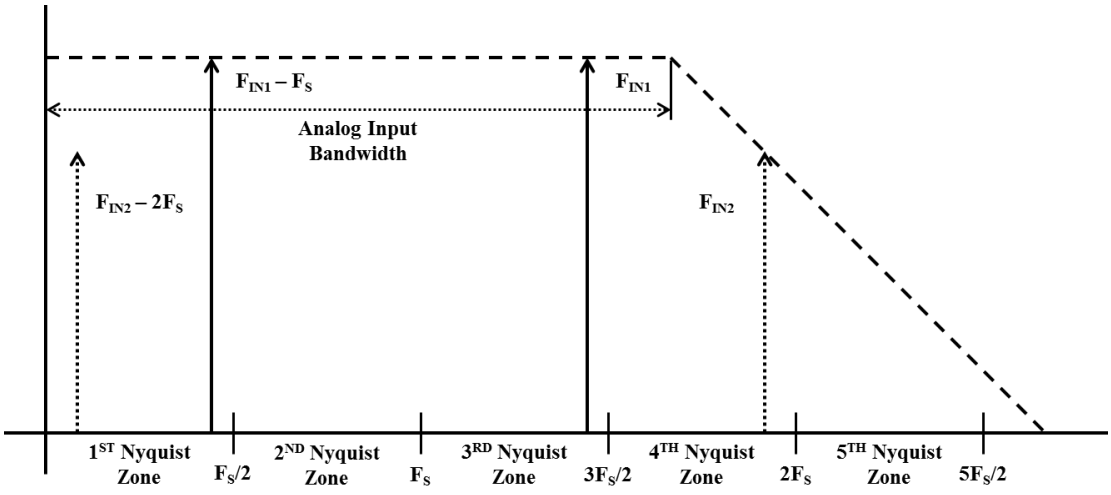


Figure 2.1: Ideal FFT Illustrating Aliasing and Analog Input Bandwidth

2.1.2 Resolution and Quantization Noise

The resolution of an ADC indicates the ideal number of distinct levels the analog input signal to the ADC can be discretized to. It is usually expressed in terms of the number of bits, N, that are required to represent the binary number of discrete levels, 2^N. Due to the finite number of levels an ADC can represent, an error will typically exist between the actual sampled analog signal level and the discrete level the ADC uses to represent it. Provided certain conditions are met, this error is random and is commonly referred to as quantization noise. Mathematically the magnitude of the quantization noise can be expressed as [2]:

$$V_{QNOISE} = \frac{V_{FS}}{2^N\sqrt{12}} \tag{2.6}$$

where V_{QNOISE} is the root mean squared (rms) noise voltage due to quantization. Note that V_{QNOISE} is the total quantization noise and it is spread uniformly over the first Nyquist zone ($DC \rightarrow F_{SAMPLE}/2$).

The value, V_{QNOISE}, is commonly used as a limit or level to which non-ideal behaviours in ADCs should be kept below and one that is used in later sections to set the desired degree to which to correct timing skews and limit jitter.

2.1.3 Signal-to-Noise Ratio

The signal-to-noise ratio (SNR) of an ADC is typically defined as the ratio between the input signal's rms amplitude and the rms value of the sum of all other frequencies within the first Nyquist zone, excluding harmonics of the input and DC [2]. If the only noise present in the ADC is due to the quantization noise given by (2.6) then the SNR is:

$$SNR = \frac{\frac{V_{FS}}{2\sqrt{2}}}{\frac{V_{FS}}{2^N\sqrt{12}}} \tag{2.7}$$

More commonly, Equation (2.7) is expressed in decibels (dB) as:

$$SNR = 6.02N + 1.76\ dB \tag{2.8}$$

Note that this is the best possible SNR for an ADC and in reality, it is degraded by many additional noise sources, one of which, as is shown in Section 2.4, is jitter. However, when an FFT plot of the output of the ADC is produced, the apparent SNR is often much better than the level predicted by (2.8).

The FFT conversion process takes the total noise in the discretized input signal and divides it uniformly, assuming the noise is random, among the frequency bins in the first Nyquist zone. This spreading of the noise appears as a decrease in the SNR of the ADC (processing gain), where the improvement in the SNR, in dB, is given by [2]:

$$10\log_{10}\left(\frac{L}{2}\right) \tag{2.9}$$

Adding this to (2.8) gives the output SNR for an *N*-bit ADC, viewed by an L point FFT as:

$$SNR = 6.02N + 1.76\,dB + 10\log_{10}\left(\frac{L}{2}\right) \tag{2.10}$$

Figure 2.2 illustrates the different SNR's with an $L = 32{,}768$ point FFT plot of an $N = 16$ ADC with only quantization noise, sampling an input with a $F_{IN} = 110\ MHz$[1] at a rate $F_{SAMPLE} = 125\ MHz$.

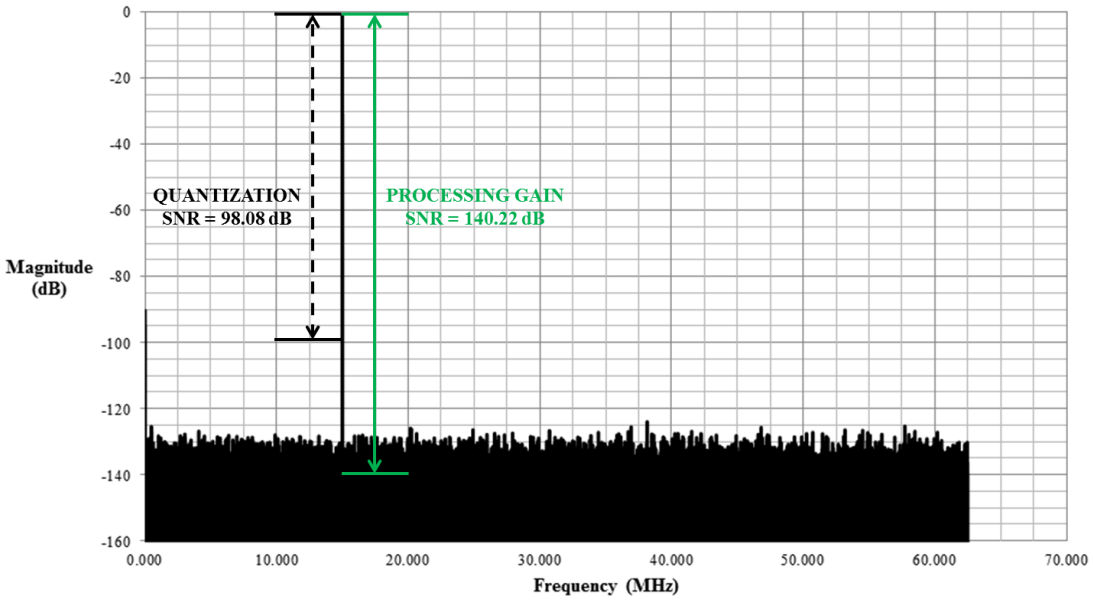


Figure 2.2: FFT Plot Illustrating Various SNR Calculations for a $F_{IN} = 110\ MHz$ and $F_{SAMPLE} = 125\ MHz$

[1] The actual coherent frequency used is 110.00442553 MHz

2.1.4 Spurious Free Dynamic Range

A spurious tone is a distinct frequency that is generated from non-idealities within an ADC or TI-ADC as they sample a signal. Spurious tones (spurs) are almost always undesirable as they can interfere in trying to resolve the sampled input signal. An important performance specification for ADCs that measures how bad the worst spurious tone is in the ADC is the spurious free dynamic range (SFDR). It is usually defined as the ratio between the magnitude of the input sinusoid and the magnitude of the largest spurious tone V_{SPUR}, as seen on an FFT plot:

$$SFDR = \frac{|V_{IN}|}{|V_{SPUR}|} \tag{2.11}$$

In Section 2.3, it is shown that TI-ADCs subject to timing skews, give rise to spurious tones. For the purpose of this thesis, unless otherwise noted, SFDR is the ratio between the magnitude of the input and the magnitude of the timing skew spurious tone $V_{\Delta SKEW}$:

$$SFDR = \frac{|V_{IN}|}{|V_{\Delta TSKEW}|} \tag{2.12}$$

Figure 2.3 illustrates this definition of the SFDR for two different magnitudes of timing skew spurious tones.

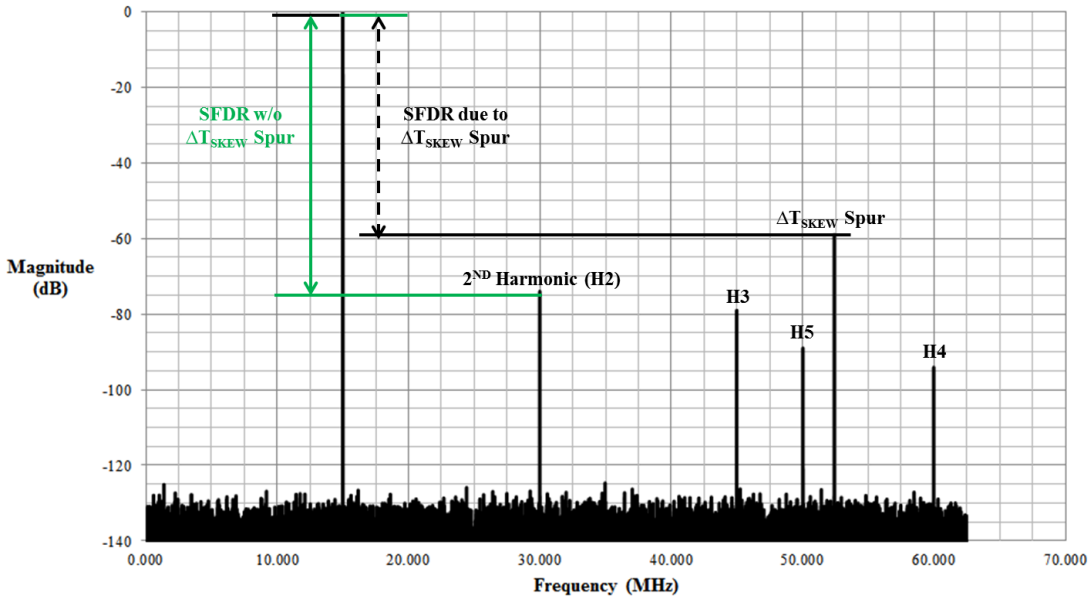


Figure 2.3: SFDR as Defined by Two Different Spur Magnitudes

It is important to note that the SFDR provides a direct measurement for characterizing timing skews in TI-ADCs.

2.2 TI-ADC Concepts

A TI-ADC is composed of M sub ADCs whose inputs and outputs are clocked at a rate of F_{CLOCK} or $1/T_{CLOCK}$. Each of the sub ADCs clocks are precisely shifted relative to one another, such that only one of the sub ADCs at a time samples the input signal and outputs a digital code. The shifts for each of the clocks are derived from a master clock whose rate $F_{SAMPLE}(1/T_{SAMPLE})$ is given by:

$$F_{SAMPLE} = MF_{CLOCK} \tag{2.13}$$

which sets the overall sample rate of the TI-ADC [1]. In other words, if an ADC with a sample rate of F_{CLOCK} is time-interleaved M times, the overall sample rate F_{SAMPLE} of the formed TI-ADC has increased by M times compared to the sub ADCs sample rate. An example of an $M = 4$ TI-ADC, with the corresponding clocking scheme, is shown in Figure 2.4.

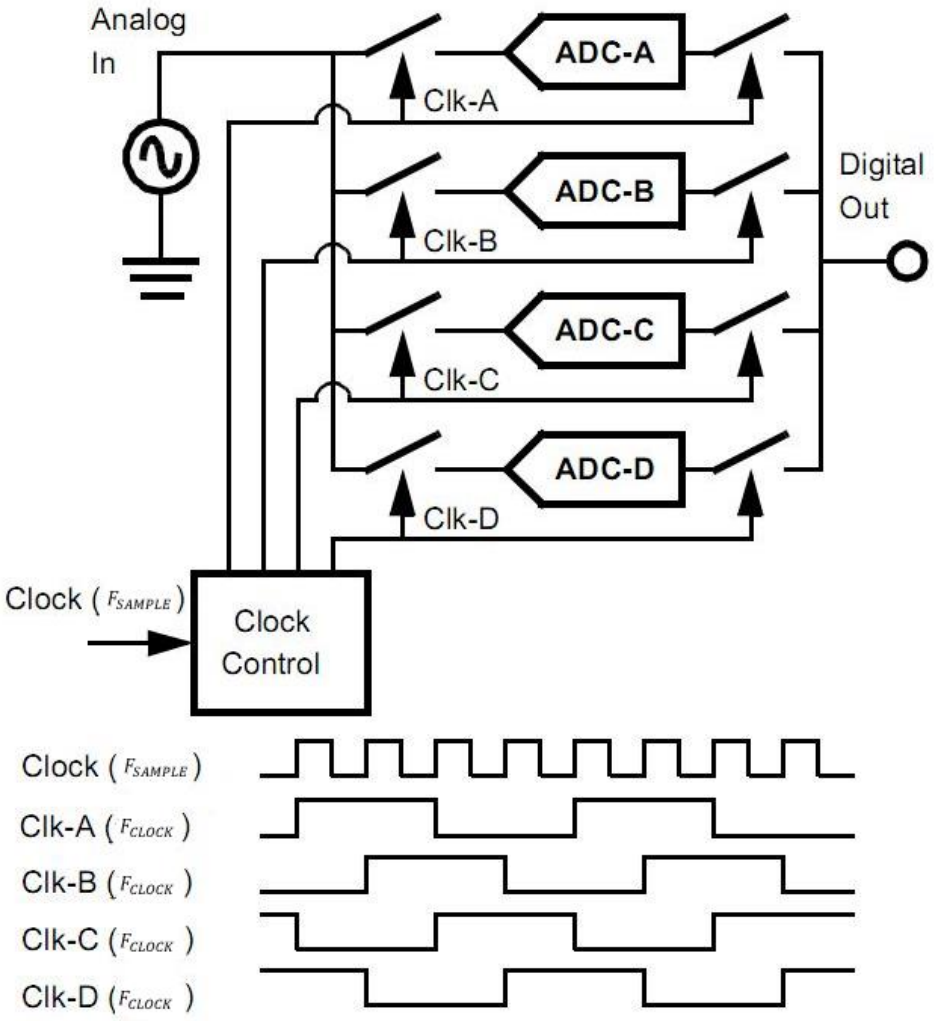


Figure 2.4: 4-Way TI-ADC System with Clocking [1]

It should be noted that each of the digital codes output by the sub ADCs are combined to form the complete digital representation of the sampled signal.

Two important implementation details are assumed in the above theory. The first is that each of the sub ADCs has an analog input bandwidth equal to or greater than $F_{SAMPLE}/2$ such that it can sample a Nyquist rate signal (i.e. $DC \rightarrow F_{SAMPLE}/2$). The second assumption is that everything is ideal, as in each of the sub ADCs are identical and the clocks have perfect relative timing to one another such that they can sample a signal uniformly. In reality, things are non-ideal and mismatches occur between the sub ADCs and the timings of each of the clocks are skewed from their ideal positions.

2.2.1 Mismatches

A mismatch in this thesis refers to the variation in a designed operating parameter between each of the sub ADCs within the TI-ADC. Mismatches in the offset, gain and clock timing (timing skews) are usually the most problematic for TI-ADCs, however bandwidth and linearity mismatches also pose problems [1]. A brief discussion of offset, gain and bandwidth mismatches is presented below. A detailed discussion of timing skews is left to Section 2.3.

Mismatches in the offsets between the sub ADCs of a TI-ADC spawn spurious tones. The frequencies of these tones F_{Vos} are given by [1]:

$$F_{Vos} = \frac{iF_{SAMPLE}}{M}$$

$$i = 0, 1, \ldots M - 1 \tag{2.14}$$

These offset induced tones can interfere with the spurious tones produced as a result of gain and timing skews. For example, as will be shown later, in a 4-way TI-ADC with $F_{IN} = F_{SAMPLE}/4$, the spurious tones due to offset, gain and timing skew mismatches all overlap. However, with careful selection of F_{IN}, the use of a 2-way TI-ADC or the correction and/or elimination of the possibility of the offset mismatches, the spurious tones induced only due to timing skews can be isolated.

Gain mismatches between each of the sub ADCs result in spurious tones whose frequencies $F_{\Delta A}$ are given by [1]:

$$F_{\Delta A} = \frac{iF_{SAMPLE}}{M} \pm F_{IN}$$

$$i = 1, 2, \ldots M - 1 \tag{2.15}$$

Unfortunately, the frequencies of these tones are not exclusive to gain mismatches. It will be shown in the next section that timing skews also result in spurious tones whose frequencies are given by (2.15). When trying to characterize, measure and/or correct timing skews, all of which are of vital importance to this thesis, it is critical to have the ability to correct or eliminate the possibility of gain mismatches. This ensures that the observed spurious tones in the output of the TI-ADC under consideration are only due to the timing skews themselves and not the combination of gain and timing skew mismatches.

Finally, bandwidth mismatches between the sub ADCs result in both gain mismatches and timing skews producing spurious tones at frequencies given by (2.15). However, in the bandwidth mismatch case, the magnitude of the gain and timing skew tones depend non-linearly on the input frequency F_{IN} [3]. Once again, care must be taken to correct or remove the possibility of bandwidth mismatches if analysis of only timing skews in TI-ADCs is the goal. A testing architecture that does this is presented in Chapter 3.

2.3 Timing Skews

Clock timing mismatches or more commonly, timing skews, pose one of the biggest challenges for TI-ADCs. To explain what timing skews are, it is useful to refer back to the clocking diagram in Figure 2.4. Each of the clocks for the sub ADCs are shifted with respect to one other by exactly $1/MF_{CLOCK}$, such that the rising edge of each clock, the edge that an ADC samples on, does not overlap with any of the others. This allows only one sub ADC to sample at a time. For a $M = 2$ TI-ADC, this can be mathematically expressed as:

$$T_2 - T_1 = \frac{1}{MF_{CLOCK}} \tag{2.16}$$

where T_1 and T_2 are the times consecutive samples are taken by the first and second sub ADCs respectively. Based on this, a timing skew ΔT_{SKEW}exists if $T_2 - T_1 \neq 1/MF_{CLOCK}$ which is defined as:

$$\Delta T_{SKEW} = \left|(T_2 - T_1) - \frac{1}{MF_{CLOCK}}\right| \tag{2.17}$$

Once a TI-ADC is manufactured there are 3 main components that can contribute to ΔT_{SKEW}; fixed timing shifts between the sub ADCs due to design and process variations, drifts in timing between sub ADCs due to aging and random noise or jitter on each of the sub ADCs clocks'. Note that in general, timing skews can exist between each sub ADC within the TI-ADC.

Timing skews are problematic because they shift the times at which each of the sub ADCs sample the input, which causes non-uniform sampling of the input signal [4]. An illustration of a timing skew in an $M = 2$ TI-ADC and its impact on the sampling of a sine wave is shown in Figure 2.5. The blue waveform/points are the ideal sampled sine wave, which can also be thought of as the average between the red and green points. The red waveform/point corresponds to sub ADC 'A' sampling later in time than it should, whereas the green waveform is sub ADC 'A' sampling sooner in time than it should.

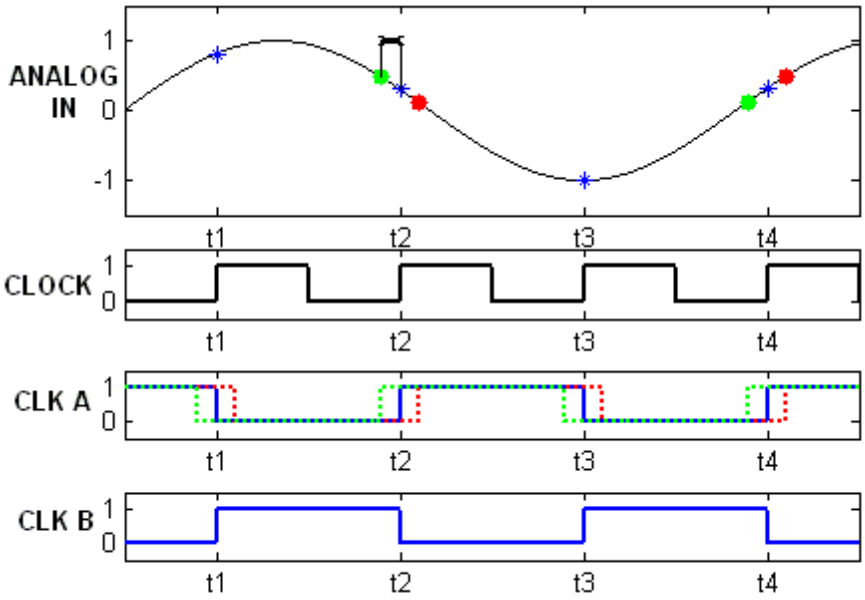


Figure 2.5: Time-Domain Plot of an Ideal and Timing Skewed Sampled Sine Waves

2.3.1 Analysis

A full frequency domain analysis of non-uniform sampling, which can be thought of as timing skews being applied to a uniformly sampled signal, is performed in [4]. This thesis analyzes timing skews in an alternative, time-domain based way, yielding similar results as [4]. To simplify the analysis and to match the test architecture used to evaluate the circuit designed in this thesis, an $M = 2$ TI-ADC case is presented where the timing skew between the two sub ADCs is ΔT_{SKEW}. Note that for an $M = 2$ case, the SFDR is the worst for a given ΔT_{SKEW} and the difference between the SNR for an $M = 2$ case and the $M = \infty$ case is only 3 dB, with typical practical values being $M \leq 8$, however very large scale integration (VLSI) makes larger values of M practical [4].

Referring back to Figure 2.5, it shows that the non-uniform sampling of a sine wave appears like two sine waves that are uniformly sampled and shifted with respect to one another by the amount $2\pi F_{IN}\Delta T_{SKEW}$. Alternatively, the shift can be viewed with respect to the input sine wave by $+2\pi F_{IN}(\Delta T_{SKEW}/2)$ for the red wave and $-2\pi F_{IN}(\Delta T_{SKEW}/2)$ for the blue wave. These two sine waves can then be thought of as inputs to two sub ADCs which exhibit no timing skew, since the sine waves themselves now capture the timing skew. One sine wave is applied to the first sub ADC and the other to the second, where the sine waves can be mathematically expressed using (2.1) as:

$$V_{IN1} = \frac{V_{FS}}{2}\cos\left(2\pi F_{IN}t + 2\pi F_{IN}\frac{\Delta T_{SKEW}}{2}\right) \tag{2.18}$$

$$V_{IN2} = \frac{V_{FS}}{2}\cos\left(2\pi F_{IN}t - 2\pi F_{IN}\frac{\Delta T_{SKEW}}{2}\right) \tag{2.19}$$

When the outputs of the two interleaved ADCs are combined, the overall output contains two terms, an average of the two inputs and an error term as explained in [5]. Taking the average of the two input terms yields:

$$V_{OUTAVG} = \frac{1}{2}\left(\begin{array}{c}\frac{V_{FS}}{2}\cos\left(2\pi F_{IN}t + 2\pi F_{IN}\frac{\Delta T_{SKEW}}{2}\right)\\ +\frac{V_{FS}}{2}\cos\left(2\pi F_{IN}t - 2\pi F_{IN}\frac{\Delta T_{SKEW}}{2}\right)\end{array}\right) \tag{2.20}$$

Simplifying (2.20) gives:

$$V_{OUTAVG} = \frac{V_{FS}}{4}\left(\begin{array}{c}\cos\left(2\pi F_{IN}t + 2\pi F_{IN}\frac{\Delta T_{SKEW}}{2}\right)\\ +\cos\left(2\pi F_{IN}t - 2\pi F_{IN}\frac{\Delta T_{SKEW}}{2}\right)\end{array}\right) \tag{2.21}$$

Equation (2.21) can be further simplified by using the cosine identity $\cos(a \pm b) = \cos(a)\cos(b) \mp \sin(a)\sin(b)$ to give:

$$V_{OUTAVG} = \frac{V_{FS}}{4}\left(\begin{array}{c}\cos(2\pi F_{IN}t)\cos\left(2\pi F_{IN}\frac{\Delta T_{SKEW}}{2}\right)\\ -\sin(2\pi F_{IN}t)\sin\left(2\pi F_{IN}\frac{\Delta T_{SKEW}}{2}\right)\\ +\cos(2\pi F_{IN}t)\cos\left(2\pi F_{IN}\frac{\Delta T_{SKEW}}{2}\right)\\ +\sin(2\pi F_{IN}t)\sin\left(2\pi F_{IN}\frac{\Delta T_{SKEW}}{2}\right)\end{array}\right) \tag{2.22}$$

which, when reduced to its most compact form, results in:

$$V_{OUTAVG} = \frac{V_{FS}}{2}\left(\cos(2\pi F_{IN} t)\cos\left(2\pi F_{IN}\frac{\Delta T_{SKEW}}{2}\right)\right) \tag{2.23}$$

According to (2.23) ΔT_{SKEW} affects the amplitude of the signal, however given that timing skews are usually on the order of picoseconds at most which result in a negligible change in amplitude, (2.23) can be further reduced using the small-angle approximation of $\cos(x) = 1$ for small x, yielding:

$$V_{OUTAVG} = \frac{V_{FS}}{2}\cos(2\pi F_{IN} t) = V_{IN} \tag{2.24}$$

Note that this is the ideal sampled input from (2.1), which shows that the desired input does appear in the output of a TI-ADC subject to timing skews.

Dealing now with the error term, it appears in the output as a consequence of the difference between the sine waves that each sub ADC sees and the interleaving process. As the interleaving process grabs one sample from one sub ADC and next from the other sub ADC, the interleaved output samples appear to oscillate back and forth. This oscillation can be represented by a series of alternating magnitude impulses, i.e. $(1, -1, 1, -1 \ldots)$, with a frequency of $F_{SAMPLE}/2$ [5]. The impulses modulate the difference between the two sine waves. Given this, the error term, $V_{OUTERROR}$ can be expressed as follows:

$$V_{OUTERROR} = V_{ERROR}\sin\left(2\pi\frac{F_{SAMPLE}}{2}t\right) \tag{2.25}$$

V_{ERROR} is obtained by taking the difference between the sine waves, (2.18) and (2.19) yielding:

$$V_{ERROR} = \frac{V_{FS}}{2}\begin{pmatrix} \cos\left(2\pi F_{IN}t + 2\pi F_{IN}\frac{\Delta T_{SKEW}}{2}\right) \\ -\cos\left(2\pi F_{IN}t - 2\pi F_{IN}\frac{\Delta T_{SKEW}}{2}\right) \end{pmatrix} \quad (2.26)$$

Once again using the cosine identity to simplify results in:

$$V_{ERROR} = \frac{V_{FS}}{2}\begin{pmatrix} \cos(2\pi F_{IN}t)\cos\left(2\pi F_{IN}\frac{\Delta T_{SKEW}}{2}\right) \\ -\sin(2\pi F_{IN}t)\sin\left(2\pi F_{IN}\frac{\Delta T_{SKEW}}{2}\right) \\ -\cos(2\pi F_{IN}t)\cos\left(2\pi F_{IN}\frac{\Delta T_{SKEW}}{2}\right) \\ -\sin(2\pi F_{IN}t)\sin\left(2\pi F_{IN}\frac{\Delta T_{SKEW}}{2}\right) \end{pmatrix} \quad (2.27)$$

Combining terms reduces (2.27) to:

$$V_{ERROR} = -V_{FS}\sin(2\pi F_{IN}t)\sin\left(2\pi F_{IN}\frac{\Delta T_{SKEW}}{2}\right) \quad (2.28)$$

Substituting (2.28) into (2.25) gives:

$$V_{OUTERROR} = -V_{FS}\sin\left(2\pi F_{IN}\frac{\Delta T_{SKEW}}{2}\right)\sin(2\pi F_{IN}t)\sin\left(2\pi\frac{F_{SAMPLE}}{2}t\right) \quad (2.29)$$

Equation (2.29) shows the amplitude modulation, $K\sin(at)\sin(bt)$, that occurs due to the interleaving impulses. Using the sine identity $\sin(a)\sin(b) = \frac{1}{2}(\cos(a-b) - \cos(a+b))$ on (2.29) results in:

$$V_{ERROR} = \frac{-V_{FS}}{2}\sin\left(2\pi F_{IN}\frac{\Delta T_{SKEW}}{2}\right)\begin{pmatrix}\cos\left(2\pi F_{IN}t - 2\pi\frac{F_{SAMPLE}}{2}t\right)\\ -\cos\left(2\pi F_{IN}t + 2\pi\frac{F_{SAMPLE}}{2}t\right)\end{pmatrix} \quad (2.30)$$

Rearranging the arguments of the two cosine terms:

$$V_{ERROR} = \frac{-V_{FS}}{2}\sin\left(2\pi F_{IN}\frac{\Delta T_{SKEW}}{2}\right)\begin{pmatrix}\cos\left(2\pi\left(F_{IN} - \frac{F_{SAMPLE}}{2}\right)t\right)\\ -\cos\left(2\pi\left(F_{IN} + \frac{F_{SAMPLE}}{2}\right)t\right)\end{pmatrix} \quad (2.31)$$

The total output is given by the sum of (2.23) and (2.31):

$$V_{OUT} = \frac{V_{FS}}{2}\begin{pmatrix}\cos\left(2\pi F_{IN}\frac{\Delta T_{SKEW}}{2}\right)\cos(2\pi F_{IN}t)\\ -\left(\sin\left(2\pi F_{IN}\frac{\Delta T_{SKEW}}{2}\right)\begin{pmatrix}\cos\left(2\pi\left(F_{IN}-\frac{F_{SAMPLE}}{2}\right)t\right)\\ -\cos\left(2\pi\left(F_{IN}+\frac{F_{SAMPLE}}{2}\right)t\right)\end{pmatrix}\right)\end{pmatrix} \quad (2.32)$$

Equation (2.32) shows that for an $M = 2$ TI-ADC with a timing skew ΔT_{SKEW} between the two sub ADCs clocks there are three tones that appear in the output. The first tone is the desired sampled input tone with a magnitude of:

$$|V_{IN}| = \frac{V_{FS}}{2}\cos\left(2\pi F_{IN}\frac{\Delta T_{SKEW}}{2}\right) \quad (2.33)$$

The two other tones are spurious tones, generated by the timing skew with magnitudes of:

$$|V_{\Delta TSKEW}| = \frac{V_{FS}}{2} \sin\left(2\pi F_{IN} \frac{\Delta T_{SKEW}}{2}\right) \tag{2.34}$$

and frequencies of:

$$F_{\Delta TSKEW} = F_{IN} \pm \frac{F_{sAMPLE}}{2} \tag{2.35}$$

It should be noted that the two frequencies actually appear as the same spurious tone in an FFT plot, as they both alias to the same frequency. In general, with $M > 2$, additional spurious tones appear with magnitudes typically less than the tone in the $M = 2$ case and at frequencies given by [1]:

$$F_{\Delta TSKEW} = F_{IN} \pm \frac{iF_{sAMPLE}}{M} \tag{2.36}$$

$$i = 1, 2, \ldots M - 1$$

As an example, Figure 2.6 shows a 32,768 point FFT plot of an $F_{IN} = 110\,MHz$ input, sampled at a rate $F_{SAMPLE} = 125\,MHz$ with an $M = 2$ TI-ADC, subject to a timing skew $\Delta T_{SKEW} = 6\,ps$.

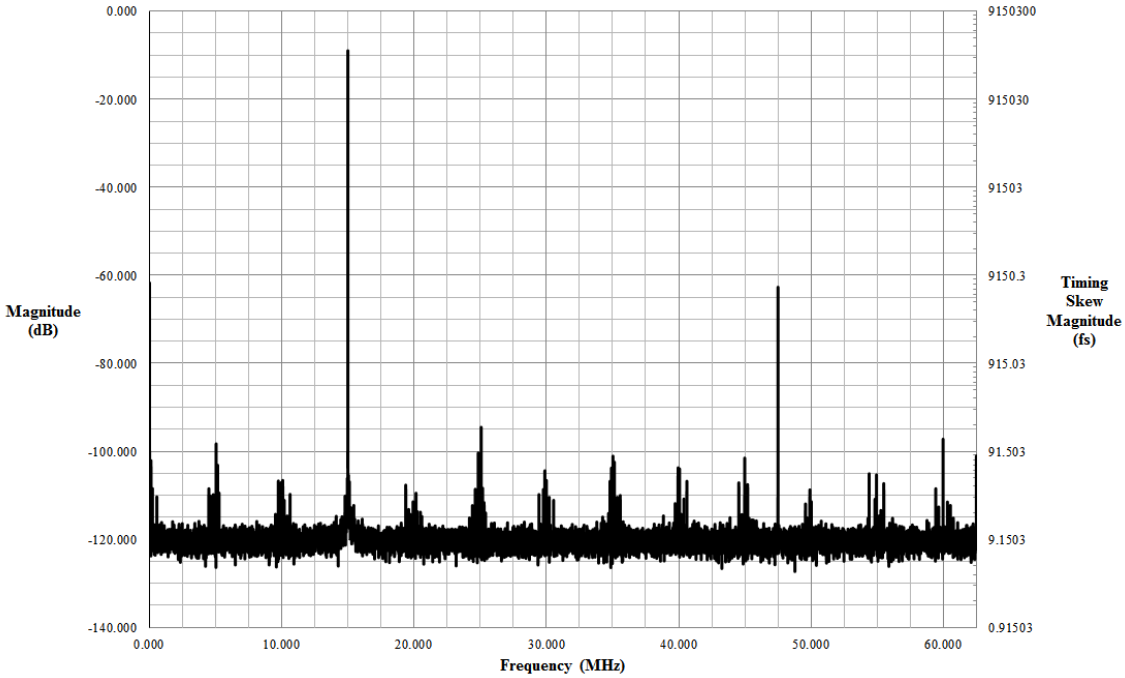


Figure 2.6: FFT Plot of a 2-way TI-ADC with $F_{IN} = 110\ MHz$ and $F_{SAMPLE} = 125\ MHz$, Subject to a 6 ps Timing Skew

The most useful way to consider Figure 2.6, in terms of timing skews, is to calculate the SFDR. Using equations (2.12), (2.33) and (2.34), the SFDR for a $M = 2$ TI-ADC is given by:

$$SFDR = \frac{\frac{V_{FS}}{2\sqrt{2}}\cos\left(2\pi F_{IN}\frac{\Delta T_{SKEW}}{2}\right)}{\frac{V_{FS}}{2\sqrt{2}}\sin\left(2\pi F_{IN}\frac{\Delta T_{SKEW}}{2}\right)} \tag{2.37}$$

Simplifying (2.37) yields:

$$SFDR = \frac{\cos\left(2\pi F_{IN}\frac{\Delta T_{SKEW}}{2}\right)}{\sin\left(2\pi F_{IN}\frac{\Delta T_{SKEW}}{2}\right)} \tag{2.38}$$

Equation (2.38) shows that the SFDR for a 2-way TI-ADC subject to timing skews directly depends on the ratio between the input and the spurious tone due to the timing skew. This is a very important result, implying that timing skews can be detected and characterized from the measured SFDR of a TI-ADC.

From Figure 2.6 and the analysis in this chapter, it is clear that timing skews degrade output spectrum of TI-ADCs. This degradation is captured in the resolution and SFDR specifications and must be corrected to a certain limit described in the next section.

2.3.2 Timing Skew Requirements

The timing skews and corresponding spurious tones that occur in a TI-ADC system can never be eliminated entirely, as this would require a correction method with infinite precision. However, perfect elimination is not required. It is only necessary to supress the spurious tones to a level that does not affect the desired resolution and SFDR of the TI-ADC. Usually this means correcting the timing skews to the point where the spurious tones are below the quantization noise level.

To establish concrete design goals for this thesis and push the boundaries of what current ADCs are doing by time interleaving, a modern high resolution, high speed ADC is considered. The 16-bit, 20 MSPS AD9266 by Analog Devices is representative of a modern high resolution, high speed ADC [6]. It is assumed that an

improvement of 16 to 32 times the original sample rate (interleaving 16 or 32 AD9266 ADCs) is representative of a push in the boundaries. This assumption is valid as recent, state of the art TI-ADCs have 2 to 24 interleaved ADCs [7], [8], [9], [10], [11]. In addition, it is assumed that achieving a timing skew limited $SFDR = 100\,dBc$ for a $F_{IN} = 100\,MHz$ is representative of boundary pushing performance. The implication this value has on the precision the analog timing skew correction circuit needs to achieve is shown later in this section.

Considering the previous statement about the quantization noise level, the rms values of (2.6) and (2.34) are used to express, for a 2-way TI-ADC, the relationship between the quantization noise level and the magnitude of the timing skew spurious tone:

$$\frac{V_{FS}}{2^N\sqrt{2}\sqrt{12}} \geq \frac{V_{FS}}{2\sqrt{2}}\sin\left(2\pi F_{IN}\frac{\Delta T_{SKEW}}{2}\right) \tag{2.39}$$

Using the small-angle approximation $\sin(x) = x$ for small x and rearranging to solve for the input frequency F_{IN} yields:

$$F_{IN} \leq \frac{2}{\pi 2^N\sqrt{12}\Delta T_{SKEW}} \tag{2.40}$$

This relation shows that for a given resolution N and timing skew ΔT there is a limit on the maximum input frequency to the TI-ADC such that the resolution does not degrade below N bits. A plot of (2.40) is shown in Figure 2.7, illustrating the maximum input frequency possible for a given resolution, subject to various orders of timing skew.

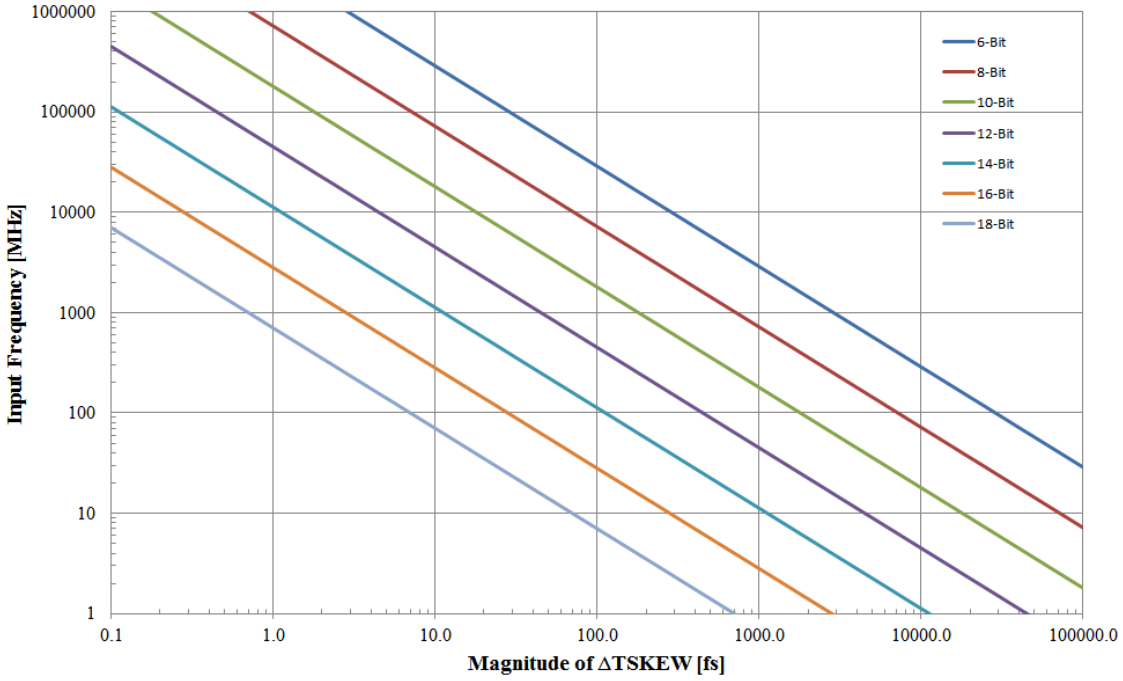


Figure 2.7: Input Frequency vs. Timing Skew for Specific Resolutions

It is evident from Figure 2.7 that as the input frequency increases, the degree to which timing skews need to be corrected also increases in order to maintain a certain resolution. Alternatively, if the assumption is made that the input frequency to the TI-ADC will be set at the highest rate possible within the first Nyquist zone, i.e. ($F_{IN} = 1/2T_{SAMPLE}$), then (2.40) becomes:

$$\frac{\Delta T_{SKEW}}{T_{SAMPLE}} \leq \frac{4}{\pi 2^N \sqrt{12}} \tag{2.41}$$

Equation (2.41) is also a useful way to think of timing skews as it relates them to the sample rate. Furthermore, it works out that the ratio of $\Delta T_{SKEW}/T_{SAMPLE}$ needs to be on the same order as the resolution of the converter when sampling at the Nyquist rate.

As mentioned in the previous section, a very useful way to consider timing skews is in terms of the SFDR of the TI-ADC. Equation (2.38) can be further simplified by using the small angle approximations for both $\cos(x)$ and $\sin(x)$ and putting it in dB, which results in:

$$SFDR = 20\log_{10}\left(\frac{1}{\pi F_{IN}\Delta T_{SKEW}}\right) \tag{2.42}$$

Equation (2.42) shows that the SFDR of a TI-ADC will degrade as F_{IN} increases, unless there is a corresponding decrease in the timing skew ΔT_{SKEW}. Figure 2.8 illustrates this behaviour, showing the expected SFDR for a range of input frequencies, given various orders of timing skew.

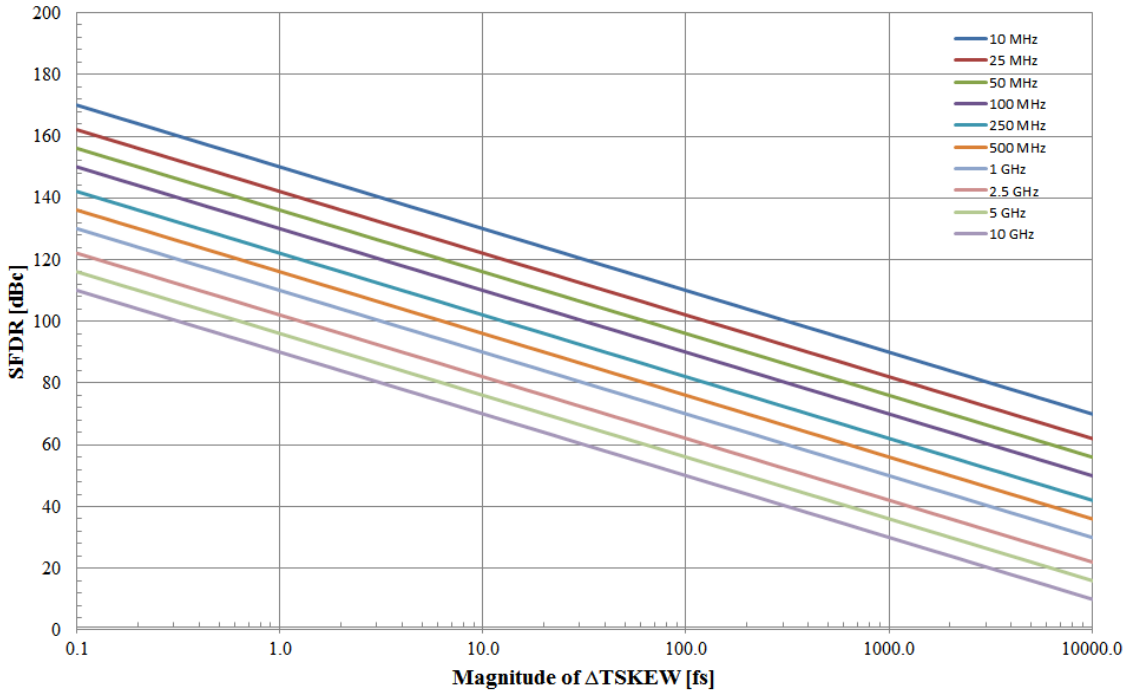


Figure 2.8: SFDR vs. Timing Skew for Specific Input Frequencies

It is very important to note that Figure 2.8 is a vital reference as it quickly shows the precision level to which timing skews need to be corrected for a given input frequency and SFDR. This is useful to know when either designing or measuring the performance of a circuit for correcting timing skews in TI-ADCs since the precision level is one of the main specifications to consider for such a circuit. Based on Figure 2.8 then, a timing skew limited $SFDR = 100\,dBc$ for a $F_{IN} = 100\,MHz$, results in a precision requirement of 25 fs for the timing skew. This means that in order reduce the spurious tone 100 dB below the fundamental; the correction circuit requires a precision/step size of 25 fs when correcting the timing skew. This serves as the first main design goal of this thesis and is representative of a boundary pushing goal as recently reported TI-ADCs [7], [11], [9] are achieving approximately 65 fs, 250 fs and 570 fs of timing skew correction precision respectively.

The second main design goal related to timing skews is the largest magnitude of timing skew the correction circuit can handle, which herein is referred to as the range. The range requirement determines how large of a timing skew can exist between any two sub ADCs in a TI-ADC and still be corrected for down to the precision requirement. The maximum range that needs to be covered is usually on the order of tens to hundreds of picoseconds, with 25 ps [12], 50 ps [13] and 500 ps [14] being reported in the literature. In this thesis, a range of approximately 100 ps to 200 ps is set as the design goal. This range specification represents a rough average of what the literature reports, leaning more towards the low end in order to cater to integrated circuit based TI-ADCs.

2.4 Jitter

Jitter is the random variation in timing of when a signal crosses a specific threshold. The random variation in timing is a result of noise being present on the signal whose

threshold crossing is important. All ADCs whether they are TI-ADCs or not, are degraded by the presence of jitter on their sampling clocks and on the input signal to the ADC. In this thesis the jitter of concern is that on the sampling clocks provided to the sub ADCs in a TI-ADC. Jitter on a sampling clock gives rise to an error in the sampled voltage as shown in Figure 2.9.

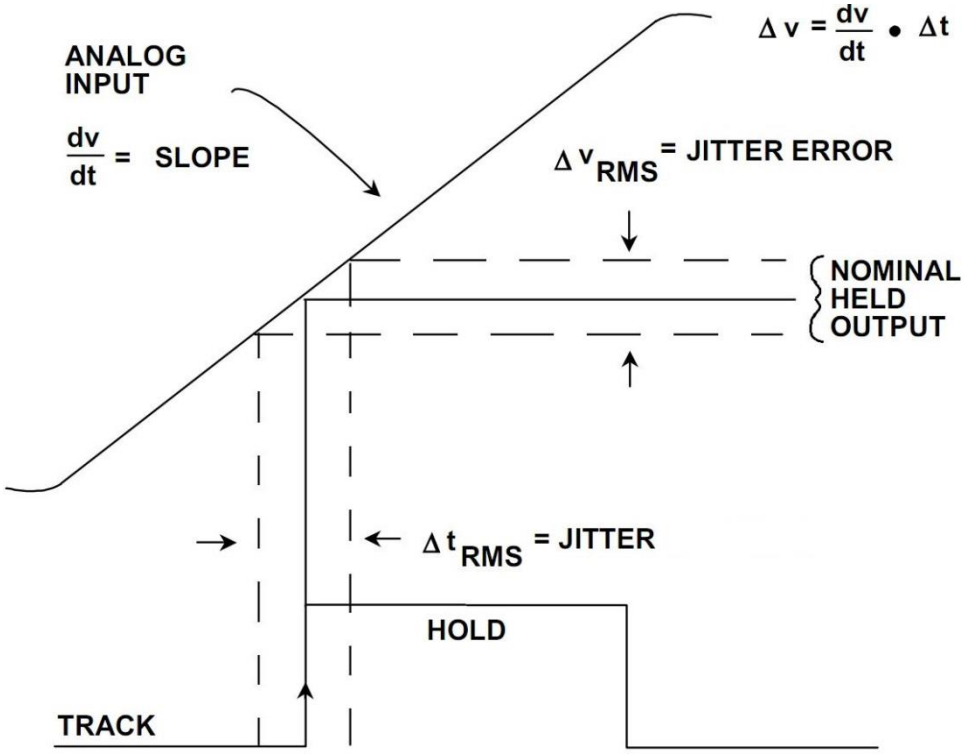


Figure 2.9: Sampling Clock Jitter's Effect on the Sample Analog Input [2]

Figure 2.9 shows that for a given jitter ΔT_{JITTER}, the error in the sampled voltage V_{NOISE} is related to the jitter through the slope or slew rate (SR) of the sampled signal. Mathematically this is expressed as:

$$V_{NOISE} = SR \times \Delta T_{JITTER} \tag{2.43}$$

Note that the error in the sampled voltage is referred to as a noise V_{NOISE} because ΔT_{JITTER} is a random value, which means the voltage error is a random value and will appear as a noise on the output of the ADC. Furthermore ΔT_{JITTER} is typically expressed as an rms value, resulting in V_{NOISE} also being an rms voltage.

As mentioned in Section 2.1, ADCs are usually tested with a sinusoidal input signal. Given this, the worst-case V_{NOISE} for a given ΔT_{JITTER} on the sampling clock, occurs when the maximum slew rate is observed on the sinusoidal input. The sinusoidal input can be expressed as follows:

$$V_{IN} = \frac{V_{FS}}{2}\sin(2\pi F_{IN} t) \tag{2.44}$$

Taking the derivative with respect to t and solving for the maximum value yields:

$$\frac{dV_{IN}}{dt} = V_{FS}\pi F_{IN} = SR(max) \tag{2.45}$$

Substituting (2.45) into (2.43) results in:

$$V_{NOISE} = V_{FS}\pi F_{IN}\Delta T_{JITTER}) \tag{2.46}$$

It is important to note that for either an increase in ΔT_{JITTER} or an increase in F_{IN} the noise output from the ADC will increase. Additionally the jitter does not depend on the sample rate. The sample rate only establishes the Nyquist zone that F_{IN} falls into.

2.4.1 Jitter Requirements

As in the case with the timing skews, jitter can never be eliminated from a TI-ADC or any ADC for that matter, only controlled to within a set limit. Similarly then, it is desirable to have the jitter controlled to a level that is below the quantization floor. This can be expressed, using the rms values of (2.6) and (2.46), as follows:

$$\frac{V_{FS}}{2^N\sqrt{2}\sqrt{12}} \geq \frac{V_{FS}}{\sqrt{2}}\pi F_{IN}\Delta T_{JITTER} \tag{2.47}$$

Rearranging to solve for F_{IN} yields:

$$F_{IN} \leq \frac{1}{\pi 2^N\sqrt{12}\Delta T_{JITTER}} \tag{2.48}$$

A plot of (2.48) is shown in Figure 2.10, which illustrates the highest F_{IN} for a specific resolution subject to various amounts of jitter on the sampling clock.

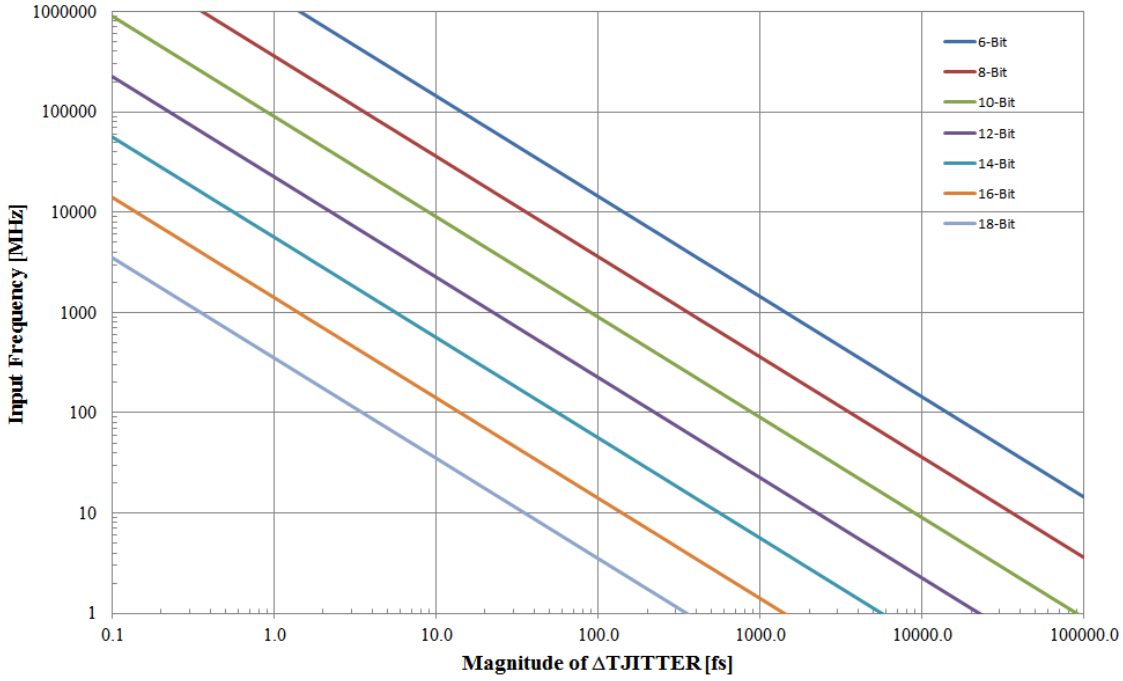


Figure 2.10: Input Frequency vs. Jitter for Specific Resolutions

Just as in the timing skew case, as a higher F_{IN} is required, the amount of jitter that can be tolerated on the sampling clocks is reduced for a given resolution. One interesting observation that is seen when comparing Figure 2.7 with Figure 2.10 is the factor of 2 difference between the ΔT_{SKEW}level and the ΔT_{JITTER} level at the same F_{IN}.

Alternatively if a specific SNR is desired, which is jitter limited, it is useful to have an expression as follows:

$$SNR = \frac{\frac{V_{FS}}{2\sqrt{2}}}{\frac{V_{FS}}{\sqrt{2}}\pi F_{IN}\Delta T_{JITTER}} \tag{2.49}$$

Simplifying (2.49) and putting it in dB yields:

$$SNR = 20\log_{10}\left(\frac{1}{2\pi F_{IN}\Delta T_{JITTER}}\right) \tag{2.50}$$

Figure 2.11 shows a plot of (2.50) for various amounts of jitter.

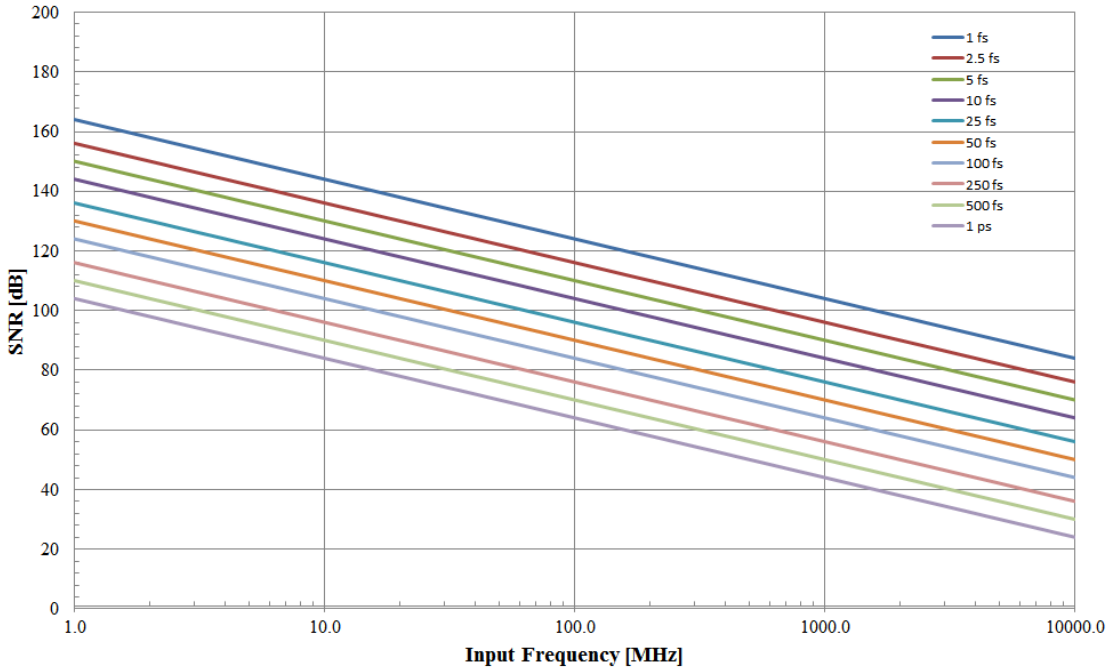


Figure 2.11: SNR vs. Input Frequency for Various Amounts of Jitter

Just as in the case with timing skews, it is important to control the amount of additive jitter that the clocking sources for the sub ADCs experience. Similar to the

timing skew SFDR goal, an additive jitter limited $SNR = 95\,dB$ for a $F_{IN} = 100\,MHz$ is assumed representative of a boundary pushing performance goal. Based on Figure 2.11 then, an additive jitter limited $SNR = 95\,dB$ for a $F_{IN} = 100\,MHz$, results in the correction circuit having an additive jitter requirement of 25 fs rms allowing the SNR degradation due to jitter to not mask the desired timing skew correction precision. This serves as the third and final main design goal of this thesis.

2.5 Summary

Timing skews result in non-uniform sampling of a signal in TI-ADCs. This non-uniform sampling gives rise to distinct spurious tones, whose magnitude depends on the input frequency to the TI-ADC and the how large of a timing skew is present between any two sub-ADCs. These spurious tones degraded the SFDR and resolution of the TI-ADC. In addition, jitter on the sampling clocks to the sub ADCs further degraded the resolution or SNR of the TI-ADC. From these two phenomena, timing skews and jitter, three system level requirements or design goals are established. The first being the precision required to correct timing skews, the second being the largest range required to correct the timing skews and the third being the amount of additive jitter that can be tolerated on the sampling clocks, such that the SFDR, resolution and SNR are not impacted up to a maximum input frequency. Based on the example TI-ADC system with boundary pushing performance levels of a timing skew limited $SFDR = 100\,dBc$ and an additive jitter limited $SNR = 95\,dB$ for a $F_{IN} = 100\,MHz$, the resulting design goals are a precision/step size of 25 fs for ΔT_{SKEW} with a range of 100 ps to 200 ps for ΔT_{SKEW} and an additive jitter ΔT_{JITTER} of 25 fs. Circuits to achieve these design goals are explored in the following chapters.

Chapter 3

Analog Techniques to Correct Timing Skews

This chapter begins with a brief comparison between correcting timing skews in the analog domain and correcting them in the digital domain. It then proceeds to analyze and compare different analog circuit techniques that can be used to correct timing skews. Next, two circuit architectures that use the analog circuit techniques are compared, with one being selected as the design for this thesis. After this, a discussion is presented on how the selected architecture is implemented such that it can be tested in terms of the three design goals. Lastly, a summary of the complete architecture to be designed is presented along with the design goals for each block within the architecture.

3.1 Analog vs. Digital Correction

At the heart of any method to correct timing skews in TI-ADCs is the idea of adjusting the timing of the samples such that they appear as uniform as possible. In

the analog domain, this is accomplished by adjusting the clock edges of each sub ADC such that the TI-ADC's samples are taken in a uniform manner. Whereas in the digital domain, the samples are taken with the timing skews present and then the output is post processed, adjusting the phase of each sub ADCs data such that the overall digital data appears to be uniformly sampled. Correction methods designed in either domain are subject to the three main design requirements of precision, additive jitter and range. Additionally the bandwidth over which the correction method operates and how power intensive they are, matter to both analog and digital domain correction methods. Given these five requirements, the two domains can now be compared.

As previously mentioned correcting timing skews in the analog domain requires a circuit to adjust the clock edges the sub ADCs use to sample. Fortunately there are circuits already present in TI-ADCs that can be modified to perform the clock edge adjustment such as the on chip clock buffers or clock divider circuits. In addition, analog correction does not affect the bandwidth F_{BW} of the TI-ADC and allows multiple input signals in different Nyquist zones to be converted while having the timing skews corrected. Analog correction circuits also offer high correction precision, while not always being directly proportional to the power. Unfortunately, analog circuits are subject to noise and thus jitter, which usually requires adding power to reduce the jitter. Similarly, in order to cover a larger range, i.e. larger timing skew between any two sub ADCs, more power is also needed.

Digital correction of timing skews is usually accomplished through the design of a fractional delay filter or interpolation filter, which allows for the phase shifting of the digital data samples [1]. This signal processing adds noise due to the finite precision of the arithmetic and rounding errors, requiring more bits for less noise and thus more power. In addition, the precision, range and bandwidth are all proportional to the order of the digital filters used to correct the timing skews, meaning better performance in any of these requires more power. Furthermore, the bandwidth is

fundamentally limited to slightly less than one Nyquist zone due to aliasing. This means that for digital correction methods to cover more of one Nyquist zone, more power is required. Furthermore, if the signal being sampled by the TI-ADC changes Nyquist zones, the digital correction method has to re-configure the filter for the new Nyquist zone in real-time. Finally, the filters require multipliers running at a rate at least equal to the sub ADC rate if not the full clock rate of the TI-ADC. This is also power intensive, as high-speed multiplication is generally a high power operation.

A summary of how analog domain and digital domain timing skew correction compare in terms of the five requirements; additive jitter/noise, precision, range, bandwidth and power is presented in Table 3.1.

Table 3.1: Performance Comparison of Analog Domain and Digital Domain Timing Skew Correction

	Analog Correction	**Digital Correction**
Additive Jitter/Noise	$\propto \frac{1}{Power}$	$\propto Power\ through\ the\ number\ of\ bits$
Precision Level	$dependent\ but\ not\ always\ \propto Power$	$\propto Power$
Range	$\propto Power$	$\propto Power$
Bandwidth	$Independent\ of\ Power\ and\ not\ limited$	$\propto Power$ and limited to < one Nyquist zone

There are two important things to note between analog and digital correction of timings skews. The first is that while analog correction requires power to reduce the

amount of additive jitter, digital correction requires power to increase the precision level to which timing skews are corrected. The second is that analog correction can tolerate signals that change Nyquist zones or span multiple Nyquist zones, while digital correction for the most part cannot tolerate these signals. Both domains are useful for the specific applications that are unaffected by the limitations they each have. This thesis focuses on analog correction and minimizing the limitations that exist with it.

3.2 Circuit Techniques

Analog correction of timing skews is a matter of adjusting clock edges while affecting little else in the TI-ADC. In circuit terms, this means being able to vary the delay of a clock edge while not loading the clock or adding significant jitter. To understand what techniques can be used to accomplish this, it is best to consider a buffer or inverter. Figure 3.1 shows the schematic of a MOSFET based differential buffer/inverter with a capacitive load.

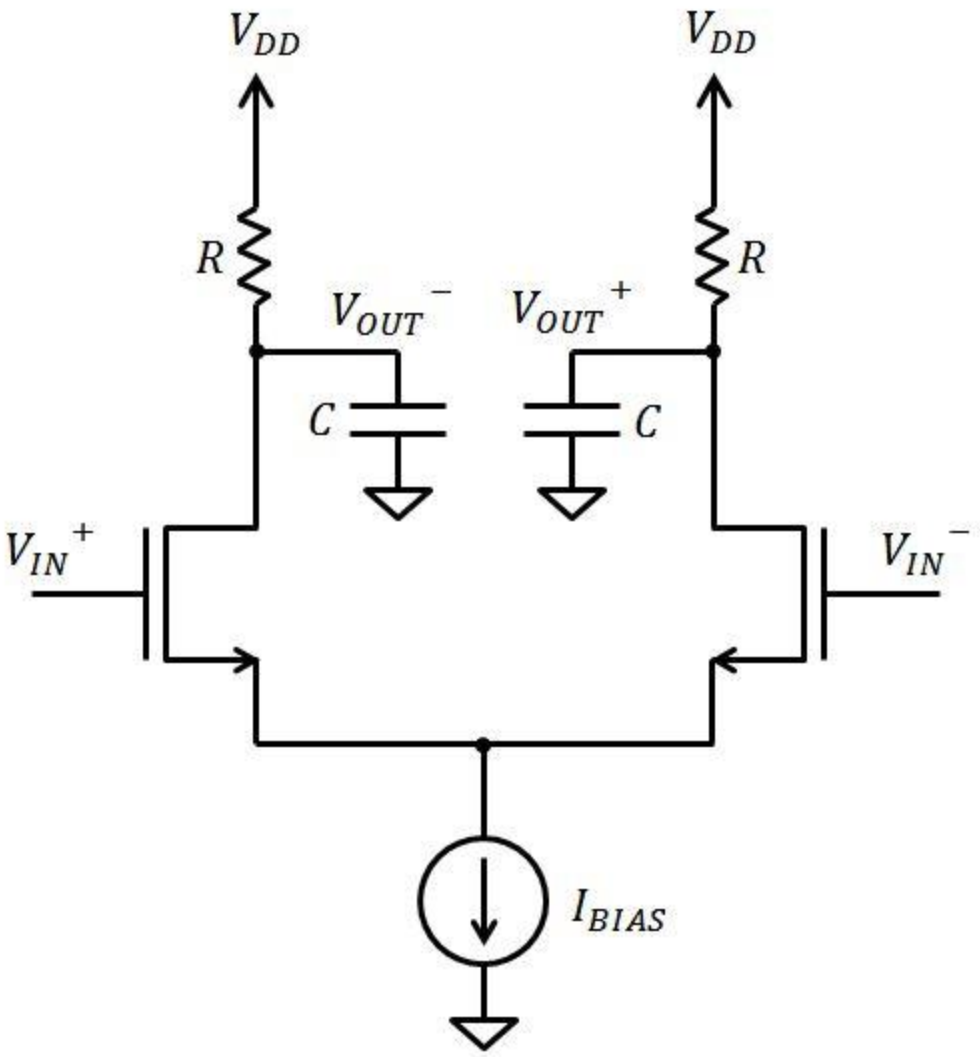


Figure 3.1: Schematic a Differential Buffer/Inverter

A buffer/inverter takes in a clock edge and outputs a delayed edge due to the charging/discharging of the capacitive load C. This delay, T_{DELAY}, is usually on the order of 10's of picoseconds for a capacitive load comparable to the intrinsic capacitance of the buffer/inverter. The intrinsic delay of a single buffer then is too small to cover the desired delay range of 100 ps to 200 ps. The delay is also too large for fine-tuning, as placing two buffers in series provides too large a delay step to

achieve the desired precision or step size of 25 fs. Given this, it is useful to analyze the buffer/inverter to see how delays in between a single buffer and two buffers can be achieved and varied to meet the precision requirement. Note the analysis of how delays much larger than the intrinsic delay can be achieved is left to Section 3.3.

3.2.1 Analysis

Two important aspects of the differential buffer/inverter need to be considered, how the delay can be varied and how this impacts the additive jitter of the buffer. To simplify the analysis of the differential buffer/inverter in Figure 3.1, a single-ended model of it is considered, shown in Figure 3.2

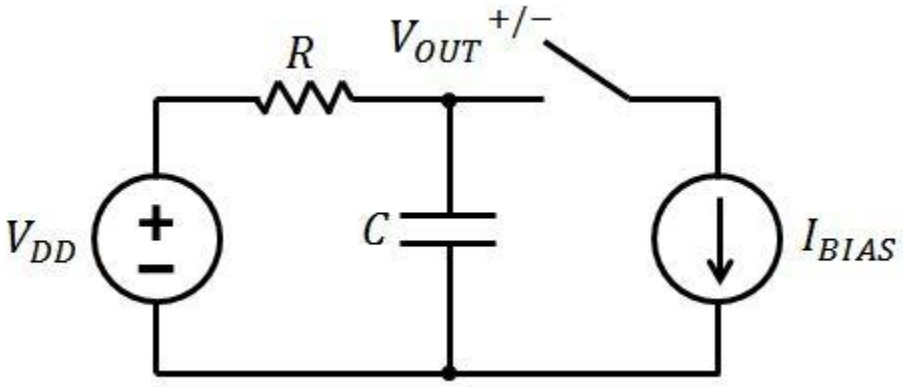


Figure 3.2: Single-Ended Model of a Differential Buffer/Inverter

The switch in the model is controlled by the input clock, opening when it transitions from high to low (falling edge) and closing when transitioning from low to high (rising edge). To understand the delay behaviour of the model in terms of I_{BIAS}, R and C, the step response is calculated. Equations (3.1) and (3.2) are the step responses for

the rising V_{OUTR} and falling V_{OUTF} input clock edge respectively assuming zero initial voltage on the capacitor.

$$V_{OUTR} = V_{DD} - I_{BIAS}Re^{\frac{-t}{RC}} \tag{3.1}$$

$$V_{OUTF} = V_{DD} - I_{BIAS}R(1 - e^{\frac{-t}{RC}}) \tag{3.2}$$

The step response of the model turns out to be very similar to that of the familiar RC circuit and shows that varying I_{BIAS}, R or C will vary V_{OUTR} and V_{OUTF} and correspondingly the delay. Note V_{DD} is considered the supply voltage for the majority of analog circuits in the TI-ADC and thus a constant, non-variable value since it would change the behaviour of other circuits. Additionally, it is assumed that the output swing $V_{DD} - I_{BIAS}R$ is kept constant due to practical reasons, i.e. the need to keep the current source MOSFET in saturation. The implication of this is that if I_{BIAS} increases by a factor of two, R must decrease by a factor of two to maintain the same output swing.

For differential circuits, a common way to calculate the delay is based off when the output reaches the common-mode value, since it is at this point the following stage switches. Typically, the common-mode value corresponds to the time when the output has achieved 50% of its final value, assuming a symmetric swing about the common-mode. In terms of the single-ended model this corresponds to the time t when $V_{OUTR/F} = V_{DD} - (I_{BIAS}R)/2$. Using this, the assumption of a fixed swing, (3.1) and (3.2), the delay T_{DELAY} is solved for yielding the familiar RC circuit expression:

$$t = 0.69RC = T_{DELAY} \tag{3.3}$$

Note that (3.3) applies for either the rising or falling edge. Equation (3.3) shows that the delay of the differential buffer/inverter is proportional to C and R or $1/I_{BIAS}$. The delay then can be varied by scaling C, R or I_{BIAS} such that it covers the range in between a single buffer and two series buffers. With the delay behaviour of the differential buffer/inverter characterized, the jitter behaviour is now considered.

Referring back to (2.43), the jitter for a circuit can be approximated to the first order by:

$$\Delta T_{JITTER} = \frac{V_{NOISE}}{SR} \tag{3.4}$$

In this case, V_{NOISE} is the total rms noise voltage at the T_{DELAY} point and SR is the slew rate at the same point. Using (3.1), (3.2) and (3.3) the slew rate at time $t = T_{DELAY}$ is calculated yielding:

$$SR = \frac{I_{BIAS}}{2C} \tag{3.5}$$

Note the slew rate is the same whether V_{OUT} is rising or falling. Furthermore, the slew rate is linked to R only through the fixed output swing assumption.

To simplify the calculation of V_{NOISE} it is assumed that only R and I_{BIAS} contribute noise and not the switch or supply V_{DD}. Note that the noise due to I_{BIAS} is a result of the current source being implemented by using a MOSFET in saturation. In addition, only the thermal noise of the two elements is considered to simplify further

the analysis of V_{NOISE}. Given these assumptions, Figure 3.3 shows the noise model of the circuit in Figure 3.2.

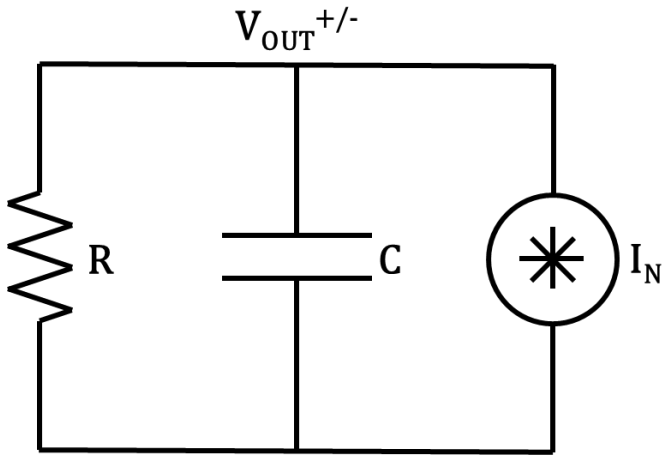


Figure 3.3: Simplified Noise Model of a Differential Buffer/Inverter

In Figure 3.3, I_N is the total thermal noise, which is composed of the I_{BIAS} noise (I_{NI}) and R thermal noise (I_{NR}). The expressions for the thermal noise of a MOSFET in saturation I_{NI}, thermal noise of a resistor I_{NR} and the total noise I_N are [15]:

$$I_{NI}{}^2 = \frac{8KTg_m}{3}\Delta F \tag{3.6}$$

$$I_{NR}{}^2 = \frac{4KT}{R}\Delta F \tag{3.7}$$

$$I_N{}^2 = \left(\frac{8g_m}{3} + \frac{4}{R}\right) KT\Delta F \tag{3.8}$$

where K and T are constants and ΔF implies that the noise is per Hz. ΔF is usually set to $1/4RC$ which approximates the noise bandwidth of the circuit [15]. The term g_m is the transconductance of the MOSFET and relates to I_{BIAS}, i.e. ($g_m \propto \sqrt{I_{BIAS}}$). Given these things, (3.8) is rewritten as:

$$I_N \propto \sqrt{\left(\frac{8\sqrt{I_{BIAS}}}{3} + \frac{4}{R}\right)\frac{KT}{4RC}} \tag{3.9}$$

Relating I_N to the output noise V_{NOISE} requires multiplying I_N by R yielding:

$$V_{NOISE} \propto \sqrt{\left(\frac{8R\sqrt{I_{BIAS}}}{3} + 4\right)\frac{KT}{C}} \tag{3.10}$$

Simplifying and rearranging results in:

$$V_{NOISE} \propto \sqrt{\left(1 + \frac{2R\sqrt{I_{BIAS}}}{3}\right)\frac{KT}{C}} \tag{3.11}$$

The $R\sqrt{I_{BIAS}}$ term is usually appreciably greater than one to allow a reasonable output swing. Note that this implies that the active device (MOSFET) noise is typically greater than the passive devices. Using this, (3.11) is approximated as:

$$V_{NOISE} \propto \sqrt{\left(\frac{2R\sqrt{I_{BIAS}}}{3}\right)\frac{KT}{C}} \tag{3.12}$$

Since only the relation of I_{BIAS}, R and C to V_{NOISE} matter; (3.12) is simplified resulting in:

$$V_{NOISE} \propto \sqrt{\frac{R\sqrt{I_{BIAS}}}{C}} \tag{3.13}$$

Using equations (3.4), (3.5) and (3.13) the relationship between I_{BIAS}, R and C and the additive jitter ΔT_{JITTER} is given by:

$$\Delta T_{JITTER} \propto \frac{\sqrt{\frac{R\sqrt{I_{BIAS}}}{C}}}{\frac{I_{BIAS}}{2C}} \tag{3.14}$$

Simplifying (3.14) gives:

$$\Delta T_{JITTER} \propto \frac{\sqrt{R}\sqrt{C}}{I_{BIAS}{}^{3/4}} \tag{3.15}$$

With (3.15), the relationship between R, I_{BIAS} and C is established and a comparison can be made between each in terms of their influence on T_{DELAY} and ΔT_{JITTER}.

3.2.2 Comparison

Using (3.15), the effects of varying R, I_{BIAS} and C on the delay and jitter of the differential buffer/inverter are shown in Table 3.2 and Figure 3.4. C is varied independently of R and I_{BIAS}, whereas R and I_{BIAS} are varied in two ways. The first way is that for both T_{DELAY} and ΔT_{JITTER}, the assumption that $I_{BIAS}R = Constant$ is considered. The second way is that for only ΔT_{JITTER}, the effect of varying R and I_{BIAS} independently is considered. Although the effect on the delay is not considered in Table 3.2 for the second way, the general trend is that increasing I_{BIAS} by $2\times$ results in a $> 2\times$ decrease in T_{DELAY} whereas increasing R by $2\times$ results in a $\ll 2\times$ increase in T_{DELAY} when considering the same output voltage level at which T_{DELAY} is measured. The opposite variation of R and I_{BIAS} is not valid as decreasing either shrinks the signal swing, which can lead to the output not swinging enough to switch subsequent gates.

Table 3.2: Effect of Varying R, I_{BIAS} and C on T_{DELAY} and ΔT_{JITTER}

	$\Delta(Parameter)$	$\Delta(T_{DELAY})$	$\Delta(\Delta T_{JITTER})$	
			$I_{BIAS} \times R = Constant\ (cst.)$	$I_{BIAS}, R = Independant(ind.)$
R	$2\times$	$2\times$	$\frac{\sqrt{2}}{\left(\frac{1}{2}\right)^{3/4}} \times \cong 2.38$	$\sqrt{2} \times \cong 1.41$
	$\frac{1}{2}\times$	$\frac{1}{2}\times$	$\frac{\frac{1}{\sqrt{2}}}{(2)^{3/4}} \times \cong 0.42$	$\frac{1}{\sqrt{2}} \times \cong 0.71$
C	$2\times$	$2\times$	$\sqrt{2} \times \cong 1.41$	$\sqrt{2} \times \cong 1.41$
	$\frac{1}{2}\times$	$\frac{1}{2}\times$	$\frac{1}{\sqrt{2}} \times \cong 0.71$	$\frac{1}{\sqrt{2}} \times \cong 0.71$
I_{BIAS}	$2\times$	$\frac{1}{2}\times$	$\frac{\frac{1}{\sqrt{2}}}{(2)^{3/4}} \times \cong 0.42$	$\frac{1}{(2)^{3/4}} \times \cong 0.59$
	$\frac{1}{2}\times$	$2\times$	$\frac{\sqrt{2}}{\left(\frac{1}{2}\right)^{3/4}} \times \cong 2.38$	$\frac{1}{\left(\frac{1}{2}\right)^{3/4}} \times \cong 1.68$

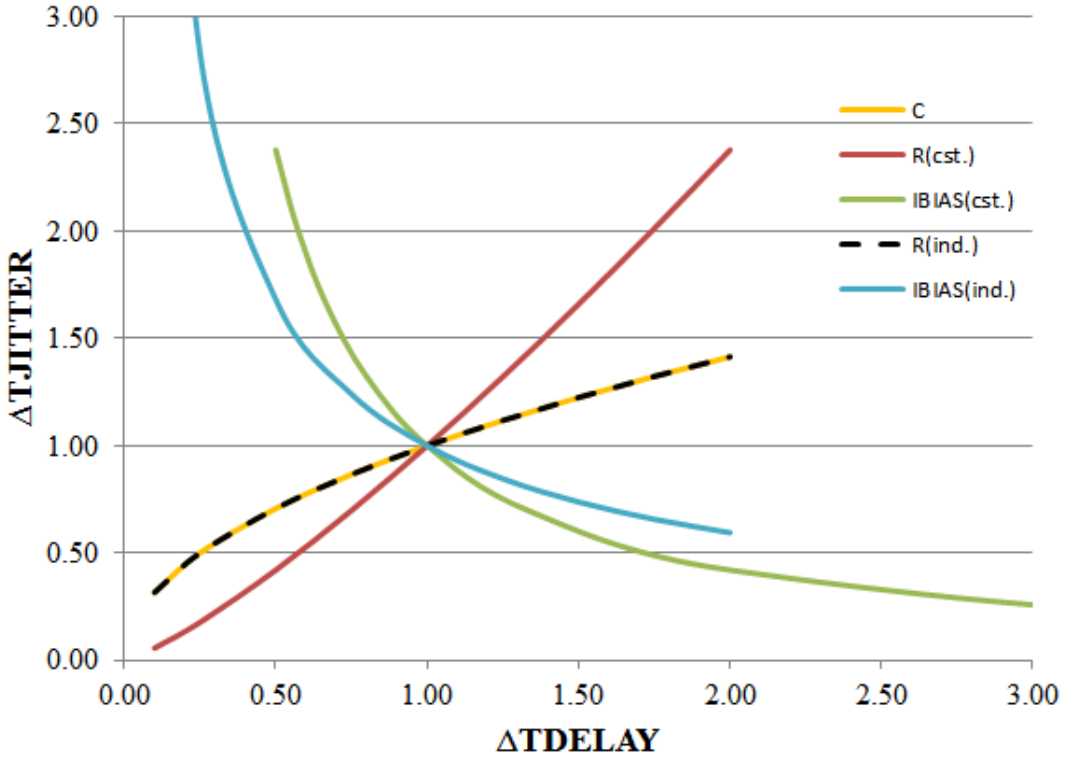
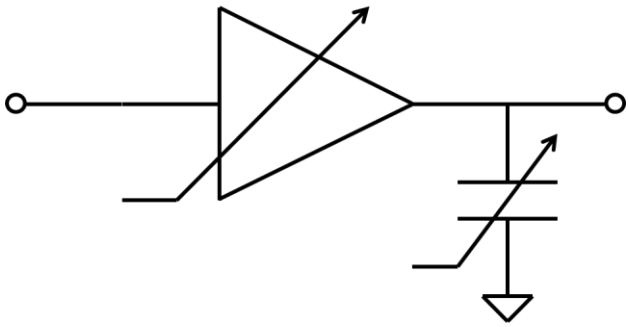


Figure 3.4: ΔT_{JITTER} vs. T_{DELAY} Trade-off when Varying R, I_{BIAS} and C

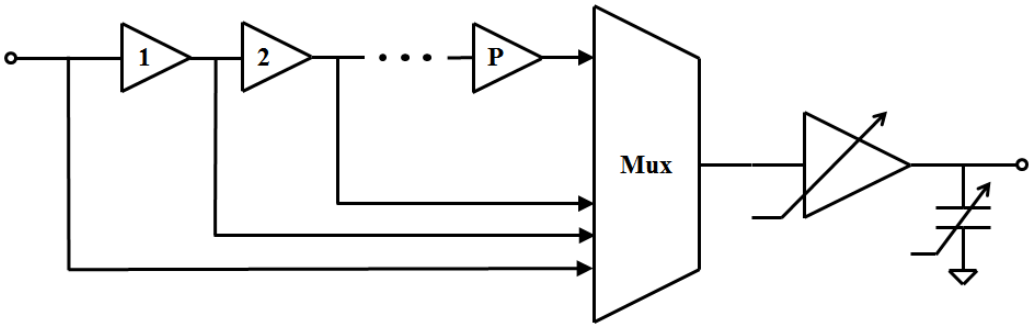
Based on Table 3.2 and the above statements it is best to vary the load capacitance (C) to achieve delays larger than a single intrinsic buffer as it provides a better delay increase vs. additive jitter trade-off as compared to R and I_{BIAS}. However, the precision of the delay steps is limited to the smallest capacitor that can be implemented in the chosen process. If a more precise delay step is desired an interesting option exists in terms of the best delay vs. jitter trade-off. Consider adding a unit C, the smallest C possible, to the load, the current I_{BIAS} can then be increased to shrink the delay step from the unit C, which according to Table 3.2, allows for better precision and for the jitter to improve as more current is added. Note that this assumes I_{BIAS} can be increased in smaller units relative to its original value then a unit C. The validity of this assumption will be shown in Chapter 4.

3.3 Circuit Architectures

The differential buffer and the variable capacitor technique will serve as the basis for the two circuit architectures considered. Similar to the previous section, the goal is to establish how both architectures behave in terms of delay and jitter only over a range covering multiple buffer delays instead of a single buffer. The first architecture to be evaluated is a single differential buffer with a variable capacitor load as shown in Figure 3.5(a). The second circuit architecture consists of P selectable fixed delay differential buffers with a single variable differential delay buffer on the output as shown in Figure 3.5(b) [16]. Note the differential buffers are represented by their single ended equivalent in Figure 3.5.



a) Single Variable Delay Buffer



b) *P* Fixed Delay Buffers with a Single Variable Delay Buffer

Figure 3.5: Two Circuit Architectures for Correcting Timing Skews

For the analysis of both architectures, the single-ended model and corresponding equations from Section 3.2 are used.

3.3.1 Single Differential Buffer with Variable Capacitor Load

The delay of the differential buffer with a variable capacitor load can be expressed using (3.3):

$$T_{DELAY} = 0.69RC\left(1 + \frac{\Delta C}{C}\right) \tag{3.16}$$

In this case, C represents the minimum capacitive load on the buffer and ΔC represents the amount of added capacitance such that the delay variation of the buffer meets the range specification for the timing skew correction. Similarly, the additive jitter is expressed using (3.15):

$$\Delta T_{JITTER} \propto \sqrt{RC\left(1 + \frac{\Delta C}{C}\right)} \tag{3.17}$$

As expected, the additive jitter maintains its square root relationship with the varying of the buffers capacitive load. Furthermore, the additive jitter has a square root relationship with delay of the buffer, which illustrates the inherent trade-off between the range of timing skews that can be corrected and the amount of additive jitter from the correction circuit.

3.3.2 P Fixed Delay Buffers and One Variable Delay Buffer

Referring back to Figure 3.5 (b), the operating principle behind this circuit architecture is that the single variable delay differential buffer is set to cover the delay range between any two selectable paths and as the delay needs to be extended beyond this, more fixed delay buffers are added in [16]. Note that once an additional fixed delay buffer is added in, the variable delay buffer is reset back to its minimum delay so delays in between the current path and next path can be achieved. The delay for this circuit architecture can be expressed in a similar manner as the previous architecture:

$$T_{DELAY} = \mathrm{D}0.69RC + 0.69RC\left(1 + \frac{\Delta C}{C}\right) \tag{3.18}$$

$$D = 0, 1, 2, \ldots P$$

In (3.18), P represents the number of fixed delay buffers needed such that the overall circuit architecture can achieve the range specification required of the timing skew correction circuit.

It is assumed that the additive jitter of each buffer is uncorrelated to any of the other buffers. This enables the magnitude of each buffer's jitter to be summed as follows:

$$\Delta T_{JITTER} = \sqrt{\Delta T_{J0}{}^2 + \Delta T_{J1}{}^2 + \cdots \Delta T_{JP}{}^2} \tag{3.19}$$

where ${\Delta T_{J0}}^2$ is the jitter of the single variable delay buffer and ${\Delta T_{J1}}^2 \rightarrow {\Delta T_{JP}}^2$ are the additive jitters of each fixed delay buffer that is currently added between the input and the variable delay buffer. Assuming each of the fixed delay buffers have the same magnitude of additive jitter, (3.19) is rewritten:

$$\Delta T_{JITTER} = \sqrt{P{\Delta T_{J1}}^2 + {\Delta T_{J0}}^2} \tag{3.20}$$

Substituting (3.17), which represents the additive jitter if a single variable delay buffer, into (3.20) results in:

$$\Delta T_{JITTER} \propto \sqrt{P{\Delta T_{J1}}^2 + RC\left(1 + \frac{\Delta C}{C}\right)} \tag{3.21}$$

The jitter for the fixed delay buffer can be represented by the same equation by setting $\Delta C = 0$, which yields the following:

$$\Delta T_{JITTER} \propto \sqrt{PRC + RC\left(1 + \frac{\Delta C}{C}\right)} \tag{3.22}$$

Equation (3.22) shows the same square root relationship as the single variable buffer architecture only for this case, either P or ΔC is used to vary the delay.

3.3.3 Comparison

The square root relationship between the additive jitter and delay of both circuit architectures given by (3.17) and (3.22) is shown in Figure 3.6.

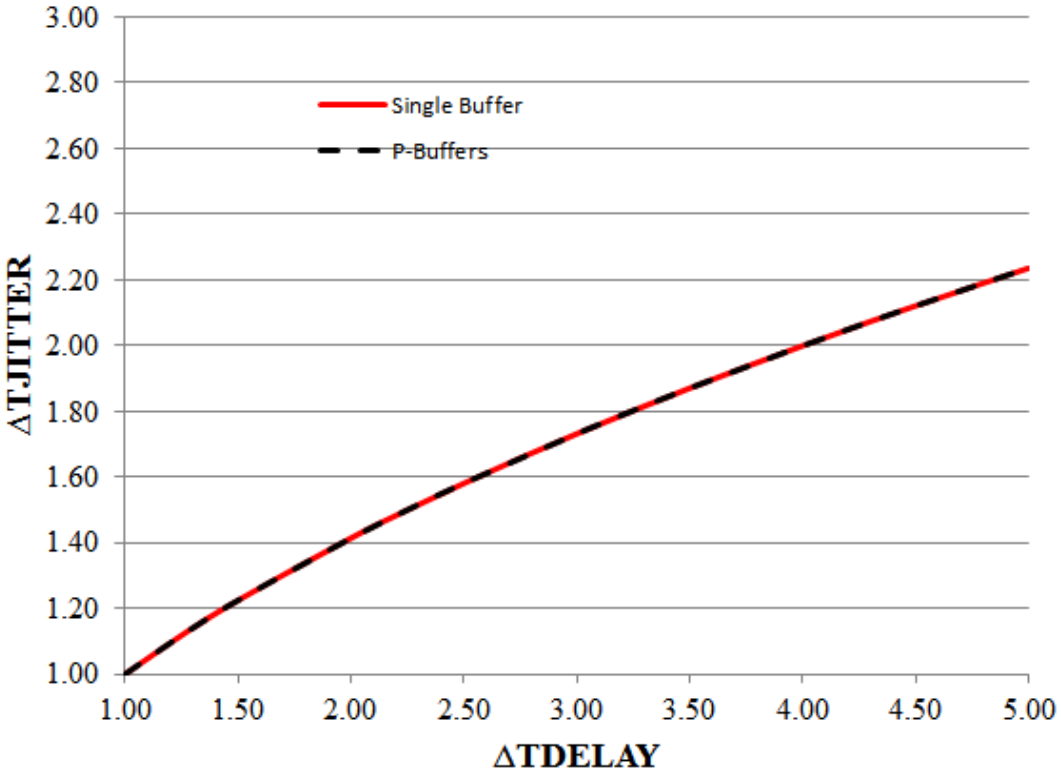


Figure 3.6: ΔT_{JITTER} vs. T_{DELAY} Trade-off for the Two Circuit Architectures

Based on Figure 3.6 alone, both architectures perform equally well in terms of the jitter and delay trade-off. However, when the gain and parasitic capacitances of the buffer and variable capacitors are considered, the jitter/delay behavior changes.

For practical reasons, the small signal gain of the differential buffer is usually greater than one over some bandwidth. This means that any noise within that

bandwidth and present on the input of the buffer increases by gain, thus increasing the jitter at the output of the buffer. The second architecture then, is susceptible to potentially large increases in the output jitter when many buffers are placed in series to correct large timing skews. On the other hand, since the first architecture contains only a single buffer, the output jitter would increase by a much smaller amount.

The parasitic capacitances from the MOSFET switches, wiring and MOSFETS in the differential buffer both benefit and hurt the jitter/ delay behavior of the variable delay differential buffer. The benefit is that since the unit capacitor is added in parallel with the parasitic capacitances present in the circuit, the relative change in delay becomes smaller or the precision of the unit capacitor increases. However, this also results in the delay range shrinking and therefore more unit capacitors are needed in order to span the desired timing skew correction range. The increased amount of capacitance on the output of the differential buffer causes the jitter to degrade, although by the same square root relationship as before. In addition, for a large timing skew correction range the area required for the variable capacitors could become prohibitive. The first and second architecture both exhibit this behavior since they both use a variable delay differential buffer, though the first architecture sees a greater increase in the jitter and area since more capacitors are needed to span the same delay range as the second architecture.

Based on these two non-idealities, the first architecture is selected to be designed. The jitter degradation is less sensitive to the gain for this architecture and although extra area is required for the additional variable capacitors, the second architecture requires extra area for each additional fixed delay buffer required to span the correction range. Furthermore, each additional buffer in the second architecture increases the power requirement of the timing skew correction circuit in a linear fashion, whereas the first architectures power increases less according to (3.15), to compensate for the increased jitter due to the parasitic capacitors. It is important to note that the two architectures jitter vs. delay behavior is close enough that both are

worth investigating however, due to time constraints, only one architecture could be designed.

3.4 Implementation and Testing Architecture

To explicitly illustrate how the proposed circuit architecture is used to correct timing skews in a TI-ADC, Figure 3.7 shows a revised version of Figure 2.4 with analog timing skew correction.

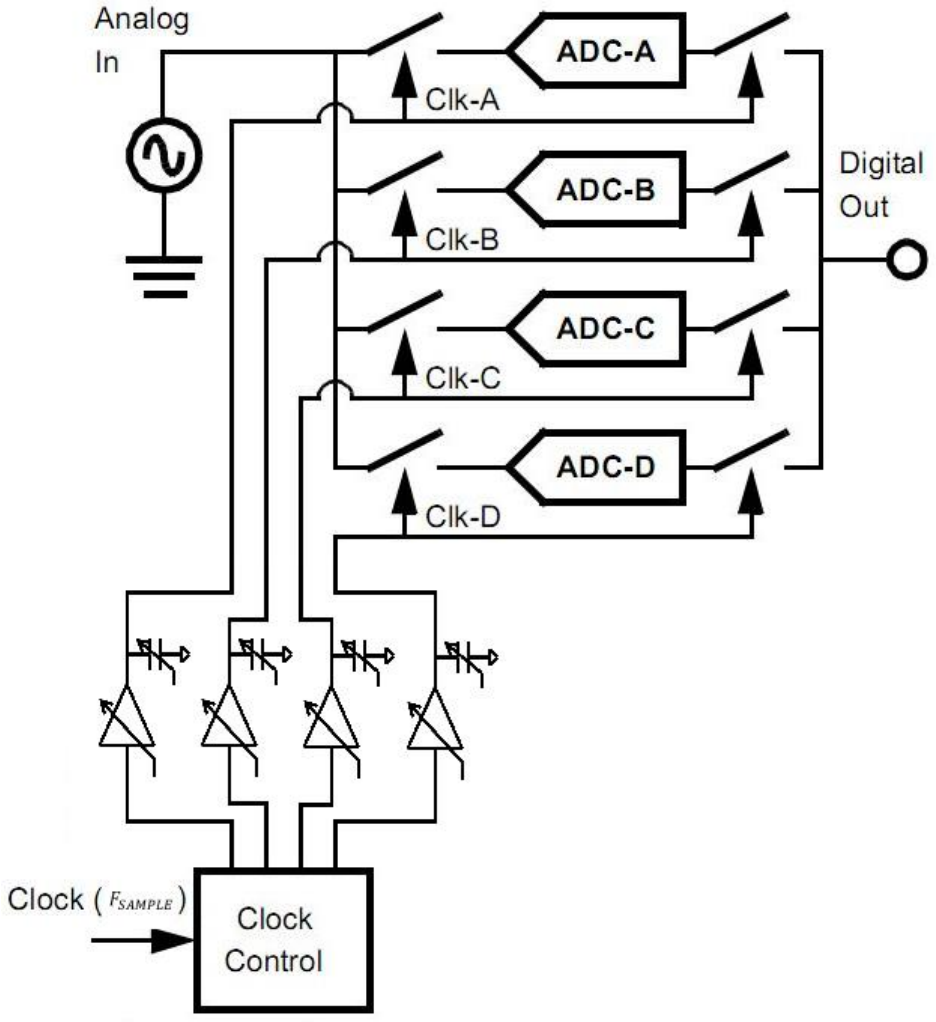
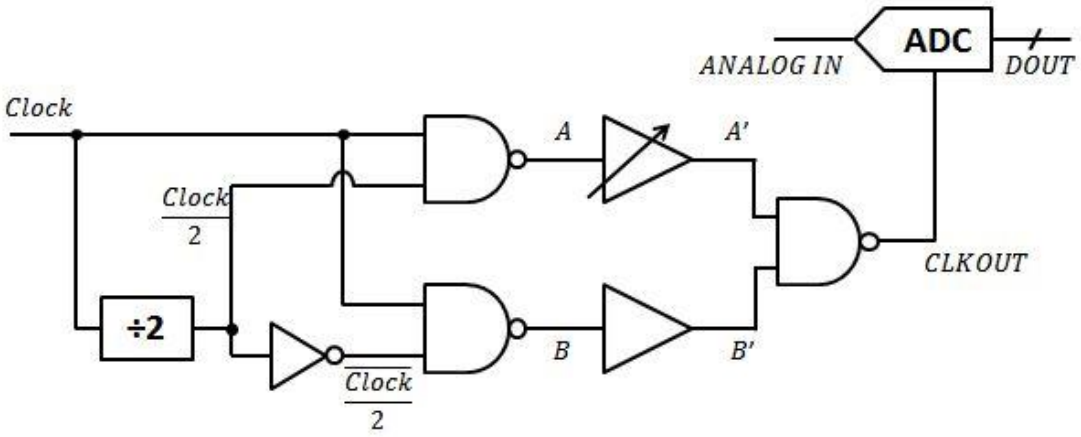


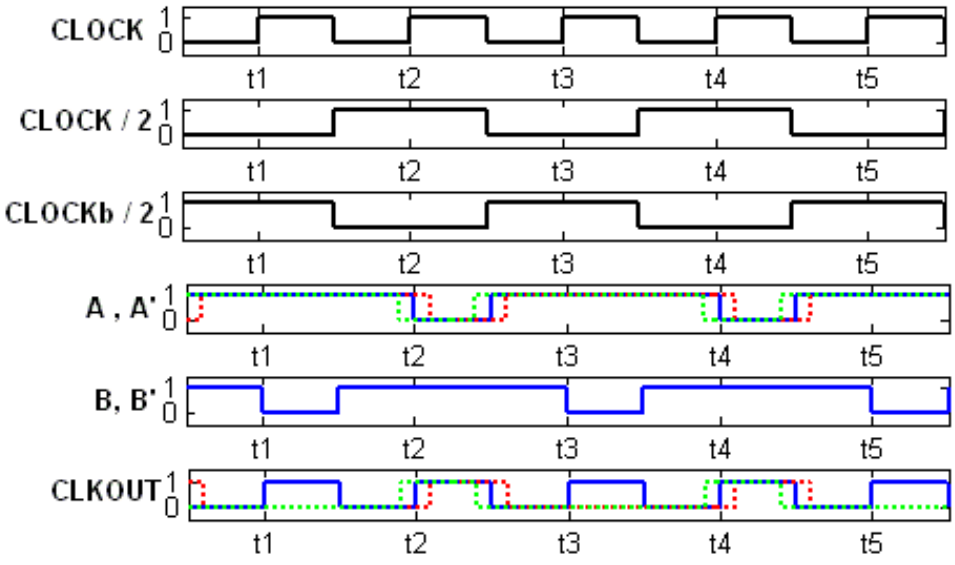
Figure 3.7: A TI-ADC with the Proposed Timing Skew Correction Circuit [1]

In Figure 3.7, each sub ADC has a correction circuit associated with it, such that any timing skew on the clock can be corrected by adjusting the delay introduced by the correction circuit itself. It is important to note that only the relative difference in timing between each sub ADC matters and that if the delay/skew introduced by each correction circuit is set to be equal for each, the timing skew will still exist. Also, note that the correction circuit itself could be made a part of either the sub ADC or the clock generation circuit.

Although Figure 3.7 represents the manner in which the correction circuit should be implemented in a TI-ADC, it does not represent the best way to test and prove the circuit architectures ability to correct timing skews. The reason for this comes from Chapter 2's description of the other mismatches that occur within a TI-ADC. To best prove the circuits' ability, the chance of having gain or offset mismatches must be eliminated completely. One way to do this is to test the circuit with a single ADC, which eliminates the possibility of any mismatches. However, the single ADC needs to operate in a way that allows the proposed correction circuit to introduce non-uniform sampling, while allowing the degree of non-uniform sampling to be adjusted. Figure 3.8 shows a circuit and its operation, which does just this. Note Figure 3.8 presents a single-ended version of the test architecture however, in this thesis a differential version is used [5].



a) Schematic



b) Operation

Figure 3.8: Schematic and Operation of the Proposed Test Architecture

Figure 3.8 (b) shows that when a clock CLK_{IN}, whose frequency corresponds to the maximum sample rate F_{SAMPLE} of the ADC, is input to the test architecture, it is first gated through two NAND gates by $CLK_{IN}/2$ and $\overline{CLK_{IN}}/2$. This produces two signals A and B which are 75% duty cycle clocks, shifted with respected to one another by one period of CLK_{IN}. Signal A passes through a variable delay buffer, while signal B passes through a fixed delay buffer whose delay is set at half of the entire delay adjustment range of the variable delay buffer. The resulting signals, A' and B' are then recombined using the final NAND gate to produce CLK_{OUT}, which has the same frequency as CLK_{IN} but has one set of rising edges (dashed lines) controlled by signal A', and a second set of rising edges (solid lines) controlled by signal B'. When the variable delay buffer controlling signal A' is set to the same delay as the fixed delay buffer controlling signal B', the output CLK_{OUT} is a standard 50% duty cycle clock (ideally). This allows the ADC, which samples on the rising edges of CLK_{OUT}, to sample A_{IN} uniformly since the time between each rising edge is equal. Note that the time between each rising edge, or between a dashed rising edge and solid rising edge, in this case is $1/F_{SAMPLE}$. However, if A' is shifted using the variable delay buffer to not have the same delay at B' then the time between consecutive rising edges in CLK_{OUT} are not equal and non-uniform sampling occurs.

Relating the above back to Chapter 2's definition of timing skews, if the time of a dashed rising edge is T_1, the time of the previous solid rising edge is T_2 and the ideal time between the two consecutive rising edges is $1/F_{SAMPLE}$, then (2.17) can be used to define the timing skew created by the test architecture as:

$$\Delta T_{SKEW} = (T_2 - T_1) - \frac{1}{F_{SAMPLE}} \tag{3.23}$$

Equation (3.23) shows that when the dashed rising edge and solid rising edge have a time difference between them of $1/F_{SAMPLE}$ as is the case when A' and B' have the same delay, then no timing skew exists. However, when the delay of A' is varied

away from that point using the variable delay buffer, the time difference between a dashed rising edge and the previous solid rising edge is no longer $1/F_{SAMPLE}$ and this results in a timing skew ΔT_{SKEW}. Therefore, the test architecture successfully avoids the gain and offset mismatches associated with a TI-ADC, while allowing the proposed analog timing skew correction circuit to vary the magnitude of the timing skew the single ADC sees, which can be measured by looking at the SFDR. It is important to note that when operating the single ADC in this manner, it essentially behaves as two ADCs interleaved. Therefore, the timing skew induced spurious tone that appears in the FFT output has a frequency given by (2.35).

Additional circuitry is needed for the test architecture in the form of a differential NAND to gate the two paths and recombine them (while acting as an output driver) and a differential D-Flip Flop (DFF) that is used to generate $CLK_{IN}/2$. The design of both circuits along with the design of the variable delay differential buffer is presented in Chapter 4.

3.5 Summary

Analog correction of timing skews involves adjusting the times each sub ADC samples the input signal in a TI-ADC. The adjustment of the times and corresponding correction of the timing skews is accomplished by varying the delay of each sub ADC's sampling clock. The differential buffer/inverter is analyzed in terms of its additive jitter vs. delay performance, showing that low jitter precise delay adjustments are best achieved by varying either the capacitive load of the buffer or the buffer's bias current. Two circuit architectures are then analyzed in a similar fashion, showing that both are capable of achieving precise delay adjustment over a broad delay range while having a favourable additive jitter behavior. The single variable delay differential buffer is selected as the preferred timing skew correction circuit, due to its likely lower noise/jitter gain. Finally, a test architecture that uses a

single ADC, eliminating the gain and offset mismatches associated with a TI-ADC, for the proposed timing skew correction circuit is shown. Based on this, a variable delay differential buffer, differential NAND and differential D-Flip Flop are required. The design of each circuit is presented in Chapter 4.

Chapter 4

Design of an Analog Timing Skew Correction Circuit

The design of the three main circuit blocks and their supporting circuitry for the test circuit described previously is presented in this chapter. The first design presented is that of the variable delay differential buffer which includes the variable capacitor bank load and the variable current source as well as the bias circuit. Next, the differential NAND circuit design is discussed along with its corresponding bias circuit. The design of the final main circuit block, the differential D-Flip Flip (DFF), which is composed of 2 D-latches is then presented. The final sections detail the full test chip's design, layout, and fabrication. The design, layout and fabrication is done in TSMC's 0.18μm CMOS process with the option for metal-insulator-metal (MIM) capacitors and a nominal supply voltage of 1.8 V.

4.1 Variable Delay Differential Buffer

The variable delay differential buffer is the key circuit design in this thesis, as it stands as the only circuit that is needed in a TI-ADC to correct for the timing skews aside from the digital logic to control its variable delay. Figure 4.1 shows the schematic of the variable delay differential buffer, complete with the variable capacitor load and the variable current source.

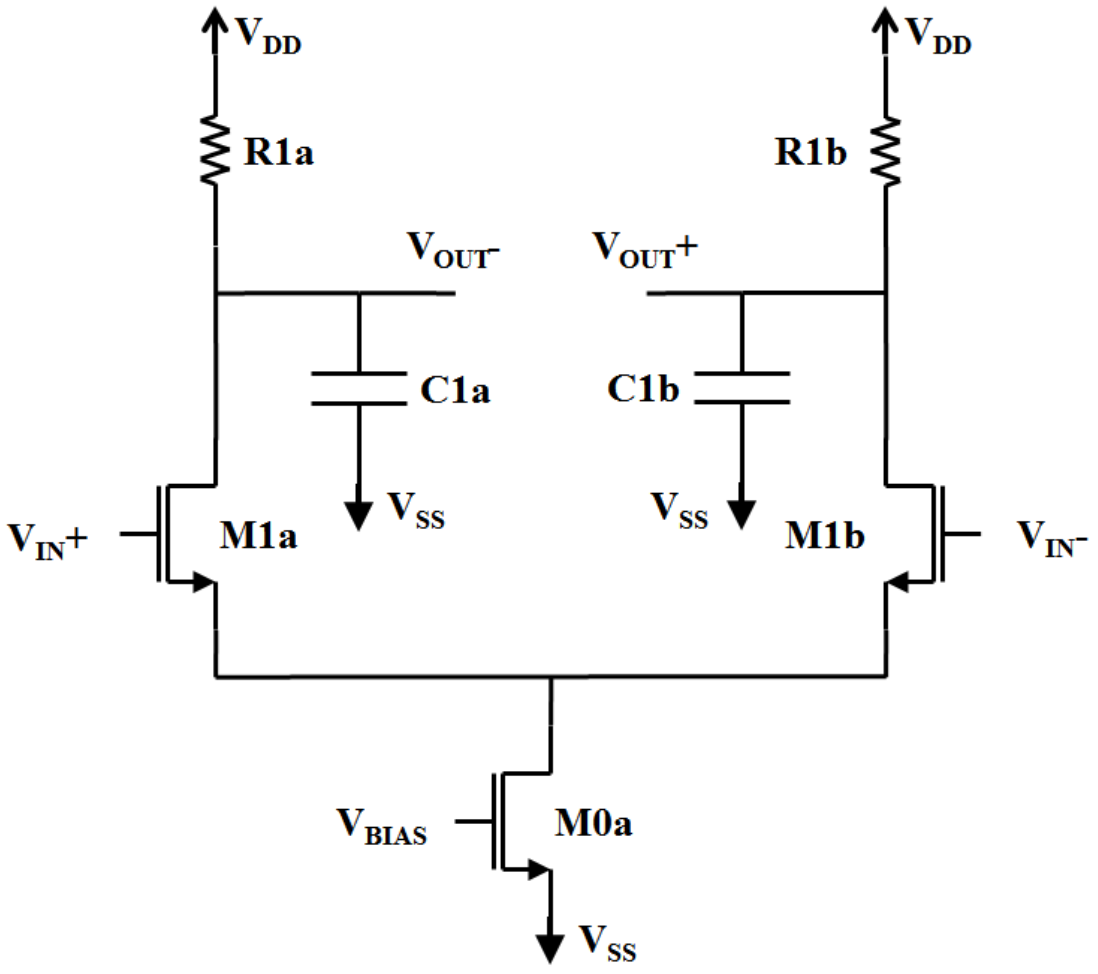


Figure 4.1: Schematic of the Variable Delay Differential Buffer

The differential architecture for the variable delay buffer is selected due to its attractive aspect of rejecting common-mode noise, either from the inputs or from the power supplies. Additionally, it is just good practice in noise and speed critical designs to use a differential architecture. In saying this, the performance goals that dictate the areas in which the design focuses on are minimizing output noise, maximizing speed/slew rate (i.e. minimizing the output jitter) and keeping the power consumption as low as possible.

4.1.1 Common-Mode and Output Swing

Three of the parameters that dictate how a differential circuit interfaces with other circuits surrounding it are its common-mode levels and its output swing. The input common-mode level V_{CMIN} is tied to the gate-to-source voltage of transistors $M1a$ and $M1b$ (V_{GS1}) and therefore will affect how they are biased and serves as the first design parameter for the differential buffer. The output common-mode level V_{CMOUT} for the differential buffer is given by:

$$V_{CMOUT} = \frac{I_{BIAS}}{2} \times R1 \tag{4.1}$$

Similarly, the single-ended output swing V_{SWING} is given by:

$$V_{SWING} = I_{BIAS} \times R1 \tag{4.2}$$

For both equations, $R1$ refers to the value of either $R1a$ or $R1b$ since both would be equal in a differential design. Equations (4.1) and (4.2) show that the output common-mode and the output swing are directly linked to one another, differing only by a factor of 2 and thus can be thought of as one design parameter.

In order to determine appropriate values for both such that the design/performance goals are met, two aspects are considered. The first and most important is how the two parameters V_{CMIN} and V_{CMOUT}/V_{SWING} relate to the output jitter. An extensive analysis of the output noise/jitter of the differential buffer/inverter is performed in [17]. According to the thesis's findings, the total rms output jitter for the differential buffer including the terms relating to V_{CMOUT} and V_{SWING} is:

$$\Delta T_{JITTER} = \sqrt{\frac{kT\varepsilon^2}{2}} \times \frac{\sqrt{C1}}{I_{BIAS}} \times \frac{V_{SWING}}{V_{GS1} - V_{T1}} \tag{4.3}$$

It is important to note that (4.3) and this thesis's approximate model of the differential buffer's jitter, (3.15), are comparable in their component dependencies, confirming the validity of the analysis and conclusions reached in Chapter 3. The terms of interest in (4.3) for the parameters currently considered are V_{GS1} and V_{SWING}. From (4.3) it is clear that in order to minimize the output jitter of the differential buffer, V_{SWING} should be minimized and V_{GS1} maximized, while insuring the circuit can still operate properly (i.e. provide sufficient swing for any following circuits and maintain M0 in saturation). This implies that V_{CMIN} should be maximized to allow for a large V_{GS1} value and V_{CMOUT} should be maximized to minimize V_{SWING}. Since both V_{CMIN} and V_{CMOUT} should be maximized and to simplify the interfacing of each of the circuits with each other, the input and output common-mode voltages are set to be the same (i.e. $V_{CMIN} = V_{CMOUT} = V_{CM}$). This restriction applies to all circuit blocks, meaning the variable delay differential buffer, differential NAND and differential DFF all have the same common-mode levels.

The second important aspect to consider in selecting V_{CM} and V_{SWING} is what V_{CM} and V_{SWING} can be tolerated by differential clock inputs to the testing ADC. The test ADC used in this thesis is Analog Devices AD9265 16-bit 125 MSPS ADC, which can tolerate a common mode voltage of up to 1.4 V on its differential clock inputs and a signal swing as low as 0.15 V peak-to-peak [18]. Therefore to allow the

test chip to directly drive the clock inputs of the AD9265 a $V_{CM} = 1.4\,V$ is selected for the differential buffer as well as the other circuit blocks.

4.1.2 Output Noise and Jitter

At the heart of the design of the variable delay differential buffer is its output noise/jitter behaviour and thus the most time is spent on it. To begin with, an $I_{BIAS} = 2\,mA$ is chosen as a start point for the bias current which corresponds to a load resistor value of $1a/b = 400\,\Omega$. As was shown in Chapter 3 and confirmed in (4.3), a high bias current is required for a low jitter design, which establishes the $2\,mA$ starting current as not unreasonable. As a starting point for the widths and lengths of $M1a/b$ and $M0a$, all are set to have $W = 1\mu m$ and $L = 180nm$. From this starting point a periodic steady state (PSS) noise and jitter analysis is performed to identify the main contributors to the output noise and jitter of the differential buffer. The resulting noise contribution break down shows that $M1a$ and $M1b$ are the largest contributors to the output noise, then the load resistors $R1a$ and R1b and after that some of the transistors in the bias network for the differential buffer and lastly $M0a$. The next step in the design process is to identify how to reduce the noise due $M1a$ and $M1b$. Note that the reduction of the output noise due to the bias network is covered in Section 4.1.4 which deals with the bias network.

The expressions for the thermal noise and flicker noise of a MOSFET in saturation are [15].

$$i_n{}^2 = \frac{8kTg_m\Delta F}{3} \tag{4.4}$$

$$i_n{}^2 = \frac{K_F g_m{}^2 \Delta F}{C_{ox} W L F} \tag{4.5}$$

Note, all of the MOSFETs at the point of interest, i.e. when the crossing threshold occurs, are in saturation by design. The transconductance g_m of the MOSFET is given by [15]:

$$g_m = \sqrt{\mu_n C_{ox} \frac{W}{2L} I_{BIAS}} \tag{4.6}$$

Substituting (4.6) into (4.4) and (4.5) results in:

$$i_n{}^2 = \frac{8kT\Delta F}{3} \times \sqrt{\mu_n C_{ox} \frac{W}{L} I_{BIAS}} \tag{4.7}$$

$$i_n{}^2 = \frac{\mu_n K_F I_{BIAS} \Delta F}{L^2 F} \tag{4.8}$$

From (4.7) and (4.8) it is clear that in order to lower the noise of a MOSFET a large L and small W is desirable. The implication of this in terms of typical bias terms is best explained by considering the following equation for the MOSFET's drain current I_D in saturation [15]:

$$I_D = \mu_n C_{ox} \frac{W}{2L} (V_{GS} - V_T)^2 \tag{4.9}$$

In order to maintain the same I_D while increasing L and decreasing W, the overdrive voltage $V_{OV} = (V_{GS} - V_T)$ needs to increase, i.e. a large V_{OV} is desirable. Additionally, the equations indicate that a low bias current is needed however; the noise is only one part of the story in lowering the output jitter.

As mentioned in the Section 4.1.1, an in depth analysis of the differential buffer/inverter's output jitter has been performed in the literature [17]. From the analysis in the thesis, the general expression for the total output jitter from the differential buffer is [17]:

$$\Delta T_{JITTER} = \sqrt{\frac{kT\varepsilon^2}{2}} \times \frac{A_V\sqrt{C1}}{I_{BIAS}} \tag{4.10}$$

In (4.10) ε is a scaling term that captures the noise contributions from $M1a/b$ and $R1a/b$ (the noise contribution from $M0a$ in the thesis's analysis is assumed zero for the operating point of concern). A_V is the small-signal gain of the differential buffer, which is given by [17]:

$$A_V = g_{m1} \times R1 = \frac{2(\frac{I_{BIAS}}{2})}{(V_{GS1} - V_{T1})} \times \frac{V_{SWING}}{I_{BIAS}} \tag{4.11}$$

If (4.11) is substituted into (4.10), the resulting expression is (4.3) from the previous section. As (4.11) shows (and is expected), increasing not decreasing the bias current reduces the output jitter due to the output slew-rate being important to the total output jitter.

Using the results from (4.3) and (4.6) to (4.11), the following design guidelines reduce the output jitter of the differential buffer. First, it is best to have as

large a V_{OV} on $M1a/b$ as possible, while keeping enough headroom for $M0a$ to remain in saturation over process variations. To achieve a large V_{OV} requires $M1a/b$ to be sized for a small W and large L for a given constant I_{BIAS} value. As part of this A_V shrinks due to both the large V_{OV} and the smaller $R1a/b$ as part of the reduced V_{SWING} (which was optimized based off the limit on the common-mode levels from the previous section). The second guideline is to increase I_{BIAS}as necessary to reach the targeted output jitter performance after the first guideline is performed. The third and final guideline is to keep the load capacitance to a minimum, including both the parasitic capacitances due to the transistors and the variable capacitor load.

Applying the guidelines, the W and L of $M1a$ and $M1b$ are scaled until their noise contributions are comparable to $M0a$'s noise contribution. The resulting transistor size for $M1a$ and $M1b$ is $W = 8 \times 4.5\mu m$ and $L = 1.2\mu m$. $M0a$ is sized to ensure it remains in saturation over the process corners, resulting in a size of $W = 16 \times 2.25\mu m$ and $L = 180nm$. This forms the unit variable differential buffer, where instances are then paralleled to raise the bias current until the output jitter requirement is met. The final circuit details including simulation results are presented in Section 4.1.7.

4.1.3 Gain and Bandwidth

As was shown in the previous sections, the design decisions that reduce the output jitter are coupled with reducing the gain of the differential buffer (i.e. to reduce one is to reduce both). In terms of the gain and bandwidth of the differential buffer, the expression for the frequency response of the differential buffer is given by [15]:

$$\frac{V_{OUT}}{V_{IN}} = \frac{g_{m1}R1\left(1 - s\frac{C_{GD1}}{g_{m1}}\right)}{1 + s(C_{GD1}R1 + C_{GS1}R_S + g_{m1}R1R_SC_{GD1}) + s^2R1R_SC_{GD1}C_{GS1}} \quad (4.12)$$

From this the dominant pole, which sets the -3 dB bandwidth for the circuit, is obtained yielding [15]:

$$P_1 = \frac{1}{R_S\left(C_{GS1} + C_{GD1}\left(1 + g_{m1}R1 + \frac{R1}{R_S}\right)\right)} \quad (4.13)$$

In (4.12) and (4.13), all of the terms except for R_S and R_1 depend on the sizing and biasing of transistors $M1a/b$. R_S represents the source resistance of the circuit driving the differential buffer, which ends up being the same value as R_1 since all circuit blocks are designed with the same common-mode levels. In saying all of this, the steps and analysis performed to reduce the output jitter from the previous section already set the parameters within these two equations. Therefore, the gain and bandwidth of the differential buffer cannot be design independently from the output noise/jitter design. However, the transistor sizing decisions from the previous section do work to reduce gain and bandwidth. For example, in sizing $M1a/b$ for a large V_{OV} value the gate area of the transistor increases, increasing C_{GS1}, which reduces the bandwidth of the differential buffer. The final circuit's simulated gain and bandwidth is shown in Section 4.1.7.

4.1.4 Bias

The bias for the variable delay differential buffer is established with a replica bias circuit. The schematic for the replica bias circuit is shown in Figure 4.2.

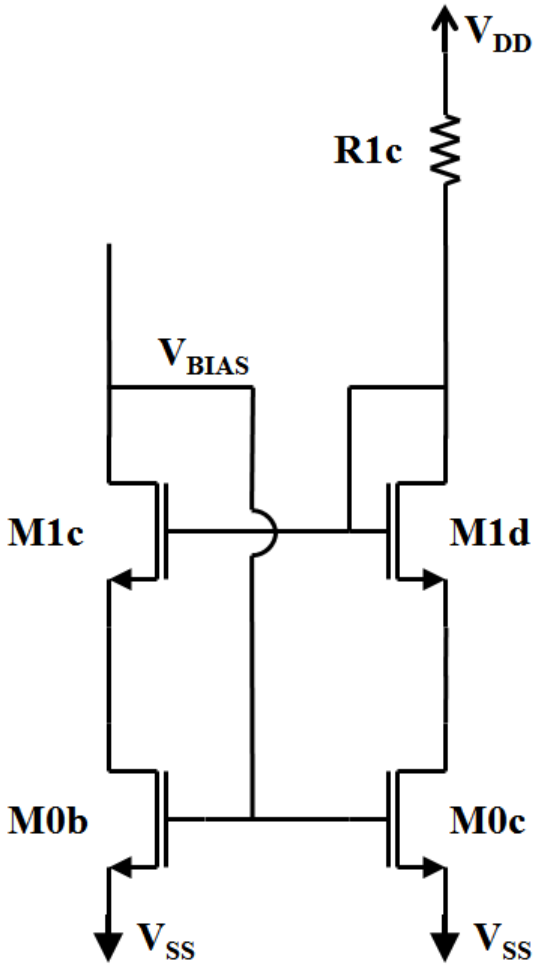


Figure 4.2: Replica Bias Circuit for the Variable Delay Differential Buffer

There are two design aspects to the bias circuitry, the first is the circuit parameter(s) or performance the bias is intended to set and the second is the desired current mirroring ratio between the master bias current input to the V_{BIAS} node and I_{BIAS} in the differential buffer. Dealing with the first aspect, the replica bias circuit is designed around the input and output common-mode voltages being the same. The reason for this is that the output common-mode voltage sets the crossing threshold for the rising edge (or falling edge) and thus sets when the ADC samples and correspondingly the

time point which needs to be varied to correct the timing skews in TI-ADCs. Therefore, it is important to set the biasing of the transistors in the differential buffer based off the crossing threshold/output common-mode voltage to ensure the jitter and timing at the threshold is controlled. In addition, since the bias point of the transistors sets their performance and process variations can shift the design points, the bias current I_{BIAS} is brought out to a pad to be set and controlled externally. This provides the simplest means of tuning the performance of the differential buffer to compensate for process variations or potential design errors.

It is important to note that the bias circuitry contributes a significant amount of noise and thus jitter to the output of the differential buffer as any noise in the bias circuitry is amplified by the gain $M0a$ to the output. To reduce the noise due to the bias circuitry a large 10µF filtering capacitor is placed on the V_{BIAS} node, which would be placed externally on the test chip's printed circuit board since the node is brought out of the chip. If an external filtering capacitor is not viable, switched-capacitor techniques can be used to provide filtering.

For the second design aspect of the bias network, the mirroring ratio, is selected to be 1:8 for the final sizing of the variable delay differential buffer. Once again, the final device sizes for the bias circuitry are shown in Section 4.1.7.

4.1.5 Variable Capacitor Load

The analysis in Chapter 3 showed that the best way to correct for timing skews with the differential buffer is to adjust the output delay by adjusting the capacitive load on the output. To accomplish this, a variable capacitor bank (represented by $C1a/b$ is designed using the MIM capacitors in the 0.18µm process. Given the importance of achieving the smallest delay step possible with the capacitor bank to give the best

precision when correcting timing skews, the capacitor bank is designed around the smallest capacitor available in the 0.18µm process. The smallest capacitor, referred to as a unit capacitor, is achieved with a $4\mu m \times 4\mu m$ MIM capacitor, which yields a capacitance of 20.3 fF. The next step in the design of the variable capacitor bank is deciding how the array of unit capacitors is switched to connect/disconnect them from the output of the differential buffer. Previous work found that it is best, in terms of smallest capacitor array area and the least parasitic capacitance, to connect the unit capacitors that form the array to the output in a single-ended fashion [5]. Figure 4.3 shows the final single ended capacitor array.

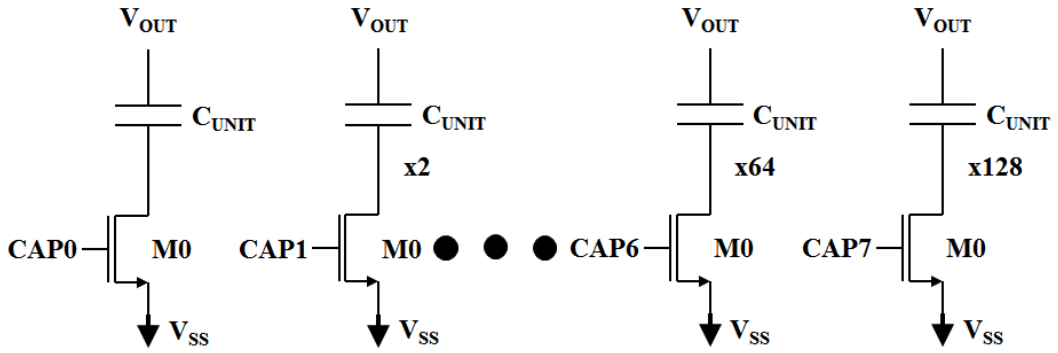


Figure 4.3: Final Variable Capacitor Load

Two instances of the variable capacitor load are required, one to load V_{OUT+} and one to load V_{OUT-} since both signals form the differential pair and need to be delayed equally.

The final capacitor bank size is determined by scaling the number of unit capacitors forming the array in a binary fashion until the designed delay range is achieved. This results in an array of 255 unit capacitors that are switched in binary weighted arrays, each consisting of the appropriate number of unit capacitors paralleled together as shown in Figure 4.3. In addition to the sizing of the array, the other design aspect of the variable capacitor load is sizing the MOSFET switch. As

discussed in the output jitter section, minimizing the capacitive load is important to ensure as low an output jitter as possible. This implies that the MOSFET switch should be sized as small as possible to ensure the parasitic capacitance between the drain-to-bulk/substrate, which appears in series with the MIM capacitor, is as small as possible. The final size for the MOSFET switch is $W = 1 \times 1\mu m$ and $L = 180nm$. This is not the smallest MOSFET possible however, it is the smallest that allows two contacts to the drain and source of the MOSFET. The two drain/source contacts are done to ensure a reliable connection (i.e. if one contact is manufactured incorrectly, the other allows the circuit to still function). The final variable capacitor load generates a post-layout extracted delay range of approximately 150 ps, with step sizes of approximately 600 fs at the output of the test chip with 8 control bits.

4.1.6 Variable Current Source

The 600 fs step size from the variable capacitor load is not precise enough, therefore as suggested in Chapter 3, a variable current source is needed in order to reach the desired 25 fs step size. The design of the variable current source is approached in the same manner as the variable current source. Relative to the main current source for the differential buffer $(M0a)$, a smaller current source is added in parallel that allows the output delay to change by the desired step size of 25 fs. This forms the unit current source, which adds 15.625 µA of current and can be shut off as shown in Figure 4.4.

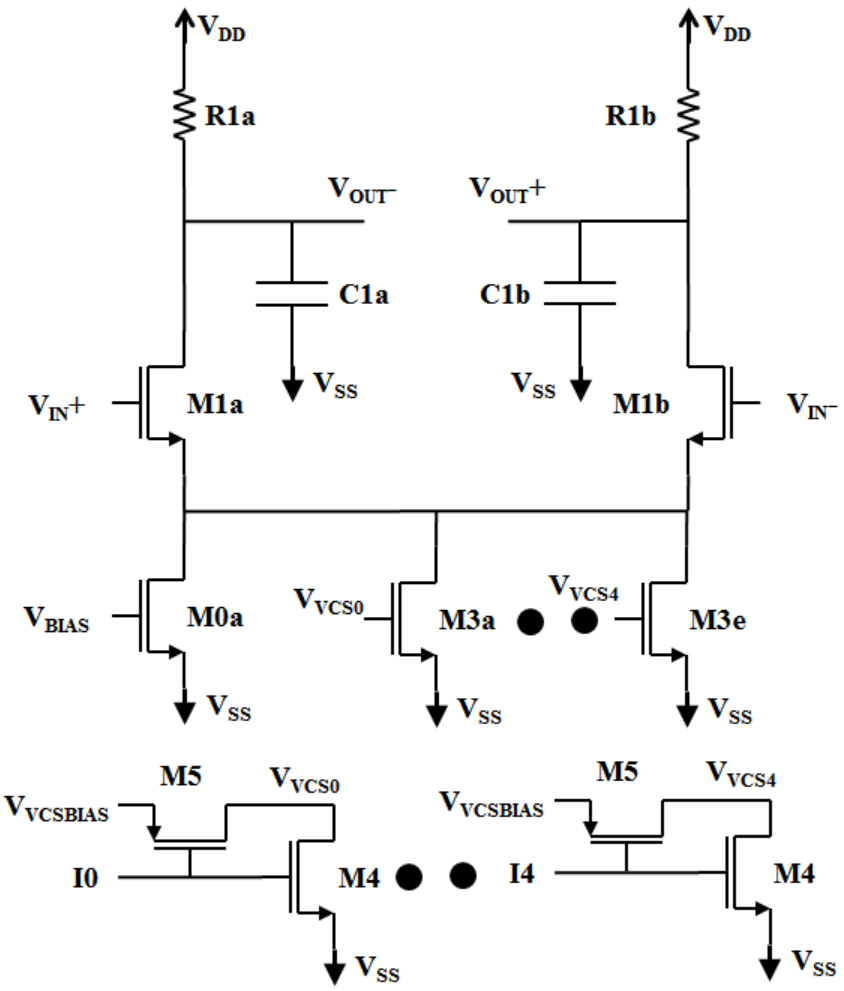


Figure 4.4: Variable Current Source Added to The Variable Delay Differential Buffer

As in the case of the variable capacitor load, more unit current sources are added in a binary switched fashion until the step size of variable capacitor load is covered with margin for process variation. This results in 5 control bits for the variable current source, where the simulated current for each of the most significant bits (MSBs) is given in Table 4.1.

Table 4.1: Variable Current Source's Switch Currents

Variable Current Source Bit	Additional Bias Current Added (µA)
I0	15.8
I1	31.6
I2	63.16
I3	126.18
I4	251.8

In order to allow for the variable current source to be biased independently of the main bias for the differential buffer, a duplicate scaled version of the main bias circuitry shown in Figure 4.2 is used with a master bias current on V_{BIAS} of 250 µA supplied externally. The final sizing of the transistors used in the variable current source and its corresponding bias circuit are presented in Section 4.1.7

4.1.7 Final Circuit and Simulation Results

The final circuit is simulated at an approximated die temperature of 60 degrees Celsius. The final sizes and bias currents for the full variable delay differential buffer are shown in Table 4.2.

Table 4.2: Final Device Sizes and Bias Currents for the Variable Delay Differential Buffer

Component	Width	Length	Bias Current
$M1a, M1b$	$16 \times (8 \times 4.5\mu m)$	$1.2\mu m$	$16 \times (1\ mA)$
$M0a$	$16 \times (16 \times 2.25\mu m)$	$180nm$	$16 \times (2\ mA)$
$R1a, R1b$ [~25 Ω effective]	$16 \times (4 \times 2.5\mu m)$	$14.4\mu m$	$16 \times (1\ mA)$

The values in parentheses in Table 4.2 correspond to the sizes for the unit differential buffer and the 16 times multiplier represents the 16 parallel instances of the unit differential buffer to make the final circuit. The resistors $R1a/b$ are poly resistors whose equivalent resistance at 60 degrees Celsius for the final differential buffer is approximately 25 Ω. The final sizes and bias currents for the replica bias circuit are shown in Table 4.3.

Table 4.3: Final Device Sizes and Bias Currents for the Differential Buffer Bias Circuitry

Component	**Width**	**Length**	**Bias Current**
$M1c$	$2 \times (8 \times 4.5\mu m)$	$1.2\mu m$	$2 \times (1\ mA)$
$M1d$	$2 \times (2 \times 4 \times 4.5\mu m)$	$1.2\mu m$	$2 \times (2 \times 500\ \mu A)$
$M0b$	$2 \times (8 \times 2.25\mu m)$	$180nm$	$2 \times (1\ mA)$
$M0c$	$2 \times (2 \times 4 \times 2.25\mu m)$	$180nm$	$2 \times (2 \times 500\ \mu A)$
$R1c$ [~200 Ω effective]	$2 \times (2 \times 2 \times 2.5\ \mu m)$	$14.4\ \mu m$	$2 \times (2 \times 500\ \mu A)$

The sizing and currents for the final unit current source that forms the basic building block for the variable current source and its bias circuit are shown in Table 4.4 and Table 4.5.

Table 4.4: Final Device Sizes and Bias Currents for the Unit Current Source

Component	**Width**	**Length**	**Bias Current**
$M3a$	$1 \times (1 \times 1.5\mu m)$	$540nm$	$1 \times (15.8\ \mu A)$
$M3b$	$2 \times (1 \times 1.5\mu m)$	$540nm$	$\sim 2 \times (15.8\ \mu A)$
$M3c$	$4 \times (1 \times 1.5\mu m)$	$540nm$	$\sim 4 \times (15.8\ \mu A)$
$M3d$	$8 \times (1 \times 1.5\mu m)$	$540nm$	$\sim 8 \times (15.8\ \mu A)$
$M3e$	$16 \times (1 \times 1.5\mu m)$	$540nm$	$\sim 16 \times (15.8\ \mu A)$
M4	$1 \times (2 \times 6\mu m)$	$180nm$	$0\ mA$
M5a	$1 \times (2 \times 4\mu m)$	$180nm$	$0\ mA$

Table 4.5: Final Device Sizes and Bias Current for the Variable Current Source Bias Circuitry

Component	**Width**	**Length**	**Bias Current**
M1c, M1d	$1 \times (2 \times 4.5\mu m)$	$1.2\mu m$	$1 \times (250\ \mu A)$
M3f, M3g	$1 \times (16 \times 1.5\mu m)$	$180nm$	$1 \times (250\ \mu A)$
R1c [~1600 Ω effective]	$1 \times (1 \times 2.5\mu m)$	$14.4\mu m$	$1 \times (250\ \mu A)$

The parasitic extracted post-layout simulation results for the final design of the differential buffer are shown in Figure 4.5 to Figure 4.8. First, Figure 4.5 shows the transient response illustrating the designed 1.4 V output common-mode voltage and the approximate 0.8 V peak-to-peak output voltage swing for the 125 MHz frequency the differential buffer is designed to handle.

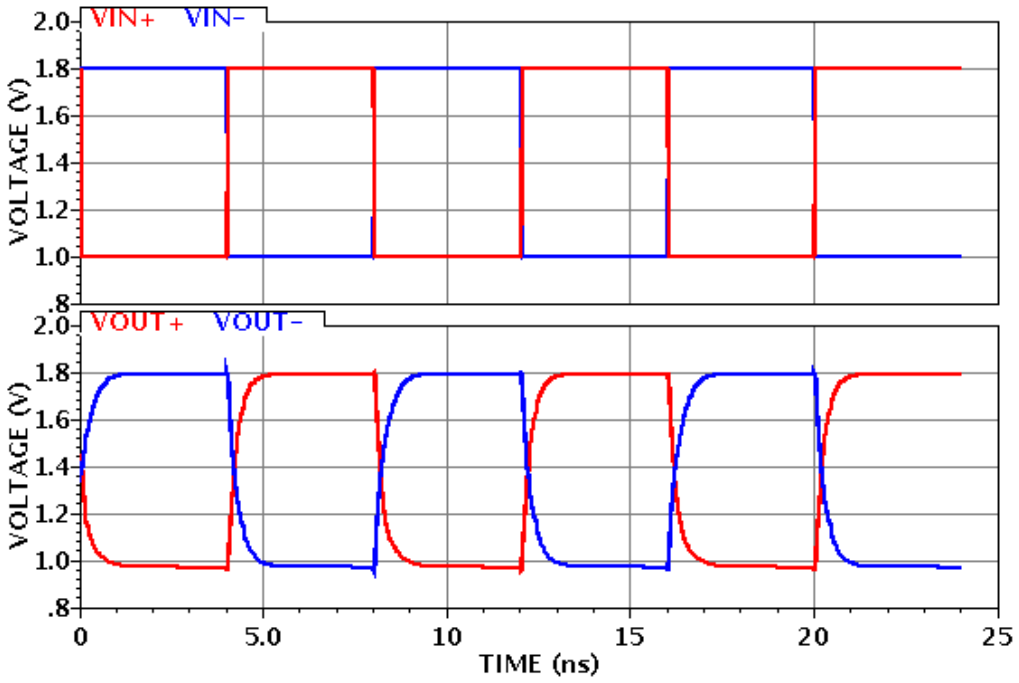


Figure 4.5: Simulated Transient Response of the Variable Delay Differential Buffer

A magnified plot of the rising and falling edge of V_{OUT+} along with the slope of the output for the worst case jitter scenario (i.e. the maximum capacitor load corresponding to code 255) is shown in Figure 4.6. The slope of $1.8732\ GV/s$ indicated on the figure is taken at the crossing threshold for the edge with the slowest slew-rate. Using (3.4) and the total integrated output noise of $45.64\ \mu V/\sqrt{Hz}$ in Figure 4.7 results in a total rms output jitter of:

$$\Delta T_{JITTER(DLY)} = \frac{45.64\ \frac{\mu V}{\sqrt{Hz}}}{1.8732\ GV/s} = 24.36\ fs \tag{4.14}$$

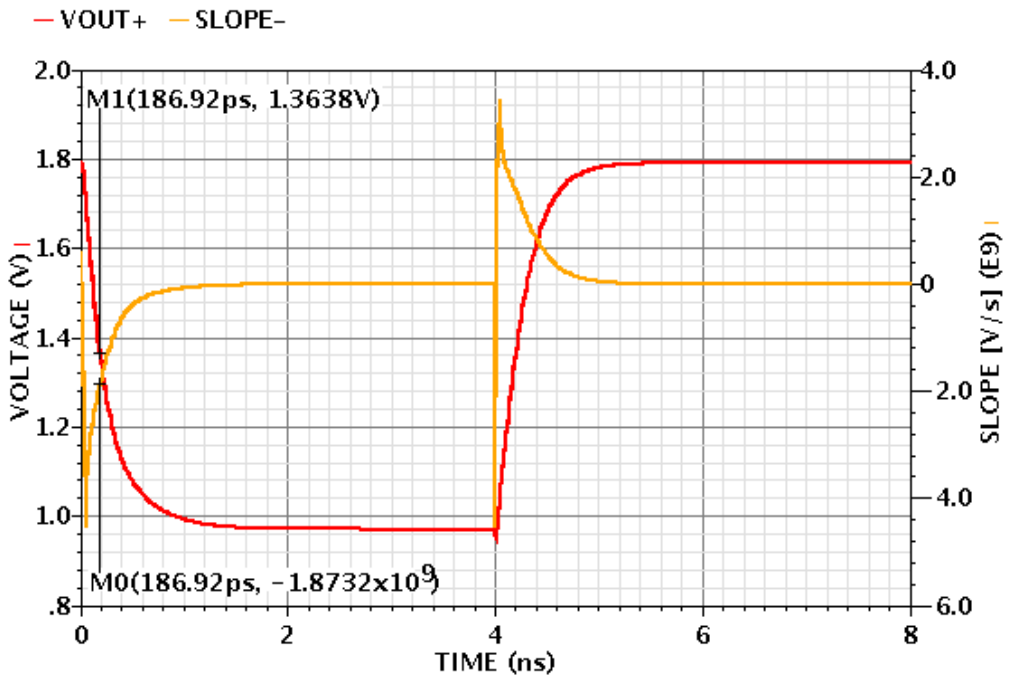


Figure 4.6: Simulated Slope of the Worst-Case Slew-Rate Edge for the Differential Buffer

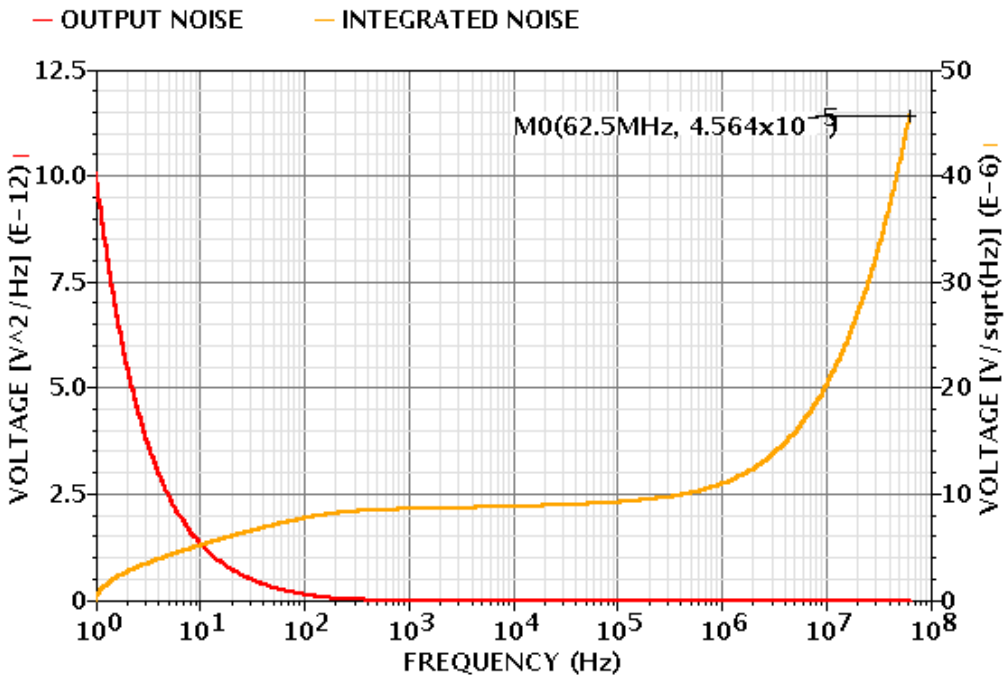


Figure 4.7: Simulated Total Output Noise for the Differential Buffer

The resulting jitter for the output meets the design goal of 25 fs. Figure 4.8 shows the final differential buffer's gain and bandwidth for the output jitter-optimized circuit.

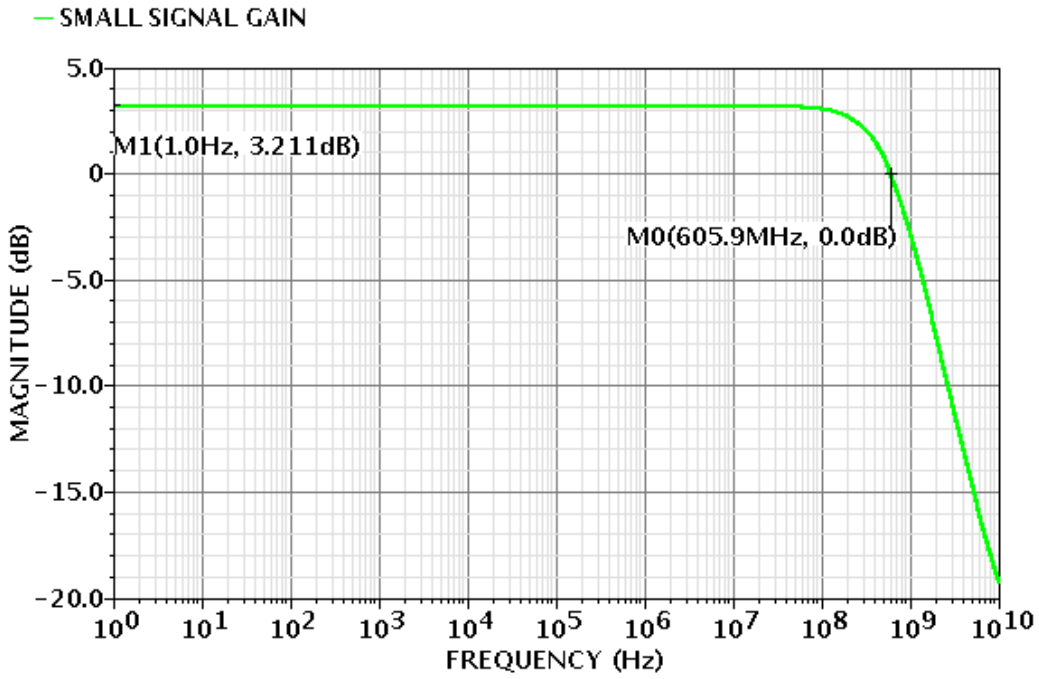


Figure 4.8: Simulated Gain and Bandwidth of the Differential Buffer

To ensure the circuit would still operate as expected under process variations, corner case simulations are run, ensuring that $M0a$ remains in saturation and no unusual behaviour is observed.

4.2 Differential NAND

The design of the differential NAND is approached in the exact same manner as that of the differential buffer since the same noise/jitter trends in sizing the transistors apply. In previous low noise/jitter designs using differential or current-mode logic (CML) NANDs, two architecture's that are not well suited to differential signalling

principles were used [5], [19]. A schematic similar to these architectures that illustrates the differential signalling issue is shown in Figure 4.9.

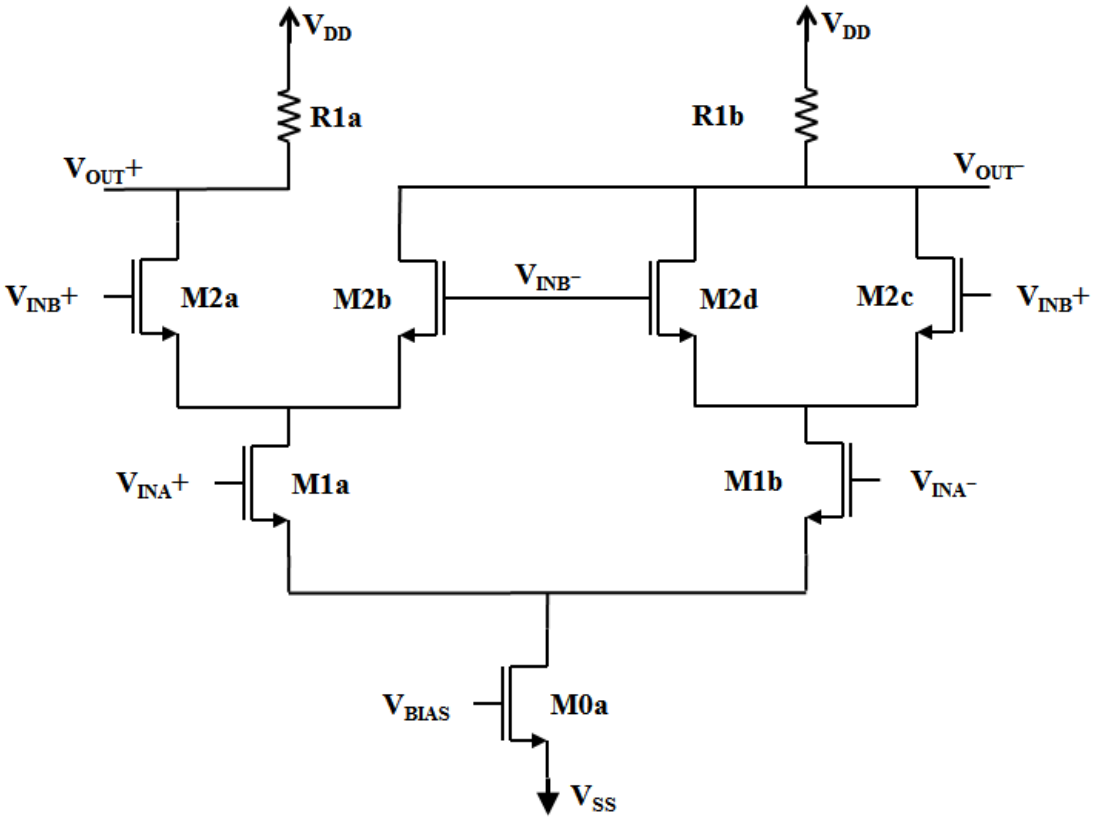


Figure 4.9: Schematic of a CML NAND Gate [19]

The issue in terms of the differential signalling with the circuit in Figure 4.9 is the imbalance in the parasitic capacitances. For example, on the $OUT-$ node there are 3 MOSFET drains each having their own set of parasitic capacitances whereas on the $OUT+$ node there is only one MOSFET drain and thus one set of parasitic capacitances (assuming all transistors are the same size). This imbalance usually gives rise to distortion in differential circuits as well as giving different delay times on the positive and negative signalling lines. To solve this issue, an alternative differential/CML NAND architecture is proposed. The schematic for the proposed differential NAND designed for the test chip is shown in Figure 4.10.

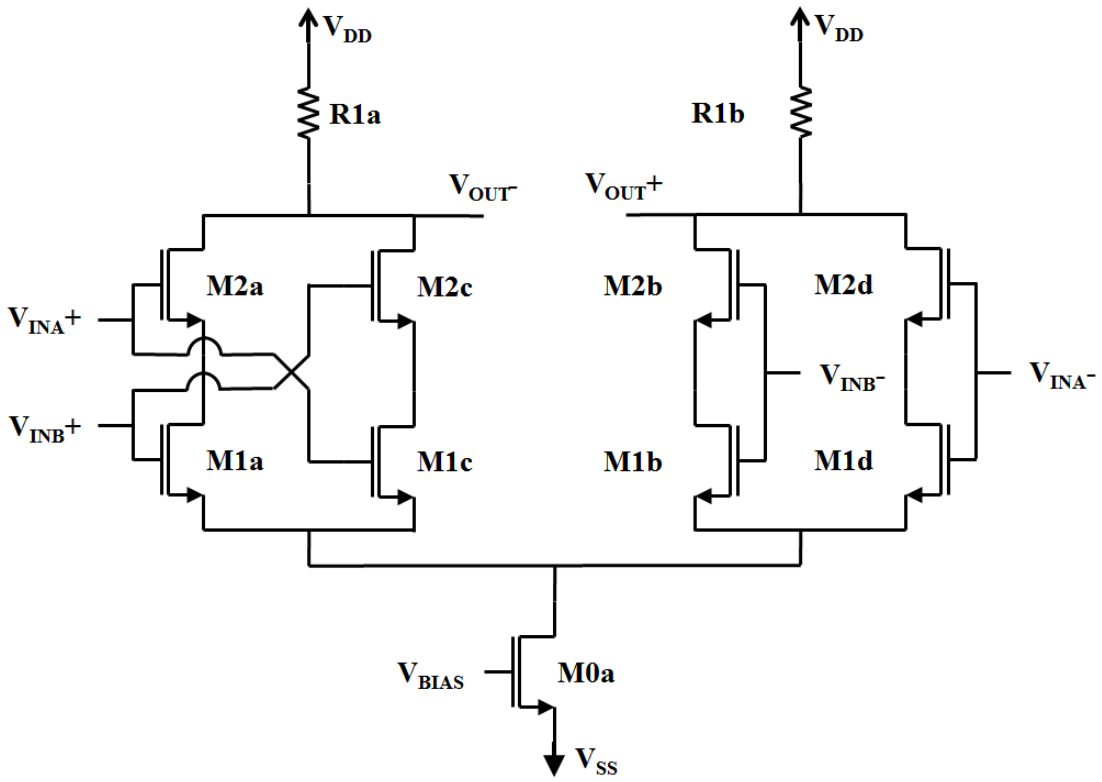


Figure 4.10: Schematic of the Proposed Differential NAND Circuit

As is seen from Figure 4.10, if $M1a$ to $M1d$ and $M2a$ to $M2d$ all have the same sizes, then all the differential inputs and outputs of the NAND will have equal parasitic capacitances on the positive and negative signalling lines. This ensures good differential behaviour since all signalling and parasitics are symmetric.

The differential NAND circuit shares the same design requirements as the differential buffer, i.e. low jitter, low gain and the same 1.4 V input and output common-mode levels. This combined with the similar circuit structure, means the same principles governing the design of the differential buffer can be applied to the differential NAND. The point of the similar circuit structure comes from the idea that the input transistor for the differential buffer can be split apart (length and width

wise) to form the inputs to the differential NAND. This allows the NAND to maintain enough voltage headroom such that $M1a$ to $M1d$ and $M2a$ to $M2d$ have the proper operating point for the common-mode levels given the double vertical stack of transistors. The final transistor sizing's for $M1a$ to $M1d$ and $M2a$ to $M2d$ for the unit differential NAND are $W = 8 \times 4.5\mu m$ and $L = 600nm$. The resistor and bias transistor sizing's for the unit differential NAND are duplicates of the unit differential buffer's. Additionally, the differential NAND uses a replica bias circuit designed in the same fashion as that of the differential buffer's. Figure 4.11 shows the schematic of the differential NAND's replica bias circuit, with the final sizing shown in the following section.

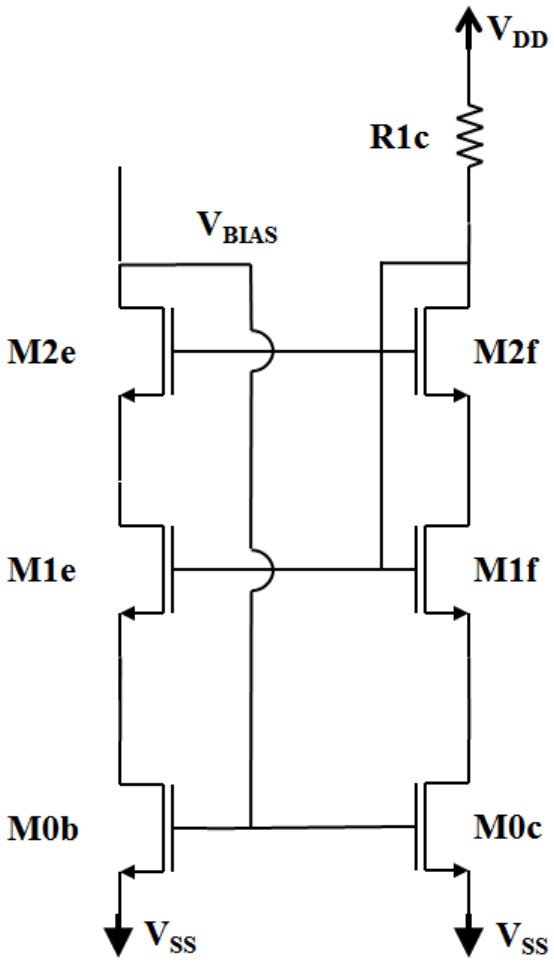


Figure 4.11: Schematic of the Differential NAND Replica Bias Circuit

Just as in the differential buffer's case, the final differential NAND gates in the design consist of multiple parallel instances of the unit cell whose sizing is tabulated in the next section.

4.2.1 Final Circuit and Simulation Results

The differential NAND is simulated under the same conditions (60 degrees Celsius and post-layout) as the differential buffer. In addition, the differential NAND is simulated for its two operating scenarios (path gating device and path recombining/output device) by varying the capacitive load the final differential NAND sees. The NAND's used for both operating scenarios share the same final sizing's, 16 parallel instances of the unit differential NAND. The final component sizes for the differential NAND and its replica bias circuit are shown in Table 4.6 and Table 4.7.

Table 4.6: Final Device Sizes and Bias Currents for the Differential NAND

Component	**Width**	**Length**	**Bias Current**
$M1a, M1b, M1c, M1d, M2a, M2b, M2c, M2d$	$16 \times (8 \times 4.5\mu m)$	$600nm$	$16 \times (500\ \mu A)$
$M0a$	$16 \times (16 \times 2.25\mu m)$	$180nm$	$16 \times (2\ mA)$
$R1a, R1b$ [~25 Ω effective]	$16 \times (4 \times 2.5\mu m)$	$14.4\mu m$	$16 \times (1\ mA)$

Table 4.7: Final Device Sizes and Bias Currents for the Differential NAND Bias Circuit

Component	Width	Length	Bias Current
$M1e, M2e$	$2 \times (16 \times 4.5\mu m)$	$600nm$	$2 \times (1\ mA)$
$M1f, M2f$	$2 \times (2 \times 8 \times 4.5\mu m)$	$600nm$	$2 \times (2 \times 500\ \mu A)$
$M0b$	$2 \times (8 \times 2.25\mu m)$	$180nm$	$2 \times (1\ mA)$
$M0c$	$2 \times (2 \times 4 \times 2.25\mu m)$	$180nm$	$2 \times (2 \times 500\ \mu A)$
$R1c$ [~200 Ω effective]	$2 \times (2 \times 2 \times 2.5\mu m)$	$14.4\mu m$	$2 \times (2 \times 500\ \mu A)$

The two capacitive loads used to simulate the two operating scenarios for the differential NAND are 5 pF single-ended on each output node (path gating device) and 100 pF single-ended on each output node (output driver). Note that when using the differential NAND as the output driver it should be able to drive a 100 Ω differential load for proper termination. Given the approximate 50 Ω differential load (2×25 Ω single-ended) the final differential NAND naturally drives, this is not an issue. The final post-layout simulated transient response of the differential NAND for the two capacitive loads/operating scenarios is shown in Figure 4.12.

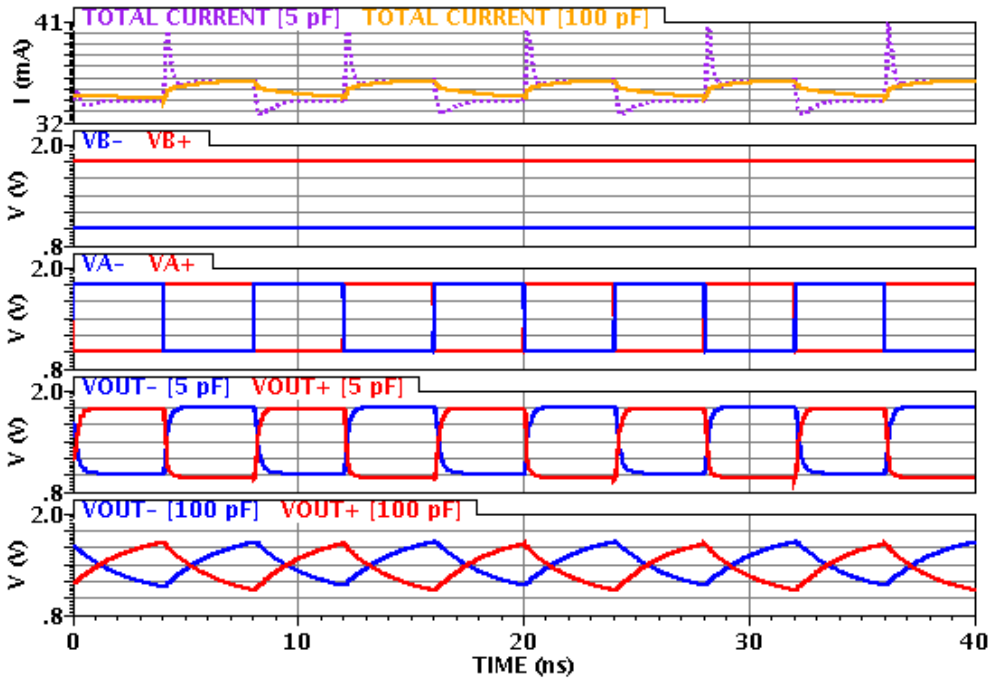


Figure 4.12: Simulated Transient Response of the Differential NAND

From Figure 4.12 it is easy to see the reduced slew-rate of the differential NAND gate when it is operating as the path recombining/output driver due to the significantly larger capacitive load. Due to the large capacitive load, the jitter analysis in either (3.15) or (4.3) and the simulated jitter of the designed differential buffer, it is expected that the output driver NAND is the dominant jitter source in the overall test circuit. The total worst-case output jitter for the differential NAND gate with the 100 pF load is calculated from the worst-case output slope in Figure 4.13 and the total integrated noise in Figure 4.14 and is shown in (4.15).

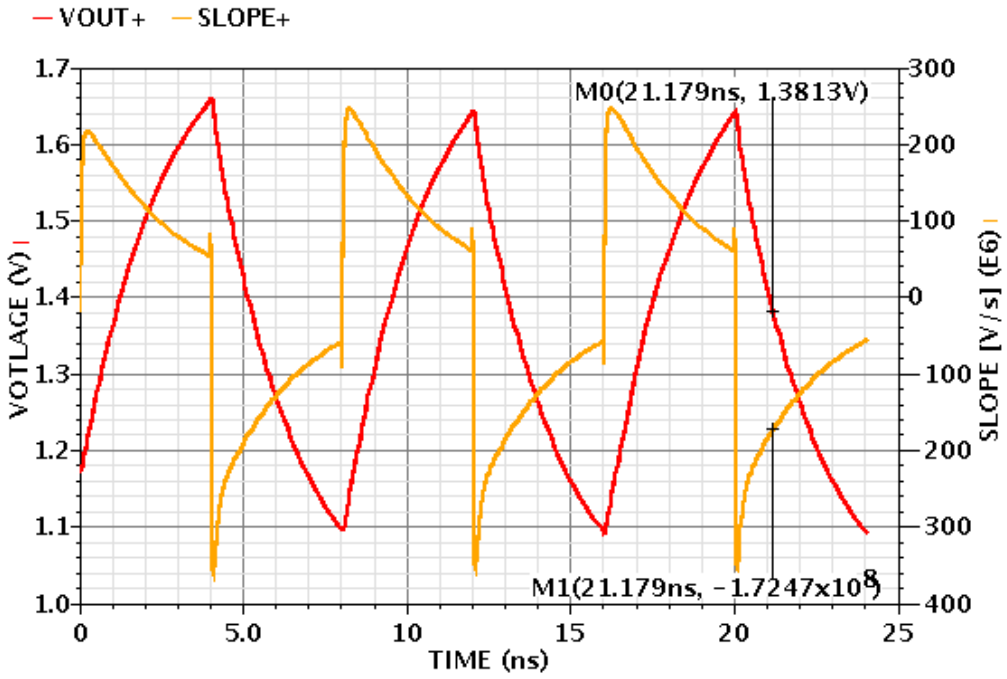


Figure 4.13: Simluated Slope of the Worst-Case Slew-Rate Edge for the Differential NAND with a 100 pF Load

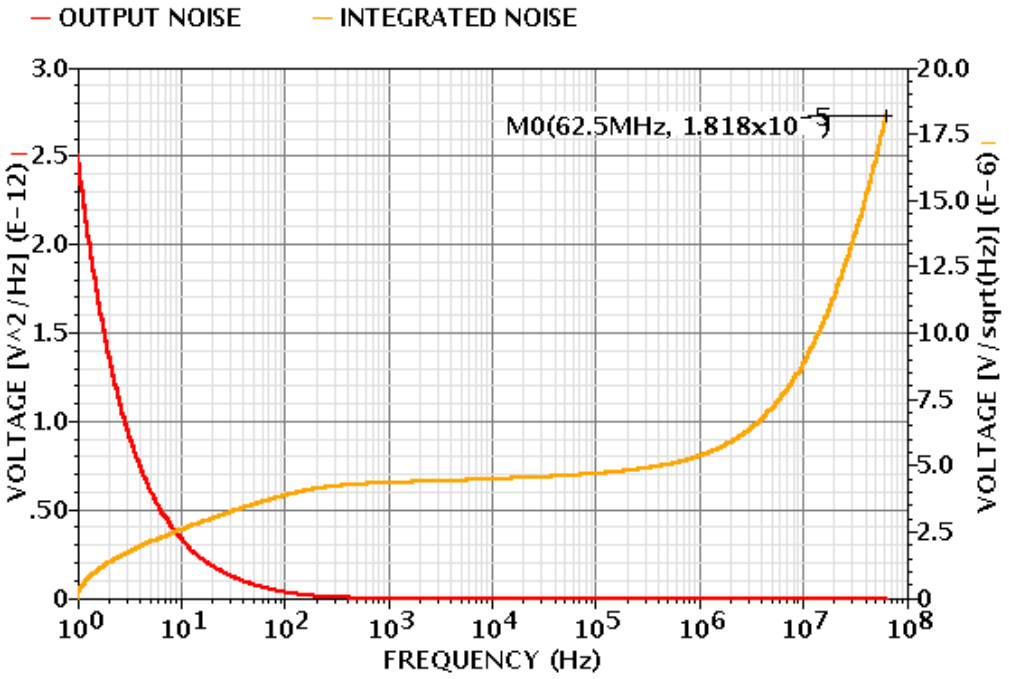


Figure 4.14: Simulated Total Output noise for the Differential NAND with a 100 pF Load

$$\Delta T_{JITTER(100\,pF)} = \frac{18.18\ \frac{\mu V}{\sqrt{Hz}}}{0.1725\ GV/s} = 105.39\ fs \tag{4.15}$$

As expected, the 105.39 fs of rms output jitter for the output driver differential NAND is much higher than that of variable delay buffer's 24.36 fs. The total rms output jitter of the differential NAND when acting as the path gating device (5 pF load) is also simulated, but at lower accuracy (i.e. less jitter than the circuit will actually have) due to time constraints and determined to be approximately 16 fs. However, using a quick calculation based on (4.3) and the difference in the capacitive

loads between the two operating scenarios, another approximation of the rms output jitter for the path gating NAND can be calculated and is shown in (4.16).

$$\Delta T_{JITTER\ (5\ pF)} \cong \frac{105.39\ fs}{\sqrt{\frac{100\ pF}{5\ pF}}} = 23.57\ fs \tag{4.16}$$

The value in (4.16) correlates well with the simulated output jitter of the variable delay differential buffer (24.36 fs) which is the most accurately simulated jitter in this thesis. Note that the two circuit's rms output jitter should be close given the similar capacitive loads (approximately 5 to 10 pF single-ended on each output node for the differential buffer) and shared design philosophies.

4.3 Differential D-Flip Flop

The design of a differential D-Flip Flop (DFF) is required in order to generate the $CLK_{IN}/2$ signal, which is accomplished by feeding back an inverted version of the DFF's output to its input. A simple way to create a differential DFF is with two differential latches as shown in Figure 4.15.

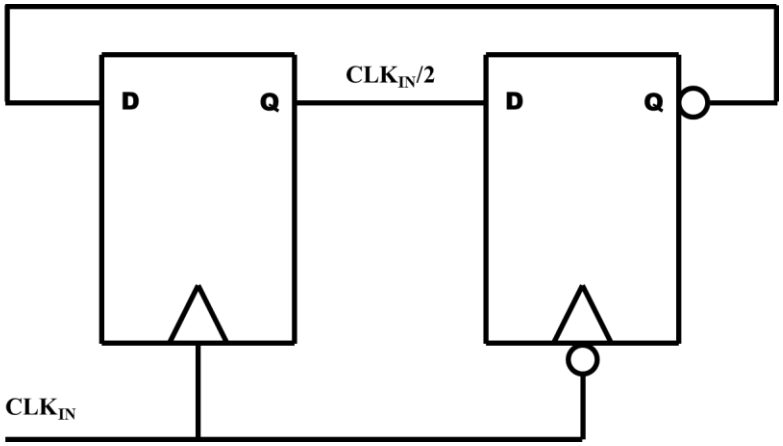


Figure 4.15: Schematic of the Differential DFF Using Two Latches

The schematic for a differential latch is shown in Figure 4.16 [19].

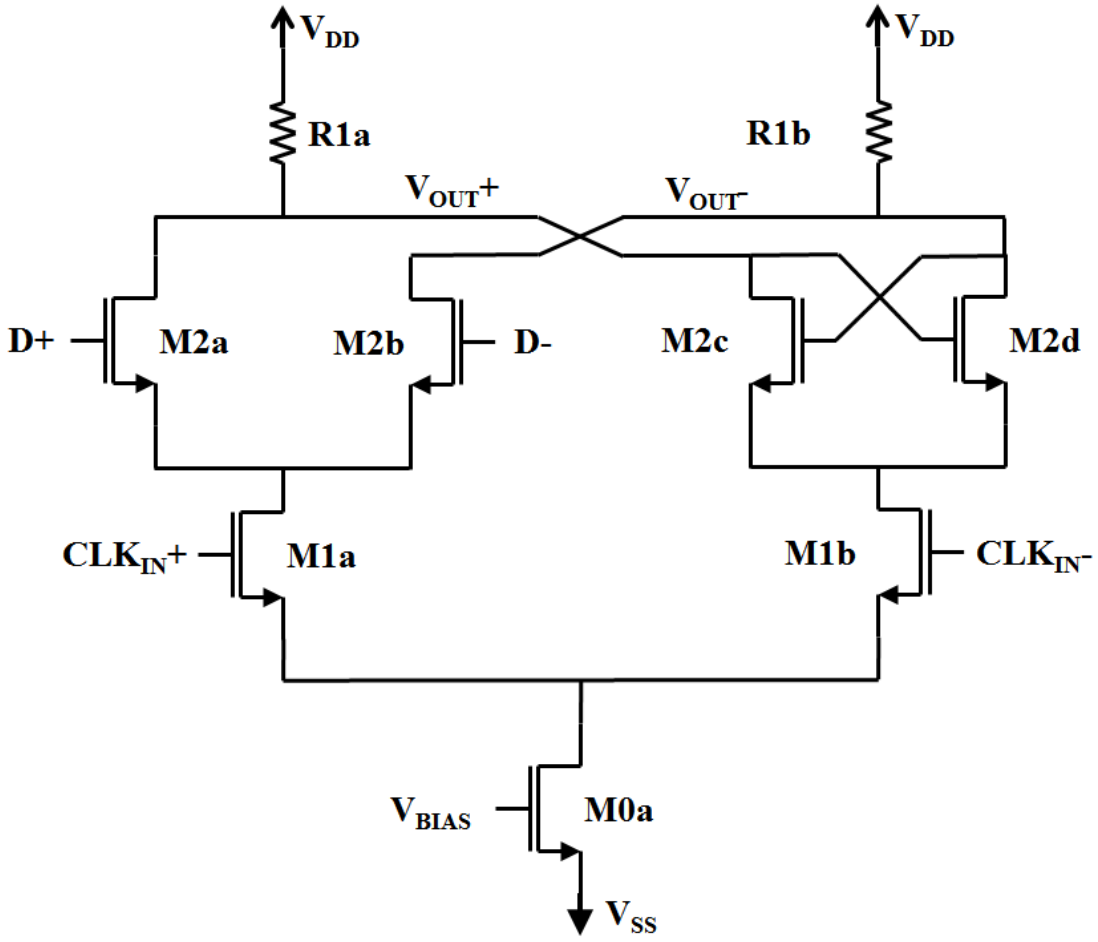


Figure 4.16: Schematic of a Differential Latch [19]

Like the differential NAND, the design of the differential latch borrows from the design of the variable delay buffer to achieve the same design goals. The unit differential latch is designed by again splitting the transistors of the variable delay buffer vertically and maintaining the widths to ensure sufficient voltage headroom. The final device sizes for the differential latch are shown in Table 4.8. Note that there are only 8 parallel instances of the differential latch to establish one half of the DFF, for layout purposes and since the output jitter of the DFF isn't important for the design.

Table 4.8: Final Device Sizes and Bias Currents for the Differential Latch

Component	Width	Length	Bias Current
$M1a$, $M1b$	$8 \times (16 \times 2.25\mu m)$	$600nm$	$8 \times (1\ mA)$
$M2a$, $M2b$, $M2c$, $M2d$	$8 \times (8 \times 4.5\mu m)$	$600nm$	$8 \times (500\ \mu A)$
$M0a$	$8 \times (16 \times 2.25\mu m)$	$180nm$	$8 \times (2\ mA)$
$R1a$, $R1b$ [~50 Ω effective]	$8 \times (4 \times 2.5\mu m)$	$14.4\mu m$	$8 \times (1\ mA)$

The replica bias circuit for the differential latch is shown in Figure 4.17 and the final device sizes are in Table 4.9.

Table 4.9: Final Device Sizes and Bias Currents for the Differential Latch Bias Circuit

Component	Width	Length	Bias Current
$M1c$, $M1d$	$1 \times (16 \times 4.5\mu m)$	$600nm$	$1 \times (1\ mA)$
$M2e$, $M2f$	$1 \times (2 \times 8 \times 4.5\mu m)$	$600nm$	$1 \times (2 \times 500\ \mu A)$
$M0b$	$1 \times (8 \times 2.25\mu m)$	$180nm$	$1 \times 1\ mA$
$M0c$	$1 \times (2 \times 4 \times 2.25\mu m)$	$180nm$	$1 \times (2 \times 500\ \mu A)$
$R1c$ [~200 Ω effective]	$1 \times (2 \times 2 \times 2.5\mu m)$	$14.4\mu m$	$1 \times (2 \times 500\ \mu A)$

Finally, the transient output of the differential DFF is plotted in Figure 4.19 in Section 4.4.

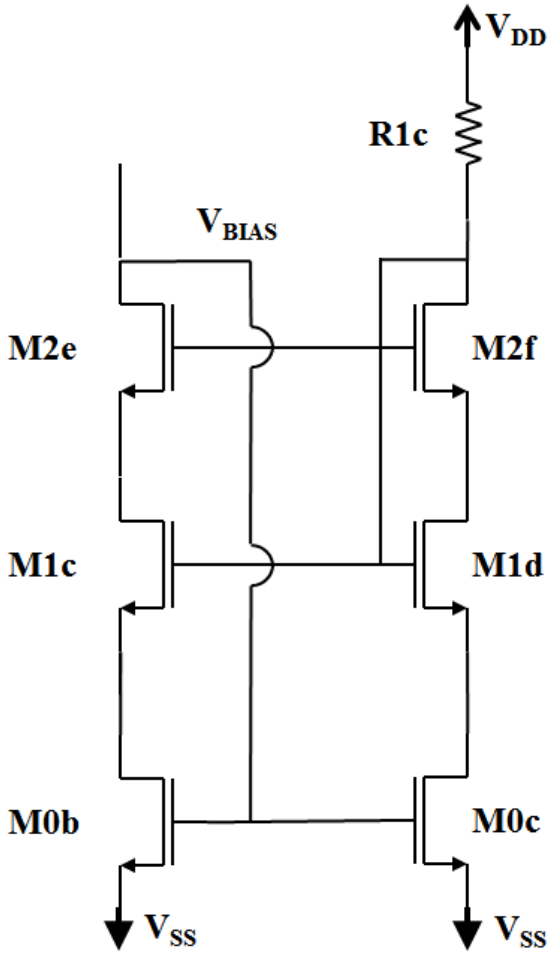


Figure 4.17: Schematic of the Replica Bias Circuit for the Differential Latch

4.4 Complete Test Circuit

The basic schematic and operation of the test circuit was shown in Figure 3.8; however a complete schematic of the test chip with the important pin names, is shown in Figure 4.18.

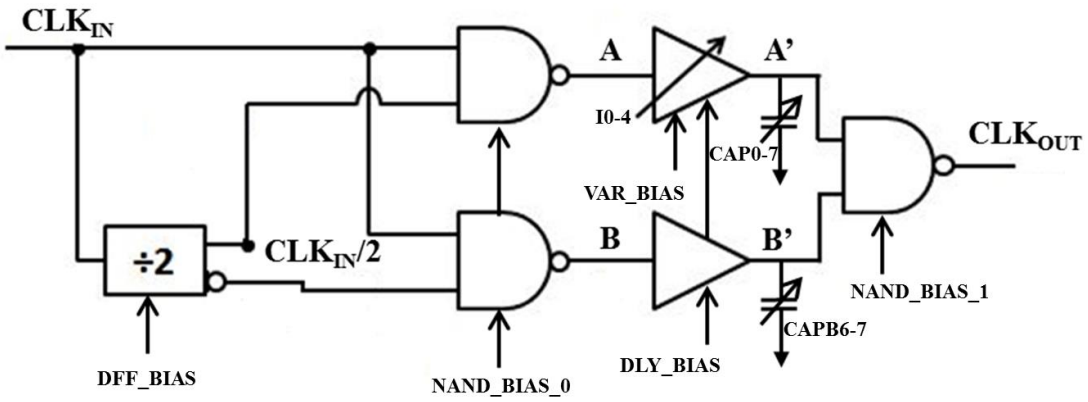
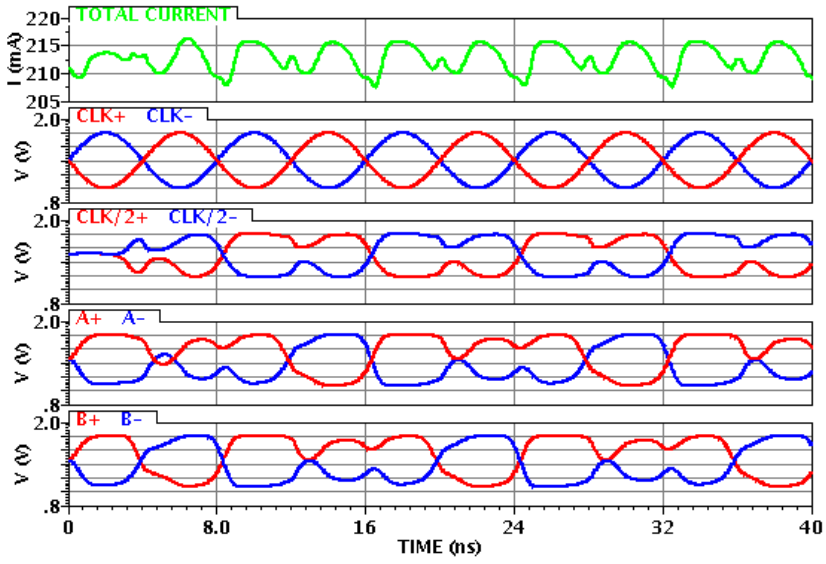


Figure 4.18: Schematic of the Complete Test Circuit

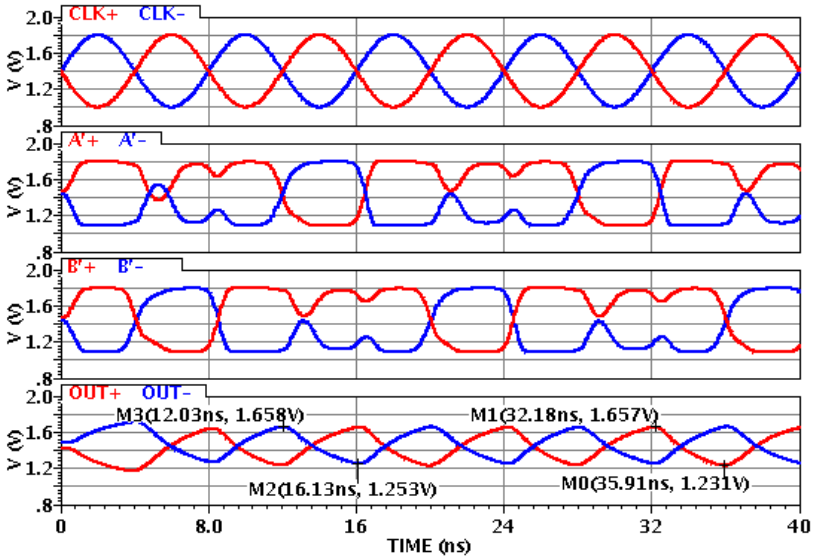
First, in order to allow the circuit to compensate for process variations and potential design errors, each of the major blocks (DFF's, path gating NAND's, buffers… etc.) contained within the test chip had their biases generated off chip. In combination with this a duplicate of the unit resistor common to all the major circuit's is included in order to tune, in combination with the bias currents, the common-modes of each of the circuit blocks. Next, the controls for the variable capacitor bank and the variable current source are brought directly out of the chip. Although this requires a large number of I/O pins, it minimizes the risks of designing additional circuitry to control them internally via an external serial communication bus. Finally, the variable delay buffer of path *A* is set as the variable path, whereas the variable delay buffer in path *B* is configured with only its two most significant bits of its delay control (i.e. the binary weighted banks of 64 and 128 capacitors) switchable and its variable current source

disabled. This is done for three reasons; first to allow any positive or negative timing skew introduced between the two paths by process variation or layout non-idealities to be correctable for different delay regions, in case due to some defect a certain delay region proves unreachable/correctable. Second it allows the inherent timing skew introduced for the above reasons between paths A and B to be explicitly shown when they are both set at the same delay point while thirdly showing that timing skews depend only on the relative timing difference and not the absolute.

The complete test circuit is simulated under the same 60 degree Celsius operating temperature and at the process corners to ensure functionality. The nominal DC current for the test chip is 252 mA $(32\ mA \times 7 + 4\ mA \times 7)$. Figure 4.19 shows the post-layout transient simulation for the complete test circuit with a 100 pF capacitive load placed on the NAND output driver.



a) Transient Response of DFF and Path Gating NANDs



b) Transient Response of the Delay Buffers and Output Driver NAND

Figure 4.19: Simulated Transient Response of the Complete Test Circuit

From the transient simulation, glitches are observed in the $CLK_{IN}/2$ signals that the DFF's generate, resulting in further glitches in the subsequent gates. In simulations, these glitches did not affect the performance of the test circuit and due to the impending tape out deadline they were left in the design. A discussion about this issue and its effects on the measured test chip is left to Chapter 5. Further simulations dealing with the timing skew precision and jitter proved extremely difficult to perform due to the large circuit, limited computing resources, and limited knowledge of the author in large-scale simulations. For example, the jitter simulations which are perform using Cadence Spectre simulation tool by performing a periodic-steady-state (PSS) noise simulation would not converge before the computer would run out of memory. Additionally, the timing skew precision simulations proved to be too large and long as well for the desired accuracy settings of the simulator. The post-layout simulated timing skew range for the test chip is determined to be approximately 143 ps. In order to get a rough estimate of the total output jitter of the test chip the simulated output jitter for path gating NAND, variable delay buffer and output driver NAND can be root-sum-squared (RSS) together as illustrated in (4.17) and (4.18).

$$\Delta T_{JITTER} = \sqrt{\Delta T_{JITTER(100pF)}{}^2 + \Delta T_{JITTER(DLY)}{}^2 + \Delta T_{JITTER(5\,pF)}{}^2} \qquad (4.17)$$

$$\Delta T_{JITTER} = \sqrt{105.39^2 + 24.36^2 + 16^2} = 109.34\,fs \qquad (4.18)$$

This results in a rough estimate for the final test chip's rms output jitter of approximately 110 fs.

4.4.1 Layout and Fabrication

As mentioned earlier in this thesis, the design, layout and fabrication of the test chip is done in TSMC's 0.18µm CMOS process with MIM capacitors option. A die size of $3\ mm^2 = (2\ mm^2 \times 1.5\ mm^2)$ is selected and approved by Canadian Microelectronics Corporation (CMC) for fabrication on March 19, 2012 with a chip designation of ICFWTAB1. The test chip is packaged in a 80-pin CQFP lead frame to ensure a sufficient number of I/O and supply pins.

In order to ensure the best chance of the taped out test chip operating correctly and as predicted by simulations, several recommended and essential layout guidelines are followed. First, ESD bond pads and protective circuits are implemented and latch-up prevention measures (maximize substrate contacts) are followed to protect the test chip from both types of failure events. Second, due to the high current requirements of the circuitry, current densities are considered for relevant areas (routing for clocks, routing for device outputs, routing for supply and ground lines, transistors, resistors and capacitors) and the poly resistors are sized in order to minimize the odds of overheating due to their high power dissipation. Third, extensive efforts are taken to ensure equal path lengths and capacitive loading for all critical signals, since matched timing is at the heart of designing a TI-ADC and any mismatches will show the insufficiency of best layout practices and the need to be able to correct timing skews. Additionally, dummy transistors, resistors, and capacitors are placed around their respective devices that are desirable to match, again to minimize timing and performance differences. The test load resistor to tune the bias currents on the test chip is placed and centered around the majority of the load resistors used in the chip to ensure better thermal and device matching. On chip decoupling capacitors are placed where possible to minimize transient switching effects and the noise in the test chip. Finally, all switches include pull-ups/pull-downs to ensure their nodes are defined and the switches are not partially on/off.

The final layout of the test chip and bonding diagram are shown in Figure 4.20 and Figure 4.21 respectively. Furthermore, the pin out and pin description for the test chip is include in Table A.1 in Appendix A. A die photograph of the fabricated test chip is shown in Figure 4.22.

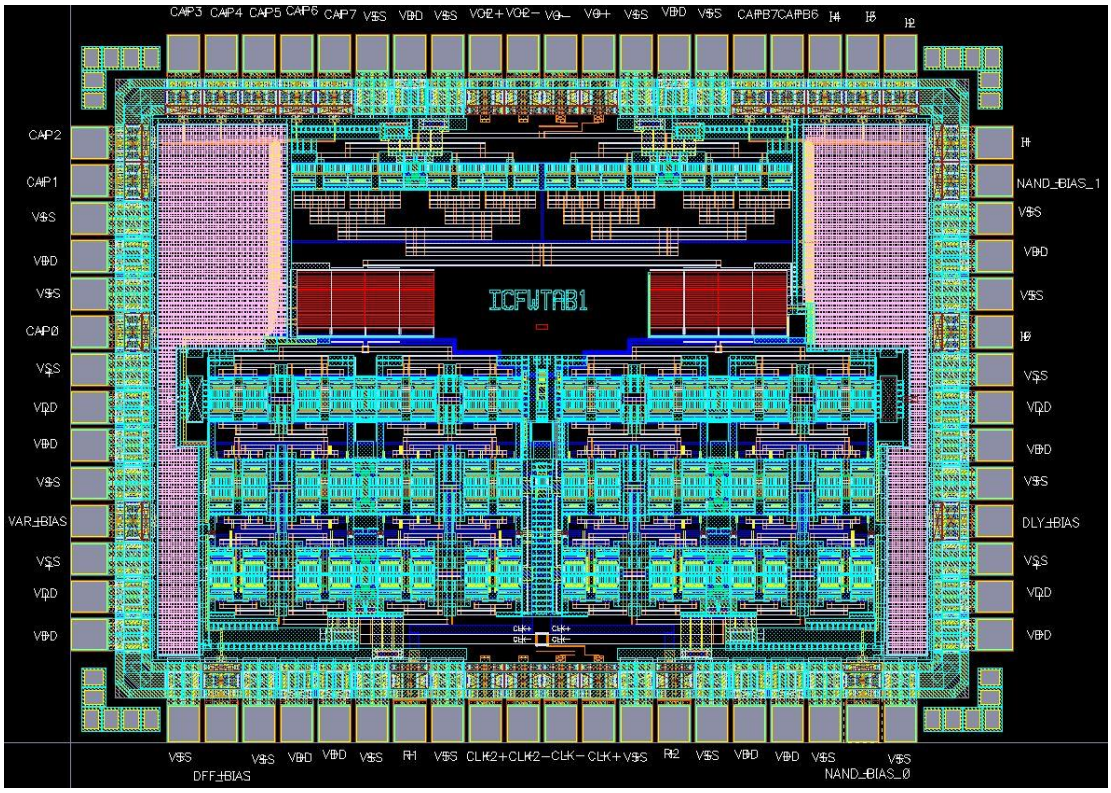


Figure 4.20: Final Layout of the Test Chip

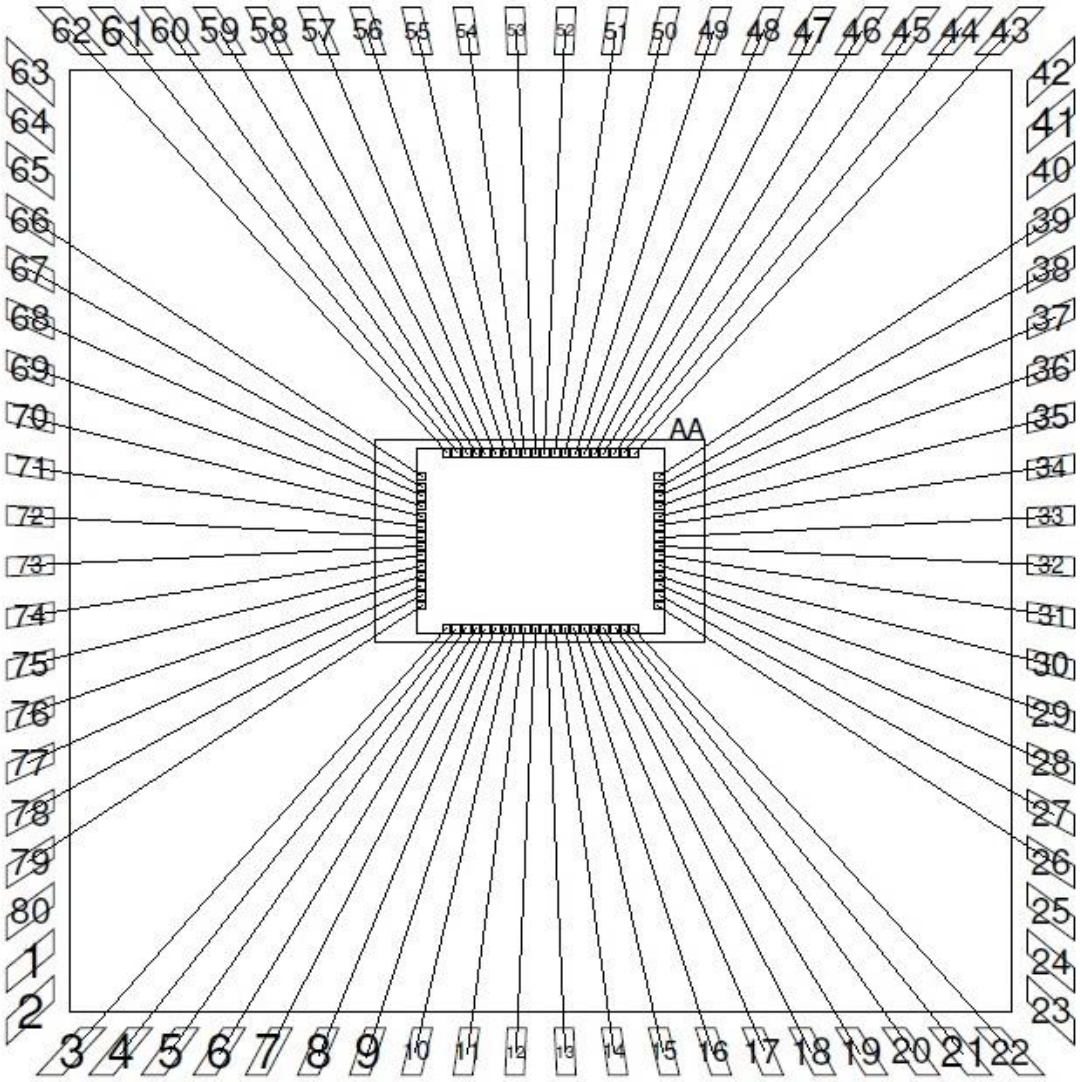


Figure 4.21: ICFWTAB1 Test Chip Bonding Diagram

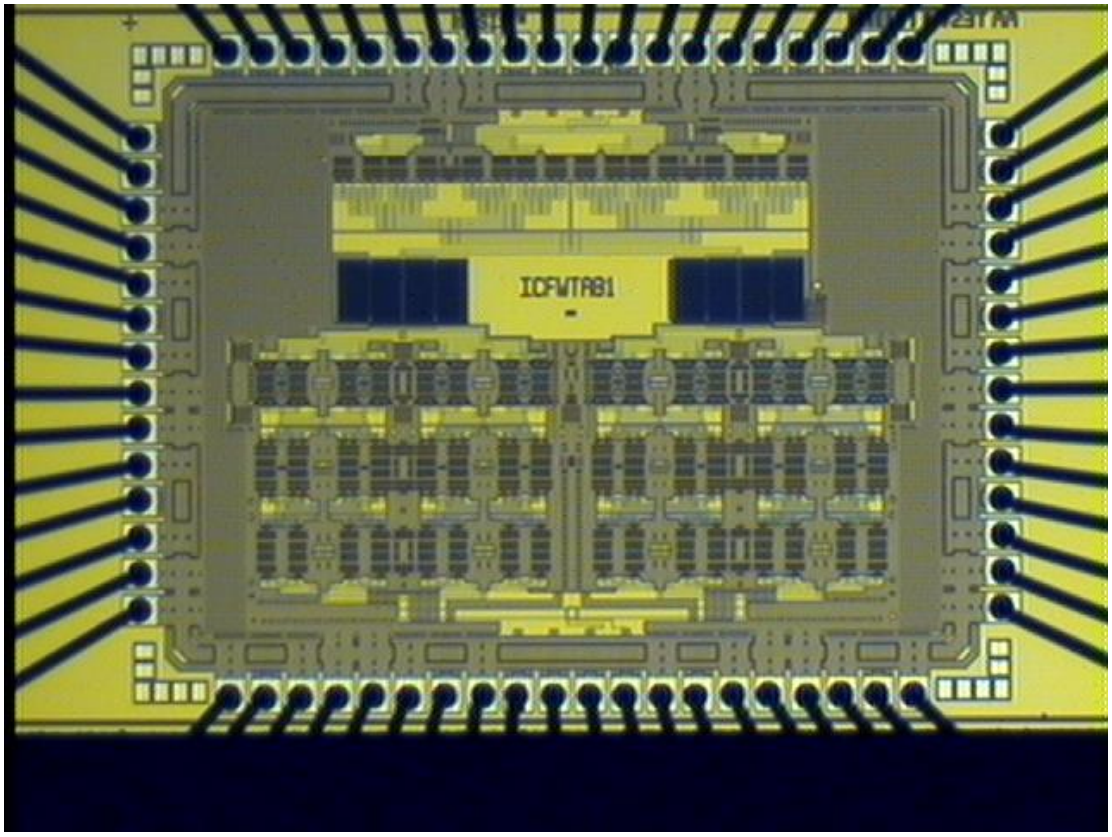


Figure 4.22: ICFWTAB1 Test Chip Die Photograph

Chapter 5

Testing Details and Measurement Results

The testing details and measurement results of the fabricated test circuit designed in Chapter 4 are presented in this chapter. The design of the printed circuit board (PCB) used to interface with the fabricated chip is first discussed. Next, the details of the test setup are presented including all the equipment used. The test procedures for the DC, transient, timing skew's precision and range, as well as the jitter measurement are then shown. Finally, the measured results are presented, comparing them when possible to the simulated results shown in Chapter 4. Lastly, suggestions for improving the designed timing skew correction and test circuit are discussed and future things to explore are suggested.

5.1 Test Board Design

A custom PCB is designed to power and interface with the fabricated test chip in Chapter 4. The PCB uses a FR-4 substrate and contains 4 layers, of which the top and bottom are reserved for signal routing and the two middle layers consist of separate power and ground planes. Any leftover area on the top and bottom layers is filled with copper and connected to the ground plane. The schematics and layout of each layer of the PCB are included in Appendix B. As part of the layout, a means of decoupling of the chip from the surface mount components during assembly is included, such that the possibility of harming the fabricated chip with an electrostatic discharge (ESD) event is minimized. In addition, this decoupling allows any shorts between power and ground to be checked before power is applied to the chip. Furthermore, the decoupling provides a way to tune and verify the operation of the PCB's support circuitry before it is connected to the fabricated test chip. As a final note on the layout of the PCB, thermal relief vias are placed under the fabricated test chip in case thermal sinking of the package is needed due to the high current draw/power dissipation of the test chip.

Since the test chip is designed to minimize the amount of output noise and jitter, a low noise linear regulator is used to supply power to the test chip. The linear regulator's output is adjustable via R74, a 100 KΩ potentiometer. Resistors R82, R84, R85, R86, R90 and R91 are included to allow the linear regulator to be setup and tested before it is connected to the fabricated chip. In addition, placeholder resistors R79, R80, R81 and R89 are provided to allow the current being supplied to the PCB to measured. Two sets of two parallel 22 µF ceramic capacitors are used as input and output capacitors on the linear regulator to smooth out high transient currents. Additional, 1 uF decoupling capacitors are placed as close as possible to each VDD pin on the fabricated chip. Connectors CONN5 and CONN6 are used to supply power and ground from a bench top power supply to the PCB's linear regulator.

To allow the performance of the chip to be tuned and to compensate for process variations, tunable bias networks are provided. Potentiometers R64, R66, R68, R70 and R72 are used as variable resistors to tune the bias currents of each circuit's internal bias structure independently. As part of the tuning procedure resistors R65, R67, R69, R71 and R73 are used to measure the bias current for each circuit block, ensuring each block is biased with the correct current. Furthermore, test points TP13 and TP14 are included to measure the process variation of the calibration load resistors, such that the bias currents can be tuned to obtain a common-mode voltage of 1.4 V for all the circuits within the test chip. To protect from an ESD event while measuring the calibration resistor, either R1 or R2 is left connected to the ground plane. The noise generated by the internal bias networks and external tuning networks are filtered using 10 μF capacitors placed on each circuit's bias network. Finally, note that the fabricated chip can be completely shut down by shorting the bias tuning networks to the ground plane while disconnecting them from the power plane. This allows the background current draw of the chips support circuitry to be measured.

The test chip requires differential inputs; however the signal generator used to provide the sampling clock is single-ended, requiring a single-ended to differential conversion. An RF transformer with good amplitude and phase balance, T1, is included to convert the signal generator's output to a differential one. The RF transformer has a center tap on the differential side, to provide a means to set and adjust the input common mode via R59, a 500 Ω potentiometer. As part of the input path, placeholders for 50 Ω termination resistors are included if needed to allow for good matching of the input signal. The PCB traces for the input and output clock paths are sized to have approximately 50 Ω characteristic impedances. The output differential pair also includes a set of resistors R62 and R63 which can be replaced by capacitors to AC couple the output, allowing any DC paths on the output such as 50 Ω terminations to not change the output NAND's bias point. Lastly, a set of clamping diodes, D1, is used to allow a large amplitude sine wave to be applied to the input and subsequently clipped to present a square wave like edge to the test chip

without over driving the input of the test chip. The steeply sloped, high slew rate edges reduce the jitter on the sampling clock.

Several switch banks, SW1 to SW4, are included to control the 10-bit lines for the variable capacitor banks and to control the 5-bit lines for the variable current sources. On each lines, 1 KΩ pull up and pull down resistors are used to further ensure that the internal MOSFET switches are not left floating. In addition, 100 nF capacitors are placed on each line to dampen the transient current when the switches are toggled.

5.2 Test Bench Setup and Procedures

The complete test bench setup for evaluating the fabricated test chip is shown in Figure 5.1. The test setup consists of two Rhode & Schwarz SMA100A signal generator, one provides the analog input signal to the test ADC and the other provides the sampling clock to either the fabricated test chip or the test ADC. The analog input signal is filtered using one of two band pass filters from TTE, depending on the input frequency used. The first filter, used for low frequency testing, is an 8-pole elliptical band pass, with a center frequency of 10 MHz and a bandwidth of 50% designed for ADC testing. The second filter, used for high frequency testing, is a 9-pole Chebyshev band pass, with a center frequency of 110 MHz and a bandwidth of 5% designed again for ADC testing. The filters are high order to ensure any noise or harmonic content from the signal generator(s) is minimized such that it does not interfere with the FFT based testing. In addition, the filter frequencies were selected such that any aliasing of the fundamental or harmonics would not interfere with the spurious tone generated due to the introduced timing skew and so they fall in a bin within the FFT to ensure coherent sampling.

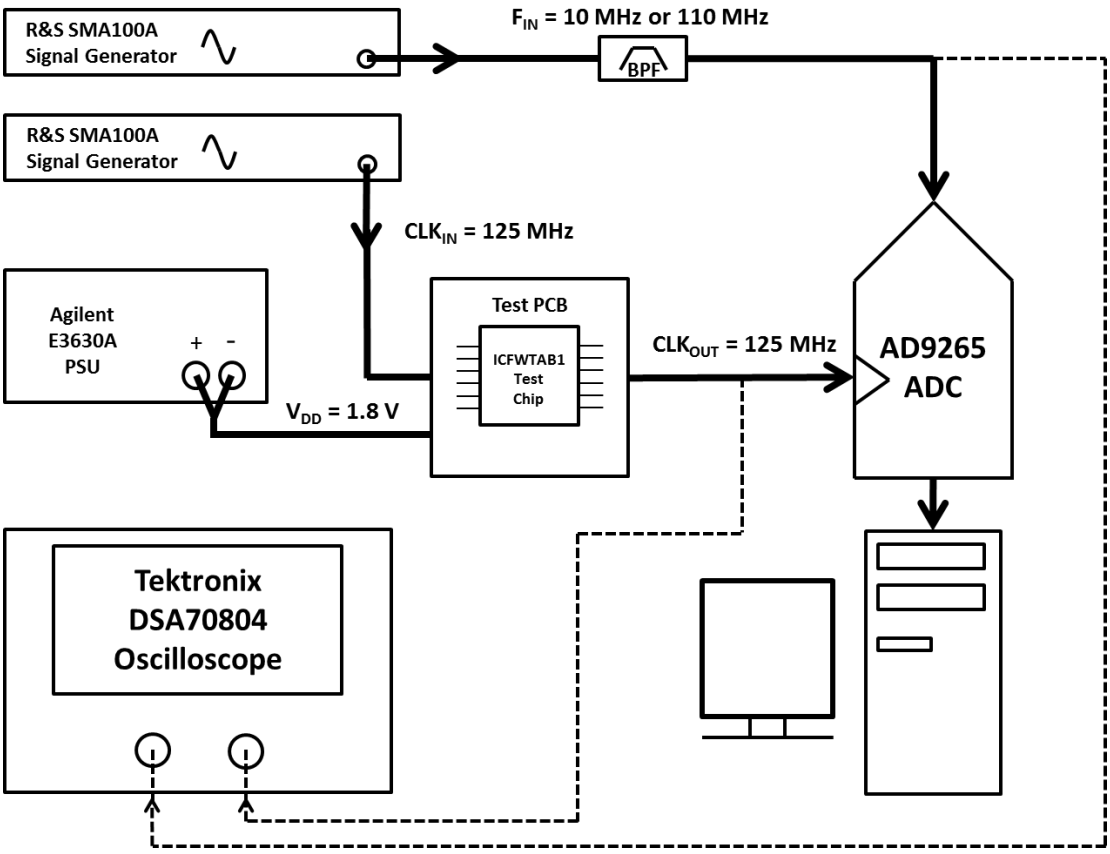


Figure 5.1: Test Bench Setup

An Analog Devices AD9265 16-bit 125 MSPS ADC evaluation board is used as the test ADC. The evaluation board outputs its digital data to a high speed FPGA based FIFO buffer capture board, which then sends the data to a desktop computer. The desktop computer has running on it Analog Devices Visual Analog software, which allows the output data to be viewed using a FFT plot. To ensure the test chip does not damage the ADC, the differential output of the chip is AC coupled into the AD9265 evaluation board. It is important to note that the AD9265 has a built in duty cycle stabilizing (DCS) circuit, which could interfere with the clock signal produced by the test chip [18]. For the testing conducted in this thesis, the DCS circuit is disabled to make sure it cannot interfere.

An Agilent E3630A bench top power supply is used to power the test chip through the linear regulator on the test PCB. Note that under certain test scenarios, the linear regulator is bypassed and the test chip is supplied directly from the bench top power supply. In addition, a Tektronix DMM4020 digital bench top multimeter (DMM) and Tektronix DSA70804 oscilloscope are only utilized for specific test scenarios as well.

5.2.1 Chip Staging and DC Measurement Details

To ensure that each circuit block within the test chip can be DC biased correctly, each is powered up independently. First, the background current draw of the test chip is measured, with the test chip shut down as described in Section 5.1 and the input common-mode voltage set to 0 V. Next, the bias network potentiometer for the first circuit, the differential D-Flip Flops, is tuned using the DMM to the nominal resistance value calculated to provide the proper bias current when the supply voltage is set at 1.8 V. Note no power has been applied yet. After this, power is applied to the test board using the bench top power supply, sweeping the supply voltage from 0 V to 1.8 V in 0.1 V increments to ensure predictable behavior is observed. Note that the linear regulator is bypassed and disconnected from the power plane since it cannot provide voltages in between 0 V and 1.0 V. The input common-mode voltage is then swept from 0 V to 1.8 V in 0.1 V increments, allowing the D-Flip Flops to draw current. The current draw is measured, with the supply at 1.8 V and input common-mode at 1.4 V, using the DMM to determine the voltage drop across a 10 Ω resistor. The current measured is compared to the nominal simulated DC current draw to verify the two are close. The power supply is then cycle three times by disconnecting and reconnecting the power cable to ensure the D-Flip Flops start up predictably and draw the same DC current as the first measurement. After this, when the board is powered down, the bias network for the D-Flip Flops is disconnected from the power

plane and shorted to ground to ensure the it remains off while the other circuits are staged. The above procedure is then repeated, with the exception of the background current draw and the changing of the common-mode voltage, which is left at 1.4 V, for every other circuit block (input NANDs, variable delay buffer and output NANDs). Note that only one circuit block is powered up at a time, with the others being disconnected and shorted to ground via their bias network. This concludes the first part of the chip staging.

The second part of the chip staging involves powering up all the circuit blocks sequentially, to ensure the chip does not behave adversely as more blocks are active at a time. Note that in this case, the bias networks are left connected to the power plane but the pins on the chip (DFF_B, NAND_B0, NAND_B1, DLY_B and VAR_B) are shorted to ground for any not currently powered up. This requires the background current to be measured as each circuit block is powered. After each additional circuit block is added, the current is measured, only this time due to the higher current draw, a 1 Ω resistor is used to determine the voltage drop and corresponding supply current. Once again, the power is cycled to verify that the circuit starts up as expected and that no latch-up events occur. The next step is to measure the calibration load resistor, after the chip has been powered up for a while to stabilize the resistor's temperature. Using the measured value, the bias networks are adjusted such that the input/output common-mode level is set to approximately 1.4 V for each circuit block. After this, the linear regulator bypass is removed to allow it to regulate the power supply's voltage. Note that the correct operation and output voltage (1.8 V) is verified before connecting the linear regulators output to the power plane. With this, the DC measurements can take place.

Characterizing the DC performance of the test chip involves four measurements. The first is to measure and record the voltage on the output of the linear regulator. The second measurement is to record the voltage on each of the bias networks test points, TP1 to TP5, allowing the bias current for each circuit block to

be calculated. The third measurement records the total current being supplied to the test chip via the 1 Ω resistor placed between the power supply and the input to the linear regulator. It is important to note that the background current draw of the linear regulator and other ancillary circuitry that is not included on the fabricated chip needs to be subtracted off this measurement. The final fourth DC measurement is to record the common-mode output voltage on VO+ and VO-. One final note is that, no other equipment is used in the chip staging or measurements other than the bench top power supply and the DMM.

5.2.2 Transient Measurement Details

The transient measurement is done to verify that the output of the test chip resembles the post-layout simulated output. The output of the test board is connected to channel 1 and channel 2 of the oscilloscope and AC coupled by replacing resistors R62 and R63 with 100 nF capacitors. This is done to prevent the oscilloscope, which has a 50 Ω input impedance, from shifting the bias point of the output NANDs. One of the Rhode & Schwarz signal generators is set to output a sine wave at 125 MHz with a peak-to-peak amplitude of 0.8 V, corresponding to an output power of approximately 2.5 dBm. The output of the signal generator is verified using the oscilloscope. The output of the signal generator is then disabled and connected to the input of the test board. The signal generator is then enabled and measurements detailing the peak-to-peak amplitude, frequency and rising and falling slew rates are setup. A screen capture of VO+ and VO- is recorded with the measurements displayed.

Note that it is important to measure the output transient behavior using the same cables as those that take the timing skew and additive jitter measurements, to ensure the same capacitive loading. In saying this, the SMA cables used to connect the output of the test board to the oscilloscope are approximately 3’ long and have a capacitive load of approximately 90 pF [20].

5.2.3 Timing Skew Precision and Range Measurements

As was mentioned in Chapter 2, the best way to measure and characterize timing skews is to use a FFT plot and monitor the SFDR with respect to the spurious tones due to the timing skews. Visual Analog by Analog Devices is used to capture and display the FFT of the AD9265's output in order to measure the SFDR and characterize test circuit's timing skew behavior. For all timing skew characterization measurements, ten 32,768-point FFT plots are captured with a running average of the measurements being generated over time to ensure the measurements are accurate and repeatable. The details of the signals used for the timing skew measurements are shown in Table 5.1.

Table 5.1: Test Signals Used for Timing Skew Measurements

Purpose	**Frequency [Aliased] (MHz)**	**Signal Generator Amplitude (dBm)**	**Filtered**	**Aliased Timing Skew Spurious Tone Frequency (MHz)**
Analog Input	9.99832153	3.15	Yes	52.502
Analog Input	110.004425 [14.996]	17.33	Yes	47.504
Clock Input	125	2.5	No	N/A

The filters used for the analog input signals are the ones described in Section 5.2. An important thing to note is the amplitude of each input signal is set such that the measured fundamental (signal) power in the captured FFT is -9 dBFS. Normally the fundamental's power would be set to -1 dBFS, however due to the high insertion loss of the 110 MHz filter (approximately 11 dB) the required output power from the signal generator is too high to maintain the desired noise performance. Given this, the -9 dBFS level is selected as the reference level for both analog input signals for all the

timing skew and jitter measurements. The frequencies for the timing skew tones that are controlled and corrected by the test chip are calculated from (2.35).

Several measurements are required to characterize the test chip's precision level in correcting timing skews and the total range over which the timing skews can be corrected. Table 5.2 lists the various measurements that are taken to characterize the timing skew correction circuit. Note that measurements 1 to 10 are all taken with the 110 MHz input signal, while measurements 11 to 13 are taken with the 10 MHz input signal. For the measurements listed in Table 5.2, the path B capacitor bank is set to the middle of the range (i.e. code 127). The path A variable capacitor bank is varied according to measurements 1 to 6 in Table 5.2 such that all the major code transitions (i.e. 00111111 to 01000000) are covered, the range of correction is covered and a reasonable number of steps (approximately 100) are covered to characterize the precision of the steps. Measurement 4 is comprised of three code sweeps of the variable capacitor bank around the middle of the correction range, each taken on a different day after the test chip has been powered off for some time to characterize the repeatability and consistency of the timings steps and of the mismatch between the two paths. The decimal values for the code ranges in measurement 4 and measurement 8 correspond to the three measurement time points, where matching decimal numbers indicate the same testing time at which the measurements are taken. It is important to note that when path A is set to code 127, which matches path B, the timing skew measured from the FFT represents the inherent path mismatch due to process and manufacturing variations. It is also important to note that for measurement 4, the variable capacitor code that minimizes the timing skew (i.e. provides the best possible timing skew correction with just the variable capacitor bank) is then used as the starting point for measurement 8.

Table 5.2: Measurements for Characterizing the Timing Skew Correction Ability

Measurement Purpose	Measurement Number	Path A Variable Capacitor Code(s)	Variable Current Source Code(s)
Variable Capacitor Timing Skew Correction Precision and Range	1	0 – 20	0
	2	30 – 33	
	3	54 – 74	
	4.1	116 – 137	
	4.2	115 – 137	
	4.3	108 – 130	
	5	182 – 202	
	6	235 – 255	
Variable Current Source Timing Skew Correction Precision and Range	7	0	0 – 31
	8.1	118	0 – 8
	8.2	118	0 – 23
	8.3	119	0 – 31
	9	127	0 – 31
	10	255	0 – 31
Timing Skew Correction Holds Over Input Frequency	11	127	0
	12	118	0
	13	118	4

Similar to measurements 1 to 6 for the variable capacitor bank, measurements 7 to 10 are used to characterize the range of correction and precision of the steps for the variable current source. Measurement 8 sweeps the variable current source around the variable capacitor code that minimized the timing skew tone, to show the best timing skew correction the chip can achieve for the nominal variable bias current setting. The final measurements, 11 to 13, are FFT plots used to show that the timing skew correction settings hold for a different input frequency.

5.2.4 Additive Jitter Measurement Details

The procedure for measuring the additive jitter of the test chip is taken from Analog Devices AN-501 application note [21]. Based on the application note, four measurements are required to characterize the additive jitter performance of the fabricated test chip. Two low frequency SNR measurements are taken, one without the test chip in the sampling clock path (measurement 'A') and one with the test chip present (measurement 'B'). Note that the test without the test chip is done with a duplicate test PCB that does not have the test chip attached, instead the differential input traces are connected directly to the output traces. The other two measurements are high frequency SNR measurements, one without the test chip (measurement 'A'), and one with the test chip in the sampling clock path (measurement 'B').

The first two low frequency SNR measurements, SNR_{LFA} and SNR_{LFB} are taken at approximately 10 MHz in order to determine noise level of the AD9265 when no jitter effects are present. Figure 5.2 shows that for the AD9265 with an input frequency of 10 MHz that the SNR is indeed not limited by the jitter.

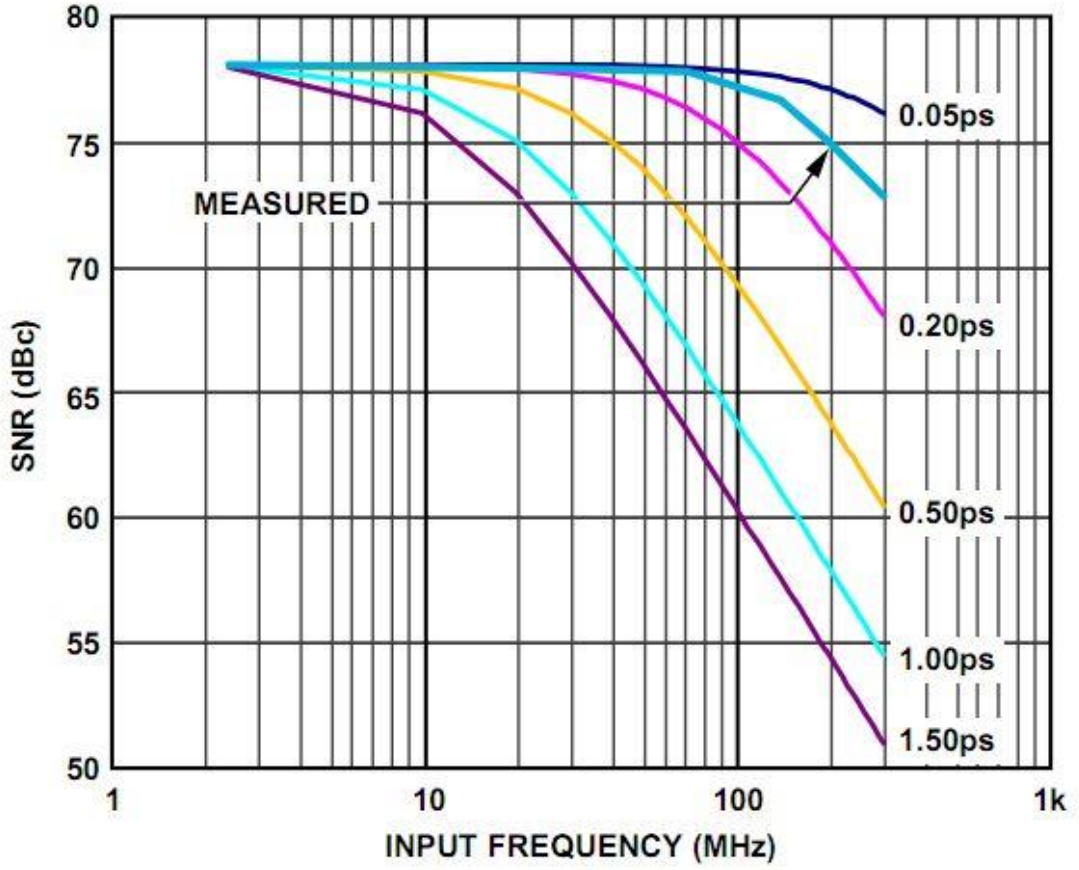


Figure 5.2: AD 9265 SNR vs. Input Frequency for Various Amounts of Jitter [18]

With this, the following equation is used to calculate the composite rms DNL ε for both measurements, A and B, which captures the noise contributions of all sources other than jitter using the low frequency measured SNR's [21]:

$$\varepsilon_{A/B} = 2^N \times 10^{\frac{-SNR_{LFA/LFB}}{20}} - 1 \tag{5.1}$$

The high frequency SNR measurements, SNR_{HFA} and SNR_{HFB} are taken at an input frequency of approximately 110 MHz, which according to Figure 5.2 results in an SNR that is jitter dependant. The SNR_{HFA} measurement, which is without the test

chip, captures the jitter induced noise of all components other than the test chip, whereas the SNR_{HFB} measurement captures all the noise from all jitter contributing sources in the sampling clock path, test chip included. The total rms jitter without the test chips contribution, $\Delta T_{JITTERA}$, and with its contribution, $\Delta T_{JITTERB}$, is calculated from the two SNR_{HF} measurements and two calculated ε values from (5.1) using the following equation [21]:

$$\Delta T_{JITTERA/JITTERB} = \frac{\sqrt{\left(10^{\frac{-SNR_{HFA/HFB}}{20}}\right)^2 - \left(\frac{1+\varepsilon_{A/B}}{2^N}\right)^2}}{2\pi F_{IN}} \tag{5.2}$$

Using the two total rms jitters calculated from (5.2), the rms additive jitter due to the test chip alone is calculated using the following:

$$\Delta T_{JITTER} = \sqrt{\Delta T_{JITTERB}{}^2 - \Delta T_{JITTERA}{}^2} \tag{5.3}$$

Just as in FFT measurements from the previous section, Analog Devices Visual Analog software is used to capture the FFT and the corresponding SNR measurements to characterize the additive jitter performance of the test chip. Similarly, ten 32,768-point FFT plots are captured with a running average of the measurements being generated over time to determine the SNR for each of the four measurements. Additionally the same signals and signal parameters that are listed in Table 5.1 are used for the four required SNR measurements.

5.3 Measured Results

The major results for each of the measurements detailed in the previous section are now presented.

5.3.1 Chip Staging and DC Measurements

The measured DC bias points from the test chip as each stage is powered up are shown in Table 5.3. The calibration load resistor used to set the bias points is measured to be approximately 463 Ω, which results in the desired bias of 1.715 mA/3.43 mA for each of the gates such that the 1.4 V common-mode voltage for all the gates is met.

Table 5.3: Initial Measured DC Bias Points of the Test Chip

Gate(s) Powered	**V_{TP}(Gate) (V)**	**I_{BIAS}(Gate) (mA)**	**$I_{MEASURE}$ (mA)**	**$I_{BACKGROUND}$ (mA)**	**I_{GATE} (mA)**
DFF (V_{CM} = 0)	1.457	3.43	27.74	20.91	0
DFF (V_{CM} = 1.4V)	1.457	3.43	83.41	20.91	55.7
DFF + NAND0	1.457	3.43	139.97	14.16	56.45
DFF + NAND0 + DLY	1.457	3.43	195.23	7.42	55.14
DFF + NAND0 + DLY + VAR	1.55	0.25	195.7	7.03	See Table 5.4
DFF + NAND0 + DLY + VAR + NAND1	1.628	1.715	223.14	3.66	27.74

V_{TP}(Gate) is the test point voltage used to calculate the bias current (I_{BIAS}(Gate)) for the most recent gate powered up. For example, in the case of DFF + NAND0, the gate of concern is NAND0 and all measurements titled with the word gate in it are for the NAND0 gate. Based on Table 5.3 the total chip current for the initial DC measurements is 219.48 mA (223.14-3.66) which compares well with the simulated post layout extracted current of 218.7 mA when the same gate bias currents are used. The common mode voltages for the outputs, VO+ and VO-, are measured to be 1.377 V and 1.422 V respectively. This compares to the simulated post-layout extracted common-mode voltages for the outputs of 1.444 V and 1.46 V for VO+ and VO- respectively. The difference between the two values is mainly due to the load resistors in simulation being the nominal approximate 400 Ω rather than the 463 Ω measured.

The measured currents I_{VCS} for each of the five taps in the variable current source are shown in Table 5.4. The corresponding simulated currents from Section 4.1.6 are also included in Table 5.4 for comparison purposes.

Table 5.4: Comparison of Simulated and Measured Variable Current Source Currents

Variable Current Source Code	**Nominal Simulated I_{VCS} (µA)**	**Measured I_{VCS} (µA)**
00001	15.8	17.X
00010	31.6	32.X
00100	63.16	69.X
01000	126.18	133.X
10000	251.8	270.X

Compared to the nominal simulated currents, the measured currents are slightly higher by up to approximately 10%, which is within the expected values for process variations.

During the measurement process for the test chip a non-ideal/unexpected behaviour was observed, which consisted of a raised and sporadic noise floor in the measured FFT. The non-ideal behaviour was found to be due to the D-Flip Flops not having enough gain to switch properly and generate the $CLK_{IN}/2$ signal, leaving both inputs of the clock gating NANDs on. The fix for this was to lower the bias current through the D-Flip Flops, which increases the gain of the transistors, allowing the D-Flip Flops to switch properly. The corrected DC bias point for the D-Flips Flops is shown in Table 5.5. V_{TP}(Gate) was measured from the test chip, however the I_{GATE} current report in Table 5.1 is not measured, it is calculated based off of the mirroring ratio of 16.23 times between I_{BIAS}(Gate) and I_{GATE} from the DFF measurement in Table 5.3 to give an idea as to the total bias current for the D-Flip Flops.

Table 5.5: Corrected DC Bias Point for the DFF

Gate Powered	**V_{TP}(Gate) (V)**	**I_{BIAS}(Gate) (mA)**	**$I_{MEASURE}$ (mA)**	**$I_{BACKGROUND}$ (mA)**	**I_{GATE} (mA)**
DFF	1.57	2.3	N/A	N/A	37.33

Due to limited time, the revised total test chip current could not be re-measured. However, based on the approximate change in the D-Flip Flops bias current the revised total test chip current would be 201.11 mA, which compares favorably to the 199.2 mA from simulations.

5.3.2 Transient Measurements

During the transient measurements, it was found that the clamping diodes on the PCB, D1, did not work as well as expected. The diodes appeared to have a large internal resistance and did not sink enough current fast enough to allow a large amplitude sine wave to be clamped and appear as a square wave with sharp rising and falling edges. Due to this, the input to the test chip CLK_{IN} was a sine wave as shown in Figure 5.3.

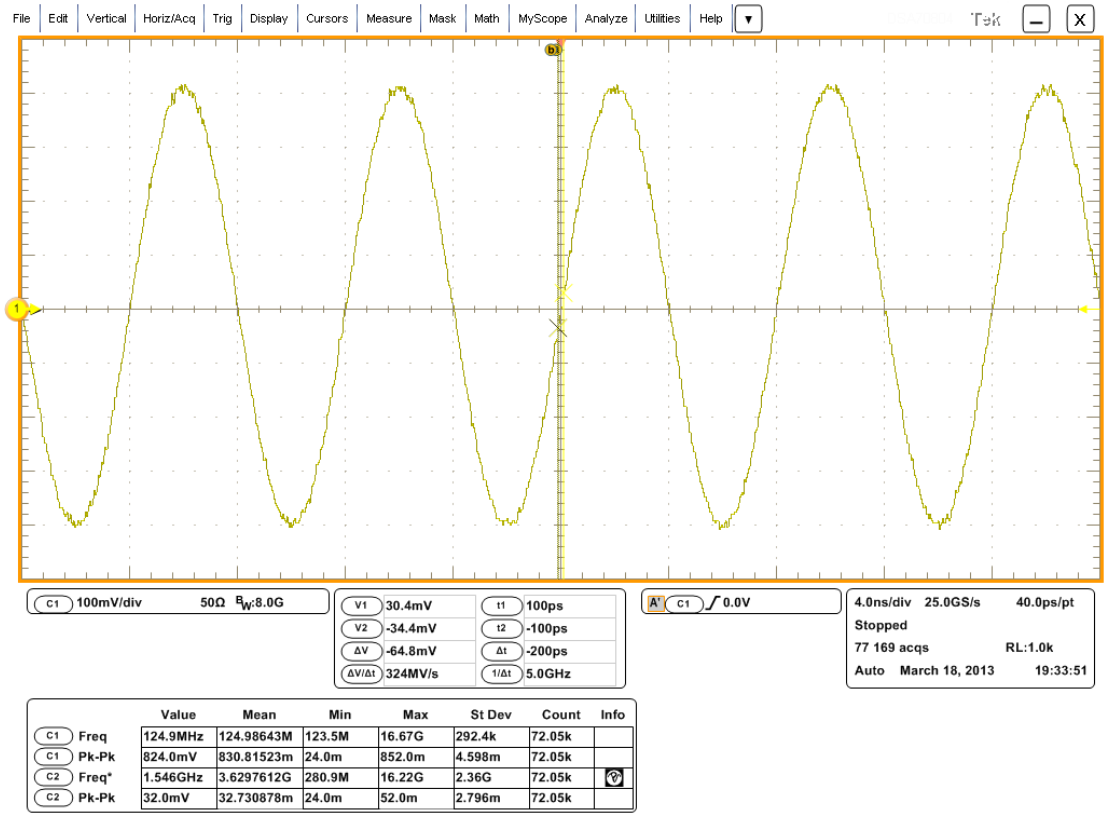


Figure 5.3: Oscilloscope Capture of the Input Signal CLK_{IN} to the Test Chip

Additionally, the use of a sine wave input pointed out a non-ideal behavior in the test chip as the chip was simulated using an input signal with faster edges then a sine wave. The non-ideal behaviour, which consisted of a raised and unstable FFT noise floor, was observed while taking the timing skew measurements however, it also appeared in the transient output as a random shift in the triggering point of the output.

The measured transient output for the corrected D-Flip Flops bias current of the test chip using the 90 pF SMA cables are shown in Figure 5.4. Channel 1 (Yellow) corresponds to VO+ and Channel 2 (Blue) corresponds to VO-.

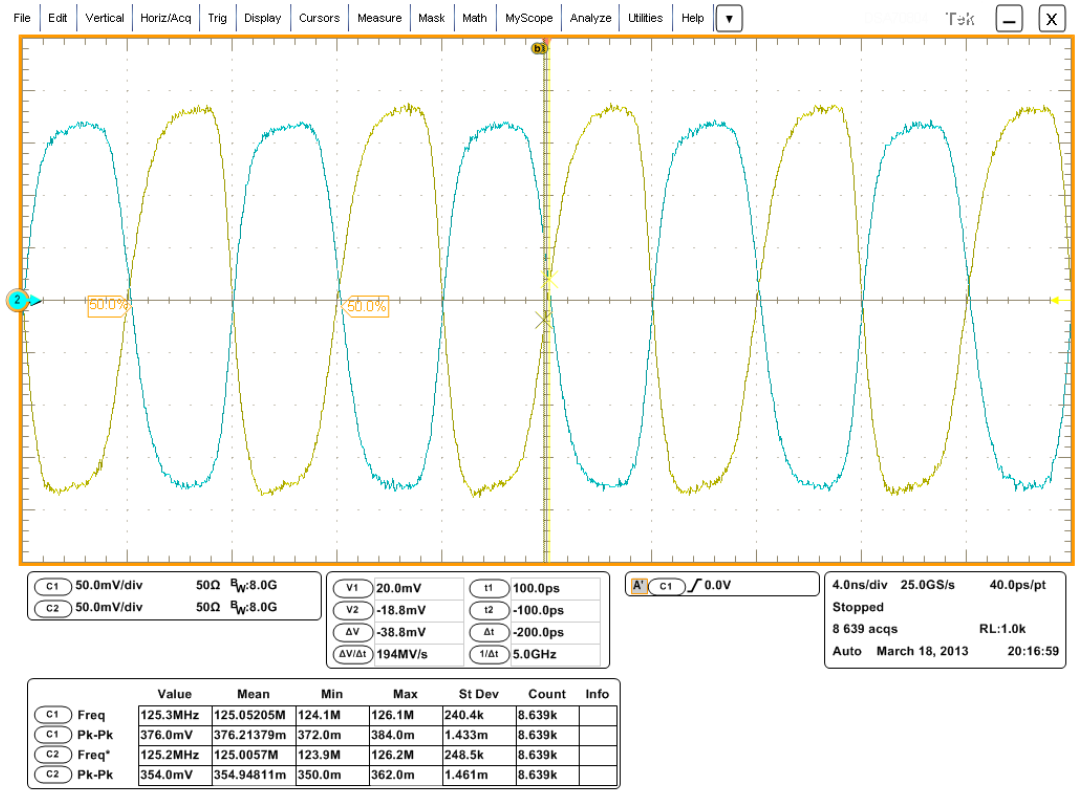


Figure 5.4: Measure VO+ and VO- Using the 90 pF SMA Cables

The measured VO+ and VO- peak-to-peak values of 376 mV and 354 mV respectively compare reasonably well with the simulated post-layout extracted values

of 426 mV and 405 mV taken from Figure 4.19 in Section 4.4. The difference could be attributed to the simulation not capturing the transmission line effects between the test chip and the ADC clock inputs or the clamping diodes that were left on the ADC evaluation board to protect the ADC's clock inputs from being over driven which could leak current and reduce the output swing.

5.3.3 Timing Skew Precision and Range Measurements

The results for measurements 1 to 6 detailed in Section 5.2.3 are shown in Figure 5.5 to Figure 5.8. First, Figure 5.5 shows the measured SFDR and corresponding timing skew magnitude for the variable capacitor code sweep ranges. Note that the SFDR presented in Figure 5.5 is relative to the input signal level since it is the ratio between the analog input level and the timing skew spur that is important. The timing skew magnitude on the right vertical axis is in a log scale and is calculated using (2.42).

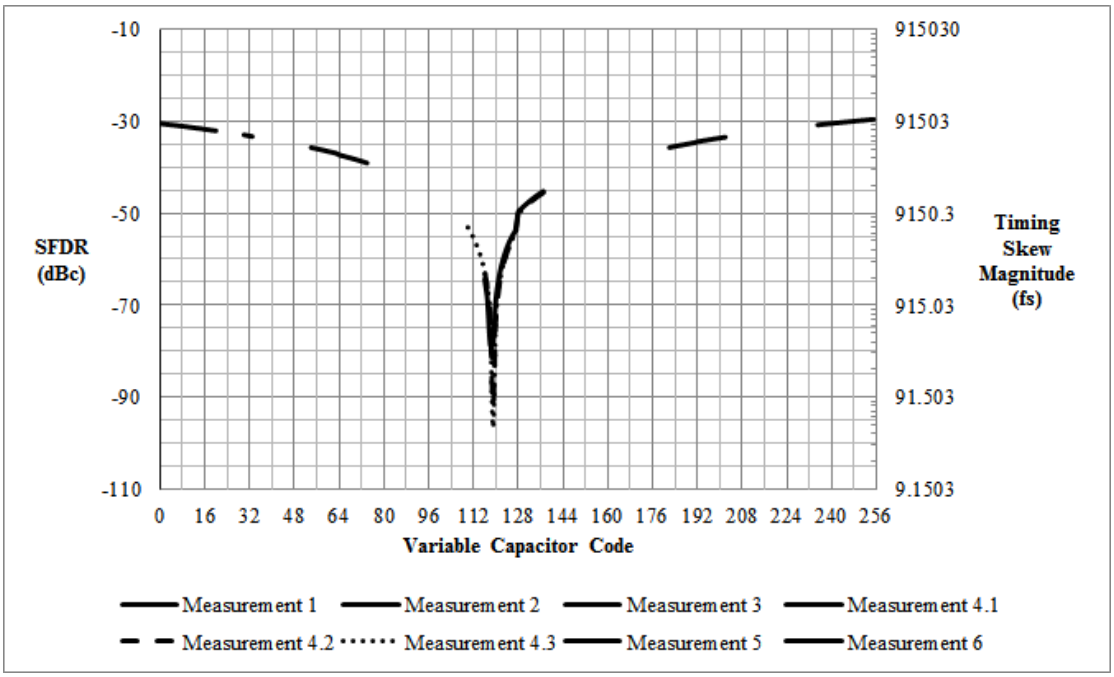


Figure 5.5: Variable Capacitor Timing Skew Performance Over Capacitor Codes

From Figure 5.5 the entire timing skew adjustment range is approximately 183 ps given by the code 0 to code 255 timing skew magnitude difference. This meets the original design goal range of 100 ps to 200 ps, successfully showing the test chip's timing skew range performance. Figure 5.6 shows a magnified view of the mid-range variable capacitor codes for the three different timing points measured. The results show that at different time points and with power cycles, the capacitor bank performance is quite consistent. Note that the SFDR/timing skew magnitude minimum between measurement 4.1 and measurements 4.2 and 4.3 corresponds to a timing skew magnitude difference of only approximately 300 fs, which could easily be compensated for using a background calibration routine.

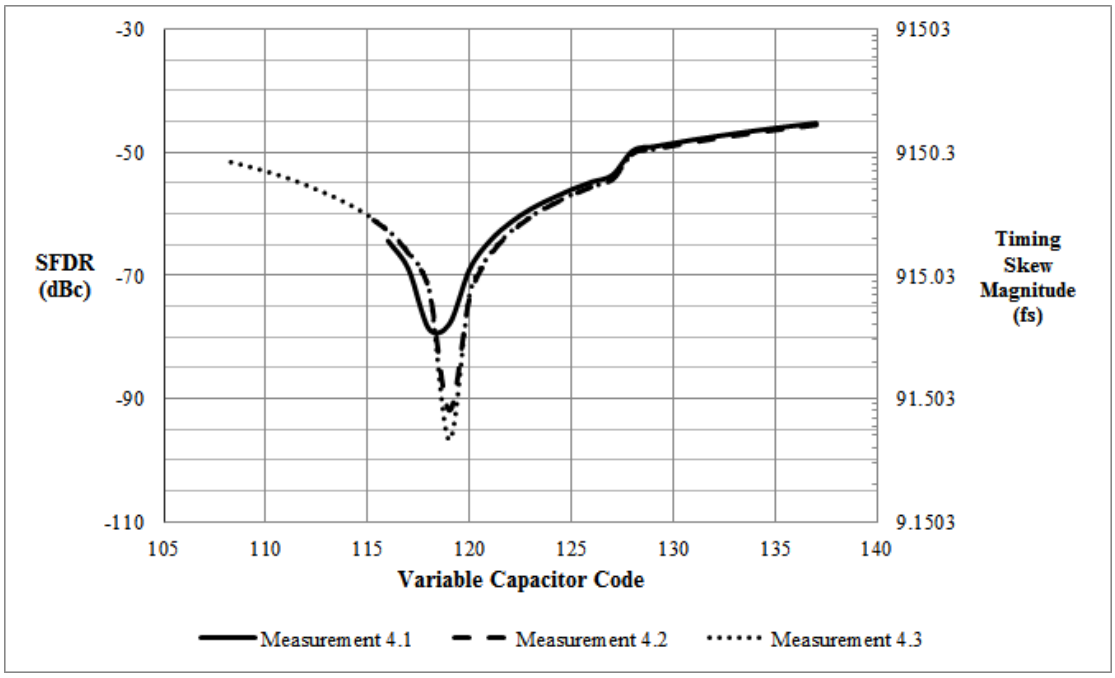


Figure 5.6: Variable Capacitor Timing Skew Minimization Performance

The precision of the timing skew correction using the variable capacitor bank is shown in Figure 5.7 and Figure 5.8. Figure 5.7 shows the magnitude of the timing skew steps between consecutive capacitor codes over the code ranges measured. The step sizes are relatively consistent over the entire capacitor code range, gradually reducing as the capacitive load on the differential buffer increases, which is expected. The spikes observed in the measurements, occur at the MSB change points (i.e. 00011111 to 00100000), and are a result of capacitor mismatch in the process and the binary switching scheme. To reduce these effects, unit switching for the capacitor bank should be used and further matching optimized layout of the capacitors should be observed. Figure 5.8 shows a histogram plot of the approximately 110-capacitor steps record for the first time point set of measurements. The histogram clearly shows that the average step size is approximately 700 fs and thus the precision to which the timing skew tone can be corrected is approximately 700 fs using only the variable

capacitor bank, which is within the expected +/- 20% of the 600 fs determined in simulation.

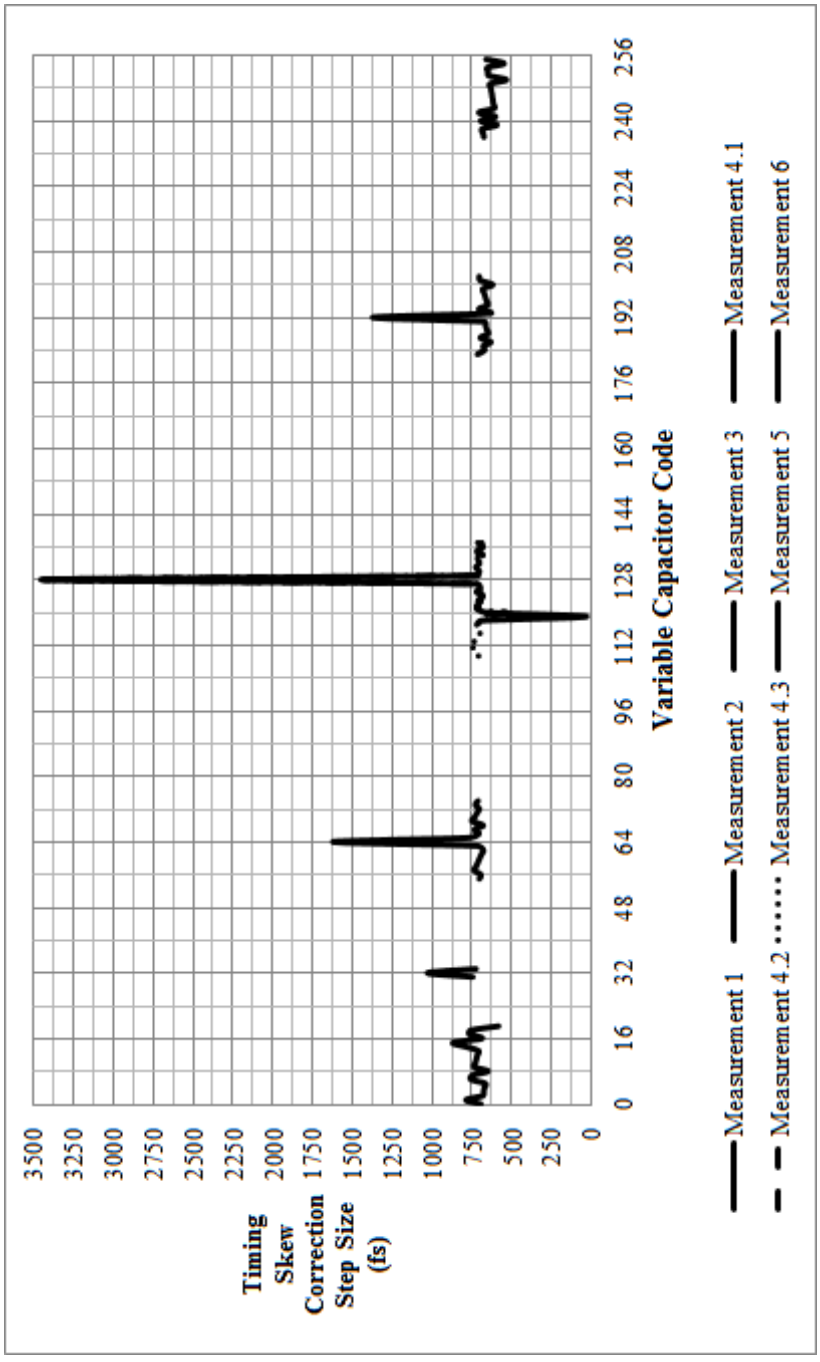


Figure 5.7: Variable Capacitor Timing Skew Precision Over Capacitor Codes

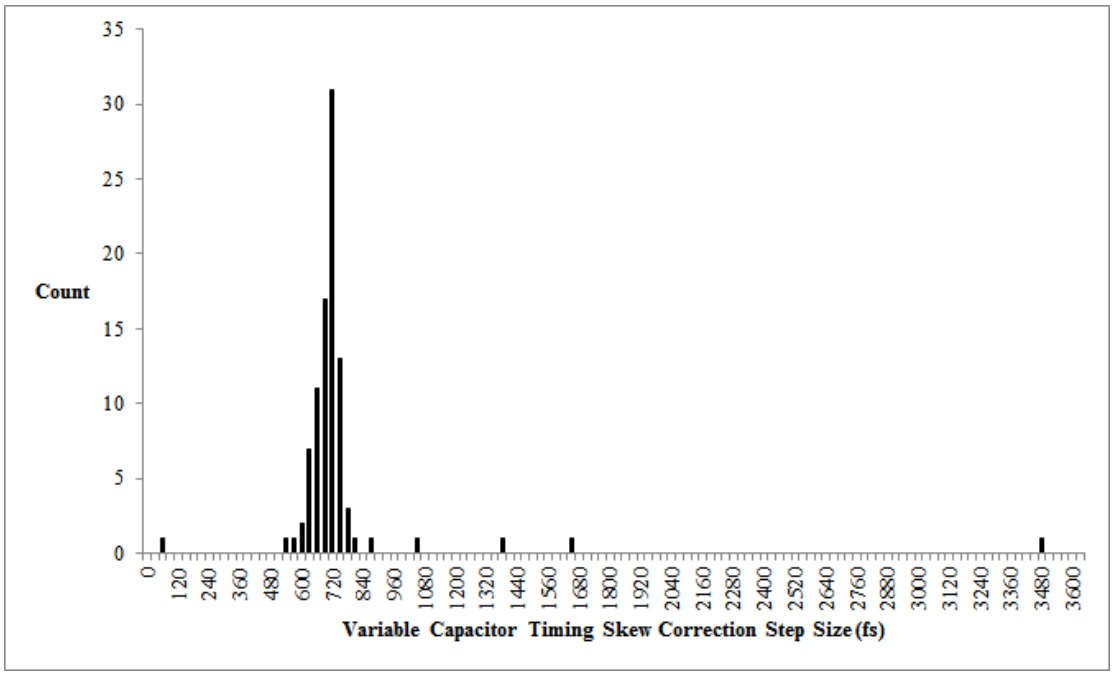


Figure 5.8: Distribution of the Variable Capacitor Timing Skew Correction Precision

The results from measurements 7 to 10 for the variable current source are captured in Figure 5.9 to Figure 5.11. Similar to the variable capacitor measurements, the first figure, Figure 5.9, shows the SFDR and resultant timing skew magnitude for the three time point measurements. The SFDR/timing skew tone minimum points occur at different code ranges over time, which is not unexpected since the sensitivity of the system to temperature and environment variation and even circuit burn-in is likely high at this precision level. Although the codes that minimize the timing skew spurious tone vary for the different time points, the ultimate minimum is very similar between each case proving the precision level and repeatability of the correction.

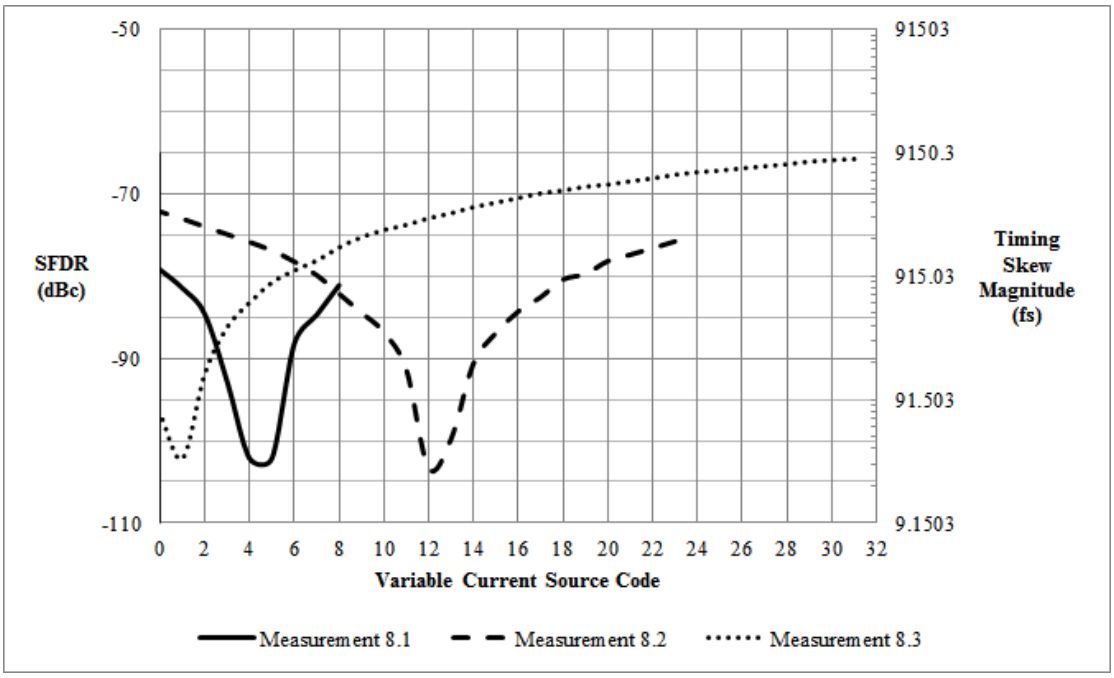


Figure 5.9: Variable Current Source Timing Skew Minimization Performance

Expanding on the timing skew correction precision achieved by the variable current source, Figure 5.10 and Figure 5.11 show the timing skew correction step size and the corresponding histogram of the 90 steps. The average measured step size is approximately 60 fs, which is reasonably close to the design goal of 25 fs. It is important to note that the precision level can improved as well by reducing the bias current of the variable current source; however due to time constraints only the nominal 250 μA bias point was measured.

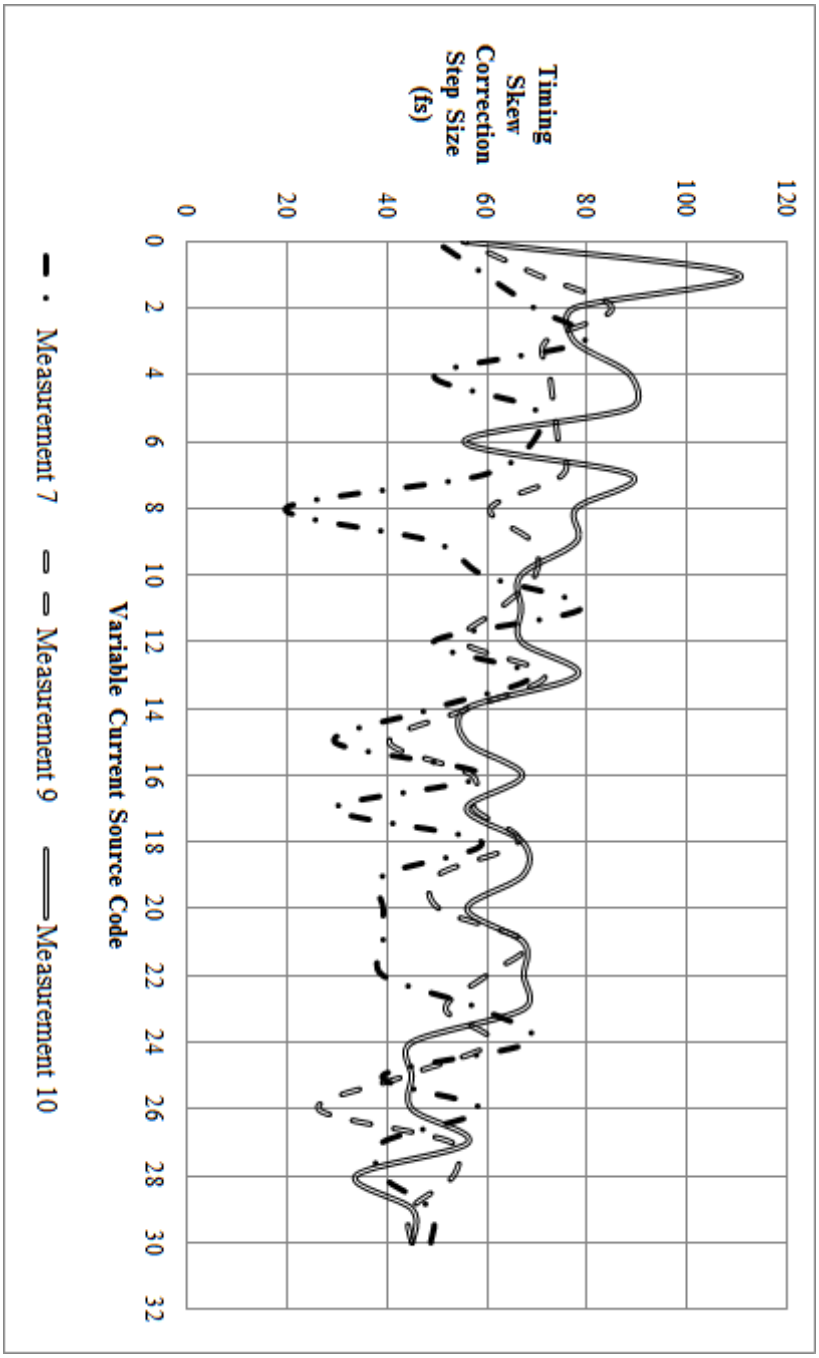


Figure 5.10: Variable Current Source Timing Skew Precision Over Current Source Codes

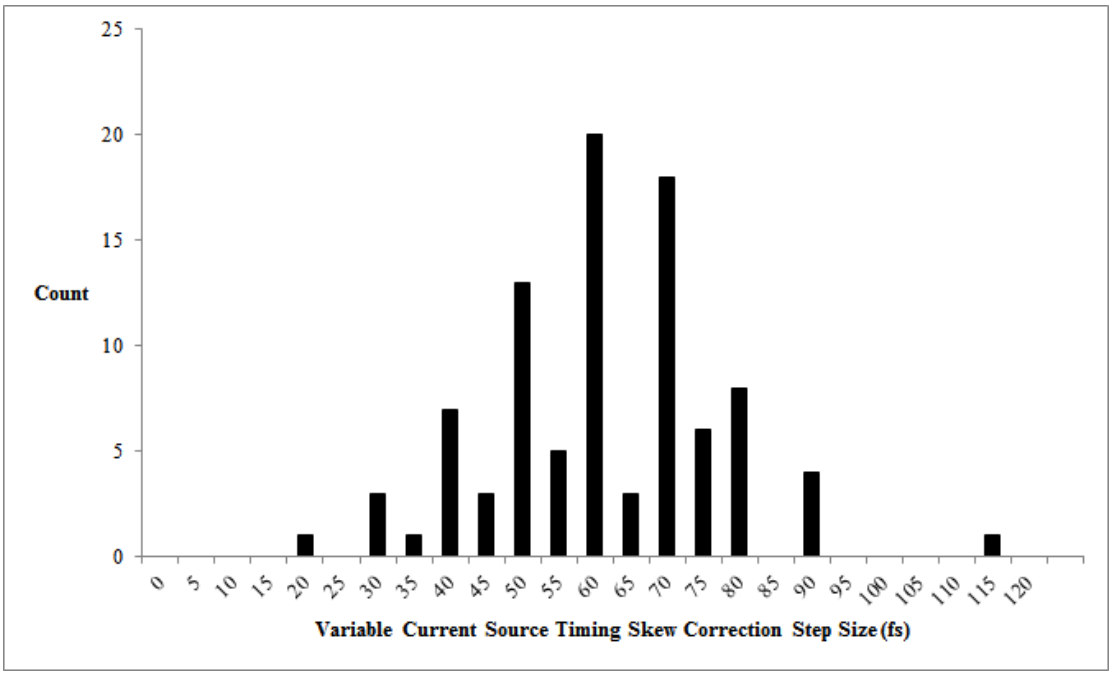


Figure 5.11: Distribution of Variable Current Source Timing Skew Correction Precision

A compilation of the captured FFT plots from the key timing skew performance measurements are shown in Figure 5.12. In Figure 5.12 VC serves as the short form of variable capacitor bank and VCS serves as the variable current source short form. Further note that the timing skew magnitude axis does not correspond to the dB value on the left axis, but instead represents the magnitude of the timing skew for a tone of that vertical height, which is again calculated based off of the SFDR. These FFT plots show that the timing skew introduced by the test chip can be corrected to well below the other spurious and harmonic tones at an input frequency of 110 MHz. Additionally the test chip can correct timing skew tones corresponding to magnitudes of up to +/- 91.5 ps (i.e. the range of 183 ps). Furthermore, the timing skew tone appears at the expected frequency of 47.504 MHz. The timing skew range compares reasonably well with the post-layout simulated range of 143 ps, with the

discrepancy likely being due to the difference in the simulated and measured capactive load the test chip drives.

Lastly, the measurements verifying that the timing skew correction applies to and holds over different input frequencies are shown in Figure 5.13 to Figure 5.15. The timing skew spurious tone appears at the expected frequency of 52.502 MHz and can be corrected for with the same settings as in the 110 MHz case. Furthermore, the tone magnitude is smaller for the same correction settings for example, the capacitor code setting of 127 which for 10 MHz the tone is approximately at -82 dB whereas for an input frequency of 110 MHz the tone magnitude is approximately -62 dB. This agrees with the theory presented in Chapter 2 which showed the dependence of the timing skew tone on input frequency which increases in magnitude as the input frequency increases.

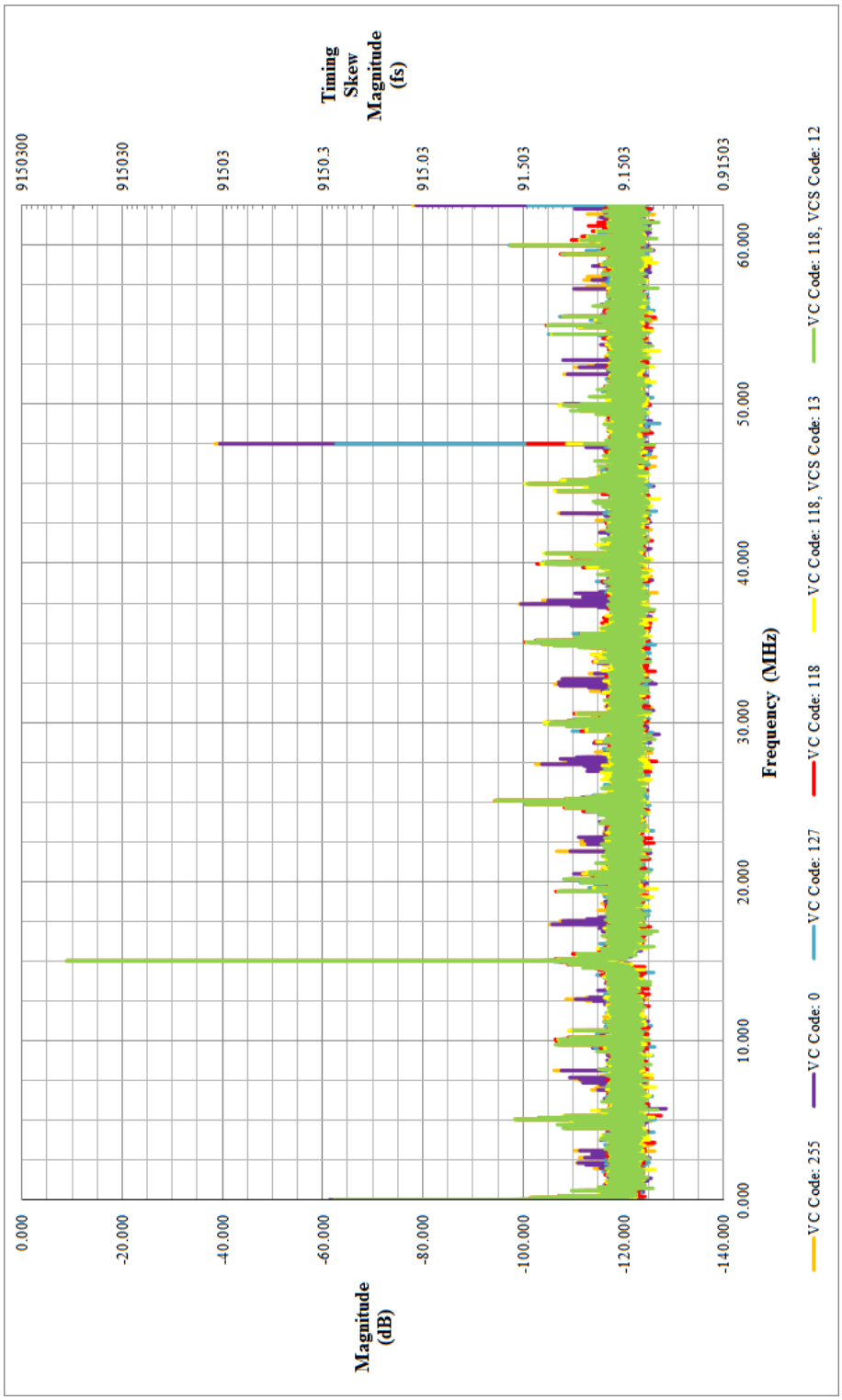


Figure 5.12: FFT Timing Skew Correction Range and Precision Performance

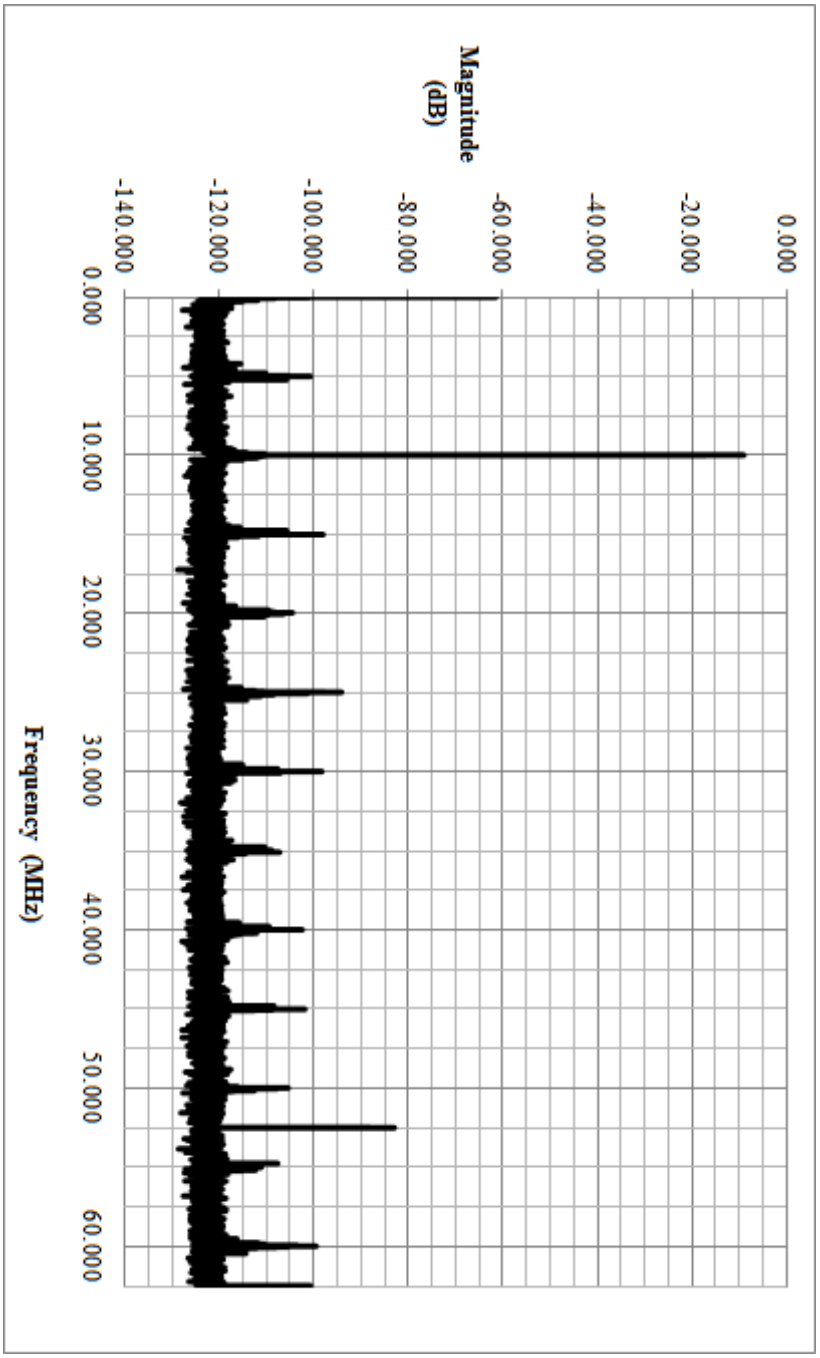


Figure 5.13: Alternate Input Frequency FFT Performance for Variable Capacitor Code 127

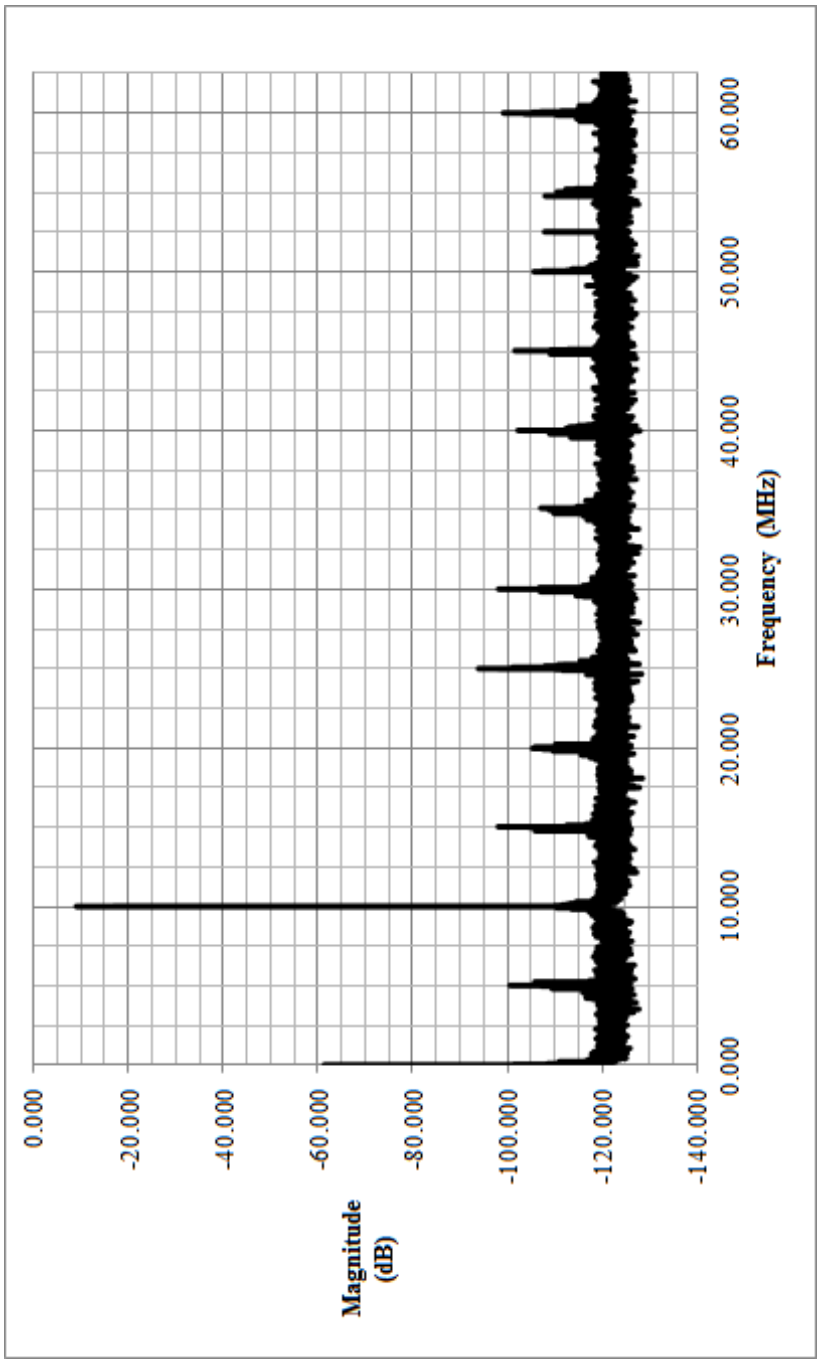


Figure 5.14: Alternate Input Frequency FFT Performance for the Variable Capacitor Code 118

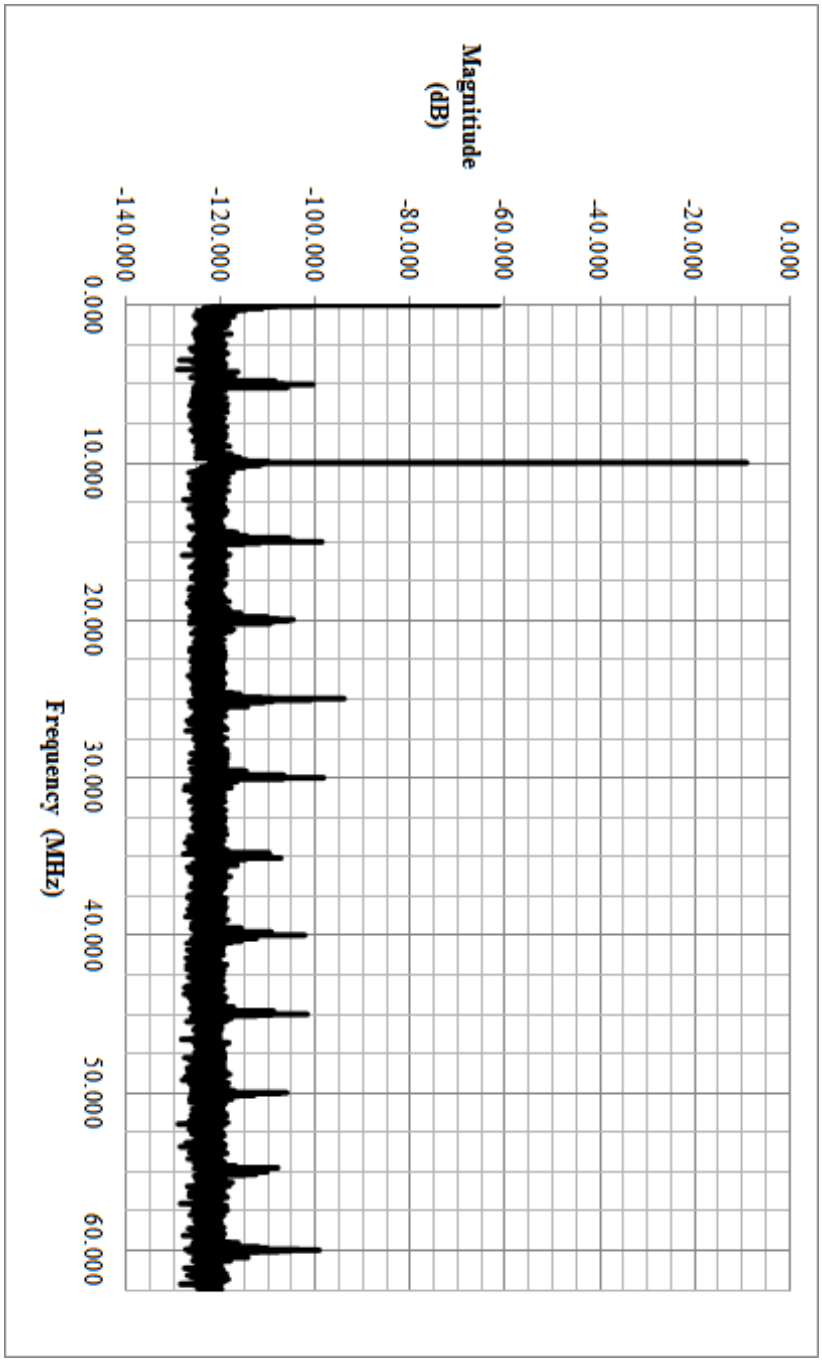


Figure 5.15: Alternate Input Frequency FFT Performance for Variable Capacitor Code 118 and Variable Current Source Code 13

5.3.4 Additive Jitter Measurements

The four SNR measurements from the test chip are shown in Table 5.6.

Table 5.6: SNR Measurements for Output Jitter Calculation

Measurement Type	**Input Frequency (MHz) [Aliased]**	**Measured SNR**	**Calculated ε**	**Calculated $\Delta T_{JITTERA/B}$ (fs)**
A	9.99832153	70.01	19.70	N/A
	110.004425 [14.996]	69.05	N/A	227.3
B	9.99832153	70.29	19.044	N/A
	110.004425 [14.996]	68.7	N/A	294.2

As was stated in Section 5.2.4, 'A' measurements were taken without the test chip in the sampling clock while 'B' measurements were taken with it present. Based on these measurements and (5.3) the total rms jitter ΔT_{JITTER} for the test chip is:

$$\Delta T_{JITTER} = \sqrt{294.2^2 - 227.3^2} = 186.8\, fs \tag{5.4}$$

Comparing the measured jitter in (5.4) to the approximate simulated jitter calculated in Section 4.4 results in approximately 110 fs for the simulated total chip jitter and 186.8 fs for the measured total test chip jitter. As expected, the simulated jitter is quite a bit better than the measured, most likely due to the precision/time/convergence limitations on accurate jitter simulations for large circuits. However, the measured and simulated do not differ by more than a factor of two which is encouraging in that the simulations seem to model the jitter relatively well (i.e. if longer, higher precision simulations were/could be performed on the full

test chip the simulated value would likely converge on the measured). In regards to the original design goal of 25 fs of additive jitter for the variable delay differential buffer, it is not possible to measure the additive jitter of just the test chip's differential buffer to verify how close the fabricated buffer is to the design goal. However, in comparing the results of (5.4) and the approximate simulated jitter calculation in Section 4.4, it is not unreasonable to say that the measured jitter of just the variable delay differential buffer should be relatively close (i.e. within a factor of 2) of the design goal. In saying this, a test chip should be fabricated with just the variable differential buffer on it to better verify its jitter performance relative to the design goal.

5.4 Improvements and Future Considerations

The fabricated test chip overall operated as expected and produced results that were within reason. However, there were two non-ideal behaviors found with the circuit. First, as mentioned in the previous section, the test chip exhibited an unstable bias point which resulted in the raised and sporadic noise floor. This is attributed to the DFF's that divide the incoming clock by 2, not having sufficient gain at the nominal bias current to switch properly with a sine wave input. To improve this in a future implementation of the test chip, either a lower bias current or revised transistor sizing's to increase the gain of the D-latches should be used. The second non-ideal behaviour, was observed in the final simulation of the test chip with the input as a sine wave instead of the sharp rising square wave used in the simulations pre-tapeout. The issue observed is with the glitch at time points 20 ns and 36 ns for the A path and 12 ns and 28 ns for the B path. These glitches should not be present, as the signal at these points should not be switching. The reason for this switching is due to the delay between CLK_{IN} and $CLK_{IN}/2$, therefore to fix this a buffer should be inserted such that all the signals applied to the first set of NAND's arrive at the same time.

Due to limited time and die area, not all of the circuits or tests that are useful to fully characterizing the performance of the test chip and its internal circuits could be included or performed. In terms of the circuits, both the NAND gate and the variable delay differential buffer should be fabricated as individual circuits so that their jitter or just for the NAND, their performance can be compared to the traditional implementations in terms of transient and harmonic performance. For the additional tests that should be performed, there are several. First, the performance metrics measured in the previous sections should be done over different supply voltages, temperatures and over longer time spans. This is to characterize how stable the timing skew correction circuit is under these common variations. Second, the power supply rejection ratio (PSRR) performance of the test circuit and the individual gates previously mention should be measured. This is to verify the noise suppression ability of the differential structures used. Lastly, the oscilloscope's input capacitance as well as the all the sources of capacitance between the test chip and the clock inputs on the AD9265 should be measured to more accurately compare simulations to the measured results. In addition to these suggest future steps and improvements, a calibration algorithm could be developed to allow the timing skew correction circuit to have a closed loop means of minimizing the spurious tones due to the timing skews. This calibration method should be designed to handle varying samples rates, operating temperatures and supply voltages.

Chapter 6

Conclusions and Future Work

The SFDR and SNR performance of time-interleaved analog-to-digital converters suffer if the non-idealities of timing skews and jitter are not minimized. A good way to minimize/correct for these non-idealities is in the analog domain. This thesis successfully presented the analysis, design and fabrication of an analog timing correction test circuit that was able to isolate timing skew behaviour, precisely control the timing skew over a wide range of timing skew and add minimal jitter while doing this. The fabrication test chip achieved a measured timing skew precision of approximately 60 fs over a timing skew range of approximately 183 ps. Additionally the entire test circuit had a measured total rms output jitter of approximately 187 fs. These measured results achieved are reasonably close to the original design goals of the thesis and prove the success of the designed test chip.

In order to achieve these results, it was found that using a variable delay differential buffer is a good way to balance the timing skew precision, range and output jitter requirements demanded of a timing skew correction circuit. The variable delay should be achieved by varying both the capacitive load seen the differential buffer in combination with varying the bias current to achieve the desired timing skew correction precision. In designing the variable delay differential buffer it was

determined that the overdrive voltage if the input transistors should be maximized in combination with minimizing the gain of the buffer such that the overall output jitter is minimized. Additionally the noise of the bias transistor and bias network should also be considered and minimized in order to further reduced the output jitter of the variable delay differential buffer. Beyond this, the design of a unique (to this author's best knowledge) differential NAND gate was presented that better balances the signalling and parasitics within the gate for better differential operation. Finally, an architecture that allows timing skews exclusively to be tested and evaluated was shown and proved to operate as intended.

During the design and evaluation of the test chip, some recommendations for future work and improvements were identified. The variable delay differential buffer should be taped out on as a separate circuit with different sizing's to completely evaluate the output jitter performance of the circuit and the accuracy of the simulations. The same should be done for the differential NAND gate to evaluate not only its jitter performance but also its harmonic and transient performance to confirm its improved differential behavior. As mentioned earlier, the accuracy of the jitter simulations should be verified by accurately determining the load capacitance in combination with the previous recommendations. Furthermore, research should be done to find methods to improve the simulation time, accuracy and convergence of precise jitter simulations on large circuits; helping to solve some of the jitter simulation issues encountered in this thesis. The performance of the test chip should be evaluated over temperature, voltage, and time to evaluate how the timing skew correction holds over these variations. In combination with this, a method of incorporating an online background calibration routine should be developed to ensure the correction is maintained over these variations. Finally, to improve the existing test chip, the DFF and input clock path should be redesigned such that the low gain and observed glitching is corrected.

Appendices

Appendix A

Test Chip and PCB Pin Mapping and Pin Description

The pin mappings between the test chip and test PCB as well as their corresponding pin description are included in Table A.1.

Table A.1: Pin Mapping and Pin Description of the Test Chip and PCB

Pin Number	Layout Pin Name	PCB Pin Name	Pin Description
1	NC	GND	Not Connected/Signal Ground
2	NC	GND	Not Connected/Signal Ground
3	VSS	GND	Signal Ground
4	DFF_BIAS	DFF_B	DFF Circuit Bias
5	VSS	GND	Signal Ground
6	VDD	1.8V	1.8V Supply
7	VDD	1.8V	1.8V Supply

Pin Number	Layout Pin Name	PCB Pin Name	Pin Description
8	VSS	GND	Signal Ground
9	R1	TP14	Bias Resistor Test Point
10	VSS	GND	Signal Ground
11	CLK2+	N/A	Not Implemented
12	CLK2-	N/A	Not Implemented
13	CLK-	CLK-	Negative Differential Clock Input
14	CLK+	CLK+	Positive Differential Clock Input
15	VSS	GND	Signal Ground
16	R2	TP13	Bias Resistor Test Point
17	VSS	GND	Signal Ground
18	VDD	1.8V	1.8V Supply
19	VDD	1.8V	1.8V Supply
20	VSS	GND	Signal Ground
21	NAND_BIAS_0	NAND_B0	NAND0 Circuit Bias
22	VSS	GND	Signal Ground
23	NC	GND	Not Connected/Signal Ground
24	NC	GND	Not Connected/Signal Ground
25	NC	GND	Not Connected/Signal Ground
26	VDD	1.8V	1.8V Supply
27	VDD	1.8V	1.8V Supply
28	VSS	GND	Signal Ground
29	DLY_BIAS	DLY_B	Delay Circuit Bias
30	VSS	GND	Signal Ground
31	VDD	1.8V	1.8V Supply

Pin Number	Layout Pin Name	PCB Pin Name	Pin Description
32	VDD	1.8V	1.8V Supply
33	VSS	GND	Signal Ground
34	I0	I0	Variable Current Source Control Bit 0
35	VSS	GND	Signal Ground
36	VDD	1.8V	1.8V Supply
37	VSS	GND	Signal Ground
38	NAND_BIAS_1	NAND_B1	NAND1 Circuit Bias
39	I1	I1	Variable Current Source Control Bit 1
40	NC	GND	Not Connected/Signal Ground
41	NC	GND	Not Connected/Signal Ground
42	NC	GND	Not Connected/Signal Ground
43	I2	I2	Variable Current Source Control Bit 2
44	I3	I3	Variable Current Source Control Bit 3
45	I4	I4	Variable Current Source Control Bit 4
46	CAPB6	CB6	Path B Variable Capacitor Bank Bit 6
47	CAPB7	CB7	Path B Variable Capacitor Bank Bit 7
48	VSS	GND	Signal Ground
49	VDD	1.8V	1.8V Supply
50	VSS	GND	Signal Ground

Pin Number	Layout Pin Name	PCB Pin Name	Pin Description
51	VO+	OUT+	Positive Differential Output
52	VO-	OUT-	Negative Differential Output
53	VO2-	OUT2-	Not Implemented
54	VO2+	OUT2+	Not Implemented
55	VSS	GND	Signal Ground
56	VDD	1.8V	1.8V Supply
57	VSS	GND	Signal Ground
58	CAP7	C7	Path A Variable Capacitor Bank Bit 7
59	CAP6	C6	Path A Variable Capacitor Bank Bit 6
60	CAP5	C5	Path A Variable Capacitor Bank Bit 5
61	CAP4	C4	Path A Variable Capacitor Bank Bit 4
62	CAP3	C3	Path A Variable Capacitor Bank Bit 3
63	NC	GND	Not Connected/Signal Ground
64	NC	GND	Not Connected/Signal Ground
65	NC	GND	Not Connected/Signal Ground
66	CAP2	C2	Path A Variable Capacitor Bank Bit 2
67	CAP1	C1	Path A Variable Capacitor Bank Bit 1
68	VSS	GND	Signal Ground
69	VDD	1.8V	1.8V Supply

Pin Number	Layout Pin Name	PCB Pin Name	Pin Description
70	VSS	GND	Signal Ground
71	CAP0	C0	Path A Variable Capacitor Bank Bit 0
72	VSS	GND	Signal Ground
73	VDD	1.8V	1.8V Supply
74	VDD	1.8V	1.8V Supply
75	VSS	GND	Signal Ground
76	VAR_BIAS	VAR_B	Variable Current Source Circuit Bias
77	VSS	GND	Signal Ground
78	VDD	1.8V	1.8V Supply
79	VDD	1.8V	1.8V Supply
80	NC	GND	Not Connected/Signal Ground

Appendix B

Test PCB Documentation

The schematics for the test PCB are shown in Figure B.1 to Figure B.3. Additionally the corresponding layer masks and signal routing are included in Figure B.4 to Figure B.9.

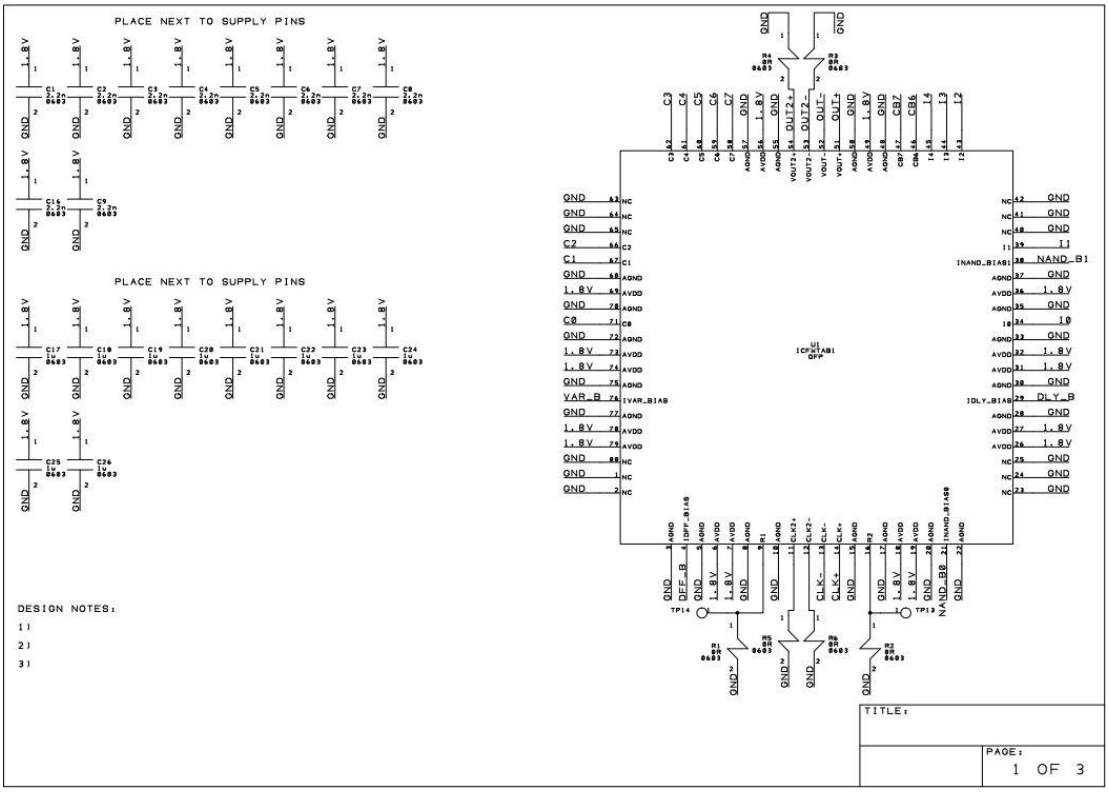


Figure B.1: Page 1 of the PCB Schematics Showing the Test Chip Connections

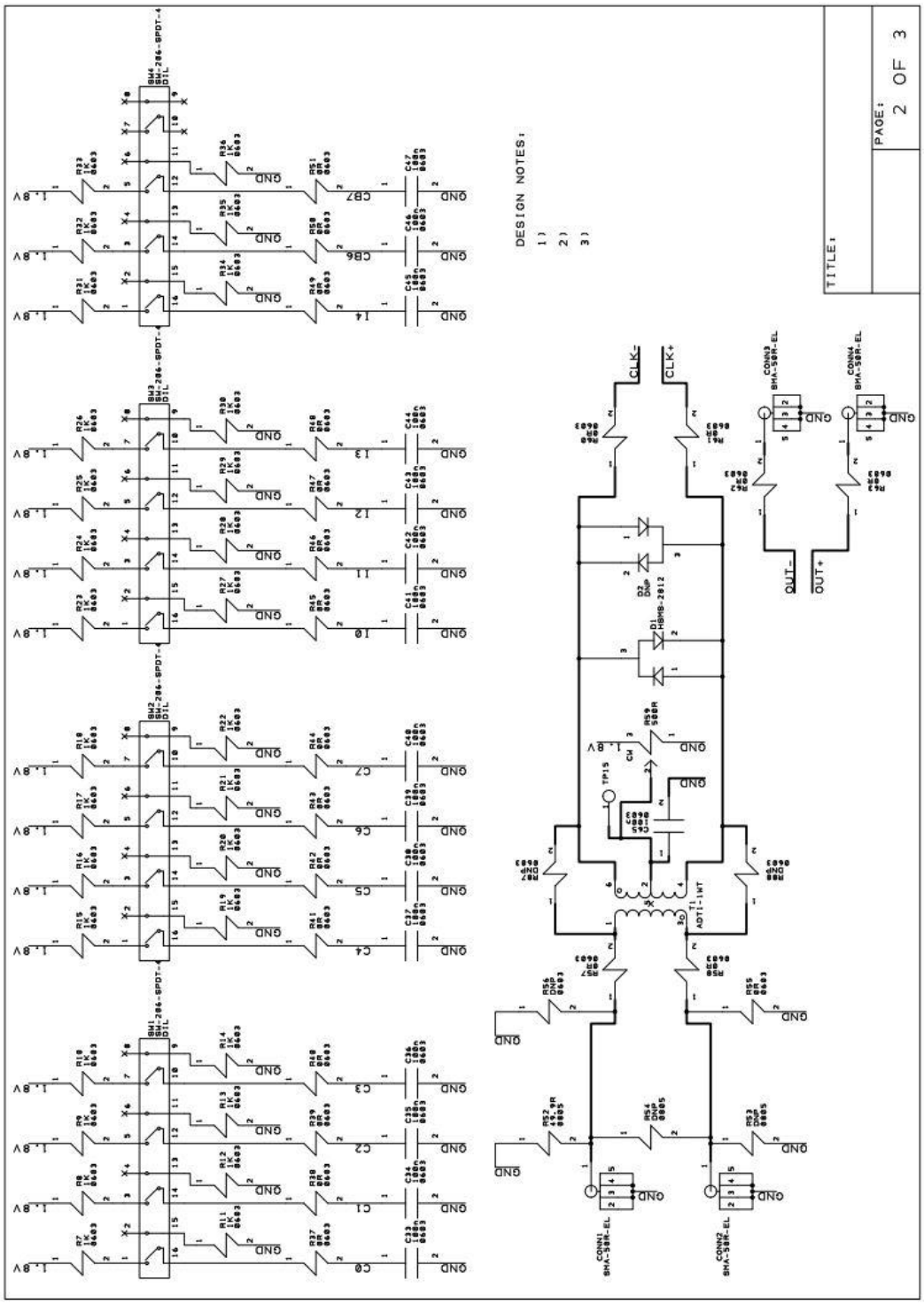


Figure B.2: Page 2 of the PCB Schematics Showing the I/O Connections

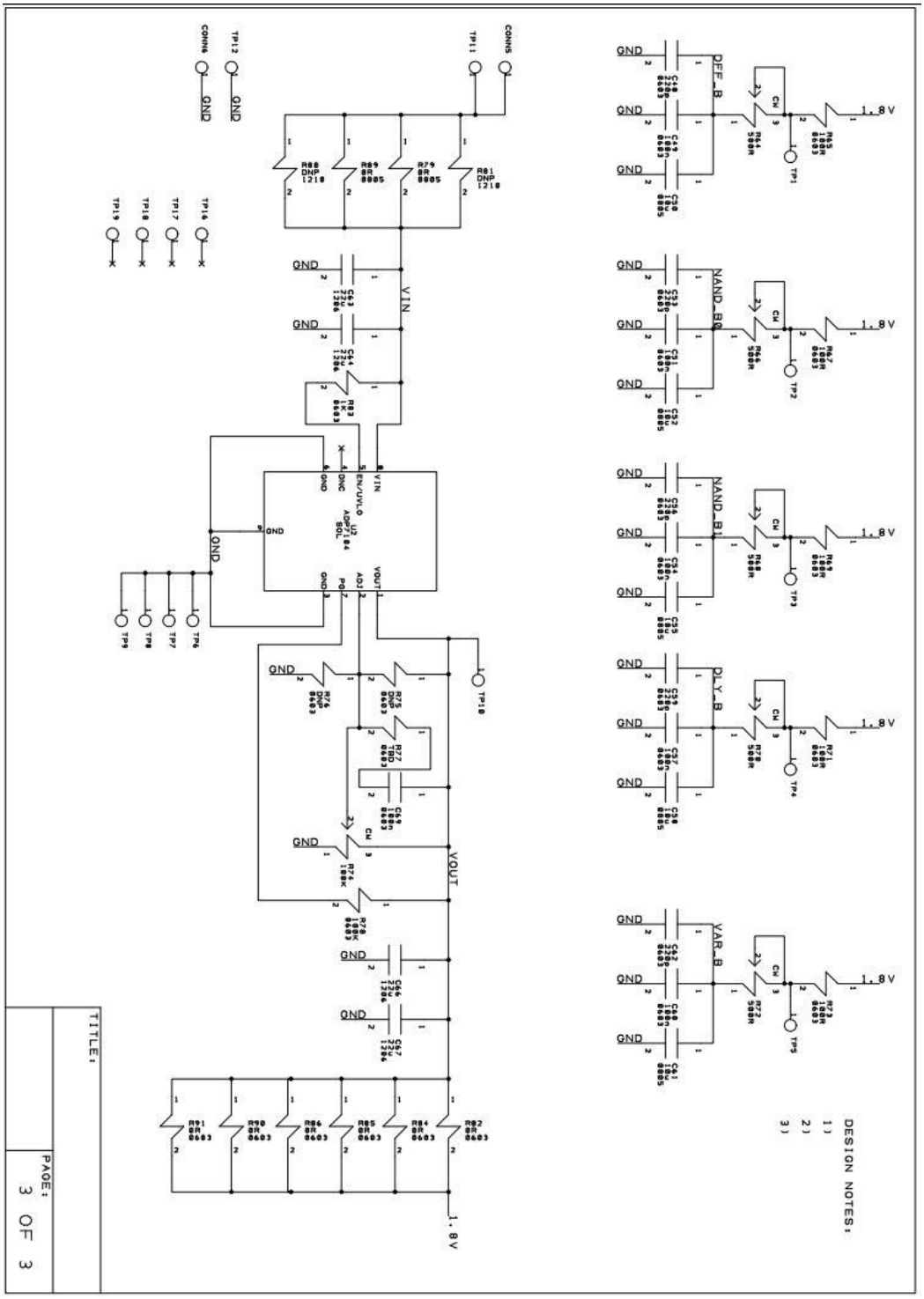


Figure B.3: Page 3 of the PCB Schematics Showing the Power and Bias Supplies

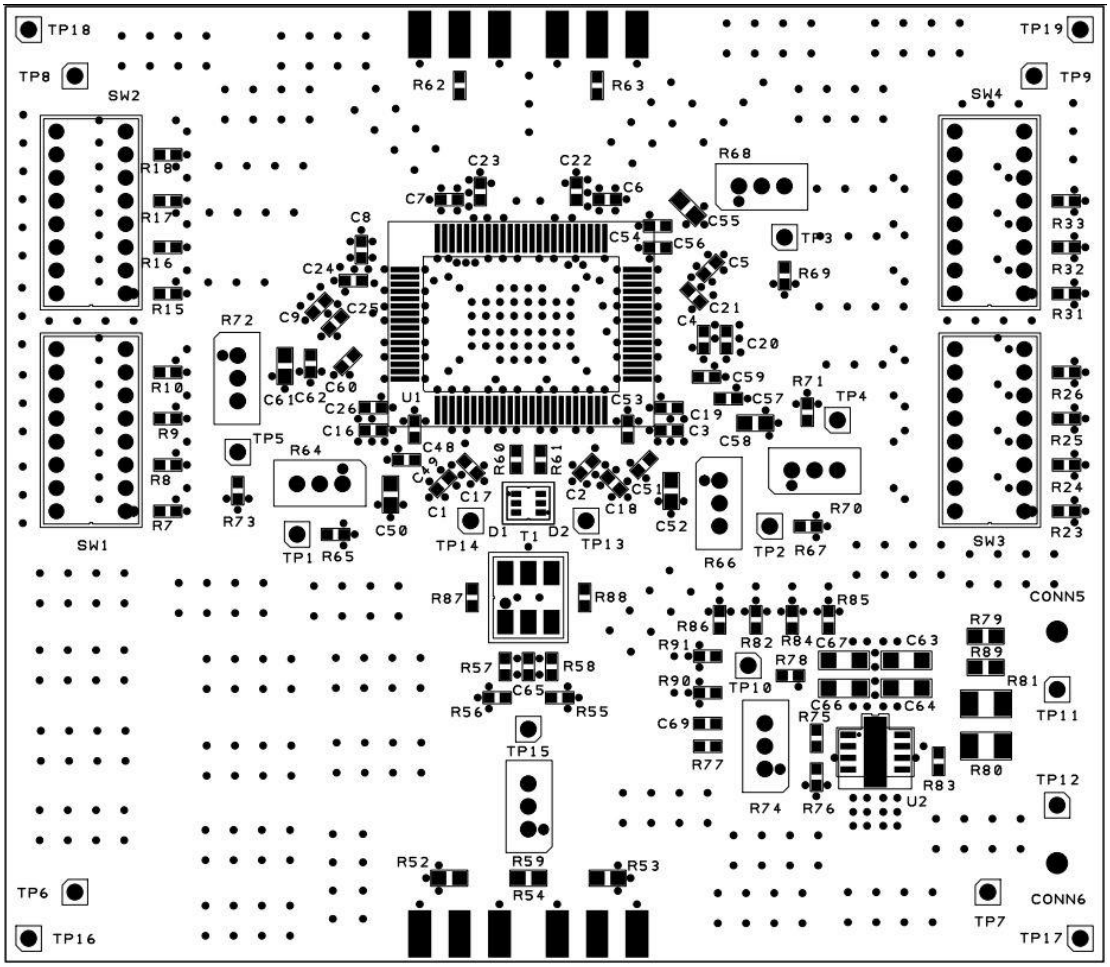


Figure B.4: Component Locations on Top Layer of the Test PCB

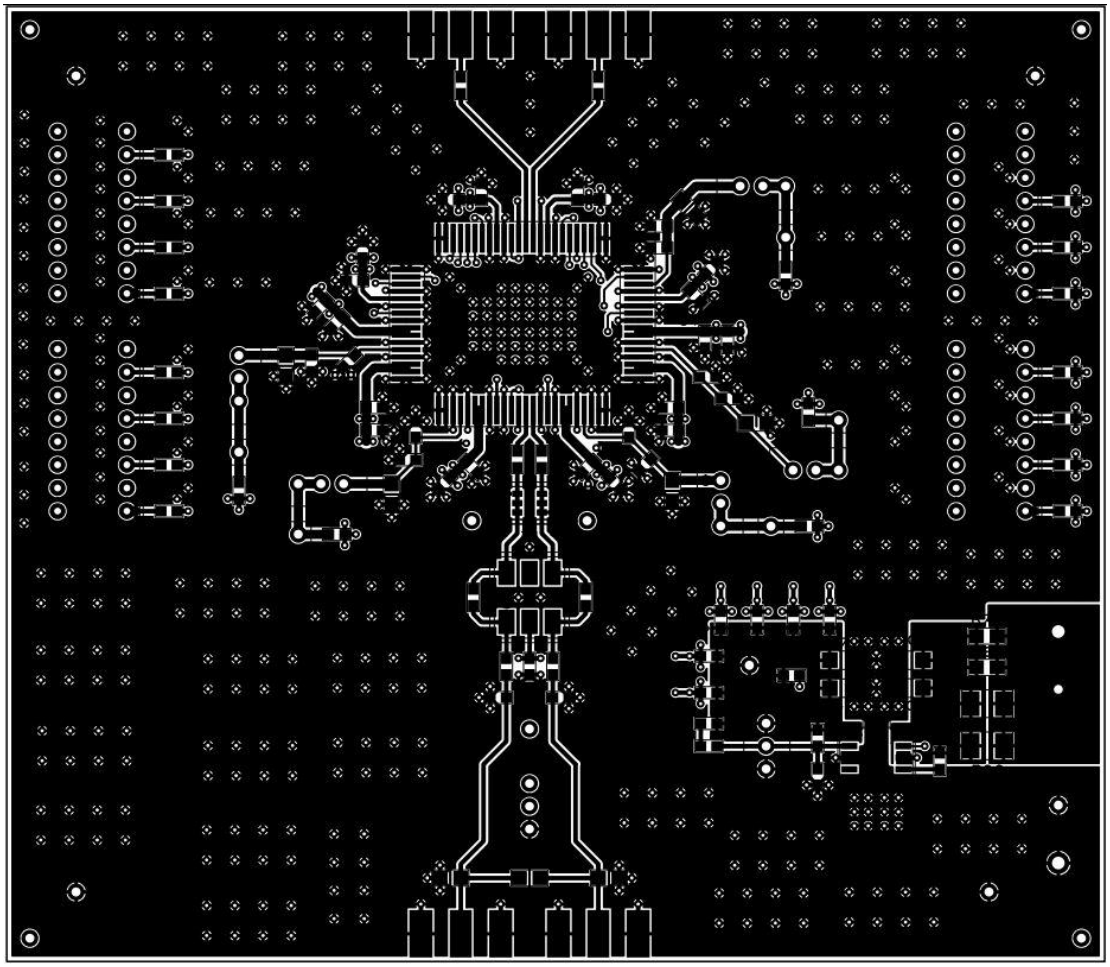


Figure B.5: Signal Routing on Top Layer of the Test PCB

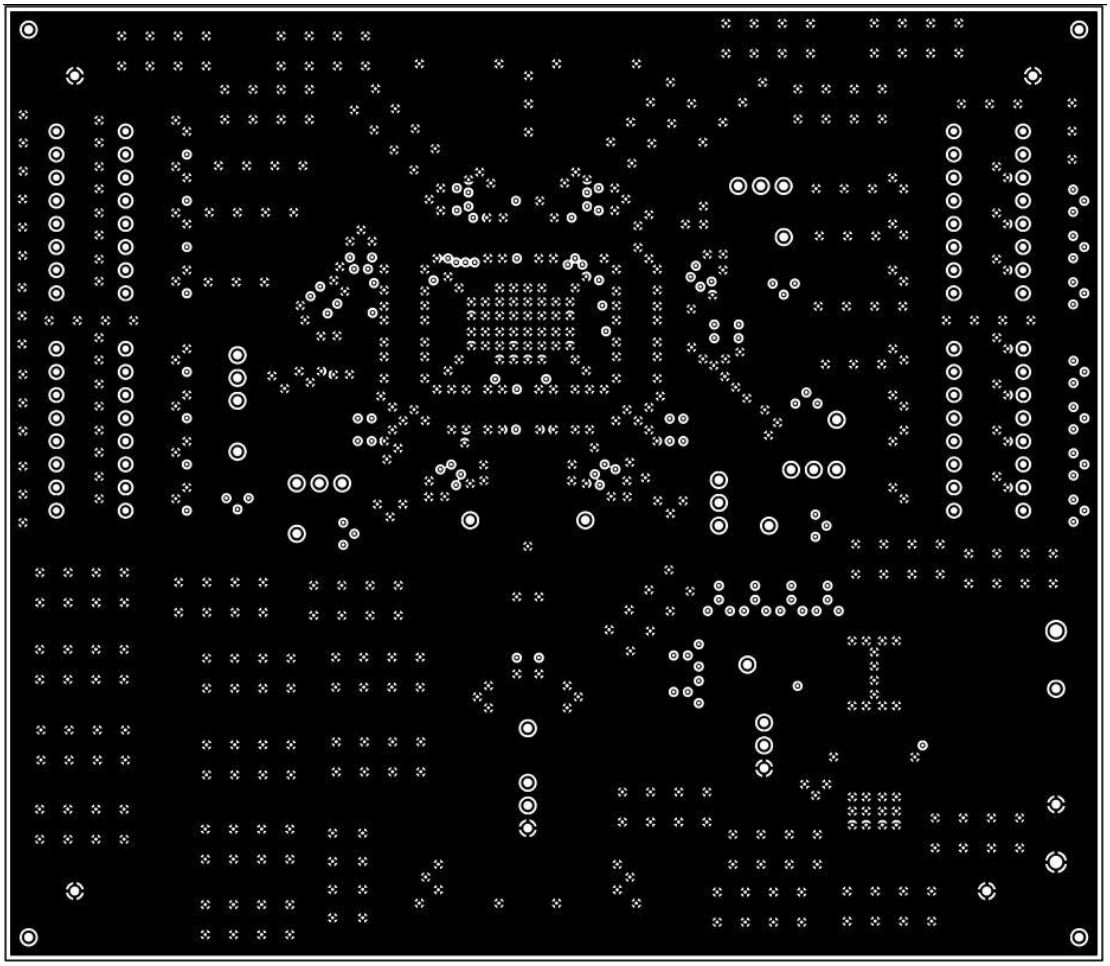


Figure B.6: Ground Plane (2nd layer) of the Test PCB

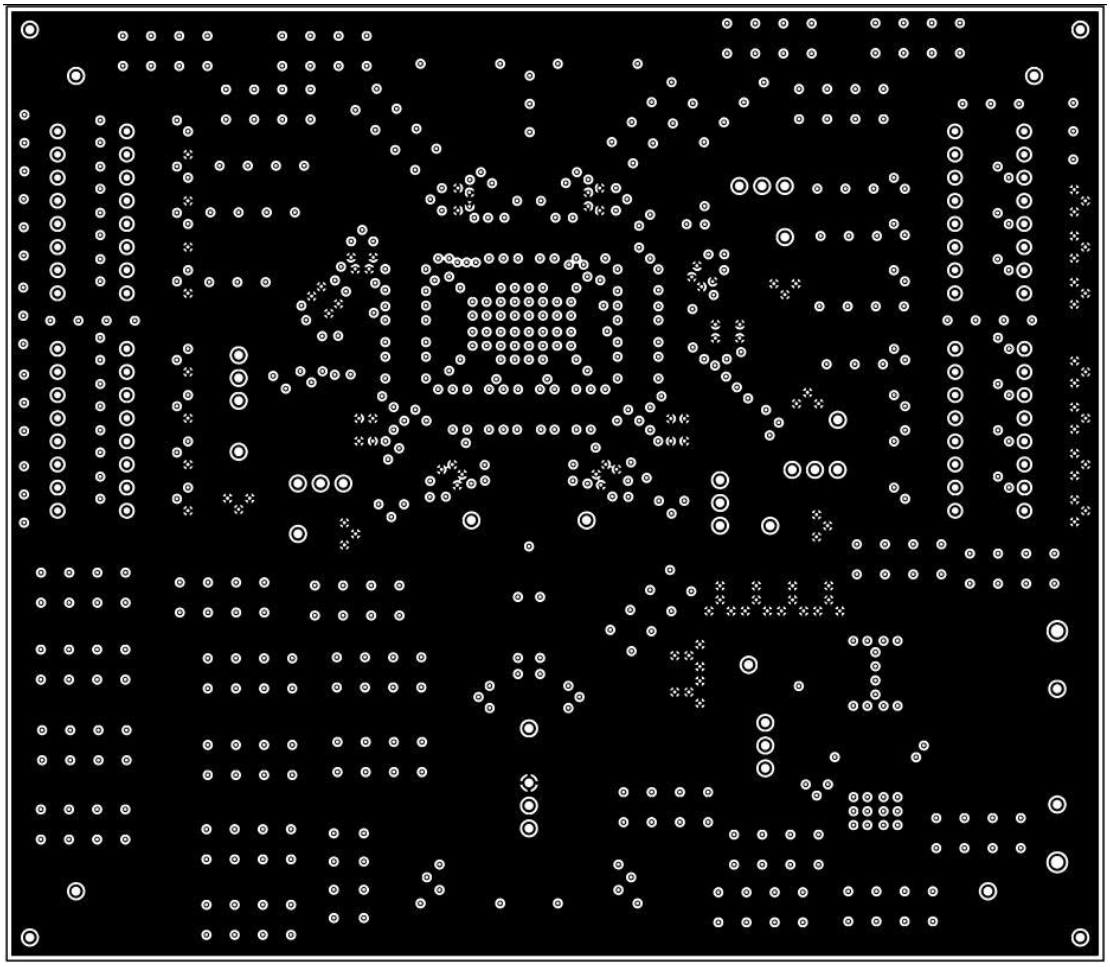


Figure B.7: Power Plane (3rd Layer) of the Test PCB

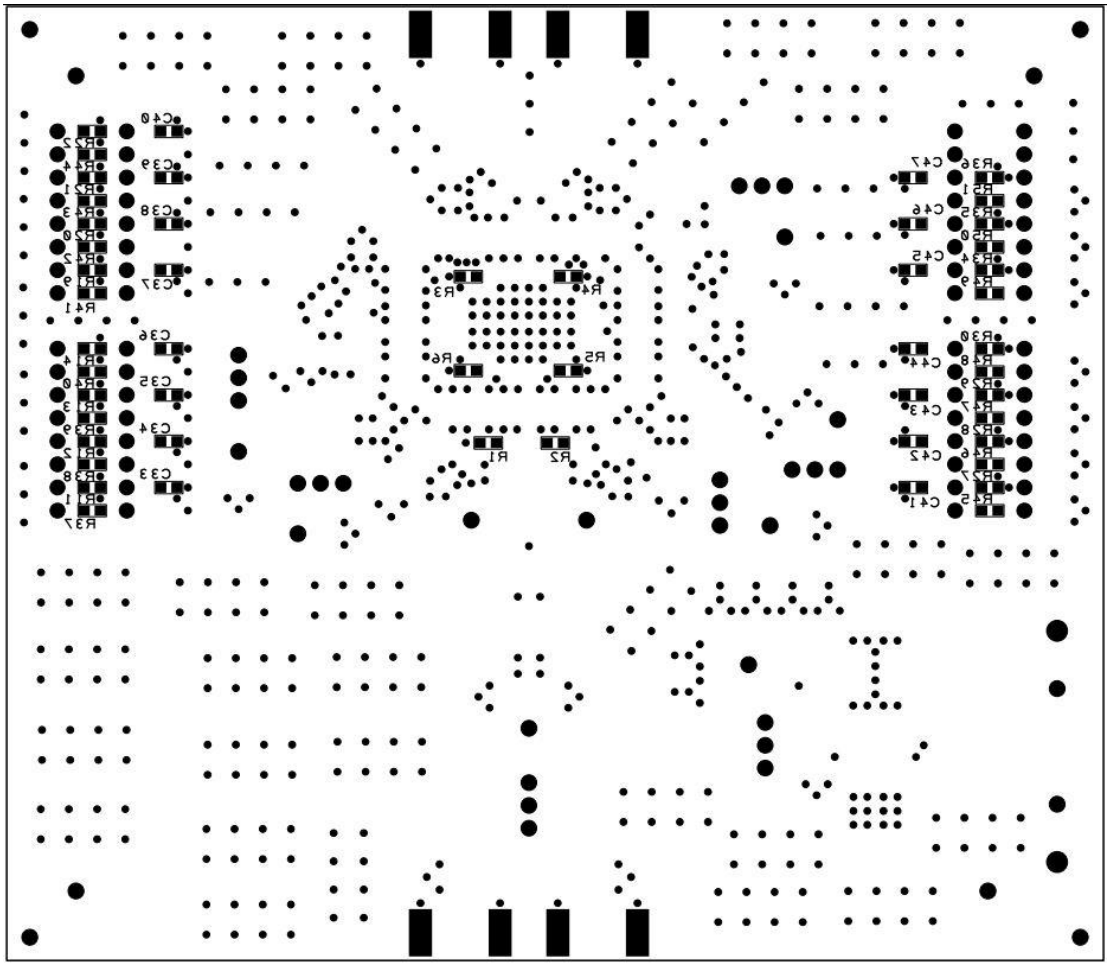


Figure B.8: Component Locations on Bottom Layer of the Test PCB

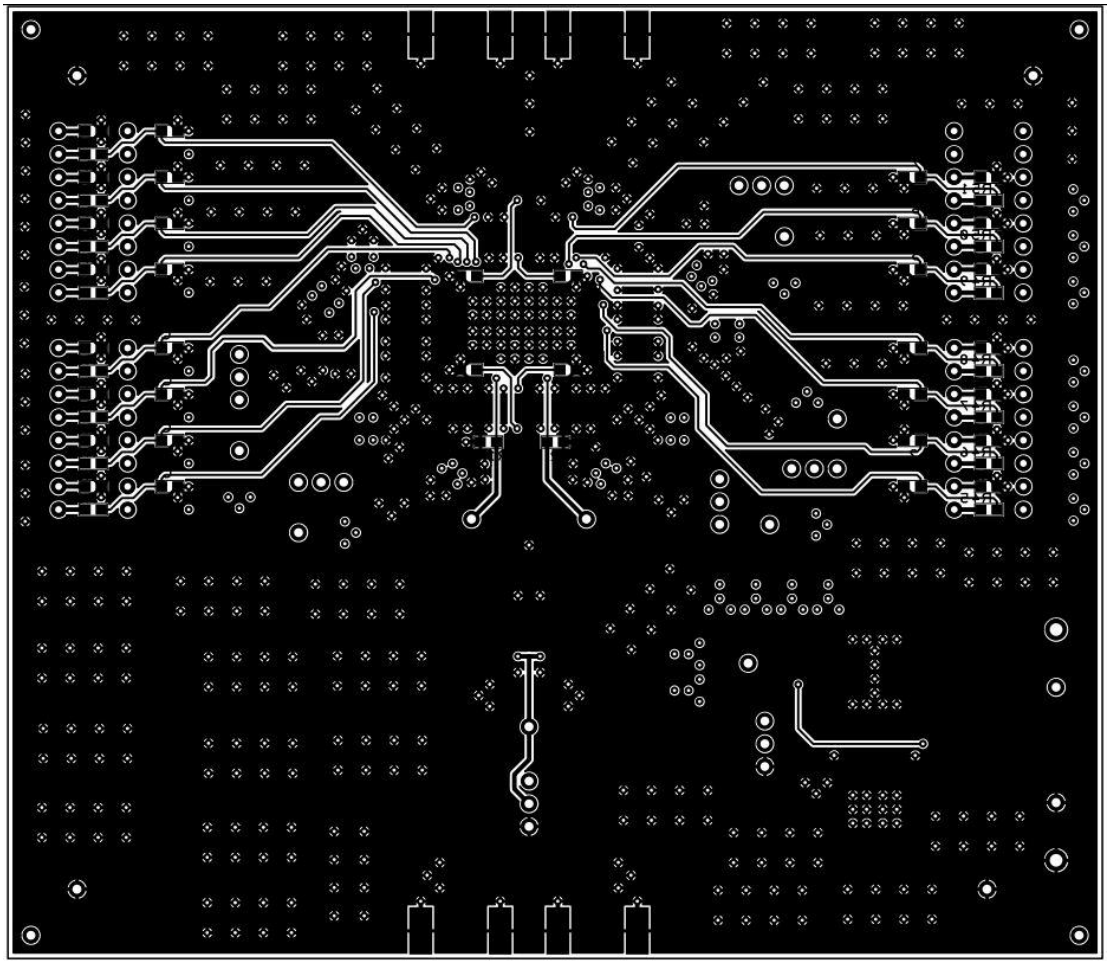


Figure B.9: Signal Routing on Bottom Layer of the Test PCB

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