Design of a Time Based Analog to Digital Converter

by

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I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

Analog to digital converter (ADC) plays a very important role in any mixed analog/digital system. Because digital CMOS technology can take advantage of technology scaling, system designers try to increase the percentage of the digital part of the system. This means moving the ADC more and more towards the input of the system which results in making the role of the ADC more and more critical. With technology scaling, the switching characteristics of MOS transistors offer superb timing accuracy at high frequencies. This makes the time based analog to digital converter (TADC) a good alternative to the conventional ADCs in sub-micron region.

In this thesis, an all digital TADC structure is proposed. This TADC is based on an analog to time converter (ATC), followed by a time to digital converter (TDC). The TDC is based on sigma-delta ($\Sigma\Delta$) modulation. A non-linear multi-bit internal quantizer in $\Sigma\Delta$ modulator is used to counteract the nonlinearity introduced when the VCO is used as the ATC. The novel TADC also uses an implicit sample and hold (S/H) circuit to reduce area. Dynamic element matching (DEM) is used to improve the robustness of the system against random mismatch in the multi-bit quantizer. Both first and second order $\Sigma\Delta$ modulator TADC are proposed. Simulations and measurements on the proposed TADC are provided. Measurements, from a prototype chip fabricated using 0.13μm CMOS technology, show that the first order TADC has achieved a dynamic range of 11 bits for a bandwidth of 2MHz. While simulation results show a dynamic range of 12 bit. Simulations show that the second order TADC has achieved a dynamic range of 12bit for a bandwidth of 20MHz.

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Dedication

To my parents, My brother, and my sister

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List of Abbreviations

ADC	Analog to Digital Converter
AFC	Analog to Frequency Converter
APC	Analog to Period Converter
BW	Bandwidth
CAL	Clocked Level Averaging
CMC	Canadian microelectronics cooperation
CMOS	Complementary Metal Oxide Semiconductor
D	Number of bits
DAC	Digital to Analog Converter
dB	decible
DEM	Dynamic Element Matching
D-FF	D flip-flop
DMD	Dual Modulus Divider
DNL	Differrential Non Linearity
DR	Dynamic Range
DSP	Digital Signal Processing
DWA	Data Weighted Averaging
ENOB	Effective Number Of Bits
FDC	Frequency to Digital Converter
FFT	Fast Fourier Transform
FM	Frequency Modulation
FS	Full Scale signal
GRO	Gated Ring Oscillator
ILA	Individual Level Averaging
INL	Integral Non Linearity
LSB	Least Significant Bit
MOS	Metal Oxide Semiconductor
MSB	Most Significant Bit
MUX	Multiplexer
NMOS	N-type Metal Oxide Semiconductor
NUS	Non-Uniform Sampling
op-amp	Operational Amplifier

OSR	Oversampling Ratio
PCB	Printed Circuit Board
PDC	Period to Digital Converter
PI	Phase Interpolation
PM	Phase Modulation
PMOS	P-type Metal Oxide Semiconductor
RF	Radio Frequency
S/H	Sample and Hold
$\Sigma\Delta$	Sigma Delta
SAR	Successive Approximation Register
SNR	Signal to Noise Ratio
SNRD	Signal to Noise and Distortion Ratio
TADC	Time based Analog to Digital Converter
TDC	Time to Digital converter
T_{ref}	The reference period
VCO	Voltage Controled Oscillator
VDL	Vernier Delay Line
V_{dd}	The supply voltage
V_{in}	The analog input voltage
V_{ref}	The reference voltage
V_{th}	The threshold of the inverter

Chapter 1

INTRODUCTION

Analog to digital converter is an essential block used in any mixed analog/digital system. As an example, in communication transceiver ADC plays the role of an interface between the analog front-end and the back-end digital signal processing (DSP) functions. Another example of other mixed analog/digital systems is disk drives application. Digital CMOS enjoys the advantage of technology scaling in terms of reducing the area of the digital part of the system [1, 2]. This results in making the ratio of analog to digital blocks increases. Thus, the general trend is to reduce the analog portion of the system (which generally cannot take advantages of this scaling) as much as possible, and to move the ADC more and more towards the input of the system. Moving the ADC towards the system input makes its design more challenging.

According to the way in which sampling is preformed, ADCs are divided into two types. The first type is called the Nyquist-rate ADCs. Flash ADC, successive-approximation ADC, and pipelined ADC are examples of this type of ADCs. The second type is called oversampling ADCs. Sigma-delta modulator is an example of this type. The oversampling conversion technique has recently become popular as it avoids many of the difficulties encountered with Nyquist ADCs, such as the use of anti-aliasing analog filters. According to the way in which conversion is performed, ADCs are divided into two types. The first type directly converts the analog input into digital output. The second type does the conversion in an indirect way by first converting the analog signal into an intermediate representation such as time. Then it converts this intermediate representation into digital code [3]. The focus of

this thesis is on the second type which is more suitable in deep submicron region. Time-based ADC (TADC) is more suitable in deep submicron region because the supply voltage reduction that comes along with technology scaling results in lower voltage swing. Small voltage swing causes two problems. The first problem is the low signal to noise ratio. The second problem arises from the fact that the threshold voltage of the transistor does not decrease with the same rate as the supply voltage. This results in making the design of the operational amplifier (op-amp), which is an essential building block in design of the ADC, difficult. Meanwhile with technology scaling, the switching characteristics of MOS transistors improve at high frequencies.

1.1 Motivation

One way to convert the analog voltage into a time representation is to use a voltage controlled oscillator (VCO). The VCO converts the analog voltage into time format by modulating its period according to the value of the analog voltage. The modulation is done by using the analog input to control the charging/discharging current of a capacitor that is connected to one of the VCO stages. The charging/discharging time of a capacitor, $t_{ch/disch}$, is governed by the non-linear input/output equation

$$t_{ch/disch} = C\frac{V_{swing}}{K \times V_{in}} \tag{1.1}$$

Here we assume that the charging/discharging current is linearly related to the analog input voltage, V_{in}. This non-linear relation results in making the conversion from analog to time a non-linear operation. This inherent non-linear property of VCO is the bottleneck for TADC design and cause distortion.

In the past, feedback [4] and digital calibration [5] techniques have been used to overcome this problem. However, the feedback technique reduces the input range while the calibration technique is complicated.

Timing jitter is another important aspect of the TADC. Reducing the timing jitter results in increasing the TADC resolution. Technology scaling helps directly in reducing the timing jitter by increasing the speed and hence slew rate of the circuit. However, technology scaling's role in reducing the distortion due to the non-linear relation in (1.1) is less obvious.

The objective of this thesis is to present a novel TADC structure. This TADC is based on an analog to time converter (ATC), followed by a time-to-digital converter (TDC). The TDC is based on sigma-delta ($\Sigma\Delta$) modulation. A non-linear internal quantizer in $\Sigma\Delta$ modulator is used to counteract the non-linearity introduced when the VCO is used as a ATC. The TADC uses an implicit sample and hold (S/H) circuit to reduce area. Dynamic element matching (DEM) is used to improve the robustness of the system against random mismatch.

1.2 Thesis Organization

The thesis consists of five chapters. Chapter 2 presents a review on some background material for ADC. Four new TADCs are presented in Chapter 3. System-level simulations are presented in this chapter along with some techniques to improve the performance of the TADC. In Chapter 4, circuit implementations of three TADC designs along with their layouts, and the printed circuit board (PCB) used for testing are presented. Circuit level simulations using Cadence and Eldo, and measurement results are also presented in Chapter 4. The conclusions of this work are drawn in Chapter 5.The suggested future work are also presented in this chapter.

Chapter 2

BACKGROUND

2.1 Analog to digital converter

An ADC is a device which converts continuous analog input signals to discrete output digital codes. Each digital code is a quantized version of the sampled analog signal at the corresponding time instant. Figure 2.1 shows an example of the output of a 3-bit ADC. The reverse operation is performed by a digital-to-analog converter (DAC) [6].

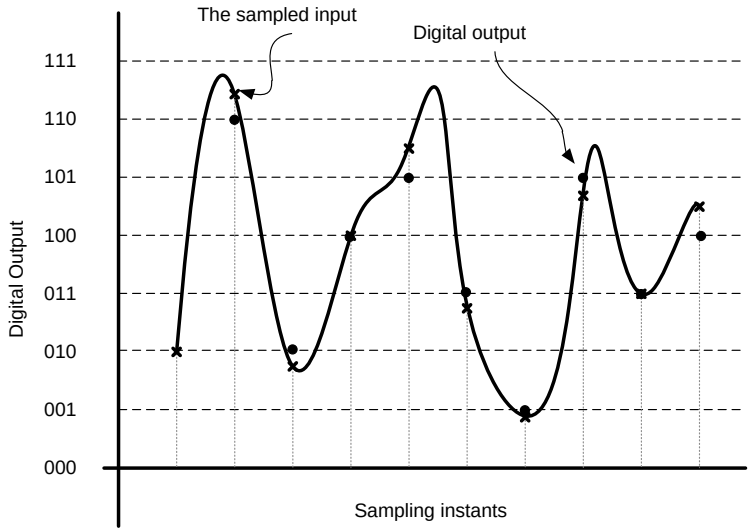

Figure 2.1: Example of 3-bit ADC

2.2 Sampling

The ADC samples the input signal with a rate called the sampling frequency, f_s. The sampling frequency must be at least equal to twice the maximum frequency appearing in the input signal Bandwidth f_{BW}, this condition is referred to as the Nyquist criterion [7].

$$f_s \geq 2 \times f_{BW} \tag{2.1}$$

If the system does not meet the Nyquist criterion, aliasing occurs, and we will not be able to reconstruct the original signal from its samples. Aliasing can be understood if we study the frequency spectrum of the signal. Assume that we have a signal which has a triangle frequency spectrum representation. From the Fourier transform theory, the sampling of a signal in time domain with a frequency f_s is represented in frequency domain by replicating the frequency spectrum of the signal around multiples of f_s. If $f_s > 2f_{BW}$, the frequency spectrum of the sampled signal will be as shown in Figure 2.2; otherwise it will be as shown in Figure 2.3.

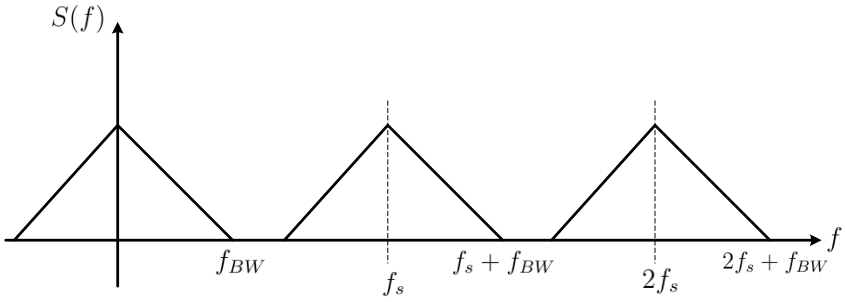

Figure 2.2: The spectrum of the samples signal in case $f_s \geq 2 \times f_{BW}$

As we can see from Figure 2.2, the replica around f_s does not affect the original spectrum of the signal. The original signal can be reconstructed using a low-pass filter. However, in Figure 2.3, the replica around f_s distorts the original spectrum of the signal (the dashed areas in Figure 2.3), and we will not be able to reconstruct the original signal from its samples. To avoid aliasing, an aliasing filter is usually required to band limit the input signal before applying it to the ADC.

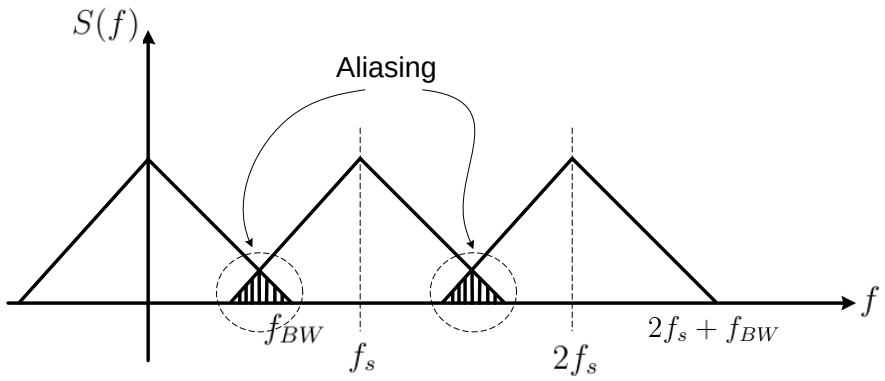

Figure 2.3: The spectrum of the samples signal in case $f_s \geq 2 \times f_{BW}$

2.3 Quantization

Quantization error happens when the ADC produces the same output for a certain range of the input. We define the resolution of the ADC as the smallest change in the input that results in change in the output digital code. Thus, making the resolution of the ADC as small as possible will result in reducing the quantization error in the ADC.

The resolution is defined in terms of the least significant bit (LSB), which is defined as

$$LSB = \frac{V_{FS}}{2^D} \tag{2.2}$$

Here, V_{FS} is the full scale input of the ADC and D is the number of the bits contained in the output digital code of the ADC. Therefore, to increase the resolution of the ADC we need to increase the number of bits. Quantization error (quantization noise) is defined as the difference between the original analog input and the resulting digital output. Figure 2.4 gives an example of quantization noise.

For an ADC, quantization error is always in the range of

$$-0.5 \times LSB \leq Quantization\ error \leq 0.5 \times LSB$$

2.4 ADC characteristics

Understanding the ADC characteristics helps to decide which type of ADC is suitable for a certain application. Due to non-idealities in circuit implementation of

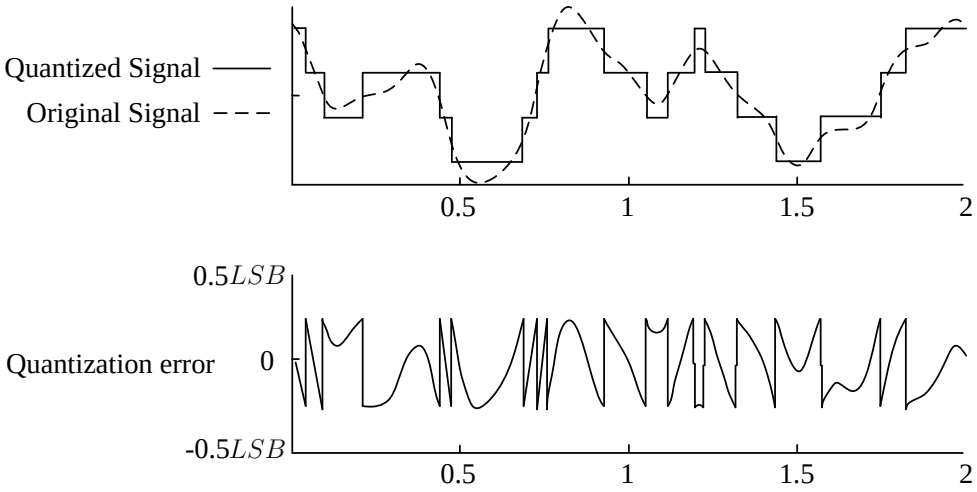

Figure 2.4: An example of quantization noise

the ADC, new types of error, other than the quantization error, are introduced. Appendix A.1 reviews some of these types of error that are independent of time (static). Appendix A.2 reviews some of these types of error that are time dependent (dynamic).

2.5 ADC types

As we can see in Figure 2.5, ADCs are divided into direct conversion ADCs, and indirect conversion ADCs. Direct conversion ADCs directly convert the analog signal into digital code. Indirect conversion ADCs do the conversion in an indirect way by first converting the analog signal into an intermediate representation; like time, by modulating the edges of a reference signal. Then this intermediate representation is converted into digital code. According to the sample frequency rate, both direct conversion ADCs and indirect conversion ADCs are divided into Nyquist rate ADCs, and oversampling ADCs. Nyquist rate ADCs, compared to oversampling ADCs, are usually suitable for applications that require high input signal frequency, while oversampling ADCs are usually suitable for applications that require low input signal frequency but also require high resolution.

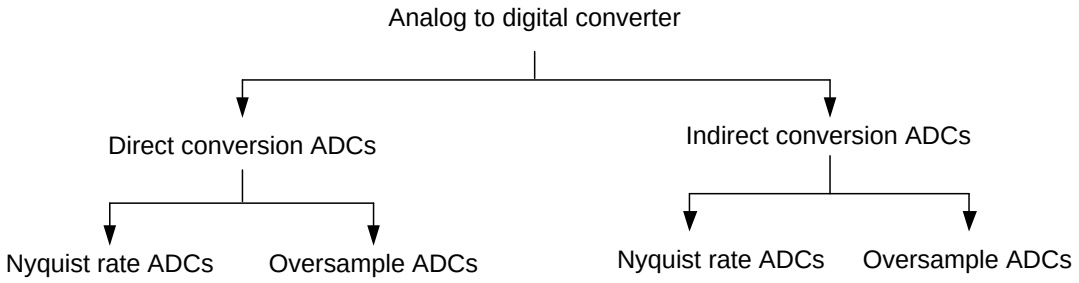

Figure 2.5: ADCs Types

2.5.1 Nyquist rate direct conversion ADCs

A Nyquist rate ADC is an ADC type in which the sampling frequency is equal to twice the maximum frequency in the input signal BW (the Nyquist frequency) [6], practically the sampling frequency is 5-10 times the BW. Flash ADC, pipelined ADC, and successive-approximation ADC are typical Nyquist-rate direct-conversion ADCs. As an example, we overview the flash ADC.

Flash ADC is the fastest type of ADC [8]. In this type of ADC the analog voltage input sample is compared with $2^D - 1$ reference values using $2^D - 1$ comparators. As we can see from Figure 2.6, the reference voltages are generated using a resistive divider with 2^D resistors. Each reference voltage is one LSB greater than the reference voltage immediately below it. Each reference voltage is connected to one of the comparators inputs, while the other input is connected to the analog voltage input sample. Each comparator produces a "1" when the analog input voltage sample is higher than the reference voltage connected to it. Otherwise, the comparator produces "0". The comparators produce thermometer code. The thermometer code is then decoded to the appropriate digital output code.

The drawback of this type of ADC is that it requires a large number of comparators compared to other types of ADCs, which means consuming large area and more power. This drawback makes flash converters typically impractical for resolution greater than 8 bits (255 comparators). Moreover, the large number of comparators connected to input voltage results in a large parasitic capacitance that load the input terminal and limit the speed of the converter and requires a power-hungry buffer at the input terminal [6].

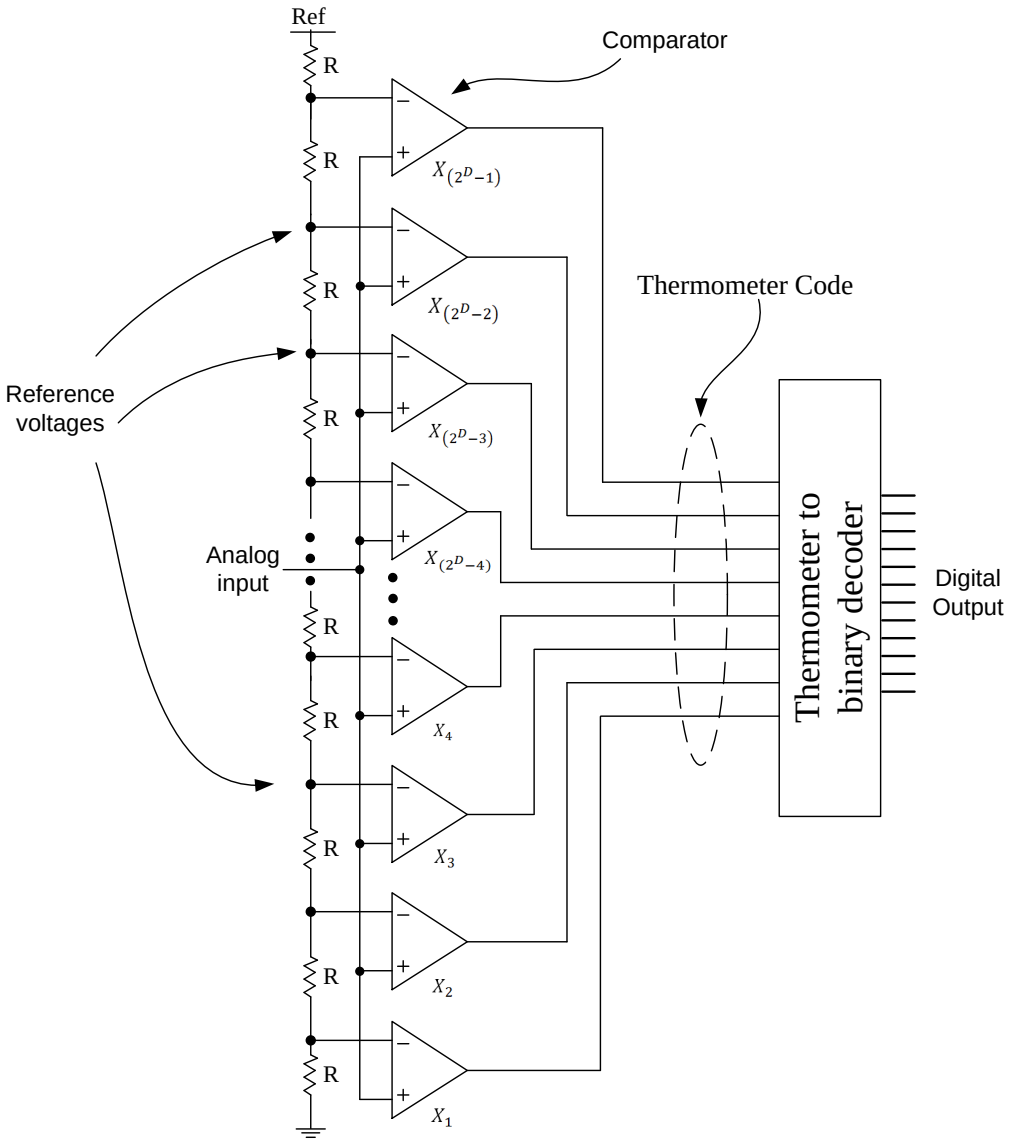

Figure 2.6: Flash ADC

2.5.2 Oversampling direct-conversion ADCs

The oversampling ADC is the ADC type in which the sampling frequency is much higher than the input signal frequency [6]. The oversampling conversion technique have become popular as it avoids many of the difficulties encountered with conventional method for analog-to-digital conversion, such as use of anti-aliasing analog

filters [9].

The basic concept of the sigma-delta modulator is the use of high sampling rate and feedback for improving the effective resolution of the quantizer [9]. Sigma-delta modulator modulates the analog signal into a digital code, usually single-bit code, at a frequency much higher than the Nyquist rate. The use of high frequency modulation and demodulation eliminates the need for sharp cutoffs in the analog anti-aliasing filter at the input of the ADC. One of the most important sigma-delta modulator characteristics is the oversampling ratio (OSR), which is defined as the ratio of the sampling frequency f_s to the Nyquist frequency. Figure 2.7 shows the simplest sigma-delta modulator, the first-order sigma-delta modulator. The input to the circuit feeds to the quantizer via an integrator, and the quantized output is fed back to be subtracted from the input signal [10].

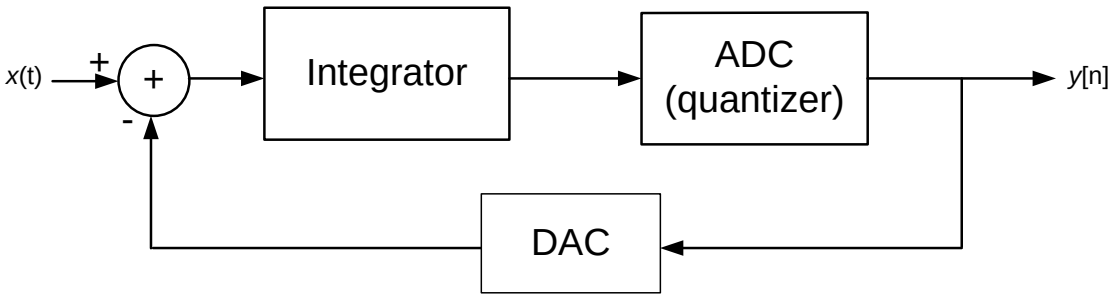

Figure 2.7: First-order sigma-delta modulator

We will analyze the first-order sigma-delta ADC by using the equivalent circuit shown in Figure 2.8. For simplicity, we replace the nonlinear operation of the ADC with a linear one through the addition of signal $e[n]$, which represents the quantization error of the internal quantizer. Moreover, we assume both the ADC and DAC have a gain of unity. As this is a sampled-data circuit, we represent the integration by accumulation, also with unity gain.

We can write the output of the accumulator as

$$w[n] = (x[n] - y[n-1]) + w[n-1] \tag{2.3}$$

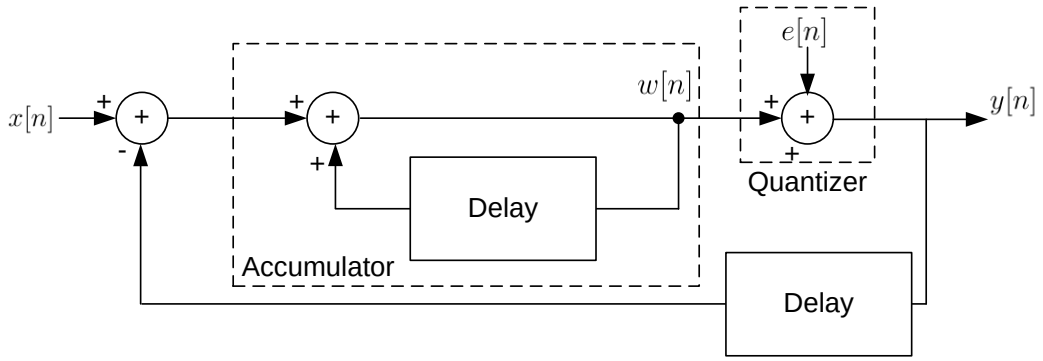

Figure 2.8: First-order sigma-delta modulator equivalent circuit

as $y[n]$ can be written as

$$y[n] = w[n] + e[n] \tag{2.4}$$

Then we can rewrite $w[n]$ as

$$w[n] = x[n] - e[n-1] \tag{2.5}$$

and then we can write $y[n]$ as

$$y[n] = x[n] + (e[n] - e[n-1]) \tag{2.6}$$

As we can see, the system differentiates the quantization error, while leaving the signal unchanged. Assuming the input signal is uncorrelated, the error e behaves as a white noise that is uncorrelated with the signal. $N(f)$, the spectral density of the overall quantization noise, $\epsilon[n]$, calculated as $\epsilon[n] = e[n] - e[n-1]$, can be written as

$$N(f) = E(f)(1 - e^{-jt}) = 2e_{rms}\sqrt{T}\sin(\frac{\omega T}{2}),\ e_{rms}^2 = \frac{\Delta^2}{12} \tag{2.7}$$

where $E(f)$ is the power spectral density of the noise of the internal quantizer, and Δ is its step size.

Figure 2.9 compares between the spectral densities of the noise. As we can see from Figure 2.9, the feedback around the quantizer reduces the noise at low frequencies but increases it at high frequencies. This process is called noise shaping.

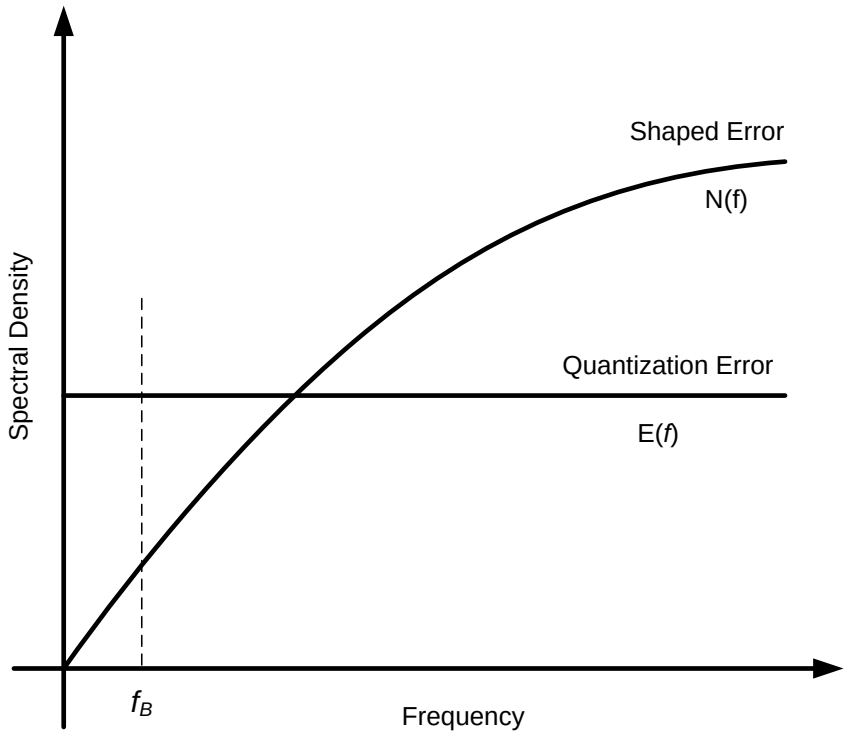

Figure 2.9: The spectral density of $N(f)$ compared with that of $E(f)$

We can calculate, e_{SB}, the total noise power in the signal bandwidth (BW) by integrating the square of the absolute value of $N(f)$ over the signal BW, which gives

$$e_{SB}^2 = \int_0^{f_{BW}} |N(f)|^2 = \frac{\pi^2}{3} e_{rms}^2 \, OSR^{-3}, \; OSR = \frac{f_s}{2f_{BW}} \tag{2.8}$$

and the noise value is then given by

$$e_{SB} = \frac{\pi}{\sqrt{3}} e_{rms} \, OSR^{-3/2} \tag{2.9}$$

From equation (2.9), we can see that doubling the oversampling ratio of this circuit reduces the noise by 9 dB and provides 1.5 bits of extra resolution.

Figure 2.10 shows the second order sigma-delta modulator. As we can see, the differences between the second and the first-order modulator are the existence of another integrator (accumulator), and another feedback path from the output [10].

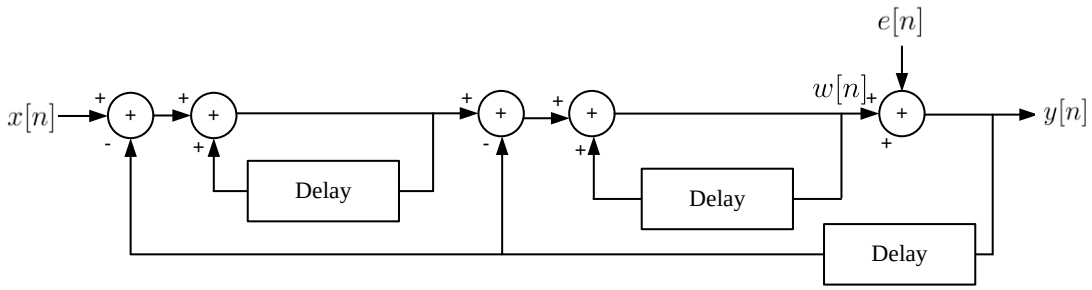

Figure 2.10: The second order sigma-delta modulator

Following the same analysis procedure used with the first-order sigma-delta ADC, the quantizer output can be written in the form

$$y[n] = x[n] + (e[n] - 2e[n-1] + e[n-2]) \tag{2.10}$$

As we can see, the system differentiates the quantization error, but this time making the modulation error the second difference of the quantization error, while leaving the signal unchanged. The spectral density of the modulated noise $\epsilon[n]$ defined as $\epsilon[n] = e[n] - 2e[n-1] + e[n-2]$ can be written as

$$N(f) = E(f)(1 - e^{-jt})^2 = 4e_{rms}\sqrt{T}\sin^2(\frac{\omega T}{2}) \tag{2.11}$$

and the noise rms value is then given by

$$e_{SB} = \frac{\pi^2}{\sqrt{5}} e_{rms}\ OSR^{-5/2} \tag{2.12}$$

From equation (2.12), doubling the OSR results in decreasing the quantization error by 15 dB and providing 2.5 bits of extra resolution. A complete design of second-order sigma-delta modulator is covered in [11].

The technique can be extended to higher order loop ADC by adding more feedback loops to the circuit [10]. In general, when a modulator has L loops, it can be shown that the spectral density of the modulation noise is

$$N(f) = E(f)(1 - e^{-jt})^L = e_{rms}\sqrt{T}\Big(2\sin(\frac{\omega T}{2})\Big)^L \tag{2.13}$$

And the rms noise in the signal band is given by

$$e_{SB} = \frac{\pi^L}{\sqrt{2L+1}} e_{rms}\ OSR^{-(L+\frac{1}{2})} \tag{2.14}$$

From equation (2.14), doubling the OSR results in decreasing the quantization error by $3(2L+1)\ dB$ and providing $(L+1/2)$ extra bits of resolution. The reason behind not using L-order sigma-delta modulator, where L is greater than 2, is the stability of the system [10]. Due to feedback, signal at the input of the quantizer may accumulate. This leads to overloading the modulator, and making the modulator unstable.

2.5.3 Nyquist rate TADCs

TADC is the type of ADC that performs the analog to digital conversion in an indirect manner by first converting the analog input to time representation and then quantizes this time representation into digital code. This means that TADC is a type of indirect conversion ADCs. Dual slope ADC is an example of Nyquist rate TADC.

2.5.3.1 Dual slope ADC

Dual slope ADC, also called integrating converter, is usually used for application that requires high accuracy but low data rate. This type of ADC has very low offset and gain error. It also requires only small amount of circuitry to be implemented [6]. Figure 2.11 shows a simplified diagram of the dual slope ADC.

The ADC name, dual slope, comes from the fact that this type of ADC performs the conversion on two phases. The first phase has a fixed duration T_1 controlled by the running of a counter for 2^D clock cycles. During this phase, the integrator input is connected to the analog input sample and the integrator output starts to ramp up. Thus, we can write the integrator output as

$$V_{out} = -\int_0^t \frac{-V_{in}}{RC}\ dt = \frac{V_{in}t}{RC} \tag{2.15}$$

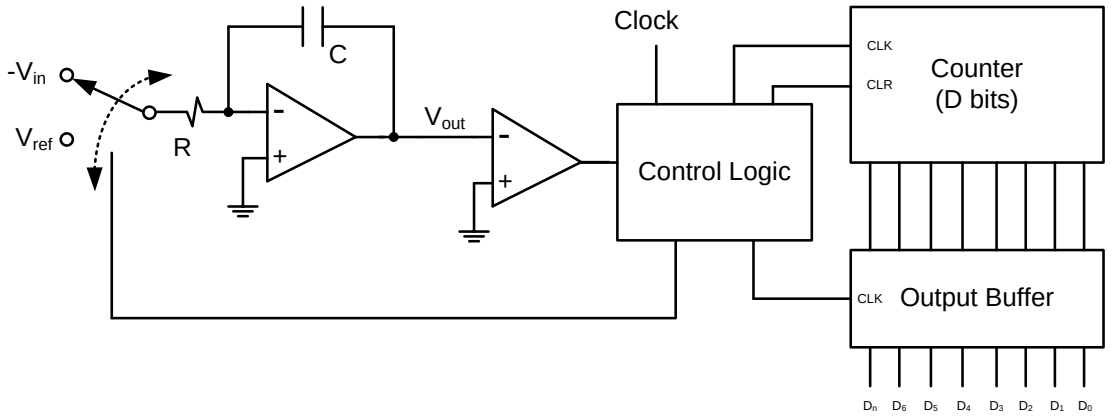

Figure 2.11: The dual slope ADC

At the end of the first phase the integrator output will be given by

$$V_{out} = \frac{V_{in}T_1}{RC} \tag{2.16}$$

In the second phase, the input of the integrator is switched to the reference voltage V_{ref}. This means that the slope is fixed during this phase, unlike the first phase, which has variable slope. This results in a variable duration T_2 for the second phase. The integrator output starts to go down until it reaches zero. Again we can write V_{out} as

$$V_{out} = -\int_{T_1}^{t} \frac{V_{ref}}{RC}\, dt + \frac{V_{in}T_1}{RC} = \frac{-V_{ref}}{RC}(t - T_1) + \frac{V_{in}T_1}{RC} \tag{2.17}$$

To calculate the value of T_2, we equate V_{out} to zero, giving:

$$T_2 = T_1 \frac{V_{in}}{V_{ref}} \tag{2.18}$$

In the beginning of this phase, the counter is first reset and then start to count during the time in which the integrator output is greater than zero. The value of the time constant RC does not affect the digital output, as we can see from equation (2.18). However, this value should be properly chosen such that it does not cause clipping of the integrator output in the first phase [6].

2.5.4 Oversampling TADC

2.5.4.1 Analog-to-time converter

The conversion form the analog domain to the time domain is usually implemented either by using single-input-single-output inverter or by differential pair inverter. The conversion is done by using the analog input signal to control the rate by which the output capacitor, C_L, is charged or discharged. Figure 2.12 shows an example of current starved inverter. The upper two transistors (M2, and M3) are the transistors appearing in a conventional inverter, while M1 is introduced to control the discharging current of C_L.

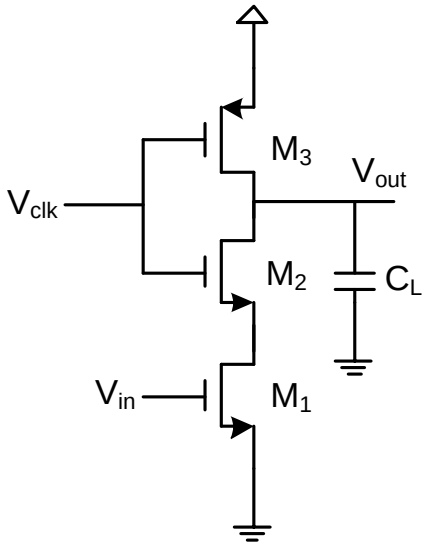

Figure 2.12: Current starved inverter

By controlling the discharging current of C_L, through the varying of the input voltage V_{in}, we control the delay time it takes V_{out} to reach a certain voltage, say the threshold voltage of another inverter driven by V_{out}. The main problem with this delay cell is the nonlinear relationship between the control voltage (V_{in}) and the delay time. This nonlinear relationship introduces distortion. Many publications address the improvement of the linearity of the current starved cell, such as the one reported in [12].

2.5.4.2 Time to Digital converter

The function of the time to digital converter (TDC) is to quantize the time representation of the analog input into a digital code. Figure 2.13 shows one TDC approach [13, 14]. In this TDC, the modulated signal propagates along a line of delay elements. The output node of each delay element is connected to the data input of a D-flip-flop. The state of the delay line is sampled on the rising edge of the reference signal. The position of one/zero transfer in the thermometer code represents the time difference between the modulated and the reference signal. This type of TDC uses only two very simple and small cells, namely, digital delay elements and flip-flops. The resolution is given by the delay of the delay cell.

The resolution of the TDC can be improved by using the Vernier method [14], shown in Figure 2.14. In a Vernier delay line (VDL) two delay buffer chains are used. The delay of the cell in the upper delay chain t_1 is slightly greater than the delay of the cell in the lower delay chain t_2. As the modulated and reference signals propagate in their delay chains, the time difference between the two pulses decreases in each Vernier stage by $t_\Delta = t_1 - t_2$. The position in the delay line, at which the reference signal catches up with the modulated signal, gives information about the measured time, with a resolution t_Δ.

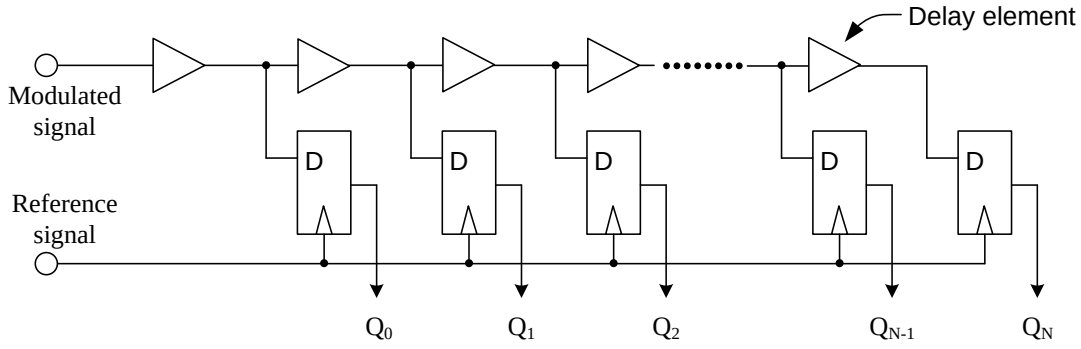

Figure 2.13: An example TDC

2.5.4.3 Analog-to-frequency/period converter

The function of the analog-to-frequency converter (AFC) and analog-to-period converter (APC) is to manipulate the frequency and the period, respectively, of the

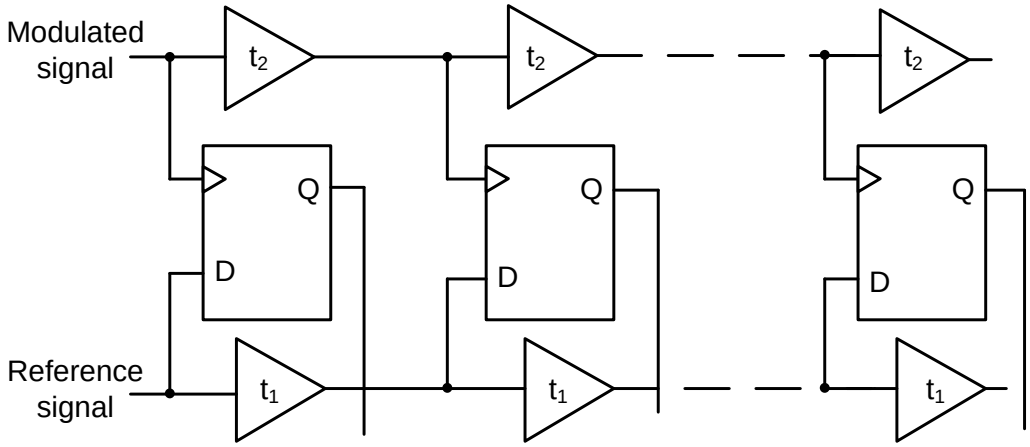

Figure 2.14: Vernier delay line

output waveform according to the value of the analog input. For example, ring oscillator based voltage controlled oscillator (VCO) [10] is an AFC/APC.

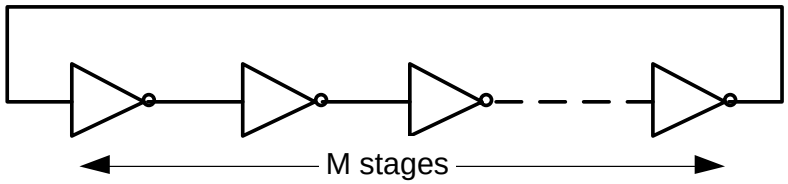

Figure 2.15: Simplified diagram of VCO

As we can see from Figure 2.15, a ring oscillator generally consists of a chain of delay cells connected in series, and a ring is formed by connecting the output of the last stage to the input of the first stage. The delay cell can be implemented either by using a single-input-single-output inverter or by using a differential pair inverter. In case of single-input-single-output inverters, the number of delay cells (M) must be an odd number. In case of differential-pair-inverters, the number of stages can be either odd or even, but if we use an even number of stages the output of the one of the the stages must be swapped before connecting to the input of the next stage [15]. To understand how the ring works, assume that we have an odd number of single-input-single-output inverters and the output of the first stage is one. As the output of the first stage is the input of the second stage, this results in making the output of the second stage to be zero , the same procedure continue in

all the ring stages until we reach the last stage whose output is one. The output of the last stage forces the output of the first stage to switch to zero and this output starts to propagate in the ring until the output of the first stage is forced again to be one and so on. As we can see, it takes two cycles through the ring to complete one period, as shown in Figure 2.16. Thus, we can write the relation between the period of oscillation T and the delay of one delay cell t_d as

$$T = 2Mt_d \tag{2.19}$$

and so we can write the frequency of the VCO output as

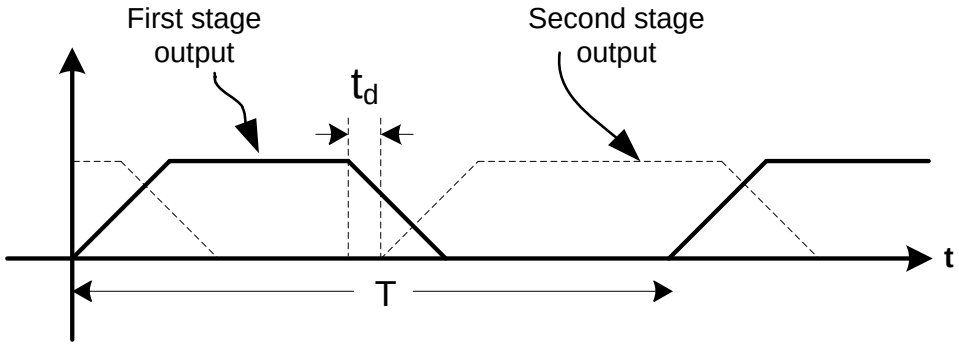

Figure 2.16: Example of VCO output signal

$$f = \frac{1}{T} = \frac{1}{2Mt_d} \tag{2.20}$$

As we can see from the above equation, besides the condition on the number of the stages M, the value of M is determined from the required output frequency and the value of t_d. Controlling the value of t_d, through the change of the input voltage V_{in}, will enable us to control the value of F. We define the tuning parameter K_{VCO} as the ratio of the change in the output frequency to the change in the input voltage [10]

$$K_{VCO} = \frac{d\omega}{dV_{in}} = 2\pi\frac{dF}{dV_{in}} \tag{2.21}$$

As an example, for the VCO built by single-input-single-output inverter we can write K_{VCO} as

$$K_{VCO} = \frac{2\pi G_m}{2MCV_{swing}} \tag{2.22}$$

where $G_m = dI_{tune}/dV_{in}$, I_{tune} is the inverter current, and V_{swing} is the voltage swing.

Many work and publications, such as those reported in [16, 17], address the design of VCOs that are suitable for various types of applications.

2.5.4.4 Period to digital converter

The primary objective of the period-to-digital converter (PDC) is to convert the period of a modulated signal, T_{in}, into a digital code. To do this, the PDC counts and quantizes the number of rising edges of the period modulated signal during the sampling interval T_{ref}.

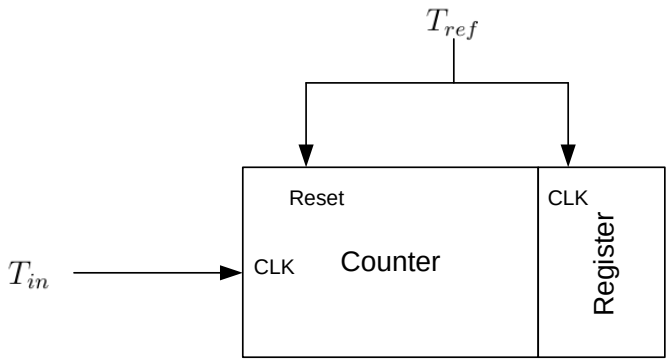

Figure 2.17: One simple PDC

One simple PDC may be implemented as a count and dump converter [17], as shown in Figure 2.17. The drawback of this type of PDC is the counter resetting operation, which is a limiting factor for high-speed operation.

The counter does not need to be reset every T_{ref}, if the count and dump circuit is considered as an ideal counter with no upper limit followed by a digital differentiator. The ideal counter may be realized as a modulo 2^n counter, as shown in Figure 2.18, on the condition that the maximum number of received rising edges during T_{ref} is smaller than the module of the counter to avoid signal aliasing [17]. The differentiation is done by subtracting two consecutive readings of the counter.

If the maximum received number of edges during T_{ref} is smaller than two, we may use modulo 2^1 arithmetic (D-flip-flop), and the subtraction operation can be

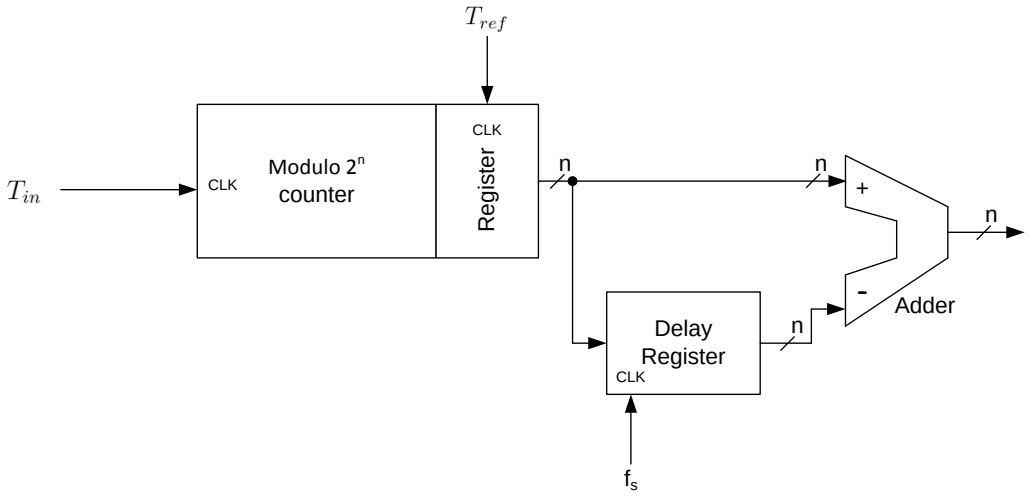

Figure 2.18: Modulo 2^n implementation of the FDC

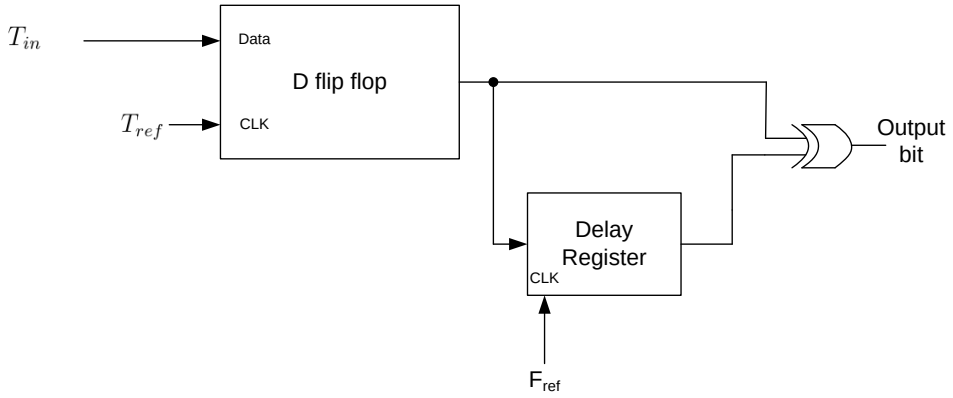

Figure 2.19: Modulo 2^1 implementation of the FDC

implemented using an XOR gate [17], as shown in Figure 2.19. The only problem with decreasing module size of the counter is that we need very high sampling frequency equal to the free running frequency of the VCO.

Time-based sigma-delta modulator [12, 18–25]can also be used to act as PDC. This is the focus of this thesis and we will discuss it in details in Chapter 3.

Chapter 3

TIME-BASED ΣΔ ANALOG-TO-DIGITAL CONVERTER

In this chapter, four different implementations of TADC are presented. The four implementations consist of an APC followed by a PDC. The PDC is a time-based ΣΔ modulator. The idea of dispensing with the explicit sample-and-hold circuit is also discussed in this chapter.

3.1 First-order ΣΔ modulator in time domain

Time version of amplitude-based ΣΔ modulator has been presented and discussed in literature such as [26–28]. In this work we are proposing new ΣΔ-based TADCs. To elaborate on the new idea, let's start with Figure 3.1 which shows the block diagram of a simple system that will be used to demonstrate how the time-based ΣΔ action is implemented. As we can see in Figure 3.1, the system contains two VCO's. The first VCO, denoted as the input VCO, converts the analog voltage input into phase input, T_{in}, by varying its period according to the value of the analog voltage. The second VCO, denoted as the reference VCO, generates a reference phase/period, T_{ref}. The multiplexer (MUX) generates a shifted version of the phase input signal, where the amount of shift is governed by the ΣΔ output, D_{out}, through the ΣΔ

feedback action. The MUX allows the phase input to pass to the D flip flop (D-FF), when the MUX select signal is "0"; or delay it by $t_{unit\ delay}$ before feeding it to the D-FF, when the MUX select signal is "1". The D-FF acts as a quantizer. It compares MUX_{out} with the reference phase, digitizes it, and generates the ΣΔ output.

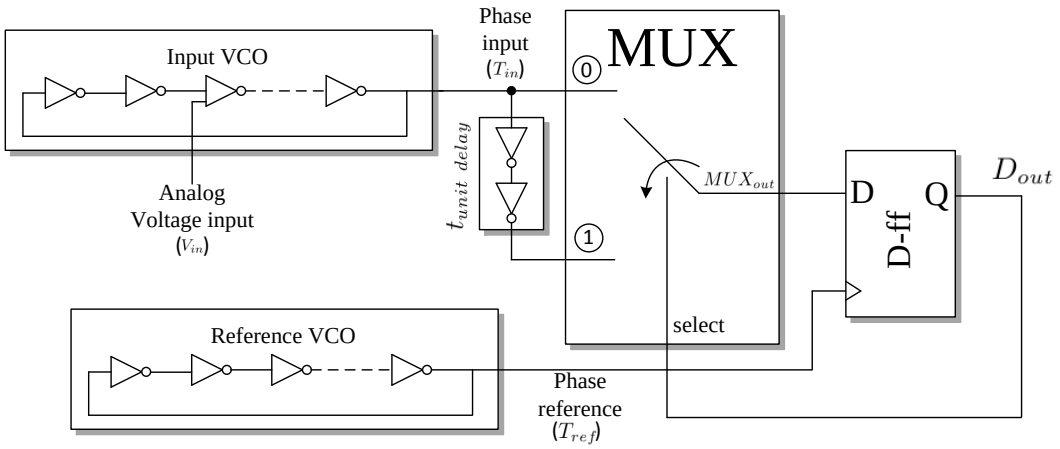

Figure 3.1: Time version of the first order ΣΔ modulator

Figure 3.2 illustrates the waveform of the case when the analog voltage is at $V_{ref}/2$. This sets the period of the analog VCO to be equal to that of the reference VCO. Assume that the digital output is initially "0". This results in making the MUX copies from the the input labeled by "0", the output of the input VCO. Compared to the first edge of the reference signal, the phase of the MUX output signal leads the phase of the reference signal. This results in making the digital output of the D-FF goes to "1". Because the digital output changes, the MUX starts copying from the input labeled by "1", the delayed version of the output of the input VCO. Compared to the second edge of the reference signal, the phase of the MUX output signal lags the phase of the reference signal. This results in making the digital output of the D-FF goes back to "0" and so on.

We can model the system, shown in Figure 3.1, mathematically, by writing the time domain equation that governs the variable $\tau(k)$, in Figure 3.2. $\tau(k)$ represents the phase/time difference between MUX_{out} and reference phase, and k is the time index. $\tau(k)$ is considered positive when the reference phase leads the MUX output

and it is considered negative when the MUX output leads the reference phase. The time equation of $\tau(k)$ can be written as

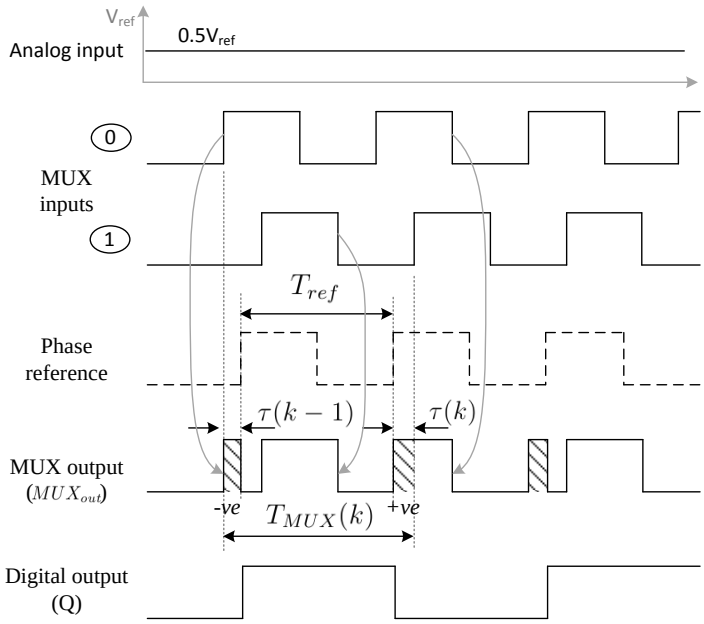

Figure 3.2: Waveform representation of Fig. 3.1 when $V_{in} = V_{ref}/2$

$$\tau(k) + T_{ref} = \tau(k-1) + T_{MUX}(k) \tag{3.1}$$

where $T_{MUX}(k)$ is defined as

$$T_{MUX}(k) = T_{VCO}(k) - Sgn(\tau(k-1)) \times t_{unit\ delay} \tag{3.2}$$

here $T_{VCO}(k)(= T_{ref} + T_{in}(k))$, is the period of the input VCO, and $T_{in}(k)$ is the variation of the input VCO period, from T_{ref}, that corresponds to the value of the analog input voltage. $T_{in}(k)$ is equal to zero in the example shown in Figure 3.2. $Sgn()$ is the sign function. Substitute equation (3.2) into equation (3.1), $\tau(k)$ can be written as

$$\tau(k) = \tau(k-1) + T_{in}(k) - Sgn(\tau(k-1)) \times t_{unit\ delay} \tag{3.3}$$

Figure 3.3 shows the block diagram representation of equation (3.3). As we

can see, it represents a time version of amplitude-based first-order single-bit ΣΔ modulator.

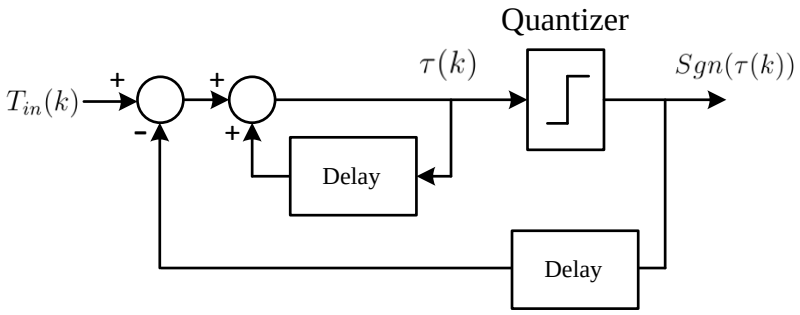

Figure 3.3: Block diagram representation of equation (3.3)

The system in Figure 3.1 works fine only in the case when the analog input is equal to $V_{ref}/2$ (period of the input VCO is equal to the reference period). In other words, when the digital output is toggling equally between "0" and "1". This is because the system can advance or delay the phase of the phase input signal, through the MUX and the unit delay, only one time. However, if the analog input voltage is changed such that sequences of consecutive "0's" or "1's" is generated, the phase of the phase input signal will need to be delayed/advanced more than one time. The single delay element, shown in Figure 3.1, will not be enough to do this. Theoretically speaking, to be able to delay/advance the phase of the phase input signal for any arbitrary sequence of "0's" or "1's", a chain of infinite delay elements is needed, but this solution is not practical.

The key feature in the system shown in Figure 3.1 is the ability of changing the period of the D-FF input according to the previous output of the D-FF. The period is increased, by $t_{unit\ delay}$, if the D-FF output is "1" and it is decreased if the D-FF output is "0". To overcome the problem of requiring a chain of infinite delay elements, [27] has proposed the usage of dual modulus divider (DMD). The dividing ratio of the DMD is controlled by the output of the D-FF. In this work, three other different techniques will be proposed to overcome this problem.

3.2 Implicit sample and hold in the VCO

In this section, the usage of the implicit sample and hold (S/H) in the input VCO, instead of using an explicit S/H, will be discussed. This has the advantage of saving area and reducing complexity. Also, the effects of the non-idealities that accompany the usage of the implicit S/H have on the system performance will be investigated.

3.2.1 The VCO implicit sample and hold operation

In this subsection, the implicit S/H mechanism happening in the input VCO will be explained. Figure 3.4 shows the input VCO. It is a typical 2-transistor inverter-based ring oscillator, except that one of its stages, the sampler, has an extra transistor that samples the input. It acts like a current starved inverter.

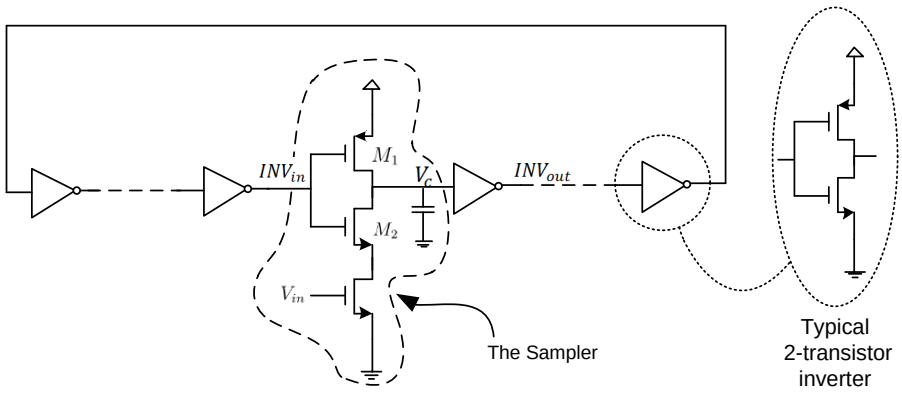

Figure 3.4: The input VCO

As shown in Figure 3.5, at the rising edge of INV_{in} (the gate voltage of M_1, and M_2), V_C (the voltage on the parasitic capacitor at the drain of M_1, and M_2) starts to fall down, at a rate determined by the analog input voltage, V_{in}. To illustrate the operation, let us consider the situation when V_{in} is a low frequency signal, so that it varies slowly. As the input signal frequency is small, we can consider it constant during the discharging operation of the capacitor, and so V_C will discharge linearly with time, as shown in the zoomed in area of Figure 3.5.

When V_C crosses the threshold of the next inverter, V_{th} at $t_{V_{in}}$, the inverter output (INV_{out}) will switch to V_{dd}. After this point, any further change in V_{in} will

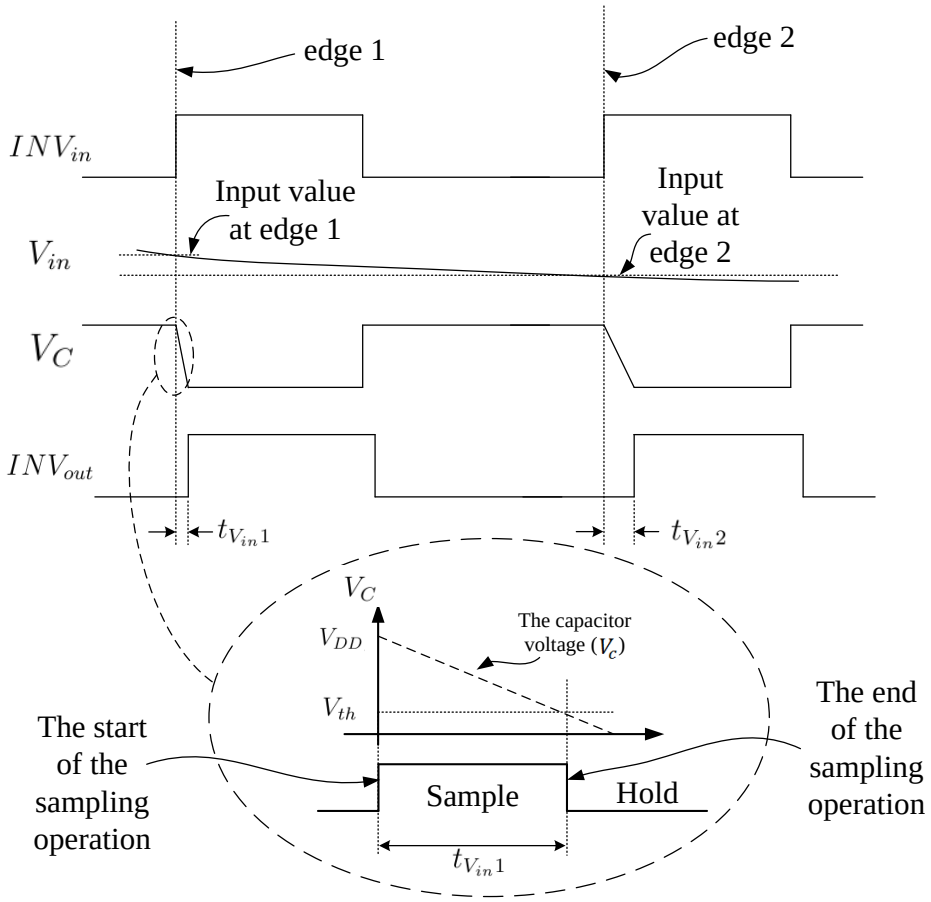

Figure 3.5: The inherent sample and hold

not have any effect on $t_{V_{in}}$ and so $t_{V_{in}1}$ is sampled. On the next rising edge of the INV_{in}, V_C will again fall down but this time with different slope that depends on the new value of V_{in}. A new $t_{V_{in}}$ ($t_{V_{in}2}$) results, which corresponds to the new value of V_{in}. Thus, as shown in the lowest trace (the zoom in circle) of Figure 3.5, the sample and hold operation is done inherently. The sampling window starts at the rising edge of INV_{in} and ends when V_C crosses V_{th} of the next inverter. Then the hold operation starts from this point and lasts until the next rising edge of INV_{in}.

The usage of the inherent S/H to sample input signal saves area and eliminates the non-idealites that accompany the explicit S/H, like charge injection and clock feed through. However, the usage of the inherent S/H introduces some nonidealites to the system. Examples of these nonidealites are the tracking error and the non

uniform sampling. These nonidealites will be investigated in the next subsections.

3.2.2 Tracking error

In real life, V_{in} is not varying slowly and so cannot be considered constant during the capacitor discharging operation. If V_{in} is assumed to vary linearly during this operation and if the relation between the capacitor discharging current and V_{in} is assumed to be linear, then V_c falls down quadraticlly, as shown in Figure 3.6 (solid line). Thus, V_c crosses V_{th} at a time that is different than the case when an explicit S/H is used. There V_{in} is the sampled (explicitly) input, and is constant while V_c is falling (dotted line in Figure 3.6). If V_{in} is increasing with time, this means that

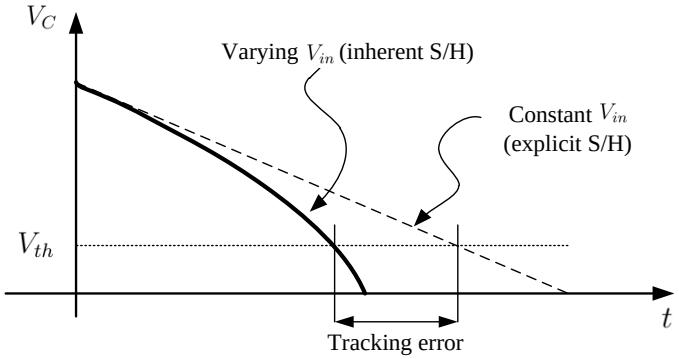

Figure 3.6: Definition of tracking error

the current increases, and so the output voltage will cross the threshold earlier than the explicit S/H case. However, if V_{in} is decreasing with time, the output voltage will cross the threshold latter than the explicit S/H case.

The difference between the two times (for implicit S/H and for constant V_{in}) is called the tracking error, t_{error}. This reflects that the implicit S/H is trying to track the varying V_{in} by adjusting the threshold crossing times. To be able to use an inherent S/H, this error has to be less than the time corresponding to 1 LSB change in the V_{in}, t_{1LSB}. This t_{1LSB} is calculated for 2 values of V_{in}. In each value; V_{in} is assumed to be explicitly sampled and hence constant in the sampling window. This is shown in Figure 3.7. Note that because V_{in} is constant, the two dotted line

have constant, but different, slopes. This is because V_{in} increases by V_{1LSB}, where V_{1LSB} is the voltage corresponding to 1 LSB.

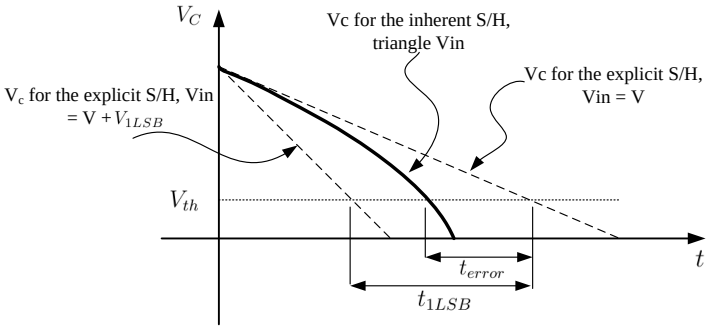

Figure 3.7: The relation between t_{error} and t_{1LSB}

The tracking error sets a condition on the maximum frequency of the input signal to the VCO. For a triangle wave input, we can derive the maximum allowed frequency, F_{max} (see Appendix A.3) as

$$F_{max} = k_f \frac{V_{1LSB}(V_{start} + V_{1LSB})}{A(V_{dd} - V_{th})} \tag{3.4}$$

where k_f is a constant depending on the design of the inherent S/H and V_{start} is the value of V_{in} when the capacitor starts discharging. V_{start} depends on the relative phase between V_{in} and INV_{in}. To get a bound on F_{max}, $F_{(max-bound)}$, which is true for all relative phases, we should set V_{start} to be the worst case, which happens when V_{start} is at the minimum, i.e., $V_{(shift-triangle)}$ in Figure 3.8.

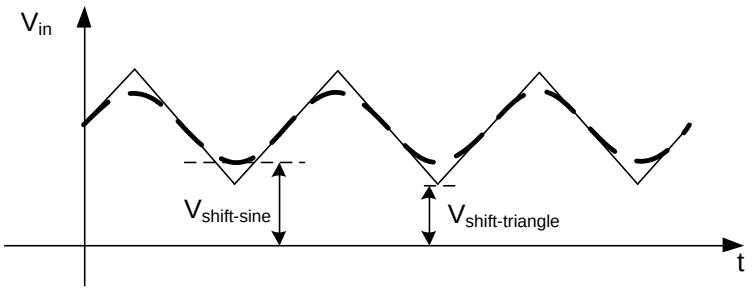

Figure 3.8: The relation between the triangle and sinusoidal V_{in}

$$F_{max} = k_f \frac{V_{1LSB}(V_{(shift-triangle)} + V_{1LSB})}{A(V_{dd} - V_{th})} \tag{3.5}$$

Now let us investigate the case when V_{in} is a sinusoidal wave. To find a bound on F_{max} let us assume that the frequency of the sine wave is equal to the frequency of the triangle wave, as shown in Figure 3.8. Since the triangle wave has a slope greater than or equal to the slope of the sine wave, $F_{(max-bound)}$, derived from the triangle wave (equation (A-23)) provides a bound on $F_{(max-bound)}$, using a sine wave.

3.2.3 Non-uniform sampling

The non-uniform sampling (NUS) [29] can lead to distortion/non-linearity due to the fact that the reconstruction of the signal is done using a periodic clock. Figure 3.9 shows an example of a linearly ramping signal that is sampled non-uniformly. When the samples are used to reconstruct the signal using a periodic clock, the reconstructed signal is no longer ramping up linearly.

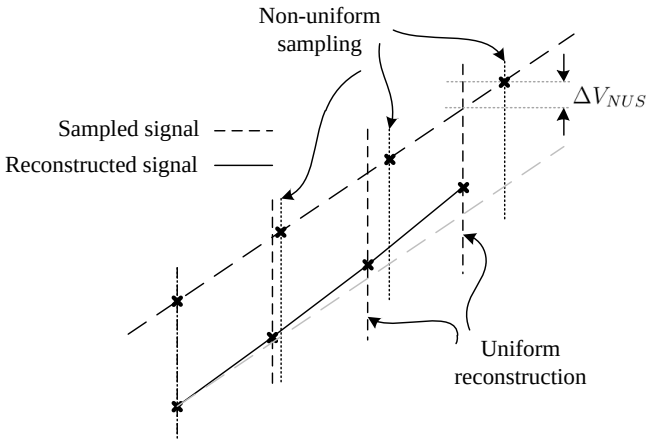

Figure 3.9: Non-linearity due to non-uniform sampling followed by uniform reconstruction

From the ADC design point of view, if the difference ΔV_{NUS}, between the non-uniform sampled voltage and the uniformed sampled counterpart, as shown in Figure 3.9, is less than the resolution of the ADC, the NUS distortion is acceptable. Thus, our design requirement is that

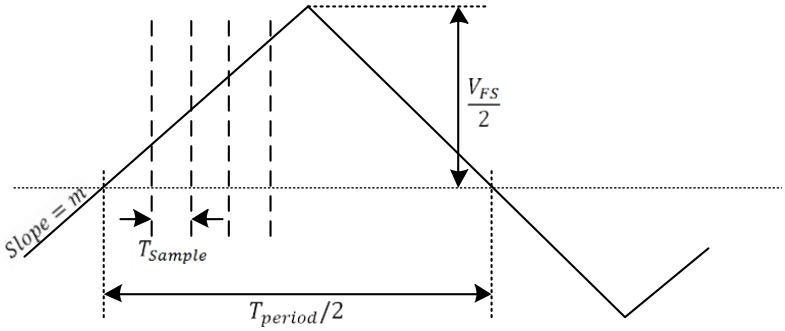

Figure 3.10: An example of a triangle wave

$$\Delta V_{NUS} \leq \frac{V_{FS}}{2^D} \tag{3.6}$$

For a ramp signal with slope m, as shown in Figure 3.10, we can express ΔV_{NUS} in terms of the deviation in the sampling period ΔT as

$$\Delta V_{NUS} = m \times \Delta T \tag{3.7}$$

From Figure 3.10, we can express m in terms of V_{FS} and T_{period} as

$$m = \frac{2V_{FS}}{T_{period}} \tag{3.8}$$

where T_{period} is the period of the input signal. By substituting in equation (3.7), we can write

$$\Delta T \leq \frac{T_{period}}{2^{D+1}} \tag{3.9}$$

Equation (3.9) sets the maximum time difference between the uniform and the non-uniform sampling edges.

3.3 The non-linear internal quantizer

The internal quantizer of a ΣΔ modulator can be either single-bit or multi-bit. A 1-bit quantizer is inherently linear since it has just two quantization levels. However in the case of multi-bit quantizers, the mismatch between quantization steps causes the quantizer to become non-linear.

If the APC input/output relation is linear, the ΣΔ TDC internal quantizer characteristic curve must also be linear to achieve a linear TADC input/output relationship. However, in the case when the VCO is used as APC, the APC output, T_{in} in Figure 3.1, is not linearly related to the analog input voltage. This non-linearity arises due to the non-linear relation between t_{delay} and V_{in} (which arises from charging/discharging of C; for simplicity, here, I is further assumed to be linearly related to V_{in})

$$t_{delay} = \frac{C\ V_{swing}}{I} = \frac{C\ V_{swing}}{KV_{in}} \tag{3.10}$$

Thus, making the quantizer linear will result in non-linear relation between the input and the output of the TADC and this will result in distortion.

The linearity of the TADC can be improved by using a multi-bit non-linear internal quantizer. In the multi-bit non-linear internal quantizer, the quantizer characteristic curve is divided into segments with non-equal pedestals, as shown in Figure 3.11(b). The segments are constructed such that the lines that connect the mid-points of each segment form a piecewise linear representation of the non-linear curve that governs the conversion between the voltage and the time in the VCO in (3.10). The integral non-linearity (INL), see Appendix A.1, is the key non-linearity

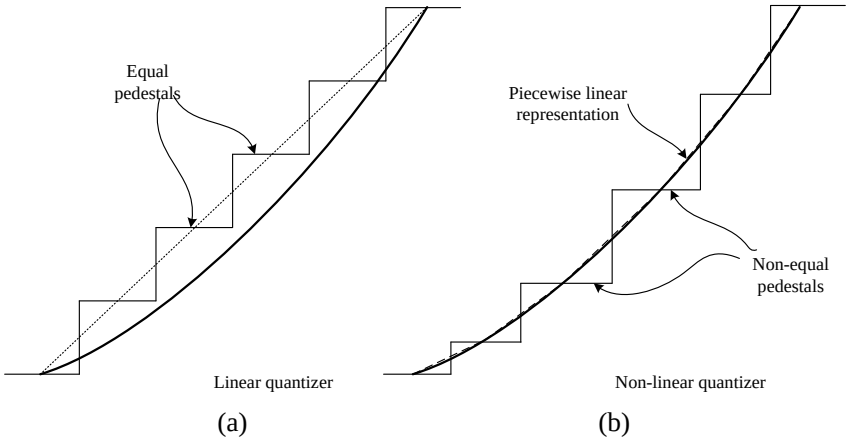

Figure 3.11: An example of non-linear quantizer

in this TADC because the characteristic curve is practically monotonic. The main goal of the non-linear quantizer technique is to make the INL of the quantizer

segments less than or equal to the limit set by the resolution. This is done by the proper choice of the number of the segments and the size of each segment. Figure 3.12 illustrates the improvement of the INL in the case of the multi-bit non-linear quantizer compared to the case of linear quantizer.

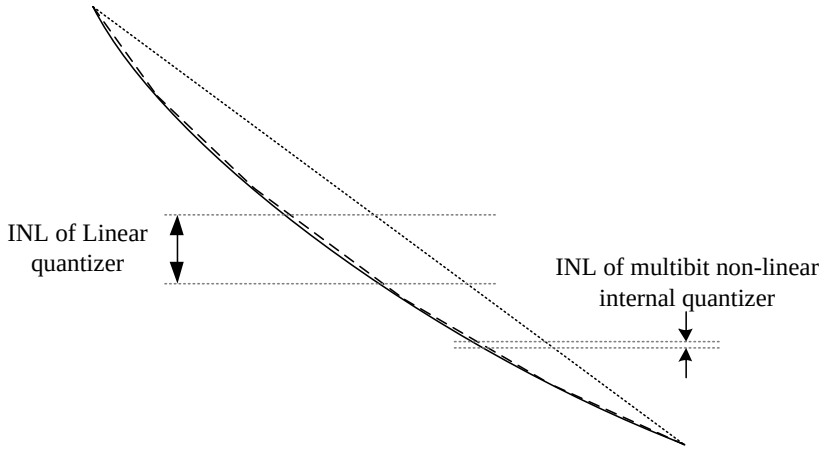

Figure 3.12: Improving the linearity of the TADC by using non-linear quantizer technique

3.4 Preliminary design: varying the reference clock

In Section 3.1, we conclude that the ΣΔ action in time domain can be implemented by adjusting the relative phase, between the phase input signal and the reference phase, according to the output of the ΣΔ modulator. Instead of controlling the relative phase by adjusting the phase of the input phase signal, the phase difference can be controlled by adjusting the phase of the reference signal, by noticing that the T_{ref} is generated from a ring structure that consists of identical delay cells, as shown in Figure 3.13. The ring structure can be considered as an infinite chain of delay cells which can manipulate the phase of its output signal. The manipulation is done by connecting all the reference VCO internal nodes to the input of a multiplexer (MUX). The selection signal of the MUX selects which node of the reference VCO to be connected to the output of the MUX. For example, let us assume that the

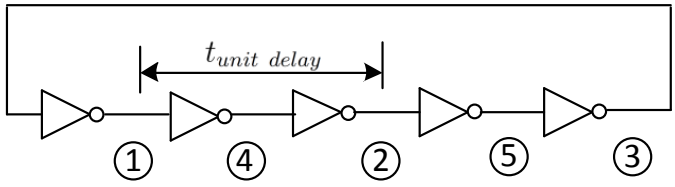

Figure 3.13: Reference VCO structure

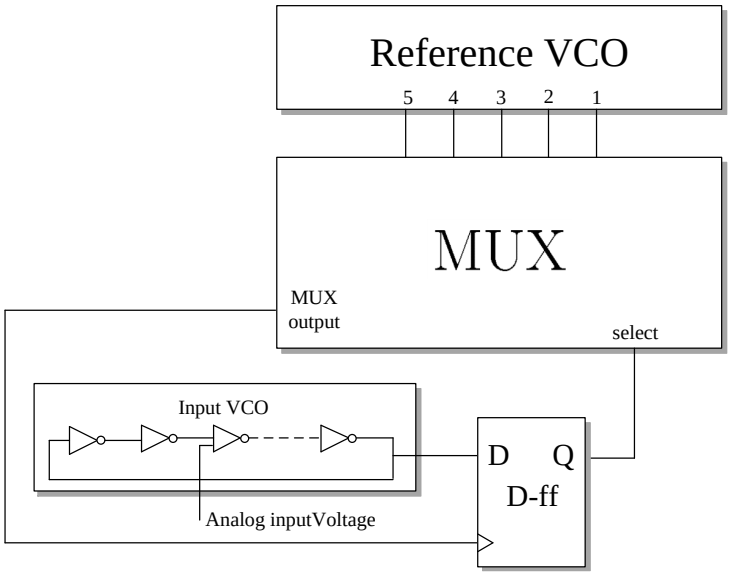

Figure 3.14: Preliminary design block diagram

MUX output is initially connected to the input coming from node 1, in Figure 3.13, of the reference VCO and a rising edge has been generated from the MUX output. If the MUX selection signal is then changed such that the MUX output is connected to node 2 of the reference VCO, the period of the MUX output will equal to the period of the reference VCO + $t_{unit\ delay}$ (assuming that the delay of two consecutive inverters is $t_{unit\ delay}$). On the other hand, if the MUX selection signal is changed such that the MUX output is connected to node 5 of the reference VCO, the period of the MUX output will equal to the period of the reference VCO - $t_{unit\ delay}$.

Figure 3.14 shows the proposed TADC. The select input of the MUX is con-

nected to the output of the D-FF to form the feedback action of the ΣΔ. Figure 3.15 illustrate an example of the system waveform in the case when the two VCO's have the same period. Here, $\tau(k)$ is considered positive if the phase of the input phase signal leads that of the MUX output signal. From Figure 3.15, we can write the time equation of $\tau(k)$ as

$$\tau(k) + T_{VCO}(k) = \tau(k-1) + T_{MUX}(k) \tag{3.11}$$

where $T_{MUX}(k)$ here is equal to $T_{ref} - Sgn(\tau(k-1))$, and T_{VCO} is the input VCO period. Then $\tau(k)$ can be written as

$$\tau(k) = \tau(k-1) - T_{in}(k) - Sgn(\tau(k-1)) \tag{3.12}$$

equation (3.12) again represents a phase version of the amplitude based first order single bit ΣΔ modulator.

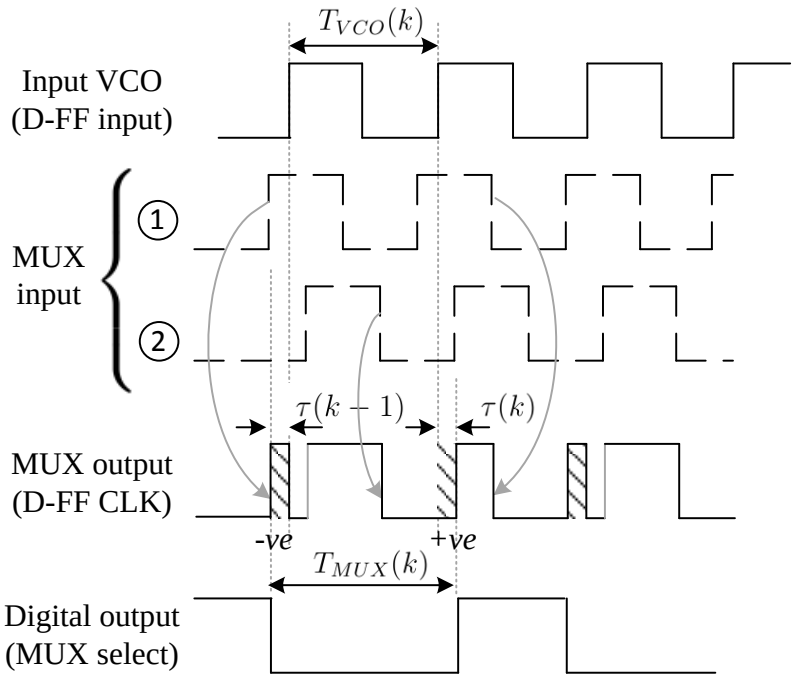

Figure 3.15: Waveform example of the preliminary design

Figure 3.16 shows the Fast Fourier Transform (FFT) of the digital output of the

system with input of 1 MHz and f_{ref} of 100 MHz. As we can see the FFT shows a noise shaping of a first order ΣΔ modulator (it rises with 20dB/decade).

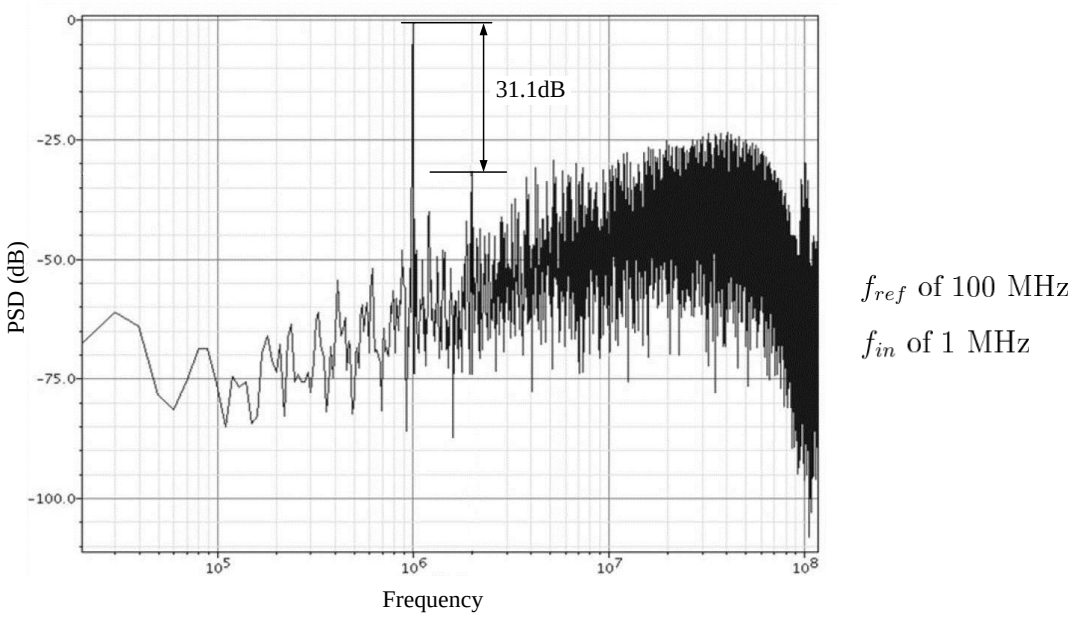

Figure 3.16: FFT of the digital output

Figure 3.16 shows that the distortion is about 31.1dB. This distortion arises from the fact that the weights of the symbol "1" and "0" are different. To elaborate this fact, let's assume that $t_{unit\ delay}$ is equal to $T_{ref}/4$. This will result in making the duration of symbol "1" equal to $(3T_{ref})/4$ and the duration of symbol "0" equal to $(5T_{ref})/4$. This results in making the output "010101010...", for example, average to 3/8 instead of 0.5. Thus, the characteristic curve of the new system will not be linear.

One way to improve the linearity of the proposed system is by modifying the feedback values to be 0 and $t_{unit\ delay}$ (which correspond to 0 and V_{ref} in amplitude based ΣΔ modulator) instead of $-t_{unit\ delay}$ and $t_{unit\ delay}$ (which correspond to $-V_{ref}$ and V_{ref} in amplitude based ΣΔ modulator). This can be done by delaying the MUX output edge, by selecting a node that is lagging by $t_{unit\ delay}$, if the digital output is "1", and keep selecting the same node if the digital output is "0".

The linearity can be improved even more by decreasing the ratio $t_{unit\ delay}/T_{ref}$. The goal is to make the difference between the average of the generated digital

output and the required average less than or equal to the required resolution, $1/2^D$.

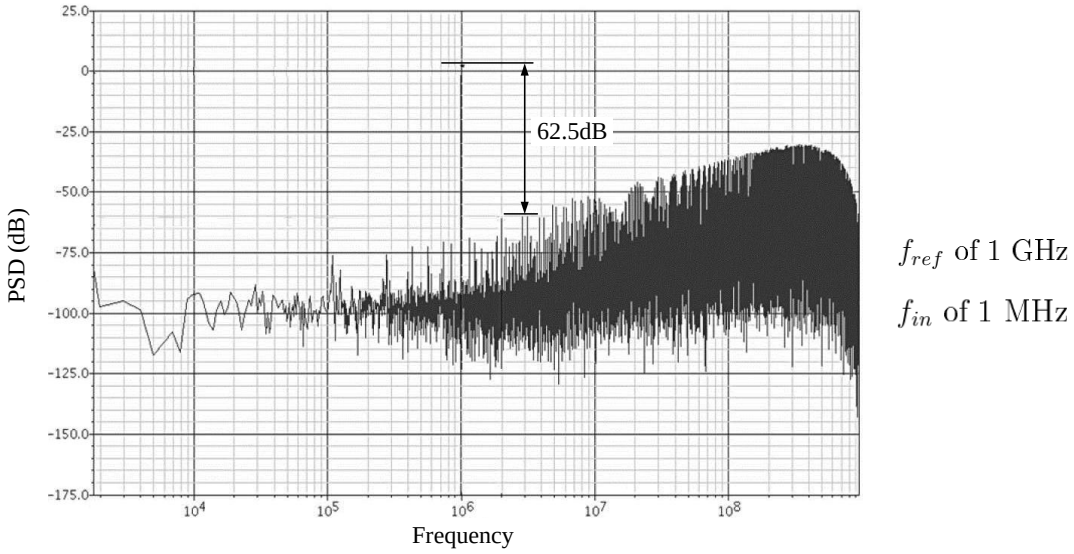

Figure 3.17: FFT of the digital output for the improved system

Figure 3.17 shows the FFT of the improved system after applying the above two improvements. In this system we set $t_{unit\ delay}/T_{ref}$ to be 0.001. As we can see, the distortion goes down to 62.5 dB compared to 31.1 dB in Figure 3.16.

Lower the $t_{unit\ delay}/T_{ref}$ ratio means that the proposed TADC is limited for low frequency applications. This is because T_{ref} needs to be large, which results in reducing the sampling frequency. Because the OSR is set by the required resolution, the frequency of the TADC input signal must be reduced.

3.5 Design I: First-order ΣΔ modulator, phase interpolation incorporated

Another way to overcome the need of having a chain of infinite delay cells in the TADC is to modify the input VCO structure.

3.5.1 New structure for the input VCO

In this new design, instead of modifying the period of the input phase signal after being generated from the input VCO, using a chain of delay cells and a MUX, the structure of the input VCO is modified such that the period of the input VCO is directly controlled by the output of the TADC.

Figure 3.18 shows the new structure of the input VCO. As we can see in Figure 3.18, the VCO's ring is modified and a delay chain/MUX is inserted. Specifically, the chain of delay cells, whose output is connected to a MUX, is inserted in between. The ring is closed again by connecting the output of the inverter at the left hand side of the broken VCO ring to the delay chain input and subsequently connecting the MUX output back to the input of the inverter at the right hand side of the broken VCO ring. The selection input of the MUX is controlled by the output of the ΣΔ modulator.

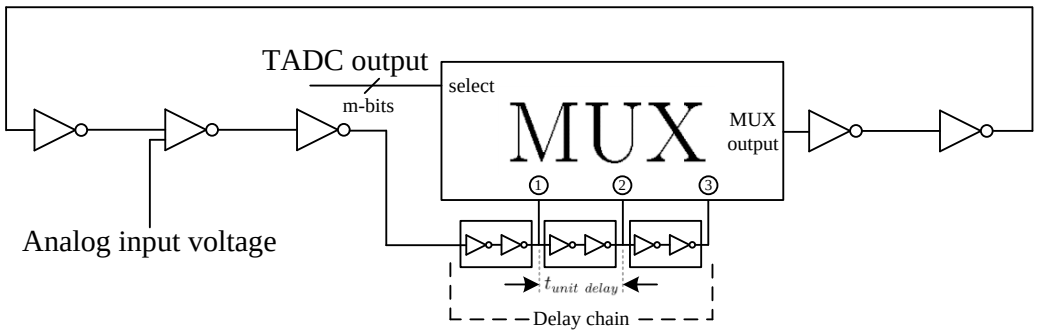

Figure 3.18: The new structure for the input VCO

To elaborate on how the new VCO is working, let us assume that the analog input voltage is set constant, and the MUX selection signal is initially set so the MUX output selects from node 2 of the delay chain. Furthermore, let's assume that the period of the input VCO in this case is the nominal period, $T_{VCO_{nominal}}$. If the selection of the MUX is changed such that the MUX output starts to select from node 3 of the delay chain, the new period of the input VCO will be equal to $T_{VCO_{nominal}} + t_{unit\ delay}$. However, if the selection of the MUX is changed such that the MUX outout starts to select from node 1 of the delay chain, the new period of the input VCO will be equal to $T_{VCO_{nominal}} - t_{unit\ delay}$.

By using this new architecture of the VCO, in building the ΣΔ TADC shown

in Figure 3.1, if the output of the TADC is a sequence of "1's", the MUX selection signal needs to be set such that the MUX output keeps selecting from node 3 of the delay chain. If the output of the TADC is a sequence of "0's", the MUX selection signal needs to be set such that the MUX output keeps selecting from node 2 of the delay chain. Compared to Figure 3.1, there is no need to increase the number of the delay units inside the delay chain.

For proper operation of the proposed TADC, the MUX output, in the VCO, must copy the falling edge from the same delay chain node regardless of the output of the TADC. In other words, the TADC output controls only the rising edge of the MUX output. This is because the MUX inputs are generated from the VCO itself. In other words, the phase of the MUX input signal depends on the phase of the falling edge of the MUX output. Thus, for proper operation of the TADC, the falling edge of the MUX output must be fixed and should not depend on the TADC feedback.

Figure 3.19 illustrates a set of representative waveforms for the VCO shown in Figure 3.18. For simplicity, the MUX in Figure 3.19 has only two inputs and the MUX selection input is just one bit. The analog input voltage is assumed to be constant and the D-FF output is assumed to be toggling between "1" and "0". As we can see from figure Figure 3.19, the period of the VCO is controlled by the D-FF output. When the D-FF output is "1", the period of the VCO increases, compared to the case when the D-FF output is "0", by a time duration equals to the delay of one delay unit.

To incorporate the non-linear multibit internal quantizer technique in the new architecture of the VCO, phase interpolation is used.

3.5.2 Phase interpolation

Phase interpolation (PI) technique is generally used to increase phase resolution of the system without increasing the speed of the system [30,31] or to push the phase resolution beyond the limit dictated by the inverter delay in a given technology.

Figure 3.20 shows the phase interpolator. For proper operation, Φ_A and Φ_B must have the same period of oscillation and derived from the same source. The location of the edge Φ_b between Φ_a and Φ_c is determined by the relative size ratio

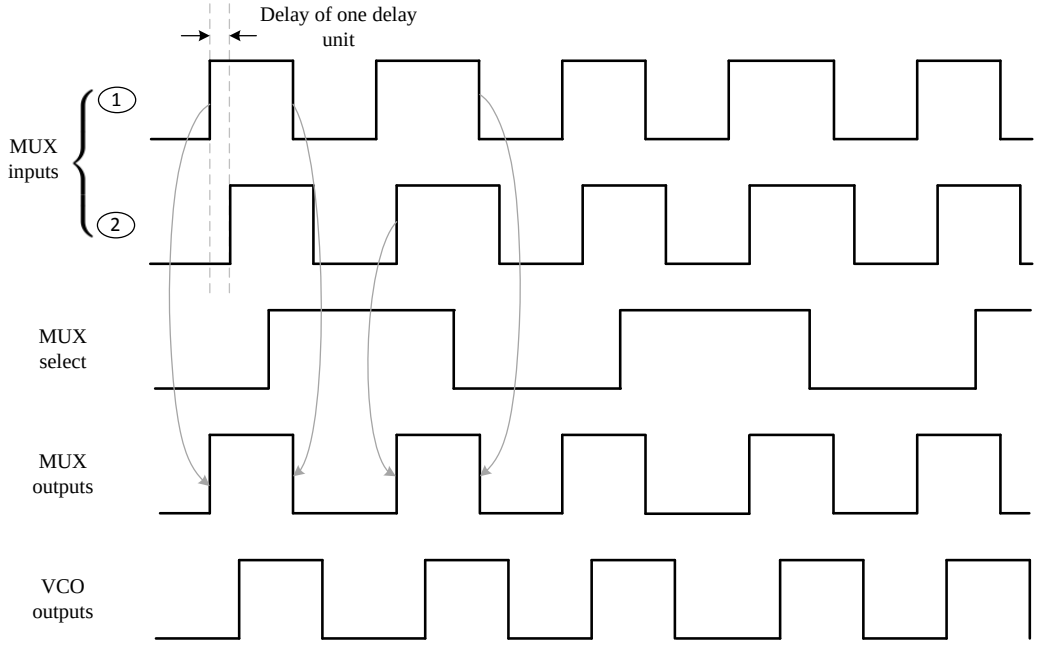

Figure 3.19: Representative waveforms for the VCO shown in Figure 3.18

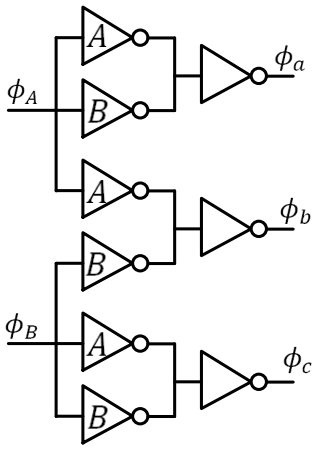

Figure 3.20: The phase interpolator

of the device widths in inverter A to the total device widths in both inverters A and B [32]. For example, to set Φ_b exactly at the middle of Φ_a and Φ_c, the relative size ratio should be 0.6.

Multi-level PI can be used to divide the phase between Φ_A and Φ_B into even

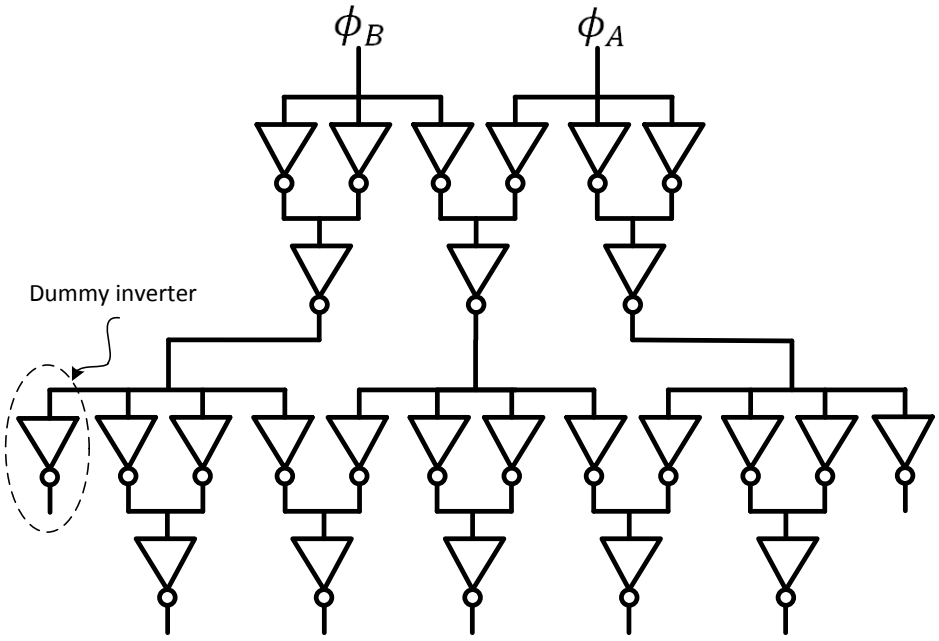

Figure 3.21: 2-level phase interpolator

smaller divisions. Figure 3.21 shows a 2-level phase interpolator. As we can see in Figure 3.21, dummy inverters is needed to ensure the balance of the intermediate nodes.

By controlling the relative size ratio of the phase interpolator inverters, the PI can be used to divide the phase between Φ_A and Φ_B into non-equal divisions. This is used in implementing the non-linear multibit internal quantizer in the TADC. Figure 3.22 shows an example of a non-linear characteristic curve that relates the delay of the VCO sampler to its analog input. To generate a non-linear feedback phase levels for this curve, the curve is divided into equally spaced horizontal divisions. This results in non-equal vertical divisions due to the non-linear curve. Let us assume that we divide the curve into five divisions. The goal of the phase interpolator is to generate a set of edges (phases) that are spaced in time according to the values of these vertical divisions. This can be done using a 2-level PI. In the first level, PI level 1 in Figure 3.22, the relative size ratio of the inverters is set such that the time difference between the edges of the input signals is divided into A_1 and B_1. The second level of PI, PI level 2a and PI level 2b in Figure 3.22, divides

the two regions, A_1 and B_1, into A_{2a} and B_{2a} and A_{2b} and B_{2b}, respectively. The final phase interpolator output is shown in the upper right hand corner of Figure 3.22. For proper operation of the TADC, the comparison levels must be set at

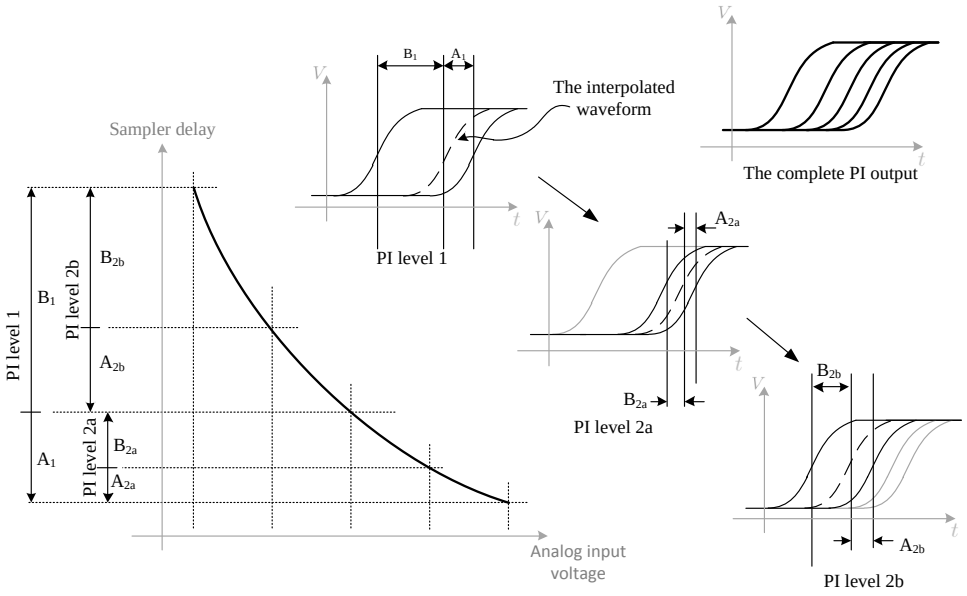

Figure 3.22: Non-uniform phase interpolation: an example

exactly the midpoint of the feedback levels. For the example in Figure 3.22, the reference signals must be separated in time by the values $L1$, $L2$, and $L3$, as shown in Figure 3.23.

As we can see from Figure 3.23, the level differences are also not equal, i.e., $L1 \neq L2 \neq L3$. 2-level PI can be used again to generate the required 4 signals, where one of the actual 5 outputs of the PI will not be used.

3.5.3 Implementing the non-linear multibit internal quantizer in TADC using PI

3.5.3.1 Input VCO with PI

To incorporate the non-linear multibit internal quantizer in the TADC, non-uniform quantization levels and non-uniform feedback values are required. As discussed in

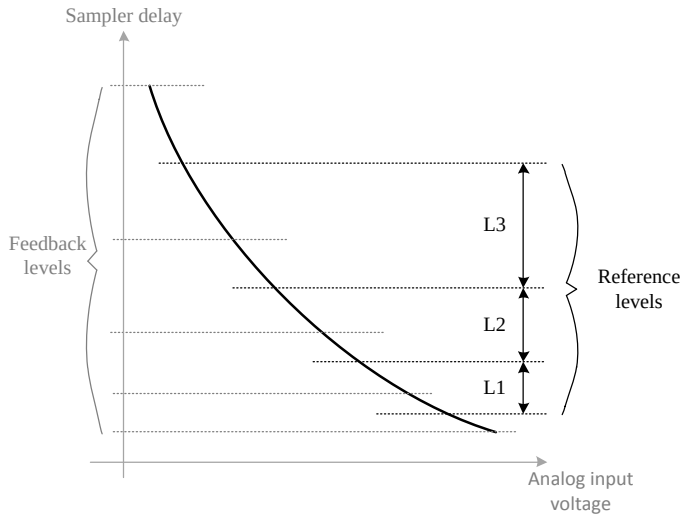

Figure 3.23: An example of a reference levels for a nonlinear curve

Section 3.5.2, the PI can be used to provide these levels. Figure 3.24 shows the modified version of the VCO of Figure 3.18. Again a delay chain together with MUX is inserted in the VCO ring, but this time the output of the original VCO inverter is connected to only one delay element. The delay elememt generates Φ_A and Φ_B signals, which are fed to a phase interpolator. The phase interpolater generates the required edges by changing the relative size ratios of its inverters. The loop is closed by connecting the MUX output back to the rest of the VCO inverter.

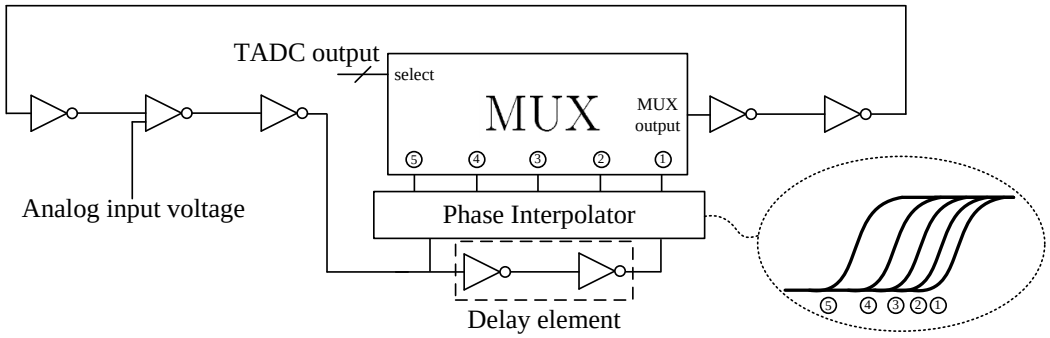

Figure 3.24: Input VCO with PI

Continuing on the example given in Figure 3.23, if MUX select is "10000", the MUX output starts copying from node 1 of the phase interlopator in Figure 3.24. The input VCO period in this case will be considered the nominal period, $T_{VCO_{nominal}}$. If MUX select is "01000", the MUX output starts copying from node 2 of the phase interlopator in Figure 3.24. Thus, the period of the input VCO will be equal to $T_{VCO_{nominal}} - A_{2a}$, where A_{2a} is shown in Figure 3.22. If MUX select is "00100", the MUX output starts copying from node 3 of the phase interlopator in Figure 3.24. Thus, the period of the input VCO will be equal to $T_{VCO_{nominal}} - A_1$, where A_1 is shown in Figure 3.22, and so on.

3.5.3.2 Reference VCO with PI

For proper operation of the multi-bit non-linear internal quantizer technique, the reference signals from the reference VCO must have the same period, but shifted from each other according to the non-linear characteristic curve, as discussed in Section 3.5.2. Figure 3.25 shows the reference VCO. The ring oscillator inside generates the reference period T_{ref}. Two of the ring oscillator inverter outputs are connected to the phase interpolator which generates the required reference signals.

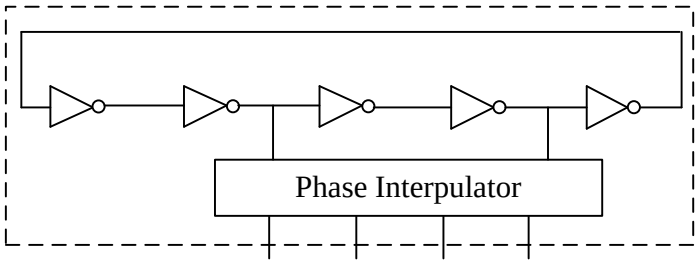

Figure 3.25: The reference VCO with PI

3.5.4 The functionality of the proposed TADC

Figure 3.26 shows the complete block diagram of the proposed TADC with multi-bit non-linear inherent quantizer. The output of the input VCO is connected to the data input of a bank of identical D-FFs. The clock input of each D-FF is

connected to one of the reference VCO outputs. The MUX control circuit converts the thermometer code generated by the D-FFs into proper form to control the selection of the MUX in the input VCO, thus realizing proper shifting (equivelant to subtraction in amplitude based ΣΔ modulator).

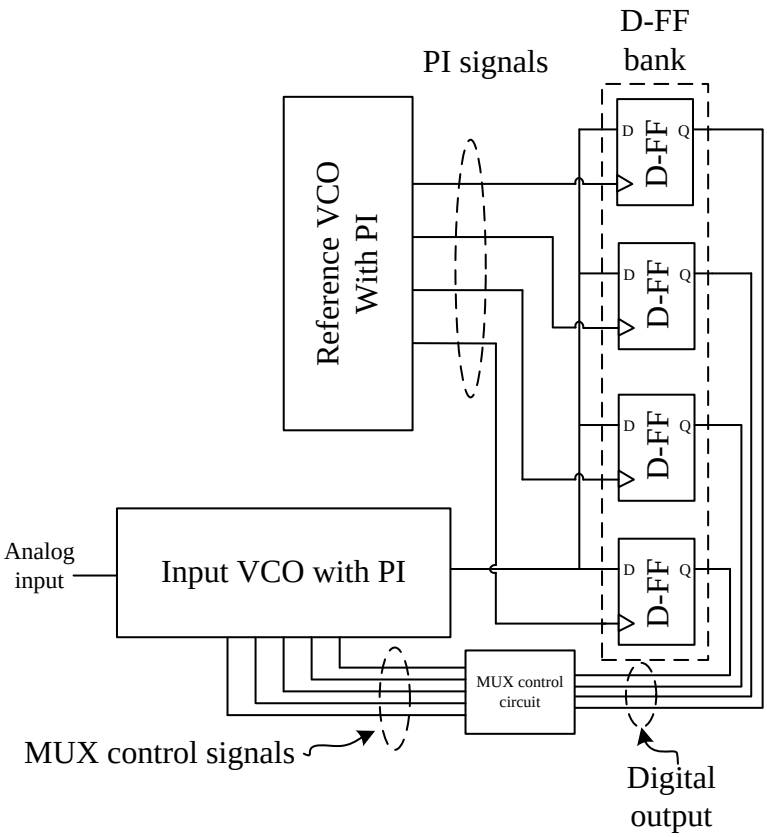

Figure 3.26: The proposed TADC with PI

Figure 3.27 illustrates set of representative waveforms for the TADC shown in Figure 3.26. As we can see in Figure 3.27, the rising edge of the input VCO output is compared with the rising edges of the reference signals, using the D-FFs. In the first reference period, the digital output is "0000" and the MUX control circuit produces "10000". This results in making the MUX output to copy from node 1 of the phase interploator output and hence, the period of the VCO is equal to $T_{VCO_{nominal}}$. In the second period of the reference signals, the digital output is "0011" and the MUX control circuit produces "00100". This results in making the

MUX output to copy from node 3 of the phase interploator output and hence, the period of the VCO is equal to $T_{VCO_{nominal}} - A_1$.

Note: For proper operation of the proposed TADC, the MUX output, in the VCO, must copy the falling edge from the same phase interpolator node, regardless of the output of the TADC. In Figure 3.27, the MUX output keeps copying the falling edge from node 1 of the phase interpolator, when the ΣΔ output is "0000" and "0011".

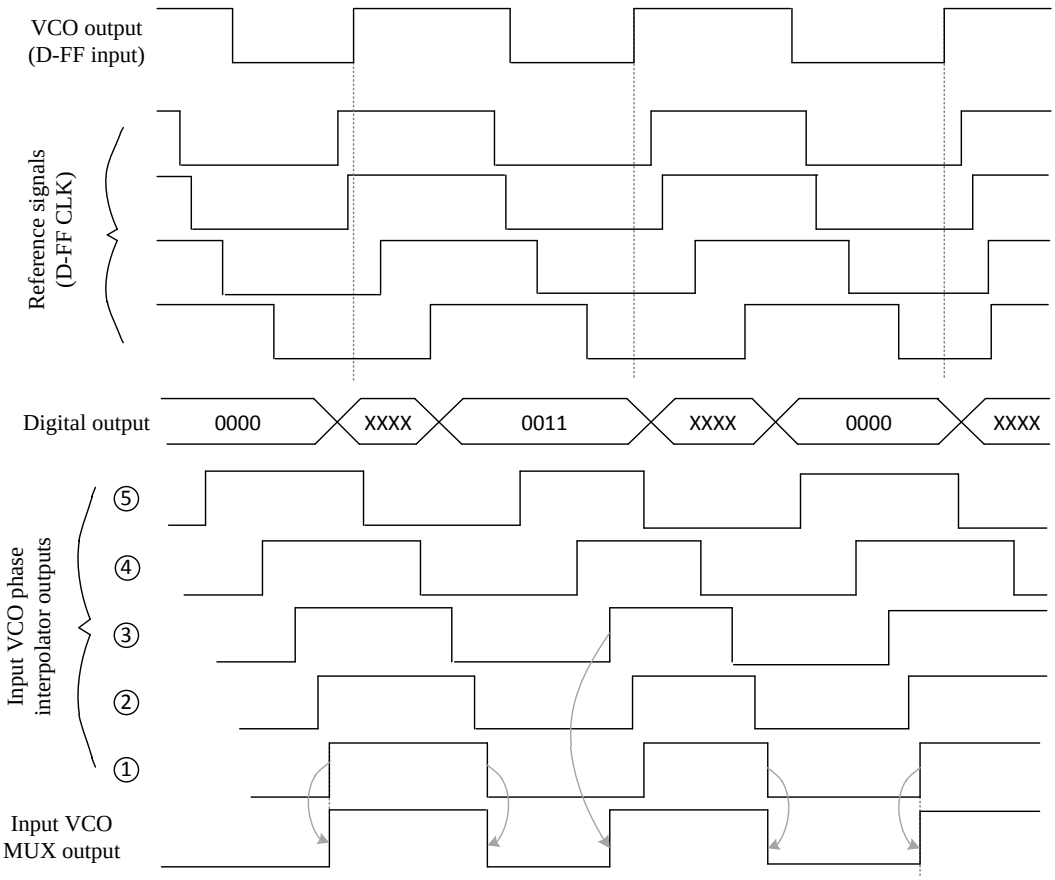

Figure 3.27: Set of representative waveforms for the proposed TADC when $V_{in} = V_{ref}/2$

3.5.5 Simulation results

To prove the functionality of the proposed TADC in 0.13μm CMOS and to measure its performance, a complete system has been built, with non-idealities introduced and simulated. Our design methodology stars by doing block diagram simulations of the proposed. Then transistor levels simulations followed by post-layout simulations are performed. Finally, the the TADC is fabricated (using 0.13μm CMOS technology) and the chip is measured. In this chapter, block diagram simulation using Matlab is presented. In Chapter 4, Cadence and Eldo are used to do both the transistor-level and the post-layout simulations of the TADC. Eldo is used to do timing jitter simulations. The measurement results from a fabricated chip is also presented in Chapter 4.

Our goal is to build a TADC that has a 12bit resolution for 2MHz bandwidth. Thus the distortion should be below 12bit. Figure 3.28 shows the FFT of the digital output of the TADC, starting with a linear quantizer (i.e., nonlinear multibit quantizer has not been introduced yet). The input frequency is $1MHz$ and the reference frequency is 1GHz. As we can see in Figure 3.28, the distortion level is about 17dB, which corresponds to 3bit resolution.

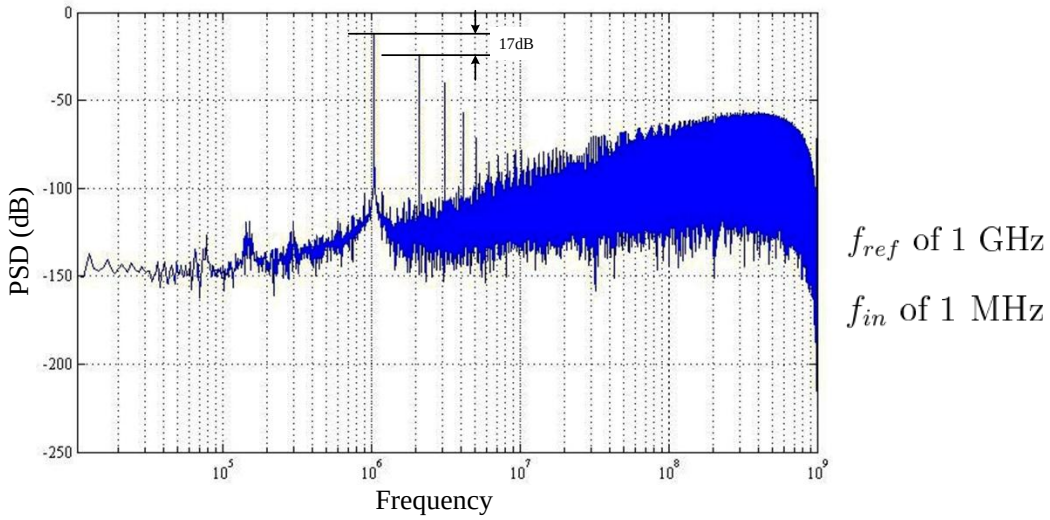

Figure 3.28: FFT of the system with linear quantizer

On the other hand, Figure 3.29 shows the FFT of the digital output of the TADC with the multibit non-linear quantizer. As we can see from Figure 3.29, the

distortion level is about 78dB. For the quantization noise, the level of the noise floor is about 130dB below the peak value. For the bandwidth of 2MHz, this translates into a SNDR of 75*db*. This means that the resolution of TADC is more than 12bit. Thus, with multibit non-linear internal quantizer, the TADC achieves the required 12bit resolution for 2MHz bandwidth.

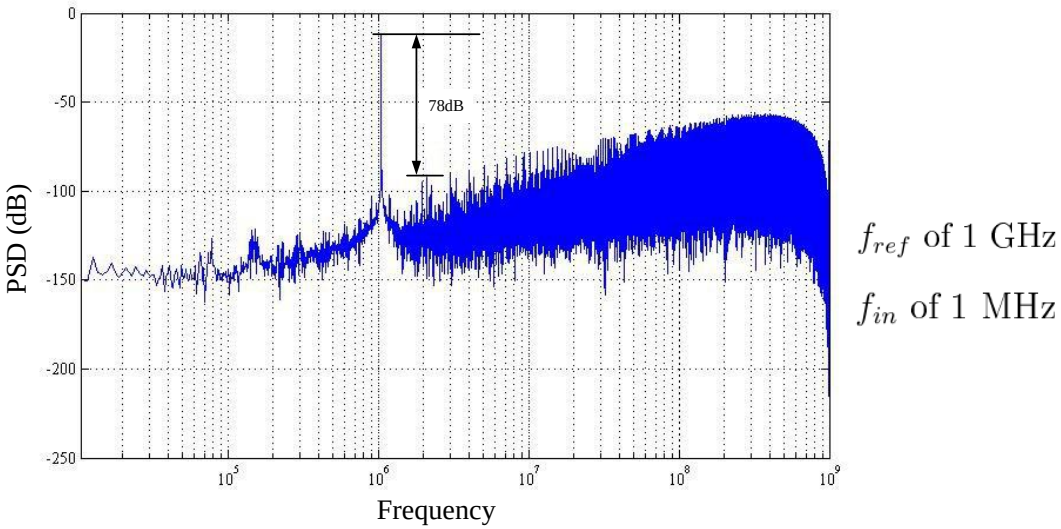

Figure 3.29: FFT of the system with non-linear multibit quantizer

Figure 3.30 shows SNR as function of the input signal amplitude.

While the reference VCO is designed such that the reference frequency is 1GHz, post-layout simulations show that the reference frequency drops to 300MHz after layout. This drop in frequency is due to the parasitic and interconnection capacitors. Block level simulation is redone for the system with a 300MHz reference frequency to investigate the effect of the reduction of the reference frequency on the performance of the TADC. Figure 3.31 shows the FFT of the digital output. As we can see, the distortion level is the same as the case when the reference frequency is 1GHz. This is expected because the multi-bit non-linear internal quantizer technique does not depend on the value of the reference frequency.

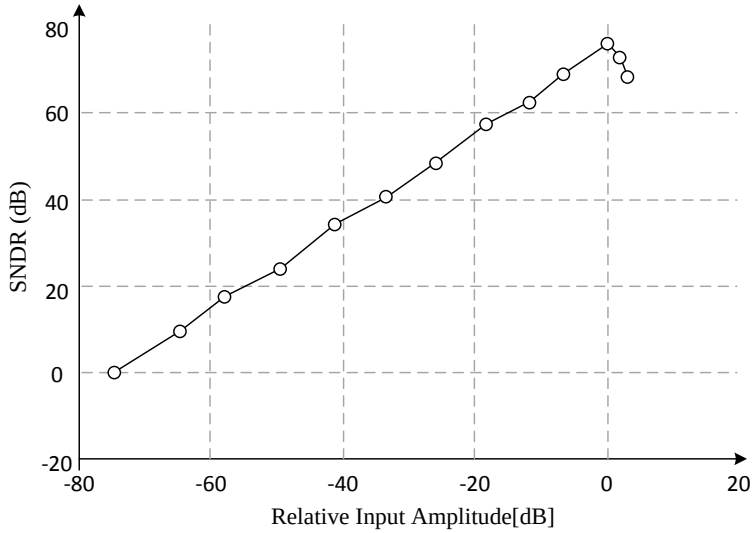

Figure 3.30: System level simulation SNDR as function of signal amplitude

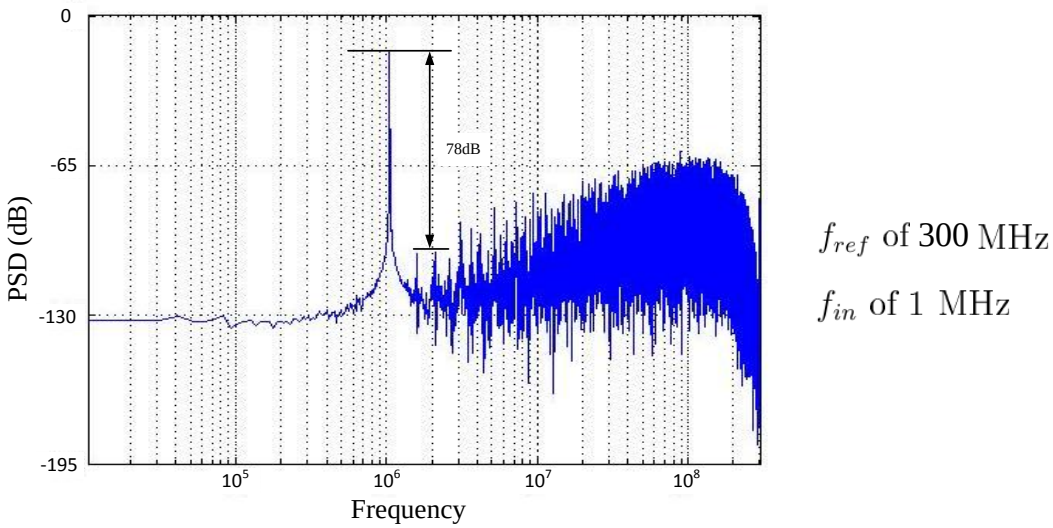

Figure 3.31: FFT of the system with non-linear multi-bit quantizer, and 300MHz reference frequency, same distortion level as the 1GHz case

3.5.6 Nonidealities

3.5.6.1 Non-uniform sampling

Figure 3.32 shows the deviation of the input VCO period from its nominal value, 1ns, during one period of the input signal. As we can see from Figure 3.32, the maximum deviation is about 60 ps. From Section 3.2.3, Equation (3.9) sets 122ps as a maximum limit for the sampling period deviation that results in NUS distortion less than the 12bit resolution. Because the deviation of the input VCO period is

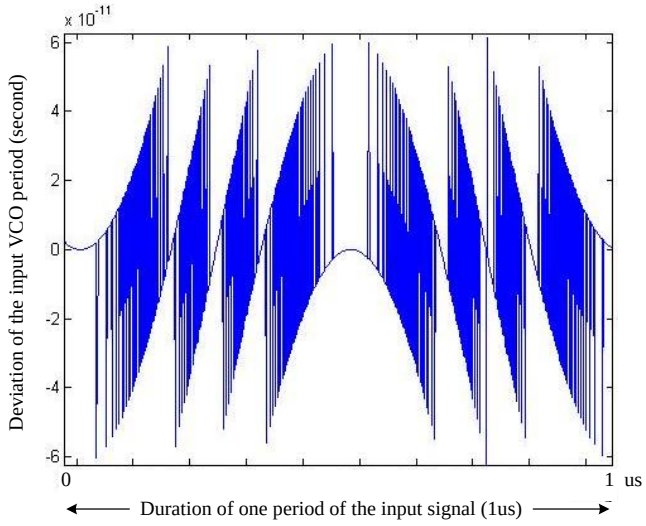

Figure 3.32: The deviation of the input VCO period from its nominal value

less than this limit, the NUS distortion is acceptable.

To illustrate the NUS distortion, the same system has been simulated again but this time the deviation of the input VCO period is increased to around 250ps, as shown in Figure 3.33. Figure 3.34 shows the FFT of the digital output of the TADC after increasing the deviation of the input VCO period. As we can see from Figure 3.34, the perfomance of the TADC is degraded due to the NUS distortion. The level of the distortion is about 65dB which results in lowering the resolution of the TADC to below 11bit.

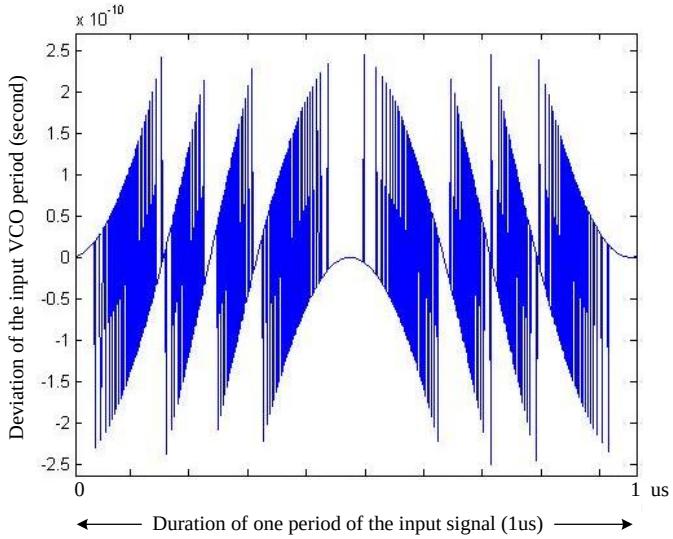

Figure 3.33: The deviation of the input VCO period from its nominal value, K_{VCO} is four time that of Figure 3.32

3.5.6.2 Mismatch in the DTC

Fabrication process limitations, temperature gradients across the circuit, and component aging cause circuit component values to differ from their design values. The random part of these variations, called random mismatch, degrades the performance of the TADC and causes distortion. The difference between the actual component value and the ideal component value is called mismatch error. It is known that for multi-bit ΣΔ modulator, the mismatch induced distortion arises from the random mismatch in the feedback DTC. To explore such effect, the TADC is simulated with 5% random mismatch in the feedback DTC; realized with PI, i.e., 5% mismatch in the phase interpolator inverters sizes, from the designed values.

As we can see in Figure 3.35, the distortion level is about $51dB$. This results in lowering the TADC resolution to below 9bits.

To overcome the problem of the DAC random mismatch in ΔΣ, dynamic element matching is used. A design that uses dynamic element matching will be discussed in the next section.

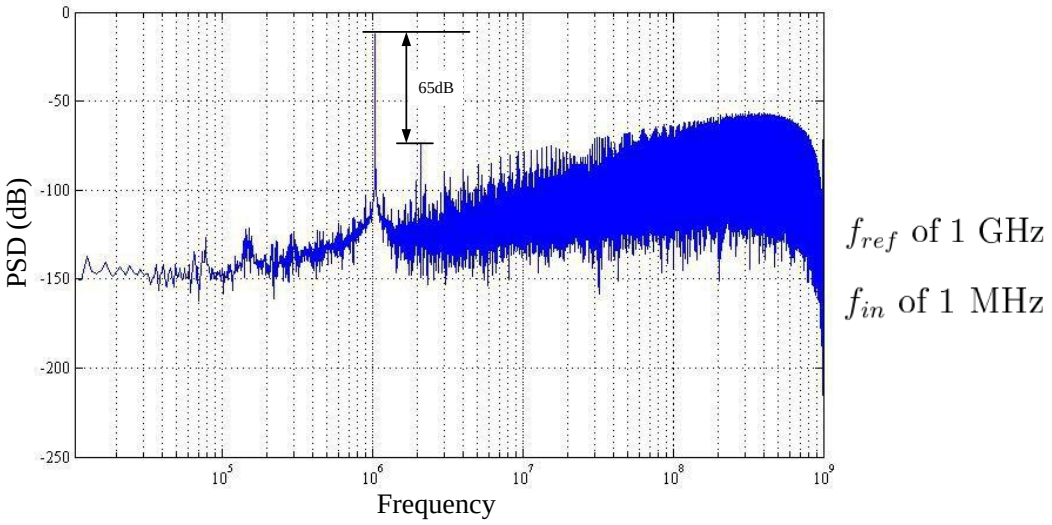

Figure 3.34: FFT of the TADC with NUS distortion that is present at input VCO period deviation of $250ps$

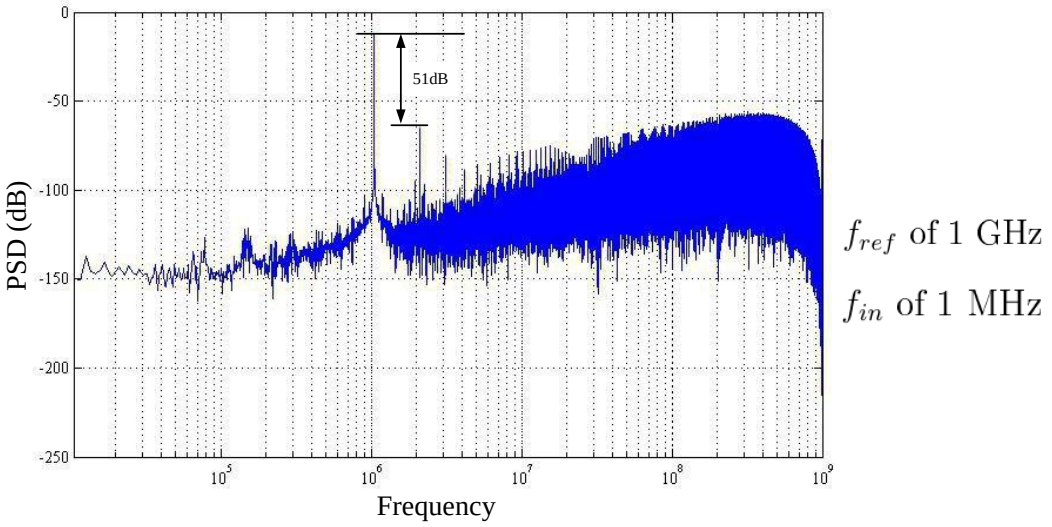

Figure 3.35: FFT of the TADC with 5% mismatch

3.6 Design II: First-order ΣΔ modulator, PI, and Dynamic element matching incorporated (to further decrease distortion)

To improve the TADC performance against the mismatch in the DAC (the feedback levels), Design II is proposed. In this design, dynamic element matching is used to improve the DAC performance.

3.6.1 Dynamic element matching: Review

Dynamic element matching (DEM) [33] is used to reduce the impact of the component mismatch errors in the DAC on the performance of the TADC.

To demonstrate the principles of DEM in DAC, consider the D bit DEM DAC topology in Figure 3.36 [34]. This topology performs DEM by mapping a D bit input signal, $x[n]$, to 2^D single-bit DACs through a 2^D line interconnection network. In this topology, a thermometer encoder converts the D bit binary-coded

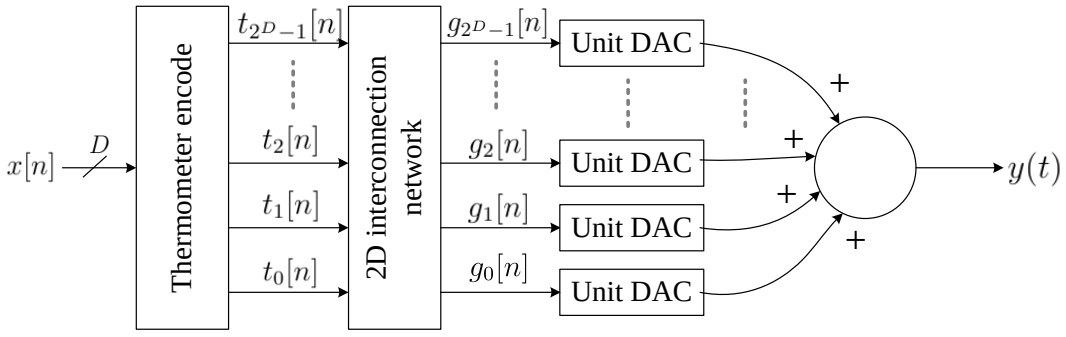

Figure 3.36: D bit DEM DAC

signal into a thermometer coded signal, $t[n]$. Without the interconnection network, the thermometer coded signal activates particular single bit DACs. Ideally, each deactivated single bit DAC generates an analog signal of amplitude zero, and each activated single bit DAC generates an analog signal of amplitude A. The outputs of all the single-bit DACs are summed to produce the DAC's output, $y(t)$. In practice, the mismatch of the unit DACs causes conversion errors that cause harmonic

distortion. Using the interconnection network to randomize the mapping between the thermometer coded signal and the array of unit DACs, the mapping between $t[n]$ and $g[n]$, the positions of mismatched unit DACs can be virtually moved. With a deterministic DEM interconnection network, the thermometer coded signal activates single bit DACs chosen according to a deterministic algorithm. As a result of this rearrangement of unit DACs, the mismatched components lead to harmonic distortion. This distortion is reduced or removed in subsequent processing, typically by lowpass filtering. With a random DEM interconnection network, the thermometer coded signal activates single bit DACs randomly chosen. As a result of this virtual rearrangement of unit DACs, the mismatched components lead to noise instead of harmonic distortion. Thus, we can conclude that the DAC mismatch effect on the ADC can be reduced by using DEM. In the next subsections, we will go through, in some details, the simplest DEM approach, clocked level averaging. We will then briefly review the more sophisticated ones.

3.6.1.1 Clocked level averaging DEM

Clocked level averaging DEM (CLA) cyclically shifts each element in the chain one position in the same direction every time interval T [33, 35, 36]. Figure 3.37 shows an example of a chain of N equal resistors that provide series of tap voltages. If there is no mismatch between the resistor, the voltage between any two adjacent taps, $V_{i,j}$, should be equal.

To illustrate how CLA works, let us assume that the resistor is ordered as shown in Figure 3.37(a). Using electronic switches which are not shown in 3.37, the voltage divider resistors are sequentially rotated from position to position. After one rotation, the resistor chain will appear as illustrated in Figure 3.37(b).

After N cycles, each mismatched element will have occupied each of the chain positions. Rotating the mismatched elements creates a chain where mismatch in tap voltage is average out.

Specifically the voltage, $V_{i,j}$, across the resistor in the ith resistor location when the resistor R_j is occupying it is

$$V_{i,j} = I \times R_j \tag{3.13}$$

Here I is the current flowing through the resistors. After N cycles, each resistor

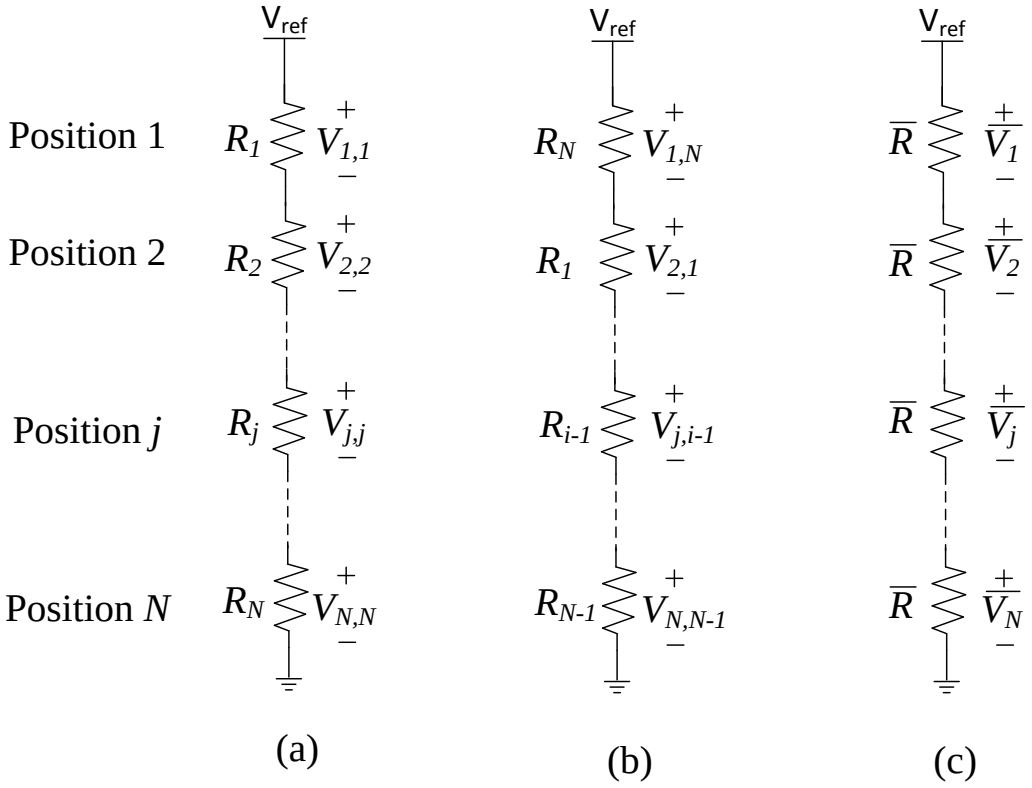

Figure 3.37: An example of a clocked level averaging

has occupied each of the resistor positions and the average voltage, $\bar{V_i}$, at the ith resistor position is

$$\bar{V_i} = \frac{1}{N}\sum_{j=1}^{N} V_{i,j} = I(\frac{1}{N}\sum_{j=1}^{N} R_j) = I \times \bar{R} \tag{3.14}$$

Here $\bar{R}$ is the average resistance of the mismatched resistors. On average, applying DEM to the voltage divider shown in Figure 3.37(a) is equivalent to the equivalent voltage divider shown in Figure 3.37(c) where each resistor has resistance $\bar{R}$ and $\bar{V_1} = \bar{V_2} = \cdots = \bar{V_N}$. Thus, on average, clocked averaging DEM creates an equivalent voltage divider with no mismatch.

When a CLA is used in an multibit oversampling ADC, the correlation between the CLA and the averaging action inherent to the $\Delta\Sigma$ modulator causes harmonic distortion [37].

3.6.1.2 Individual level averaging DEM

Individual level averaging (ILA) rotates or flips circuit elements in a periodic fashion, but a separate rotation state is maintained for each digital level. The advantage of the ILA algorithm over the CLA is that distortion is moved into higher frequency bands while preserving the noise shaping characteristics of the ΔΣ converters [37, 38].

3.6.1.3 Data weighted averaging DEM

The data weighted averaging DEM algorithm (DWA) also rotates circuit elements according to the ΣΔ output code words. The circuit components are rotated at high rate, causing the mismatch errors to sum to zero more quickly. The DWA preserved the noise shaping characteristics of the modulator in ΔΣ converters but has tones [39].

3.6.1.4 Stochastic level averaging DEM

While the deterministic DEM algorithms, such as clocked level averaging, individual level averaging and data weighted averaging, moves the harmonic distortion to higher frequency bands, stochastic level averaging spreads the mismatch error energy across the spectrum [34, 40]. Stochastic level averaging, or stochastic DEM, randomly order the DAC elements each sample.

Next, the structure of the proposed VCO will be presented. We will then, in section 3.6.4, explain how DWA is inherent in the proposed VCO.

3.6.2 Proposed VCO structure: block diagram

Figure 3.38 shows the proposed VCO structure. The core of the VCO is a normal inverter ring oscillator and in the example design in Figure 3.38 has 13 stages numbered $1, 2, \ldots, 13$. In normal operation, one of the delay stages is replaced by the sampler. Switches are connected on each input of the ring oscillator stages. These switches are used to shift the sampler inside the ring where for illustration the sampler position is initially in parallel with inverter 1 with switches SW_{13} and

SW_1 open. This effectively replaces inverter 1 in the ring so that the ring consists of $S(\text{the sampler}), 2, 3, 4, \ldots, 13$. With different feedback values the sampler replaces different inverters in the ring e.g. $1, 2, S, 4, \ldots, 13$. As will be explained later such shifting of the sampler in the VCO effectively preforms DEM. The outputs of all the VCO core inverters are connected to multi-level phase interpolator. Each portion of the phase interpolator divides the time duration between the output phases of inverters i and $i + 2$ of the ring oscillator into uniform spaced divisions. The level of the phase interpolator is chosen according to the required time resolution.

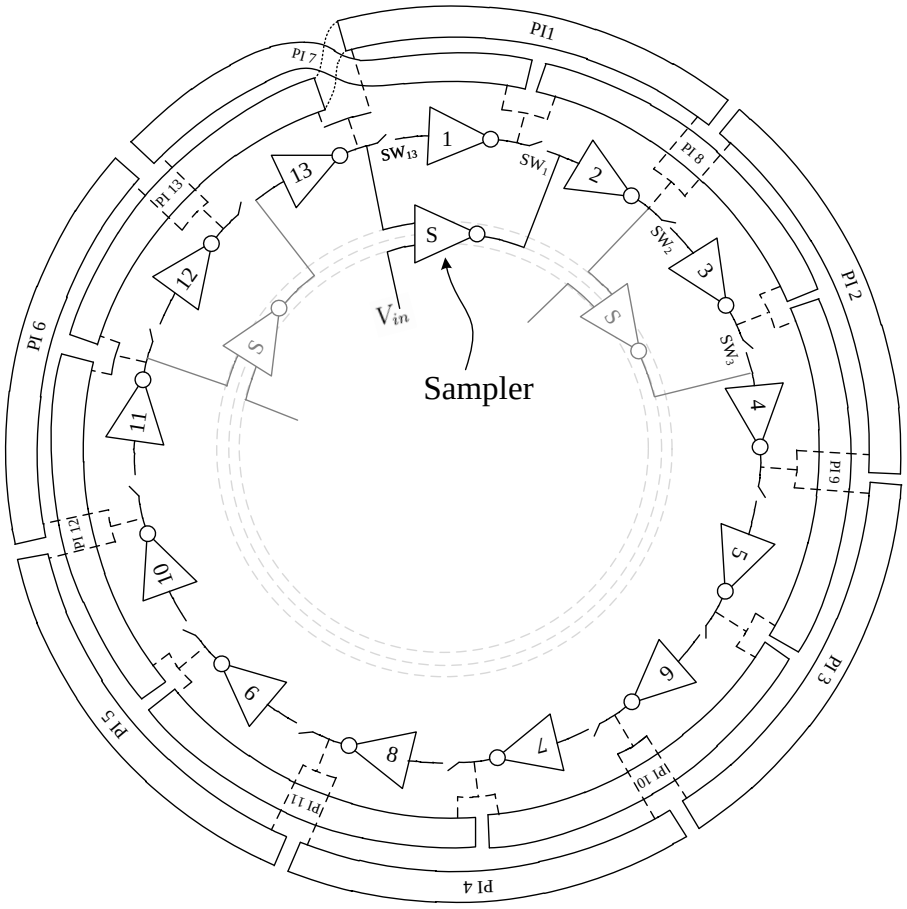

Figure 3.38: The proposed input VCO structure with DEM

The digital output of the TADC controls the period of the proposed VCO by

selecting which output of the phase interpolator is connected to the output of the VCO. The selection is done through a MUX, not shown in Figure 3.38, whose inputs are connected to the outputs of the phase interpolator and its output is controlled by the feedback signals that come from the output of the TADC. If the feedback is zero, the MUX output will continue copying from the same phase interpolation output. This results in making the period of the MUX output signal equal to $T_{VCO_{nominal}}$. If the feedback is positive (decrease the period of VCO), the MUX will start copying from an phase interpolation output whose edge rises before the one that corresponds to the current position. This results in making the period of the MUX output signal equal to $T_{VCO_{nominal}} - T_{feedback}$, where $T_{feedback}$ is the absolute value of the phase difference between the two phase interpolator outputs. The level of the feedback determines how big is the jump between the current position and the new position where the MUX starts copying, the value of $T_{feedback}$. On the other hand, if the feedback is negative (increase the period of VCO), the MUX will start copying from a phase interpolation output whose edge rises after the one that corresponds to the current position. This results in making the period of the MUX output signal equal to $T_{VCO_{nominal}} + T_{feedback}$. Again the level of the feedback determines how big is the jump between the current position and the new position, where the MUX starts copying.

Initially, using the switches, the sampler is switched in and replaces inverter 1 in the ring oscillator. The MUX output is initially connected to the middle output of portion 11 of the phase interplator (PI11), which interpolate the output of inverter 7 and 9. The analog input controls the period of the inner ring of the VCO. The output of the phase interpolator, which the MUX output copies, moves according to the feedback value. If the feedback causes the MUX to copy from the output of different phase interpolator portion, the switches status changes, such that the sampler replaces another inverter (inverter $i+2$) that is two delays from the current inverter (inverter i). For example, if the MUX needs to copy from portion 12 of the phase interpolation (PI12), the sampler will replace inverter 3.

3.6.3 Proposed VCO: Implementation of non-linear multibit quantizer

In the proposed VCO, the phase interpolator divides the time duration between the output of inverters i and $i+2$, of the ring oscillator, into equal divisions. In other words, the VCO output can be manipulated, by the feedback from the TADC output, by multiples of the smallest division generated by the phase interpolator.

To be able to implement the multibit non-linear quantizer as discussed in section 3.5.2, the smallest division, generated by the phase interpolator, needs to be such that all the differences between the feedback levels can be expressed as multiples of such smallest division, while keeping the deviation, (the differences between the actual t_{delay} vs V_{in} characteristic and the piecewise linear approximation), smaller than the required resolution. Making the division small requires the level of the phase interpolator to be high. This is not practical because increasing the level of the phase interpolator means increasing the power and the area of the phase interpolator. Moreover, the accumulated timing jitter of a multi-level phase interpolation increases.

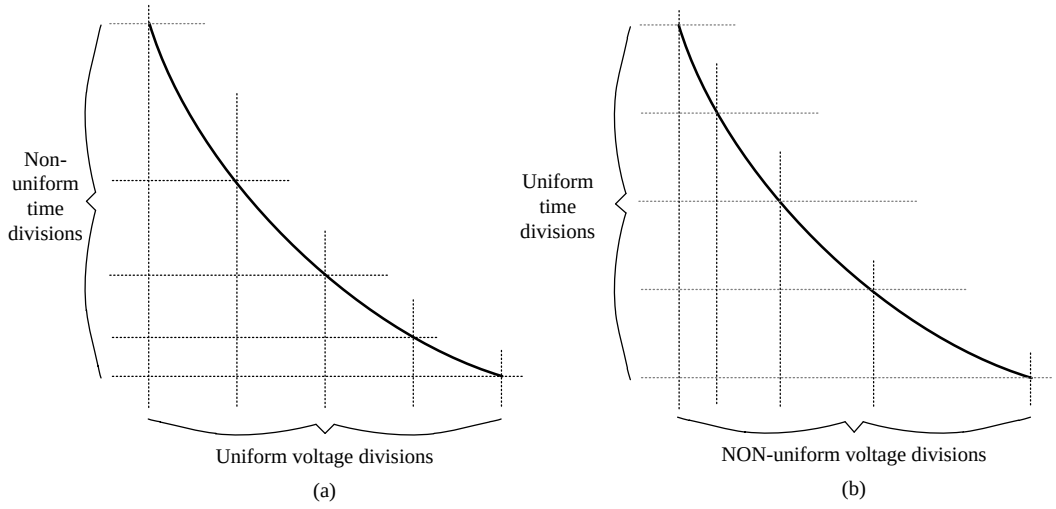

Figure 3.39: (a)uniform voltage non-linear quantizer approach (b)uniform time non-linear quantizer approach

Figure 3.39 shows another approach to perform the multibit non-linear quantizer, to overcome the need of using multi-level phase interpolator. Instead of divid-

ing the non-linear characteristic curve, which governs the conversion from voltage to time, into uniform voltage divisions, as shown in Figure 3.39(a), the curve is divided into uniform time divisions or into time divisions that are multiples of the smallest division of the phase interpolator, as shown in Figure 3.39(b). The number (and hence the duration) of the time divisions, in which the curve is divided, must be chosen such that the INL of the piecewise linear approximation is smaller than the required resolution.

Dividing the non-linear curve into uniform time divisions, or time divisions that are multiples of the smallest division of the phase interpolator results into non-uniform voltage divisions.

3.6.4 DWA in the feedback DAC

The technique in which the DAC action is done in the proposed VCO inherently incorporate DWA in time domain. As we discussed in section 3.6.2, the feedback is applied to the VCO by moving the position of output of the phase interpolator from where the MUX output copies. This corresponds to applying the first available element (hitherto unused) in the DWA algorithm. The new position of the phase interpolator output, from which the MUX will start copying, is determined by the value of the feedback. This corresponds, to the DWA algorithm, where the number of the elements used from the array, is determined by the value of the feedback. It should be noted that all the smallest time divisions of the phase interpolator output sum up to one complete period of the inner ring. As a result, when all the outputs of the phase interpolator is exercised, averaging is assured. As with DWA, to cycle through all the elements as soon as possible, the period of the inner VCO should be made as small as possible.

Note: for proper operation of the TADC, the reference edges should be set in the middle between the feedback edges.

3.6.5 Simulation results

To show the functionality of the proposed TADC and its performance, a complete system has been designed and simulated. Our goal here is to build a TADC that achieves 12bit resolution for 2MHz and be robust against the random mismatch.

Figure 3.40 shows the FFT of the digital output of the TADC. As we can see from Figure 3.40, the distortion level is about 75*db*. For the quantization noise, the level of the noise floor is about 130dB below the peak value. Thus, the SNR of the TADC is 75dB for a bandwidth of 2MHz. This means that the resolution of TADC is 12*bit*. Figure 3.41 shows SNDR as function of the input signal amplitude.

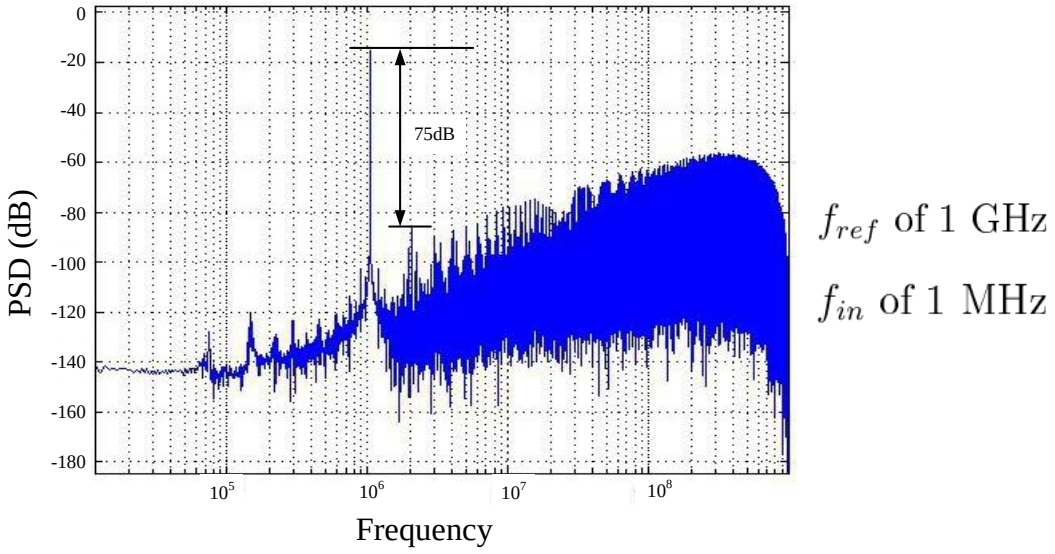

Figure 3.40: FFT of the output of the proposed system

Figure 3.42 shows the FFT of the digital output of the TADC after introducing 10% mismatch to the output phases of the phase interpelaator. As we can see from Figure 3.42, the distortion level does not increase. This shows that the DEM algorithm is working for this example. The noise floor increases to become 120*dB* below the peak value. Thus, this TADC show a good performance even with random mismatch. The TADC resolution is 12bit for 2MHz bandwidth.

Distortion can also be generated due to the mismatch between the piecewise linear approximation curve and the actual characteristic curve of the sampler (which is subject to process variation), as shown in Figure 3.43(a). Figure 3.44 shows the FFT of the digital output of the TADC after introducing 10% mismatch between the the piecewise linear approximation curve and the characteristic curve of the sampler. The output of the TADC correspond to V_1, V_2, V_3, and V_4, in Figure 3.43(a). As we can see from Figure 3.44, the distortion level is 60dB. This means

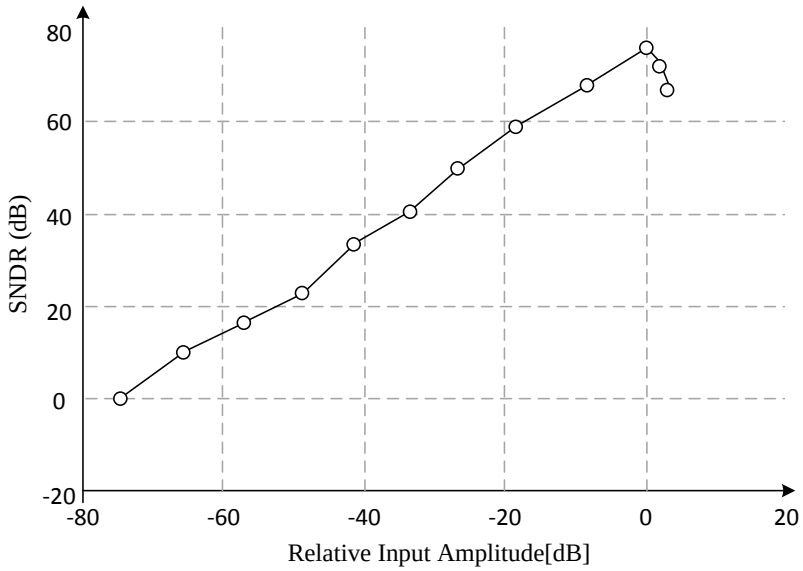

Figure 3.41: System level SNDR as function of signal amplitude

that the resolution of the TADC is 10bit.

One way to overcome this problem is to use digital calibration, as shown in Figure 3.43(b). Instead of making the digital output correspond to V_1, V_2, V_3, and V_4, they are correspond to V_1', V_2', V_3', and V_4'. This is determined by measuring on-chip the output at point of largest expected INL (typically the mid-point) and make calibration accordingly. Since the characteristic curve is monotonic, one measurement (at the mid-point; and for the worst case) should be sufficient. Figure 3.45 shows the FFT of the digital output of the TADC with digital calibration. As we can see from Figure 3.45, the distortion level goes back to 73dB. This means that the resolution of the TADC is restored back to 12bit.

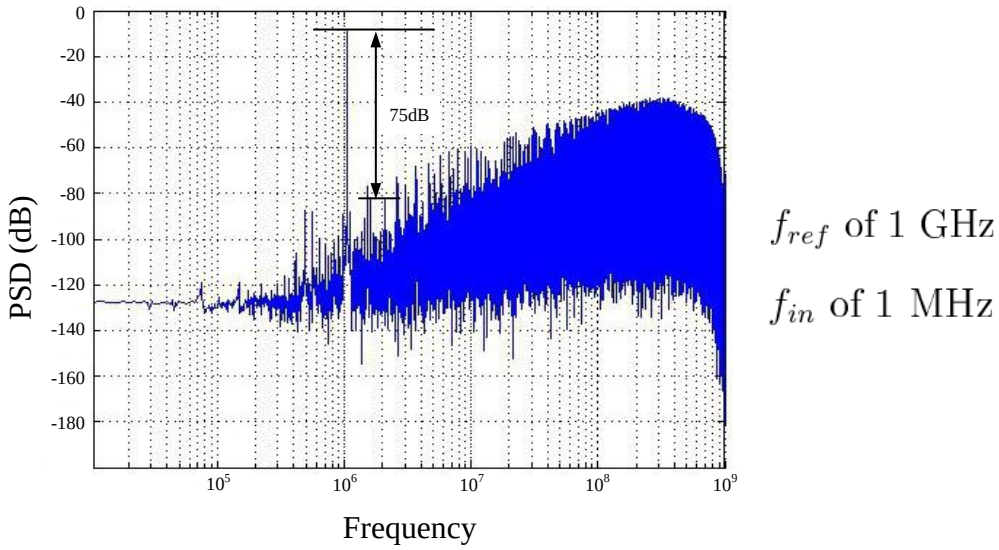

Figure 3.42: FFT of the output of the proposed system with 10% mismatch

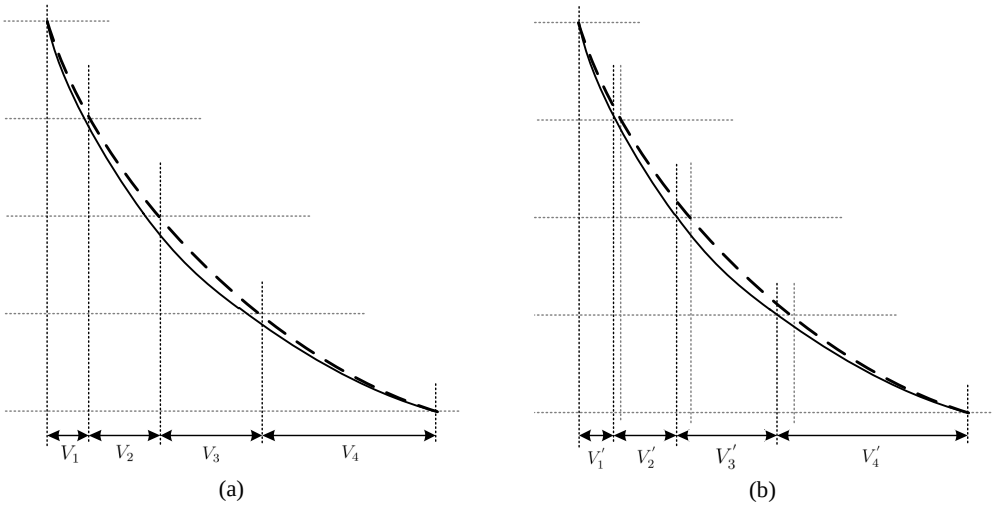

Figure 3.43: Improving the mismatch between the piecewise linear approximation and the actual characteristic curve of the sampler using digital correction

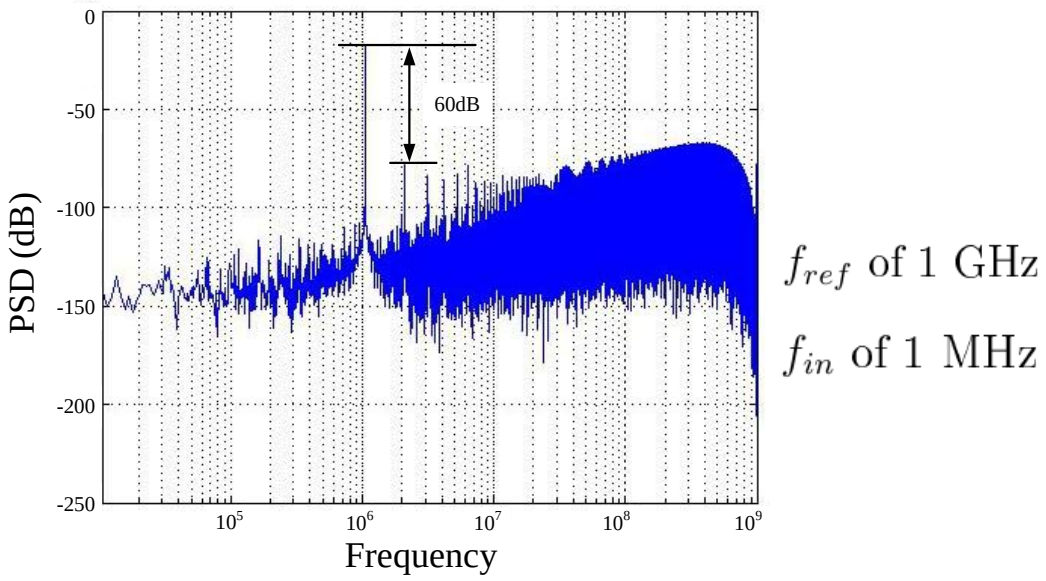

Figure 3.44: FFT of the output of the proposed system with 10% mismatch between the the piecewise linear approximation curve and the actual characteristic curve of the sampler

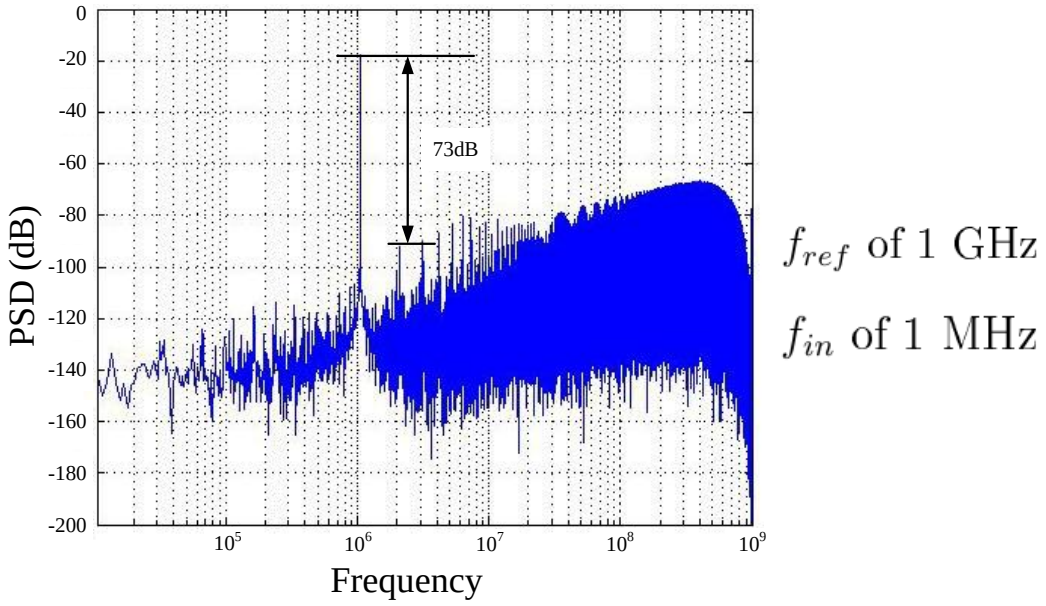

Figure 3.45: FFT of the output of the proposed system with digital correction

3.7 Design III: Second-order ΣΔ modulator, PI, and DEM incorporated (to increase the bandwidth)

High order TADC has been proposed in many literature [26, 28, 41]. Both [26, 28] use DMD to preform the first stage integration. Instead of quantizing the time difference between the DMD output and the reference clock, to perform a first order ΣΔ TADC, a phase/frequency detector is used to measure this time difference. This time difference is converted into voltage using a charge pump, as shown in Figure 3.46 [26]. Then a capacitor is used to preform the second stage integration. The D-FF is used as voltage comparator to generate the digital output. This means that the system is not completely time based ADC. It is a hybrid time-amplitude ADC.

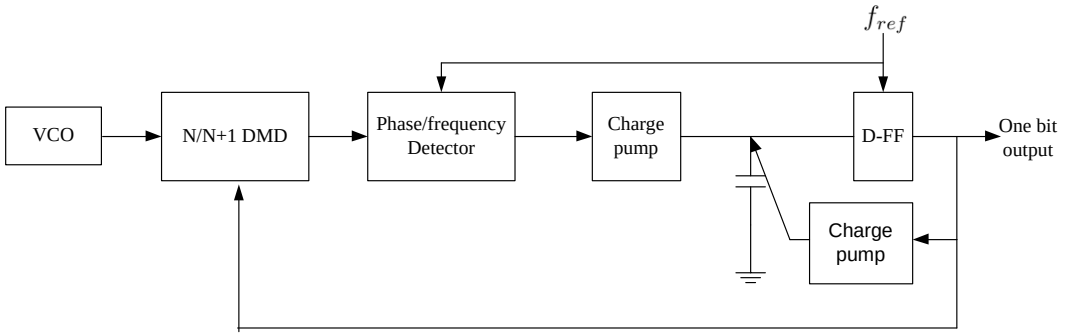

Figure 3.46: The second order system proposed in literature

In [41], the author use 1-1-1 mash structure to build a third-order system. Relaxation oscillator is used to preform the integration in each of the first-order parts.

In this section we propose a new time-based second-order ADC where both integrations are done in time domain.

3.7.1 The second-order sigma-delta modulator in time domain

In section 3.1, we show that by manipulating the edge of the VCO output signal, first order ΔΣ modulator in time domain can be implemented. In this section, this idea will be extended to the second order ΔΣ modulator.

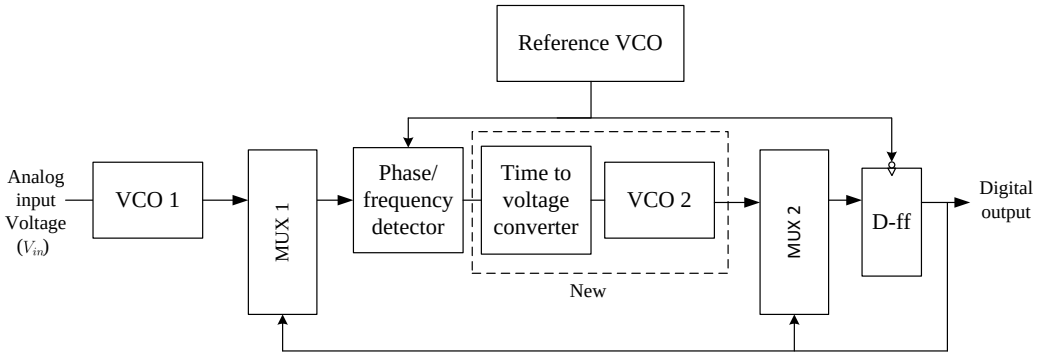

Figure 3.47: Block diagram of the second order ΔΣ TADC

Figure 3.47 shows the general system that implements the second order ΔΣ in time domain, it is an extension of the one shown in Figure 3.1. Instead of quantizing the phase difference between the shifted version of VCO1 output signal and the phase of the reference clock, using a D-FF, the time difference now is used to control the period of VCO2. A shifted version of VCO2 is generated, using a MUX, and the phase difference between the shifted version of VCO2 output signal and the phase of the reference clock is quantized to produce the digital output of the ΔΣ modulator. The digital output is fedback to control the generation of the shifted version of both VCO1 and VCO2. For proper operation of the system, the phase of shifted version of VCO1 needs to be compared to the rising edge of the reference clock while the phase of the shifted version of VCO2 needs to be compared with the falling edge of the reference, or vice versa.

Figure 3.48 illustrates a set of representative waveforms for the system shown in Figure 3.47. As we can see from Figure 3.48, the period of the VCO2 (MUX2 input 0), trace 5 in Figure 3.48, is controlled by the time difference, $\tau_1(k)$, the time difference between the rising edge of shifted version of VCO1 output and rising edge

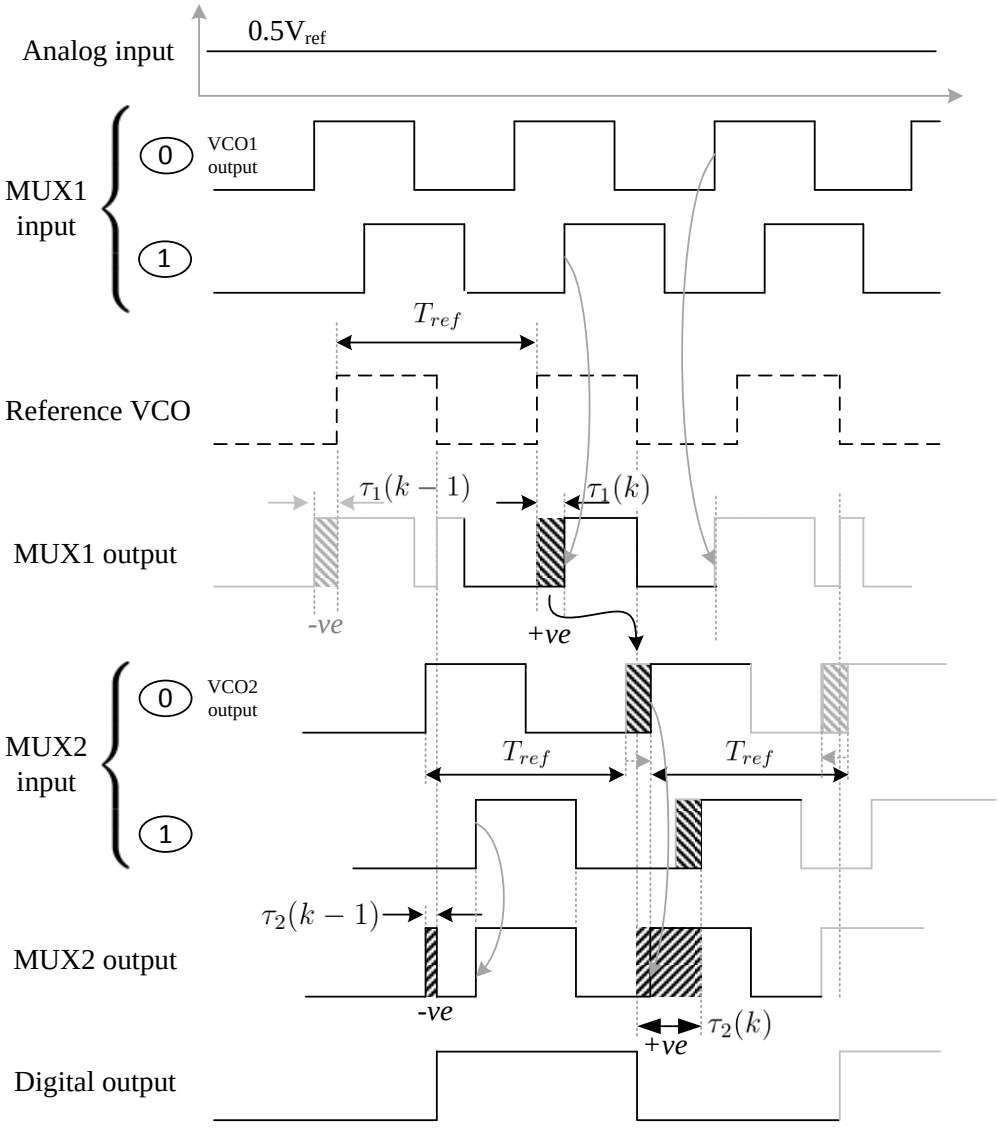

Figure 3.48: Representative waveforms for the system shown in Figure 3.47, $V_{in} = V_{ref}/2$

of the reference signal. The period of VCO2 is given by

$$T_{VCO2}(k) = T_{ref} + \tau_1(k) \tag{3.15}$$

Again, the system can be mathematically modeled by writing the time equation

of $\tau_1(k)$ and $\tau_2(k)$. $\tau_2(k)$ is the time difference between the rising edge of shifted version of VCO2 output and falling edge of the reference signal. The time equation of $\tau_2(k)$ can be written as

$$T_{ref} + \tau_2(k) = T_{VCO2}(k) - Sgn(\tau_2(k-1)) \times t_{unit\ delay} + \tau_2(k-1) \tag{3.16}$$

By reordering the terms of (3.16) and by substituting from (3.15), we can write

$$\tau_2(k) = \tau_2(k-1) + \tau_1(k) - Sgn(\tau_2(k-1)) \times t_{unit\ delay} \tag{3.17}$$

The time equation of $\tau_1(k)$ can be written as

$$\tau_1(k) = \tau_1(k-1) + T_{in} - Sgn(\tau_2(k-1)) \times t_{unit\ delay} \tag{3.18}$$

where T_{in} $(= T_{VCO1}(k) - T_{ref})$ is the time representation of the analog input.

Figure 3.49 shows a block diagram representation of equations (3.17), and (3.18). As we can see in Figure 3.49, the block diagram represents a second order $\Delta\Sigma$ in time domain.

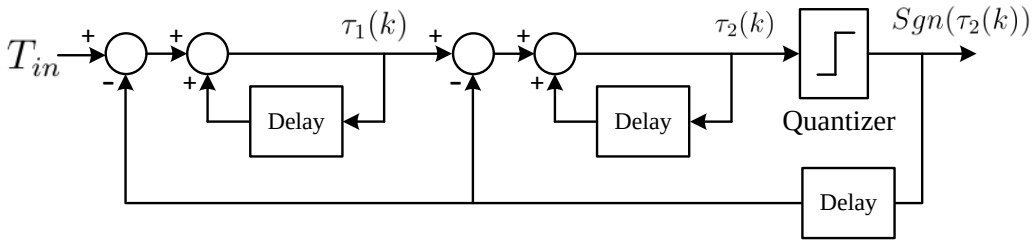

Figure 3.49: The equivalent block diagram of (3.17), and (3.18)

One problem with the system shown in Figure 3.47 is the need of a phase to voltage converter to convert the phase difference $\tau_1(k)$ into voltage to control the period of VCO2. One solution to overcome this problem is to use the gated ring oscillator.

3.7.1.1 Gated Ring Oscillator

Figure 3.50 illustrates the gated ring oscillator (GRO) [42–44]. In GRO, two transistor switches are added to each inverter of the conventional ring oscillator. The NMOS switch and the PMOS switch are controlled by the enables signals E and $\bar{E}$ respectively.

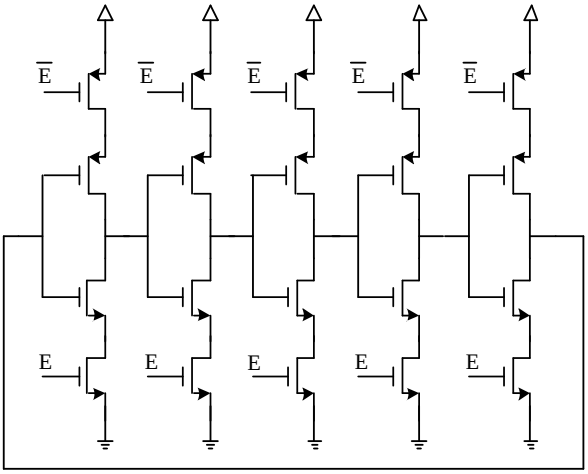

Figure 3.50: The gated ring oscillator

If the switches are closed, E is '1', as shown in Figure 3.51(a), the supply will be connected to the inverters and the ring starts oscillation. On the other hand, if the switches are open, E is '0', as shown in Figure 3.51(b), the paths to V_{dd} and *gnd* will be disconnected and there is no path for the parasitic capacitance, at the output of each inverter, to charge or discharge . This means that when the GRO is not enabled. It will retain the state of the ring just before the enable signal switches from '1' to '0'. When the GRO is enabled again the ring will start oscillating from the last saved state.

3.7.1.2 Second order TADC with GRO

If we replace the dotted box in Figure 3.47, VCO2 and the time to voltage converter, by the GRO, as shown in Figure 3.52, the system becomes time based ADC. A timing interface circuit is needed to control the GRO. The timing inter-

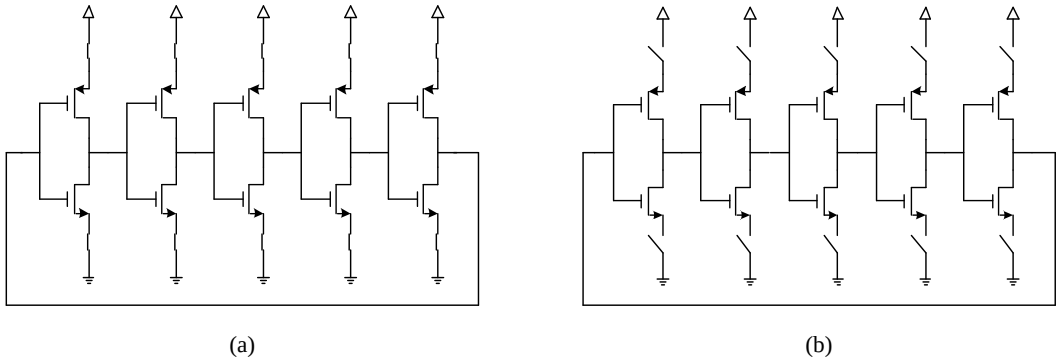

Figure 3.51: (a)GRO is enabled (b)GRO is not enabled

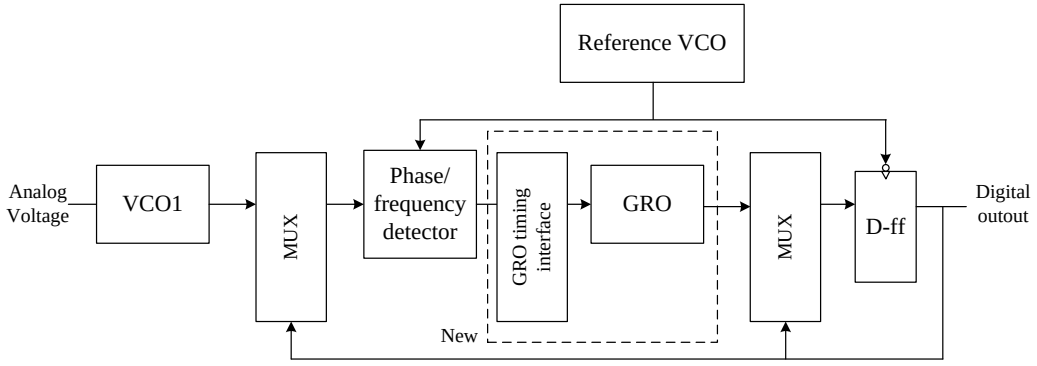

Figure 3.52: The second order system with GRO

face circuit generates the required signal that control the period of the GRO; if the time difference between the manipulated VCO1 edge and the reference edge, $\tau_1(k)$, is positive, the GRO period needs to be increased by $\tau_1(k)$. If we assume that the phase/frequency detector produces logic "1" during the time $\tau_1(k)$, and logic "0" otherwise, then an inverted version of the phase/frequency detector output can be connected directly to the enable control of the GRO. Thus, when the phase/frequency detector output switches to "1", the enable signal of the GRO will switch to "0". This results in freezing the GRO for a duration of $\tau_1(k)$. This will result in increasing the period of the GRO by $\tau_1(k)$.

A problem arises when $\tau_1(k)$ is a negative value. The cause of the problem is that the period of the GRO needs to be decreased. Freezing the GRO will not

result in decreasing the period but, actually, it will result in increasing it. Figure 3.53 shows a solution for this problem. Let us assume that all the GRO outputs are

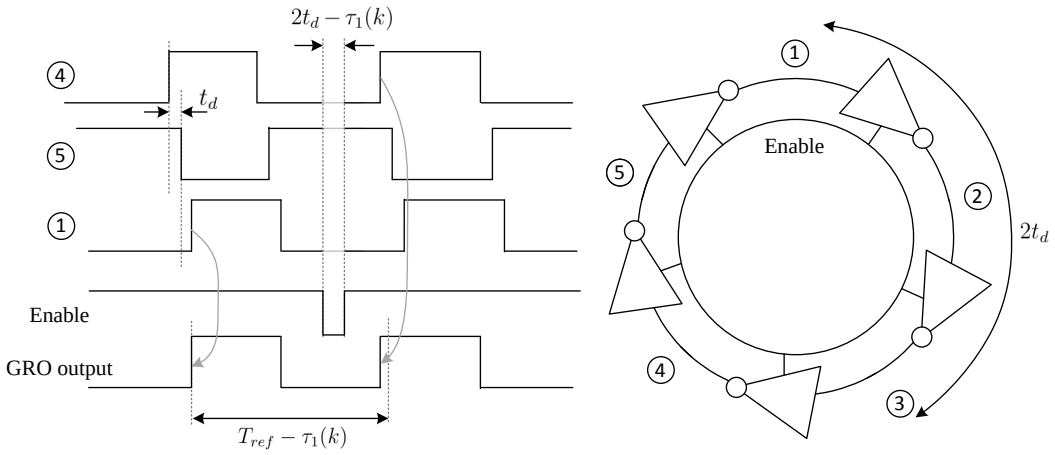

Figure 3.53: The proposed idea to decrease the GRO period

connected to a MUX, not shown in Figure 3.53. Let us also assume that the MUX output is copying from node 1 of the GRO. The first step of the solution is to freeze the GRO for $2t_d - \tau_1(k)$, instead of $\tau_1(k)$, where $2t_d$ is the phase difference between two non-consecutive GRO inverters. The second step is to change the selection control of the MUX such that the MUX output starts copying from node 4 of the GRO. Because the phase difference between node 4 and node 1 is $-2t_d$, the net change to the period of the MUX output is equal to $-\tau_1(k)$ and the period of the MUX output will equal to $T_{ref} - \tau_1(k)$.

3.7.1.3 The phase detector and the timing circuit for the GRO

Figure 3.54 shows a block level diagram of the circuit that does the phase detection and generates the proper signals to control the GRO.

A D-FF is used to quantize $\tau_1(k)$. It produces "1" if $\tau_1(k)$ is positive and "0" if $\tau_1(k)$ is negative. Two delay units are used to delay the shifted version of VCO1 and the reference signal by T_d. The delayed signals are XNORed to provide a pulse signal with a duration that corresponds to the time $\tau_1(k)$. The shifted version of VCO1 is further delayed by $2t_d$ and again is XNORed with the delayed version

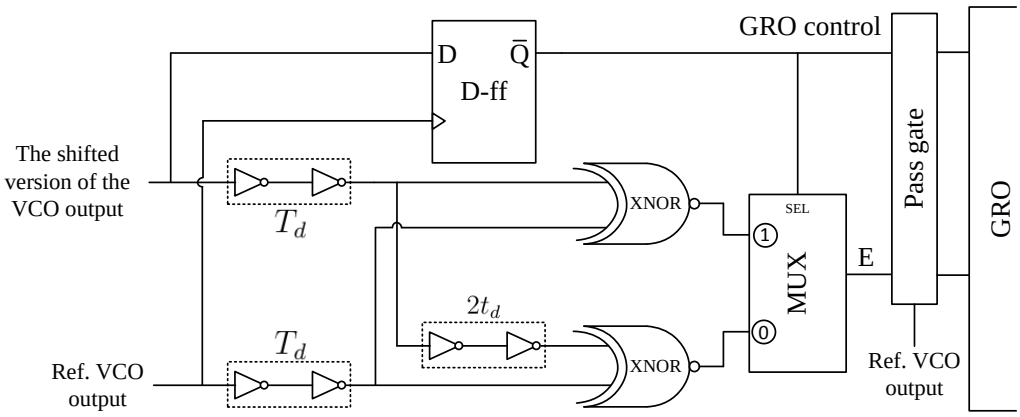

Figure 3.54: The timing circuit for the GRO

of reference signal to generate a pulse signal with a duration that corresponds to the time $2t_d - \tau_1(k)$. The D-FF output is used to determine which output of the two XNOR will be connected to the enable signal of the GRO. This is done by connecting the D-FF output to the selection control of a MUX. The D-FF output is also sent to the GRO to control the selection of GRO MUX output. If D-FF output is "1", the GRO MUX will continue copying from the same GRO node. On the other hand, if D-FF output is "0", the GRO MUX will start copying from a GRO node that leads the current node by $2t_d$.

Figure 3.55 illustrates a waveform of the block diagram shown in Figure 3.54. As we can see from Figure 3.55, the output of the XNOR changes two times during one period of the the reference clock. To allow only one of these two changes, from the XNOR output, to propagate to the enable control of the GRO, and block the other change, a pass gate is used. The pass gate is controlled by the reference clock. If the reference clock is "1", the MUX output will be connected to the enable control of the GRO. If the the reference clock is "0", the MUX output will be disconnected and the enable control will be connected to V_{dd}.

For proper operation of the the timing circuit, the delay T_d must be greater than $max(\tau_1(k))$ + the D-FF delay. This will guarantee that the D-FF output has settled and the suitable path, either the positive or the negative path, is selected and connected to the enable control of the GRO before the output of XNOR gate starts changing. If T_d is less than $max(\tau_1(k))$, the XNOR gate in the negative $\tau_1(k)$

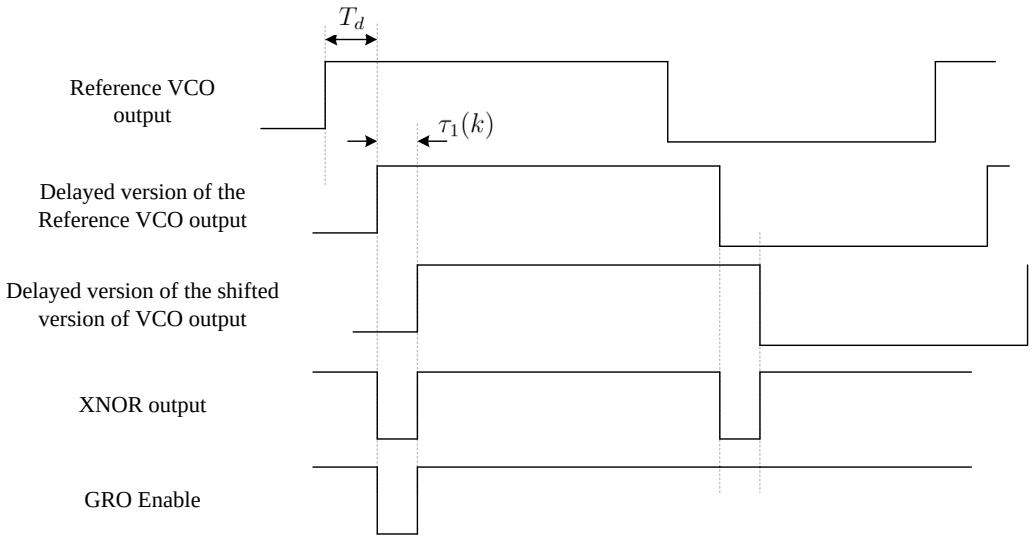

Figure 3.55: Waveform of timing circuit for the GRO, only one GRO enable pulse per period

path may change its output before the pass gate is properly controlled.

3.7.2 Simulation results

The goal this time is to build a TADC that can achieve 12bit resolution for 20MHz bandwidth. Figure 3.56 shows the FFT of the digital output of the second order TADC . The input frequency is $10MHz$ and the reference frequency is $1GHz$. As we can see from Figure 3.56, the distortion level is about $72db$. For the quantization noise, the level of the noise floor is about 140db below the peak value. Thus, the SNR of the TADC is $75db$ for a bandwidth of 20MHz. This means that the resolution of TADC is $12bit$. Thus, the proposed second-order TADC achieves the required resolution, 12bit, for 20MHz bandwidth. Figure 3.57 shows SNDR as function of the input signal amplitude.

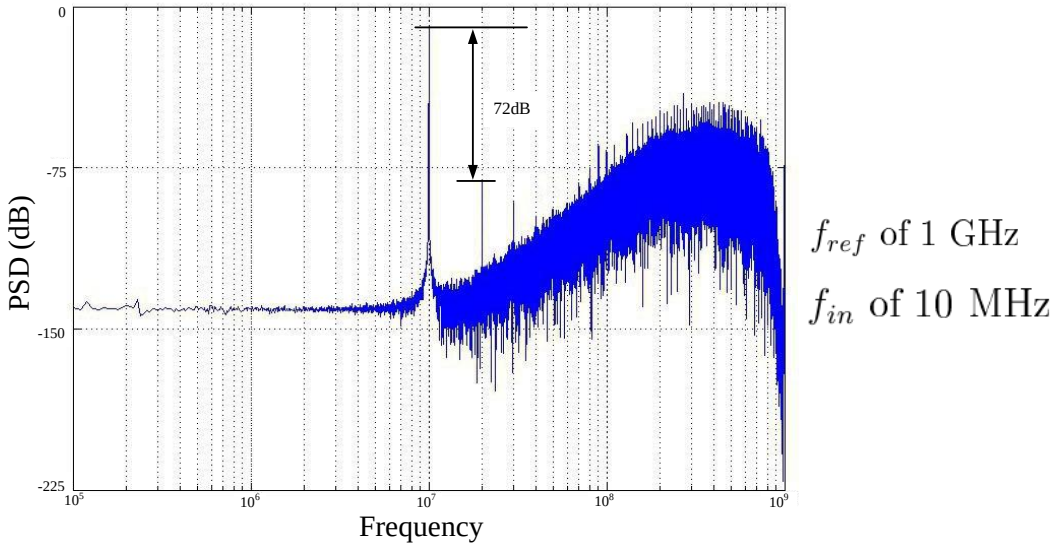

Figure 3.56: FFT of the output of the second order system

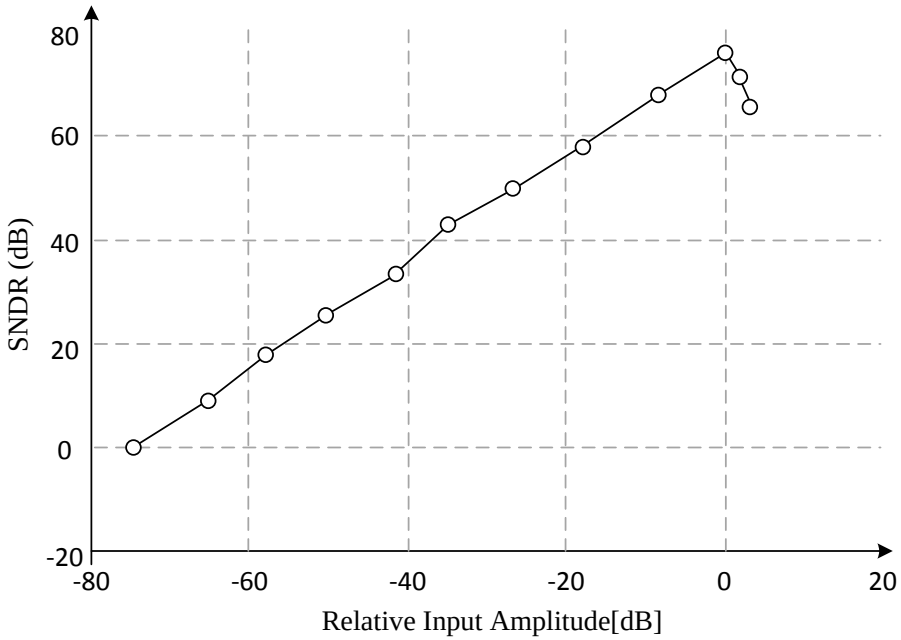

Figure 3.57: system level simulation SNDR as function of signal amplitude, 10% mismatch is included

Chapter 4

TRANSISTOR LEVEL SIMULATIONS, FABRICATION, AND TESTING

In this chapter, schematics and layouts of the TADCs will be presented. The results of transistor level simulations, that prove the functionality of these TADCs, using Cadance and Eldo will be illustrated. Target technology is 0.13μm CMOS. The design of the PCBs that have been used in testing will be also presented.

4.1 Design I: First-order $\Sigma\Delta$ modulator, phase interpolation incorporated

4.1.1 Transistor-level simulation

To prove the functionality of the proposed TADC, a complete system is designed and transistor level simulations are done using Cadanc and Eldo.

In the first design step, the sampler is simulated to obtain the characteristic curve that relates the input voltage to the delay of the sampler. Figure 4.1 shows the sampler characteristic curve. The input voltage range is $500mV$ (from $0.7V$ to $1.2V$) and the maximum change in the sampler delay that corresponds to the input voltage range is $125.8ps$. As we can see from Figure 4.1, the characteristic curve

is not linear and multibit non-linear quantizer is needed to generate the piecewise linear curve that approximates it. To achieve 12 bit resolution, the maximum INL must be less than 1LSB at the 12 bit level. For the non-linear curve under consideration, which is roughly hyperbolic, and within the input range, i.e. $500mv$, to achieve 12 bit INL, an 8 segment piecewise linear approximation is used.

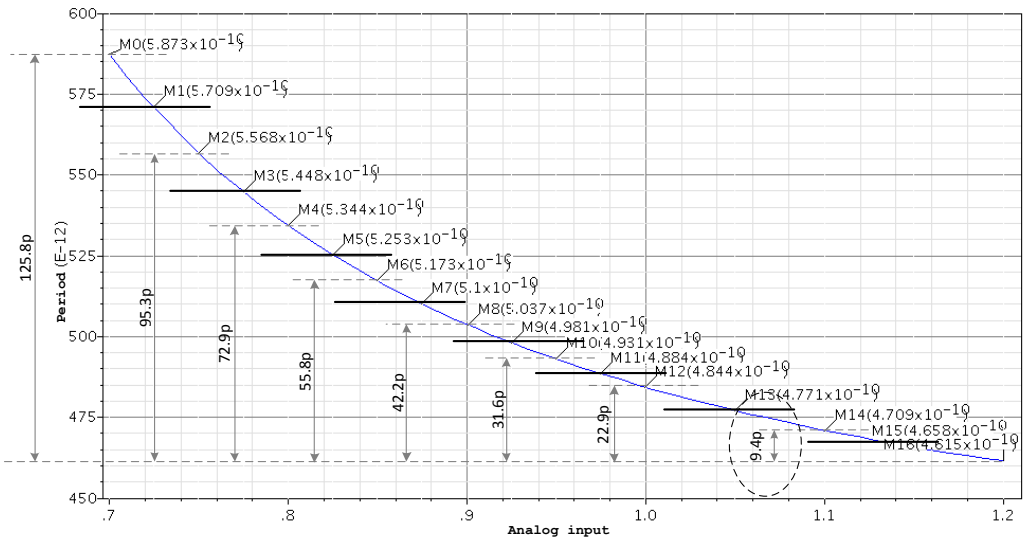

Figure 4.1: The non-linear characteristic curve of the VCO sampler

As mentioned in section 3.5.3.1, PI is used to generate time edges for both comparison (in internal quantizer) and feedback (internal DAC). To generate the required feedback edges, the gray dotted horizontal lines in Figure 4.1, a 1-level phase interpolator with 5 inputs is used. Figure 4.2 shows the circuit schematic of the phase interpolator (for illustration purpose 1-level with 2-inputs are shown). The top set of transistors are for buffering while the lower set of transistors are responsible for doing the PI. The relative size ratios of the inverters in the lower set are adjusted to set the phase differences, between the generated signals, to the required values.

Figure 4.3 illustrates the output of the phase interploator. From Figure 4.3, the phase difference between the generated signals is equal to the required values. As an example, the smallest time division, 9.4 ps (in dotted line), required in Figure 4.1, is generated in Figure 4.3 (9.4 ps, in dotted line).

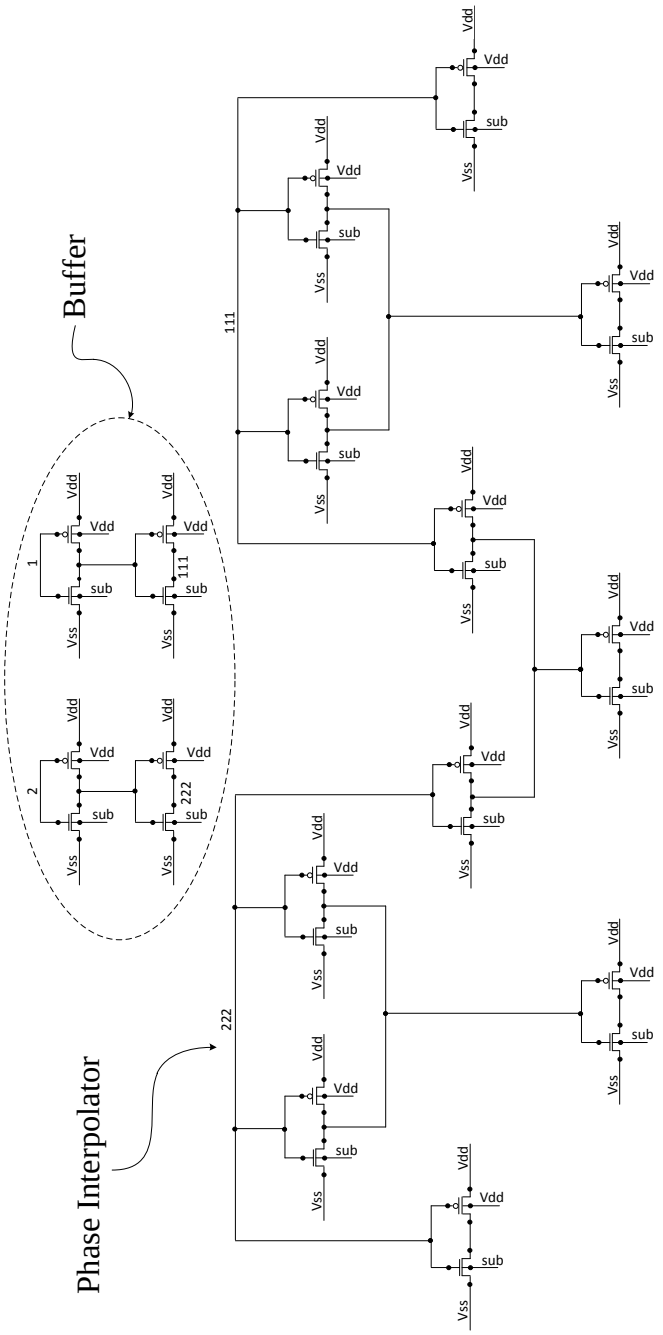

Figure 4.2: Schematic of the phase interpolator

Figure 4.4 shows the monte-carlo simulation on the output of the phase interploator. As we can see from Figure 4.4, the standard deviation is less than 0.1%.

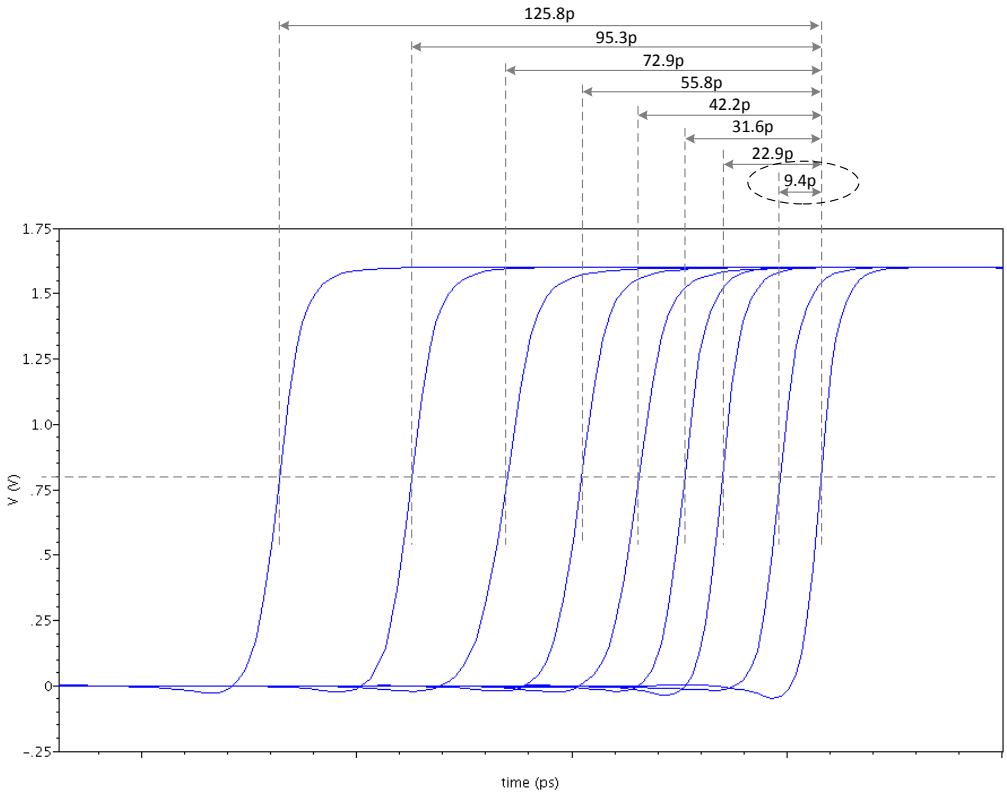

Figure 4.3: The output of the phase interploator

This means that the phase interpolator works under different process corners. it should be noted that the locations of the generated edges are controlled by the ratio of sizes of the inverters, and do not depend on the size of one inverter. Thus, for different corners, even if the inverter parameters changes the ratio will be almost the same.

Figure 4.5 shows the circuit schematic of the MUX control circuit. The definition/function of each signal is given in Table 4.1. As discussed in Section 3.5.3.1, the MUX output copies one of its inputs, according to the value of the TADC digital output i.e. feedback signals that select/control the MUX. This means both rising and falling edges are copied. However, as discussed in section 3.5.4, for the proper operation of the TADC, the MUX output should copy only the rising edge. As TADC digital output changes, the falling edge that should be passed to the MUX output should be kept the same. This is done by NANDing all the control signals,

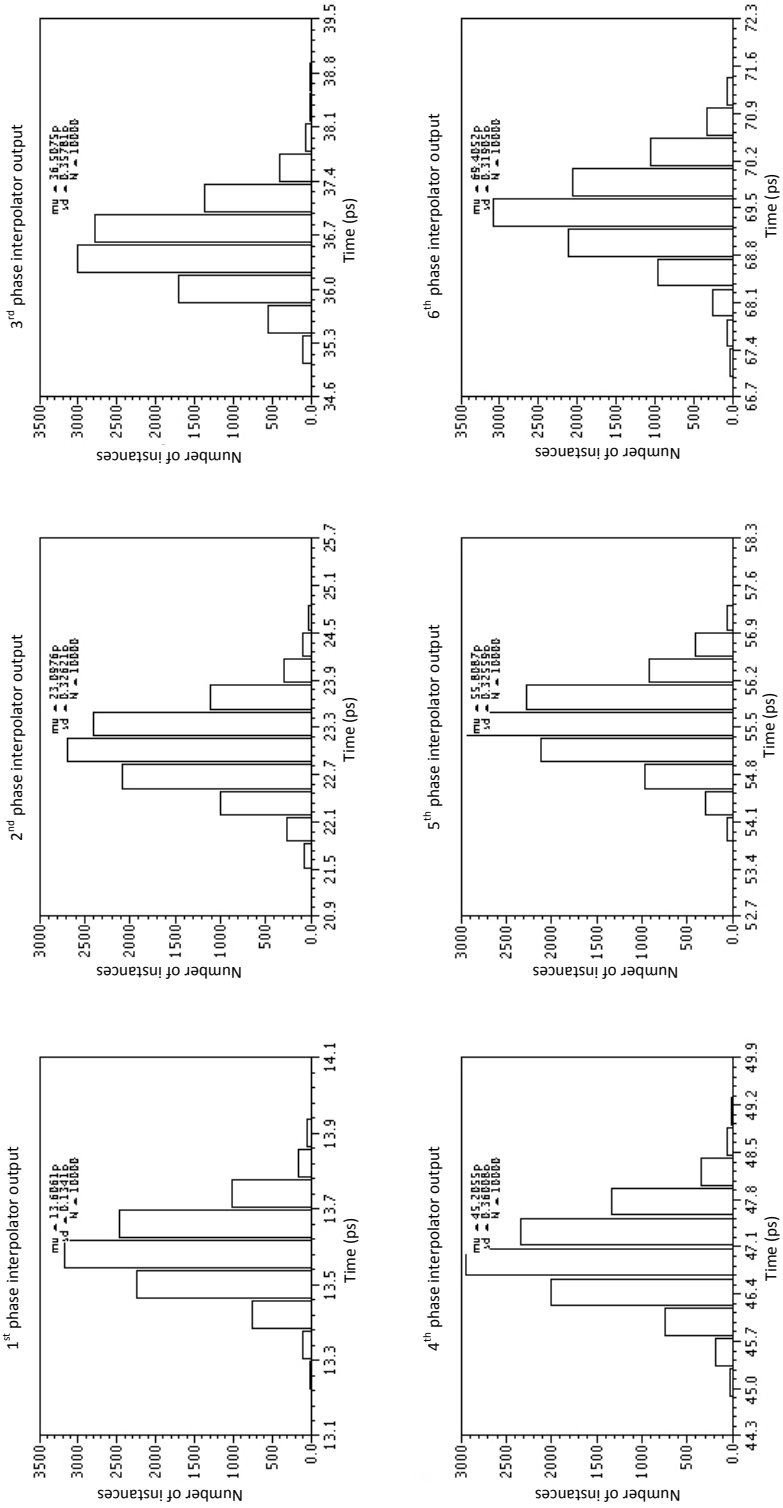

Figure 4.4: Monte-carlo simulations on the output of the phase interploator, 0.1% standard deviation

except one, with the output of the VCO, signal "f" in Figure 4.6. The remaining control signal is NORed with the inverted version of the output of the VCO, signal "f_bar" in Figure 4.6. By doing this the NANDed control signals will be effective only during one half of the period of the VCO. The output of the NAND and NOR gates are used to control a group of transmission gates. Each transmission gate is connected to one of the phase interpolator outputs. When a transmission gate is enabled, the phase interpolator output that is connected to this transmission gate will propagate and trigger the next VCO inverter.

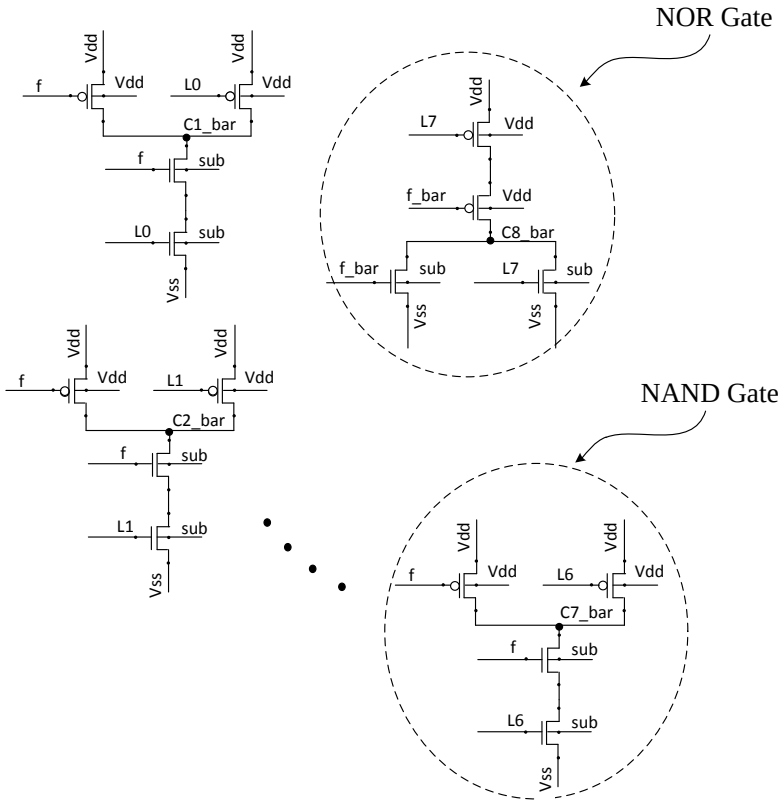

Figure 4.5: Schematic of the MUX control circuit

Figure 4.6 shows the circuit schematic of the whole VCO with PI. Simulations show that the period of the VCO is 1ns for any pair of the analog voltage and feedback digital code shown in Table 4.2.

To generate the required comparison edges, the solid horizontal lines in Figure 4.1, another phase interpolator is used. The relative size ratios of the inverters

Table 4.1: Definitions of symbols used in Figure 4.5

Name	abbreviation	function
VCO output (shown in Figure 4.6)	f	Allows the feedback signals to affect the MUX during the on period of the VCO
Inverted version of the VCO output (shown in Figure 4.6)	f_bar	Forces the MUX to copy the same falling edge regardless the values of the feedback signals
TADC output signals	L0 - L8	MUX control signals
MUX Internal signals	C1_bar - C9_bar	Control the MUX switches

Table 4.2: Analog values and feedback codes that result in $1ns$ VCO period

Analog voltage	Digital code L0-L8
1.2	000000001
1.1	000000010
1.0	000000100
0.95	000001000
0.9	000010000
0.85	000100000
0.8	001000000
0.75	010000000
0.7	100000000

are again adjusted to set the time difference between the generated signals to the required values. Figure 4.7 illustrates the output of the phase interpolator of the reference phase generator.

Figure 4.8 shows the block diagram of the whole TADC. Two identical VCO implementations are used for input and reference VCO. The input VCO is connected to the analog input voltage and its MUX control signals are connected to the digital outputs of the TADC. The reference VCO is connected to the reference voltage ($1.2V$ in this design), and its MUX control signals are connected to a fixed digital

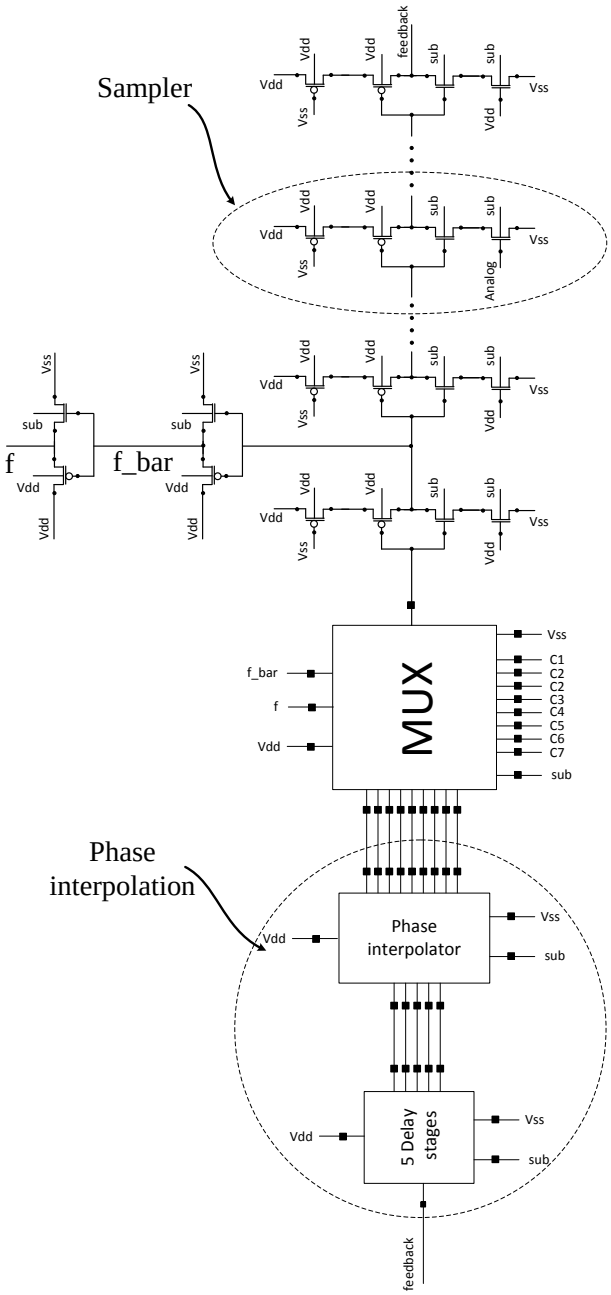

Figure 4.6: Schematic of the VCO with PI

code "000000001". This results in a reference period of $1ns$. The output of the input VCO is connected to the data input of all the D-FFs in the quantizer. The clock input, CLK, of each D-FF is connected to one of the reference signals, CLK1-

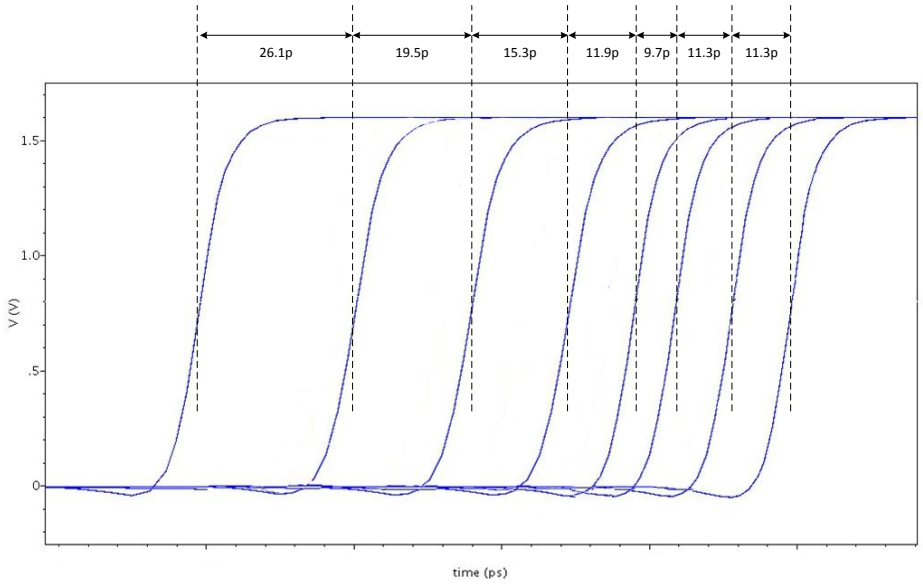

Figure 4.7: The output of the phase interpolator of the reference phase generator

CLK8, generated from the the reference signal generator.

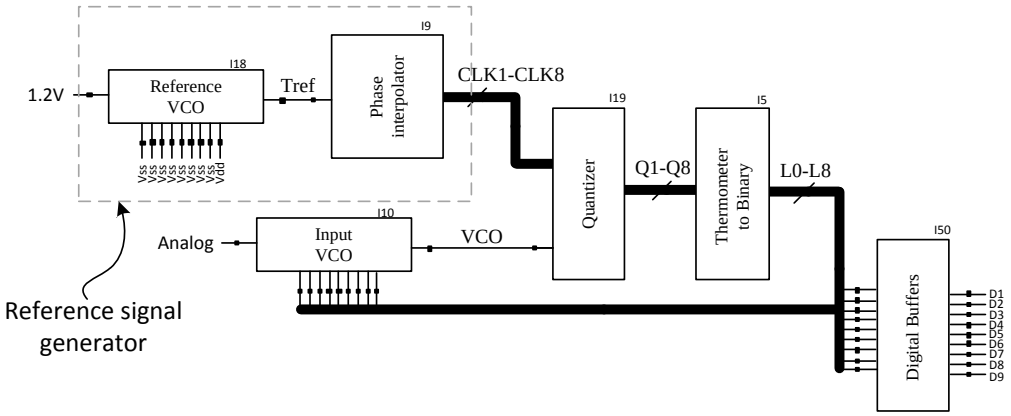

Figure 4.8: Schematic of the TADC

Thermometer to on/off binary (T2B) code converter is needed to convert the thermometer code generated by the D-FFs, in the quantizer, into a on/off digital code that can drive the MUX control circuit. The T2B passes only the most significant "1" in the D-FFs output code e.g if the D-FFs output code is "00001111", the

T2B output will be "000010000". However, if all the D-FFs outputs are "00000000", the T2B output will be "000000001".

4.1.2 Timing Jitter

In this section, we briefly review the timing jitter [45–50]. We investigate how the timing jitter limits the performance of the VCO. Noise introduces timing uncertainty in the moment when the inverter output voltage crosses the threshold voltage of the next inverter in the VCO, or timing jitter σ_t. In our analysis, we assume that the inverter output crosses the threshold only one time, which means we calculate the jitter for the first passage time [47,48]. Moreover, thermal noise is the only noise source assumed is this section.

For a VCO consisting of 2-transistor inverters, if the output voltage of an inverter, V_C, crosses the threshold voltage of the next inverter, V_{th}, before crossing the saturation/triode barrier, $V_{(sat/triode)}$, as shown in Figure 4.9, the jitter can be calculating using the formula [45]

$$\sigma_t^2 = \frac{1}{2}\frac{\bar{t}_{V_{th}} S_{i_n}/C_L^2}{SR^2} \tag{4.1}$$

where C_L is the loading capacitor at the output node of the inverter, SR is the slew rate and it is defined as the ratio between the mean of the discharging (or charging) current and C_L. $\bar{t}_{V_{th}}$ is the mean value of the time needed for V_C to cross V_{th} and it is equal to b/SR. b is the barrier value (shown in Figure 4.9). S_{i_n} is the power spectral density of the noise in discharging (or charging) current and is equal to $4kT\gamma g_m$. γ, is the excess noise factor due to short channel effect, and g_m is transconductance of transistor.

However, as technology scales, and supply voltage reduced, transistor goes into triode more often. Thus, if V_C crosses $V_{(sat/triode)}$ before crossing V_{th}, then σ_t is given by [50]

$$\sigma_t = \sqrt{\sigma_{t_1}^2 + \sigma_{t_2}^2} \tag{4.2}$$

where σ_{t_1} is the jitter when the inverter output voltage crosses $V_{(sat/triode)}$ (at time t_1 in Figure 4.10), and σ_{t_2} is the additional jitter when the inverter output voltage crosses V_{th} (at time $t_{V_{th}}$ in Figure 4.10). Both σ_{t_1} and σ_{t_2} are again calculated using equation (4.1). Substitute in equation (4.2), σ_t can be written as

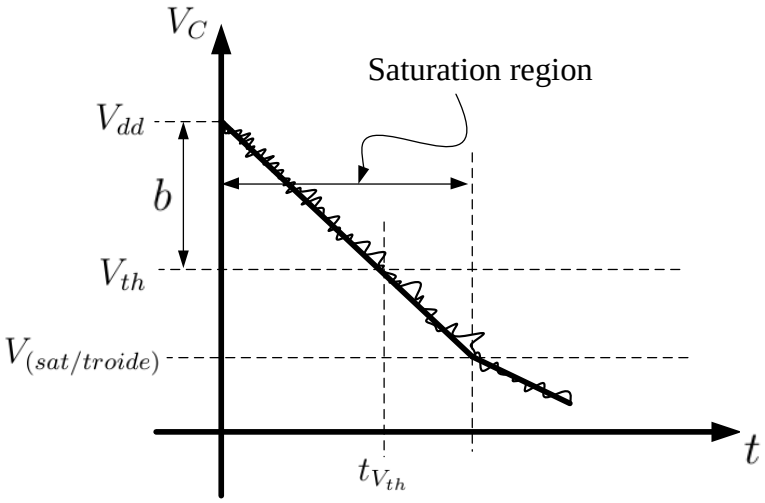

Figure 4.9: Timing jitter when V_{th} is greater than $V_{(sat/troide)}$

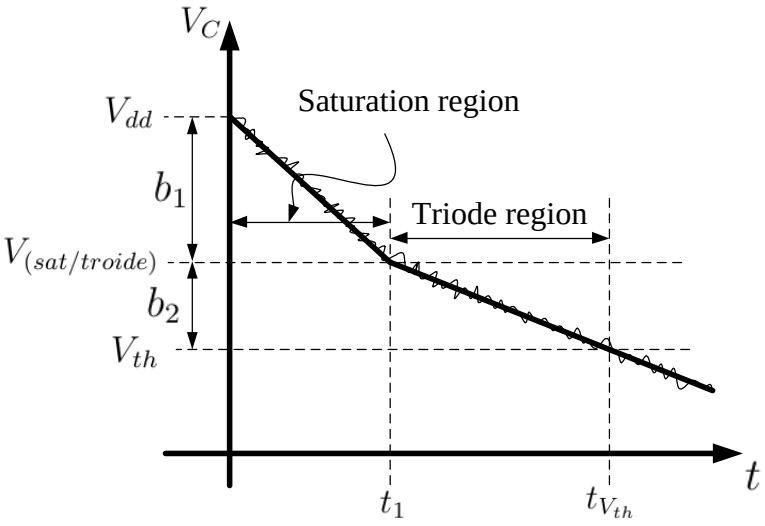

Figure 4.10: Timing jitter when V_{th} is smaller than $V_{(sat/triode)}$

$$\sigma_t = \frac{1}{\sqrt{2}}\sqrt{\frac{b_1 S_{i_{n_1}} C_L}{\bar{I}_{sat}^3} + \frac{b_2 S_{i_{n_2}} C_L}{\bar{I}_{tri}^3}} \tag{4.3}$$

where $\bar{I}_{sat}$ and $\bar{I}_{tri}$ are the mean values of the current in the saturation and triode

region, respectively. If the VCO consists of N stages and by assuming that the jitter caused by the NMOS and PMOS transistors are the same, the total jitter in the VCO period, σ_{VCO}, will be given by

$$\sigma_{VCO} = \sqrt{2N} \times \sigma_t \tag{4.4}$$

For the design under consideration, the VCO consists of 11 delay cells, the sampler, and the phase interpolator. All these components contribute to the total timing jitter of the VCO period. Each of the delay cells is a 4-transistor inverter (redrawn in Figure 4.11). Because M_0 and M_3 are connected to V_{ss} and V_{dd}, respectively, they will operate in the triode region all the time before V_C crosses V_{th}. During the discharging phase of C_L, V_C starts at V_{dd} (that is 1.6V in this design) and V_P starts at V_{th} (that is 0.8V in this design). This result in making M_2 to operate in the saturation region. Eventually, as V_C decreases and V_P increases, M_2 will change its region of operation and start operating in the triode region before crossing V_{th}. Thus, V_C will follow the pattern in Figure 4.10 and $\sigma_{t_{delay\ cell}}$ is given by equation (4.3). The same situation holds for M_1, during the charging phase of C_L. For simplicity, we assume that the timing jitter for both the charging and discharging phases are equal. Thus, the total timing jitter contribution of the 11 delay cells, $\sigma_{t_{11\ delay\ cell}}$, will be given by

$$\sigma_{t_{11\ delay\ cell}} = \sqrt{22} \times \sigma_{t_{delay\ cell}} \tag{4.5}$$

To estimate the bound on the timing jitter generated from the sampler, the case when analog input voltage is at its minimum will be studied. This gives a bound, because the discharging current is at its minimum. This results in making the slope of inverter output voltage minimum. Thus, the noise current from discharging transistors flows for the longest time onto the load capacitor (the parasitic capacitor at the output of the sampler), thereby depositing the largest amount of noise. Notice from [47, 48], since σ_t increases as the amount of noise deposited increases and as the slope of inverter output voltage decreases, the present situation gives the worst case. This then gives the bound on the timing jitter generated from the sampler. As the sampler structure is the same as the delay cell except that the gate of the lowest transistor (M_3 in Figure 4.11) is connected V_{in}, instead of V_{dd}, the lowest transistor will not continue to operate in the triode region during the discharging

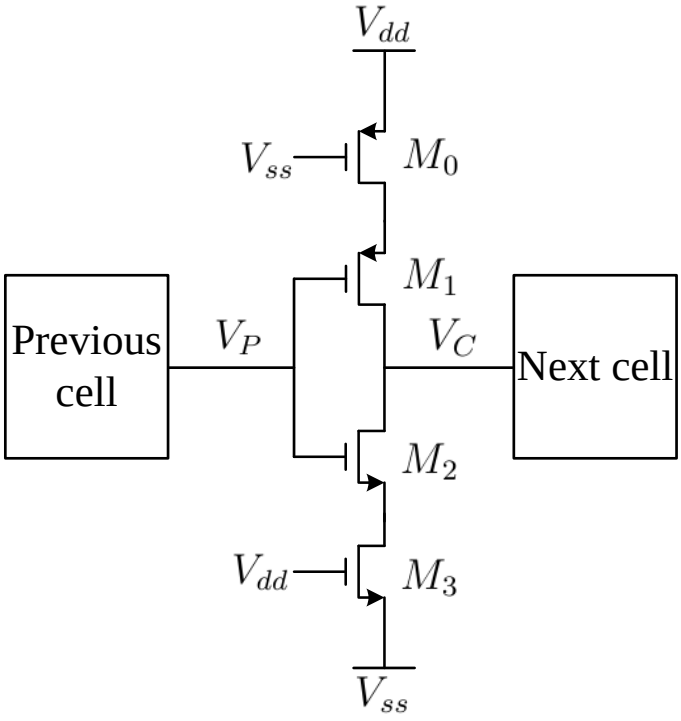

Figure 4.11: the 4-transistor inverter

of the load capacitor. It will start operating in triode and eventually it will operate in the saturation region. This means that V_C will have two break points and the timing jitter of the sampler discharging phase, $\sigma_{t_{sampler\ discharge}}$, will be the sum of three components. For the charging phase, the sampler will act exactly like a delay cell because the top transistor is also connected to V_{ss}. Thus, the total timing jitter generated form the sampler,$\sigma_{t_{sampler}}$, is given by

$$\sigma_{t_{sampler}} = \sqrt{\sigma^2_{t_{sampler\ discharge}} + \sigma^2_{t_{delay\ cell}}} \tag{4.6}$$

For the phase interpolator, the inputs are fed into 2-stage buffer and each of its output edges is generated by connecting the output of two inverters again to 2-stage buffer. Thus, the total timing jitter generated from the phase interpolator, $\sigma_{t_{phase\ interpolator}}$, will be the summation of all the timing jitter of all theses inverters

$$\sigma_{t_{phase\ interpolator}} = \sqrt{2\sigma^2_{t_{buffer}} + 2\sigma^2_{t_{PI\ inverter}}} \tag{4.7}$$

Summing all the contributions from the 11 delay cells, the sampler, and the phase interpolator will result in the total timing jitter in the VCO period, $\sigma_{t_{VCO}}$

$$\sigma_{t_{VCO}} = \sqrt{\sigma^2_{t_{11\ \ delay\ \ cell}} + \sigma^2_{t_{sampler}} + \sigma^2_{t_{phase\ \ interpolator}}} \tag{4.8}$$

The values of the current, load capacitor, and g_m have been obtained from simulations. By substituting in equation (4.8), this results in $\sigma_{t_{VCO}}$ of 2ps. Simulation is done using Eldo to measure the timing jitter of the VCO period. Figure 4.12 shows that the timing jitter is about $2.2ps$. The 10% differnce between the theoretical and simulated value is due primarily to the simplified assumption and the MUX contribution that has been ignored in the theoretical calculations.

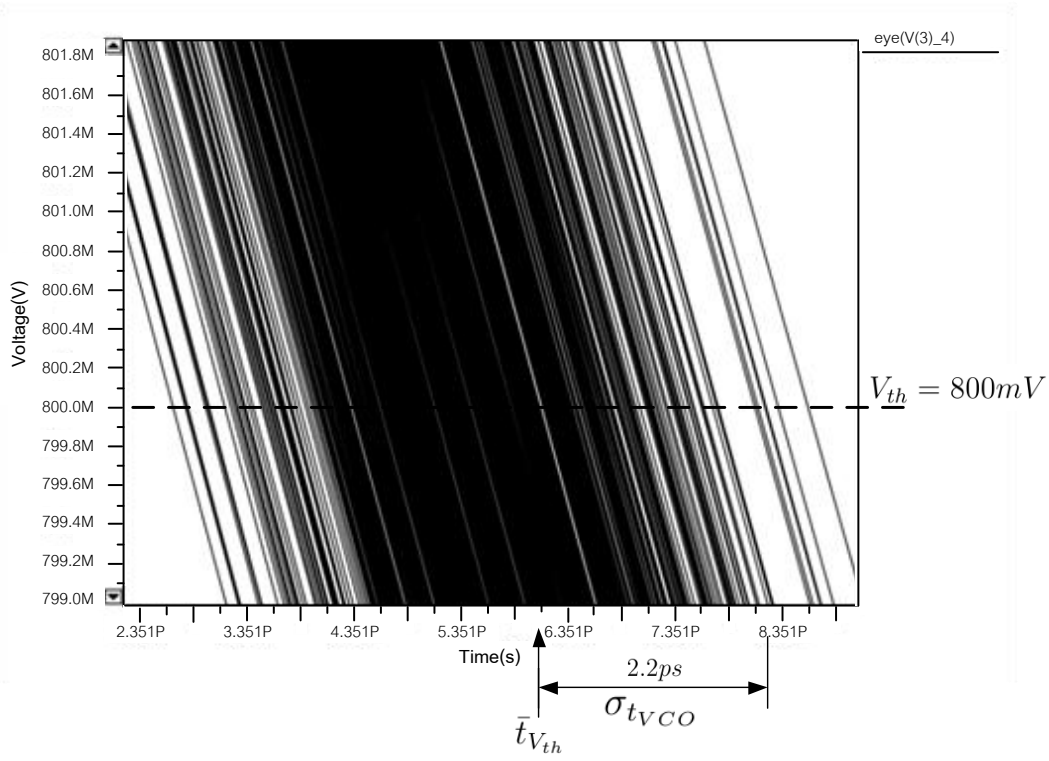

Figure 4.12: Eldo simulation for the timing jitter

4.1.3 Power consumption

To calculate the total power consumption of the TADC, all the TADC sub-modules have been connected to a single voltage supply, V_{dd}. The supplied current, $I_{supplied}$ driven from the voltage supply, has been obtained. The average power is calculating using the formula

$$P_{av} = \frac{1}{T_{sim}} \int_{T_{sim}} V_{dd} \times I_{supplied}\, dt \tag{4.9}$$

where V_{dd} is $1.6V$, and T_{sim} is the simulation time and it is equal to $100\mu s$ (100 period of the input voltage signal whose frequency is 1MHz). The average power consumed by the TADC is 25mW.

4.1.4 Layout

The TADC, shown in Figure 4.13, occupies an area of $100\mu m \times 480\mu m$, excluding the pads. Separate supply and ground pins are provided for the analog, digital portions of the chip. The analog supply is used for providing power to the sampler of the TADC. The rest of the core blocks are powered by the digital supply. The reference voltage are provided off chip for better testability.

In the layout, double diodes are used to act as electrostatic discharge (ESD) protection and the guard rings are used to improve the system robustness against the latchup.

4.1.5 PCB design

A 2-layer FR4 PCB, shown in Figure 4.14, is designed to test the prototype TADC. The PCB routing is done such that 100% of the bottom layer is used as a ground plane to provide a good current return path. $0.1\mu F$ and $10\mu F$ surface-mounted decoupling capacitors are used at all the supply pins.

4.1.6 Testing

After doing the post-layout simulation of the TADC using Cadane and verifying its functionality, the TADC has been fabricated through Canadian Microelectronics

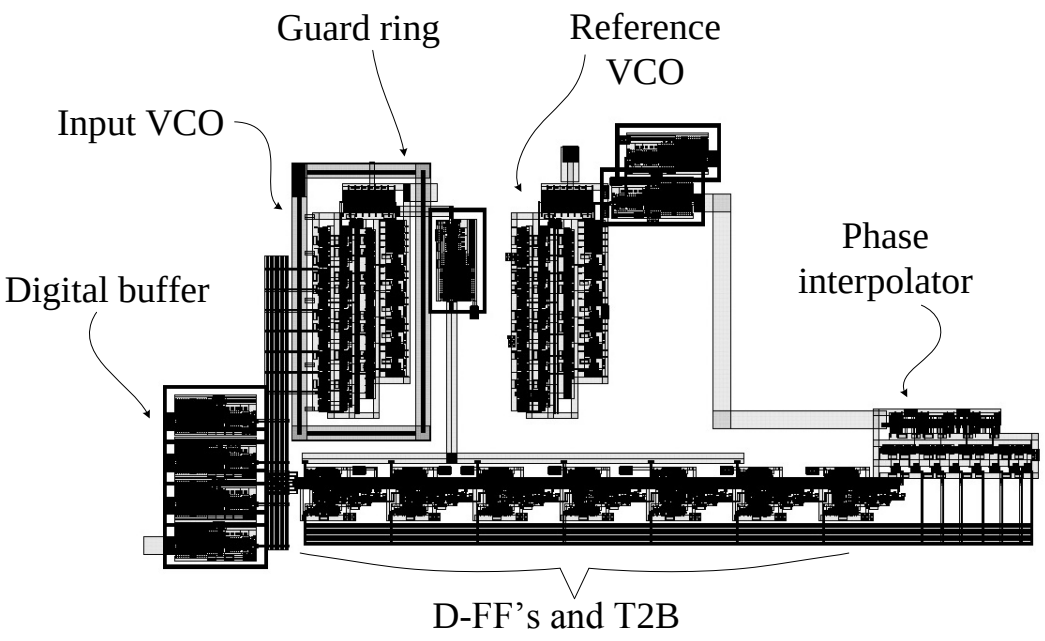

Figure 4.13: The layout of the core TADC

Cooperation (CMC). Figure 4.15 shows the testing setup used to test the TADC. The chip is packaged in a surface-mounted 44-pin CQFP package, and is soldered on the PCB.

Figure 4.16 shows the output of the reference VCO. The measured reference period is 2.728ns. This measured reference period is about 1% different from the value obtained from the post-layout simulation. The math function in Tektronix DSA70404B is used to display a square wave that has the same frequency as that of the reference VCO output. This is done by setting a threshold level, that is 0.8V here. The Tektronix output, M1 in Figure 4.16, is high if the reference VCO output is higher than the threshold level, otherwise it is low. This display method simplify the time domain analysis of the TADC.

The testing is started by applying DC values to the input of the TADC. Figures 4.17, 4.18, and 4.19 show examples of the output of the TADC's D-FF, that corresponds to the lowest comparison level, for different values of the analog input voltage. For Figures 4.17, the input DC voltage is 1.195V close to the highest amplitude (lowest time equivalent) value of 1.2V. As we can see, the D-FF output is mostly 0 because we are close to the lowest time input equivalent. For Figures 4.18,

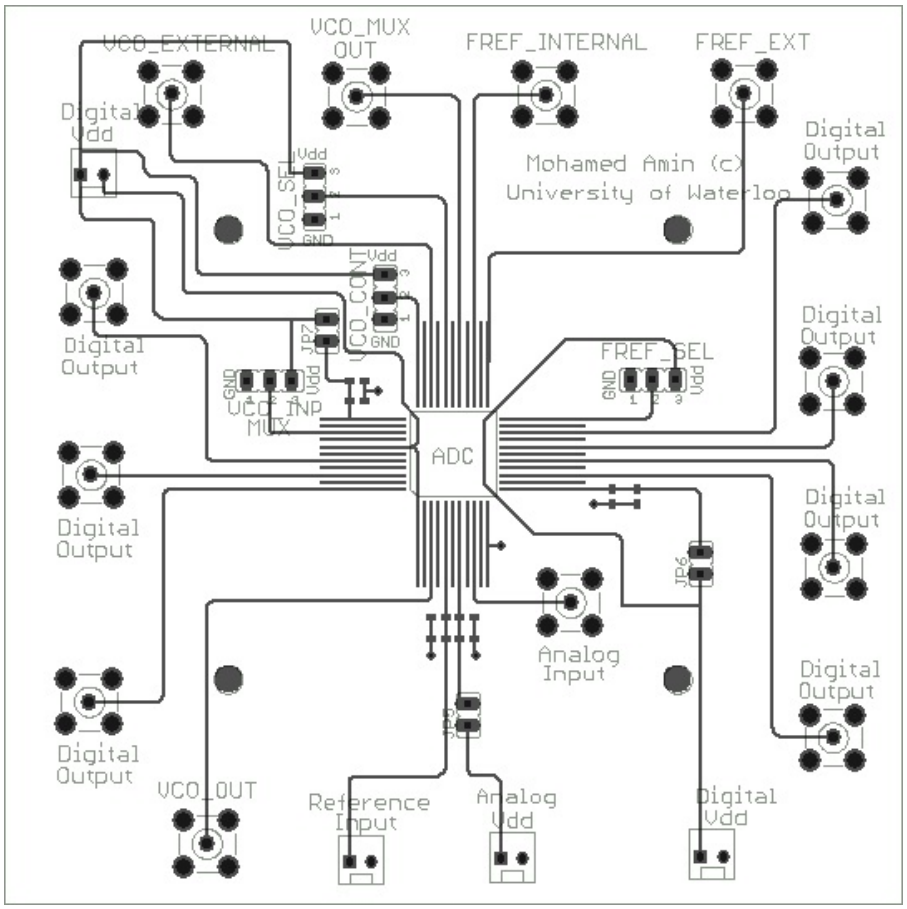

Figure 4.14: The top view of the PCB used to test design I

the input DC voltage is 1.151V. As we can see, the D-FF output is roughly half in 1 and half in 0 because the analog input value is close to 1.15V (the mid-point between 1.1 and 1.2). Finally, for Figures 4.19, the input DC voltage is 1.107V(close to 1.1). As we can see, the D-FF output is mostly 1.

After using the DC signals to check the functionality of the system, a sinusoidal signal is applied to the input of the TADC to measure its performance. Figure 4.20 illustrates the output of the lowest three D-FFs of the TADC when a 1 MHz 250mV (from 0.95V to 1.2V) sine wave is connected to the input of the TADC. As we can see from Figure 4.20, the TADC output toggles between two output values that sandwich the analog input and tracks the input voltage value. Again the math function in Tektronix DSA70404B is used to combine all the 4 chip outputs into one graph. For illustration purpose, a sinusoidal curve has been drawn, in dotted

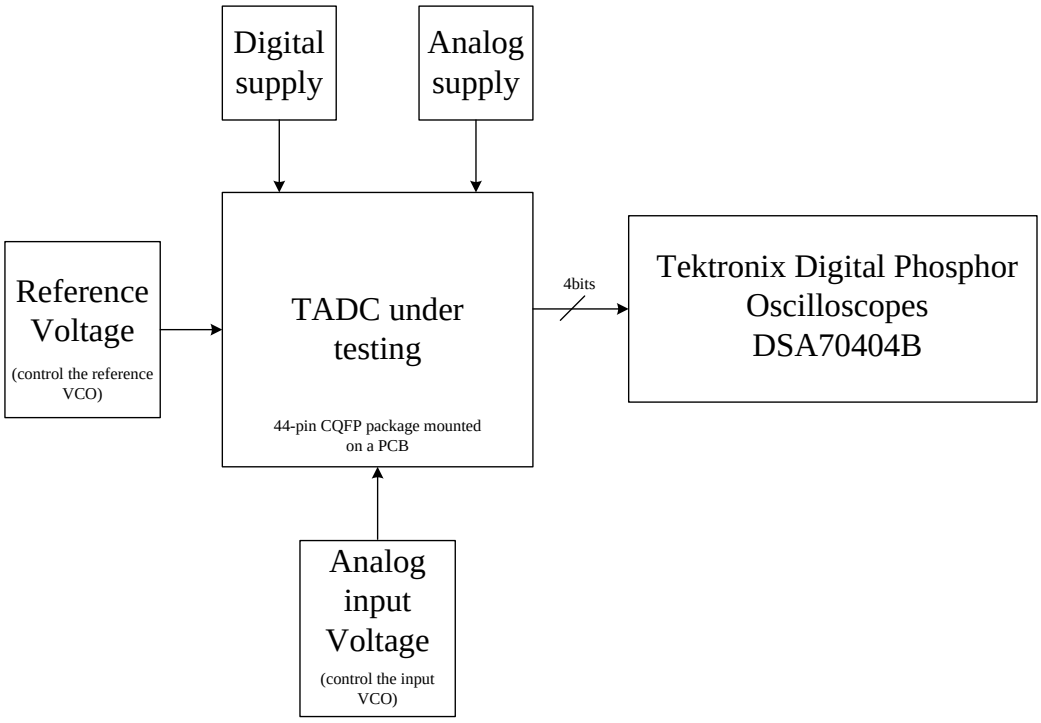

Figure 4.15: Testing setup for design I

line, in Figures 4.20.

FFT has been performed on the signal shown in Figure 4.20. Figures 4.21, and 4.22 show the result. Figure 4.21 shows the noise shaping at the output of the TADC. Figure 4.22 is a zoom in version, in the 0.5-5.5MHz range, of Figure 4.21. Figure 4.22 shows that the peak SNDR is about 61dB. This is an improvement from the 3bit in Figure 3.28, where no non-linear multibit internal quantizer has been introduced to compensate for APC non-linearity. Figure 4.23 shows SNDR as function of the input signal amplitude. The dynamic range is 66dB or 11bit. Thus, the fabricated TADC achieves 10bit resolution for 2MHz bandwidth.

The difference in the distortion levels between Figure 4.22 and Figure 3.31 is due to the fact that the block digram simulation does not take into consideration the process variation. The process variation cases the deviation between the VCO characteristic curve and the internal quantizer curve to be more than 12 bit resolution. This results in increasing the distortion level.

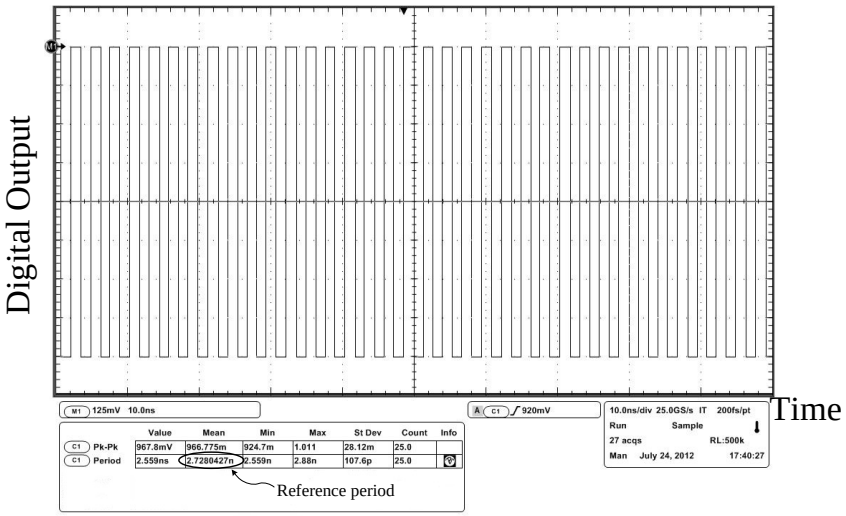

Figure 4.16: The output of the reference VCO

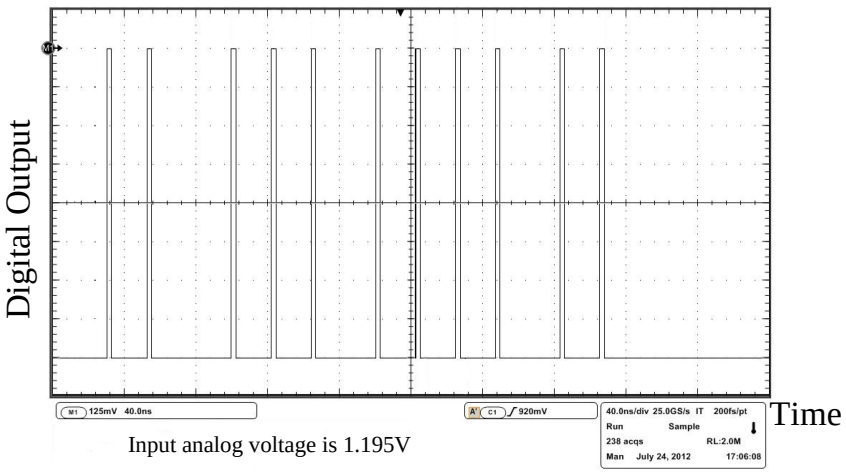

Figure 4.17: Examples of the output of the TADC's D-FF when $V_{in} = 1.195V$

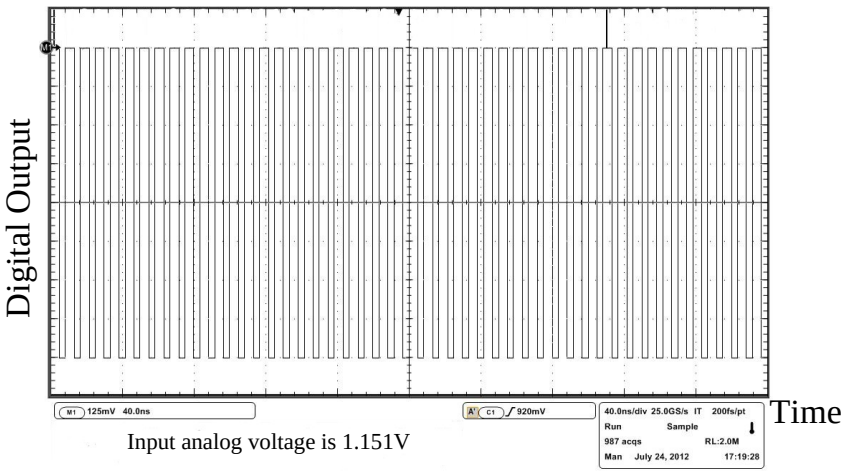

Figure 4.18: Examples of the output of the TADC's D-FF when $V_{in} = 1.151V$

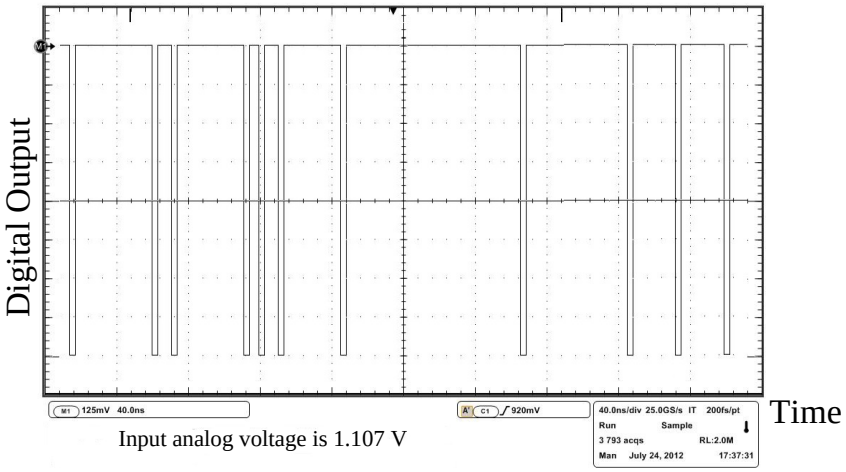

Figure 4.19: Examples of the output of the TADC's D-FF when $V_{in} = 1.107V$

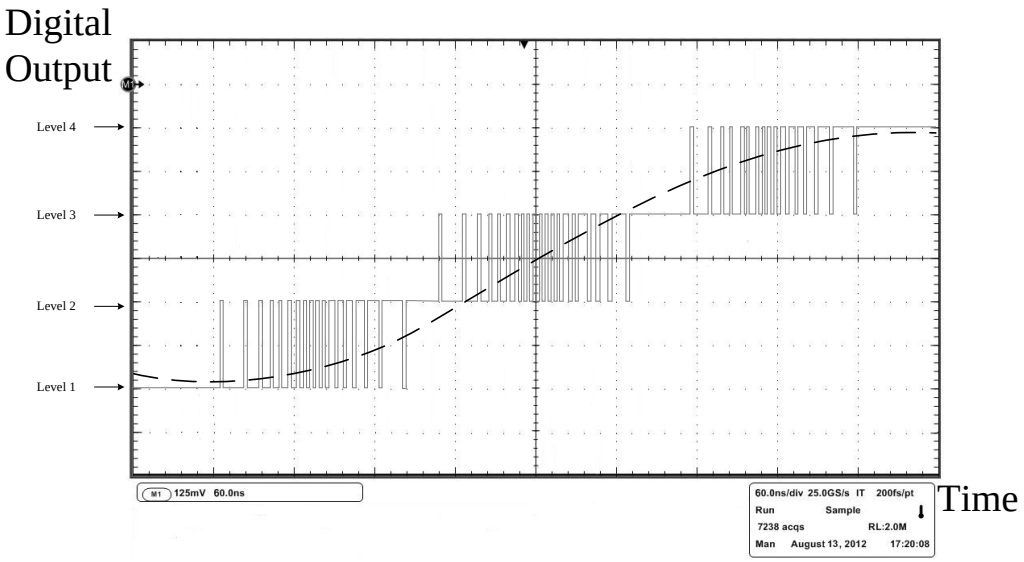

Figure 4.20: The output of the TADC for a sinusoidal input signal

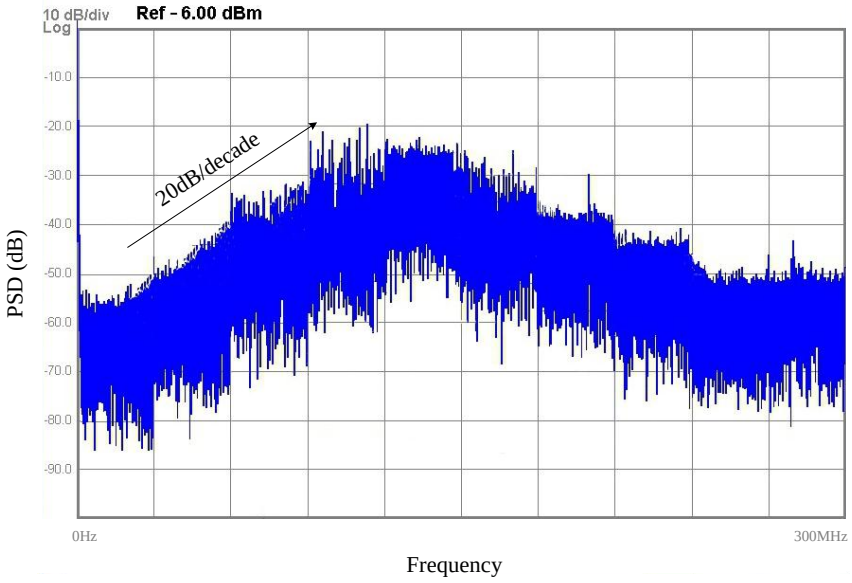

Figure 4.21: 2^{19} point FFT of the signal shown in Figures 4.20

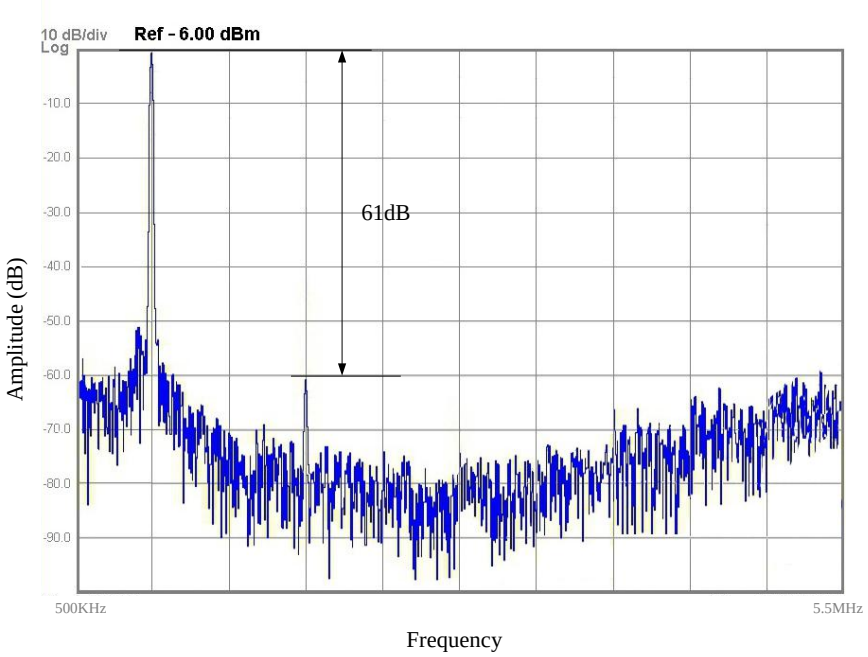

Figure 4.22: A zoom in version of Figure 4.21

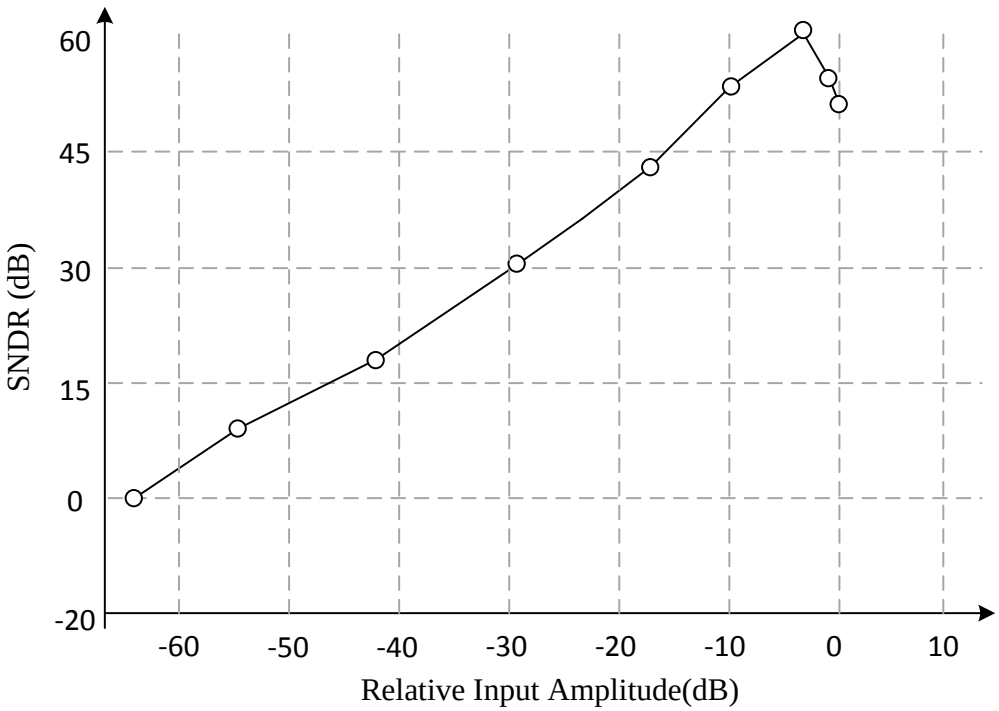

Figure 4.23: SNDR as function of signal amplitude

4.2 Design II: First order ΣΔ modulator, PI, and Dynamic element matching incorporated

4.2.1 Transistor-level simulation

In the first design step, the sampler is simulated to obtain the characteristic curve that relates the input voltage to the delay of the sampler. Figure 4.24 shows the sampler characteristic curve. The input voltage range is $200mV$ (from $1.0V$ to $1.2V$) and the maximum change in the sampler delay that corresponds to the input voltage range is $100ps$. As we can see from Figure 4.1, the characteristic curve is not linear and multibit non-linear quantizer is needed.

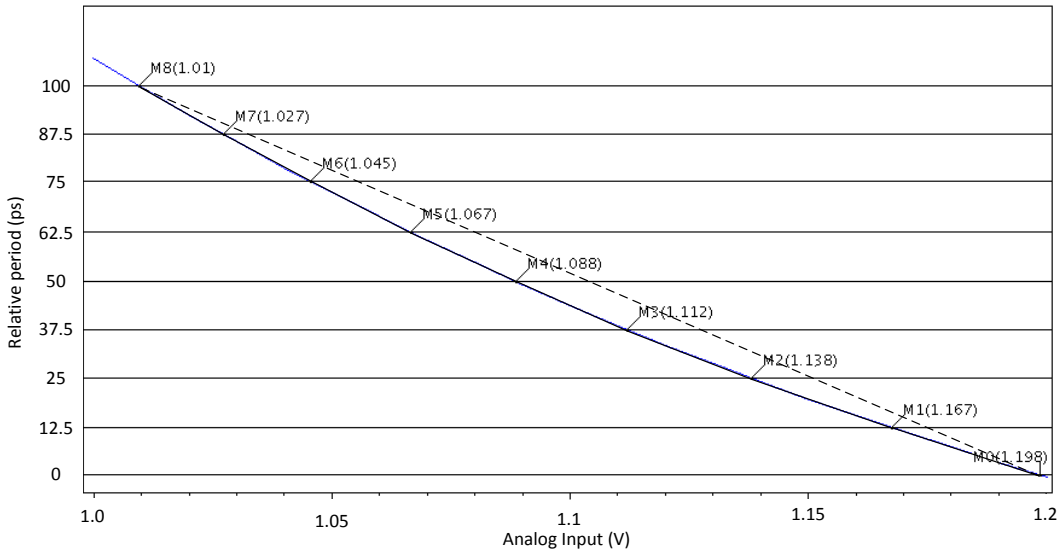

Figure 4.24: The non-linear characteristic curve of the VCO sampler

As mentioned in section 3.6.3, the non-linear quantizer technique will be implemented by dividing the non-linear charctristic curve into equal vertical devisions. To achieve 12 bit resolution, the maximum INL must be less than 1LSB. For the non-linearity under consideration, which is roughly hyperbolic, and within the range, i.e. $200mv$; to achieve 12 bit INL, an 8 segment piecewise linear approximation is used. Thus, the curve has been divided into 8 equally vertical divisions, each division is $12.5ps$. PI is used to generate both the comparison and feedback levels.

Figure 4.25 shows the schematics of the VCO. It consists of the VCO core, the phase interplator, and the MUX and controller units.

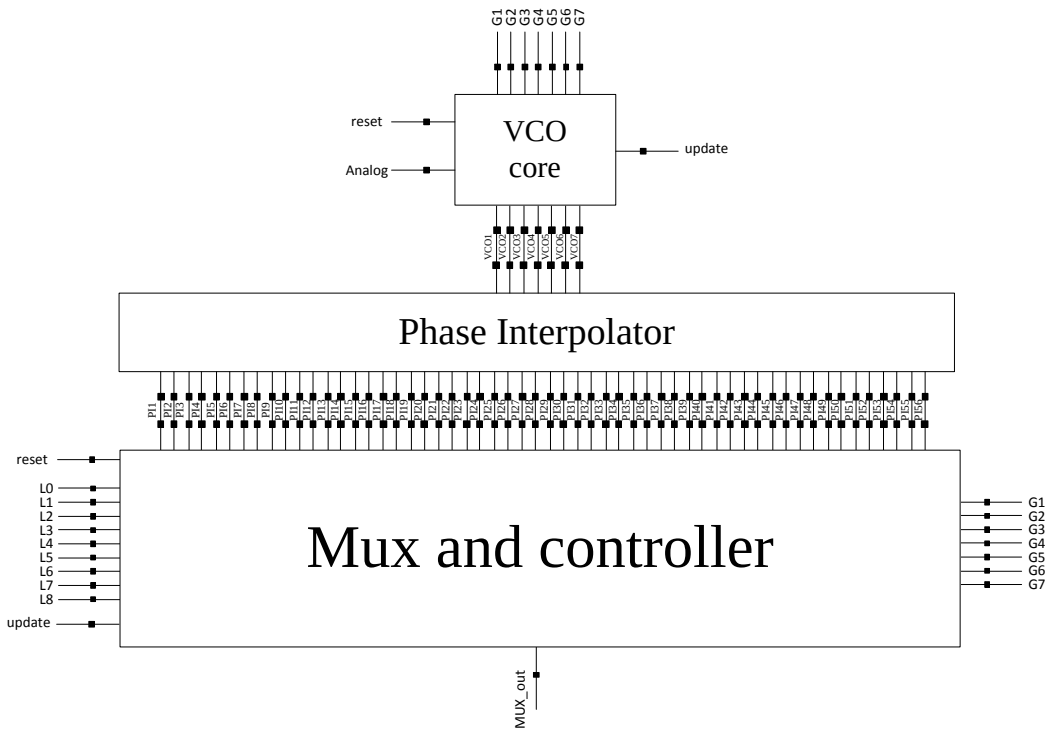

Figure 4.25: Schematic of the VCO

The VCO core, shown in Figure 4.26 and the definition/function of each signal is given in Table 4.3, consists of 7 stages. The delay time of each stage is $50ps$. Switches are used to break the loop of the VCO and close it back through the sampler. The update signal controls when the feedback signal determines the period of the VCO. The update signal timing is very important; it must be delayed until all the digital outputs are generated because each D-FF is clocked with different phase of the reference clock. Moreover, the update signal must not interrupt the sampler. It can be activated only when the sampler is idle. Finally, the update signal must come before the rising edge of the next reference clock. The reset signal is used to initiate the state machine that control the VCO. When the reset signal is "1", the VCO is held by holding the input of the sampler to "1". When the reset signal is "0", the controller is initialized by setting the switches state such that the first delay cell of the VCO core is replaced by the sampler. The output of all the 7

VCO stages, VCO1, VCO2, . . . , VCO7 in Figure 4.26, are connected to the phase interpolator, as shown in Figure 4.25.

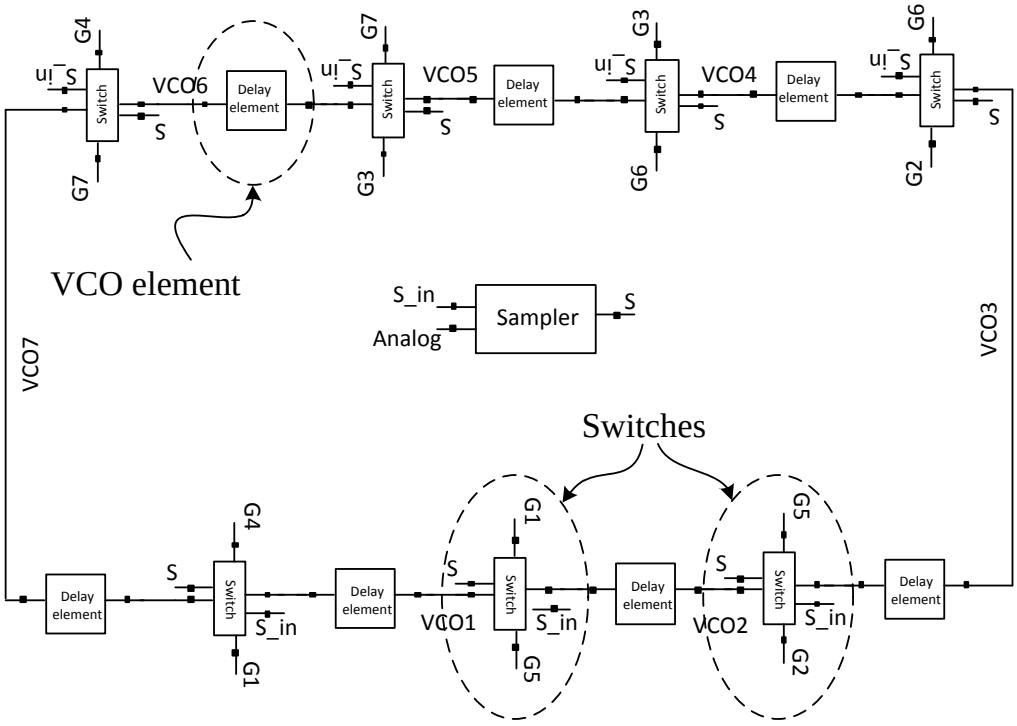

Figure 4.26: Schematic of the VCO core

Table 4.3: Definitions of symbols used in Figure 4.26

Name	**abbreviation**	**function**
Group control signals	G1 - G7	determine the position of the sampler inside the input VCO
Sampler input	S_in	input signal to the sampler
Sampler outout	S	output signal from the sampler

To generate the required feedback phases, 3-level phase interpolator is used to

divide the phase difference between each of the two consecutive VCO elements, that is 100*ps*, into 8 equal divisions. To divide the phase difference into equal divisions, the generated edge must be set exactly at the middle of the original two edges. This is done by setting the relative size ratios of the inverters to 0.6.

Figure 4.27 shows the circuit schematic of the MUX. The MUX consists of 7 groups, sub-MUXs. Each sub-MUX consists of 8 transmission unit. Each transmis-

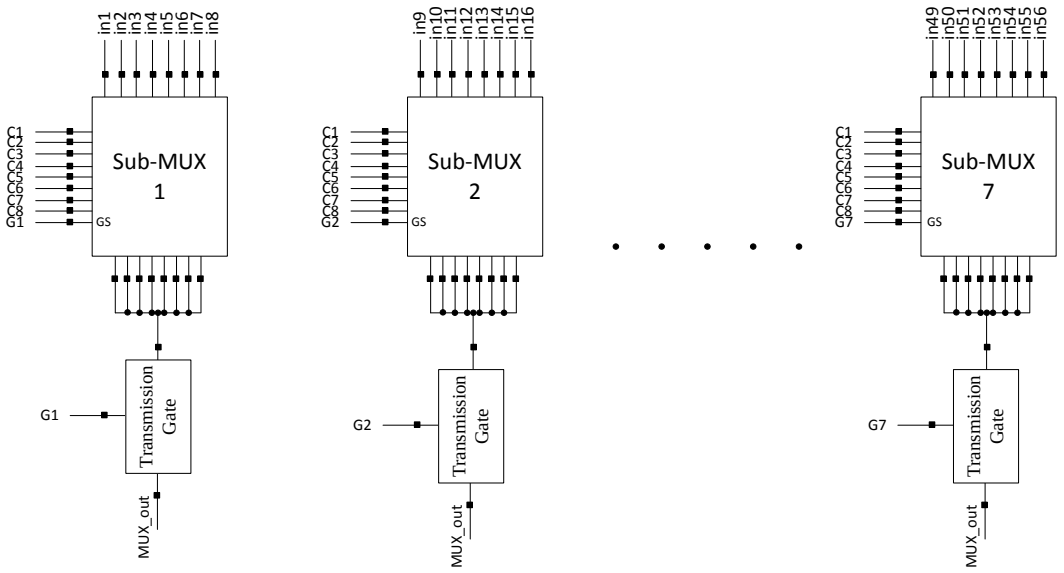

Figure 4.27: Schematic of the MUX

sion unit consists of two transmission gates, as shown in Figure 4.28. Transmission gate 1 determines whether the group is active or not. If the group selector, GS, is "1", the group will be activated and the control signal, Ci, will pass through transmission gate 1 and control transmission gate 2. If Ci is "1", transmission gate 2 will pass its input, inX, to its output, outX. However, if GS is "0", the group will not be activated and the control signal of transmission gate 2 will always be "0" and nothing will pass through.

The controller of the VCO is a state machine built using D-FFs and logic gates. the controller consists of two interactive sub-controllers. The first sub-controller, the group controller (shown in Figure 4.29), determines which group of the MUX is active. The second sub-controller, the element controller (shown in Figure 4.30), determines which transmission gate inside the group will be active.

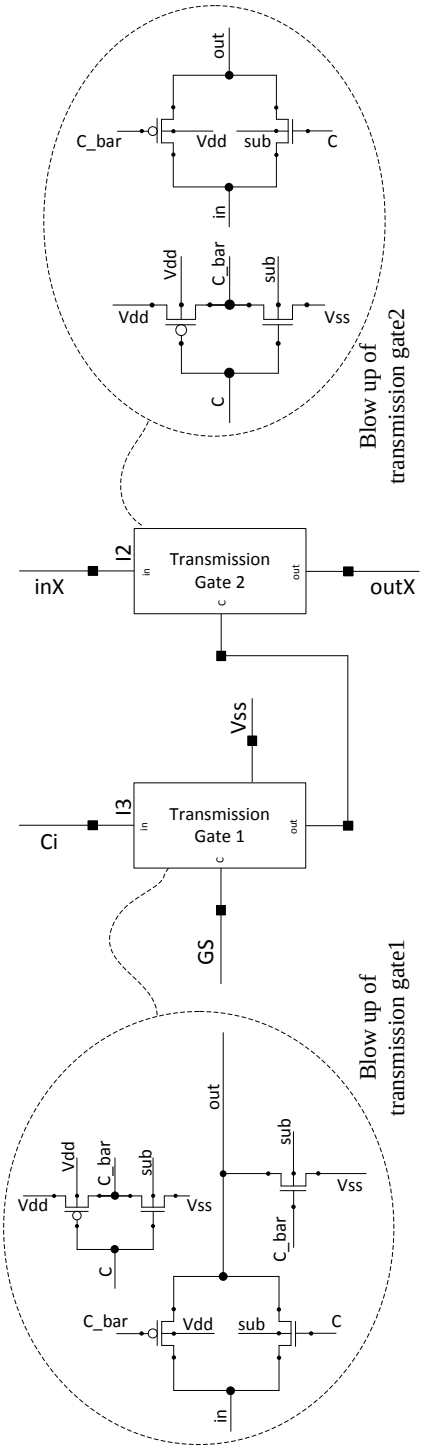

Figure 4.28: Schematic of the two transmission unit

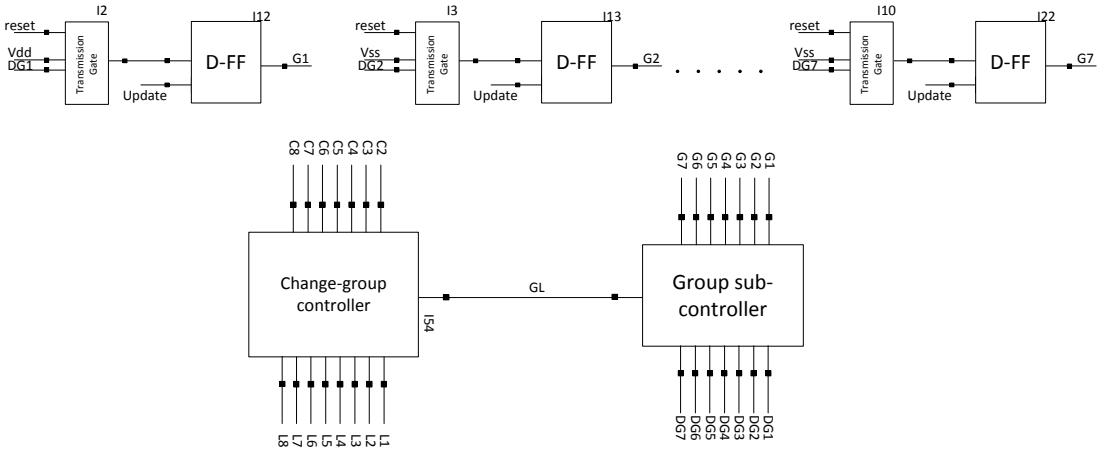

Figure 4.29: Schematic of the group controller

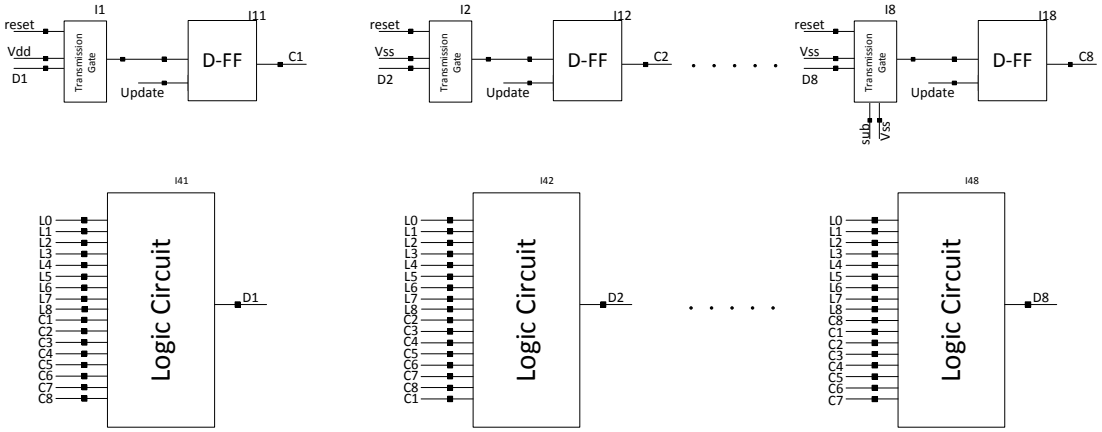

Figure 4.30: Schematic of the element controller

In this design, the element controller consists of 8 element-sub-controllers because the phase interpolator divides the phase difference between any two consecutive delay elements of the VCO core into 8 divisions. Each element-sub-controller, shown in Figure 4.31 controls one of the element control signals, $C_1, C_2, C_3, \ldots, C_8$. The element-sub-controllers check the current status of the element control signal and the value of the feedback signals and determine the next status of the element control signals. For example, the C_8 signal becomes "1" if its element-sub-controller detects any of the current status/feedback codes pairs shown in Table 4.4.

Change-group control signal, GL in Figure 4.29, is used to control the status of the group control signals. If the change-group control signal is "0", the next group

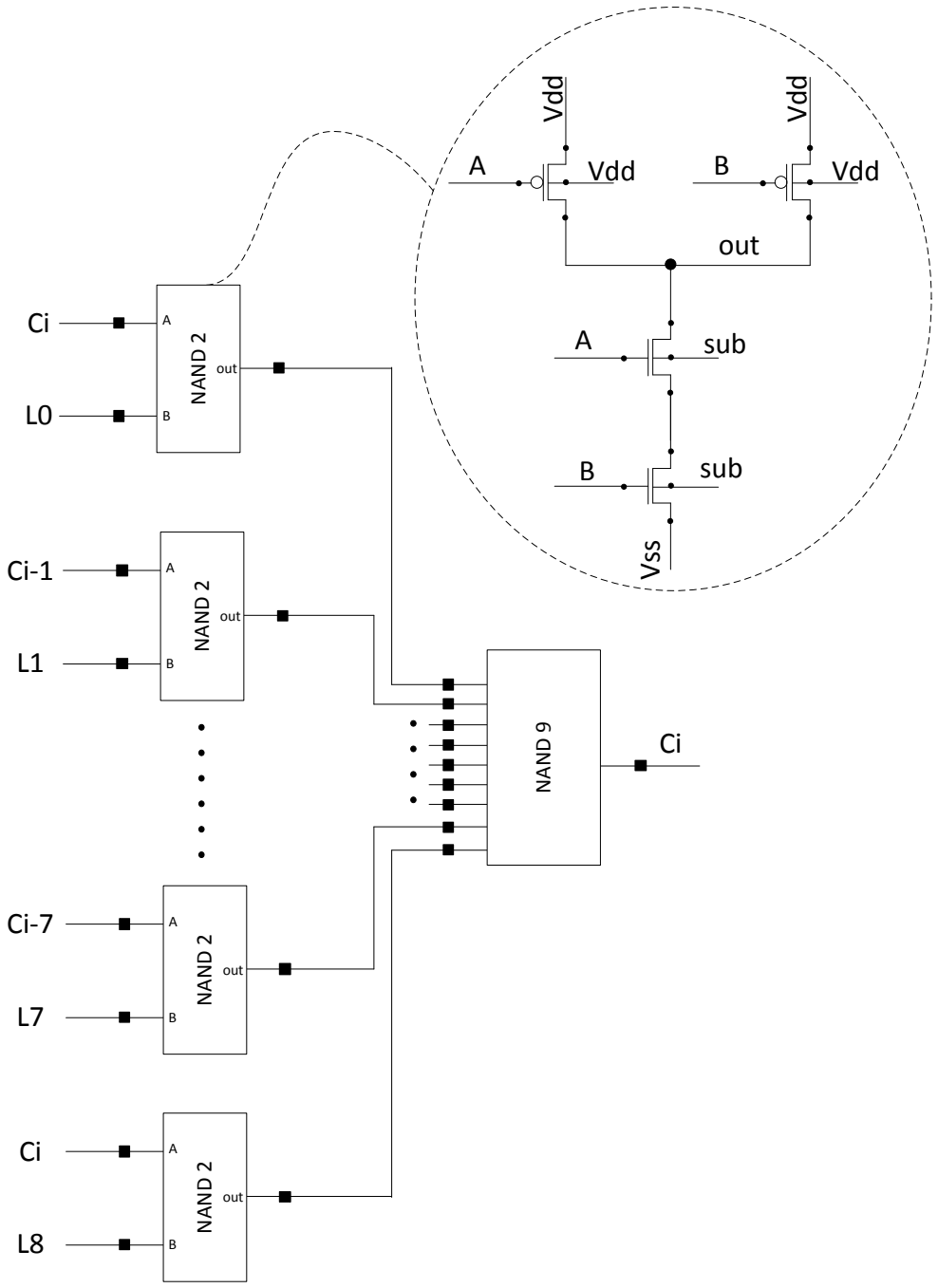

Figure 4.31: Schematic of the element-sub-controller

controls status will be the same as the current group control status and the same group, group i, will be activated. However, if the change-group control signal is

Table 4.4: current status/feedback codes pairs to active C_8

Current status	**Active element**	**Feedback digital code (L0 - L8)**	**Equivalent jump**
00000001	C_8	000000001	0
00000010	C_7	000000010	1
00000100	C_6	000000100	2
00001000	C_5	000001000	3
00010000	C_4	000010000	4
00100000	C_3	000100000	5
01000000	C_2	001000000	6
10000000	C_1	010000000	7
00000001	C_8	100000000	8

"1", the next group controls status will change such that the next group, group $i+1$, will be activated. The change-group control signal becomes "1" if one of the events in Table 4.5 occurs. Figure 4.32 shows the the schematic of the change-group controller, here $C1b, C2b, \ldots, C8b$ are the inverted version of the element control signals, and $L0, L2, \ldots, L8$ are the TADC feedback signals.

Table 4.5: Conditions for change-group control signal activation

Current active element	**Condition (equivalent jump)**
C_8	Not (0)
C_7	Not (0, or 1)
C_6	Not (0,or 1, or 2)
C_5	Not (0, or 1, or 2, or 3)
C_4	5 or 6 or 7 or 8
C_3	6 or 7 or 8
C_2	7 or 8
C_1	8

To change a particular group's group-control signal, the change-group-control signal, GL, is used to control a small MUX and implements the change. This small MUX consists of 2 transmission gates, as shown in Figure 4.33. The input of one of the two transmission gates is connected to the group-control signal that

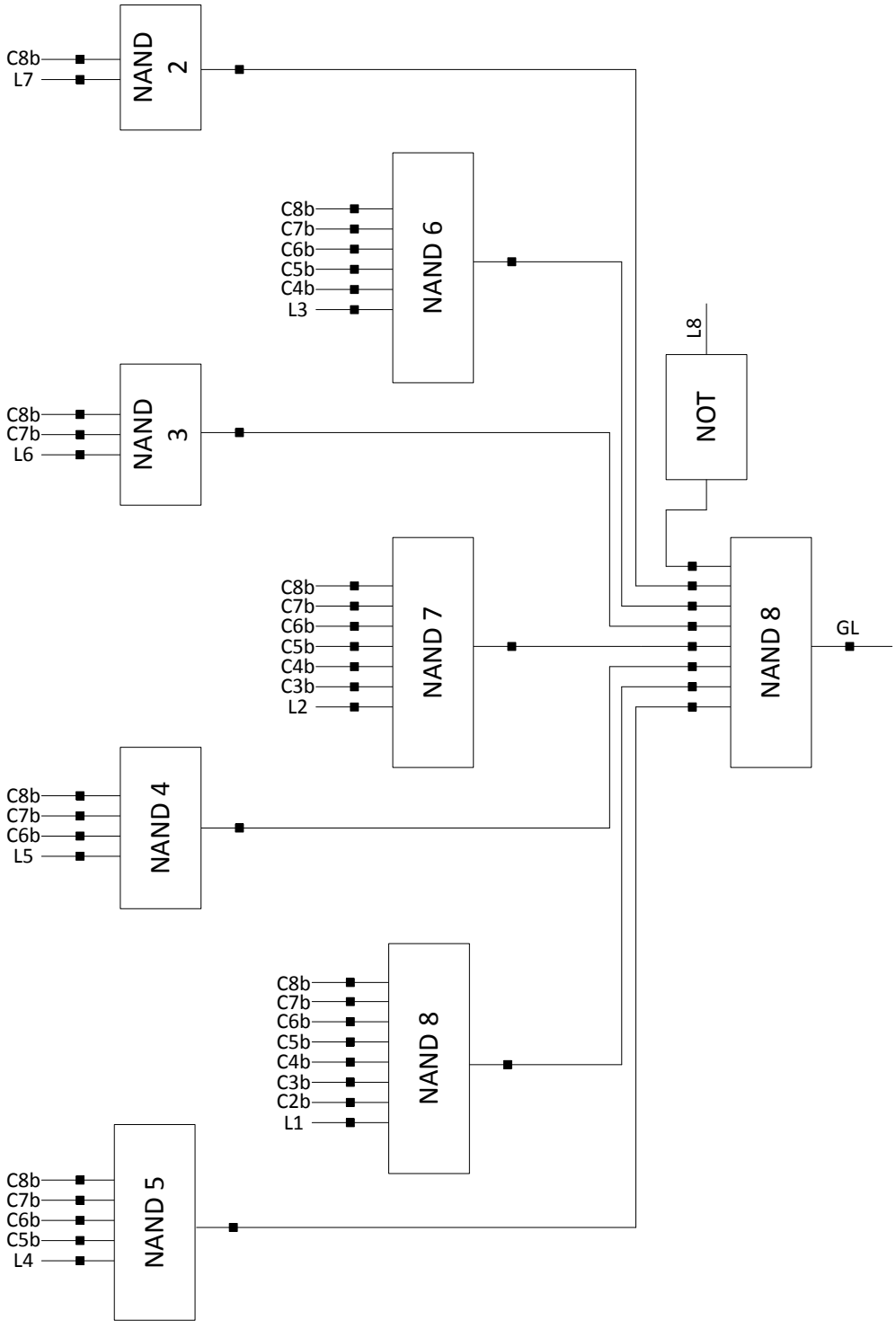

Figure 4.32: Schematic of the change-group control signal generator

controls the current group, G_i, while the input of the other transmission gate is connected to the group-control signal that controls the previous group, G_{i-1}. The output of the two transmission gate are connected to the data input of a D-FF. The change-group-control signal, GL, selects which transmission gate is active, thus selecting which one of the two group-control signals will be connected to the data input of the D-FF. In this design, the group sub-controller consists of 7 of such configuration, one to control each group. The change-group-control is connected to all the 7 configurations. When the change-group-control is "0", the input of the D-FF that control group i will be connected to the group-control signal of the group i. Thus, after triggering the D-FF, the status of the group-control signals will remain unchanged and the same group will remain active. In other words, if group i was active before the triggering of the D-FF's, then group i will be active after the triggering of the D-FF. However, when the change-group control is "1", the input of the D-FF that control-group i will be connected to the group control-signal of group $i-1$ and the D-FFs will act as a shift register. Triggering the D-FFs will result in changing the group-control signal status and the next group will be activated. In other words, if group i was active before the triggering of the D-FF's, then group $i+1$ will be active after the triggering of the D-FF.

For proper operation of the TADC the comparison levels must be in the middle of the feedback levels. Due to the fact that the feedback phase levels are equally spaced in time, the comparison phase levels will also be equally spaced and the phase difference between two consecutive comparison phase levels will be equal to the phase difference between two consecutive feedback phase levels, that is $12.5ps$ in this design. The reference signal generator generates the required comparison phase levels. To improve the matching, the reference signal generator has to be made a replica of the input VCO without using the MUX-controller unit. The reference voltage, 1.2V in this design, is connected to the sampler input and the proper control signals are set to replace one of the core delay cell with the sampler. The core feeds a phase interpolator and a proper 8 consecutive phase interpolator outputs are used as the comparison phase levels.

Figure 4.34 shows the whole TADC. The definition/function of each signal is given in Table 4.6. The output of the input VCO is feed to the quantizer, which consists of 8 D-FFs in this design, the VCO output is connected to all the data input of the D-FFs. The clock input of each D-FF is connected to one of the

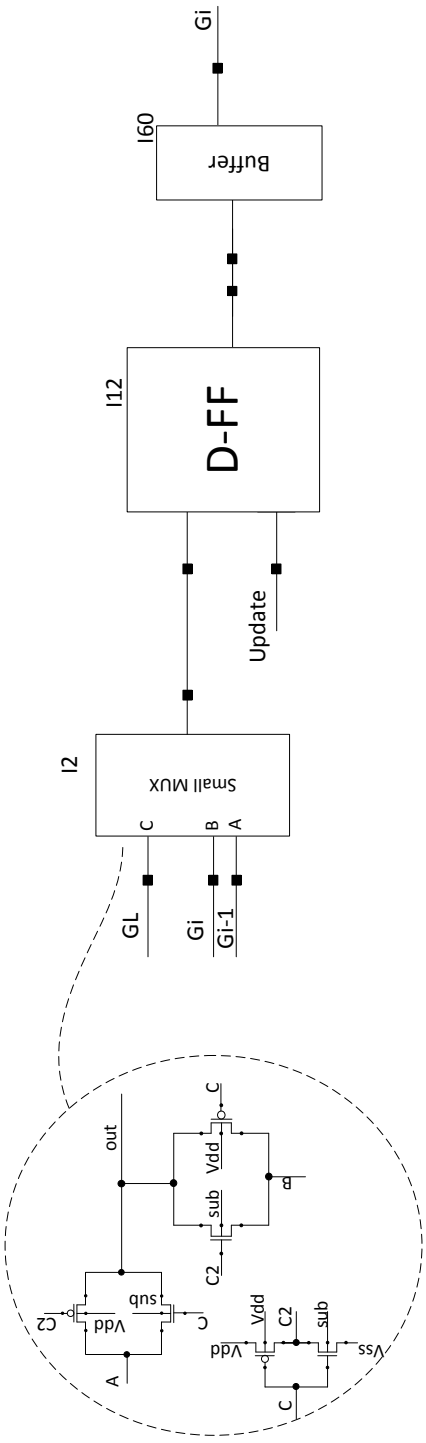

Figure 4.33: Schematic of the group controller sub-sub-controller

reference signals generated from the reference signal generator. The output of the quantizer is connected to T2B. The output of the T2B is fedback to control the input VCO and also is connected to the digital buffers which are used to drive the load capacitance.

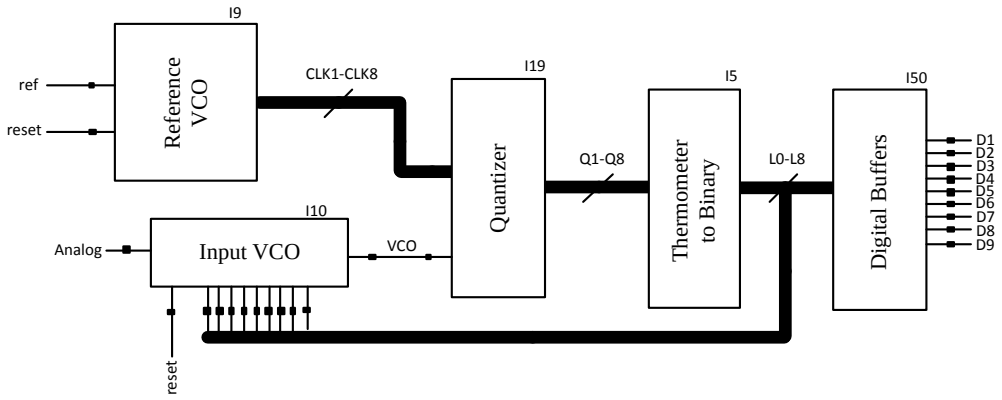

Figure 4.34: Schematic of the TADC

Table 4.6: Definitions of symbols used in Figure 4.34

abbreviation	**description/function**
VCO	The output of the input VCO
CLK1-CLK8	The reference edges
reset	reset signal to initialize the TADC
ref	The reference voltage
Analog	The analog input to the TADC
L0-L8	The output of the quantizer
D1-D9	The digital output of the TADC buffered by the digital buffers

Following the same procedure in Section 4.1.2, the total jitter in the input VCO is found to be 2.5ps. Moreover, following the procedure in section 4.1.3, the total average power consumed by the TADC is $32mW$.

4.2.2 Layout

A prototype of TADC is designed by using a 130-nm CMOS process. The TADC, shown in Figure 4.35, occupies an area of $700\mu m \times 700\mu m$, excluding the pads. Separate supply and ground pins are provided for the analog, digital, and output buffer portions of the chip. An analog supply is used for providing power to the sampler of the TADC. The rest of the core blocks are powered by the digital supply. The output buffers consume high power so that they are powered with a separate supply to avoid coupling the noise originating from these buffers to analog or digital portions of the chip. The reference voltage are provided off chip for better testability.

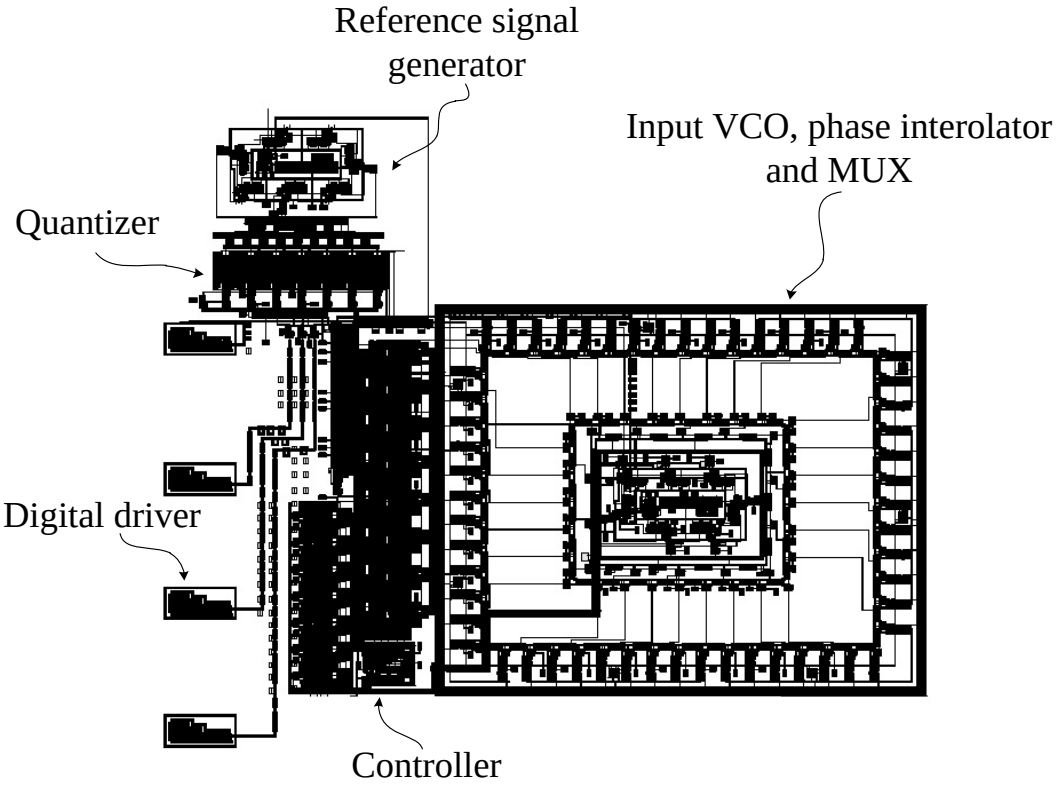

Figure 4.35: The layout of the TADC

4.2.3 Testing

A complete custom layout of the TADC is done and sent to be fabricated by CMC. Although post-layout simulations are done and the functionality of the system is checked, testing reveals a much larger than expected supply current of 140mA (expected supply current is 20mA) suggesting a possible latchup. When the supply voltage is increased above 0.8V, supply current starts to increase rapidly from 5mA to 140mA. The same design guidelines against latchup as in design I, such as guard rings, was followed.

4.3 Design III: Second order $\Sigma\Delta$ modulator, PI, and DEM incorporated

4.3.1 Transistor level simulation

This system is an extension of design II to second order system. The input VCO, and the reference signal generator circuit used in design II are also used in this design. The new parts in this TADC are the GRO, and the the GRO timing circuit.

The structure of the GRO, shown in Figure 4.36, is similar to that of the input VCO. The GRO core consists of 7 stages. The GRO oscillates when the top PMOS and the lower NMOS of each stage are enabled. When the switches are enabled, the delay time of each stage is $50ps$. The reset signal is used to initiate the state machine that control the GRO. When the reset signal is "1", the GRO is held by holding the input of the sampler to "1". When the reset signal is "1", the controller is initialized by setting the switches such that the sampler is switched in and replaces the first delay cell of the GRO core. In addition, the reference voltage, 1.2V in this design, is connected to the input of the sampler. The reference voltage sets the nominal period of the GRO to be equal to the period of the reference signal generator. The outputs of all the 7 stages in the GRO are connected to the phase interpolator. Each inverter in the phase interpolator is consisted of 4 transistors. The phase interpolator is enabled by turning on the top PMOS and the lower NMOS of each inverter. Finally, the feedback phases are generated as in design II.

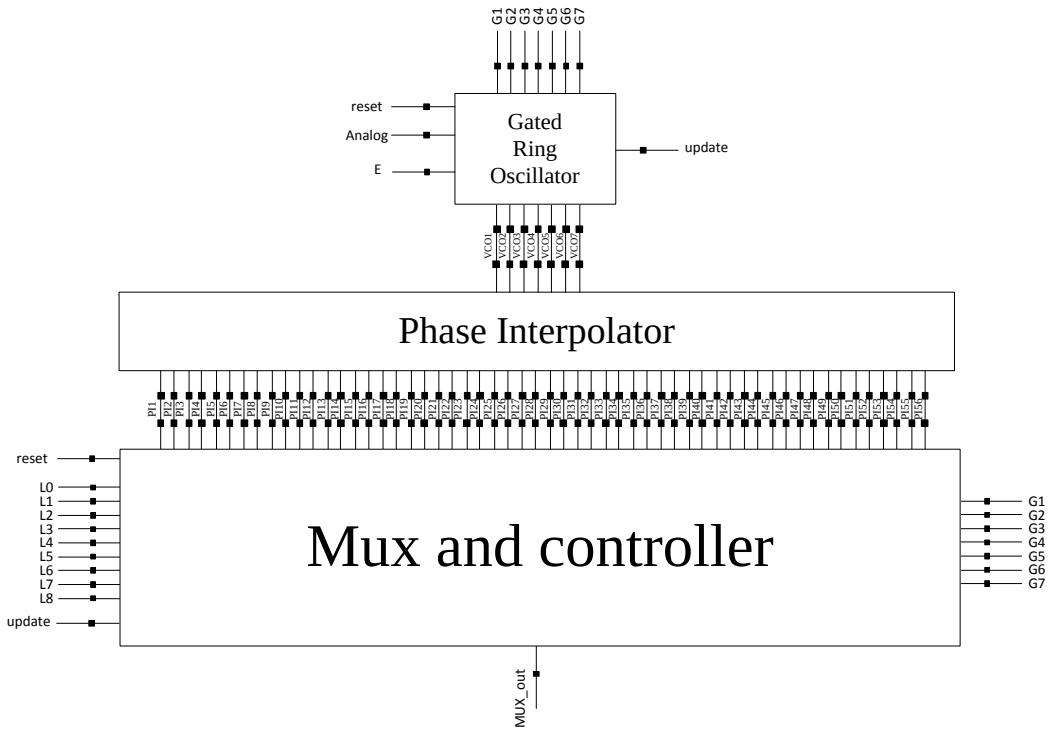

Figure 4.36: Schematic of the GRO

As discussed in subsection 3.7.1.3, the GRO timing circuit senses the phase difference between the output of the input VCO and the reference VCO and accordingly generates the proper control signals to control the GRO. Figure 4.37 shows the schematic of the GRO timing circuit. The phase of the input VCO is compared to the phase of the reference clock using a D-FF. Both the input VCO signal and the reference signal are delayed by T_d, that is 100ps in this design. The two signals are compared using an XNOR gate. The XNOR gate generates a pulse signal with an on duration equal to the time difference between the two signals, $\tau(k)$. The input VCO signal is delayed farther more by $2t_d$, which is 100ps in this design, and again compared to the delayed version of the reference signal using another XNOR gate. The XNOR gate, this time, generates a pulse signal with an on duration equal to the time difference between the two signals, i.e. $2t_d - \tau(k)$. A MUX is used to pass one of the two XNORs' output signals to the GRO. The selection of the MUX is controlled by the output of the D-FF. Two transmission gates are used to pass one version of the control signals to the GRO.

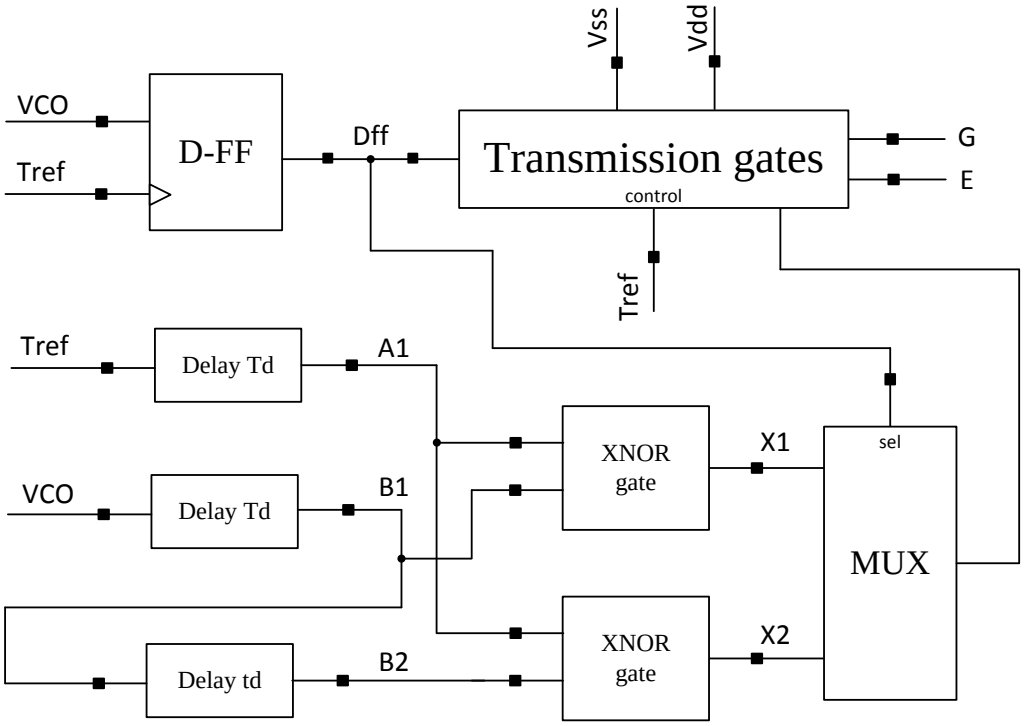

Figure 4.37: Schematic of the GRO timing circuit

Figure 4.38 shows the whole TADC. The definition/function of each signal is given in Table 4.8. Starting from the lower left hand corner, we have analog controls the input VCO. Then, VCO, the output of the input VCO, is fed to the GRO timing circuit to be compared to the reference phase. The output of the GRO timing circuit is used to control the GRO period. The output of the GRO is fed to the quantizer, which consists of 8 D-FFs in this design, the GRO output is connected to all the data input of the D-FFs. The clock input of each D-FF is connected to one of the reference signals generated from the reference signal generator. The outputs of the D-FFs are connected to T2B. The output of the T2B is connected to the digital buffers which are used to drive the load capacitance.

Following the procedure in section 4.1.3, the total average power consumed by the TADC is $45mW$.

Table 4.7: Definitions of symbols used in Figure 4.37

abbreviation	**description/function**
VCO	The output of the input VCO
Tref	The output of the reference VCO
A1	Delayed version of the output of the input VCO
B1	Delayed version of the output of the reference VCO
B2	Delayed version of B1
X1	The output of the XNOR 1
X2	The output of the XNOR 2
Dff	The output of the D-FF
G	The GRO group control signal
E	The GRO enable signal

Table 4.8: Definitions of symbols used in Figure 4.38

abbreviation	**description/function**
VCO	The output of the input VCO
Tref	The output of the reference VCO
CLK1-CLK8	The reference edges
GRO	The output of GRO
reset	reset signal to initialize the TADC
ref	The reference voltage
Analog	The analog input to the TADC
L0-L8	The output of the quantizer
D1-D9	The digital output of the TADC buffered by the digital buffers
E	The GRO enable signal
Group	The GRO group control signal

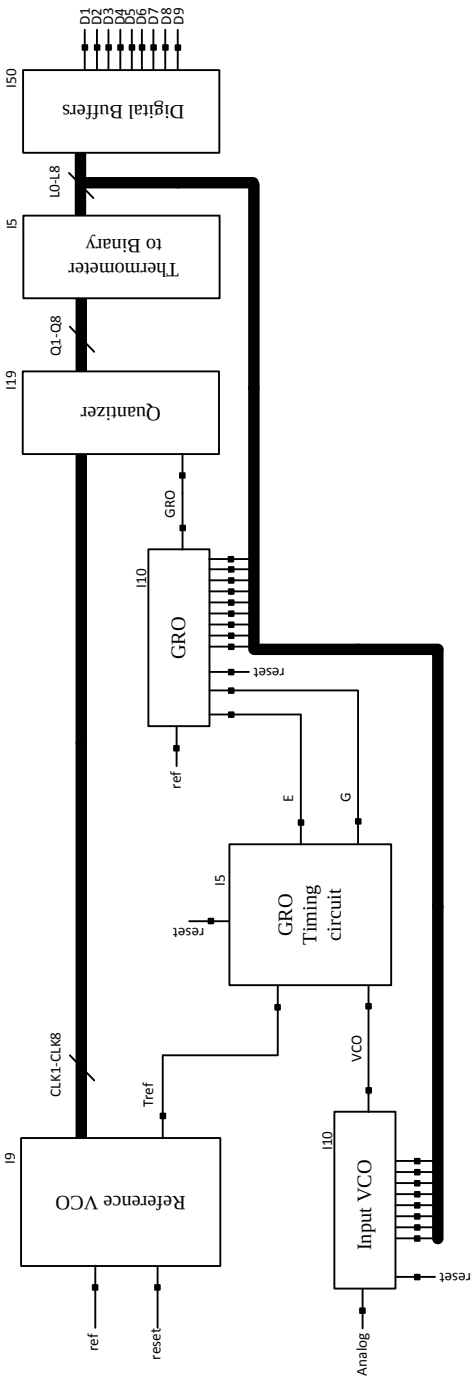

Figure 4.38: Schematic of the TADC

4.3.2 Layout

A prototype of TADC is designed by using a 130-nm CMOS process. The TADC, shown in Figure 4.39, occupies an area of $1200\mu m \times 700\mu m$, excluding the pads.

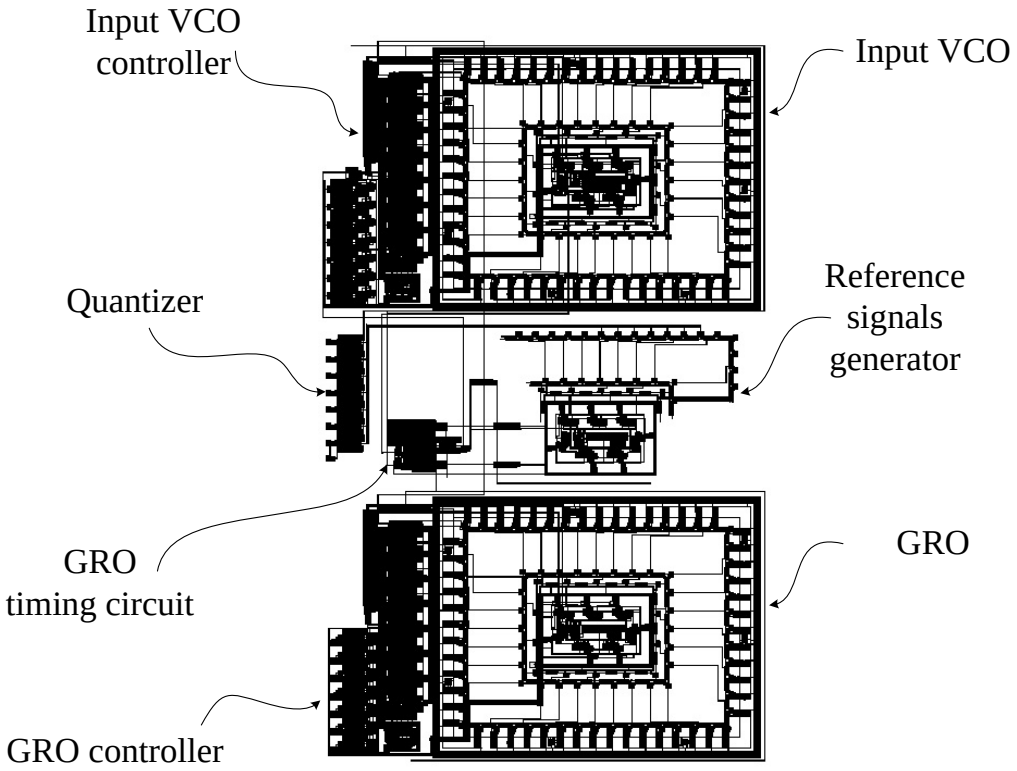

Figure 4.39: The layout of the TADC

4.3.3 Testing

A complete custom layout of the TADC is done and sent to be fabricated by CMC. All VCOs seem function properly on their own. However, the whole TADC is not functioning correctly. More than one of the digital outputs are stuck at "1" for all the chips that we have tested. This is unexpected since a proper functioning chip should have only one of its output is "1" and the rest is "0" (verified by simulations on the extracted layout).

Chapter 5

CONCLUSIONS AND FUTURE WORK

The importance of ADC is becoming more crucial in applications such as software-defined radios and high definition TVs where ADC is starting to become the system bottleneck in performance. One way to overcome the challenge of low-voltage design, due to technology scaling, is to process the signal in the time-domain. Since, as technology scales, time resolution improves despite the reduction in supply voltage, time-domain signal processing offers a better solution compared to that of the existing voltage-based methods.

One major issue in time-based ADCs using VCO as ATC is the non-linear voltage to period characteristics, leading to distortion. For some input voltage range, such distortion can be as severe as 18dB below fundamental, reducing resolution to only 3bit. In this thesis, $\Sigma\Delta$ based TADCs have been designed with non-linear multi-bit internal quantizer to compensate such nonlinear curve. DEM technique is used to improve the robustness of the TADC against the mismatch in the internal DAC. To improve the performance of the TADC even more, the S/H implicit in the VCO based APC has been used. This is used instead of an explicit S/H to reduce complexity and chip area. Prototype chips were designed and fabricated using a 0.13μm CMOS process. Measurements on a first-order $\Sigma\Delta$ based TADC show that the TADC has achieved 11bit dynamic range for 2MHz bandwidth. Simulations shows that the first order $\Sigma\Delta$ based TADC achieved 12bit resolution with random mismatch included. For the second order $\Sigma\Delta$ based TADC, simulations show that

TADC has achieved 12bits resolution for 20MHz bandwidth with random mismatch included.

5.1 Major contributions

In this research work, new architectures to build TADC have been introduced. The major contribution of this research work are:

- **Non-linear multibit internal quantizer (with DEM) in first-order $\Sigma\Delta$ TDC and inherent S/H in APC**
  The usage of the non-linear quantizer (with DEM) in the TDC to improve the linearity of the overall TADC has been studied. The characteristic curve of the internal quantizer is designed to match the APC non-linear curve. The linearity has been improved by setting the deviation between the piecewise linear curve, that represent the internal quantizer, and the APC non-linear curve to be smaller than or equal to the required resolution. The inherent sampling operation of the APC has been explored. The usage of the inherent S/H in the VCO instead of the explicit S/H circuit has been studied. The constrains on the TADC design due to the non-idealities of the implicit S/H have been investigated. In measurements, it has been shown that 11 bit dynamic range in 2MHz bandwidth can be achieved using the non-linear quantizer. In simulations, 12bit resolution in 2MHz bandwidth has been achieved.

- **Second-order $\Sigma\Delta$ modulator in time domain**
  A complete second order $\Sigma\Delta$ modulator in the time domain has been proposed. In previous works, typically, the second integration has been done in amplitude domain. In this work both the first and the second integration are done in time domain. This is done by using the GRO to implement the second integrator. Simulations show that the TADC achieve 12bit resolution for 20MHz bandwidth.

5.2 The state-of-the-art

Table 5.1 compares the performance of the proposed TADC with the state-of-the-art. It should be noted that only design I has measured result and that simulation results for design II, and III are just included for completeness. The figure of merit (FOM), in Table 5.1, is calculated as

$$FOM = \frac{Power}{2 \times Bandwidth \times 2^{ENOB}} \tag{5.1}$$

where the effective number of bits (ENOB) is calculated from SNDR, see Appendix A.2.

In Design I, the usage of the implicit S/H restricts the bandwidth of the input signal. This restriction results in making the BW smaller compared to the case when an explicit S/H is used. This results in increasing the FOM. Designs in Table 5.1, which use explicit S/H, the bandwidth used can be about 10 times higher, but at the expense of being more complicated and occupying more chip area. Specifically, comparing to [18] which also uses explicit S/H, Design I achieved better FOM. Comparing to [51], Design I achieved almost the same dynamic range while the area and order of the modulator is smaller. [52] achieved higher dynamic range than Design I but the order of the modulator is 4. Increasing the order of the modulator results in increasing the area and having stability considerations. Comparing to [53], although it achieved 80dB dynamic range, its area is about 20 time larger than Design I, and also the order of [53] is 2.

5.3 Future work

The following aspects of this work can be extended:

- **Layout improvement**
  More work needs to be done on the layout to improve the performance of the TADC. Moreover, more observability and controllability points are need to investigate the chip problems. These points must be chosen carefully so that it does not disturb the performance of the TADC.

- **Differential implementation**
  All the TADC introduced in this thesis are built using single-ended implementations. To improve the performance of the TADC, differential implementation should be used. Differential implementation can be better than the single-ended in terms of distortion and power supply rejection.

- **Eliminating digital calibration**
  In design II and III, digital correction is needed to improve the linearity of the TADC. Improving the linearity of the TADC without the usage of digital calibration is a good area of research.

- **Improve the performance of the second order TADC**
  The GRO timing circuit is considered the bottleneck in the design of the second order TADC. More work is needed to fix the nonidealities of this circuit and thus improve the performance of the TADC.

Table 5.1: Comparison of performance of the proposed TADC with the state-of-the-art

Research work	CMOS Technology	Dynamic range (dB)	Bandwidth (MHz)	Order of $\Sigma\Delta$	Sample and hold	Power (mW)	FOM ($fJ/Step$)	Area (mm^2)
Design I	0.13μm	66	2	1*	implicit**	25	1220	0.048
[18]	0.18μm	55	0.8	1	implicit	47.5	2600	0.037
[51]	65nm	67	6	3	explicit	10.5	325	0.15
[52]	0.13μm	75	20	4	–	87	330	0.45
[5]	65nm	67	18	1	–	17	230	0.07
[53]	0.13μm	80	4	2	explicit	14	298	0.7

*Simulation results on a 2^{nd} order shows bandwidth (BW) increases to 20MHz, while resolution performance stays above 12bit. On the other hand, for the same BW, it is expected that DR will increase. In addition BW can also increase when technology scales down from 0.13μm.

**Tracking error and NUS effect on distortion is handled

APPENDIX

A.1 Static specification

Due to non idealities in circuit implementation of the ADC, other types of error, other than the quantization error, are introduced. In this section we review some of these types of error that independent of time (static).

Offset error

The offset error is defined as deviation of the ADC characteristic from the ideal one at input equal to zero [6]. It also can be defined as the deviation of the ADC characteristic line (the line connecting the mid-point of the ADC levels, shown in Figure A.1, to the right or to the left, from the one of the ideal ADC [8]. Offset

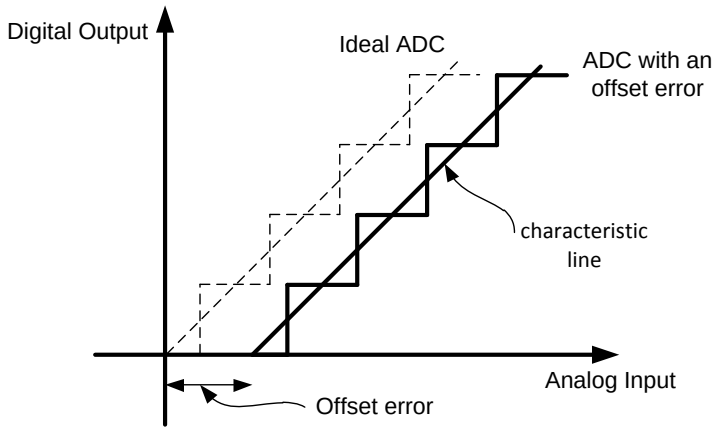

Figure A.1: Example of an ADC has an offset error

error affects all the digital code the same way and can be removed by calibration. Figure A.1 shows an example of an ADC with an offset error.

Gain error

After the offset error has been removed, the gain error is defined as deviation in the slope of the ADC characteristic line from the one of the ideal ADC [8]. Figure A.2 shows an example of an ADC has a gain error.

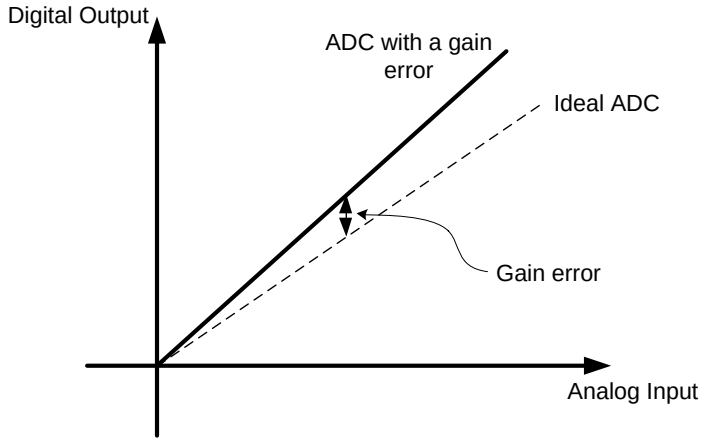

Figure A.2: Example of an ADC has a gain error

Differential non-linearity

The differential non-linearity (DNL) is defined as the deviation of the individual code width from the ideal 1 LSB [6], Figure A.3 shows an example of an ADC which has a DNL. For code k, DNL_k is expressed as

$$DNL_k = \frac{width\ of\ code\ k - 1\ LSB}{1\ LSB} \tag{A-1}$$

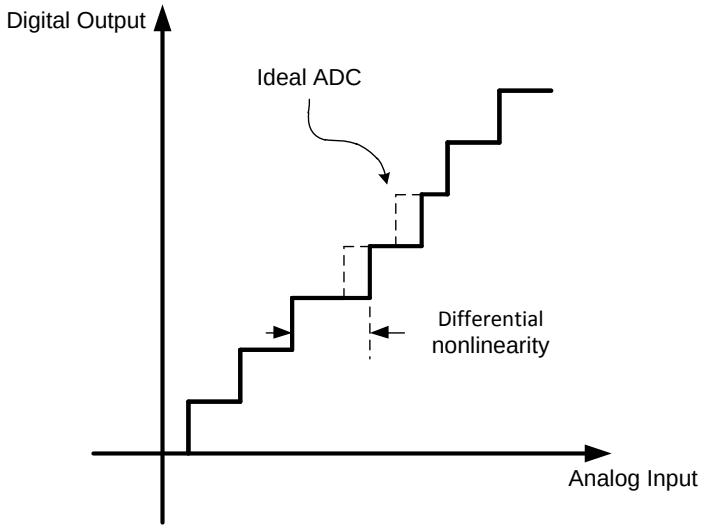

Figure A.3: Example of differential non linearity in ADC

Integral non-linearity

The integral non-linearity (INL) is defined as the deviation of an actual transfer function from a straight line [8], Figure A.4 shows an example of an ADC having an INL. The INL is given by

$$INL = \sum_{i=0}^{k} DNL \tag{A-2}$$

Missing codes

The ADC is said to have missing codes when it skips one of its digital output. An ADC is guaranteed not to have missing codes if the maximum DNL is less than 1 LSB or if the maximum INL error is less than 0.5 LSB.

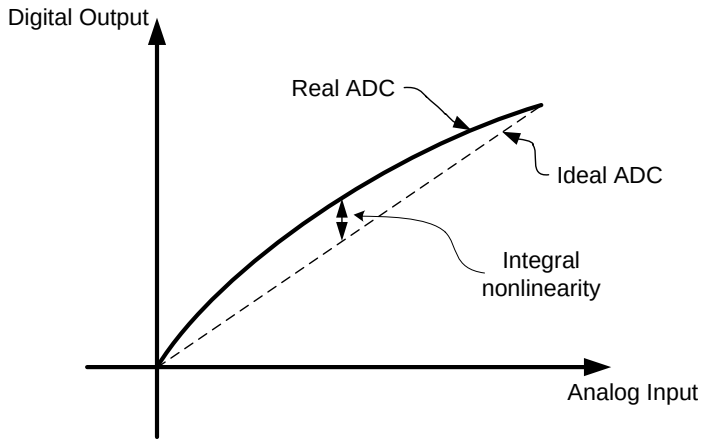

Figure A.4: Example of integral non linearity in ADC

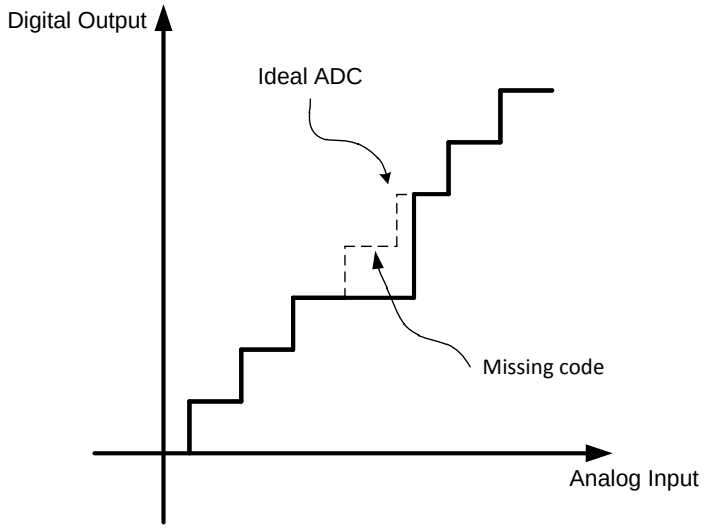

Figure A.5: Example of a missing codes

A.2 Dynamic specification

In this section we will review some of the time dependent (dynamic) ADC specifications.

ADC conversion time and sampling rate

The ADC conversion time is defined as the time taken by the converter to complete a single conversion including the acquisition time of the input analog signal [8]. The maximum sampling rate is the speed that the ADC can continuously convert analog input samples into digital form, and is equal to the inverse of the conversion time.

Signal to noise ratio

Signal to noise ratio (SNR) is defined as the ratio of the power of the full scale input signal to the power of the noise at the output of the ADC.

$$SNR = 10\log\Big(\frac{Full\ scale\ input\ power}{Quantization\ noise\ power + circuit\ noise\ power}\Big)db \qquad \text{(A-3)}$$

For the quantization noise only (ignoring the circuit noise), the SNR is given by

$$SNR = 6.02D + 1.76dB \qquad \text{(A-4)}$$

As we can see, from equation (A-4), as the number of bits increases the system SNR increases.

Signal to noise and distortion ratio

Signal to noise and distortion ratio (SNDR) is defined as the ratio of the power of the full scale input signal to the power of the noise plus the distortion power.

$$SNR = 10\log\Big(\frac{Full\ scale\ input\ power}{Noise\ power + Distortion\ power}\Big)db \qquad \text{(A-5)}$$

Figure A.6 shows an example of a signal has a second and third order harmonic distortion.

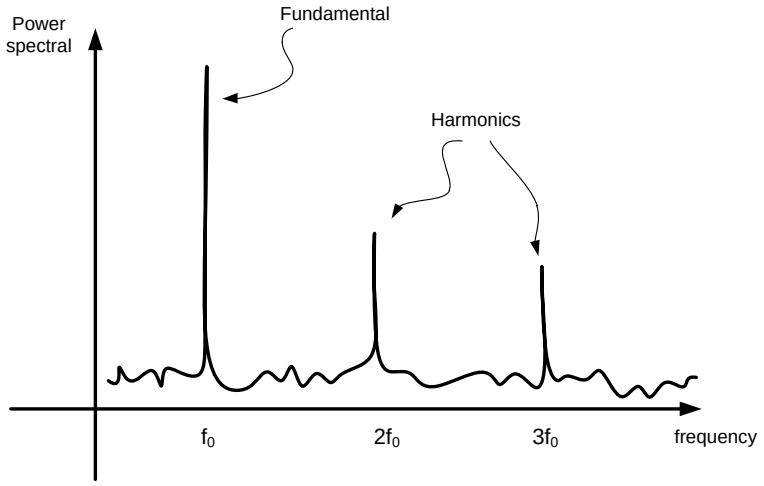

Figure A.6: Example of a signal has harmonic distortion

Effective number of bits

As the system SNDR is less than the ideal ADC SNR (which includes only the quantization noise), the actual number of bits will be less than the one we get from equation (A-4). Effective number of bits (ENOB) is the number of bits that if we substitute in the equation (A-6), the value of SNR will equal to the system SNDR value [54]. Thus, we can express ENOB as

$$ENOB = \frac{SNDR_{db} - 1.76}{6.02} \tag{A-6}$$

A.3 Maximum frequency due to the tracking error

The explicit S/H

The relation between the voltage of a capacitor and the charging (or discharging) current is given by

$$I = C_L \frac{dV_c}{dt} \tag{A-7}$$

For simplicity, let's assume that the discharging transistor is in saturation region so I becomes I_{SAT}. Let's further assume that the relation between the input voltage, V_{in} and I_{SAT} is linear. Then we can write the capacitor equation during the

discharging period of the cycle as

$$-I_{SAT} = -k_1 V_{in} = C_L \frac{dV_c}{dt} \tag{A-8}$$

where k_1 is a constant. Since V_{in} is constant, due to the usage of the explicit S/H, then we can replace V_{in} by V_{const} and we can write the capacitor, V_c voltage as

$$V_c = -\frac{k_1}{C_L} \int V_{const}\ dt = -\frac{k_1}{C_L} V_{const}\ t + k_0 \tag{A-9}$$

The constant k_0 can be determined from the initial condition. The capacitor is initially charged to V_{dd} (at $t = 0$, $V_c = V_{dd}$). Then can write V_c as

$$V_c = D_{dd} - \frac{k_1}{C_L} V_{const}\ t \tag{A-10}$$

To determine the time when V_c crosses the threshold of the next inverter, $t_{V_{th\_const}}$, we set V_c to V_{th} and solve for $t_{V_{th\_const}}$. This is given by

$$t_{V_{th\_const}} = \frac{C_L}{k_1} \frac{(V_{dd} - V_{th})}{V_{const}} \tag{A-11}$$

The implicit S/H

Let us first assume that V_{in} is a triangle wave with a frequency F (i.e. period $T = 1/F$), slope m, and an amplitude A, as shown in Figure A.7. $V_{shift-triangle}$ is the minimum value of the triangle wave V_{in}.

We assume that the sampling window is small compared to T. Thus, we assume that the slope of V_{in} is not likely to change (from m to $-m$ or from $-m$ to m) during the sampling window. Therefore we can write V_{in} as

$$V_{in} = V_{const} + m \times t \tag{A-12}$$

where V_{const}, a constant, is the value of V_{in} when the capacitor starts discharging, in other words, V_{in} at the beginning of the sampling window . by Substitute in

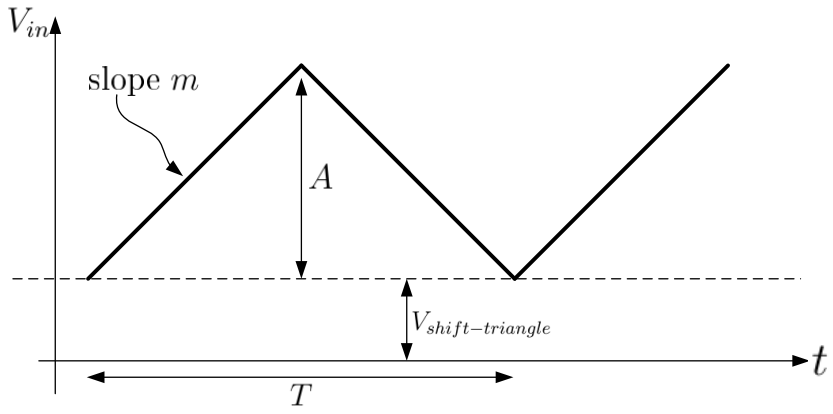

Figure A.7: An example of a triangle V_{in}

equation (A-8), V_c cn be written as

$$V_c = -\frac{k_1}{C_L}\int (V_{const} + m \times t)\ dt = -\frac{k_1}{C_L}(V_{const}\ t + \frac{m}{2}t^2) + k_0 \tag{A-13}$$

Again the value of k_0 can be determined from the initial condition, and V_c can be written as

$$V_c = V_{dd} - \frac{k_1}{C_L}(V_{const}\ t + \frac{m}{2}t^2) \tag{A-14}$$

The time at which V_c reaches the threshold voltage for a triangle V_{in}, $t_{V_{th\_triangle}}$, is then given by

$$t_{V_{th\_triangle}} = \frac{-k_1 V_{const} + \sqrt{(k_1 V_{const})^2 + 2k_1 m C_L (V_{dd} - V_{th})}}{k_1 m} \tag{A-15}$$

Tracking error due to the usage of the implicit S/H for a triangle input signal

The tracking error t_{error} is the difference between $t_{V_{th\_const}}$ and $t_{V_{th\_triangle}}$. From equations (A-11) and (A-15), we can write t_{error} as

$$t_{error} = \frac{C_L}{k_1}\frac{(V_{dd} - V_{th})}{V_{const}} - \frac{-k_1 V_{const} + \sqrt{(k_1 V_{const})^2 + 2k_1 m C_L (V_{dd} - V_{th})}}{k_1 m} \tag{A-16}$$

To be able to use an inherent S/H in the VCO, this error has to be less than

the time corresponding to 1 LSB change in the V_{in} (t_{1LSB}) (this 1 LSB change is calculated for 2 values of V_{in}. In each value; V_{in} is assumed to be explicitly sampled and hence constant in the sampling window). Then the condition on t_{error} is

$$t_{error} \leq t_{1LSB} \tag{A-17}$$

Substituting from equation (A-16) and solve for m results in

$$m \leq \frac{2V_{const} \times t_{1LSB}}{\left(t_{1LSB} - \frac{C_L}{k_1}\frac{(V_{dd}-V_{th})^2}{V_{const}}\right)^2} \tag{A-18}$$

For a triangle V_{in}, F is given $m/2A$ then we can write the condition on the frequency of the input signal as

$$F \leq \frac{2V_{const} \times t_{1LSB}}{A\left(t_{1LSB} - \frac{C_L}{k_1}\frac{(V_{dd}-V_{th})^2}{V_{const}}\right)^2} \tag{A-19}$$

Thus, the maximum frequency of V_{in} that can be applied to the VCO with an inherent S/H is given by

$$F_{max} = \frac{2V_{const} \times t_{1LSB}}{A\left(t_{1LSB} - \frac{C_L}{k_1}\frac{(V_{dd}-V_{th})^2}{V_{const}}\right)^2} \tag{A-20}$$

As t_{1LSB} is given by the time difference between two constant values of V_{in} that differ by V_{1LSB}, then t_{1LSB}, using equation (A-11), can be written as

$$t_{1LSB} = \frac{C_L}{k_1}\frac{V_{1LSB}(V_{dd} - V_{th})}{V_{const}(V_{const} + V_{1LSB})} \tag{A-21}$$

As we can see from equation (A-21), t_{1LSB} is change as V_{const} changes. It decreases as V_{const} increases. Therefore as we sweep the rang of V_{in}, t_{1LSB} changes from t_{1LSB_min} to t_{1LSB_max}. Figure A.8 illustrates this fact.

Substitute from equation (A-21) in equation A-20), F_{mx} can be written as

$$F_{max} = \frac{k_1}{C_L}\frac{V_{1LSB}(V_{const} + V_{1LSB})}{A(V_{dd} - V_{th})} \tag{A-22}$$

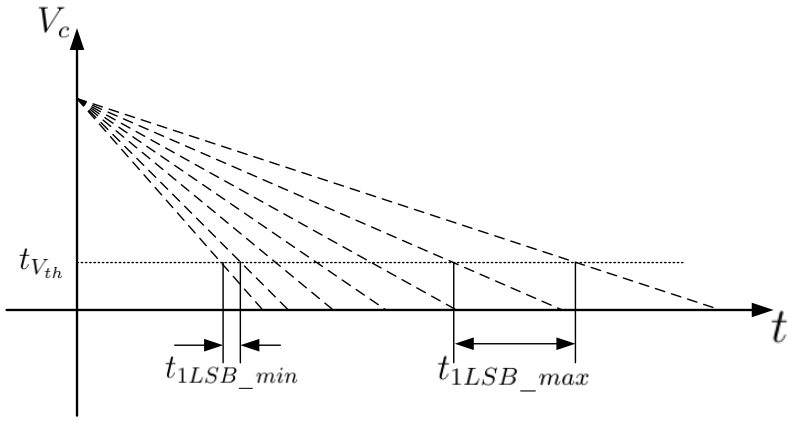

Figure A.8: t_{1LSB} changes as V_{in} sweep through the range

As we can see from equation (A-22), F_{max} is a function of V_{const}. Since V_{const}, is the value of V_{in} when the capacitor start discharging/charging, it depends on the relative phase between V_{in} and INV_{in}, in Figure 3.5. Then F_{max} also depends on this. To get a bound on F_{max}, F_{max_bound} , which is true for all relative phase, we should set V_{const} to the worst case, which happens when V_{const} is at the minimum, i.e. $V_{shift-triangle}$ in Figure A.7. This results in

$$F_{max\_bound} = \frac{k_1}{C_L} \frac{V_{1LSB}(V_{shift-triangle} + V_{1LSB})}{A(V_{dd} - V_{th})} \tag{A-23}$$

A.4 Fabrication of MOS transistor

This section briefly describes a simplified version of the fabrication of a transistor on the silicon wafer. For CMOS process, the silicon substrate is usually p-type. The first step in CMOS fabrication is the well formation. The N-well is formed by Implanting n-type impurities into the wafer followed by diffusing the impurities deep into the substrate. The next stage in CMOS fabrication is to identify the active areas. Active areas are defined as areas where the CMOS transistors are fabricated. Active areas are isolated using thick oxide, sometimes is called Field oxide. Then gate oxide formation stage takes place. In this stage, a thin gate oxide is grown across the wafer. Gate oxide is the insulator between the transistor's gate and its channel. After that, poly (poly-silicon) is deposited on the wafer to

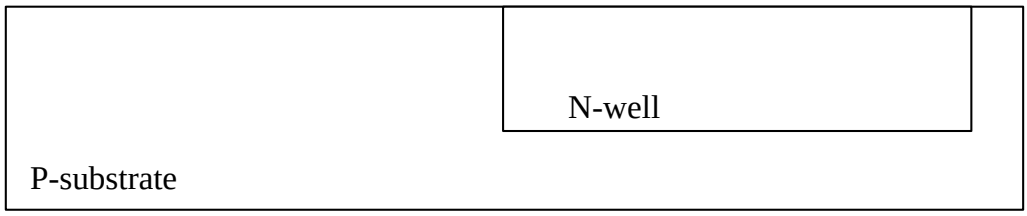

Figure A.9: N-well formation

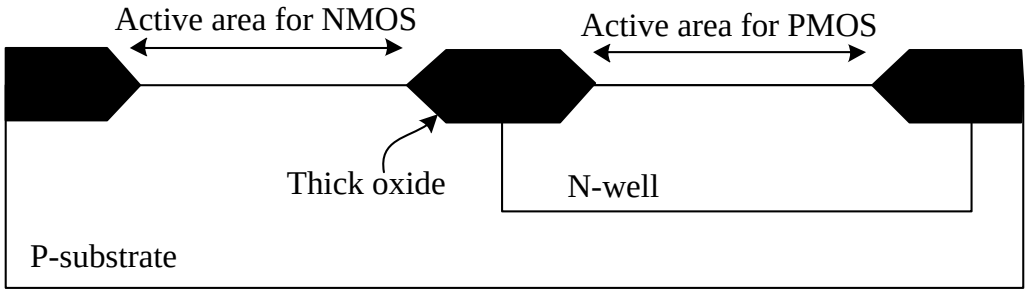

Figure A.10: Active area identification

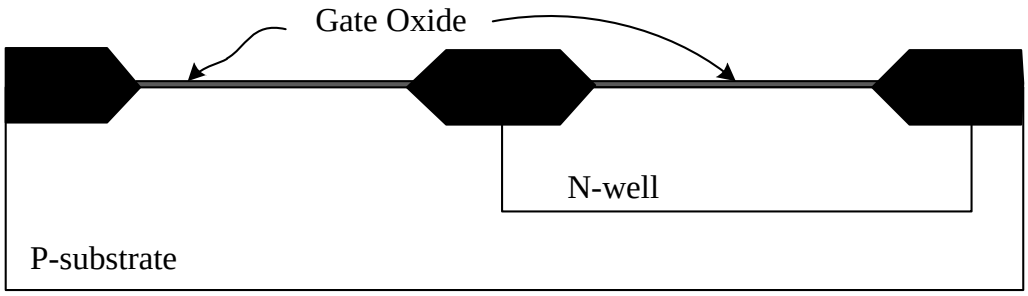

Figure A.11: Gate oxide foundation

form the gates of the transistors. The gate oxide in the active area that are not covered by the gate poly will be etched away to form the source and the drain of the transistor. The source terminal and the drain terminal of the transistor is formed by diffusing p-type and n-type impurities into the active areas. The diffusions for the

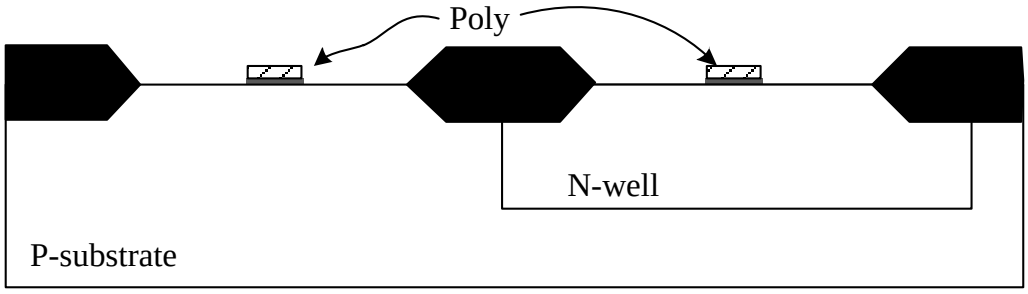

Figure A.12: Poly gate formation

sources and the drains of NMOS and PMOS are N-diffusion ($n+$) and P-diffusion ($p+$) respectively. As the impurities diffuse both vertically and laterally, the gate poly will slightly overlap the sources and the drains. This results in gate overlap capacitances. The P-substrate should be biased to the lowest voltage potential

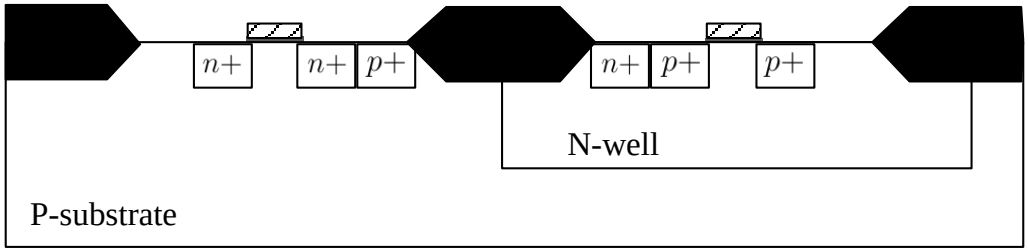

Figure A.13: Sources and drains formation

while the N-well should be biased to the highest voltage potential. In this way, all the P-N junctions in/between the P-substrate and the N-well are reverse biased and hence the transistors are electrically isolated from one another. The substrate and the N-well are doped lightly. A direct connection from the metal routing layer to the bulk is not allowed. The connection should be made through a higher doped diffusion. Connections from the metal routings to the substrate and the N-wells are made through the p-tap (the $p+$ in the P-substrate in Figure A.13) and the n-tap (the $n+$ in the N-well in Figure A.13).

Guard rings

Because a reverse biased diode has the electrical properties of a capacitor, circuit signals can be coupled through the substrate. To reduce the substrate coupling, guard rings are used. By surrounding the NMOS in the P-substrate with n-guard ring and by connecting the n-guard ring to VDD, any injected electrons from the NMOS will be attracted and collected efficiently by the n-guard ring. Also, by surrounding the PMOS in the N-well with p-guard ring and by connecting the p-guard ring to GND, any injected holes from the PMOS will be attracted and collected efficiently by the p-guard ring.

For the guard rings to be effective, the resistance of the path starting from the guard ring to the voltage source must be kept as low as possible. Hence, the guard rings are usually made wide to decrease its resistance. Also the number of contacts that connect the metal layer to the guard ring must be as large as possible to reduce the resistance. Ideally, the guard rings should be placed as closely to the likely noise sources as possible.

Guard rings can be used to protect critical transistors. Guard rings are placed around the critical transistors to absorb stray electrons and stray holes. This is done by surrounding NMOS in the p-substrate with p-guard ring that is connected to ground or surrounding PMOS in the N-well with n-guard ring that is connected to VDD. Double guard rings can be used to provide more protections. As current will flow through the path of least resistance to ground, the ESD protection path must have small resistance to cause the to flow through that path away from the internal circuits.

Electrostatic discharge protection

Electrostatic discharge (ESD) is a high current event that can cause damage to the chip at processing stages and/or handling stage [55, 56]. The voltage levels that are involved during an ESD event can exceed the highest breakdown voltage of any device in an advanced silicon technology. The objective of ESD protection is not to prevent current from flowing, but to redirect it through circuits that have been designed to withstand large currents without failure.

Double diode

One of the most commonly used ESD protection strategies is to use two diodes on the pin, one to the supply bus and the other to the ground bus. As we can see from Figure A.14, the two diodes are turned off during normal operation and turn on during an ESD event to provide a very low resistance discharge path. For a

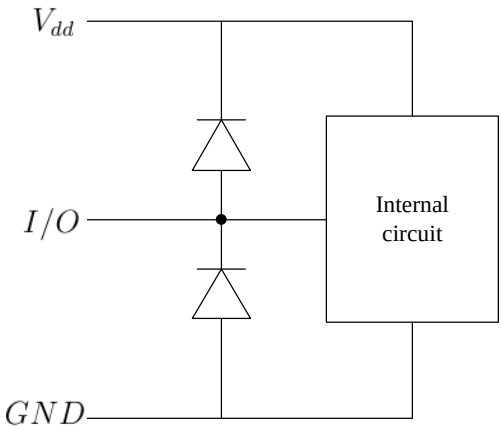

Figure A.14: Double diode for ESD

positive pulse with respect to Vdd, the current passes through the upper diode to the supply pin. For a negative pulse with respect to ground, the current passes through the lower diode and out the signal pin.

The Latchup problem

Latch-up occurs as a result of parasitic bipolar transistors between the NMOS and PMOS devices [15]. The P-substrate forms the base of a parasitic npn transistor, while all N-doped regions , the drain and source of the NMOS transistor, function as emitters. The collector of this transistor is formed by the N-well. The latter, with the P-doped regions , the drain and source of the PMOS transistor, and the P-substrate, forms a parasitic pnp transistor. The npn and pnp transistors form a parasitic thyristor, as shown in Figure A.15, which turns on when triggered and conducts large amounts of current.

Once the thyristor is started, the current flow is usually impossible to interrupt without removing all power from the device. The amount of current drawn can

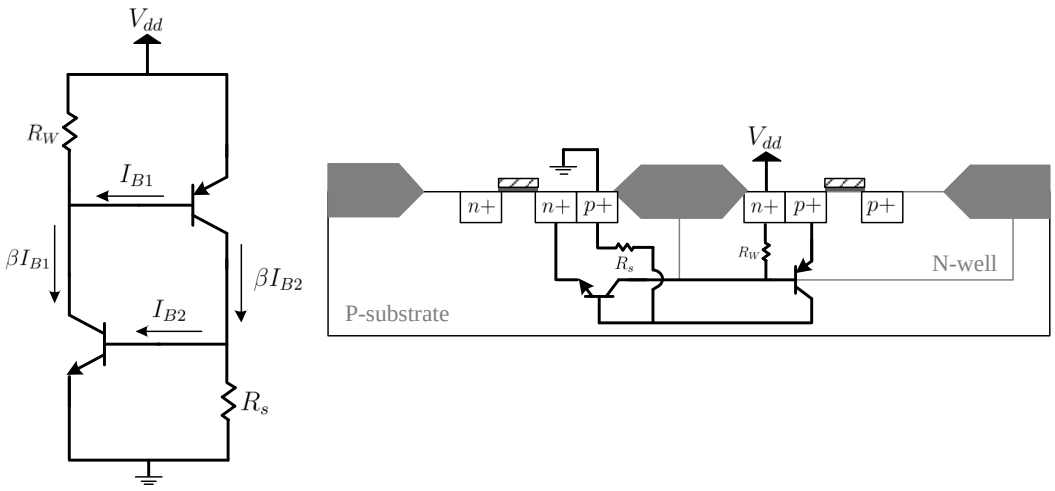

Figure A.15: The thyristor

be so high that it can either overload a power supply or, if the power supply can supply large amounts of current, destroy the device.

The thyristor is an intrinsic part of the CMOS structure and cannot be eliminated. The thyristor must be made as difficult as possible to turn on. ESD can trigger the parasitic thyristor. Thus, ESD protection is a useful not only to protect the circuit from being damaged due to ESD but also to reduce the probability of latchup. Decoupling capacitors are very useful in reducing the probability of initiating the latchup by reducing the voltage supply spikes. Some literatures suggest that a resistor should be placed in series with the supply voltage connection to the integrated circuit. If the thyristor does trigger, this resistor limits the current to a value that no longer poses any danger to the device. another strategy to fight the latchup is to locate the NMOS and the PMOS as far as possible from each other. This reduces the current gain, β, of the parasitic transistors, and the triggering sensitivity of the thyristor is reduced [57]. Surrounding the critical parts of the circuit with guard rings is another way to reduce the probability of latchup. These guard rings form additional collectors for the parasitic transistors. Such collectors are connected to the voltage supply. These additional collectors are placed considerably closer to the base-emitter region of the transistor than the corresponding connections of the complementary transistor. As a result, the charge carriers injected into one of the two transistors is diverted largely via these guard rings to the

voltage supply [57].

Antenna problem

The gate oxide underneath the poly is incredibly thin (in the range of Ångstrom). If the charges accumulated on the poly is sufficiently large, the charges accumulated can damage the gate oxide. This is known as process antenna effect. The maximum amount of charges that can be accumulated on the poly is proportional to the area of the poly. To prevent process antenna, the antenna ratio in the design rule of the respective technology must be followed.

A.5 Design of printed circuit board

A printed circuit board (PCB) is used to mechanically support and electrically connect electronic components using conductive signal traces, generally, mounted on top of a non-conductive substrate.

Originally, every electronic component had wire leads, and the PCB had holes drilled for each wire of each component. The components' leads were then passed through the holes and soldered to the PCB trace. Nowadays, small surface mount parts have been used increasingly instead of through-hole components; this has led to smaller boards for a given functionality and lower production costs.

Traces

Traces are the conducting paths on the PCB that carry the signal from the source to the sink. A right angle in a trace, as shown in Figure A.16(a), can cause radiation. The capacitance increases in the region of the corner, and the characteristic impedance changes. This impedance change causes reflections. To avoid these problems, traces need to be routed at least with two 45^o corners, as shown in Figure A.16(b). To minimize any impedance change, the best routing would be a round bend ,as shown in Figure A.16(c).

To minimize crosstalk between adjacent layers, traces on different layers need to routed with 90^o to each other.

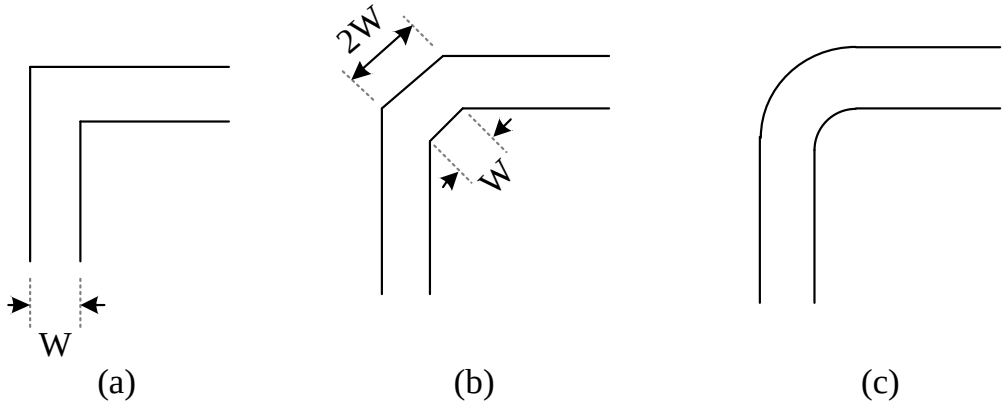

Figure A.16: Different trace routing

Vias

The use of vias is sometimes necessary for routing a signal. But they add additional inductance and capacitance to the trace, and reflections occur due to the change in the characteristic impedance. Vias also increase the trace length.

Vias can result in current loop areas in multi-reference PCB, as shown in Figure A.17. To avoid such a problem, the path of the return current must flow ideally underneath (beside) the signal trace. A good way to realize this is to add some ground vias around the signal via.

Decoupling capacitor

Decoupling capacitors between the power pin and ground pin of the device ensure low ac impedance to reduce noise and to store energy. The target impedance, Z_{target}, that allow for a maximum ripple $r_{allowed}$ in the supply voltage is given by [58]

$$Z_{target} = \frac{V_{dd} \times r_{allowed}}{I_{V_{dd}}} \tag{A-24}$$

where $I_{V_{dd}}$ is the current driven from the supply voltage. For reliable operation of a power delivery system, its impedance spectrum needs to be maintained below

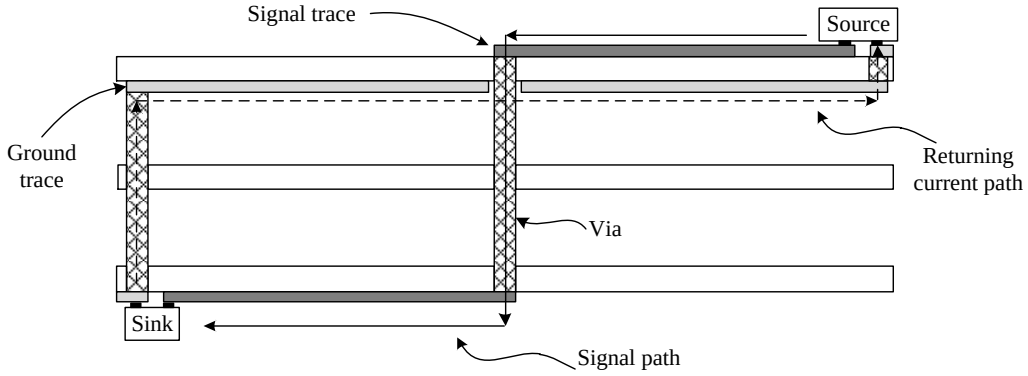

Figure A.17: Current loop due to via

the target impedance at the frequencies from DC to f_{max}, where f_{max} maximum frequency of any chip powered by the power supply [58].

To reach this impedance value over a wide frequency range, several capacitors must be used. A real capacitor consists of its capacitance and a parasitic inductance and resistance. Therefore, every real capacitor behaves as a resonant circuit. The capacitive characteristics are only valid up to its self-resonant frequency (SRF). Above the SRF, the parasitic effects dominate, and the capacitor acts as an inductor. With the use of several capacitors with different values, low ac impedance over a wide frequency range can be provided.

Capacitors with high values have low impedance in the lower frequency range and a low SRF, whereas small-valued capacitors have their SRF in the upper frequency range. This depends on the equivalent series resistance (ESR) and the equivalent series inductance (ESL). A good combination of several capacitors leads to a low impedance over a wide frequency range. To avoid anti-resonance peaks in the impedance spectrum, decoupling capacitors must be chosen such that every two neighboring resonance points apart from each other by a decade.

A power and GND plane can represent a capacitance that ensures low impedance at high frequencies. Therefore, a well-designed board can minimize the number of capacitors required having low-capacitance values. Figure A.18 shows an example of a combination of decoupling capacitors [58]. The gap (increase of the impedance) at around 60 MHz is the result of a missing capacitance. If there were a value

between 100 nF and 10 nF, the Cparallel curve would not increase.

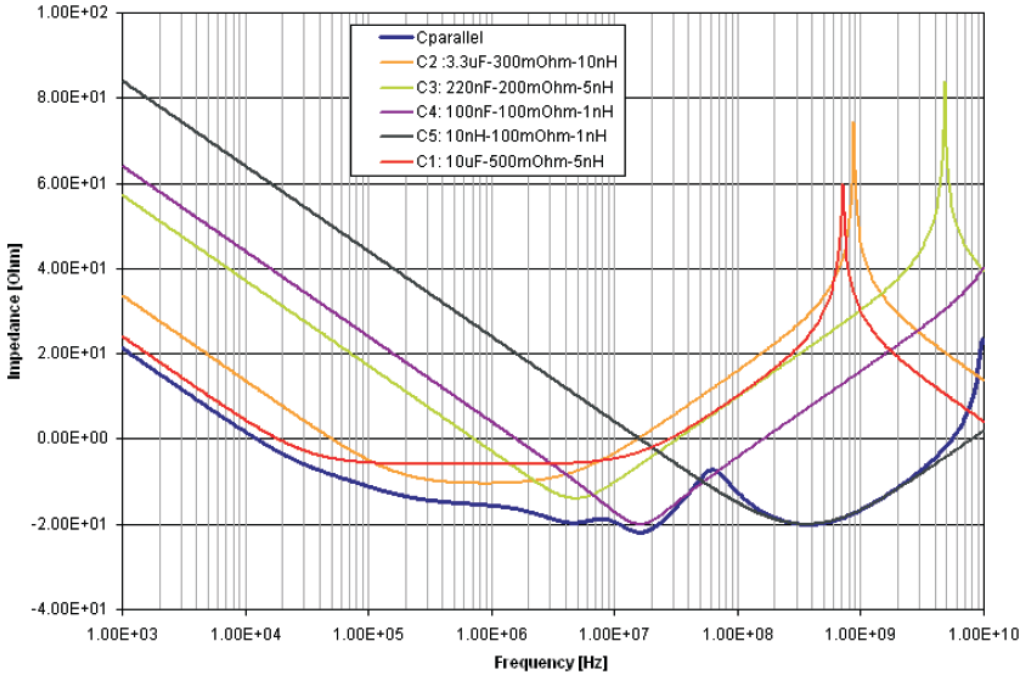

Figure A.18: An example of a combination of decoupling capacitors

The frequency at which serial resonance occurs is determined by the capacitance together with the total inductance, which is the sum of the capacitor's intrinsic inductance plus the mounted inductance. The mounted inductance is the inductance formed by the current loop of the capacitor's pins connecting to the power and ground plane. The larger the area of the current loop, the larger the mounted inductance. Thus, the decoupling capacitor needs to be placed very close to the package to reduce mounted inductance. The smaller capacitors should be placed closer to the package than the larger capacitors because the mounted inductance effects the resonance frequency of the smaller capacitors more than the larger ones.

Transmission Lines

Because the proposed TADC is high speed system, the effects of transmission lines need to be considered. These effects include time delay, reflections, and crosstalk.

Two common structures for trace are shown in Figure A.19. The microstrip structure is illustrated in Figure A.19(a). It has one reference, often a ground plane, and these are separated by a dielectric . The stripline structure is illustrated in Figure A.19(b). It has two references, often multiple ground planes, and are surrounded with the dielectric.

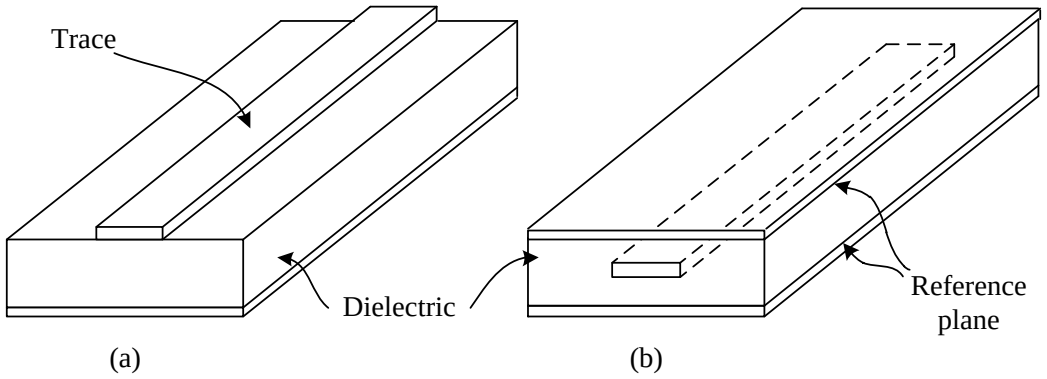

Figure A.19: Two common structures for trace

Signal speed and propagation delay time

A signal cannot pass through a trace with infinite speed. For a certain trace length, the signal needs a certain time to pass it, and this is called the propagation delay time. For the dielectric in a PCB environment, the speed of the signal on a stripline is given by

$$V = \frac{3 \times 10^8}{\sqrt{\epsilon_r}} m/s \tag{A-25}$$

where ϵ_r is the relative permittivity of the PCB dielectric. For a microstrip, it is more complicated because the trace is not surrounded by one dielectric. There are at least two: the substrate under the trace and the air above the trace. If the PCB contains a solder mask, a third medium would be present. Therefore, the calculation of an effective ϵ_r is necessary before determining the signal speed. ϵ_r depends on the width of the microstrip and the distance to the reference plane [59]. An estimate for the propagation time of a microstrip trace is to multiply it the

propagation time for the same trace in a stripline by a factor ϵ_{factor} [60]

$$\epsilon_{factor} = 0.8566 + 0.0294 \times \ln(W) - 0.00239 \times H - 0.0101 \times \epsilon_r \tag{A-26}$$

Characteristic impedance, reflections, and termination

If there are any impedance changes in the signal path (source, trace, vias, connectors, and sink), reflections occur. These reflections cause overshoots and undershoots. The reflection coefficient, ρ, expresses the relationship between the impedance of the transmission line and the impedance of the source or sink.

$$\rho = \frac{R - Z_0}{R + Z_0} \tag{A-27}$$

where Z_0 is the characteristic impedance of the transmission line, and R is the impedance of the source or sink. The two extreme are a transmission line with an open end ($R = \infty$) and a shorted end ($R = 0$). $\rho = 1$ for an open ended transmission line while $\rho = -1$ for a shorted ended one. $\rho = 1$ means that the complete signal reflects at the impedance change location and goes back to the source. To avoid this problem, get no reflections, ρ must equal to 0. This is the case if the impedance at the source has the same value as the characteristic impedance of the transmission line. Therefore, a proper termination is required. The most common termination techniques are series termination, parallel termination, thevenin termination, and AC termination.

Crosstalk

The mutual influence of two parallel, nearby routed traces is called crosstalk. One of the two traces is called the aggressor (this trace carries the signal) and the other one is called the victim (this trace is influenced by the aggressor). Due to the electromagnetic field, the victim is influenced by an inductive and a capacitive coupling. They generate a forward and a backward current in the victim trace [61]. For the stripline traces, the forward and the backward currents cancel each other. While for a microstrip traces, the forward current of the inductive coupling tends to be larger than the influence of the capacitive coupling. Separation between traces will reduce the crosstalk between the traces. Also making the traces close as much

as possible to their reference planes will result in reducing the crosstalk. Crosstalk is inversely proportional to the square of the distance between the traces and their reference planes [62–66].

Power and Ground Planes

An electrical circuit must always be a closed loop. Up to now, only the signal path was discussed but not the path back to the source. With DC, the return current takes the way back with the lowest resistance, as shown in Figure A.20(a). With a higher frequency, the return current flows along the lowest impedance. The lowest impedance path is directly beside the signal, as shown in Figure A.20(b). Figure A.20(b) has lowest impedance because running a signal and its ground return close together results in reducing the inductive impedance of the total path by a factor equivalent to the mutual inductance between the two paths, thus

$$L_{loop} = 2(L - M) \tag{A-28}$$

where L_{loop} is the effective inductance of loop, L is the self-inductance of each half of the loop, and M is the mutual inductance between the two paths. Keeping the signal and return paths adjacent along their length, and therefore maximizing their mutual inductance, will ensure minimum coupling with the magnetic fields around the PCB. If the return path has a obstacle , the return current has to take another way and this results in a loop area as shown in FigureA.20(c). The larger the area, the more radiation and electromagnetic interference (EMI) problems occur. To avoid this problems, the return current should flow directly underneath the signal trace. One solution is to route the signal the same way as the return current flows, as shown in FigureA.20(d).

For high-speed design, a complete ground plane is essential [67]. In a mixed-signal design, several regulated voltages can be present, like digital V_{dd} and analog V_{dd}. The best solution is for every voltage to have its own layer and its own ground plane. But this would result in a huge number of layers just for ground and supply voltages. One solution is to use one ground plane and place the devices by function and route their signals only in their region , as shown in Figure A.21. An alternative is to to split the analog ground and the digital ground to avoid noise coupling between the digital part and the sensitive analog part. If ground plane

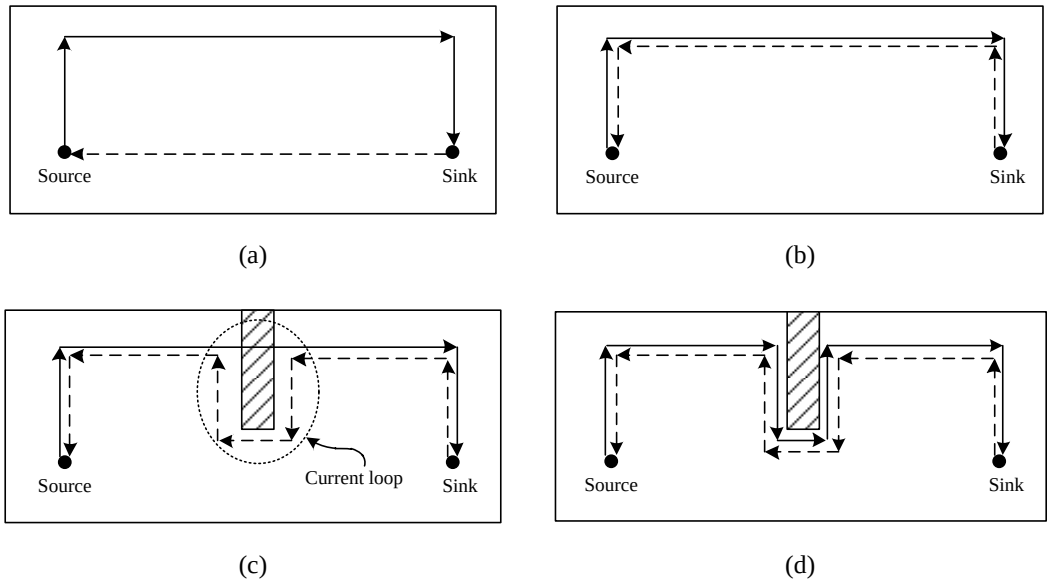

Figure A.20: Return current and resulting loop area

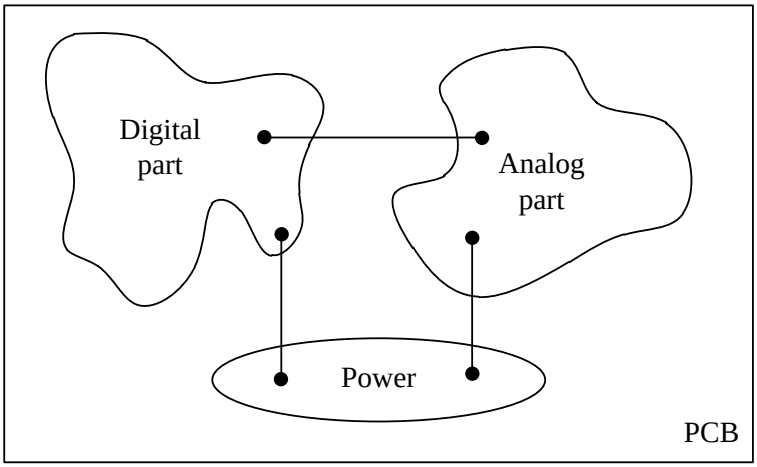

Figure A.21: Common ground plane

splitting is used, any signal referenced to digital ground must not be routed over analog ground and vice versa. This is because the return current cannot take the direct way along the signal trace and so a loop area occurs. Furthermore, the signal induces noise, due to crosstalk. Also, Every ground plane must have its own path

to the common ground to reduce noise.

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