

Development of Non-planar Interconnects for Flexible Substrates using Laser-assisted Maskless Microdeposition

by

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AUTHOR'S DECLARATION

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Steven Tong

Abstract

With the industry striving for smaller devices, new technologies are developed to further miniaturize electronics devices. To this end, realization of 3D/non-planar interconnects, which aim at miniaturizing the interconnects formed between components on the same device, has attracted many researchers. This thesis focuses on a feasibility analysis for developing non-planar interconnects on various flexible substrates using laser assisted maskless microdeposition (LAMM), which is a pressure-less process. There are two types of flexible substrates that are used: double-sided copper substrates separated by a layer of polyethylene terephthalate (PET) as well as a polyethylene terephthalate flexible substrate with surface-mounted resistors. For both substrates, multiple types of experiments were conducted to discover procedures which result in the highest rate of success for forming conductive interconnects. Optimal process parameters and deposition techniques were determined after multiple experiments. After experiments were completed, the resultant substrates were subject to various characterization methodologies including optical and scanning electron microscopy, energy-dispersive X-ray spectroscopy, X-ray diffraction and profilometry. The results of these methodologies are documented in this thesis.

After many types of experiments involving substrate manipulation of the double-sided copper substrates, it was shown that the silver nano-particles were more likely to form a conductive interconnect when a polished slant was fabricated on the substrate.

Many deposition patterns were used for the flexible substrates with surface-mounted resistors. Of these patterns, the two patterns, the ‘zigzag’ and ‘dot solder’ patterns, proved to

have a much higher success rate for creating conductive interconnects compared to the other patterns.

During this study, the results of the experiments using the LAMM process show that this technology has great potential for creating non-planar interconnects on flexible substrates. The experiments however suggest that the process is very sensitive to the material composition and process parameters. As such, with a small change in parameters, the 3D interconnects can fail to be produced. It was also observed that the possibility of silver interconnect fractures is higher where dissimilar materials with different thermal expansion rates are used for the underlying substrates.

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Chapter 1

Introduction

1.1 3D Interconnects for Flexible Substrates

Industries are constantly investigating new technologies and methods that will allow them to produce smaller and faster devices. In addition to miniaturization, the industry strives for more reliable and higher quality devices, which leads to new technologies that grant improvements such as using less material and consuming less energy during operation [1]. Fabrication of 3D interconnects are one such method that has garnered much interest and research. Traditionally, components on electronic devices are designed on planar surfaces; however, as components are designed smaller, wire routing becomes more complex, which can lead to longer signal delays due to inefficient routing patterns while compromising the miniaturization goal. As the industry is constantly striving for faster devices, the aforementioned problem needs to be addressed. By introducing a third dimension into devices, routing patterns can be more efficiently developed. This also allows substrates to be stacked, which allows for shorter interconnects due to having more components in proximity. Shorter interconnects allow shorter signal travelling time, and stacked substrates will allow components to be rearranged such that there can be optimal component arrangements which reduce the interconnect length.

Stacked substrates also reduce the size of devices as well as allowing different types of substrates to be combined on a single device with less difficulty. A very popular technology that stacks substrates is wire bonding, which has been available for many decades. During these decades, devices have been constantly designed to be smaller, to a point where wire bonding is unable to meet some of the demands in miniaturization. Due to the desire to miniaturize devices

further, other technologies have been introduced such as through-silicon VIAs and direct-write printing. Certain 3D interconnect technologies such as Aerosol® Jet deposition also allow interconnects to be formed on non-planar surfaces, allowing manipulation of substrate designs as well as forming interconnects on flexible substrates.

Although this technology holds very much promise, the substrates are usually restricted to rigid substrates due to the sintering process, which takes place after deposition. The sintering process will allow the deposited material to adhere well to the substrate, with the most common form of sintering being oven or hotplate curing. Oven and hotplate curing have no issues with rigid substrates, but flexible substrates are generally unable to endure the high temperatures without distorting. This causes a problem, as flexible substrates are used in many applications, and miniaturization of components on flexible substrates are also highly desired. Some flexible substrate applications include devices that are disposable; making a need for a fast, cost-efficient and low temperature process for creating 3d interconnects on flexible substrates.

1.2 Thesis Objective

In this study, a method for creating 3D interconnects is applied to various flexible substrates to investigate the feasibility of this method, while also adjusting experimental parameters to optimize the process. The method involves using Aerosol® Jet technology, which is a relatively new technology that has been introduced for creating 3d interconnects. This pressure-less process also does not have multiple stages during the formation of the interconnects, making the process a fast and low-cost approach to creating interconnects. The formation of the interconnects in this process is also laser-assisted, which allows for localized sintering that will not damage heat-sensitive substrates. The flexible substrates in which the interconnects are printed upon in this study are planned to be used for a variety of applications

such as electrocardiography purposes. Flexible substrates are excellent for this purpose, as they can conform to the movement of a person's body as well as being comfortable and unobtrusive to have under clothing. Research is conducted on developing non-planar interconnects upon the surface of flexible substrates for the purpose of analyzing a fast and cost-efficient method of forming non-planar interconnects that can be used not only for electrocardiography purposes, but also in any situation where non-planar interconnects are manufactured in large succession.

1.3 Outline

The thesis is outlined as follows: Chapter 1 contains the introduction and goals of the project. Chapter 2 includes literature review of some 3d interconnect technologies currently in existence as well as their applications. Chapter 3 presents details on the technology, laser-assisted maskless microdeposition, which is used for the experiments. Chapter 4 contains the experimental procedures and results of experiments performed on double-sided copper substrates that have been separated by a layer of polyethylene terephthalate. Chapter 5 contains the experimental procedures and results of experiments performed on flexible substrates with surface mounted resistors. Lastly, Chapter 6 presents the conclusions drawn from the experiments as well as recommendations for future work.

Chapter 2

Literature Review

2.1 3D Interconnect Techniques

There are a variety of 3D interconnect techniques that are available, with some techniques already in use within the industry. This chapter provides background on the advantages and shortcomings of various 3D interconnect techniques, namely wire bonding, through silicon VIAs and thin film deposition.

2.1.1 Wire Bonding

One of the first technologies that was discovered and used in the industry for creating 3D interconnects was wire bonding. This technology involves physically stacking substrates on top of one another and then routing wires that travel from one substrate to another substrate that is above or below it, as shown in Figure 1.

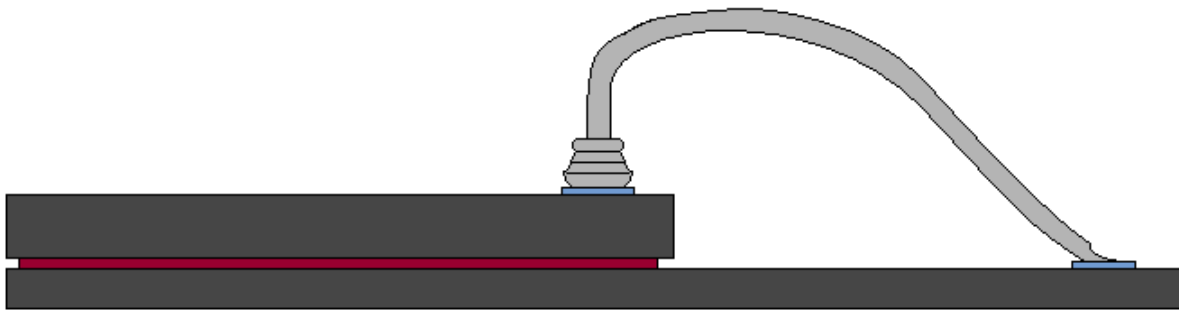


Figure 1 – Schematic showing an example of wire bonding on stacked dies, adapted from [2]

There are a variety of techniques to form a wire bond; however, most of the techniques rely on the same principle. The main principle consists of feeding a wire through a capillary, in which the wire is then melted at the tip of the capillary to form a ball. The capillary then presses

the newly formed ball of wire onto the contact pad. During contact, ultrasonic waves are then emitted into the ball, which allows the ball to be welded onto the surface of the contact pad. Once the ball is welded, the capillary moves towards the second contact pad, while feeding the wire out from the capillary. The capillary then presses down on the second contact pad, welding the wire to the second contact pad. Afterwards, the wire is sheared from the capillary, resulting in a wire ball bond formed on two contact pads. The most predominant material that is used for wiring was gold. However, due to increases in the prices of gold, other materials such as copper have been considered [3, 4].

Wire bonding has existed for many decades, and as such has become a very mature method and has been used in very many industries for creating electronics. By allowing the stacking of substrates, wire bonding reduces the total system size of electronics as well as reducing the signal travel time. Heterogeneous integration of different substrate materials is also an option when stacking substrates, as the components are no longer required to be placed on the same substrate [5]. This is particularly useful for many purposes such as sensor array applications, which rely on specific materials and require high-density circuits [6]. Wire bonding is excellent in many cases; however, as the industry strives for smaller electronics, new methods and technologies are discovered in order to create smaller interconnects.

With regards to flexible boards, wire bonding has a number of shortcomings. The first shortcoming is the suspended wires, which can be applied to all 3D interconnect applications. The suspended wires increase the system size slightly due to the wires looping from one substrate to another. This also causes some substrates to require a protective cover or mold to prevent external forces from damaging the wire bonds. Although stacking of substrates reduces the system size, the nature of wire bonding causes the entire system to be larger compared to

other techniques used in a similar fashion. Lastly, the formation of wire bonds requires the capillary to press down the ball bond onto the substrate. Rigid substrates can tolerate the pressure; however, when used on flexible substrates, there can be cases of permanent deformation due to the pressure induced by the ball bond creation process [7]. This is not to say that wire bonding on flexible boards is impossible. Wire bonding on flexible boards can still be accomplished through use of more heat resistant substrates or compromising the speed, temperature or wire composition of the process [8].

2.1.2 Through Silicon VIAs (TSVs)

A new 3D interconnect technology that has begun to gain much attention is that of through-silicon VIAs (TSVs). TSV technology uses VIAs created in substrates to form interconnects, which can be a lengthy process, but can provide very short interconnects. The process is outlined in Figure 2. A VIA is first etched into the substrate, as shown in Figure 2(b). Normally, the etching process is performed with the use of lithography and dry etching processes such as reactive ion etching [9, 10]. However, there has also been some success with using laser etching in order to reduce the cost of the overall process [11, 12]. Once the VIA has been formed, an insulation layer is deposited on the walls of the VIA, shown in Figure 2(c), which can be performed with deposition techniques such as chemical vapor deposition. Next, a conductive material is used to fill the VIA, shown in Figure 2(d). This conductive material becomes the interconnect itself, which connects the bond pad to the desired location on the substrate. If one is required, a diffusion barrier layer can also be deposited along the walls of the VIA before filling the VIA with the conductive material [13].

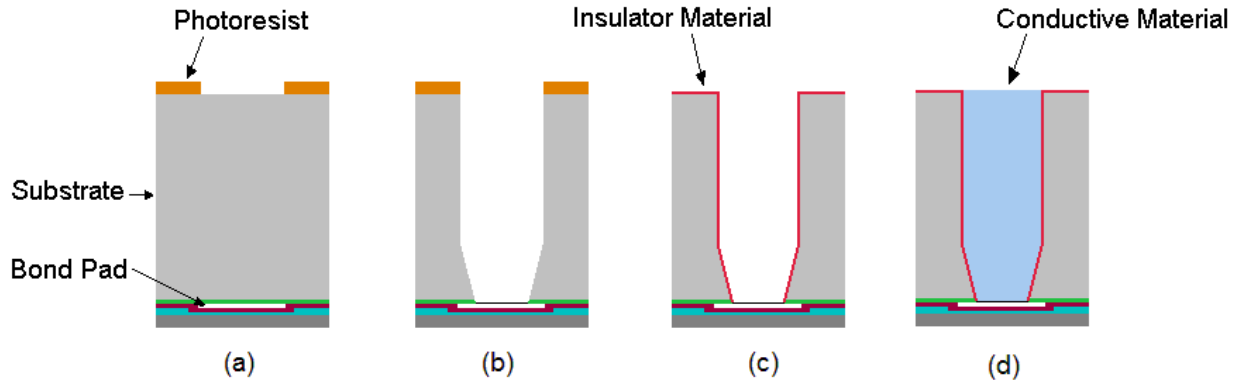


Figure 2 - TSV formation process, adapted from [11], showing (a) photoresist deposition, (b) etching of the VIA, (c) deposition of the insulator material, and (d) deposition of the conductive material.

Compared to wire bonding, TSVs are able to provide a smaller system size, due to the interconnects residing inside the substrate rather than outside. Consequently, the interconnects are also shorter, which reduces signal travelling time as well. The process to creating a TSV, however, is an extremely lengthy process, which generally involves many different stages of manufacturing due to the various etching and deposition processes that are required. Due to the number of stages in this process, the cost of producing TSVs becomes a major issue. Variations of producing TSVs have been investigated, such as using laser etching in the place of reactive ion etching or using mechanical caulking when assembling the substrates. However, for the case of laser etching, the resultant TSVs were intended for applications that valued low cost and did not require high-speed signal transmissions [11]. The use of mechanical caulking during assembly can increase the speed of the process, while reducing the cost [14]. Although an improvement in terms of yield, it remains that the process is still multi-staged and require etching due to the nature of TSVs.

2.1.3 Thin Film Deposition using Aerosol Jet® Direct Write Printing

Another technology for creating 3D interconnects that has begun to gain attention is thin film deposition. As opposed to wire bonding, which creates an interconnect suspended in air, and TSVs, which create interconnects within the substrates, thin film deposition aims to create conformal interconnects along the face of the substrate. One such technology that can perform this task is the Aerosol Jet® system. This system includes a pattern-generating device, such as an ink deposition nozzle or laser optics, as well as a positioning stage that is computer controlled [15]. The process works by generating a mist of the conductive material, which is then injected onto the substrate. The Aerosol® Jet system is capable of printing on a large variety of substrates, such as metals, glass, ceramics, solar cells, polymer substrates and resins [16, 17, 18, 19]. This system is also capable of depositing a variety of materials, such as metals, polymers adhesives and even single-walled carbon nanotubes, into complex patterns that can be made on both planar and non-planar surfaces [20, 21, 22].

By controlling the speed of the injection nozzle and the volume of silver that is deposited, a variety of shapes and paths can be formed. Due to the material being in an aerosol form, the substrate is not limited to material or shape as long as there is proper adhesion between the deposited material and the substrate. This allows the process to create tracks or patterns of conductive material over non-planar surfaces. A schematic showing an example of the types of interconnects that can be formed is shown in Figure 3.

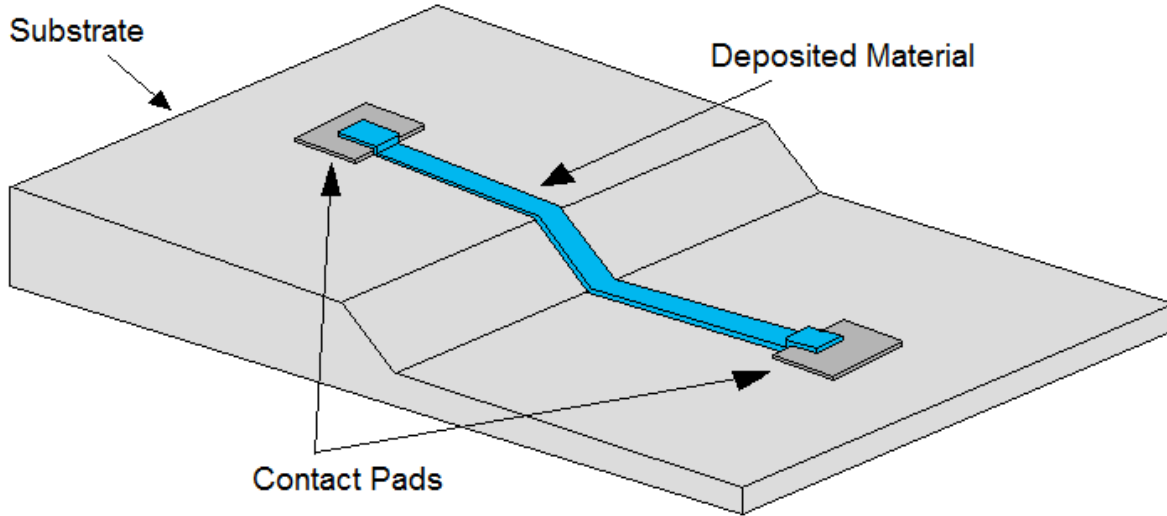


Figure 3 – A schematic of deposited material using a direct-write deposition technique

The direct-write technology is an additive process, as opposed to the traditional fabrication processes used in many manufacturing methods, particularly in integrated circuits, which use subtractive processing methods such as photolithography, nano-imprinting or various etching techniques [23, 24]. The subtractive method is a multi-stage process, which is similar to how TSVs are fabricated, with the use of chemical etching and photolithography. By using an additive process, there is no need for chemical etchants or masks, which are rather expensive. In addition, a mask must be created for each pattern that is desired when using a subtractive process, but with an additive process, only a CAD model is required for each pattern that is desired [25]. This makes the direct-write technology a much faster and cheaper alternative to the existing subtractive methods for creating micro-sized patterns on substrates. However, the direct-write technology does not fare as well for larger scaled patterns, as it would take much more time in order to draw the pattern onto the substrate. Using direct-write technology on patterns with the

width of multiple millimeters can be compared to that of painting a wall with a toothbrush. Some images of deposited patterns are shown in Figure 4.

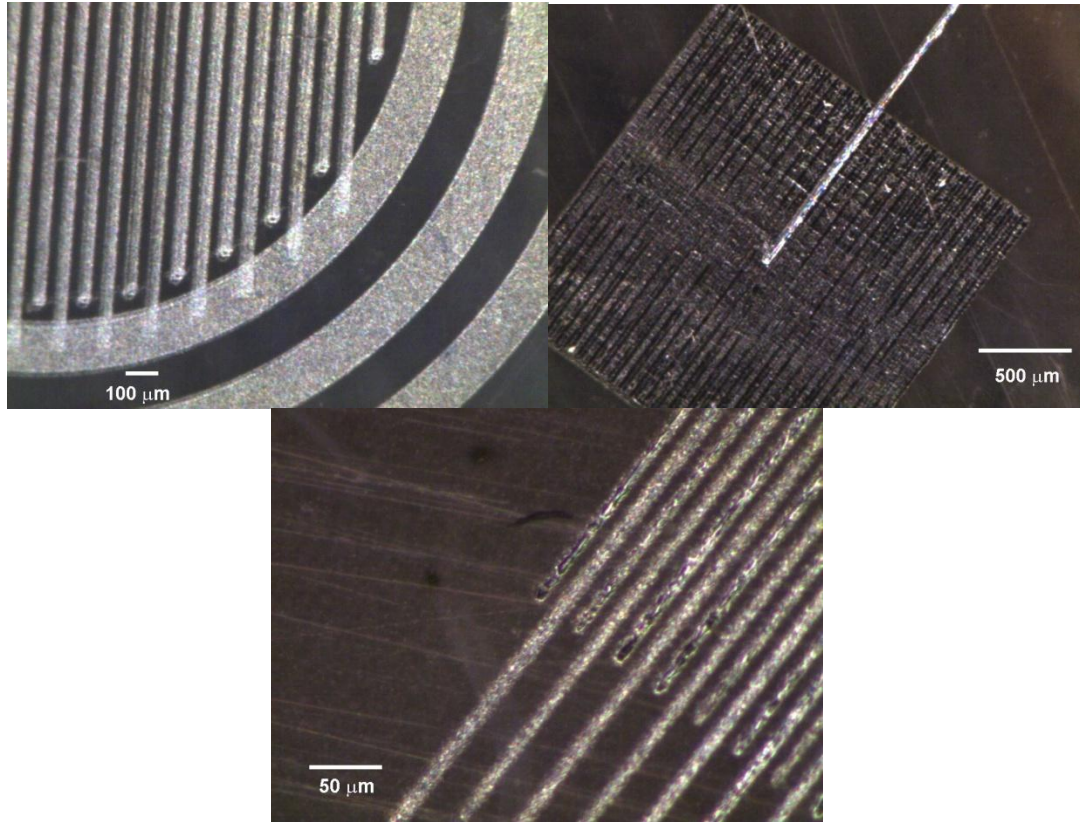


Figure 4 - Images showing various patterns of silver tracks deposited using an Aerosol Jet® Deposition system. Patterns fabricated at the Multi-Scale Additive Manufacturing lab of the University of Waterloo.

After the material has been deposited, sintering will take place in order to cure the newly deposited material. This process can be done in a variety of ways, such as with a laser, hotplate, oven curing or electrical sintering [26, 27]. For thermally sensitive substrates, sintering methods such as laser and electrical sintering that can be focused towards a specific area are generally preferred as these methods will only heat the area in which the material has been deposited, rather than the entire substrate, which can lead to thermal expansion problems or damaging of the substrate. Although these methods are slightly more sophisticated, the sintering process can be performed much faster.

The system size of a substrate does not increase too greatly with the use of direct-write printing, since the deposition is deposited as a thin film that is on the surface of the substrate, making the system size reduction comparable to that of TSVs. Compared to wire bonding however, the direct-write printing process provides a much smaller system size.

The Aerosol Jet ® process does not perform very well for high frequency applications, where edge accuracy and surface roughness are extremely important. The Aerosol Jet ® system is known to have variations in edge accuracy and occasionally overspray, which produces a varying width of the deposited track. Inconsistent surface roughness can lead to signal loss in high frequency applications, due to the skin effect, where the current travels close to the outer edge of the conductive material. Overspray can be reduced by controlling the process parameters, but it is extremely difficult to prevent it entirely. Marinov V and Atanasov Y approached this problem and developed a method termed “Enhanced M3D”, which introduces micromachining to produce a substrate with a channel that will contain the deposited material, shown in Figure 5 [28]. The channel can be fabricated with a number of micromachining methods, such as laser cutting, chemical etching, electron-beam micromachining, etc. The purpose of the channel is to contain the deposited material such that overspray has a very minimal effect on the system. Once tested, Marinov V and Atanasov Y found that the signal quality increased significantly [28]. Bhattacharya S and Marinov V used a similar approach with laser etching trenches within a substrate and achieved the goal of creating interconnects within a close proximity of around 6 μm [29]. Although this method is capable of producing interconnects for high frequency applications, the inclusion of micromachining increases costs greatly, and it must be remembered that cost is one major factor that makes direct-write printing very appealing.

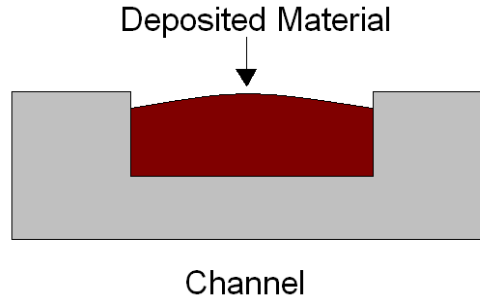


Figure 5 - Schematic showing a cross-section of the deposited material inside the fabricated channel, adapted from [28]

2.2 Applications

3D interconnects can be used in a variety of applications. With wire bonding being available for the past few decades and being one of the most widely used techniques for creating 3d interconnects, it comes as no surprise for this technology to be used in a variety of industries, such as automotive, computer, communication and network applications [30]. Although the applications remain the same, a desire to switch from gold wire bonding to copper wire bonding is apparent, especially with the increasing prices on gold.

Some TSV applications include MEMs, mobile applications, integrated circuits and a variety of sensors such as CMOS image sensors [31, 32, 33, 34]. TSVs can be applied to any industry that uses devices that contain stacked dies or wafers, making TSVs applicable to many industries immediately. Though there are not many devices using TSVs that are on the market at the moment, TSVs can certainly miniaturize devices, and much research is being performed to make this technology more affordable.

Aerosol® Jet direct write technology can also be used in many applications, such as solar cells, radio-frequency devices, touch screen displays, integrated circuits and automotive applications [16, 35, 36, 37, 38]. Recently, a “smart wing” was created for a small aerial drone in a joint project involving Optomec, Aurora Flight Sciences and Stratasyss. The Aerosol® Jet

process was used to print circuits, sensors and an antenna on the wing of this aerial drone [39]. Due to this technology being capable of producing thin film interconnects, there exists a lot of potential on using direct write technology for flexible substrates. Due to the nature of flexible substrates, any devices mounted upon them must be able to maintain functionality amidst the stresses upon bending the flexible substrates. Thin film deposition is one method of producing interconnects capable of withstanding stress on flexible substrates. Flexible substrates also bring with itself many industry applications, such as temperature and pressure sensors, smart cards, electrocardiogram patches and light emitting diodes [28, 40].

2.3 Summary

There are many different types of techniques for creating 3D interconnects on various substrates. Wire bonding was one of the earlier techniques discovered and is still widely used in industries today for creating 3D interconnects. This allows for the stacking of substrates and the wire bonds are formed from one substrate layer to another. Due to the nature of suspended wires in wire bonding, the wire bonding process has limitations on miniaturization. The wire bonding process also has some difficulty with flexible substrates, as the pressure from the process has the potential to permanently deform the substrates.

Different techniques have been discovered and researched to address some of these limitations. One such technology is through-silicon VIAs (TSVs), which is based on creating interconnects within substrates rather than the traditional exterior methods such as wire bonding. By having the interconnects within the substrates, further miniaturization can be reached; however, the process is time consuming and costs of TSVs is extremely high due to the various processes involved. Many flexible substrate applications are towards disposable devices, which make cost an extremely important factor when manufacturing.

Thin film deposition techniques are fast and cost-efficient, which make this process excellent for creating 3D interconnects for flexible substrates, including those of which are used for disposable applications. The thin film deposition process works by depositing aerosols of material onto a substrate to form conformal interconnects on the exterior of the substrate, followed by sintering. Since the interconnects are conformal, miniaturization is still achieved. Very little research has been documented in using thin film deposition for flexible substrates, and the published documentation that is available has not performed any optimization of parameters. For many of the published experiments regarding Aerosol® Jet technology, the sintering methods performed were with the use of a hotplate. As such, there is a lack of knowledge in this field with regards to using laser sintering in addition to Aerosol® Jet deposition. The goal of this work is to investigate the usage of Aerosol® Jet technology incorporated with laser sintering for various flexible substrates and find optimal parameters for creating thin film 3D interconnects on the aforementioned flexible substrates.

Chapter 3

Laser Assisted Maskless Microdeposition

3.1 LAMM Process

The 3D-interconnect technology that is used in this research study is called a laser assisted maskless microdeposition (LAMM) process, which is based on the Aerosol Jet ® direct-write technology, with a continuous-wave single-mode erbium fiber laser (ELR-20-1550, IPG Photonics Corporation, Oxford, Massachusetts) with a wavelength of 1550 nm that has been installed into the system. The laser assisted maskless microdeposition (LAMM) process consists of two main steps. The first step is microdeposition, where nano-particles suspended in a liquid are atomized and then deposited onto the substrate. The second step is laser sintering, where a laser is used to pass over the newly deposited nano-particles, sintering them and causing them to agglomerate. The main components of the system are shown in Figure 6. The atomizer and positioning stage are both manufactured by OPTOMECH Inc.

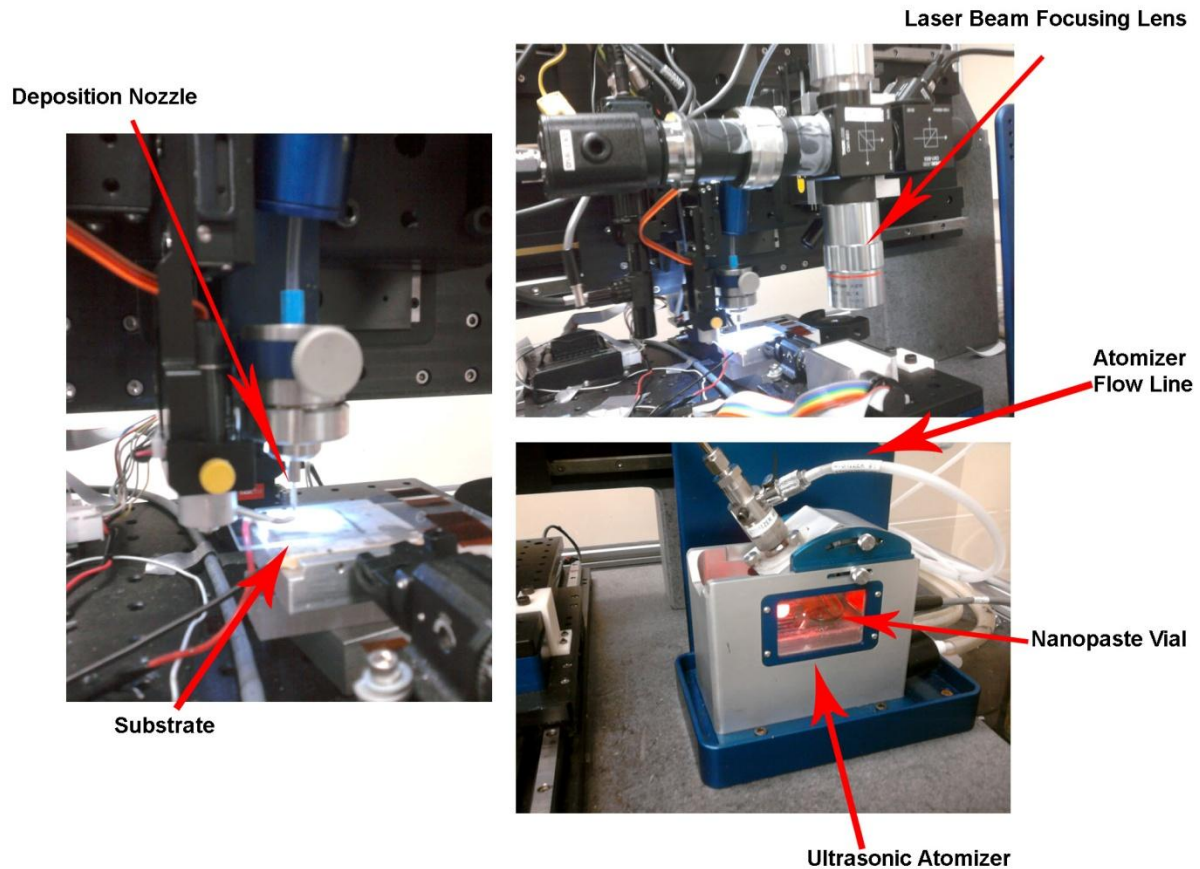


Figure 6 - The main components of the LAMM system: Atomizer (bottom right), Deposition Nozzle (left), Laser (top right).

3.2 Deposition Process

The LAMM process begins at the ultrasonic atomizer, where a VIAL of nano-particles is suspended in a liquid. This solution is generally labeled as nano-paste. When ultrasonic waves approach the nano-paste, droplets of the solution are released into the air, forming a dense mist from the accumulation of released droplets. This phenomenon of the ejection of droplets that occurs during atomization can be described with the cavitation and capillary wave hypotheses [41, 42]. The size of the droplets are a function of the density, viscosity, ultrasonic wave frequency and liquid surface tension [42, 43]. Larger droplets are formed with high values in surface tension and viscosity, while smaller droplets are formed with high values in density and

ultrasonic wave frequency. Thus, the thermo-physical properties of the nano-paste are required to be in a specific range. This can be achieved by diluting the nano-paste before it is placed within the atomizer [20].

After the nano-paste has been atomized into a mist, the mist is carried towards the deposition nozzle with the help of a neutral gas such as N_2 . Once the stream of mist arrives at the deposition nozzle, another flow of a neutral gas, called sheath gas, is introduced into the stream, as shown in Figure 7. This secondary flow of gas will focus the nano-particles stream such that the diameter of the stream that exits the nozzle can be as small as 10% the diameter of the nozzle, which typically has a diameter between 100 and 250 μm . The deposited patterns can have widths as small as 10 μm [20].

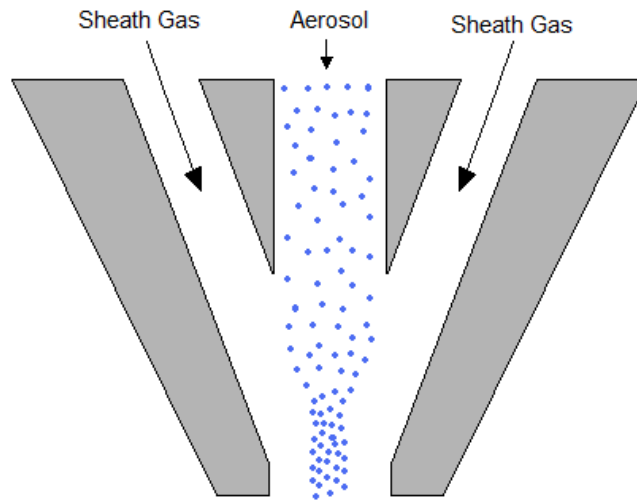


Figure 7 - Diagram showing the main stream of nano-particles and the sheath gas that is introduced in the nozzle, adopted from [19].

The nano-particles are then deposited onto the desired substrate, which is mounted upon the positioning stage. This stage is controlled by a motion control module and has two degrees of

freedom, allowing a large variety of patterns to be formed by moving the positioning stage while the nano-particle stream is exiting the deposition nozzle. A heater can also be mounted upon the stage, which can heat the mounted substrate during deposition.

Once the deposition has completed, laser sintering will take place with the use of a continuous-wave single-mode erbium fiber laser with a wavelength of 1550 nm, which was installed onto the system, as seen in Figure 6. By having the laser mounted on the same stage as the deposition nozzle, the axis of motion is retained, allowing the laser to trace the same deposited path of material by executing the same path adjusted with an offset.

3.3 Laser Specifications

The laser has a focal length of 40 mm and an unfocused diameter of 5 mm, shown in Figure 8. The diameter of the beam at the focal point can be calculated with Equation (3.1):

$$\omega_0 = \frac{4\lambda f}{\pi D} \quad (3.1)$$

where ω_0 is the focal point diameter, λ is the laser wavelength, f is the focal length and D is the unfocused beam diameter. Using Equation (3.1), the diameter at the focal point can be calculated as 15 μm . The angle θ , as seen in Figure X can be calculated with the use of Equation (3.2):

$$NA = n \sin \theta \quad (3.2)$$

where N is the numerical aperture, n is the index of refraction of the medium and θ is half of the angle that represents the largest cone of light that can exit the lens. With the numerical aperture of the objective lens as 0.14, θ can be solved for, which will be used in a later equation.

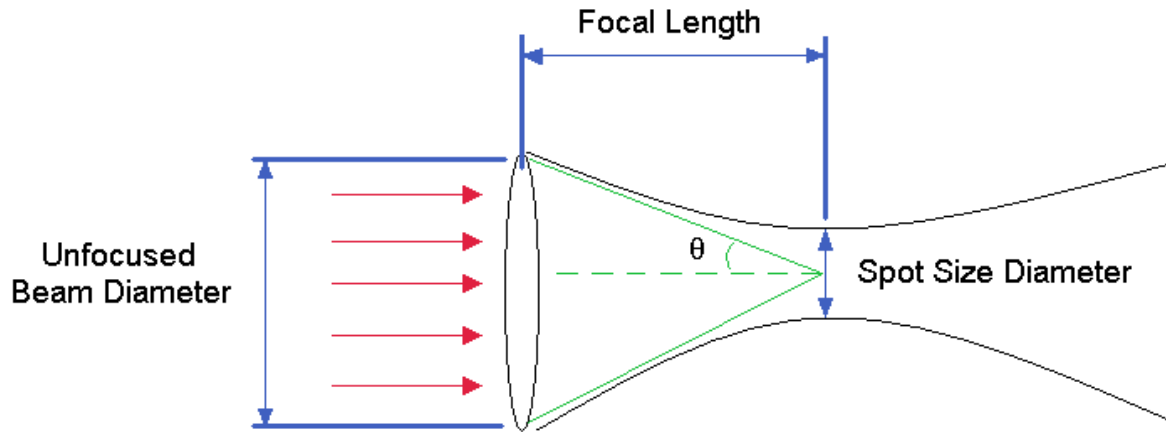


Figure 8 - Diagram showing the beam size as the unfocused beam travels through the lens

The beam shape is a TEM₀₀ Gaussian beam, which means that the laser spot size can be characterized with the use of Figure 9 and Equation (3.3):

$$r^2(z) = r_0^2 + 4\theta_1^2 (z - z_0)^2 \quad (3.3)$$

where r is the diameter of the beam with respect to distance z from the focal point, r_0 is the beam diameter at the focal point, θ_1 is twice the angle of θ which was solved for earlier, and z_0 is the offset. With this equation, the laser spot size can be calculated and controlled with the distance at which the object to be irradiated is placed from the laser. The laser beam produced is capable of emitting 0.5 to 3.5 W of power to the desired area. With laser powers under 2 W, the laser beam does not act consistently and is unstable at times. In order to allow use of low laser powers, a splitter and damper were installed onto the processing head of the laser, which reduces the power of the laser by 50%. This splitter also enables the attachment of a camera to view the area of irradiation from the point of view of the laser.

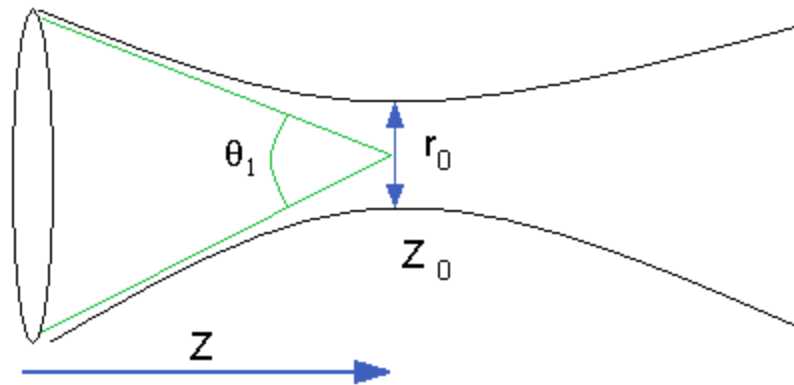


Figure 9 - Diagram showing variables used in Equation 3.3 for laser spot size

Once the laser irradiates the deposited material, the material will begin to sinter. During this process, the solvent that the nano-particles were originally suspended in will evaporate, and the nano-particles will begin to agglomerate, as shown in Figure 10 and 11. By applying the laser energy to the nano-particles, the density of these particles would increase, resulting in an increased electrical conductivity [44, 45, 46].

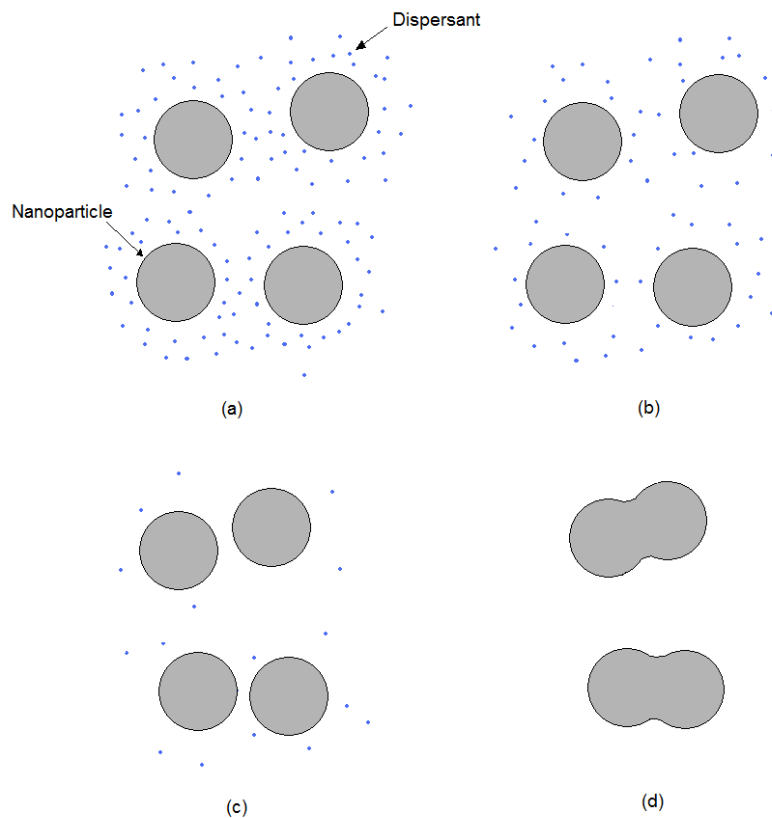


Figure 10 - Process of agglomeration: (a) before sintering, (b) solvent evaporation, (c) beginning of agglomeration, (d) end of agglomeration. Image adapted from [20]

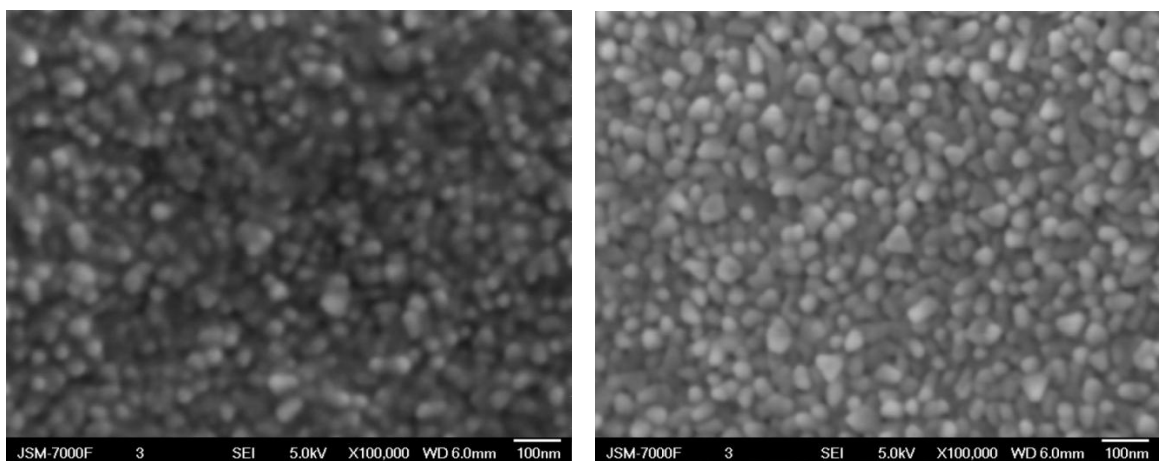


Figure 11 - SEM images of silver nano-particles sintered at 0.44 W (left) and 1.24 (right). Image taken from a JEOL JSM7000F field emission scanning electron microscope

3.4 LAMM Process Parameters

The parameters that are used to control the LAMM process are listed in Table 1. For proper atomization, the atomizer voltage should be higher than the threshold value of 37-48 V, while the viscosity of the nano-paste should be within (0.7 – 30 cP). In order to successfully atomize the nano-paste, the vial containing the nano-paste must also be placed in a specific location relative to the atomizer. The atomizer gas flow rate, deposition nozzle velocity and number of layers control the amount of silver that will be deposited onto the substrate. The sheath gas flow rate in combination with the atomizer gas flow rate controls the width of the track that will be deposited. The substrate temperature will determine how well the nano-particles will adhere to the surface on contact. The laser power, velocity and beam size control the amount of power that is introduced to the substrate during sintering [20].

Table 1 - LAMM process parameters

Atomization	Microdeposition	Laser Sintering
Atomizer voltage	Atomizer gas flow rate	Laser power
Nano-paste viscosity	Deposition nozzle velocity	Laser velocity
Nano-paste vial placement	Number of layers	Laser beam size
	Sheath gas flow rate	
	Substrate temperature	

The nano-particles that are deposited for the experiments included in this study are silver nano-particles suspended in a liquid. The suspension was 45-55wt% of silver with an average particle size of 60 nm in ethylene glycol ($C_2H_4(OH)_2$) provided by Cabot Superior Micro Powders. The Aerosol® Jet is also capable of depositing a variety of materials, including other conductor inks such as platinum, palladium and copper [47].

Chapter 4

Double-sided Flexible Copper Substrates

This chapter details the experiments and results of depositing non-planar interconnects on double-sided copper substrates separated by a layer of polyethylene terephthalate (PET). The initial goal was to deposit a non-planar interconnect on a chamfered via. Due to technical complications, numerous types of substrate modifications were performed to simplify the process. Results for each modification are detailed in their respective sections.

4.1 Materials

For the purpose of these experiments, the substrate that was used was a double-sided flexible copper substrate separated by a layer of polyethylene terephthalate (PET), provided by Assembly Automation Alternatives (AAA). The copper layers were adhered to the PET layer through the means of an epoxy. A cross-sectional diagram of this substrate is shown in Figure 12 and an optical image of a side view is shown in Figure 13. The total height of the substrate is 0.21 mm.

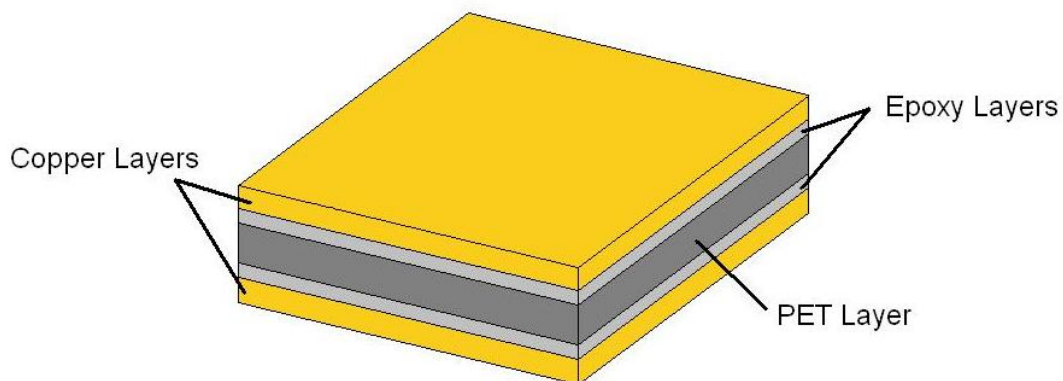


Figure 12 - Cross-sectional diagram of copper and PET substrate

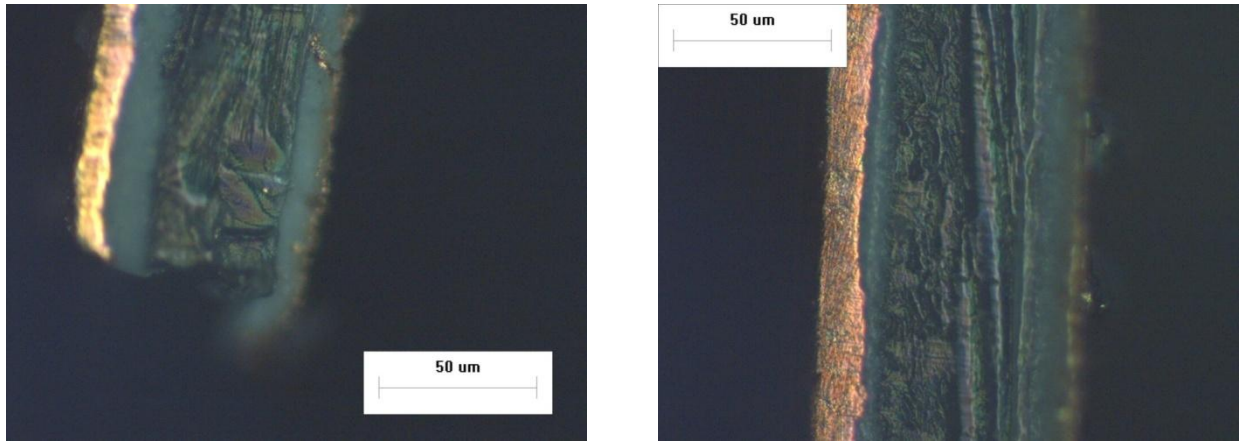


Figure 13 - Side view of double-sided copper substrates as seen from microscope

The goal for the double-sided copper substrates was to successfully form a silver interconnect that would travel from the top layer of copper to the bottom layer of copper while passing over the PET layer. For the specific application at AAA, the interconnect was requested to travel through a micro-sized circular chamfered VIA within the substrate, as shown in Figure 14. The diameter of the top of the chamfered VIA was desired to be around 0.5 mm. Since the provided double-sided copper substrates did not include a chamfered VIA, it was required to manufacture this VIA.

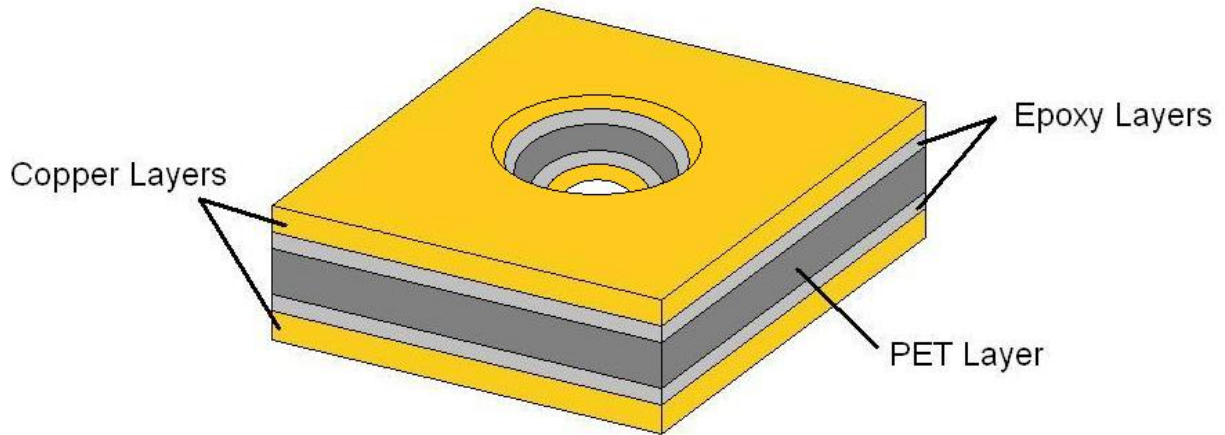


Figure 14 - Cross-sectional view of copper and PET substrate with a chamfered VIA

4.2 Characterization Methodologies

After depositing and sintering, the substrates were examined with the use of optical imaging and scanning electron microscopes. For optical imaging, a machine vision camera (EO-3112, Edmund Optics, Barrington, New Jersey, USA) was used in combination with a zoom imaging lens (Techspec® VZM 1000I, Barrington, New Jersey, USA) and a fiber optic illuminator (Dolan Jenner MI-150, Barrington, New Jersey, USA). The scanning electron microscopes used were a LEO 1530 FESEM (LEO 1530, Zeiss, Oberkochen, Germany) and a JEOL JSM-6460 SEM (JSM-6460, JEOL Ltd, Tokyo, Japan) with energy-dispersive X-ray spectroscopy (EDS). For further analysis, an optical profiler (WYKO NT1100, Veeco Instruments Inc, Plainview, New York, USA) was used to examine the profile of the silver track and a micro x-ray diffraction machine (Rigaku SA-HF3, Rigaku Corporation, Tokyo, Japan) was used to observe the crystalline structure of the substrate.

The substrates were also measured for resistance after deposition and sintering with a digital multimeter (Omega® HHM32, Omega® Engineering Inc, Stamford, Connecticut, USA)

in order to determine the successfulness of the silver interconnects. Although these measurements are not an exact representation of the resistance value due to the contact resistance of the measurement probes, an approximate resistance value can be obtained to determine the resistance of the track. In order to determine a more accurate resistance value, a source-measure unit (Keithley 2612 SourceMeter, Keithley Instruments, Cleveland, Ohio, USA) was used.

4.2 Experiments involving Substrates with Chamfered Vias

4.2.1 Fabrication of a Chamfered Via

Many different fabrication methods were proposed. A vast number of these methods were discarded due to inconsistency. Some of these methods included physically puncturing the substrate with a sharp object as well as laser drilling. The major issue with the majority of these methods rested upon the inability to create substrates with consistent VIAs. Each VIA produced using these methods was unique and thus, would not provide meaningful experimental results. It would also not be a good representation of the chamfered VIA that was desired.

The method for manufacturing the chamfered VIAs that was chosen was based on lowering a spinning conic-shaped drill head onto the substrate. The substrate would be placed upon a hard surface while the conic-shaped drill head would be lowered extremely slowly into the substrate. This procedure is shown in Figure 15. After drilling, the substrates are washed with isopropanol and sonicated. Once finished, the samples would then be ready for deposition.

Due to the machining of the chamfered holes, the walls of the holes were not very smooth, but attempts to create an interconnect between the two layers of copper using these substrates were performed regardless.

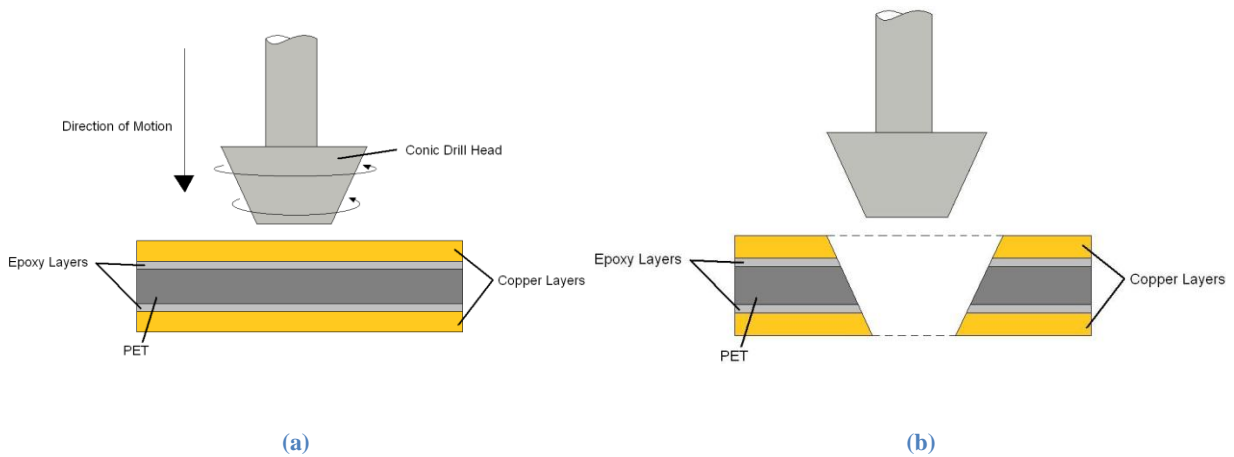


Figure 15 – Cross-sectional schematic showing the manufacturing process for fabrication of chamfered VIAs (a) before and (b) after

4.2.2 Depositing the Silver Track for a Substrate with Chamfered Via

In order to form an interconnect to join the two copper layers, the injection nozzle was to move horizontally across the substrate while depositing the silver nano-particles. This process would allow a silver track to be deposited along the chamfered hole that was produced from the conic drill. This process is shown in Figure 16.

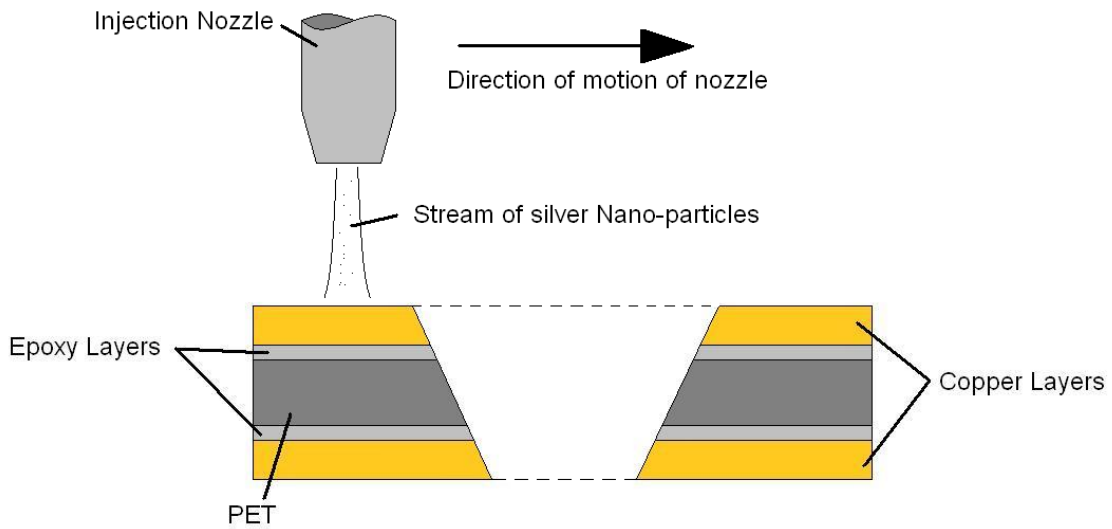


Figure 16 - Cross-sectional schematic showing silver deposition on substrates fabricated with a conic drill

With the deposition process done as such, the silver nano-particles would ideally be able to form a thin-film silver track along the chamfered edge of the hole, as shown in Figure 17, which should provide the substrate with a successful interconnect between the two layers of copper. This deposition process would then be repeated to provide multiple layers of silver as desired. The width of each track of silver is approximately 50 to 60 μm .

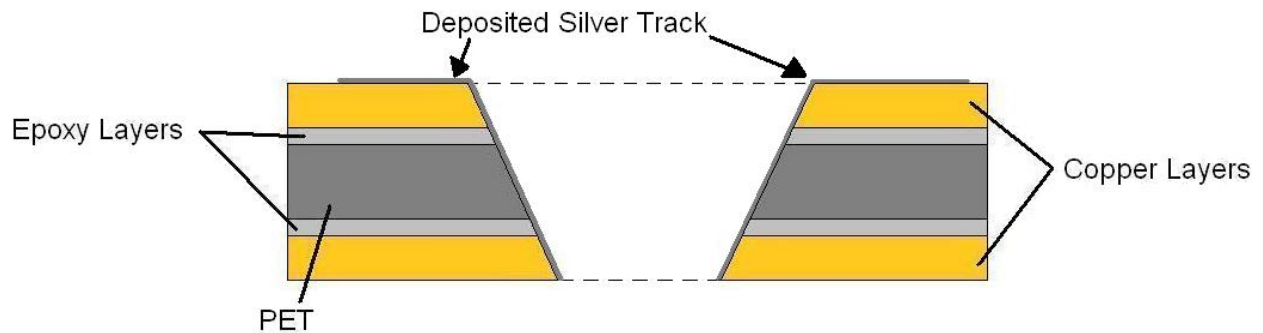


Figure 17 - Cross-sectional schematic showing the ideal result of a successfully formed silver interconnect

There are many parameters that must be managed in order to produce silver interconnects that are free of cracks and delamination. Optimum parameters and their chosen values are listed in Table 2. There are a few parameters in this table that have ranges of values. This is mainly due to placing the formation of the silver track in higher priority than other parts of the process, such as sintering. The reason for this was due to uncertainty of success, since the fabricated chamfered holes were not as smooth as originally thought. If the current parameters produced good interconnects, the parameters with ranges of values can be optimized and other lower priority

parameters can be optimized afterwards, particularly parameters involving speed such as injection nozzle and laser sintering speeds.

Table 2 - LAMM Process Parameters for Deposition on Substrates with Chamfered Holes

LAMM Process Parameters						
Sheath Gas Flow Rate	Atomizer Gas Flow Rate	Atomizer Voltage	Injection Nozzle Speed	Number of Silver Layers	Laser Speed	Laser Power
50 ccm	12 - 14 ccm	50 V	0.1 mm/s	20 - 50	1 mm/s	1.24 W

4.2.3 Results for Substrates with a Chamfered Via

The silver nano-particles were deposited across the chamfered hole in a cross-like fashion, as shown in Figure 18. By introducing more than one path of silver over the chamfered hole, there would be a higher chance of creating a successful silver interconnect, since a total of four tracks would be deposited for each sample.

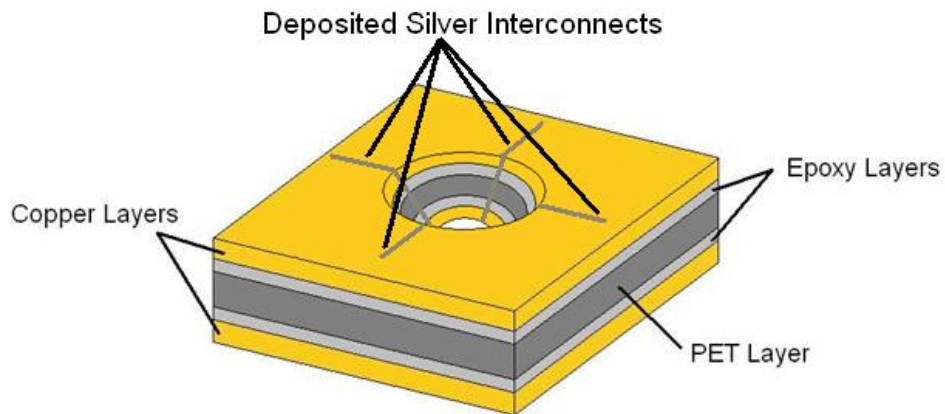


Figure 18 - Cross-sectional schematic showing deposited silver tracks on double-sided copper substrates with a chamfered VIA

After many experiments with the substrates containing chamfered VIAs, it was evident that this process was not very successful. A JEOL JSM-6460 scanning electron microscope

(SEM) was used to examine the substrate after deposition and sintering. An SEM image is shown in Figure 19, which shows some of the challenges associated with these experiments. As seen, the steepness and inaccuracies of the fabrication process combined caused the interconnects to break at various points. The VIA was expected to be smooth and uniform, but from SEM images, it could be seen that the surface was not as well machined as desired. It was concluded that this approach towards creating an interconnect between the two layers of copper had an extremely low chance of success, due to inaccuracies of the fabrication process.

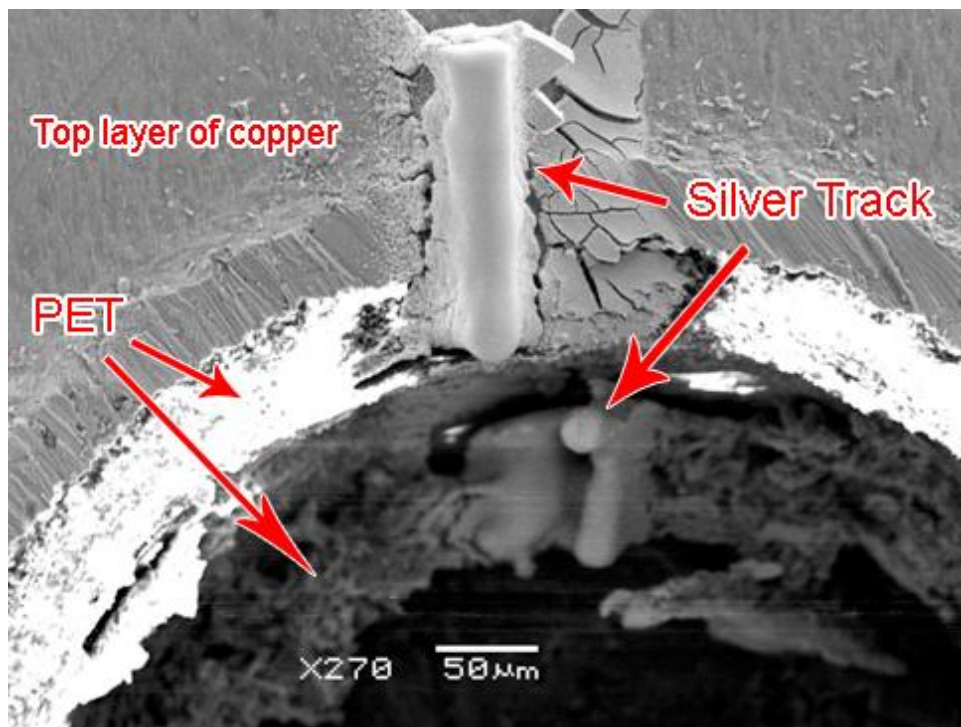


Figure 19 - SEM image of an attempt to form an interconnect on the fabricated chamfered via

4.3 Experiments Involving Substrates with Polished Slants

4.3.1 Fabrication of Polished Slants

A different approach was taken to create silver interconnects that connected the two layers of copper. Due to the fabrication inaccuracies of the conic-drilling process, the fabrication of the chamfered VIAs was simplified down to a slant created after polishing the substrate at an angle, shown in Figure 20. Since depositing along the chamfered VIA would be equivalent to depositing along a slanted edge, the experiments were simplified to depositing nano-silver particles onto slanted edges. In industrial practices, fabrication of the chamfered VIAs would not be extremely difficult, as automated tools with high precision can be used.

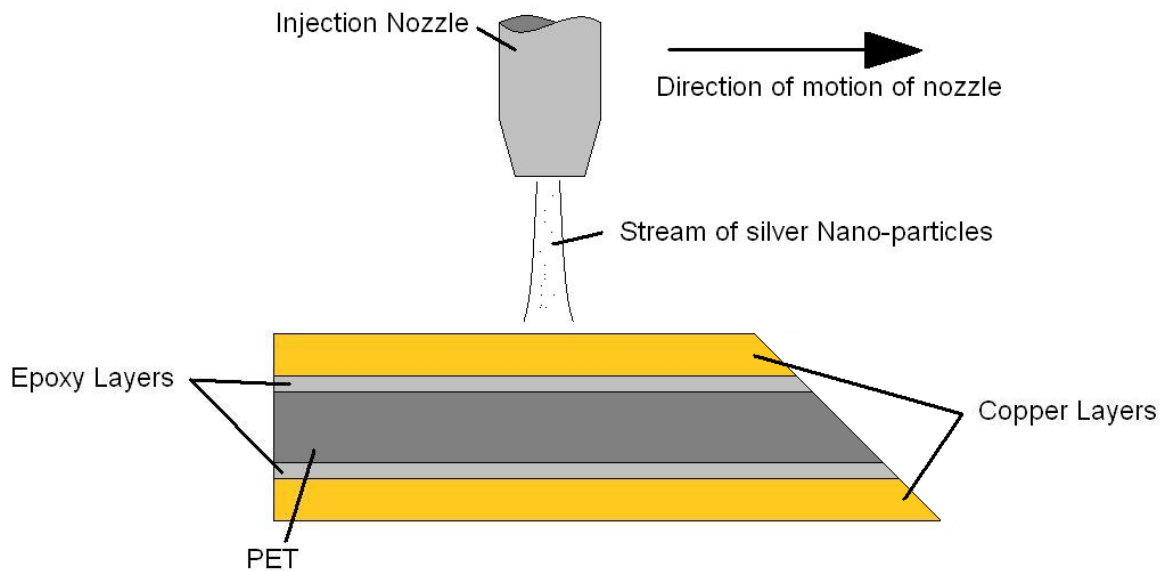


Figure 20 - Cross-sectional Schematic Showing the Deposition Process on Substrates with a Polished Slant

The polishing process is much more controlled compared to conic drilling, and the resultant edge is extremely smooth. The substrates were polished at an angle of 45° to the polishing pad with a very fine abrasive. The abrasive used was an aluminum oxide powder with

grain sizes of 0.05 μm . The finished polished substrate would have the bottom layer of copper exposed along the polished edge, much like the intended result of the conic drilling process. After polishing, the substrates are washed with an isopropanol solution and sonicated.

4.3.2 Depositing the Silver Track for Substrates with Polished Slants

As shown in Figure 20, the deposition process performed on the substrates with polished slants is identical to that of the substrates with chamfered VIAs. The injection nozzle would be passed over the substrate’s polished edge, depositing silver nano-particles in a single path that would span the length of the polished slant. This silver track would then be sintered using a laser to complete the process. The process parameters are listed in Table 3.

Table 3 - LAMM Process Parameters for Substrates with a Polished Slant

LAMM Process Parameters						
Sheath Gas Flow Rate	Atomizer Gas Flow Rate	Atomizer Voltage	Injection Nozzle Speed	Number of Silver Layers	Laser Speed	Laser Power
50 ccm	12 - 14 ccm	50 V	0.1 - 1 mm/s	4 - 10	1 mm/s - 5 mm/s	0.44 - 3.1 W

Upon running various experiments, it was discovered that the silver track would form much easier than the experiments with a fabricated VIA. With this information, many process parameter values were modified in order to better optimize the experiments. The most time consuming part of the process was the deposition of the silver nano-particles. Due to the silver track forming much easier on the polished slant, the injection nozzle speed was increased and the number of silver layers was decreased.

The main reason for the high number of silver layers used in the experiments with chamfered VIAs was due to the extremely large crack formations of the silver track that appeared consistently along the face of the VIA. With the substrates with a polished slant, there

did not appear to be much of a difference between 10 and 50 silver layers, as both were able to create a silver track that spanned the entire face of the polished slant. Although cracks did appear for the silver tracks deposited along the polished slants, these cracks were not caused by the injection nozzle having difficulty depositing the silver nano-particles upon certain areas of the surface and would be investigated.

4.3.3 Initial Results for Substrates with a Polished Slant

When examining the substrates with the use of the optical imaging system, it was noted that the deposited silver track appeared to form a solid track that travelled from the top copper layer to the bottom copper layer, as shown in Figure 21. The images taken of the substrates with polished slants appeared to be much better than that of the substrates with chamfered VIAs, since there were no extremely large cracks visible. It can also be noted that the bottom layer of copper does not have a large amount of exposure when viewed from the top, since the copper layers are very thin.

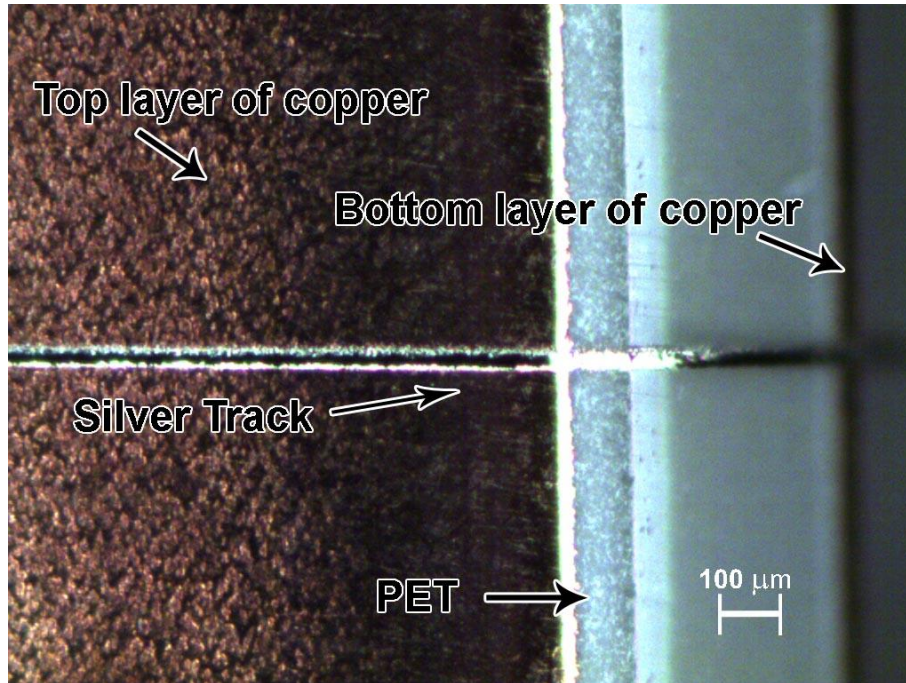


Figure 21 - Top view of a substrate with a polished slant after 4 layers of deposition at 0.1 mm/s and sintering at 0.4 W and 1 mm/s.

At times there would be cracks in the silver track visible from the optical images, as shown in Figure 22 along the face of the PET. However, these cracks were not on the same magnitude as those from the substrates with chamfered VIAs. In order to view the cracks, the substrate would be required to be examined with a scanning electron microscope. Upon viewing the interconnects with an SEM as shown in Figure 23, very fine cracks were seen in both conductive and non-conductive interconnects. When measured with an ohmmeter by connecting a probe on either end of the interconnect, the conductive samples showed resistances in the range of 7 Ω to 10 Ω .

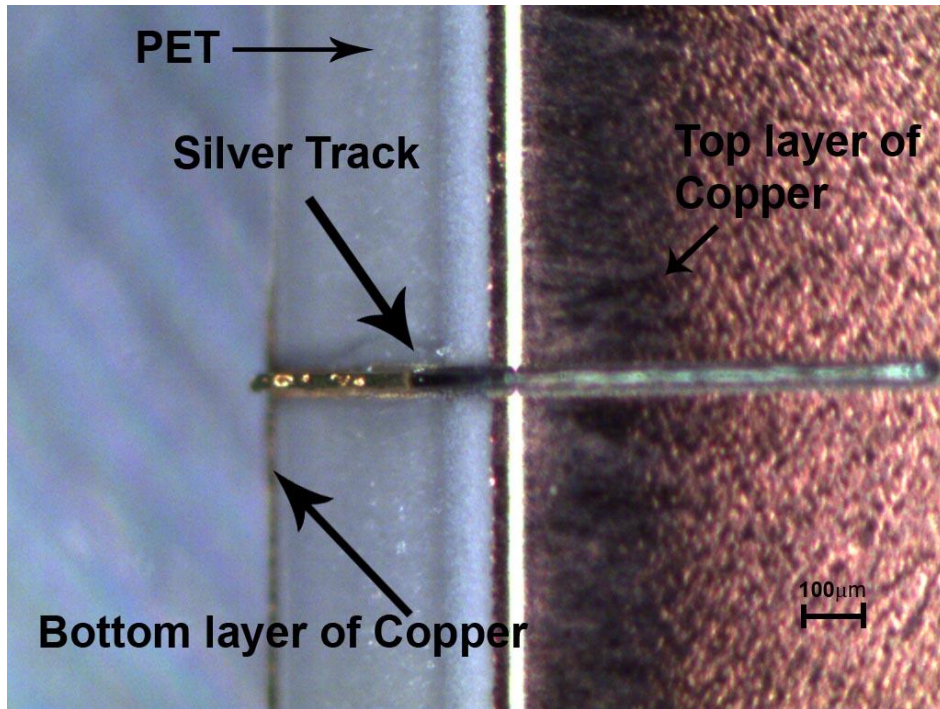


Figure 22 - Top view of a substrate with a polished slant after 4 layers of deposition at 0.1 mm/s and sintering at 1.24 W and 1 mm/s.

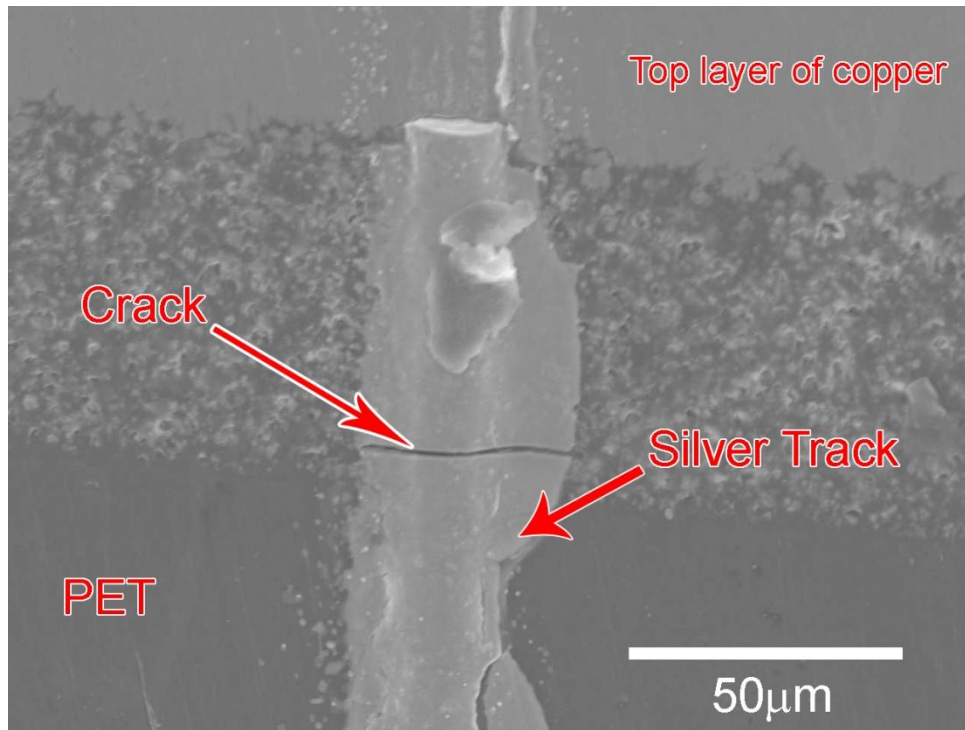


Figure 23 - SEM Image of a substrate with a polished slant displaying a crack in the interconnect

4.3.4 Repeated Deposition and Sintering

In an attempt to increase the chances of creating successful interconnects on the polished slant, some substrates underwent the deposition and sintering process multiple times. For these substrates, the process would work as follows: after depositing and sintering the silver track, another few layers of silver were deposited upon the already existing track and sintered once again. By repeating the process multiple times, the new layers of silver were expected to be able to fill in the cracks formed in the previous process and potentially create a good interconnect.

4.3.4.1 Optical Imaging Results

One observation that can be noted is that upon multiple deposition and sintering repetitions, the PET around the silver track will appear to melt slightly. This is more evident in experiments where the deposition and sintering process were repeated up to three times, as shown in Figure 24. The silver track in Figure 24 was measured for conductivity during each iteration of the deposition and sintering processes, however none of the measurements showed any conductivity. The melting of the PET may have played a role in creating a non-conductive result due to material stresses that may have formed once the PET began to change shape.

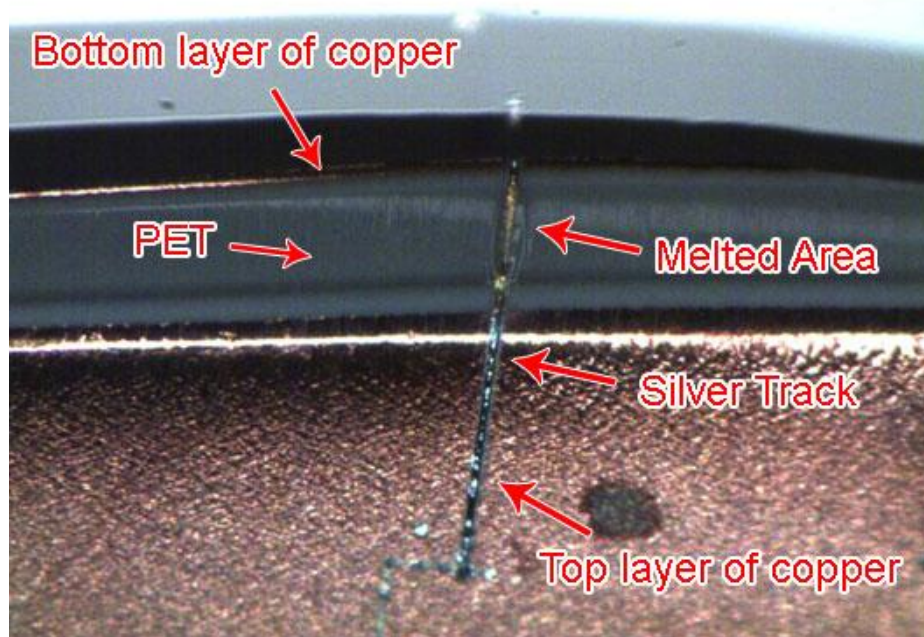


Figure 24 - Top view of a deposited silver track that was sintered multiple times, resulting in a slightly melted area of PET around the silver track

Deposition and sintering iterations are repeated for substrates that contained non-conductive interconnects after the first deposition and sintering process. However, it appears that multiple sintering stages cause the PET around the silver track to melt and possibly add more problems for the silver track. Repeating the deposition and sintering stages once for a total of 2 deposition and sintering stages appears to not melt the PET very much, and has even resulted in some conductive results, but further iterations will change the PET greatly.

4.3.4.2 SEM Results

An SEM image of a conductive interconnect that was created through multiple stages of deposition and sintering is shown in Figure 25. The silver track appears to be very solid along the entire slant, with the exception of an extremely fine crack that can be seen near the interface between the top layers of material. Although a crack is present, the interconnect was still able to form a connection between the top and bottom layers of copper. This type of experiment showed

very few cracks compared to experiments that did not repeat the deposition and sintering process. It is likely that the repetition of the deposition process allows previously formed cracks to be filled in with the new deposition of silver, allowing for a solid track to be formed along the polished edge. The reason for the crack is hypothesized to be from the cause of a difference in thermal expansion between materials. More experiments were required to be performed in order to determine if this hypothesis was feasible.

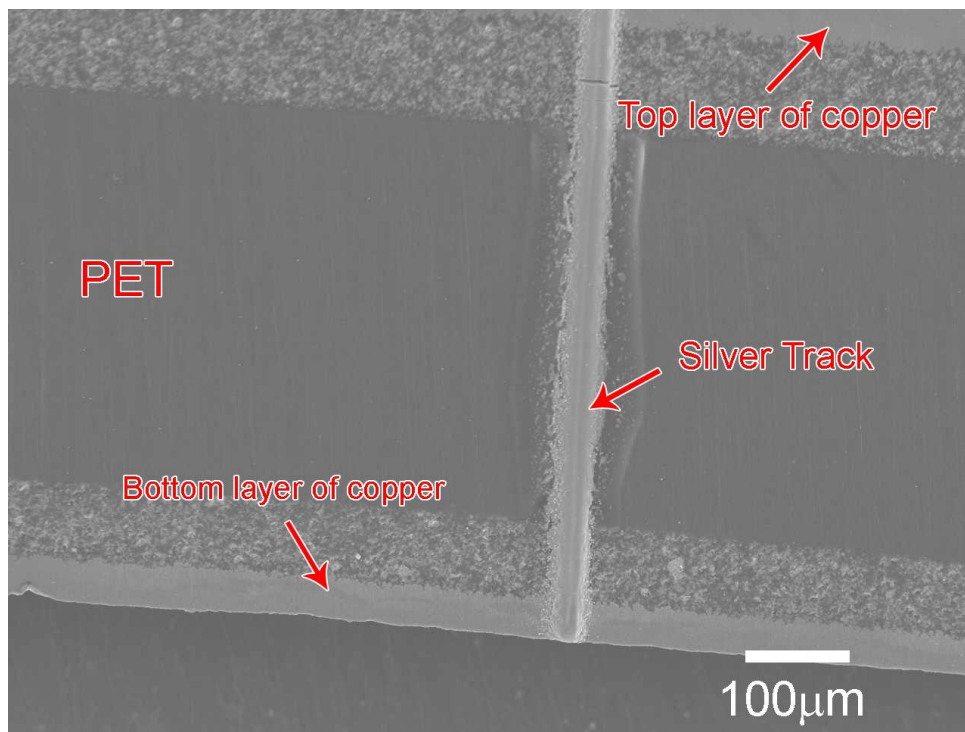


Figure 25 - SEM image of a conductive interconnect formed on a substrate with a polished slant. Two stages of deposition were performed, each with 5 layers at 1 mm/s.

Upon measuring the resistance values of the interconnects with the use of an ohmmeter, the resistances were found to range from 5 Ω to 8 Ω . Some of these substrates were analyzed with a source-measure unit for more accurate resistance values, and these values were found to

range from 3.2 Ω to 4.31 Ω . This resistance value appears to be much higher than the resistance that can be calculated using the equation involving electrical resistivity, Equation (4.1):

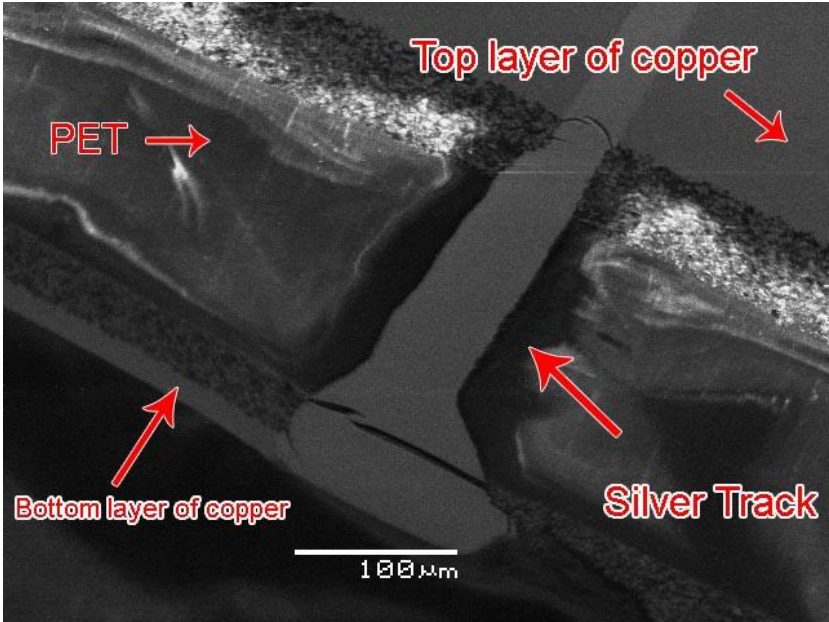
$$R = \rho \frac{l}{A} \quad (4.1)$$

where R is the electrical resistance of the material, ρ is the electrical resistivity of the material, l is the length of the track, and A is the cross-sectional area of the track. Using the electrical resistivity value of bulk silver (15.87 n Ω m), the theoretical resistance calculated is 0.017 Ω . The measured resistance is larger than the theoretical resistance by at least 100 times. This is likely attributed to the formation of pores in the silver tracks during sintering. When the silver nanoparticles are sintered, the evaporation of the solvent material causes pores to be formed within the microstructure of the silver track [48]. Voids and pores that are formed within conductive material have shown to increase the resistance of the material, which is likely the reason that the measured resistance is much higher than the calculated resistance [49].

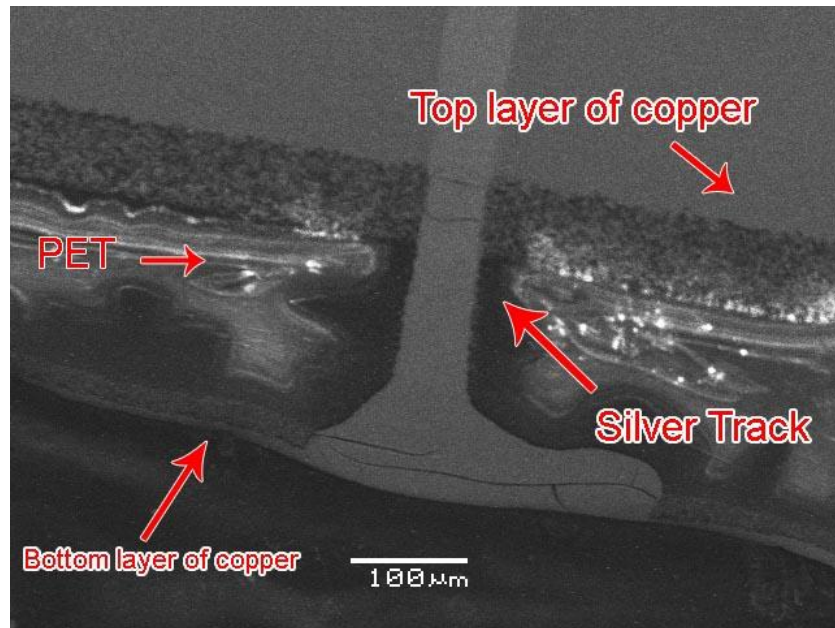
4.3.5 Insufficient Heating of Substrate

As noted before, the substrate should be heated during the deposition process in order to allow the silver nano-particles to adhere well upon contact with the surface. When the substrate is not heated sufficiently, the silver track will not stay uniform, as shown in Figure 26. Due to the nature of the polished slant, the silver nano-particles will tend to flow downwards along the slant when the substrate is not heated sufficiently, creating non-uniform shapes for the resultant silver track. Surprisingly, Figure 26 (a) shows this as well as cracks in the silver track while still resulting in forming a successful interconnect between the two layers of copper. Upon inspecting the SEM image closely, it can be seen that there is a small sliver of silver that appears to bridge the crack formed at the bottom of the polished slant. It is most likely due to this extremely small

connection that the entire interconnect is able to bridge the two layers of copper. Figure 26 (b) shows a substrate that demonstrates the same behavior when the substrate is not heated during deposition, but resulted in an unsuccessful interconnect. There appear to be many cracks that have formed at the top and bottom of the interconnect. These cracks are most likely the reason the interconnect was unable to join the two layers of copper.



(a)



(b)

Figure 26 - SEM images of substrates with polished slants after deposition during insufficient substrate heating temperatures. The substrates were sintered with (a) 1.25 W at 1 mm/s, which formed a successful interconnect and (b) 1 W at 2 mm/s, which did not form a successful interconnect.

The silver interconnect track at many times appears to be breaking around areas where different materials are joined together. Figure 27 shows another example of this. There appears to be a crack that travels across the track entirely around the region where the bottom layer of epoxy is joined with the PET, as well as small fractures that appear near the top of the interconnect between the top layer of epoxy and the PET.

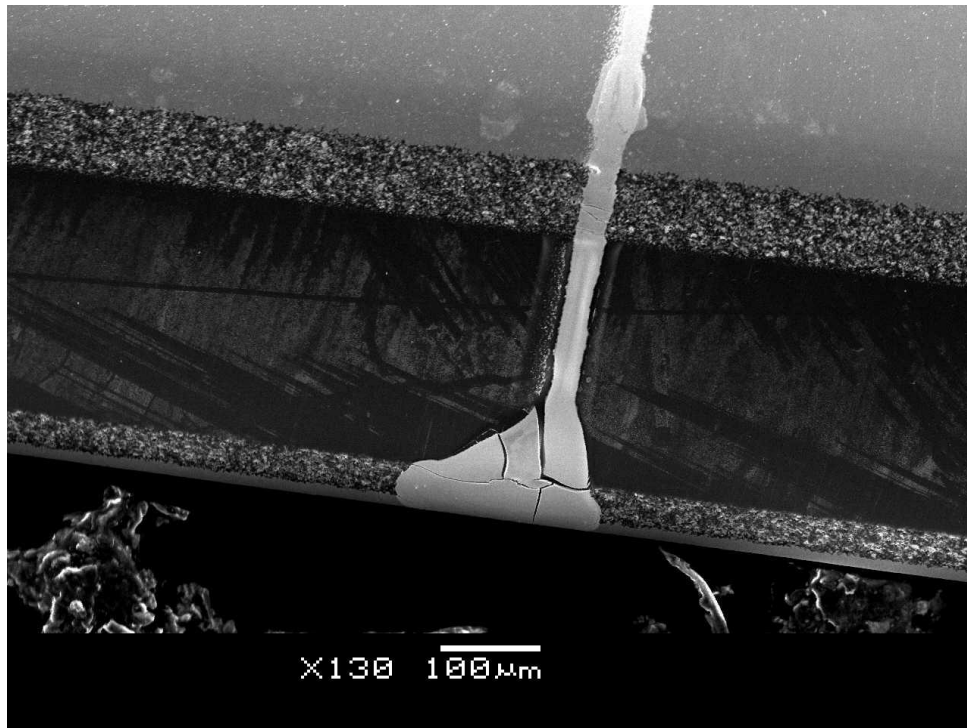
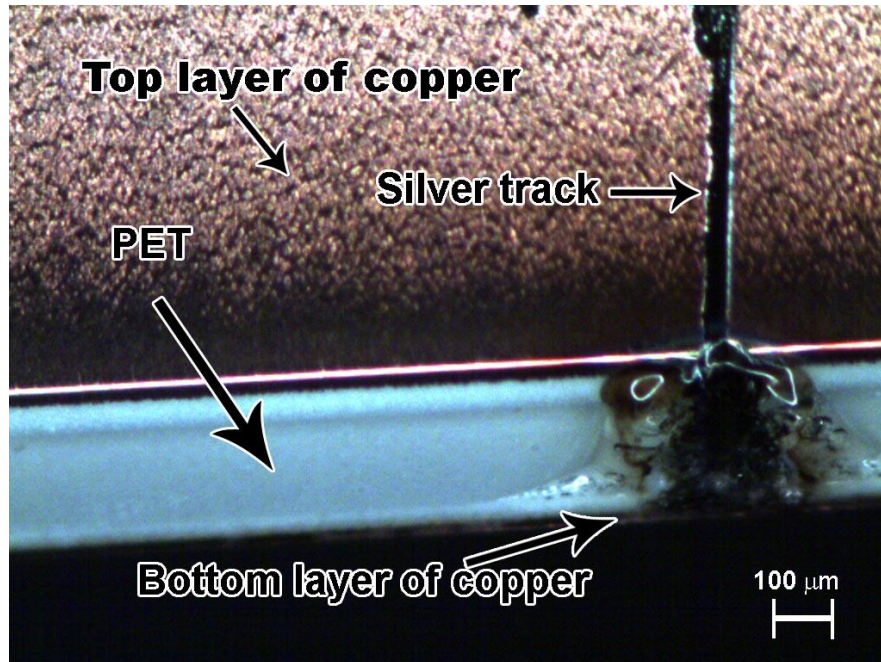


Figure 27 - SEM images of a substrate with a polished slant after deposition during insufficient substrate heating temperatures. This substrate was sintered at 1.24 W and 1 mm/s.

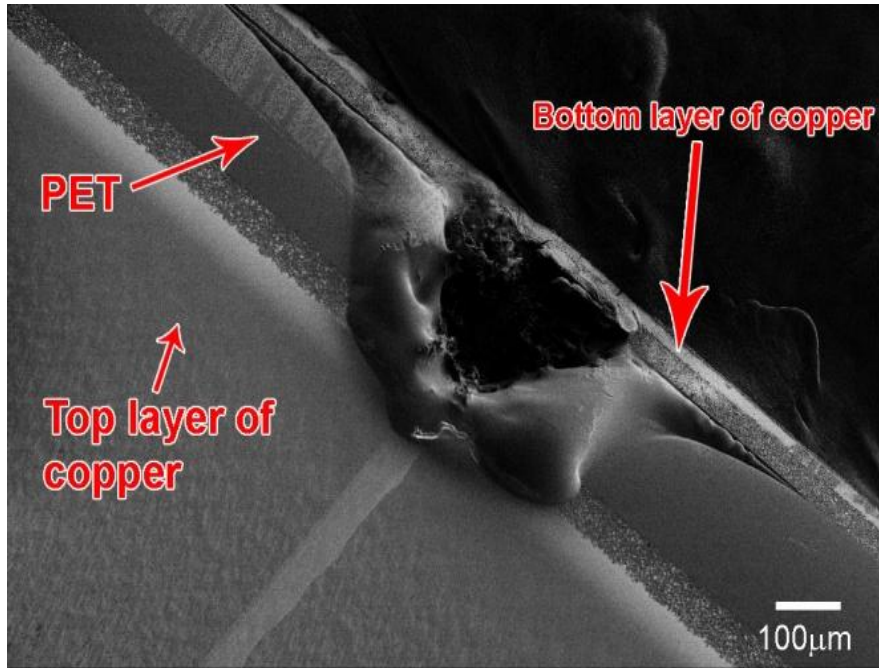
4.3.6 Increasing the Laser Power

When experimenting with higher laser powers, it was noted that the intensity of the laser has the capability to burn the PET layer when the laser power was increased to 3 W. Shown in Figure 28, it can be seen that upon sintering the silver nano-particles, the laser was able to burn the PET surrounding the silver track. However, although the substrate was burned, when measured for conductivity, the results were positive for this particular substrate. This was likely due to coincidence that while burning the PET, the silver nano-particles managed to form a path downwards to the bottom layer of copper. When other burned substrates were measured, the majority did not contain a successful interconnect. For the few substrates that did contain conductive results, the results ranged from 500 Ω to 2.5 k Ω . These resistance values are

extremely high compared to the results from the conductive substrates that did not burn. This shows that although the substrates were able to have conductive interconnects after burning, the interconnects would not be usable for any devices as the resistance is much too large.



(a)



(b)

Figure 28 - Images of substrate with polished slant after high-power sintering (3W) at 4 mm/s. Images taken from an (a) optical microscope, and (b) SEM.

4.3.7 Alternative Sintering Method

An alternate sintering method was proposed due to the burning of the PET layer when the power was increased for the laser during sintering. Although it is still possible to sinter the silver nano-particles with a lower laser power, investigating into possible alternatives is a reasonable choice of action. In fact, the majority of the samples that resulted in successful interconnects were those that were sintered with a lower laser power (1.24 W). The alternate sintering method that was used was sintering with the use of a hotplate or oven. The hotplate or oven would be set to the sintering temperature (170 °C) and the substrates would be left to sinter for 30 minutes [50]. After this, the hotplate or oven would be turned off and the substrates would be allowed to cool down to room temperature before removing the substrate from the hotplate or oven.

After a number of experiments with this alternate sintering method, it was discovered that the chance of success with this method was rather low. One of the reasons for the low success rate is likely due to the PET glass transition temperature, which is around 70 °C [51]. This means that the PET would begin to distort while the hotplate or oven was sintering the substrate. It was noticed that the substrates were slightly distorted after sintering. Although the copper layers managed to maintain the general shape of the substrate by holding the PET layer in place, signs of distortion were still observed.

The majority of the samples resulted in an unsuccessful interconnect, although there were some successful interconnects that were formed. An SEM image of a successful interconnect is shown in Figure 29.

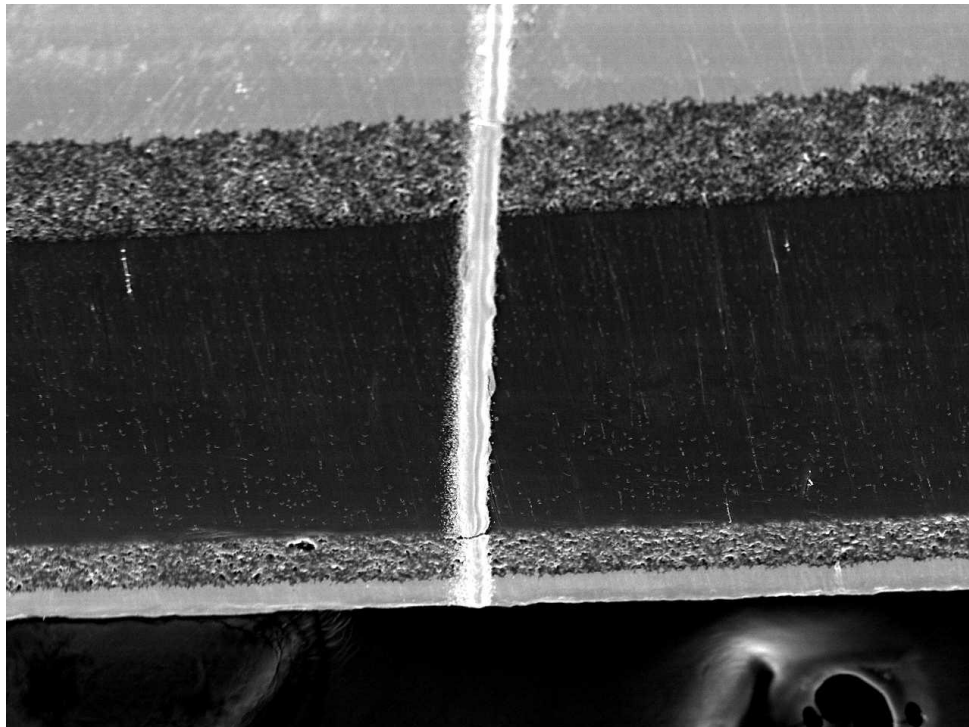
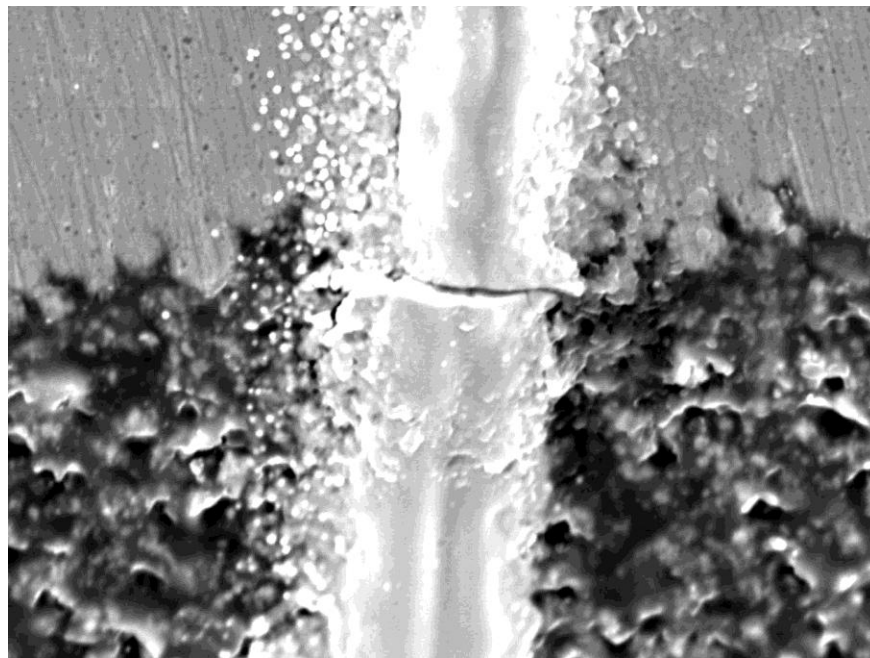
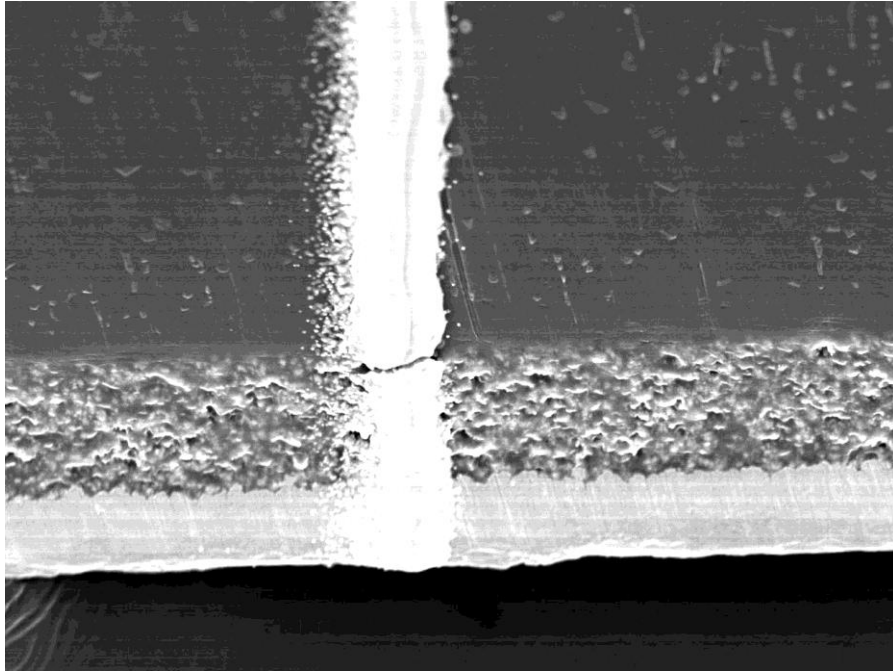


Figure 29 - SEM image of a substrate with a polished slant after sintering with a hotplate

At higher magnification, it can be seen that there are two main cracks that have formed in the silver interconnect: One near the top of the substrate where the top layer of copper meets the epoxy layer and one near the bottom where the PET meets the lower epoxy layer. Magnified images of the cracks are shown in Figure 30. Previously, with substrates sintered with the use of a laser, it was noted that many cracks were formed on the areas where different material layers were joined. This result was much more noticeable with the substrates that were sintered with the use of a hotplate or oven. In particular, the crack that appears in Figure 30 (a), which was formed between the top layer of copper and the top layer of epoxy, was present in every substrate that was sintered this way.



(a)



(b)

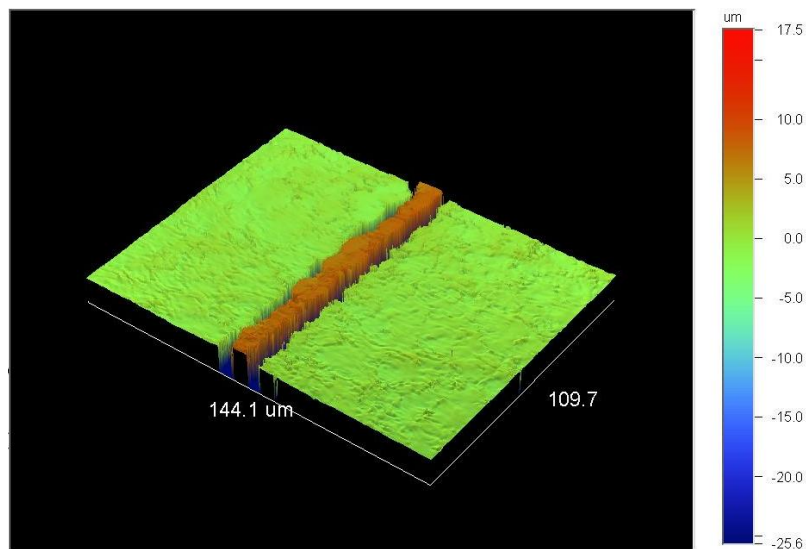
Figure 30 - SEM images of cracks formed between (a) the top layer of copper and top layer of epoxy, and (b) the PET layer and the bottom layer of epoxy.

With cracks forming on the interfaces between materials, the hypothesis that a difference in thermal expansion rates was creating the cracks was strengthened. Since copper expands at a much faster rate than PET, this could create thermal stresses within the silver track that cause it to crack. Upon observing the substrates that were sintered using the hotplate or oven, this speculation appears to hold strongly. For the substrates that were sintered with a laser, the speculation does not hold as strongly, but it is entirely possible that the silver tracks sintered with a laser were cracking due to differences in thermal expansion rates, since the laser does emit a large amount of energy.

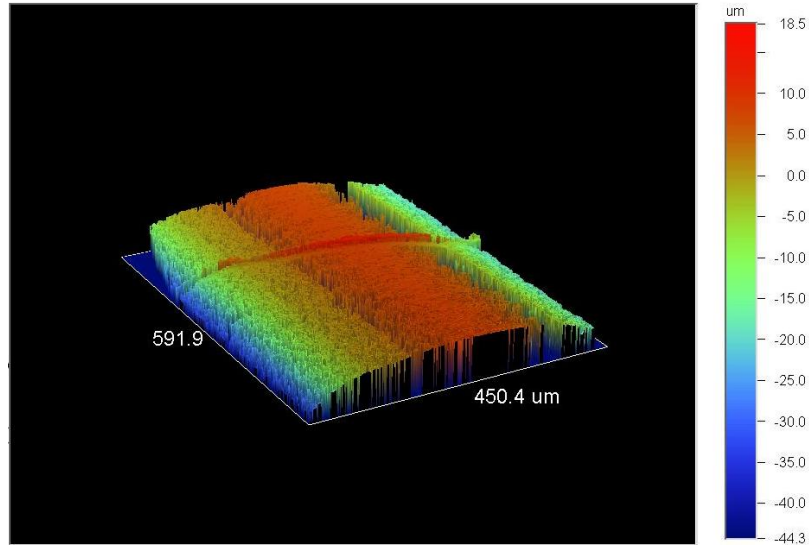
4.3.8 Profilometry Analysis

A profilometry analysis was also performed on a successful interconnect that was deposited and sintered on a substrate with a polished slant. Isometric images generated by the

profilers are shown in Figure 31. Figure 31(a) shows the portion of the silver track that was deposited on the top layer of copper. It can be seen that the silver track is of a uniform height, which was to be expected. Figure 31(b) shows the portion of silver track which was deposited on the polished slant. For this image, the substrate was tilted such that the polished slant would be perpendicular to the viewing angle. This image shows that the polished slant is not perfectly planar, with elevation variations of roughly $15\ \mu\text{m}$. The reason for this variation is likely due to inaccuracies during the polishing process. However, the substrate in question contained a successful interconnect, which shows that this elevation variation does not have a very large impact on the result of the silver interconnect after depositing and sintering.



(a)



(b)

Figure 31 - Images generated by a profiler when analyzing a substrate with a successful interconnect. Different views show (a) the silver track on the top layer of copper and (b) the silver track along the polished edge of the substrate

4.4 Experiments Involving Substrates Mounted on an Incline

4.4.1 Fabrication Process for Substrates Mounted on an Incline

As an alternative fabrication process, the possibility of depositing and sintering a silver track upon a substrate that was not polished at an angle was considered. In place of the polished slant, the substrate would be inclined at an angle that would simulate the polished slant and allow for the silver nano-particles to be deposited upon the edge as shown in Figure 32. The inclination mount would contain multiple inclination angles to allow various angles to be experimented with. The mount, shown in Figure 33, was created through the use of a uPrint 3D printer. The substrate would be polished in a similar manner as the ones with polished slants. In this case, the same aluminum oxide powder abrasive would be used. However, instead of polishing the substrate at a 45° angle, the substrate would be polished vertically, such that the polished edge

would be free of surface deformities. After polishing, the substrate would be washed with isopropanol and sonicated in preparation for the deposition process.

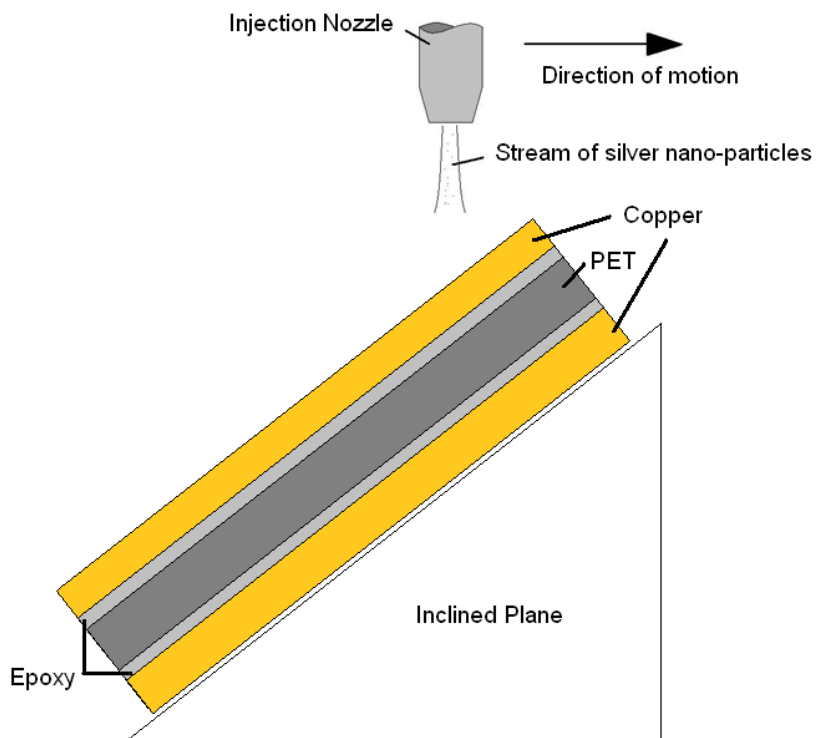


Figure 32 - Schematic showing the deposition process for substrates mounted on an incline



Figure 33 - Mounting containing various inclination angles

4.4.2 Depositing the Silver Track for Substrates Mounted on an Incline

The deposition process is very similar to the process for substrates with a polished slant. The substrates in this case will be mounted on an inclined surface such that the edge will be visible to the injection nozzle as depicted in Figure 32. The nozzle will then travel across the edge of the substrate while depositing the silver nano-particles. The resultant silver track should be very similar as the idea behind the fabrication of the substrates is the same.

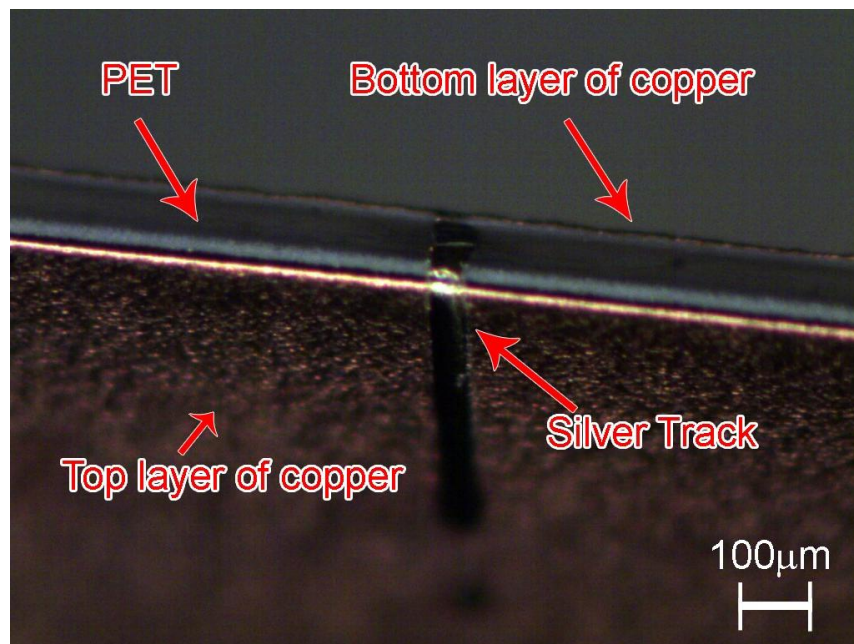
The reason this process was approached was due to its mass production potential, as it does not require much modification to the substrate. In order for fabrication, this substrate only requires a smooth vertical edge to deposit on, as opposed to the polished slant, which would require much more fabrication time. In fact, the inclination of the substrate is meant to simulate the tilting of the injection nozzle. This way, the substrate would remain horizontal on the platform and the injection nozzle would be rotated at an angle. By tilting the injection nozzle, the substrate does not require any inclination and the process can be done quickly on assembly lines. The reason for the inclination plane in this case is due to restrictions in the LAMM machine at the university. It is unable to rotate the injection nozzle, but depositing with a tilted injection nozzle has been accomplished in practice.

Due to the similarity between the experiments with substrates containing polished slants and substrates mounted upon an incline, the range of deposition and sintering parameters were not changed.

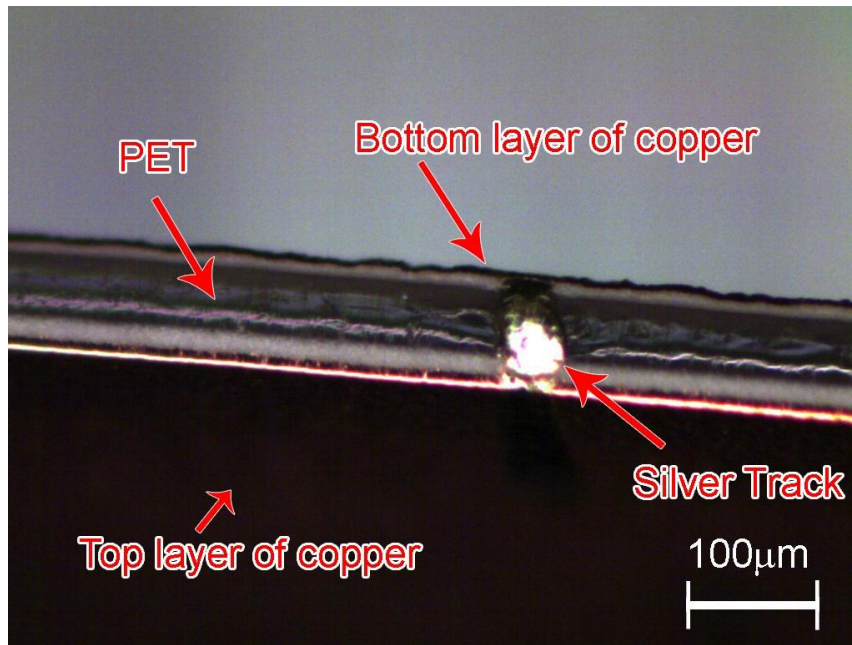
4.4.3 Results for Substrates Mounted on an Incline

After many experiments with substrates mounted on an incline, it was observed that none of the resultant substrates contained a successful silver interconnect track along the edge of the substrate. Figure 34 shows optical images of the substrates after deposition and sintering. It

appeared that the silver track was unable to reach the bottom layer of copper for some substrates. This is more evident in Figure 34(a), where the lower layer of epoxy can be seen between the silver track and the bottom layer of copper. This certainly would be a reason for an unsuccessful interconnect. However, not all substrates displayed this trait. As a result, a scanning electron microscope would be required to investigate further on the reason for the unsuccessful interconnects.



(a)



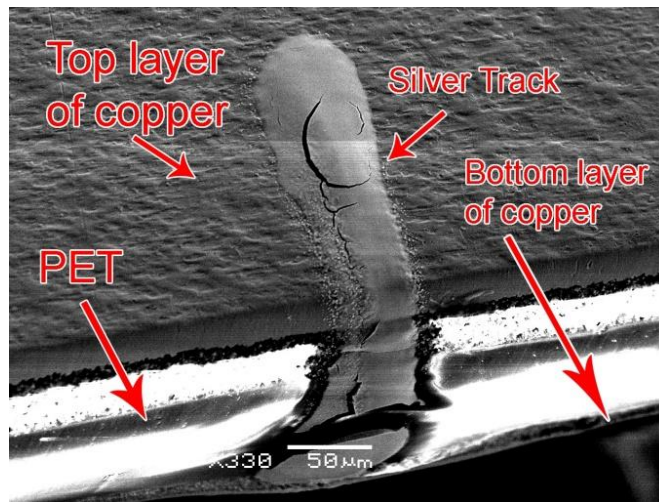
(b)

Figure 34 - Images taken from an optical microscope for substrates mounted on a (a) 30° and (b) 45° incline. Sintering was done at 1.25W and 2 mm/s.

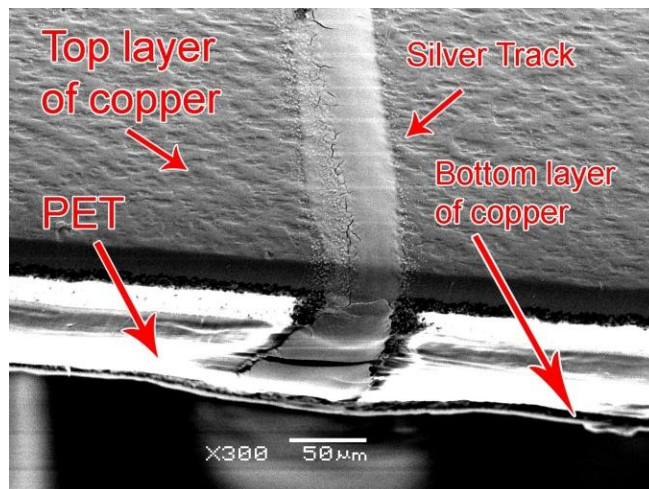
SEM images of some substrates that were mounted on an incline are shown in Figure 35. It appeared in the optical images in Figure 34 that the silver track did not reach the bottom layer of copper on certain substrates, which appears to be true when looking at the SEM images. Figure 35 (b) particularly shows that the silver track did not reach the bottom layer of copper. Although this is a potential reason for the unsuccessful interconnects, this was not portrayed in each substrate. Every substrate that was examined with the use of an SEM showed another potential reason for failure, which was an extremely large crack that appears to split the silver track near the middle of the edge. It should be noted that due to the fact that the mount created was not composed of a conductive material, the substrate could not be preheated during the

deposition process, which would mean that the silver nano-particles will not adhere during the deposition stage as well as the previous experiments involving the polished slants.

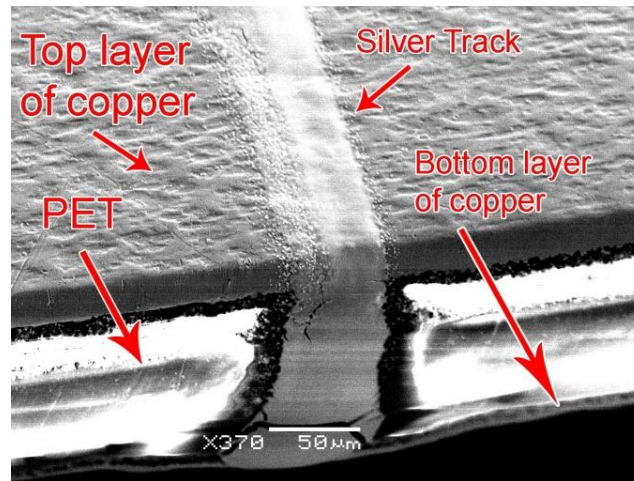
However, when comparing the results of substrates that were not preheated during the deposition stage for both the polished slants and those mounted upon an incline, it can be noted that extremely large cracks that were formed only on the substrates mounted on an incline. The cracks that were formed on the substrates with polished slants were not on the same magnitude as those formed on substrates mounted on an incline.



(a)



(b)



(c)

Figure 35 - SEM images of inclined substrates deposited at (a) 25°, (b) 30° and (c) 35°. Sintering was done at 1.25W with a speed of 2 mm/s

In an attempt to discover the reason for the poor results of the substrates mounted on an incline, an SEM image was taken of an unsintered substrate that was mounted on an incline, which is shown in Figure 36. Minor cracks can be seen in the silver track, which may be the reason that the interconnects have failed, since the sintering process may expand these cracks into the extremely large cracks that were seen in Figure 35. Reducing the amount of silver may help resolve this issue, since it has been observed that large amounts of silver appear to create larger cracks upon sintering [52]. The differences in thermal expansion of the materials as the laser passes over the silver track may also be a reason for the cracks formed in the interconnect.

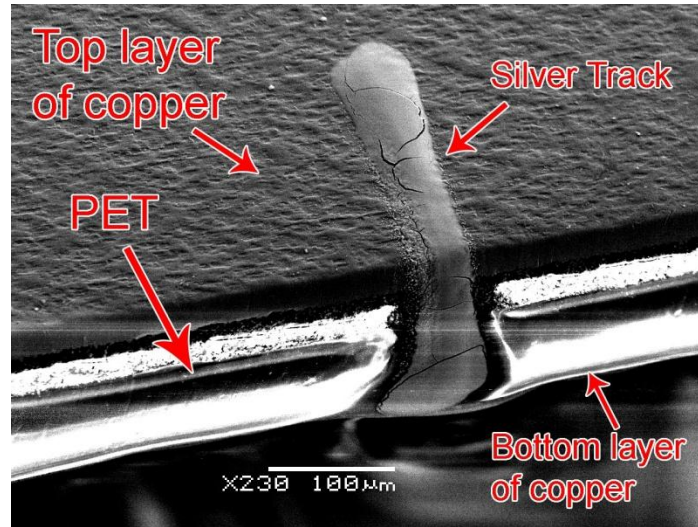


Figure 36 - SEM image of silver track deposited on an inclined substrate before sintering.

4.5 Contaminant Analysis

The substrates were analyzed for contaminants, as surface contaminants are a potential cause for delamination or crack formation within the silver track. An x-ray diffraction analysis as well as an x-ray spectroscopy analysis was performed on substrates with a silver track that was previously deposited onto the top surface of copper. The fabrication method of the substrate was not important, as the only information of interest was the material composition of the substrate after deposition and sintering.

4.5.1 X-ray Diffraction Analysis

An x-ray diffraction (XRD) analysis was conducted to observe the crystalline structure of the substrate. The XRD patterns for substrates with polished slants after deposition and sintering are shown in Figure 37. Peaks (3), (5), (7) and (9) correspond to copper and peaks (2), (4), (6) and (8) correspond to silver. A polycrystalline material that does not contain lattice strain and consists of particle sizes larger than 500 nm will show sharp lines in a diffractogram [53]. Thus,

large crystallites of copper will give sharp peaks. It is known that as the crystallite size reduces, the peak width increases, and the intensity decreases. This way, silver nanoparticles will give peaks with very low intensity. Since polymers are never 100% crystalline, XRD is a primary technique to determine the degree of crystallinity (DOC) in polymers. Based on Joan's work that is given for PET XRD curves in different particle sizes, it has been shown that the position of PET's peak is around $2\theta = 20^\circ$. With this, it can be concluded that the peak at (1) is associated with PET [53]. From this XRD result, it can be concluded that there were no obvious contaminants in the copper surface or the silver track.

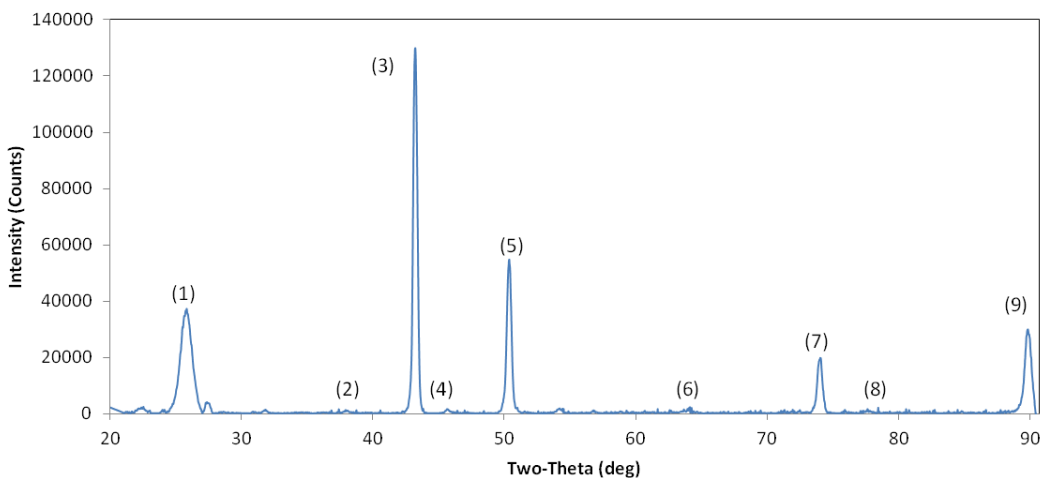


Figure 37 - XRD curve of a conductive substrate with a polished slant

4.5.2 X-ray Spectroscopy Analysis

An energy-dispersive X-ray spectroscopy (EDS) was performed to examine the chemical composition for any contaminants that may have been embedded into the silver track or copper surface. Contaminants in the copper surface or silver track have the capability to delaminate the silver track, which in turn may result in possible cracks in the silver track and prevent

conductivity between the two copper layers. An EDS image is shown in Figure 38. The corresponding composition of materials for each selected location is shown in Table 4. From the results of the EDS analysis, there were no obvious contaminants found on the copper surface or the silver track. Traces of aluminum were found in spectrum 5 in Table 4, which correspond to the analysis of the edge in Figure 38. This is likely due to the polishing process done on the edge of the substrate, which was done with aluminum oxide powder.

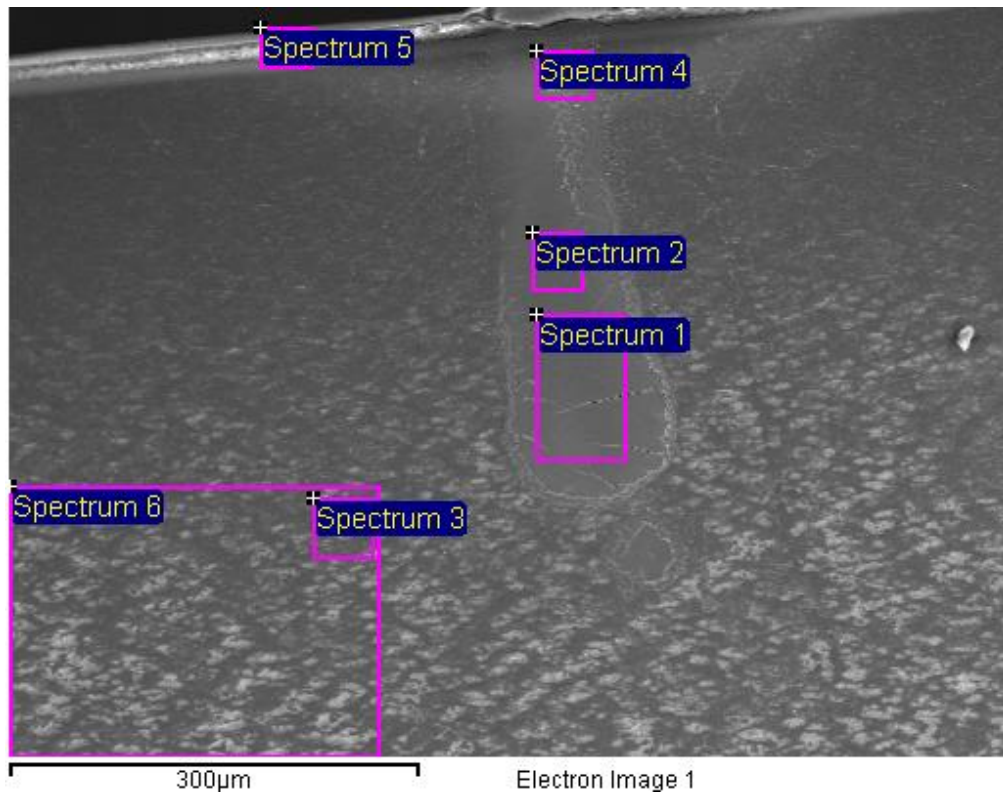


Figure 38 - EDS image for a substrate that was sintered at 1.4W with a speed of 2 mm/s.

Table 4 - EDS results for locations shown in Figure X

Spectrum	C (wt%)	O (wt%)	Al (wt%)	Cu (wt%)	Ag (wt%)
Spec 1	n/a	n/a	n/a	n/a	100
Spec 2	n/a	n/a	n/a	n/a	100
Spec 3	n/a	n/a	n/a	100	n/a
Spec 4	n/a	n/a	n/a	8.78	91.2
Spec 5	58.7	13.9	3.7	23.8	n/a
Spec 6	n/a	n/a	n/a	100	n/a

4.6 Summary

A double-sided copper flexible substrate separated by a layer of polyethylene terephthalate (PET) was used for experiments. Initially, the goal was to create a non-planar interconnect that would be deposited on a VIA fabricated within the substrate. This could not be achieved due to technical complications and as such, two other methods of fabrication were proposed to simulate the chamfered VIA.

The first method consisted of polishing the substrate an angle such that the polished slant would act as one side of a chamfered VIA. After several types of experiments, it was found that repeating the depositing and sintering process resulted in an interconnect with less cracks. However, repeating this process multiple times also showed that the heat from multiple sintering processes would cause the PET area around the silver track to melt slightly. Overall, there were some interconnects that were found to be conductive, which suggests the feasibility of the process but its sensitivity to process parameters. It is hypothesized that one reason for the unsuccessful interconnects is due to the difference in thermal expansion rates between the layers of material. SEM images showed many cracks occurring near the interfaces between different

materials, which strengthens this hypothesis. It was also observed that higher laser powers would cause the PET to burn, resulting in unsatisfactory interconnects.

The second method of simulating a VIA consisted of tilting the substrate instead of polishing on an angle. By having the substrate on a tilt, the experiments would be similar to that of the polished slant substrates. None of the substrates placed on an incline resulted in a conductive interconnect. SEM images also showed extremely large cracks formed on the silver interconnects that were not seen in the polished slant substrates. It was also observed that the silver particles were unable to reach the entire side of some of the substrates that were placed on an incline. Although the substrates placed on an incline were not sufficiently heated, the insufficiently heated polished slant substrates did not show problems to this degree.

The substrates were also analyzed for contaminants with the use of XRD and EDS, since contaminants can cause delamination and cracks for the silver interconnects. After the element composition analysis, there were no contaminants found in the substrates.

Chapter 5

Flexible Boards with Surface Mounted Resistors

This chapter consists of experiments performed on polyethylene terephthalate flexible boards with surface mounted resistors. The goal was to create non-planar interconnects between the silver coated pads of the resistor to the silver contact pads that the resistor was placed upon. Multiple deposition patterns were used and the details and results of each pattern are listed in the subsequent sections.

5.1 Materials and Fabrication

A number of experiments that were performed focused on creating micro-sized interconnects for surface mounted resistors on flexible boards, shown in Figure 39. The application for these flexible boards is towards heart monitoring devices. It should be noted that the experiments performed on these flexible boards were a pilot study to observe the feasibility of using the laser-assisted maskless microdeposition process for such substrates. The results from these experiments will be applied to surface-mounted components with smaller feature sizes in future studies.

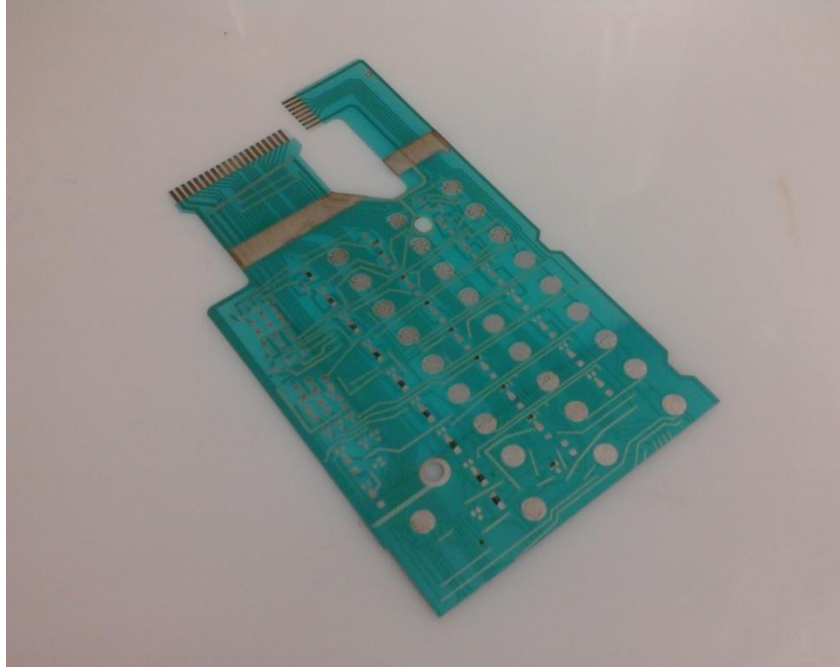


Figure 39 - Flexible board with surface mounted resistors

The resistors are attached to the board through the use of an epoxy, shown in Figure 40, which will leave a very small gap between the resistor and the pad in which the resistor is to connect to. Both the ends of the resistor as well as the pads are coated with silver, which should allow good adhesion with the silver nano-particles. With the use of the LAMM machine, silver nano-particles will be used to create an interconnect that connects the resistor to the pad underneath it. There are many different deposition patterns that can be used to deposit the silver nano-particles in an attempt to create the silver interconnect. Multiple deposition patterns were used to deposit the silver nano-particles, which resulted in varying results. The thickness of the flexible board is 18 μm . The surface mounted resistors have dimensions of 3.2 mm L x 1.6 mm W with a height of 0.6 mm.

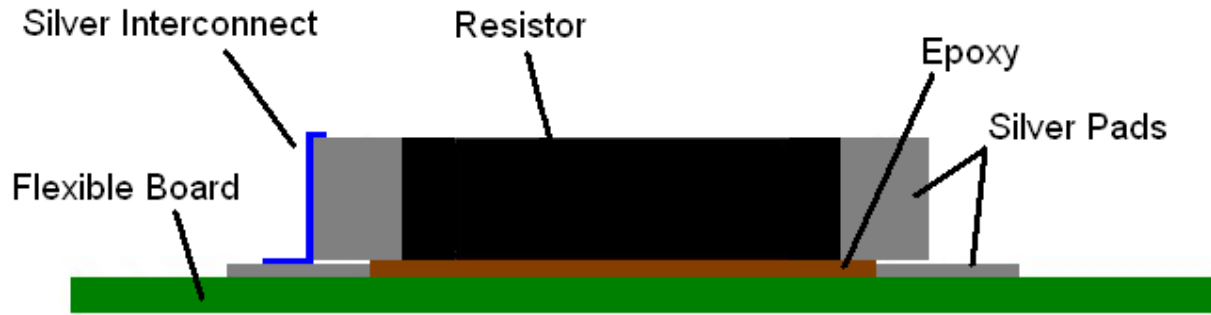


Figure 40 - Schematic of a surface mounted resistor on the flexible board after deposition

5.2 Characterization Methodologies

After deposition and sintering of the interconnects, similar characterization methodologies to those used for double-sided copper substrates were performed. The substrates were viewed under an optical microscope and SEM.

It was soon discovered that the interconnects formed on these substrates can be broken fairly easily, which made ohmmeter measurements extremely difficult and delicate procedures. In many cases, after the ohmmeter measurement was taken, the interconnect would no longer be conductive due to the pressure from the measurement probes destroying the interconnect. In order to perform reliable measurements, future measurements were taken using a combination of a source-measure unit as well as precision positioners (DCM 210 Series Precision Positioner, Cascade Microtech Inc, Oregon, USA), shown in Figure 41. This precision positioner contains two extremely fine probes that can be moved with micrometer precision onto the substrate of interest. The probe size is on the scale of micrometers, so the pressure induced by placing the probes on the resistor will not break the interconnects, which allows for reliable measurements.

The probes are connected to the source-measure unit in order to take the resistance measurements.

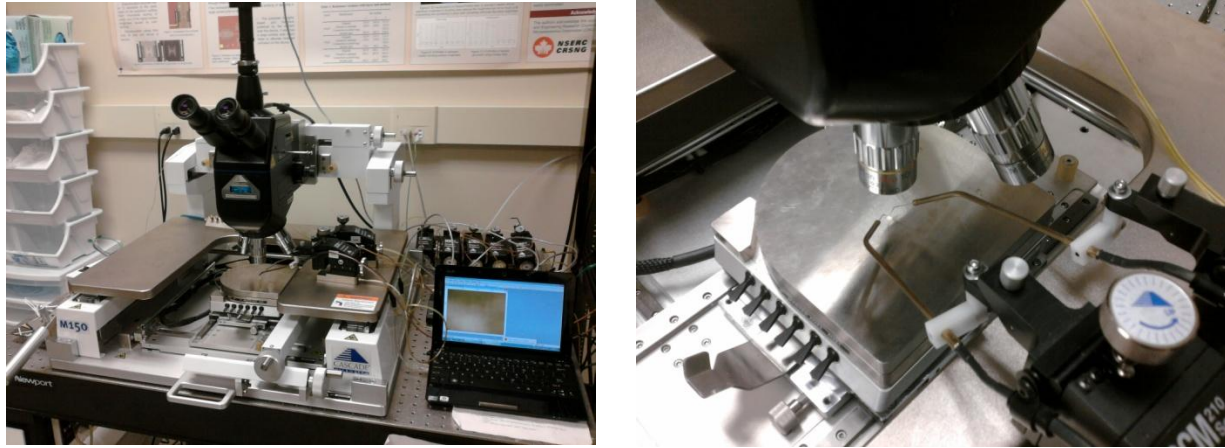


Figure 41 – Set-up for resistance measurements (left) and a close-up image of the probes (right)

5.3 Deposition Patterns

5.3.1 Overhead Pass Deposition Pattern

The first deposition pattern that was used was very similar to the deposition paths used in the experiments regarding the double-sided copper substrates. In this method, the substrate was mounted on an incline to allow the silver nano-particles to fall on a larger surface area during deposition. The injection nozzle would travel along the surface of the substrate while depositing, as shown in Figure 42. After deposition, the silver track would be sintered with the use of a laser.

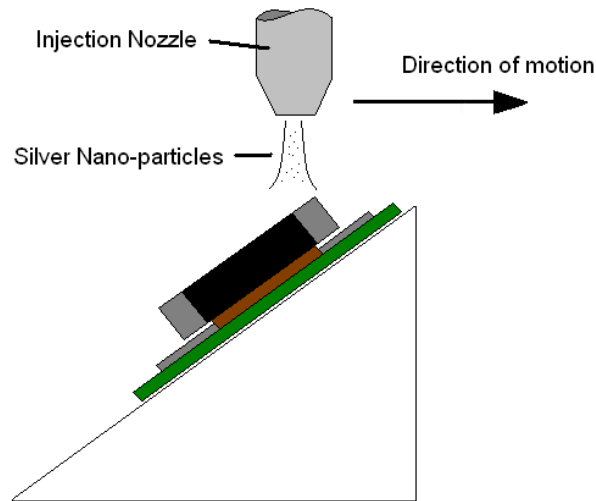


Figure 42 - Schematic showing the deposition process of the 'overhead pass' pattern

The goal of this method was to create a fillet-like interconnect that was shown in Figure 42. By passing the injection nozzle over the area where the resistor hovers over the silver contact pad, the silver nano-particles that are deposited during this time should accumulate and form a bond between the resistor and the contact pad.

Multiple tests were performed with this experimental setup, using experimental parameters from the experiments with the double-sided copper substrates as a guideline. A design of experiments was done involving these parameters in order to reveal the parameters that would most affect this deposition and sintering process. A table containing the results of the design of experiments is shown in Table 5.

Table 5 - Tabulated results of a design of experiments for surface mounted resistors on flexible boards

Test Number	Angle of Inclination	Resistor Size	Deposition Speed	Layers	Laser Speed	Laser Power	Burned	Conductive
1	45	Large	0.1 mm/s	4	1 mm/s	1.25 W	Yes	Yes
2	40	Small	0.5 mm/s	4	1 mm/s	1.25 W	No	No
3	45	Large	1 mm/s	16	1 mm/s	1.25 W	Yes	Yes
4	40	Small	0.5 mm/s	8	1 mm/s	1.25 W	Yes	No
5	45	Large	5 mm/s	32	1 mm/s	0.6 W	No	No
6	40	Large	1 mm/s	16	1 mm/s	0.6 W	No	No
7	45	Large	5 mm/s	32	1 mm/s	1.25 W	No	Yes
8	40	Large	1 mm/s	16	1 mm/s	1.25 W	No	Yes
9	45	Small	5 mm/s	32	1 mm/s	1.25 W	Yes	Yes
10	40	Small	1 mm/s	16	1 mm/s	1.25 W	Yes	Yes
11	45	Large	5 mm/s	50	1 mm/s	1.25 W	No	Yes

Due to very unsuccessful results from the double sided copper substrates which were placed on the same inclined mounting, only inclinations of 40° and 45° were used, as these two inclination angles should provide the best results compared to lower angles. From Table 5, the results show a mixed amount of successful and unsuccessful interconnects (labeled by the “conductive” column). The most important parameters are deposition speed and the number of layers, both which control the amount of silver that is deposited to form the silver track. A higher amount of silver placed onto the substrate provides a higher chance of a successful interconnect, which does not come too much as a surprise. It can also be noted that a lower laser sintering power appears to produce unsuccessful interconnects. Although only two tests have been done, the results should be taken into account in future experiments.

5.2.1.1 Damaging of Substrates During Sintering

Another important result to note is that there were a number of substrates that were burned during the deposition process. This was due to the close proximity of the laser to the edge of the silver pad while passing over the, or to the fact that some silver pads contained a hole, as

shown in Figure 43. This hole would expose the underlying layer of PET to the laser upon sintering the silver track and subsequently result in burning. Some burned results are shown in Figure 44. Although some burned results also contained successful interconnects, prevention of burning should be prioritized, as a damaged substrate is not desired. Through better deposition path positioning, future experiments no longer burned the substrates during sintering.

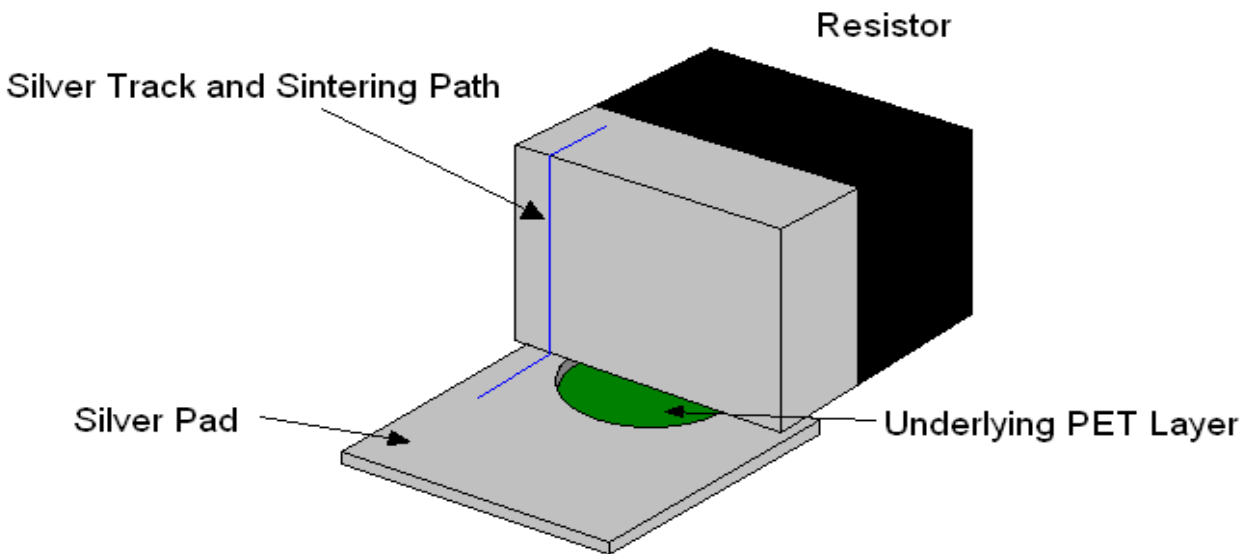
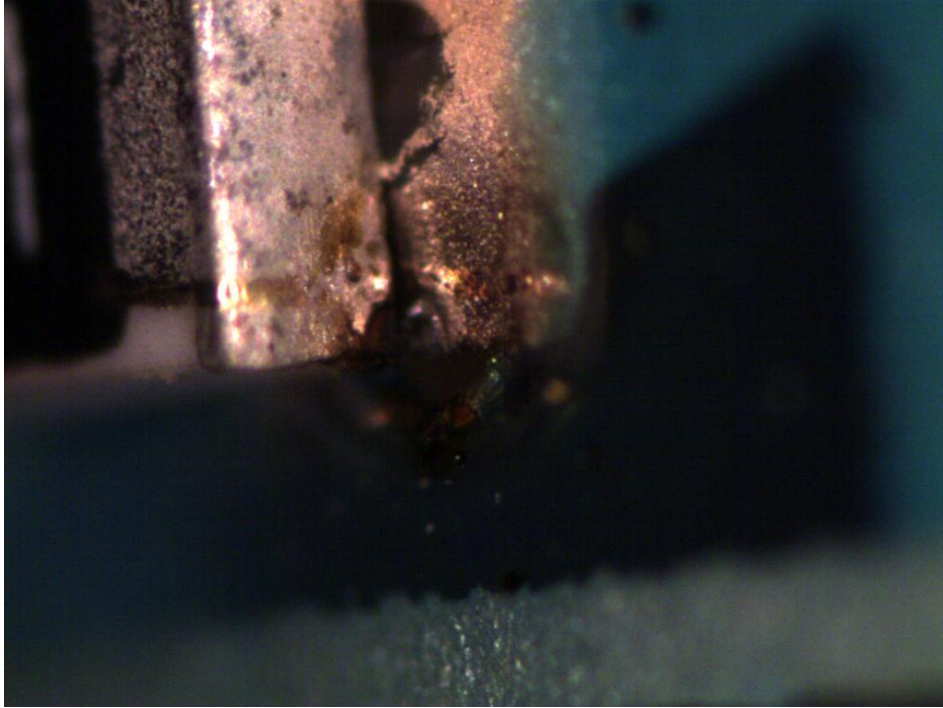


Figure 43 - Isometric schematic of a surface mounted resistor over a silver pad that contains a hole



(a)

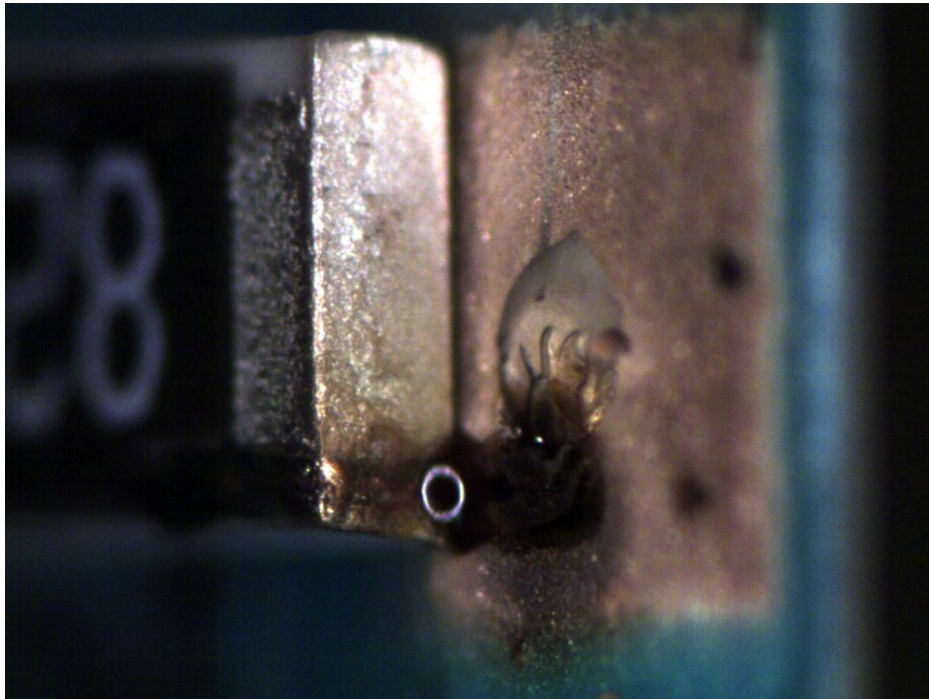
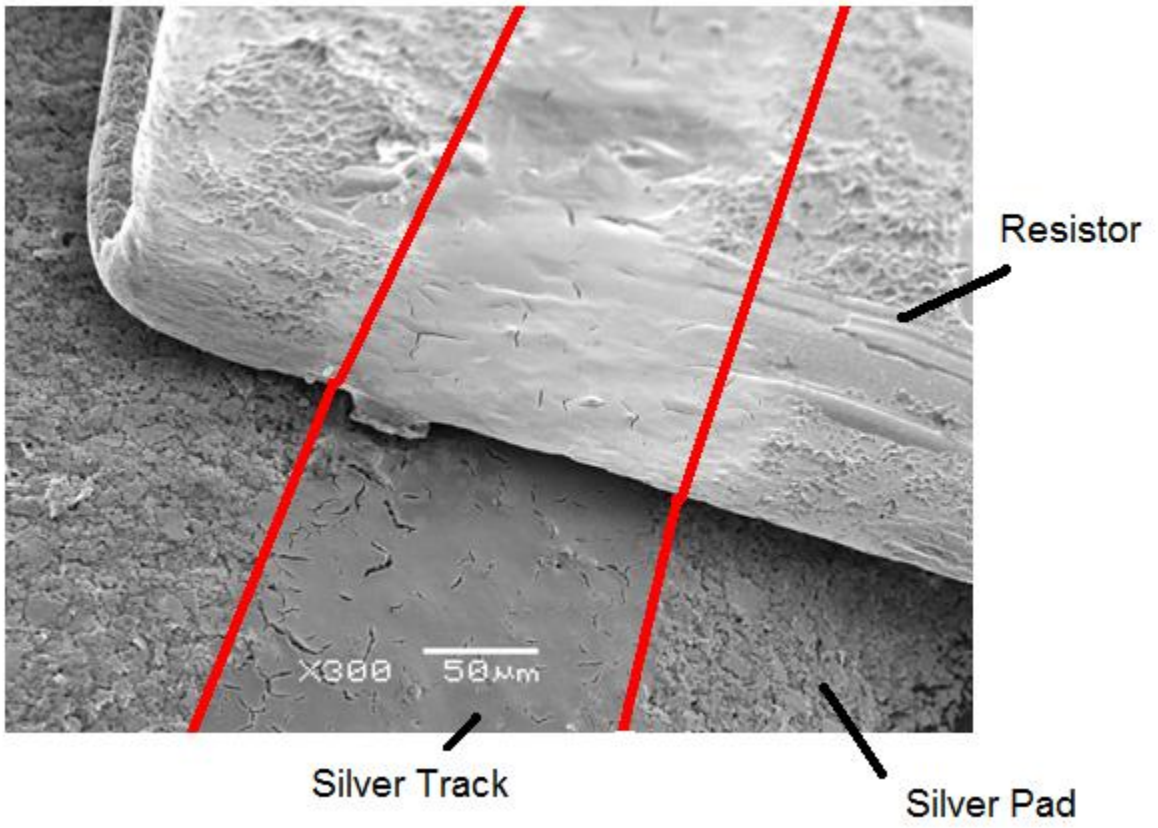


Figure 44 - Images showing parts of the flexible substrate which burned due to (a) laser passing too close to the edge of the silver pad during sintering, and (b) laser passing over the silver track which was too close to the hole in the silver pad

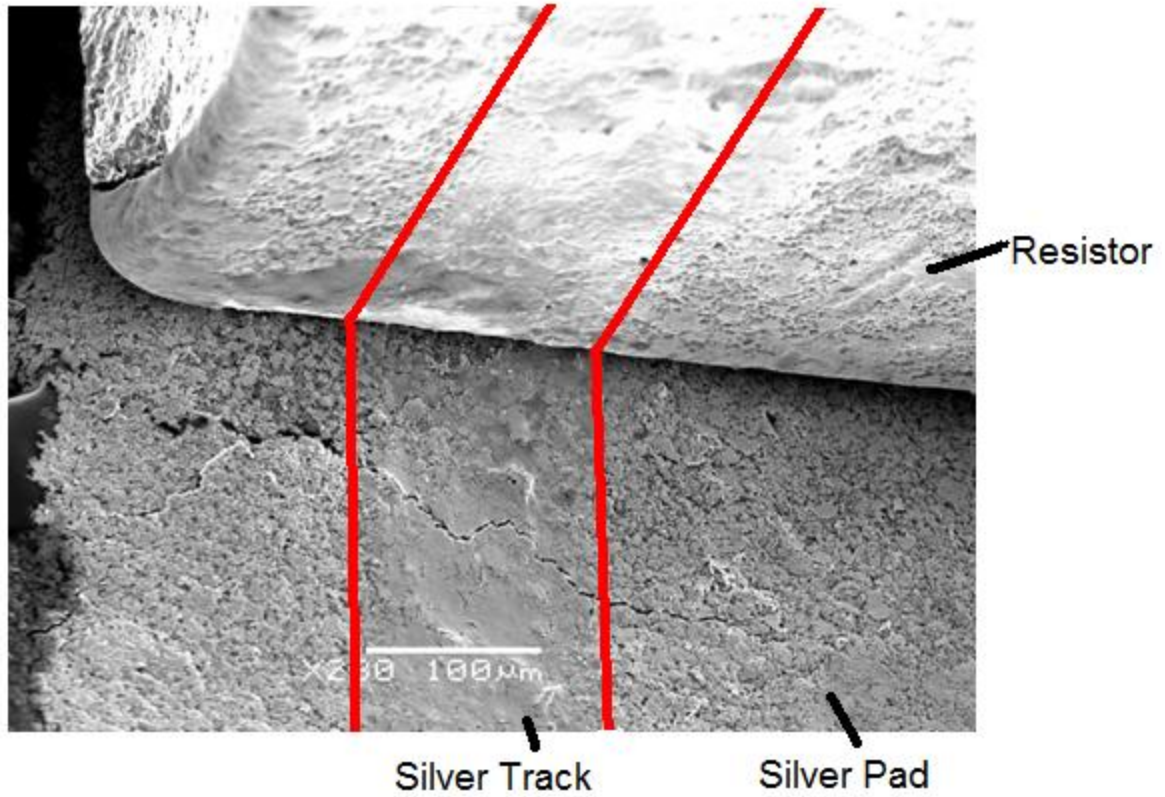
5.2.1.2 SEM Analysis

An SEM analysis was performed on some of the conductive samples in order to further analyze the results. These images are shown in Figure 45. Figure X(a) shows what is likely a fillet-type of interconnect that was formed during the deposition process. Since this particular substrate was conductive, it is likely that the fillet is the reason for the successful result.

However, the fillet does appear to cast a shadow beneath it, which raises doubt as to whether this fillet is the sole reason for the conductivity. It was noted that during the deposition process, the silver ink that was deposited remained in liquid form for some time. This combined with the inclination of the substrate may cause the silver to flow in between the resistor and the silver pad, creating an interconnect that is directly underneath the resistor. Figure X(b) shows the resultant SEM image of a conductive experiment. Here, it can be noted that there is no visual confirmation of an interconnect forming, which strengthens the speculation that silver is indeed flowing underneath the resistors and at times creating a successful interconnect. It can also be seen from the images in Figure 45 that the silver that remained on the deposition path was very thin, as the contours of the silver pad underneath the path are still visible.



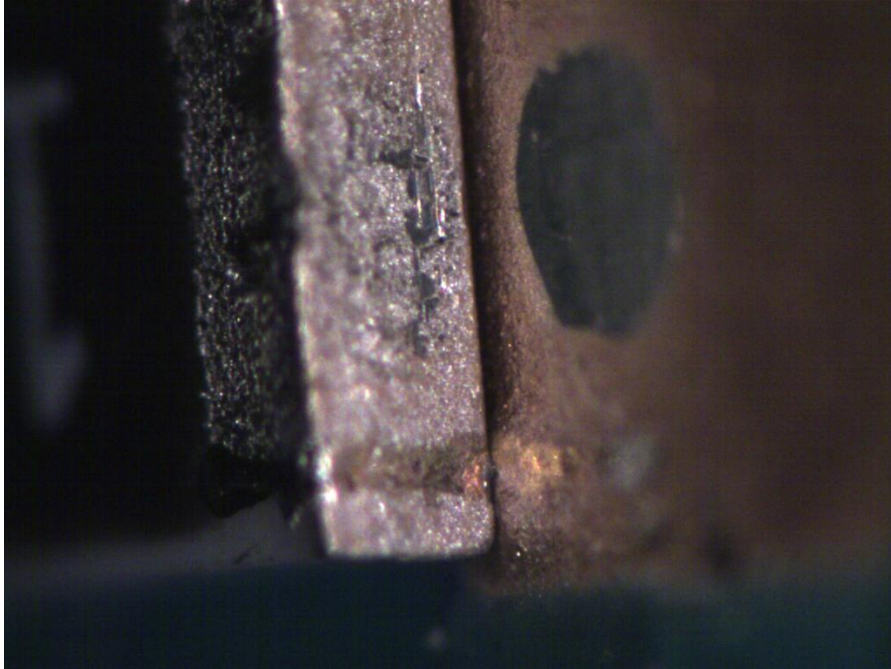
(a)



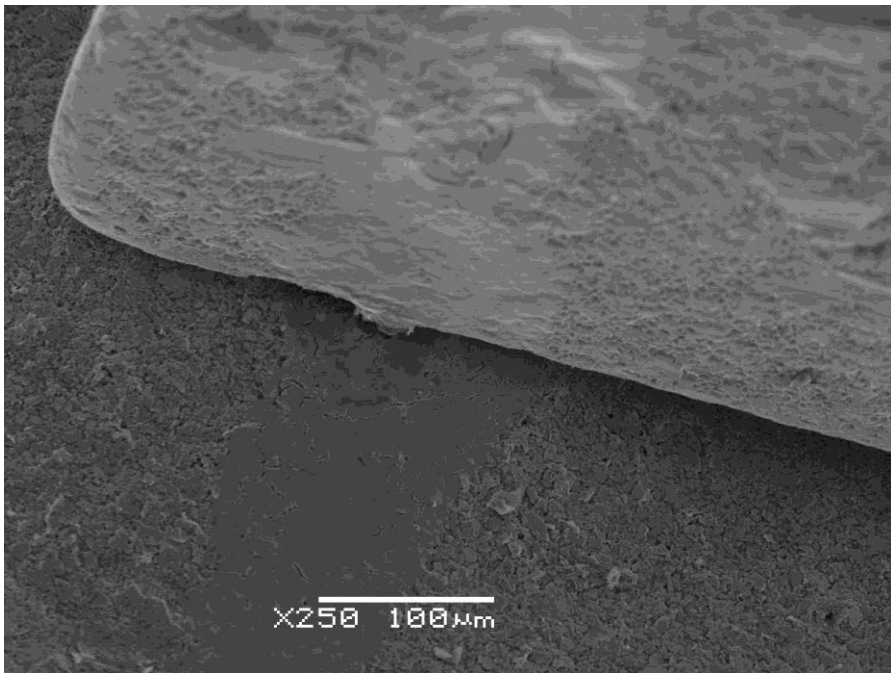
(b)

Figure 45 - SEM images of mounted resistors after deposition at (a) 40° inclination, 5 mm/s and 16 layers, (b) 45° inclination, 5 mm/s and 32 layers. The red lines in both images show the area where the silver path was deposited.

In an attempt to increase the thickness of the silver track, the atomizer flow rate was increased. This would allow more silver particles to flow onto the substrate to potentially create a thicker track. Figure 46 shows the optical and SEM images of one such experiment which resulted in a conductive interconnect. The optical image shows that there is indeed a visible confirmation of a fillet formed from the silver particles. Close inspection with the SEM shows the fillet connecting the silver pad to the resistor. However, it can still be noted that the silver track does not appear to have thickened very much compared to the previous experiments.



(a)



(b)

Figure 46 - Images of a fillet formed with silver deposition shown from (a) an optical camera, and (b) SEM.

The reason for the silver ink flowing somewhat freely as a liquid during the deposition phase was due to the inclined mounting. Since the mounting was not made of a conductive material, the hot plate on which the mounting was placed over did not heat the substrate enough to allow the silver to adhere well on contact. The inclination of the mounting adds to the effect by allowing the silver to flow down the incline and beneath the resistor. By replacing the mounting with a conductive mounting, the silver should adhere much better and should not flow beneath the resistor. An aluminum mounting was fabricated to address this problem.

5.2.1.3 Use of an Aluminum Inclined Mounting

By using the aluminum mounting in place of the previously used ABS mounting, the thickness of the track could be increased without much issue. This however produced a second problem related to track thickness. When large amounts of silver layers were deposited on one another, the silver track would crack in multiple places upon sintering, as shown in Figure 47. Since the substrate was now heated during deposition, the silver particles would adhere better on contact, which meant that large numbers of layers were no longer needed. By reducing the number of layers, the cracks showed less frequently while still producing some conductive results. The experiments showed many conductive interconnect results, but not many contained a visible fillet when inspected under the SEM.

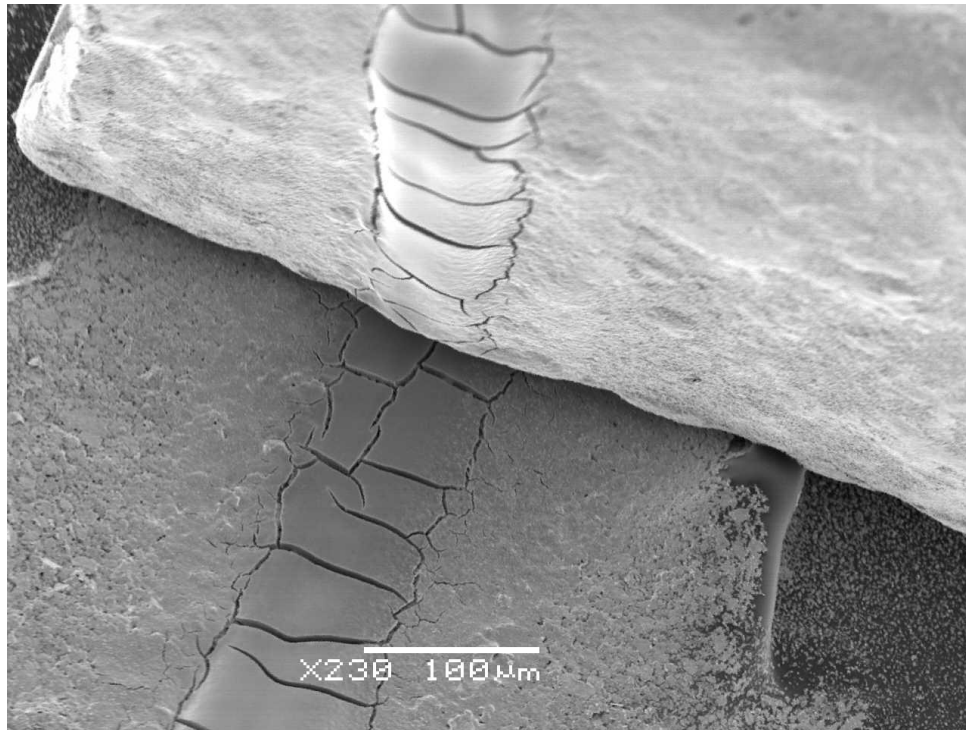


Figure 47 - SEM image showing a cracked silver track containing 100 layers of silver

Overall, this path pattern for deposition showed conductive results which were successful fillet interconnects on the edge of the resistor. However, there were also many experiments which resulted in a conductive interconnect being formed without forming a fillet, which is likely due to silver flowing beneath the resistor.

5.3.2 Across Path Deposition Pattern

Another path pattern that was considered consisted of depositing the silver nano-particles along the entire edge where the resistor is hovering over the silver pad as shown in Figure 48. This would allow the silver interconnect to have the potential of forming an interconnect in multiple places along the edge of the resistor, which would theoretically produce successful results in the majority of the experiments. Compared to the ‘overhead pass’ pattern, the across path deposition pattern takes slightly more time, but should be more reliable. The ‘overhead

pass' path pattern required 1 second for each layer, as opposed to 1.5 seconds for each 'across path' path pattern layer.

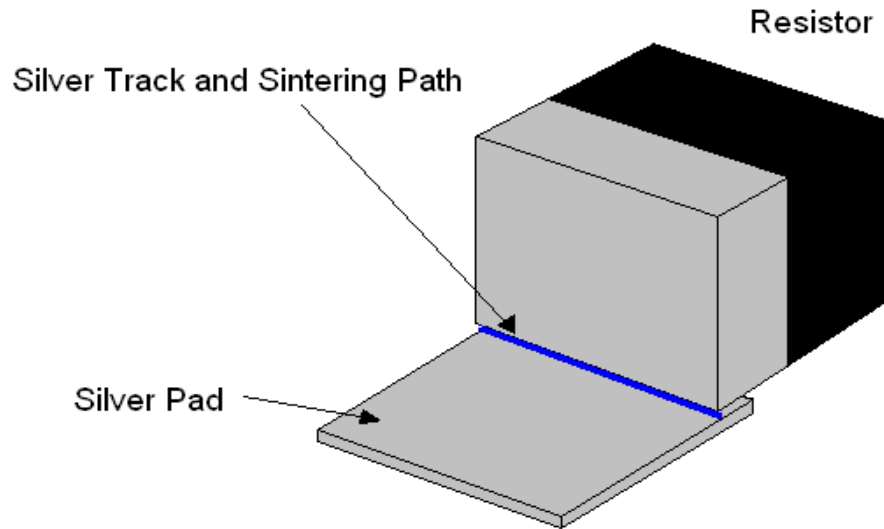
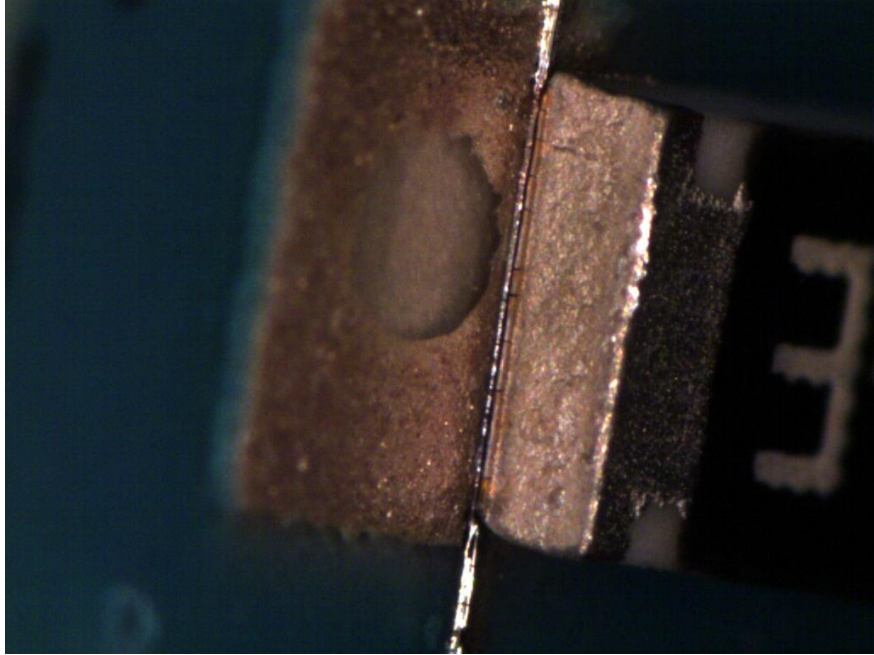


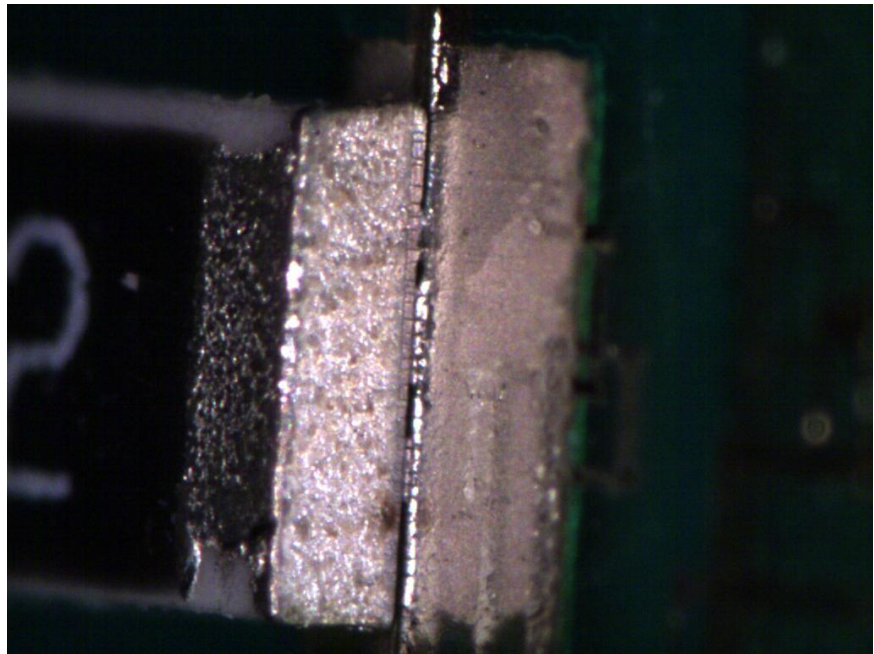
Figure 48 - Schematic showing the across path deposition pattern

5.3.2.1 Optical Imaging Analysis

Some of the across path pattern experiments resulted in successful interconnects. When observing through an optical microscope, the substrates appear to all have potential to contain successful interconnects, as shown in Figure 49. Figure 49(b) in particular shows an experiment where the silver track formed multiple instances of connections between the resistor and the silver pad.



(a)

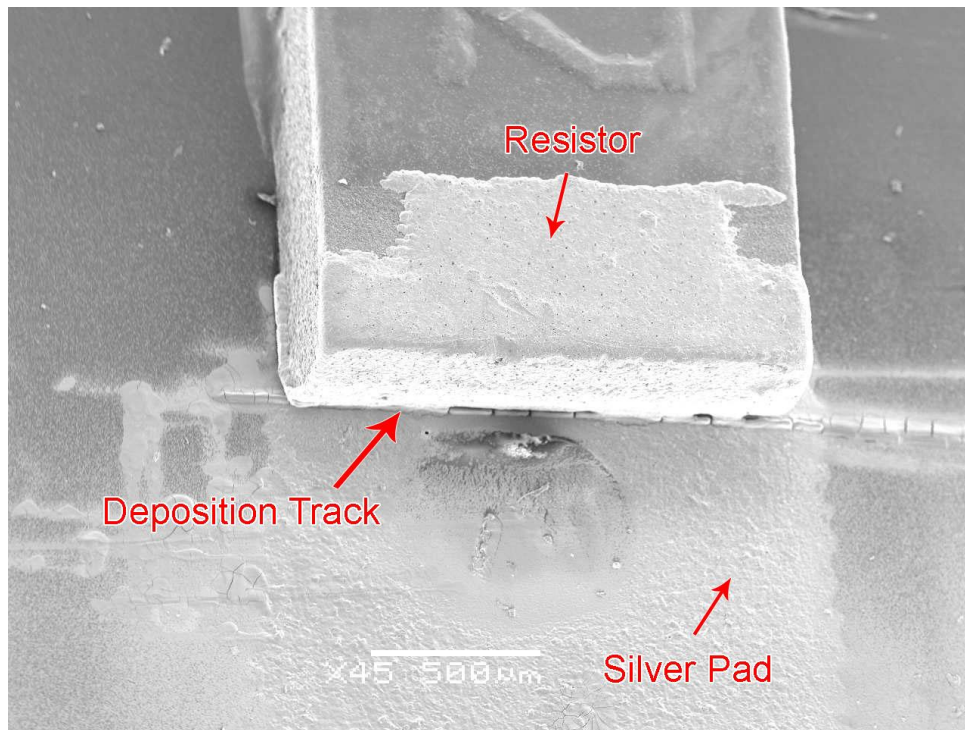


(b)

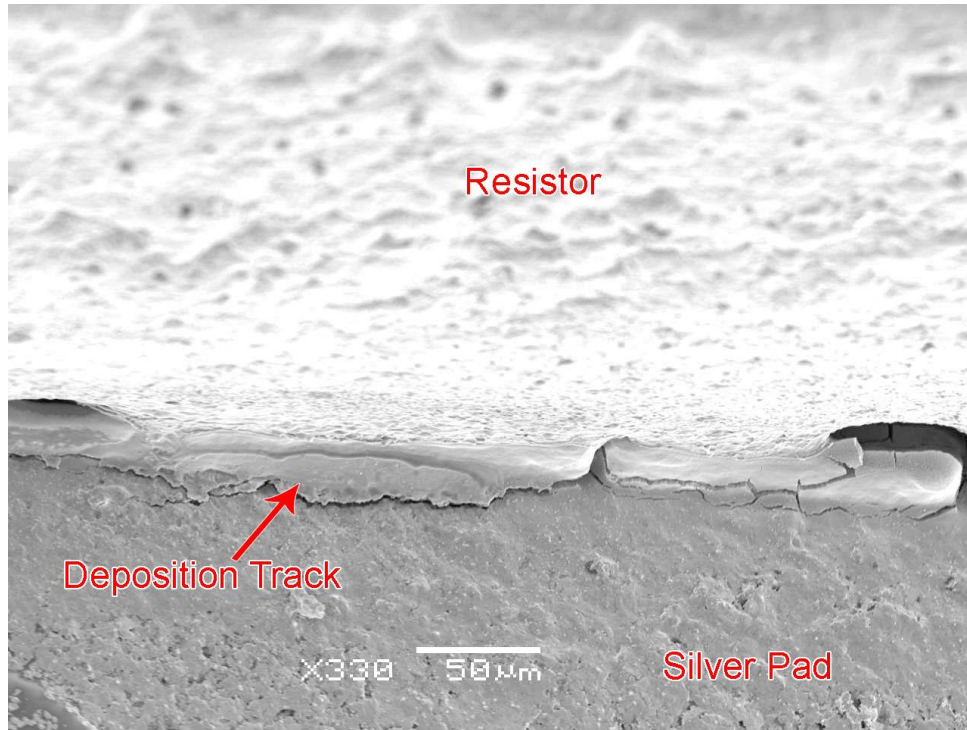
Figure 49 - Optical images showing a deposited silver track using the 'across path' pattern

5.3.2.2 SEM Analysis

When viewed under an SEM for further analysis, the successful interconnects showed multiple areas where the interconnect formed between the silver pad and the resistor as shown in Figure 50. Here, the interconnect has formed three different fillet-like connections along the edge of the resistor. Measuring the resistance of these interconnects with the precision positioner apparatus resulted in resistances in the range of 0.3Ω to 0.7Ω .



(a)



(b)

Figure 50 - SEM images of a successful interconnect formed with the 'across path' pattern. (a) shows the overall path while (b) shows a close-up of one of the interconnect fillets formed.

Although this deposition pattern had multiple chances for creating a successful interconnect, the occurrence of a successful interconnect was extremely rare, with the majority of the experiments resulting in non-conductive interconnects. It is theorized that the reason the success rate is extremely low is due to the large gap that is between the resistor and the silver pad. In order for the interconnect to be successful, the width of the silver track must be large enough to encompass the entire gap as well as part of the resistor and silver pad in order to form a successful interconnect. Although Figure 50 was conductive, it can be seen that there are many areas of the interconnect that do not reach the resistor from the silver pad, which is likely due to the width of the silver track not being wide enough. Even with the use of the widest silver

deposition width, the results were mostly non-conductive. This path pattern was deemed inefficient due to inconsistency and limitations of the LAMM system.

5.3.3 Zigzag Path Deposition Pattern

Due to the shortcomings of the previous deposition patterns, a new path pattern was proposed. A zigzag deposition pattern was chosen in order to gain the advantages of the previous patterns and is shown in Figure 51. A schematic showing this path pattern deposited on the substrate is shown in Figure 52.

One of the main problems with using the ‘across path’ pattern was based on the limitation of the width of the silver track that was deposited. Since the width of the silver track was unable to consistently cover both areas that required contact, the ‘across path’ pattern performed rather poorly. By using a zigzag, it does not have problems with the limitations on the width of silver, since the zigzag path travels over the gap between the resistor and silver pad rather than depositing only within the gap. Also, compared to the ‘overhead pass’ pattern, the zigzag will have multiple points in which the interconnect may have created a successful connection as opposed to one. The ‘overhead pass’ pattern also showed that it is capable of creating fillet-like interconnects, which means that the zigzag pattern has the potential to combine the advantages of both previous methods while discarding the disadvantages. An important change to note is that the effective path distance has increased, which means that the LAMM system will require more time to deposit the silver nano-particles along a zigzag path compared to the ‘across path’. The LAMM system required 3 seconds to trace the path once, as opposed to 1.5 seconds with the ‘across path’.

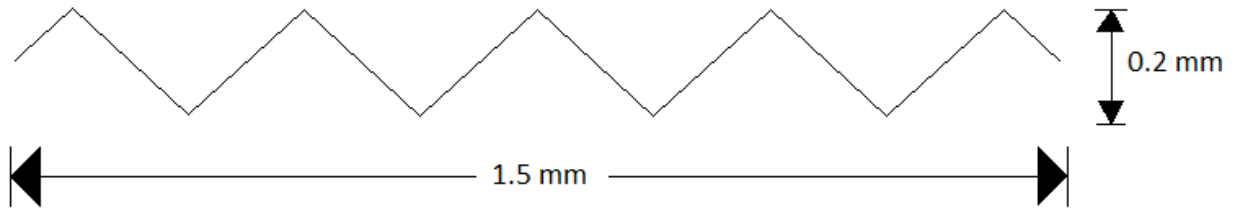


Figure 51 - Zigzag Path Deposition Pattern

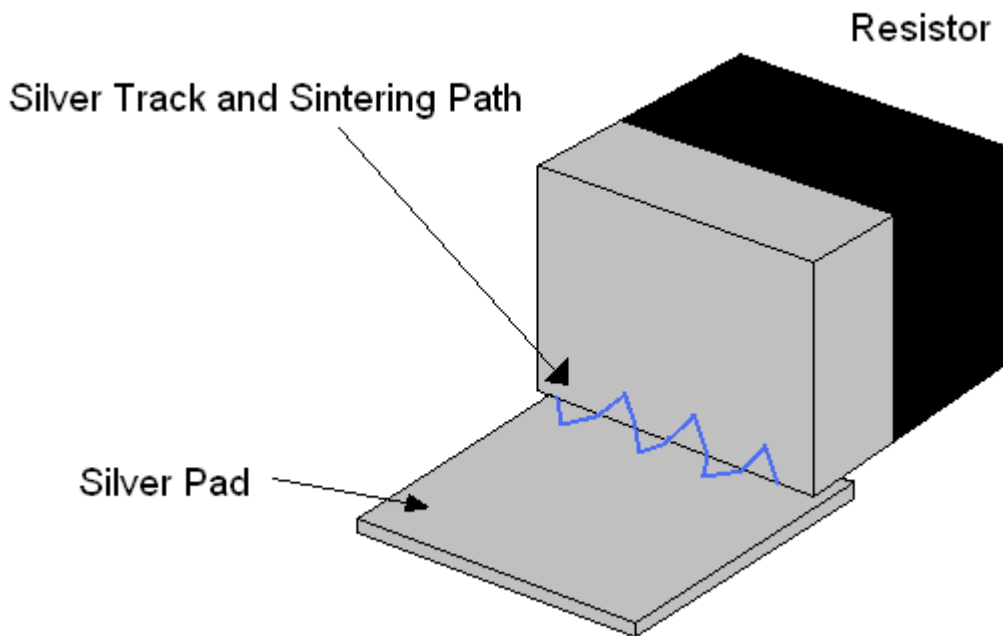


Figure 52 - Schematic showing the zigzag path pattern of deposition

The experiments involving the zigzag path pattern were able to form successful interconnects. Due to a limited supply of substrates, only 5 experiments were performed in this manner, with all 5 experiments resulting in successful interconnects. The main factor that likely allowed such a large number of successful results was likely the fact that the zigzag path allowed for the silver interconnect to form a successful interconnect in multiple areas on the same substrate. For these experiments, 6 layers of silver were deposited with an increased atomizer

flow rate of 16 ccm in order to allow more silver to be deposited. The remaining parameters were left unchanged.

5.3.3.1 Optical Imaging Analysis

Upon inspecting the substrates after deposition and sintering, in many cases it was possible to visibly confirm that the silver nano-particles had formed a successful interconnect, as shown in Figure 53. Measurement with an ohmmeter afterwards would be able to confirm that conductivity.

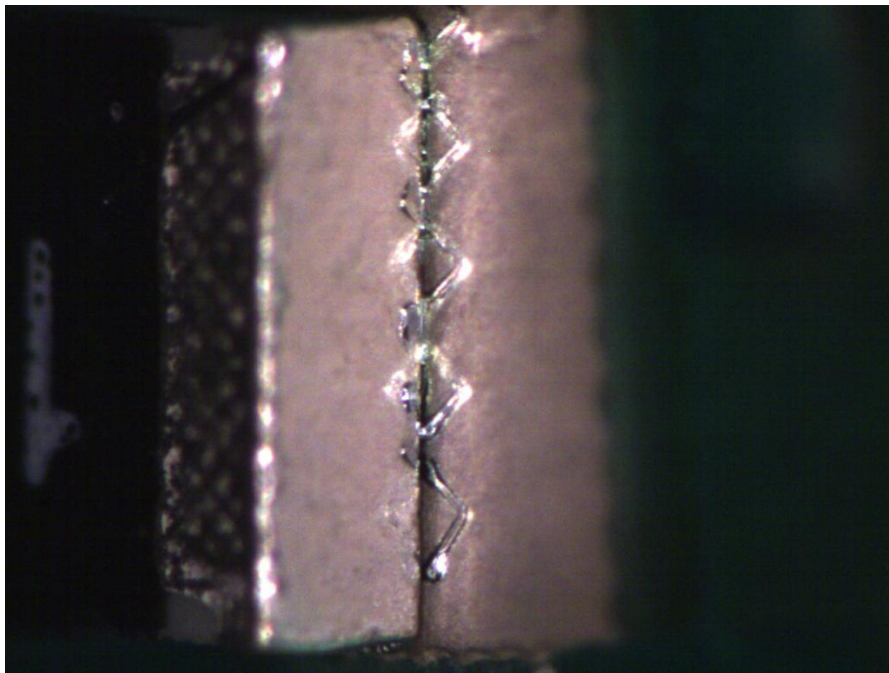


Figure 53 - Optical image showing a conductive interconnect deposited using a zigzag path pattern

A shorter zigzag path pattern was utilized in order to reduce the amount of time the system would require to deposit all layers of silver. The path was shortened by half, such that the path no longer spanned the entire width of the resistor, which would reduce the deposition time by half in the process. Shown in Figure 54, the shortened zigzag path was still capable of

forming successful interconnects, and did not have any unsuccessful results. Since the shortened zigzag path also contains multiple areas where the interconnect can create a successful bond, it is likely that this is the reason for the successful results.

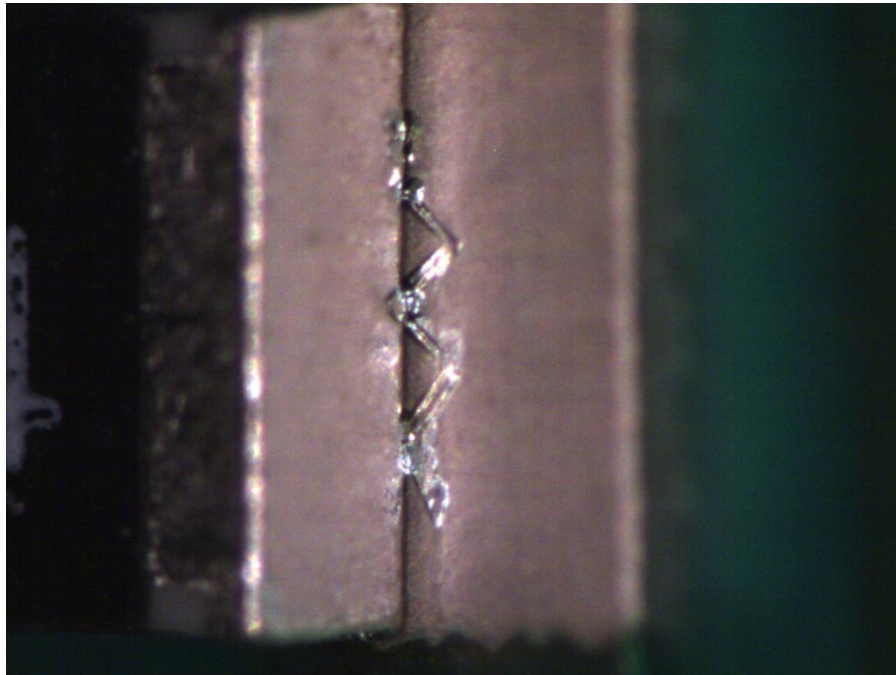


Figure 54 - Optical image of a silver interconnect deposited using a shortened zigzag path pattern

5.3.3.2 Manual Mounting of Resistors

In order to continue future experiments with surface mounted resistors on flexible substrates, the resistors were required to be manually mounted due to a shortage of supply from the supplier. By manually mounting the resistors with an epoxy, the resistor would not be placed as precisely as if it were placed with the use of an automated system. Due to this lack of precision, many resistors faced many problems after mounting, such as having the epoxy flow outwards onto the silver pad or having an insufficient amount of epoxy, which resulted in having the resistor touching the pad, rendering these substrates unusable for experimentation. Also, after

mounting the resistors, the gap between the resistor and the silver pad would vary between substrates due to the imprecision of the placement process, which would be problematic when performing repeatability experimental tests.

When the zigzag path pattern was applied to these new substrates, it was quickly observed that a large number of deposited interconnects failed to produce conductive results. Approximately half of the experiments were unsuccessful at creating a conductive interconnect. The tabulated results are shown in Tables 6 and 7. The reason for these poor results was likely due to the variance in the gap caused by manually mounting the resistors. The zigzag path patterns demonstrated approximately a 50% success rate using the full zigzag path pattern, while the shortened path pattern performed with approximately a 33% success rate when used on the new substrates.

Table 6 - Conductivity results using a full zigzag path pattern on surface mounted resistors manually placed on a flexible board

Full Zigzag Path Pattern			
Experiment	Layers	Atomizer Flow Rate (ccm)	Conductivity
1	10	16	Yes
2	10	16	Yes
3	10	16	Yes
4	10	14	No
5	20	14	No
6	10	14	Yes
7	10	16	No
8	10	16	No
9	10	16	No
10	10	16	Yes
11	10	16	No
12	10	16	Yes
13	10	16	Yes
14	10	16	No

Table 7 - Conductivity results using a shortened zigzag path pattern on surface mounted resistors manually placed on a flexible board

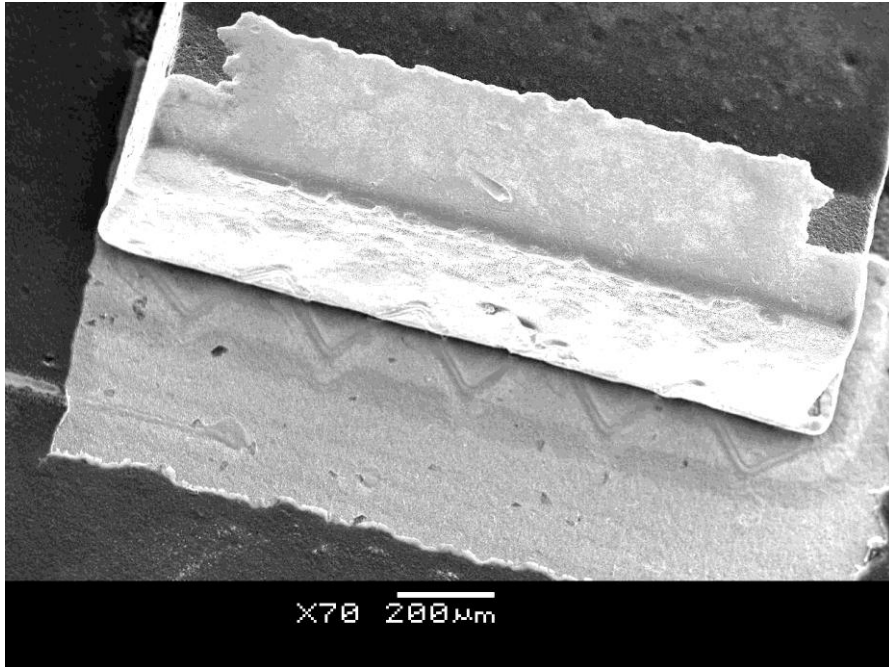
Shortened Zigzag Path Pattern			
Experiment	Layers	Atomizer Flow Rate	Conductivity
1	20	14	No
2	10	14	Yes
3	10	14	No
4	10	14	Yes
5	10	14	Yes
6	10	14	No
7	10	14	No
8	10	16	No
9	10	16	No

The results show the shortened zigzag path pattern demonstrating a very low success rate throughout the experiments regarding the new substrates. This is somewhat expected, as the chances of forming a successful connection between the resistor and the silver pad has been reduced by using the shortened path in place of the full path, thus reducing the number of successful experiments. The reason the shortened path contained less experiments was due to the initial poor results from using the shortened path. After repeated failures, the focus was switched to the full zigzag path, since the full zigzag path pattern is more reliable than the shortened path pattern.

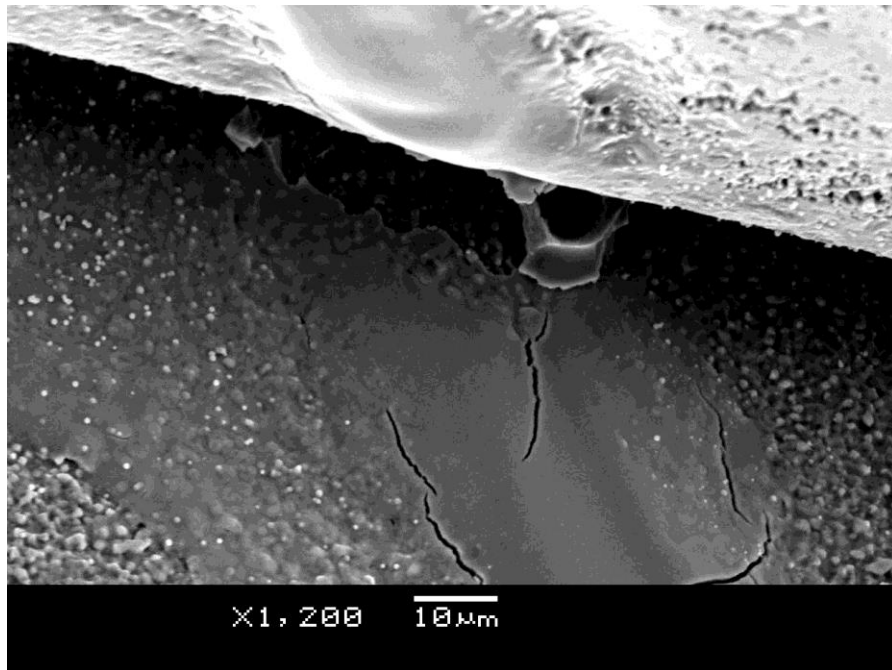
5.3.3.3 Optical and SEM Analysis for Manually Mounted Resistors

When an SEM analysis was performed on a conductive substrate, it was quickly observed that the interconnects formed on many of these new substrates were not formed very well, as shown in Figure 55. Although the interconnect formed a conductive connection between the resistor and the silver pad, Figure 55(a) shows that the interconnect formed was not a fillet-type

of connection, and appears to be on the verge of breaking. With interconnects formed as such, it is not surprising that the experiments on the new substrates performed poorly.



(a)



(b)

Figure 55 - SEM images of the silver interconnect formed using the zigzag path pattern. Full interconnect is shown in (a) and one of the connections formed between the resistor and the silver pad is shown in (b).

It was also observed at times that the part of the silver track that was deposited on the front face of the resistor may not adhere to the resistor too well, which would cause the silver to flow away, resulting in an extremely small amount of silver that would remain on the front face of the resistor, as seen in Figure 56. The silver particles acting in such a manner is most likely due to insufficient heating on the front face of the resistor. Since this did not occur with the previous substrates that were mounted with an automated system, it is theorized that the gap between the resistor and silver pad have increased such that the heat from the aluminum mounting is unable to sufficiently heat the resistor.

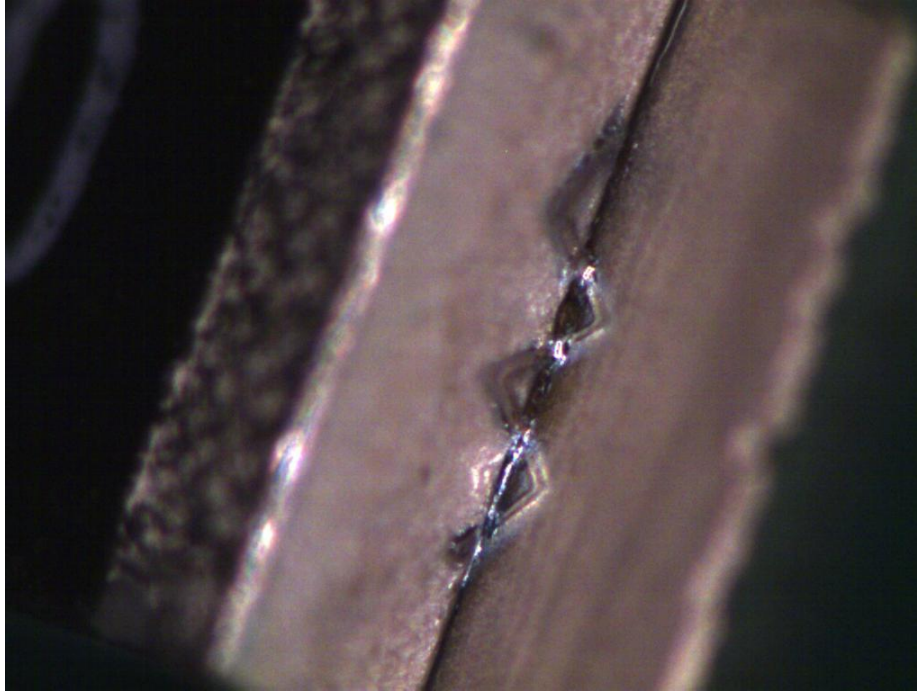


Figure 56 - Optical image of a silver interconnect that did not adhere well to the front face of a surface mounted resistor

Overall, the zigzag path pattern performed well with the substrates that contained resistors mounted with an automated system. When a new substrate that contained resistors mounted manually was introduced, the zigzag path pattern did not perform very well, but managed to have a 50% success rate when using the full zigzag path pattern.

5.3.4 Dot Solder Deposition Pattern

Due to the recent change in the substrates, a new deposition pattern was needed to produce more reliable interconnects on the new substrates. A ‘dot solder’ method was proposed, which consisted of depositing silver nano-particles on the corner formed between the resistor and the silver pad, as shown in Figure 57. The silver particles are then left to accumulate and form a ball of silver, which will act as the interconnect between the resistor and the silver pad. This is very similar to soldering, hence the name of the method dubbed as the ‘dot solder’ method.

Compared to traditional soldering, this process does not require extremely high temperatures in order to liquefy the conductive material. If traditional soldering methods were incorporated into this substrate, the extremely high temperatures would damage or warp the flexible substrate beyond recovery.

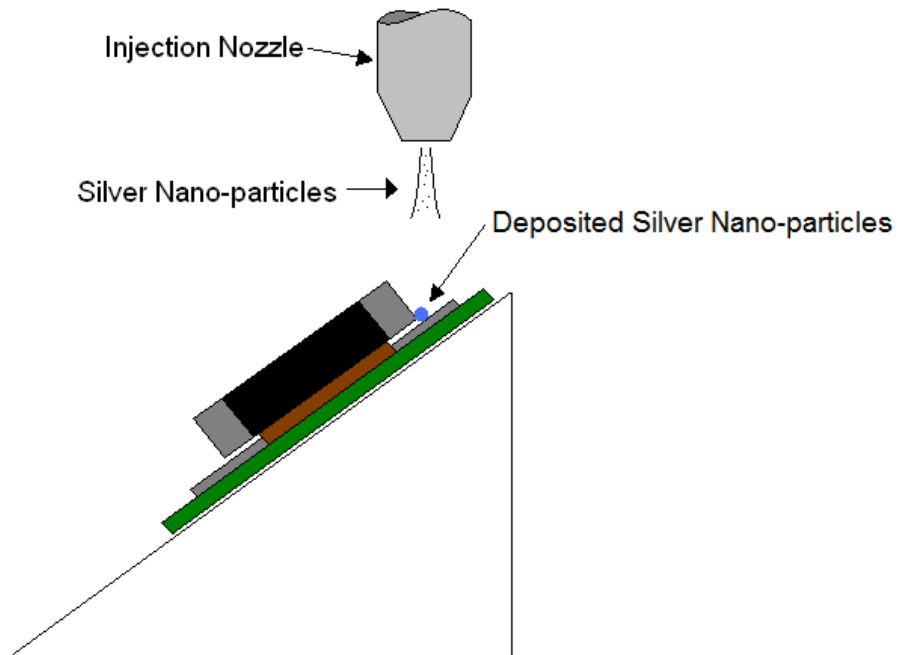


Figure 57 - Schematic showing the deposition process using a 'dot solder' method

A proof of concept was performed initially in order to ensure that the procedure was feasible. The atomizer gas flow rate was set to 16 ccm, and the silver nano-particles were deposited on the corner of the substrate for 8 seconds. The silver particles accumulated into a ball and visibly formed an interconnect. After sintering, the substrates were tested for conductivity with the use of an ohmmeter. The ohmmeter showed that the interconnects were indeed successful, and a design of experiments was implemented. The chosen parameters for the design of experiments were atomizer flow rate, deposition duration and laser sintering duration.

The atomizer flow rate and deposition duration were chosen for the design of experiments, as these two parameters control the amount of silver nano-particles that are deposited onto the substrate. The deposition duration parameter replaces the deposition speed and number of layers from the previous experiments, since the injection nozzle will not be required to move for the ‘dot solder’ experiments. Instead, the duration for which the nozzle is depositing will be the parameter that controls the thickness of the silver ‘track’. The laser sintering duration was chosen as the parameter that controls the sintering process. The sintering process did not appear to be a very large issue in the previous experiments, aside from any substrate burning problems. This parameter was placed as a lower priority in the design of experiments. A table showing the process parameter ranges is shown in Table 8.

Table 8 - Process parameter ranges for the design of experiments using the 'dot solder' method

Process Parameters Ranges		
Deposition Duration	Atomizer Flow Rate	Laser Sintering Duration
1 - 7 seconds	12 - 16 ccm	1 - 3 seconds

The results from the initial experiments of the design of experiments are shown in Table 9. These initial experiments were done in order to determine which direction the future experiments would follow based on the effect of the parameters. It was observed that when the laser sintering duration was increased to 2 seconds from 1, the results were mainly non-conductive. This is likely due to over-sintering. When sintering with high temperatures for a long duration, it has been shown that silver nanoparticles will begin to form pores and a deposited silver track may become discontinuous [54]. It is possible this state was reached earlier, due to the laser intensity being higher than the required sintering temperature of around 150 °C to 350

°C [50]. Also to note is that once the flow rate was reduced, the deposition duration needed to increase in order to maintain conductive results.

Table 9 - Results for the design of experiments regarding the 'dot solder' method

Experiment Type	Deposition Duration (s)	Atomizer Flow Rate (ccm)	Laser Sintering Duration (s)	Conductive	Non-Conductive	% Success
A	1	16	1	4	1	80.00%
B	1	14	1	0	4	0.00%
C	1	16	2	2	3	40.00%
D	2	14	1	5	0	100.00%

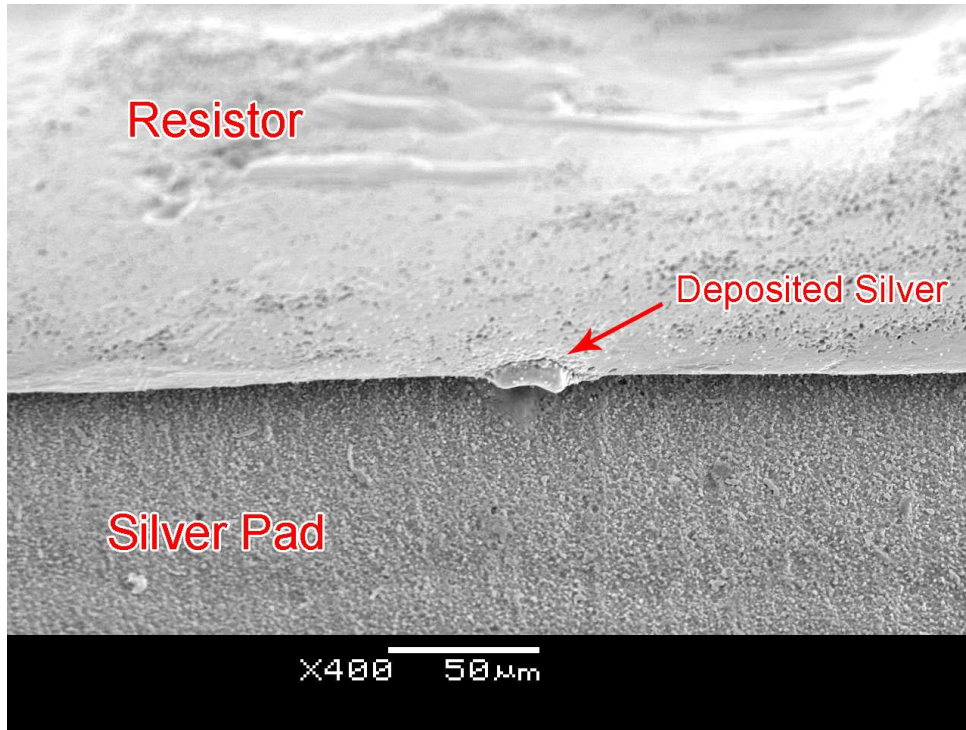
Due to the need to increase the deposition duration while decreasing the atomizer flow rate to maintain conductive results, the lower deposition speeds were not considered. A faster process is more preferable, as it would have a more meaningful impact on the industry. Experiments A and D were chosen to be repeated, as experiment A requires the least processing time and Experiment D demonstrated the best success rate. The results of these repeated tests are shown in Table 10. It can be seen that the success rate for both experiment types decreased, with Experiment D decreasing drastically. However, despite the decrease in the success rate, the success rates were not poor. It should also be remembered that the 'dot solder' method was introduced in order to increase the success rate for the new substrates with manually mounted resistors. This method has performed rather well considering the varying gap distances in the new substrates and can be expected to improve if used on substrates with resistors mounted through an automated system.

Table 10 - Repeatability results for the 'dot solder' method

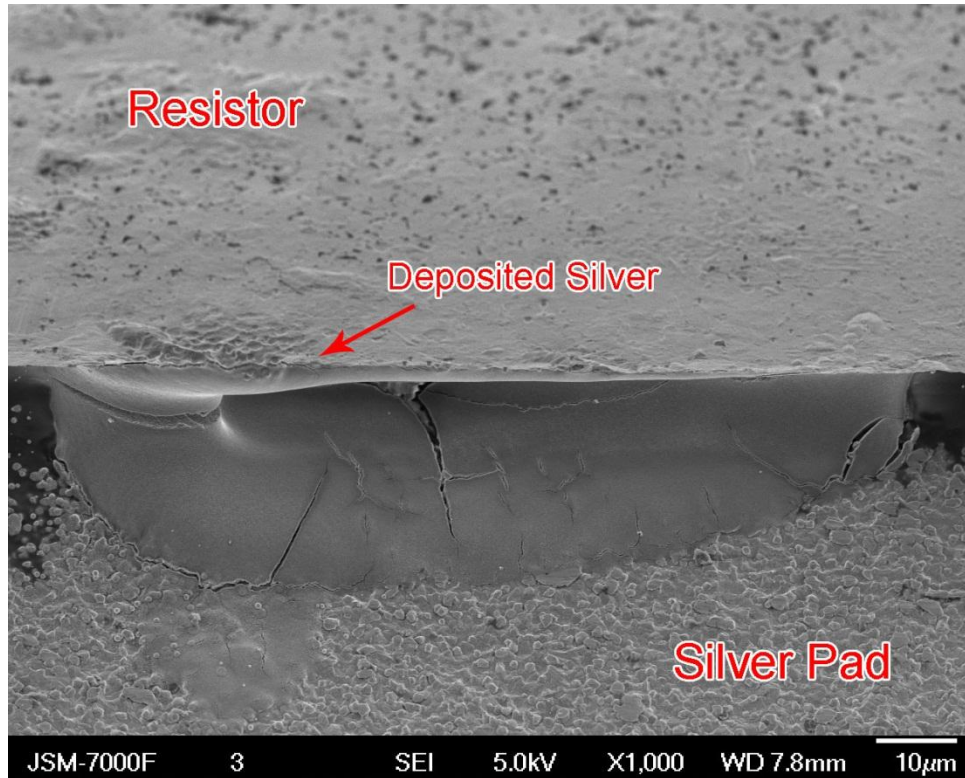
Experiment Type	Deposition Duration (s)	Atomizer Flow Rate (ccm)	Laser Sintering Duration (s)	Conductive	Non-Conductive	% Success
A	1	16	1	12	5	70.59%
D	2	14	1	6	4	60.00%

5.3.4.1 SEM Analysis

Some experiments with successful interconnects were analyzed by an SEM and the results are shown in Figure 58. As seen from Figure 58, the formation of the interconnect appears to differ greatly between the two different experiments. In fact, each substrate that was analyzed with the use of an SEM showed a different shape of the interconnect. Some were not easily visible, yet some very clearly showed the silver interconnect reaching to both the resistor and the silver pad, such as in Figure 58(b). Interconnects formed using the same parameters also showed the possibility of differing greatly in terms of the shape of the interconnect. Due to this large variation between the formation of the interconnects, no conclusion could be drawn with regards to the shape formation of the interconnect and the parameters used in the deposition and sintering process.



(a)



(b)

Figure 58 - SEM images showing the resultant 'dot solder' experiments that used the parameters of (a) Experiment A, and (b) Experiment E.

5.3.4.2 Creation of an Effective Variable

Due to changing multiple variables in order to gain successful interconnects, the resistances of the interconnects would need to be contrasted to the amount of silver deposited in order to draw a conclusion. The amount of silver deposited is controlled by multiple parameters: sheath gas, atomizer flow rate, and duration of deposition. In order to quantify these parameters together, an effective variable τ_{eff} was developed to represent the amount of silver deposited in compilation of all three parameters together, as shown in Equation 5.1:

$$\tau_{eff} = \frac{Q_{atomizer}}{Q_{sheath}} t \quad (5.1)$$

Where $Q_{atomizer}$ represents the atomizer flow rate, Q_{sheath} represents the sheath gas flow rate, and t represents the duration of deposition. This equation was formed after observation on how each parameter affects the resultant amount of silver. Whenever the atomizer flow rate was increased, it was noted that the amount of silver that was deposited was increased. The sheath gas controlled the width of the silver tracks in previous experiments, where a lower sheath gas flow rate would result in a thinner path. Duration of deposition, as can be expected, would increase the amount of silver if the duration was increased.

The volume of the deposition was measured from a test where numerous depositions of silver were performed on a glass plate with various parameters. Table 11 shows the ranges of the parameters used in this test. An optical microscope was used to measure the height of the silver for each deposition. This value was used in conjunction with the diameter to achieve the volumetric value that would represent the effective variable τ_{eff} .

Table 11 - Ranges of values for parameters used in experiment to determine volumetric value of silver deposition

Sheath Gas	Atomizer Flow	Time
45 - 50 ccm	12 - 16 ccm	1 - 3 s

The volume of silver was calculated using the height and diameter of the silver deposition measured from the optical microscope. The equation for the volume of a cylinder ($\pi r^2 h$) was used as an approximation for the shape of the deposition. Although the silver deposition did not have a uniform diameter along the entire height, the equation for a cylinder would suffice for an

approximation. The values of the approximated volume are plotted against the effective variable τ_{eff} in Figure 59. It can be seen that different values of time affect the resultant effective variable greatly and are separated into different clusters. Each cluster shows the approximate volume increasing as the effective variable increases, although at different rates for each value of time. With this information, as long as the duration of deposition is kept constant when analyzing, the effective value can be used as a comparable measurement towards volume of silver when analyzing the resistance of each successful experiment.

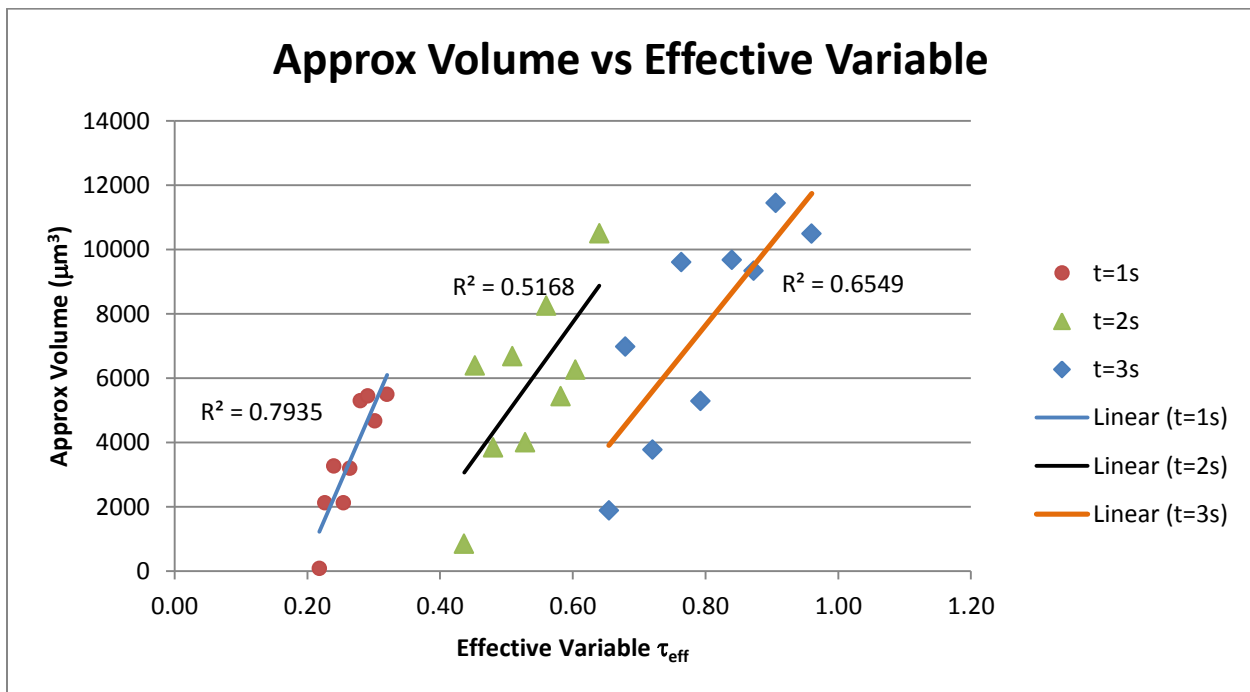


Figure 59 - Approximate volume of deposited silver on a glass plate plotted against the effective variable τ_{eff}

The experiments with successfully formed interconnects were analyzed for resistance using the DCM 210 precision positioners and source measure unit, since manual resistance measuring with the use of a digital multimeter has an extremely high chance of destroying the interconnect bond. Overall, the resistance values ranged from 0.184Ω to 42.5Ω . The comparison between resistance and effective variable is shown in Figure 60. Only two

experiments (A and D) were measured and plotted due to these experiments resulting in enough successful interconnects that were capable of resistance measurements. Experiment D, which was performed with 2 seconds of deposition, 1 second of laser sintering and 14 ccm atomizer flow rate, showed a wider distribution of resistances compared to experiment A, which was performed with 1 second of deposition, 1 second of laser sintering and 16 ccm atomizer flow rate.

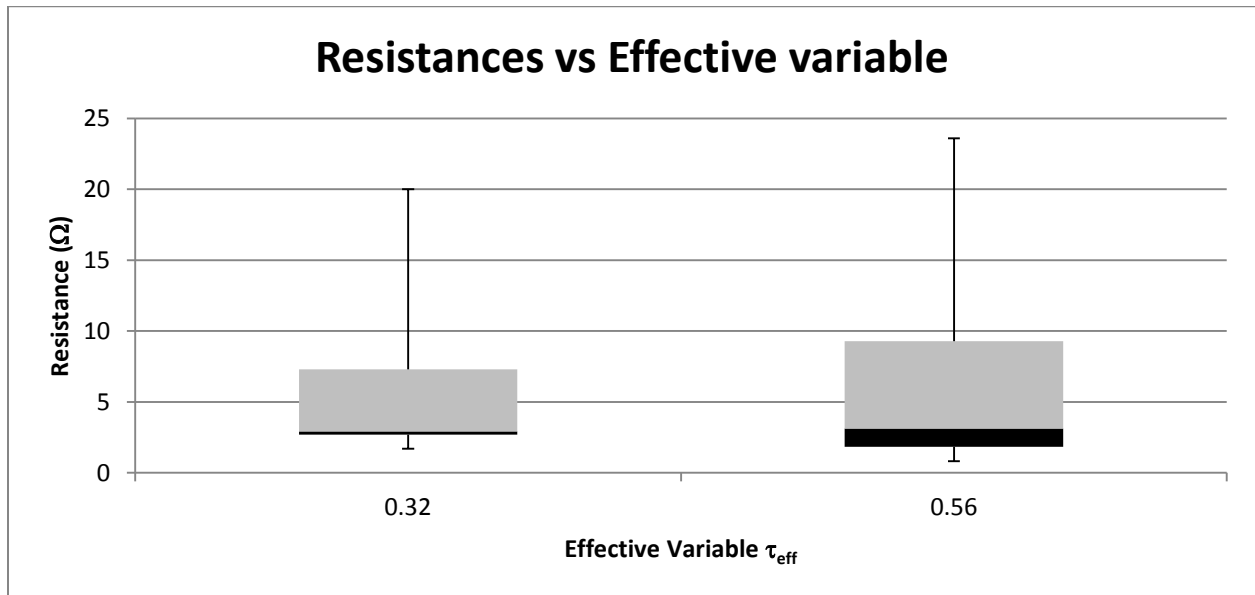


Figure 60 – Box and whisker plot showing measured resistances plotted against effective variable τ_{eff} for Experiments A (0.32) and D (0.56)

As seen from Figure 60, both experiments A and D managed to create interconnects with a range of resistances, however, the majority of the resistances are under the 5 Ω range. This shows that the quality of interconnects is good and generally have low resistances. It can also be noted that with an increase in the effective variable, the spread of resistances appears increase. Although it is difficult to compare effective variables that use different deposition duration times, it must be remembered that the effective variable scales with the approximate volume of silver, which then shows that increasing the amount of silver likely creates a wider range of resistances.

This is likely due to the appearance of cracks in the silver as mentioned in a previous chapter, which appear more frequently when the amount of silver is increased. It is also important to note that Experiment A had a higher success rate compared to Experiment D, which also shows this trend. There is lack of data to form a solid conclusion; however, it appears that the increase of silver increases the range of resistances, while keeping the majority of the resistances below 5 Ω .

5.3.5 Summary

A number of deposition patterns were used in an attempt to form an interconnect between surface mounted resistors and underlying contact pads on a flexible board. All patterns were able to form conductive interconnects; however some patterns had more success than others.

The ‘overhead pass’ deposition pattern attempts to form a single fillet on the corner between the resistor and silver pad. This method failed often due to the pattern only creating one fillet for a chance at forming a successful interconnects. It was also noted at this point that the laser has the potential to burn the flexible substrate if the area of irradiation is too close to an exposed area of the flexible substrate. Experiments were adjusted accordingly to maximize the distance between the area of irradiation and the closest exposed areas of the flexible substrate.

The ‘across path’ deposition pattern attempts to form a silver track along the width of the resistor and the silver pad, theoretically forming a large conductive band as an interconnect. This pattern also had little success due to the width of the silver track being insufficiently wide enough to cover the entire gap formed between the resistor and silver pad.

The ‘zigzag’ deposition pattern had much more success than the previous deposition patterns due to the method incorporating the benefits of both previous patterns. The ‘zigzag’ pattern forms multiple ‘overhead pass’ patterns, while simulating a smaller ‘across path’ pattern.

This method proved to be quite successful. When a variation was introduced to the placement of the surface mounted resistors, which caused a variation in the gap size between the resistor and contact pad, the 'zigzag' deposition pattern showed much poorer results. Due to a lack of supply for the substrates, all future experiments would use the variant substrates. This would require a new deposition pattern, since the 'zigzag' pattern did not have a very high success rate with the new substrates.

A new deposition pattern, the 'dot solder' pattern, was proposed for the new substrates. This method consisted of leaving the deposition nozzle stationary and having the silver nanoparticles pile up onto the substrate, forming a bridge between the contact pad and the resistor. A design of experiments was performed and two sets of parameters were presented as the most successful. The results from the two parameter sets could not be compared easily due to the number of parameters involved. In order to compare the different sets of parameters, an effective variable was formed based on observations on the effects of the parameters with respect to the amount of silver that was deposited. Due to time constraints, only a small amount of data was available for analysis; however, the data shows a trend in which an increase in the amount of silver causes a wider range of resistances for the interconnects. The resistances on average showed values under 5Ω .

Chapter 6

Conclusions and Recommendations

6.1 Conclusions

The following conclusions can be drawn from this thesis:

- 1) The double-sided copper substrates were intended to have the interconnect formed within a chamfered VIA, however due to technical limitations, the VIA was simplified to a chamfered edge to simulate the same effect. It was discovered that repeating the deposition and sintering process multiple times created tracks with less cracks, as the later deposition stages would fill in cracks formed previously. As a side effect, it was observed that multiple sintering stages would begin to visibly affect areas where a silver track was deposited on heat sensitive parts of the substrate. These areas occasionally showed signs of melting after multiple sintering attempts. Some experiments were able to create a successful interconnect that joined the top and bottom layers of copper conductively, with resistances in the range of 3.2Ω to 4.31Ω . The non-conductive results showed cracks near areas where different material layers were joined, leading the hypothesis that the cracks were formed from differences in thermal expansion rates.
- 2) The double-sided copper substrates were also used in mounted incline experiments, where the substrates were not polished to a chamfered edge, but were placed upon an incline to simulate that of a slant. However, due to the use of a non-conductive inclined

mount, the substrates were unable to be heated sufficiently and none resulted in creating conductive interconnects.

- 3) Many different deposition patterns were used in the experiments concerning the flexible substrates with surface mounted resistors. Success varied in each deposition pattern, however it became evident that the most successful experiments were the ‘zigzag’ and ‘dot solder’ patterns. Both performed with a high success rate; however the ‘zigzag’ approach was discontinued due to poor results when the resistors were required to be hand-placed due to lack of supply. With the new mounted resistors, the ‘dot solder’ approach performed well, with two separate sets of experimental parameters that provided conductive results ranging from 2.5 Ω to 20 Ω . An effective variable was created to quantitatively compare the two different sets of parameters. A trend was discovered where an increase in the amount of deposited silver would increase the range of resistance values.
- 4) Overall, the laser assisted maskless microdeposition process proved to have great potential for creating non-planar interconnects on flexible substrates in a pressure-less environment. When using laser sintering, the material composition of the substrates must be considered, as different thermal expansion rates can lead to cracks along the deposited interconnect.

6.2 Recommendations

For further investigation on experiments involving creating 3d interconnects on flexible substrates, the following recommendations are proposed:

- 1) Thermal models should be created and analyzed for the double-sided copper substrates in order to determine the effect of different thermal expansion rates. With this information, experiments regarding double-sided substrates, a decision can be formed as to whether experiments with these substrates should be continued.
- 2) The effects of pores and voids in the silver track should be investigated further, since the values of resistances are much higher than expected. There is also not much research done on inspecting the effects on resistance from voids in nano-particles, which makes this an open topic for research.
- 3) Experiments involving mounting substrates on an incline should be repeated with a conductive mount, allowing the silver particles to adhere well to the surface of the substrate on contact.
- 4) The laser power and beam spot size should be adjusted in an attempt to find a set of laser parameters that allows sintering of silver on a heat sensitive substrate that does not result in damaging the substrate.
- 5) Repeatability experiments should be performed with the 'dot solder' pattern approach in order to achieve a good understanding of the performance for this pattern.
- 6) The measurement regarding the approximate volume of silver should be refined, as the equation for a cylinder was an approximation.

- 7) The relationship between the approximate volume of silver and the resistances should be further investigated, as the current amount of data is limited and cannot draw a confident conclusion.

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