Electrostatic Discharge Protection Devices for CMOS I/O Ports

by

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AUTHOR'S DECLARATION

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Qing Li

Abstract

In modern integrated circuits, electrostatic discharge (ESD) is a major problem that influences the reliability of operation, yield and cost of fabrication. ESD discharge events can generate static voltages beyond a few kilo volts. If these voltages are dissipated in the chip, high electric field and high current are generated and will destroy the gate oxide material or melt the metal interconnects. In order to protect the chip from these unexpected ESD events, special protection devices are designed and connect to each pin of the IC for this purpose. With the scaling of nano-metric processing technologies, the ESD design window has become more critical. That leaves little room for designers to maneuver. A good ESD protection device must have superior current sinking ability and also does not affect the normal operation of the IC.

The two main categories of ESD devices are snapback and non-snapback ones. Non-snapback designs usually consist of forward biased diode strings with properties, such as low heat and power, high current carrying ability. Snapback devices use MOSFET and silicon controlled rectifier (SCR). They exploit avalanche breakdown to conduct current.

In order to investigate the properties of various devices, they need to be modeled in device simulators. That process begins with realizing a technology specific NMOS and PMOS in the device simulators. The MOSFET process parameters are exported to build ESD structures. Then, by inserting ESD devices into different simulation test-benches, such as human-body model or charged-device model, their performance is evaluated through a series of figures of merit, which include peak current, voltage overshoot, capacitance, latch-up immunity and current dissipation time. A successful design can sink a large amount of current within an extremely short duration, while it should demonstrate a low voltage overshoot and capacitance. In this research work, an inter-weaving diode and SCR hybrid device demonstrated its effectiveness against tight ESD test standards is shown.

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Dedication

To my family and friends!

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Chapter 1 Introduction

1.1 Motivation

Electrostatic Discharge (ESD) is a commonly observed event that occurs in nature. ESD can occur in many situations, which scale from the outer space to sub-micron integrated circuits. One of the most common examples is a person walking through the living room on a piece of dry carpet and touching a metal door knob followed by a brief moment of shock, which is sometimes accompanied by a spark. The theory behind this phenomenon is that when two different materials, one being the shoes and the other one being the carpet, rub against each other, they cause charges to separate and accumulate on each material. The achieved electrostatic potential could be over a few thousand volts. As soon as the person touches the metal door knob, the charges that have been previously stored on his body will quickly dissipate through the conductor and give a shock to the person. Thus, it is defined that an ESD event happens when a charged insulator is brought close to a conductive object isolated from ground. The presence of the charged object creates an electrostatic field that causes charges on the surface of the other object to redistribute.

In the semiconductor industry, ESD is a subset of Electrical Overstress (EOS), which is a general failure that devices suffer from by excessive voltage, current or power. ESD is separated from EOS due to its special form of single-event and rapid transfer of electrostatic charge between two objects [1]. It is capable of damaging the integrated circuit immediately and permanently, or dealing latent damage that increases degradation rate [2].

In integrated circuits, the dielectric material is mainly silicon dioxide (SiO_2). ESD stresses can cause the thin MOSFET gate SiO_2 to breakdown. When a high voltage is applied across the gate oxide, which has high impedance, it can cause a weak spot within. Current can flow through that weak spot due to the loss of dielectric isolation. Therefore, localized heat is generated. It can induce a larger current flow. This cycle of increased current flow and localized heat can eventually cause a meltdown of the silicon or dielectric material. Thus, a short circuit is created at the spot, where it is supposed to be isolated by the silicon dioxide. When the scale of processing technology turns into deep sub-micron regime, ESD threatens the successful operation and yields from the fabrication processes, and subsequently increases device failure rate. It has been reported that the ESD and EOS have taken up to 70 percent of the failures in IC technology [3]. In order to bring down the ESD related failure rate, it is crucial for IC designers to understand the ESD phenomenon and provide every possible effort to tackle those failures.

Taking the person walking on the carpet example again, it can be seen that a few kilo volts static potential is easily generated in a normal daily situation. In assembly lines, where ICs are fabricated, the accumulated potential can reach tens of kilo-volts. These extremely high static voltages are capable of producing high current and electric fields on ICs. With high current flow, excessive heat can be generated and thus melt the substrate, or silicon dioxide insulator. It can even vaporize the metal interconnects in extreme circumstances. The high electric field can rupture the dielectric layers. In current semiconductor processing technologies, gate oxide has been reduced to tens of angstrom to achieve high switching speed. With the scaling of technology, thinner gate oxide thickness has made the chip more susceptible to ESD damages. Moreover, with increasing operating frequency, the I/O pad parasitic capacitance has a strong influence on the delay of the driving inverter. Thus, the parasitic capacitance should be minimized wherever possible. With those considerations and constraints, the ESD protection design becomes more difficult and increasingly important. This research work demonstrates ESD devices for I/O port protection on chips in 65 nano-meters technology.

1.2 ESD Design Window

A fundamental rule for any ESD design is that it cannot disrupt the normal operation of the chip. Thus, the triggering voltage, i.e. reaction voltage, of any ESD device should be above the safety operating range of the circuit [2]. This is illustrated in **Figure 1-1** below [4]:

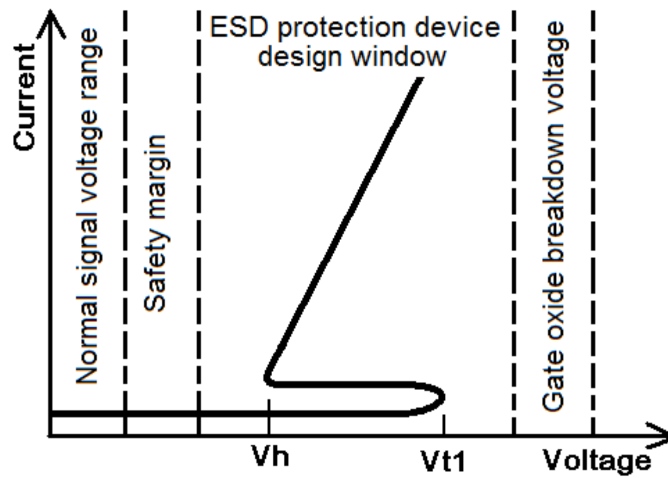


Figure 1-1: I-V curve of a typical snapback device and ESD design window

Figure 1-1 demonstrates a typical I-V characteristic curve of a snapback ESD protection device under stress. The figure can be obtained through device simulators and hardware measurement equipment called Transmission Line Pulse Analyzer (TLP). In simulators, when ESD stresses are applied to the anode of a protection device, the voltage at the anode rises up to the V_{t1} in Figure 1-1. Then, due to the internal structure of the snapback devices, which are elaborated in later chapters, the devices start to conduct current at V_{t1}. Afterwards, the voltage at the anode drops while the conduction current keeps increasing. This process is a negative resistance phenomenon. Only specific device simulators are able to trace its I-V curve. These curves possess the characteristics of multi-valued I-V curve with abrupt changes. TCAD Sentaurus® uses a continuation method that is based on a dynamic load-line technique adapting the boundary conditions along the traced I-V curve to ensure convergence [5].

The following paragraph is an excerpt from the Sentaurus manual [6]:

"An external load resistor is attached to the device's anode and the device is being indirectly biased through the load resistance. The boundary condition consists of an external voltage applied to the other end of the load resistor not attached to the device. By monitoring the slope of the I-V curve, an optimal boundary condition (external voltage) is determined by adjusting the load line so it is orthogonal to the local tangent of the I-V curve. The boundary conditions are generated automatically by the algorithm without prior knowledge of the I-V curve characteristics. Continuation method calculates the slope at each point. The simulation advances to the next operation point if the solution has converged. Before moving to the next step, the load line is recalibrated so that it is orthogonal to the local tangent of the I-V curve. A user-defined window specifies the limits for curve tracing."

Using this method, Sentaurus can plot the snap-back behavioral curve that is not a function any more. A TLP analyzer is hardware measuring equipment that is commonly used for ESD purposes on actual chips. A TLP analyzer is based on a technique that first charges a long and isolated cable to a preset voltage, and discharges it to a protection device. The cable discharge event simulates an ESD event. By employing time-domain reflectometry, the change in the device impedance can be then monitored as a function of time.

The design window is limited to be between the Safety Margin and the Gate oxide breakdown voltage. The ESD protection device should only trigger at V_{t1}, which is higher than the normal signal plus safety margin but below the gate oxide breakdown voltage. Then, after the ESD event has occurred, it is expected to drop to a holding voltage that is higher than the safety margin voltage. This is because no false triggering should occur during the normal operation of the chip where it is possible to reach the upper boundary of the safety range. With newer processing technologies, the gate oxide is becoming ever thinner; the range of possible voltage boundaries has become narrower. Thus, the ESD design room has been squeezed. This leaves designers very limited maneuverability to come up with new designs.

1.3 ESD Zapping Mode

A packaged IC has many pins around it. The pins are generally categorized into three types, V_{DD}, V_{SS} and I/O. When ESD events happen associated with I/O port, which is the focus of this research work, there are possibly four zapping modes [7], PS, NS, PD and ND as shown in **Figure 1-2**. The zapping modes indicate the polarity of I/O ESD events with respect to power supply (V_{DD}) and ground (V_{SS}).

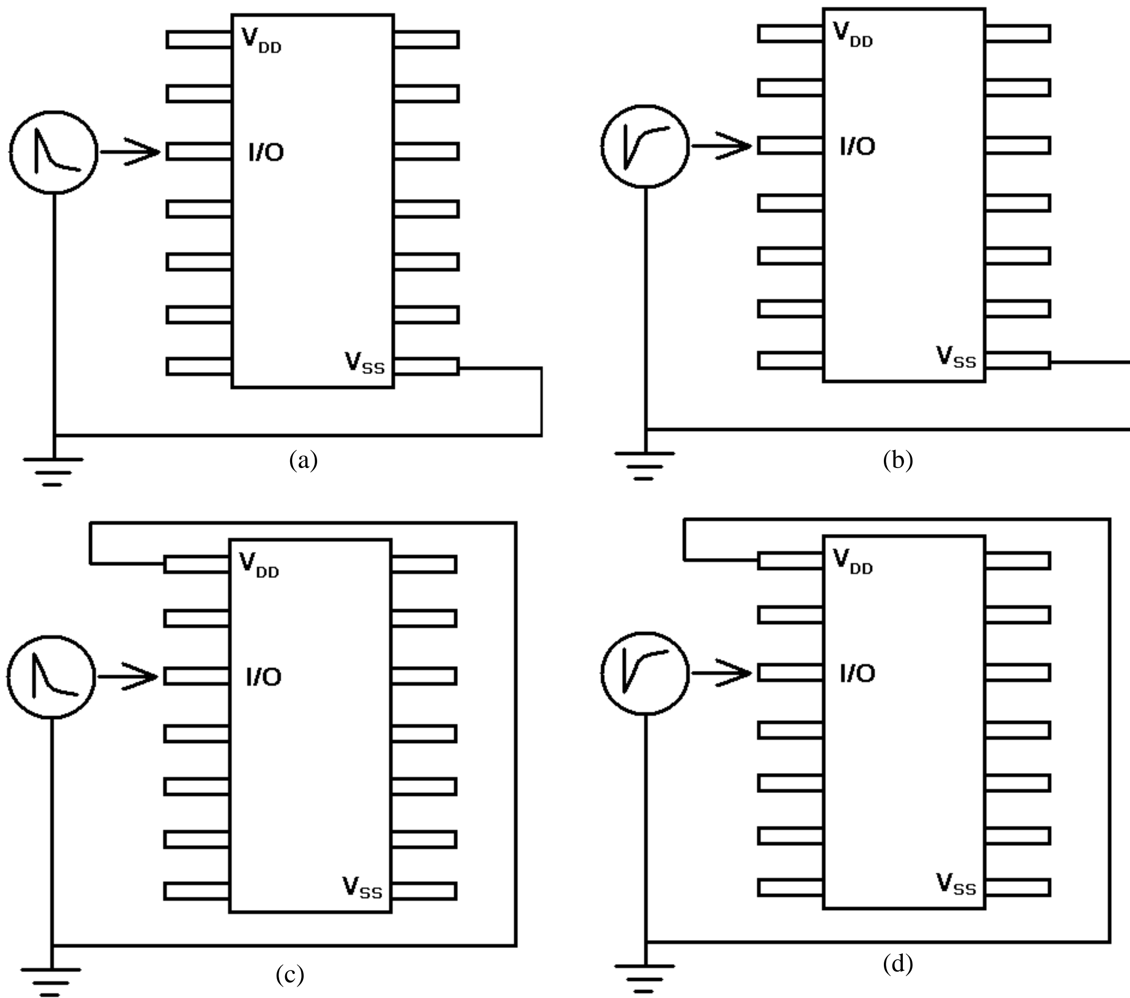


Figure 1-2: Four possible ESD zapping mode associated with I/O ports (a) Positive ESD voltage with respect to V_{SS} (PS) (b) Negative ESD voltage with respect to V_{SS} (NS) (c) Positive ESD voltage with respect to V_{DD} (PD) (d) Negative ESD voltage with respect to V_{DD} (ND)

The PS mode, shown in **Figure 1-2** (a), happens when a positive ESD voltage is supplied at the I/O port with respect to V_{SS} pin. Oppositely, NS mode, shown in (b), depicts the case when a negative ESD voltage is applied to the I/O pin with respect to V_{SS} pin. For the other two modes, the only difference is that the discharge path is through V_{DD} rail. In reality, there should be two more discharging modes, which are directly between V_{DD} and V_{SS} rails. The ESD events happening between those two rails are usually taken care of by power clamps [2], which are not the focus of this research work.

1.4 ESD Event Modeling

ESD devices go through a series of tests to classify their performance on different discharge situations. According to JEDEC® [8], several important test situations are to be considered for ESD purposes. They include Human-Body Model (HBM), Machine-Model (MM), and Charged-Device Model (CDM). These tests simulate real-world ESD events. In order to qualify ESD protection devices, they need to pass those tests and obtain an assigned classification.

1.4.1 Human Body Model (HBM)

Under many circumstances, a human body becomes charged to a high potential. **Figure 1-3** is a simplified representation of this situation. First, the human body, which is represented by the 100 pF capacitor, is charged to a high voltage. Then, the switch connects the capacitor through the 1500 ohm resistor that represents the resistance of the human body. The charges stored on the capacitor will be dissipated through the Device under Test (DUT), which is the ESD protection device [9].

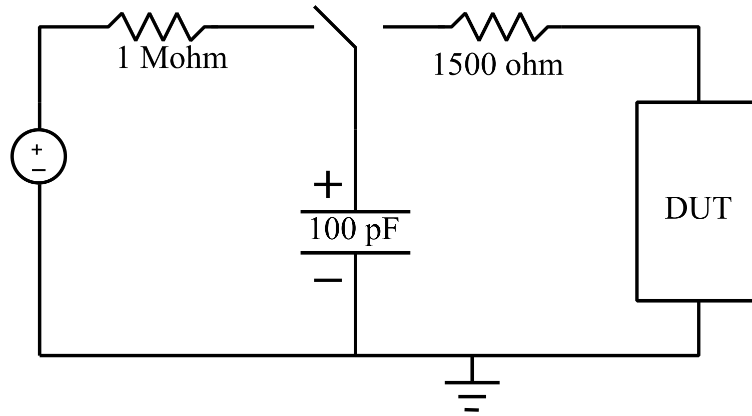


Figure 1-3: ESD event HBM modeling circuit specified by JEDEC standard, the switch controls the charging and discharging of the source capacitor

Due to the large series resistance of 1500 ohms of the human body, the peak current reaches 1.2~1.48 A under a 2 kV HBM stress, while the rise time of the current is 2~10 nano-seconds and the decay time is less than 200 nano-seconds [9], as shown in **Figure 1-4** below.

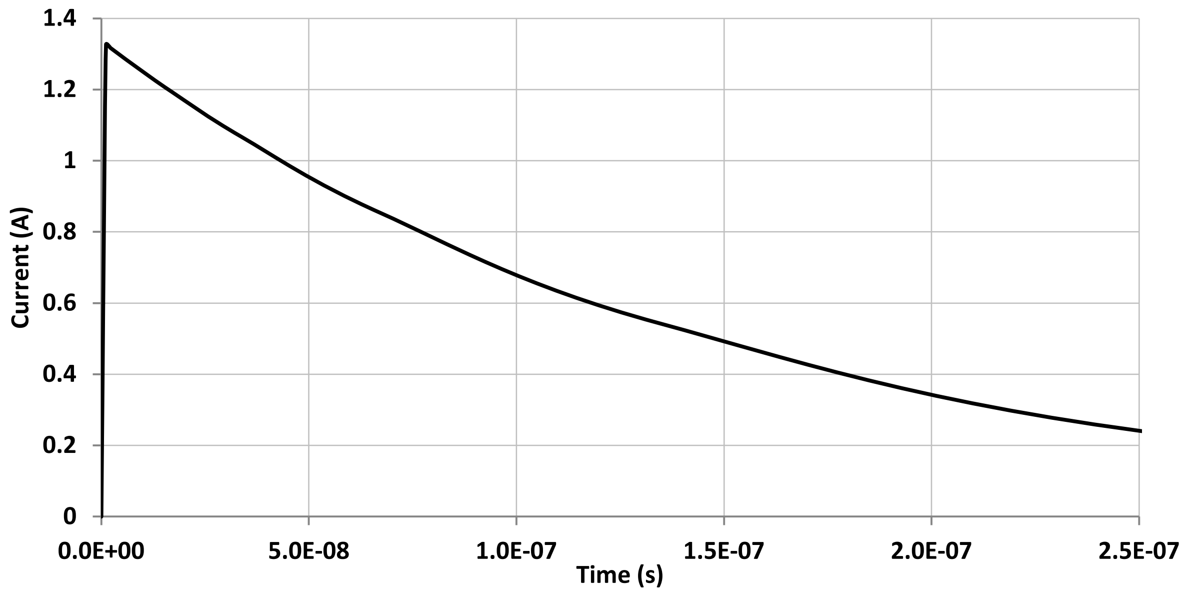


Figure 1-4: A typical current vs. time response of an ESD protection device under 2 kV HBM stress

However, in practice, the human body has different characteristics than the simple model, and these factors include temperature, humidity, and body mass or more. Therefore, the actual human

body discharge can differ significantly from what the tester is seeing from the results. In order to classify ESD components' capability of handling HBM stresses, **Table 1-1** categorizes them into voltage ranges.

Table 1-1: HBM voltage classification

Class	Voltage Range (V)
Class 0	<250
Class 1A	250 ~ 500
Class 1B	500 ~ 1000
Class 1C	1000 ~ 2000
Class 2	2000 ~ 4000

1.4.2 Machine Model (MM)

The Machine model is similar to HBM, and the differences are to replace the 1500 ohm resistor with a 750 nH inductor and the capacitor value is increased to 200 pF as shown in **Figure 1-5** [10]. MM serves the purpose to represent the damage caused by equipment used in the manufacturing process.

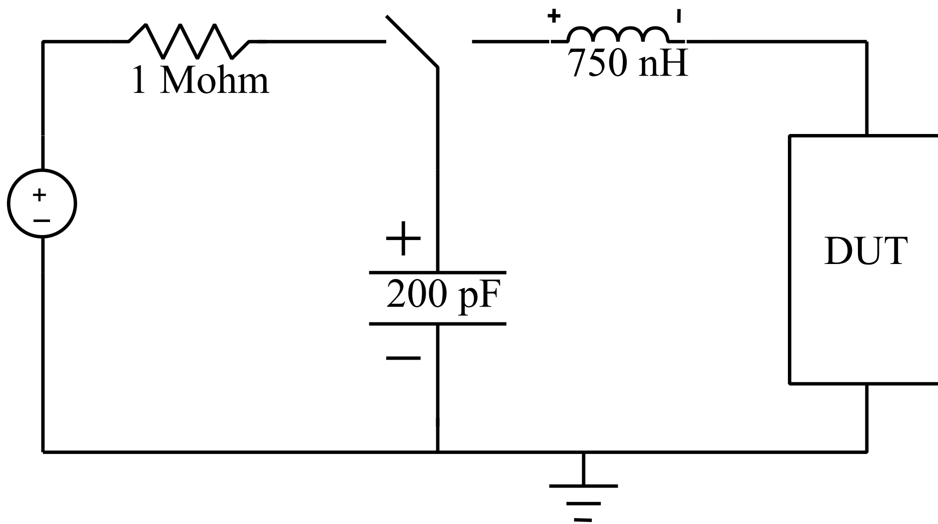


Figure 1-5: ESD event MM modeling circuit specified by JEDEC standard, the switch controls the charging and discharging of the source capacitor

MM testing is also classified regarding protection voltage level as depicted in **Table 1-2** below:

Table 1-2: MM voltage classification

Class	Voltage Range (V)
Class M1	<100
Class M2	100 ~ 200
Class M3	200 ~ 400
Class M4	>400

1.4.3 Charged Device Model

The Charged Device Model (CDM) is a new testing model and it has the highest ESD stress among the three types and it is the most difficult one to reproduce [2]. This model attempts to simulate the event that is related to the packaging on the assembly line. During packaging, the chip can be charged by a number of methods. Then, when the robotic arm, which is considered as a large grounded current sink, is reaching close to the package, the charges on the chip will spark and dissipate to ground through the metal on the robot. This event happens much faster compared to the HBM. The entire discharge usually finishes within 10 nano-seconds in comparison with the HBM's hundreds of nano-seconds time. Thus, the peak current is also higher than the HBM. With advanced fabrication technologies nowadays, HBM and MM ESD events are showing a trend of decreasing prevalence [11]. Thus, CDM events are likely to dominate the causes of ESD related failures. According to JEDEC standard [12], the CDM discharge is modeled as shown in **Figure 1-6**:

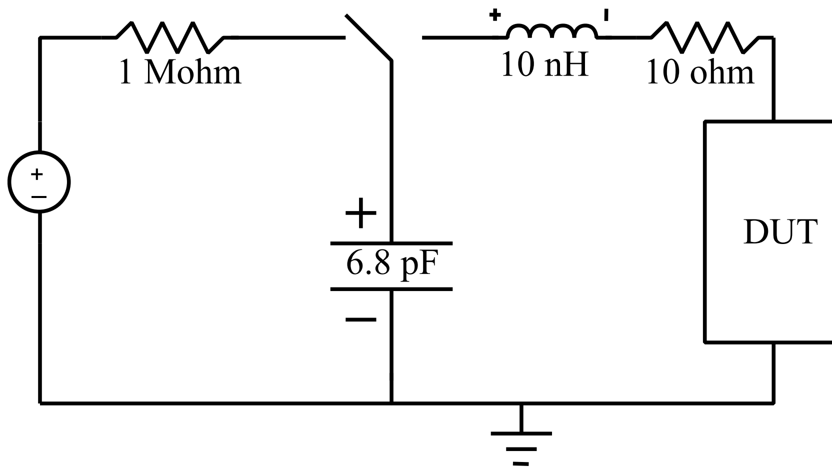


Figure 1-6: ESD event CDM modeling circuit specified by JEDEC standard, the switch controls the charging and discharging of the source capacitor

The 6.8 pF capacitor represents a small packaging capacitance; the 10 nH and 10 ohm depict the discharging path from the chip to ground. This path includes the inductance and resistance from the bonding wires and the spark. According to JEDEC Roadmap [2] [13], modern assembly lines are shifting towards low voltage equipment, thus making the protection level requirement lower. In this research work, the peak voltage of 100V is chosen to test all devices for comparison purposes. **Figure 1-7** depicts a typical CDM current response under 100V situation.

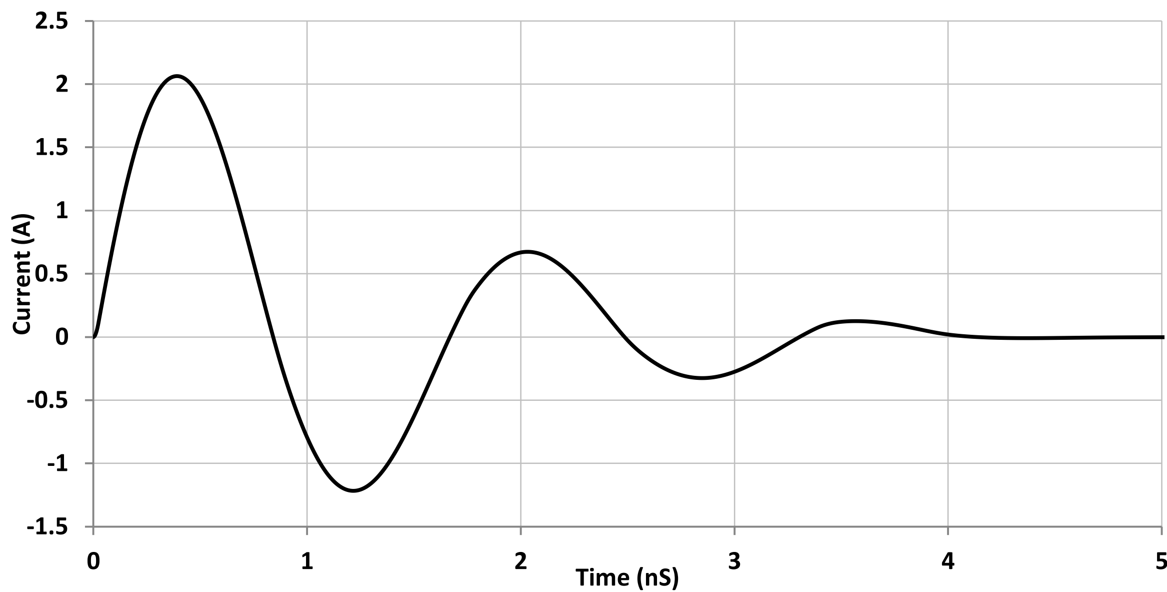


Figure 1-7: A typical CDM current vs. time response of an ESD protection device under 100V CDM stress

As specified by JEDEC standard, the rise time of the first peak current is below 400 nano-seconds. The first undershoot is roughly half of the peak current, and the second overshoot is approximately one quarter of the peak current.

The CDM qualification is also classified as in **Table 1-1** below.

Table 1-3: CDM voltage classification

Class	Voltage Range (V)
Class I	100
Class II	100 ~ 200
Class III	200 ~ 500
Class IV	500 ~ 1000

1.5 ESD Event Correlations

Among the various ESD testing methods, there are correlations between different models. First, HBM and MM model exhibit a correlation [14] because most HBM and MM failures are related to thermal damage. Pierce [15] shows that by equating the energy deposited in the IC during the stress and assuming that all ESD energy is used to create damage, it leads to an MM:HBM voltage ratio of 1:25. After analyzing failure rate data, JEDEC shows an average MM:HBM voltage ratio of 1:20 [16]. Therefore, A HBM of 2 kV is comparable to a MM of 100V. However, CDM does not show any correlation with the other two methods due to its completely different discharge method in nature. Therefore, HBM and CDM are the two most common methods to qualify ESD protection devices. In this research work, a HBM of 2 kV and CDM of 100V are used as the target protection level of components.

For the actual hardware testing of ESD failures, the designated equipment Transmission Line Pulsing Analyzer (TLP) is used [14]. TLP applies square voltage pulses with different pulse widths to the device under test. There is a correspondence between a 2 kV HBM and a 100 nano-seconds TLP

pulses [17]. It is now used as the de facto standard for HBM testing [14]. **Figure 1-8** below depicts the maximum voltage that ICs with different processes can sustain when under the test of 100 nano-seconds TLP pulses [18]. This reference serves as the guideline for the ESD device design in this research work. As seen in the figure, when gate oxide thickness is below 2.2 nano-meters, which is the size used in 65 nano-meter process technologies, the maximum voltage the MOSFET's gate can undertake is **below 5V**. Thus, this condition is the most crucial governing guideline for qualifying different devices to protect gate oxide damages under 2 kV HBM situation in this research work.

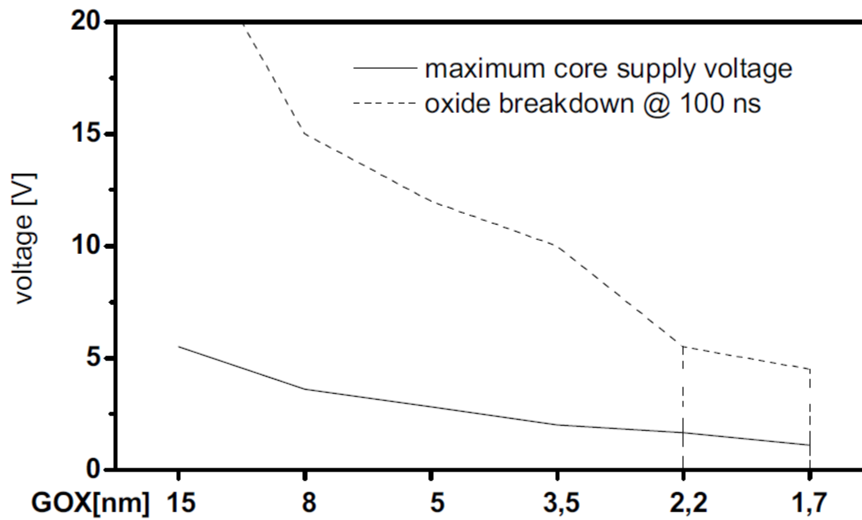


Figure 1-8: Maximum TLP voltage vs. gate oxide thickness

1.6 ESD Device Design Flow

With JEDEC standards serving as the design guidelines, the procedure of developing ESD protection devices for specific technologies are introduced. Due to very limited access to important process specific parameters, the design procedure is a trial and error iterative method [19]. Only a few numbers, such as gate oxide thickness and I_{DS} vs. V_{DS} curve can be extracted directly from the technology documents. By applying another useful tool, PTM-BSIM4 [20] MOSFET models developed by Arizona State University, more useful parameters can be supplied. However, they only serve as the purpose of rough estimation. The exact numbers still need to be determined through TCAD device simulators. Then, using those values, ESD structures can be constructed and put to test

regarding their capabilities. The following flowchart (**Figure 1-9**) is the design procedure of this research work.

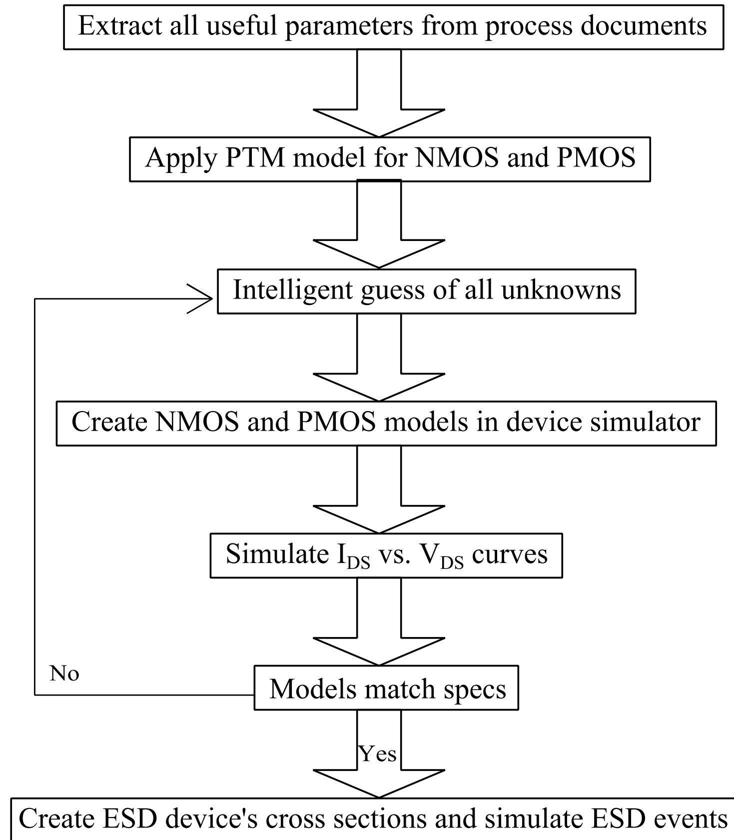


Figure 1-9: ESD protection devices construction and ESD event simulation methodology

1.7 Chapter Summary and Thesis Outline

In this chapter, the concept of electrostatic discharge is introduced, as well as the modern challenges, four zapping modes and three types of ESD event modeling. Then, the device design flow is introduced.

The remainder of this thesis is divided into the following chapters: Chapter 2 describes the different ESD protection devices and their theoretical working principles, Chapter 3 elaborates the NMOS and PMOS matching process which leads to the subsequent construction of different ESD

devices in TCAD simulator, Chapter 4 details the simulation test bench setup for various ESD situations and compares a set of figures of merit, finally, in Chapter 5 conclusions presented.

Chapter 2 ESD Devices and Theoretical Comparison

For on-chip ESD protection purposes, there are a large number of devices and circuits available in the industry already. These device components are categorized into two types, snapback and non-snapback. All ESD damages happen when a large potential difference is applied to high impedance are and thus generate excessive heat [2]. The combination of high current and temperature is the principal cause of most chip ESD failures. In this chapter, a discussion and comparison will be presented for various ESD protection devices. Section 2.1 will focus on diode devices. Section 2.2.1 will present the MOSFET based protection devices. Section 2.2.2 to 2.2.3 will introduce silicon-controlled rectifier devices. Section 2.3 will be a comparison of all the above devices.

2.1 Diode ESD Protection Device

Diode is the simplest ESD protection device. The major electrical property of a diode comes from its two oppositely doped regions, as seen in **Figure 2-1**. The p-type side has higher net concentration of holes and the n-type side has higher net concentration of electrons. The junction between the oppositely doped regions can be forward or reverse biased depending on the polarity of the applied voltage. Forward and reversed biased diodes have different characteristics which can be exploited for ESD events. In this section, both configurations are compared to identify their strengths and weaknesses.

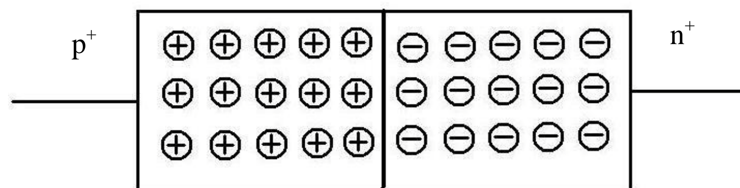
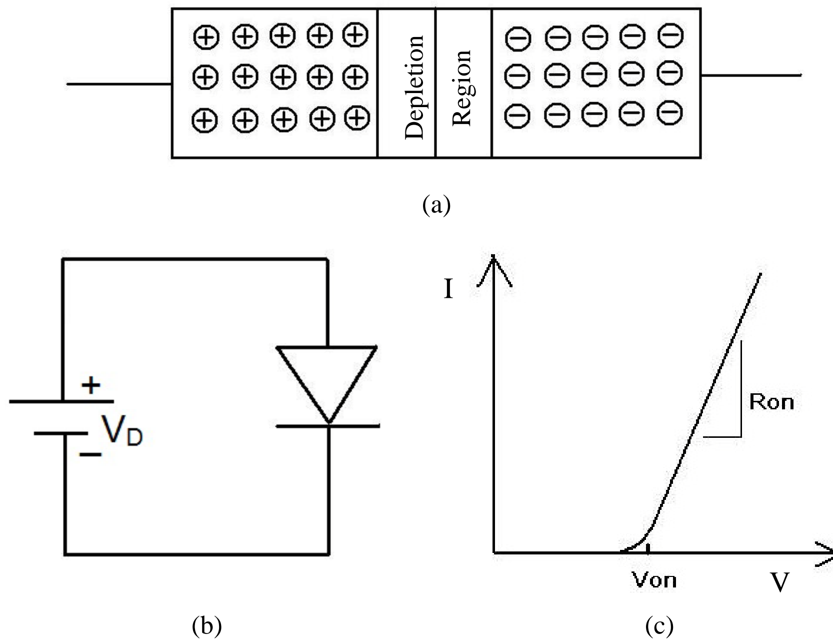


Figure 2-1: Basic diode structure with p-type and n-type materials on each side of the junction

2.1.1 Forward-Biased Diode

At the p-n junction of a diode, due to the diffusion of minority carriers to both sides, a depletion region is formed shown in **Figure 2-2**a. That leaves unfilled holes on the n-side and unfilled electrons on the p-side. These unbalanced charges induce an electric field across the depletion region and thus cause a built-in potential in the range of 0.5~0.7V depending on the doping levels on both sides. When the p-type side of the diode is connected with a higher potential than the n-type side, it is considered as forward-biased as shown in **Figure 2-2**b. Under this forward condition, diodes are able to conduct a large amount of current with a very low on-resistance as depicted in the I-V curve in **Figure 2-2**c. Equations 2-1 to 2-3 demonstrate the behavior of a diode in the forward region.



(b) (c)

Figure 2-2: Diode properties (a) depletion region formation between oppositely doped regions (b) forward bias diode circuit (c) I-V curve of a forward biased diode

$$\mathbf{I_D = I_S\left(e^{V_D/V_t} - 1\right)} \qquad \mathbf{V_t = 26mV} \; \boldsymbol{at\ room\ Temperature} \qquad \textbf{[21]} \qquad \text{Equation 2-1}$$

$$\mathbf{V_{ON} = V_t ln\frac{N_D N_A}{n_i^2}} \qquad \textbf{[21]} \qquad \text{Equation 2-2}$$

$$\mathbf{R_{ON}} = \left(\mathbf{dI_D}/\mathbf{dV_D}\right)^{-1} = \frac{\mathbf{V_t}}{\mathbf{I_S}}\mathbf{e}^{-\mathbf{V_D}/\mathbf{V_t}} \quad \textbf{[21]} \qquad \text{Equation 2-3}$$

It is seen that the on-voltage and on-resistance are functions of doping concentration and junction area, thus making them process dependent. Due to the advantages of high current conducting ability, low internal junction temperature and low power consumption [2] forward biased diodes are very effective for the ESD protection purpose, where those characteristics are crucial.

With the specific process technology of this research work, the voltage difference between V_{DD} and V_{SS} is 1.0V, the same as between the I/O port and V_{SS}. One forward biased diode, which possesses the ~0.6V built-in voltage barrier, is not capable of functioning within the IC's normal operation range without disrupting the circuit. This is an undesired quality of ESD protection devices. When one diode is placed forwardly between I/O port and V_{SS}, once the I/O is at the logic high state (1.0V), the diode will conduct and draw a large amount of current roughly 20~50 mA/um [22]. As shown in **Figure 2-3**, when the diode is conducting, its low on-resistance will be much smaller compared to the input resistance of the I/O driver inverter.

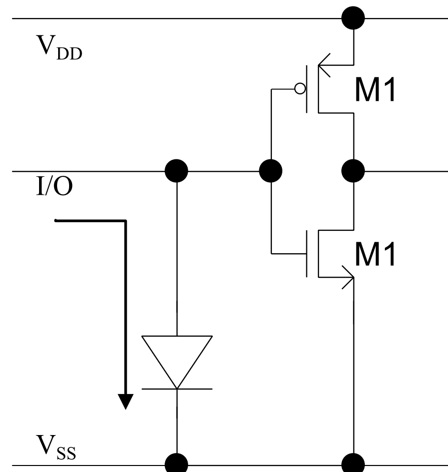


Figure 2-3: One forward biased diode connected between I/O driver inverter and V_{SS}

Thus, the gate of the NMOS transistor cannot be charged to 1.0V, but to the diode's clamping voltage ~0.6V. This weak V_{GS} cannot turn on the NMOS completely and cause the output of the inverter to discharge slowly. As a result of this circumstance, the signal's integrity is compromised due to the low turn-on voltage of a single forward-biased diode. To overcome this problem, stacks of diodes [23] are realized. When two p-n junction diodes are connected in series with the same polarity,

their combined turn-on voltage will be twice as much, thus reaching ~1.2V. This voltage is higher than the normal signal range of the I/O port or V_{DD} of this technology process, but not sufficient to overcome the noise margin, which can reach up to 50% of the maximum signal voltage. The trade-off emerges between the forward biased diode ESD performance and normal operation disruption.

2.1.2 Reverse-Biased Diode

Reverse-biased diodes utilize avalanche breakdown to conduct current [24]. Avalanche breakdown is a phenomenon that occurs in insulating and semiconducting materials. In semiconductor circuits, there are two types of carriers, free electrons and holes. When a large reverse-biased voltage is applied across a diode's p-n junction, a fixed electron may break itself free due to its thermal energy, thus, creating a free electron-hole pair. Then, assisted by the high electric field induced by the large potential difference, the electron can move toward the electrode with higher potential and the hole will move toward the end with lower potential. Under high voltage situations, a free electron can travel very fast and break the bonding of other electron-hole pairs, thus, creating more free electrons and holes. When there are enough free electrons and holes travelling towards the opposite directions in the diode, it becomes a conductor [25]. Normal diodes are likely to be destroyed under avalanche conditions. However, there are specially designed avalanche diodes for this purpose that can survive the high temperature and current.

The reverse voltage when avalanche breakdown happens is called the breakdown voltage [26]. It is governed by the following equation.

$$\boldsymbol{Breakdown\ Voltage} = \frac{\varepsilon(N_A+N_D)}{2qN_AN_D}E_{crit}^2 \qquad \text{Equation 2-4}$$

Typically, the breakdown happens at above 10V [2] and it is process dependent, and the on-resistance is larger than forward-biased diodes. Due to these characteristics, reverse-biased diode will reach high temperature during ESD discharges. Thus, this makes it inferior than a forward-biased diode for ESD protection purposes because high temperature is capable of melting components on a chip. However, a reverse-biased diode carries very low leakage current under normal signal operating range due to its high on-voltage. It also demonstrates less capacitance compared to a forward biased diode due to the reverse biasing.

2.1.3 Diode Types in Concurrent CMOS Technology

In standard single well CMOS process, the substrate is a lightly doped p-type silicon material. Three types of diodes that can be realized, such as n^+-diode, p^+-diode, and n-well diode demonstrated in **Figure 2-4**.

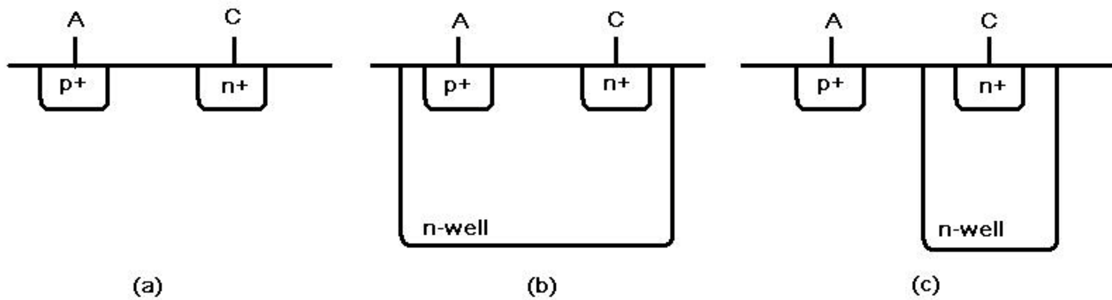


Figure 2-4: Three diode types in single-well CMOS processes (a) n^+-diode (b) p^+-diode (c) n-well-diode

Each of the three types of diodes has its designated location on an IC. The n^+-diode uses the junction between p-substrate and n^+. Because the substrate has to be connected to V_{SS}, this diode is used between the I/O pad and ground and it is capable of handling the NS ESD discharge mode. The p^+-diode's junction is formed between p^+ and n-well. Since n-well needs to be connected to V_{DD}, this diode is used between V_{DD} and I/O pad and it is used to discharge ND ESD stresses. Lastly, n-well diode has its junction between p-substrate and n-well and this type of diode is used between V_{DD} and V_{SS} as a power clamp.

2.2 Snapback Devices

In this section, snapback devices are introduced. In theory, snapback devices are similar to reverse biased diodes because they are both required to reach avalanche breakdown voltage to conduct current. After breakdown has occurred, the anode potential drops to holding voltage due to the internal positive feedback loop inherited in the structures to sustain the current flow. Two major types of devices, ground gate NMOS (GGNMOS) and Silicon Controlled Rectifier (SCR) are analyzed in this section.

2.2.1 Ground Gate NMOS

The most simple snapback protection structure is a ground-gate NMOS in which the gate and source are connected together to ground. Shown in **Figure 2-5**, GGNMOS depicts the formation of a parasitic *npn*-bipolar junction transistor consisted of the drain (n^+), p-substrate (p^-) and source (n^+) terminals.

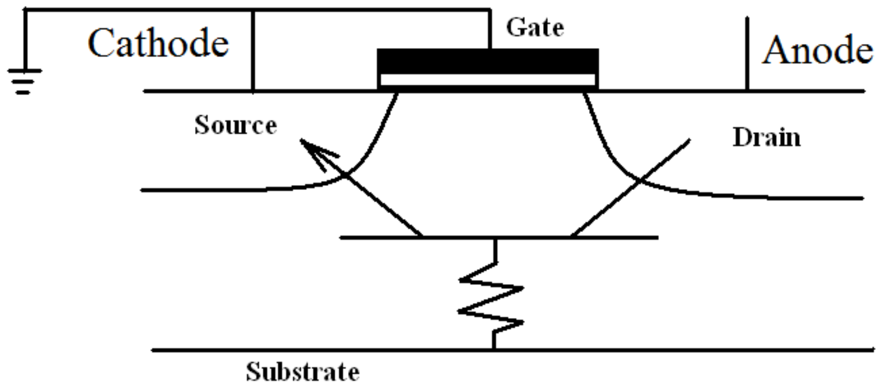


Figure 2-5: Ground gate NMOS cross-sectional view with parasitic *npn* transistor

The drain contact is connected to the I/O pad. When the pad voltage increases, the drain to p-substrate junction becomes reverse biased. Once the voltage reaches the avalanche breakdown condition, the generated free moving holes will be swept to the substrate contact by the applied high electric field. Since the positive charges accumulate at the p-substrate contact, the base voltage of the parasitic BJT increases. When the voltage reaches the diode's turn-on value at 0.7V, which is the V_{BE} of the *npn* transistor, the p-substrate and source junction diode starts to conduct, thus making the BJT in active mode. The anode voltage at the time is the first breakdown voltage V_{t1}. Once the BJT is on, there is no need to maintain a high voltage at the anode to facilitate the flow of drain to source current. Subsequently, the drain voltage is dropped to the holding voltage V_h. This process is the behavior of snapback. When the drain voltage keeps going higher, the device will ultimately suffer from thermal damage and snaps back again as shown in **Figure 2-6**. At this point, the device reaches second breakdown voltage (V_{t2}) and current (I_{t2}) and it will be destroyed thermally [2].

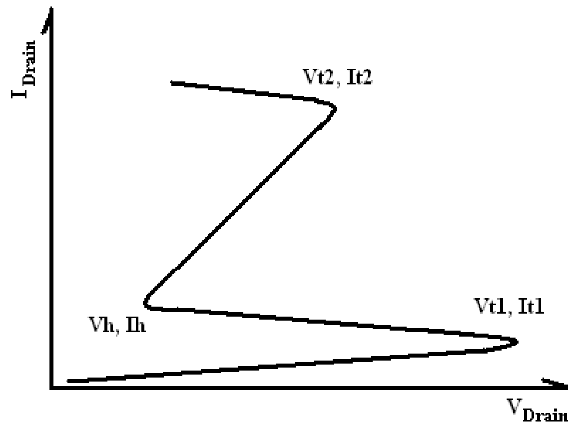
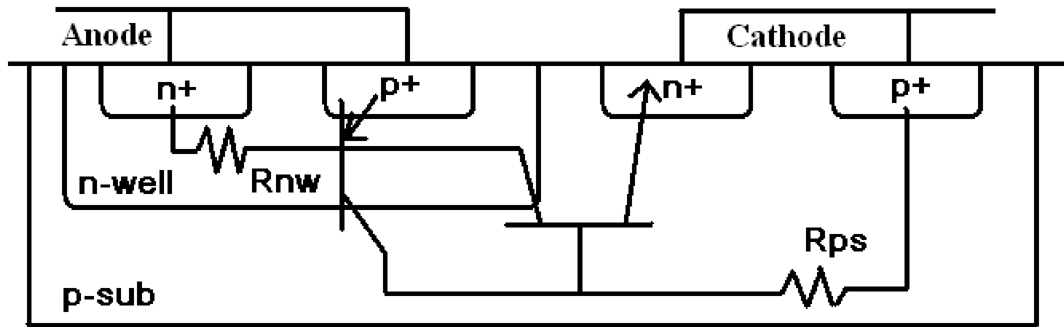


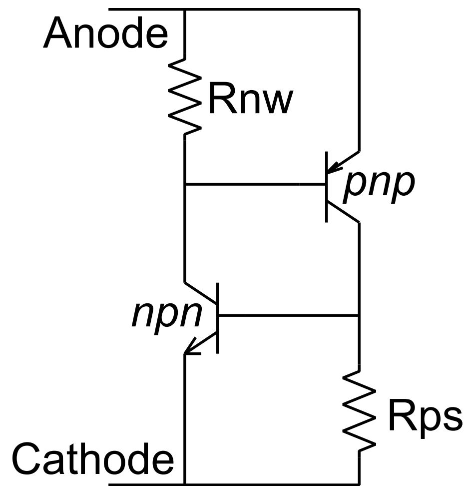
Figure 2-6: GGNMOS I-V curve

2.2.2 Silicon Controlled Rectifier

Silicon Controlled Rectifier (SCR) is another type of snapback ESD protection device as shown in **Figure 2-7**a. It consists of a combination of p-type and n-type diffusions. A normal SCR has four highly doped active diffusions, two p^+ and two n^+, along with a lightly doped n-well region. The n^+ and p^+ diffusions that reside in the n-well form the anode. The other n^+ and p^+ in the substrate form the cathode. The anode is connected to I/O pad and the cathode is connected to ground. This depicts the physical structure of an SCR device.



(a)



(b)

Figure 2-7: Silicon-Controlled Rectifier (SCR) structure realized in CMOS technology (a) cross-sectional view (b) schematic view

The operation principle of an SCR is qualitatively analyzed. The simplified schematic of an SCR is shown in **Figure 2-7**b. When the anode voltage rises, the n-well to p-substrate junction becomes reversely biased. When it reaches avalanche breakdown, the generated current in the p-substrate can turn on either one of the two parasitic bipolar transistors. Because the *npn* transistor has a higher gain than the *pnp* transistor, that makes it easier to turn on. When the *npn* transistor turns on, its collector current, which flows through the n-well, can generate a voltage drop across the n-well resistance R_{nw}. As a result of this voltage difference, the p^+ contact of the anode can have a higher voltage than its immediate surrounding n-well region and making this p-n junction forward biased. When the forward voltage is higher than 0.7V, the *pnp* transistor will turn on. In turn, the collector current of the *pnp* transistor flows across the p-substrate region and creates a voltage drop due to the substrate resistance Rps. This potential difference is the base-emitter junction voltage of the *npn* transistor, it helps to keep this transistor conducting current. The operation of the two parasitic

transistors forms a positive feedback loop to help increase the gain of each other. When the current flow path is formed between the anode and cathode, it becomes unnecessary for the anode to keep a high reverse biased voltage to facilitate the avalanche breakdown of the *npn* transistor. The anode voltage will lower to V_h. This process is the snapback behavior of an SCR device.

In comparison with the GGNMOS's junction formed between n^+ diffusion and p-substrate, SCR uses the n-well to p-substrate region for its avalanche breakdown. From Equation 2-6 and 2-7, SCR demonstrates a higher voltage required to trigger avalanche breakdown [27].

$$\boldsymbol{Breakdown\,Voltage = \frac{\varepsilon(N_A+N_D)}{2qN_AN_D}E_{crit}^2} \quad \text{Equation 2-5}$$

When applying experimental values, such that p-substrate doping is 6×10^{16} /cm^3, n-well doping is 4×10^{17} /cm^3, and n^+ diffusion is 2×10^{20} /cm^3, calculated values are shown below:

$$\boldsymbol{GGNMOS\,Breakdown\,Voltage = \frac{\varepsilon E_{crit(NMOS)}^2}{2q} \times 1.667 \times 10^{-17}} \quad \text{Equation 2-6}$$

$$\boldsymbol{SCR\,Breakdown\,Voltage = \frac{\varepsilon E_{crit(SCR)}^2}{2q} \times 1.916 \times 10^{-17}} \quad \text{Equation 2-7}$$

From the two equations above, it is shown that SCR requires more than 20 percent applied voltage to trigger its avalanche breakdown when compared to the GGNMOS. In circuits, this breakdown voltage can reach up to 20V [2].

SCR's internal positive feedback loop induces a negative quality that can disrupt the normal operation of the pad signals, which is its low holding voltage. In the holding point of the I-V curve seen in **Figure 2-8**, both *npn* and *pnp* transistors are in saturation region [2].

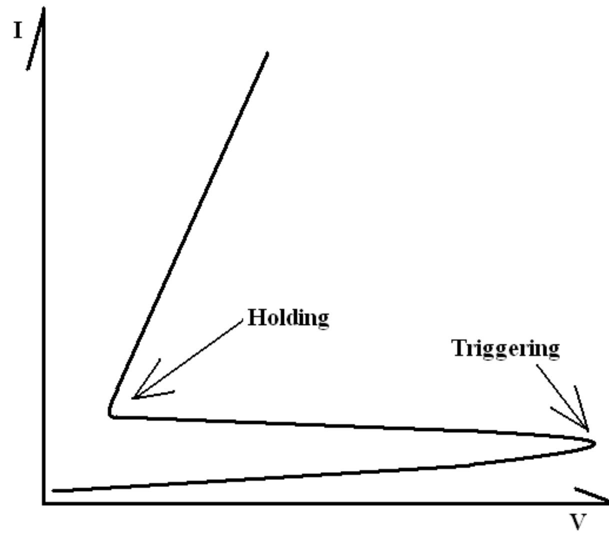


Figure 2-8: SCR triggering voltage point and holding voltage point on an I-V curve

The holding voltage at the anode is the sum of $V_{BE\,(npn)}$ and $V_{EC\,(pnp)}$ as shown in Equation 2-8. The two voltages are 0.7V and 0.3V in saturation region respectively. Then, the anode voltage is 1.0V. This low holding voltage makes the SCR device susceptible to latch-up [28] because the I/O high state and V_{DD} are both 1.0V in 65 nano-meters technology. When noise voltages exceed the holding voltage of the SCR, they can cause the SCR to trigger and start to sink current. Thus, an undesired disruption occurs because of the SCR's low holding voltage property.

$$\boldsymbol{V_h = V_{BE(npn)} + V_{EC(pnp)}} \qquad \text{Equation 2-8}$$

2.2.3 Darlington Based Silicon Controlled Rectifier (DSCR)

In section 2.2.2, it has shown that SCR requires a first trigger voltage far too high to be considered as a valid ESD protection device for modern integrated circuits which only operate under a few volts. According to the analysis in section 2.2.2, SCR triggers at the avalanche breakdown voltage between n-well and p-substrate junction. When the gain of the *npn* transistor is increased, such that more current flows to the n^+ diffusion at the cathode, the triggering voltage (V_{t1}) can be lowered. This method was proposed by Dr. H. Sarbishaei and Prof. M. Sachdev [29]. In order to increase the current, a Darlington pair BJT is realized by adding an extra n-well with a p^+ active diffusion inside [29], as shown in **Figure 2-9**a.

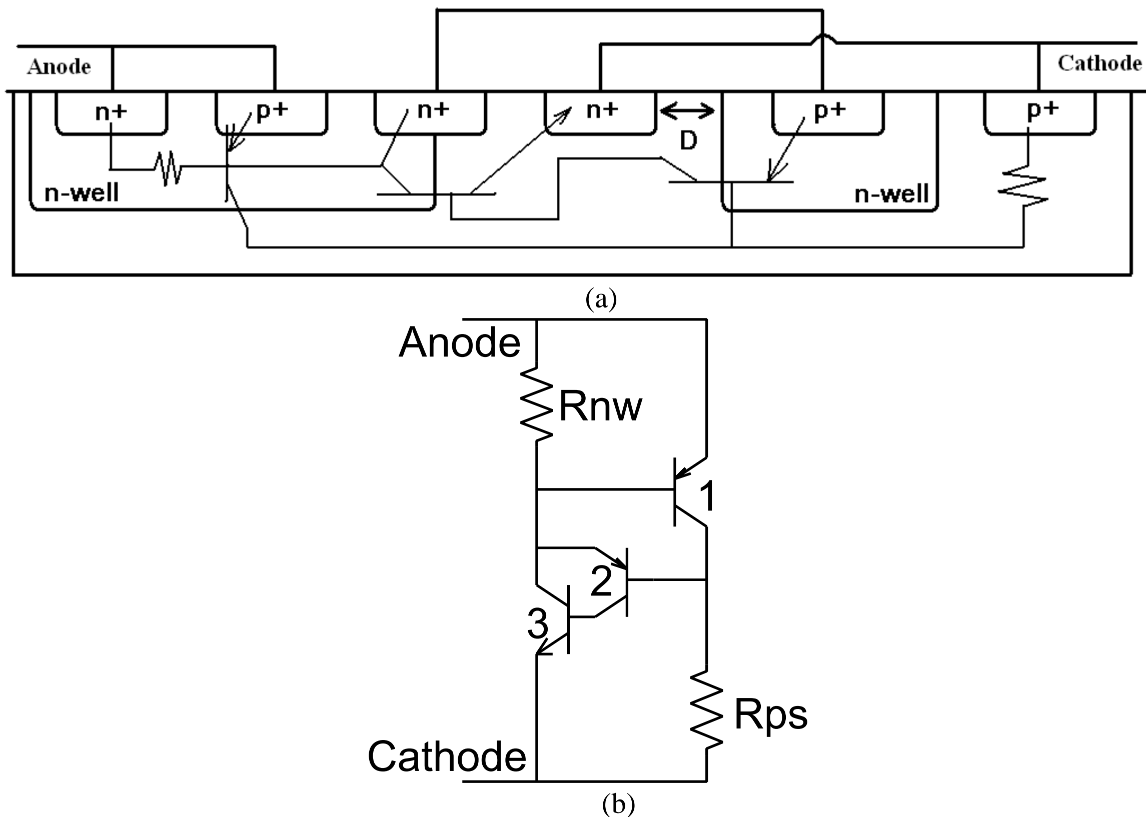


Figure 2-9: DSCR structure realized in CMOS technology (a) cross-sectional view (b) schematic view

The operation principle of the DSCR has changed from the original SCR. As seen in **Figure 2-9**a, in the anode's n-well, an extra n^+ diffusion is implanted to split the some of the n-well current to the emitter of the added *pnp* transistor (2). When the *npn* transistor (1) is on, the remaining n-well current will flow to the p-substrate and to the n^+ diffusion (cathode) on the left side of "D". The extra gain supplied by the *pnp* (1) is from its collector, which injects the current into the same n^+ diffusion.

As a result of the extra n-well, the gain of the additional *pnp* transistor is a function of distance "D" between the n-well and the n^+ diffusion region. In the "D" area, the collector current from transistor (1) will supply the base current of the *npn* (3). Thus, by making the "D" smaller, the current will be less hindered by the p-substrate resistance, and the device will have a lower triggering voltage. This is the distinct advantage of DSCR. However, when "D" is too small, the leakage becomes high and it will disrupt the normal operation of the I/O pad. In later sections, detailed simulations with different "D" will be presented. However, using the same principle of positive

feedback as the SCR, when the BJTs are in saturation region, the holding voltage of the DSCR is also around 1.0V, which is susceptible to latch-up.

2.2.4 Major Deficiency of SCR Based Devices

Theoretical analysis in section 2.2.2 and 2.2.3 demonstrates the operating principles of SCR and DSCR. The holding voltages of the two devices are both 1.0V. This voltage is the same if compared with the normal operating voltage of 65 nano-meter technology. Thus, when there is a small undesired current being injected into the p-substrate, it can result in the trigger of SCR and DSCR devices. When these devices are on, they will function as current sinks. This latch-up phenomenon disrupts the integrity of the I/O signals.

Besides normal operating conditions, under high temperature (~ 125 °C) environment, for an IC with 1.5V V_{DD}, a voltage spike of 2.5V is observed [30]. In order to avoid latch-up, the holding voltage of ESD protection devices must be at least 50% higher than the maximum signal voltage [2]. This is an important design consideration.

2.3 Chapter Summary

After detailed theoretical analysis of various non-snapback and snapback ESD protection devices is presented, it is concluded that:

- Forward-biased diodes demonstrate promising ESD performance due to its simple design and high current conducting capability. However, one diode is not sufficient to protect this specific processing technology because the chip's V_{DD} and I/O signal voltages are higher than the diode's turn-on voltage of 0.7V. Thus, stacks of diodes can be used to correct this deficiency, which will be shown in chapter 4.
- Reverse-biased diodes contribute less capacitance during a chip's normal operations compared to forward-biased diodes. However, they require much higher voltage to trigger the avalanche breakdown, which is beyond 10 volts. This property makes reverse-biased diodes a less prominent choice for ESD purposes.

- Ground Gate NMOS is the simplest snapback device. However, it is difficult to realize a perfect stand-alone NMOS device in deep sub-micron CMOS technology that meets all the requirements (2.2.1) [2].
- Silicon Controlled Rectifier (SCR) engages a positive internal feedback scheme to trigger the snapback. However, the conventional SCR is not sufficient to protect modern ICs due to its high triggering voltage. It is used as a design reference for other SCR based devices.
- Darlington Triggered SCR (DSCR) inserts another parasitic *pnp* transistor to amplify the gain of the *npn* transistor and it is manipulative by changing the "D" value. Comparisons of DSCR performance with different "D" values will be done when the DSCR is constructed in the device simulator.
- The SCR based devices have demonstrated a major deficiency in latch-up problem due to the low holding voltage in comparison with the supply and signal voltages of 65 nm technology.

To design a device that can perform well in ESD situations and does not harm the normal operation of an IC, the factors about triggering voltage, holding voltage, leakage, capacitance, area and latch-up immunity, all have to be considered. In chapter 3, a detailed device modeling process will be elaborated, and the introduced ESD protection devices, such as diode, GGNMOS, SCR and DSCR will be compared regarding their performance.

Chapter 3 Device Modeling

3.1 Motivation

In this chapter, a complete design flow will be presented and placed to test for its accuracy and reliability. The design is conducted in Synopsys® TCAD environment, in specific the device construction and simulator tool Sentaurus®. It is capable of 3D device building with a high mesh grid limit. The modeling parameters are partially collected from this specific technology process document and Predictive Technology Model [20]. However, these parameters are not sufficient to complete the model construction. Several possible design variables are explored and put to a trial and error procedure. The modeling process starts with building an NMOS and a PMOS. Then, the technology parameters are exported to build various ESD devices.

3.2 Introduction to Design Tools

3.2.1 Sentaurus®

Sentaurus® has several components that combine to form its overall function as a device simulator. Sentaurus® has a graphical user interface called Sentaurus Structure Editor, which allows users to define custom structures in either 2D or 3D. Another component is Sentaurus Device, which numerically simulates the electrical behavior of an isolated semiconductor device or several physical devices that combine into a circuit [6]. An unlimited mesh grid definition is the advantage of Sentaurus®.

3.2.2 PTM Device Parameters

Predictive Technology Model (PTM) provides accurate, configurable and predictive MOSFET models [20], for transistors and interconnects technologies. This work is developed by Arizona State University. A 65nm process PTM model is used in this research work.

3.3 NMOS Design Process

For correctly modeling a transistor, the important data that device simulators need to construct the model includes the following:

1. Substrate doping

Substrate is the foundation of any process technology. For the case of 65 nano-meters fabrication, it is a piece of lightly doped p-type silicon. Lighter doping correlates with higher resistance because the there are less mobile free charges in the substrate. The level of doping will influence the substrate resistance and avalanche breakdown voltage of snapback ESD protection devices.

2. n-well doping and junction depth

An n-well is essential in ESD device structures. N-well resistance facilitates the triggering of the parasitic *pnp*-transistor in SCR. Also, the n-well connected to I/O port or V_{DD} rail contributes a large amount of capacitance to these nodes due to its depth of hundreds of nano-meters and light doping level. Thus, the n-well must be minimized to reduce the ESD overshoot voltage, which is induced by anode capacitance.

3. Active diffusion doping and junction depth

N^+ and p^+ diffusions form the source and drain of the MOSFET and the emitter or collector of the parasitic BJTs in the SCR structure. Their junctions, in the order of tens of nano-meters, are significantly shallower compared to the n-well doping.

4. Gate oxide thickness

Gate oxide of the MOSFET is the primary ESD protection focus of this research. Because the I/O MOSFET's gate is directly connected to the input signal, any overstress has the potential to punch through the thin oxide. However, this data is readily available from the foundry data sheet. It does not need to go through a trial and error process compared to other parameters.

5. Horizontal-to-vertical diffusion length ratio (XY-ratio)

In fabrication process, it is seen that the thermal annealing after ion implantation will drive the dopants both horizontally and vertically [31]. That ratio also needs to be modeled because it defines the length and depth of a diffusion area.

These five important parameters are required to complete the models of various ESD structures. The starting point of the procedure is to match an n-channel MOSFET device between Cadence® and Sentaurus®.

Firstly, an n-channel MOSFET with a gate length of 65 nano-meters and 1 micro-meter width is used, and a circuit schematic has been constructed in Cadence® environment shown in **Figure 3-1**. In this testing circuit, DC bias voltages, such as V_{GS} and V_{DS} are set to plot the I_{DS}-V_{DS} graph as seen in **Figure 3-2**. Due to the limitation of access to foundry parameters, intelligent trial and error correction become a necessary step in modeling of the NMOS. With the help of PTM parameters, this process becomes relatively easier since some of the important unknowns are narrowed down to a smaller range.

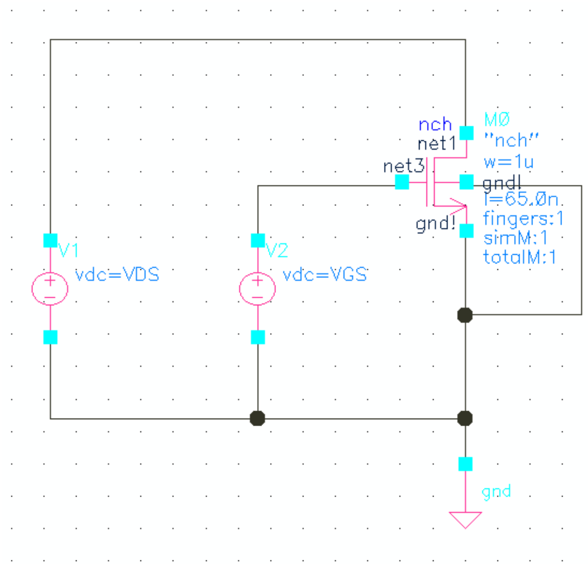


Figure 3-1: 65nm NMOS DC current tracing circuit setup in Cadence environment

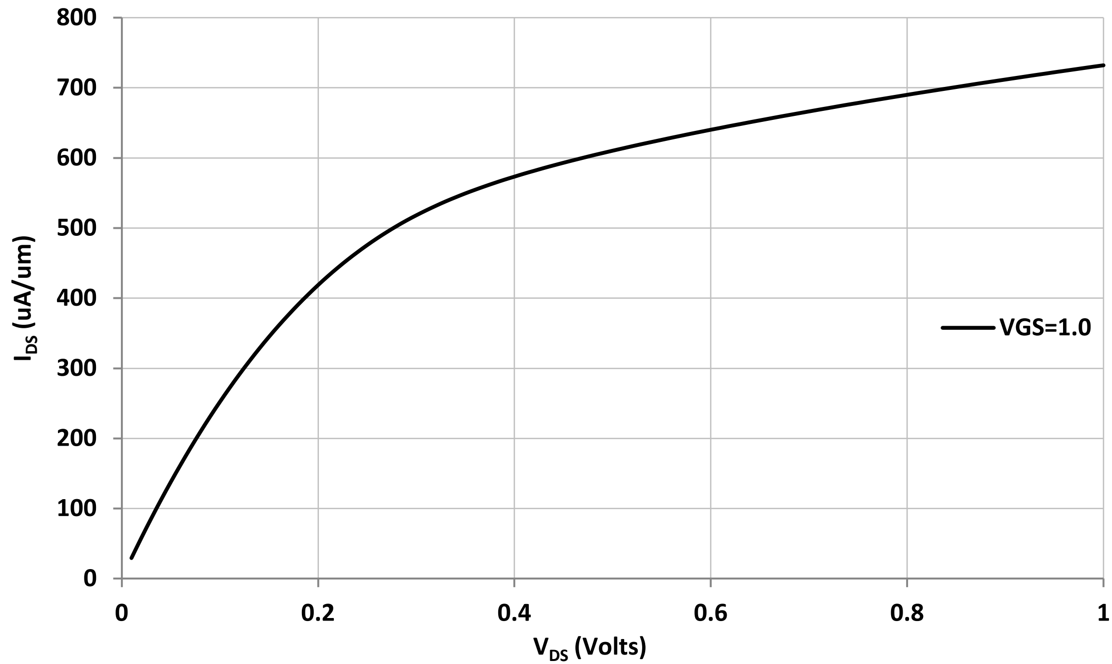


Figure 3-2: Cadence plot of I_{DS} vs. V_{DS} of a 65nm gate length NMOS at V_{GS}=1.0V

Secondly, from the layout structure of the actual NMOS in Cadence® some useful information can be extracted. It is measured that the length of an entire NMOS with gate length equal to 65 nano-meters is 675 nano-meters. The two n^+ active doping regions for the drain and source are

equal in length, i.e. 305 nano-meters on both sides of the gate. Also, the contact length is 9 nano-meters. However, the two active doping zones' halo implantation under the gate is not visible. This is an unknown parameter that needs to be determined. The above information is what the layout can supply to the modeling in Sentaurus®.

Thirdly, from the data sheet of the process technology, more useful parameters that can be obtained are the gate oxide thickness and n-well junction depth. In this case, for NMOS, the gate oxide thickness is 20 angstroms, which is equal to 2.0 nano-meters. The gate oxide is a separator of the polysilicon gate terminal from the channel. The thinner it is, the more capacitance it possesses and the easier it is to be punched through by various kinds of ESD discharge events.

After applying Cadence® as the first modeling step, PTM is used to extract useful doping information. By configuring the PTM model to have a 65 nano-meters gate length and 2.0 nano-meters oxide thickness, the generated model shows accurate results when compared with Cadence plot. The maximum error is 8%. Therefore, the PTM model can be used as a design reference.

From the PTM modeling file, useful parameters are extracted as charted in **Table 3-1**:

Table 3-1: PTM extracted parameter values for 65 nm NMOS process

Parameter	Value
Substrate doping (p-type)	Constant value: 6×10^{16} /cm^3
Active drain/source doping (n-type)	Peak value: 2×10^{20} /cm^3
Drain/source junction depth	19.6 nano-meters
Channel doping (p-type)	Constant value: 1.75×10^{18} /cm^3

With the curve of I_{DS} and V_{DS} from Cadence® and PTM parameters, the model structure building process can proceed. The following steps are presented to construct a model of NMOS in the device simulator.

The model construction is conducted in Sentaurus® Structure Editor (SDE) environment. The following figures in Chapter 3 and 4 are all representing the cross-sectional views of various devices. The x-axis depicts the width of a device and the y-axis depicts the depth of a device, which is set to 1 micro-meter in most cases.

1. A substrate silicon region is defined shown in **Figure 3-3** with 1 micro-meter thickness and 675 nano-meters in width to comply with the Cadence® NMOS layout. The p-type doping concentration of this region is defined as a constant value.

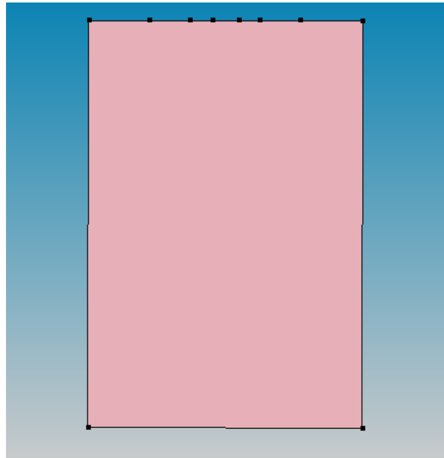


Figure 3-3: A 670nm wide and 1um thick slab p-substrate (shown as pink) as the foundation of the NMOS

2. Drain and source doping regions have been initially defined to match the gate length, which are 65 nano-meters. Therefore, the gate is defined as 305~370 nano-meters. Drain is 0~305 nano-meters and source is 370~675 nano-meters. Their junctions are both 20 nano-meters below the surface with peak doping of 2×10^{20} /cm^3. However, the extension of drain and source under the gate is unknown, which needs to be calibrated.

3. Gate oxide thickness is obtained through the process technology document which is equal to 20 Angstrom, i.e. 2.0 nano-meters as seen in **Figure 3-4**.

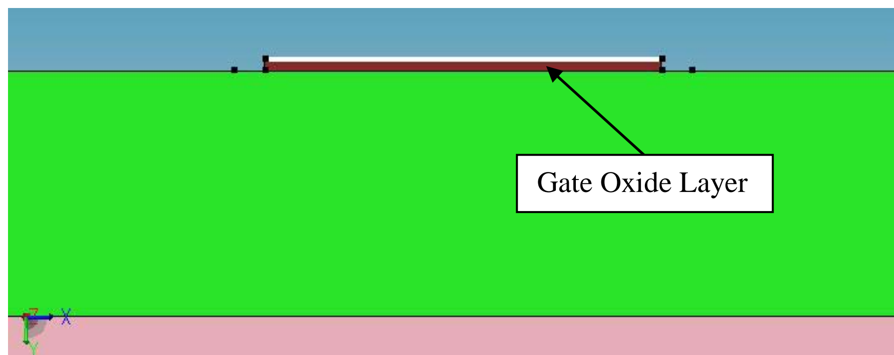


Figure 3-4: A 2nm thick Gate oxide layer (shown as brown) on top of the slab p-substrate

4. A channel depth of 10 nano-meters is defined as an initial trial value, which will be adjusted to fit the actual curve.

5. The diffusions are activated and driven into their corresponding width and depth shown in **Figure 3-5**. In order to obtain good numerical analysis accuracy, finer mesh grids are defined at all the depletion regions and material boundaries, such as between n^+ diffusions and channel.

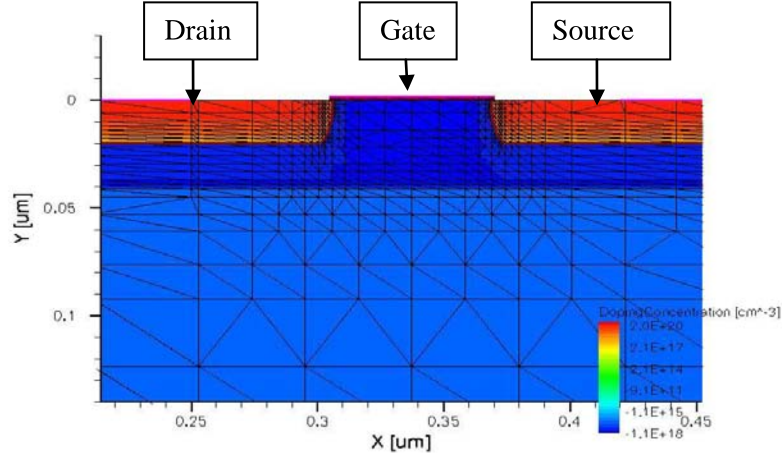


Figure 3-5: Cross-sectional view of Sentaurus generated mesh of a 65 nm NMOS structure

3.3.1 Design Variable Exploration

To meet the I_{DS} vs. V_{DS} curve generated by Cadence® simulation, several design variables are explored to observe their correlations with the actual NMOS properties.

1. The substrate doping level is put to test. The device's behavior differs according to the substrate doping level. Because the drain's n^+ diffusion and the substrate's p^- doping will form a p-n junction which has influence on the threshold voltage of the MOSFET, as Equation 3-1 and 3-2 depicted:

$$V_T = V_{FB} + 2\phi_F + \frac{\sqrt{2\varepsilon_s q N_a (2\phi_F + V_{SB})}}{C_{ox}} \quad \textbf{[21]} \qquad \text{Equation 3-1}$$

$$V_T \propto \sqrt{N_a} \qquad \text{Equation 3-2}$$

It is seen that the substrate doping N_a has a direct relation with the threshold voltage [31]. When the doping level is higher, V_T becomes higher. From Equation 3-3 of the saturation current of an NMOS, it can be observed that when substrate doping N_a is higher, I_{DS} becomes lower with the same bias condition V_{GS} and vice versa.

$$I_{DS} = \frac{1}{2}\mu_N C_{ox}\frac{W}{L}(V_{GS} - V_T)^2$$ Equation 3-3

From **Figure 3-6** below, it is seen that with a variation of substrate doping concentration from 1×10^{15} /cm^3 to 1×10^{17} /cm^3 the drain current becomes lower with a higher concentration. In the range of 1×10^{16} /cm^3 the curve is the closest to the Cadence reference line.

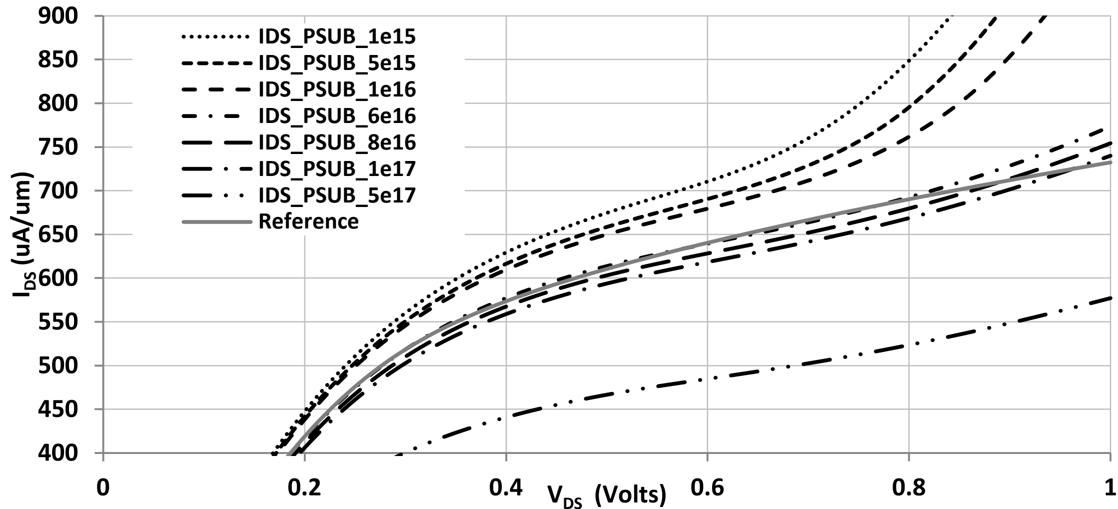


Figure 3-6: 65nm NMOS I_{DS} vs. V_{DS} curves with p-substrate doping variation

2. Two doping reference windows are placed on the surface of the slab substrate silicon. They are the drain and source locations. Similar to the fabrication processes, the impurity sources are implanted at the surface that is where the peak concentration is. Active doping impurities are then driven into the substrate when the annealing happens. The exact length of the n-type extension under the gate is defined by trying a set of different drain and source combination. In **Table 3-2** below, six sets of drain and source doping windows are defined and so are the effective gate lengths (L_{eff}) which is the actual distance between two active n^+ diffusions under the gate.

Table 3-2: 65nm NMOS drain/source configuration sets

Set Number	Drain (nm)		Source (nm)		L_{eff} (nm)
1	0	280	395	675	103.0
2	0	285	390	675	92.8
3	0	290	385	675	82.4
4	0	295	380	675	73.0
5	0	300	375	675	62.8
6	0	305	370	675	53.0

In **Figure 3-7** below, it is seen that when the effective channel length is greater than 65 nanometers, i.e. when the polysilicon gate does not overlap any portion of the n^+ active doping regions. The induced drain-to-source current is very low as shown in Set 1, 2, 3 and 4 of **Figure 3-8**. This gap between the polysilicon gate and the n^+ diffusion is too large for the DC bias voltage V_{GS} to function properly to create a channel for the current to flow through.

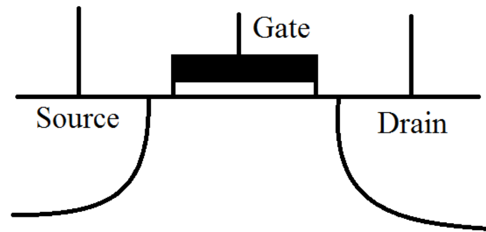


Figure 3-7: NMOS drain, source and gate configuration without gate oxide overlapping halo region

When the effective channel length is too short, such as Set 6, the current is too much compared to the reference line. The set with the closest match to the standard is Set 4. This phenomenon can be verified by the I_{DS} formula in Equation 3-4. The L_{eff} term is the effective length of the gate channel. When this value is small, the current becomes high.

$$I_{DS} = \frac{1}{2}\mu_N C_{ox}\frac{W}{L_{eff}}(V_{GS} - V_T)^2$$

$$\boldsymbol{I_{DS} \propto \frac{1}{L_{eff}}} \qquad \text{Equation 3-4}$$

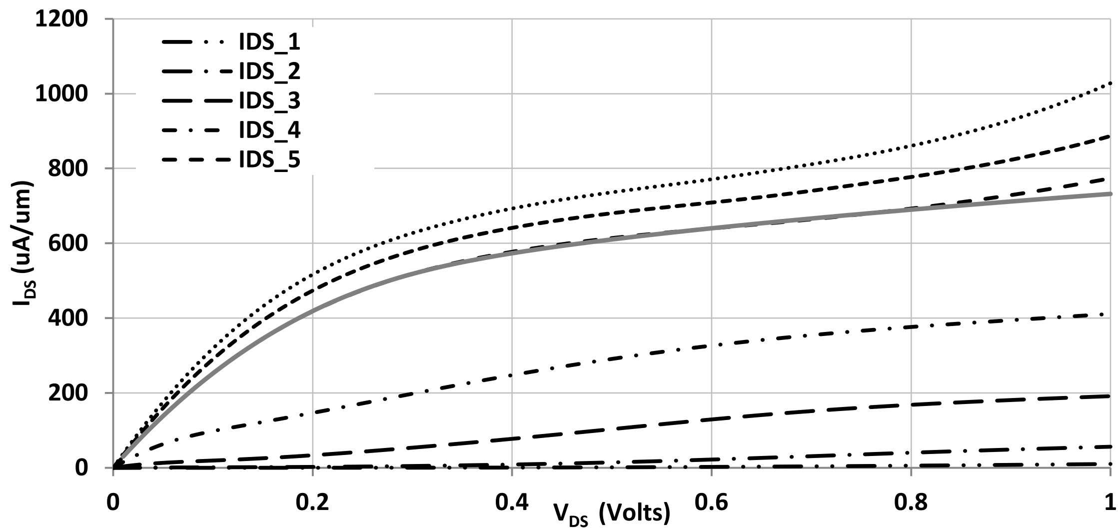


Figure 3-8: 65nm NMOS I_{DS} vs. V_{DS} curves with different drain/source and gate configurations

3. A p-type doping level of 2×10^{18} /cm^3, which is decided from PTM's 1.75×10^{18} /cm^3 reference, is used for the channel as a starting point before the calibration. The determination process has evaluated various doping levels from 1×10^{17} /cm^3 to 2×10^{18} /cm^3 [32].

The MOSFET channel is created by the voltage difference between the gate and substrate contacts. In NMOS transistors, under normal operating mode, the gate is connected to a positive voltage and substrate is connected to ground. Due to this potential difference, and the gate oxide insulator between the polysilicon gate and the substrate, a capacitor is formed shown in **Figure 3-9**. When positive charges are accumulated on the top plate of the capacitor, the other side will respond by gathering negative charges as a result.

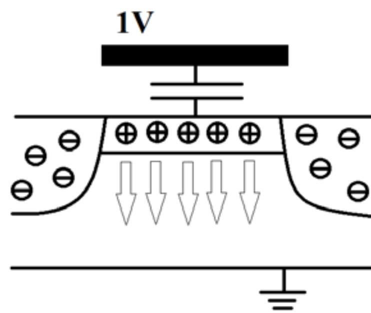


Figure 3-9: Holes in the NMOS channel being expelled when gate and substrate has a positive potential difference

When the channel has a higher p-type doping, there will be less minority carriers, which are electrons in this case, present in the channel. The electric field in the capacitor will be less effective to pull the negative charges up from the substrate. Thus, the n-type channel is more difficult to form and eventually results in less current conducting ability between the source and the drain of the NMOS. This theoretical phenomenon is proven with simulation results. Shown in **Figure 3-10**, it is seen that with higher p-type channel doping, less current I_{DS} is generated with the same bias voltage of 1.0V.

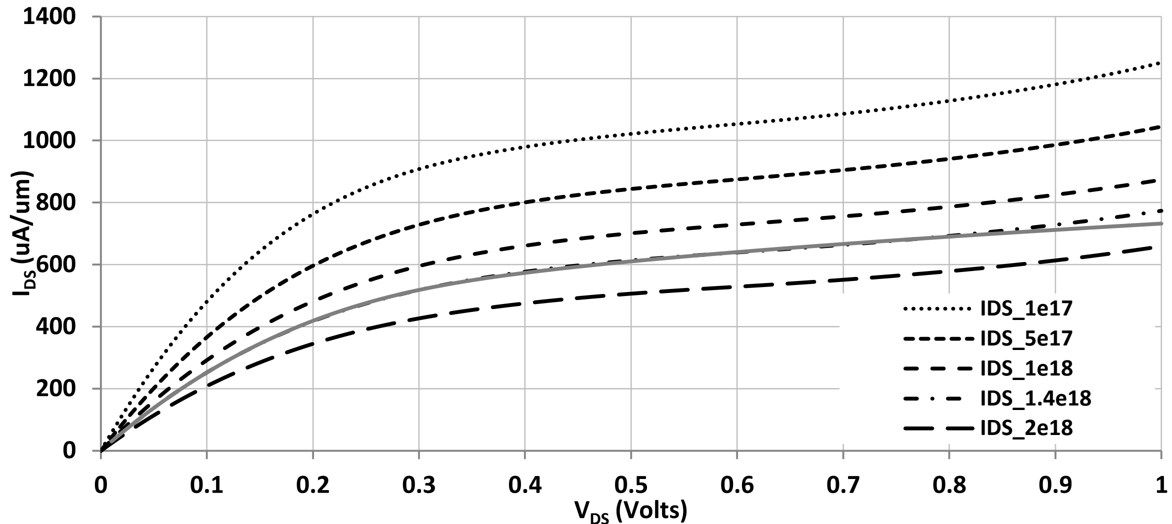


Figure 3-10: 65nm NMOS I_{DS} vs. V_{DS} curves with different channel doping

4. Using same concept as channel doping, channel depth is also an important parameter for the device modeling. **Figure 3-11** depicts a range of channel depth from 5 nano-meters to 30 nano-meters.

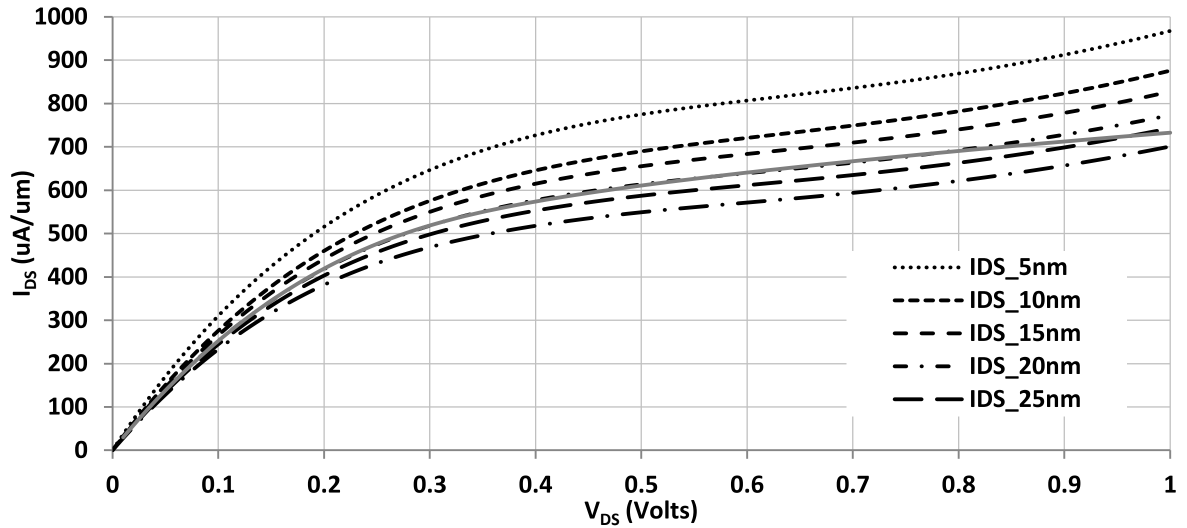


Figure 3-11: 65nm NMOS I_{DS} vs. V_{DS} with different channel depths from 5nm to 25nm as indicated in legend

After the above design parameters are explored with an intelligent trial and error process, the final values of parameters presented in **Table 3-3** below:

Table 3-3: Final parameters for NMOS with 65 nano-meters gate length

Doping	Reference Window		L_{eff}	Peak Concentration	Junction Depth
Drain	0 um	0.300 um	62.8 nm	2×10^{20} /cm^3	20 nm
Source	0.375 um	0.675 um		2×10^{20} /cm^3	20 nm
Channel	X	X	X	1.4×10^{18} /cm^3	20 nm

Figure 3-12 shows the final matching result of NMOS between Cadence® and the constructed model in Sentaurus®. The figure demonstrates the I_{DS} at different V_{GS} conditions; from top to bottom V_{GS} varies from 1.0V to 0.4V. The gray solid lines represent Cadence reference results and the dashed black lines represent the Sentaurus modeled NMOS results. By comparing the curves, the maximum error is 3.1%. Thus, the constructed NMOS model is reliable.

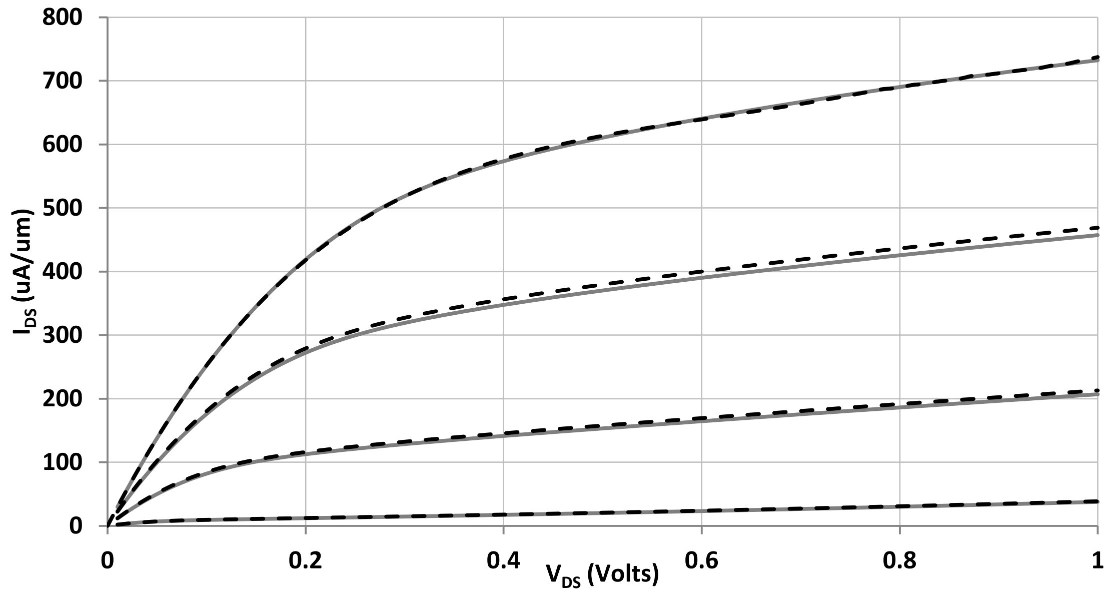


Figure 3-12: Final Sentaurus modeling vs. Cadence reference (gray lines represent Cadence reference and dashed black lines represent Sentaurus results)

The final constructed NMOS model's cross-sectional view is shown in **Figure 3-13**. The red-yellow color represents n-type doping, as the red being higher concentration. Bluish color represents p-type doping with lower concentration, while dark blue represents higher p-type doping.

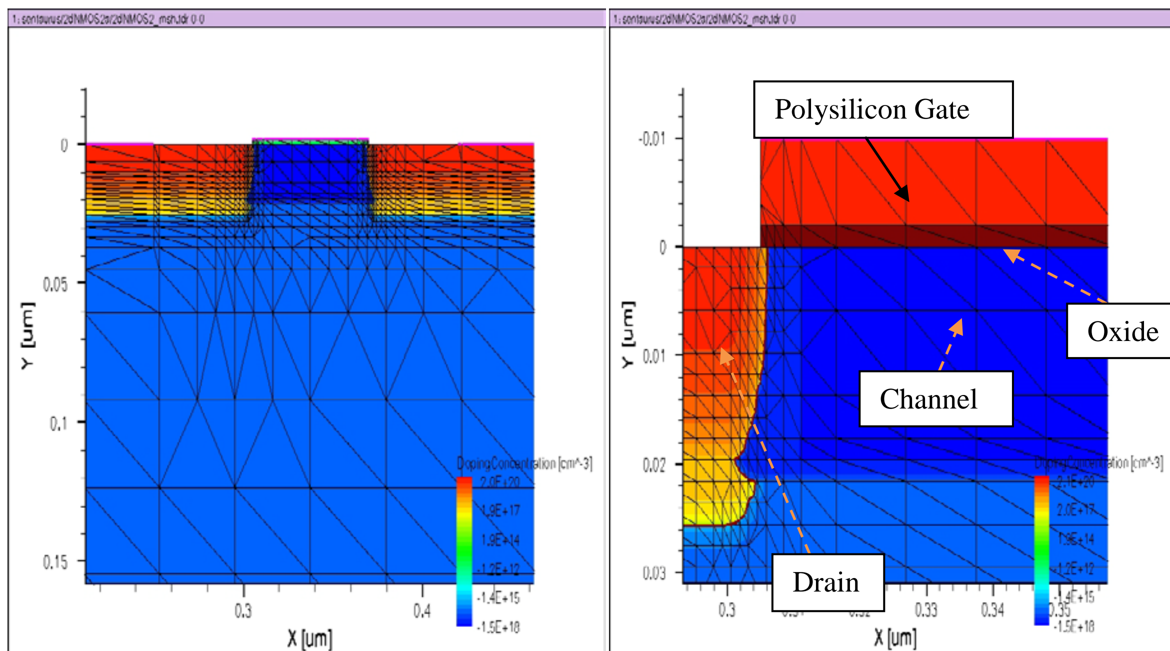


Figure 3-13: Final NMOS model in Sentaurus

3.4 PMOS Design Process

Using the same process of the NMOS building methods, the PMOS structure matching is also conducted between Cadence® and Sentaurus®. The importance of PMOS modeling is to find the accurate values of p^+ active doping and n-well parameters.

From the foundry document, it is found that the PMOS gate oxide thickness is more than the NMOS. It is equal to 22 angstrom (2.2 nano-meters). The PMOS test circuit in built Cadence shown in **Figure 3-14**. PTM generated parameters are shown in **Table 3-4** below.

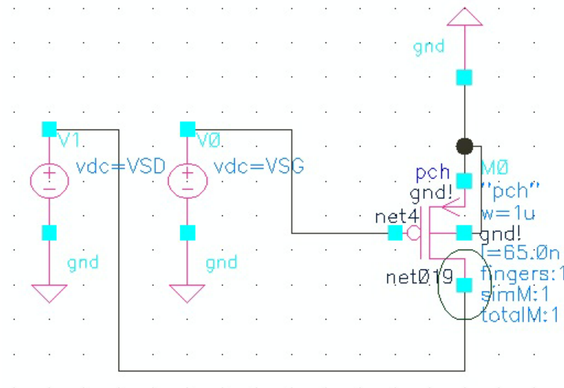


Figure 3-14: 65nm PMOS DC current tracing circuit setup in Cadence environment

Table 3-4: PTM values for PMOS with 65 nano-meters gate length

Parameter	Value
Substrate doping (p-type)	Constant value: 6×10^{16} /cm^3
n-well doping	Constant value: 4×10^{17} /cm^3
Active drain/source doping (p-type)	Peak value: 2×10^{20} /cm^3
Drain/source junction depth	19.6 nano-meters
Channel doping (p-type)	Constant value: 1.36×10^{18} /cm^3

By applying the intelligent trial and error procedure, parameters are adjusted to match between Cadence and Sentaurus. Their final values are presented in **Table 3-5**.

Table 3-5: Final parameters for PMOS with 65 nano-meters gate length

Doping	Reference Window		L_{eff}	Peak Concentration	Junction Depth
Drain	0 um	0.300 um	63.0 nm	2×10^{20} /cm^3	20 nm
Source	0.375 um	0.675 um		2×10^{20} /cm^3	20 nm
n-well	X	X	X	4×10^{17} /cm^3	600 nm
Channel	X	X	X	3×10^{18} /cm^3	13 nm

Figure 3-15 shows the cross-sectional structure of PMOS built in Sentaurus. The red-brown color represents n-type doping, as the red being higher concentration and brown being lower concentration. Bluish color represents p-type doping with lower concentration, while dark blue represents higher p-type doping.

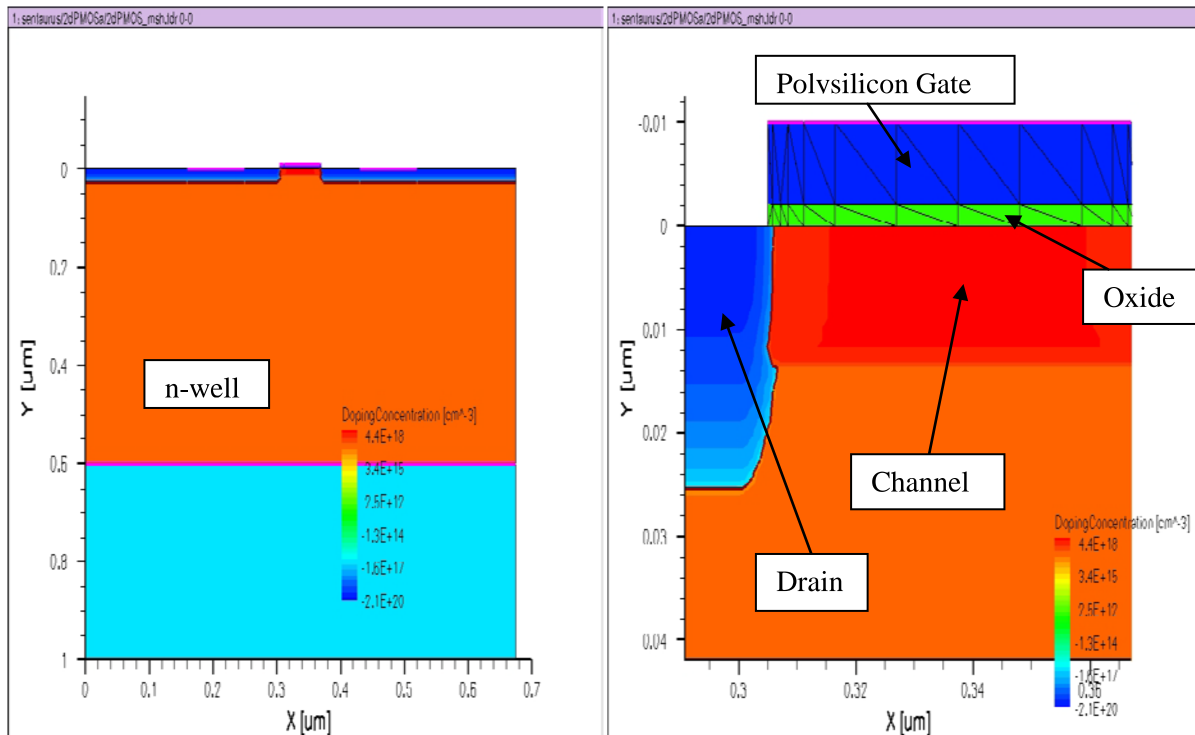


Figure 3-15: Final model of PMOS in Sentaurus

Figure 3-16 shows the final matching result of PMOS between Cadence® and the constructed model in Sentaurus®. The figure demonstrates the I_{SD} at different V_{SG} conditions; from top to bottom V_{SG} varies from 0.4V to 1.0V. The gray solid lines represent Cadence reference results and the dashed black lines represent the Sentaurus modeled NMOS results. By comparing the curves, the maximum error is 3.8%. Thus, the constructed PMOS model is reliable.

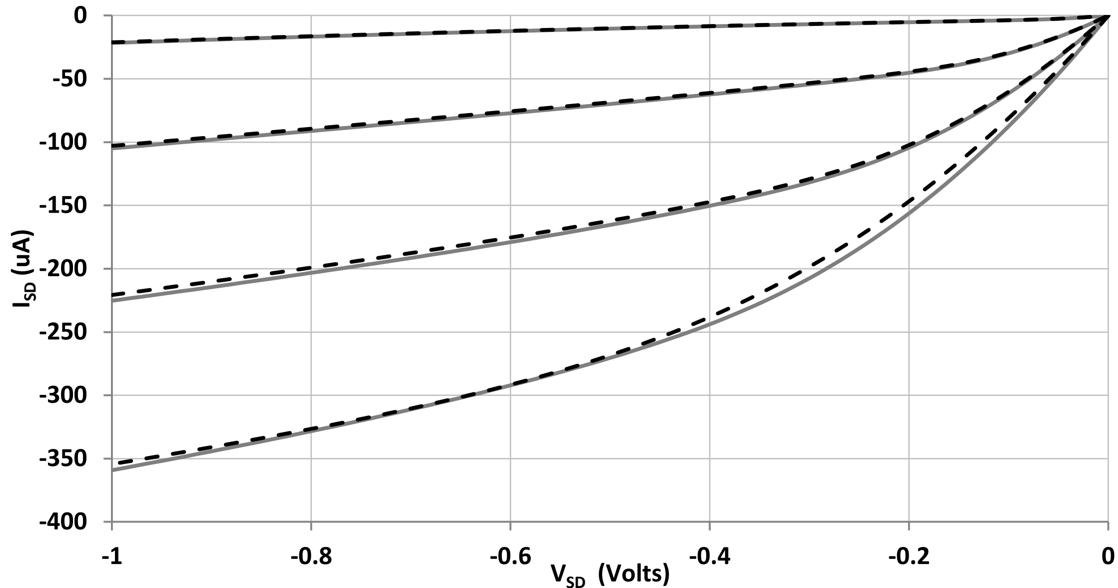


Figure 3-16: Final Sentaurus model vs. Cadence reference I_{SD} vs. V_{SD} curves

3.5 Diode

As analyzed in Chapter 2, diode is a promising solution for ESD protection purposes. With the parameters extracted from the MOSFETs, a diode structure is built in Sentaurus shown in **Figure 3-19**. This diode is an n^- diode, with a p^+ and n^+ active diffusions residing in the n-well and its p-n junction is located between p^+ and n-well. It is configured as 100 micro-meters in width, which will be kept constant for all other devices to perform parallel comparison. In this diode structure, the n-well length is 3 micro-meters and the two active doping regions are 1.3 micro-meters in length.

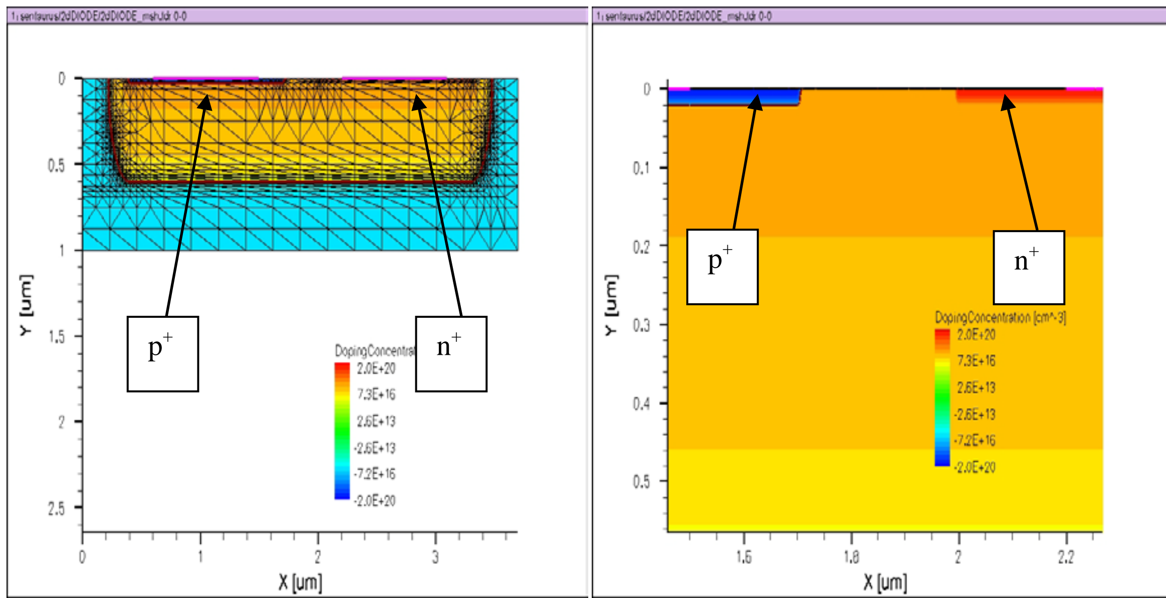


Figure 3-17: n- diode model's cross-sectional view in Sentaurus®, blue color indicates p-type doping, red color indicates n-type doping and yellow color indicates lower concentration n-type doping

There are two polarities that a diode can be used in an ESD protection scheme, forward biased and reverse biased. The I-V curves for both cases are shown in **Figure 3-18**.

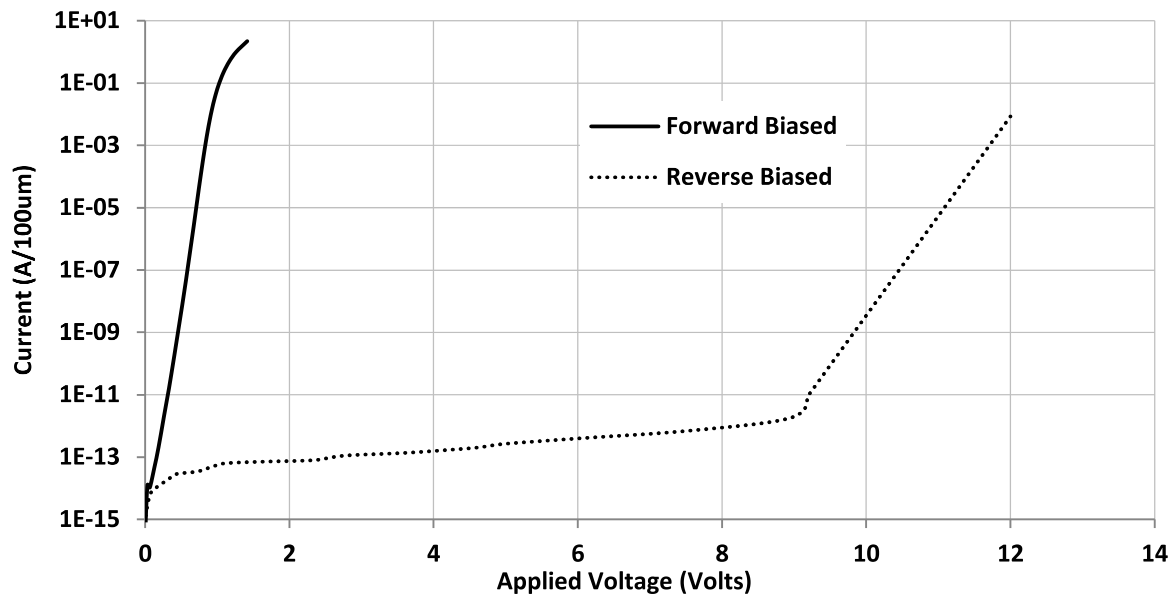


Figure 3-18: Forward and reverse biased diode I-V curves

The I-V curves correspond with the analysis from Chapter 2. Forward-biased diode displays an exponential current increase with the applied voltage at p^+ node.

$$I_D = I_S\left(e^{V_D/V_T} - 1\right) \approx I_S e^{V_D/V_T} \qquad V_T = 0.026V$$

$$\log I_D = \log I_S e^{V_D/V_T}$$

$$\log I_D = \frac{V_D}{V_T}\log(I_S e) = Constant \times V_D$$

On **Figure 3-18**, it is seen that in 0~1.0V range, the forward biased diode's current is linear on log scale. When the current is higher, the diode enters high injection region and the slope becomes flat. This correlates with the theory [21], and it shows that the constructed model is reliable.

A reverse-biased diode has to reach a high voltage, in this case 9.2V, for the avalanche breakdown to happen, and then conducts current. **Figure 3-19** depicts the condensed impact ionization happening at the p^+ region (Orange zone) after heavily biased from the n^+ node.

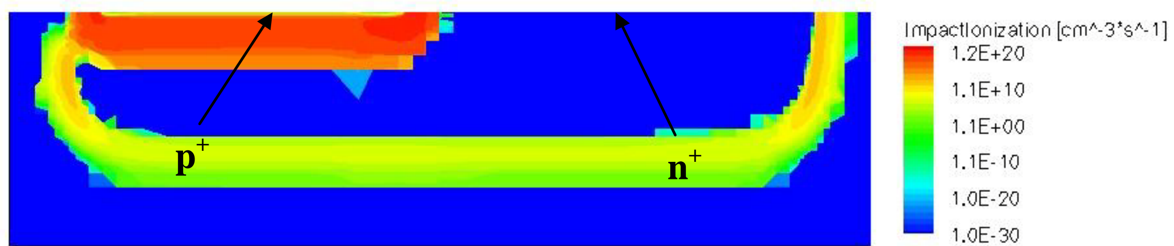


Figure 3-19: Impact ionization zone of reverse biased diode, red color indicates heavy recombination

Since the nominal supply voltage in this process technology is 1.0V, it is concluded that one forward-biased diode is not a good choice for ESD purpose. At 1.0V, the diode will conduct and draw a large amount of current, thus making the I/O port ineffective due to diode's on-voltage of 0.7V, which is substantially lower than the 1.0V normal condition. However, with more stacking diodes, the configuration becomes a prominent choice. Diode-stacking ESD solution will be discussed in the next chapter.

3.6 Ground-Gate NMOS (GGNMOS)

As discussed in Chapter 2, ground-gate NMOS is the simplest snapback ESD protection device. With the constructed Sentaurus® NMOS model, the I-V curve of this device is plotted in the simulator shown in **Figure 3-20**. It demonstrates that at supply voltage or logic high state of 1.0V, the GGNMOS conducts 72 micro-amps as leakage current. This is undesirable and thus the direct use of GGNMOS has not been considered as an effective I/O protection tool for deep sub-micron technologies [2].

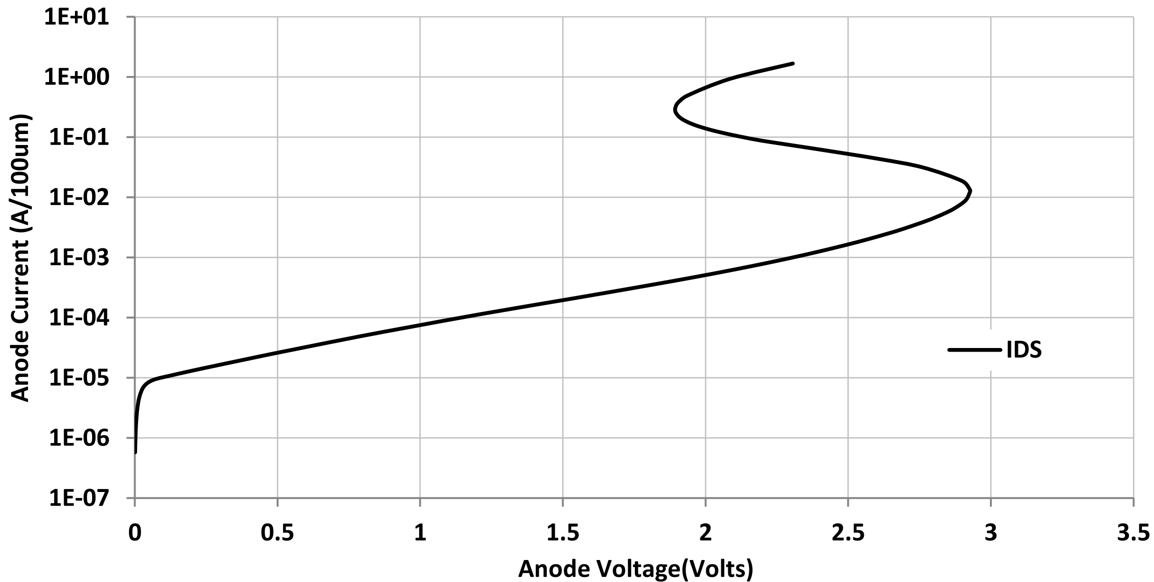


Figure 3-20: GGNMOS snapback I-V curve

3.7 Silicon Controlled Rectifier (SCR)

SCR device is implemented in Sentaurus with NMOS and PMOS parameters to test its performance. Firstly, an SCR shown in **Figure 3-21** with wide inter-diffusion distance is constructed. Its p^+ and n^+ diffusions have 1.0 micro-meter distance in between. This model is served as a reference to other modified ones.

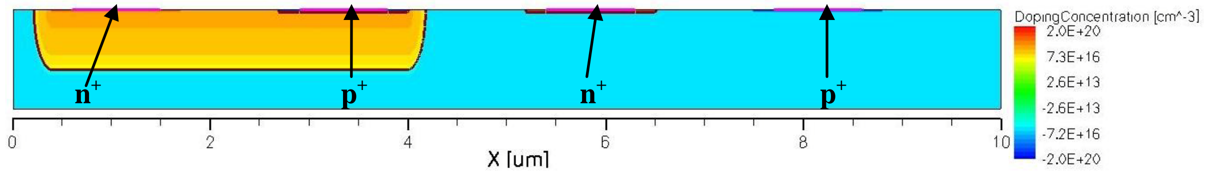


Figure 3-21: SCR model's cross-sectional view in Sentaurus, red-yellow colors indicate n-type doping and bluish color indicates p-type doping

By using a complex continuation simulation method, which is an arbitrary shape tracing tool in Sentaurus, the I-V curve of this SCR is plotted as in **Figure 3-22** below. The triggering voltage V_{t1} is at 18.5V. However, this voltage is too high for this processing technology. The MOSFET gate breakdown voltage is less **than 5V** as outlined in Chapter 1, and then the first triggering voltage needs to be lower than that voltage to prevent gate oxide damage.

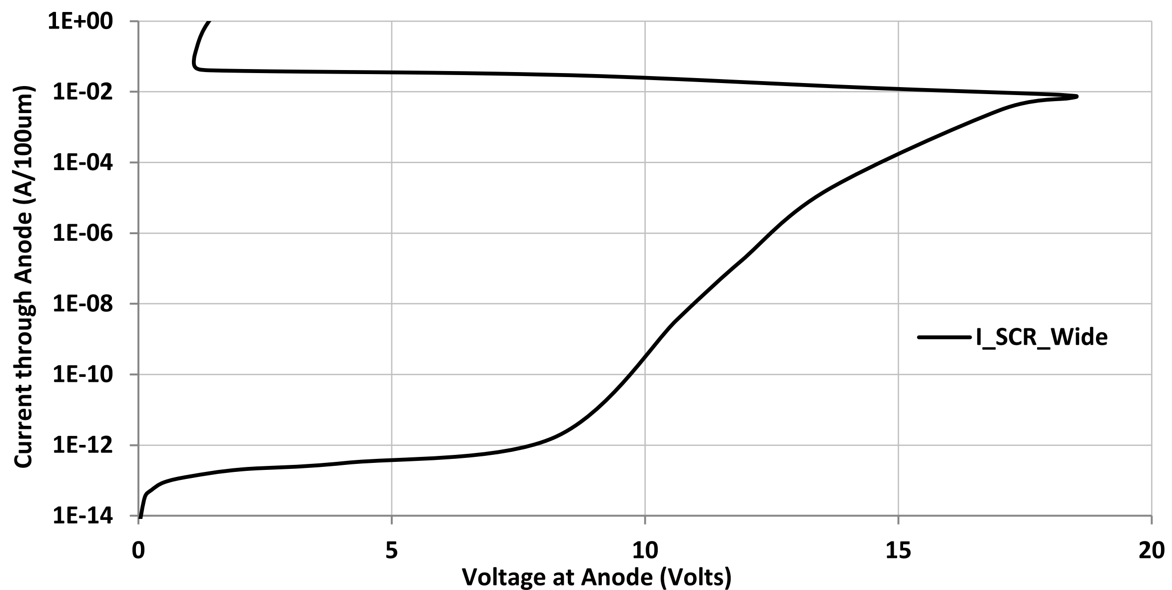


Figure 3-22: Wide SCR I-V curve

To the triggering voltage, the tab distance between active diffusions is reduced. As depicted in **Figure 3-23** below, a new narrower SCR is constructed which has the inter diffusion distance of 300 nano-meters.

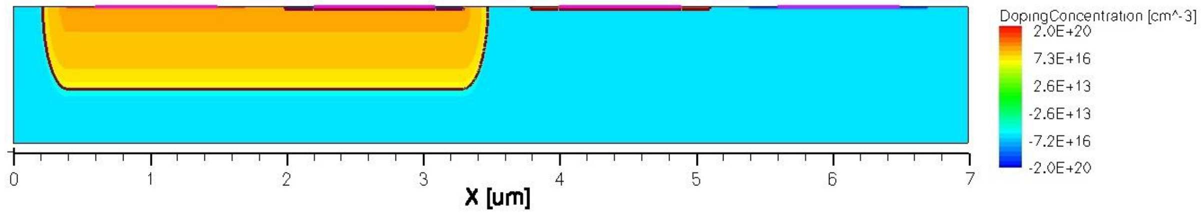


Figure 3-23: Narrow SCR model's cross-sectional view in Sentaurus, red-yellow colors indicate n-type doping and bluish color indicates p-type doping

This distance is decided from various factors. Firstly, the processing technology requires the n^+ and p^+ diffusions to have greater than 180 nano-meters' spacing. However, a safety margin is kept to avoid any variation during the fabrication process. Then a distance is chosen at 300 nano-meters. By decreasing the inter-diffusion distance, the current travelling from the n-well to the n^+ active region is increased. This is because that the current in the substrate is travelling a shorter distance compared to the wide SCR. Also, due to the potential difference between anode and cathode, an electric field is realized between the n-well and n^+ region [33]. With the distance becoming narrower, the electric field increases as seen in **Figure 3-24**, thus it provides a stronger driving force for the current to travel through the p-substrate region between n-well and n^+ diffusion [33]. These phenomena have caused the base current of the parasitic *npn*-transistor to increase, thus providing more current to the collector of the *npn*-transistor. Therefore, the narrower inter-diffusion distance can bring down the first triggering voltage of the SCR.

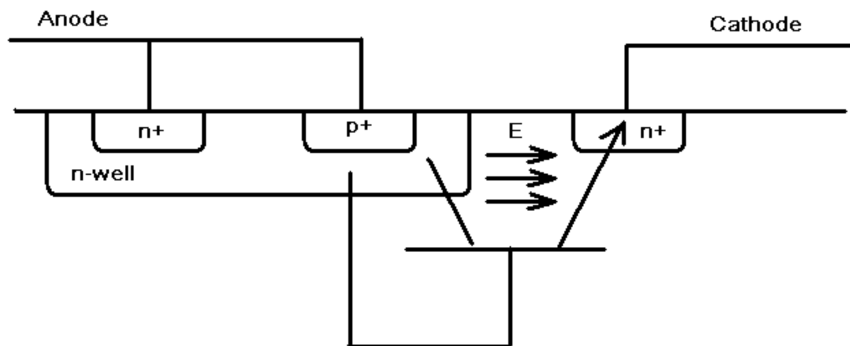


Figure 3-24: Electric field and *npn* transistor between n-well and n^+ in SCR

In the I-V curve depicted in **Figure 3-25**, it is seen that the first triggering voltage decreases to 12.1V compared with the 18.5V of the original wide SCR.

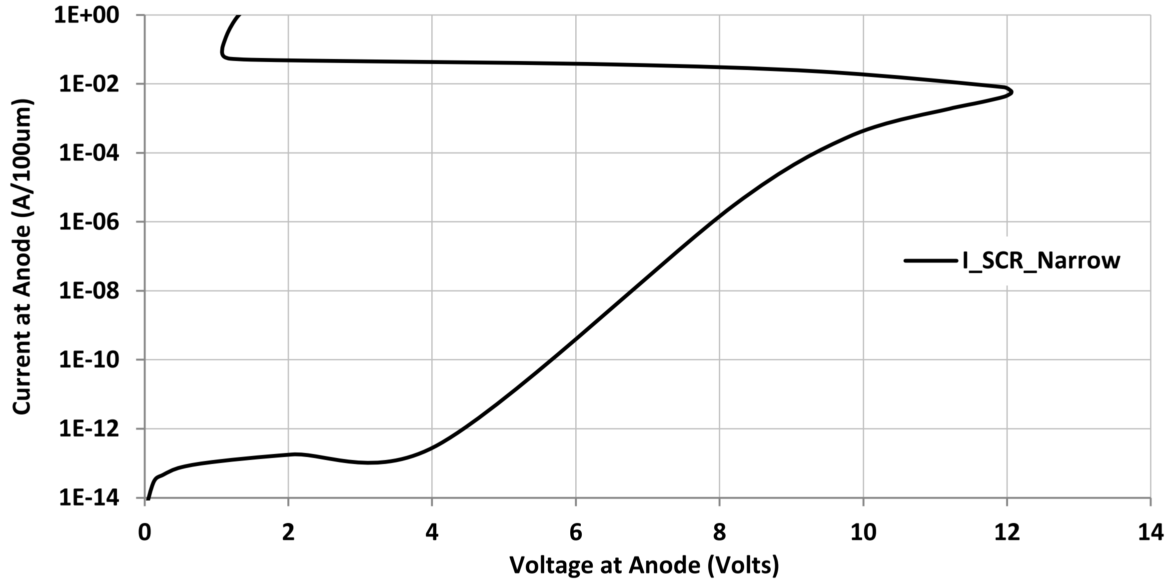


Figure 3-25: Narrow SCR I-V curve

3.8 Darlington-Based Silicon Controlled Rectifier (DSCR)

DSCR has the advantage of an extra triggering *pnp* transistor shown in **Figure 2-9**, whose collector is connected to the base of the *npn* transistor. From Chapter 2, it is explained that the reduction of the "D" value can cause the triggering voltage (V_{t1}) to become lower. The structure of the DSCR is constructed in Sentaurus and depicted in **Figure 3-27**.

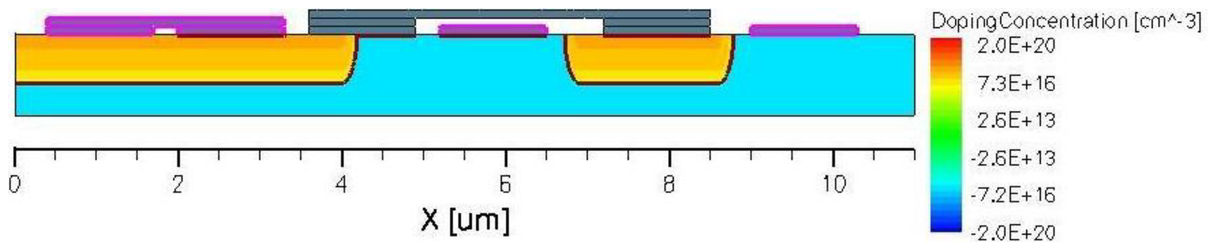


Figure 3-26: DSCR model's cross-sectional view in Sentaurus, red-yellow colors indicate n-type doping and bluish color indicates p-type doping

The I-V curves of DSCR with different "D" values are plotted in **Figure 3-28**. It can be seen that when "D" is reduced to the design limitation, which is 200 nano-meters, the leakage current at 1.0V becomes excessive, more than 3 micro-amps compared to the limitation of 1 nano-Amp. Thus, high leakage current that a narrow "D" DSCR possesses is not energy efficient.

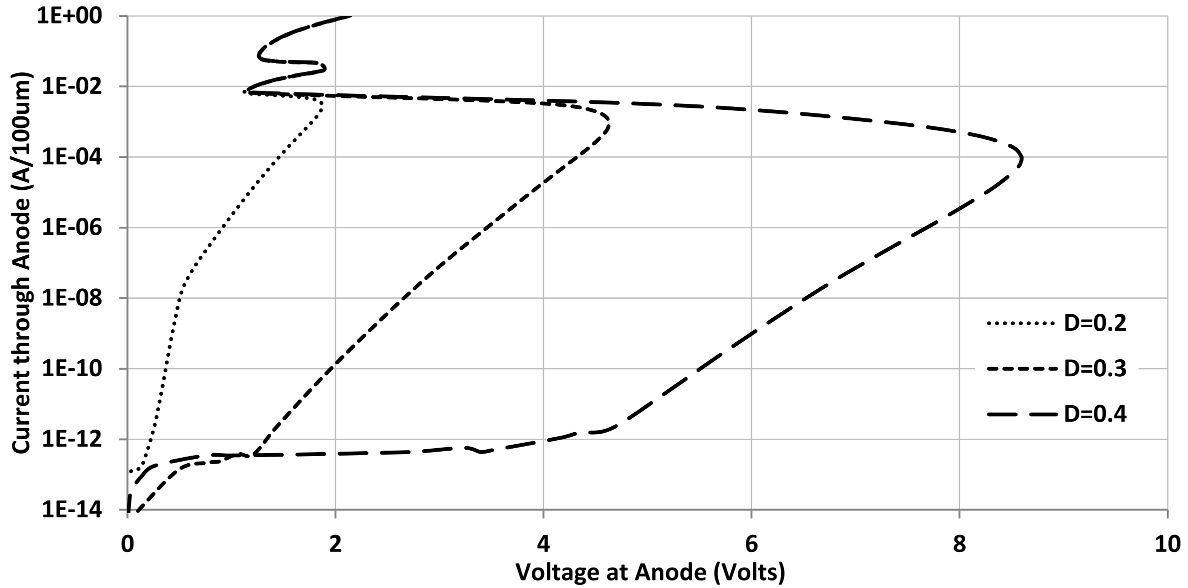


Figure 3-27: DSCR I-V curves with various "D" values (D=0.2, 0.3 or 0.4 um)

From **Figure 3-29**, which demonstrates the total current density while the DSCR is conducting, it is seen that the extra *pnp* transistor injects current to the *npn* transistor's collector, where the arrow is pointing.

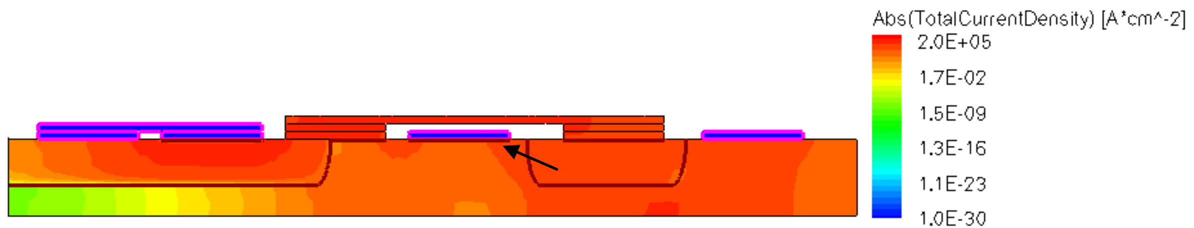


Figure 3-28: Current density contour for DSCR with D=0.3um, red color indicates higher current density

3.9 Diode Triggered Silicon Controlled Rectifier (DtSCR)

From the I-V curves of different SCR based snapback devices above, it is seen that the devices either have an excessive triggering voltage or leakage current. They are both undesirable characteristics for an ESD protection device. For this processing technology the triggering voltage must be lower than 5V with leakage current lower than 1 nano-Amp. Moreover, the holding voltage must be above 1.5V to avoid latch-up from happening.

As an enhancement technique, the triggering voltage can be reduced by adding diodes between the n-well and the p^+ active diffusion in the substrate [34]. These diodes can contribute to higher holding voltage, which makes the SCR less susceptible to latch-up. These diodes can also make the triggering of the *npn* transistor quicker due to the voltage drop across these diodes. **Figure 3-30** is a schematic representation of this diode-triggered SCR technique with one or two diodes. To implement these DtSCRs on device level, various modifications of the original SCR are conducted as shown in **Figure 3-31**.

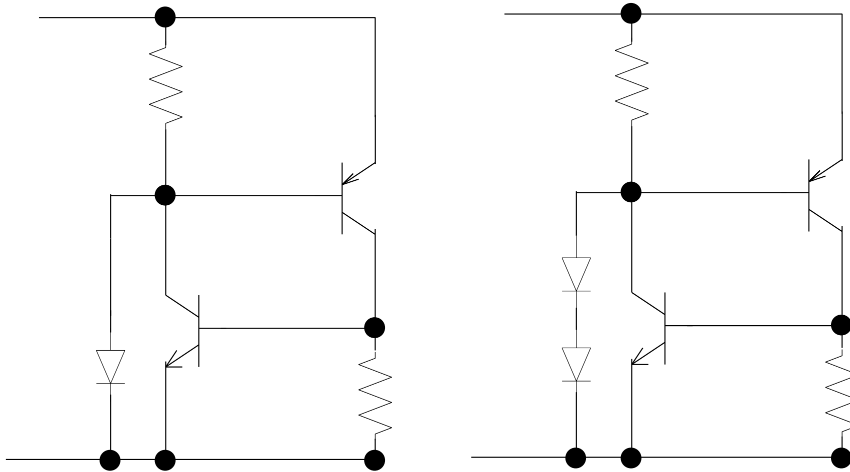


Figure 3-29: DtSCR schematic models with one and two diode configurations

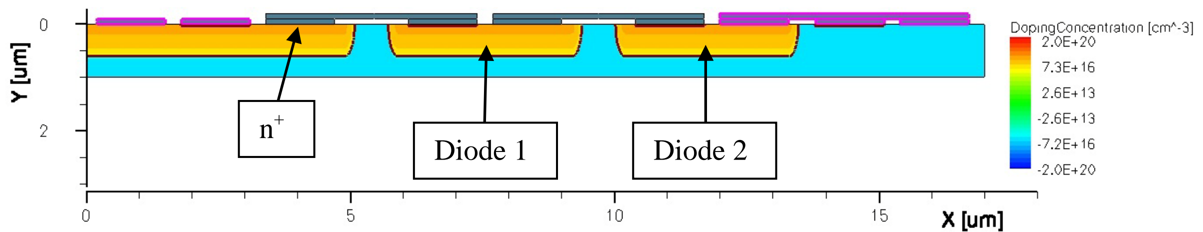


Figure 3-30: DtSCR model's cross-sectional view with two diodes in Sentaurus, red-yellow colors indicate n-type doping and bluish color indicates p-type doping

1. An extra n+ diffusion is added to the right of the p^+ diffusion to form an n-well connection to the diodes.

2. One or two n^- diodes are placed in series between the first n-well and cathode n^+/p^+ diffusions.

After these modifications, several new phenomena are observed. Firstly, the extra n^- diodes are forming into two stacks of *pnp* transistors as shown in **Figure 3-32** and **Figure 3-33**. From the base of the *pnp* transistor in the second n-well, the current injects to the emitter of the *pnp* transistor in the third n-well. The collector current of these two transistors travels through p-substrate resistance and sink to the cathode. Secondly, the *npn* transistor between the first and the second n-well will function as a current injector to inject current into the second n-well from left to right, which is the base current flow direction of *pnp* (2). Thus, this current enhances the base current of *pnp* (2), and results in more collector current of *pnp* (2) being sunk into the substrate [34] [35]. This is verified by the current density contour in **Figure 3-34**, in which it is seen that the current is dissipated through the stacks of *pnp* and the *npn* transistors.

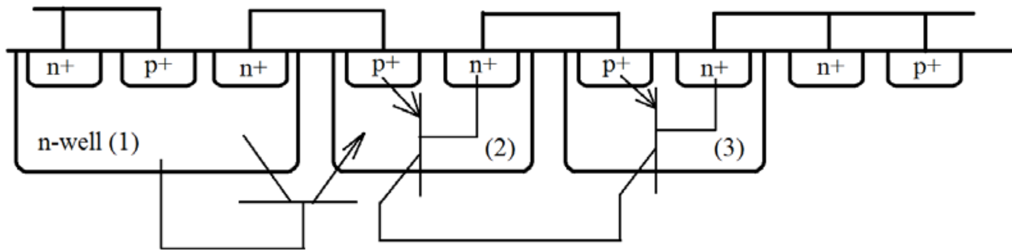


Figure 3-31: DtSCR diodes' formation of stacks of *pnp* transistors

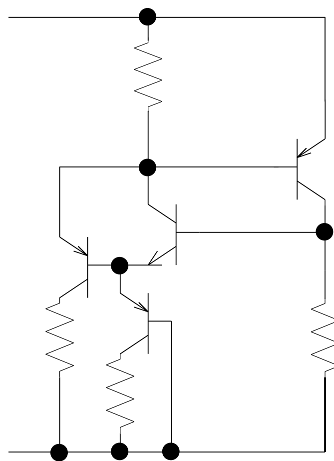


Figure 3-32: DtSCR's actual schematic view

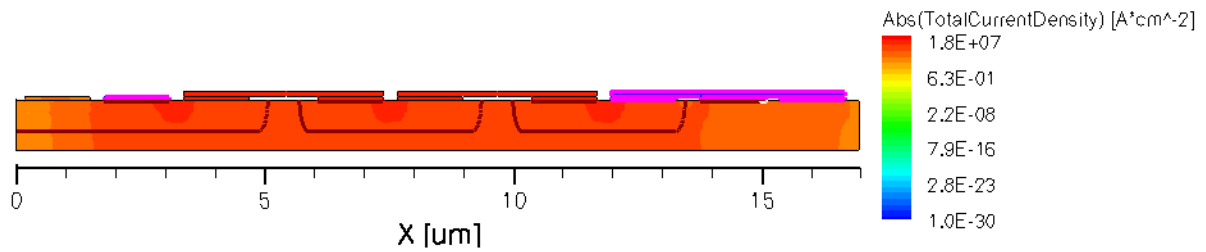


Figure 3-33: Current density contour for DtSCR when conducting, red color indicates higher current density

The quasi-DC simulation of the I-V curve is shown in **Figure 3-35** below. When one diode is added, it is seen that the configuration is disqualified due to its high leakage current at 1.0V. The 2-diode DtSCR demonstrates a low triggering voltage of 2.26V, a high holding voltage of 2.05V, and a low leakage current at 1.0V. It meets the requirements for ESD protection purposes.

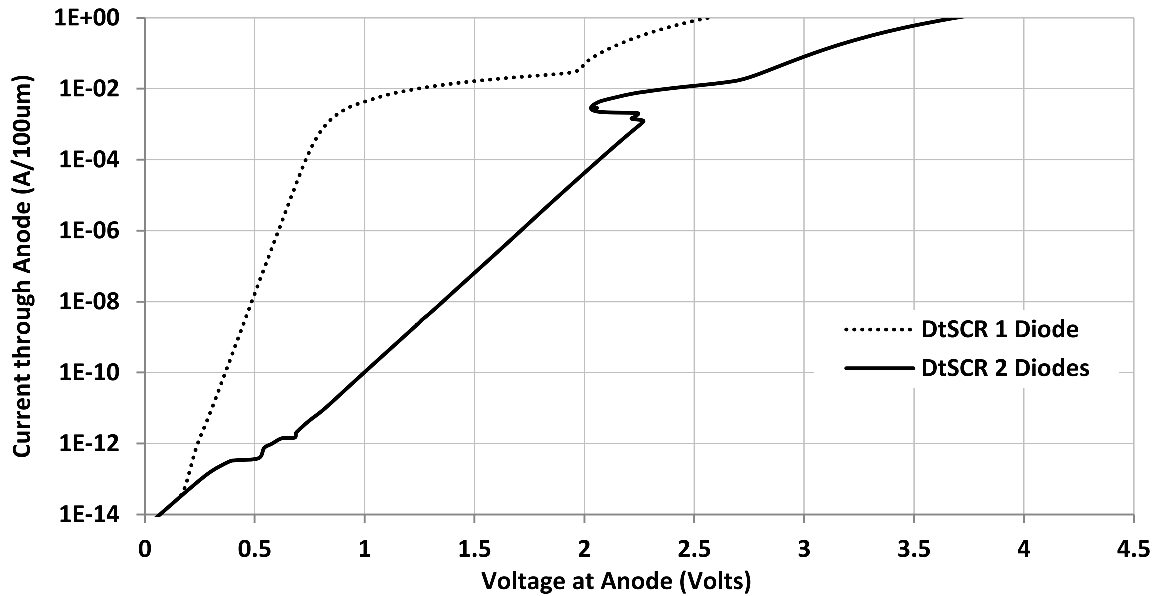


Figure 3-34: DtSCR I-V curves for one diode and two diode cases

3.10 Chapter Summary

In this chapter, the design flow and modeling results of various ESD devices are presented. Using parameters extracted from Cadence® and PTM, an NMOS and a PMOS with 65 nano-meter gate lengths are constructed in Sentaurus. They serve as the modeling foundation of the latter ESD

devices. From the NMOS and PMOS models, n^+, p^+, n-well, and p-substrate parameters are all defined. Combining diodes and SCR, a proposed diode-triggered SCR device is constructed. It has a low triggering voltage and leakage current, also a high holding voltage to avoid latch-up. The device characteristics of all models are summarized in **Table 3-6**. In this chart, all devices are constructed with a 100 micro-meters length.

Table 3-6: Device performance comparison

Device	V_{t1} (Volt)	V_h (Volt)	Leakage @1V	On-Resistance (Ohm)
GGNMOS	2.91	1.90	72.0 uA	0.31
SCR (Narrow)	12.1	1.10	0.11 pA	0.15
DSCR D=0.40	8.58	1.12	0.35 pA	0.44
DSCR D=0.30	4.61	1.13	0.35 pA	0.44
DSCR D=0.20	1.87	1.14	2.80 uA	0.44
DtSCR (2 Diodes)	2.26	2.05	0.10 nA	0.50

According to the performance chart, GGNMOS has good V_{t1} and V_h values; however its leakage is too high. The narrow SCR's V_{t1} and V_h performance is poor but the leakage and on-resistance are in good range. DSCR (D=0.3) is the best choice among various DSCRs, it has a good V_{t1} voltage, leakage; however a low V_h makes it susceptible to latch-up. DtSCR has exceptional performance on the aspects of V_{t1} and V_h, also, it has a leakage current one order of magnitude below 1 nano-Amp. These devices with different qualities are put to test in the ESD event simulations in Chapter 4.

Chapter 4 ESD Test Simulations

4.1 Figures of Merit

Using the devices constructed from Chapter 3, it is possible to conduct ESD test simulations. This chapter will elaborate the test bench setup and simulation results. A number of figures of merit are considered and compared for the purpose of evaluating different ESD protection devices. Those figures include:

1. Current sinking ability of HBM and CDM discharges. This is bench mark measurement of each device's capability in conducting ESD current. Since ESD events are manifested as a large amount of charges moving through the devices in a short period of time. Thus, the amount of current that devices can sink becomes a priority. For the purpose of comparison, the peak current is chosen as this figure. Then, a higher value of this figure indicates better current sinking ability of an ESD protection device.

2. Peak voltage overshoots. At the anode of ESD protection devices, there is parasitic capacitance. At the first few hundred pico-seconds of time, when ESD events occur, protection devices are not fully turned on. Then, there are charges accumulating on the parasitic capacitor which ramps up the voltage at the anode. This voltage overshoot is highly undesirable because a large voltage overstress can damage the gate oxide. Then, a low value of this figure indicates better ESD protection against voltage overshoots.

3. Complete ESD charge dissipation time. This figure is the measurement of how quickly ESD events can be completely dissipated by protection devices. When overstresses pass through protection devices quicker, ICs can be better protected from ESD damages. Then, a lower value of this figure indicates faster charge dissipation and thus better protection.

4. Leakage current under normal operation. This is an important evaluation of different ESD devices. An ESD event happens under a fraction of a second. However, during the IC's entire operational life cycle, the ESD devices are leaking current. When the leakage current is small, it provides high energy efficiency of the IC. Thus, a low value of this figure gives better leakage performance.

5. Capacitance at anode under different frequencies. All ESD devices are adding extra capacitance into the protected ports. As a verification criterion, the capacitance must not vary under different frequencies. Since the input/output signals can have different frequencies, the capacitance of the ESD devices can not cause distortion to the integrity of the input/output signals. Thus, when this figure does not vary with different frequencies, it indicates low disruption from ESD devices to the protected port.

6. Area consideration. The area of ESD devices varies with the design and protection level requirement. To compare this quality, the efficient use of area becomes a priority. Thus, the design that offers higher ESD protection characteristics among all devices with the same area wins.

These six criteria are the qualities to compare among various protection devices. To establish a justified conclusion, all devices are built to have the same area. Since most ESD devices are large in size, it is crucial to find out the efficiency of devices with respect to the same area. To decide this constant value of area, the device with the longest cross-sectional length, which is the DtSCR with 17 micro-meters, is set to 100 micro-meters in width. Thus, DtSCR's area becomes 1700 square micro-meters. All other devices are configured to have the same area. Their widths are charted respectively in **Table 4-1**.

Table 4-1: Device sizing to reach a common area of 1700 um^2

Device	Diode 2x	Diode 3x	SCR	DSCR	DtSCR
Cross-section length (µm)	8.7	13.0	7.0	11.0	17.0
Width (µm)	195.4	130.7	242.8	154.5	100
Area (μm^2)	1700	1700	1700	1700	1700

4.2 HBM Test setup and results

HBM is the most common ESD testing scheme. It depicts a charged human's finger touching a pin on the chip. The test is modeled as a pre-charged 100 pico-farad capacitor connected in series with a 1500 ohm resistor. The other lead of the resistor connects to ESD protection devices, which are labelled as DUT in **Figure 4-1**.

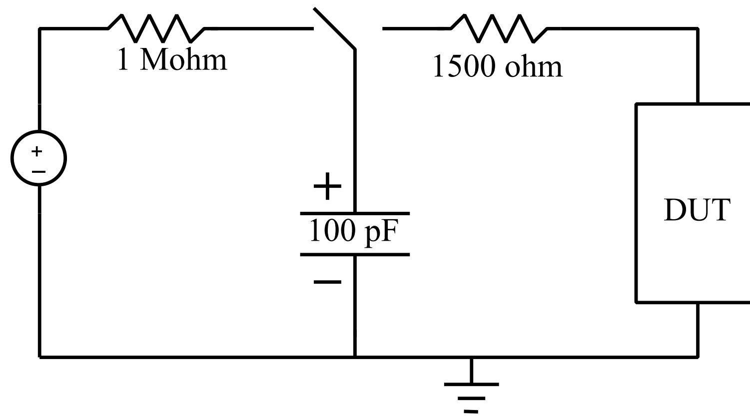


Figure 4-1: ESD event HBM modeling circuit specified by JEDEC standard, the switch controls the charging and discharging of the source capacitor

This test is conducted in the device simulator Sentaurus. However, Sentaurus does not have a proper "switch" component, which controls the charging and discharging of the capacitor, as seen in **Figure 4-1** above. A work-around is designed for this purpose. Instead of applying a DC voltage source in parallel with the capacitor, it is realized to use a pulsed voltage source in series with the capacitor shown in **Figure 4-2**. The reasoning is shown in the following equations.

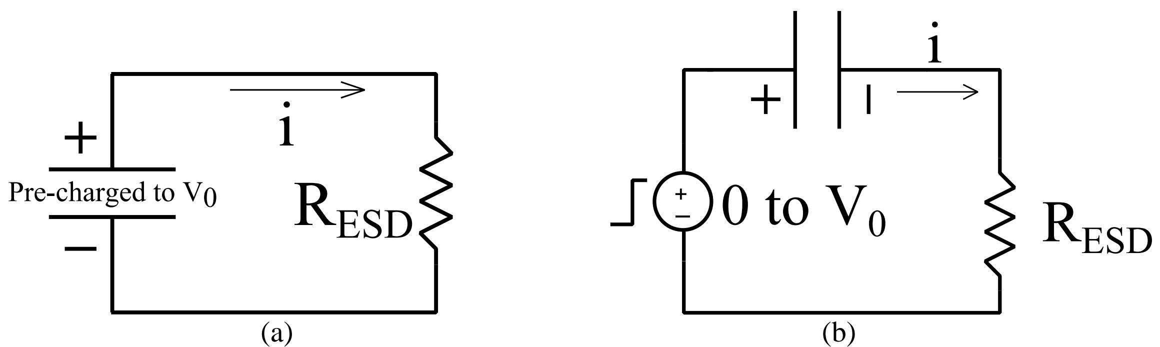


Figure 4-2: HBM theoretical test-bench (a) and work-around method (b)

In Figure 4-2, the ESD protection device (DUT) is modeled as a resistance R_{ESD}, thus, both circuits supply the same voltage at the R_{ESD}'s positive node (V_{ESD}). The capacitance is set to "C" and the voltage across it is set to "V_C". **Figure 4-2**a depicts a normal RC natural response which simulates the discharge of a HBM. Then, the result of V_{ESD} is shown as Equation 4-3.

$$\boldsymbol{i(t) = -C \times \frac{dV_C(t)}{dt}}$$ **Equation 4-1**

$$\boldsymbol{i(t) \times R_{ESD} = -V_{ESD}(t) = -V_C(t)}$$ **Equation 4-2**

$$C \times \frac{dV_C(t)}{dt} \times R_{ESD} = -V_{ESD}(t)$$

$$C \times \frac{dV_{ESD}(t)}{dt} \times R_{ESD} = -V_{ESD}(t)$$

$$\frac{dV_{ESD}(t)}{dt} = -\frac{V_{ESD}(t)}{C \times R_{ESD}}$$

$$\boldsymbol{V_{ESD}(t) = V_0 e^{-\frac{t}{R_{ESD} \times C}}}$$ **Equation 4-3**

Figure 4-2b is the work-around solution to function as the switch action of a normal discharging circuit. The voltage source is configured as a step-response pulse, which models a Heaviside function with the amplitude of V_0 [36]. Frequency domain and Laplace Transform are used to solve this circuit.

$$\boldsymbol{V_{IN} = \frac{V_0}{s}}$$ **Equation 4-4**

$$\boldsymbol{V_{ESD} = \frac{R_{ESD}}{R_{ESD} + \frac{1}{sC}} V_{IN}}$$ **Equation 4-5**

$$V_{ESD} = \frac{sCR_{ESD}}{sCR_{ESD} + 1} V_{IN}$$

$$V_{ESD} = \frac{sCR_{ESD}}{sCR_{ESD} + 1} \frac{V_0}{s}$$

After solving with partial fractions, the result of V_{ESD} is shown in Equation 4-6:

$$V_C = V_0 \left(1 - e^{-\frac{t}{R_{ESD} \times C}}\right)$$

$$\boldsymbol{V_{ESD} = V_0 e^{-\frac{t}{R_{ESD} \times C}}}$$ **Equation 4-6**

Both analysis give the same V_{ESD} results, it is concluded that the work-around depicted in **Figure 4-2**b can fulfill its purpose of simulating the natural response in **Figure 4-2**a. Then, this pulsed voltage method is applied to both the ESD device test benches, HBM and CDM.

Because there is no perfect pulsed voltage sources like a Heaviside function with zero rise time in the device simulator. A clocked signal with a very wide duty cycle and a small rise time is applied in Sentaurus. In the case of HBM 2 kV classification, a rise time of 1 nano-second is selected, since the actual voltage ramp time is 200 V/ns [37], which takes 10 nano-seconds to reach 2000V. To rule out the effect of the pulsed voltage source's influence on the actual discharge of the test bench, one order of magnitude is set as the margin to compensate the non-ideality. Thus, a 1 nano-second rise time for the voltage source to ramp from 0V to 2000V is decided. This method is also applied for the CDM modeling case.

The following sections will present the simulation results for different devices in HBM situations which include diode stacks, SCR, DSCR and DtSCR.

4.2.1 Non-Snapback device in HBM (Diodes)

A single diode cannot function as a ESD protection device as shown in Chapter 3. Stacks of diodes are exploited for their multiplicative turn-on voltage compared to one forward biased diode. This voltage must be 50 percent greater than the nominal voltage of 1.0V in order for the nominal condition to operate without false triggering the ESD discharge event [30]. Therefore, at least 2 stacks of diodes should be arranged as shown in **Figure 4-3**a.

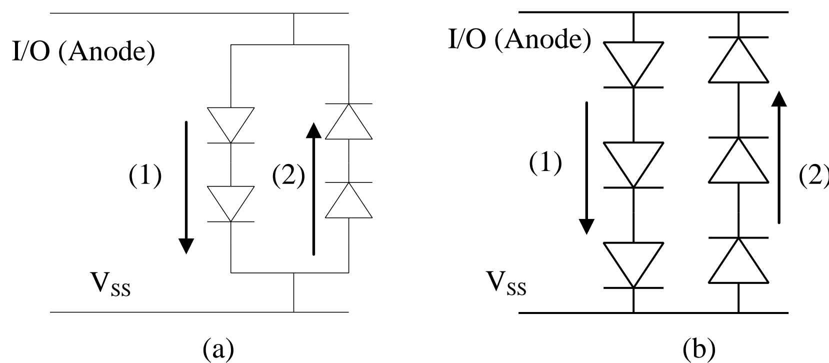


Figure 4-3: 2x diodes and 3x diodes circuit configurations

When diodes are connected in this method, they can conduct in either direction. The two branches can handle the ESD discharge from I/O port or V_{SS}, which are PS and NS discharge mode. Using this configuration, branch (1) will be capable of conducting the current when PS ESD event occurs. On the other hand, branch (2) can allow current to flow through when NS ESD event happens. From the simulation in Sentaurus®, the Current vs. Voltage responses of the 2 and 3 diodes configurations are depicted in **Figure 4-4**.

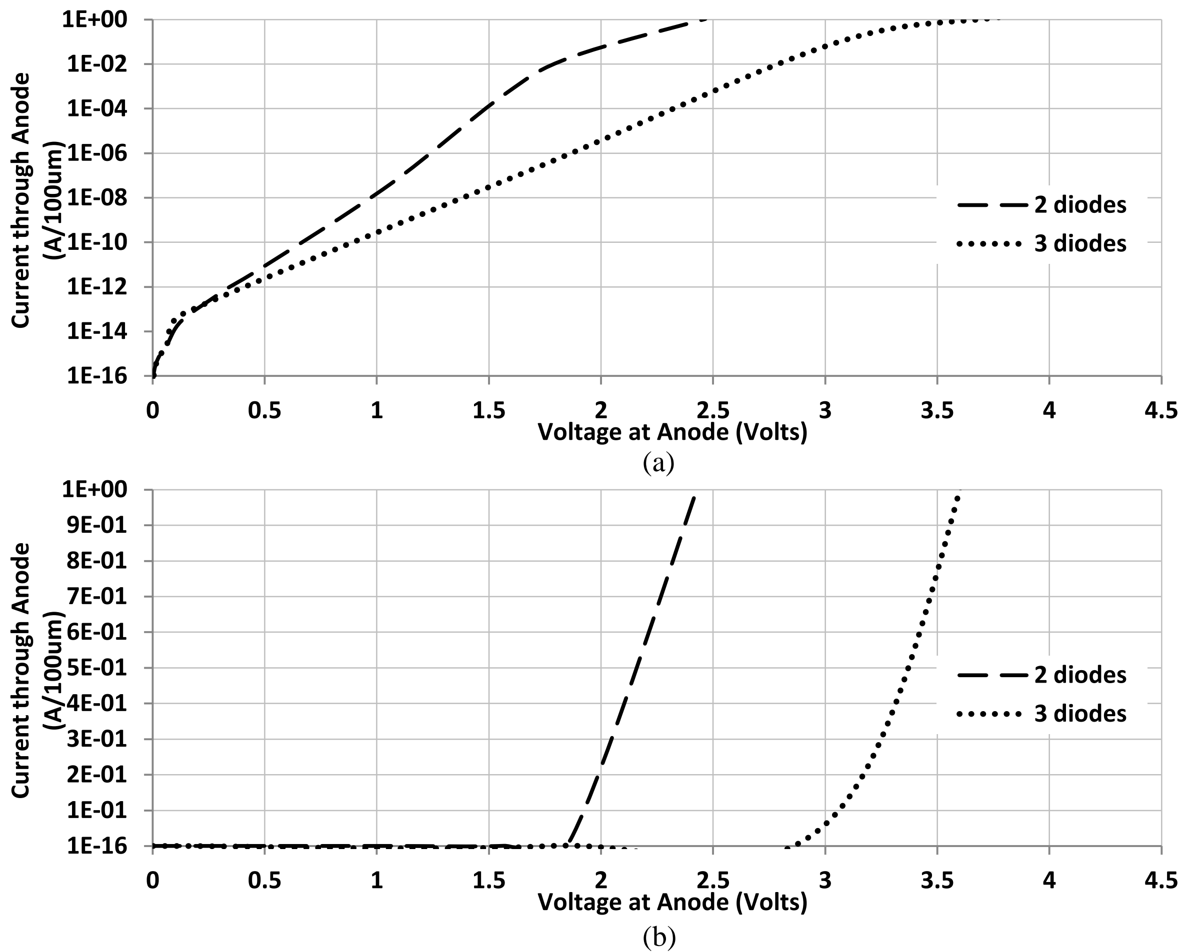


Figure 4-4: I-V curves of 2x and 3x diodes (a) log scale (b) normal scale

From the results in **Figure 4-4**, it is seen that 2 stacks of diodes possess the advantage of lower turn-on voltage. However, it suffers from a large amount of leakage current at 1.0V. This current is reaching 40 nano-Amps compared to the 0.23 nano-Amps of the 3 stacks of diodes configuration.

From this simulation, it rules out the possible use of 2 stacks of diodes in I/O ESD protection due to its high leakage current.

Then, a HBM test with PS mode is conducted to test the ESD performance for diode configurations as shown in **Figure 4-5**.

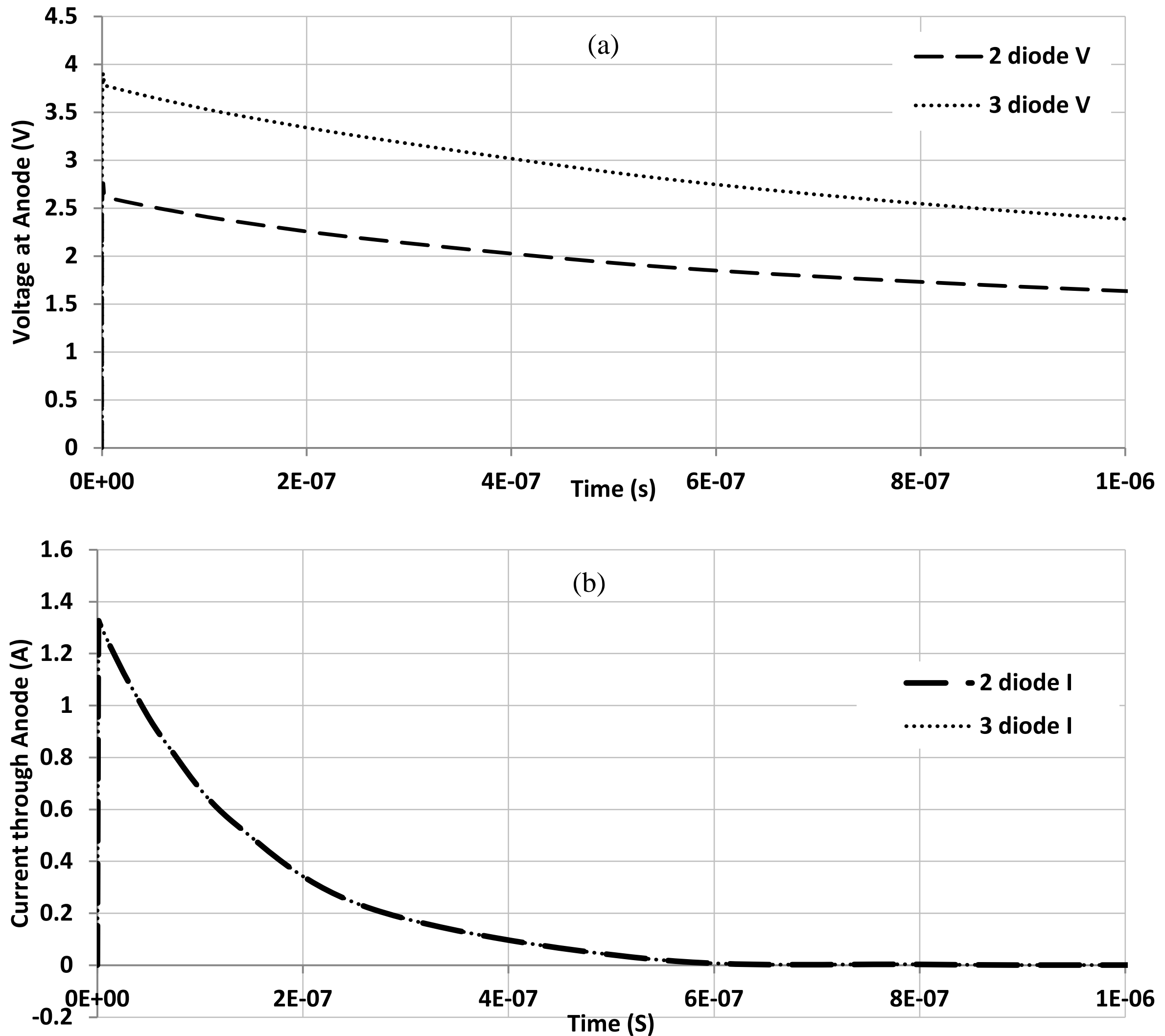


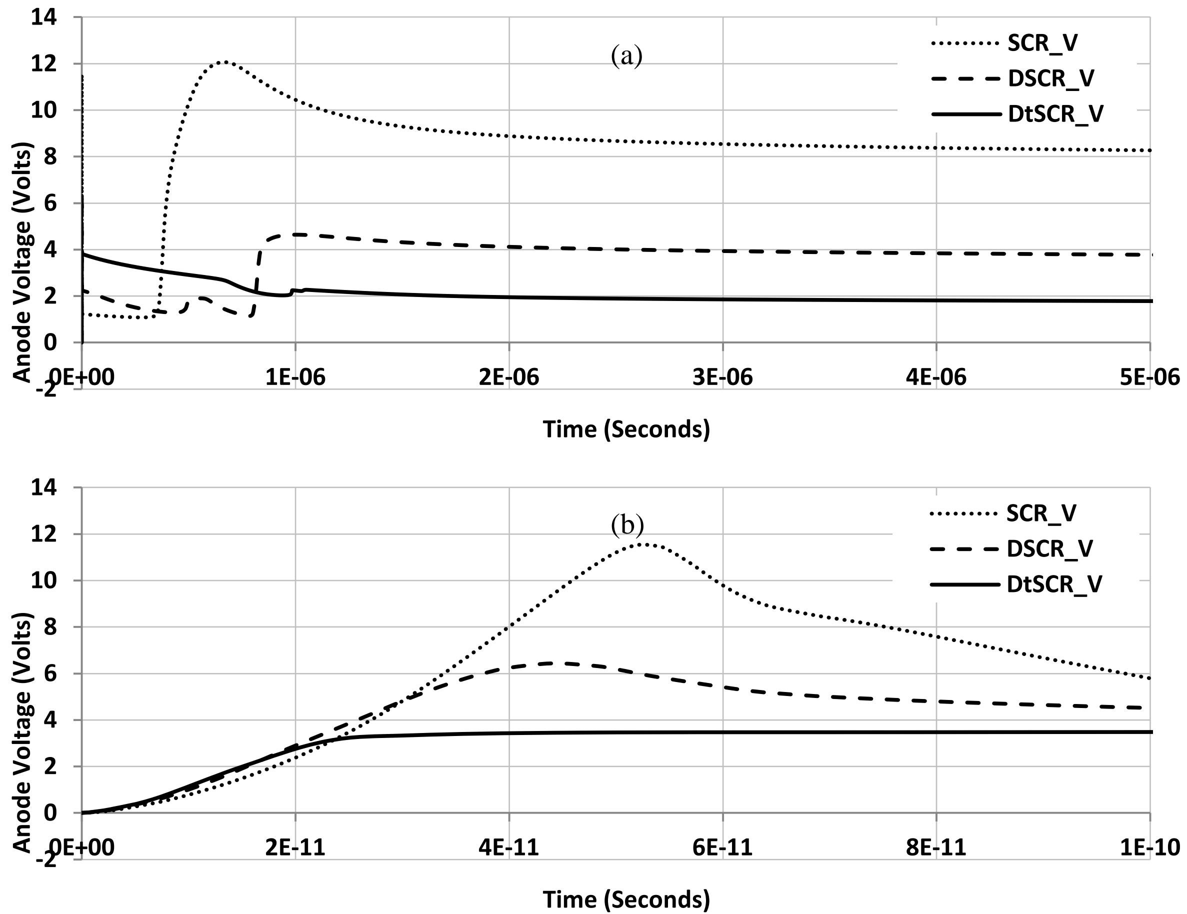
Figure 4-5: Voltage and current responses of 2x diodes and 3x diodes (a) Voltage (b) Current

From the simulation results, it is seen that a voltage overshoot lasts for 1 nano-second time. This is caused by the very rapid voltage rise $\frac{dV}{dt}$ at the anode side [38]. When the human body model is discharging to the anode, the parasitic capacitance at the node will accumulate charges initially, thus forming an overshoot voltage, which correlates to the discharging speed of the ESD protection device. The more the capacitance per area it is, the slower the device can discharge. When the device

can allow current to pass through more rapidly, the accumulation of charges will not build up to a level that is harmful to the I/O transistor's gate oxide which is sensitive to both current overdose and voltage overshoot.

4.2.2 Snapback devices (SCR, DSCR and DtSCR)

The following diagrams in **Figure 4-6** are the HBM simulation results of SCR, DSCR and DtSCR devices under the same test bench as the diodes. From the simulations of these snap-back devices, a second overshoot phenomenon happens.



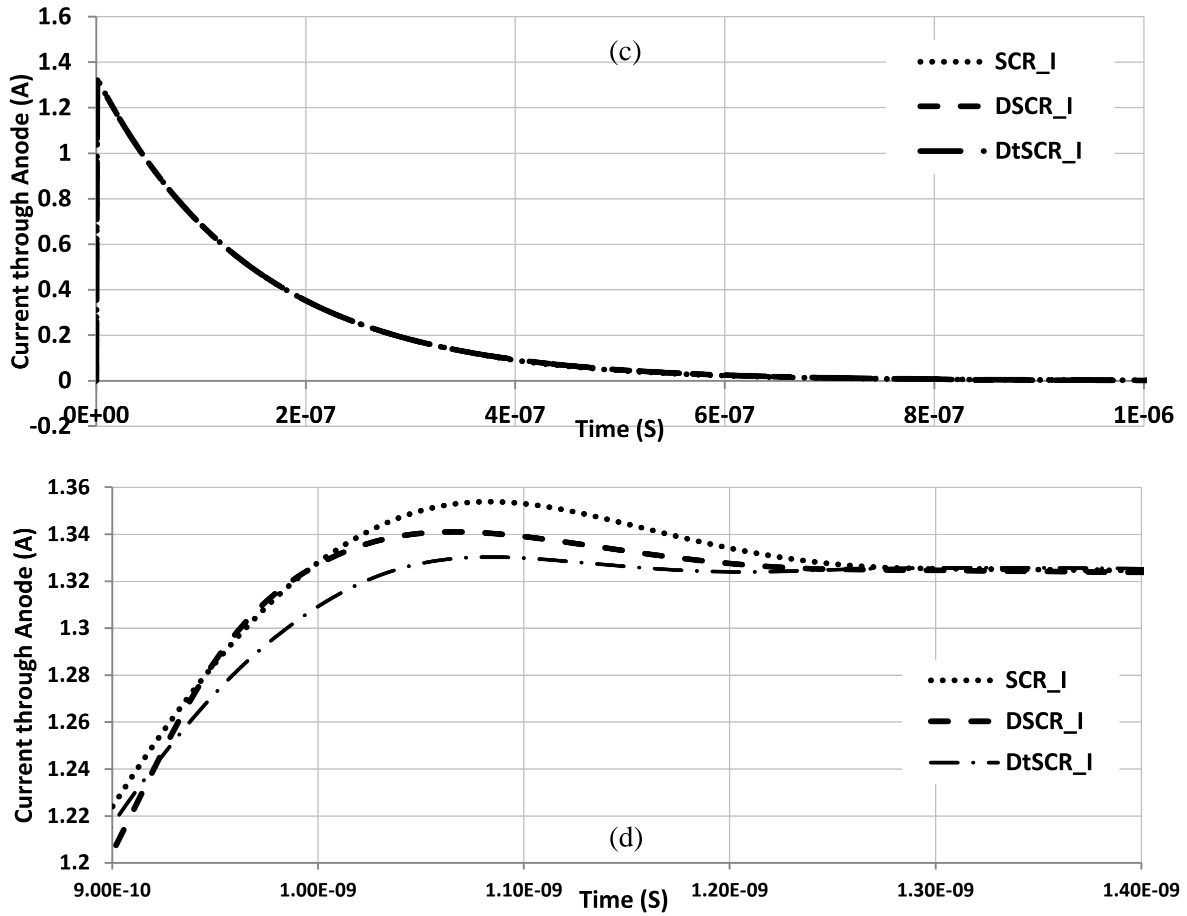


Figure 4-6: Snapback devices HBM voltage (a) (b) and current (c) (d) responses

From **Figure 4-6**a, it can be seen that the devices experience two voltage overshoot events in a 1 micro-second time frame. During the first 100 pico-seconds shown in **Figure 4-6**b, all three devices reach their first voltage peak. This high peak value is expected due to the rapid rise of the ESD impulse voltage from 0 to 2 kV in 1 nano-second. Because the devices require time to turn on and start to sink the current, once they start, it is seen that the voltages begin to drop and the current start to rise rapidly. Also, it is confirmed from the figures that DtSCR has the shortest reaction time, i.e. it does not reach a high overshoot voltage like the SCR or DSCR. DtSCR triggers at 30 pico-seconds, while the SCR triggers at 50 pico-seconds.

After a few hundred nano-seconds, the second voltage overshoot is observable on the SCR and DSCR devices. This “snap-up” happens during the latter stage of the HBM discharge event [33]. The reason behind this phenomenon is that when the discharge current falls below the holding current

of the device, the parasitic BJT transistors will enter saturation mode, which has high impedance. Thus, it results in another voltage rise. This phenomenon is also confirmed by Di Sarro et al [33]. Due to the sustained DC-like high voltage after the "snap-up", the IC has more possibility to be damaged.

The following figures in series as shown in **Figure 4-7** are the electrostatic voltage (left column) and total current density (right column) plots of a SCR at time equals 50 ps, 100 ps, 200 ps, 1ns, 350 ns, 400 ns and 1 us. The red color indicates higher potential or current density.

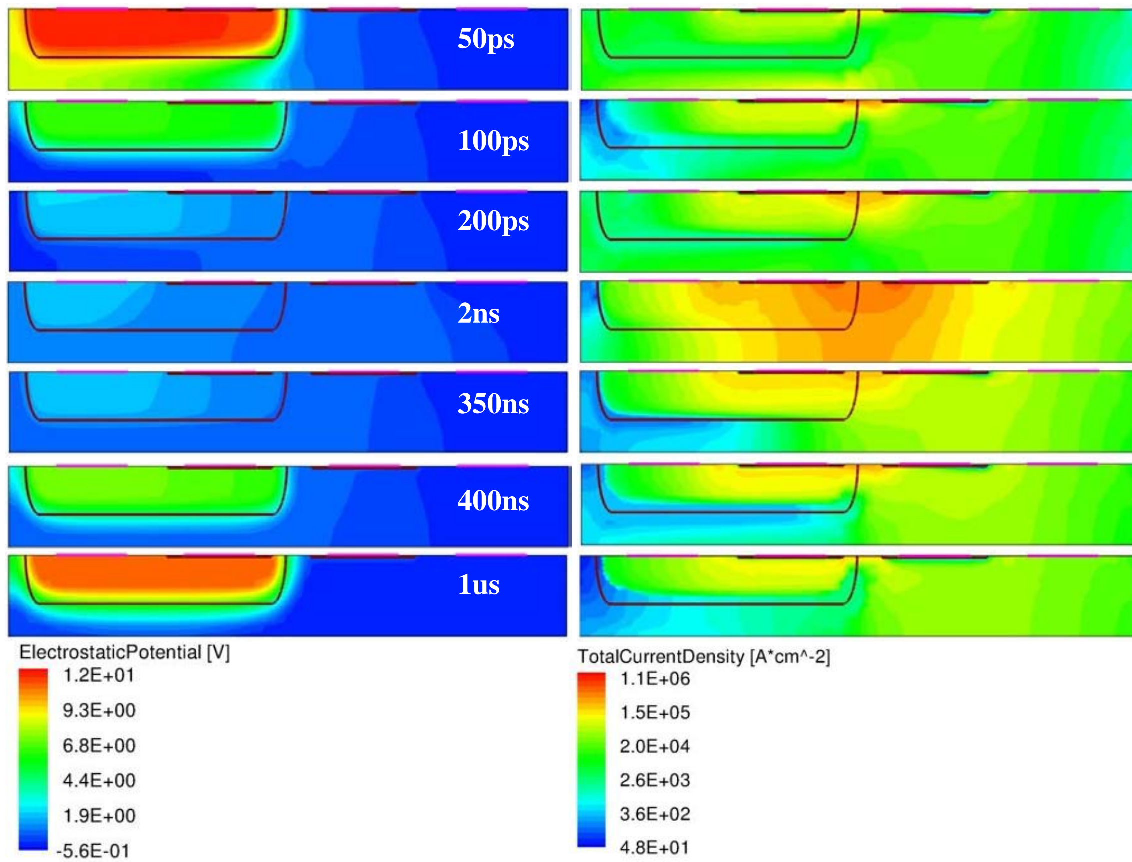


Figure 4-7: Electrostatic voltage (left) and total current density (right) vs. Time for SCR HBM responses

From **Figure 4-7**, it is seen that at 50 pico-seconds, which is the time that the first peak overshoot voltage happens, the anode has accumulated enough charges and the voltage has reached close to 12V. This is demonstrated as the red n-well zone in the electrostatic potential diagram in **Figure 4-8**. At this point of time, the impact ionization due to avalanche breakdown has happened enormously between the n-well and p-substrate boundary.

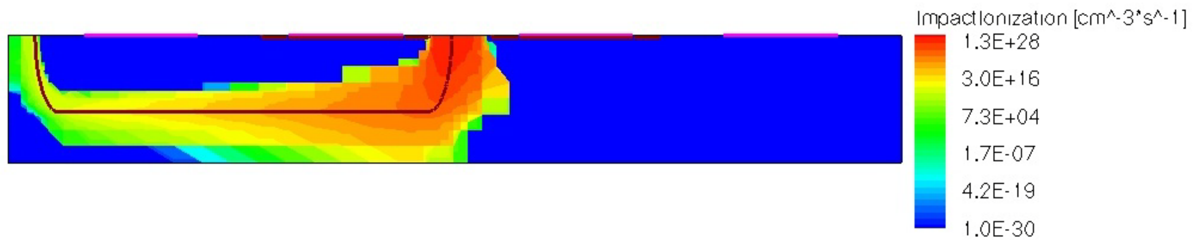


Figure 4-8: Impact ionization of SCR at 50 ps

Then, at 100 pico-seconds, the *npn* transistor formed between n-well/p-sub/n^+ starts to conduct current. This is verified in the total current density diagram (Time=100ps). At the same time, the voltage at the anode drops to around 6V due to charge dissipation.

When the time goes on, the conduction becomes increasingly significant. At Time=2ns, the conduction area becomes very large, as depicted by the large red color profile contour in the total current density diagram (Time=2ns). During this turned-on mode of SCR's operation, it allows a large amount of current to pass through without needing a high anode voltage. This is verified on the electrostatic potential diagram of Time=2ns, which shows the anode voltage is below 2V.

After 350 nano-seconds, when the majority of the ESD overstress has been sunk through the SCR, the *npn* conduction current starts to reduce. As shown from the profile contour, the region becomes less red. When the current drops to the value that it cannot facilitate itself from keeping the *npn* transistor in the active region, the current flow path is cut off. At this moment, SCR starts another cycle of accumulating charges at its anode and snaps back when reaching the triggering point.

From the Time=1us diagrams, it is seen that the voltage at anode rises to more than 10V for the second time and the current flow path between the n-well and p-substrate is almost invisible.

The repeated voltage overshoots and the sustained high DC voltage after the second overshoot will harm the IC. When comparing all devices, DtSCR has a low triggering voltage, and its anode does not experience a high "snap-up" for the second time. The decaying anode voltage is almost as smooth as diode configurations.

The following figures of merit shown in **Figure 4-9** are (a) first overshoot voltage (b) second overshoot voltage (c) peak current achieved and (d) 90% current dissipation time of the four devices for comparison, 3x diodes, SCR, DSCR and DtSCR.

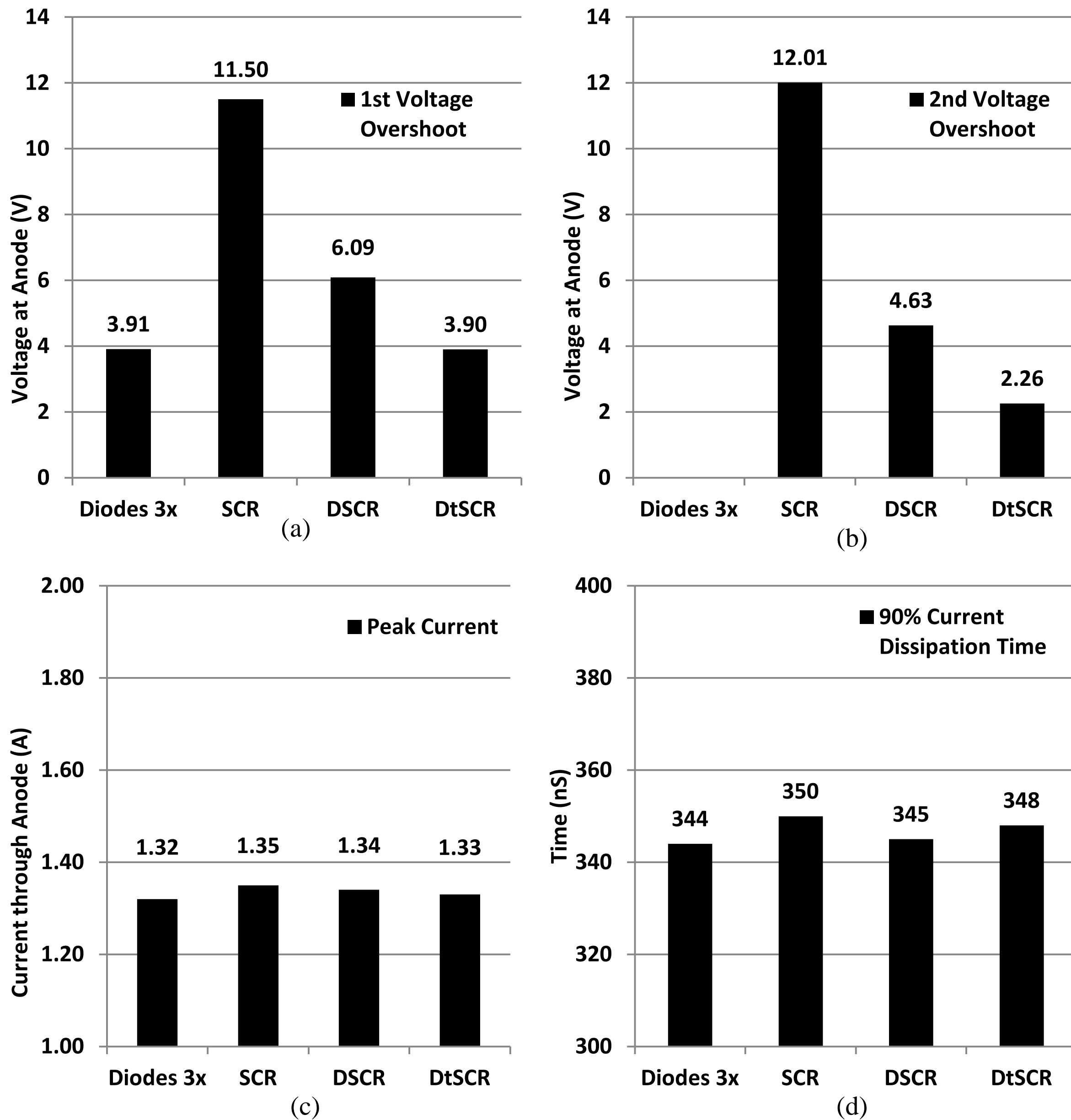


Figure 4-9: Figures of merit comparison

From the overall performance of these devices, it is concluded that their abilities to sink current is equivalent under a 2 kV HBM test bench, when each device is occupying the same area on chip. Their peak currents are all around 1.33A. Meanwhile, the response time, which is the time that the current reaches its maximum value, is under 1.1 nano-seconds for all devices. Since their current-

sinking behaviours are identical, the time to dissipate 90 percent of the peak current is very comparable. All devices take around 345 nano-seconds to drop to 10 percent of the peak current.

From chart (a) it is seen that the first voltage overshoot is comparable to the second voltage overshoot peak. The first overshoot time duration is very short, the peak diminishes in less than 100 pico-seconds [39]. Therefore, the damage that the first voltage overshoot can do to the protected IC is limited. The sustained DC-like voltage after second voltage overshoot happens is destructive to the chip. In **Figure 4-6**a, it is seen that after 10 micro-seconds, SCR is still holding more than 8V, and DSCR is holding close to 4V. This situation is caused by the low current conduction in the snapback devices, thus, making the anode charges not sunk to the cathode.

In summary, among all devices with the same area, the difference is observed. From the SCR performance in (a), it is seen that the first voltage overshoot peak reaches 11.5V, and the second voltage peak is 12.01V. These voltages are too high for the processing technology to handle. For the DSCR, the voltage performance is not meeting the desired values as outlined in Chapter 1. From figure (c) and (d), it is seen that the maximum current sinking capability and current dissipation time is comparable among devices, the variation is less than 1 percent.

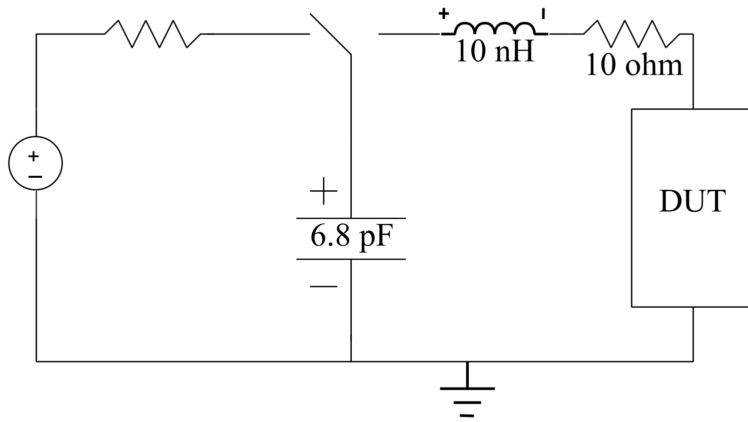
From the comparison above, it is concluded that the 3x diode configuration, and DtSCR can handle a 2KV HBM ESD event with low overshoot voltage (less than 5V [18]), comparable current sinking ability and dissipation time.

The conclusion for HBM testing is that **3x diode** and **DtSCR** can meet the voltage and current requirements when area is held constant.

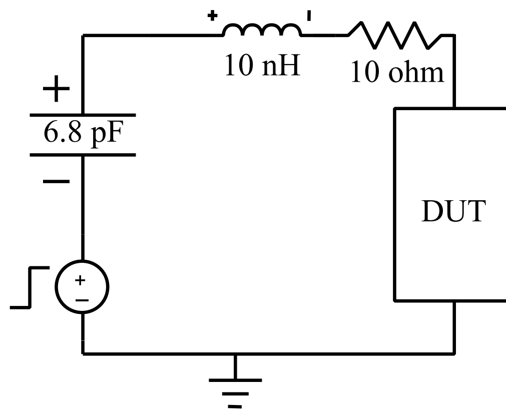
4.3 CDM Test Setup and Results

CDM failures constitute more ESD damages beyond the HBM. CDM simulation is a vital component to facilitate the understanding of device behaviours under CDM test conditions, which are stricter, compared to HBM.

Applying the same technique as the HBM test setup, the CDM test bench is depicted in **Figure 4-10**. (a) is the desired test bench and (b) is the work-around method.



(a)



(b)

Figure 4-10: CDM test-bench (a) and work-around method (b)

The capacitor value is decided as 6.8 pico-Farads, which resembles a small packaging capacitance according to the JEDEC standard, the inductor is chosen as 10 nano-Henrys, and the resistor is 10 Ohm [2] [12]. In the JEDEC standard, the pogo pin used to discharge the capacitor is 1 Ohm. In reality, the phenomenon happens when the charged chip package is brought close to a grounded conductor. When the distance between these two objects is decreasing, the charges on the chip will arc through the thin air. This arcing behaviour has a relevant resistance. According to several publications [40] [41], this resistance varies from a few ohms to tens of ohms. In this simulation work, it is chosen at 10 ohm for all devices to perform parallel comparison in accordance with other research parties.

CDM Class A (100V) standard is applied in this simulation work. According to the standard, the rise time of the current is 100 ~ 500 pico-seconds. The peak current is in the 1~3 Amps range [42]. Thus, the rise time of the voltage source is also applied in the same method as the HBM simulation, which is one tenth of the actual rise time. JEDEC states that the fastest rise time is 100 pico-seconds. Then, 10 pico-seconds' time is defined in the simulator to rule out the effect of the pulsed source, which can bias the results from the device behaviour. The choice of 10 pico-seconds' rise time also leaves possible design margin, since this rise time value is the tightest criterion in the JEDEC standard, which defines the range of 100 ~ 500 pico-seconds. The real world current rise time is not as short as this simulation.

From the CDM test-bench, it is seen that the charge on the capacitor travel through an inductor and a resistor. Thus, this path produces an RLC oscillation for both the voltage and current responses. The constructed devices are only capable of sinking the current through PS mode. Therefore, it is needed to add another discharge branch to take care of the NS mode, which allows the current to pass from V_{SS} to I/O port.

From the discussion in Chapter 3, it is reasonable to choose stacks of diodes again for this purpose as shown in **Figure 4-11**. Because I/O port has a higher voltage than V_{SS} except when the logic is in low state, in that case, I/O voltage is the same as V_{SS}. As a result of normal chip operation, the diodes are reverse biased for most of the time and give a very low capacitance. Moreover, diodes possess a proven ESD protection performance. This has been verified by the HBM simulations in the previous section.

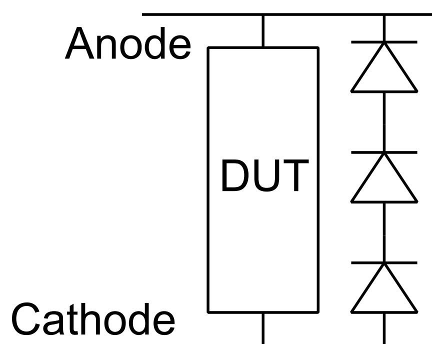


Figure 4-11: DUT with NS protection diodes

For simulation purposes, the diode stacks are set to the same area and then attached in parallel with the ESD devices.

The goal of the design is to sink large current and maintain a low voltage overshoot. There is no foundry guideline on the voltage overshoot tolerance with respect to different gate oxide thickness or technology node. Then, from a recent publication (March 2012) on experiments conducted with 65 low-power nano-meter technology, it reports the lowest simulated and measured voltage overshoot is **6.3V** without device failures [43]. Thus, this result is used as a bench mark for the simulation conducted in this research work.

Figure 4-12 demonstrates the voltage and current transient simulation results for 3x diodes, SCR, DSCR and DtSCR.

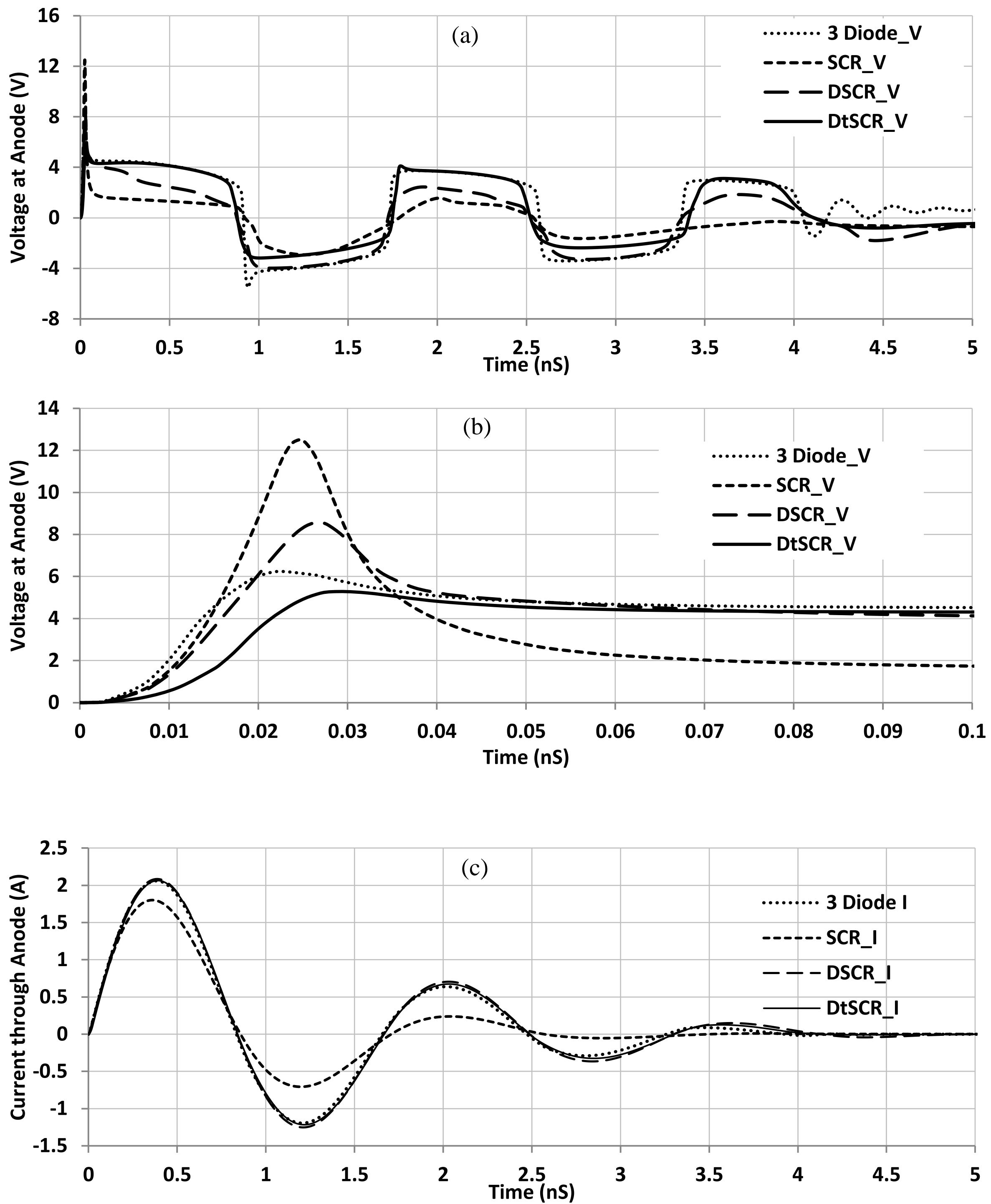


Figure 4-12: CDM test results of four devices (a) voltage vs. time plot of a 5 ns duration (b) voltage vs. time plot of a 0.1 ns duration and (c) current vs. time plot of 5 ns duration

Figures of merit shown in **Figure 4-13** are derived from CDM simulation results, (a) depicts the first voltage overshoot values, (b) indicates the maximum current sinking capability among devices, and (c) demonstrates the time it takes for the devices to sink 90% of the maximum current.

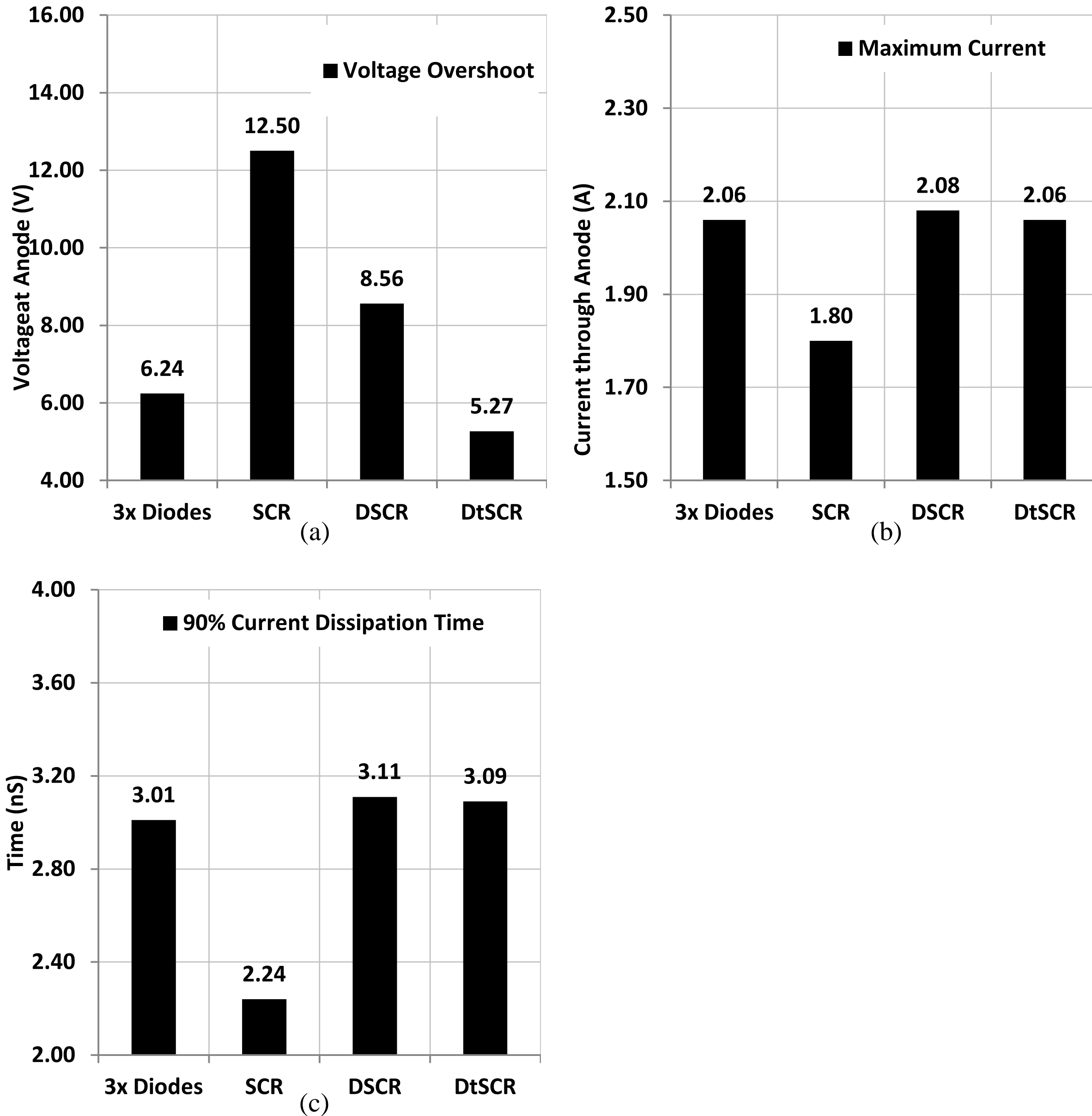


Figure 4-13: Figures of merit for CDM tests

It is seen that among all the devices with the same area, the DtSCR has the lowest voltage overshoot value of 5.27V, with comparable current sinking ability of 2.06A and dissipation time of

3.09 nano-seconds. The 3x diode configuration has similar performance on the maximum current and dissipation time; however its overshoot voltage 6.24V is a small amount higher than the DtSCR. Both of these two device configurations have demonstrated excellent CDM capabilities in comparison with the reported results [43].

4.4 Capacitance Approximation

The capacitance of these ESD devices also contributes to several aspects such as the overshoot voltage peak and the extra input capacitance the I/O port. Therefore, it is required to estimate the capacitance from the device simulators.

An ESD device can be modeled as a capacitor and a resistor in parallel [2] shown in **Figure 4-14**.

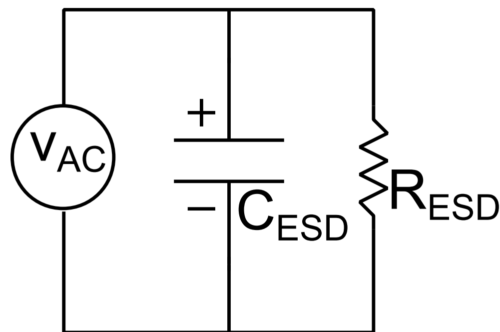


Figure 4-14: Capacitance estimation schematics

The AC input source has a DC voltage component and also a sinusoidal voltage source superimposed onto it. In order to simulate the actual operational circumstance, a sine wave with a DC offset of 0.8V and amplitude of 0.2V is used. Therefore, the highest signal is 1.0V and the lowest signal is 0.6V. These voltages represent the logic high and low states. The calculation of capacitance is described as follow:

$$v_{AC} = V + Asin(\omega t)$$

The current through the ESD device has two paths, the capacitor and the resistor. The current through the capacitor is:

$$i_C = C\frac{dv_{ESD}}{dt} = C\frac{dv_{AC}}{dt} = C\frac{d[V+Asin(\omega t)]}{dt}$$

$$i_C = C\frac{d[Asin(\omega t)]}{dt} = CA\omega\cos(\omega t)$$

The current through the resistor is:

$$i_R = \frac{v_{AC}}{R} = \frac{V}{R} + \frac{Asin(\omega t)}{R}$$

Thus, the total current is:

$$\boldsymbol{i_{TOTAL} = i_C + i_R = \frac{V}{R} + \frac{Asin(\omega t)}{R} + CA\omega\cos(\omega t)}$$ **Equation 4-7**

From the total current equation, it is seen that the overall current flowing into the ESD device is also a sinusoidal waveform with the same frequency as the input voltage source. Thus, at its peak value, the derivative of the current i_{TOTAL} is zero.

$$\frac{di_{TOTAL}}{dt} = 0$$

$$\boldsymbol{\frac{di_{TOTAL}}{dt} = \frac{A}{R}\omega\cos(\omega t) - CA\omega^2\sin(\omega t) = 0}$$ **Equation 4-8**

From Sentaurus® simulations, the total current can be obtained, and then with the two equations 4-7 and 4-8, capacitance of the ESD devices can be calculated.

Since the I/O port may have signals coming in at different frequencies, it is important to verify that the capacitance does not vary with frequency. Then, by applying different frequencies to the various devices, the capacitance is presented as in **Table 4-2** below.

Table 4-2: Capacitance chart of devices at different frequencies

Device \ Capacitance @	1 MHz (fF)	10 MHz (fF)	100MHz (fF)	1 GHz (fF)
3x Diodes	201	202	201	200
SCR	358	360	360	360
DSCR	645	650	648	650
DtSCR	403	400	405	401

For all the devices, the capacitance does not exhibit strong dependency on frequency, which is a highly desirable quality. It is has shown that for the same device area, diode stacks contain the lowest capacitance.

Since DtSCR has the best overall performance in ESD tests from HBM and CDM simulations, it logical to modify its structure to reduce its anode capacitance.

4.4.1 Capacitance Reduction of DtSCR

Anode capacitance influences the circuit in operational mode because more capacitance will slow down the rise time of a logic high signal. Therefore, it is logical to pursue a solution that reduces the anode capacitance when the chip is powered on.

Shown in **Figure 4-15** below, which is a cross-section view of the DtSCR's anode region, the n^+ and p^+ are originally connected together as the anode. When the two active diffusions are separated with the p+ connected to anode, and n+ connected to V_{DD}, that will bring the n+ and subsequently the entire n-well voltage to a constant 1.0V during normal operation [34]. Thus, this makes the anode p^+ diffusion always in reverse bias mode. The equation of p-n junction capacitance is shown below. When V_a is a reverse voltage, C_j becomes smaller.

$$C_j = \frac{\varepsilon_S}{w} = \sqrt{\frac{q\varepsilon_S}{(\phi_i - V_a)} \frac{N_a N_d}{N_a + N_d}} \qquad \textbf{Equation 4-9}$$

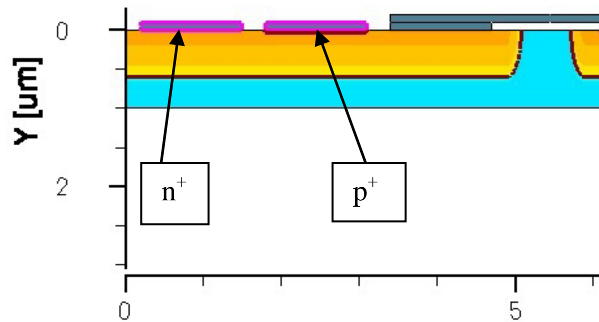


Figure 4-15: Anode cross-sectional view of a DtSCR

Capacitance simulation in Sentaurus is conducted again. The new DtSCR with n-well pulled high demonstrates 240 fF capacitance when the V_{DD} is at 1.0V. This method has reduced the anode capacitance by 40 percent.

One advantage of this modification is that between I/O and V_{DD}, there is a p-n junction formed by the p^+ diffusion and n-well/n^+. This diode is formed by the n-well pulled high scheme;

thus, the PD ESD event can be discharged using this p-n junction without adding additional protection devices.

Repeated simulations of ESD test-benches (HBM and CDM) are conducted again. The results are not varied by this modification. Thus, this n-well pulling high method does not compromise the ESD performance.

4.5 Latch-up Setup and Simulation

Latch-up is an important consideration of chip's operation. In this case, ESD protection devices cannot induce latch-up events. From the JEDEC standard [44], it has the specifications outlined as shown in **Figure 4-16** and **Table 4-3** below.

In the proposed design of DtSCR, due to the pulled high n-well, it is crucial to verify the latch-up events that are caused by a voltage/current spike that is between I/O port and V_{DD}.

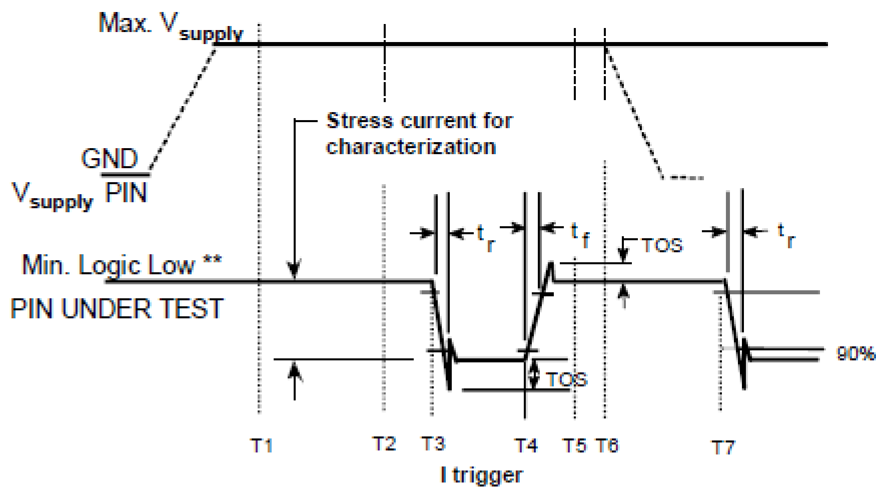


Figure 4-16: Latch-up waveform specifications specified by JEDEC **[44]**

Table 4-3: JEDEC Latch-up specifications

Symbol	Time Interval	Parameter	Limits	
			MIN	MAX
T_r		Trigger rise time	5 µs	5 ms
T_f		Trigger fall time	5 µs	5 ms
T_{width}	T3 to T4	Trigger duration	2x T_r	1 s
TOS		Trigger over-shoot	+/- 5% of pulse voltage	
T_{cool}	T4 to T7	Cool down time	>= T_{width}	
$T_{measure}$	T4 to T5	Wait time before measuring	3 ms	5 s

To supply a nominal voltage of 1.0V at V_{DD} and I/O, two separate power sources are used. Thus, a current source is placed in parallel with the I/O voltage source to inject the 50 mA current [44]. To make sure that all current is pumped into the device instead of the voltage source, a large resistor is placed in series with the I/O voltage source. In this case, a 10 Mega-ohm resistor is used for this purpose. The schematic of latch-up test and the simulation results are demonstrated in **Figure 4-17** and **Figure 4-18**.

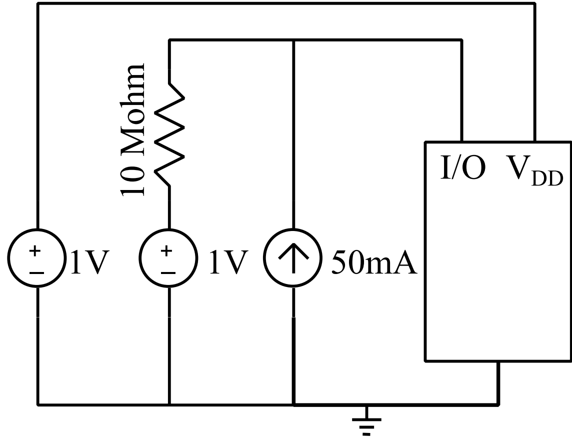


Figure 4-17: Latch-up test-bench in device simulator

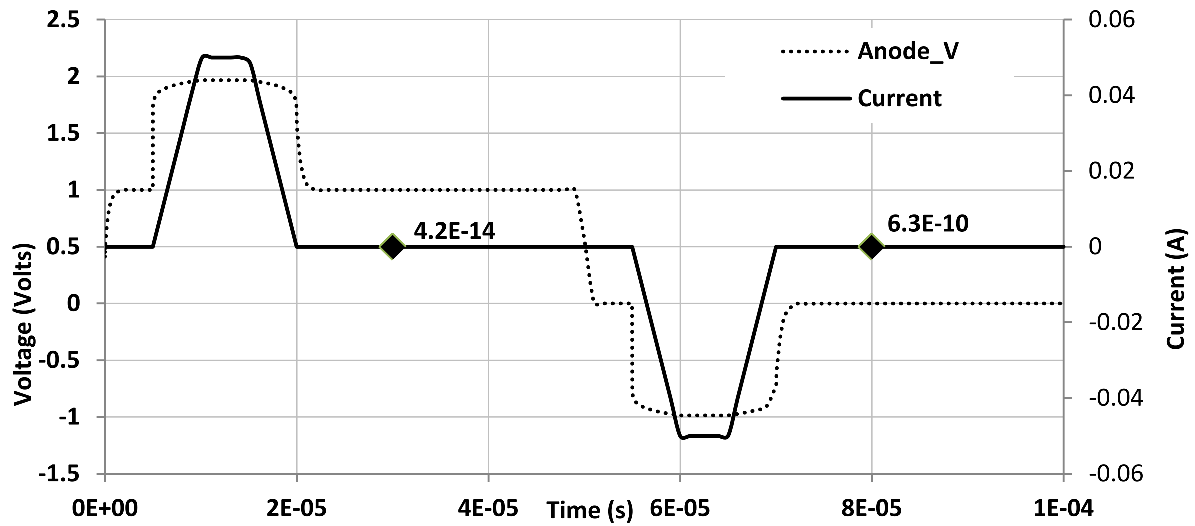


Figure 4-18: Latch-up simulation results

From the figures above, it is seen that the current falls below 1 nano-Amp at 3 ms and 8 ms $T_{measure}$ points. This has proven that the device is immune to latch-up from either a positive or negative current pulse. On real chips, latch-up is a system level event that has many influential factors. The layout of all components is an important contributor. Due to the limitation of this research, chip level latch-up is beyond the scope and thus not investigated.

4.6 Conclusions of Figures of Merit

The conclusions of figures of merit are presented in **Table 4-4**. In this chart, all the devices have the same size of 1700 um^2. The figures that are clear winner of several categories are shaded.

Table 4-4: Overall figures of merit comparison chart

	3x Diodes	SCR	DSCR	DtSCR
HBM Peak Current (A)	1.32	1.35	1.34	1.33
HBM 1st Overshoot Voltage (V)	3.91	11.5	6.09	3.90
HBM 2nd Overshoot Voltage (V)	X	12.01	4.63	2.26
HBM Current Dissipation Time (ns)	344	350	345	348
CDM Peak Current (A)	2.06	1.80	2.08	2.06
CDM Overshoot Voltage (V)	6.24	12.5	8.56	5.27
CDM Current Dissipation Time (ns)	3.01	2.24	3.11	3.09
Leakage	0.23nA	0.27pA	0.54pA	0.10nA
Capacitance (fF)	201	360	650	402 (240)

It is concluded that DtSCR and 3x Diodes have comparable performance regarding HBM events. In CDM events, DtSCR demonstrates a lower overshoot voltage of 5.27V. For the leakage current, both devices are under 1 nA, however, DtSCR has less than half of the 3x diode leakage. For anode capacitance, the diodes are the best performer with 201 fF, n-well-high DtSCR comes close with 240 fF, and both of them out-perform the SCR and DSCR by a wide margin.

4.7 Overall Protection Scheme

From the concluded figures of merit above, an overall protection scheme is proposed to utilize the advantage of both diode strings and DtSCR. The PS ESD stress is taken care of by the DtSCR, which has the advantage of low leakage, low triggering voltage and high holding voltage. The PD ESD stress is also handled by the pulled-high n-well. NS and ND modes are protected by 3 serial diode strings as shown in **Figure 4-19**.

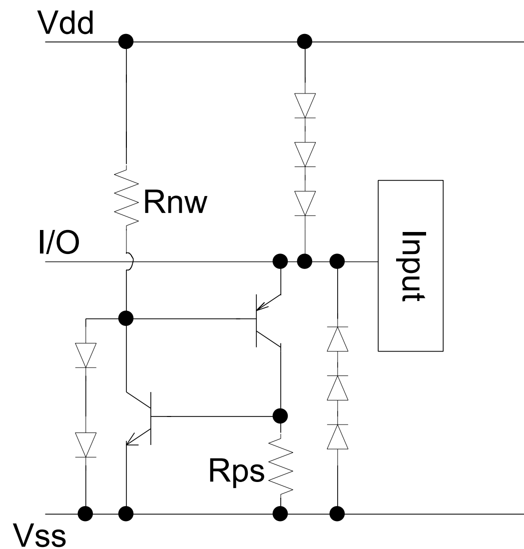


Figure 4-19: Final protection scheme utilizing DtSCR and diode strings

This n-well pulled high DtSCR device can handle 2 kV HBM and 100V CDM ESD events with low overshoot voltage and high current sinking capability. At the same time, it possesses a comparable anode capacitance similar to diodes, which shows 240 fF on a 1700 square micro-meters device with diodes being 200 fF. It is also immune to latch-up or false triggering according to the simulations in section 4.5.

The simulation results of four different modes of ESD events are concluded in **Table 4-5** below.

Table 4-5: Overall protection scheme performance regarding four different ESD discharging modes

I/O port ESD event modes	PS	PD	NS	ND
Protection device	DtSCR	DtSCR's n-well	3x diode string	3x diode string
HBM 2kV current	1.33A	1.33A	1.32A	1.33A
HBM 2kV voltage overshoot	3.90V	1.10V	3.91V	3.91V
CDM 100V current	2.06A	2.06A	2.06A	2.06A
CDM 100V voltage overshoot	5.27V	2.21V	6.24V	6.24V

From the results in **Table 4-5**, it can be seen that all four possible ESD discharge modes are protected by the proposed scheme, which passes the HBM 2kV and CDM 100V classifications.

After placing this protection scheme to test with an actual 1 GHz I/O signal shown in **Figure 4-20**, it is seen that the ESD structures settle below 1 nano-Amp in less than 0.2 nano-second of the signal reaches its designated values. This simulation result has verified that the ESD protection scheme does not influence the normal operation of the I/O ports.

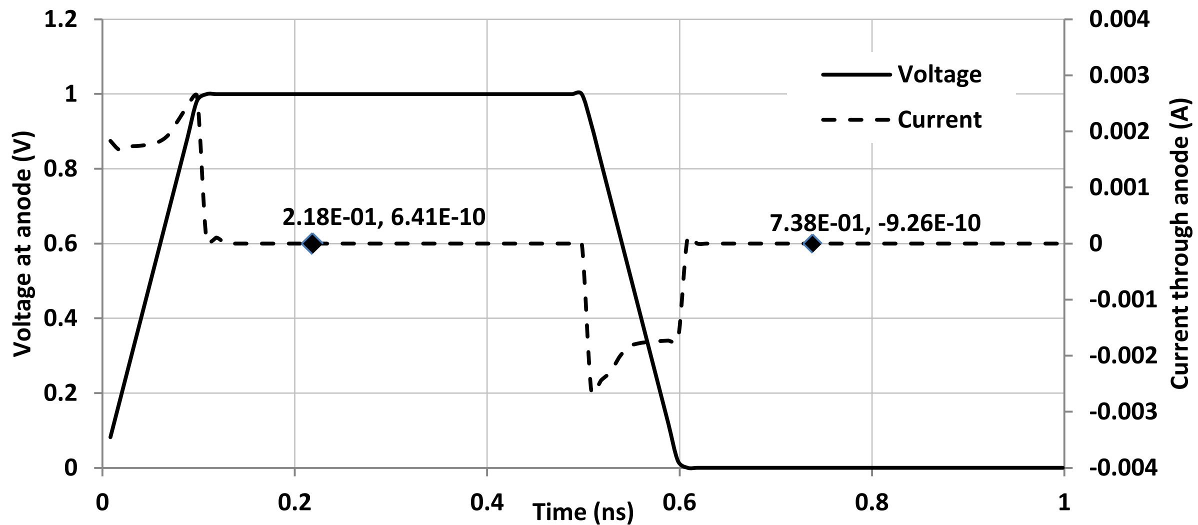


Figure 4-20: ESD protection scheme voltage and current responses under 1GHz I/O signals

Various ESD protection devices presented in this thesis have been placed onto a test chip for hardware verification. The layout of these devices is shown in **Figure 4-21**. Diode strings, SCR, DSCR and DtSCR are all placed in this corner. These devices are configured as square shapes to facilitate

the discharge current flowing in all directions. Due to time constraints, hardware testing of this chip was not completed before thesis submission, so it is left as future work.

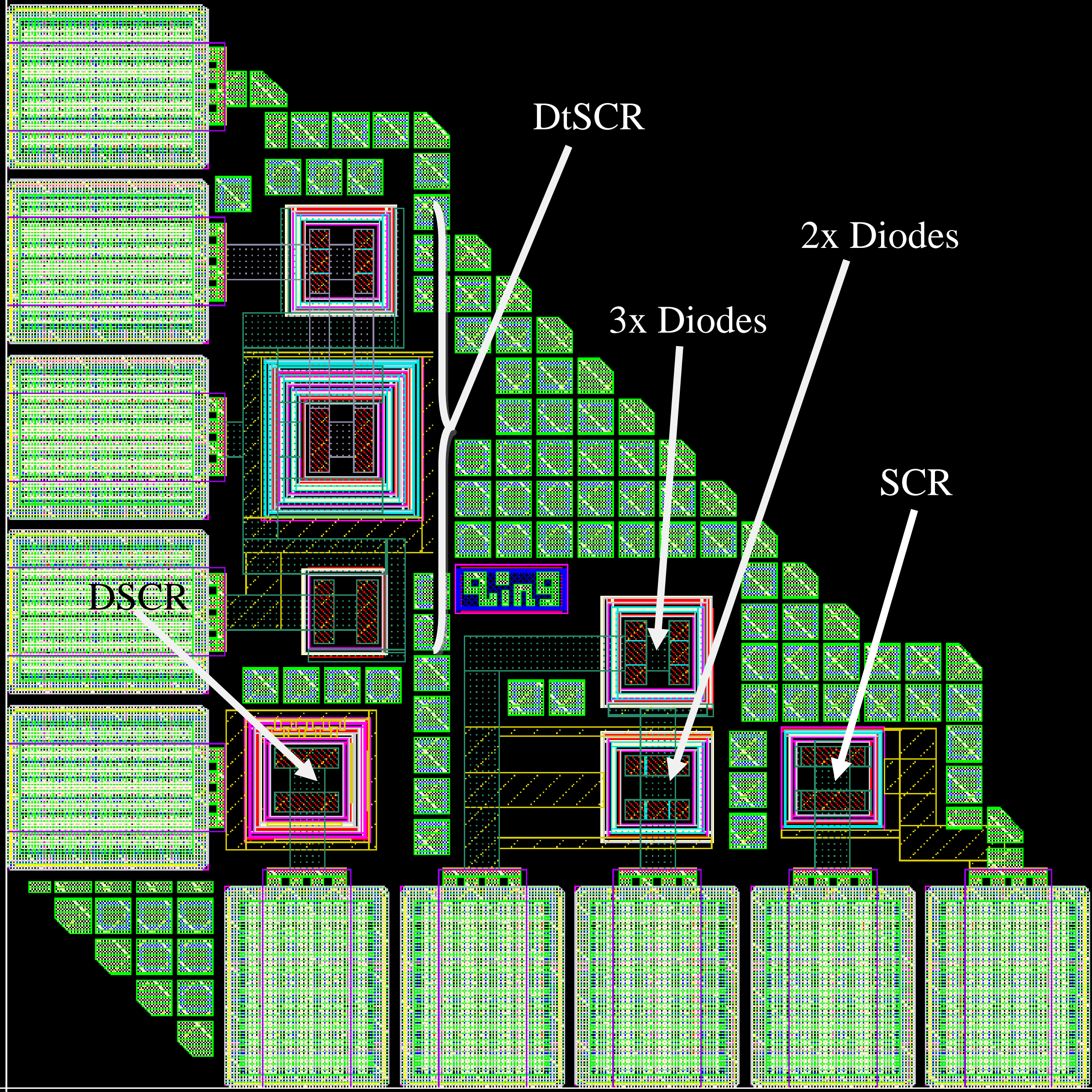


Figure 4-21: ESD protection devices on test chip corner

4.8 Chapter Summary

This chapter demonstrates different ESD test methods include HBM, CDM, capacitance, and latch-up. These tests are conducted in the device simulator Sentaurus®. The test-bench methodologies are explained and proven in each section. The results are compared among all devices. DtSCR is the ultimate choice with superior HBM and CDM performances. After the modification of its n-well, it comes out with a lowered capacitance which is comparable to diodes and also immune to latch-up.

Chapter 5 Conclusion

Electrostatic discharge phenomenon is regarded as a major reliability issue in semiconductor industry for a long time, and in the foreseeable future it will still dominate most of the failures in the IC world. Many research parties around the world have been putting great efforts into the ESD protection regime to reduce the device failure rate and cost of fabrications. As the principles of chip-level ESD designs, the protection devices must be capable of handling large crowded current and high overshoot voltages, while they do not interfere the IC's normal operating range. Along with the CMOS industry's scaling trend, the gate oxide thickness is reduced drastically. Now only ten angstroms of silicon dioxide layer is used for the most current process technologies. As a side effect of thinner gate oxide, low voltage tolerance has pushed the ESD design window narrower. Also, with higher operating frequencies, the capacitance seen from the driver will lower the switching speed, and if it varies significantly with frequencies, the signal's integrity is also compromised. Therefore, modern ESD protection device design has a number of challenges to tackle, low triggering voltage, high current sinking ability, low and non-variable capacitance. They are all difficult criteria to meet.

To qualify ESD protection circuits, they are put to test for all four zapping modes, PS, NS, PD and ND. The two categories of devices are snapback and non-snapback. The non-snapback devices are mainly consisted of different types of diodes, such as n^- or n-well diodes. They have various placement topologies, i.e. priorities are given to specific diode with a desired quality. These diodes are used in their forward biased region, in which they can sink a large amount of current with low heat and power generated. The snapback devices involve MOSFETs and SCRs. The use of ground-gate NMOS has been a simple choice for designers. However, with technology scaling, GGNMOS becomes more difficult to meet all design criteria, especially high leakage and large area. A conventional SCR is a *pnpn* structure, and there are many ways that the SCR are modified to fit different purposes, such as low triggering voltage, or low capacitance.

The non-snapback devices and circuits can be simulated in common circuit simulators, such as SPICE or Cadence environment. However, the snapback devices are more difficult to simulate. They require special finite element analysis tool, such as TCAD Medici and Sentaurus, to solve Poisson's equations within defined doping mesh grids. These tools are capable of simulating avalanche breakdown regions, where snapback devices are conducting in ESD events.

The modeling of ESD devices begins from the matching of an NMOS and PMOS transistor between device simulators and foundry provided data. However, limited information from the process

technology is not sufficient. Therefore, an external MOSFET modeling tool, PTM is used, which is developed by Arizona State University. By giving PTM limited foundry data, it is capable of generating other required values within a reasonable range. Then, by intelligent guessing, trial and error process, the MOSFET devices are constructed in device simulators. By extracting the process parameters, it is possible to build various ESD devices, in this case, diodes and different SCRs.

According to the JEDEC standard, to qualify ESD devices, Human-Body Model, Machine-Model, and Charged-Device Model tests are to be conducted. Due to the strong correlation of HBM and MM, only HBM and CDM are required. In order to setup the test-benches for the ESD devices in Sentaurus, the mesh grids are put to a mixed-mode circuit simulator. However, due to the lack of a proper "switch" in the tool to control the charging and discharging event. A work-around is designed for this purpose.

In order to establish a justified devices' comparison, the area of them is kept the same. From the simulation results of SCR, and DSCR, it is seen that they are not able to handle the discharge in 65 nm technology. Therefore, a modification of adding diode string into a conventional SCR is proposed, which is designated as Diode-triggered SCR. The extra diodes contribute to a higher holding voltage and faster triggering speed. This idea is implemented in the device simulator and the quasi-DC simulation shows a low triggering voltage of 2.26V and a high holding voltage of 2.05V. DtSCR has demonstrated lower than 5V overshoot in HBM test and 5.27V in CDM, which is lower than contemporary publicised result. At the mean time, the current sinking capability is on par as well. With 1700 um^2 area, DtSCR is only leaking 0.1 nA at 1.0V. After another modification, which is connecting the n-well contact to $V_{DD,}$ during normal operations, the anode n-well is reverse biased, which gives a low capacitance that is comparable to diodes. The p^+ at the anode and the n^+ tied to V_{DD} forms a forward biased diode to handle the ESD discharge mode of PD.

With a high holding voltage, DtSCR is immune to latch-up. This result is confirmed by simulating a positive and negative current injection event in accordance with JEDEC standard. However, latch-up is not related to ESD devices alone, the entire chips' floor planning is crucial.

As for the future, with more aggressive scaling or other nano-scale IC fabrication breakthrough, ESD damages will still persist. With higher frequency and smaller design window, better devices need to be designed. Based on the experiments conducted in this research work, a combination of diode and SCR devices presents strong capabilities to fulfill this purpose.

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Appendix A
Sentaurus® Code for NMOS Simulation

```
Title ""

Controls {}

Definitions {
	AnalyticalProfile "AnalyticalProfileDefinition.DrainSource" {
		Species = "ArsenicActiveConcentration"
		Function = Gauss(PeakPos = 0, PeakVal = 2e+20, ValueAtDepth =
1.4e+18, Depth = 0.02)
		LateralFunction = Gauss(Factor = 0.3)
	}
	Constant "ConstantProfileDefinition.Poly" {
		Species = "ArsenicActiveConcentration"
		Value = 2e+20
	}
	Constant "ConstantProfileDefinition.Channel" {
		Species = "BoronActiveConcentration"
		Value = 1.4e+18
	}
	Constant "ConstantProfileDefinition.Psub" {
		Species = "BoronActiveConcentration"
		Value = 6e+16
	}
	Refinement "RefinementDefinition_1" {
		MaxElementSize = ( 0.05 0.05 )
		MinElementSize = ( 0.001 0.001 )
		RefineFunction = MaxTransDiff(Variable = "DopingConcentration",Value
= 1)
	}
}

Placements {
	Constant "ConstantProfilePlacement.Psub" {
		Reference = "ConstantProfileDefinition.Psub"
		EvaluateWindow {
			Element = region ["Psub"]
		}
	}
	Constant "ConstantProfilePlacement.Channel" {
		Reference = "ConstantProfileDefinition.Channel"
		EvaluateWindow {
			Element = Rectangle [(0 0) (0.675 0.02)]
		}
	}
	AnalyticalProfile "AnalyticalProfilePlacement.Source" {
		Reference = "AnalyticalProfileDefinition.DrainSource"
		ReferenceElement {
			Element = Line [(0.375 0) (0.675 0)]
		}
	}
	AnalyticalProfile "AnalyticalProfilePlacement.Drain" {
		Reference = "AnalyticalProfileDefinition.DrainSource"
		ReferenceElement {
```

```
				Element = Line [(0 0) (0.3 0)]
			}
		}
		Constant "ConstantProfilePlacement.Poly" {
			Reference = "ConstantProfileDefinition.Poly"
			EvaluateWindow {
				Element = region ["region.gate"]
			}
		}
		Refinement "RefinementPlacement_1" {
			Reference = "RefinementDefinition_1"
			RefineWindow = region ["Psub"]
		}
		Refinement "RefinementPlacement.Psub" {
			Reference = "RefinementDefinition_1"
			RefineWindow = region ["Psub"]
		}
		Refinement "RefinementPlacement.Poly" {
			Reference = "RefinementDefinition_1"
			RefineWindow = region ["region.gate"]
		}
}
```

```
;; Defined Parameters:

;; Contact Sets:
(sdegeo:define-contact-set "Drain" 4 (color:rgb 1 0 0 )"##" )
(sdegeo:define-contact-set "Source" 4 (color:rgb 1 1 0 )"##" )
(sdegeo:define-contact-set "Sub" 4 (color:rgb 0 1 0 )"##" )
(sdegeo:define-contact-set "Gate" 4 (color:rgb 1 1 1 )"##" )

;; Work Planes:
(sde:workplanes-init-scm-binding)

;; Defined ACIS Refinements:
(sde:refinement-init-scm-binding)

;; Reference/Evaluation Windows:
(sdedr:define-refeval-window "RefEvalWin.Channel" "Rectangle" (position 0 0 0)
(position 0.675 0.02 0))
(sdedr:define-refeval-window "RefEvalWin.Drain" "Line" (position 0 0 0) (position
0.3 0 0))
(sdedr:define-refeval-window "RefEvalWin.Source" "Line" (position 0.375 0 0)
(position 0.675 0 0))

;; Restore GUI session parameters:
(sde:set-window-position 819 4)
(sde:set-window-size 838 750)
(sde:set-window-style "Windows")
(sde:set-background-color 0 127 178 204 204 204)
```

```
File {
	* Input Files
	Grid    = "2dNMOS2_msh.tdr"

	* Output Files
	Current = "NMOS2"
```

```
	Plot    = "NMOS2"
	Output  = "NMOS2"
}

Electrode {
	{Name="Drain"        Voltage=0.0}
	{Name="Source"       Voltage=0.0}
	{Name="Sub"          Voltage=0.0}
	{Name="Gate"         Voltage=1.0}
}

Physics {
	Hydrodynamic( hTemperature )
	AreaFactor=0.12
	EffectiveIntrinsicDensity(BandGapNarrowing(Slotboom))
	Mobility (
		DopingDependence
		HighFieldSaturation
	)
	Recombination (
		Auger
		SRH(DopingDependence)
		Avalanche(Okuto)
	)
}

Insert="PlotSection_des.cmd"


Math {
	Number_Of_Threads=2
	DrForceRefDens=1e12
	Extrapolate
	AvalDerivatives
	Iterations=10
	Digits=5
	NotDamped=50
}

Solve {
	Coupled(Iterations=100) {Poisson}
	Coupled{Poisson Electron Hole}

	Quasistationary(
		InitialStep=1e-3 MinStep=1e-5 MaxStep=0.01 Increment=1.41 Decrement=2
		Goal{Name="Drain" Voltage=1.0}
	){Coupled{poisson electron hole}}

*	Quasistationary(
*		InitialStep=1e-4 MinStep=1e-12 MaxStep=0.01
*		Goal{Name="Gate" Voltage=1.0}
*	){Coupled {poisson electron hole}}

*	Continuation (
*		Name="Drain"
*		Normalized
*		InitialVstep= 1e-3
*		MaxVoltage= 20
*		MinVoltage= -0.1
```

```
*             MaxCurrent= 1
*             MinCurrent=-1
*             Iadapt= 1e-6
*      ) { Coupled {Poisson Electron Hole hTemperature } }
*
}
```