Dual-band Power Amplifier for Wireless Communication Base Stations

by

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AUTHOR'S DECLARATION

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

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Abstract

In wireless communication systems, multiple standards have been implemented to meet the past and present demands of different applications. This proliferation of wireless standards, operating over multiple frequency bands, has increased the demand for radio frequency (RF) components, and consequently power amplifiers (PA) to operate over multiple frequency bands.

In this research work, a systematic approach for the synthesis of a novel dual-band matching network is proposed and applied for effective design of PA capable of maintaining high power efficiency at two arbitrary widely spaced frequencies. The proposed dual-band matching network incorporates two different stages. The first one aims at transforming the targeted two complex impedances, at the two operating frequencies, to a real one. The second stage is a dual-band filter that ensures the matching of the former real impedance to the termination impedance to 50 Ohm. Furthermore, an additional transmission line is incorporated between the two previously mentioned stages to adjust the impedances at the second and third harmonics without altering the impedances seen at the fundamental frequencies. Although simple, the harmonic termination control is very effective in enhancing the efficiency of RF transistors, especially when exploiting the Class J design space.

The proposed dual-band matching network synthesis methodology was applied to design a dual-band power amplifier using a packaged 45 W gallium nitride (GaN) transistor. The power amplifier prototype maintained a peak power efficiency of about 68% at the two operating frequencies, namely 800 MHz and 1.9 GHz. In addition, a Volterra based digital predistortion technique has been successfully applied to linearize the PA response around the two operating frequencies. In fact, when driven with multi-carrier wideband code division multiple access (WCDMA) and long term evolution (LTE) signals, the linearized amplifier maintained an adjacent channel power ratio (ACPR) of about 50 dBc and 46 dBc, respectively.

Acknowledgements

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Chapter 1
Introduction

With the development of wireless communication systems, an increasing number of communication standards have been proposed and implemented to meet the performance requirements of different applications. Since the power amplifier (PA) dominates the power consumption of the radio system, it is imperative that the PA satisfy some stringent performance requirements. Those requirements and the design target for a power amplifier include high drain efficiency, a minimum power level, linearity, multi-band and broadband operational ability, efficiency enhancement at back-off power level, etc.

The major function of a power amplifier is to draw power from a direct current (DC) power supply and use the power to enlarge the input signal. Drain efficiency describes the efficiency of the transformation from DC power to radio frequency (RF) power. Since the power amplifier is the RF component that consumes most of the power in transceiver systems, the power amplifier should have high efficiency to minimize wireless infrastructure operating expenses. Also, a PA with low efficiency will result in a large amount of unused DC power heating up the transistor and consequently affecting transistor performance. To enhance the efficiency of a power amplifier, several classes of operation have been proposed to shape the output voltage and current waveform so that DC power consumption can be minimized. Since output voltage and current waveform can be affected by the termination at both fundamental and harmonic frequencies, some operation modes use harmonics to re-shape the voltage and current waveform for better PA performance. The classes of operation mode can be categorized in two types. In one type, a transistor acts as a voltage controlled current source, and output power will depend on the input signal. This kind of operation mode includes Classes A, AB, B, J, C, F/F^{-1}, etc. In the other type, such as Class E or Class D operation mode, a transistor acts as a switch that will turn on and off depending on the input signal. This type of operation mode can be applied when an input signal has a constant envelope. Since our work deals mainly with a modulated signal for a wireless communication application with a variable envelope, the first type of operation mode is chosen for design.

Since a high-efficiency PA is always achieved by re-shaping the voltage and current waveforms at drain, the linearity of the PA may not be maintained and thus the output signal will be distorted. The nonlinearity of a PA will cause spectral re-growth adjacent to the operating frequency band and will affect signals in the adjacent channel. To deal with this nonlinearity problem, several approaches have

been proposed in the literature. One very attractive and popular linearization technique is the pre-distortion (DPD) technique, especially digital pre-distortion [1]. This technique “pre-distorts” the signal at the input in exactly the opposite way that the PA circuit does, so that the overall system has a linear input-output performance. However, applying the DPD technique with a high-efficiency nonlinear PA may not always guarantee a relatively linear performance. In some cases the DPD technique fails to linearize the PA, partly because the nonlinear performance of the PA is too complicated to model. Hence, it is necessary to demonstrate the linearizability of a high-efficiency PA.

Traditionally, PA design focuses mainly on one single frequency. However, since multiple communication standards such as global system for mobile communications (GSM), wideband code division multiple access (WCDMA), long term evolution (LTE), etc. have been implemented to meet the demands of different applications in wireless communication systems, specific hardware needs to be designed for each frequency band and thus multi-radio is needed to cope with multiple frequencies. While the multi-radio solution is simple to implement, it is a cost-inefficient solution. An alternative and very attractive solution would be radios that can operate over multiple bands or broadband. This solution requires the RF front-end, and consequently the power amplifier, to operate over multiple frequency bands or broadband. The broadband PA is suitable when operation frequencies are close to each other; the multi-band PA is a good candidate if the operation frequencies are far apart. Some design approaches have been proposed for multi-band PAs and broadband PAs. For a broadband PA, wideband matching network (MN) topology is needed to achieve optimal impedance matching within a wide frequency range. Structures such as multi-sections LC circuits [2] and tapered transmission lines [3] have shown their ability to achieve wideband matching. For a multi-band PA, circuit topologies such as an impedance buffer [4][5], a multi-section impedance transformer [6], and T and Pi type stub loaded quarter-wave transformers [7] have been proposed to realize impedance matching at multiple frequency bands. Among other solutions, a PA with a reconfigurable MN designed for each specific frequency can be applied in both broadband and multi-band PA design. Also, it is found that choosing a proper class of operation with wider design space and less sensitivity of harmonic mismatch can help lessen the restriction of broadband or multi-band matching and thus provide more flexibility in PA design [8].

Modern communication standards generate signals with high peak-to-average power ratio (PAPR) for more efficient data rates. This approach requires the power amplifier to operate not only at peak

power, but also at around 6-10dB backed off. However, since the power amplifier is usually designed for peak power, maximum efficiency is attained only at peak power and degrades significantly when input power is backed off. Several efficiency enhancement techniques have been proposed to deal with this issue, such as the linear amplification using nonlinear components (LINC) technique [9], Doherty amplifier technique [10], envelope elimination and restoration (EER) technique [11], envelope tracking (ET) technique [12], etc. Because of its simplicity of implementation, the Doherty amplifier technique which is based on load modulation has been widely investigated in recent years. In addition, the research work on broadband and multi-band Doherty amplifiers has been increasing rapidly these years and the combination of broadband/multi-band MN design approach and the Doherty technique is very promising.

In this thesis, an overview of high power amplifiers is presented in Chapter 2, which introduces the basic operation mode of a PA and a design strategy to achieve a high efficiency high-power PA. A literature review of broadband and multi-band PAs is also presented. In Chapter 3, a systematic dual-band matching network design approach for a dual-band Class J PA is introduced and analyzed. A dual-band PA working at 0.8GHz and 1.9GHz with 45W output power is designed using this approach. The design procedure and measurement results are given in Chapter 4. Finally, a conclusion and suggestions for future improvement are presented in Chapter 5.

Chapter 2
High power Amplifier Overview

2.1 Class of Operation of Power Amplifiers

Different classes of operation of power amplifiers can be employed for different design requirements and applications. Some common performance measures for PA design include gain, operation bandwidth, output power delivered to the load, drain efficiency/power added efficiency, and linearizability, etc. In the following subsections, several classical classes of operation of power amplifier will be introduced, including Classes A, B, AB, C, F/F^{-1}, and switch mode PA [13]. Also, Class B/J continuous mode of operation will be introduced. Before introducing the operation mode, some important parameters need to be defined:

$$Gain = \frac{P_{out}}{P_{in}} \tag{2.1}$$

$$Drain\ efficiency\ (DE) = \frac{P_{out}}{P_{DC}} \tag{2.2}$$

$$Power\ added\ efficiency\ (PAE) = \frac{P_{out} - P_{in}}{P_{DC}} \tag{2.3}$$

where P_{out} is the fundamental RF power of the output, P_{in} is the input signal power, and P_{DC} is the DC power consumption.

2.1.1 Class A Operation Mode

Figure 2.1 shows the biasing point (in red) of the transistor and the waveform of drain voltage and current of Class A operation mode. The DC-IV curves in this figure assume an ideal transistor with a knee voltage of zero and output impedance of infinity.

Class A is the only operation mode that allows a transistor to conduct for the full signal period. The current waveform of Class A is sinusoidal, which exactly follows the variation of the input voltage. Class A has good linearity performance since the transistor is biased in the active linear region; however, because of its current and voltage characteristics, the maximum drain efficiency of Class A mode is only 50%. The low efficiency feature makes Class A not a popular class of operation for high efficiency PA design.

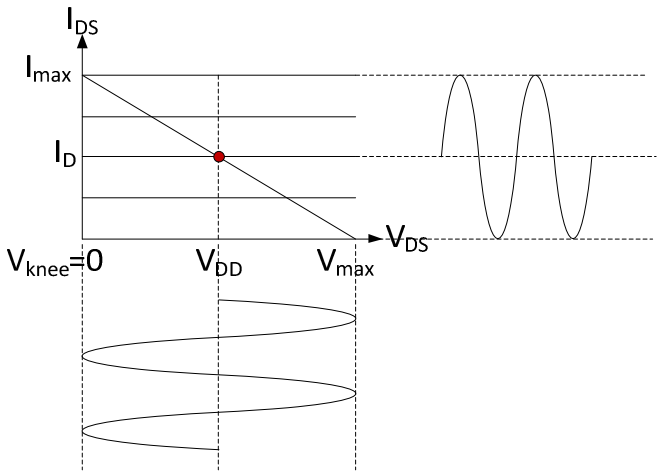


Figure 2.1 Class A operation mode

2.1.2 Reduced Conduction Angle Mode- Classes AB, B, C

Several classes of operation mode have been proposed to improve the drain efficiency of power amplifiers. Some conventional high efficiency amplifier modes include Class AB, Class B, and Class C.

By reducing the conduction angle α of the drain current, these three modes allow for the minimization of the overlap between output voltage and current waveforms and consequently the DC power consumption. The conduction angle is defined as the proportion of the RF cycle during which the transistor is conducting. Figure 2.2 shows the current waveform of different conduction angles for Classes A, B, AB and C. It can be seen that the conduction angle α is 2π for Class A, π for Class B, π to 2 π for Class AB, and 0 to π for Class C. It is worth mentioning that the Classes A, B, AB and C share the same drain voltage waveform.

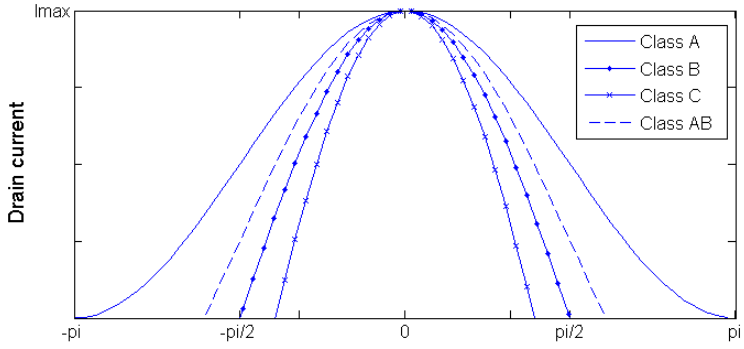


Figure 2.2 Drain current vs. conduction angle of Classes A, B, AB and C

The conduction angle of drain current is reduced by lowering the gate biasing point so that a portion of the input voltage cycle drops below the threshold voltage and prevent the transistor from conducting current. Figure 2.3 shows the biasing points of Classes A, B, AB and C.

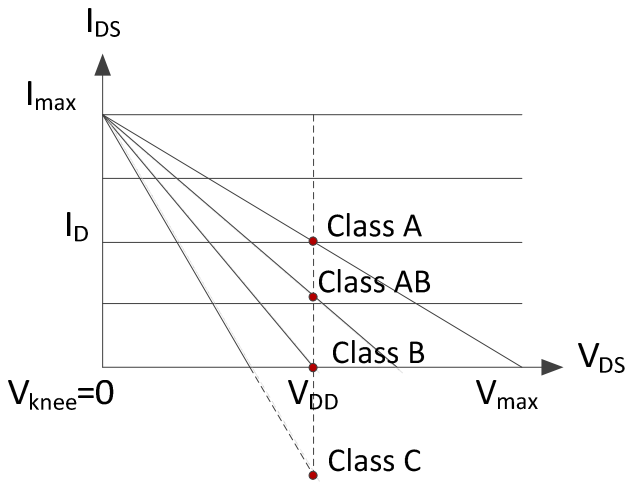


Figure 2.3 Biasing points for Classes A, AB, B and C

Assuming a perfect harmonic short, maximum current swing up to I_{max}, and maximum voltage swing up to V_{max} (or equally $2V_{DD}$), the RF fundamental output power is:

$$Pout = \frac{V_{DD}}{\sqrt{2}} \cdot \frac{I_1}{\sqrt{2}} \tag{2.4}$$

DC power consumption is given by:

$$P_{DC} = V_{DD} \times I_{DC} \tag{2.5}$$

where I_1 and I_{DC} are the fundamental and DC components of drain current respectively. Using Fourier analysis we can obtain:

$$I_1 = \frac{I_{max}}{2\pi} \cdot \frac{\alpha - \sin\alpha}{1 - \cos\left(\frac{\alpha}{2}\right)} \tag{2.6}$$

$$I_{DC} = \frac{I_{max}}{2\pi} \cdot \frac{2\sin\left(\frac{\alpha}{2}\right) - \alpha\cos\left(\frac{\alpha}{2}\right)}{1 - \cos\left(\frac{\alpha}{2}\right)} \tag{2.7}$$

Thus the drain efficiency can be calculated as:

$$DE = \frac{P_{out}}{P_{DC}} \tag{2.8}$$

Substituting the conduction angle value of each operation mode, the maximum drain efficiency of Class B PA can be calculated as 78.5%. However, since the biasing point of Class B PA is outside the active linear region, Class B PA may face the nonlinearity problem.

The conduction angle of Class AB operation mode is between Class A ($\alpha=2\pi$) and Class B ($\alpha=\pi$), and the maximum efficiency of Class AB is between 50% and 78.5%. Class AB operation provides the opportunity to balance the tradeoff between linearity and efficiency.

Class C PA is biased more deeply than Class B PA and thus has a smaller conduction angle of current waveform. The drain efficiency of Class C can be higher than 78.5%; however, Class C PA suffers more from nonlinearity issues.

In order to get the same I_{max}, more input voltage is needed if the operation mode has lower gate biasing, and it can be seen that the achievable gain reduces as we shift from Class A to Class C and passing by AB and B.

2.1.3 Class F/Inverse Class F Operation Modes

In previously mentioned modes, all the harmonics are assumed to be shorted and the drain voltage waveforms are sinusoidal, whereas in Class F and inverse Class F modes, the odd/even harmonic frequency components are used to genuinely shape the waveform of the output voltage/current to enhance drain efficiency. Figure 2.4 illustrates how adding harmonics can help to improve efficiency. The parameter r in Figure 2.4 is the ratio of the third harmonic to the fundamental component; r=0 means the output voltage has no third harmonic and represents the voltage waveform of Class A, AB, B or C. It can be seen that if r is lower than 0.25, the peak voltage of the harmonic re-shaped waveform is smaller than the peak voltage of the purely sinusoidal waveform. This analysis indicates that to achieve the same peak voltage, the third harmonic re-shaped waveform can contain more fundamental component while DC power consumption remains the same. Thus, drain efficiency is increased.

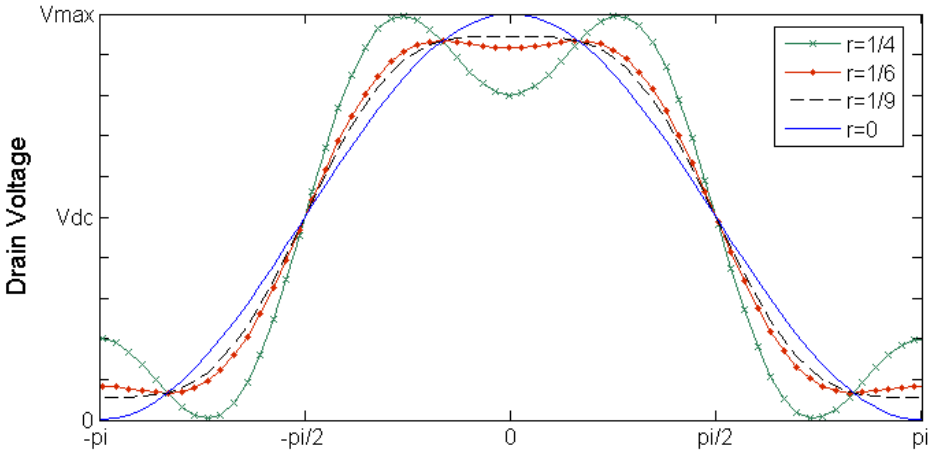


Figure 2.4 Drain voltage reshaped by adding the third harmonic

In Figure 2.4, only the third harmonic is added. It has been shown that if higher order harmonics are used to properly re-shape the voltage waveform, drain efficiency can be further improved. Figure 2.5 and Figure 2.6 show the ideal voltage and current waveforms of Class F and Class F^{-1}, respectively. To achieve the required voltage and current waveforms, Class F operation mode requires short circuit at even harmonics and an open circuit at odd harmonics whereas Class F^{-1} does the opposite. Theoretically, the efficiency of Class F and Class F^{-1} can be 100% if the entire fundamental and harmonic termination requirements are met; however, in reality it is impossible to control all the harmonics. Analysis demonstrates that having control of up to third harmonics usually is good enough to achieve high efficiency performance of PA. Since the fundamental optimum impedance of Class F^{-1} is higher than that of Class F, Class F^{-1} is preferred in design because it requires a lower impedance transformation ratio and therefore allows easier matching.

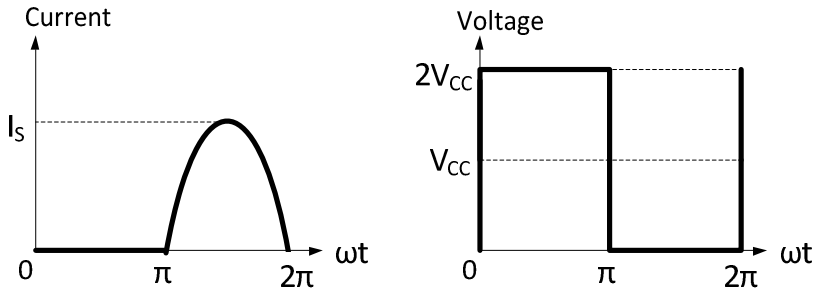


Figure 2.5 Current and voltage waveform of Class F operation mode

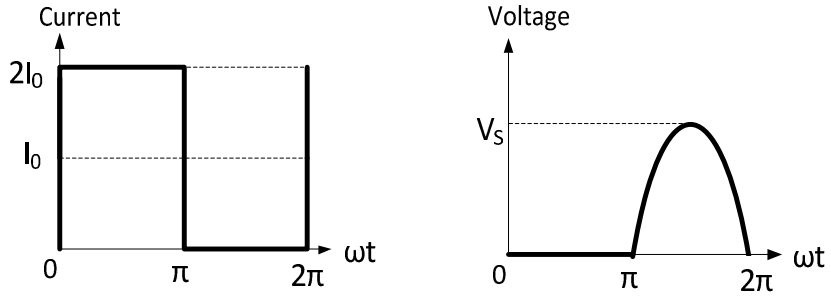


Figure 2.6 Current and voltage waveform of Class F^{-1} operation mode

2.1.4 Class B/J Continuous Mode

The analysis of Class J continuous mode is inspired by Class B operation mode. In Class B mode, all the harmonics are shorted and the optimum impedance is Ropt, which equals to the ratio of V_{DD} to I_1 in Equation 2.4. However for Class J, the optimum impedance is Ropt plus a reactive component. Also, second harmonics are presented at the drain to help shape the waveform of drain voltage in Class J mode. In terms of efficiency, Class J maintains the same efficiency as Class B.

Some analysis has focused on relationship of the optimum impedance of Class J PA at fundamental and harmonics frequencies. It has been shown [8] that the optimum impedance requirements are:

$$Z_{f0} = Ropt + j \cdot \alpha \cdot Ropt \qquad (-1 < \alpha < 1) \tag{2.9}$$

$$Z_{2f0} = 0 - j \cdot \alpha \cdot \frac{3\pi}{8} Ropt \qquad (-1 < \alpha < 1) \tag{2.10}$$

Z_{f0} and Z_{2f0} are the optimum impedances at fundamental frequency and second harmonic respectively. The higher harmonic components are assumed to be shorted. It can be seen that α=0 represents the condition for Class B operation mode. In the range of $0 < \alpha < 1$, the operation mode is called Class J; in the range of $-1 < \alpha < 0$, the operation mode is called Class J*. Figure 2.7 shows the drain voltage and current waveform for Class J ($\alpha = 1$), Class J* ($\alpha = -1$), and Class B ($\alpha = 0$). Class J, J* and Class B share the same biasing point of V_{GS}, so their current waveform are the same. Class J* gives the mirrored voltage waveform of Class J with same $|\alpha|$. Comparing Class J/J* with Class B drain voltage waveform, it can be found that the waveform is reshaped and the peak voltage value of Class J/J* is higher than that of Class B, which means the transistor operating at Class J needs to withstand higher voltage than that of Class B.

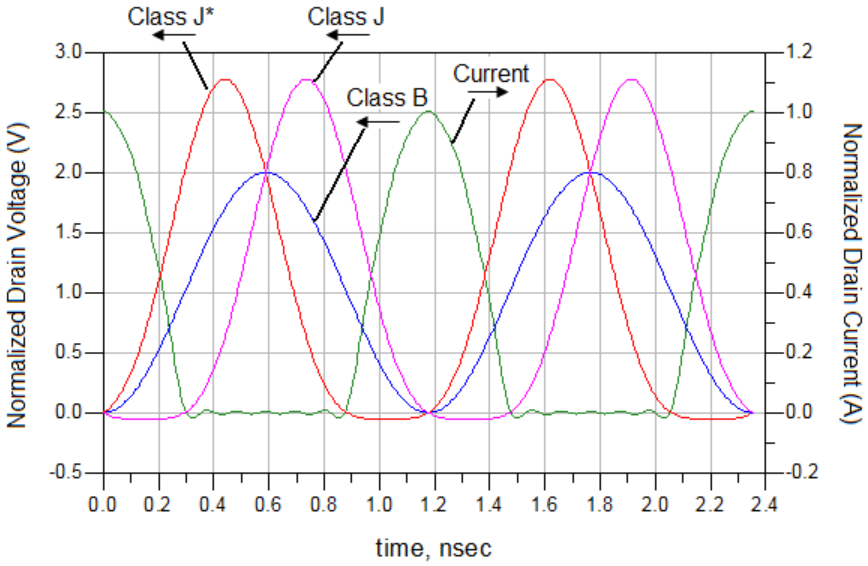


Figure 2.7 Drain voltage and current waveform of Class J/J* and Class B operation mode

Figure 2.8 shows the normalized optimum impedances at the ideal current source reference plane at fundamental and second harmonic frequencies with different values of α. The third harmonic is fixed to short circuit. In reality this plot will be shifted in the Smith chart because of the effect of Cds, which is the capacitance between drain and source of the transistor, and package parasitic of the device.

Furthermore, research has been done on the design space and sensitivity of the harmonic mismatch for Class B/J continuous mode. Analysis [8][14] shows that if the fundamental impedance in Class J operation mode is properly chosen, the design space of the phase of harmonic impedance for Class B/J continuous mode PA is much larger than that of Class B PA itself while keeping the same high drain efficiency. Thus, when designing the matching network of harmonic frequency impedance, if the small range of phase where the efficiency drops fast is designed to be properly avoided, impedance in anywhere else should be sufficient to achieve high efficiency. Figure 2.9 shows an example of the design space of second harmonic impedance for Class J PA. This figure shows the simulation results of PAE versus the phase of reflection coefficient Γ at second harmonic frequency at the load side of 45Watt GaN high electron mobility transistor (HEMT) device as an example. As shown in the figure, PAE remains high in a very wide range, indicating a wide design space. The wide design space feature of Class J PA makes it a good candidate for broadband and multi-band PA design, which will be discussed in Section 2.3.

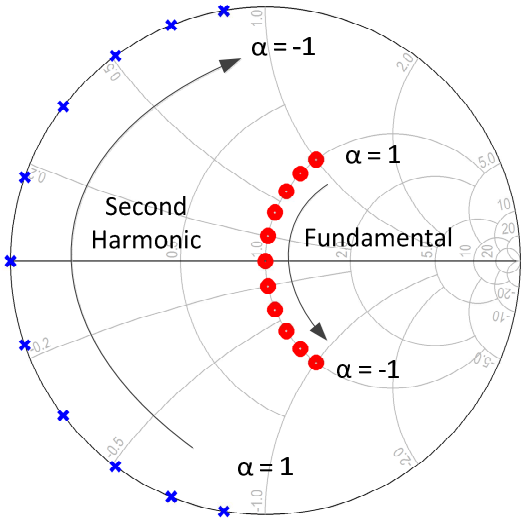


Figure 2.8 Design space of fundamental and second harmonic impedance of Class J mode

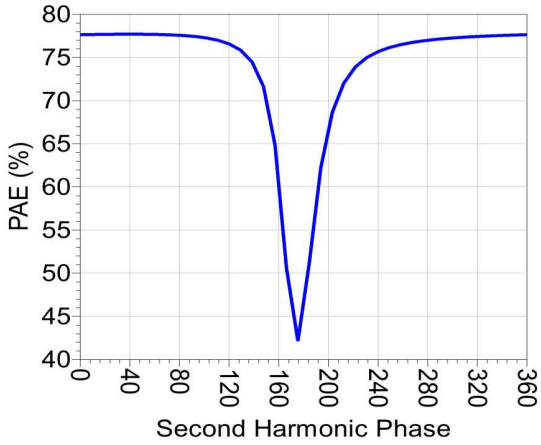


Figure 2.9 Design space of second harmonic phase of Class J PA

2.1.5 Switch Mode PA

In this operation mode, the input signal will either saturate the transistor or keep the transistor in cutoff. Thus the transistor will behave like an RF switch, rather than a voltage controlled current source as in the previous operation modes. Since the magnitude information of the input signal will not be captured at the output, switch mode PA is usually applied to amplify the constant envelope signal. The efficiency of switch mode PA is 100% with idealized assumptions such as non-zero saturation resistance of the transistor, instantaneous and lossless switching action, etc. The conventional switch mode PA includes Class E PA and Class D PA. Class E PA can be realized with

shunt capacitance, a parallel circuit, and transmission lines. Class D PA is realized in a push-pull structure. Since our work focuses on wireless communication applications with a modulated signal of non-constant envelope, the switch mode PA will not be discussed in detail.

2.2 Practical Issues of Power Amplifier Design

Most theoretical analysis of transistors is done at the ideal current source plane; however, in reality the transistor performance is affected by internal and external factors. Also, the DC-IV curves of realistic transistors will have a knee region that affects the transistors' performance and thus PA design. In this section the knee region interaction, the internal capacitor effect and the package effect of the transistor device are discussed. To determine the optimum impedance of the package transistor, the load pull and source pull techniques are widely used in practice. Finally, the stability of the circuit is also an important issue that needs to be considered during design.

2.2.1 Knee Region Interaction

The DC-IV curves shown in Figure 2.1 assume knee voltage to be zero; however, in reality the knee voltage will always be a significant percentage of the DC supply. Figure 2.10 shows the actual DC-IV curves of a GaN HEMT 45W transistor (the thermal resistor has been set to zero to eliminate the long term thermal effect). The Class B load line is plotted on Figure 2.10 for different cases. The dashed load line is the load line for the ideal case, where the knee voltage is zero, the current waveform is half sinusoidal and 78.5% peak efficiency can be obtained. However, if the same load line is used for the actual DC-IV behavior, the waveform of the current will be distorted as shown in Figure 2.11. Usually a dip will be observed at the peak region of the current waveform since it is where the drain voltage intrudes into the knee region. Since the drain voltage also depends on the drain current, the distortion of the waveform will be affected recursively. This waveform distortion will change the fundamental component and thus affect the linearity of the PA.

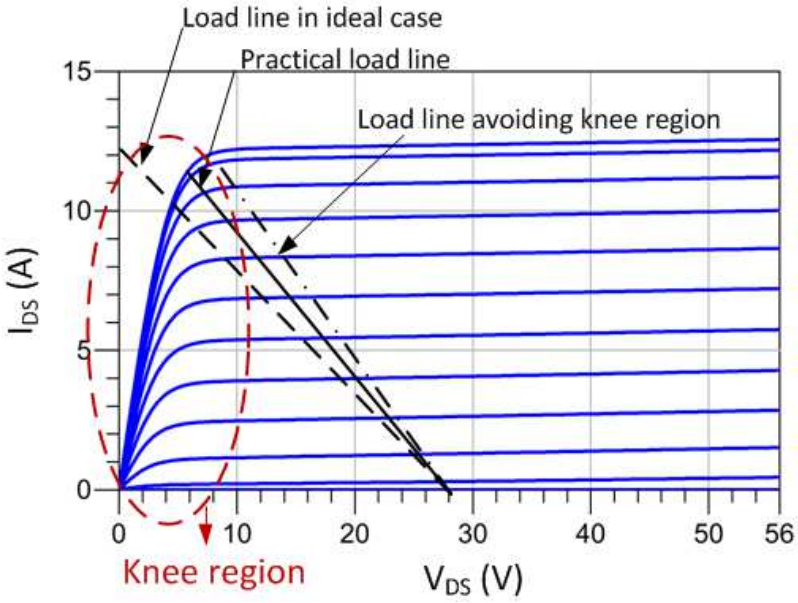


Figure 2.10 Load line with/without knee region interaction

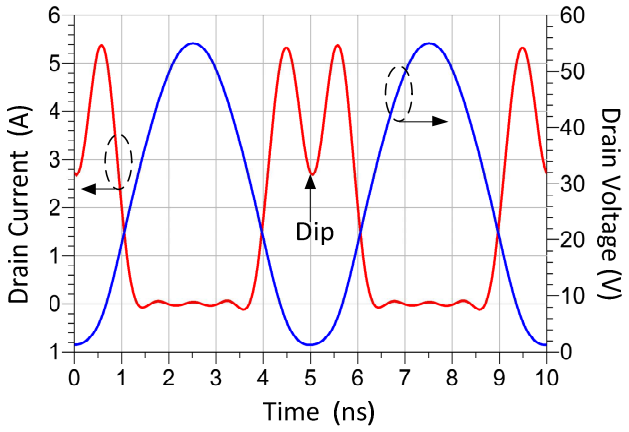


Figure 2.11 Drain current and voltage waveform with knee region interaction

To avoid the waveform distortion, the dot-dashed load line in Figure 2.9 can be chosen to prevent the drain voltage from entering the knee region. It can be seen that by choosing this load line, DC power consumption remains the same whereas the RF power is reduced because the output voltage swing is no longer maximized. Thus, the drain efficiency will be sacrificed.

In practical design, the solid load line shown in Figure 2.10 is chosen as a compromise between linearity and efficiency. This load line allows the transistor to go slightly into the knee region and have some extent of distortion, such that the efficiency is not unduly sacrificed.

2.2.2 Internal Capacitor of the Device

Because of the physical characteristic of the transistor structure, transistor performance will be affected by its internal parasitic, including the capacitance among drain, source and gate. For field effect transistors, the two most important capacitors that affect the transistor analysis are Cgs and Cds. The behavior of the capacitor will depend on different device technology. For example, Cgs of a GaN device is nonlinear but Cds of a GaN HEMT transistor is relatively linear, whereas for a laterally diffused metal oxide semiconductor (LDMOS) transistor, it is the opposite. The capacitor of the device will affect the transistor performance in many aspects, such as gain, optimal impedance matching, bandwidth, etc.

2.2.3 Package Effect of the Device

Figure 2.12 shows an example of a package transistor [15]. The figure illustrates the internal construction of a 2.1GHz 90W LDMOS transistor from Freescale.

The gate and drain leads provide connections between the package device and the external circuit. The bond-wires are used to connect the die to the lead. For this transistor, the bond wires are also used to realize a pre-matching inside the transistor package together with the MOS capacitors, to improve the performance of the transistor. Usually, the bond-wires behave like inductors and the leads behave like a combination of inductor and capacitor. It can be seen that the performance of the transistor will be affected by the package. Usually, the optimum impedance for a package transistor will be shifted a lot from the theoretical optimum impedance calculated using ideal transistor.

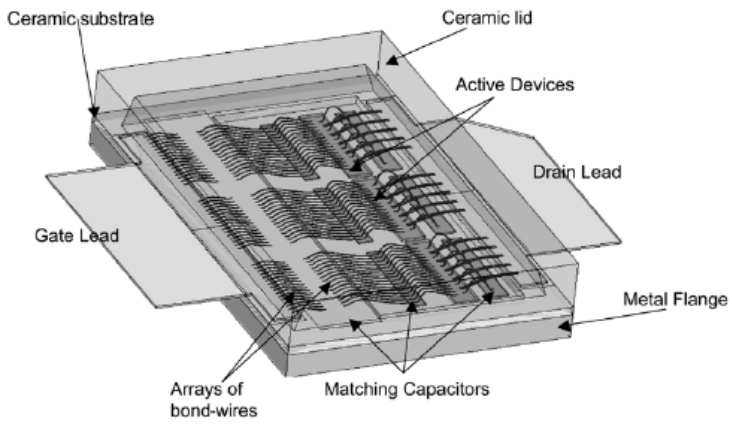


Figure 2.12 Illustration of LDMOS package transistor (with pre-matching) [15]

2.2.4 Load Pull/ Source Pull Technique

According to the discussion above, in most cases the optimum impedance of PA design cannot be chosen using the ideal transistor analysis. In practice, optimum impedance is usually determined using the load pull/ source pull technique, which can be done either on the test bench or in simulation software if the the transistor device has been modeled with adequate accuracy. Figure 2.13 shows the simplified set up of load/source pull. First the biasing point of gate and drain, the input power, and the operating frequency need to be selected. Then the input and output tuner will be adjusted to provide different reflection coefficients at the source side (Γ_{source}) and load side (Γload) of the transistor. The corresponding output fundamental power and DC power consumption will be measured for each Γ.

The results of the load pull/ source pull are usually presented as constant power added efficiency (PAE) and output power contours. Since the optimal value of Γ_{load} will depend on the value of Γ_{source} and vice versa, the process will be repeated several times until optimum performance is achieved. Usually, the optimum PAE (or DE) and the optimum output power will not share the same optimal impedance for load side, and thus the maximum PAE and maximum output power cannot be achieved at the same time. Figure 2.14 illustrates an example of the load pull result for a 45W GaN transistor at 1.9GHz. A trade off strategy is needed when selecting the optimum impedance. As can be seen in Figure 2.14, the design target impedance is finally selected between the two optimum impedances. In addition, the load/source pull technique can be applied to determine optimum impedances at harmonic frequencies.

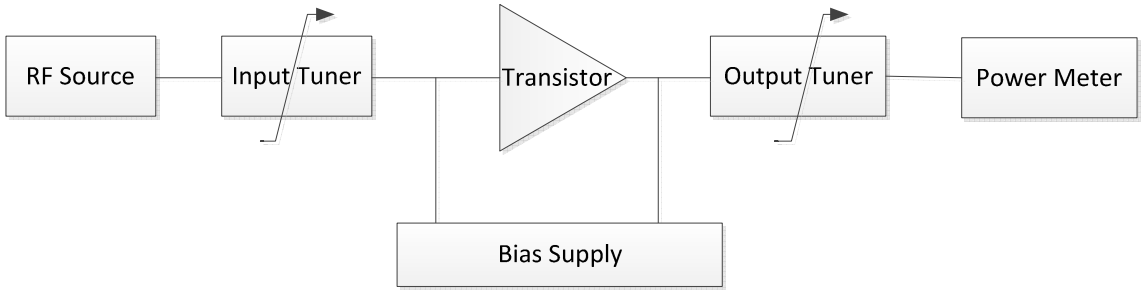


Figure 2.13 Load/Source pull set up

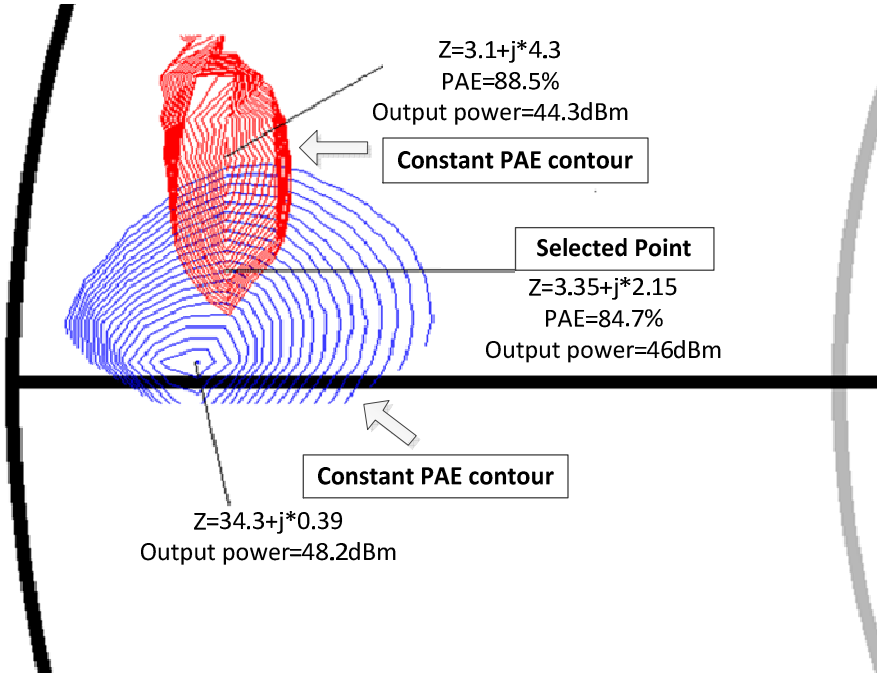


Figure 2.14 Load pull result of 45W GaN transistor at 1.9GHz

Since the load pull/ source pull technique treats the transistor device as a black box, we lose the insight of the intrinsic voltage and current of the transistor drain and thus have less understanding of the class of operation mode that the transistor is working at. Also, since the voltage and current of the current source plane cannot be monitored, we increase the possibility of exceeding the voltage limitation of the device and harming the transistor.

A better solution would be to conduct load pull/ source pull and then verify the performance using an exploded transistor device model, by which we can access the current source plane and monitor the intrinsic voltage and current.

2.2.5 Stability Issues of PA Design

In PA design, stability analysis needs to be done to avoid oscillation, especially in the low frequency range where gain is relatively high. Pozar et al. [16] analyzed the stability of a small signal. Adding resistors in series or in shunt with the transistor usually will help to stabilize the circuit. A properly selected capacitor will be added in parallel with the resistor to let the RF signal pass through instead of being attenuated by the resistor. For a high-power high-efficiency amplifier, the stabilization circuit is usually added at the source side to minimize the loss of RF signal.

It is worth mentioning that the instability at RF working frequency cannot be stabilized by adding a resistor for high efficiency consideration. Thus, before selecting the target impedance, it is important that the stability analysis be done at the working frequency and the selected target impedance is in the stable region.

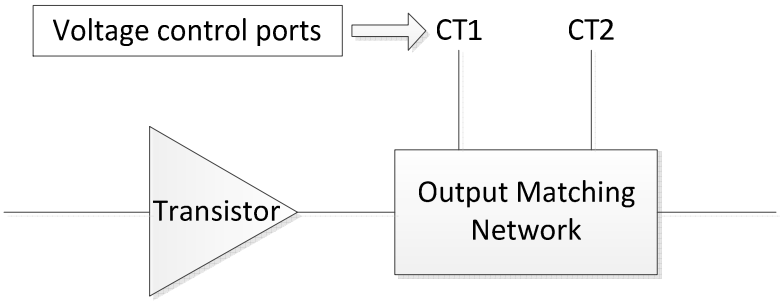
2.3 Broadband and Multi-Band Power Amplifier

The demand for broadband access and the proliferation of the applications of wireless communication have motivated the constant development of wireless standards. Different communication standards increase the requirement of broadband or multi-band communication systems, and consequently of broadband or multi-band power amplifiers with good performance. Traditionally, a PA is designed for each frequency band, a solution that can be easily implemented but is cost inefficient. Thus, power amplifiers are needed that can operate over a broadband or multiple frequency range. This section discusses the current approaches of broadband PA and multi-band PA design.

2.3.1 Broadband Power Amplifier

Since broadband power amplifiers need to achieve a required output power and high efficiency at a broad frequency range, the difficulty of MN design is increased. Several approaches have been proposed in the literature to achieve broadband PA performance.

One approach is to design a tunable broadband PA with a reconfigurable matching circuit. Figure 2.15 gives an example of a reconfigurable PA proposed by Zhang et al. [17]. The output matching of the PA is realized with LC circuits using PIN diodes controlled by voltage control ports (CT1, CT2) to adjust the equivalent inductor value. In this way, the matching network can be optimized at each sub-frequency band by adjusting the equivalent inductor value. The disadvantage of this technique is that the PA cannot operate at the broadband frequency range concurrently and the switching time between different operation bands may also be an issue.



CT1	CT2	Frequency band (GHz)
0	0	1.9-2.0
0	1	1.7-1.8
1	0	1.5-1.7
1	1	0.8-1.0

Figure 2.15 Prototype of reconfigurable broadband PA [17]

To design a concurrent broadband PA, a wideband MN is needed. Li et al. [2] proposed a low Q multistage matching network, where the multistage LC circuit shown in Figure 2.16 is applied to decrease the quality factor and smooth the variation of the impedance in the frequency range. Similar approaches such as wideband MN implemented by capacitors and micro-strip lines [18] can also achieve a wideband MN performance.

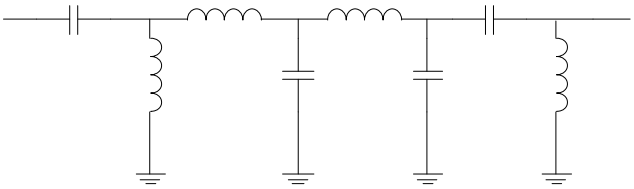


Figure 2.16 Low Q multistage LC matching network [2]

Another approach to realize wideband MN is to use tapered transmission line [3], which causes the impedance to vary in a continuous way. Figure 2.17 shows an example of broadband PA MN realized by tapered transmission line.

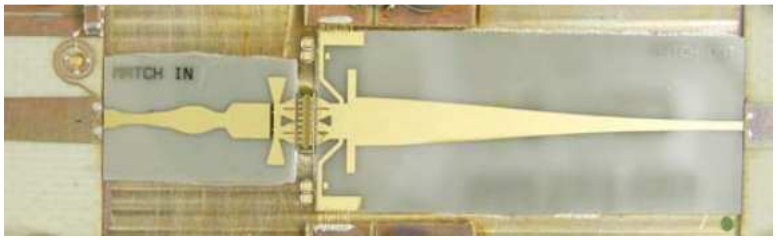


Figure 2.17 Broadband PA using tapered transmission line [3]

The class of operation of broadband PA has also been discussed, and recently Class J and Class F3 [19] have been found to have wideband potential for PA design.

Previous discussion of Class J operation mode in Subsection 2.1.4 has shown that Class J operation mode (or Class B/J continuous mode) can benefit from the existence of multiple sets of fundamental and harmonic impedances. Furthermore, it has been shown that if the fundamental impedance in Class J operation mode is properly chosen, the sensitivity of harmonic impedance mismatching, which is evidence in Class B design, can be largely reduced and thus implies a wider design space [8][14]. Wright et al. [8] have shown the wide bandwidth potential of the Class J mode due to the wide design space of Class J PA and successfully applied this operation mode in broadband PA design; the PA achieved 60%-70% drain efficiency cross the frequency range of 1.4-2.6GHz.

Carrubba et al. [19] proposed a class of operation mode called “Continuous-ClassF3” power amplifier mode was proposed recently and showed its potential for broadband PA design. The origin of continuous Class F3 mode is Class F mode; however, in Class F3 mode the open or short circuit harmonic termination requirement is relaxed. Similar to Class J operation mode, Class F3 mode has multiple sets of fundamental and harmonic impedances for the same PA performance, and it also has a wider design space of harmonic impedance, indicating the wideband operation potential of this operation mode.

2.3.2 Multi-Band Power Amplifier

Several approaches have been proposed recently in the literature to design multi-frequency power amplifiers. As has been done for broadband PAs, reconfigurable MN topology can be applied to multi-band PA design. Several attempts have explored the application of electronically tunable devices, such as MEMS (micro-electromechanical systems) switches to design reconfigurable matching networks needed to develop frequency agile and flexible power amplifiers. Figure 2.18 shows an example of multi-band reconfigurable PA designed by Fukuda et al [20]. However, this solution suffers from the slow switching speed and the limited power handling capabilities of the

tunable devices. More importantly, as with the drawback for the broadband reconfigurable PA, this solution does not allow for concurrent amplification of multiple signals operating at different frequencies.

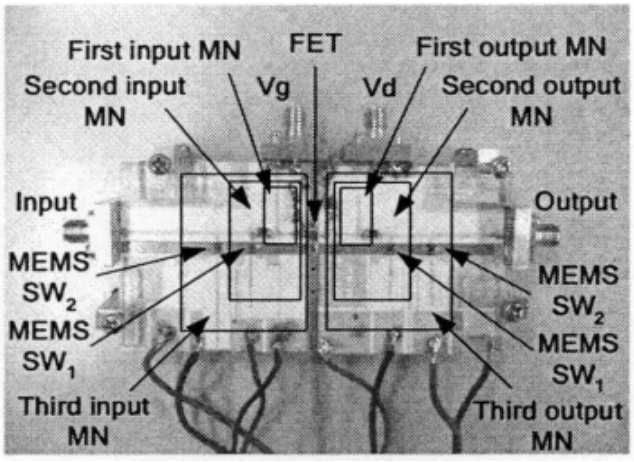


Figure 2.18 Reconfigurable triple-band PA employing RF-MEMS switches [20]

Alternatively, other authors [4][5][6][7][21][22][23][24] have suggested a number of matching networks capable of simultaneously providing necessary impedance transformations at multiple frequencies to enable the design of multi-band power amplifiers. It is worth mentioning that the need for proper impedances at the fundamental frequency and its harmonics (especially second and third harmonics), as imposed by power amplifiers with enhanced power efficiency, renders the design of multi-frequency power amplifiers a very complicated task.

As an example, Kalim and Colantonio et al. [4][5] introduced “impedance buffers” to design a multi-stage, multi-frequency and multi-harmonic matching network. This matching network is implemented in multiple steps and designed MN from the highest frequency to the lowest frequency considering fundamental, second, and third harmonic frequencies. Figure 2.19 shows the circuit topology of the MN using impedance buffer. As can be seen in Figure 2.19, a λ/4 open ended transmission line is added at the end of each matching stage for each frequency to eliminate the impact of subsequent matching network stages. The authors demonstrate the capability of this approach to realize optimal impedances at each fundamental and harmonic frequency. However, it yielded large matching networks and consequently large insertion losses.

A. Cidronali et al. [6] proposed a multi-section impedance transformer, which achieves impedance transformation for multi-frequencies. The multi-section impedance transformer consists of cascading transmission lines with different characteristic impedance and physical length for fundamental

impedances matching, followed by stubs in parallel for harmonic impedances matching, as shown in Figure 2.20. This technique has been applied to design a dual-band PA. However, since the number of stubs and transmission lines need to be increased until enough freedom is provided to achieve the impedance matching at fundamental and harmonic frequencies, this technique has a drawback similar to that described in paper [4][5].

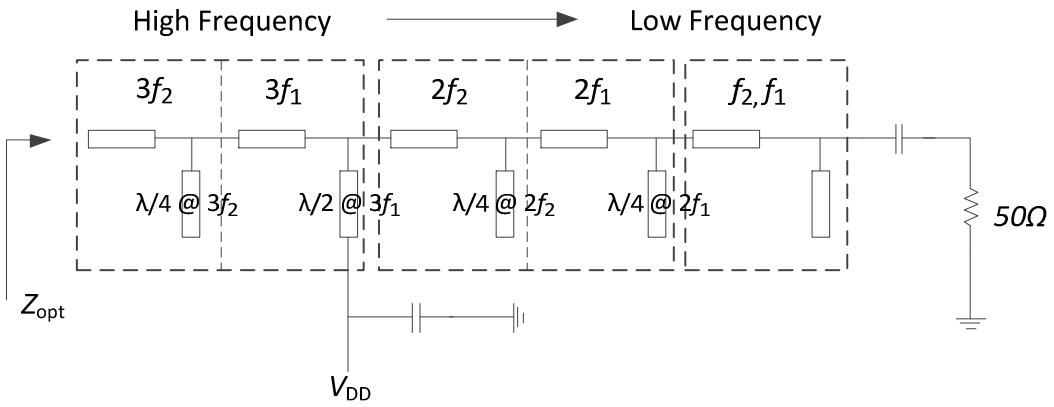


Figure 2.19 Dual-band PA MN using impedance buffer [4]

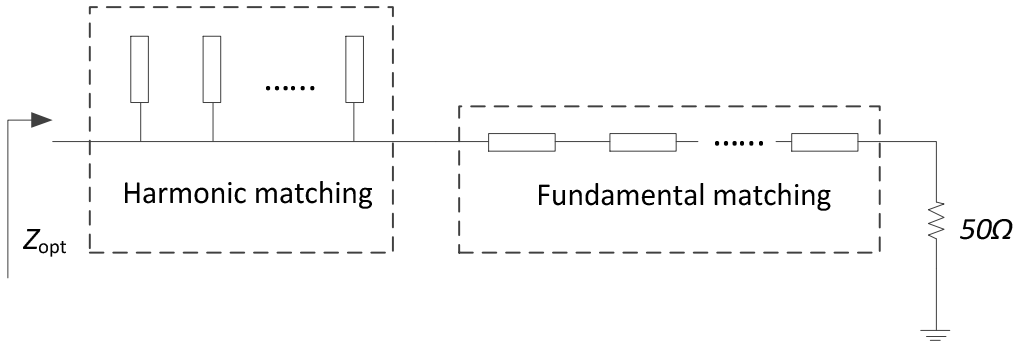
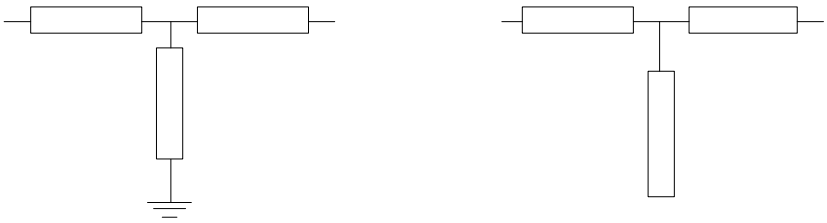


Figure 2.20 Multi-section impedance transformer [6]

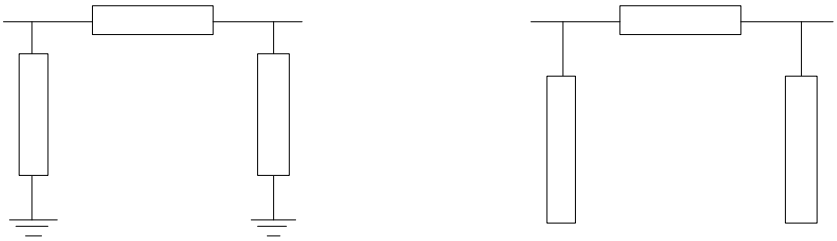
The literature outlines other methods to design a multi-harmonic, multi-band impedance matching network. Rawat et al. [7]proposed dual-band T and Pi type stub loaded quarter-wave transformers, shown in Figure 2.21 and Figure 2.22, respectively. The T/Pi type transformer can achieve the real-to-real impedance transformation from 50 ohm to two different real impedances at two operation frequencies. The derivation and equations to calculate the characteristic impedances of the transmission lines and stubs are introduced. This approach provides a systematic way to realize the real-to-real dual-band impedance matching. However, since this design approach does not control the

harmonic, the PA was not optimized to achieve optimal efficiency. The T-type or Pi-type circuits also have limitations in terms of width and length of transmission lines and stubs. Thus, for a particular frequency ratio and impedance values that need to be transformed to, the T/Pi type transformers do not always guarantee realizable solutions.



(a) T-type with short ended stub (b) T-type with open ended stub

Figure 2.21 Dual-band T-type quarter-wave transformers [7]



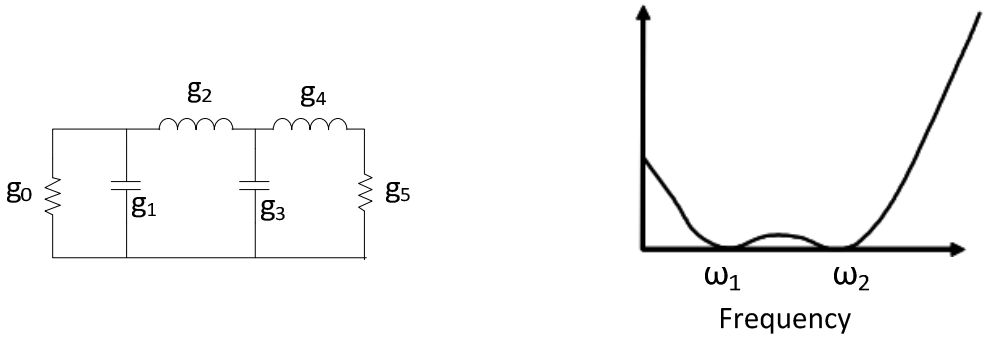
(a) Pi-type with short ended stub (b) Pi-type with open ended stub

Figure 2.22 Dual-band Pi-type quarter-wave transformers [7]

Gao et al. [21] proposed a novel bias line with LC resonator and transmission lines at both gate and drain sides to control the second harmonic for both input and output of the PA at two frequency bands. Although the PA is realized in a compact structure, PA efficiency is still not optimized because the third harmonic is not controlled.

Ding et al. [22] presented an interesting idea to control the second and third harmonic impedances of two frequencies by exploiting the relationships between the harmonic impedances of Class F and inverse Class F. Authors succeeded in presenting the required impedances at the two operating frequencies and their second and third harmonics so that the transistor operates in Class F mode at one frequency band and in inverse Class F mode at the second frequency band. Unfortunately, this adroit technique can be applied only when designing dual-band amplifiers with the two operation frequencies related by the ratio of 1:1.5.

Uchida et al. [23] presented a dual-band PA implemented using low pass Chebyshev-form impedance transformer. It has been proven that the low-pass Chebyshev-form impedance transformer has null attenuation frequencies corresponding to the number of LC ladder circuit stages [25]. Since the impedance transformation can be achieved at null attenuation frequencies, there are N matching frequencies for an N-stage LC ladder circuit. In this paper, a two-stage low-pass Chebyshev-form impedance transformer is designed to realize the dual-band impedance transformation. Figure 2.23 (a) shows the prototype of the LC circuit and Figure 2.23 (b) shows the transmission characteristic. ω_1 and ω_2 are the two target frequencies. However this impedance transformer deals only with real impedances and the harmonics are not controlled.



(a) Low pass impedance transformer (b) Transmission characteristic

Figure 2.23 Low pass Chebyshev-form impedance transformer

An approach called active load modulation was proposed recently, inspired by the Doherty PA concept, to modulate the load of a main amplifier at different frequency ranges while using switches to switch the auxiliary amplifier on and off [24], but again the structure and implementation of the associated methods are complicated.

2.4 Conclusion

This chapter provided an overview of high power amplifiers and included the classes of operation mode and practical issues of PA design. Also, a literature review was provided on broadband PA and multi-band PA. The next chapter will focus on dual-band power amplifier design.

Chapter 3
Dual-Band Power Amplifier Design Approach

In this chapter, a systematic approach for the design of dual-band matching networks is proposed and applied for a power amplifier (PA) capable of concurrently maintaining high power efficiency at two widely spaced frequencies. This approach combines the automated synthesis of a dual-band filter with the relaxed harmonic tuning requirements of the Class-J mode of operation, to systematically design a dual-band PA. In this chapter, first the class of operation is discussed, and then the systematic approach is introduced step by step.

The work in this chapter was previously presented in [26].

3.1 Choice of PA Operation Mode

As discussed in Chapter 2, the Class J mode has good potential and can be successfully applied to the design of a high efficiency broadband PA. The previously mentioned flexibility brought by the Class J design space can be extended to the design of dual-band high efficiency power amplifiers. In fact, designing a dual-band Class B, F, or F^{-1} power amplifier would require the synthesis of optimum impedances at the two fundamental frequencies and their second and third harmonics. Thus, the MN needs to simultaneously match the optimum impedances at six frequencies in total, which may result in very complicated MN-even if feasible. However, benefiting from the Class J design space, the MN will need only to satisfy the impedances at the two fundamental frequencies and limit the matching at the second and third harmonics to a simple harmonic impedance control. Such a control is needed only to avoid the harmonic impedances from being located within a small portion of the edge of the Smith chart; the segment can be determined from the source/load pull characterization of the transistor.

As can be seen from the literature review of dual-band PAs, most techniques that achieve multi-fundamental and multi-harmonics matching suffer from complicated MN structure and thus degrade the drain efficiency of the PA. In this work, the design of dual-frequency matching networks has been tackled in combination with the transistor mode of operation. In fact, the integration of the Class J mode of operation and its attributes has been very influential in the development of the proposed dual-frequency matching network topology and its synthesis. The adoption of the Class J mode of operation significantly reduced the design complexity of the matching network by limiting the explicit matching to the fundamental frequencies and relaxing the requirements on the matching at

harmonics. This complexity reduction enabled the adoption of a systematic methodology in designing the multi-frequency matching networks by exploiting the different techniques devised for automated synthesis of multi-band filters.

3.2 Dual-band Matching Network Design for Package Devices

Benefiting from the previous attributes of Class J design space, the two optimum impedances required for transistor input and output at the two targeted frequencies are determined. Furthermore, the harmonic terminations study helped identify the regions to avoid in the edge of the Smith chart. An effective design of matching network to achieve the targeted impedance relies on the proper choice of the circuit topology and its synthesis methodology. Figure 3.1 shows the proposed topology of the dual-band matching network. Since the optimum impedances needed by packaged transistors are usually complex valued ones, the dual-band matching is performed in two steps, namely real-to-complex and 50ohm-to-real impedance transformations. An additional transmission line is inserted between the two transformation stages to control the second and third harmonic impedances. The following sub-sections describe the synthesis of each stage of the proposed dual-band matching networks.

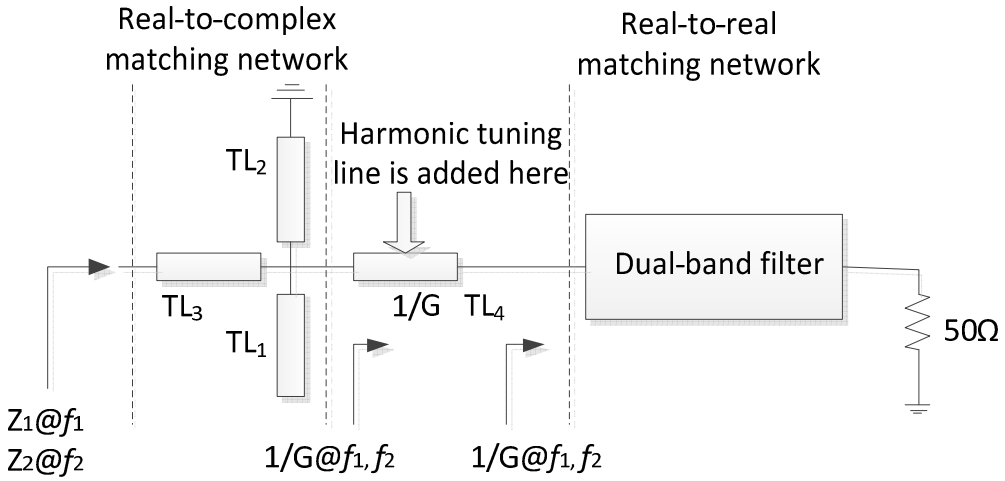


Figure 3.1 Proposed dual-band matching network topology

3.2.1 Real-to-Complex Impedance Transformation

The circuit shown in Figure 3.2 is used to transform the two complex impedances, Z_1 and Z_2, at two operating frequencies, f_1 and f_2, to an intermediate real impedance, R (G=1/R). An open-circuit stub (TL_1), short-circuit stub (TL_2), and transmission line (TL_3) were used to provide enough degrees of

freedom for the realization of this transformation. The method used to choose the resistance value R or conductance value G is discussed later.

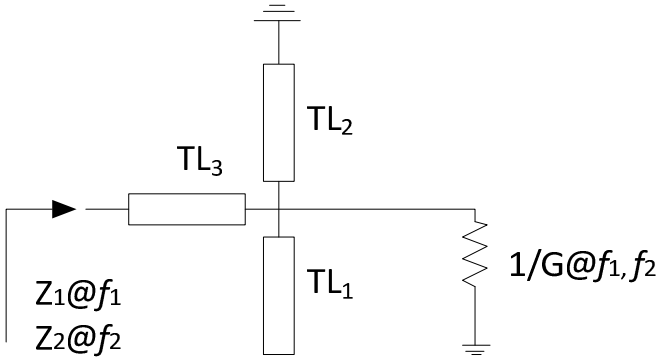


Figure 3.2 Real-to-complex fundamental impedance matching network

Figure 3.3 shows how the matching network transforms the impedances in the Smith chart. The transformation includes two steps:

- Starting with a conductance G, the dimensions of the two open and short stubs are adjusted to attain the two points along a constant conductance circle that are marked with the star symbol in Figure 3.3.
- In the second step, the dimensions of the TL_3 are adjusted so that the two points of the Smith chart that were obtained in the previous step are moved to the target impedances.

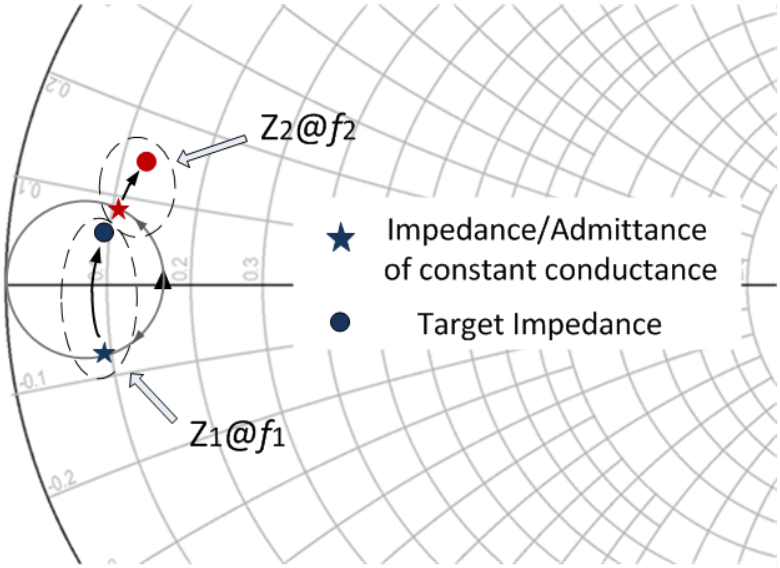


Figure 3.3 Impedance transformation in Smith chart

Having the bandwidth of the matching network as an additional design factor, the choice of the value of G needs to be carefully chosen so that a reasonable quality factor is maintained. The conductance value G should be chosen close to both of the two fundamental impedances so that $G \approx \Re(1/Z_1) \approx \Re(1/Z_2)$. Also, the transmission line (TL_1, TL_2, TL_3) length must be $<< \lambda/4$.

Hence, the impedance transformation of the real-to-complex transformation is relatively low and the bandwidth of the overall dual-band matching network will be dominated by the real-to-real transformation.

It is also worth mentioning that the topology of the real-to-complex impedance transformation is not fixed. The selection of the circuit topology will depend on the position of the two target fundamental impedances. In this work, the topology with one transmission line and two short/open ended stubs is chosen among other topologies because it achieves the minimum transformation while maintaining some design flexibility. In addition, this topology is relatively simple and compact.

3.2.2 Dual-band Real-to-Real Impedance Transformation

The second impedance transformation is designed to match the intermediate conductance G to 1/50 Siemens. As discussed in [26], when transforming impedance over a wide range of frequencies, a matching network has a filter-like characteristic. Benefiting from the established theory of automated synthesis of dual-band filters, the design of dual-band real-to-real impedance matching will be treated as a dual-band filter synthesis problem where the impedances of the dual-band filter ports are equal to 1/50 Siemens and G, at the two operating frequencies.

Step 1: Low pass filter to single-band pass filter

The filter design begins with the determination of the low pass filter prototype in Figure 3.4. The *g* values of the low pass filter prototype are chosen from the g-table of the Chebyshev filter, given in [26], where the filter order was set to 1. In fact, a higher order filter will result in higher insertion losses for unnecessary high roll-off.

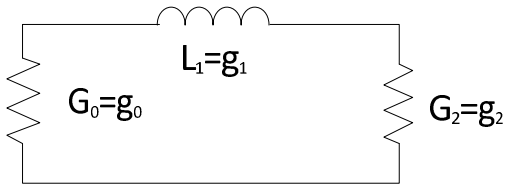


Figure 3.4 Prototype of low pass filter

The low pass filter prototype is first transformed into a single-band pass filter, where the center frequency f_0 is equal to the average of the two working frequencies f_1 and f_2. For that the inductor L_1 needs to be transformed into an LC series resonator that resonates at $f_0 = \omega_0/2\pi$ as is shown in Figure 3.5. Such a series resonator is not suitable for micro strip line realization. Hence, a series resonator to shunt resonator (C_2, L_2) transformation using a J-inverter (J_1 and J_2) is applied as shown in Figure 3.6. The two J inverters are also used to realize the admittance transformation from G to 1/50 Siemens, where G is the intermediate conductance value chosen in the real-to-complex matching network.

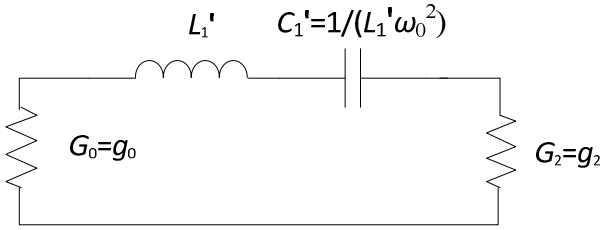


Figure 3.5 Single-band pass filter with LC series resonator

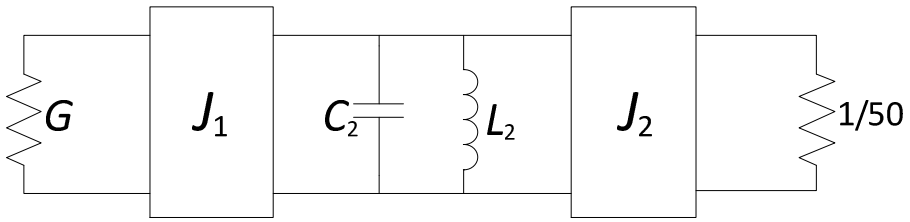


Figure 3.6 Single-band pass filter with LC parallel resonator and J inverters

In Figure 3.6, the values of J_1, J_2 and C_2, L_2 are calculated using the following expressions. The generalized equations for N-th order single-band pass filter are given in [26]:

$$J1 = \sqrt{\frac{FBWs \times G_A \times b_2}{g_0 g_1}} \tag{3.1}$$

$$J2 = \sqrt{\frac{FBWs \times G_B \times b_2}{g_1 g_2}} \tag{3.2}$$

$$w_0 = 2\pi f_0 \tag{3.3}$$

$$f_0 = \frac{f_1 + f_2}{2} \tag{3.4}$$

where G_A = G, and G_B = 1/50 Siemens, and FBWs is the fraction bandwidth of the single-band pass filter. b_2 is the susceptance slope parameter of the LC resonator, which is defined as

$$b_2 = \frac{w_0}{2} \cdot \frac{\mathrm{dB}_2}{\mathrm{d}w} \quad \text{(mhos)} \tag{3.5}$$

where B_2 is susceptance of the parallel LC resonator. It can be calculated that b_2 in this circuit is

$$b_2 = w_0 \times C_2 = \frac{1}{w_0 \times L_2} \tag{3.6}$$

The value of b_2 is not fixed and can be chosen provided that Equation 3.6 is satisfied. It will be used later to facilitate harmonic impedances control as discussed in the following sub-section.

Step 2: Single- band pass filter to dual-band pass filter

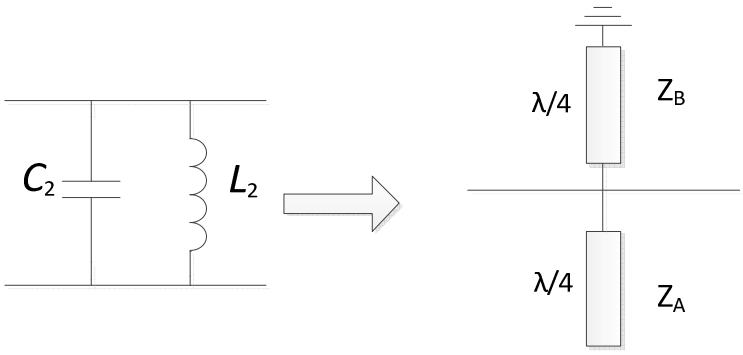
The next step is to convert the lumped-elements single-band pass filter in Figure 3.6 to a distributed-elements based dual-band pass filter, with two center frequencies f_1 and f_2. For that, the single frequency resonator and J inverters in Figure 3.6 need to be transformed in to dual-band elements. Figure 3.7 and Figure 3.8 show the transformation from a single-band resonator to a dual-band resonator and the transformation from a single-band J inverter to a dual-band J inverter [27]. The dual-band resonator is realized using an open-ended λ/4 stub that behaves like series LC, in parallel with a short-ended λ/4 stub that behaves like parallel LC. Here, λ is the wavelength at the frequency of f_0. To achieve the correct impedance transformation at both frequencies, the parameters of the dual-band J inverter shown below are determined using the following equations [27]:

$$Z_A = \frac{1}{4f_0C_2} cosec^2\left(\frac{\pi}{2} \times \frac{f_2 - f_1}{f_2 + f_1}\right) \tag{3.7}$$

$$Z_B = \frac{1}{4f_0C_2} sec^2\left(\frac{\pi}{2} \times \frac{f_2 - f_1}{f_2 + f_1}\right) \tag{3.8}$$

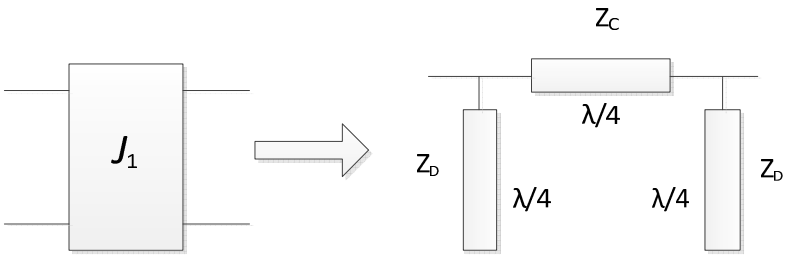
$$Z_C = \frac{1}{Jcos(\frac{\pi}{2} \times \frac{f_2 - f_1}{f_2 + f_1})} \tag{3.9}$$

$$Z_D = \frac{1}{Jsin(\frac{\pi}{2} \times \frac{f_2 - f_1}{f_2 + f_1}) \times tan(\frac{\pi}{2} \times \frac{f_2 - f_1}{f_2 + f_1})} \tag{3.10}$$



(a) (b)

Figure 3.7 Single-band resonator (a) to dual-band resonator (b) [27]



(a) (b)

Figure 3.8 Single-band J inverter (a) to dual-band J inverter (b) [27]

Figure 3.9 shows the resulting dual-band filter used to realize the dual-band real-to-real matching network. It is worth mentioning that the different circuit transformations applied to obtain the final dual-band real-to-real matching allow for a step-by-step design process in which the circuit parameters are chosen to satisfy the impedance transformation ratio and the requirements in terms of bandwidth around the two carrier frequencies.

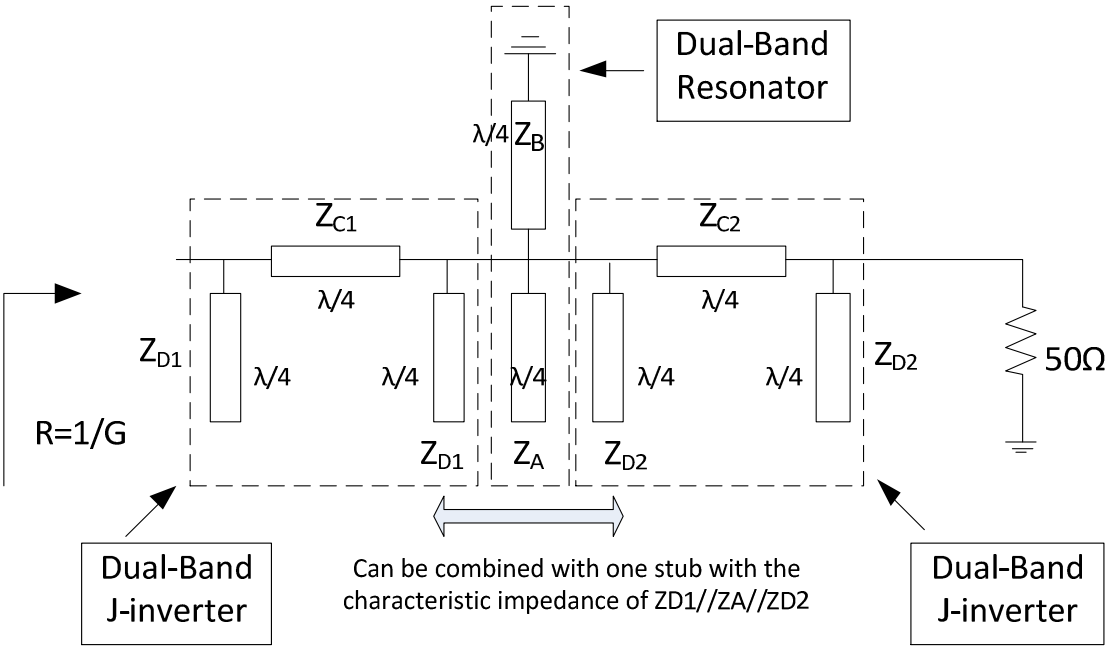
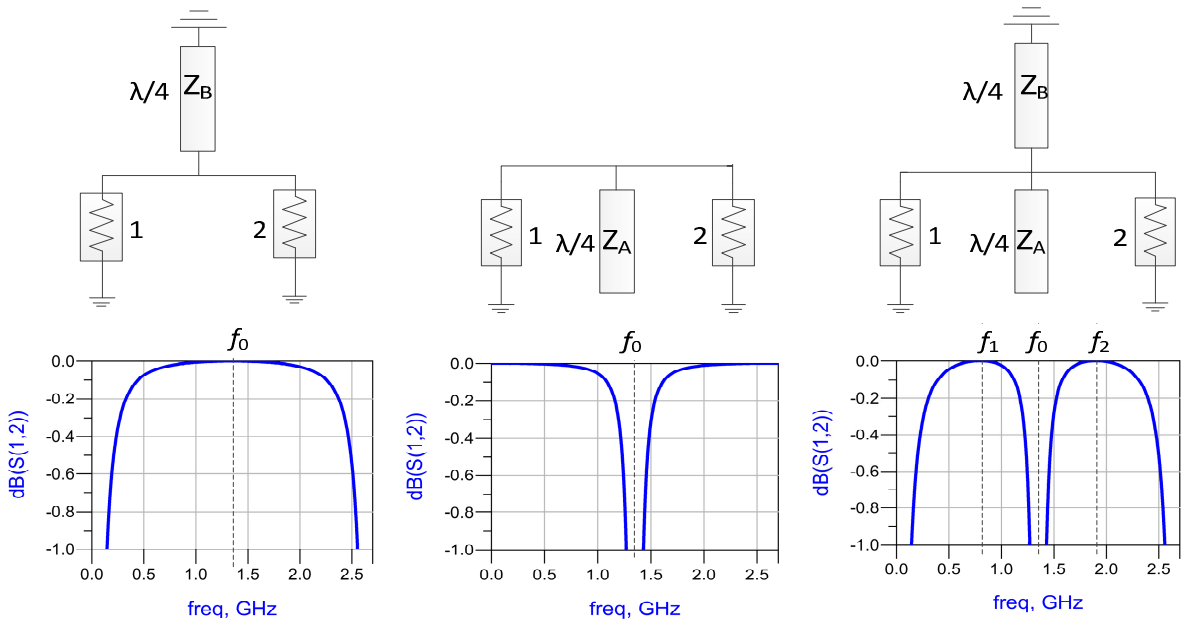


Figure 3.9 Circuit topology of real-to-real impedance matching network

Dual- band characteristics discussion

As introduced in Step 2, the dual-band resonator, which is composed of a short-ended quarter wave stub in parallel with an open-ended quarter wave stub, is applied to achieve the dual-band pass transmission at f_1 and f_2. This topology has a dual-band transmission characteristic because it has a band pass structure, which is the short-ended quarter wave stub, and a band stop structure, which is the open-ended quarter wave stub. When aligning the center frequency of the band pass structure and band stop structure to be at f_0 and properly control the bandwidth, the combined structure can achieve a dual-band pass characteristic. Figure 3.10 illustrates the band pass frequency response of the short-ended stub, the band stop frequency response of the open-ended stub and the dual-band pass frequency response of the combined structure.



(a) Short-ended quarter wave stub (b) Open-ended quarter wave stub (c) Combination of the two

Figure 3.10 Frequency response of band pass (a), band stop (b) and dual-band pass (c) topology

Bandwidth discussion

The relationship of the bandwidth of the single-band pass filter with a parallel LC resonator and the bandwidth of the dual-band pass filter with distributed elements needs to be discussed. In this design, we transform the lumped LC resonator directly to the distributed element dual-band resonator. Actually, there is a hidden step in between, which is the dual-band lumped element resonator shown in Figure 3.11. To implement the circuit in Figure 3.11 using distributed elements (transmission line), the LC in parallel can be realized by a quarter-wave short stub and the LC in series can be realized by a quarter-wave open stub. Thus, we end up with the dual-band resonator shown in Figure 3.7 (b). The fractional bandwidth factor (FBW) is defined for the single-band pass filter (FBW_{single}), and it will retain a linear relationship with the FBW of the dual-band filter using LC resonators (FBW_{dual}), which is

$$\mathrm{FBW_{dual}} = \mathrm{FBW_{single}} \times \frac{f_2 - f_1}{f_2 + f_1} \tag{3.11}$$

However, since the susceptance values of the lumped element circuit and distributed element circuit are different, the FBW of the dual-band filter with distributed elements will change during the transformation from lumped elements to distributed elements.

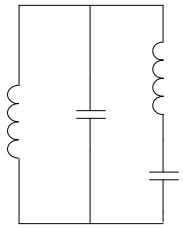


Figure 3.11 Dual-band resonator realized by lumped elements

Figure 3.12 shows the imaginary part of the dual-band resonator admittance (or susceptance), implemented by lumped elements and by distributed elements respectively. It can be seen that for lumped elements, the susceptance changes more slowly at the higher band (f_2) than at the lower band (f_1) and both bands share the same fractional bandwidth. However, in the distributed element's case, the slope of susceptance around each band is the same, thus indicating the same bandwidth for both bands and, hence, different FBWs.

This analysis shows that the FBW factor set in the single-band pass filter design will not be the FBW of the dual-band filter using distributed elements; however, this fact does not mean that the bandwidth of the designed dual-band filter is out of control. It is found that the bandwidths of the designed dual-band filter at both bands are directly related to the FBW of the single-band pass filter; therefore, the bandwidth can still be controlled by adjusting the FBW factor in filter design.

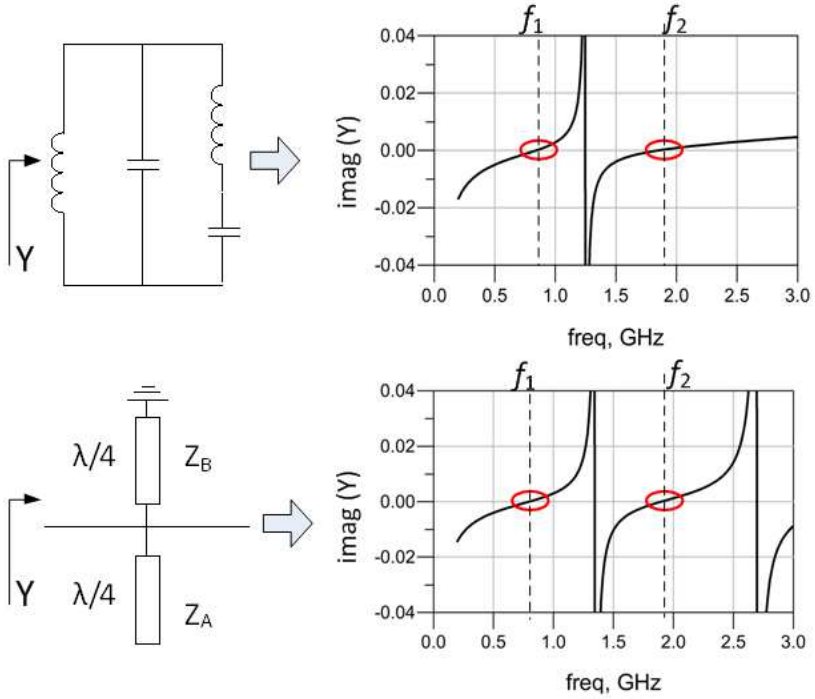


Figure 3.12 Imaginary part of admittance for dual-band resonator, using lumped element (top) and distributed element (bottom)

Realizability discussion

The realizability of the circuit topology should always be considered for practical design. For transmission lines or stubs, the realizability depends mainly on the dimension, which is the length and the width that are determined by transmission lines' characteristic impedance and electrical length. In our case, the electrical length of each transmission line or stub of real-to-real impedance MN has been fixed to 90 degrees, which is usually realizable, so the analysis is focused on the range of characteristic impedance values, which can be calculated from Equations 3.6 to 3.9.

Figures 3.13 to 3.15 show the characteristic impedances of Z_A, Z_B, Z_{C1}, Z_{C2}, Z_{D1}, and Z_{D2} of the real-to-real impedance MN in Figure 3.9 versus the ratio of the two operating frequencies (f_2/f_1). Since the three stubs with characteristic impedances of Z_A, Z_{D1}, and Z_{D2} in parallel will be combined into one stub, the value of $Z_A//Z_{D1}//Z_{D2}$ versus f_2/f_1 is considered (Figure 3.16). The impedance transformation is from 8.3ohm to 50ohm, and the FBW parameter in Equation 3.1 and 3.2 is set to be 0.2, which is a reasonable value in practical cases.

Transmission lines with very high characteristic impedance may end up with very narrow width and are difficult to fabricate. On the other hand, transmission lines with very low characteristic impedance may become too wide. The realizable characteristic impedance should not be lower than approximately 8 ohm nor higher than approximately 120 ohm. The exact range will depend on the substrate that is used for designs.

According to Figures 3.13 to 3.16, it can be seen that when the ratio of f_2 to f_1 is high, the value of each transmission line or stub remains within the realizable range. However, when f_2/f_1 is approaching 1, which means the two operating frequencies are close to each other, Z_{C1} becomes too low, and Z_{D1}, Z_{D2}, $Z_A//Z_{D1}//Z_{D2}$ become extremely high, indicating that this MN topology is difficult to realize by transmission lines or stubs.

The dimension analysis shows that this approach has feasible solutions when the two operating frequencies are far from each other; however, when the two frequencies are close to each other, a feasible solution may not be guaranteed. This limitation will not affect the application of this topology very much because the dual-band MN topology always targets frequencies that are far away from each other. If the two operating frequencies are close to each other, then the broadband MN topology, rather than the dual-band topology, should be chosen for designs.

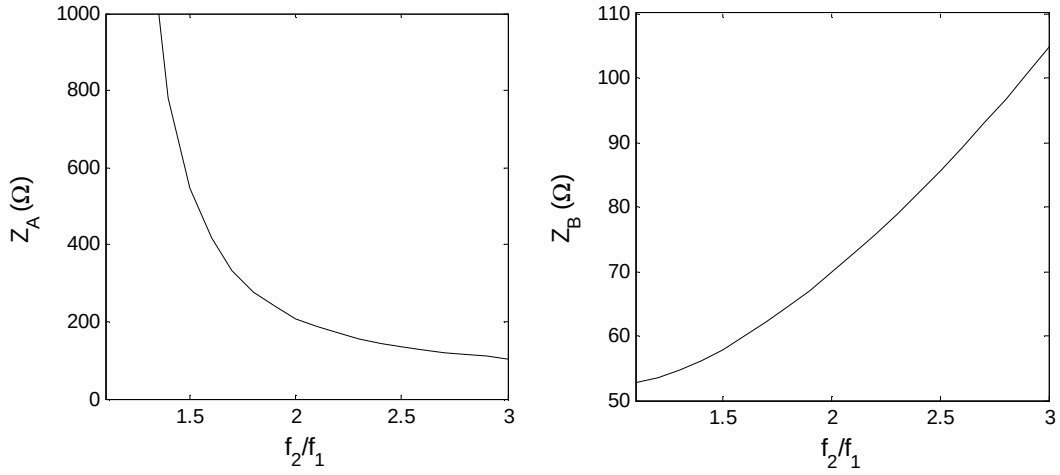


Figure 3.13 Z_A and Z_B vs. f_2/f_1

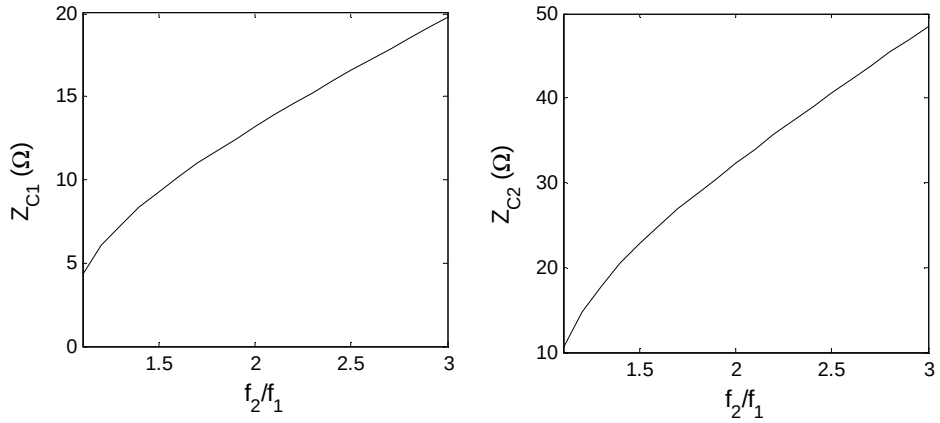


Figure 3.14 Z_{C1} **and** Z_{C2} **vs.** f_2/f_1

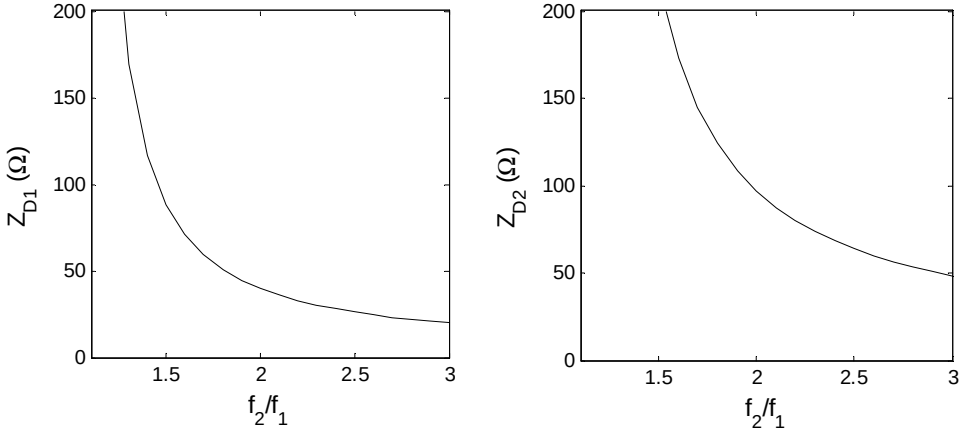


Figure 3.15 Z_{D1} **and** Z_{D2} **vs.** f_2/f_1

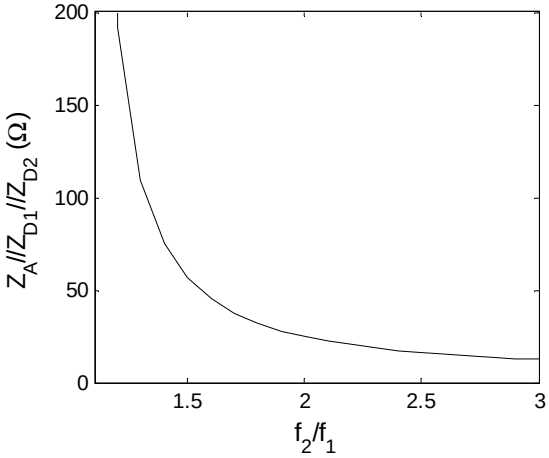


Figure 3.16 $Z_A//Z_{D1}//Z_{D2}$ **vs.** f_2/f_1

3.2.3 Harmonic Impedance Controls

The previous two sub-sections described the details of the topology and synthesis of the dual-band matching network that allow the realization of the optimum impedances at two frequencies without any specific control on the resulting harmonic impedances. However, as previously stated, a high efficiency can be obtained if the fundamental impedances are chosen within the Class J design space so that the sensitivity of the efficiency to the harmonic impedance variation is reduced. In fact, the efficiency drops significantly over only a small range of the phase of the reflection coefficient seen by the transistor at the harmonics and remains within an acceptable range over a wide range of phases. Hence, as shown in Figure 3.1, a transmission line (TL_4) with a characteristic impedance equal to Z_0=1/G is added between the real-to-real and the real-to-complex impedance transformations to tune the harmonic impedances. This tuning is achieved through the adjustment of the length of the added transmission so that the impedances at $2f_1$, $3f_1$, $2f_2$, and $3f_2$ are located outside of the sensitive region predicted by the Class J operation. It is worth mentioning that the choice of the value of parameter b_2 in Equation 3.3 to 3.6 is used as an additional degree of freedom to help with the achievement of the proper harmonic impedances. In fact, b_2 can take an arbitrary value in the real-to-real impedance transformation; however, adjusting its value has a direct effect on the tuning range of the harmonic impedances for a given value of the length of TL_4. Since the impedance looking into the real-to-real matching network is 1/G, adding this TL_4 line, which has characteristic impedance equal to 1/G, will not affect the fundamental impedance matching while tuning the harmonic impedances.

Figure 3.17 illustrates how impedances of second ($2f_1$, $2f_2$) and third harmonic ($3f_1$, $3f_2$) may change with and without the transmission line TL_4 while the fundamental impedances (f_1, f_2) remain the same.

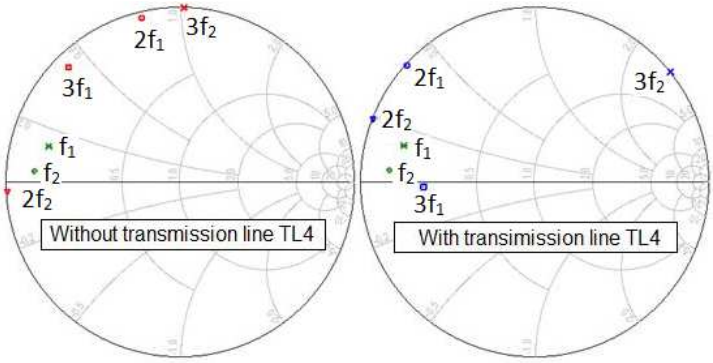


Figure 3.17 Illustration of harmonic impedances control

3.2.4 Biasing Approach of Dual-band PAs

DC power supplies need to be connected to the gate and drain of the transistor to control its operation mode and supply the power. Usually, the DC power supplies connected to an RF short-ended quarter wave transmission line (Figure 3.18) provide an open circuit at RF frequency. Thus, this biasing network prevents the DC supplies from being interrupted with RF signals. Also, the biasing the circuit will not affect MN at the RF fundamental frequency. This approach works for single-band-frequency PA design; however, using the same topology cannot prevent the interruption between DC and RF signals at two frequencies. An alternative approach would be to replace the single-frequency quarter-wave transmission line with dual-frequency quarter-wave transmission lines; however, this approach increases the complexity of the biasing circuit and may not be necessary. In this design, we took advantage of the RF short-ended stubs in the MN and used these stubs to connect with the DC power supply. Thus, the RF signal is prevented from going through the biasing circuit, and the load and source matching at fundamental and harmonic frequencies will not be affected by the biasing circuit. The entire dual-band PA topology with biasing circuit is shown in Figure 3.19. Note that a parallel RC circuit was added in series and in shunt with the transistor to ensure the stability of the transistor at the low frequency range.

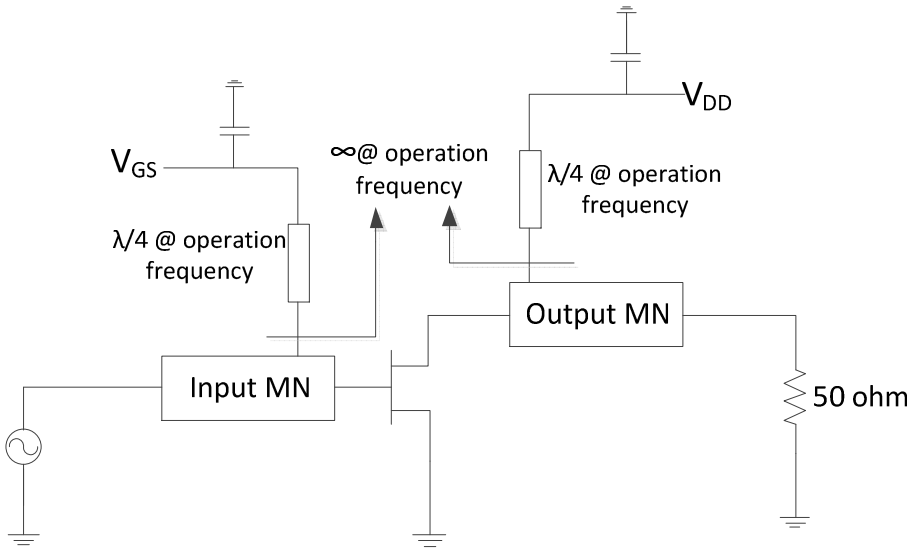


Figure 3.18 Biasing circuit for single-band PA

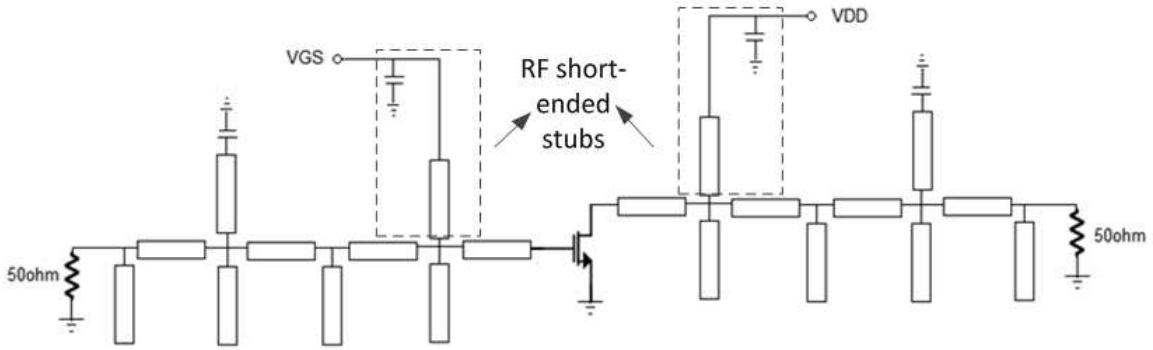


Figure 3.19 Dual-band PA topology with biasing circuit

In Chapter 4, a dual-band PA operating at 0.8GHz and 1.9GHz is designed using this systematic approach. The detailed design procedure is presented in Chapter 4.

3.3 Revised Dual-band Matching Network Design Approach for Transistor Die

The systematic MN design approach presented in previous sections is divided into two parts: the real-to-complex MN and the real-to-real MN. However, for a transistor die, its output can be modeled as a resistor (Rout) in parallel with a capacitor (Cds). This is a much simpler model and provides a better chance to integrate the real-to-complex MN part into the whole dual-band filter; thus, the entire MN design will become a dual-band filter design. The advantage of merging the real-to-complex MN into the dual-band filter is that we can have better control of the bandwidth and insertion loss of the entire MN. The suggested revised dual-band MN design is introduced as follows.

Assuming a dual-band filter has the topology shown in Figure 3.20, which contains dual-band resonators and dual-band J inverters, then, if Y_0 is chosen as the output resistor Rout and C_{11} is equal to or larger than Cds, the transistor with Cds can be merged into the entire filter design.

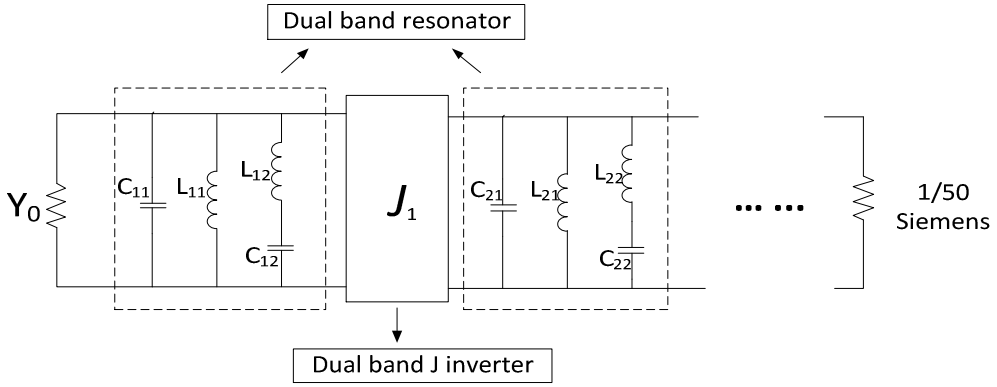


Figure 3.20 Possible dual-band pass filter topology

Guan et al. [28] analyzed a dual-band filter with a topology similar to that in Figure 3.20. If C_{11} is set equal to Cds, then L_{11}, L_{12} and C_{12} can be calculated once the two working frequencies and fractional bandwidth are chosen.

According to the relationship of the values of LC elements in dual-band resonators and single-band resonators during the transformation between the dual-band pass filter and the single-band pass filter, the value of C_1 and L_1 of the single-band pass filter shown in Figure 3.21 can be determined according to the value of C_{11} (or C_{12}, L_{11}, L_{12}), two working frequencies, and FBW. Consequently the value of g_1 in the low pass filter prototype shown in Figure 3.22 can be determined according to C_1.

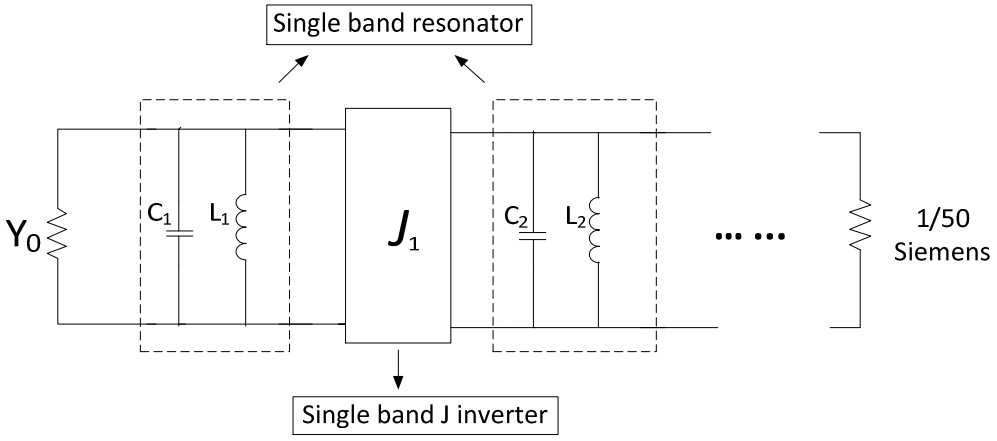


Figure 3.21 Single-band pass filter topology

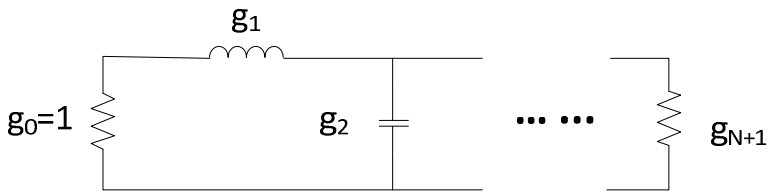


Figure 3.22 Low-band pass filter topology

Therefore, other than starting with g values that can be chosen from tables given in [26], we determined the other g values according to the two fixed parameters, which are g_0 and g_1.

Matthaei et al. [26] has proven that given the requirement of the ripples, the other g values of a low pass filter can be calculated.

First define

$$H = antilog_{10}\frac{(db\ Chebyshev\ ripple)}{10} \tag{3.12}$$

$$d = sinh\frac{sinh^{-1}\sqrt{\frac{1}{H-1}}}{n} \tag{3.13}$$

where n is the number of reactive elements in the prototype.

To characterize the fixed load of the filter (g_0 and g_1), its decrement δ is defined in Equation 3.14.

$$\delta = \frac{1}{g_0 g_1 w_1} \tag{3.14}$$

where g_0 and w_1 are normalized to 1. The meaning of decrement δ is the reciprocal of the quality factor (Q) of the load evaluated at the edge of the impedance matching band.

Then define

$$D = \frac{d}{\delta \sin(\frac{\pi}{2n})} - 1 \tag{3.15}$$

Also,

$$D = \frac{g_0 g_1}{g_{n+1} g_n} \tag{3.16}$$

Thus, the following g values can be calculated as

$$g_{n+1} = \frac{1}{D\delta g_n w_1} \tag{3.17}$$

Once all the g values have been chosen for the low pass filter, a low pass filter to single-band pass filter transformation and consequently single-band pass filter to dual-band pass filter transformation can be conducted. The dual-band resonator and dual-band J inverter topology in Figure 3.7 and 3.8 can still be employed to transform lumped elements to distributed elements.

Chapter 4
0.8GHz and 1.9GHz Dual-band PA Design

To validate the proposed dual-band matching network topology and synthesis, a dual-band amplifier is designed using a packaged 45W GaN HEMT transistor from Cree to operate at 800 MHz and 1.9 GHz. In this chapter, a step-by-step design procedure applying the systematic dual-band MN design approach is presented. The entire PA prototype is shown and measurement results using both continuous wave (CW) and modulated signal are shown.

The work in this chapter was previously presented in [26].

4.1 Dual-band PA Design Procedure

4.1.1 Choosing the Target Fundamental Impedance and Design Space

The first step is to determine the optimum two impedances to be seen by the transistor at the two target frequencies, 0.8GHz and 1.9GHz. These impedances are chosen from the set of impedances described by the Class J design space that minimize the sensitivity to the harmonic termination. The output power needs to be monitored. In addition, as discussed in Section 3.2, the conductance value G needs to be as close as possible to the two fundamental impedances in the Smith chart so that the bandwidth of the total matching network is dominated by the real-to-real MN; thus, the two impedances are chosen such that they are close to the same constant conductance circles to facilitate the complex to real transformation. Also, stability at the operation frequencies needs to be checked. If the impedance is in or near to the unstable region, some compromise is required to move the target impedance away from the unstable region since a high efficiency PA at operation frequency cannot afford to be stabilized by adding a resistor. The fundamental impedances are chosen as follows:

Table 4-1 Target fundamental impedances

Impedance	0.8GHz	1.9GHz
Load side	5.85+j6.6	4+j1.9
Source side	4.68+j3.66	2.1-j2.7

The design space for the phase of harmonic impedance can be found after selecting the fundamental impedances. Figure 4.1 shows the simulation results of PAE versus the phase of Γ at the second harmonic frequency of the load side at 0.8GHz in an all ideal case as an example. As shown in

the figure, PAE dropped more than 40% between 150 degrees and 250 degrees, whereas in other ranges, PAE will remain almost the same, which is around the maximum value. Thus, the design space for the second harmonic phase at the 0.8GHz load side should be within 0-150 degrees and 250-350 degrees. A similar type of design space is noticed in other harmonic frequencies as well.

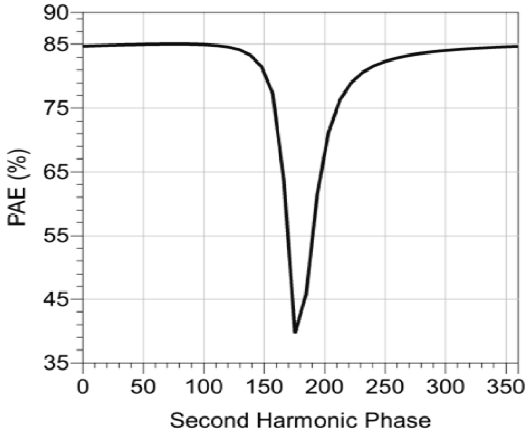


Figure 4.1 PAE vs. phase of the load second harmonic impedance at 0.8GHz

4.1.2 Real-to-Complex Matching Network Design

Given the two selected fundamental impedances and the outcomes of the sensitivity analysis to the harmonic terminations, the dual-band MN can now be designed starting with the real-to-complex MN portion. The previously described synthesis approach was applied. For that, the intermediate conductance G value was set to be equal to 1/8.3 and 1/6 Siemens for the load and source sides respectively.

The designed real-to-complex MN topology was shown in Figure 3.2. These ideal transmission lines will be transformed to actual transmission lines. The MN transforms 8.3 ohm to the two optimal impedances shown in Table 4-1 at the load side and transforms 6 ohm to the two optimal impedances shown in Table 4-1 at the source side. The characteristic impedance and electrical length of the MN at the load side is shown in Table 4-2. The source side can be designed likewise.

Table 4-2 Dimension of real-to-complex MN at the load side

Load side	Characteristic impedance (ohm)	Electrical length (degree)
TL1	43.6	57.6
TL2	77.2	12.2

TL3	14.4	18.6

4.1.3 Real-to-Real Matching Network Design

The real-to-real matching network is designed using dual-band filter theory to transform 1/G to 50ohm at two operation frequencies 0.8GHz and 1.9GHz. As introduced in subsection 3.2.2, first a low pass filter will be transformed to a single-band pass filter, and then a single-band pass filter will be transformed to a dual-band pass filter. This subsection describes the implementation procedure of the load side in detail.

A. Low pass filter

The g values are chosen as $g_0=g_2=1$, $g_1=0.1128$ for the low pass filter shown in Figure 3.4. Figure 4.2 shows the filter response.

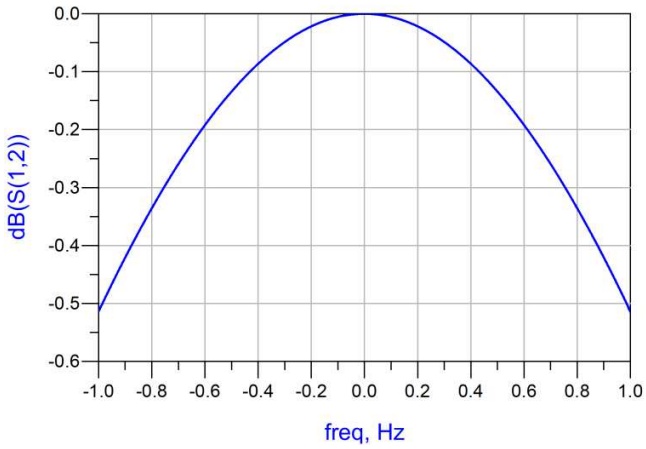


Figure 4.2 Low pass filter response (order 1)

B. Single- band pass filter

A single-band pass filter is then transformed from a low pass filter using the topology shown in Figure 3.6. The J inverter can be realized with a quarter-wave transmission line. C_2 in Figure 3.6 is calculated to be 3.54pF; L_2 is calculated to be 3.93nH; J_1 and J_2 are 0.079 and 0.032 Siemens, respectively. The center frequency is (0.8+1.9)/2=1.35GHz. The impedance transformation is from 50 ohm to 1/G, which is 8.33 ohm for the load side. Fractional bandwidth FBW is set to be 0.2. Figure 4.3 shows the frequency response of the single-band pass filter.

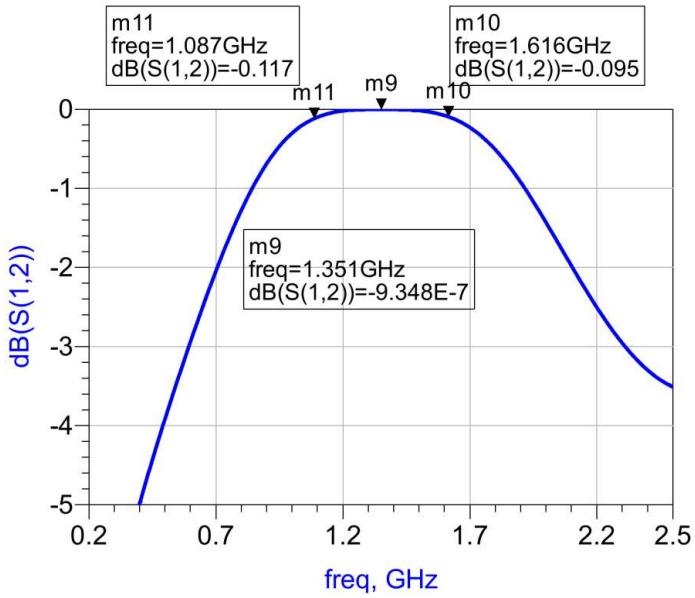


Figure 4.3 Frequency response of single-band pass filter

C. Dual-band pass filter

A dual-band pass filter is then transformed from a single-band pass filter to transforms 50 ohm to 8.33 ohm at 0.8GHz and 1.9GHz concurrently. A dual-band resonator and dual-band J inverter are used as discussed in Section 3.2.2 in Chapter 3. A dual-band pass filter is designed using the topology shown in Figure 3.9. The characteristic impedance of each quarter-wave stub in Figure 3.9 is shown in Table 4-3. Figure 4.4 shows the frequency response of the designed dual-band pass filter. Figure 4.5 shows the impedance looking into the dual-band pass filter with 50ohm termination. It can be seen that the MN designed with dual-band filter topology transforms 50 ohm to 8.33 ohm at both operating frequencies.

Table 4-3 Characteristic impedances of quarter-wave stubs (units: ohm)

Z_A	Z_B	Z_{C1}	Z_{C2}	Z_{D1}	Z_{D2}
81.38	81.38	15.75	38.58	28.41	69.6

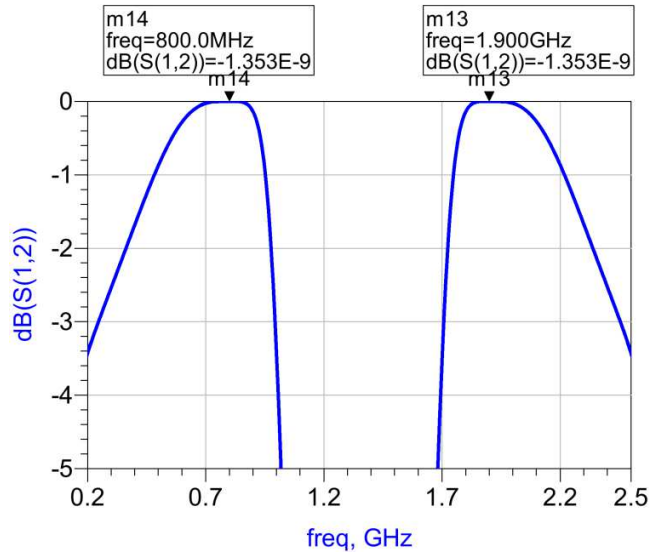


Figure 4.4 Frequency response of the dual-band filter

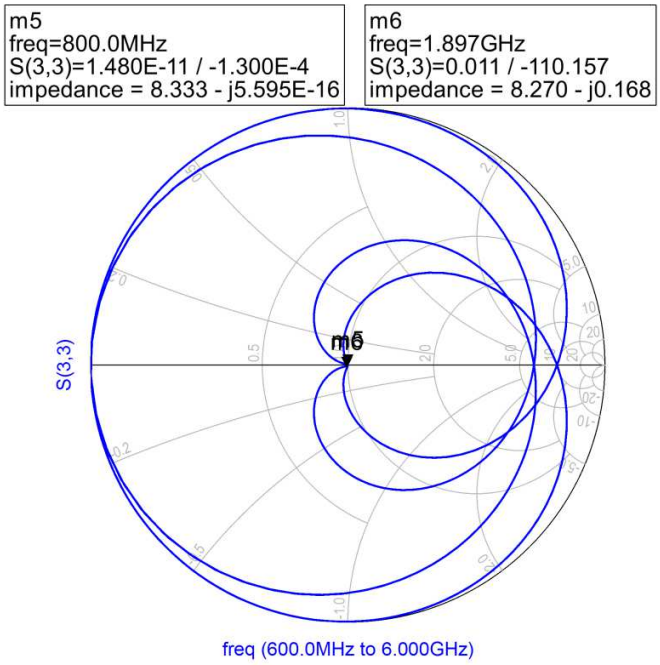


Figure 4.5 Impedance transformation of the dual-band filter

Figure 4.6 shows the targeted and actual fundamental impedances obtained by the dual-band source and load matching networks. The good agreement between the target and obtained impedances

confirms the ability of the proposed topology to concurrently synthesize the correct impedances at different frequencies with good accuracy.

The finalized dual-band PA is designed and fabricated using Duroid 6006 substrate and the prototype is shown in Figure 4.7.

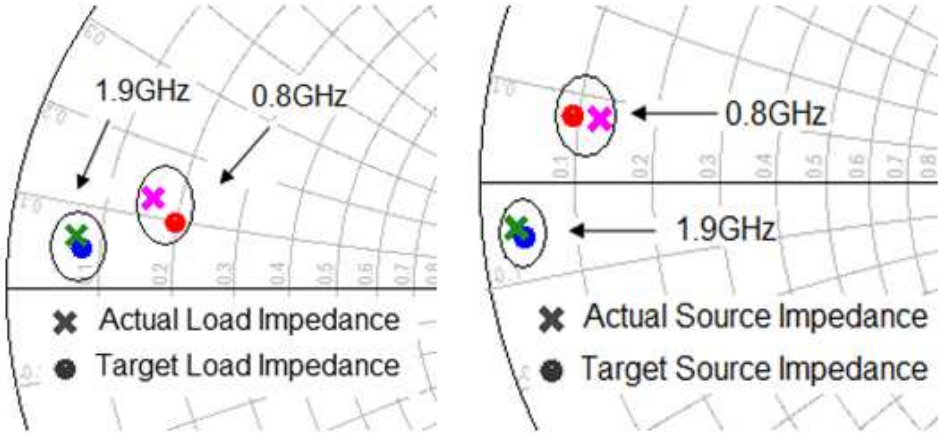


Figure 4.6 Target fundamental impedances and the actual fundamental impedances

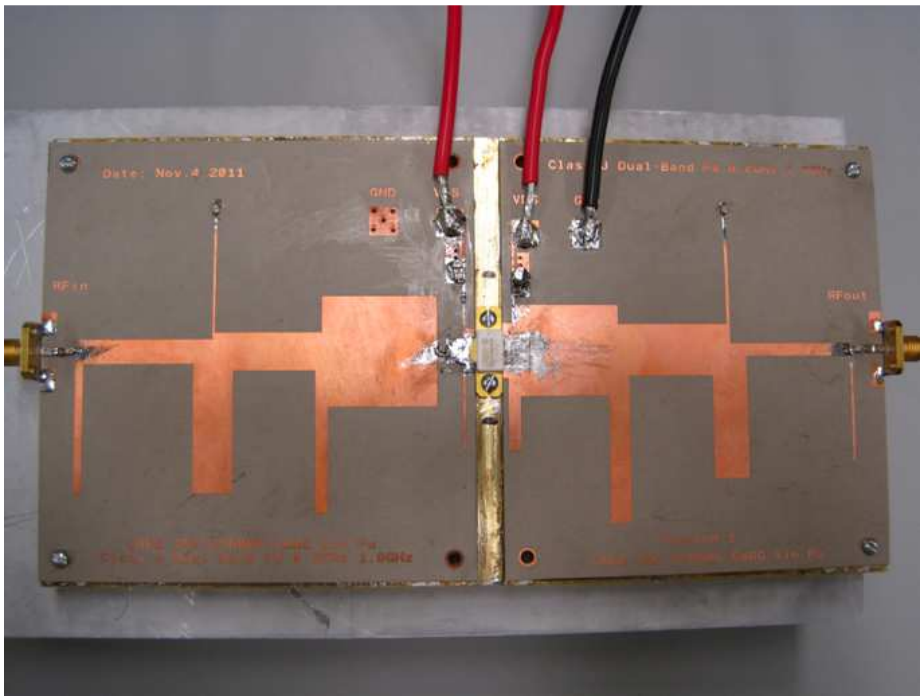


Figure 4.7 Fabricated dual-band PA

4.2 Measurement Results

4.2.1 Continuous Wave Measurement

Power amplifier performance was initially measured using a continuous wave stimulus. According to Figure 4.8 and Figure 4.9, the measurements of the drain efficiency and output power for both operating frequencies 0.8 GHz and 1.9 GHz are in relatively good agreement with the simulation ones except for the frequency shift experienced at the higher band. This shift can be attributed to the lack of accuracy in MN fabrication and transistor model. In addition, a drain efficiency and output power of about 68% and 46 dBm were recorded at the two bands.

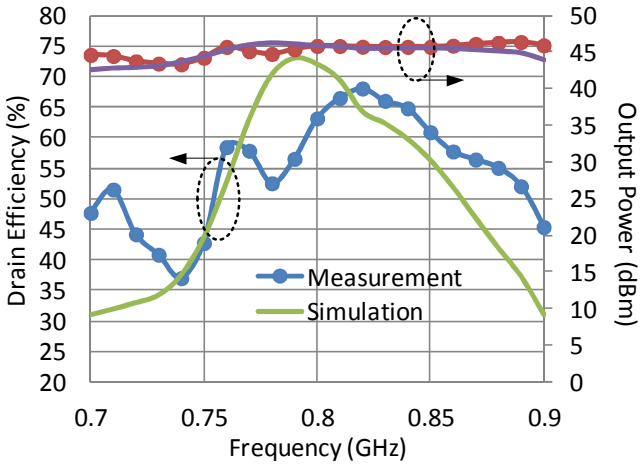


Figure 4.8 Output power and drain efficiency for the lower band (0.8 GHz)

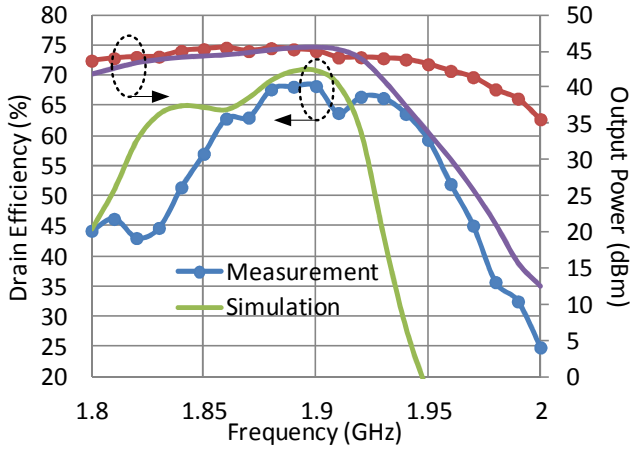


Figure 4.9 Output power and drain efficiency for the upper band (1.9 GHz)

4.2.2 Modulated Signal Measurement

Further measurements were conducted using different types of modulated signals in order to assess the linearizability of the designed dual-band power amplifier. For that, a digital predistortion (DPD) technique was chosen, more precisely, a Volterra series Dynamic Deviation Reduction (DDR) digital predistortion [29] with a nonlinearity degree equal to 5 and a memory depth equal to 7, 5 and 3 for the 1st, 3rd and 5th kernels, respectively. The dynamic order reduction of the Volterra series was set to 2 (r=2).

In addition, the linearizability assessment was conducted while stimulating the PA under test with three types of signals modulated around either 800 MHz or 1.9 GHz. The first signal is a four-carrier 20MHz WCDMA signal with a 7.15dB peak to average power ratio (PAPR). The second test signal is a two-carrier WCDMA signal with 15 MHz frequency separation and a PAPR equal to 7.12 dB. The third signal is a 10 MHz LTE signal and a PAPR of 9.17 dB.

Figures 4.10, 4.11, 4.12 and 4.13 show the measured power spectrum density (PSD) at the PA output before and after applying the DPDs. According to Figure 4.10, the application of the Volterra DPD to linearize the PA when driven with the four-carrier WCDMA signal around 800 MHz allowed for an ACPR of about 50 dBc at an output power and an average drain efficiency of about 39 dBm and 35%, respectively.

In Figure 4.11, the Volterra DPD linearized the PA with the same signal but at around 1.9 GHz and achieved ACPR of about 51.7 dBc at an output power and an average drain efficiency of 38.7 dBm and 39.4%, respectively. Similarly, as per Figure 4.12, the Volterra DPD was also able to linearize the PA when driven with the two-carrier WCDMA signal around 1.9 GHz for the same average power; the achieved ACPR at this power level was about 50.7 dBc.

Figure 4.13 confirms the successful linearization of the PA when driven with a 10 MHz LTE signal, around 800 MHz, using the Volterra DPD since the out-of-band emission was reduced by 15.6 dB compared to those obtained without DPD.

According to the analysis above, the application of a pruned Volterra DPD proved the linearizability of the designed PA under multi-carrier WCDMA and LTE signals at around both operating frequencies.

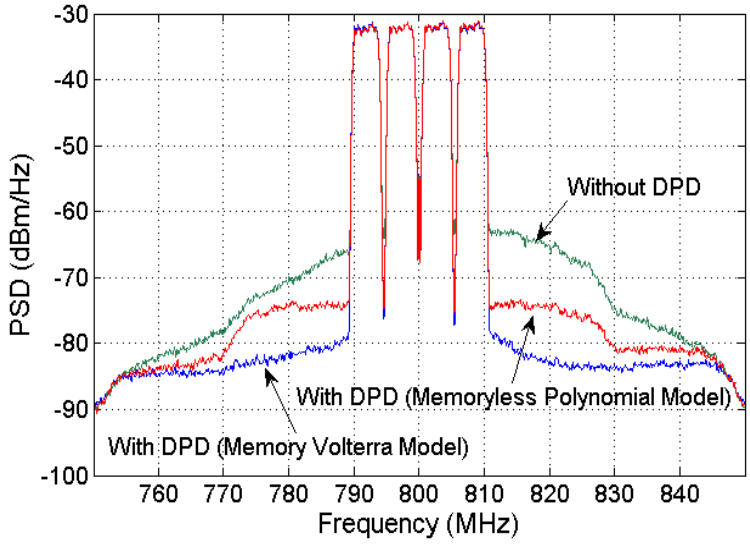


Figure 4.10 Measured output power spectrum density (PSD) before and after DPD (memory model and memoryless model) at 0.8 GHz, using four-carrier WCDMA signal

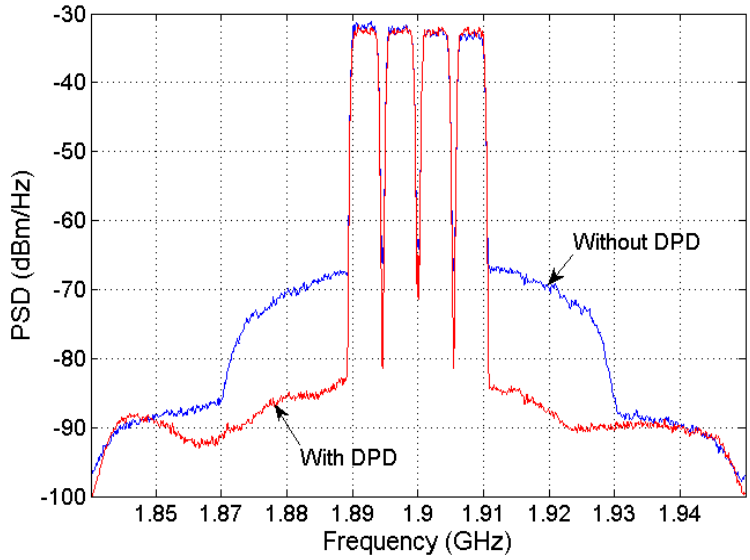


Figure 4.11 Measured output power spectrum density (PSD) before and after DPD at 1.9 GHz, using four-carrier WCDMA signal

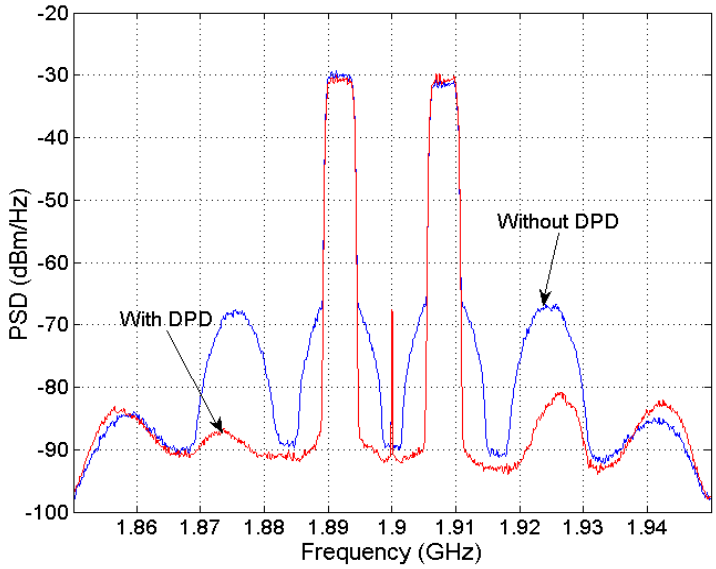


Figure 4.12 Measured output power spectrum density (PSD) before and after DPD at 1.9 GHz, using two-carrier WCDMA signal

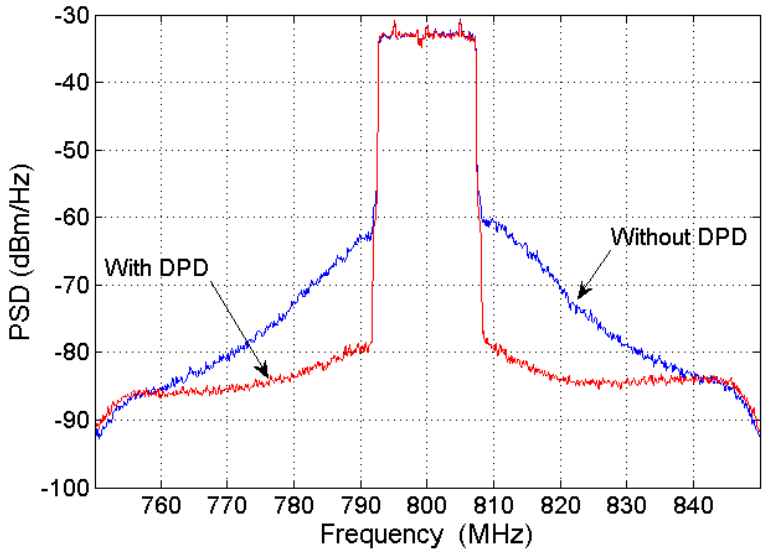


Figure 4.13 Measured output power spectrum density (PSD) before and after DPD at 0.8 GHz, using 10 MHz LTE signal

Chapter 5
Conclusion and Future Work

5.1 Conclusion

This thesis first discussed the class of operation of power amplifiers. Among all the operation modes, the Class B/J continuous mode shows itself to be a good asset for broadband and multi-band design due to its multiple sets of fundamental and harmonic impedances and, consequently, wide design space.

This work focuses on multi-band PA design, which requires an MN that can concurrently match optimal impedances at multi-frequencies. According to the literature review, most research that has managed to design the MN to match the optimal impedances at both fundamental and harmonic frequencies has resulted in very complex topology, long circuits and thus, degraded efficiency. In our work, we start by reformulating the problem by employing the wide design space of the Class J mode so that the fundamental and harmonic impedance matching constraints are relaxed. Thus, by choosing this operating condition, we can achieve the flexibility needed to design a simple, compact MN that provides competitive power-efficiency without the need for any explicit harmonic MN structures.

The dual-band matching network was designed in two stages. First, a complex-to-real impedance transformation network, with harmonic control capability, was used to transform the complex impedance for Class J operation to real impedance that is common to both operation frequencies. Then, a real-to-real trans-impedance transformer was synthesized using the dual-band filter theory. This technique was successfully applied to design a dual-band 45W GaN Class J PA operating at 0.8GHz and 1.9GHz. The measurement results of the fabricated PA show peak efficiencies of about 68% at the two operating frequencies. In addition, the application of a pruned Volterra DPD proves the linearizability of the designed PA under multi-carrier WCDMA and LTE signals and around both operating frequencies.

5.2 Future Work

Several areas are worth further analysis. First, the revised dual-band Matching Network Design approach for a transistor die, discussed in Section 3.3, needs to be finalized and verified by designing actual MNs for a transistor die and comparing the simulation and measurement results as we did for the packaged transistor MN. Since the revised approach for a transistor die merges the real-to-

complex and real-to-real MN into the filter design, it allows better control of bandwidth and insertion loss of the MN.

In addition, the proposed MN design approach has the potential to be extended to triple-band PAs. The Class B/J continuous operation mode can still be used to provide wide design space and, thus, reduce the requirement to match harmonic impedances. Some proposed topology for a triple band filter in the literature [30] can be applied to design the real-to-real impedance transmission stage. More analysis needs to be done on the triple-band real-to-complex MN stage and the harmonic control circuits.

Another application of the proposed MN design approach is the dual-band Doherty amplifier. The Doherty efficiency enhancement technique is widely used today since the PAPR of the input signal is much higher for more efficient date rates, and the need for broadband Doherty and multi-band Doherty is also increasing, including the requirement of broadband MN and multi-band MN. More investigation is needed in the impedance transformation requirements of dual-band MN for Doherty amplifiers. Revision and improvement of the proposed MN design approach is also needed to meet the new requirements.

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