Development and characterization of PECVD grown silicon nanowires for thin film photovoltaics

by

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AUTHOR'S DECLARATION

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

Nanowires are high aspect ratio nanostructures with structural diameters on the order of nanometers to hundreds of nanometers. In this work, the optical properties of highly crystalline silicon nanowires grown by the Vapor-Liquid-Solid (VLS) method surrounded by a thin silicon shell are investigated for thin film solar cell applications. Crystalline core nanowires were surrounded by a conformal amorphous silicon shell and exhibited extremely high absorption of 95% at short wavelengths (λ<550nm) and very low absorption of <2% at long wavelengths (λ>780nm). Nanowires were disordered with average lengths ranging from 1.3 to 2.3 μm. The absorption increased at longer wavelengths as a function of amorphous shell radial thickness, significantly higher than the absorption of a reference planar a-Si thin film.

In addition, a new method to grow epitaxial silicon at low growth temperatures on glass substrates is demonstrated. Highly crystalline silicon nanowires with an average length of 800 nm were used as the seed crystal to grow an epitaxial silicon shell around, using a low temperature process. The nanowire core was grown at 400° C, and the shell was grown at about 150°C. Such epitaxial grown nanowire shells could be used as a building block for nanotechnology applications in which epitaxial silicon is required over large-area substrates such as glass. Furthermore, the epitaxial silicon shell nanowires exhibited absorption > 90% up to a wavelength of 600 nm, which was significantly higher than that of a planar 1 μm nanocrystalline silicon film. The high absorption exhibited by nanowires with both amorphous and crystalline silicon shells makes them promising for use in photovoltaic and photodetector applications.

Silicon nanowires were incorporated into thin film silicon n-i-p solar cells in two configurations: as a nanostructured back reflector, and in core-shell nanowire solar cells. First, domed-shaped nanostructures were fabricated by coating an array of silicon nanowires with a thick layer of amorphous silicon. After the nanostructures were coated with Ag and ZnO:Al, they were used as the backreflector in an n-i-p amorphous silicon solar cell. The nanostructured backreflector improved light scattering within the solar cell, leading to a short circuit current of 14.8mA/cm^2, a 13% improvement over that of the planar device, which had a J_{sc}=13.1 mA/cm^2. The overall conversion efficiency of nanostructured backreflector device was $\eta = 8.87\%$, a strong improvement over that of the planar device ($\eta = 7.47\%$).

Silicon nanowires were also incorporated into core-shell nanowire solar cells. The first device architecture investigated consisted of nanowires incorporated as the intrinsic absorption layer between a planar n+ layer and conformal p+ layer. However, the fabricated devices exhibited very low collection efficiencies of $< 2\%$ due to the presence of impurities incorporated by the catalyst used during nanowire growth. As a result, the device architecture was modified such that the nanowires provided high aspect ratio structure to enhance absorption in a shell material, but the nanowires themselves were not used as an active device component.

Nanowire core-amorphous silicon shell solar cells, on average 525 nm long and about 350nm in total diameter, exhibited an impressive low total reflectance of <3% in the wavelength interval of $410\ nm < \lambda < 640nm$ and exceeded 10% only for $\lambda>700$ nm. As a result, the core-shell nanowire devices exhibited enhancement in quantum efficiency at low wavelengths, $\lambda < 500nm$ and high wavelengths, $\lambda > 600nm$ as compared to a planar device. The resulting short circuit current was 14.1 mA/cm^2 compared to 12.3 mA/cm^2 for the planar device, an improvement of ~15%. Nanowire core-nanocrystalline silicon shell solar cells were also fabricated using the same device architecture. Core-shell nanowires with an average length of 800 nm showed significant enhancement in quantum efficiency over all wavelengths as compared to a 1 μm thick planar solar cell. The core-shell nanowire device had a short-circuit current of 16.2 mA/cm^2, a ~25% improvement over that of the planar thin film solar cell (J_{sc}=13.0 mA/cm^2). Core-shell nanowire devices did, however, have lower open circuit voltage compared to the planar device. Non-conformal coverage was found to be a limiting factor in device performance, but further improvements can be expected with optimization of the n-i-p deposition conditions and nanowire density.

Acknowledgements

Dedication

For my parents, Sachiyo, and Aidan.

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Chapter 1

Introduction

An introduction to silicon-based photovoltaic devices is presented in this chapter. Thin film silicon is a large area and low cost alternative to market-dominant mono or multi-crystalline silicon solar cells. Factors that limit device performance in thin film silicon solar cells are discussed. Nanostructures, such as nanowires, are introduced as a method to improve light absorption in thin film silicon. The thesis chapter layout is presented in the last section of this chapter.

1.1 Thin film photovoltaics

Photovoltaic devices (also called solar cells) convert solar energy directly to electricity. The photovoltaic effect was first discovered in 1839 by Edmond Becquerel when he observed an electrical current when light was incident on a silver coated platinum electrode immersed in an electrolyte solution. In 1876, William Adams and Richard Day observed photocurrent in a selenium layer when contacted by two heated platinum contacts. However, it wasn't until the 1950s with the development of high quality silicon that photovoltaic devices became available for applications such as powering electronic equipment located in remote locations or satellites. The oil crisis of 1973 spurred a sudden growth of interest in renewable energies particularly in photovoltaics and wind power. Then, in the early 1990s, concerns of global warming caused by CO_2 emissions became another driving force for promoting renewable energies. However, the cost of electricity generated by photovoltaics today is not yet competitive with to commercially available sources powered by nuclear, hydro, and fossil fuels.

The photovoltaic market is currently dominated by mono or multi-crystalline silicon solar cells which have a typical solar module solar energy-to-electricity conversion efficiency of around 15%. Silicon is an ideal material for a vast range of electronic and photonic applications because it is cost-effective, readily forms thermally grown silicon dioxide, is stable after oxidation, is non-toxic, and is an abundantly available material. Additionally, silicon-based device fabrication technology is mature and well-established in the microelectronic industry. However, the optical properties of silicon are less than ideal mainly because of its indirect bandgap. In other words, recombination and generation of electrons require a phonon interaction. Consequently, thick layers are necessary to

efficiently absorb light and high purity silicon production costs are high. In fact, material costs are the largest single contributor to completed solar module costs.

Thin film technologies have gained much interest because of their potential for low cost, large area fabrication. Amorphous silicon, a well-established thin film material both in photovoltaics and large area displays, has a high absorption coefficient because the absence of periodicity means the crystal momentum conservation requirement is relaxed. However, this lack of long range atomic order also results in high defect densities, limiting the film thickness to values ~ 300-500 nm for efficient charge collection. Optical absorption in thin layers is generally weak at infrared wavelengths and therefore requires a light trapping mechanism to increase the path of light travel within the film. Therefore, there is an ongoing interest in improving cell efficiencies (typically ~ 5% for stabilized commercial single junction a-Si solar cells) while maintaining the low-cost large area advantage of thin film technology. This work examines silicon nanostructures for enhancing the optical properties of thin film photovoltaics.

1.2 Nanostructures in photovoltaics

A number of methods have been developed to improve light absorption in crystalline and amorphous silicon. In crystalline silicon solar cells, surface texturing, by anisotropically-etching pyramids, improve device performance by lowering optical reflectance [Haynos et al. 1974]. In thin film silicon solar cells the most common light trapping mechanism is texturizing of the transparent conductive oxide layer such as SnO_2:F [Sato et al. 1992] and ZnO:Al [Kluth et al. 1999]. In recent years, a number of alternative methods have been investigated to further improve light absorption in thin film silicon such as plasmonic back-reflectors [Ferry et al. 2010], photonic crystals [Bermel et al.2007], periodic nanodome back-reflectors [Zhu et al. 2010], and silicon nanowires [Tsakalakos et al. 2007].   In this thesis, silicon nanowires are investigated to enhance optical absorption in thin film silicon solar cells. Silicon nanowires can be defined as nanostructures having a very high length-diameter aspect ratio with diameters on the order of nanometers to hundreds of nanometers. Larger diameter silicon nanowires with diameters on the order of tens to hundreds of nanowires have been shown to exhibit strong anti-reflective properties and can enhance optical absorption as compared to bulk silicon. Furthermore, improvements in collection efficiency are possible in radial p-n junction

solar cells for materials with low minority-carrier diffusion lengths, by shortening of the collection length of carriers [Kayes et al. 2005].

Arrays of subwavelength sized structures have been known to have anti-reflective properties since at least 1967 when Bernhard showed that a periodic array of conical perturbations on the corneal lens of a moth eye suppressed optical reflection [Bernhard 1967]. He proposed that the perturbations gave rise to a gradient in the refractive index between that of air and the lens and showed by microwave experiments that such perturbations significantly lowered reflectance as compared to a smooth cornea sample. Clapham, in 1973, fabricated artificial moth eye structures by patterning photoresist on glass and showed that they reduced the integrated specular reflection of white light to 0.2% [Clapham et al. 1973]. In 1979, Gittleman et al. showed that Si nanopillars reduced reflectance of polished Si wafers for solar thermal conversion applications [Gittleman et al. 1979]. Reactive sputter etching the surface of Si into an array of pillars with diameters and spacing small compared to the incident wavelength of light was shown to lower specular reflectance to values of 10^{-3} or less at wavelengths below 1 μm. Similarly, Craighead et al. 1980 showed that submicron texturing lowered thin film amorphous silicon reflectance to nearly zero over the visible spectrum [Craighead et al. 1980]. Since then various groups have reported strong anti-reflective properties in silicon nanowires [Peng et al. 2005, Tsakalakos et al. 2007], short-aspect ratio nanorods [Sun et al. 2008, Min et al. 2008, Huang, Z. et al. 2007], tapered nanostructures [Kanamori et al. 1999, Huang,Y.F. et al. 2007], and other nanoscaled structures [Lalanne et al. 1997, Hadobás et al.2000, Koynov et al. 2006].

The optical absorption of silicon nanowires was first studied in bottom-up grown nanowires. Holmes et al. [Holmes et al. 2000] observed that the absorbance, defined as -log(Transmission), of small diameter (4-5 nm) silicon nanowires suspended in hexane exhibited discrete peaks. The peaks were strongly blue-shifted with respect to the bandgap of bulk Si of 1.1 eV. In larger diameter nanowires on the order of tens to hundreds of nanometers, strong optical absorption enhancement can be attained. A number of theoretical studies have since shown that silicon nanowires, of appropriate diameter and periodicity, can significantly enhance optical absorption for solar cells applications [Hu et al. 2007, Lin et al. 2009, Li et al. 2009]. Experimental measurements of silicon nanowires on glass substrates have also shown that silicon nanowires can enhance absorption over the entire solar spectrum [Tsakalakos et al. 2007 (2)].

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Arrays of silicon nanowires have been incorporated into solar cells by a number of groups [Peng et al. 2005, Tsakalakos et al. 2007, Stelzner et al. 2008, Fang et al. 2008, Sivakov et al. 2009, Gunawan et al. 2009, Garnett et al. 2010, Li et al. 2010, Kumar et al. 2011]. The overall performance of these devices remains much lower than that of the highest recorded crystalline Si conversion efficiency of 24.7% [Zhao et al. 1998]. One of the main drawbacks of nanowire solar cells is that the high surface area of nanowires increases surface recombination velocity, a measure of the rate of recombination occurring at the surface of the material. Such increases in surface recombination velocity lead to a drop in carrier lifetimes and therefore lower device performance in p-n junction solar cells [Peng et al. 2005].

In this thesis, the optical properties of crystalline-amorphous core-shell silicon nanowires and crystalline-nanocrystalline core-shell silicon nanowires are investigated for the first time. Surrounding the highly crystalline silicon nanowire core with a material with differing bandgap or doping type adds functionality to nanowires [Lauhon et al. 2002], expanding potential applications in nanotechnology. Both types of core-shell nanowires exhibit significantly higher absorption than their thin film counterparts over all wavelengths due to lower reflectance and multiple scattering. An array of silicon nanowires are also incorporated into a new core-shell n-i-p device architecture. In an n-i-p device structure, photogenerated carriers are transported by an internal electric field, which spans most of the semiconductor region, rather than by diffusion. The core-shell n-i-p solar cells show very low total reflectance (including both specular and diffuse components) over most of the visible spectrum leading to higher net external quantum efficiency than a planar reference device. Furthermore, the core-shell solar cell consisting of an amorphous silicon absorbing layer is the first bottom-up grown nanowire solar cell to have a conversion efficiency of $\eta = 6\%$.

1.3 Thesis organization

The main focus of this thesis is the study of optical properties of core-shell nanowires and the incorporation of silicon nanowires into core-shell nanowire solar cells. First, the material properties of amorphous silicon are discussed in Chapter 2. The modeling of a planar n-i-p thin film solar cell is also presented to better understand the mechanisms of device performance losses associated with this device structure. In addition, an overview of the Vapor-Liquid-Solid nanowire growth method and a literature review of recent nanowire solar cell studies are discussed. At the end of Chapter 2, other

applications for silicon nanowires are considered, particularly thermal electric power conversion and water splitting. The fabrication of metal-semiconductor-metal silicon nanowire photodetectors for medical imaging application is also discussed in Appendix A.

The experimental methodology for nanowire growth and solar cell deposition is described in Chapter 3. In addition, the nanowire and device characterization methods are also presented. The experimental findings of the structural and optical properties of core-shell silicon nanowires are presented in Chapter 4. Both amorphous and nanocrystalline shell nanowires were investigated in this chapter.

Nanowires were incorporated into thin film silicon solar cells by two methods: 1) nanostructured back reflector solar cells, and 2) core-shell nanowire solar cells. The device structure and device performance for both methods are discussed in Chapter 5. Both amorphous silicon and nanocrystalline silicon material were investigated as the absorbing layer in core-shell nanowire solar cells. Finally, conclusions and contributions of this work are presented in Chapter 6.

Chapter 2
Background

An overview of the material properties of amorphous silicon and n-i-p device structure is presented in this chapter. In particular, challenges involved in using amorphous silicon and sources of collection efficiency loss in thin film silicon solar cells are discussed. Various nanowire fabrication methods are considered but the focus of discussion is the vapor-liquid-solid technique. This method facilitates large area fabrication and can be used in conjunction with conventional thin film silicon deposition techniques. At the end of the chapter, a literature overview of the optical properties of silicon nanowires, and silicon nanowire based solar cells is presented.

2.1 Amorphous silicon: The challenge

Amorphous silicon (a-Si) offers many advantages over crystalline silicon such as large area deposition on low cost substrates such as glass, stainless steel, or polymers, and has a higher absorption coefficient for wavelengths up to about $\lambda \sim 700$ nm requiring only thin layers (300-500 nm in thickness) in solar cells. However, there are also a number of disadvantages that limit its competitiveness in the solar cell industry currently dominated by mono- and multi-crystalline silicon. These disadvantages include light induced degradation, also known as the Staebler-Wronski effect, low absorption at infrared wavelengths and the presence of deep traps and band tails within the mobility bandgap, which limit film thickness for efficient charge collection.
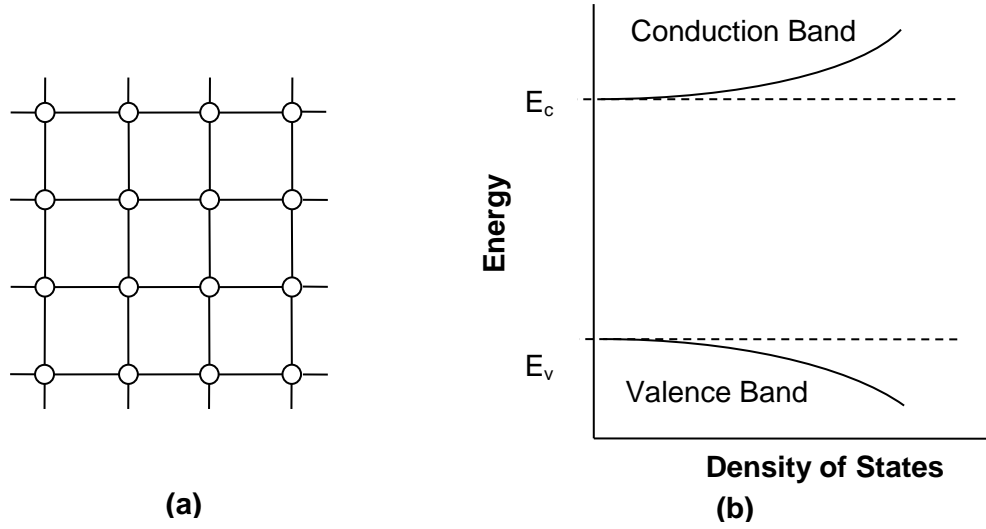
Figure 2-1: Illustration of a periodic network of Si atoms (a) and density of states diagram for crystalline silicon (b).
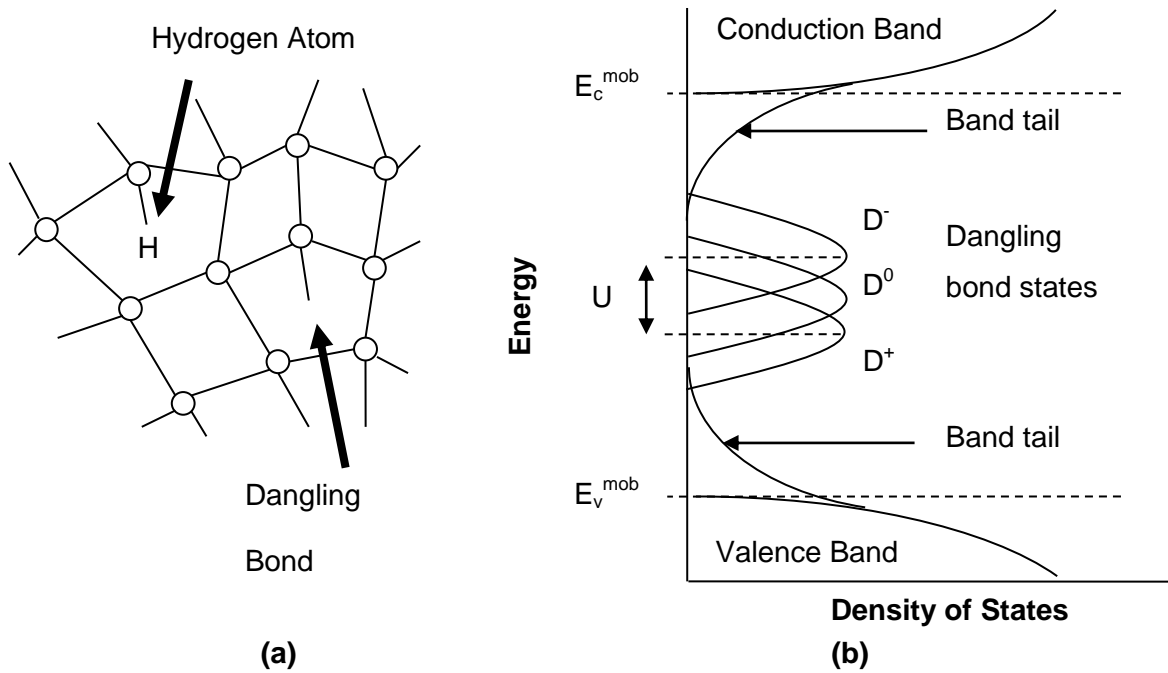
Figure 2-2: Illustration of a random network of Si atoms (a) and density of states diagram for amorphous silicon (b).

Table 2-1: Correspondence between atomic structure and resulting electronic properties [Street 1991].

Structure	Electronic Properties
Bonding Disorder	Band tails, localization, scattering
Structural Defects	Electronic states within the bandgap
Alternative bonding configurations	Metastable states

An illustration of the periodic network of atoms for crystalline silicon is shown in Figure 2.1 (a) and the corresponding energy versus density of states (DOS) diagram is shown in Figure 2.1 (b), where the bandgap of crystalline silicon is $E_g = E_c\text{-}E_v = 1.12$ eV. In comparison, Figure 2.2 (a) illustrates the random network of atoms for an amorphous material. Amorphous silicon does not have long range order but retains its short range order because the covalent bonds between silicon atoms are much like crystalline silicon consisting of the same average bond lengths, bond angles, and number of neighboring atoms [Street 1991]. Table 2-1 indicates how the atomic structure influences the electronic properties of a-Si [Street 1991]. The energy versus density of states diagram of amorphous silicon is shown in Figure 2.2 (b). First, deviations in bond length and angle in a-Si result in a broadened band tail which extend into the forbidden gap along the conduction and valence bands. Second, a-Si consist of atoms that are missing a neighboring atom which result in dangling bonds that create defect states deep within the forbidden gap. Such defects can be positively charge D^+, negatively charge D^-, or neutral D^0 [Smith and Wagner 1989, Winer 1990, Street 1991, Powell et al. 1993, 1996]. One method to minimize recombination caused by dangling bonds is by passivating them with hydrogen atoms as illustrated in Figure 2.2 (a). Finally, the alternative bonding configurations in a-Si result in metastable states. An external excitation such as illumination or current flow can induce defects in a-Si causing degradation in device performance. The first report of light-induced degradation was the degradation of a-Si solar cells in 1977 caused by an increase in induced defects thereby reducing solar light to electricity conversion efficiency [Staebler and Wronksi, 1977]. Light induced degradation effects are more prominent in thick films and can

therefore be minimized by using thinner films in which the electric field within the intrinsic layer is enhanced [Shah et al. 1999]. Alternatively, nanocrystalline silicon (nc-Si) (also called microcrystalline silicon) can also be grown by PECVD but under high hydrogen dilution conditions. The main advantages of nc-Si solar cells are that they are stable under illumination and absorb light at infrared wavelengths [Meier et al. 1994] since the bandgap of nc-Si is close to that of crystalline Si (1.12 eV).

2.2 Device modeling

Device simulations were carried out using Sentaurus, which calculates charge transport in semiconductor devices by solving the Poisson equation and the electron and hole continuity equations. Basic formulas used in Sentaurus are listed in Appendix B. The optical generation within semiconductor regions was calculated using the Ray Tracing Method in which the transmission and reflectance of source rays are tracked in a number of incident rays as they pass through different materials. The propagation of incident light through the glass and TCO layers was calculated using the Transfer Matrix Method which can account for wave interference of light traveling through multi-layers of films.

Material parameters used in the simulation are listed in Table 2-2. The a-Si conduction band-tail (CBT) and valence band tail (VBT) DOS shown in Figure 2.2 (b) are given by the formulas:

$$N_{CBT}(E) = N_C^{tail} \exp([E_c^{tail} - E]/E_{C0}^{tail})$$

(1)

$$N_{VBT}(E) = N_V^{tail} \exp([E_v^{tail} - E]/E_{V0}^{tail})$$

(2)

where N_C^{tail} and N_V^{tail} are the density of band-tail states at the conduction and valence-band mobility edges E_C^{tail} and E_V^{tail}, and E_{C0}^{tail} and E_{V0}^{tail} are the characteristic energy of the conduction band and valence band exponential. The dangling bond defects were neglected to due convergence limitations during the solving process. The band tail parameters used in modeling are shown in Table 2-3.

Table 2-2: Material parameters used in modeling a single junction planar a-Si solar cell.

Material parameters	Value
intrinsic layer thickness	300 nm
Mobility gap	1.78 eV [Schropp et al. 1998]
Relative permittivity	11.9
Electron affinity	4.05 eV
Electron Mobility	10 cm^2/Vs [Street 2001]
Hole Mobility	1 cm^2/Vs [Street 2001]

Table 2-3: Modeling band tail parameters for a reference single junction a-Si solar cell.

Band tail parameters	Value and Reference
DOS at conduction band mobility edge, N_C^{tail}	2×10^{21} (eV^{-1}cm^{-3}) [Powell et al. 1993]
DOS at valence band mobility edge, N_V^{tail}	2×10^{21} (eV^{-1}cm^{-3}) [Powell et al. 1993]
Conduction band characteristic energy, E_{C0}^{tail}	0.03 eV [Schropp et al. 1998]
Valence band characteristic energy, E_{C0}^{tail}	0.045 eV [Powell et al. 1993]
Capture cross section (electrons)	1×10^{-15} cm^2 [Street 1991]
Capture cross section (holes)	1×10^{-15} cm^2 [Street 1991]
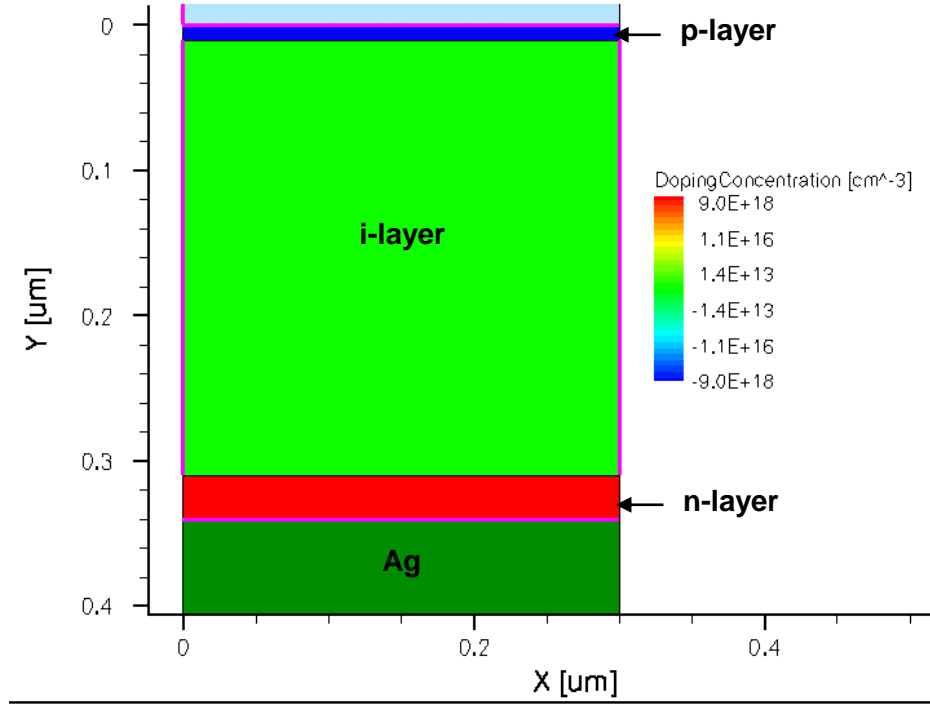
Figure 2-3: Device structure of a p-i-n solar cell.

The complete device structure is glass (100 μm) / SnO$_2$:F (1μm) / p$^+$ a-Si (10nm) / i a-Si (300nm) / n$^+$ a-Si (30nm) / Ag (100nm) and is illustrated in Figure 2-3. The incoming light enters from the glass/TCO side. Two dummy regions, one above the device and one below, are used to calculate the reflection, $R(\lambda)$=N$_{above}$/N$_{incident}$, and transmission, T(λ)=N$_{below}$/N$_{incident}$, where N$_{above}$ is the number of photons measured above the device, N$_{below,}$ is the number of photons measured below the device and N$_{incident}$ is the number of photons incident on the device.

Incident light is converted into current in the p-i-n solar cell in the sequence of steps shown in Table 2-4. First, incident light reaching the semiconductor layer is absorbed creating electron-hole pairs at a generation rate of:

$$G^{opt}(x, y, z) = I(x, y, z)(1 - e^{-\alpha(\lambda)L})F, \tag{3}$$

where *I* is the rate intensity (unit of s^{-1}) of the ray, $\alpha(\lambda)$ is the absorption coefficient of the material (unit of cm^{-1}), *L* is the length that light has traveled within the material, and *F* is the probability a photon absorption creates an electron-hole pair and is set to be 1. The absorption coefficient is

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related to the extinction coefficient, k, by the formula $\alpha(\lambda) = 2\pi k/\lambda$. After electron-hole pairs are generated within the semiconductor, the electric field established across the p-n junction promotes charge separation and charge flow creating drift current.

Table 2-4: Steps during p-i-n solar cell operation.

Step	Description
1. Light absorption	Described by material absorption coefficient, $\alpha(\lambda)$.
2. Separate charge	Electrons and holes are separated from each other by the electric field.
3. Collect charge	Electrons and holes travel to opposite contacts due to the electric field.
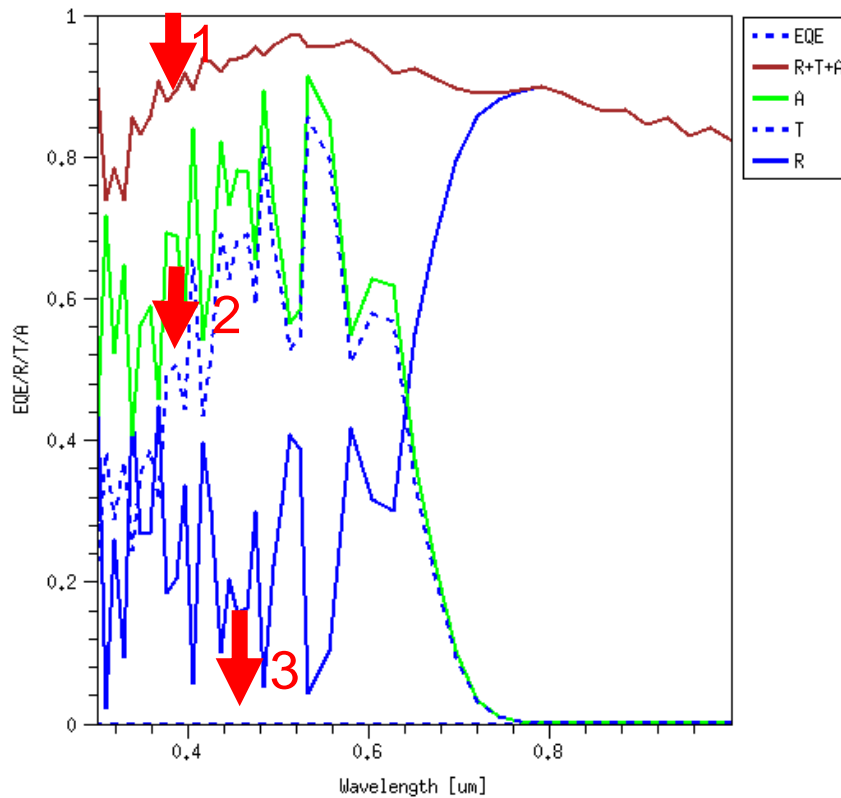
Figure 2-4: External quantum efficiency (EQE), reflectance (R), transmission (T), absorption by a-Si (A_{Si}) and the sum R+T+A_{Si} of a reference a-Si cell.

The external quantum efficiency (EQE) is defined as:

$$EQE = \frac{Ihc}{q\lambda I_O S} \quad ,$$

(7)

where I is the electrical current, h is Plank's constant, c is the speed of light, λ is the wavelength, I_O is the incident light intensity, S is the incident surface area, G is the integrated optical generation rate and q is the charge of an electron. Using the device structure shown in Figure 2-3 the simulated EQE, reflectance R, transmission T, absorption in silicon A_{Si} and the sum $R+T+A_{Si}$ are shown in Figure 2-4. The arrows indicate conversion losses which are described in Table Table 2-5. The corresponding device performance is $V_{oc} = 0.954$ V, $J_{sc} = 10.76$ mA/cm^2, $FF = 80.5$ %, $\eta = 8.27$ %. Note that the V_{oc} and FF are considerably high partly because the deep dangling bond defects were neglected. In addition J_{sc} is low since no trapping mechanism such as texturing was used.

Table 2-5: Summary of mechanisms of energy conversion losses

Mechanism of Loss	Cause of Loss
Reflectance	glass/TCO and TCO/Si interface ($\lambda<650$nm)
	low absorption in Si ($\lambda>650$ nm)
1- (R+T+A$_{Si}$)	Absorption in glass and TCO
A$_{Si}$-EQE	Absorption in p-layer and n-layer
	Recombination in the band tails, deep dangling bond defects and light induced degradation

Generally speaking, once light has entered the semiconductor material, energy conversion losses can be due to five mechanisms: (1) lattice thermalization losses, (2) junction losses, (3) contact losses, (4) recombination losses and (5) photons lacking sufficient energy to be excited to conduction band [Green 2003]. Note that in a thin film p-i-n device the electric field covers the entire intrinsic region but does not extend the entire lengths of the p and n region. Therefore, electron-hole pairs generated in the p and n-layers that are not located within the depletion region are not separated by

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the electric field. In particular, absorption in the p-layer is a substantial source of loss in p-i-n devices particularly for high energy photons for which absorption in the p-layer is high [Springer et al. 2005].

2.3 Fabrication of silicon nanowires
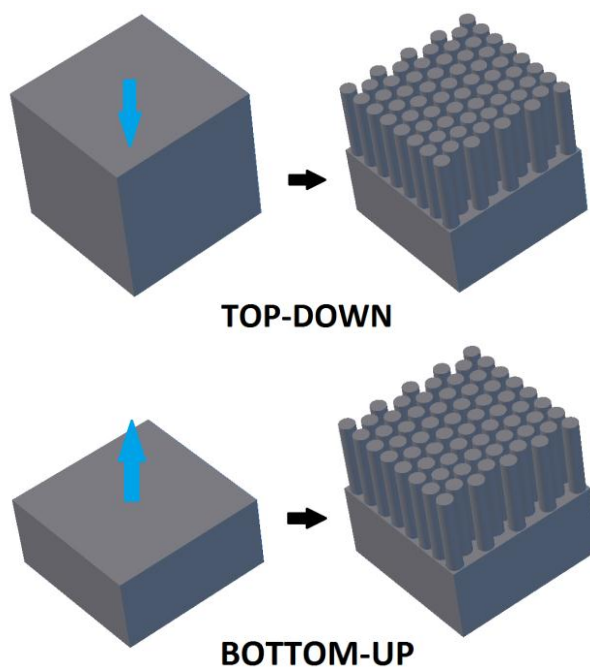
Figure 2-5: Illustration of the top-down and bottom-up fabrication approaches. **The top-down approach involves etching a silicon wafer or film by chemical or dry etching. The bottom-up approach involves growing nanowires from gas or liquid phase onto various substrates such as glass, silicon, or metal foil [Adachi, Khorasaninejad, et al 2012].**

Fabrication of silicon nanowires can be categorized into two approaches: top-down and bottom-up as illustrated in Figure 2-5. In the top-down approach a crystalline silicon wafer or silicon thin film is etched either by metal-induced (usually Ag) chemical etch using a HF-based solution [Peng et al. 2005], electro-chemical etching [Wang et al. 2010], or dry etching [Zhu et al. 2009, Lu et al. 2010] to form vertical nanowires. During the metal-induced chemical etch process, a metal induces excessive

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local oxidation at the silicon surface and submersion in HF solution leads to silicon dissolution [Peng et al. 2005]. This fabrication technique is weakly dependent on silicon crystal orientation and can therefore also be used in multicrystalline [Sivakov et al. 2009] or polycrystalline silicon [Peng et al. 2005]. Nanowires can also be formed by a two-step process of nanosphere [Zhu et al. 2009] or electron beam [Lu et al. 2010] lithography for defining an etch-mask followed by a Reactive-Ion-Etch (RIE) or electrochemical etch [Wang et al. 2010]. In nanosphere lithography, a monolayer of nanospheres can be formed by a number of methods such as spin coating [Jiang et al. 2004], floating-transferring technique [Burmeister et al. 1997] or the Langmuir-Blodgett technique [Garnett et al. 2010, Zhu et al. 2009]. Alternatively self-powered parallel electron lithography can be used to pattern photoresist into a periodic array with sub-35 nm high resolution [Lu et al. 2010]. Nanowires fabricated by the top-down approach are typically aligned vertically but can also be fabricated to be slanted [Fang et al. 2008].

There are two bottom-up nanowire growth approaches: the well-known metal-catalyzed Vapor-liquid-Solid (VLS) technique [Wagner et al. 1964] and the oxide-assisted technique [Wang et al. 1998]. In both techniques nanowires can be directly grown on various substrates such as glass, silicon wafer and metal foils. The VLS growth mechanism involves the chemical reaction between a silicon source gas such as SiH_4, Si_2H_6, SiI_2 or $SiCl_4$ and a droplet of metal catalyst. At elevated temperatures, the silicon source gas and metal droplet form a liquid alloy and super-saturation of the liquid alloy causes nanowire nucleation and growth to occur. Silicon atoms diffuse through the catalyst droplet and crystallize at the liquid-solid interface resulting in one-dimensional growth. The diameter of the nanowire is therefore controlled by the catalyst size.

Table 2-6: Advantages and disadvantages of the top-down and bottom-up fabrication approaches.

	Top-down	Bottom-up
Advantages	Nanowires have identical crystal structure and doping properties as the initial substrate [Peng et al. 2005].	Nanowires are highly crystalline or single crystal [Wagner et al. 1964].
	Simple fabrication is feasible at near room temperature [Peng et al. 2005].	Nanowires can be grown on non-silicon substrates for large area applications.
	Vertical alignment is common.	Low dimensional diameters down to 1 nm are possible [Ma et al. 2003, Li et al. 2002].
		Extremely high aspect ratios are possible (up to 100000) [Park et al. 2008].
		Nanowires can be doped in-situ axially [Gudiksen et al. 2002] and radially [Lauhon et al. 2002].
Disadvantages	Fabrication requires a starting silicon wafer or film.	Catalysts used during VLS growth introduce impurities.
	Carrier lifetimes are known to decrease after dry etching [Kumaravelu et al. 2004] and chemical etching [Peng et al. 2005].	Nanowires are not directionally aligned when grown on a non-silicon substrate.
	Aspect ratios can be limited.	Growth requires temperatures to be $\geq 320°C$ [Westwater et al. 1997].
		Nanowires grown at low temperatures and high pressures are susceptible to bending and kinking [Westwater et al. 1997].

The second bottom-up growth method is the oxide-assisted growth technique in which nanowires are synthesized by thermal evaporation or laser ablation of silicon powder mixed with silicon dioxide or pure silicon monoxide powder. In this method, oxides play a key role in the nucleation and growth of silicon nanowires [Wang et al. 1998, Zhang et al. 2003]. Fabrication is carried out in the temperature range of 850 and 1200 °C and nanowires consist of a crystalline silicon

core surrounded by an oxide shell. Diameters approaching 1 nm [Ma et al. 2003, Li et al. 2002] are achievable with this method and the growth direction is mainly <112> and <110> [Zhang et al. 2003]. A comparison between the bottom-up and top-down fabrication methods is given in Table 2-4. In this work, silicon nanowires were grown by VLS method since it is a large area fabrication technique, which is compatible with thin film silicon growth techniques, and is a relatively low temperature growth process.

2.3.1 VLS method
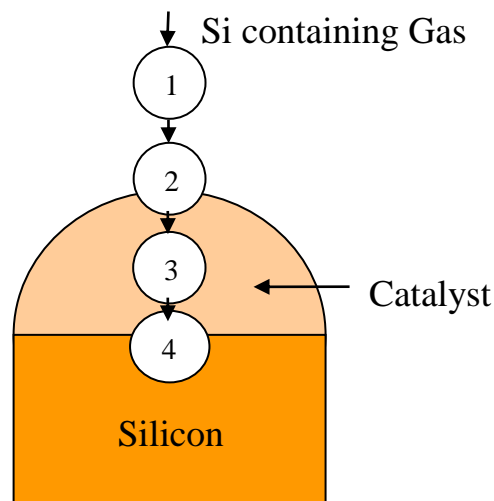
Figure 2-6: Illustration of the four steps during the Vapor-Liquid-Solid (VLS) process.

The Vapor Liquid Solid (VLS) method was first proposed by Wagner and Ellis, 1964 [Wagner et al. 1964] where a droplet of liquid Au facilitates the grown of nanowires from a silicon containing gas source. An illustration of the VLS growth process is shown in Figure 2-6 [Givargizov 1975]. Four steps can be identified: (1) Si first travels in gas phase by mass transport to the catalyst, (2) a chemical reaction occurs at the vapor-liquid interface, (3) Si diffuses rapidly through or around the catalyst and (4) the diffused Si attaches at the silicon-catalyst interface leading to the one dimensional growth of a silicon nanowire with the Au droplet located at the tip. Under suitable deposition conditions, the Au droplet catalyzes the decomposition of silicon containing gases at rates orders of magnitude higher than that of the usual uncatalyzed thin film silicon deposition. The nanowire, also called whisker, increases in length until the Au is consumed or growth conditions are changed.

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The rate-determining step, or the step which controls the nanowire growth rate, is believed to be step 4 based on differing growth rates between GaAs nanowires that grew in two different directions [Givargizov 1975]. Nanowires oriented in an inclined <211> direction were found to grow quicker than those that grew perpendicular to a (111) substrate. The higher growth rate for the inclined nanowire was because the activation energy of nucleation would be lower in the slanted case. Because of the difference in growth rates for the two different activation energies of nucleation at the silicon-catalyst interface step 4 was concluded to be the rate-determining step.

The original work by Wagner et al. involved the growth of single crystal silicon vertically aligned "nanowhiskers" by chemical vapor deposition at a substrate temperature of 950°C [Wagner et al. 1964]. More recently, silicon nanowires have been fabricated at lower temperatures either by chemical vapor deposition at growth temperatures as low at 320°C[Westwater et al. 1997] or by plasma enhanced chemical vapor deposition (PECVD) at a growth temperature of 390°C [Hofmann et al. 2003]. PECVD offers several advantages over other techniques, which include large area deposition, low temperature deposition, and perhaps most importantly it is an established industrial technology for thin film photovoltaics and large area display production.

2.3.2 Nanowire length

During Au catalyzed VLS growth, the nanowire sidewalls and the substrate are covered by thin layer of Au which can diffuse from one nanowire tip to another during deposition [Hannon et al. 2006]. As the nanowires grow there is a net transfer of Au out of the droplet at the tip of the nanowire which wets the sidewall. Therefore during growth the Au droplet is eventually consumed after which limiting the maximum nanowire length. Assuming no Au incorporation into the nanowire due to the low solubility of Au in Si, the nanowire length, L, is given as:

$$L = \frac{r^2}{2a\theta} \qquad (4)$$

where r is the nanowire radius, θ is the average coverage of Au on the sidewall estimated to be 1 - 1.5 monolayers and a^3 is the atomic volume of Au (a~0.26nm) [Hannon et al. 2006]. Therefore, the maximum length of the nanowire is limited by the radius squared of the nanowire. Nonetheless, silicon nanowires with lengths up to 2.3 mm have been reported for diameters of 30 nm [Park et al.

2008] which is much longer than predicted by eq. (4) suggesting that Au does not have to cover the entire wall surface or there is another mechanism at work during nanowire growth.

2.3.3 Nanowire diameter

During the VLS process there is a critical diameter below which nanowires do not grow. The critical diameter is related to supersaturation, $\Delta\mu$, the driving force of nanowire growth, by the Gibbs-Thomson equation:

$$\Delta\mu_{NW} = \Delta\mu_{bulk} + 4\Omega\alpha/d \,, \tag{5}$$

where $\Delta\mu_{NW}$ is the effective difference between the chemical potential of Si in the vapor phase and in the nanowire (i.e., $\Delta\mu_{NW}=\mu_{NW}-\mu_{vapor}$) , $\Delta\mu_{bulk}$ is the difference between the chemical potential of Si in the vapor phase and in bulk Si (i.e., $\Delta\mu_{bulk}=\mu_{bulk}-\mu_{vapor}$), d is the nanowire diameter, α is the specific surface free energy of the wire and Ω is the atomic volume of Si [Givargizov 1975]. This model found that nanowire growth would stop below a critical diameter $d_c \leq 0.1$ µm because of increasing vapor pressure and solubility of Si for decreasing diameter. However, nanowire with core diameters down to 2 nm have been grown by the VLS method at 440°C from SiH_4 source gas using commercially available Au nanoclusters [Cui, Lauhon et al. 2001]. The nanowire growth rate, V, for VLS grown nanowires can also be related to $\Delta\mu$ as

$$V = b(\Delta\mu/kT)^n \,, \tag{6}$$

where b is a coefficient independent of $\Delta\mu$, k is Boltzmann's constant, T is temperature, and n is a power factor experimentally found to be ~ 2 [Givargizov 1975]. From equations (5) and (6) the nanowire growth rate is found to decrease with decreasing nanowire diameter.

2.3.4 VLS catalyst

Silicon nanowires are most commonly grown using an Au catalyst but other catalysts can also be used such as Pt, Ag, Pd, Cu, Ni [Wagner et al. 1964], Al [Wang et al. 2006], Fe [Yu et al. 1998], Ga [Sunkara et al. 2001], In [Iacopi et al. 2007], Zn [Yu et al. 2000], Co [Carter et al. 2005], Ti [Kamins

et al. 2001] and Sn [Chen et al. 2007, Parlevliet et al. 2007, Jeon et al. 2009]. However, of these catalysts at least Au, Fe, and Ti are known to severely degrade device performance due to the creation of deep trap states in the electronic band in Si which reduces minority carrier lifetimes [Rohatgi et al. 1983] and Cu and Ni are fast diffusers in Si.

A requirement for large area thin film solar cell fabrication is low temperature processing such that low cost substrates such as glass can be used. Catalysts that have a low eutectic point with silicon and also have low solubility in silicon include Bi, In, Sn and Ga. Ga-Si has a very low eutectic point of 29.8 °C and form molten pools near room temperature which may not be technologically amiable. Of the remaining catalysts Sn was chosen as the catalyst in this work.

2.3.5 Sn catalyst

Tin (Sn), like Si, is a group IV element but much like all impurities is expected to create impurity energy levels within the Si forbidden gap. Impurity energy levels were measured in ion implanted Sn in MOS devices to be 0.17 eV below the conduction band and 0.37 eV above the valence band [Fahrner et al. 1972]. Note however that in these measurements deep traps of 0.34 eV below the conduction band and 0.49 eV and 0.19 eV above the valence band were also detected when Si was ion implanted into silicon substrates using the same technique suggesting that implanted ions were incorporated interstitially or in a more complex configuration rather than in a substitutional configuration [Schulz 1974].

On the other hand, deep traps were not detected by deep-level transient spectroscopy for samples in which a concentration of 4.8×10^{18} cm^{-3} Sn was grown into p-type Czochralski grown silicon [Rohatgi et al. 1983]. In this study, impurities were incorporated before crystal growth rather than after such as in the case when impurities were introduced by ion implantation. Possible reasons why deep traps did not form include thermal history or solid solubility of the impurity and defect structure of the crystal [Rohatgi et al. 1983]. Out of 22 impurities tested including Al, C, P and O, Sn was reported to have the second highest threshold concentration only after Si for grown-in impurities before degradation of solar cell performance [Rohatgi et al. 1983]. In comparison, the threshold concentration on solar cell performance for grown-in Au, Fe, Ti and Ni impurities were orders of

magnitude lower. In addition, Sn has a limited solubility of ~0.01 at% in Si [Olesinski et al. 1984] so Sn incorporation into Si is also expected to be limited.

Silicon nanowire growth using Sn catalyst has been reported previously by thermal evaporation [Chen et al. 2007], pulsed PECVD [Parlevliet et al. 2007] and microwave PECVD [Jeon et al. 2009]. In this study, silicon nanowires are grown by conventional RF PECVD using Sn as the catalyst.

2.4 Optical properties of silicon nanowires

2.4.1 Optical modeling

The optical properties of vertically aligned and periodic silicon nanowires have been modeled by a number of groups using the Finite Difference Time Domain (FDTD) method to solve Maxwell's equations [Hu et al. 2007, Li et al. 2009, Lin et al. 2009]. Lin et al. investigated the effect of diameter and periodicity on the optical properties of an array of silicon nanowires with a height of 2.33 μm. The incident light was parallel to the nanowire axis. The absorption capability of the nanowire array for solar cell application was assessed using a calculation called the ultimate efficiency [Shockley et al. 1961], which assumes that one photon with energy greater than the bandgap of the semiconductor material can only produce one electron-hole pair. The optimized array consisted of nanowires with a diameter of 540 nm, and periodicity of 600 nm at which the ultimate efficiency of the array was 72.4% higher than that of Si thin film of equivalent thickness without an anti-reflective coating. Furthermore, ultimate efficiency of the nanowire array was still 17.2% higher than that of a Si thin film with a single layer anti-reflective coating [Lin et al. 2009].

An array of silicon nanowires in which the nanowire length was 5 μm was also modeled by Li et al. A periodicity between 300 to 900 nm resulted in the highest ultimate efficiency peaking at 30.5% for a periodicity of 600 nm. The optimum ratio between diameter and periodicity was found to be 0.8 [Li et al. 2009].

In the models used in these studies the nanowires were periodic with a constant diameter and constant length. Bao et al. studied the effect of adding randomness to one parameter at a time while keeping the other parameters constant. In each case the nanowires remained vertically aligned. For

each parameter eight different configurations were simulated and results were average. For example, an array of silicon nanowires with random diameter but constant length and was periodic showed net absorption enhancement, particularly for low energy photons, compared to that of an array with a single diameter. The absorption enhancement was due to broadening to lower energies because the variation of diameter resulted in multiple resonant frequencies and absorption peaks. Similarly, an array of nanowires with random nanowire lengths while keeping the diameter and position constant also showed absorption enhancement at low energies due to optical scattering by the nanowires. Finally, an array of nanowires with random location showed only slightly higher absorption that an array that was completely periodic [Bao et al. 2010].

Silicon nanowires grown by the bottom-up approach are disordered with a tendency to grow in a range of angles around substrate normal. The optical modeling methods used so far are not suitable for such disordered nanowires due to computational limitations. However, silicon nanowires have been analyzed using an analytical model where the nanowires were treated as a scattering mat on silicon substrate [Street et al. 2009].

2.4.2 Reflectance measurements

Silicon is the most prevalent material used in solar cells but reflection of bare polished crystalline silicon is very high in air (>30% over the solar spectrum). Therefore solar cells usually employ an anti-reflection coating to lower reflection losses. However, anti-reflection coatings (ARCs) have their own disadvantages such as limited wavelength range of operation in single layer anti-reflection coatings, an increase in fabrication complexity since precise thickness control is required, or degradation over time when concentrators are used.

Microstructured or nanostructured surfaces are also commonly used to lower reflection. Surface texturing of (100) oriented silicon into anisotropically etched pyramids have been shown to improve device performance in non-reflecting (black silicon) solar cells [Haynos et al. 1974]. A well textured silicon substrate can lower the average reflection to about 10% over the solar spectrum at normal incidence which can be further lowered to about 3% using an anti-reflective coating [Sopori et al. 1983]. A nanostructured surface can also achieve ultra-low reflection over a wide range of wavelengths. For example, an array of silicon nanowires fabricated by etching in HF-H_2O_2 solution can lower reflection to values of 2.1 % or less in the wavelength range 300-1100 nm [Peng et al. 2008].

Broadband antireflective properties of nanowires have also been observed in both vertically aligned nanowires as well as disordered nanowires. Since nanowires grown by these two approaches differ in terms of structure (e.g. aspect ratio, directional alignment, variation in diameter, etc.), doping method, and fabrication conditions (e.g. substrate type, temperature, etc.) their discussion will be treated separately.

Nanowires fabricated by the top-down approach can be etched either by chemical or dry etching. An array of vertically aligned silicon nanowires fabricated by etching the surface of a monocrystalline (111)-oriented silicon wafer using an aqueous $HF/AgNO_3$ solution for 20 min. was reported by Peng et al. [Peng et al. 2005]. The nanowires after etching were confirmed by TEM to have an identical crystalline orientation as the initial silicon wafer. The reflection of the nanowire array was observed to drop to about 5% or less over the wavelength range of 300-1000 nm, significantly lower than the starting silicon substrate and also lower than a porous silicon sample. A very similar low reflection spectrum was measured for nanowires etched from a polycrystalline silicon substrate.

Periodic quasi-nanowires, fabricated using a combination of nanosphere lithography and etching, also have excellent antireflective properties [Sun et al. 2008, Wang et al. 2010]. For example, periodic quasi-nanowires fabricated by Au-assisted electrochemical etching have been reported to have a total reflectance of <15% for a short nanowire length of 332 nm and <3% for longer lengths of 2.12 μm, 3.80 μm, and 5.33 μm over the wavelength range of 250-1200 nm [Wang et al. 2010]. The reflection spectra can also be tuned by adjusting the nanowire diameter [Seo et al. 2011] or periodicity [Boden et al. 2008]. For example, periodic nanowires with varying radii of 45-70 nm have been shown to have distinctly different colors covering the entire visible spectrum [Seo et al. 2011]. The reflection spectra of nanowires dipped at wavelengths depending on the radius of nanowire. Nanowire arrays with radii of 45 nm, 55 nm, and 70 nm appeared red, blue, and green respectively. The shift in reflection dip was attributed to the guided mode properties of individual nanowires. Shift in reflection peak to higher wavelengths has also been observed in tapered silicon quasi-nanowires with increasing periodicity [Boden et al. 2008] and crystalline-amorphous core-shell nanowires with increasing shell thickness [Adachi et al. 2010]. Such color filtering effect could find application in image sensor devices.

Disordered silicon nanowires fabricated by the bottom-up approach also exhibit anti-reflective properties. Muskens et al. showed that an array of disordered nanowires with an average diameter of 50 nm showed substantially lower specular reflectance than that of a bare silicon substrate, particularly at low energies. The specular reflection decreased for increasing photon energy to near-zero values above 1.5 eV. However, the diffuse reflection of the nanowire array was high, up to 33% at 2.2 eV which was attributed to scattering. Suppression of the diffuse reflectance was suggested possible by filling the space between nanowires with an intermediate refractive index medium such as Indium Tin Oxide (ITO) or changing the nanowire diameter [Muskens et al. 2008].

VLS grown nanowires incorporated into a thin film solar cell have demonstrated ultra-low specular reflection. Tsakalakos et al. showed that nanowire solar cells consisting of p-type nanowires (diameter = 109±30 nm) coated by a conformal 40 nm thick n^+ a-Si film and 200 nm thick ITO had a specular reflection of <1% over the wavelength range of 300-1100 nm [Tsakalakos et al. 2007]. Compared to a thin film p-i-n a-Si solar cell the specular reflection of the nanowire solar cell was one to two orders of magnitude lower over the same spectral range. Although the conversion efficiency of the nanowire device was low (~0.1%), it demonstrated photovoltaic response over a broad wavelength range showing potential for collection efficiency enhancement.

2.4.3 Absorption measurements

The absorption spectrum can also be obtained by UV-VIS-NIR spectroscopy. Absorption is defined as *A=1-T-R,* where *T* is the total transmission and R is the total reflection. The transmission measurement of nanowires requires a transparent substrate such as glass [Tsakalakos et al. 2007 (2), Stelzner et al. 2008], growth in solution-phase [Holmes et al. 2000], or embedding in a transparent polymer and removal from an opaque substrate such as crystalline silicon [Kelzenberg et al. 2010]. Therefore, absorption measurements are more common in bottom-up grown nanowires since they can be grown directly onto a transparent substrate. Nonetheless, absorption measurements in nanowire arrays fabricated by etching a thin film of silicon on glass [Sivakov et al. 2009, Zhu et al. 2009] or etching a silicon-on-insulator substrate followed by removing the supporting silicon substrate [Lu et al. 2010] is also possible.

Tsakalakos et al. showed that the absorption spectra of silicon nanowires grown by the VLS method on glass grown using three different catalyst thicknesses of 5 nm, 2.5 nm, and 1 nm were

noticeably high at low wavelengths between 300-450 nm as compared to a 11 μm silicon thin film. The highest absorption was observed in the densest nanowire array, grown using an Au thickness of 5 nm, which was higher than the silicon film over a broad wavelength range of 300 - 2000 nm. Interestingly, absorption at infrared wavelengths that correspond to energies below the bandgap of silicon was also very high, which was attributed to defect states [Tsakalakos et al. 2007 (2)]. Such sub-bandgap absorption has also been reported in silicon microspikes, and was attributed to a high density of impurity and structural defects [Wu et al. 2001].

The absorption of top-down fabricated nanowires has also been shown to be high, particularly at low wavelengths. Silicon nanowires fabricated by $AgNO_3$/HF etching a 2.7 μm thick multicrystalline silicon thin film were reported by Sivakov et al. The highly dense array consisted of nanowires with diameters ranging from 20 to 100 nm and an etch depth of about 2.3-2.5 μm with respect to the surface. At wavelengths between 300 and 500 nm, transmission through the silicon nanowires was zero, reflection was < 10%, and absorption was > 90%. Furthermore, the absorption of the nanowire array was higher than the silicon film of same thickness at wavelengths > 550 nm [Sivakov et al. 2009].

Silicon nanowires with micron-sized diameters synthesized by the VLS method have also showed high absorption characteristics [Kelzenberg et al. 2010]. A periodic array of vertically aligned nanowires was fabricated by the VLS-method on a <111> silicon wafer and later removed by embedding them in a transparent polymer called polydimnethlysiloxane (PDMS) and peeling them off. Due to the vertical orientation of the wires the absorption of the nanowire array was low (<50%) at normal incidence but increased with increasing incident angle. Incorporating a metal back-contact and a SiN_x anti-reflective coating, and adding Al_2O_3 particles to the PDMS improved normal incidence absorption to 96%. This absorption enhancement was demonstrated while using about 1% of the material used in a bulk silicon solar cell device [Kelzenberg et al. 2010].

2.4.4 Silicon nanocones

Nanocones also have promising optical properties. They are structurally similar to quasi-nanowires but are tapered with a larger base diameter than tip diameter. Vertically aligned nanocones can effectively grade the refractive index between air and bulk material rather than an abrupt transition from air (n=1) to the incident material [Zhu et al. 2009, Jung et al. 2010]. When the index of

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refraction is graded the net reflection becomes a combination of a collection of incremental changes of the refractive index [Wilson et al. 1982]. The anti-reflective property of graded refractive index was mathematically studied for thin layers as far back as 1880 by Rayleigh [Rayleigh et al. 1880] and has been shown to have broadband and omnidirectional antireflective characteristics [Southwell et al. 1983, Poitras et al. 2004]. Furthermore, an array of aperiodic silicon nanotips (tapered nanostructures with sharp tips) has also been shown to suppress reflection ranging from ultraviolet wavelengths to terahertz frequencies [Huang et al. 2007].

Low broadband reflection has been measured in various tapered silicon sub-wavelength structures fabricated by dry etching [Kanamori et al. 1999, Huang et al. 2007, Wu et al. 2001, Zaidi et al. 2001, Yu et al. 2003, Lee et al. 2005, Chang et al. 2005] or chemical etching [Jung et al. 2010] a silicon wafer. In 1999, Kanamori et al. showed that an array of periodic silicon nanocones fabricated by a combination of electron-beam lithography and fast atom beam etching with SF_6 gas could lower reflectivity to less than 3% in the wavelength range of 200 – 1000 nm [Kanamori et al. 1999]. The periodicity of the array was 150 nm and height of the nanocones was ~350 nm.

Nanocones fabricated by the top-down approach from thin films of amorphous silicon [Zhu et al. 2009] and crystalline silicon [Lu et al. 2010] have also demonstrated high broadband absorption. Zhu et al. fabricated an array of amorphous silicon nanocones and quasi-nanowire by dry etching a 1 µm thick layer of amorphous silicon on ITO coated glass [Zhu et al. 2009]. Quasi-nanowires had a diameter of about 300 nm and height of about ~600 nm whereas the nanocones had a tip diameter of ~20 nm, base diameter of ~300 nm, and a height of ~600 nm. The measured absorption of the nanocone sample was an impressive 98.4% at normal incidence (0°) which was higher than that of both the quasi-nanowire array (85%) and the thin film (75%). In addition, the nanocones exhibited absorption of >90% for an incident angle of up to 60°.

A periodic vertical array of silicon nanocones fabricated from a crystalline silicon-on-insulator (SOI) wafer has also exhibited very high broadband absorption [Lu et al. 2010]. Nanocones and quasi-nanowires were fabricated by patterning a 5 µm layer of silicon on an insulator wafer by electron lithography, followed by RIE etching. The slant angles, 3.8° for nanocones and 0° for quasi-nanowire, were achieved by changing the RIE conditions. Each sample consisted of 3.5 µm of ordered silicon nanocones/quasi-nanowires on top of 1.5 µm of planar silicon and 2 µm of buried oxide. An array of nanocones with a lattice constant of 800 nm exhibited an extremely high

absorption of 99% and ultralow reflection of <1% between the wavelength region of 400-1100 nm. The nanocones were also incorporated into a radial p-n junction solar cell that demonstrated a conversion efficiency of 10.8% and short circuit current density of 26.4 mA/cm^2 [Lu et al. 2010].

2.5 Nanowire solar cells

In addition to high absorption capability and low broadband reflectivity the high aspect ratio structure of silicon nanowires can improve photogenerated carrier collection efficiency by shortening collection lengths. Kayes et al. modeled radial p-n junction nanorod solar cells and found that large improvements in performance relative to conventional planar p-n junction solar cells can be made if two conditions are satisfied: (1) the device material has minority carrier diffusion lengths that are at least 2 orders of magnitude lower than their optical thickness and (2) the material has low depletion region recombination with lifetimes >~10 ns for Si [Kayes et al. 2005].

Table 2-7: Summary of several studies reported on silicon nanowire solar cells. The structure type is differentiated between a radial and axial design and device structure is described between p-i-n, p-n, p$^+$n-n$^+$ or metal-semiconductor-metal (MSM). The fabrication type can be either a bottom-up approach grown on a substrate or a top-down approach in which nanowires are etched from a Si substrate. A single nanowire solar cell is differentiated from an array of nanowires and the method from contacting the nanowires is also listed. Finally the reported device performance is listed in terms of the energy conversion efficiency η.

Reference	Structure Type	Fabrication Type	Substrate	Single/Array	Nanowire Contact	Device Performance
[Tian et al. 2007]	Radial p-i-n	Bottom-up	c-Si	Single	e-beam lithography	η = 3.4 %
[Tsakalakos et al. 2007]	Radial p-n	Bottom-up	SS	Array (1.8 cm^2)	ITO, Ti/Al fingers	η = 0.1%
[Kelzenberg et al. 2008]	Axial MSM	Bottom-up	c-Si <111>	Single	e-beam lithography	η = 0.46%
[Kempa et al. 2008]	Axial p-i-n	Bottom-up	c-Si	Single	e-beam lithography	η = 0.5%

[Stelzner et al. 2008]	Radial p-n	Bottom-up	c-Si	Array (0.6 cm^2)	Press against TCO coated polymer	η = 0.1%
[Perraud et al. 2009]	Axial p-n (planarized)	Bottom-up	c-Si	Array (2.3 cm^2)	ITO, Ni/Al grid	η = 1.9%
[Kendrink et al. 2010]	Radial p-n	Bottom-up	c-Si <111>	Array (0.06cm^2)	cold pressed Indium	η = 2.3%
[Cho et al. 2011]	Radial p-i-n	Bottom-up	glass	Array (0.126cm^2)	ITO	η = 4.9%
[Peng et al. 2005]	Radial p-n	Top-down	c-Si or poly-Si	Array (1cm^2)	Ti/Pd/Ag grid	η = 9.3%
[Fang et al. 2008]	Axial p-n	Top-down	c-Si <111>	Array (1 cm^2)	Ti/Pd/Ag grid	η = 11.37%
[Garnett et al. 2010]	Radial p-n	Top-down	c-Si	Array (0.44 cm^2)	Al/Pd grid	η = 5.3%
[Lu et al. 2010] (Nanocones)	Radial p-n	Top-down	c-Si	Array	Al grid	η = 10.8%

Top Contact
p-type NWs
n-type film
ITO
Ta2N
[Tsakalakos 2007]

Top Contact
n-type NWs
ITO
SOG
p-type c-Si
[Perraud 2009]

Top Contact
n-type NWs
n-type c-Si
p-type c-Si
[Fang 2008]
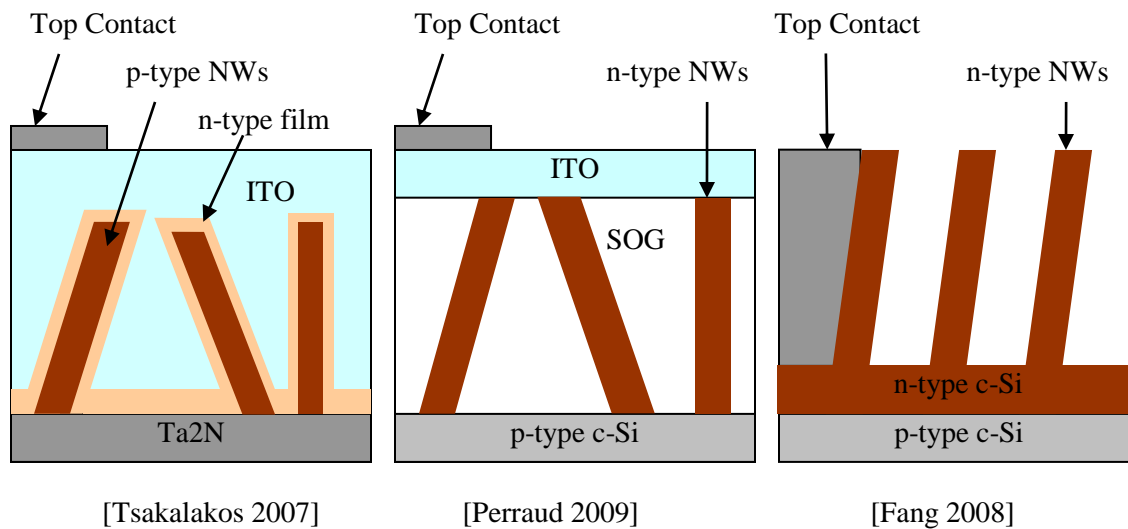
Figure 2-7: Device structure of three reports by [Tsakalakos et al. 2007], [Perraud, et al. 2009] and [Fang et al. 2008].

There are a number of challenges that exist when incorporating nanowires into solar cells such as minimizing surface recombination, high top contact resistance due to increased surface area, non-conformal coverage in high density arrays, repeatable probing of the top contact without breaking nanowires, which would cause shorting of devices. This section presents an overview of reported studies on nanowire solar cell fabrication. A list of reported nanowire solar cells is summarized in Table 2.5 of which three device structures (bolded in Table 2.5) are illustrated in Figure 2.7.

Silicon nanowire solar cells can be generalized into two structural categories, the radial nanowire solar cell where charge carriers travel radially between the core and the surrounding shell [Tian et al. 2007] and the axial nanowire solar cell where charge carriers travel longitudinally along the wire. The advantage of the radial solar cell is that the carrier collection distance is smaller than that of the longitudinal nanowire so bulk recombination is lower. A radial solar cell consisting of a p-type core surrounded by an intrinsic and n-type shell having a total diameter of 300 nm was reported with a conversion efficiency of up to 3.4 % for a single nanowire [Tian et al. 2007]. Electrical contacts were defined by e-beam lithography followed by metal contact deposition. A radial solar cell over a relatively large area was also fabricated consisting of n-type a-Si coated p-type Si nanowires fabricated on Ta_2N coated stainless steel substrates with reported open circuit voltage (V_{oc}) = 0.130 V, short circuit current (J_{sc}) = 3mA/cm^2, fill factor (FF) = 0.28 and conversion efficiency (η) = 0.1 % for a 1.8 cm^2 area device [Tsakalakos et al. 2007]. The n-type a-Si coated p-type Si was covered with indium tin oxide (ITO) on which Ti/Al finger contacts were deposited. The Ta_2N was used as the bottom contact and as a diffusion barrier during nanowire growth.

A single axial nanowire solar cell has also been fabricated using Al contacts to a silicon nanowire with a reported V_{oc} = 0.190 V, J_{sc} = 5.0 mA/cm^2, FF = 0.40 and η = 0.46 % [Kelzenberg et al. 2008]. The rectifying junction was believed to be due to the formation of a Schottky barrier or p-n alloy junction. A single nanowire axial p-i-n solar cell was also reported with a V_{oc} = 0.29 V, J_{sc} = 3.5mA/cm^2, and η = 0.5% [Kempa et al. 2008]. Again electrical contacts were defined by e-beam lithography followed by Ti/Pd contact deposition. Solar cells over an array of silicon nanowires have also be reported. Solar cells consisting of n-type silicon nanowires grown by the VLS method using a gold catalyst on p-type Si wafer were reported with V_{oc} = 0.280 V, J_{sc} = 2 mA/cm^2, FF = 0.2 and η =

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0.1% for a device area of 0.6 cm^2 [Stelzner et al. 2008]. The backside of the wafer was contacted using a thin film of Al and the nanowires on the frontside was contacted by pressing the nanowire film onto a transparent polymer foil covered with a transparent conductive oxide layer. Attempts have also been made in planarizing the nanowires by first embedding them in spin on glass (SOG) and afterward performing chemical-mechanical polishing on from surface [Perraud et al. 2009]. Nanowires were grown by VLS method using an Au catalyst on a Si substrate and the front contact consisted of an ITO layer and a Ni/Al grid on top of the planarized nanowires. The reported device performance was $V_{oc} = 0.250$ V, $J_{sc} = 17$mA/cm^2, $FF = 0.44$ and $\eta = 1.9\%$.

Silicon nanowires fabricated by etching multicrystalline p$^+$nn$^+$ doped layers deposited on glass using AgNO$_3$ and HF solutions have also been incorporated into a solar cell with a maximum device area of 0.64 mm^2. The reported device performance was $V_{oc} = 0.402$ V, $J_{sc} = 40$ mA/cm^2, and $\eta = 4.4\%$ [Sivakov et al. 2009]. However, a metal tip was used to contact the nanowires and the active area used to calculate the J_{sc} was reported to be not reliable [Sivakov et al. 2009].

Crystalline silicon solar cells fabricated by the top down approach starting with a silicon wafer have higher reported conversion efficiencies. A vertically aligned silicon nanowire array solar cell fabricated at low temperature of 50°C by etching a silicon wafer in HF-H$_2$O$_2$ solution was reported by Peng et al [Peng et al. 2005]. The nanowire device consisted of a p-n junction in which the nanowires were doped n-type in a quartz tube furnace. The nanowire array device conversion efficiency was 9.31% when fabricated from a monocrystalline silicon substrate and 4.73% when fabricated from a polycrystalline silicon substrate.

Slanted nanowire array solar cells were fabricated by etching p-type silicon substrates using a silver catalyst and HF-H$_2$O$_2$ solution and doping the wires n-type [Fang et al. 2008]. Reflectance was shown to decrease dramatically for Si substrates with silicon nanowire etched into them as compared to polished Si wafers. However the reported conversion efficiencies of $\eta = 11.37\%$ when incorporating Si nanowires was still lower than the conventional silicon nitride coated single crystalline silicon solar cells which had an efficiency of $\eta = 15.9\%$. Reasons given for the lower performance in silicon nanowire solar cells were low current collection efficiency of the front grid electrodes used and accelerated surface recombination due to the increased surface area of the nanowires which increased the number of surface defects and dangling bonds [Fang et al. 2008]. Similarly, a silicon nanowire array was fabricated by etching a silicon wafer by reactive ion etching

while using an array of silica beads as an etch mask. This device showed a slight improvement in short current density but a drop in both open circuit voltage and fill factor due to higher recombination caused by higher surface and junction area [Garnett et al. 2010]. The resulting conversion efficiency for 8 μm nanowires was about 4.8%.

2.6 Other applications of silicon nanowires

Nanowires have unique optical, electrical, and thermal properties compared to their bulk material counterparts and as a result have a wide range of potential applications. For example, silicon nanowires have been used in active bipolar transistors [Cui and Lieber 2001], electrical switches [Dong et al. 2008], lithium battery anodes [Chan et al. 2008], sub-wavelength waveguides [Law et al. 2004], chemical sensors [Zhou et al. 2003], DNA and biological species detection [Cui, Wei et al. 2001, Hahm et al. 04, Li et al. 04], and cancer marker detection [Zheng et al. 2005]. In this section, two other applications are considered in more detail: thermoelectric power generation and photoelectrochemical cells for H_2 production. Furthermore, the fabrication and characterization of silicon nanowire photodetectors for indirect medical X-ray imaging is also discussed in Appendix A.

2.6.1 Thermoelectric power generation
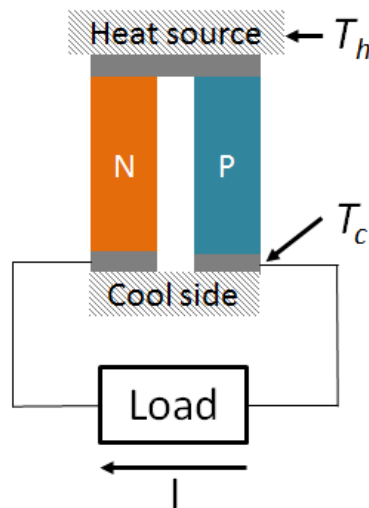
Figure 2-8: Illustration of a thermoelectric generator. The p and n regions are doped thermoelectric materials. T_h is the temperature at the heat source and T_c is the temperature at the cool end of the device.

When current is passed through a thermoelectric material, heat can be transferred from one side of the material to the other via the Peltier effect. Such materials have found application in thermoelectric refrigerators. Conversely, thermoelectric devices can be used to convert heat directly into electricity via the Seebeck effect. When a temperature gradient is applied across a thermoelectric material, free carriers generated at the high temperature end diffuse to the low temperature end. This creates an opposing electromotive force which stops the flow of current. Thermoelectric power generators find applications in automobiles, solar cells for increasing conversion efficiencies, and space probes that use radioisotope heat sources. A thermoelectric generator can be built if n-type and p-type semiconductors are connected in series electrically and in parallel thermally as illustrated in Figure 2-8. The gray regions in Figure 2-8, immediately above and below the n-type and p-type regions, represent electrical contacts.

The maximum heat-to-electricity conversion efficiency, η_{max}, can be obtained if the load and couple resistances are matched (i.e., $R_{Load}=R$, where R is the series resistance of one p-n thermoelectric couple). η_{max} is then then given by:

$$\eta_{max} = \frac{T_h - T_c}{T_h} \frac{\sqrt{1+ZT}-1}{\sqrt{1+ZT}+\frac{T_c}{T_h}}.$$

ZT is the thermoelectric figure of merit given by:

$$ZT = \frac{S^2 T}{\rho K}$$

where S is the Seebeck coefficient, ρ is the electrical resistivity and K is the thermal conductivity of the thermoelectric material. The value of Z for the most common thermoelectric material, Bi_2Te_3, is ~1. Recently, nanostructured materials have been shown to improve ZT by lowering thermal conductivity caused by phonon effects [Li et al. 03, Boukai et al. 08]. The thermal conductivity of silicon nanowires grown by VLS method have been reported to be as low as two orders of magnitude lower than bulk silicon [Li et al. 03]. Similarly, top-down fabricated silicon nanowires with rough wall surfaces also showed two orders of magnitude drop in thermal conductivity as compared to bulk Si [Hochbaum et al. 2008]. The Seebeck coefficient and electrical resistivity values of the silicon nanowires were the same as bulk Si resulting in a ZT=0.6 at room temperature. Atomic simulations have also been used to show that size reduction and phonon confinement do not necessarily decrease the thermal conductivity of nanowires [Donadio et al. 2009]. Instead, the 10 to 100 fold decrease in thermal conductivity was attributed to amorphous surface structure. In fact, the 100 fold decrease in thermal conductivity was calculated for a-Si coated silicon nanowires.

A silicon nanowire based thermoelectric device could be fabricated by replacing the n-type and p-type regions in Figure 2-8 with doped n-type and p-type silicon nanowires. The nanowires could be fabricated by the VLS-method while using dopant gases such as PH_3 or B_2H_6 to dope the nanowires n-type and p-type, respectively. Alternatively, nanowires could be fabricated by a top-down approach and doped by solid-phase or gas-gas diffusion, or by ion implantation.

2.6.2 Water splitting

Hydrogen is considered to be an ideal energy carrier because when converted to electricity by a fuel cell it produces only water. Currently the dominant method to produce H_2 is by a process called steam reforming which converts methane (CH_4) to H_2 but also produces CO_2, a greenhouse gas. An alternative method is use renewable energy to split water into H_2 and O_2. The simplest method to

achieve this is by connecting wind turbine or PV systems to an electrolyser but such systems are very expensive. Photoelectrochemical cells are an alternative approach to directly convert solar energy into chemically stored energy in the form of H_2.
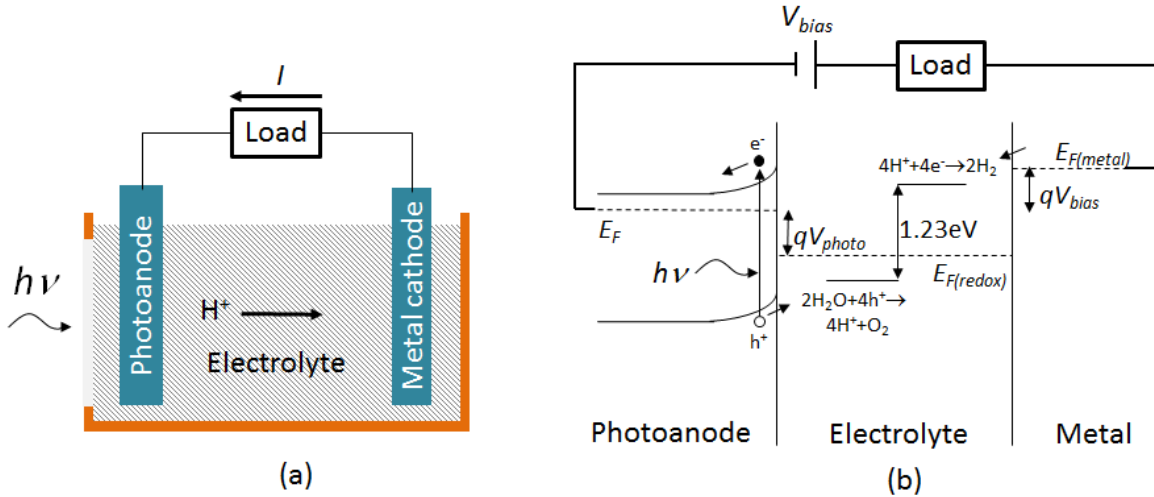
Figure 2-9: Illustration of a photoelectrochemical cell consisting of a metal cathode and the photoanode immersed in an electrolyte solution (a). The band diagram of this device under bias is shown in (b).

An illustration of a photoelectrochemical cell consisting of a metal cathode (usually Pt) and a photoanode immersed in an electrolyte solution is shown in Figure 2-9 (a). The corresponding band diagram under voltage bias is shown in Figure 2-9 (b) which is based on Ref. [Bak et al. 2002]. The photoanode is the semiconductor region where photogenerated carriers are collected and used to drive oxidation of water at the photoanode and reduction of hydrogen ions at the metal cathode. During this process, H^+ ions flow through the electrolyte from the photoanode to the metal cathode. The overall reaction can be written as:

$$4h\nu + 2H_2O \rightarrow O_2 + 2H_2,$$
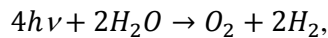
which occurs if the electromotive force of the cell is equal to or exceeds the threshold voltage (i.e., the difference between the redox potentials of H^+/H_2 and H_2O/O_2), which is 1.23 V at standard temperature of 298K. One of the most commonly used photoanode materials is TiO_2, first used in the decomposition of water by Fujishima and Honda 1972 [Fujishima and Honda 1972]. Although TiO_2 has a bandgap of 3 eV, when incorporated into a photoelectrochemical cell, it typically provides a

photovoltage (V_{photo}) of 0.7-0.9 V [Ohnishi et al. 1975] requiring a bias to exceed the threshold voltage of 1.23 V. Another method to overcome the threshold voltage is by coupling a photovoltaic cell with the photoanode. Such a hybrid photoanode-photovoltaic cell was reported by Morisaki et al. 1976. A TiO_2 coated commercially available p^+n Si solar cell was shown to split water at a solar-to-hydrogen conversion efficiency of about 0.1% [Morisaki et al. 1976]. Since TiO_2 has a bandgap of 3 eV it does not absorb the light with energies below this bandgap. Therefore, the Si solar cell was used to absorb energies between 1.1 to 3 eV. Hybrid photoanode-photovoltaic cells have also been incorporated using a WO_3- multi-junction a-Si cell, Fe2O3-multijunction a-Si cell [Miller et al. 2005], and NiFeyOx and CoMo- multi-junction a-Si cell [Rocheleau et al. 1998]. In fact, solar-to-hydrogen conversion efficiency of 2.5% was reported using Co-Mo and Fe-Ni-O coated multi-junction a-Si solar cell [Yamada et al. 2003].

A potential application for silicon nanowire based solar cells is to be used as the photovoltaic unit in the hybrid photoanode-photovoltaic cell. As discussed in section 2-4, silicon nanowires can enhance light absorption particularly at high energies and lower broadband reflection losses. One of the tradeoffs of silicon nanowire solar cell design is between a thin TCO thickness for minimizing reflectance and longer nanowires for increasing light absorption. Longer nanowires also leads to higher surface area resulting in higher TCO series resistance. In the case of photoelectrochemical cells, photogenerated carriers travel directly into the surrounding conductive electrolyte solution thereby mitigating the problem of lateral TCO series resistance. As a result, nanowires can potentially be grown longer for maximizing optical absorption when incorporated into photoelectrochemical cells.

In summary, a-Si is a large area alternative to bulk crystalline silicon. However, film thicknesses must be kept small to minimize light-induced degradation and to achieve efficient charge collection, which is limited by low carrier diffusion lengths. Device modeling of a-Si solar cells by Sentauraus showed that high reflectance and inefficient absorption at long wavelengths were significant mechanisms of collection efficiency losses. Nanostructures such as silicon nanowires can lower broadband reflectance and enhance overall absorption. Specifically, optical modeling of silicon nanowires has shown that nanowires with a suitable diameter and periodicity can exhibit significantly higher optical absorption than an equivalent thickness Si film. The higher absorption in silicon nanowires can be attributed to low broadband reflectance and strong light scattering. These optical properties make silicon nanowires promising for photovoltaic devices. Other application that may

benefit from the optical properties of silicon nanowires are thermoelectric generators and photoelectrochemical cells.

Chapter 3
Experimental and Instrumental Methodology

The experimental and instrumental methodology used to grow and characterize nanowires is presented in this section. In addition, thin film n-i-p silicon device deposition conditions and procedures are discussed. Methodology of optical and structural characterization of silicon nanowires and device performance measurements of solar cells are also discussed.

3.1 Growth of silicon nanowires

Silicon nanowires were grown by the Vapor-Liquid-Solid (VLS) technique [Wag64] in an RF parallel plate PECVD deposition system. Nanowires were grown on Corning 1737 or Corning Eagle XG glass substrate and sometimes p-type (100) silicon wafer. The native oxide on the Si substrate was not removed so that disordered nanowire growth would be similar on both glass and Si substrates. Glass substrates were cleaned by immersed ultrasonic bath in acetone for 10 min., ultrasonic bath in isopropanol for 10 min., and a DI water rinse. The Si wafers were cleaned in RCA-1 standing cleaning solution.

Sn nanoclusters were used as the catalyst for nanowire growth. The nanoclusters were formed by depositing a 2 nm thick Sn film by e-beam evaporation followed by annealing in vacuum at 400°C for 1 hour in the growth chamber. The thickness was monitored by a calibrated quartz crystal thickness monitor. Nanowires consisting of an a-Si shell were grown using pure SiH_4 source gas and nanowires with an nc-Si shell were grown using SiH_4 diluted in H_2. In the latter case, a high H_2 dilution of $[H_2]/[SiH_4]=82$ was used to suppress the growth of uncatalyzed a-Si and also improve nanowire growth uniformity across the substrate. The deposition pressure in each case was 1400mTorr controlled automatically by a PID-controlled throttle valve. A 13.56 Mhz RF plasma density was set to 0.0137 to 0.0215 W/cm^2 and was used to control the thickness of the shell. The nanowire growth temperature was 400°C and the growth time was 15 to 30 min.

3.2 Fabrication of silicon core-shell solar cells

An Al thin film deposited by magnetron sputtering on Corning Eagle XG glass was used as the back contact. An array of silicon nanowires was grown on the Al film using Sn nanoclusters as a growth catalyst. A thin layer of ZnO:Al was sputtered onto the nanowires to provide a diffusion barrier to prevent counter-doping of the n$^+$ layer by the Al back contact. The ZnO:Al layer also improved photocurrent generation within the device by increasing reflection at the back contact.

Table 3-1: Deposition conditions for the n$^+$ nanocrystalline Si (nc-Si), p$^+$ nc-Si, intrinsic a-Si and intrinsic nc-Si layers. The flow rates are given by *m* in the unit standard cubic centimeters per minute (sccm).

Film	n$^+$ nc-Si	p$^+$ nc-Si	Intrinsic a-Si	Intrinsic nc-Si
m_{SiH4}(sccm)	1.6	1.6	20	4.5
m_{H2} (sccm)	200	200	-	246
m_{PH3} (sccm)	2.5	-	-	-
m_{B2H6} (sccm)	-	1.6	-	-
Substrate Temp (°C)	230	100	180	180
Pressure (mTorr)	750	1500	400	7000
Power density (mW/cm^2)	176	234	7.8	371
Dep. Rate (nm/s)	0.042	0.148	0.167	0.231

The n-i-p device was fabricated using the same PECVD cluster tool system as the silicon nanowires which consisted of 4 separate deposition chambers. In fact, the silicon nanowires were grown in the same chamber as the nc-Si intrinsic layer. A separate chamber was used for both n$^+$ and p$^+$ doped layer depositions and another chamber used for intrinsic a-Si depositions. The last chamber was for ZnO:Al magnetron sputtering. Base pressure for all layers was < 1 µTorr and the substrate temperature was controlled using a heater well located above the substrate. The thin film silicon layers were fabricated by capacitively coupled parallel plate RF (13.56 Mhz) plasma deposition. The n$^+$ layer was nc-Si deposited using a combination of SiH$_4$ and PH$_3$ and H$_2$ source gases under high hydrogen dilution conditions [Veen 2003]. The p$^+$ layer was also nc-Si, deposited using SiH$_4$, H$_2$ and B$_2$H$_6$ source gases under low temperature, high power density deposition conditions [Du et al. 2006]. The PH$_3$ and B$_2$H$_6$ dopant gases were both 1% diluted in H$_2$. The intrinsic a-Si layer was deposited using pure SiH$_4$ source gas without hydrogen dilution. The intrinsic nc-Si layer was strongly diluted

in hydrogen ([H_2]/[SiH_4]=55) to achieve high crystallinity near the crystalline-amorphous phase transition point, known to result in the best solar cell performance [Vetterl et al. 2001]. This nc-Si layer was deposited under high power, high pressure deposition conditions, which are known to lead to high growth rate, high performance nc-Si devices [Rech et al. 2001]. An overview of the deposition conditions of each layer is shown in Table 3-1. The deposition rate was determined by measuring the thickness of the film at an etched edge on glass substrate. Transparent conductive ZnO:Al contacts were deposited by magnetron sputtering from a 4" ZnO doped with 2%wt Al target. The substrate temperature was 200°C, the target-substrate distance was 10 cm, and the deposition pressure was 2mTorr. A higher deposition pressure of 5 mTorr was used only for coating the nanowires with ZnO:Al.. The top ZnO:Al thickness was measured to be ~75 nm. Ag gridlines were deposited by e-beam evaporation to lower series resistance of the top ZnO:Al layer. Gridlines had a thickness of about 100 nm and were patterned by lift-off technique. In addition, a drop of conductive Ag paste was placed on the grid line to act as a point of contact for probes. Probing the top contact without this Ag paste led to nanowires breakage and device shorts. The active solar cell device area was ~0.44 cm^2 defined by the area of the exposed ZnO:Al top contact.

Planar control n-i-p cells were fabricated on planar Corning eagle XG glass substrates with no intentional texturing. The reference device structure was glass/Al (120nm)/ZnO:Al (60nm)/n$^+$ (50nm)/i-layer/p$^+$(30nm)/ZnO:Al (75nm)/Ag gridlines. The a-Si intrinsic layer thickness was 300 nm and the nc-Si intrinsic layer thickness was 1000 nm.

3.3 Characterization Methods

Thickness of thin films on glass was measured using a Dektak 8 stylus thickness profilometer. Radial thickness of layers grown around nanowires was determined from SEM images before and after a deposition. Similarly, the average length and diameter of nanowires were also determined from SEM images measured using a Leo 1530 field-emission SEM system. The crystal structure of nanowires and films were characterized by X-Ray diffraction (XRD), Raman spectroscopy, and Transmission Electron Microscopy (TEM). Grazing angle X-ray diffraction spectra were measured on a PANalytical X'Pert PRO X-ray diffractometer. Raman spectra were measured using a Renishaw Raman spectrometer in a backscattering setup with 633 nm or 488 nm laser excitation. TEM micrographs were measured using a JEOL 2010 field emission TEM or a FEI Titan microscope

equipped with a CEOS image corrector operated at 300 kV. TEM samples were prepared by scraping a holey-carbon TEM grid over nanowire samples.

The total optical transmission and reflectance (including both specular and diffuse components) were measured by a Cary 5000 UV-Vis-NIR spectrophotometer equipped with an integrating sphere. The total absorption (A) was defined as A=1-T-R where T is the total transmission and R is the total reflection. Diffuse and specular reflectance was also measured separately using a Shimazu UV-2501PC UV-Vis spectrophotometer over the wavelength range of 250 to 850 nm.

Solar cell performance were characterized by external quantum efficiency (EQE) and current density (J)-voltage (V) measurements under AM 1.5 global illumination (100 mW/cm^2). A PV Measurements Inc. quantum efficiency system calibrated using a silicon photodiode before measurements was used for EQE measurements. JV curves were measured using a Keithley 2400 source meter and solar simulator (ABET Technologies SUN 2000 series) system calibrated using a pre-calibrated monocrystalline silicon solar cell prior to measurements. The short current densities, J_{sc}, measured under AM 1.5 global illumination were in agreement to within 2-3% of the J_{sc} determined from integrated-EQE measurements.

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Chapter 4

Core-shell nanowires

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The structural and optical properties of two types of core-shell silicon nanowires are presented. The first type is crystalline-amorphous core-shell silicon nanowires and the second type is homo-epitaxial core-shell silicon nanowires. In both cases, the nanowire core is highly crystalline, grown by VLS method. Arrays of both types of core-shell silicon nanowires exhibit significantly higher broadband absorption than reference thin film silicon planar films.

4.1 Crystalline-amorphous core-shell nanowires
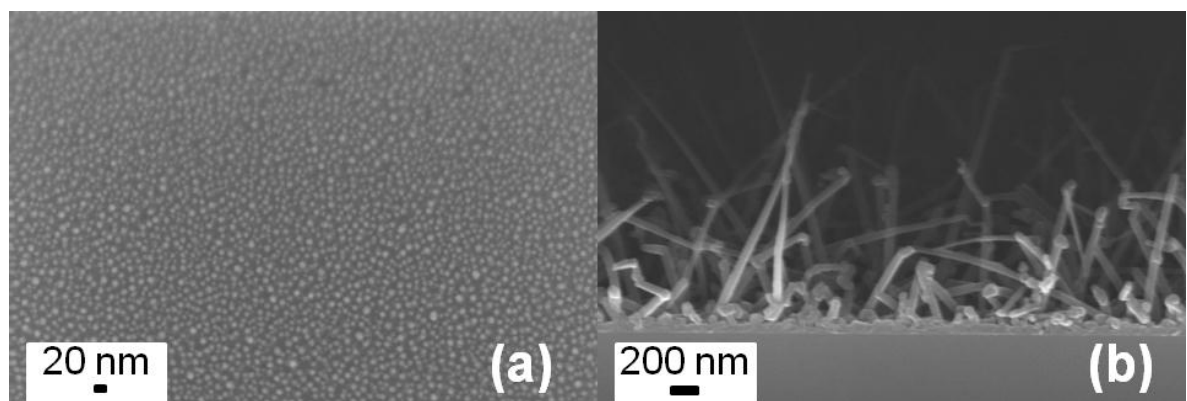
Figure 4-1: SEM micrograph of (a) plan-view of Sn catalyst islands after annealing a 2 nm thick Sn film and (b) cross sectional view of silicon nanowires grown by PECVD with diameters of 30-60 nm. Reprinted with permission from [Adachi et al 2010]. Copyright 2010 American Chemical Society.

Figure 4-1(a) shows a plan-view SEM micrograph of Sn catalyst islands with diameters ranging between 5- 10 nm which was formed after annealing the 2 nm thick Sn film. A cross-sectional SEM image of silicon nanowires grown using the catalyst shown in Fig 4-1 (a) on silicon substrate is shown in Figure 4-1 (b). The silicon nanowires were grown at a power density of 0.0164 W/cm^2 at which the nanowire diameters ranged from 30-60 nm.

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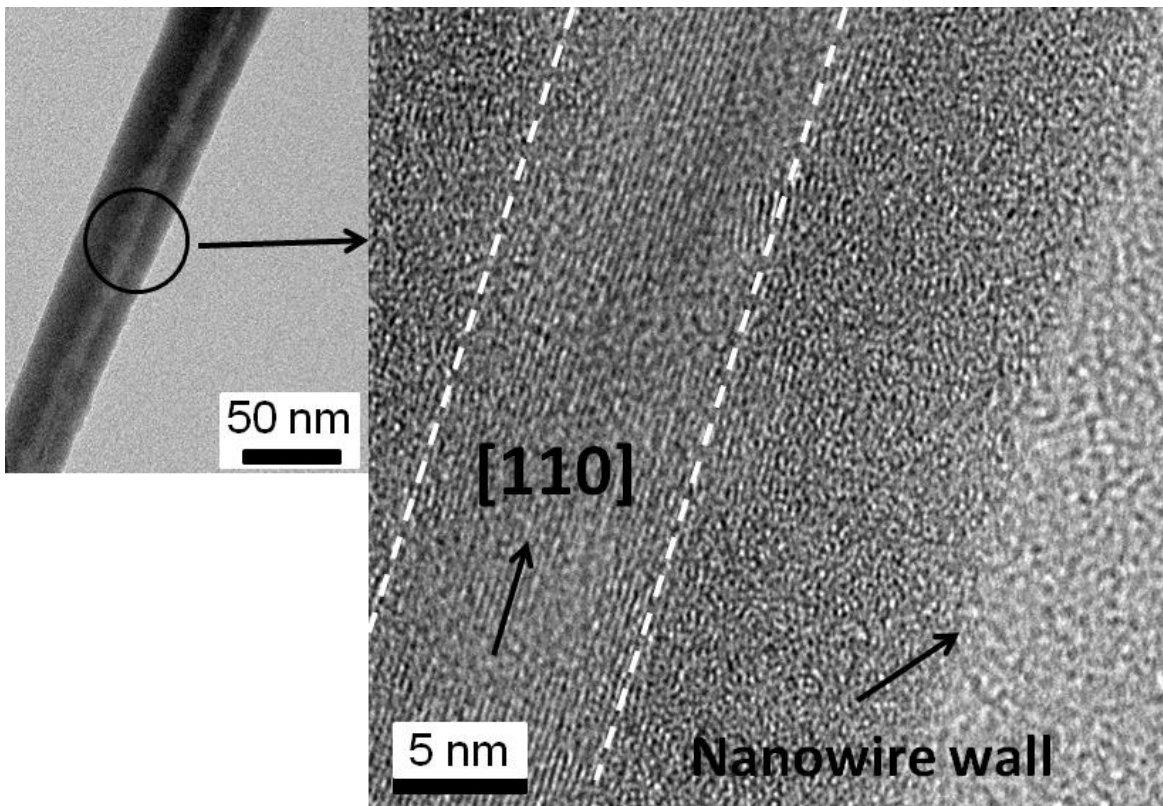
Figure 4-2: High resolution TEM micrograph of a silicon nanowire grown at a power density of P=0.0164 W/cm^2.The nanowire consists of a highly crystalline core with visible Si (111) lattice fringes with a lattice spacing of 0.31 nm surrounded by an amorphous shell. The crystalline core has a diameter of 9.2 nm and the nanowire growth direction is [110]. The lighter amorphous pattern in the background located to the right of the Nanowire wall is the carbon TEM grid. Reprinted with permission from [Adachi et al 2010]. Copyright 2010 American Chemical Society.

The high resolution TEM micrograph of a silicon nanowire grown at the same deposition conditions as in Figure 4-1 (b) is shown in Figure 4-2. The nanowire consists of a highly crystalline core with visible Si (111) lattice fringes separated by a spacing of 0.31 nm. The crystalline core has a diameter of 9.2 nm and has a growth direction of [110] surrounded by an amorphous shell resulting in a total nanowire diameter of around 42 nm. Note that the crystalline core is not centered within the

surrounding amorphous shell because deposition favored one side over the other due to slanting of the nanowire during growth.
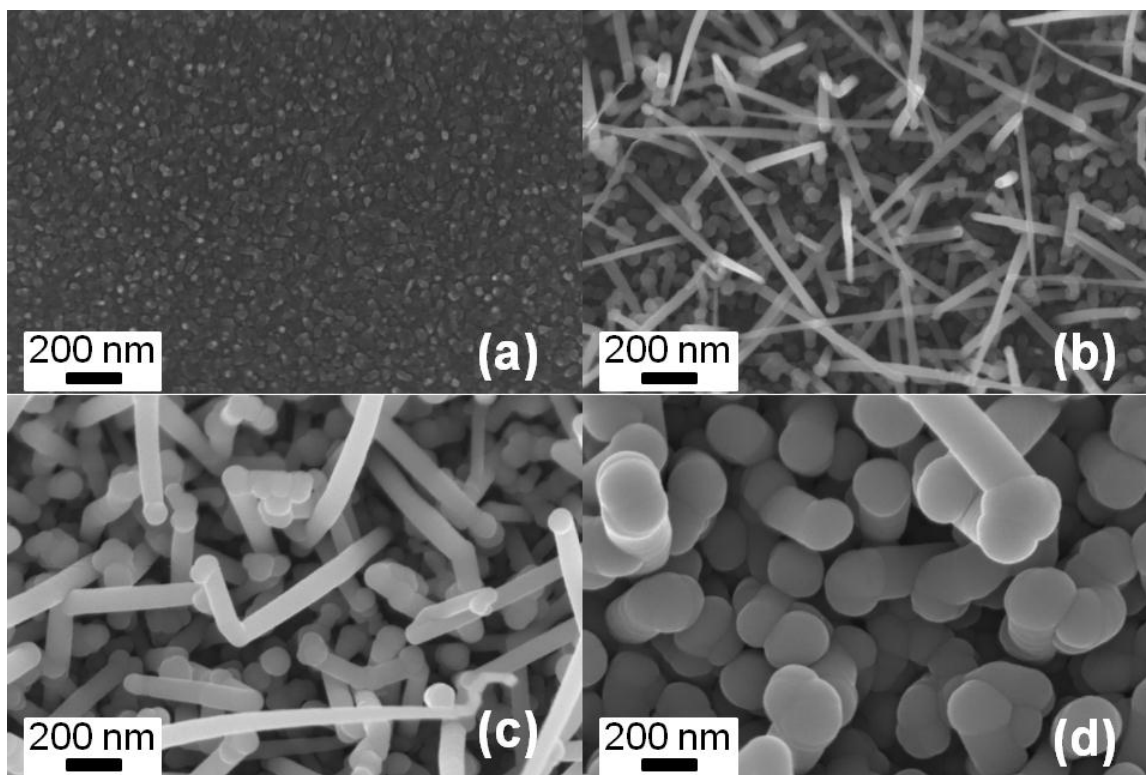
Figure 4-3: Planar SEM micrograph of nanowires grown at a pressure = 1400 mTorr for 30 min. using different power densities of (a) $P = 0.0137$ W/cm^2, (b) $P = 0.0156$ W/cm^2, (c) $P = 0.0164$ W/cm^2 and (d) $P = 0.0195$ W/cm^2. Reprinted with permission from [Adachi et al 2010]. Copyright 2010 American Chemical Society.

Energy dispersive x-ray fluorescence (EDX) on the nanowire sample showed a large Si peak followed by a tiny O peak, which may have originated from a thin layer of native surface oxide. The EDX measurements did not detect the presence of Sn either through the center of the nanowire or at the nanowire tip. The latter indicates that nanowire growth ceased because the Sn catalyst was either

consumed or evaporated. Note that some silicon nanowires were observed to lack a crystalline core and instead consisted of small crystallites surrounded by an amorphous silicon matrix.

The effect of plasma power on nanowire structure, crystallinity and optical properties was investigated. SEM micrographs of nanowires grown at four different power densities are shown in Figure 4-3 and a summary of measured nanowire lengths, diameters and uncatalyzed a-Si thicknesses on the substrate are shown in Table 4-1. No nanowire growth was observed at the lowest power density of 0.0137 W/cm^2 as shown in Figure 4-3 (a). The use of plasma was found necessary for silicon nanowire growth from Sn catalyst at the relatively low growth temperature of 400 °C used in this study. Increasing the power density to 0.0156 W/cm^2 resulted in a dense array of silicon nanowires as shown in Figure 4-3 (b). An increase in the nanowire diameter and the thickness of the amorphous shell was observed with increase in power density. Table 4-1 also shows that an increase in deposition power density leads to a thicker uncatalyzed a-Si film on the silicon substrate located below the nanowires.

Table 4-1: Summary of the effect of deposition power density on silicon nanowire (NW) diameter, NW length and uncatalyzed a-Si thickness on the substrate. Reprinted with permission from [Adachi et al 2010]. Copyright 2010 American Chemical Society.

Deposition Power Density (W/cm^2)	Total NW diameter (nm)	Average NW length (nm)	a-Si layer thickness on substrate (nm)
0.0137	No nanowires	-	-
0.0156	15-40	1738	60
0.0164	30-60	2289	80
0.0176	55-90	2100	80
0.0195	150-180	1282	100

From Table 4-1, the longest average nanowire length measured was 2289 nm, which corresponds to a power density of $P = 0.0164$ W/cm^2. As the power was increased further, the

nanowire length decreases along with an increase in the thickness of the a-Si on the nanowire. Silicon nanowires cease growing if the catalyst is consumed or the deposition conditions are changed [Wagner et al. 1964]. Since the deposition conditions were kept constant, the catalyst was likely consumed. If the power density was increased to $P = 0.0195 \text{W/cm}^2$, the nanowire length decreased to 1282 nm while the uncatalyzed a-Si thickness increased to 100 nm suggesting the competing uncatalyzed a-Si deposition led to suppression of nanowire growth. In fact, if the power was increased to 0.0438 W/cm^2 nanowire growth was almost completely suppressed resulting in only large bumps.
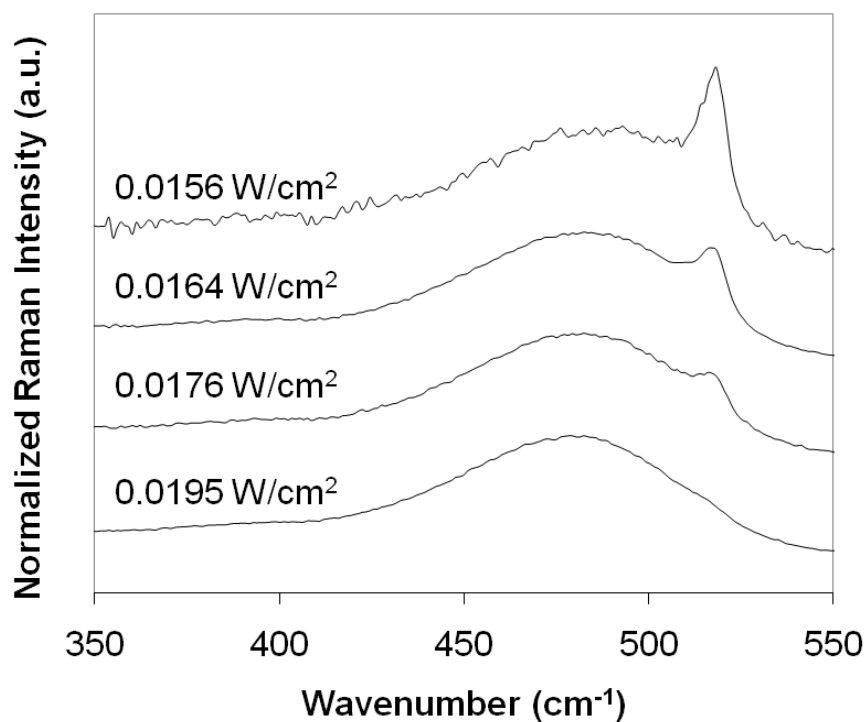
Figure 4-4: The Raman spectra of silicon nanowires grown at different power densities show that the amorphous silicon coverage increases with power density. The crystalline silicon peak at 520 cm^{-1} from the nanowires decreases for increasing power density because of increased coverage of uncatalyzed amorphous silicon indicated by the broad peak at 480 cm^{-1}. Reprinted with permission from [Adachi et al 2010]. Copyright 2010 American Chemical Society.

The transition from nanowire growth to conformal uncatalyzed amorphous silicon growth can be identified from the nanowire crystallinity. The normalized Raman spectra for nanowires grown at four different power densities are shown in Figure 4-4. The sharp peak at 520 cm^{-1} is from crystalline silicon and the broad peak at 480 cm^{-1} from amorphous silicon. The crystalline silicon peak decreases for increasing power density because of increased coverage of uncatalyzed amorphous silicon. Note that the broad amorphous peak is present even at the lowest power and is due to uncatalyzed a-Si located on the nanowires and on the substrate.
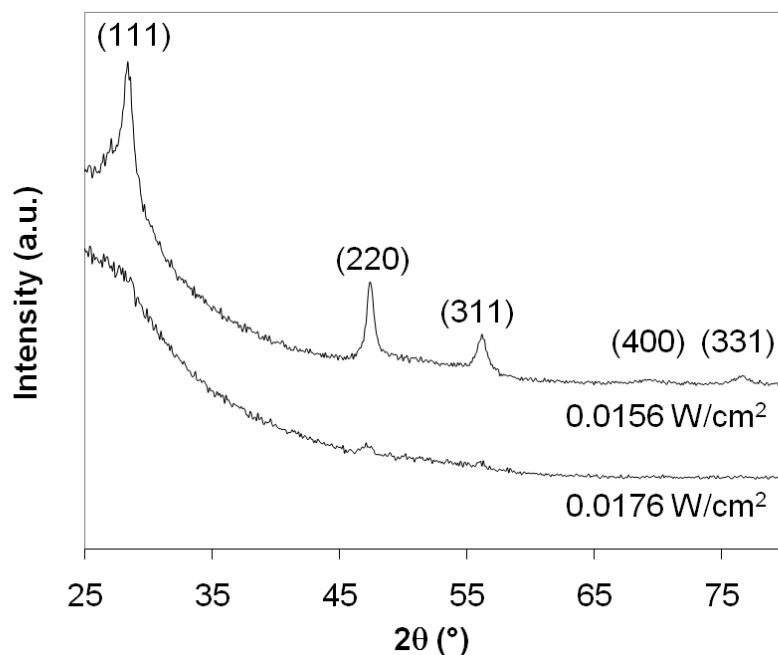
Figure 4-5: XRD intensity of silicon nanowires grown at two different power densities, 0.0156 W/cm^2 and 0.0176 W/cm^2. The crystal orientations corresponding to XRD peaks are shown in brackets. The nanowires grown at 0.0156 W/cm^2 have highly crystalline (111), (220) and (311) peaks. The same peaks for the nanowires grown at 0.0176 W/cm^2 are suppressed by the amorphous silicon shell. Reprinted with permission from [Adachi et al 2010]. Copyright 2010 American Chemical Society.

The crystalline structure of silicon nanowires grown for two different power densities of $P =$ 0.0156 W/cm^2 and $P = $ 0.0176 W/cm^2 was also characterized by X-Ray Diffraction. The XRD spectra are shown in Figure 4-5. Nanowires grown at 0.0156 W/cm^2 have large (111), (220), (311) crystalline peaks and small peaks at (400) and (331). Solving for the Scherrer formula (d =kλ/βcosθ), the crystalline size was estimated to be 12.9 nm from the (111) XRD peak, which compares well to that of the crystalline core with a diameter of 9.2 nm measured by TEM (Figure 4-2). The XRD pattern for nanowires grown at $P = $ 0.0176 W/cm^2 is shown for comparison. The coverage by amorphous silicon strongly scattered the x-rays which suppressed the peaks of the crystalline core of the nanowires.
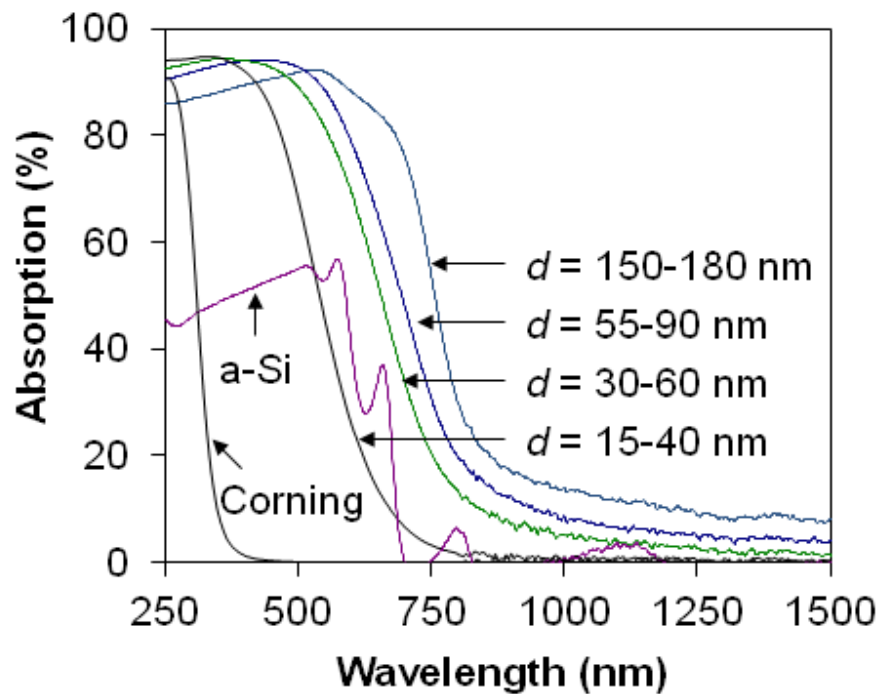
Figure 4-6: Absorption (1-T-R) as a function of wavelength for silicon nanowires with varying total diameters, d. The absorption of a thin film of a-Si with a thickness of t = 400 nm is also shown for comparison. For the lowest diameter silicon nanowire array of d=15-40nm, the short wavelength absorption is very high (95%) but drops abruptly to < 2% for longer wavelengths, λ > 780 nm. The absorption edge of silicon nanowires shifts to longer wavelengths for increasing total diameter well beyond the absorption limit of thin film amorphous silicon. Reprinted with permission from [Adachi et al 2010]. Copyright 2010 American Chemical Society.

The effect of the amorphous silicon shell on the optical properties was investigated by transmission and reflection measurements. Figure 4-6 shows the effective optical absorption of silicon nanowires with varying diameters. The absorption is defined as *1-T-R* where *T* is the total transmission and *R* is the total reflectance. For comparison, the absorption and total reflectance of a thin film of 400 nm thick a-Si is shown in Figure 4-6. The absorption by the a-Si film is limited to < 55% for all wavelengths due to the large reflectance shown in Figure 4-7 (b). At low incident optical wavelengths, all nanowires show a very high absorption of between 85 – 95 %, depending on the nanowire diameter. High absorption by VLS grown silicon nanowires has been reported previously [Tsakalakos et al. 2007, Stelzner et al. 2008] and is attributed to enhanced light trapping (i.e., increasing the path length of incoming light) in nanowire arrays. Nanowires grown from VLS method consist of a distribution of diameters [Westwater et al. 1997, Tsakalakos et al. 07, Stelzner et al. 08] mainly due to variation in the initial catalyst nanoparticle size. As a result each absorption curve in Figure 4-6 is due to the overall absorption for an array of nanowires consisting of the specified range of diameters.
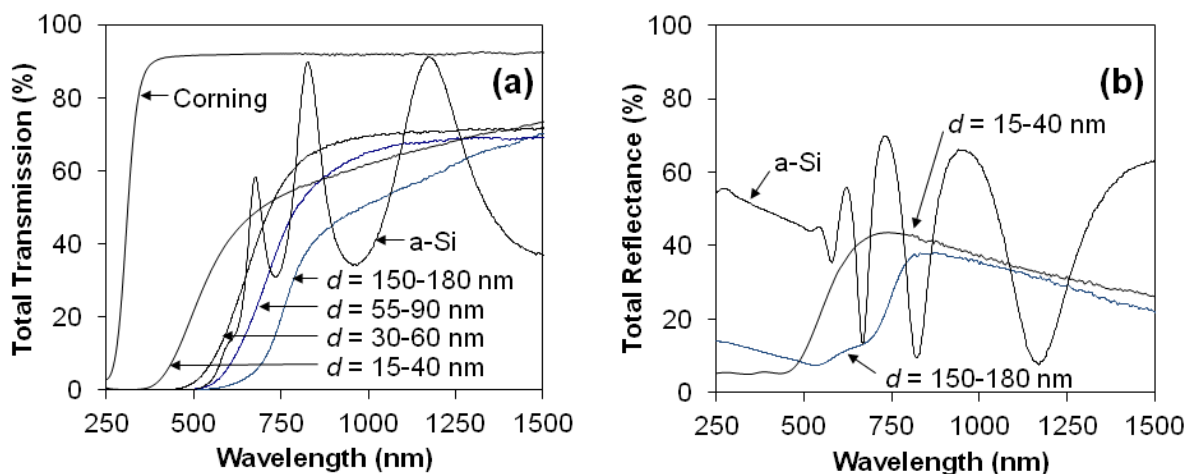
Figure 4-7: (a) Total transmission and (b) total reflectance as a function of wavelength for different total diameters, *d*. The transmission is zero at short wavelengths and becomes non-zero at wavelengths dependent on *d*. Reprinted with permission from [Adachi et al 2010]. Copyright 2010 American Chemical Society.

A significant feature of absorption spectra in Figure 4-6 is the rather abrupt drop in absorption for all nanowire diameters with the drop extending to longer wavelengths from $\lambda \sim 550$ nm to 760 nm as the diameter increases. The shift in absorption edge is explained by an increase in the filling ratio (i.e., the area ratio between nanowires and substrate). In this work, the density of nanowires (i.e., number of nanowires per area) agree within a measurement error of 10% for the first three nanowire arrays (d=15-40 nm, d=30-60nm and d= 55-90nm). As a result an increase in amorphous shell thickness results in an increase in filling ratio.

The nanowire array with the largest total diameter of d=150-180nm has a lower nanowire density than the smaller diameter arrays because neighboring nanowires merge with each other. Nevertheless, the same trend of increase in long wavelength absorption was observed for the d=150-180nm array in Figure 4-6. Interestingly the long wavelength absorption is highest for this diameter even though the length of these nanowires is considerably shorter at 1.28 μm. The bandgap of a-Si is around 1.78 eV (wavelength ~ 700 nm). However absorption at significantly longer wavelengths is observed (for example 54% at λ=750 nm) which can be attributed to enhanced light trapping ability of nanowires. The absorption could originate from the crystalline silicon core absorbing light at the wavelengths that correspond to energies longer than that of the a-Si bandgap and absorption due to bandtails of a-Si.

Another significant feature from Figure 4-6 (a) is the sudden drop in absorption at wavelengths comparable to the bandgap of amorphous silicon (1.78eV). The sub-bandgap absorption (λ>1200 nm) drops to values smaller than 10% in all samples considerably lower than that reported by nanowires grown using Au catalyst [Tsakalakos et al. 2007, Stelzner et al. 2008]. For example, using a comparable catalyst thickness of 2.5 nm as opposed to the 2 nm used in this work, the sub-bandgap absorption for Au catalyzed silicon nanowires was reported to be up to 55% at λ = 1200 nm [Tsakalakos et al. 2007]. This suggests that the type of catalyst used during nanowire growth using the VLS method has a strong influence on sub-bandgap optical absorption. In fact, sub-bandgap optical absorption has also been reported in microstructured silicon spikes [Wu et al. 2001] and the chemical impurities (i.e., Sulfur) present at the surface of the spikes were believed to be the main contributor of the sub-bandgap absorption [Younkin et al. 2003]. In contrast the optical absorption of our nanowires points to the absence of optically active energy levels in the bandgap, a key

requirement for photovoltaic and optoelectronic applications. Such energy levels give rise to trap assisted recombination, lowering carrier lifetimes and collection efficiencies.

Figure 4-7 shows the total transmission and total reflectance of silicon nanowire arrays as a function of wavelength with varying total diameters, *d*. The absorption edge shift observed in Figure 4-6(a) is due to the shift in the wavelength at which transmission increases abruptly in Figure 4-7 (a) for different *d*. The total reflectance also shows the same trend. The color of nanowire arrays was observed to change from light orange to brown to dark purple with increase in nanowire diameter.

4.2 Crystalline-epitaxial silicon core-shell nanowires

Thus far, the core-shell nanowires have consisted of an amorphous silicon shell. Amorphous silicon has a very high absorption coefficient over the visible spectrum, but its bandgap is about 1.78 eV, and therefore it does not absorb efficiently at wavelengths above ~ 700 nm. In addition, due atomic disorder, amorphous silicon is susceptible to light-induced degradation and low carrier lifetimes as discussed in Section 2.1. One way to improve infrared absorption and improve device performance stability is to use a crystalline silicon shell, which would have a bandgap of 1.12 eV. In this section, the optical properties of a nanowire array consisting of a tapered epitaxial silicon shell are investigated.

The nanowire length was limited to an average value of about 800 nm so that the same length could be used in a core-shell nanowire device. Increasing the nanowire length further would lead to high series resistance due to the high surface area of the top transparent conductive oxide layer, resulting in low device performance.
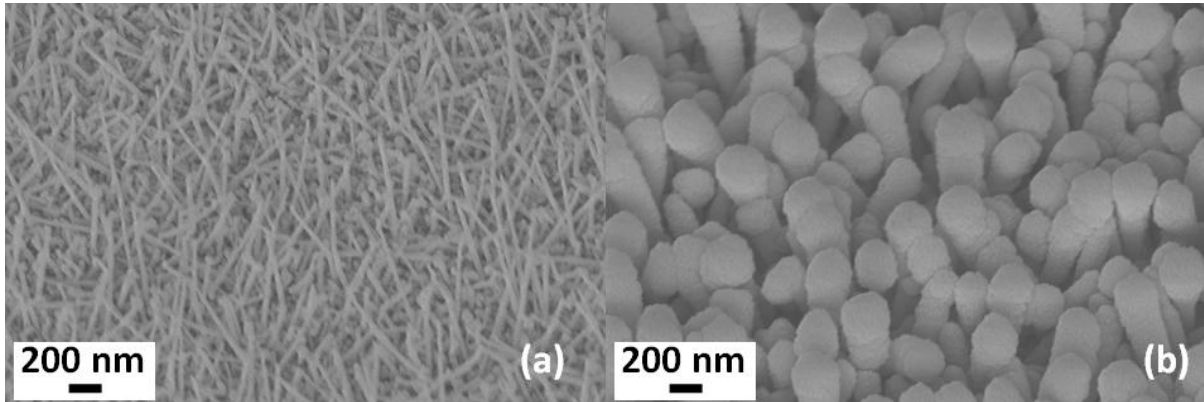
Figure 4-8: SEM (45° tilt) images of silicon nanowires (a) and silicon nanowires plus nc-Si shell (b) [Adachi et al 2012a].

Figure 4-8(a) shows a highly dense array of silicon nanowires grown directly on Corning Eagle XG glass. The average diameter of the nanowires is about 31 nm, and the average length is around 800 nm. Core-shell nanowires, grown using the same conditions as the nanowires in Figure 4-8(a) but followed by an in-situ deposition of hydrogen-diluted silicon layer, are shown in Figure 4-8 (b). The epitaxial silicon shell was deposited under high pressure (7 Torr) and high power (0.37 W/cm^2) conditions, leading to a reverse tapered profile consisting of a large rounded tip and narrow base. The average top diameter was 280 nm and average base diameter was 190 nm.
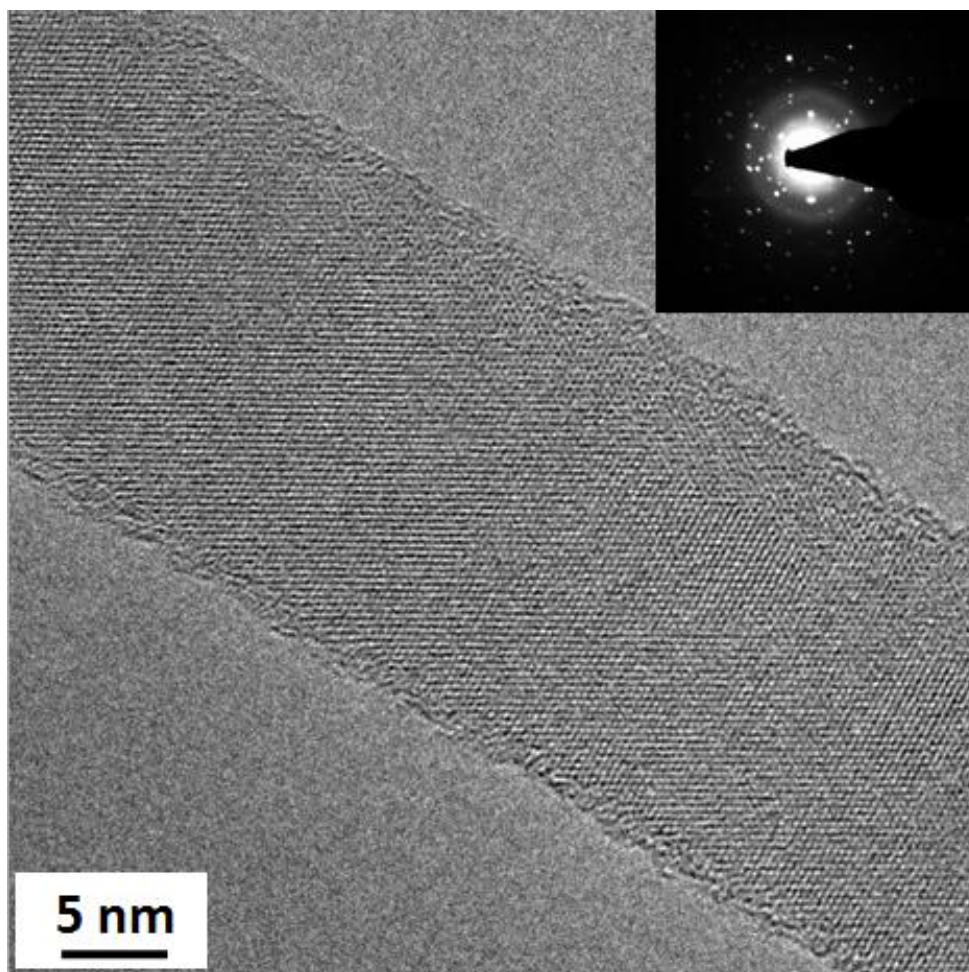
Figure 4-9: High resolution TEM micrograph of a single bare silicon nanowire. The selected area diffraction pattern of the silicon nanowire is shown in the inset at the top-right corner. The nanowire diameter is 21 nm [Adachi et al 2012a].

The high resolution TEM of a single bare silicon nanowire from the array shown in Figure 4-8(a) is shown in Figure 4-9. The nanowire is highly crystalline, with a fringe spacing of 0.31 nm, corresponding to the (111) planes of silicon. The crystalline lattice spans almost the entire diameter (21 nm) of the nanowire. Therefore, the hydrogen dilution used during nanowire growth was extremely effective in suppressing amorphous silicon growth. The selected area diffraction pattern is shown in the inset at the top-right corner. The spots are representative of high crystalline order, whereas the faint rings may be due to a very thin amorphous native oxide surrounding the nanowire.
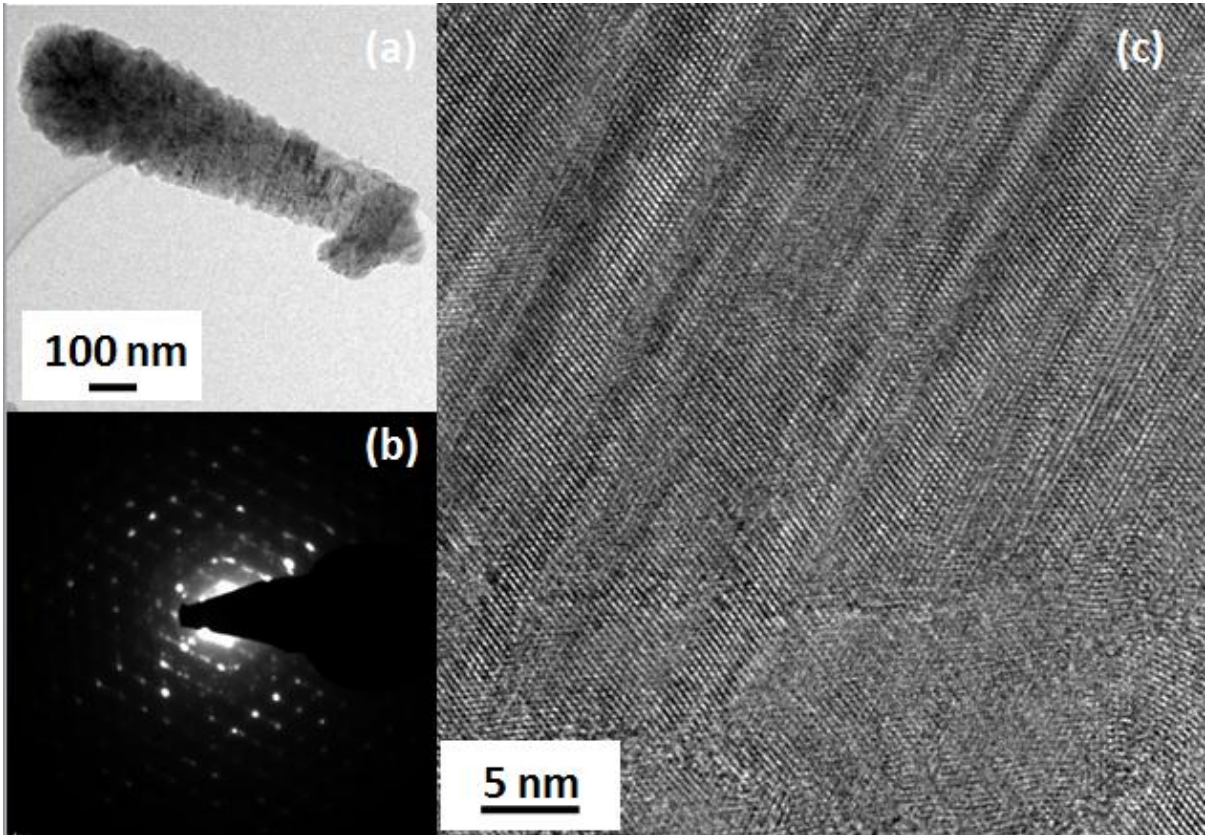
Figure 4-10: TEM micrograph of a core-shell silicon nanowire (a). The SAD pattern taken at the midpoint of the nanowire (b). High resolution TEM image taken near the edge of the nanowire shell (c) [Adachi et al 2012a].

Similarly, the high resolution TEM of a silicon nanowire after Si shell growth from array shown in Figure 4-8(b) is shown in Figure 4-10. The shell was grown by PECVD in situ in the same chamber after nanowire growth. A TEM image of a whole core-shell nanowire is shown in Figure 4-10 (a), and the selected area diffraction pattern near the center of the nanowire is shown in of Figure 4-10 (b). The diameter at the nanowire top is about 260 nm, and the diameter at the nanowire base is about 155 nm. The bright spots of the diffraction pattern are indicative of epitaxial silicon growth. A high resolution TEM image taken near the outside edge of the shell is shown in Figure 4-10 (c). The lattice spacing is ~0.32 nm which is again indicative of the (111) crystalline planes of silicon. Si-Si

homoepitaxial core-shell nanowires have previously been shown by growing an amorphous shell around a nanowire at 450°C and annealing at 600°C for 30 min. to crystallize the amorphous shell [Lauhon et al. 2002]. Figure 4-10 shows, to the author's knowledge, the first demonstration of epitaxial silicon growth on a glass substrate. Such core-shell nanowires can be used as building blocks in nanotechnology applications in which epitaxial silicon is required at low process temperatures on large area substrates.
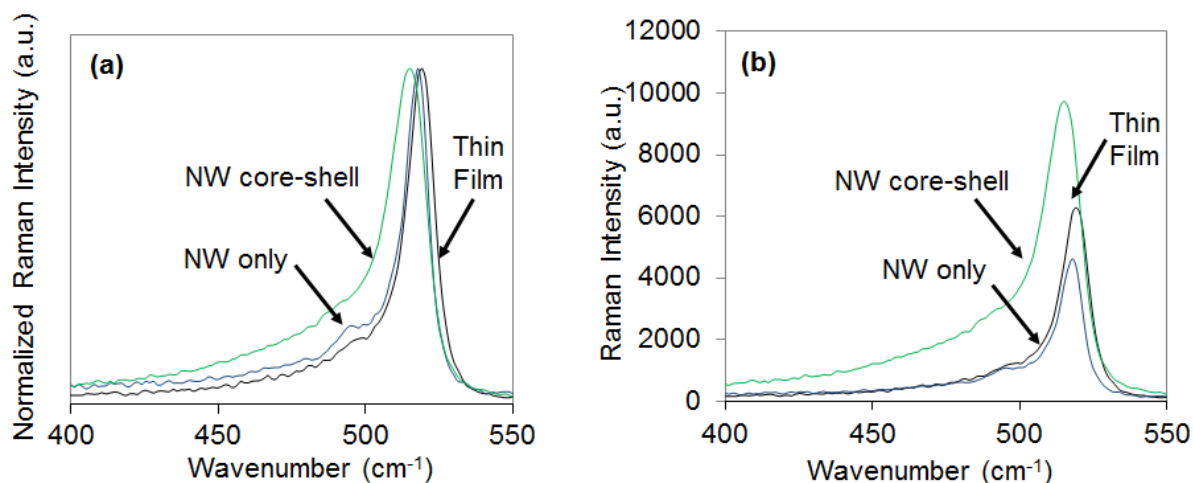
Figure 4-11: Normalized Raman spectra (a) and relative Raman intensity spectra (b) of an array of silicon nanowires, silicon core-shell nanowires and a planar nc-Si thin film (thickness=1 μm). The excitation wavelength was 488 nm [Adachi et al 2012a].

The silicon nanowires were grown under high H_2 dilution ($[H_2]/[SiH_4]$=62) conditions to suppress uncatalyzed amorphous Si growth. The normalized Raman spectrum of the silicon nanowire array without shell is shown in Figure 4-11(a). A strong crystalline peak at about 517 cm^{-1} can be observed, whereas the amorphous silicon peak at 480 cm^{-1} is suppressed. Similarly, the core-shell nanowires exhibit a strong crystalline peak at 515 cm^{-1}, with a slightly larger amorphous silicon contribution at 480cm^{-1}. Compared to a reference bulk Si crystalline peak of 520 cm^{-1}, the nanowire array exhibited a Stokes shift of 3 cm^{-1}, and the core-shell nanowire array had a Stokes shift of 5 cm^{-1}. This shift can be attributed to local heating in silicon nanowires caused by the excitation laser and due to the nanowires having lower thermal conductivity than that of bulk Si [Piscanec et al. 2003]. It

is worth mentioning that the relative Raman peak intensity of the core-shell sample was 56% higher than that of the thin film nc-Si sample, shown in Figure 4-11(b). The Raman intensity of the nanowire sample without shell was slightly lower than that of the thin film nc-Si because the sheer crystalline volume of the thin film was much greater than the volume of the nanowires.
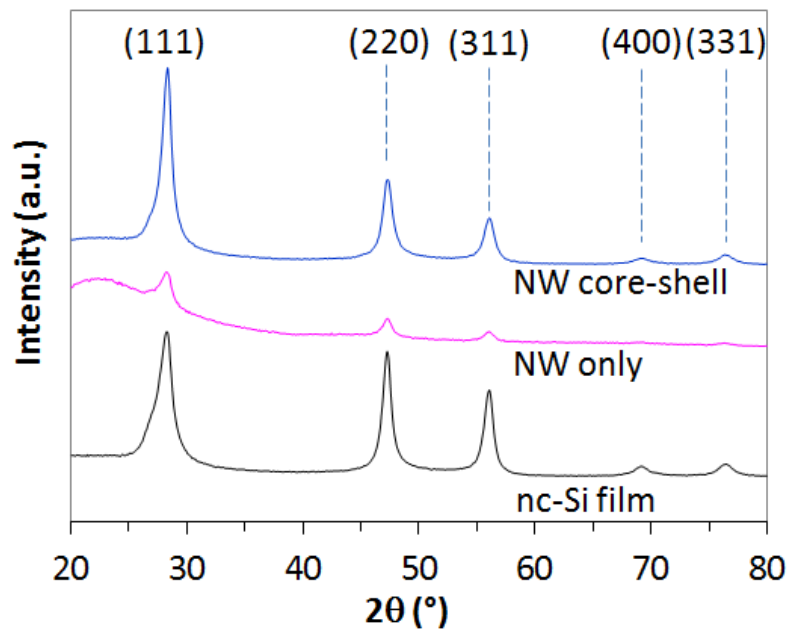
Figure 4-12: XRD intensity of core-shell silicon nanowires, bare nanowires and a planar nc-Si thin film. All samples are grown on glass substrate. The crystal orientations corresponding to XRD peaks are shown in brackets. [Adachi et al 2012a].

The X-ray diffraction spectra of the core-shell nanowire array, bare nanowire array and nanocrystalline silicon film are shown in Figure 4-12. The crystalline peaks correspond to the (111), (220), (311), (400) and (331) planes. The XRD intensity is lowest for the bare silicon nanowire array due to low material volume, which agrees with the Raman spectra in Figure 4-11. The core-shell nanowire array and nanocrystalline silicon film showed strong XRD peaks. However, they differed in that the core-shell nanowire array had a very large (111) plane peak, considerably larger than did any other plane. This difference was also the case for the bare silicon nanowire array. In contrast, in the nanocrystalline silicon film spectrum, the (111) peak had about the same intensity as that of the (220) plane.
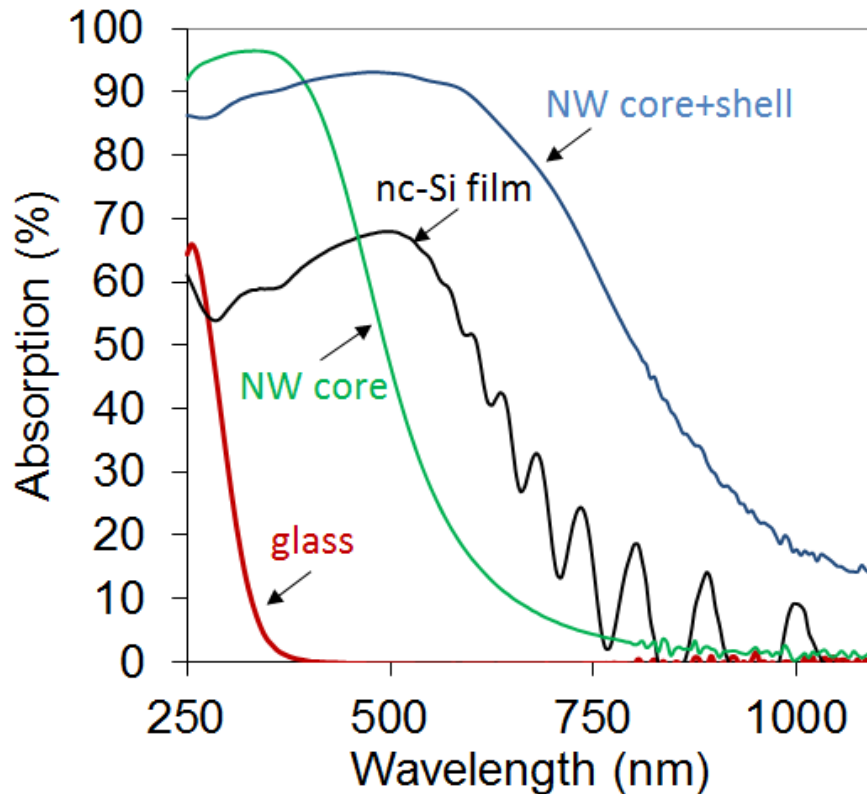
Figure 4-13: Absorption (1-T-R) of an array of nanowires (without shell), an array of core-shell epitaxial silicon nanowires, a planar nc-Si film and a glass substrate. The average nanowire length is about 800 nm. The average nanowire diameter is 30 nm without shell and 350nm with shell. The thin film nc-Si thickness is 1 μm [Adachi et al 2012a].

The optical absorption, defined as 1-T-R, of the nanowire array, the core-shell nanowire array and a thin film of nc-Si (1 μm) on a glass substrate, is shown in Figure 4-13. The oscillations of the thin film absorption are due to constructive and destructive interference between incident waves and internally reflected waves within the film. The silicon nanowire array sample exhibits very high absorption (>90%) at low wavelengths of between λ = 250 nm and 400 nm. However, the nanowires are highly transparent at longer wavelengths, resulting in low absorption of <5% at wavelengths greater than 750 nm. The nanowires with an epitaxial silicon shell show high absorption of 90% up to a wavelength of 600 nm. In comparison, the nc-Si thin film absorption peaked at 68% at about λ = 500 nm. The low absorption of the thin film can be attributed to high reflectance, as shown in Figure

4-14(a). In addition, the thin film simply did not efficiently absorb at λ> 500 nm, as shown by the high transmission at such long wavelengths in Figure 4-14(b). Therefore, disordered core-shell nanowires with an average length of just 800 nm show promise for enhancing broadband optical absorption.
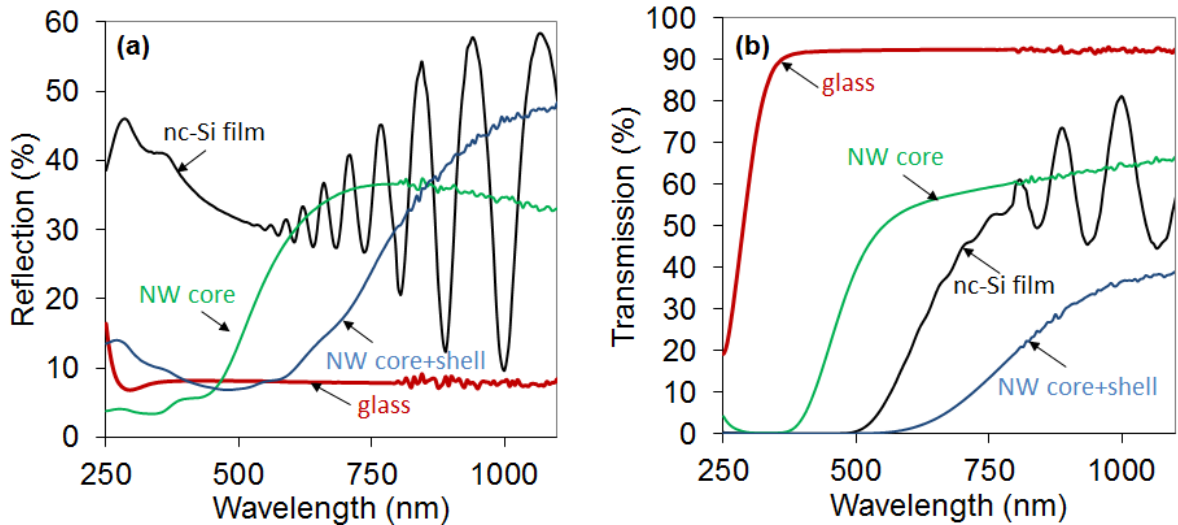
Figure 4-14: Total reflection (a) and total transmission (b) of an array of nanowires (core only), array of core-shell epitaxial silicon nanowires, a planar nc-Si film and glass substrate [Adachi et al 2012a].

In summary, disordered crystalline-amorphous core-shell silicon nanowires were grown by VLS method. TEM measurements of showed that the nanowire core was highly crystalline surrounded by an amorphous a-Si shell. The core-shell silicon nanowires exhibited strong enhancement in light absorption compared to that of a planar film over all wavelengths. Diluting the source gas with hydrogen was also found to suppress the growth of an uncatalyzed a-Si shell, which was verified by TEM measurements. The highly crystalline nanowire wall facilitated the growth of an epitaxial silicon shell, using the highly crystalline silicon nanowire as a seed crystal. The epitaxial silicon growth was verified by the selected-area diffraction pattern of the nanowire shell. Epitaxial silicon shell growth on a glass substrate is promising for large-area applications requiring an abrupt junction, and long-range atomic order.

Chapter 5

Nanowire-based solar cells

Silicon nanowires were incorporated into thin film n-i-p solar cells in two different configurations: 1) as a nanostructured back-reflector, and 2) in core-shell nanowire solar cells. The nanostructured back-reflector was fabricated by growing a thick layer of a-Si on top of an array of silicon nanowires resulting in an array of disordered dome-shaped nanostructures. The back-reflector was completed by depositing Ag/ZnO:Al on top of the nanostructures. The device architecture of core-shell silicon nanowire solar cells was modified twice because 1) impurities introduced during nanowire growth were found degrade collection efficiency, and 2) high aspect ratio back reflectors lead to high absorption losses. The final device architecture lead to core-shell nanowire devices exhibiting low broadband reflectance resulting and improved collection efficiencies at both short and long wavelengths as compared to a planar device. Core-shell nanowire solar cells consisting of both an a-Si and nc-Si shell are investigated.

5.1 Nanostructured back-reflector solar cells

Amorphous silicon solar cells are most commonly textured using V-shaped textured SnO_2:F. The morphology of SnO_2:F can be controlled by tuning the deposition conditions during atmospheric pressure chemical vapor deposition (APCVD) [Sato et al. 1992]. SnO_2:F coated glass is used as the starting on which a p-i-n amorphous silicon device is fabricated followed by the back reflector contact. In this configuration light enters the device through the transparent substrate. An alternative transparent conductive oxide (TCO) is U-shaped textured ZnO:Al which also enhances light trapping in a-Si solar cells [Kluth et al. 1999]. ZnO:Al is usually deposited by magnetron sputtering and the surface of the ZnO:Al can be textured by post-deposition wet etch in diluted HCl.

In the reverse configuration, the starting substrate is covered with a back reflector contact. An n-i-p amorphous silicon device is fabricated on top of the back reflector, followed by a thin transparent window contact deposition. In this configuration the substrate does not have to be transparent which allows for more flexibility in surface nanostructuring. For example, periodic

nanodomes fabricated by nanosphere lithography [Zhu et al. 2010] and periodic nano-patterns fabricated by imprint lithography [Ferry et al. 2010] have been shown to significantly enhance photocurrent in a-Si solar cells.

In this section, an array of disordered nanostructures is investigated for use as a back-reflector in amorphous silicon solar cells. The advantage of the disordered nanostructure is that they can be fabricated over large areas using conventional PECVD methods. In addition, this fabrication method offers a range of tailored nanostructure height and diameter. Nanostructures were fabricated using a bottom-up approach consisting of VLS-grown silicon nanowires coated by a thick layer of amorphous silicon. The density and height of the nanostructures were tailored by the nanowire length and the average base diameter of the nanostructures was tailored by the thickness of the thick amorphous silicon layer. The device structure was Ag (100nm)/ZnO:Al(100 nm)/n^+ nc-Si (50nm)/intrinsic a-Si (300nm)/p^+ nc-Si (30nm)/ZnO:Al (75nm). Ag gridlines were also deposited on top of the top contact to lower series resistance.
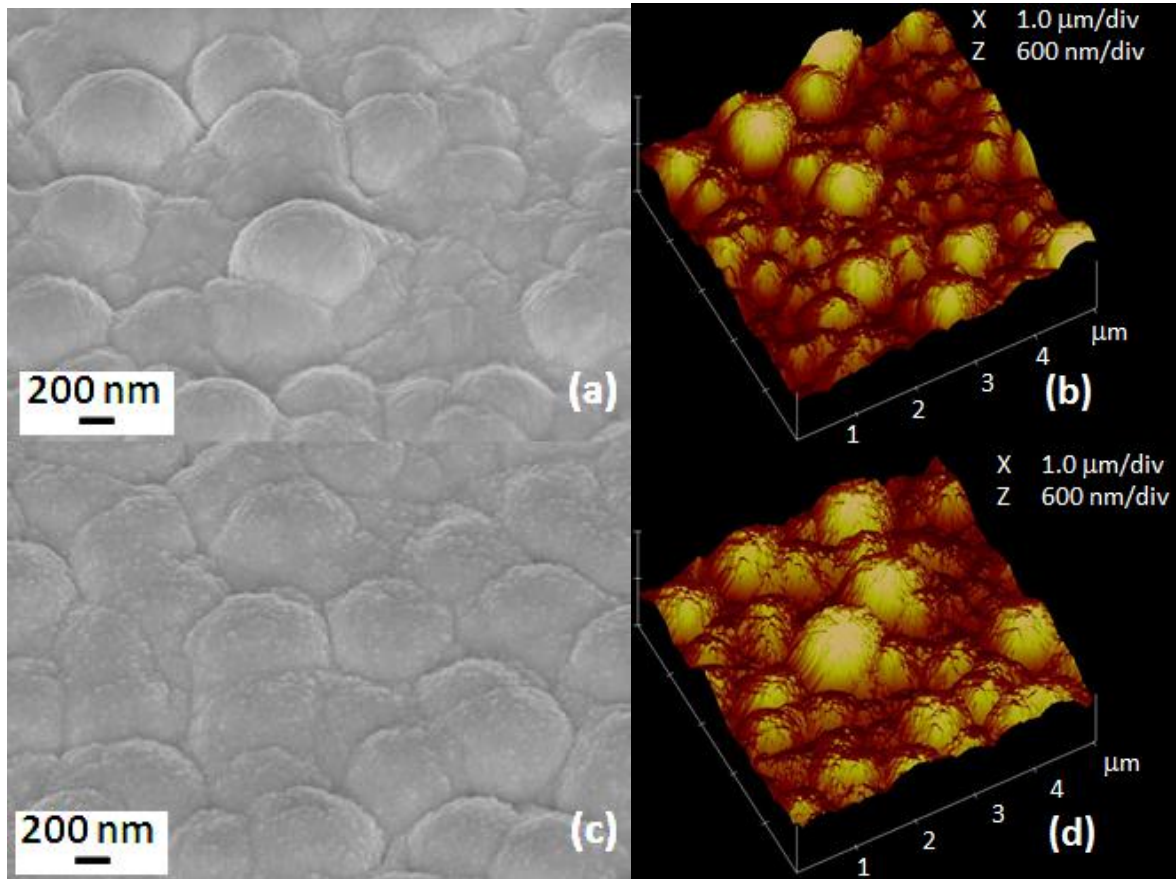
Figure 5-1: SEM image (45° tilt) (a) and AFM profile (b) of the nanostructured back reflector after Ag/ZnO deposition and the SEM image (c) and AFM profile (d) of the finished n-i-p-ZnO:Al device.

An SEM image and AFM profile of the nanostructured back reflector after Ag/ZnO:Al deposition is shown in Figure 5-1(a) and Figure 5-1(b), respectively. Similarly, Figure 5-1(c) and Figure 5-1(d) show the SEM image and AFM profile, respectively, of the finished n-i-p device. The average base diameter of the final nanostructured device was ~600 nm measured from the SEM image and the maximum peak-valley distance was 580 nm determined from the AFM profile.
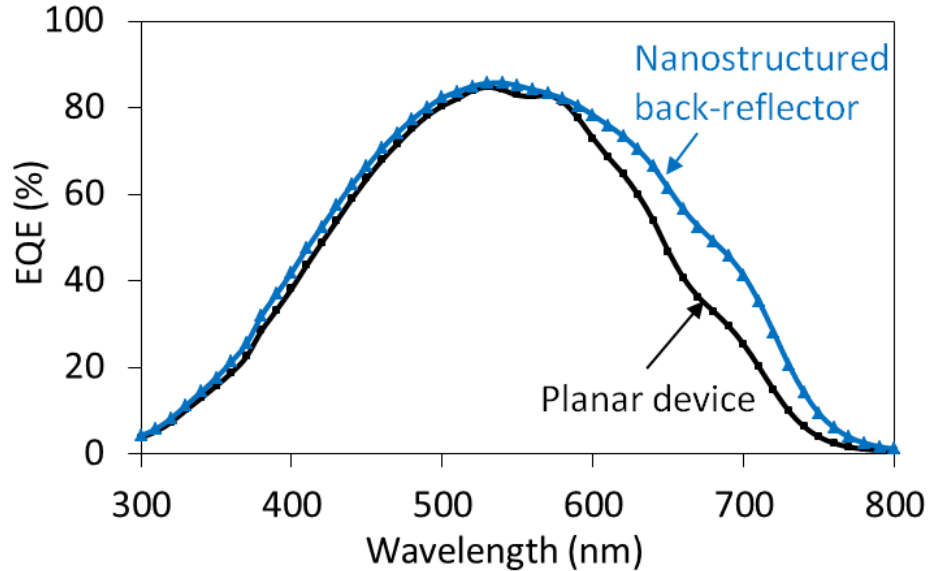
Figure 5-2: External quantum efficiency (EQE) spectra of n-i-p a-Si solar cells with nanostructured back-reflector and a planar back reflector. An Ag/ZnO:Al back-reflector was used in both devices. The deposition conditions for the n-i-p layers and top ZnO:Al contacts were the same in each case.

The external quantum efficiency spectra of n-i-p a-Si solar cells fabricated on a nanostructured back-reflector and on a planar back reflector are shown in Figure 5-2. The deposition conditions were the same for each device. The device on nanostructured back-reflector showed enhancement in EQE over the entire visible spectrum and most noticeably at wavelengths > 600nm. The nanostructured solar cell had an EQE value of 40.7% at λ=700nm, a 60% increase over that of the planar device.
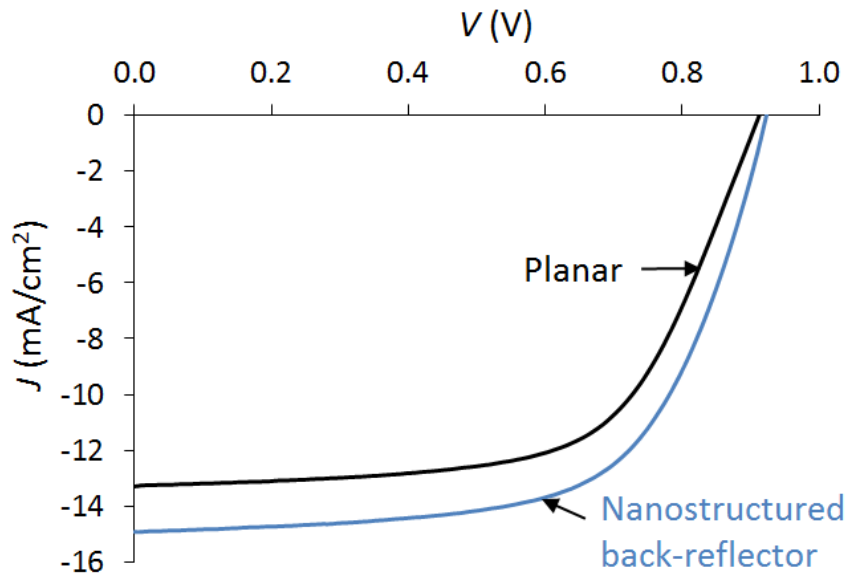
Figure 5-3: J-V curve of a-Si solar cell with nanostructured back-reflector and planar a-Si solar cell under AM 1.5 global illumination (100mW/cm^2).

The J-V curve under AM 1.5 global illumination (100 mW/cm^2) of the a-Si solar cell with nanostructured back-reflector and planar back reflector is shown in Figure 5-3. The nanostructured solar cell had a J_{sc}=14.8 mA/cm^2, V_{oc}=0.910V, FF=63.5% and conversion efficiency of η=8.87%. In comparison the planar device had a J_{sc}=13.1 mA/cm^2, V_{oc}=0.911V, FF=60.3% and conversion efficiency of η=7.47%. For the first time, a disordered nano-dome-shaped back-reflector has been fabricated by a large area amiable method and was shown to improve long wavelength collection efficiency in amorphous silicon solar cells. The nanostructuring technique used offers flexibility in tailoring the average height and base diameter of the nanostructures. Therefore, further enhancement in device performance is expected if these parameters are better optimized.

5.2 Core-shell nanowire solar cells

5.2.1 First attempt of nanowire solar cell incorporation
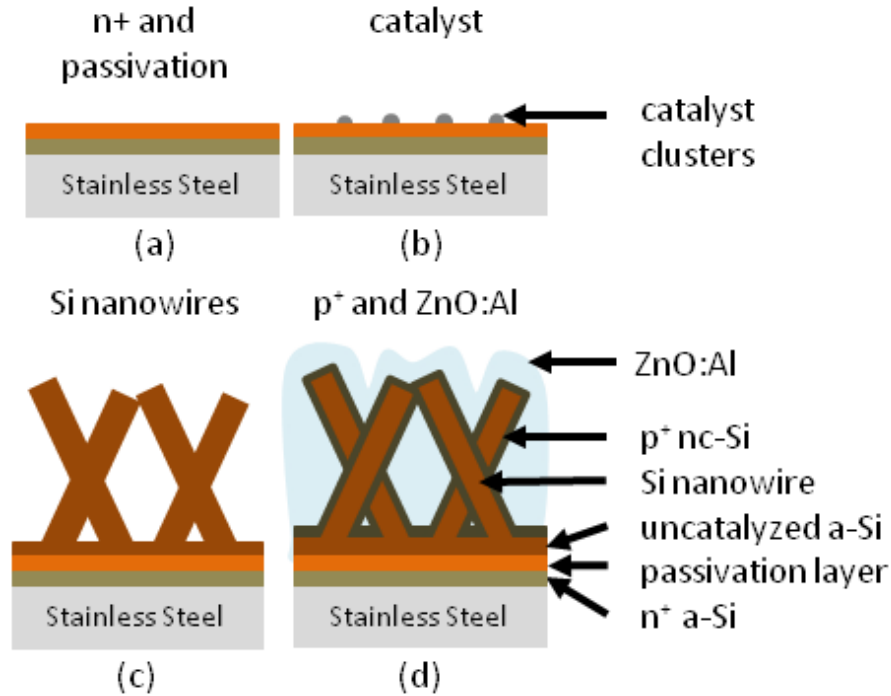
Figure 5-4: Illustration of the fabrication steps of the nanowire solar cell. The steps are: (a) an n+ a-Si thin film is deposited directly onto a stainless steel substrate followed by a thin intrinsic a-Si layer for passivation, (b) a thin catalyst film is evaporated followed by an anneal in vacuum to form nano-clusters, (c) undoped silicon nanowires are grown by VLS method, (d) a conformal p+ nc-Si film is deposited around the nanowires followed by a layer of ZnO:Al serving as the top contact.

The fabrication steps of the nanowire device are illustrated in Figure 5-4. First a 50 nm thick n^+ a-Si layer is deposited by PECVD using SiH_4 and PH_3 source gases. The substrate is a flexible 0.1 mm thick stainless steel substrate. A thin 30 nm thick intrinsic a-Si layer is deposited onto the n^+ layer which acts as a passivation layer before the substrate is transferred to another system for catalyst evaporation. The passivation layer was found necessary because n-i-p thin film a-Si devices which were removed from vacuum without it exhibited s-shaped IV-curves due to oxidation of the n^+ layer.

After the passivation layer deposition, the substrate was removed from vacuum and transferred to an e-beam evaporation system where 2nm of Sn catalyst was deposited. The thickness of Sn was measured using a quartz crystal thickness monitor. Afterward, the substrate was transferred back into the PECVD system and annealed in vacuum at a substrate temperature of 375° C to form catalyst nano-clusters. Undoped silicon nanowires were grown by PECVD using silane (SiH_4) source gas at a growth temperature of 375° C, deposition pressure of 1400 mTorr and plasma power density of 0.16 W/cm^2. A conformal p^+ nanocrystalline silicon (nc-Si) film was deposited by PECVD. Aluminum doped ZnO (ZnO:Al) served as the top contact, deposited by magnetron sputtering. The sheet resistance of the ZnO:Al film was measured to be 140 Ω/sq.

A thin film a-Si solar cell consisting only of thin films without nanowires was also fabricated for comparison. The thin film device consisted of the following structure: stainless steel/n+ a-Si (50 nm)/passivation a-Si layer (30nm)/intrinsic a-Si (400nm)/p+ nc-Si (40nm)/ZnO:Al (150nm). Note that the ZnO:Al layer for the nanowire solar cell was deposited for a longer time (30 min.) than the thin film device (9 min.) because the higher surface area of the nanowires increased series resistance. No back reflector or surface texturing was used in this study.

5.2.1.1 Structural Properties
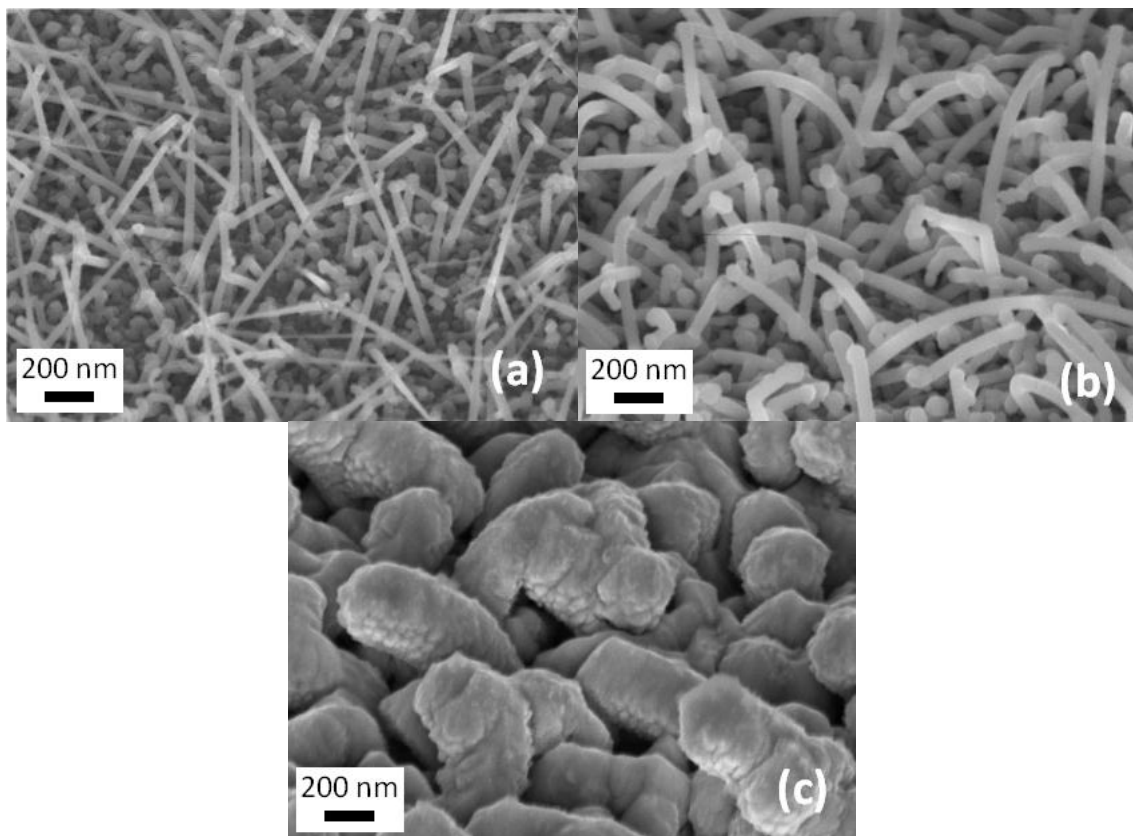
Figure 5-5: SEM micrographs of (a) silicon nanowires grown before p$^+$ deposition (b) nanowires after p$^+$ deposition, and (c) nanowires after p$^+$ and ZnO:Al deposition [Adachi and Karim 2010].

SEM micrographs of the silicon nanowires grown before p$^+$ layer deposition, after p$^+$ layer deposition and after ZnO:Al deposition, are shown in Figure 5-5. All nanowires were grown on n$^+$ a-Si and passivation layer coated stainless steel. The silicon nanowires grow straight in a range of angles away from the substrate and have lengths of up to 1200 nm and an average diameter of 40 nm as shown in Figure 5-5 (a). After p$^+$ deposition, the nanowires tend bend, as shown in Figure 5-5 (b), indicating the p$^+$ layer introduced strain in the nanowires. The total average diameter after p$^+$ deposition is 63 nm, corresponding to a p$^+$ shell thickness of about 11 nm. Note that this thickness is much less than the typical thickness of 20-30 nm for p$^+$ nc-Si layers used in thin film solar cells. The SEM

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micrograph of the device shown after ZnO:Al deposition is shown in Figure 5-5 (c). The ZnO:Al thickness along the wall of the nanowires is approximately 144 nm.

5.2.1.2 Optical Properties
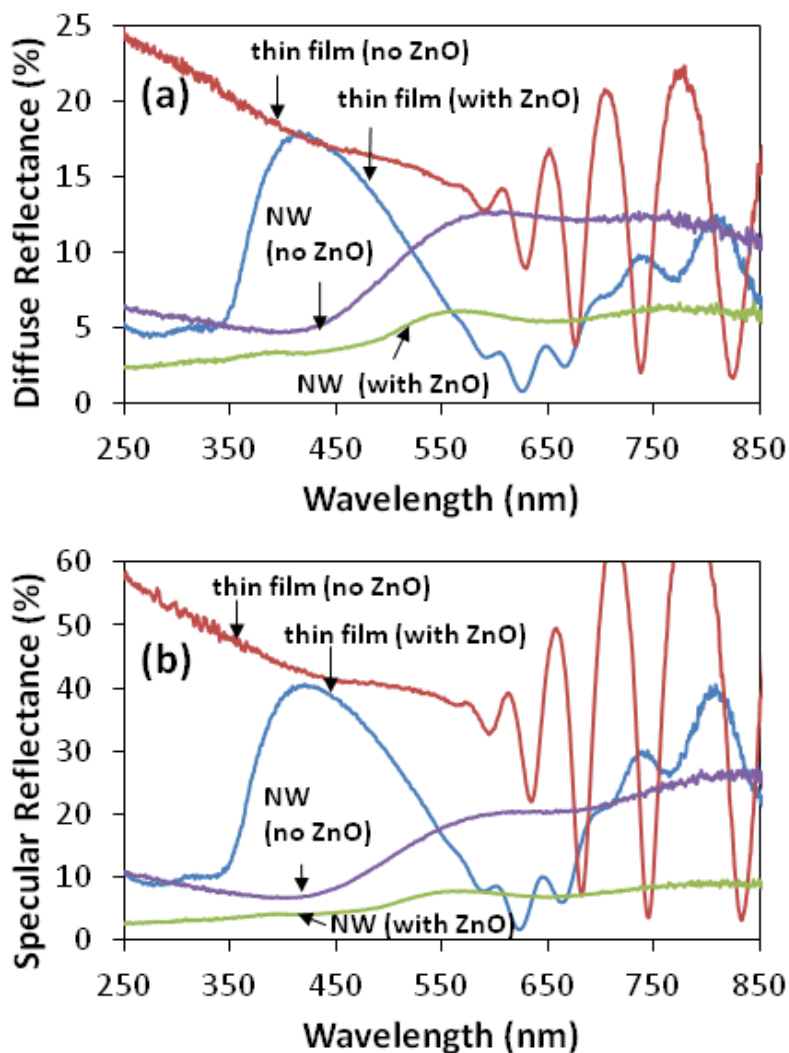
Figure 5-6: The (a) diffuse and (b) specular reflectance of silicon nanowire (NW) solar cells before and after ZnO:Al deposition. The reflectance for the thin film amorphous silicon reference solar cell is shown for comparison [Adachi and Karim 2010].

Table 5-1: Summary of the average diffuse and specular reflectance over the wavelength range
λ = 350 - 750 nm for the nanowire solar cell and a-Si thin film solar cell.

	Average Reflectance (350 nm - 750 nm)	Nanowire device	a-Si thin film device
Without ZnO:Al	Diffuse	9.6 %	15.0 %
	Specular	15.3 %	39.1 %
With ZnO:Al	Diffuse	4.9 %	9.4 %
	Specular	6.3 %	22.6 %

The diffuse and specular reflectance of the silicon nanowire array device and reference thin film a-Si device are shown in Figure 5-6. A summary of the average diffuse and specular reflectance is also given in Table 5-1. In Figure 5-6(a) the nanowire device after ZnO:Al deposition is shown to have very low diffuse reflectance as compared to the thin film device particularly in the wavelength range of 250 nm - 450 nm. Similarly, in Figure 5-6(b) the specular reflectance of the nanowire device after ZnO:Al deposition is shown to be much lower than the thin film a-Si device. Taking the average over the typical active absorption range of a-Si solar cells (λ = 350 nm – 750 nm) the nanowire device after ZnO:Al deposition has an average specular reflectance of 6.3% as compared to 22.6% for the thin film a-Si device. Similarly the average diffuse reflectance of the nanowire devices is 4.9% as compared to 9.4% for the thin film a-Si device. The reflectance of the nanowire device and thin film device before ZnO:Al deposition is also shown in Figure 5-6 for reference. Note that the ZnO:Al layer acts as an anti-reflective coating for both devices and depends on the thickness of the film. The reflectance can be lowered further for the nanowire device by optimizing the ZnO:Al thickness.

5.2.1.3 Effect of catalyst on external quantum efficiency
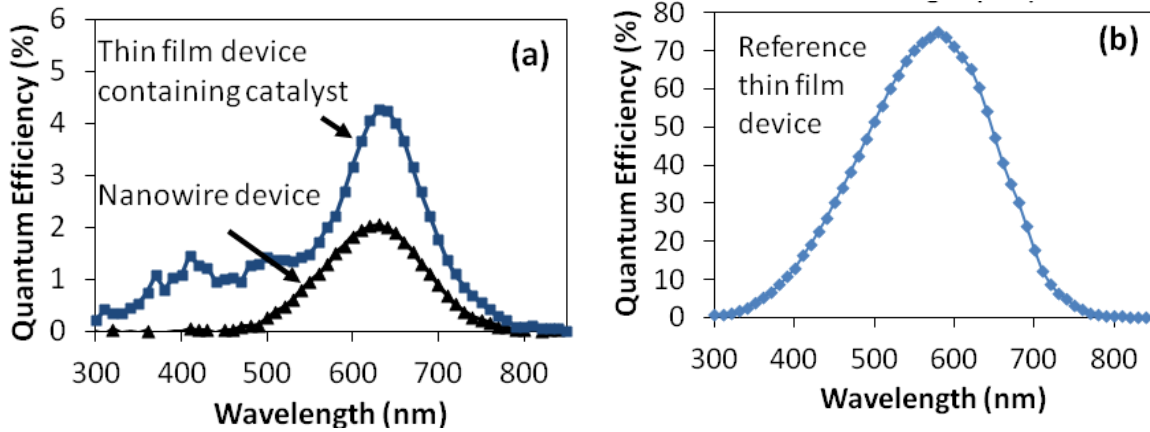
Figure 5-7: The external quantum efficiency (EQE) of (a) the silicon nanowire device and (b) a reference thin film a-Si device. A thin film a-Si device with catalyst incorporated within the intrinsic layer was fabricated to investigate the effect of the catalyst on EQE. This measurement is shown in (a) [Adachi and Karim 2010].

The measured external quantum efficiency (EQE) of the silicon nanowire device is shown in Figure 5-7 (a). The EQE peaks at 2 % at $\lambda = 630$ nm which is considerably lower than EQE of the thin film a-Si device fabricated in the same deposition system, shown in Figure 5-7 (b). The thin film a-Si device consisted of the same stainless steel substrate and n^+ and passivation layers as the nanowire device but the nanowires were replaced with a 400 nm thick intrinsic a-Si layer. No catalyst was deposited before the 400 nm thick intrinsic layer.

To determine the cause of the low EQE of the nanowire device, another thin film a-Si solar cell was fabricated using the same fabrication procedure but this time including a thin 2 nm thick Sn catalyst film deposited between the passivation layer and 400 nm thick intrinsic layer. The EQE of the resulting thin film device containing catalyst is also shown in Figure 5-7 (a). The EQE spectrum of this device is comparable to the EQE spectrum of the nanowire device, peaking at about 4.3% at λ=630 nm. Adding the thin layer of Sn catalyst within the n-i-p device significantly degrades the collection efficiency over the entire wavelength spectrum. Such impurities create traps within the electronic band-gap, degrading the lifetime of photo-generated carriers and lowering collection efficiency. These results indicate that the largest contributor to EQE losses is the presence of the

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catalyst impurities within the intrinsic layer. Another reason for the low EQE of the nanowire device is that the top ZnO:Al contact that was too thick leading to high reflectance and absorption losses. In addition, the radial p^+ layer thickness was calculated to be 11 nm from Figure 5-5 which is much thinner than a typical nc-Si p+ layer thickness of 20-30 nm in a-Si solar cells. Therefore, a thicker p^+ layer is needed for improving charge collection particularly. Both of these considerations are critical for improving device performance and will be addressed in the following sections.

5.2.2 Absorption losses in high aspect ratio aluminum

A number of attempts have been made to circumvent the effect of catalyst impurities on device performance such as chemical removal of catalyst impurities after nanowire growth [Stelzner et al. 2008] and surface passivation by an Al_2O_3 film [Gunawan et al. 2009]. However, the final device performance in both cases remained low. Another method to eliminate impurities from entering active n-i-p layers is to simply fabricate the n-i-p device above the nanowires rather than incorporating the nanowires into the active layers. In other words, the nanowires are used only to provide the high aspect ratio core to enhance the absorption in the active shell layers. The first attempt of this modified structure involved depositing Al onto nanowires to create an Al coated nanowire back-reflector.
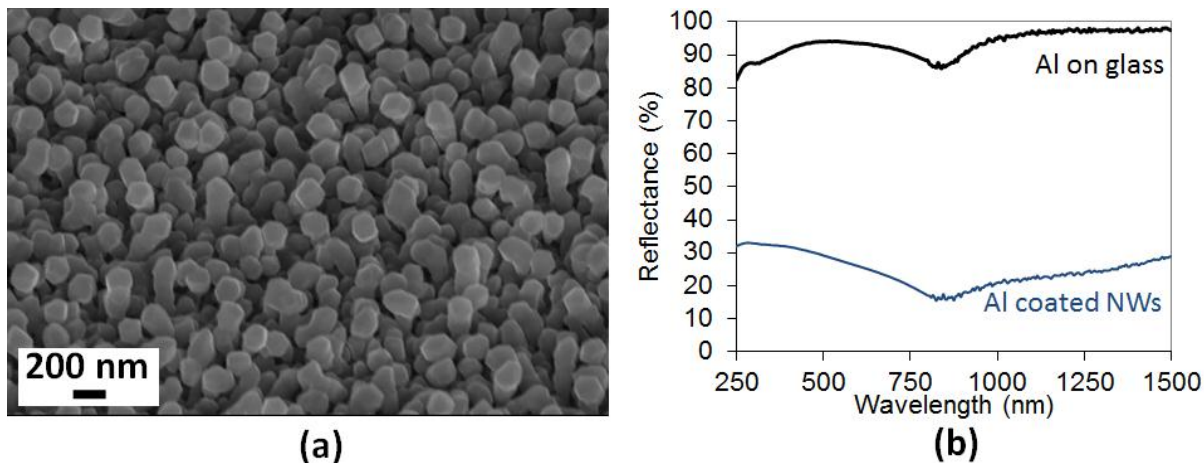
Figure 5-8: SEM (45 tilt) image of an array of Al coated silicon nanowires (left) and the total reflectance of a planar Al film on glass and Al coated silicon nanowires (right).

Figure 5-8(a) shows an SEM image of an array of short nanowires with an average length of 360 nm, coated with a thin Al film. The aim of the back reflector is to reflect light back into the device located above it to increase the path length that light travels within the device. However, the high aspect of the Al coated nanowires was found to cause strongly absorption of light. The total reflectance of a planar Al film (thickness 120 nm) on glass is compared with that of the Al coated nanowires in Figure 5-8 (b). The Al deposition time was the same for both samples. The planar Al exhibited an average reflectance of 93% over the visible spectrum (λ=400-700nm) and dipped to about 87% at 850 nm. In comparison, the total reflectance of the Al coated nanowires is just 27.5% over the visible spectrum. Visibly, the Al coated nanowire sample had a non-reflective medium gray color. Total transmission through both samples was nearly zero (≤ 2 %) over the same wavelength range. Therefore, the low reflectance of the Al coated nanowires was due to absorption in the Al coated nanowires. As a result, the Al coated nanowires are not suitable as a back contact due to high broadband absorption losses which would prevent multiple scattering within the device structure.

5.2.3 Amorphous silicon shell nanowire solar cells
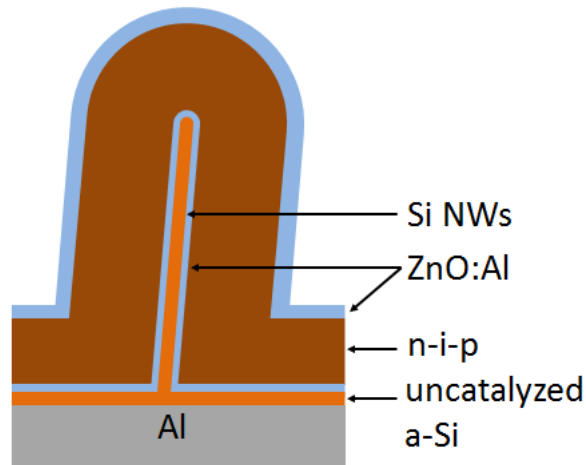
Figure 5-9: Cross-section illustration of the nanowire-a-Si core-shell device structure.

Taking into account the high absorption of Al coated silicon nanowires, the device structure was modified such that the Al film was made planar, deposited directly on glass. An illustration of the

new core-shell solar cell is shown in Figure 5-9. Silicon nanowires were grown directly on the Al back contact. A thin layer of ZnO:Al was deposited on top of the nanowires to prevent counter-doping of the n^+ layer by the Al back contact. The n-i-p thin film silicon layers are deposited radially around the ZnO:Al coated silicon nanowires. The nanowire itself is electrically inactive but facilities the high aspect ratio for enhancing absorption within the n-i-p regions [Adachi et al 2012b].
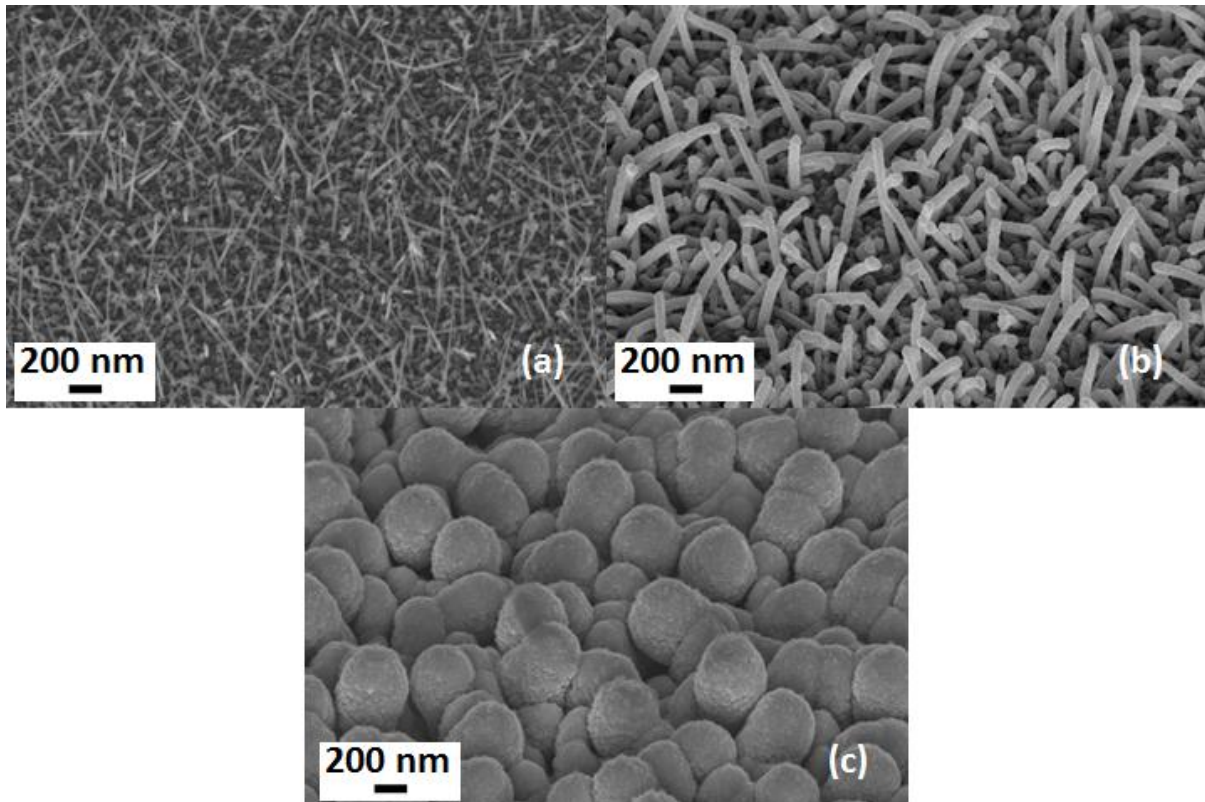
Figure 5-10: SEM (45 tilt) images of silicon nanowires grown on the Al back contact (a), ZnO coated nanowires (b), and the final n-i-p-ZnO:Al core-shell nanowires [Adachi et al 2012b].

An SEM image of the highly dense array of silicon nanowires only is shown in Figure 5-10(a). The average length of the nanowires is about 525nm and the average diameter is about 20 nm. An SEM image of ZnO:Al coated nanowires is shown in Figure 5-10 (b). The average diameter of the ZnO:Al coated nanowires was 55nm. The n-i-p semiconductor layers were then deposited by PECVD resulting in radial growth around the nanowires. The average radial thickness of the amorphous silicon absorption layer was ~152 nm, resulting in a total average diameter including the n^+ and p^+

layers of 360 nm. The final fabricated device after the top contact ZnO:Al deposition is shown in Figure 5-10 (c).
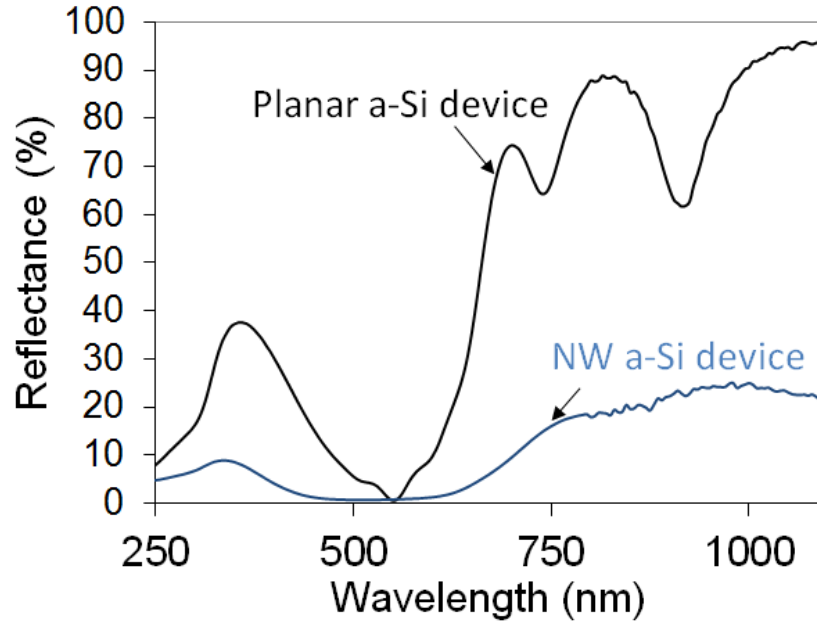
Figure 5-11: Total reflectance of a core-shell NW a-Si solar cell and a planar a-Si solar cell [Adachi et al 2012b].

The total reflectance of a core-shell nanowire a-Si solar cell and a planar a-Si solar cell is shown in Figure 5-11. The total reflectance accounts for both specular and diffuse reflectance. The top ZnO:Al contact of the planar solar cells acts as an antireflective coating. The ideal thickness of this top contact is ~80 nm, which is based on the quarter-wavelength minimum reflectance condition of $dn = \lambda/4$, where d is the thickness of the film and n is the index of refraction of the antireflective coating [Born and Wolf 2000]. The thickness of the ZnO:Al contact was ~75nm and the total reflectance reached as low as 0.5% at λ=550nm. However, at the reflectance is as high as 37% at a short wavelength of λ=360 nm and >60% at longer wavelengths (λ>670 nm). In comparison, the core-shell NW device showed a strong decrease in reflectance. The total reflectance was <3% in the wavelength interval of 410 nm $< \lambda <$ 640nm and exceeded 10% only for λ>700 nm.

Disordered silicon nanowires have been previously shown to have low broadband specular reflectance [Muskens et al. 2008, Tsakalakos et al. 2007]. However, diffuse reflectance of disordered

silicon nanowires has been known to be high at high energies due to strong scattering in the silicon nanowires [Muskens et al. 2008]. Figure 5-11 shows that low diffuse reflectance can in fact be achieved in disordered silicon nanowires coated with a suitably thick TCO (i.e., ZnO:Al). In this case the ZnO:Al layer was ~75 nm on the top of the nanowires and ~ 48 nm along the sidewalls. Therefore, collection efficiency losses due to total reflection can be minimized using disordered nanowire structures.
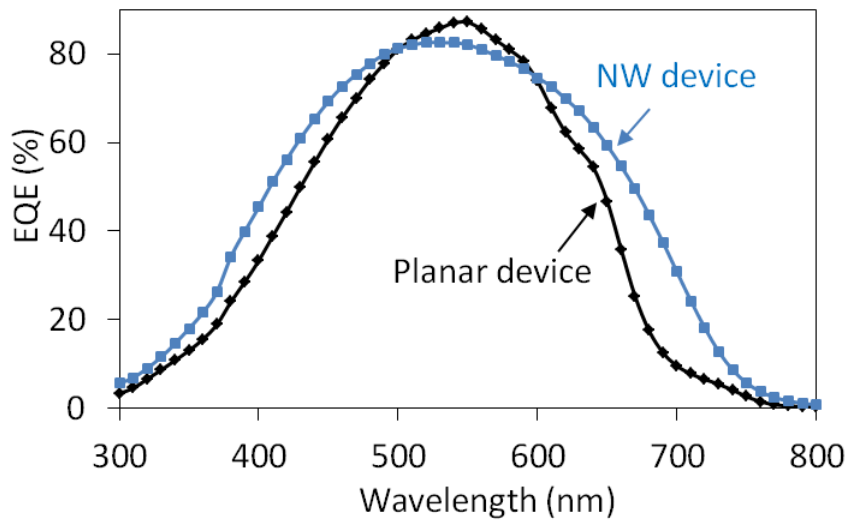
Figure 5-12: External quantum efficiency of a core-shell nanowire solar cell and a planar a-Si solar cell [Adachi et al 2012b]

The external quantum efficiency of a the core-shell nanowire solar cell as compared to that of a planar a-Si solar cell is shown in Figure 5-12. The nanowire device exhibits enhancement in quantum efficiency at low wavelengths, $\lambda < 500$nm and high wavelengths, $\lambda > 600$nm. The external quantum efficiency enhancement can be attributed to multiple scattering within the nanowire structure. The EQE enhancement ratio between the nanowire device and planar device is as high as 3.2 at $\lambda = 700$nm. As a result, the short circuit current determined from the EQE spectrum of the nanowire device was 14.1 mA/cm^2, whereas the J_{sc} of the planar device was 12.3 mA/cm^2. The EQE of the planar device is higher within the wavelength region between 500 nm to 600 nm possibly due to non-conformal deposition of the n$^+$ layer. The n$^+$ deposition conditions were not optimized for

conformal deposition. Non-uniform radial thickness would result in regions between the n$^+$ and p$^+$ layers with insufficient built in electric field for efficient charge collection.
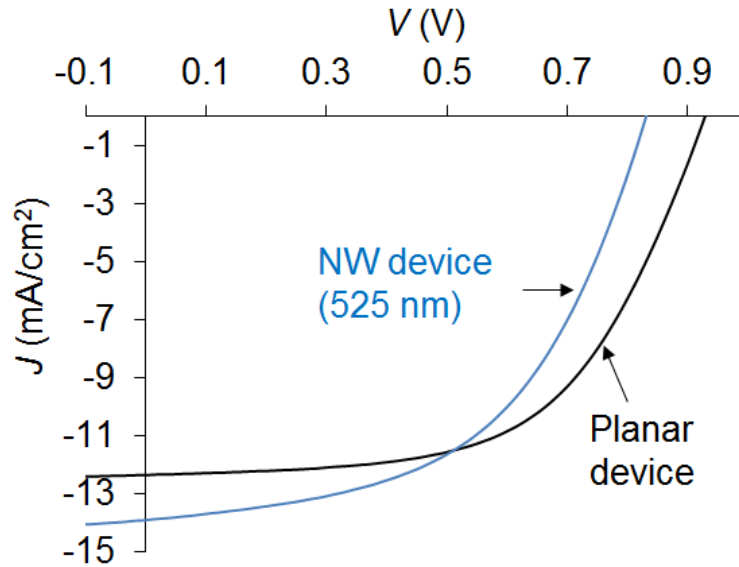
Figure 5-13: J-V curve of a planar a-Si solar cell and a core-shell nanowire solar cell under AM 1.5 global illumination (100mW/cm^2) [Adachi et al 2012b].

The J-V measurements under AM 1.5 global illumination of the nanowire device is shown in Figure 5-13 resulting in J_{sc} =13.9 mA/cm^2, V_{oc}= 0.832V, FF = 54.2%, and conversion efficiency of η=6.4%. In comparison the planar device had a J_{sc} =12.1 mA/cm^2, V_{oc}=0.928V, FF = 57.9%, and conversion efficiency of η = 6.6%. The lower V_{oc} of the nanowire device can be attributed to the larger junction area of the silicon nanowire device [Kayes et al. 2005].

5.2.4 Nanocrystalline Silicon shell nanowire solar cells
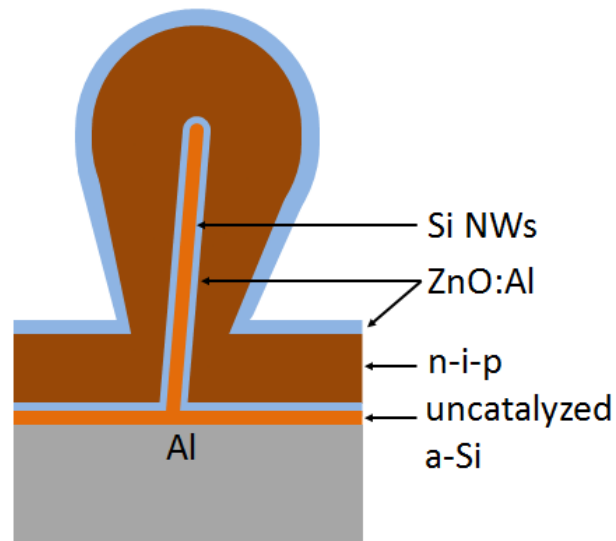
Figure 5-14: Cross-section illustration of a crystalline-nanocrystalline core-shell silicon nanowire solar cell.

As discussed in Section 5.2, an array of crystalline-nanocrystalline core-shell silicon nanowires showed higher broadband absorption than a planar film of nc-Si. A nanowire core-nanocrystalline Si shell solar cell was also investigated to take advantage of these optical properties. An illustration of the nanowire core-shell device is shown in Figure 5-14. The structure is the same as that of the nanowire-a-Si core shell solar cell in Figure 5-9, except that the sidewalls are tapered such that the base diameter is smaller than the tip diameter [Adachi et al 2012b].
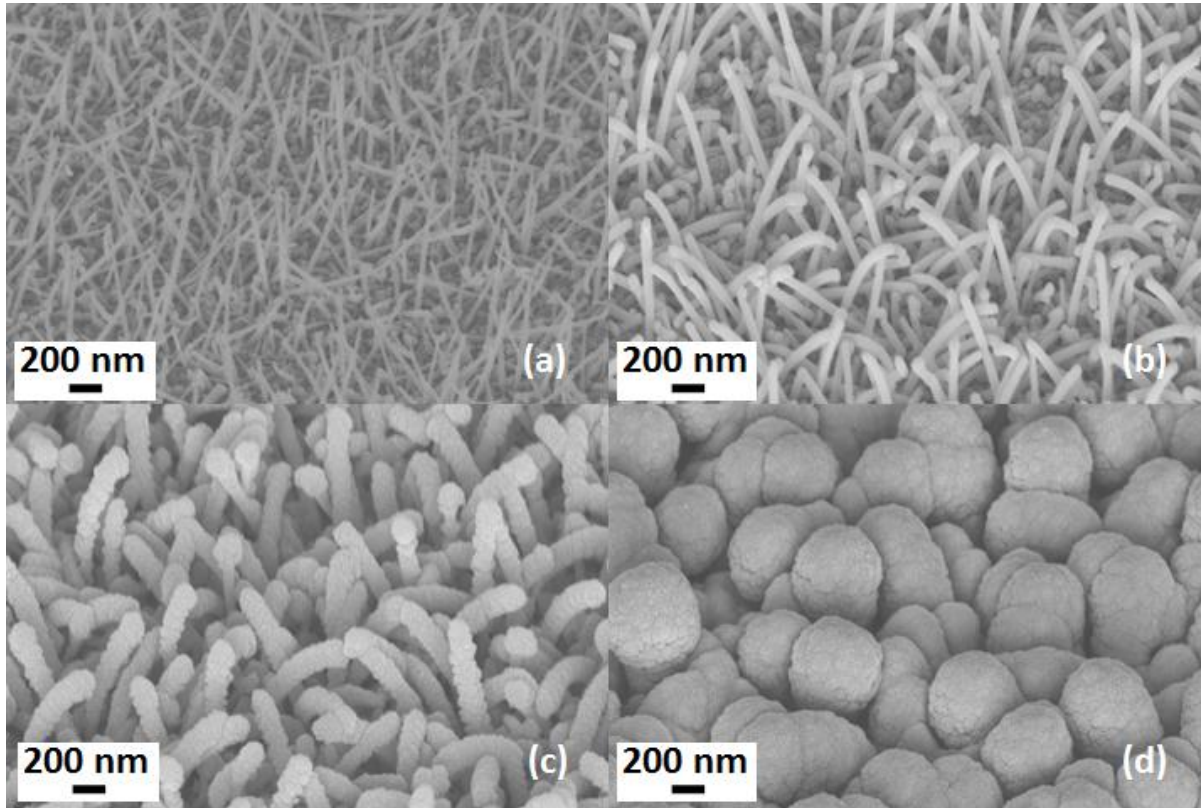
Figure 5-15: SEM (45° tilt) images of silicon nanowires only (a), nanowires coated by ZnO:Al (b), nanowires coated with ZnO:Al/n+ nc-Si (c) and the finished solar cell (d) [Adachi et al 2012b].

An SEM image of a highly dense array of silicon nanowires grown on Al-coated glass is shown in Figure 5-15(a). The average length of the nanowires is 800 nm, and the average diameter is about 30 nm. The nanowires were covered with a thin layer of ZnO:Al to prevent counter-doping of the n^+ layer by the Al back contact. The ZnO:Al coated nanowires had an average total diameter of about 55 nm, and are shown in Figure 5-15 (b). Note that stress in the ZnO:Al film caused some nanowires to bend. The nanowire array after nc-Si n^+ layer deposition is shown in Figure 5-15 (c), and the final device after n-i-p-ZnO:Al deposition is shown in Figure 5-15 (d). The radial thickness of the n+ was approximately 40 nm. Again, the nc-Si absorbing layer was deposited under high-pressure (7 Torr) and high-power (0.37W/cm^2) conditions. As a result, the sidewalls of the shell were

tapered, with a top average diameter of about 530 nm and base diameter of approximately 135 nm after the top ZnO:Al deposition.
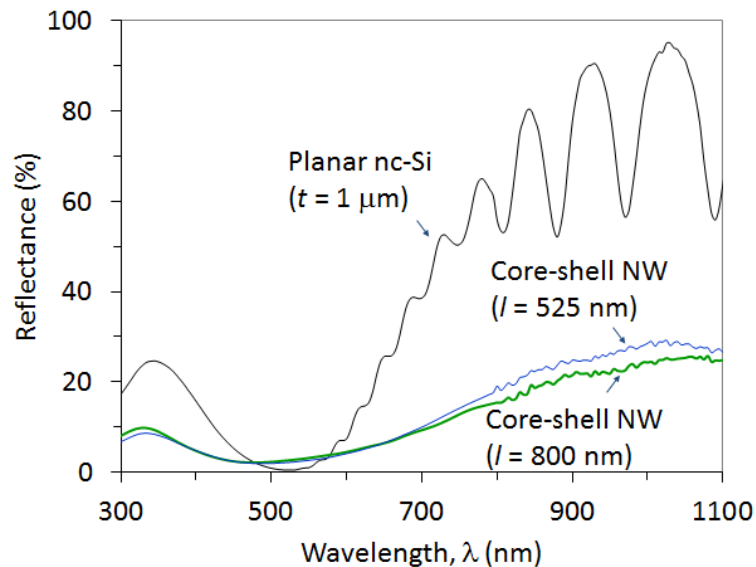
Figure 5-16: Total reflectance of core-shell nanowire solar cells with an average length of 525 nm and 800 nm and a planar nc-Si solar cell. The thickness of the intrinsic nc-Si layer of the planar device was 1 μm, resulting in a total thin film Si thickness of 1.08μm [Adachi et al 2012b].

The total reflectance spectra of core-shell nanowire solar cells with an average nanowire length of 525 nm and 800 nm and that of a planar nc-Si solar cell are shown in Figure 5-16. The total reflectance of both nanowire devices is very similar, with values ≤ 10% over the wavelength range λ = 250 nm to 700 nm.
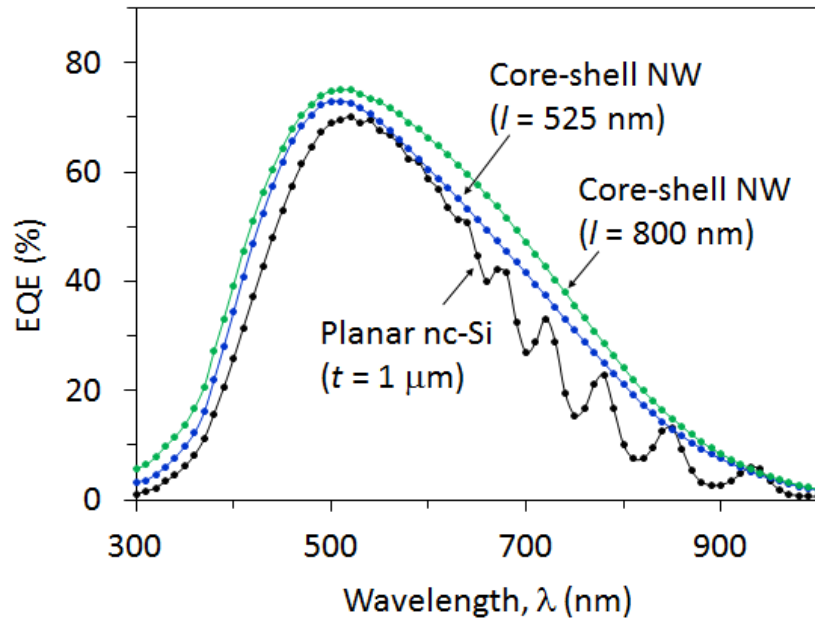
Figure 5-17: External quantum efficiency spectra of core-shell nanowire solar cells with different lengths and a planar solar cell [Adachi et al 2012b].

The external quantum efficiency spectra of core-shell solar cells with an average length of 525 nm and 800 nm are shown in Figure 5-17. The nc-Si shell deposition time was the same in both nanowire solar cells. The EQE of a planar solar cell consisting of a 1 μm thick nc-Si i-layer is also shown for comparison. The core-shell nanowire devices exhibit higher EQE over all wavelengths, which can be attributed to enhanced absorption within the nc-Si shell. As a result, the $J_{sc} = 14.9$ mA/cm^2 for the nanowire device with an average length of 525 nm and $J_{sc} = 16.6$ mA/cm^2 for the nanowire device with an average length of 800 nm. In comparison, the planar nc-Si device had a J_{sc} of 13.2 mA/cm^2.
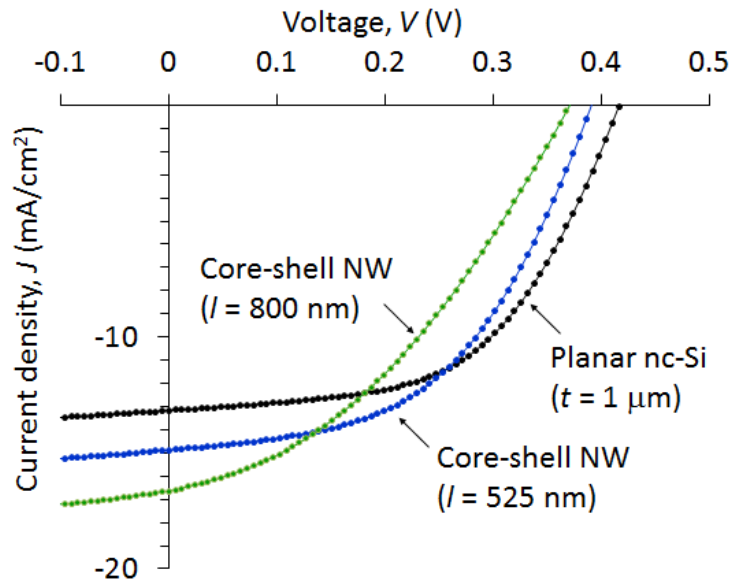
Figure 5-18: J-V curves of nanowire solar cells with nc-Si shells with nanowire lengths of 525 nm and 800 nm, and that of a planar nc-Si solar cell under AM 1.5 global illumination (100mW/cm^2) [Adachi et al 2012b].

The J-V curves of core-shell nanowire solar cells with lengths of 525 nm and 800 nm under AM 1.5 global illumination are shown in Figure 5-18. The J-V curve of the planar nc-Si solar cell is shown for reference. The core-shell solar cell with a length of 525 nm again exhibited a lower V_{oc} of 0.39V than did the planar device, which had a V_{oc} of 0.42V. The decrease in V_{oc} can again be attributed to a higher junction area. The nanowire ($l = 525$ nm) solar cell also had an FF=50.3% and J_{sc}=14.6mA/cm^2, resulting in a conversion efficiency of η=2.87%. The longer nanowires (l=700nm) showed a high J_{sc} of 16.2mA/cm^2, but the FF decreased to 38.0% and the Voc dropped to 0.37V, resulting in a conversion efficiency of η=2.26%. The planar device had an FF =60.0% and conversion efficiency of η=3.28%. The drop in device performance in both nanowire devices can be attributed to difficulty in conformal n$^+$ layer coverage of the high aspect ratio silicon nanowires. In fact, Figure 5-19 shows the SEM image of the silicon nanowire array after n$^+$ deposition. Some nanowires have thinner n$^+$ coverage at their base due to the non-conformal deposition conditions of the n$^+$ layer (750mTorr, substrate temperature of 200°C). Other possible reasons include film stress in the n$^+$ layer, as observed by bending of nanowires after n$^+$ deposition, or poor adhesion to the

ZnO:Al shell. Some methods for improving conformal deposition include decreasing the deposition pressure or increasing the substrate temperature of the n$^+$ layer. An alternative is to optimize the distribution of the nanowire catalyst before nanowire growth, thereby increasing spacing between nanowires.
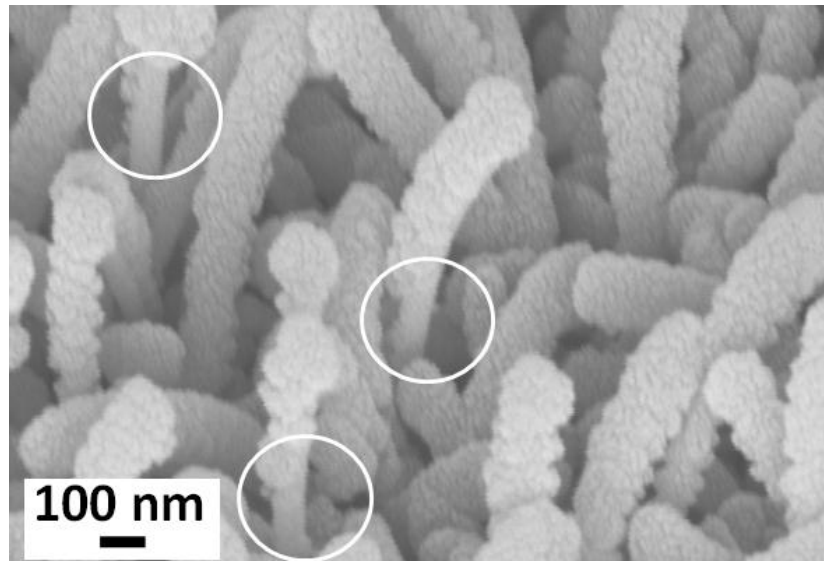
Figure 5-19: SEM (45° tilt) of the silicon nanowire array (l~800nm) after n$^+$ layer deposition [Adachi et al 2012b].

In summary, several device architectures were considered when incorporating silicon nanowires into n-i-p devices. Catalyst impurities were identified as a strong contributor to device performance degradation when the nanowires were grown on top of the n-type region. Aluminum coated nanowires were also found unsuitable as a backreflector due to high absorption losses. A core-shell device architecture was implemented in which the nanowire was separated from the active n-i-p region, and the Al back contact was deposited directly on glass to maintain high reflectance. Using this device architecture, an a-Si shell nanowire solar cell exhibited higher external quantum efficiency over most of the visible light spectrum than a planar device. Furthermore, an nc-Si shell nanowire solar cell improved external quantum efficiency over nearly all wavelengths while using considerably less material that the planar control device. A challenge associated with the core-shell nanowires is

low V_{oc} due to an increase in recombination at the p/i interface. One method that can be used lower recombination is to deposit a graded p-layer at the p/i interface. In addition, optimizing the deposition conditions for conformal growth for both the n-type and p-type shells could improve fill factor. Nonetheless, the core-shell nanowire solar cells exhibited very low total reflectance over most of the visible light spectrum and enhanced external quantum efficiency over most wavelengths compared to a planar device. Therefore, core-shell nanowire devices are an exciting variant to conventional texturing methods for improving the absorption of light in large area photovoltaic devices.

Chapter 6

Conclusions and Contributions

The optical properties of a heterostructure consisting of a crystalline silicon core and a conformal amorphous shell were investigated for the first time. For an array consisting of our smallest diameter nanowires (15 - 40 nm) the optical absorption is very high (95%) at short wavelengths ($\lambda < 550$ nm), and drops sharply to very low values (less than 2%) at long wavelengths ($\lambda > 780$ nm). Such silicon nanowires have potential applications in large area optical filters, selected area (defined by lithography) anti-scatter material or photodetectors with wavelength selectivity controlled by nanowire diameter. The largest diameter nanowires (150-180 nm) showed significantly higher long wavelength absorption (54% at 750 nm) than a planar a-Si film (~0% at 750nm).

In addition, growth of an epitaxial silicon shell around a highly crystalline silicon nanowire core was also demonstrated on a glass substrate. Such epitaxial shells can be used as building blocks for nanotechnology applications that require epitaxial silicon grown at low temperatures on large area substrates such as glass. An array of epitaxial silicon shell nanowires exhibited absorption $> 90\%$ up to a wavelength of 600 nm. The average length of the core-shell nanowire array was only 800 nm, but the array showed significantly higher absorption than a 1 μm planar nanocrystalline silicon film over all wavelengths between 250-1200nm.

Core-shell nanowire solar cells were first fabricated by incorporating nanowires into the n-i-p device. However, impurities introduced during the nanowire growth process degraded collection efficiency. As a result, the device structure was modified such that the nanowires were electrically inactive but provided the high aspect ratio structure for the purpose of enhancing absorption in the active shell regions. In the modified device architecture, the n-i-p layers were grown radially around the nanowire core.

For the first time, core-shell nanowires prepared with a bottom-up approach exhibited higher collection efficiency than a planar reference cell. VLS-method-grown silicon nanowires are promising because they are large-area amiable and can be prepared in conventional PECVD systems. Disordered nanowires have previously been reported to have high diffuse reflectance. However, core-shell nanowire devices consisting of an amorphous silicon intrinsic shell and coated with a thin layer of ZnO:Al, exhibited a very low total reflectance <3% over the wavelength range 410 nm $< \lambda <$

640nm. The total reflectance exceeded 10% only for $\lambda > 700$ nm where absorption in a-Si is weak. The EQE of these nanowire devices was higher than that of the planar device for both short wavelengths ($\lambda < 500$nm) and high wavelengths ($\lambda > 600$nm). As a result, the overall short-circuit current increased by 14%.

Core-shell nanowire devices consisting of a tapered nanocrystalline silicon shell showed higher EQE than did a planar n-i-p solar cell over all wavelengths. The resulting short circuit current of the core-shell silicon nanowire solar cell was up to 26% higher than that of the planar control device. It is worth mentioning that the deposition time of the absorption layer in the core-shell nanowire solar cell was half that of the planar device. Therefore, using the high aspect ratio of the nanowires, high carrier collection can be achieved using considerably less material, a critical factor in high throughput production. Non-conformal n+ layer deposition and high top contact resistance are remaining challenges that lower device performance. Furthermore, further room for improvement exists in optimizing the density of nanowires to increase absorption further. The core-shell nanowire structure shows promise in improving device performance in thin film solar cells. The material does not have to be limited to silicon, as the same device structure could be implemented for any material deposited by a conformal deposition technique such as other CVD techniques.

Appendix A
Nanowire MSM photodetectors

Flat panel imagers based on indirect detection of x-rays using amorphous silicon (a-Si) photodiodes in combination with a phosphor demonstrate high image quality, offer large area imaging and relatively high resistance to radiation damage [McDermott et al. 2004]. However, image lag and change in sensitivity and gain is known to occur during x-ray imaging due to trapped charges within the a-Si photodiode [Siewerdsen et al. 1999]. Image lag occurs when remnant charge generated in a previous image frame is read out in a subsequent frame. Similarly, change in sensitivity and gain occurs when charged traps alters the electric field within the photodiode [McDermott et al. 2004]. In this appendix, the use of crystalline silicon nanowires as a new photodetector material is investigated for medical imaging applications [Adachi, Wang, et al. 2010] such as continuous fluoroscopy or "singleshot" radiography (eg. chest radiography). Silicon nanowires have high hole mobilities after surface passivation [Cui et al. 2003] and low optical reflectance [Tsakalakos et al. 2007] making them promising for digital medical imaging photodetectors. The low optical reflection results in enhanced absorption of incoming light potentially increasing collection efficiency of photodetectors. In this study, crystalline silicon nanowires were fabricated and investigated as a potential alternative to a-Si for large area digital imaging applications. Crystallinity of nanowires was verified by Raman Spectroscopy. Silicon nanowires were incorporated into a metal-semiconductor-metal (MSM) device structure. The MSM structure has been reported previously using thin film amorphous silicon as the photodetector material and is attractive because of simplicity in fabrication and has comparable responsivity and collection efficiency as p-i-n photodiodes [Taghibakhsh et al. 2007]. The responsivity and collection efficiency of silicon nanowire MSM photodetectors were measured for different applied bias voltages. The temporal response of the MSM photodetector to a blue LED was also measured and discussed.
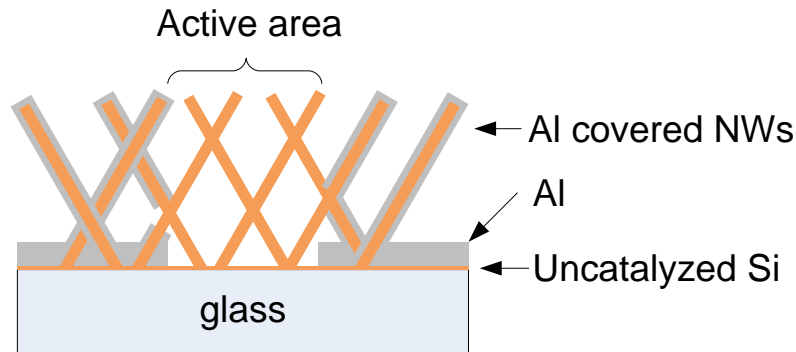
Figure A-1: Cross section illustration of Nanowire MSM photodetector with 1 μm spacing [Adachi, Wang, et al. 2010].

Al electrodes were deposited by magnetron sputtering deposition on top of the nanowires. Afterwards the Al was patterned by photolithography using a KarlSuss MA-6 mask aligner under low-vacuum contact mode to define the active device area. Al was etched using PAN etchant solution. The MSM structure operated laterally with aluminum electrode contacts spaced 1 or 2 microns apart. No surface passivation was used in this work.

An illustration of the cross section view of the MSM photodetector is shown in Figure A-1 (not to scale). The electrodes are defined by photolithography and as a result along the edges of the active area some nanowires which cross over the edge are only partially covered by Al. The uncatalyzed amorphous silicon growth occurs during the VLS growth method and is a competing process with silicon nanowire growth [Kamins 2001]. Uncatalyzed a-Si lay beneath the silicon nanowires and covers the entire substrate between electrodes. The electrodes consist of a thin layer of Al which covers the nanowires and a thicker film of Al which covers the substrate.
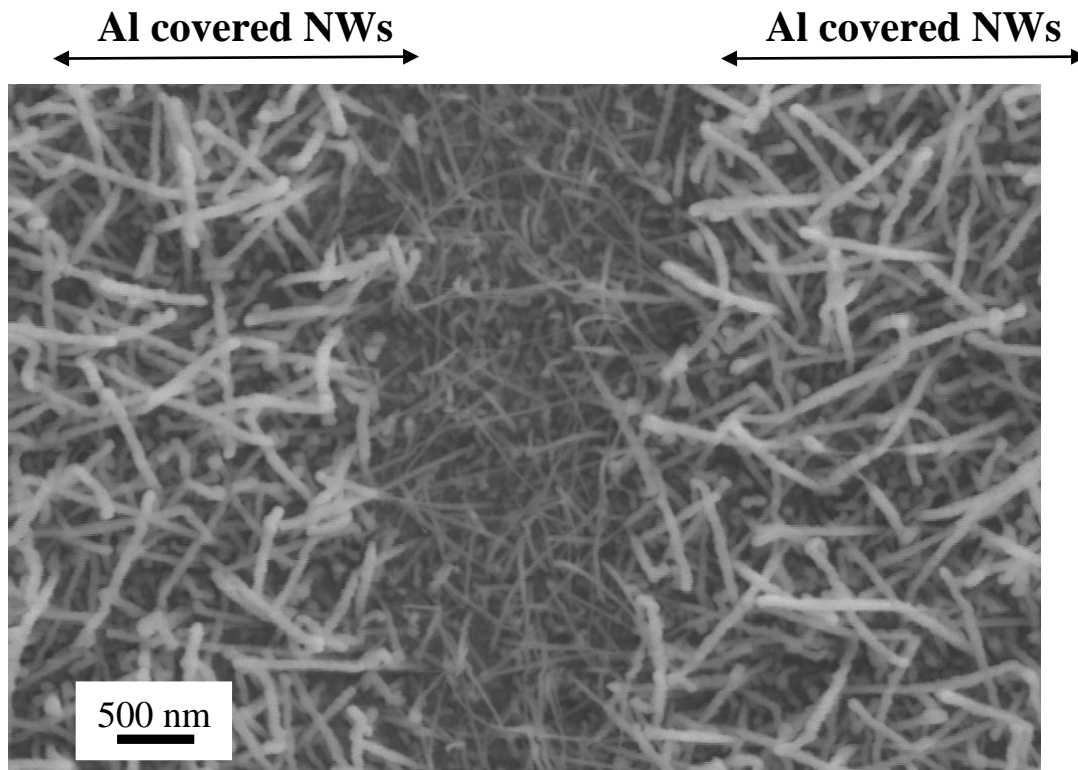
Figure A-2: Plan-view SEM micrograph of Nanowire MSM photodetector with 1 μm spacing [Adachi, Wang, et al. 2010].

A plan-view SEM micrograph of the MSM photodetector with 1 μm spacing is shown in Figure A-2. The labeled regions on the left and right side are Al covered nanowire electrodes. The uncovered silicon nanowires in the center act as the active area of the device. Nanowires are grown on glass and in the absence of a crystalline seed align randomly with respect to the substrate. The nanowire diameter is 35 nm ± 5 nm with a lateral length of up to 1.5 μm. The thickness of the Al contact was about 100 nm. Various Al contact thicknesses were attempted but due to isotropic undercut etching of the thin film of Al, the spacing between electrodes could not be well controlled if the Al film was too thick.
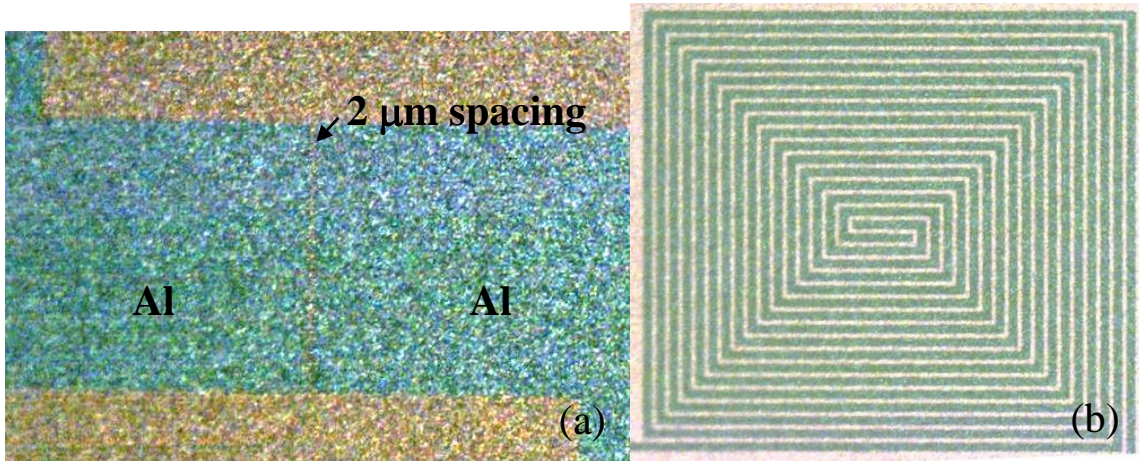
Figure A-3: Microscope image of Nanowire MSM photodetector with 2 μm spacing (a) and MSM spiral photodetector with 2 μm spacing (b) [Adachi, Wang, et al. 2010].

Microscope images of the two MSM photodetector structures are shown in Figure A-3. The first device structure shown in Figure A-3 (a) consists of two 250 μm wide rectangular electrodes separated by a spacing of 2μm. All I-V curves, collection efficiency and photoresponsivity measurements were taken using this structure. The second structure shown in Figure 4-3(b) consists of two spiral electrodes separated by a spacing of 2μm. This structure increased the active area of the device and was used for characterizing the temporal response.
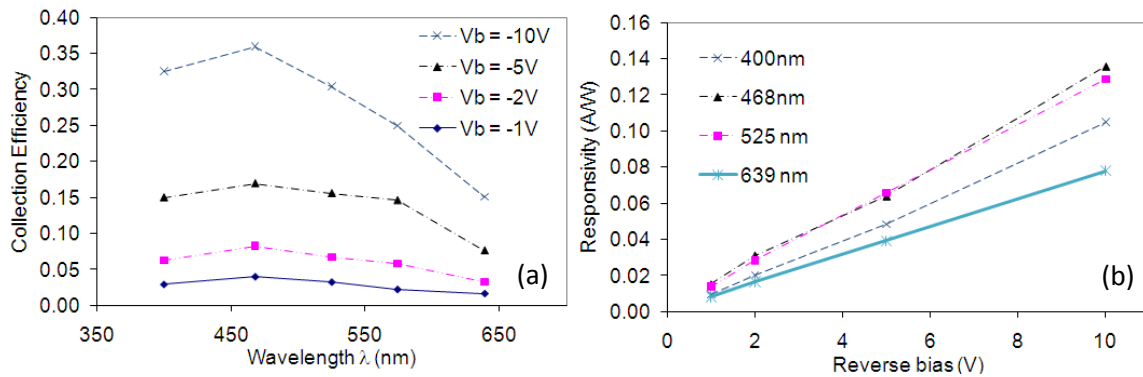
Figure A-4. Collection efficiency of Silicon nanowire MSM photodetector (active Area = 2 μm x 500 μm). Responsivity of a silicon nanowire MSM photodetector (active area = 2 μm x 500 μm) as a function of reverse bias [Adachi, Wang, et al. 2010].

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The collection efficiency of the nanowire MSM photodetector with an electrode spacing of the 2 μm x 500 μm is shown in Figure A-4(a). The area of the device was calculated to be the area between the electrodes rather than the area of the exposed nanowires which was unknown. The collection efficiency increased with increasing voltage bias indicating a strong applied electric field is necessary for efficient collection using the MSM structure. The collection efficiencies increased further with higher biases of up to -15V but fringing of electric field were believed to lead to inaccuracy of the active device area and were not included in Figure A-4(a).

The responsivity of a silicon nanowire MSM photodetector with an active area of 2 μm x 500 μm is shown in Figure A-4(b) as a function of reverse bias for four different wavelengths of incident light. Responsivity increased nearly linearly with reverse bias for all incident wavelengths with a values of up to 0.136 under a reverse bias of 10V.
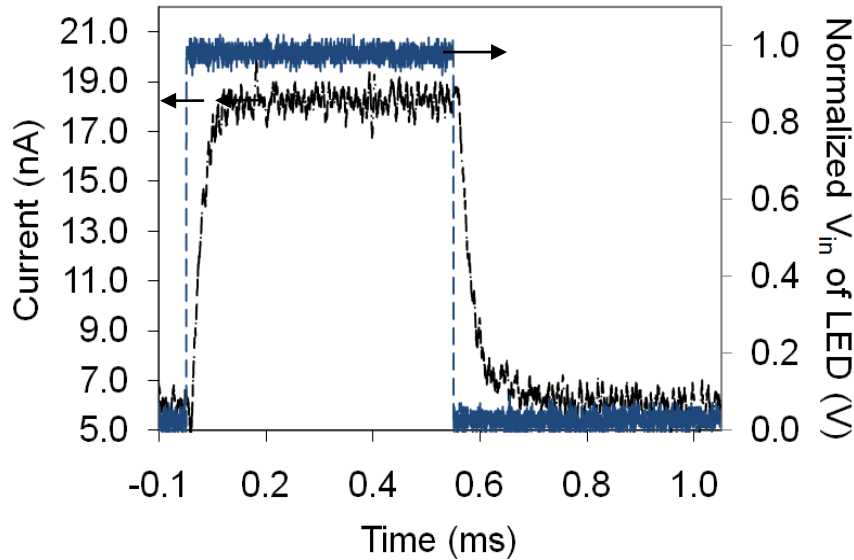
Figure A-5. Temporal Response of a silicon nanowire spiral MSM photodetector under a reverse bias of -2V excited by a blue LED [Adachi, Wang, et al. 2010].

The temporal response measurements of the spiral MSM photodetector from Figure A-3 (b) under a voltage bias of -2V is shown in Figure A-5. The time constant was measured to be 28.2 μs with respect to when the LED was turned on. The 10% to 90% rise time was measured to be 35.2 μs

and the 90% to 10% fall time was 89.8 µs. Note that the fall time was longer than the rise time when a negative bias voltage was applied to the device whereas the rise time was longer if a positive bias voltage was applied. The slower fall time using a negative bias observed in Figure A-5 is believed to be caused by trapping and releasing by surface states on the nanowire walls. One consequent of using nanowires is a significant increase in surface area. Trapping caused by surface states can be reduced by surface passivation. For example, hole mobility of nanowires increase significantly after surface passivation [Cui 2003]. No passivation layer was used in this work. Therefore to minimize the effect of surface recombination, passivation of nanowires using films such as a conformal PECVD deposited silicon nitride or thermal silicon oxide is necessary.

Another reason for the slow fall time of the nanowire photodetector is the contacting method used. As illustrated in Figure A-1, within the active area of the device the two ends of nanowires do not touch the opposite electrodes. As a result, photogenerated electrons and holes within a nanowire must travel to the electrodes via the uncatalyzed amorphous silicon which has deep traps caused by dangling bonds and bail tail states within the electronic band gap [Street 1991]. Therefore an axial path along the nanowire is required for free carrier transport by contacting both ends of the nanowires. One solution for this problem using the MSM structure is to grow nanowires with a longer lateral length.

In conclusion, silicon nanowires have advantageous optical and electronic properties as compared to amorphous silicon and are promising for digital imaging applications. Temporal response measurements in response to an LED light source showed that the fall time was 89.8 µs, relatively high compared to the rise time of 28.2 µs attributed to the deep trapping in uncatalyzed amorphous silicon and surface states. Growing nanowires with longer lateral length and nanowire surface passivation were identified as methods for increasing device performance.

Appendix B

Basic Semiconductor Formulas used by Sentaurus simulator

Poisson's Equation

$$\nabla \cdot \varepsilon \nabla \phi = -q(p - n + N_D + N_A) - \rho_{trap}$$

where ε is the electrical permittivity, ϕ is the electrostatic potential with reference to vacuum level, q is the elementary electronic charge, n and p are the free electron and hole densities, N_D is the concentration of ionized donors, N_A is the concentration of ionized acceptors and ρ_{trap} is the charge density contributed by traps and fixed charge.

Continuity Equations

$$\nabla \cdot \vec{J}_n = q\left(R_{net} - G_{opt}\right) + q\frac{\partial n}{\partial t}$$

$$-\nabla \cdot \vec{J}_p = q(R_{net} - G_{opt}) + q\frac{\partial p}{\partial t}$$

where $\vec{J}_n$ and $\vec{J}_p$ are the electron and hole current densities, R_{net} is the recombination-generation rate of electrons and holes, G_{opt} is the optical generation rate.

Drift-Diffusion Model

$$\vec{J}_n = -nq\mu_n \nabla \phi_n$$

$$\vec{J}_p = -pq\mu_p \nabla \phi_p$$

Optical Generation

$$G_{opt}(x, y, z) = I_o(x, y, z)(1 - e^{-\alpha(\lambda)L})F,$$

where I_o is the incident light, $\alpha(\lambda)$ is the absorption coefficient of the material, L is the length that light has traveled within the material, and F is the probability a photon absorption creates an electron-hole pair and is set to be 1

SRH Recombination (largest contributor to recombination in p-i-n devices)

$$R_{net}^{SRH} = \frac{np - n_{i,eff}^2}{\tau_p(n + n_1) + \tau_n(p + p_1)},$$

$$\text{where } n_1 = n_{i,eff}\ \exp\left(\frac{E_{trap}}{kT}\right)$$

$$\text{and } p_1 = n_{i,eff}\ \exp\left(\frac{-E_{trap}}{kT}\right)$$

where τ_n and τ_p are the minority lifetimes, k is Boltzmann's constant, T is temperature, $n_{i,eff}$ is the effective intrinsic density, E_{trap} is the difference between the defect level and intrinsic level.

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