Amorphous Silicon Dual Gate Thin Film Transistor & Phase Response Touch Screen Readout Scheme for Handheld Electronics Interactive AMOLED Displays

by

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AUTHOR'S DECLARATION

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Abstract

Interactive handheld electronic displays use hydrogenated amorphous silicon (a-Si:H) thin film transistor (TFT) as a backplane and a Touch Screen Panel (TSP) on top as an input device.

a-Si:H TFT used in active matrix liquid crystal displays (LCDs) in which the TFT acts as pixel switches. The low mobility and instability of a-Si:H TFT threshold voltage are major two issues for driving constant current as required for organic light emitting diode (OLED) displays. Low mobility is compensated by increasing transistor width or resorting to more expensive or less reliable material TFTs. On the other hand, the ever increasing threshold voltage degrades the drain current under electrical operation causing OLED display to dim.

Mutual capacitive TSP, the current cell phone standard, requires two layers of metals and a dielectric to be put in front of the display, further dimming the device and adding to visual noise due to sun reflection, not to mention increased integration cost and decreased yield.

This thesis focuses on the aforementioned technological hurdles of a handheld electronic display by proposing a dual-gate TFT used as an OLED current driving TFT and a novel phase response readout scheme that can be applied to a one metal track TSP.

Our dual-gate TFT has shown on average 20% increase in drive current over a single gate TFT fabricated in the same batch, attributed to the aid of a top channel to the convention bottom channel TFT. Furthermore the dual gate TFT shows three times the Poole-Frenkel current than the single gate TFT attributed to the increase in gate to drain overlap.

The dual-gate TFT shows a 50% improvement in threshold voltage shift over a single gate TFT at room temperature, but only ~8% improvement under 75ºC. This is an important observation as it shows an accelerated threshold voltage shift in the dual-gate. This difference in the rate of threshold voltage change under varying temperature is due to the difference in interface states at the top and bottom channel. Using these results, the dominant

mechanism behind threshold voltage shift is attributed to Libsch and Kanicki's multi-level temperature dependant dielectric trapping model.

The phase response TSP readout scheme requires IC only on one side of the display. Its unique design consisting provides touch signal readability and digitization without an A/D converter. Phase response readout out scheme, using Cadence Spectre simulation, showed that both touch occurrence and touch position can be obtained using only one metal layer.

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Dedication

To Ammu, Abbu, Apuni, Choto Apu, Raeed and Rizu bhai for all your patience, love and support.

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Chapter 1

Introduction

1.1 Displays and Touch Screen Electronics Niche

The invention of transistors, leading to the rise of electronic products, brought about astounding advances in the areas of computation, communication and display of information. The device that sparked the electronics industry was the Bipolar Junction Transistor (BJT)[1][2]. BJTs found many applications in the areas of computing and communications. Due to their small size compared to the previous technology of vacuum tubes, unprecedented ability for complex processing ability could be achieved in a tiny amount of space. The process of creating thousands of transistors in a compact chip came to be known as Very Large Scale Integration (VLSI) [1]. BJTs dominated the VLSI market until the late 1970s, being overtaken by Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) which continue to dominate the market today [2] [3].

Over the decades that have passed since the introduction of transistors, increasing numbers of electronics have found a place in our daily lives. The proliferation of flat panel displays – for televisions, computer and laptop monitors, cell phones and other handheld devices – is a prominent example. These products gave rise to a new type of FET device: the Thin Film Transistor (TFT).

The TFT is similar to the MOSFET, as both were developments from the original Field-effect Transistor (FET) as first proposed by J.E. Lilienfeld in his 1930 patent [4]. The design and implementation of TFTs mainly deviates from their MOS counter-parts due to their separate applications [5]. Unlike the MOSFET, TFTs were slow to gain a foothold in industry. Although TFTs were conceptualized in 1979 [36], they did not become popular until Liquid Crystal Displays (LCDs) entered the market in the 1990s. Less than two decades later, in 2007 alone, display manufacturers made about 50 square kilometres of LCDs, amounting to roughly 10^{15} TFTs. These were sold for about $100 billion [5]. Since the size

of the substrate in these applications are generally larger than the standard VLSI substrate (a $1m^2$ TFT substrate compared to a $0.114m^2$ VLSI substrate [6], this area of electronics is referred to as Large-area Electronics or Macroelectronics.

After dominating the computer monitor and television market, TFTs began to find applications in the smartphone industry as backplane components for both LCD and organic light-emitting diode (OLED) displays. A key feature of a Smartphone is its user friendly interface, which drives the increasing demand for Touch Screen Panels (TSPs) to be integrated with these displays. This technology led to a massive research effort into touch screen displays focusing on the following figures of merit: touch sensitivity, light transparency and process integration cost [8]-[23]. There are about ten different types of TSPs which are documented in an SID review paper [24]. However, only two of these technologies, "capacitive" and "resistive", have achieved popularity in handheld devices. As the focus of this thesis is on handheld electronics, only the two aforementioned touch sense methods will be further discussed in Section 1.3.

Since this thesis covers both display backplane technology and TSPs, this introduction will include a short review for TFT technologies in display backplanes that will be covered in Section 1.2, followed by a similar treatment of TSPs in Section 1.3.

1.2 Active Matrix Backplane Technologies

1.2.1 Matrix Displays

Flat panel Displays consists of a matrix of lights arranged in a rectangular configuration as shown in Figure 1.1a. Each visible dot of light in the display is known as a pixel. Pixels either emit light in case of emissive displays (e.g. plasma, EL, FED, and OLED) or modulate the light from a backlight such as LCD technology. The matrix form allows each pixel to be selected by choosing the appropriate row and column via applying voltage and provide the same brightness during the frame time. Figure 1.1b illustrates a pixel being selected using a given row and column coordinate. The rows are sequentially scanned and activated by row driver circuitry while the video signals are synchronously transferred to pixel circuits in each row by column drivers.

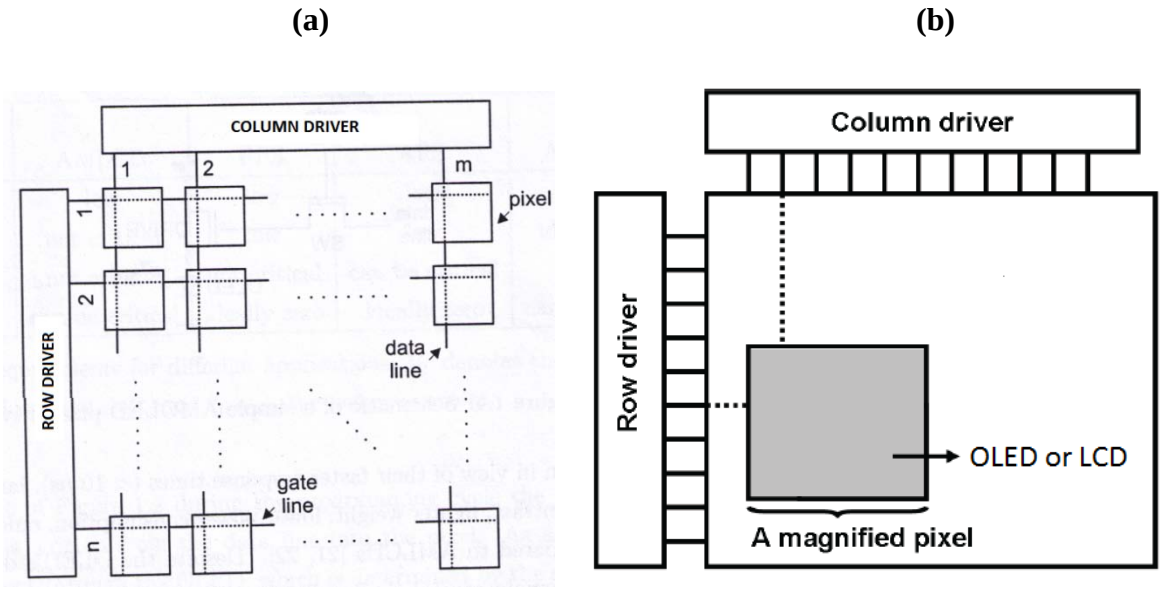


Figure 1.1: a) Display Matrix Schematic with m x n pixels [25]. **b)** Display Matrix with a selected pixel [23]

1.2.2 Passive Matrix Displays

The passive component in an LCD is a capacitor, whereas in an OLED display, it is a diode. Hence, an array of either of these components is known as a passive matrix array. Schematics of these are shown in Figure 1.2 and Figure 1.3. Major limitations of a passive matrix array are crosstalk, limited programming time, high peak brightness, and high power consumption. While other limitations affect the achievable size and resolution, cross talk can affect the image quality even in small displays. When a pixel is selected using proper row and column coordinates, the other pixels in the selected row or column would see a partial voltage and become partially turned on. This leads to a reduction in contrast between selected and non-selected pixels. Reduction in contrast is problematic for large displays that are required to show intermediate colours known as gray-scale capability. Passive Matrix Arrays also compromise viewing angle in LCDs and reliability in OLED displays [26] [29]. Due to these limitations, passive matrix is not used in the television and computer monitor industry. To overcome these faults, active matrix displays were developed.

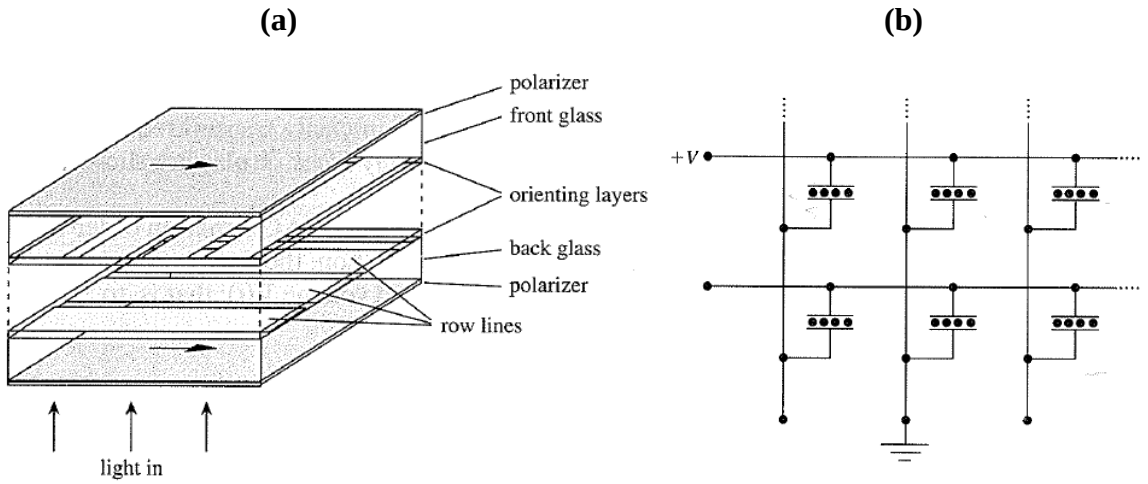


Figure 1.2: a) PMLCD Display construction with a) perpendicular row and column lines bonded with Optical polarizers to the front and back surfaces. **b)** PMLCD equivalent circuit. A pixel is addressed by applying a voltage +V. Column lines that are not selected are floating, while the column that is selected is grounded [29]

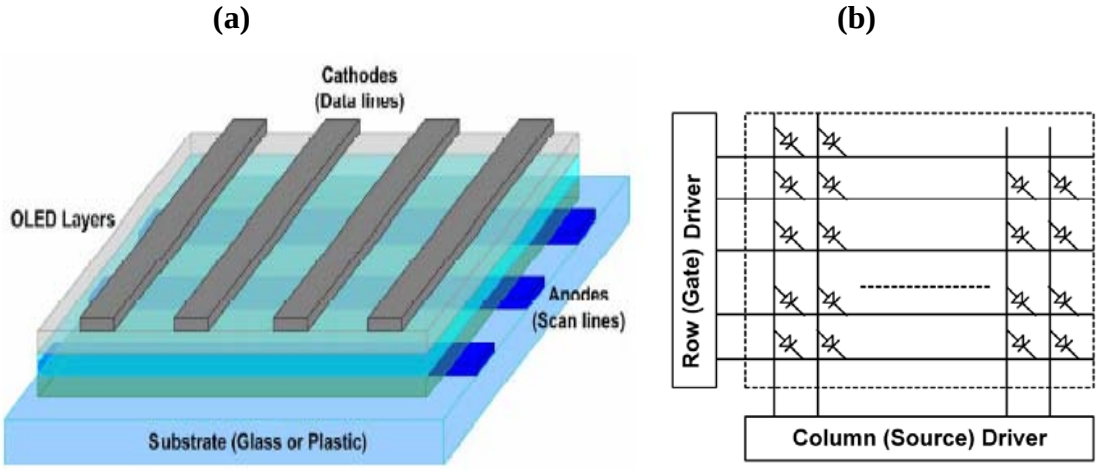


Figure 1.3: a) PMOLED Display and **b)** its equivalent circuit [31]

1.2.3 Active Matrix Displays

The active matrix displays consists of an active device in addition to the passive component in each pixel. This is integrated by adding a backplane of active devices along with the passive component as illustrated in Figure 1.4. The active devices in these backplane are TFTs and their roles can vary. For an LCD display pixels as shown in Figure 1.5a, the TFT acts as a switch and can be denoted as a S-TFT. The S-TFT selects the pixel row and drives the video signal into the capacitors C_s and C_{lc} in the form of voltages. The voltage in C_{lc} determines the orientation of the Liquid Crystals which reside in between C_{lc}. The orientation of the crystal determines the amount of back light that will be blocked. Cs is the storage capacitor that helps stabilize the voltage across C_{lc}.

The S-TFT is turned on by selecting the appropriate row signal. Otherwise, the S-TFT is turned off to select the next row. Provided that the TFT leakage current is sufficiently low, each capacitor will stay charged while the other rows are scanned. Furthermore, these turned-off TFTs will prevent significant partial charge transfer for non-selected pixels in the same row and column of the selected pixel. This eliminates the partially biased non-selected pixels and significantly improves the contrast in AMLCD.

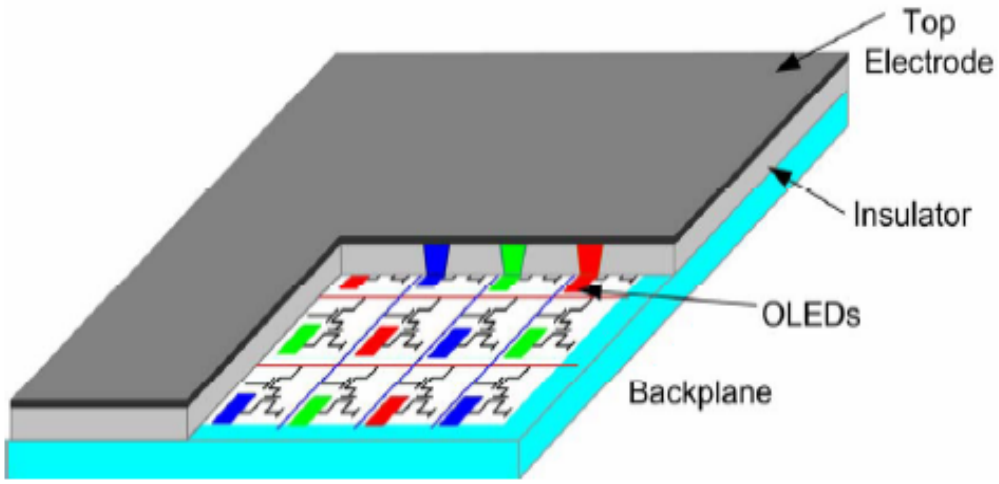


Figure 1.4: Conventional bottom emission AMOLED display that has a TFT backplane (white). The light emitted by the OLEDs go through the clear bottom glass (light blue). [31]

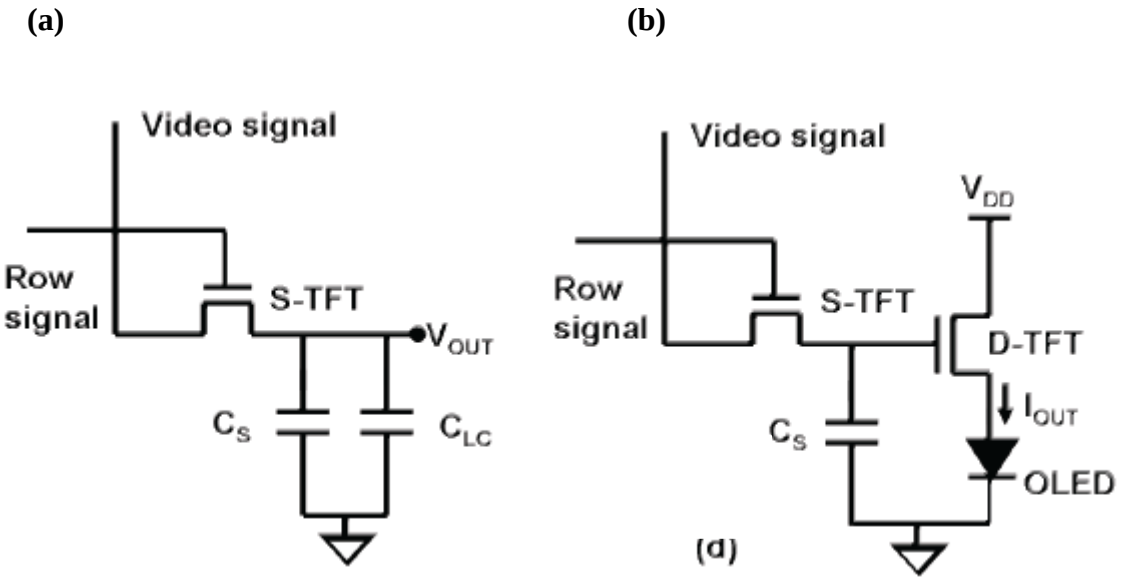


Figure 1.5: a) LCD pixel circuit schematic where S-TFT is the switch TFT, C_{LC} is the liquid crystal capacitor and C_S is the storage capacitance. **b)** OLED display pixel circuit schematic where S-TFT is the switch TFT and D-TFT is the Drive TFT. [32]

For an Active Matrix Organic Light Emitting Diode (AMOLED) display, the passive diode devices are driven by current and the switch can only be used to drive voltage. Hence another transistor is needed to convert the video signal source voltage into a current to drive the OLED in each pixel. This transistor is also referred to as a drive transistor and can be denoted as D-TFT as shown in Figure 1.5a**.** The D-TFT proves to be a challenge to implement and is a rich source of research opportunities, one of which is explored in this thesis. The problems arising from implementing the D-TFT will be discussed in the next section.

1.2.4 Drive TFT Implementation and Challenges for AMOLED Displays

OLED displays garnered much interest in the research and display industries due to their potential for low-cost fabrication, better color gamut, thinner format and low power consumption compared to LCDs [5]. Furthermore, OLEDs have demonstrated manufacturability on plastic which leads to more durable and flexible displays for cellular phones [5].

The challenge nevertheless lies in integrating the proper backplane with the OLEDs to manufacture a high-resolution, low-cost, low-power display. As mentioned in the previous section, TFTs do not act merely as a switch (S-TFT) in OLED display pixel circuits, but also an OLED current driver denoted as a D-TFT. A comparison of D-TFT and S-TFT requirements are is provided in Table 1-1.

Table 1-1: TFT requirements for AMLCD and AMOLED display applications

Parameter	AMLCD	AMOLED
V_t	Low to allow low voltage on	Low to allow low voltage on
ΔV_t	Not vital for transferring voltage	Vital for controlling exact current
μ (mobility)	Not vital (no high drive current needed)	High mobility needed to drive high current
Uniformity of μ and Vt	Vital for smooth display	Vital for smooth display

Unlike MOSFETs and BJTs that are primarily made from crystalline silicon, the TFT technology that is used for AMLCDs is a-Si:H. a-Si:H TFTs are currently the standard in the display market. a-Si:H TFTs meet the requirements needed for AMLCDs; namely low Vt, and uniformity in both Vt and mobility across the substrate. a-Si:H TFTs are currently capable of meeting the requirements needed for AMLCDs. [6].

Unlike AMLCDs, a-Si:H TFTs used for AMOLEDs have two problems: low mobility (1 cm^2/v-s for n-type and 0.001cm^2/v-s for p-type) and electrical bias-dependent Vt shift. Only n-channel TFTs are used for a-Si:H backplanes due to the extremely low mobility of p-channel TFTs. Furthermore, due to low mobility and drive current in general, TFTs with a large channel width are needed in the pixel circuit. The pixel circuit has to be shared between TFTs and the OLED for bottom emitting AMOLED displays. As pixel size is limited, a larger TFT means less area is available for the OLED as shown in Figure 1.6**.** Smaller OLED area means that higher current density is required through the OLED for the

same light output, which accelerates OLED degradation [30]. Consequently, it is preferable to maximize OLED area. The ratio between TFT and OLED area is referred to as fill factor, where high fill factor (OLED ratio) is preferred. D-TFTs take more than 75% of the circuit area in a pixel and ~15% of the pixel area itself as shown in Figure 1.6. In order to increase fill factor, the width of the TFT must be decreased but the drive current must remain the same, making high resolution OLED backplane design a challenge.

Furthermore, positive Vt shift reduces the current through the drive TFT, thus reducing the OLED luminance and causing the display to dim over time. Vt shift can be reduced by lowering gate voltage and channel current density, allowing the OLED display to retain its brightness for longer. The physics of Vt shift will be further discussed in Chapter 2.

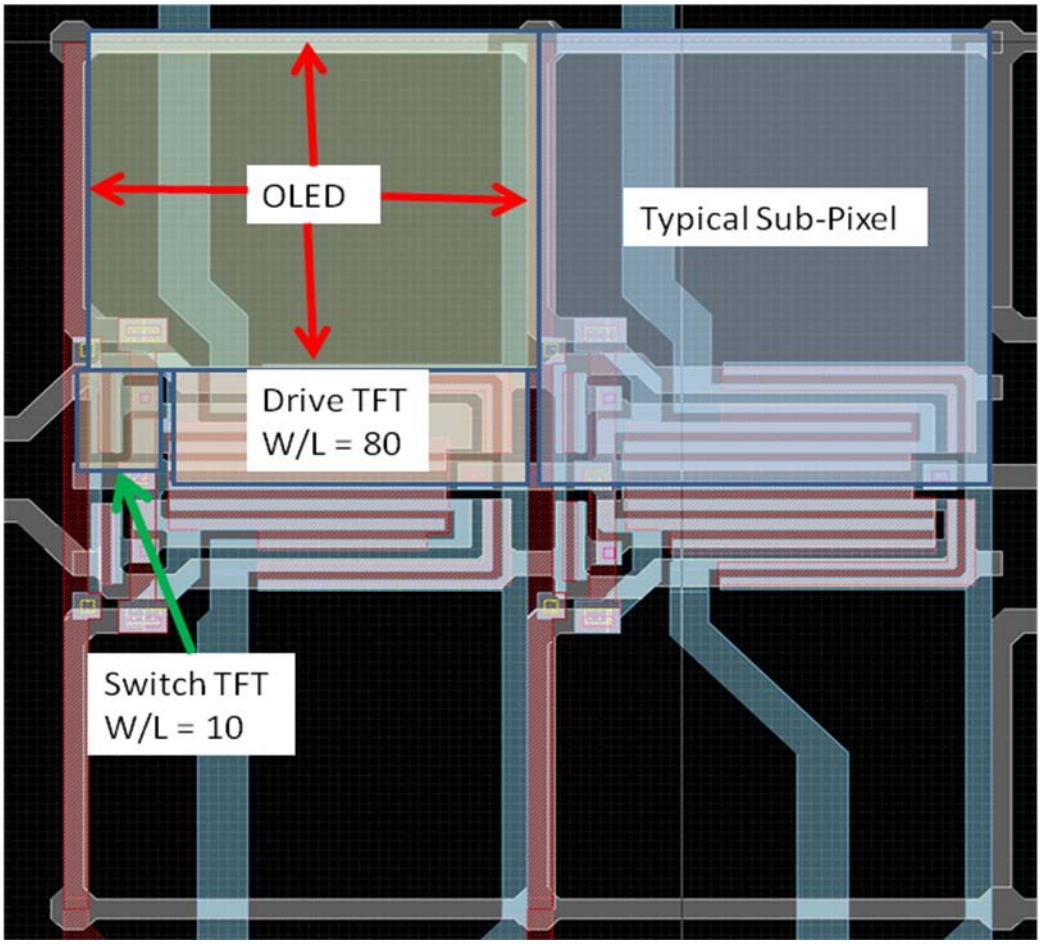
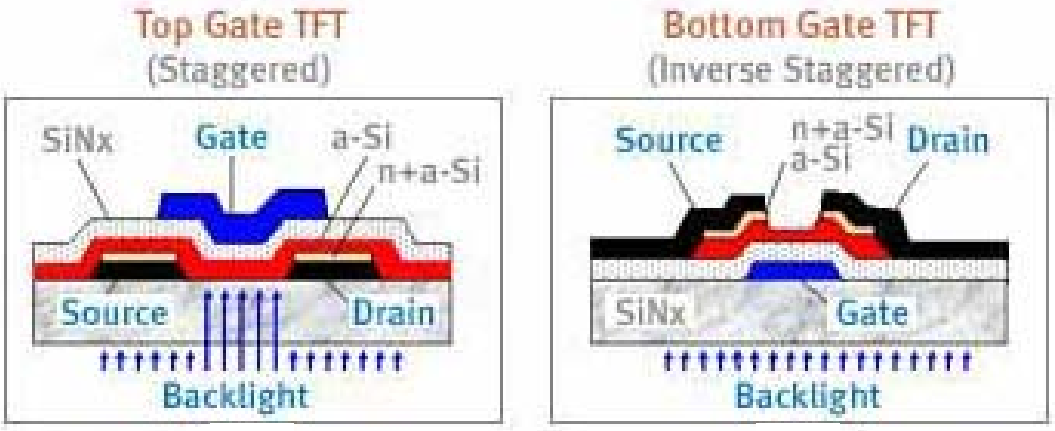


Figure 1.6: AMOLED pixel circuit with four sub-pixels, each sub-pixel dedicated for Red, Green Blue and White (RGBW). Notice that the Drive TFT takes up ~15-20% of the pixel.

Although most research regarding the D-TFT explores materials-based solutions [5], this thesis will approach the problem from a device architecture point of view. Therefore, the next two sections will provide background on conventional single-gate TFT architecture.

1.2.5 Single Gate TFTs: Bottom Gate vs. Top Gate

TFT devices can be either bottom channel depending on which order the Gate and source/drain (S/D) contacts are deposited. Figure 1.7a illustrates a top gate and Figure 1.7b illustrates a bottom gate TFT used for AMLCD [6]. The bottom gate TFT is the current standard for AMLCD. The bottom gate TFT has an advantage of using its gate as a shield against the backlight from penetrating the a-Si:H layer to prevent photo-induced degradation known as the Staebler-Wronski effect.. Furthermore, bottom gate TFT shows a higher mobility, lower threshold voltage, lower sub-threshold slope, higher driver current and lower shift in threshold voltage. A comparison between the two is illustrated in Figure 1.8



a) b)

Figure 1.7: Cross-section of **a)** Top Gate TFT **and b)** bottom gate TFT. It also illustrates that the gate is used as a shield against backlight from penetrating the a-Si layer to cause photo-induced degradation known as the Staebler and Wronski Effect. [6]

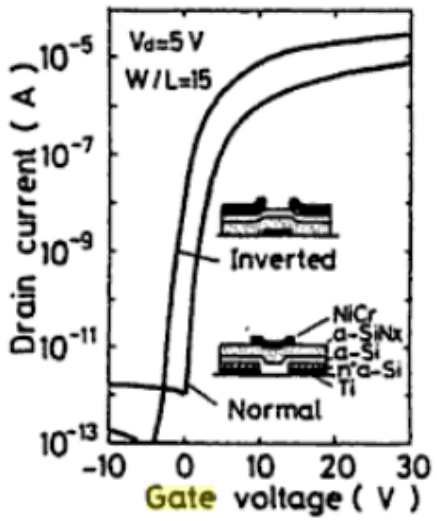


Figure 1.8: Transfer characteristics of top and bottom gate a-Si:H TFTs with same film deposition condition [7]

Bottom Gate TFT's superior performance is due to reduced hydrogen concentration, smaller gap of tail states, and better physical match than top interface devices. Furthermore, a higher SiNx plasma power and a higher SiNx plasma-phase hydrogen concentration, if deposited after the a-Si:H (top gate structure), damages the a-Si:H surface by creating dangling bonds that hinder mobility, Vth and increase threshold voltage shift [7]. Published results for top gate a-Si:H TFT mobility are capable of matching those of bottom gate TFTs subject to a dual-layer gate dielectric layer (interface layer and bulk layer) deposition [7][33]. However, the backlight, incident onto the exposed a-Si:H through the transparent substrate causes photo-induced defects (i.e. Staebler-Wronski effect) in the intrinsic silicon material and degrades device performance**.**

Regardless of which TFT structure is optimal, a combination using both bottom and top gates together in a dual-gate configuration may provide a performance advantage for drive current, current leakage control and Vt stability. However, having dual-gate TFTs means at least one extra mask and patterning step must be added to manufacturing cost, which discourages their implementation in low-cost commercial AMOLED displays.

However, it can be shown that the implementation of dual-gate device technology will not change the total manufacturing cost and is a viable improvement for bottom emission AMOLED displays.

1.2.6 Industrialization and Manufacturing Capital Cost

The display electronics industry is extremely competitive, especially in the area of consumer electronics. Figure 1.9 shows the AMOLED display market growth over the last few years and their projected growth in coming years [31].

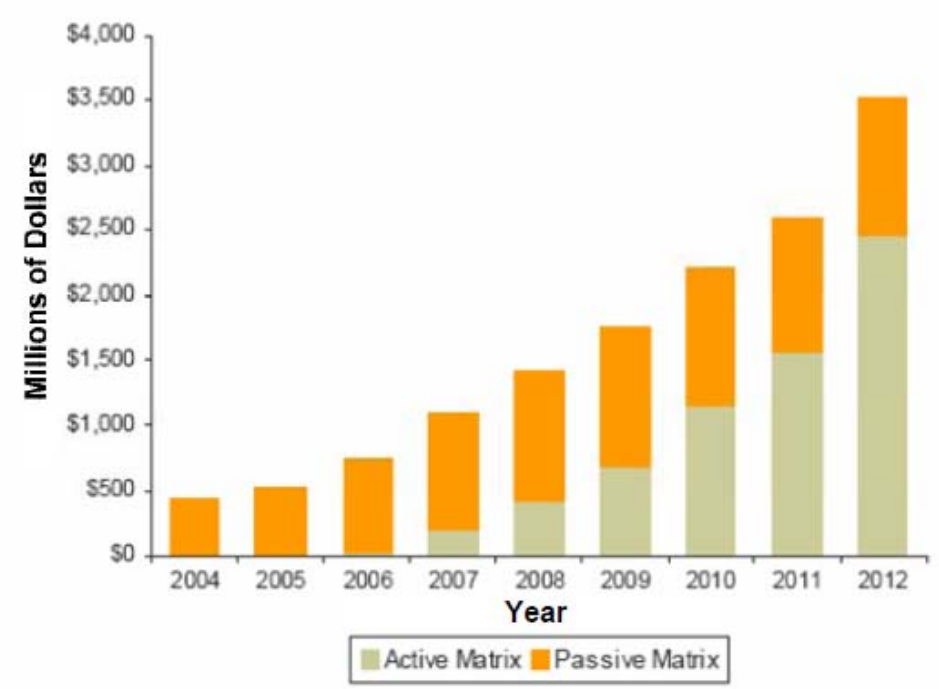


Figure 1.9: Present and Expected OLED market [27]

Market growth definitely shows opportunities for research and development for high-resolution, low-power and cost-effective displays. However, the current largest manufacturers such as Samsung and LG tend to reduce their capital/manufacturing cost per display by mass producing displays [6]. For high volume throughput, depreciation of capital occurs rapidly and in the case of LCD manufacturing, capital equipment cost can be fully depreciated with a period of less than 5 years. Hence the cost of conventional process and new process would be almost the same as long as the throughput has not been held back [6].

Having such a high throughput requires the system to be optimized and very robust. This creates a resistance to trying out new technologies such as Organic TFT (OTFT) or Metal Oxide TFTs in mass production, as any risk of hindering throughput would mean increases in capital cost and losses in profit. Therefore, it is difficult to contribute new improvements that will directly affect the industry.

However, the dual-gate TFT can significantly improve either drive current or Vt shift with a simple addition of an extra mask to the conventional fabrication method. Therefore, instead of looking at less reliable changes involving novel materials or new processes, this thesis will propose a device-architecture-level solution, using dual-gate TFTs, for the implementation of drive TFTs for OLED displays.

1.2.7 Dual-gate TFTs

Dual-gate TFTs were first proposed in 1982 [39]. Until then, the applications driving dual-gate TFT research include row/column drivers [41], and as shields against light from top-emitting display panels and X-ray imagers [35].

However, dual-gate devices have never been explored as drive TFTs for bottom emission AMOLED displays. As mentioned before, most of the circuitry in a pixel is comprised of drive TFTs, as the low mobility of a-Si:H requires large devices to drive the necessary current. Dual-gate TFTs can produce a larger sum of current than a conventional TFT without increasing device width.

On the other hand, since Dual-gate TFT uses two channels, it requires less voltage and current density to provide the same total amount of current than a conventional TFT which reduces the Vt shift.

Implementation of Dual-gate adds a mask layer which increases manufacturing cost. However, this is based on a robust process which can be implemented in large-scale manufacturing lines to make the added mask cost negligible compared to the total manufacturing cost per unit display. In the end, implementing the Dual-gate TFT provides either a higher fill factor due to high current drive or increased reliability due to reduced threshold voltage at a potentially negligible increase in manufacturing cost.

1.2.8 Contributions from Dual-Gate TFT

There are two contributions from a dual-gate TFT. The first contribution is to show with explanation an increased drive current from the dual gate compared to a single gate TFT in both forward bias and reverse bias. The first contribution from dual-gate TFT will be covered in **Chapter 2**.

The second contribution is to show that for a constant current stress test, the Vt shift under room temperature is improved by ~50% and that stressing both dual and single gate TFTs allows better understanding of the mechanism behind the Vt-shift. The second contribution from dual-gate TFT will be covered in **Chapter 3**.

1.3 Touch Screen Panel (TSP)

Touch screen panels are at the forefront of a design revolution in user interfaces of mobile devices for information input. The basic TSP is a simple transparent input layer that is put in front of the display as shown in Figure 1.12c. The most popular TSP technology for mobile devices was the resistive type among various types of TSP in the past [28]. However, recently, the capacitive TSP has become more popular due to its soft, multi-touch and flat design capability [28].

The Figure of Merit of a TSP is the following:

- Sensitivity
- Multi-touch
- Cheap material and processing cost
- Simple processing leading to low power computation
- Transparency
- Durability

After capacitive TSPs became popular amongst mobile devices, research has focused on integrating the capacitive TSP with the display in a single layer to reduce processing cost and to maximize the brightness of the display [8-18]. Although there are about ten different implementations of TSPs [24], this thesis will discuss only the resistive and capacitive TSPs due to their application towards handheld electronics.

1.3.1 Resistive Touch Screen Panel

A resistive TSP, as shown in Figure 1.12, is coated with a thin metallic film that forms part of an electrically conductive and resistive layer. It detects touch by the change in electrical current which is registered as a touch event and sent to the controller for processing. Resistive screen requires the pressure from the finger to make a connection between the conductive and resistive layer of the circuitry, changing the resistance. Resistive touch screens are very common for automotive GPS and Game systems like the Nintendo DS. Note that in a resistive TSP, any insulating device *(e.*g a plastic stylus) can be used to input information because it provides the pressure required to make the contact between the

conductive and resistive layer. Furthermore, the TSP is not affected by outside elements such as dust or water. The cost of the resistive material is much cheaper than that of its capacitive TSP counterpart [24]. Nevertheless, cheaper, more malleable material makes it less durable.

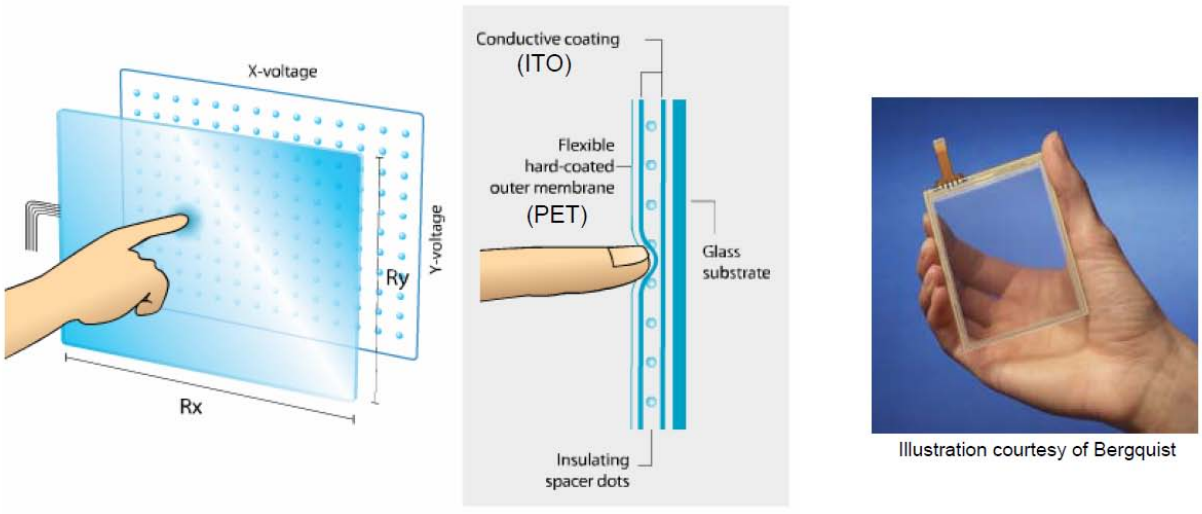


Figure 1.10: a) Resistive touch screen front view and **b)** side view while being touched to input signal and **c)** real life example [28]

A resistive touch screen works by applying a voltage across a resistor network and measuring the change in resistance at a given point on the matrix. The change in the resistance ratio marks the location on the touch screen. The two most popular resistive architectures use 4-wire or 5-wire configurations [25]. The circuits determine location in two coordinate pair dimensions, although a third dimension can be added for measuring pressure in 4-wire configurations [25].

1.3.2 Capacitive Touch Screen Panel

Capacitive TSPs, as shown in Figure 1.13, are made of glass coated with a transparent conductor that conducts a continuous electrical current across the sensor. The transparent electrode materials used for Capacitive TSP include indium tin oxide (ITO), Aluminum Zinc Oxide (AlZnO). The capacitive TSP can be divided into two categories: self capacitive and

mutually capacitive. The following section will briefly look into these two types of capacitive TSP.

1.3.2.1 Self Capacitive Touch Screen Panel

Self capacitive TSP is made by coating one side of a glass with a conductive layer. A small voltage is applied to the layer, resulting in a uniform electrostatic field. When a conductor, such as a human finger, touches the uncoated surface, a capacitor is dynamically formed (Figure 1.13). The sensor's controller can determine the location of the touch indirectly from the change in the capacitance as measured from the four corners of the panel [28]. As it has no malleable parts like its resistive counterpart, it is moderately durable but has limited resolution, is prone to false signals from parasitic capacitive coupling, lacks multi-touch/sliding capability and needs calibration during manufacture. It is therefore most often used in simple applications such as industrial controls and kiosks [28].

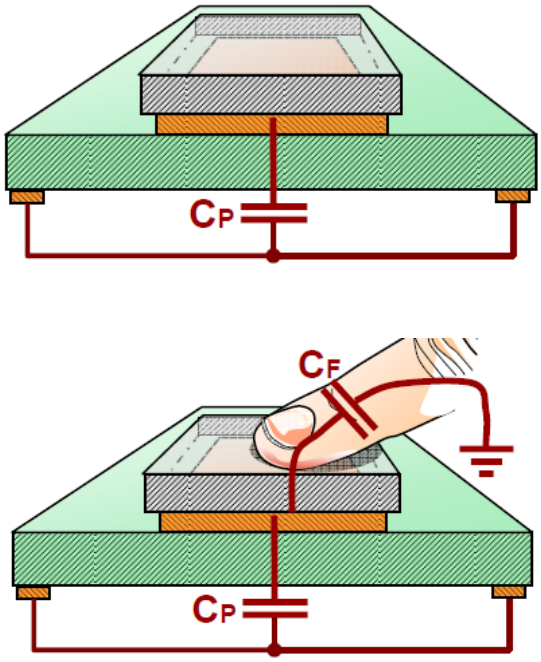


Figure 1.11a) self-capacitance touch pad showing its intrinsic capacitance and **b) increase** in capacitance due to the touch of a finger (grounded conductor) [42]

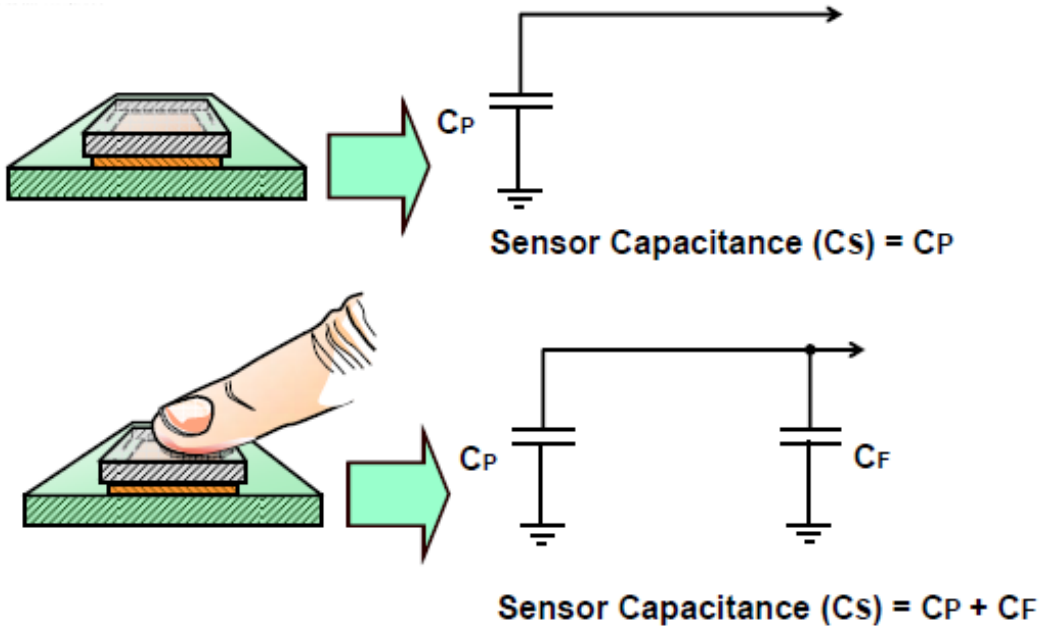


Figure 1.12: a) self-capacitance touch pad showing its intrinsic capacitance and **b) increase** in capacitance due to the touch of a finger (grounded conductor) [43]

1.3.2.2 Mutual Capacitive Touch Screen Panel

Mutual Capacitive touchscreens are made using two separate, perpendicular layers of metal track that make up an array of capacitor as shown in Figure 1.15.

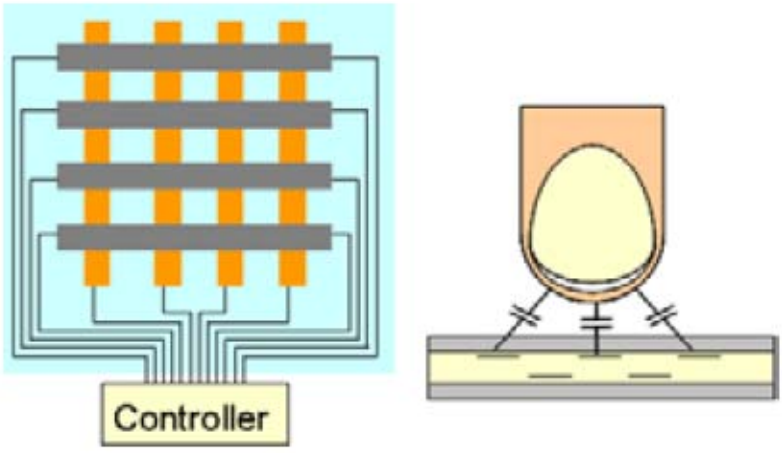
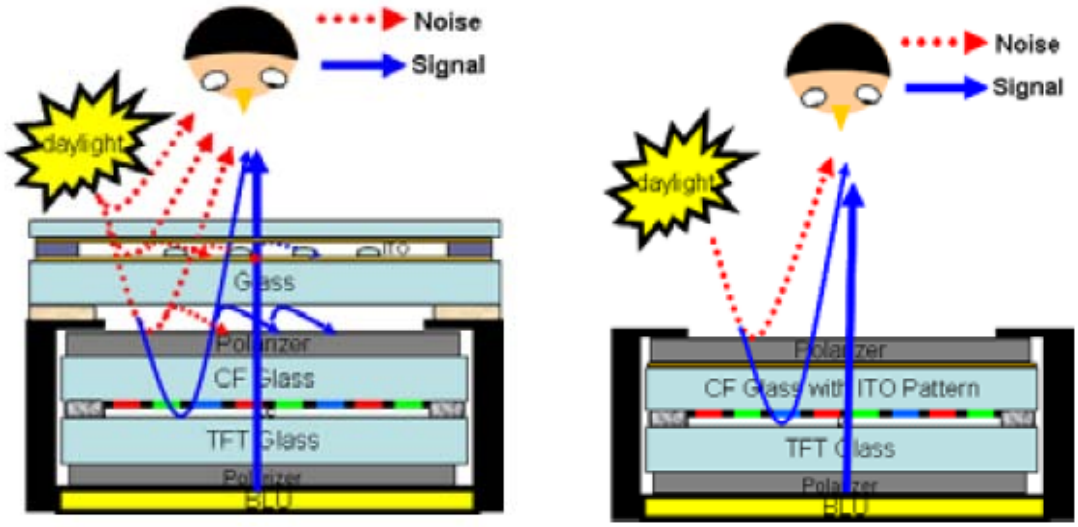


Figure 1.13: a) a mutual capacitive TSP and **b)** multiple cell detection of finger touch allowing higher touch resolution. [24]

Mutual capacitive TSP is capable of highly accurate touch input due to multiple capacitor cells sensing the same touch as shown in Figure 1.15b. A voltage is applied to the rows or columns. Using a conductor to touch the surface of the sensor changes the local electrostatic field which reduces the mutual capacitance. The capacitance change at every individual point on the grid can be measured to accurately determine the touch location by measuring the voltage in the other axis. Mutual capacitance allows multi-touch operation where multiple fingers can be accurately tracked at the same time.

A drawback to mutual capacitive TSPs is the requirement of three extra layers (two for metal tracks and one for a dielectric material) on top of the display which reduces the brightness of the display itself. Therefore, more power is needed from the OLED to make up for the brightness which leads to lower reliability and higher power consumption. Furthermore, extra layers increase process cost and also creates more reflection as shown in Figure 1.16.



a) **b)**

Figure 1.14: **a)** Standard display with external TSP which has high visual reflection and **b)** integrated TSP with reduced visual reflection [24].

Some developments made in the past year to improve on this include reducing the intermediate layers between the display and the TSP, having both row and column metal

layers on the same layer and for LCD, and integrating the touch capacitor within the LC layer.

AMLCD has an advantage over AMOLED when integrating the display and touch screen layers together, also known as integrated TSP [18] [20]. The liquid crystal media in a AMLCD array acts as a passive device and permits it to be integrated with a capacitive touch sensor in the same layer. In an AMOLED array, the passive device is the OLED device so it is not so simple to integrate a capacitive TSP on the same processing layer as the organic diode. Furthermore, these AMLCD integrated TSPs also use photo TFTs as optical sensors that complement the capacitive sensor as shown in Figure 1.17. Figure 1.18 shows how these TSPs can be integrated alongside the RGB sub pixels in an AMLCD display. The color pixel, consisting of the RGB sub pixels, will simply contain an additional sub-pixel dedicated for the photo TFT, the touch capacitor, and the appropriate readout amplifier.

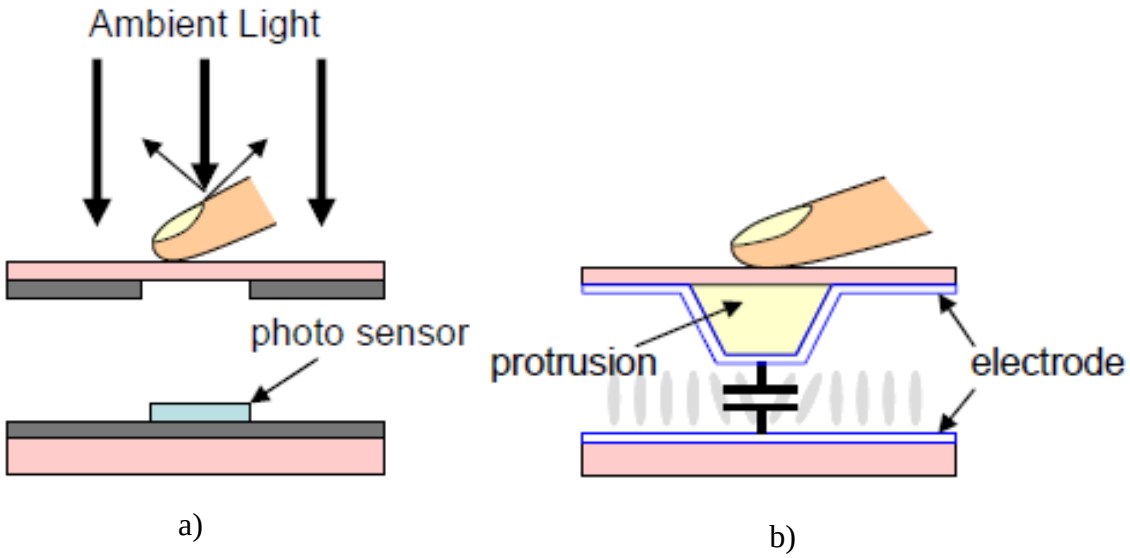


Figure 1.15: Hybrid TSP integrated with AMLCD with **a)** photosensing and **b)** capacitive sensing method [15].

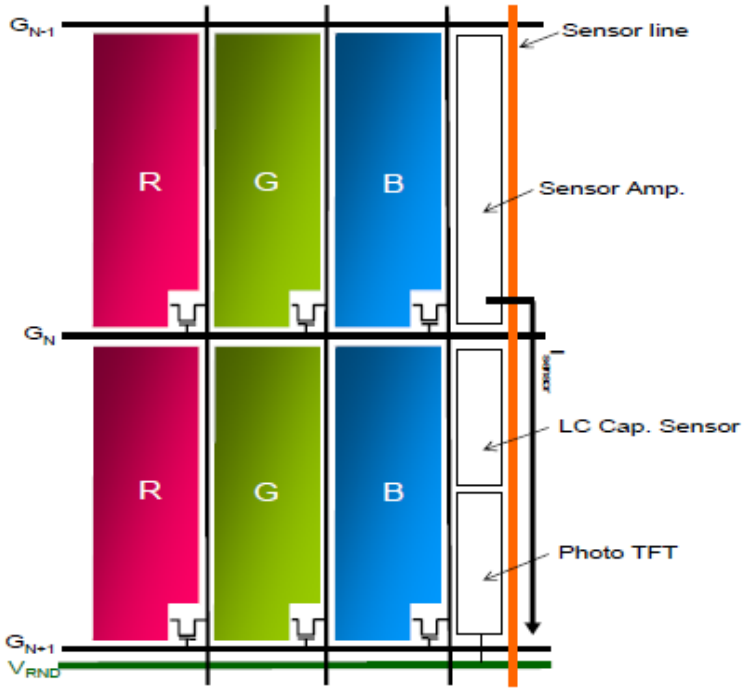


Figure 1.16: Hybrid TSP integrated with hybrid AMLCD on the same panel [15]

The integration of TSPs in AMOLED displays are described differently than their AMLCD counterpart. The integration of TSPs in AMOLED displays involves reducing the number of layers in between the display and TSP [13]. Reducing the intermediate layer creates a parasitic capacitance between the display electrode and the TSP electrode. Samsung has recently managed to suppress the effect of the parasitic capacitance through circuit techniques included in the readout circuit [13]. Further improvements on the AMOLED integrated TSP involve reducing the design of the capacitive grid itself [8][13]. Figure 1.19a shows the cross-section of the conventional TSP and Figure 1.19b shows the newly designed TSP cross section [8]. The idea here is to have both the row and column electrodes on the same layer. In order to prevent shorting between the row and column tracks, jumper metal lines are used as illustrated in Figure 1.20 [8]. The jumper metals reduce the total number of layers of TSP that is present in front of the display. Now the goal of this thesis will involve reducing the number of touch screen layers to one. In order to

reduce the number of touch screen layer to one, a novel method of touch readout will be proposed.

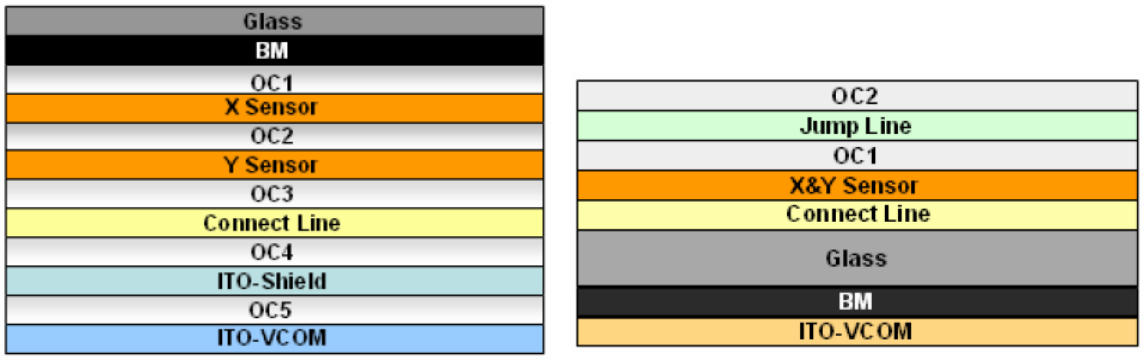


Figure 1.17: a) Conventional Mutual Capacitive TSP with separate x and y metal track sensors layers with a dielectric in between and **b)** newly designed TSP with x and y metal track sensors on the same layer [8].

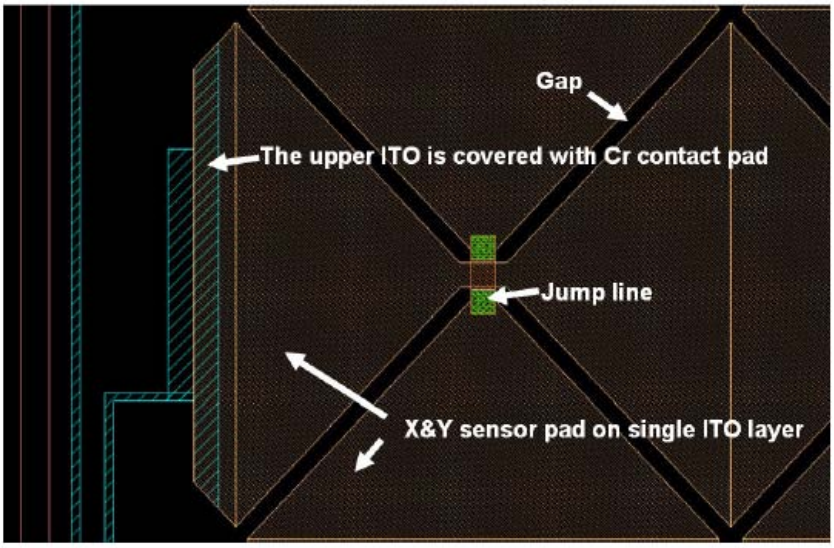


Figure 1.18: Top view of the mutual capacitive TSP with x and y sensors on the same layer with jumpers to avoid short [8].

1.3.3 Phase Response Touch Readout Method

Up until now, the capacitive TSP designs involve reading the touch input by measuring the difference in voltage on the metal tracks compared to a reference value. In short, it is a

voltage response system. Although implementation of this system is very mature, the cost of the fabrication is high due to the requirement of two metal tracks with an insulator in between.

On the other hand, it is possible to implement a one layer touch screen using a phase response readout method. The phase will depend on three components: 1.the capacitive change due to the finger touch, 2. the resistive change that will give the coordinate of the touch, and 3. the frequency that will create a current on the metal track

With the phase response readout method, a single metal track can be used to find both x and y coordinates on the TSP. The physics and methodology of the phase response will be thoroughly covered in Phase Response Touch Screen Panel Readout Scheme.

1.3.4 Contribution from a Phase Response Touch Screen Panel

The contribution from the Phase Response TSP is to provide a complete design of a readout scheme in CMOS technology. It will briefly provide the physics behind phase response and will include post-layout simulations of phase response from touch occurrence and touch position using Cadence Spectre CAD tool [44]. Although a test chip has been designed and sent to TSMC for fabrication, this thesis will not cover the physical silicon test results. All of these will be under Chapter 4.

1.4 Thesis Organization

The thesis is organized as follows: Chapter 2 will discuss dual-gate TFT fabrication, operation and superior drive current in comparison to a single gate TFT. Chapter 3 will discuss a-Si:H TFT instability mechanism, show higher stability for dual gate TFT and use both dual and single gate TFT to get better insight behind the dominating instability mechanism a-Si:H TFTs. Chapter 4 will propose a novel phase response touch screen readout scheme, including an overview on the phase-response concept, circuit-level implementation and post-layout simulation results. Chapter 5, the final chapter, will summarize the three contributions and its relevance towards the electronics market.

Chapter 2

Dual-Gate TFT Fabrication, Operation and Superior Current Drive

The objective of this chapter is to show superior driving capability and leakage current suppression of dual gate TFT over single-gate TFT. Yet, the chapter will present the background information prior to the result so it would be more coherent to explain the results right after. This chapter has four main sections which will cover the basic concepts of conventional TFTs and apply it to dual-gate TFT.

2.1 Material characteristics of amorphous silicon

Hydrogenated amorphous silicon is deposited using Plasma Enhanced Chemical Vapour Deposition (PECVD) with source gas mixture of Silane and Hydrogen. A picture of PECVD system is shown in Figure 2.1[32]. The temperature of deposition is 300°C or lower. This low temperature process along with amorphous nature of used substrates such as glass forms amorphous materials lacking structural order like that of crystalline silicon found in VLSI devices [6]. A comparison of crystalline and amorphous material is shown in Figure 2.2 [32]

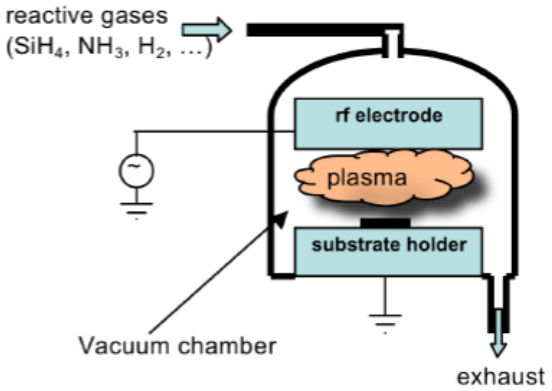


Figure 2.1: A Plasma Enhanced Chemical Vapour Depostion (PECVD) system [6]

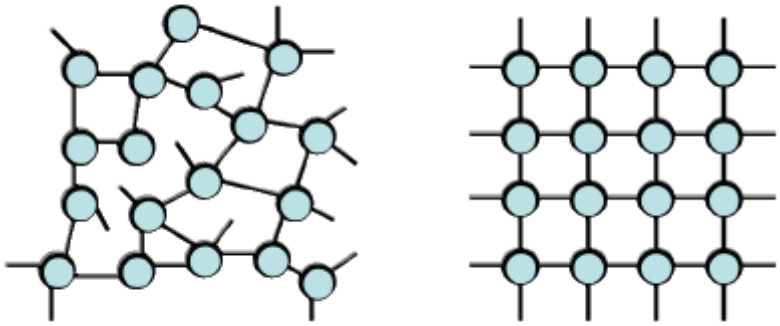


Figure 2.2: a) Amorphous silicon atomic structure and **b)** Crystalline silicon atomic structure [32]

In the crystalline structure, silicon atoms occupy specified locations with a uniform bond length and angle, while in the amorphous case, there are missing atoms and variation of bond angle and length [46]. The missing atoms create deep defect states in the middle of the energy gap and the variation of bond angle/length states that tail off right under the band gap referred to as band tails states [32] [46].

The electron mobility is degraded by the large concentration of band tail states acting as temporary traps for conduction electrons. Figure 2.3 shows a profile DOS in the enrgy gap of a-Si:H [32]. The electrons are trapped much of the time in band tail states and they are usually called band tail electrons.

The trap states below midgap tend to be donor-like (that is, positive when unoccupied and neutral when occupied by an electron), while those above midgap tend to be acceptor like. For a-Si:H TFTs, undoped silicon is used, hence n=p=ni, where n, p and ni are number of electrons, holes and intrinsic carriers. All three are all equal because the only source of electrons and holes is thermal generation [29].

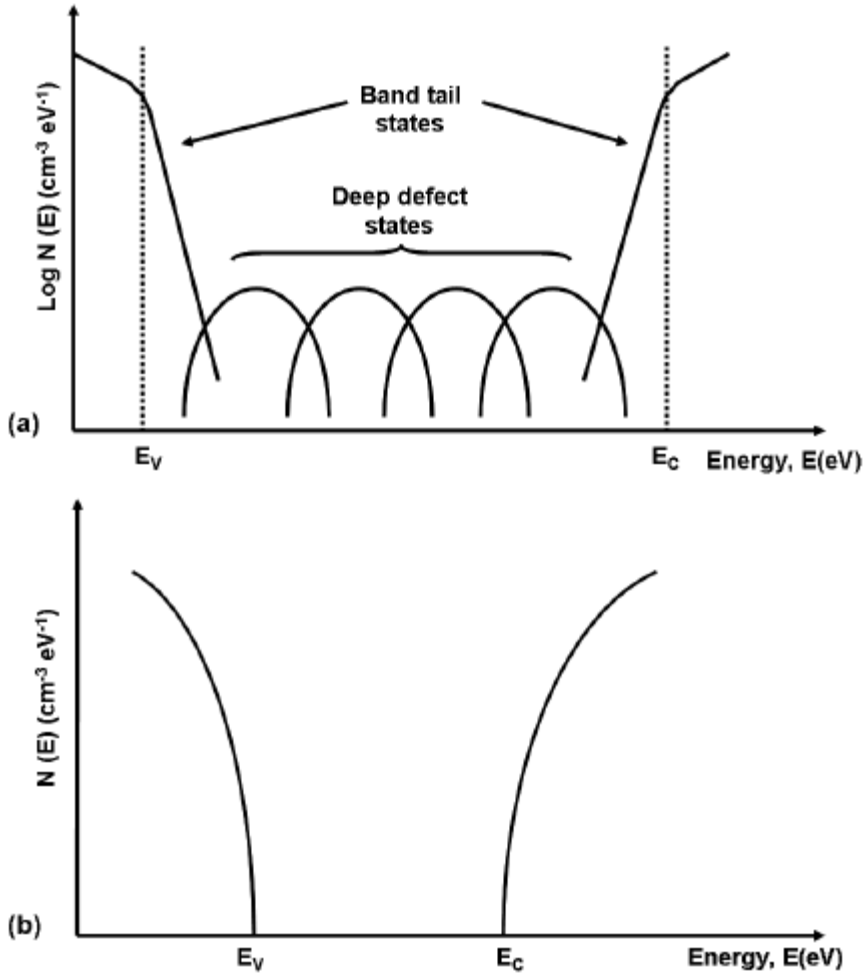


Figure 2.3: a) amorphous silicon Energy band gap diagram and **b)** crystalline silicon band gap diagram [32]

Although the deep states are passivated using hydrogen atoms, a-Si:H material has a field effect mobility (μ_{FE}) is in the range of 0.1-1 cm2/v.s [32]. The low μ_{FE} is attributed to large density of band tail states. The electrons are frequently trapped into and released from band tail states leading to such low mobility. A one dimensional view of electron transport in a-Si:H is presented Figure 2.4 and the equation that models the effective mobility is:

$$\mu_{FE} = \mu_0 \frac{\tau_{free}}{\tau_{free} + \tau_{trap}} , \qquad \textbf{(2.1)}$$

where μ_0 is the band mobility of the electrons without trapping, τ_{free} and τ_{trap} are the time intervals that electrons are free and trapped, respectively.

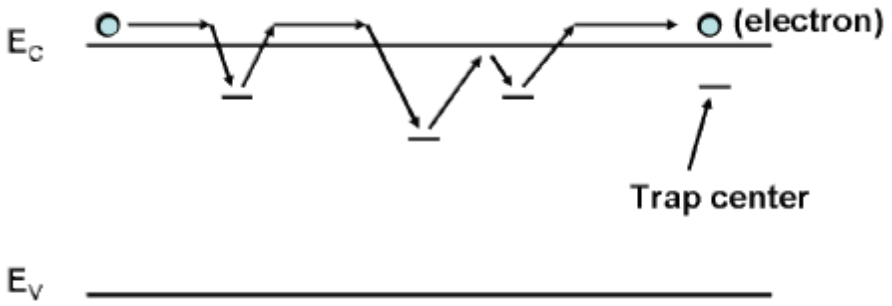


Figure 2.4: One dimensional view of electron trap and released from band tail states [32]

2.2 Device Fabrication

Bottom gate TFT is the current standard for AMLCD. Two types of bottom gate TFT: inverterted coplanar and inverterted staggard [7]. The inverted staggard is the standard process used in the industry as well as University of Waterloo G2N lab for bottom gate TFTs.

There are two process implementations used to fabricated the invertered staggard bottom gate TFT: trilayer and back-channel etch. The devices that were used in our experiments has been fabricated using the BCE process. BCE is the industry standard because it requires 4 masks whereas trilayer needs atleast one extra mask. BCE however requires strong control when the back channel is etched. Lack of control of the back channel etch process may lead to complete etching of the entire a-Si:H active layer. Hence, University facilities such as the G2N lab uses the tri-layer process which has relaxed etching requirements and cost of an extra mask is not of an issue for device prototyping. The following two sections will briefly go over the fabrication of our devices in BCE process. For Trilayer process, see [29].

2.2.1 Back Channel Etch (BCE) Process Dual Gate TFT Fabrication

Figure 2.5 shows a dual-gate TFT cross section schematic that uses BCE process. First a metal layer is deposited, by sputtering on a substrate and patterned to define the gate area (Steps 1 and 2). Then the a-SiNx:H gate dielectric, the a-Si:H undoped and n+ layer are all deposited in one PECVD cycle. Afterwards, metal contact layers are deposited and patterned to make source/drain contacts. These contacts are then used as a mask for etching unwanted areas of the n+ doped layer to separate source and drain terminals. Afterwards, another a-SiNx:H is deposited and patterned to protect the top surface of the active layer exposed during the previous etching step. Specifically for a dual gate TFT, a thick layer of metal was deposited to form the top gate electrode [39]. The dual gate top and bottom metals are shorted using a via as shown in Figure 2.6b. The deposited layers are outlined in **Table 2.1**. Both single gate and dual gate TFTs that were fabcriated all had Channel Length of 4um and Channel widths of 5um, 9um, 300um, 600um, 900um, 1600um, respectively as illustrated in Figure 2.6a.

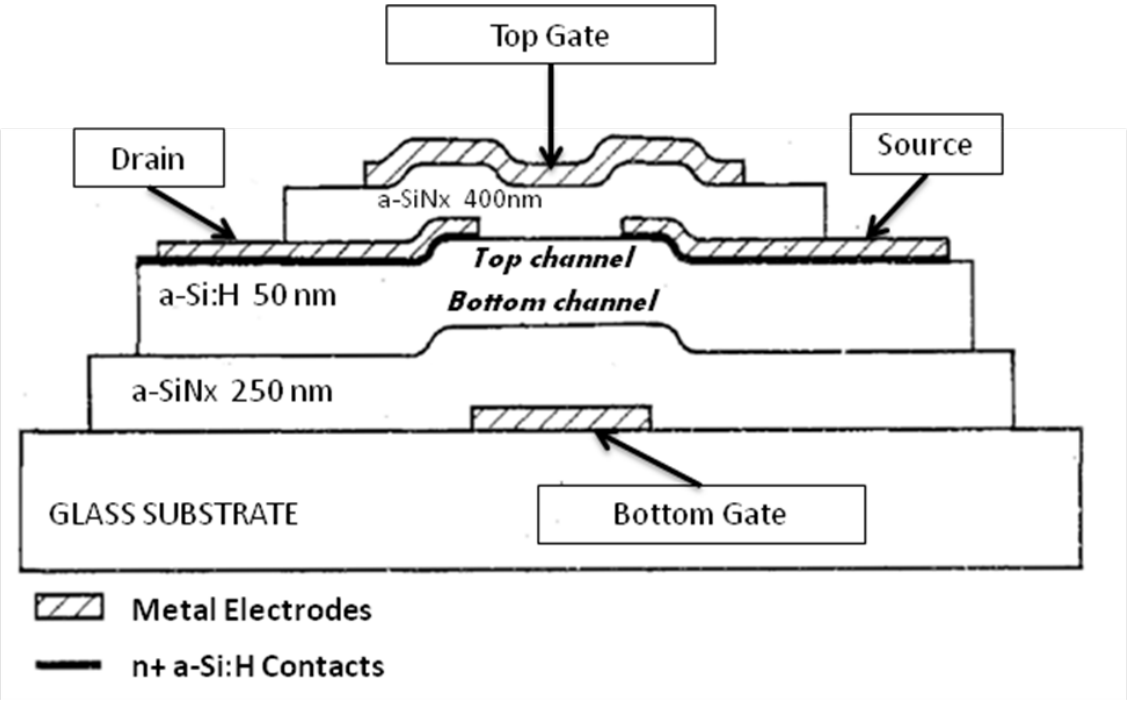


Figure 2.5: A schematic cross section of an inverted staggard dual gate TFT using Back Channel Etch (BCE) process [39]

Table 2-1: Dual gate TFT Process layers and their appropriate thickness

Process Layer	Thickness (nm)
Bottom Gate Metal	200
a-SiNx Bottom Gate Dielectric	250
a-Si:H Active Layer	50
Source and Drain Metal	200
a-SiNx Top Gate Dielectric	400
Top Gate Metal	200
ITO	42

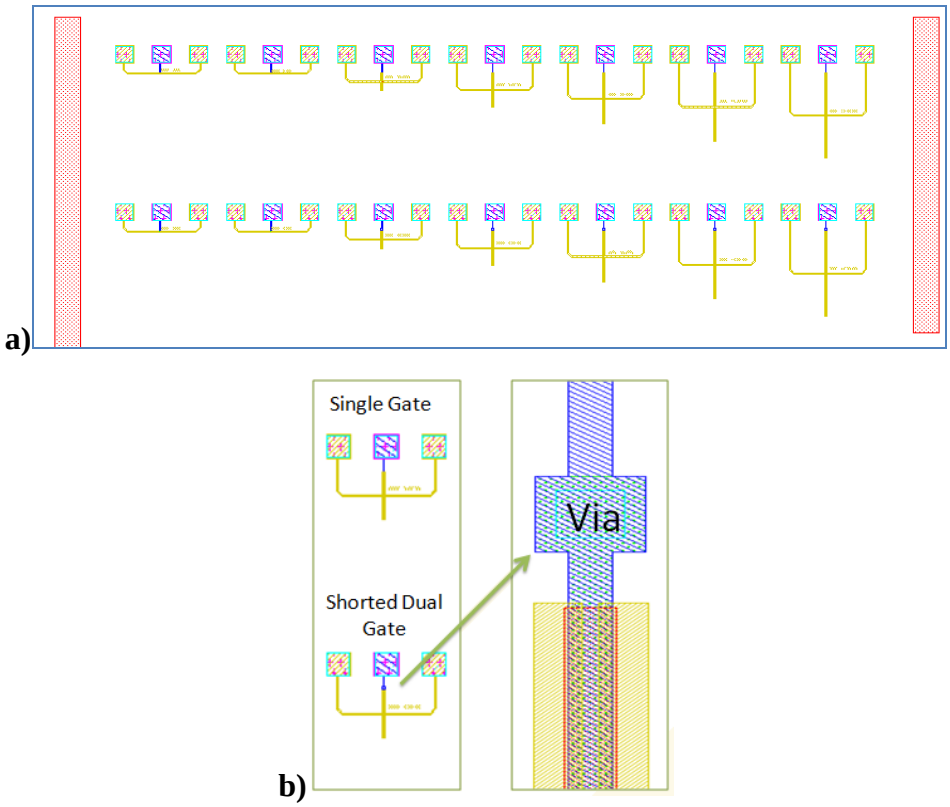


Figure 2.6: a) Top view schematic of fabricated single gate (top row) and dual gate (bottom row) TFTs at Widths of 5um, 9um, 300um, 600um, 900um, 1600um, respectively and **b)** close up capture of the via shorted top and bottom gate for the dual gate TFT

2.3 Dual-Gate TFT Device Operation

2.3.1 Top Channel and Bottom Channel Difference

TFTs generally operate in accumulation mode, while MOSFETs operate in inversion. This is because TFTs use an intrinsic (undoped) layer as an active channel. The transistor type is then determined by the doping of the source/drain contacts, rather than the doping of the semiconductor channel [29]. This is possible only because there is no bulk bias (usually ground) that is found in a bulk MOSFET device.

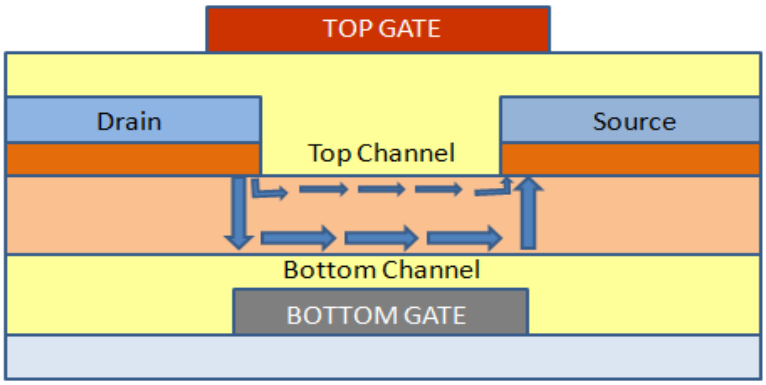


Figure 2.7: Cross section schematic showing current flow in a dual gate TFT

Similarly, a dual-gate TFT operates in accumulation mode. However when both gates are under positive bias, it has been reported to have two conducting channels in the a-Si:H film (Figure 2.7**)** [41], one at the top silicon-silicon nitride interface and one at the bottom interface. Ideally the total drain of a dual-gate TFT should be twice that of a single gate TFT given that both the channels are identical. The two channels in a dual-gate TFT is not identical, although similar. There are three generally three differences between the top and the bottom channels. First of all, the source-drain contacts are in direct contact with the top channel while they are separated from the bottom channel by an undoped a-Si:Hlayer. This means the top channel can conduct like a coplanar TFT, whereas the bottom channel can conduct more current due to its staggard structure Figure 2.8a. Coplanar is when the

Source/Drain is right under the gate and in front of the active layer and Staggard is the opposite. The effect is that staggard can form a slightly larger channel than a Coplanar structure leading to higher current drive Figure 2.8b [5]. Secondly, the bottom silicon-silicon nitride interface was formed ***in situ*** while the deposition of the top silicon nitride layer was interrupted by the fabrication of the source-drain contacts. This could have left some contaminants in the silicon nitride layer, thus affecting the performance of the top channel. Thirdly, the sequence of depositions to form the interfaces was different for the two channels [39]. While the bottom interface was formed by depositing a-Si:H over the silicon nitride, the top interface was formed by depositing silicon nitride over the a-Si:H. Therefore, the top surface of the a-Si:H layer was exposed to the NH,-SiH, plasma at 350°C during the initial deposition of the second silicon nitride layer. This exposure of the a-Si:H to both hydrogen and other energetic species in the plasma might have changed the properties of the a-Si:H near the top interface which can in turn affect the interface properties [39].

Other than the three differences mentioned above, in this experimental case, the top dielectric is twice as thick as the bottom dielectric Table 2-1, which reduces top channel current conduction by 50%.

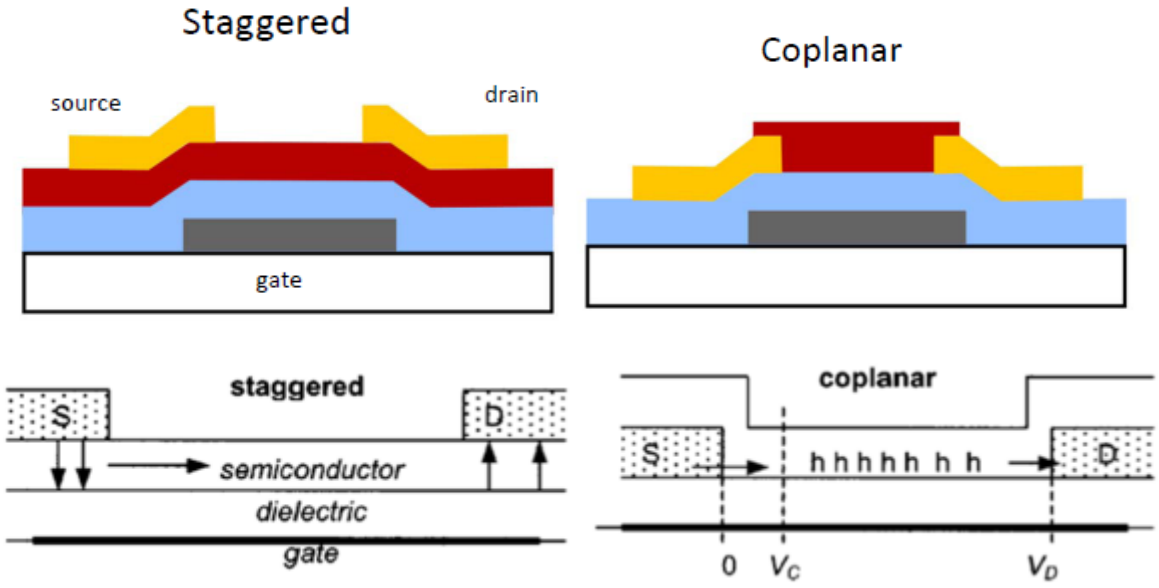


Figure 2.8: a) Inverterd staggard channel formation and **b**) Inverter coplanar channel formation [5]

2.2.2 Single bottom gate TFT Vth and its Physics

TFTs are accumulation devices. This accumulation is not instantaneous like MOSFET due to the high defect states within its band gap. Application of small positive gate bias yields band bending at the interface, but acceptor-like trap states (Qt) above the mid-gap capture most of the free electrons generated as shown in Figure 2.9b [29]. Therefore at a small gate bias, the conduction band is not close enough to the Fermi level to provide enough free carrier for a conducting channel. For a large enough gate bias, the Fermi level becomes close enough to the conduction band, providing enough free carrier to create a channel for S/D current conduction. This gate bias is also referred to as the threshold voltage (Vt). The formula for Vt for an ideal (no interface charges) single-gate TFT is given as:

$$V_t = q\aleph_T t_s \frac{(E_f - E_i)}{C_i}, \tag{2.2}$$

where q is charge, $\aleph_T$, is trap density in units of ($cm^{-3}eV$), t_s is the silicon thickness and $(E_f - E_i)$ is the Fermi level difference from midgap. This formula is valid for thin silicon films where band bending is considered negligible.

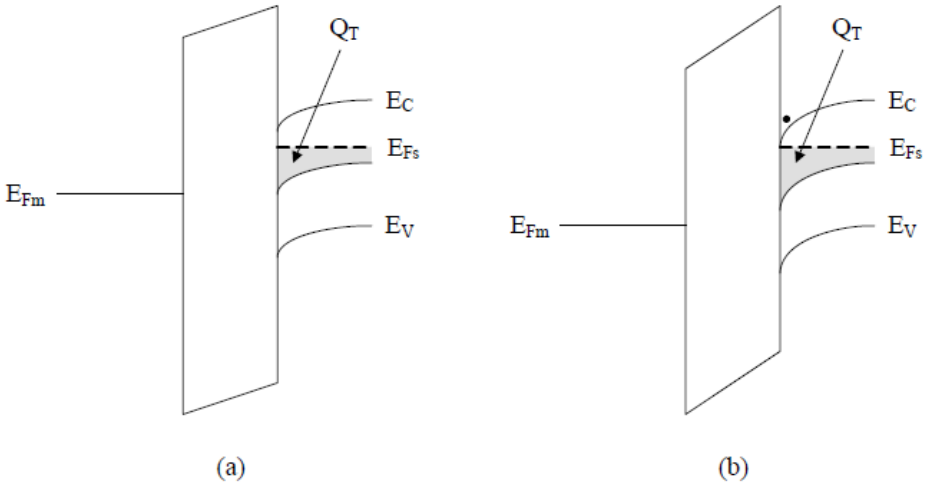


Figure 2.9: a) Band diagram of a-Si:H TFTs with high channel trap states. a) band bending due to small positive gate bias that leads to most of the free electron being captured, and **b)** larger positive gate bias leading enough band bending to have sufficient free electrons in the conduction band (or band tail) [29]

According this equation, threshold voltage depends on the trap density, Nt and active layer thickness, ts. The equation can be summarized as being the voltage required to fill all the trap states present in the entire silicon depth (thickness) so a channel can be formed at the surface.

If you take non-idealities into consideration such as the metal to semiconductor work function mismatch, insulator charge and more importantly interface charges, the threshold voltage equation becomes:

$$V_t = q\aleph_T t_s \frac{(E_f - E_i)}{C_i} + qD_{itb}\frac{(E_f - E_i)}{C_i} + qD_{itt}\frac{(E_f - E_i)}{C_i} + \frac{Q_i}{C_i} + \emptyset_{ms} \quad , \qquad \textbf{(2.3)}$$

where, D_{itb} and D_{itt} are the interface trap sites at the bottom and top interfaces respectively, also in ($cm^{-3}eV$), Q_i and C_i are the insulator charges and capacitance respectively and $\emptyset_{ms}$ is the metal to semiconductor work-function difference.

The interface traps at the top channel, D_{itt} has been reported to be 10 times larger than bottom channel interface charge,D_{itb} [36].

2.3.2 Dual Gate TFT Threshold Voltage

If both the channels in a dual gate TFT were identical, it would require half the voltage to fill the trap states, $\aleph_T$, considering the lowest E-Field would be at the middle of the a-Si:H layer. This leads to $V_{tdual} = V_{tsingle}/2$. However, the fabrication process makes the dual gate top and bottom channels asymmetric, giving each their own threshold voltage. Although the top and bottom channels have different threshold voltages, the top gate bias has an effect on the bottom gate bias, which is as follows:

$$V_{tb} = V_{tbo} - \beta V_{GT} \quad , \qquad \textbf{(2.4)}$$

where V_{Tb} is the bottom channel threshold voltage, V_{Tbo} is the bottom channel threshold voltage when the top gate is biased zero, β is the bottom channel threshold voltage sensitivity constant with respect to the Top Gate and V_{GT} is the Top Gate bias. β is an empirical value that can be extracted by V_{Tb} measurements using various V_{GT} biases. This was not possible with our devices because separate bottom and top gate electrodes are needed. All our dual

gate devices had top and bottom gate electrodes shorted (Figure 2.6b). The value of β has been characterized by Peyman as the following:

$$\beta = -\frac{dV_{tb}}{dV_{GT}} \approx \frac{C_{it}}{C_{ib}} \frac{C_s}{C_{it} + C_s + C_{sst}}, \quad \textbf{(2.5)}$$

where C_{it} and C_{ib} are the top and bottom gate insulator capacitances (F/cm^2), respectively, C_s is the a-Si:H layer capacitance, and C_{sst} is the effective top a-Si:H/a-SiN$_x$:H interface capacitance where $C_s = \frac{\epsilon_s}{t_{si}}$ and $C_{sst} = q^2 D_{sst}$, respectively. D_{sst} is the density of states at the top interface and has been reported to be $\approx 3x\ 10^{12}\ /cm^2 eV$. β has been reported to be 0.15.

If the top and bottom channels were identical, then $V_{tt} = V_{tb}$. As discussed in section 2.3.1, the channels has some differences that need to be accounted for in their unique threshold voltages. Therefore, the top gate threshold voltage is as follows:

$$V_{tt} = V_{tto} - \alpha V_{GB}, \quad \textbf{(2.6)}$$

where V_{tt} is the top channel threshold voltage, V_{tto} is the top channel threshold voltage when the bottom gate is biased zero, α is the top channel threshold voltage sensitivity constant with respect to the Bottom Gate and V_{GB} is the Bottom Gate bias. α is an empirical value that can be extracted by V_{Tb} measurements using various V_{GT} biases.

$$\alpha = -\frac{dV_{tt}}{dV_{GB}} \approx \frac{C_{ib}}{C_{it}} \frac{C_s}{C_{ib} + C_s + C_{ssb}}, \quad \textbf{(2.7)}$$

where C_{it} and C_{ib} are the top and bottom gate insulator capacitances (F/cm^2), respectively, C_s is the a-Si:H layer capacitaces, and C_{sst} is the effective top a-Si:H/a-SiN$_x$:H interface capacitance where $C_s = \frac{\epsilon_s}{t_{si}}$ and $C_{ssb} = q^2 D_{ssb}$, respectively. D_{ssb} is the density of states at the bottom interface and has been reported to be $\approx 3x\ 10^{11}\ /cm^2 eV$. Since in our experiment the top channel dielectric is twice as thick as the bottom channel, $C_{ib} = 2C_{it}$. Furthermore, using values of density of states, we get $D_{sst} = 10 D_{ssb}$. The net result is that:

$$\alpha \approx \frac{\beta}{20}, \quad \textbf{(2.8)}$$

given that $\beta = 0.15$, $\alpha = 0.0075$ for our devices, making it very negligible.

In order to get either βor α, a dual gate TFT with separated electrode is required and therefore is not extracted for this thesis. However, this relationship is needed to establish the current conduction equation for the dual gate TFT in the next section.

2.3.3 Dual Gate TFT Above Threshold Current Conduction

Given that the top and bottom channel currents, the ideal current conduction in a single gate TFT is as follows [29]:

$$I_{D-dual} = 2\,C_i\left(\frac{W}{L}\right)u_{fe}\left[(V_{GS}-V_t)V_{DS}-\frac{{V_{DS}}^2}{2}\right] \quad \text{when} \quad V_{DS} < V_{GS}-V_t \tag{2.9}$$

$$I_{D-dual} = C_i\left(\frac{W}{L}\right)u_{fe}(V_{GS}-V_t)^2 \quad \text{when} \quad V_{DS} > V_{GS}-V_t \tag{2.10}$$

where V_{GS} is gate to source voltage and $V_{DS}$is drain to source voltage. This is simply an addition of current from the two channels.

Given the difference between the two channels, the current equation becomes:

$$I_{D-dual} = C_{ib}u_{feb}\left(\frac{W}{L}\right)\left[(V_{GS}-V_{tb})V_{DS}-\frac{{V_{DS}}^2}{2}\right]+C_{it}u_{fet}\left[(V_{GS}-V_{tt})V_{DS}-\frac{{V_{DS}}^2}{2}\right], \tag{2.11}$$

when $V_{DS} < V_{GS}-V_t$, and

$$I_{D-dual} = \frac{1}{2}C_{ib}u_{feb}\left(\frac{W}{L}\right)(V_{GS}-V_{tb})^2+\frac{1}{2}C_{it}u_{fet}\,(V_{GS}-V_{tt})^2, \tag{2.12}$$

when $V_{DS} > V_{GS}-V_t$ and u_{feb} and u_{fet} are mobility in the bottom and top channel respectively. They have been reported to be different because of their dependence on the interface quality.

Dual gate essentially is a superposition of the top and bottom gate except for one factor. The only difference here is that the threshold voltage of each channel will be decreased due to the electric field from the opposite gate by a factor of beta. Hence the total dual current is accounted to be a little bit more than the exact super position of the top and bottom gate as reported by [39] but never explained.

Next section will show drive current and I-V curves of our fabricated single and dual gate TFTs with some discussion to explain the results.

2.3.4 Drive Current Results and Discussion

Drive current measurement is basically drain current measurement while sweeping the drain voltage, while having set the gate voltage at a static value (V_{GS} = 0V, 5V, 10V, 15V). We have measured both single and dual gate TFTs of Widths of 5um, 9um, 300um, 600um, 900um, 1600um. We then divided each TFT with their own width to get current drive per unit width. Figure 2.10 shows the average current drive of both single and dual gate TFTs with error bars. The average drive current is again plotted in Figure 2.11 for comparison. It confirms that dual current has superior drive current and agrees with all [35][39][40][41]. The gain of the dual gate current over the single gate current is about 20% for Vgs of 5V, 10V, 15V as shown in Figure 2.12. Due to the top channel dielectric being two times that of the bottom channel, the total current gain is already cut in half (50%), the rest of the 30% is attributed to top channel interface and the coplanar structure. Separated gate electrode dual gate TFT is needed to properly characterize the current gain to see how much of the current is coming from the top channel and how much is contributed by the reduced threshold voltage due to top gate bias.

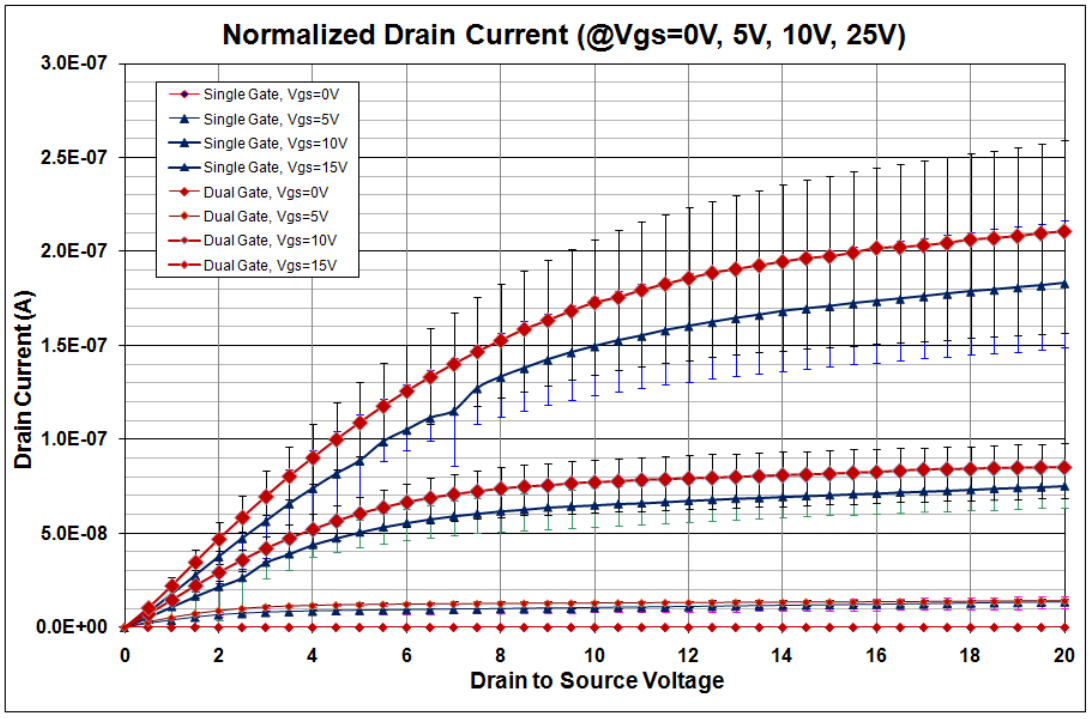


Figure 2.10: Normalized Drain Current for Vgs = 0V, 5V, 10V and 10V with error bars

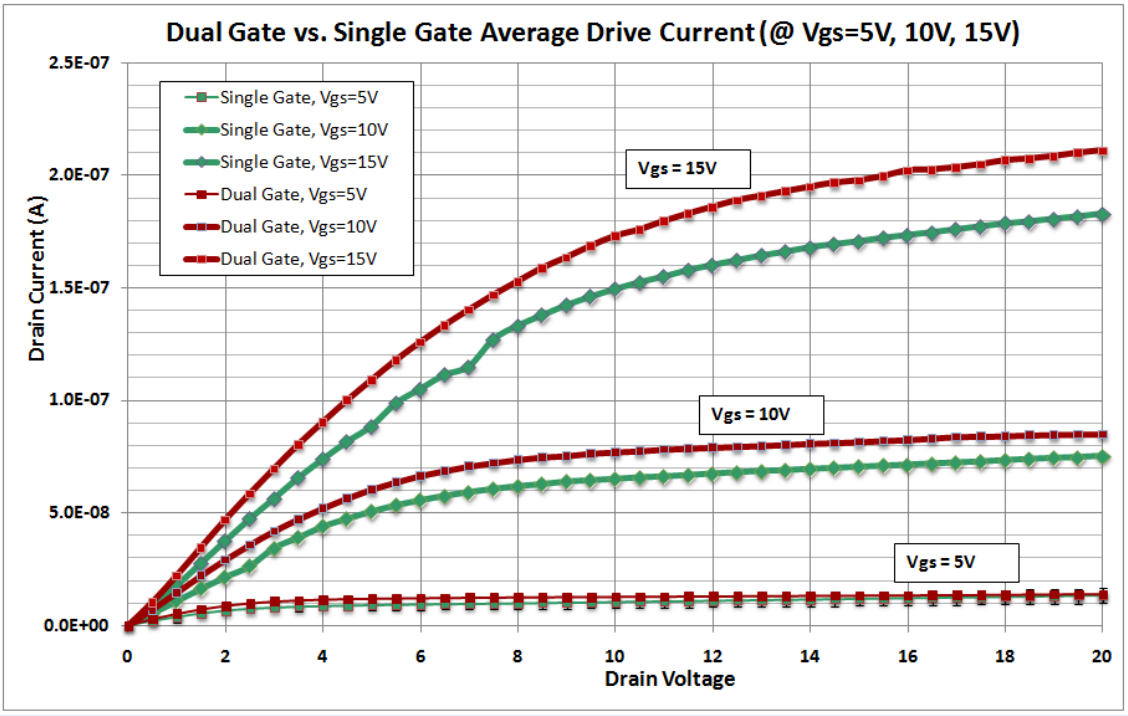


Figure 2.11: Average Dual Gate and Single Gate Drain Current

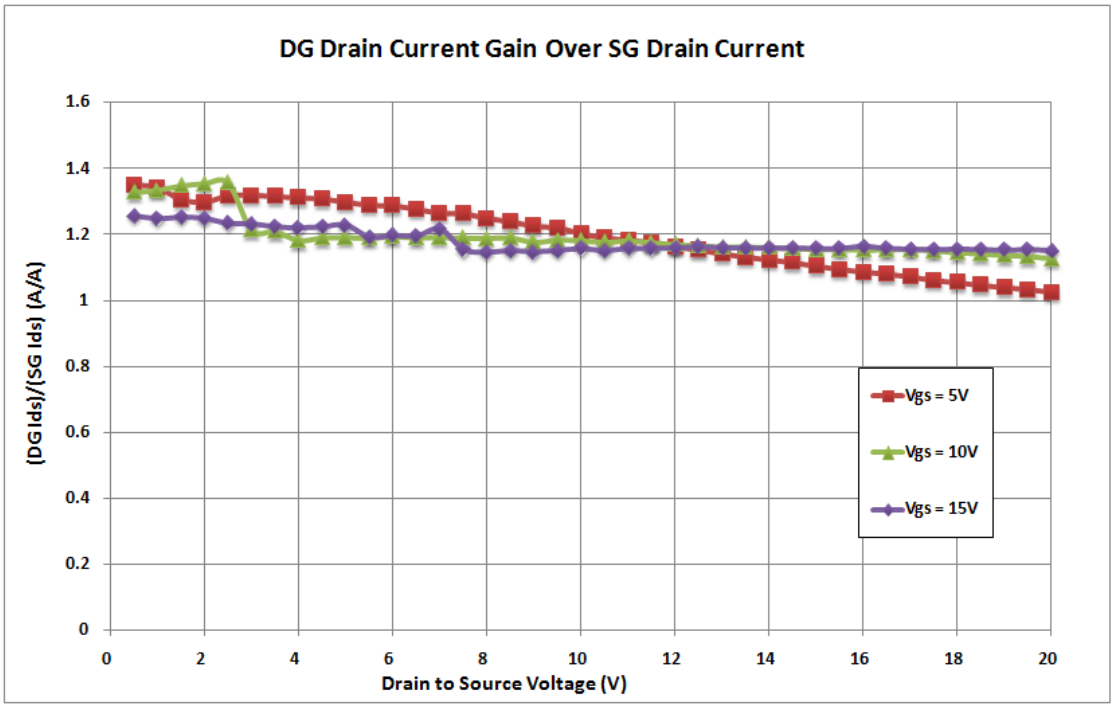
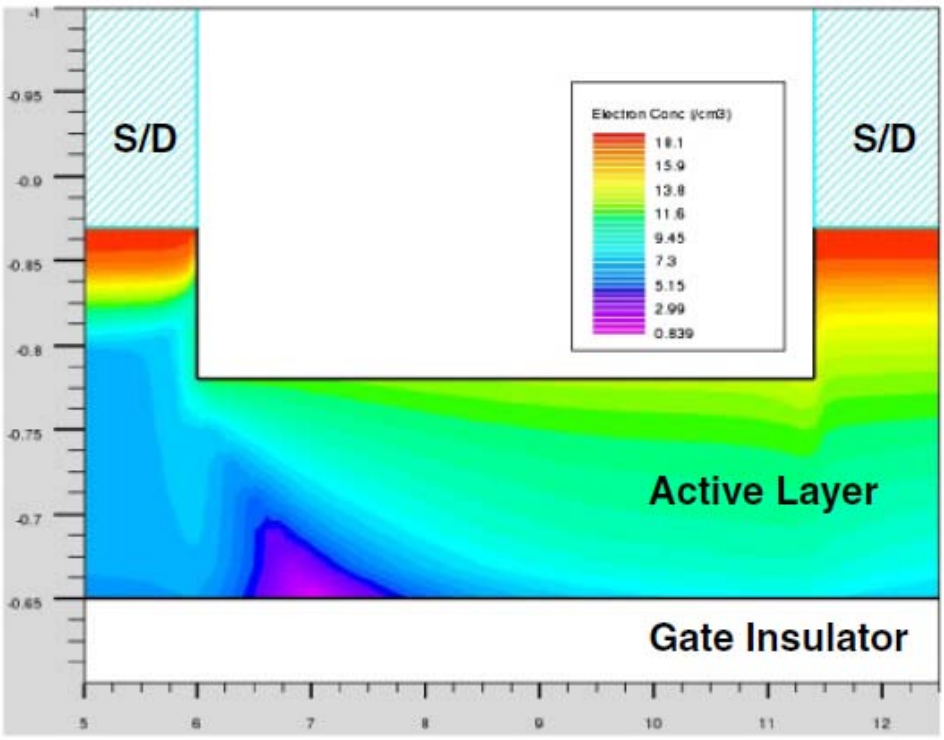


Figure 2.12: Average Dual Gate TFT drain current gain over Single Gate TFT

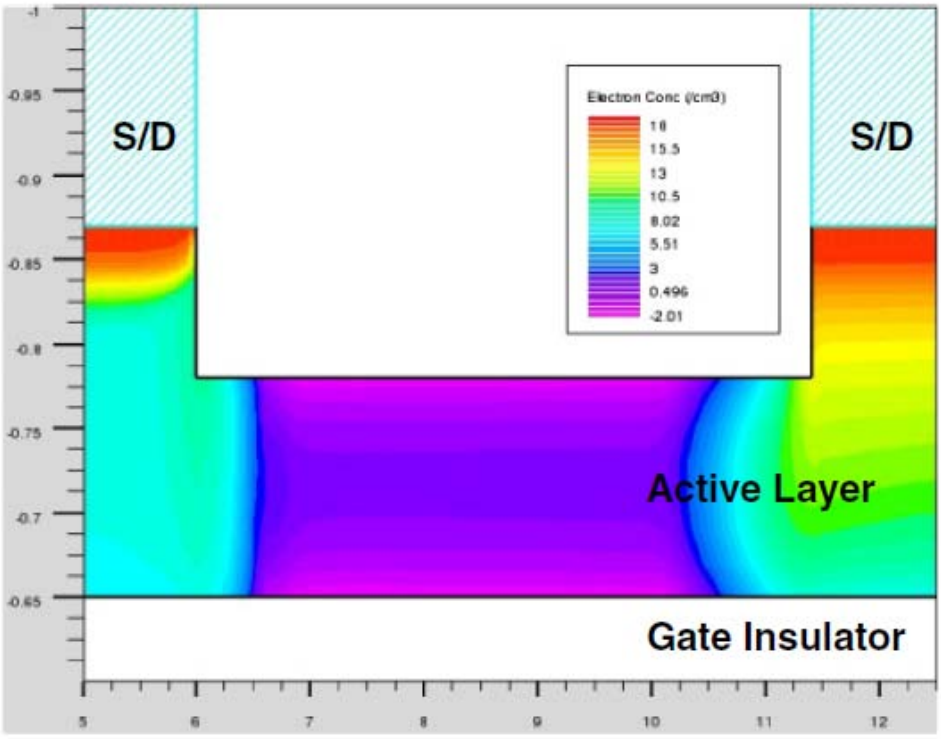
2.3.5 Leakage Current

Leakage Current measurement is done by applying 0V bias to the gate and source, then sweeping the drain voltage and measuring the drain current. The leakage current for a single gate TFT is suitable for AMLCD and AMOLED displays. However, when it comes to low power electronics such as a Smartphone, smaller leakage current means a longer standby life time due to reduced standby power consumption.

Leakage current in a single bottom gate TFT is known as sub-threshold current and is attributed to electron current conduction at the top interface. Having a top gate bias of 0V leads to a lower electron accumulation in the top interface (Figure 2.13 [41]) allowing less leakage current conduction compared to a single gate TFT. Our measurements in **Figure 2.14** confirm that. To compare, we did a current gain graph (Figure 2.15) where we show that the dual gate has about 25% leakage current compared to a single gate TFT. This is given the fact that the top insulator is 400nm thick. If the top interface is optimized to 200nm, then the leakage current is expected to be less in the dual gate TFT.



a)



b)

Figure 2.13: Simulation of electron density in **a)** single gate, and **b)** dual gate TFT [41]

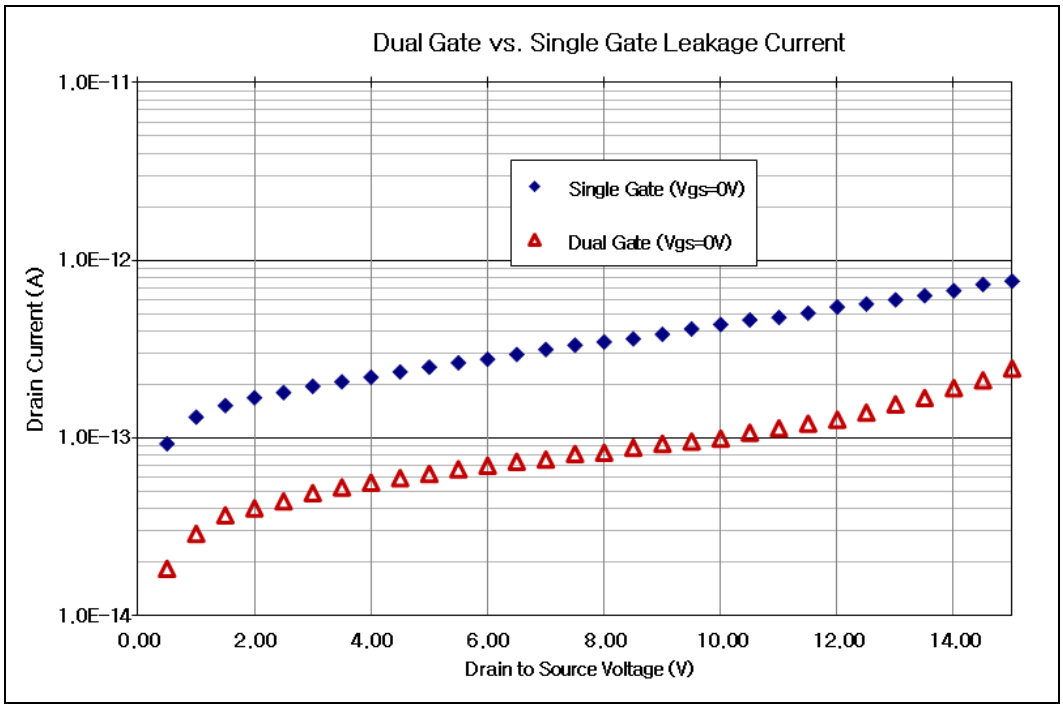


Figure 2.14: Single Gate and Dual Gate TFT leakage current

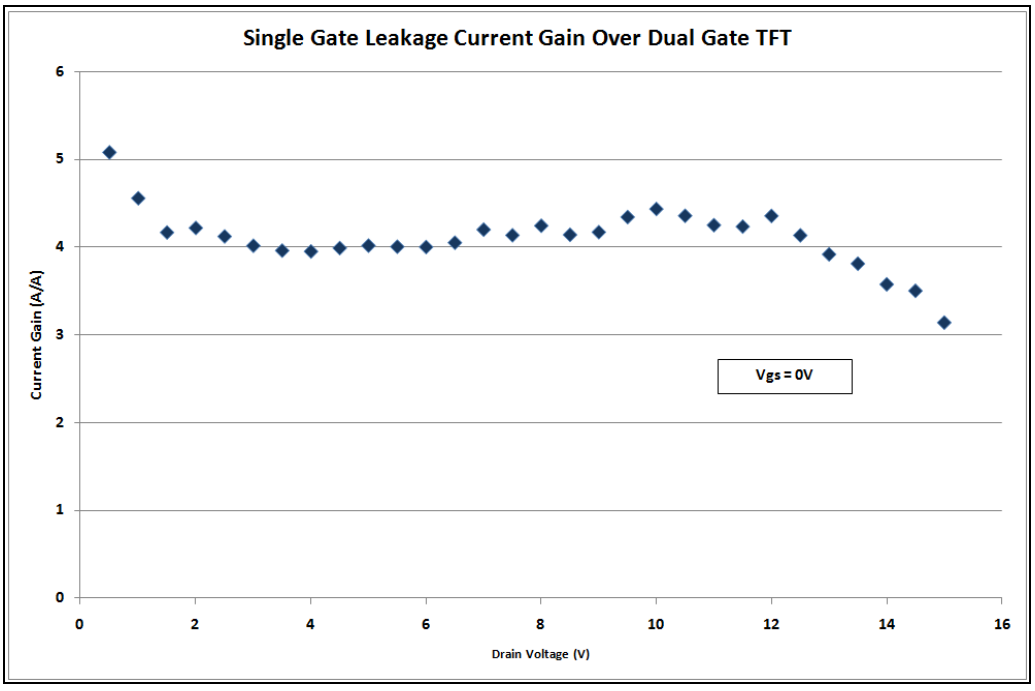


Figure 2.15: Single Gate leakage current gain over a Dual Gate TFT leakage current

2.3.6 Dual Gate and Single Gate Transfer Characteristics

Figure 2.16 shows the I-V transfer characteristic of both dual and single gates at drain voltages 5V and 10V in log scale. The transfer characteristics have same sub-threshold slope and threshold voltage of 1.3V. The threshold voltage for a dual gate TFT is the same as a single gate TFT when both the dual gate TFT is shorted (Figure 2.17b [40]). The sub-threshold slope is expected to be significantly higher for the dual gate TFT because it's turning on from a lower leakage current to a higher drive current than a single gate TFT. Such low sub-threshold slope may be due to the thick top dielectric causing negligible top gate E-field impact when creating the top channel. Further characterization is needed for TFT's with thicker dielectric and separated electrode to understand top gate impact towards the sub-threshold slope. A summary of device parameters are presented in Table 2-2.

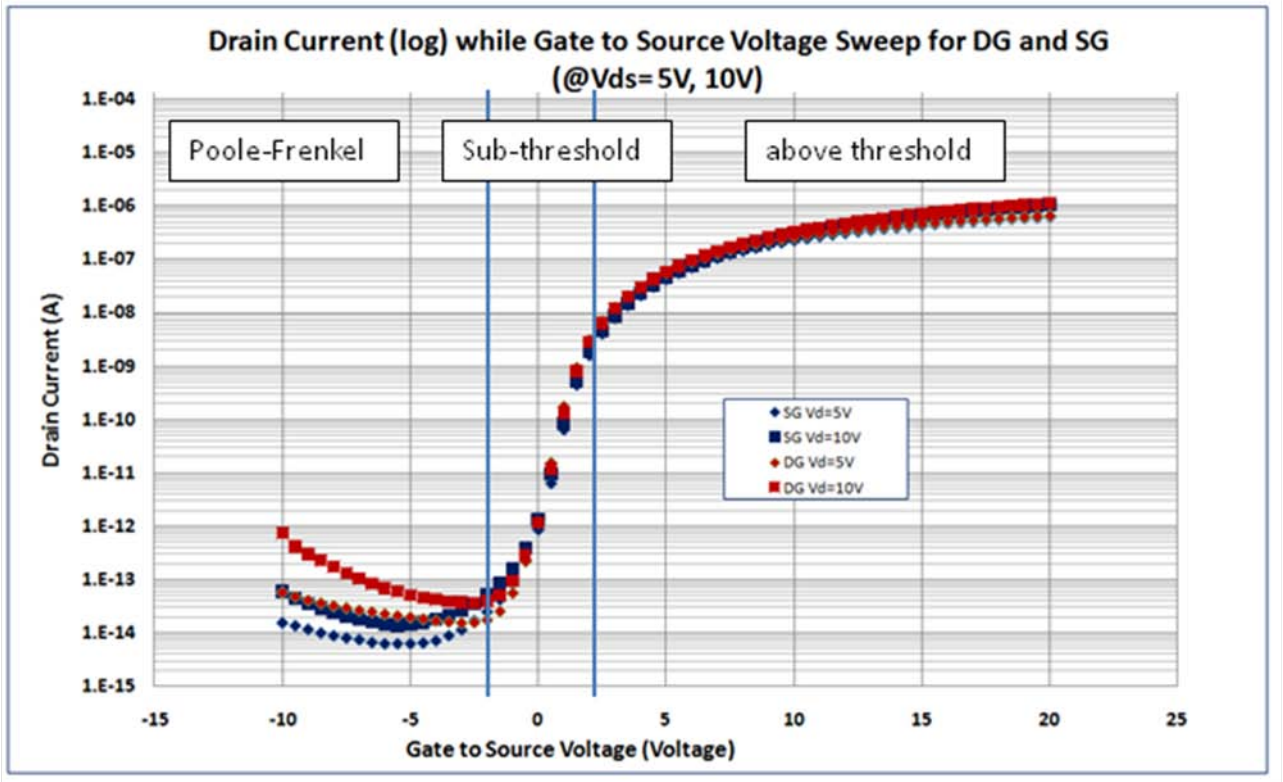


Figure 2.16: Single and Dual Gate I-V curve at drain voltages of 5V and 10V

Table 2-2: Dual Gate and Single Gate TFT parameters at Drain Voltages of 5V and 10V

TFT Type	Threshold Voltage (Vt)	Inverse Sub-threshold Slope (S) (mV/dec)	On/Off Ratio (Ion/Ioff)
Single (Vds=5V)	1.3	386	30.1 x10^6
Dual (Vds=5V)	1.3	352	31.1 x10^6
Single (Vds=10V)	1.3	368	37.5 x10^6
Dual (Vds=10V)	1.3	352	43.3 x10^6

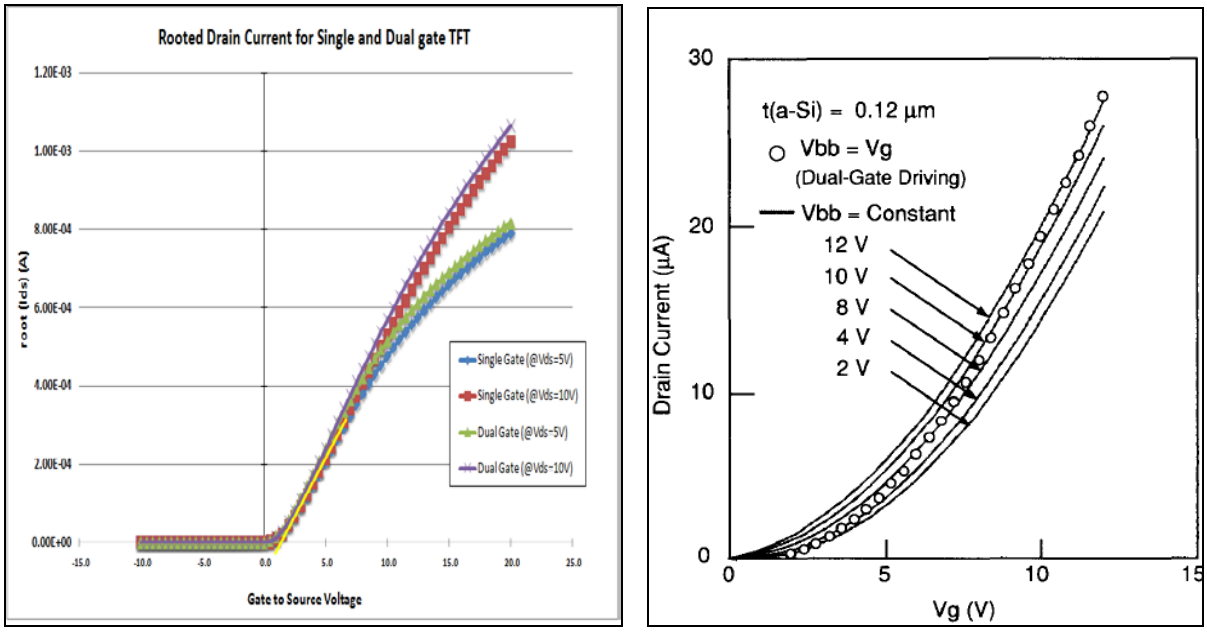


Figure 2.17: a) Threshold voltage extraction (yellow line) from a root drain current graph for both Dual gate and Single Gate TFTs, and **b)** previous work showing that shorted dual gate TFT turn on at the same voltage as a single gate TFT [40].

2.3.7 Poole Frenkel Current

In section 2.3.5, we have attributed leakage current to back channel electron conduction at a gate voltage of 0V. If the gate voltage is decreased low enough, the drain current increases exponentially with respect to decreased gate voltage. This region is known as Pool Frenkel as illustrated in **Figure 2.16**.

According to Peyman, Poole Frenkel emission occurs due to emission of electrons from valence band to conduction band at the drain depletion region that is located between drain and gate overlap area. This emission is field assisted and trap assisted causing a lower requirement of activation energy for a-Si:H TFTs where numerous traps exist in the semiconductor unlike its MOSFET counterpart. Poole Frenkel emission is also attributed to the emission of trapped electrons in the deep defect state during accumulation. This Poole Frenkel emission model is visualized in Figure 2.18 for low, medium and high negative gate voltages.

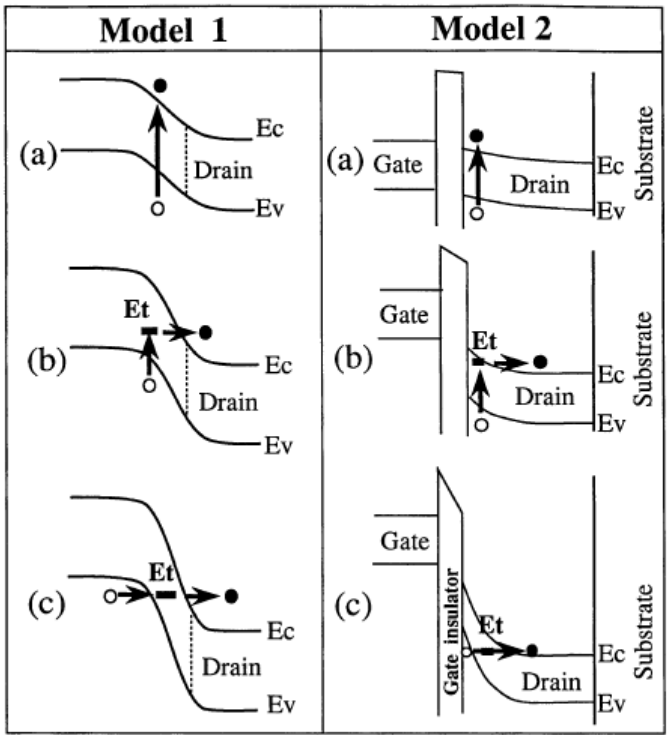


Figure 2.18: Band diagrams for two models illustrating Pool-Frenkel current where **a)** is for weak E-field, **b)** is for medium E-field and **c)** is for high E-Field [54]

Poole Frenkel current density, J_{pf}, is goverened by the following equation [36]:

$$J_{pf} = J_{pf0} e^{\sqrt{\left| E_{Si} / E_{pf} \right|}}, \tag{2.13}$$

where E_{Si} and E_{pf} electric field applied and electric field coefficient, and J_{pfo} is the effective Poole-Frenkel current when the electric field is zero.

The total Pool-Frenkel current is dependant on the gate to drain overlap region. Therefore the total Poole Frenkel current equation is [36]:

$$I_{DS} = W\ OL_D\ J_{pf} = W\ OL_D\ J_{pf0} e^{\sqrt{\left| E_{Si} / E_{pf} \right|}}, \tag{2.14}$$

where W and OL_D are the width and gate/drain overlap of the TFT. Since Poole-Frenkel current depends on the gate to drain overlap, a dual-gate TFT conducts higher current at negative gate bias than a single gate TFT (Figure 2.19).

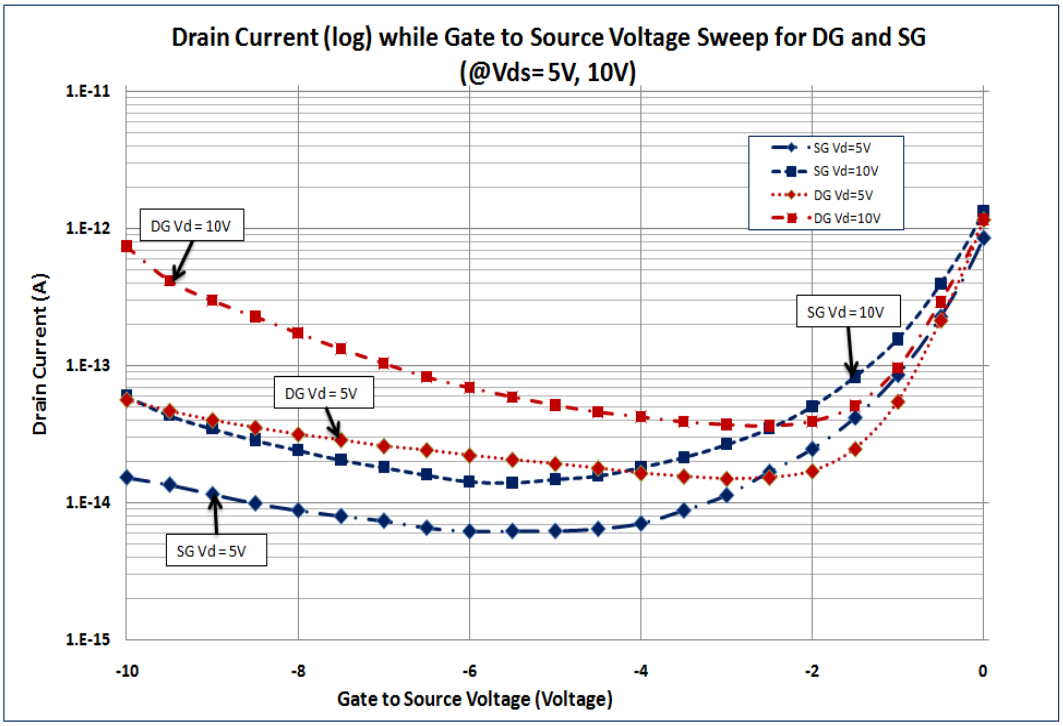


Figure 2.19: Poole-Frenkel current conduction for both dual (red) and single (blue) gate TFTs

Now besides the fact that the dual gate TFT conducts higher drain current in the Pool Frenkel region, another important characteristic to notice here is that the Poole Frenkel region starts earlier in a dual gate TFT. This means that the E_{si} is higher due to the electric field coming from both top and bottom side of the drain which accelerates the Poole-Frenkel effect at a lower negative gate bias than a single gate TFT. **Figure 2.20** shows the Poole Frenkel current gain of a dual gate TFT over a single gate TFT. Notice that the gain stabilizes at gate to source voltages lower than -6V. At this voltage is when both the TFT goes into Pool-Frenkel conduction. Gain is constant in this case perhaps because the width and gate to drain overlap dimentions are constant and is the dominant variable for Poole Frenkel current equation (**2.14**).

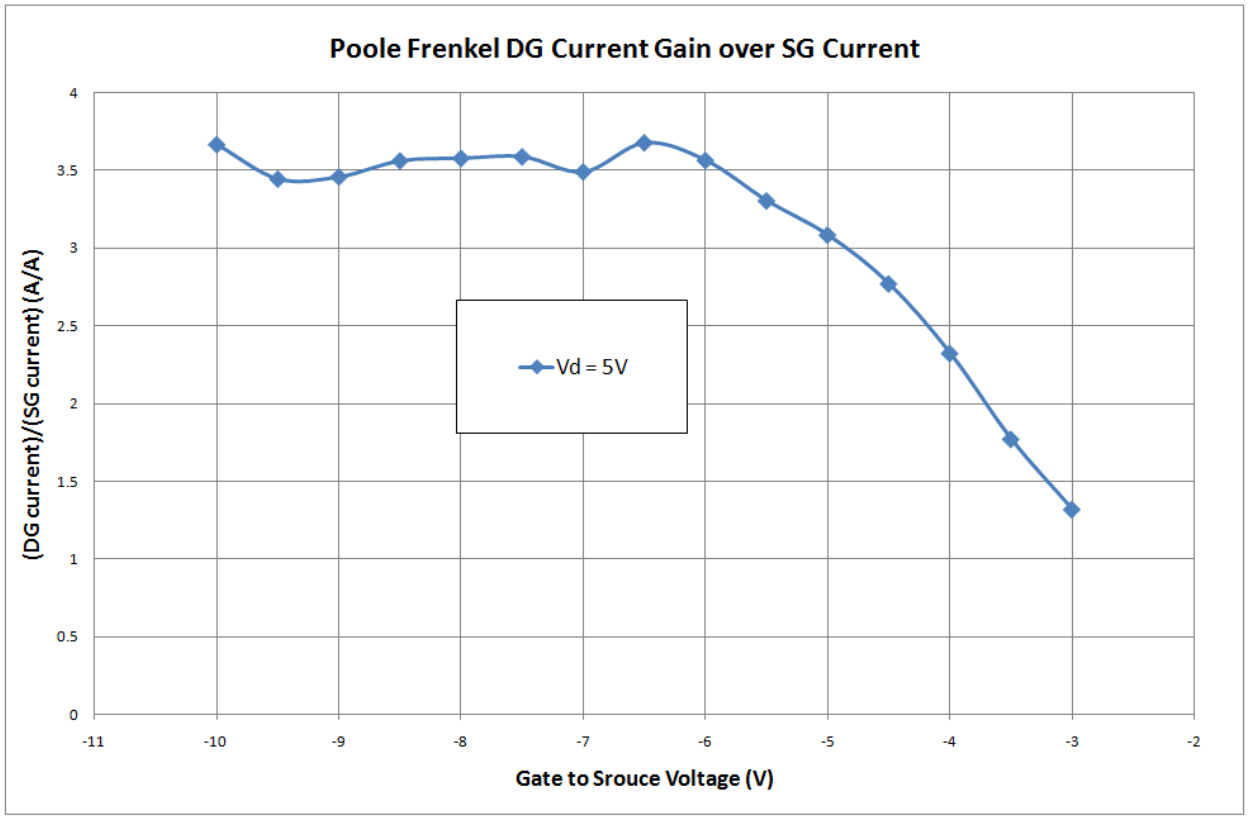


Figure 2.20: Dual Gate Poole-Frenkel current gain over Single Gate Poole-Frenkel Current

2.4 Summary and Future Work

In this chapter we showed a relationship of reduced threshold voltage due to the back gate bias with a sensitivity factor of β and α, for bottom and top channel respectively. We used this to explain drain current for a dual gate. Our measurements showed 20% more superior dual gate current drive capability by the usage of an extra top channel. We have recognized device parameters such as top gate insulators that can be changed to improve the dual current drive capability by 80% more than a single gate current. We have also showed dual gate leakage current to be 25% of single gate due to back channel electron depletion. Finally we looked at enhanced Poole-Frenkel current conduction due to dual overlap of gate and drain current. For low bias of 5V, we showed a constant current gain of 3.5 in dual gate compared to a single gate Poole-Frenkel current.

Future work would include fabricating new devices that have separated gate electrodes, more optimized back channel interface passivation, and optimized gate insulator thickness. For this, new mask designs have been completed as shown in Figure 2.21 and Figure 2.22. The following became new areas of interest in the new dual gate TFTs:

- Various length to extract source and drain contact resistance
- Various gate to drain overlap lengths to study its effect Poole-Frenkel region
- Top interface treatment and their effect on threshold voltage and stability
- C-V measurements to see whether this TFT is fast enough for today's TV frame speed

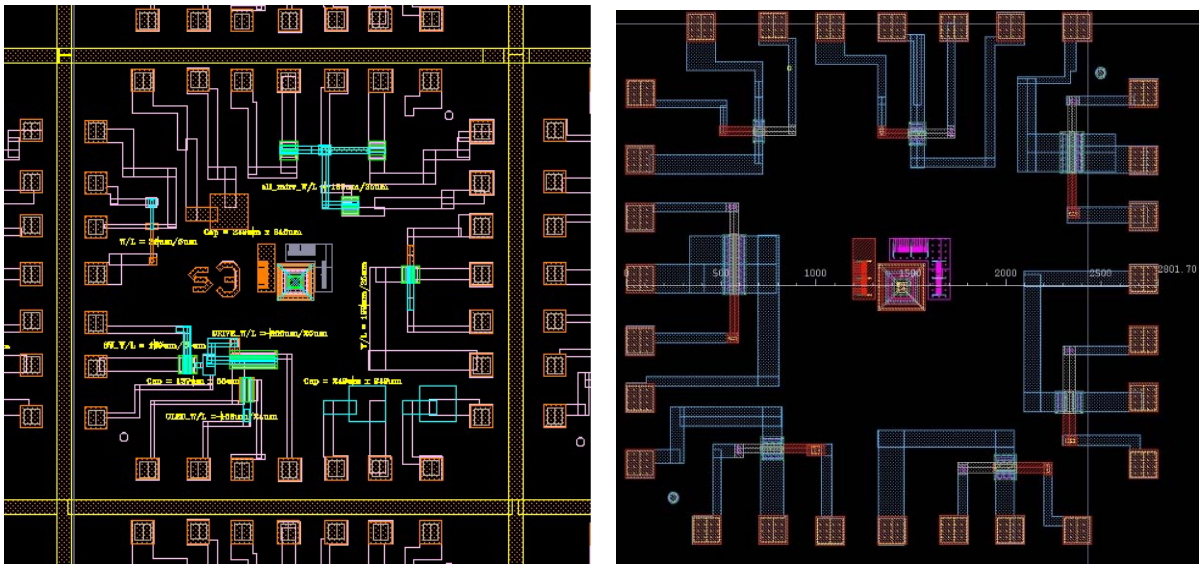


Figure 2.21: Mask design of new Dual Gate TFTs using Cadence Virtuoso CAD tool

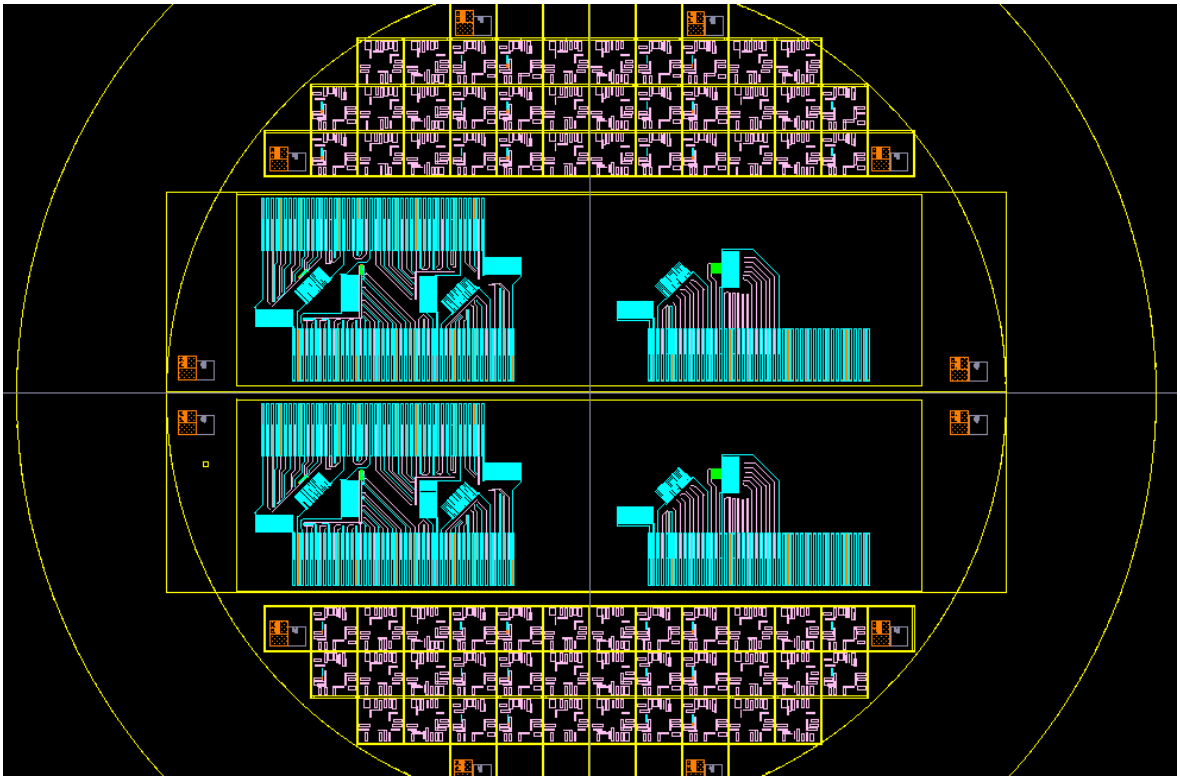


Figure 2.22: Full wafer mask design

Chapter 3

a-Si:H TFT Dominant Instability Mechanism and Improvements

The goal of this chapter is to show the superior stability of dual gate TFTs compared to single gate TFTs. The instability of the a-Si:H TFT under electrical bias is a very challenging obstacle that prevents its implementation in OLED backplanes. For this reason, understanding the mechanisms behind its stability is important for optimizing devices for such applications.

TFT instability refers the shift in the threshold voltage that occurs under electrical bias. For positive gate bias, the threshold voltage increases, thus gradually decreasing the drive current over time for the same gate bias. The reduced current dims the OLED that it is driving, causing OLED display degradation.

The threshold voltage instability mechanisms have been modeled using two theories: defect state creation in the a-Si:H active layer, which increases N_T; and charge trapping in the gate dielectric, which increases Q_i. Although it is agreed upon that both of these theories simultaneously affect the threshold voltage shift for a-Si:H devices, the interest lies in finding the mechanism that plays a dominant role in threshold voltage shift [48-53].

3.1 Defect State Creation in Amorphous Silicon

Unlike VLSI devices that are fabricated around 1000ºC, the low thermal budget for a-Si:H limits fabrication temperature to 300ºC. Due to the low temperature process, the a-Si:H contains many dangling bonds and weak silicon to silicon bonds that contribute to deep defect states and broad band tails, respectively illustrated in Figure 2.3a. Hydrogen gas is added to passivate some of the dangling bonds to eliminate the deep defect states. Regardless, when an accumulated channel is formed in the TFT to allow current conduction from drain to source, the band tail carriers start to experience frequent trapping and release

events as mentioned in Figure 2.4. During this interaction, the weak silicon to silicon bonds are broken, increasing the deep defect states. Defect states, $\aleph_T$, have a direct relation with the threshold voltage as shown in Equation (**2.2**). Therefore, increased defect states increase threshold voltage which reduces the drive current of the TFT. Furthermore, increase in $\aleph_T$ also degrades the sub-threshold slope of the TFT [29].

The most widely accepted model for defect state creation states that when a weak silicon to silicon bond is broken to form two dangling bonds, a hydrogen atom diffuses to 'plug' one of the dangling bonds (Figure 3.1) [32][37][48]. Furthermore, it is widely accepted that defect state creation is temperature dependant. Hence, electrical stress tests under different temperatures yield different $V_{t-shift}$ if the dominant mechanism is defect state creation if.

The shift in V_t is reversible by annealing at temperatures around 150°C for about two hours to obtain the initial transfer characteristics. It is reported that the $V_{t-shift}$ is reversible at room temperature over a period of 1-2 years [32].

Defect state creation has been experimentally found to be the dominant mechanism of $V_{t-shift}$ at lower gate bias (ie: 25V or less) [49][53]. Charge trapping in the silicon nitride has been observed to occur during high gate bias given that the nitride few defects (good quality).

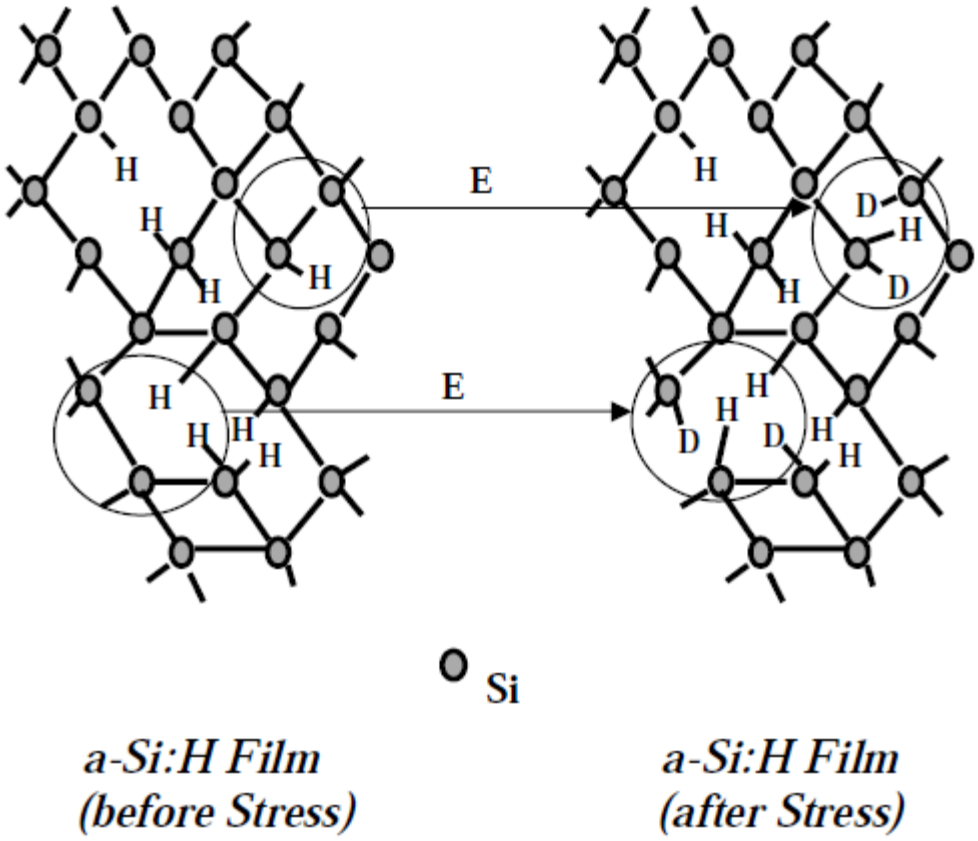


Figure 3.1: Atomic structure of a-Si:H film before and after stress, where D and H denote the dangling bonds and hydrogen atoms respectively. E – represents the weak Si-Si bond breaking associated with Hydrogen motion. [54]

3.2 Charge Trapping in Silicon Nitride Dielectric

Charge trapping leading to $V_{t-shift}$ arises due to the accumulated injection and trapping of channel electrons into the silicon nitride dielectric. The trapped electrons act as a shield against the applied gate voltage, thus increasing the threshold voltage. The mechanisms behind charge injection are explained using various models. These models, which are respectively illustrated in Figure 3.2, include direct tunneling from valence band, Fowler-Nordheim injection, trap-assisted injection, constant-energy tunneling from silicon

conduction band, tunneling from conduction band into traps close to the Fermi energy level , and hopping conduction at the Fermi level, respectively [49].

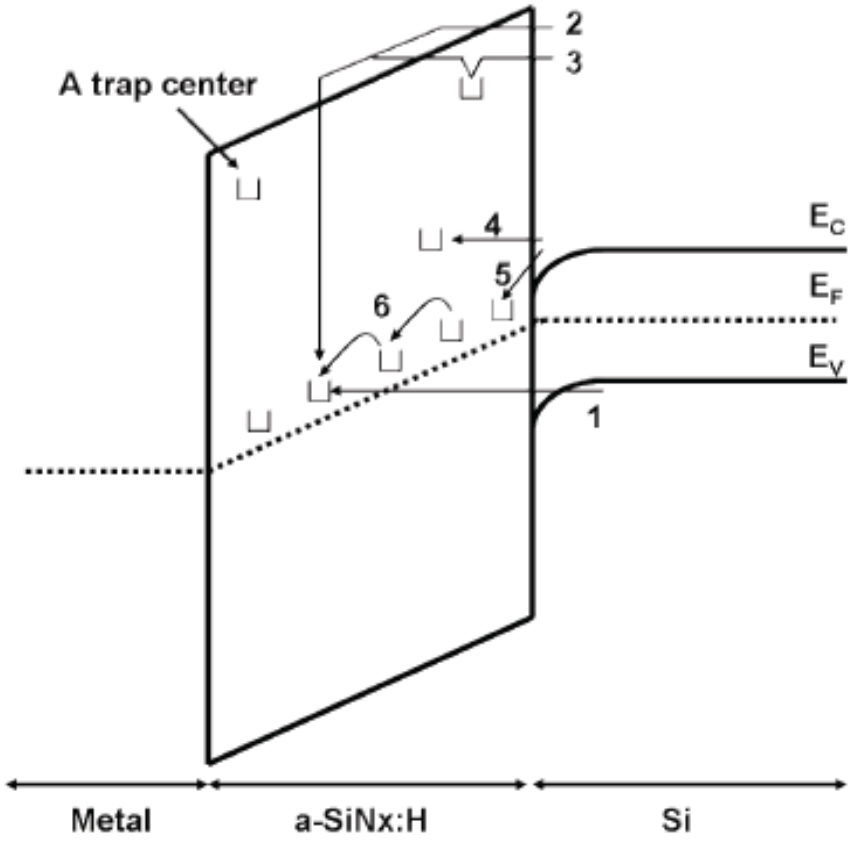


Figure 3.2: Charge trapping mechanisms: 1- direct tunnelling from valence band, 2- Fowler-Nordheim injection, 3- trap-assisted injection, 4- constant-energy tunnelling from silicon conduction band, 5- tunnelling from conduction band into traps close to E_F, and 6- hopping at the Fermi level [49].

It is not easy to deduce which mechanism is dominant. In general, this is dependent on the nitride trap density and the applied electric field. Mechanisms 1-3 are believed to occur at relatively large electric fields, while the others may occur even at low fields [49].

In contrast to the defect state creation, charge trapping is reversible even at room temperature and almost immediately [50][51]. Charge de-trapping from the nitride dielectric, back into the TFT channel layer, is energetically favourable due to the lower energy level in the channel when the gate bias is removed (Figure 3.3). Furthermore, it is reported that at negative bias, negative charges (electrons) are de-trapped while positive charges (holes) are trapped, causing a negative shift in the threshold voltage.

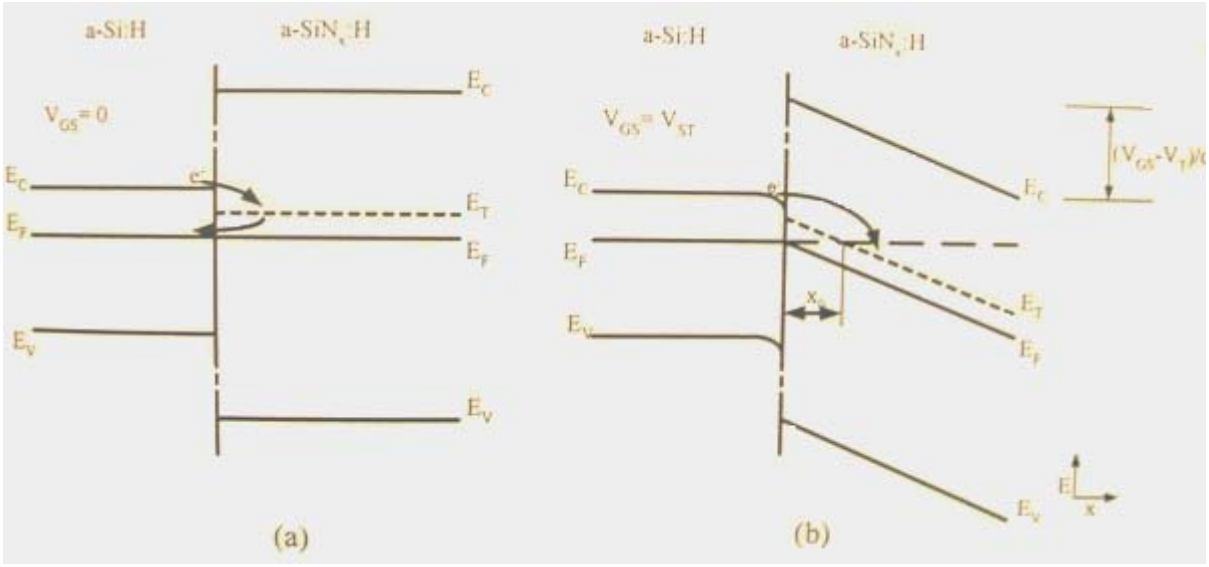


Figure 3.3: Energy-band diagram at the a-Si:H/dielectric interface at a) Vgs=0V and b) Vgs=Vst where Vst is the stress voltage bias. [37]

The mechanisms behind charge trapping, unlike for defect state creation, have remained controversial even after decades of study [32]. There are two models that explain charge trapping, one by Powell et al. [49] and the other by Libsch/Kanicki [50]. According to Powell in [49], charge injection occurs from the a-Si:H channel layer to the silicon nitride layer through trapping near the interface, with no further redistribution of the trapped charges deeper into the nitride. This is also referred to as mono-layer charge trapping. This occurs under conditions where the silicon nitride is of good quality as that prevents further penetration of the traps. Powell indicated that charge trapping is weakly temperature-

activated, therefore $V_{t-shift}$ under various temperatures should not be significant. This model does not support mechanisms 3 and 6 from Figure 3.2.

In contrast to Powell, Libsch and Kanicki in [50] reasoned that for shorter stress times, smaller gate voltages, or lower temperatures, carriers are injected from the a-Si:H channel layer into energy states located at the a-Si:H/nitride interface and in a transitional layer close to the interface. At higher stress times, larger gate voltages, or higher stress temperatures, a larger fraction of the states near the interface are filled, which increases the probability of re-emission from these filled states towards those deep in the nitride. They stated that the motion between traps is diffusive superimposed with a drift velocity by the electric field [50]. Essentially, the $V_{t-shift}$ is dependent on the number of initial interface states that act as charge trapping initiators. Furthermore, as there is re-emission of charges into deeper traps, the $V_{t-shift}$ is dependent on temperature. Higher temperatures would lead to more trapping deeper in the dielectric. It was found that $V_{t-shift}$ was dominated by dielectric trapping rather than defect creation in the a-Si:H layer as changing the dielectric from silicon nitride to silicon dioxide changed the $V_{t-shift}$.

The dual-gate TFT, with its two different interfaces, is a useful device to test the extent of $V_{t-shift}$ in the top and bottom channel under different temperatures. If the $V_{t-shift}$ behaviour between the top and bottom channel is drastically different under different temperatures, then the Libsch and Kanicki model would hold since the only difference between the top and bottom channel are the interface states (the bulk active layer has identical a-Si:H quality).

3.3 Constant Voltage & Constant Current Stress Tests

A TFT undergoes stress when an electric field is applied across the dielectric and when there is source to drain current conduction through the channel that is created. In order to observe this, two stress test conditions can be used: voltage stress (Figure 3.4a) and current stress (Figure 3.4b). In AMOLED displays the drive TFT does not undergo constant voltage or current stress, but rather pulsed stress due to video signals that change for each frame.

Nevertheless, constant stress has been used to accelerate tests to shorten stress test time compared to pulsed stressed tests [53].

A constant voltage stress test is done by simply biasing the gate and drain to a positive voltage and measuring I-V curves periodically to allow for V_t extraction and to determine the $V_{t-shift}$ (Figure 3.4a). This method has the drawback of not being able to provide constant electric field, hence channel band tail electrons are reduced over time. This is due to the fact that the threshold voltage increases over time under electrical stress hence $V_{GS} - V_t$ or $V_{OVERDRIVE}$ decreases, and hence reduces the drain current (**2.9** and **2.10**). Reduced $V_{OVERDRIVE}$ can also shift the TFT region of operation from triode to saturation to off, making it more challenging to evaluate the $V_{t-shift}$ mechanisms under different accumulated carrier densities in the channel.

A constant current stress test is done by connecting the drain with both the gates (diode connection) and applying a constant current at that node while sampling the voltage every sixty seconds. The constant current stress test has positive feedback that adjusts the drain and gate voltage to keep a constant electric field on the channel and therefore a constant number of electrons in the conduction channel (Figure 3.4b). As a result, the $V_{t-shift}$ effect due to constant electric field or constant band tail carrier density does not go away over time. In this case, the threshold voltage can increase indefinitely until the applied gate voltage hits the supply voltage or the density of weak silicon to silicon bonds become a rate limiting factor [53]. For our experiments, constant current stress was used.

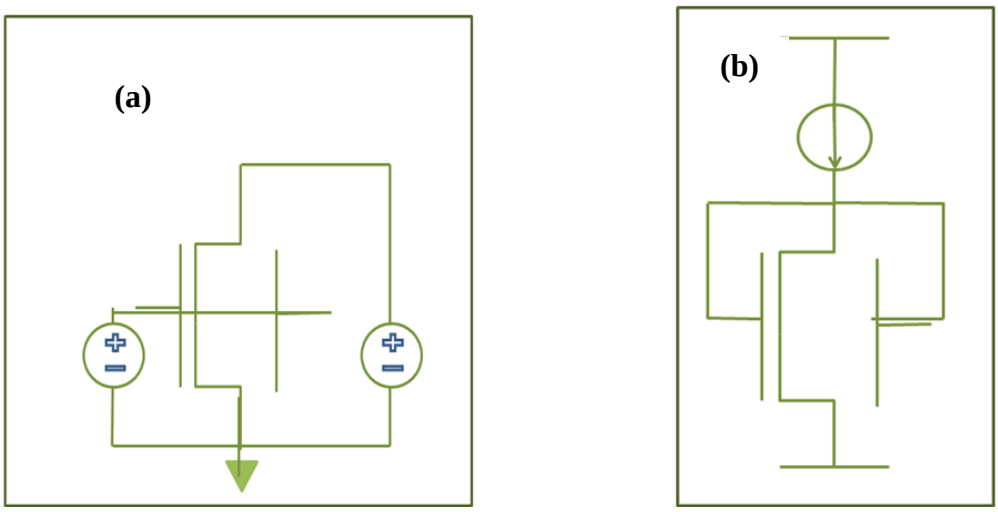


Figure 3.4: Dual gate TFT stress test with **a)** constant voltage bias and **b)** constant current bias

3.4 Constant Current $V_{t-shift}$ Results and Discussion

3.4.1 Starting Bias Voltage

Constant current bias as in Figure 3.4b for dual gate requires less gate voltage than for single gate. It is an advantage that comes with having dual channels and reduced threshold voltage as discussed in Section 2.3.2. Table 3-1 summarizes the starting gate voltage for its appropriate current bias. It clearly shows that the overdrive gate voltage advantage here ranges only from 4%-7%; far less than the 20% gain that was shown in Figure 2.11. This may be because the drain voltage is also varied here unlike for the measurement shown in Figure 2.11.

Table 3-1: Starting gate voltage for dual and single gate TFT under constant current stress test

Stress Current (uA)	Temperature (ºC)	Starting Voltage (V)			Dual Gate Overdrive Voltage Reduction (%)
		Single Gate	Dual Gate	Difference	
10	***25***	6.82	6.56	0.26	4
	75	5.08	4.72	0.36	7
50	***25***	13.21	12.44	0.77	6
	75	9.27	8.61	0.66	7

3.4.2 Definition of $V_{t-shift}$

$V_{t-shift}$ is simply the amount of voltage that has been shifted from its starting point. It can be defined as

$$V_{t-shift} = V_{Gate}(time) - V_{Gate}(0), \quad \textbf{(3.1)}$$

where $time$ can be in hours and $V_{Gate}(0)$ is the starting voltage. Although in the last section focused on the initial voltage, the $V_{t-shift}$ is the real figure of merit that is used to characterize the stability of the TFT. The initial voltage influences the $V_{t-shift}$ since it determines the electric field on the a-Si:H/nitride interface and electron density in the channel. Table 3-2 summarizes the threshold voltage for single and dual gate TFTs at 10uA and 50uA at temperatures 25ºC and 75ºC for 10 hours.

Table 3-2: Summary of constant current $V_{t-shift}$ for dual and single gate TFT

Stress Current (uA)	Temperature (ºC)	$V_{t-shift}$ (V)			$V_{t-shift}$ Improvement (%)
		Single Gate	Dual Gate	Difference	
10	***25***	0.58	0.35	0.23	40
	75	1.8	1.65	0.15	8.3
50	***25***	2.38	1.16	1.22	51.8
	75	5.43	5.07	0.33	6

Table 3-2 shows that the dual gate shows 50% $V_{t-shift}$ improvement over a single gate TFT at 25ºC. This is further illustrated in Figure 3.5. Both single and dual gate TFTs show strong dependency on temperature as the $V_{t-shift}$ increases by 3 folds at 75 ºC. Strong temperature dependency of $V_{t-shift}$ rules out Powell's model for mono-layer dielectric charge trapping as a dominant mechanism. The dual-gate $V_{t-shift}$ plot at 25ºC and 75 ºC are illustrated in Figure 3.6.

Figure 3.7 shows $V_{t-shift}$ for both dual gate and single gate TFTs with 10uA and 50uA constant current stress at 75 ºC. Compared to results at 25 ºC, the $V_{t-shift}$ has been reduced to 6% and 8.3% from 51.8% and 40% for 50uA and 10uA respectively during 10 hours of current stress. In other words, the dual gate $V_{t-shift}$ is almost the same as a single gate at 75 ºC regardless of the slightly reduced $V_{OVERDRIVE}$. Since the a-Si:H silicon is the same for both top and bottom channels, the acceleration of dual gate $V_{t-shift}$ can be attributed to Libsch and Kanicki's charge trapping model. This model assumes that the $V_{t-shift}$ is dependent on interface states, of which the top channel contains 10 times that of the bottom channel as discussed in Section 2.3.2. Having such high interface states leads to enough multi-layered charge trapping in the dielectric that the top channel threshold voltage is increased. When the threshold voltage is high enough, it reduces accumulation and filled interface states resulting in shutting off the top channel and putting all the E-field and current pressure on the bottom channel. Shutting off the top channel thus leads to $V_{t-shift}$ similar to a single-channel device. Furthermore, the $V_{t-shift}$ trend seems to improve over time. This is possibly due to the low energy dielectric traps being filled in both the top and bottom channels, leading to a more even distribution of current and electric field, hence reducing $V_{t-shift}$.

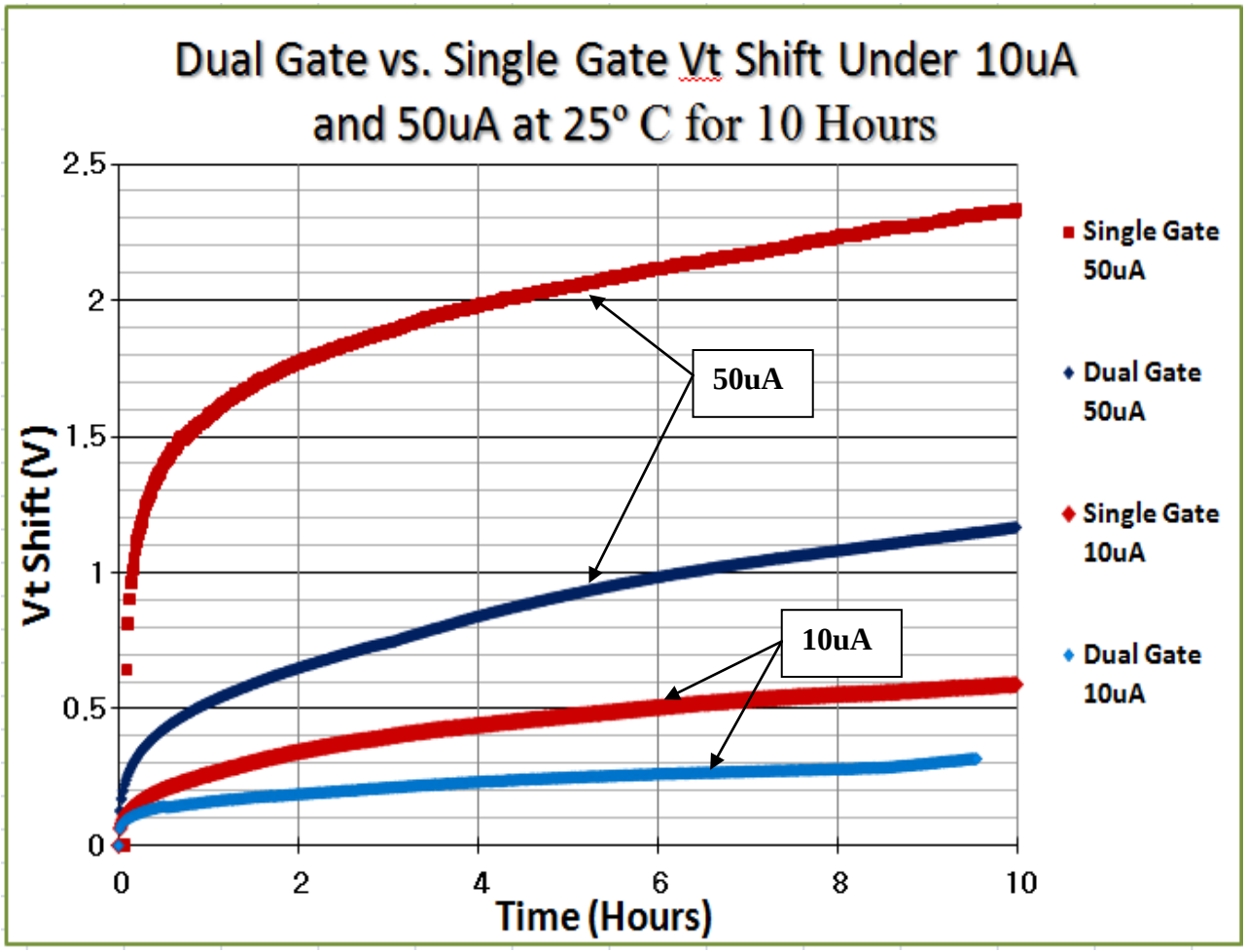


Figure 3.5: Dual gate and Single gate $V_{t-shift}$ comparison under 10uA and 50uA at 25ºC for 10 hours

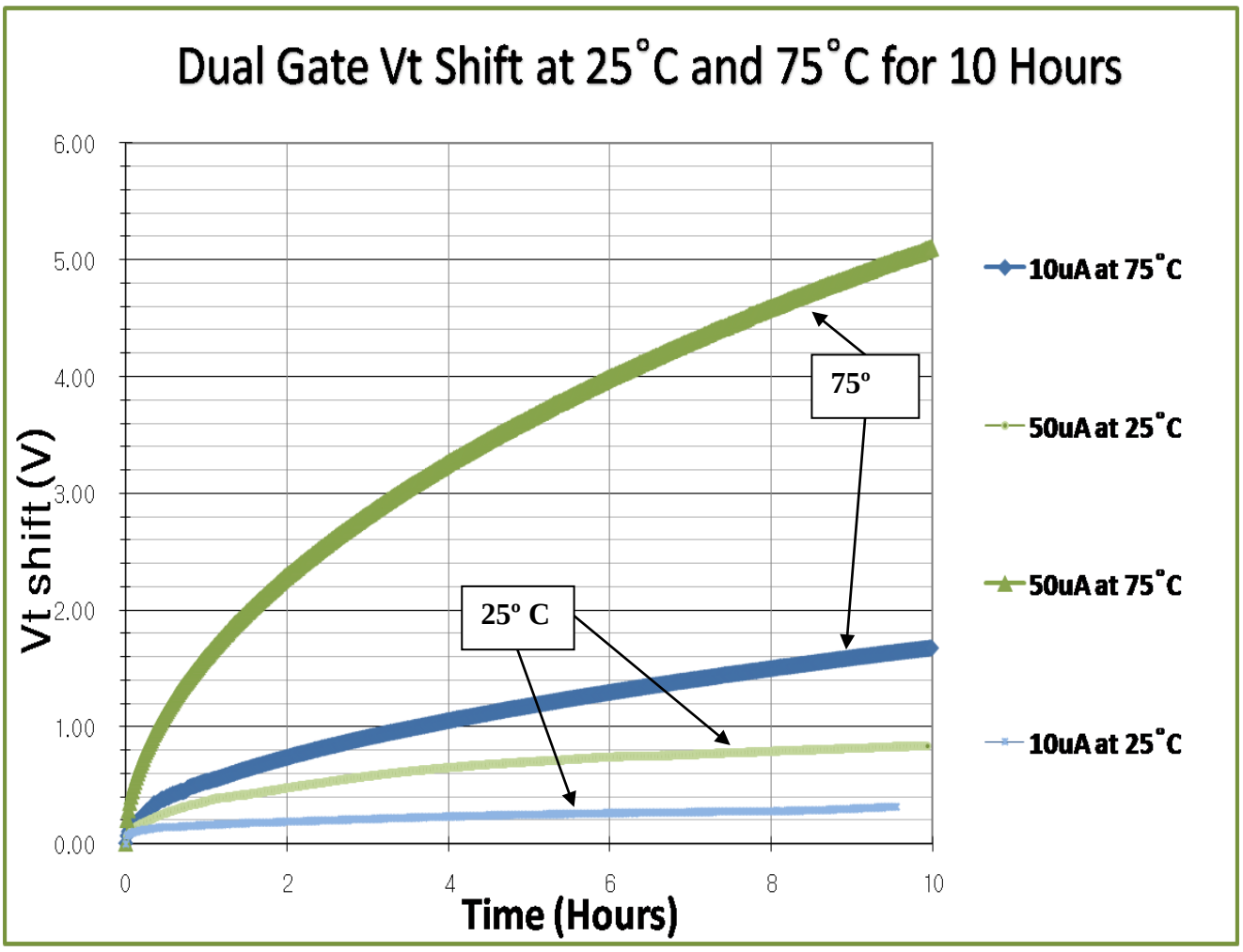


Figure 3.6: Dual gate $V_{t-shift}$ comparison under 10uA and 50uA at 25ºC and 75ºC for 10 hours

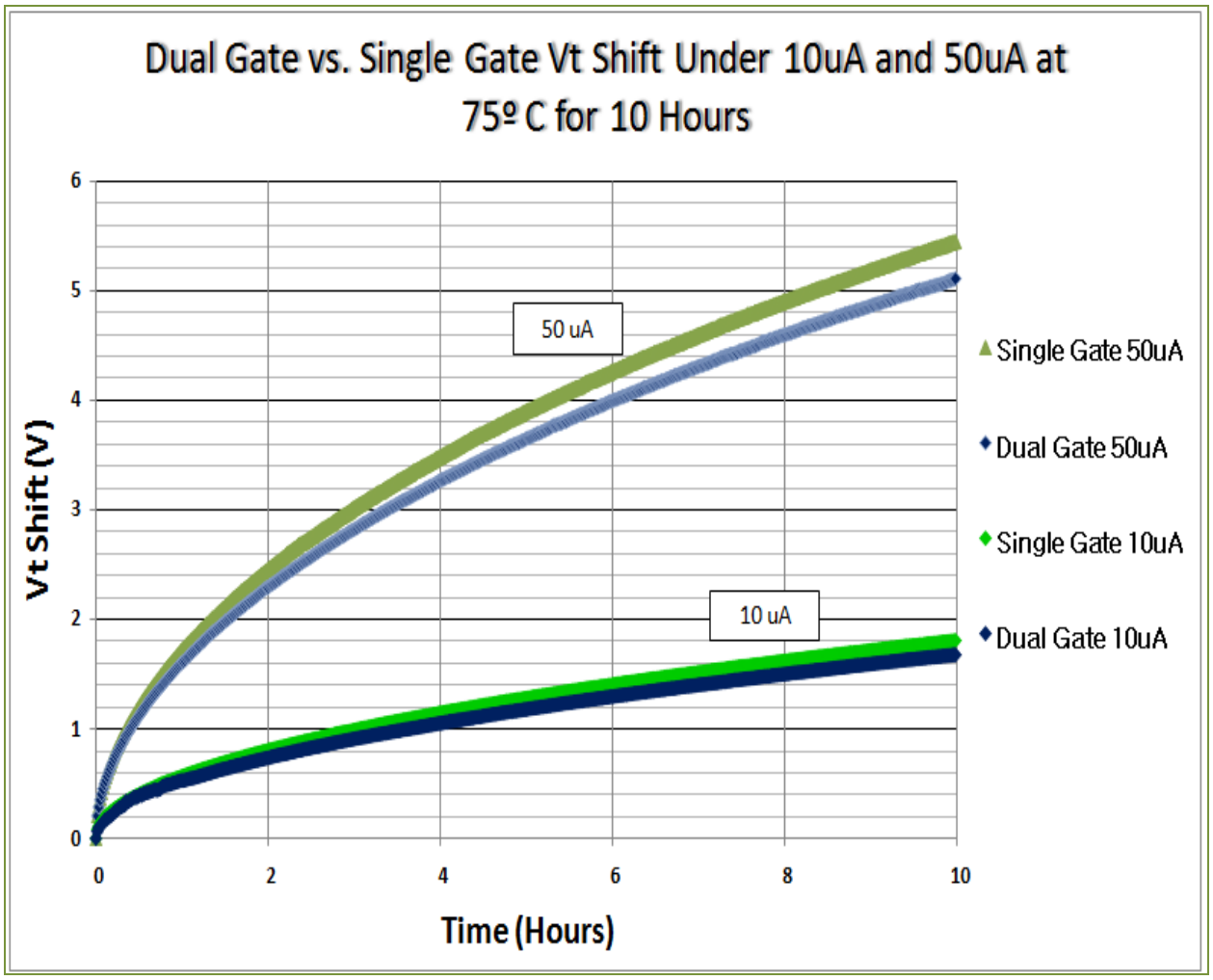


Figure 3.7: Dual gate and Single gate $V_{t-shift}$ comparison under 10uA and 50uA at 75ºC for 10 hours

3.5 Summary and Future Work

In this chapter we use results from a constant current stress test over 10 hours to show that the dual gate TFT $V_{t-shift}$ is improved by ~50% at 25ºC and only ~8% at 75ºC. The variation in the temperature dependancy between single and dual gate attributes the $V_{t-shift}$ mechanism to Libsch and Kaniki's multi-layer dielectric trapping.

Further test methods can be used to pinpoint the dominant mechanism of $V_{t-shift}$. The investigation of dominant mechanism can be done more accurately if the dual gate had separated top and bottom electrodes to isolate the two interfaces. In any case, these tests include: constant current stress under more temperatures between 25ºC and 75ºC , turnaround phenomenon of threshold voltage shifts under negative bias stress, heating the TFT to 75ºC and cooling back to room tempearture followed by constant current stressing, constant current stressing at 75ºC followed by negative bias stress under 25ºC, and finally constant current stressing at 75ºC followed by negative bias stress under 75ºC.

Characterizing $V_{t-shift}$ using separate channels will allow a superpositioned current or voltage dependent $V_{t-shift}$ equation. Constant current stress under more intermediate tempeartures would give a better undesrtanding of the temperature sensetivity of $V_{t-shift}$ which can lead to a proper temperature dependent model. Turnaround phenomenon would be an excellent way to root out whether charge trapping or defect creation is the dominant $V_{t-shift}$ mechanism for the dual gate TFT. Heating the TFT to 75ºC and cooling it back to room tempearture followed by constant current stressing will show whether the high temperature causes a-SI:H structural change. Constant current stressing at 75ºC followed by negative bias stress under 25ºC and constant current stressing at 75ºC followed by negative bias stress under 75ºC will show whether the de-trapping is temperature dependant, leading to a possible confirmation of Libsch and Kanicki's nitride trapping model.

3.6 Future Device Improvement

For the BCE process, the back-channel region is heavily damanged due to source/drain etch process and contaminated by air exposure before the passivation layer is put on. In the trilayer process however, the top SiN_x is deposited immediately after the a-Si:H in the same vacuum, making it free of etching damage and environmental contamination. On the other hand, the top channel performance is still affected by the top SiN_x deposition process condition as mentioned in Section 2.2. The top channel a-Si:H layer can be modified with various types of plasmas to lower the density of states before the deposition of the top-channel dielectric. Furthermore, dual-layer dielectric, where the first layer is optimized for better interface and the second is optimized for deposition rate, can be be used to reduce top channel interface states which leads to higher mobility, lower threshold voltage, lower leakage current and less prone to nitride trapping at the top channel.

Chapter 4

Phase Response Touch Screen Panel Readout Scheme

4.1 Conventional Voltage Readout Scheme

Mutual capacitive TSPs are currently the conventional implementation of TSP in mobile phones [24]. Mutual capacitive TSPs consist of an array of capacitors formed from a grid of metal tracks with a dielectric in between (see Sensor in Figure 4.1). A voltage response readout scheme is used to detect touch signals in this system. First, Cpix is pre-charged to Vstep in the pre-charge stage. Then in the evaluate stage, the presence of a touch signal would increase Cpix and redistribute the charge Qpix according to $\frac{Qpix}{+\Delta Cpix} = -\Delta Vtouch$, causing a decrease in voltage. The voltage signal is amplified using a charge amplifier. An example of a coordinated touch signal read is shown in Figure 23 where the output signal can be equated as:

$$V_0 = -V_{step}\frac{\Delta C_{pix}}{C_f} \quad \textbf{(4.1)}$$

Where V_{step} is the pre-charge voltage, C_f, is the feedback capacitor and ΔC_{pix} is the change in pixel capacitance due to a finger touch. This readout scheme needs two layers of metals to obtain the x and y coordinates of the touch signal. However, for more transparent TSP applicable for mobile displays, the number of layers that make up the TSP must be reduced. In order to further reduce the number of metal layers, a different signal readout method needs to be used.

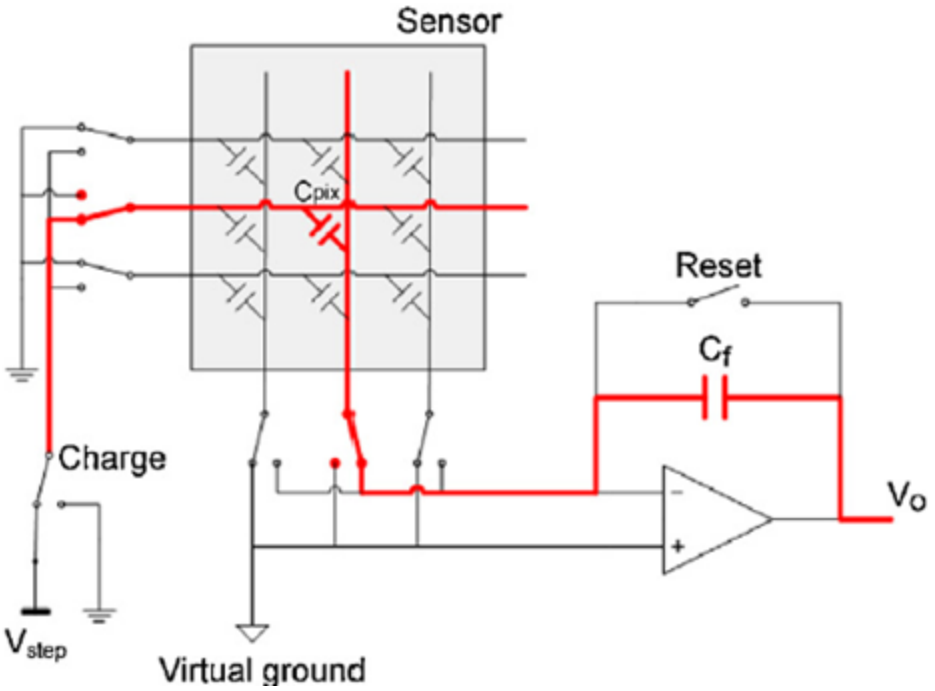


Figure 4.1: Voltage readout scheme for a mutual capacitive TSP

4.2 Novel Phase Response Readout Scheme

The contribution of this thesis is to show by simulation a phase response readout scheme that detects both the touch occurrence and touch position on a single metal sensor track. Unlike with voltage response, measuring the phase response makes use of both the capacitance and resistance of the single layer of metal tracks to calculate both of the x and y touch coordinates on the TSP as illustrated in **Figure 4.2**. Rows of sensor tracks are oriented parallel to a reference track. The sensor tracks measure the touch signal and compare the signal with that of the reference metal track. The reference signal does not change; hence when the screen is touched, the degree of phase shift can be used to determine both the touch occurrence and the position of the touch on the metal track. All results in this chapter are simulation results from Cadence Virtuoso and Spectre [44].

4.2.1 Touch Signal Phase Shift

A sinusoidal voltage signal is supplied to both the sensor and reference tracks. The phase of the sensor track signal can be changed simply by adding a signal capacitance, such as due to a finger touch. The extra capacitance will slow down the sinusoidal signal, creating a phase change. This change in phase can be defined using the following equation

$$\theta = \tan^{-1}\left(\frac{1}{2\pi f \Delta R_{out} \Delta C_{touch}}\right) \quad \textbf{(4.1)}$$

where ΔC_{touch} is the capacitance due to a finger touch and ΔR_{out} is the resistance that the voltage source faces as it charges up the capacitor. f is simply the frequency of the input signal.

4.2.2 Phase Response Design Consideration

The phase response is an inverse tangential and therefore its sensitivity depends on how small the values of $f, \Delta R_{out}$, and ΔC_{touch} are as shown in (Figure 4.3). The inverse tangent of values much greater than 1 will not yield much phase shift. Therefore optimum touch sensitivity is given by:

$$1/(2\pi f \Delta R_{out} \Delta C_{touch}) \approx 1. \quad \textbf{(4.2)}$$

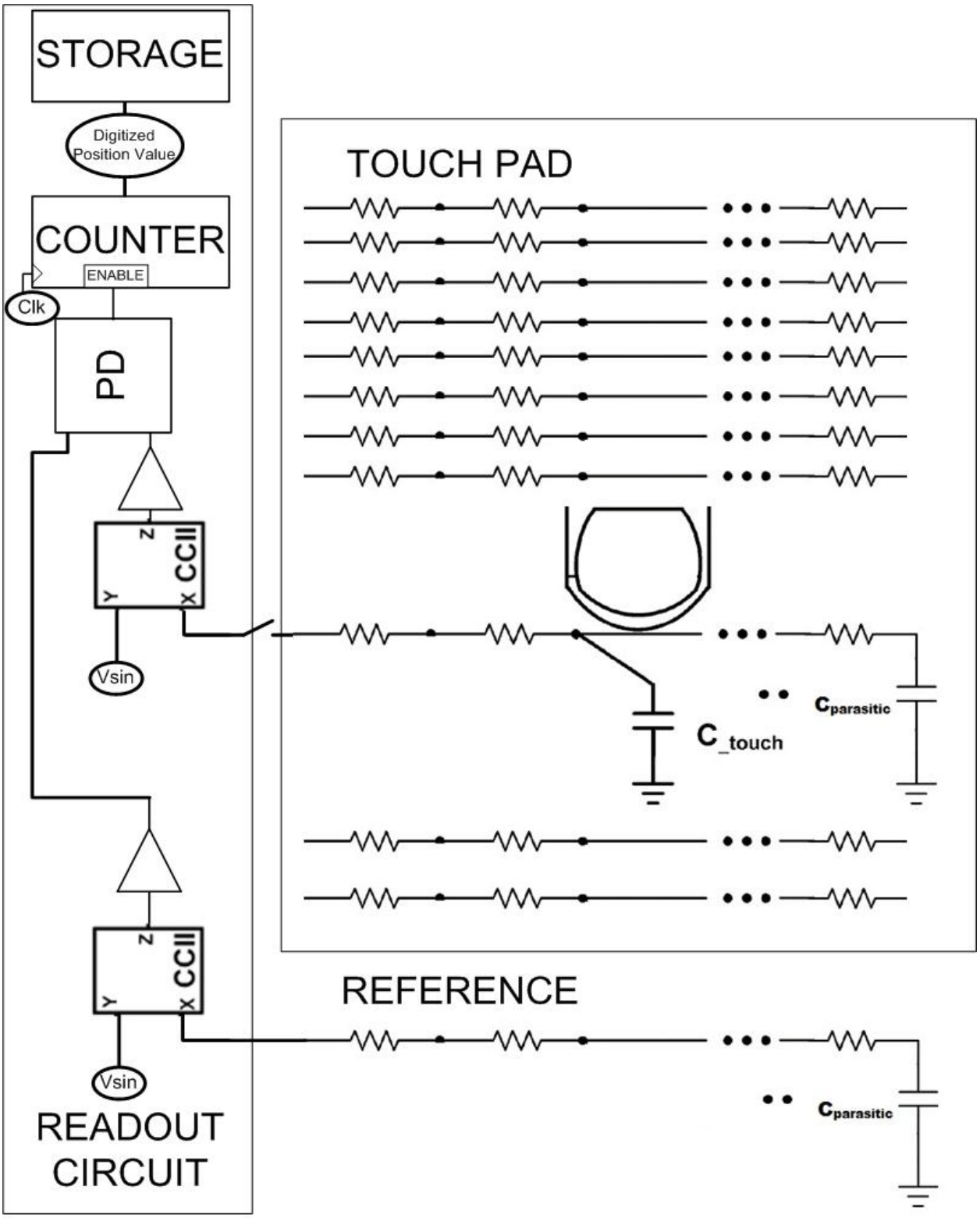


Figure 4.2: Phase Response TSP System

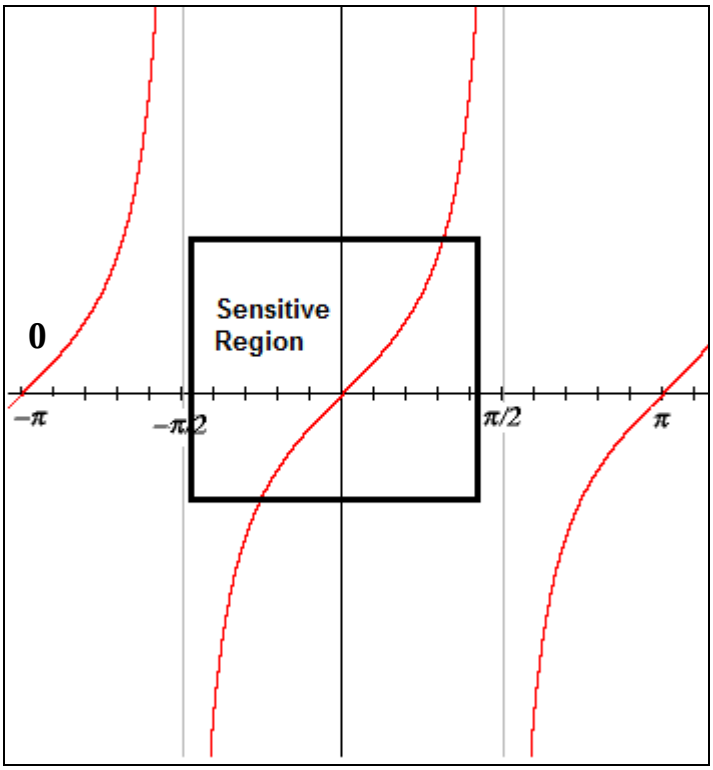


Figure 4.3: Tangential Curve highlighting the sensitive area

ΔC_{touch} Capacitor Design

The design of the capacitor is somewhat limited by the thickness of the passivation layer. The value of C is in the range of tens of pico-farads [9]. The capacitance value also depends on the area of the metal track, which introduces constraints on the resistivity and resolution. Increased metal area decreases resistance and resolution.

f Frequency Selection

An increase in frequency will increase power consumption. Hence, lower frequency is desired for mobile electronic devices. The effect of frequency on touch sensitivity will be discussed further in Section 4.2.3.1.

ΔR_{out} Metal Track Resistance

ΔR_{out} is one design parameter that can be varied greatly as it is heavily dependent on the type of material being used. Common materials are AlZnO, $AlMoO_3$ and ITO. ITO resistance depends on material anneal time and temperature, whereas $AlMoO_3$ depends on the Al to MoO_3 ratio. To get $1/(2\pi f \Delta R_{out} \Delta C_{touch}) \approx 1$, the requirement for total metal track resistance range from ~1 $k\Omega$ - ~100 $k\Omega$ to allow reasonable frequency from ~1000Hz – ~100000Hz to compensate for the ~10pF capacitance value.

4.2.3 One-Sided Readout Circuit

A one-sided readout scheme reduces the number of CMOS ICs attached to the TSP/Display glass, resulting in decreased cost and increased yield. A diagram of the readout scheme is shown in **Figure 4.2**. The Current Conveyor (CCII) [34] first supplies a sinusoidal signal to the touch and reference metal lines, then reads it back and amplifies it. Secondly, the sinusoidal signal is buffered to create a square wave. This square signal and the reference wave are then fed into the Phase Detector (PD) [55]. The PD outputs the phase difference as a voltage which depends on the touch occurrence (ΔC_{touch}) and touch position (ΔR_{out}). Positive output from the PD enables a counter which determines the amount of phase difference. This value is then stored in 8 parallel D Flip-Flops [1][2].

4.2.3.1 Current Conveyor (CCII)

The CCII can supply voltage and read back the touch pad signal simultaneously. The functionality of a CCII can be modeled as follows [34]:

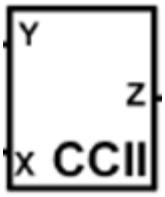
$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ M & 0 & 0 \\ 0 & K & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad \textbf{(4.3)}$$

Where $M \leq 1$and $K \leq 1$. The symbol and circuit diagram is shown in Figure 4.4. The transistor sizes are summarized in Table 4-1 and the large and small signal transfer curves for $V_X = MV_Y$ are shown in Figure 4.5. M in Figure 4.5 is shown to be 1 for V_Y of 0.8V to 1.5V.

Table 4-1: CCII Transistor Aspect Ratios from Figure 4.4

Transistor	Width/Length Ratio
M1	$2um/0.5um$
M2, M5, M6	$20um/0.5um$
M3, M4	$32um/0.5um$
M7, M8	$24um/0.5um$
M9	$12um/1um$
M10, M11	$24um/1um$
M12, M13, M14, M15	$4um/1um$
M16	$16um/1um$

a)



b)

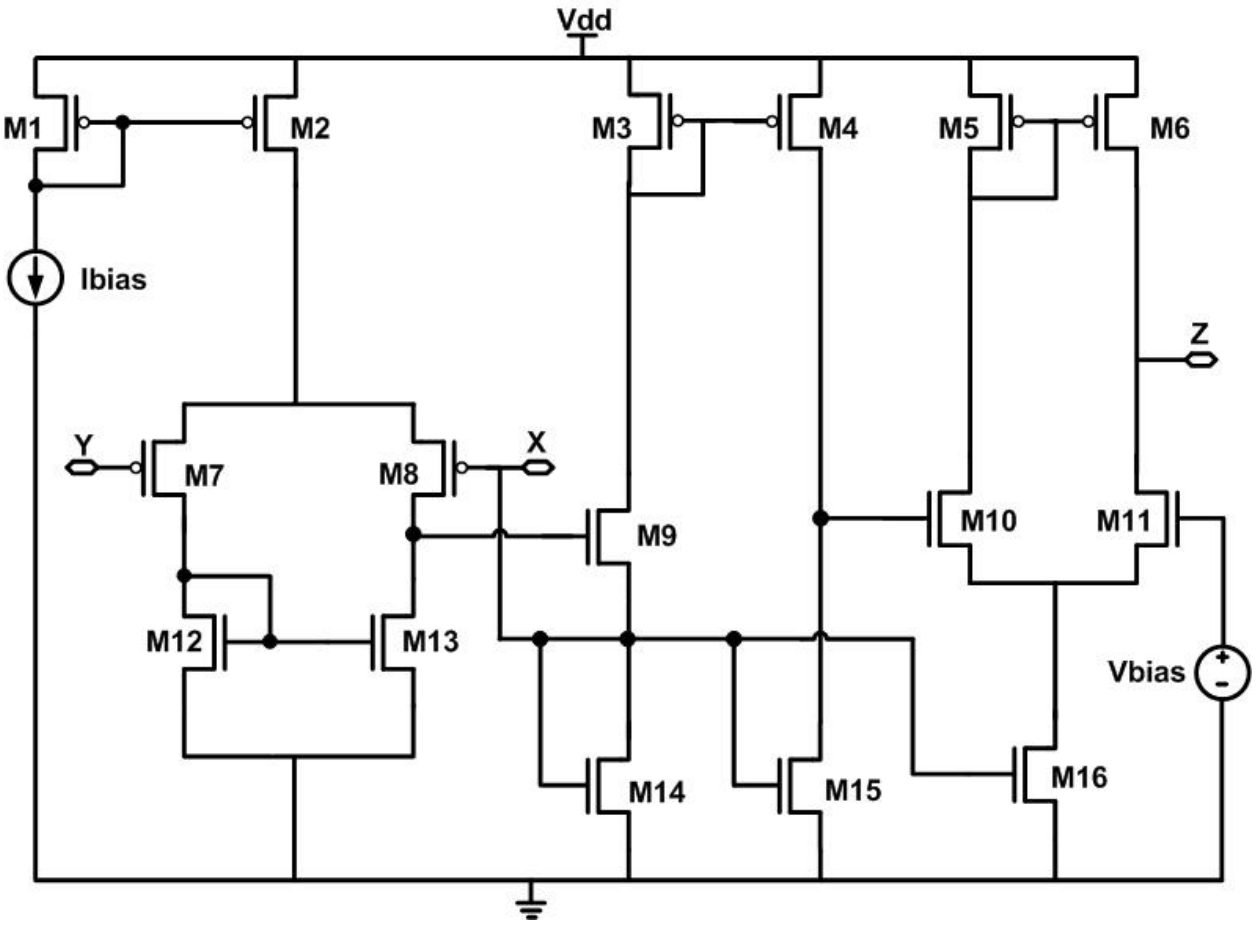
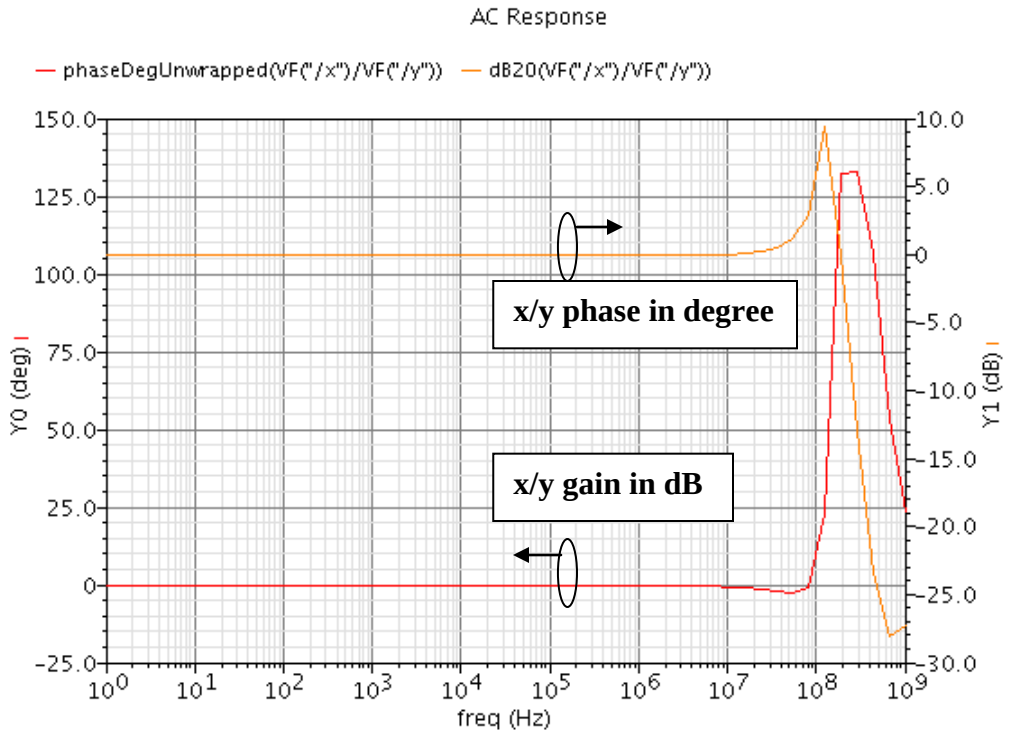
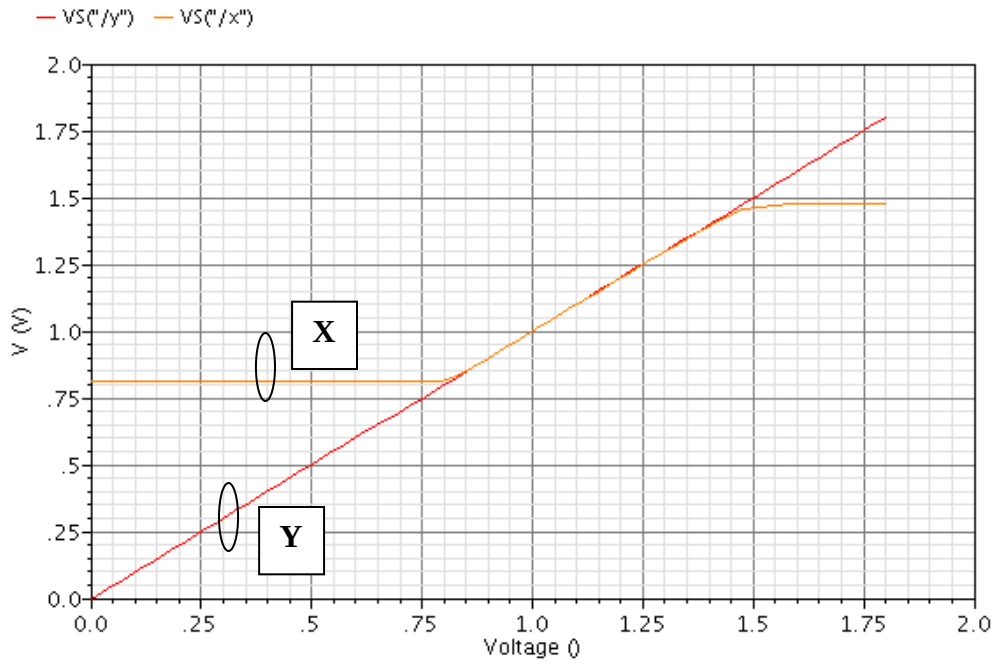


Figure 4.4: CCII a) symbol and b) circuit diagram



a)

X-terminal Large Signal under Y-terminal Sweep



b)

Figure 4.5: $(V_X = MV_Y)$ in a) small signal AC response and b) large signal DC response

The CCII will be connected to the touch pad and reference metal tracks through the x terminal while the y terminal will be toggled with a small signal sinusoid signal as shown in **Figure 4.2**. This will create a toggling voltage at the x terminal creating I_X with the following relation [30]:

$$I_X = -M\left(\Delta C_{touch} + C_{parasitic}\right)\frac{d}{dt}V_X \quad \textbf{(4.4)}$$

Where ΔC_{touch} is the touch pad capacitance change due to a figure touch, $C_{parasitic}$ is the parasitic capacitance due to the display screen underneath. The current amplitude and phase will be shifted depending on the touch signal and copied to the z terminal as follows:

$$I_Z = KI_X \quad \textbf{(4.5)}$$

At node z, there will be a small signal output resistance, which will yield a voltage if multiplied by I_Z. The voltage at the output V_Z, which is obtained from the signal and reference, will be different in phase depending on the touch location. The phase response for resistances ranging from $4k\Omega$, $40k\Omega$ to $400k\Omega$ are shown in Figure 4.6 and the touch position is modeled in Figure 4.5. You will notice that as the resistance increases, it requires less frequency to get good phase response, being consistent with equation 4.1

For this system, $40k\Omega$ was chosen because it gives decent phase difference at 200kHz and the phase change is somewhat linear relative to touch positions of increasing distance along the metal track. The CCII was laid out using common centroid and inter-digitated layout techniques with edge dummies for better transistor matching within the differential pairs (Figure 4.7**)** [56]

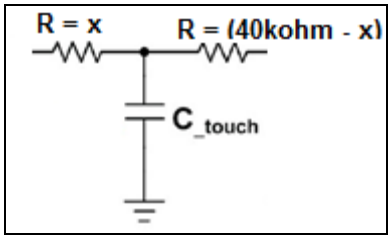
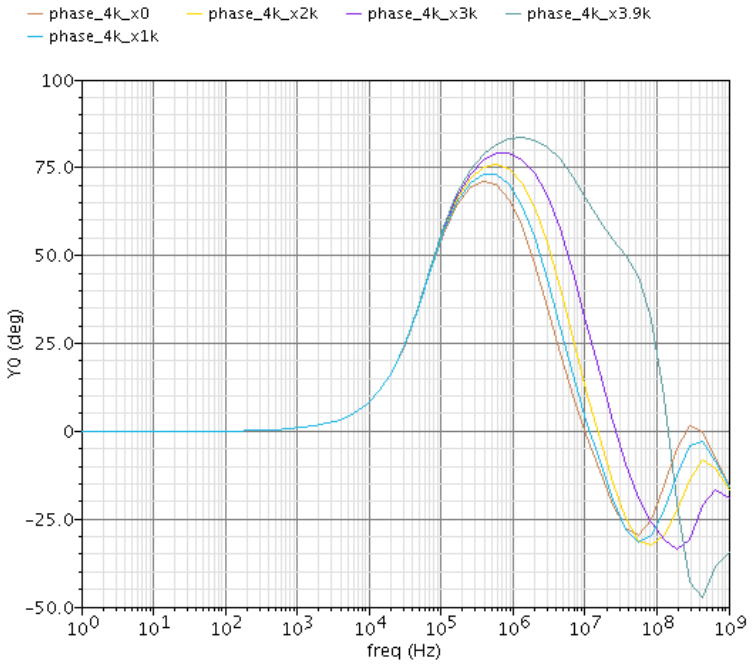


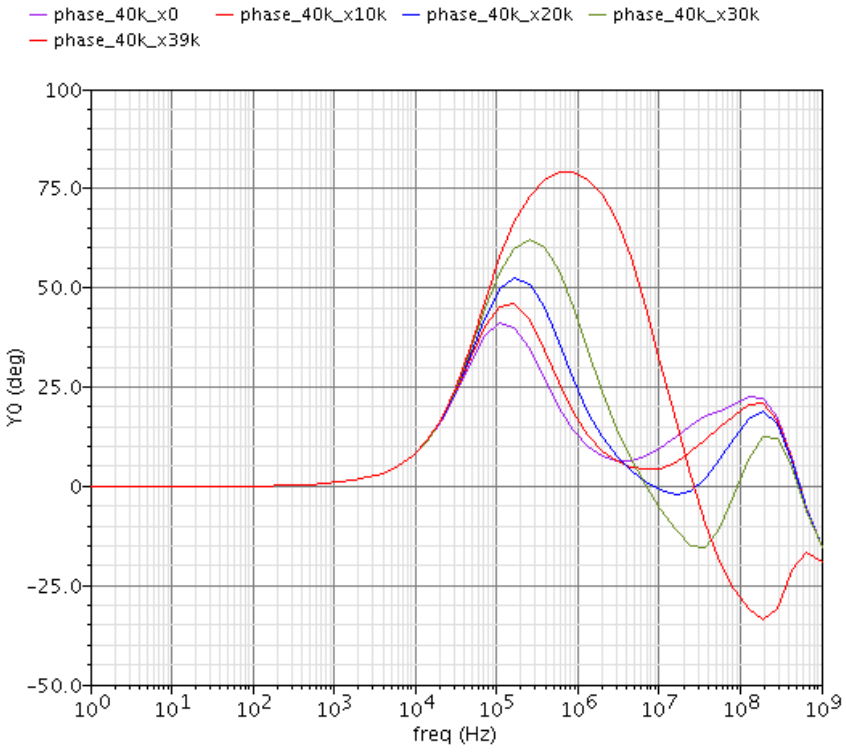
Figure 4.5: Touch capacitance model for various locations on the metal track. The variable x is swept between $0k\Omega$ to $40k\Omega$. The range variation can also be $4k\Omega$ or $400k\Omega$.

Phase Response for 4kΩ Resistor at x = 0kΩ, 1kΩ, 2kΩ, 3kΩ, 3.9 kΩ



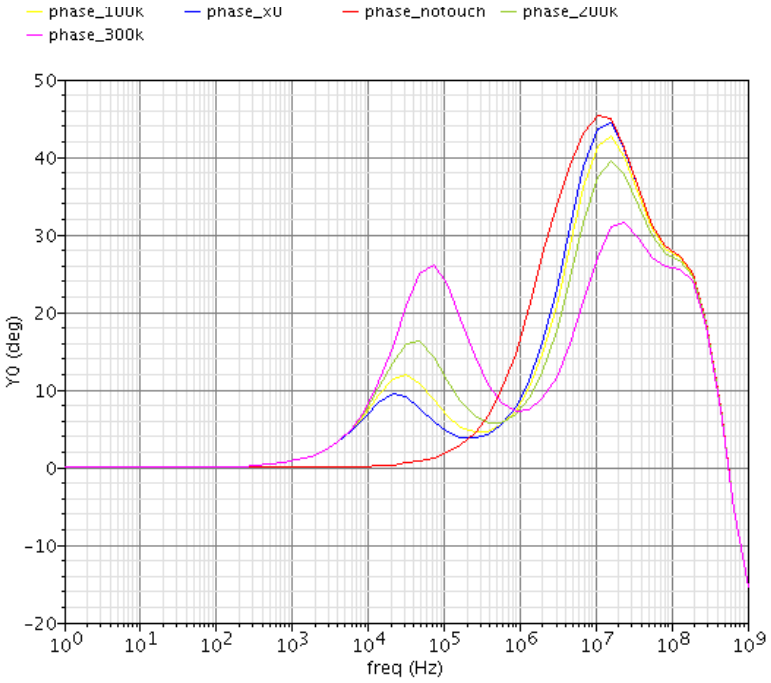
a)

Phase Response for 40kΩ Resistor at x = 0kΩ, 10kΩ, 20kΩ, 3kΩ, 39 kΩ



b)

Phase Response for 400kΩ Resistor at x = 0kΩ, 100kΩ, 200kΩ, 300kΩ, 390kΩ



c)

Figure 4.6 CCII phase response for total metal track resistances **of a)** 4$k\Omega$, **b)** 40$k\Omega$, **c)**400$k\Omega$.

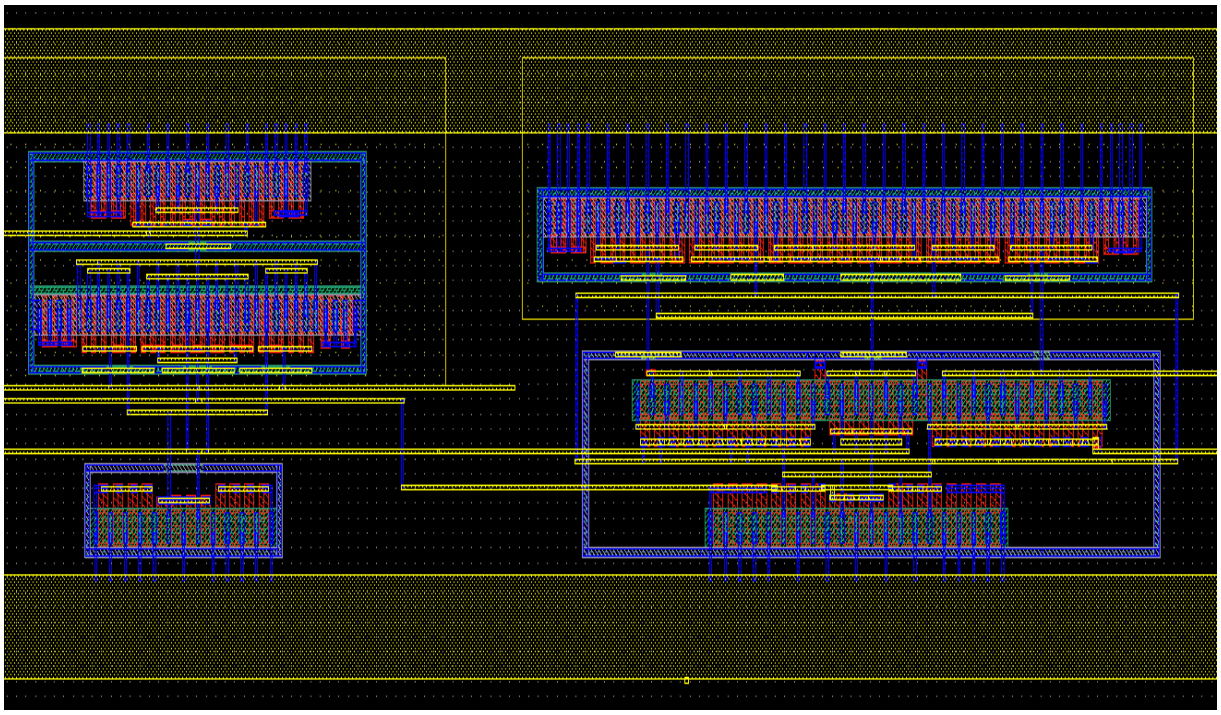


Figure 4.7: CCII layout

4.2.3.2 Exclusive OR (XOR) Phase Detector (PD)

The signals from the CCII are buffered (digitized) into square waves and then fed into the phase detector which quantifies the phase difference.

There are various architectures of phase detectors such as XOR gate, flip flop and Gilbert mixer. Since this is relatively a low frequency system, an XOR gate is used due to its simplicity [55]. The schematic is given in Figure 4.8.

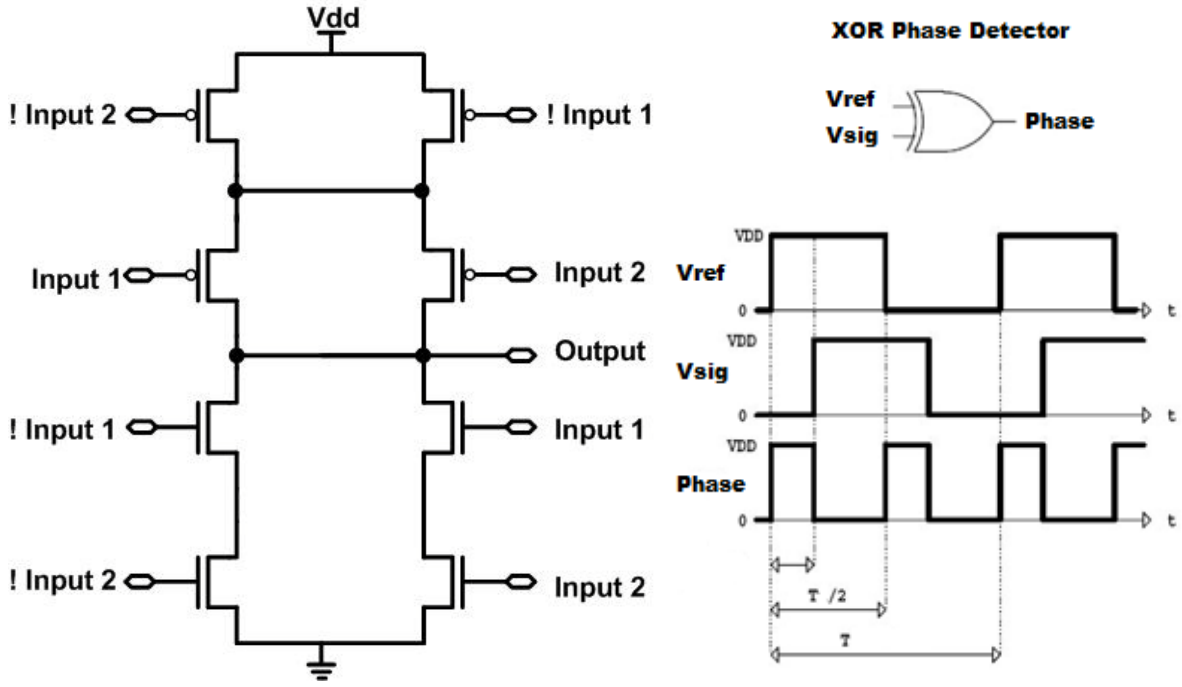


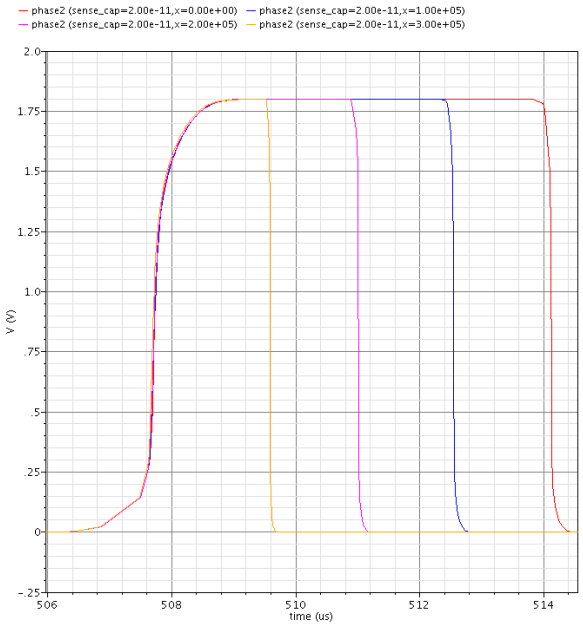
Figure 4.8: CMOS XOR Gate **a)** schematic, **b)** symbol and **c)** functional diming diagram

Table 4-2: XOR Gate Truth Table

Input 1(Vref)	Input 2(Vsignal)	XOR Output (Phase)
0	0	0
0	1	1
1	0	1
1	1	0

A CMOS-logic XOR gate was picked instead of transmission gate logic due to its superior driving capability. Although CMOS architecture requires a higher area overhead, size is not of primary concern in this system. Figure 4.9 shows that the XOR PD output yields different phase for different locations given by the variable x as defined in Figure 4.5.

a) **Phase Detector Output for 400kΩ Resistor at x = 0kΩ, 100kΩ, 200kΩ, 300kΩ, 390kΩ**



b)

Phase Detector Output for 40kΩ Resistor at x = 0kΩ, 10kΩ, 20kΩ, 30kΩ, 39kΩ

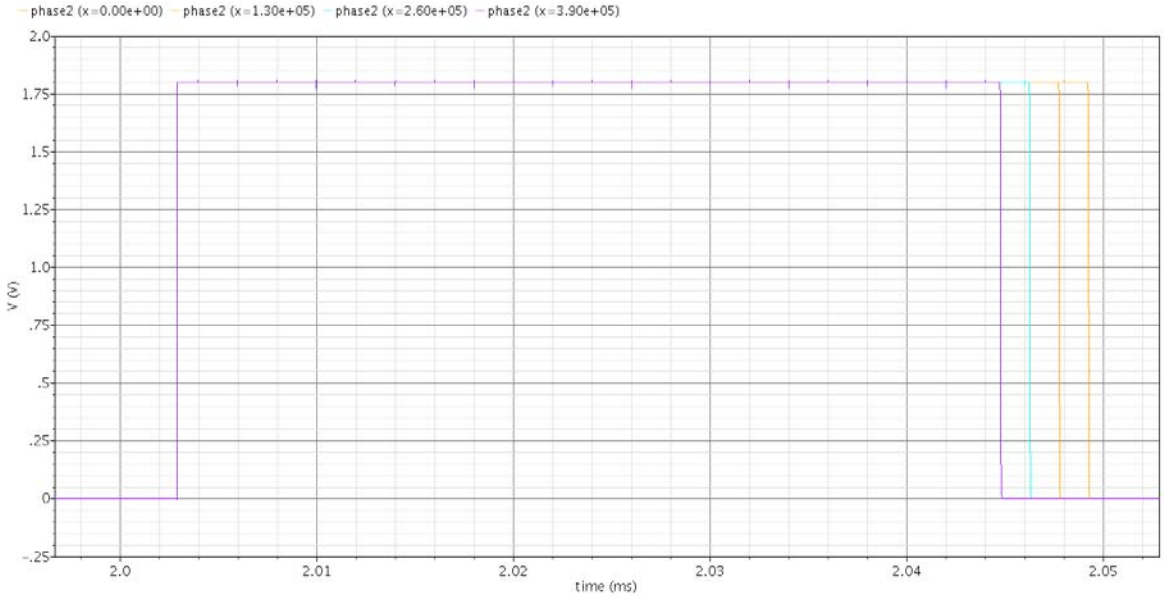
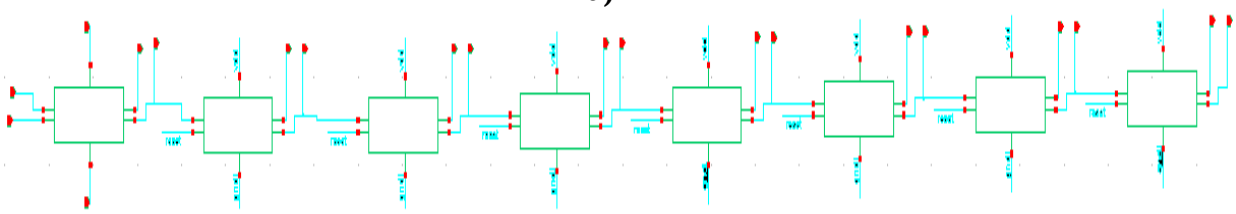


Figure 4.9: XOR Phase Detector output for **a)** 400$k\Omega$ and **b)** 40$k\Omega$**.**

4.2.3.3 Counter (8-bit)

In order to quantitatively measure the phase difference for different locations of touch, an 8-bit counter is used. Each bit is a JK flip flop (Figure 4.10) where both J and K are always connected to Vdd to force toggling in every clock cycle (last row on **Table 3**) [1]. The phase output acts as an enable signal for the counter as shown in Figure 4.11**.** When the phase output signal goes down, the reset signal turns on and resets the counter. The final value on each bit of the counter is stored in the 8 D Flip Flops that are connected in parallel.

a)



b)

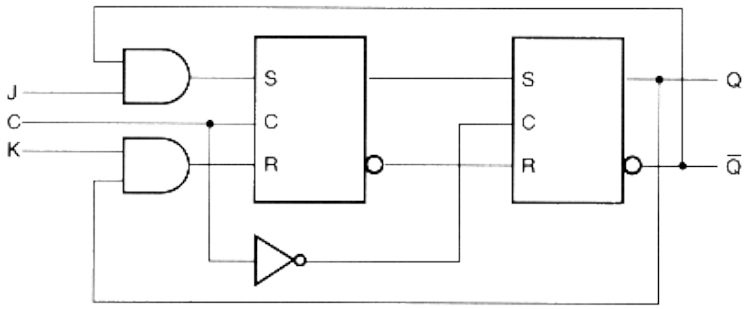


Figure 4.10: a) an 8-bit counter built with **b)** JK Flip Flops [1]

Table 4-3: JK Flip Flop Truth Table

CLK	J K	Q
0	X X	No change
1	0 0	No change
1	0 1	0
1	1 0	1
1	1 1	**Toggle**

Counter Enabled When Phase Detector Output is High

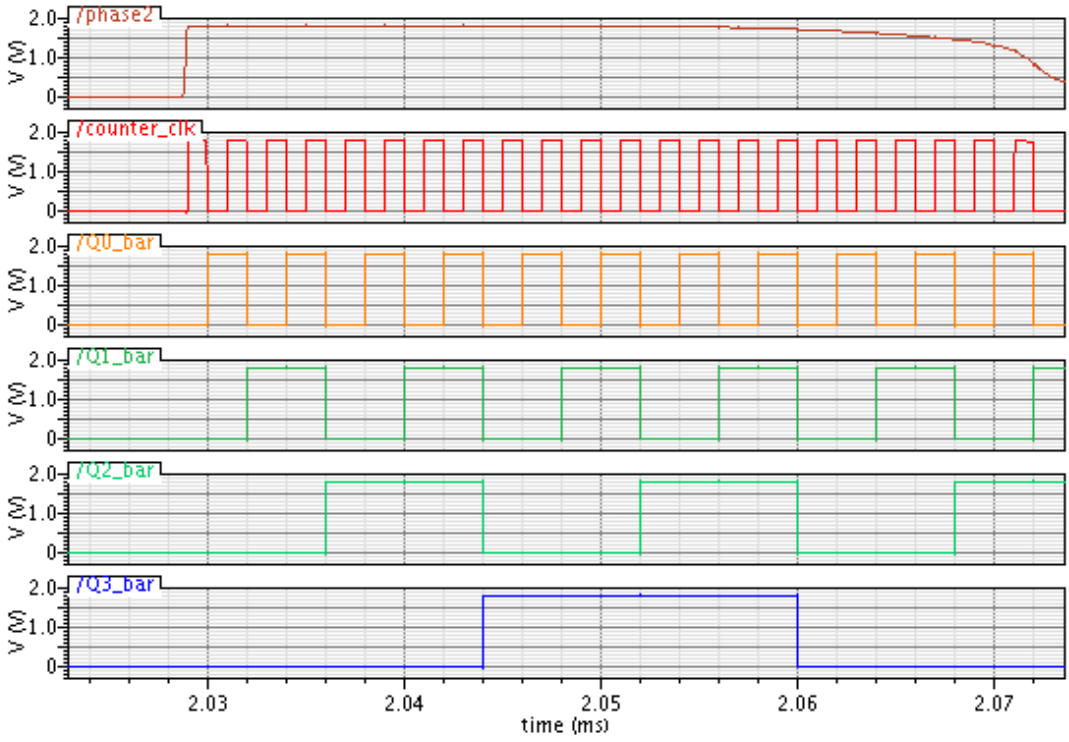
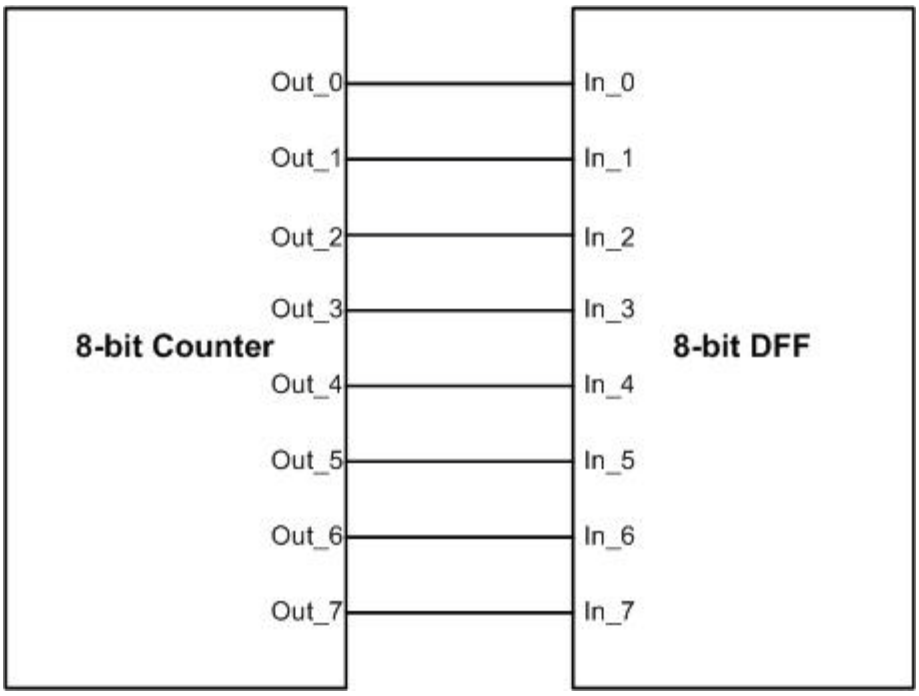


Figure 4.11: Timing diagram of counter and phase detector output

4.2.3.4 Storage (8-bit Parallel D Flip Flop)

Each output bit of the counter is stored an 8-bit master-slave D Flip Flop or 8 D Flip Flops in parallel (Figure 4.12a). Transmission gate logic was used for the master-slave D Flip Flops (Figure 4.12b). The Flip flop operates at the falling edge of the clock. In this case the clock is the phase detector output signal. This means that as the counter stops counting when the phase signal goes low, the DFF captures the final bit from the counter and stores it (Figure 4.13).

a)



b)

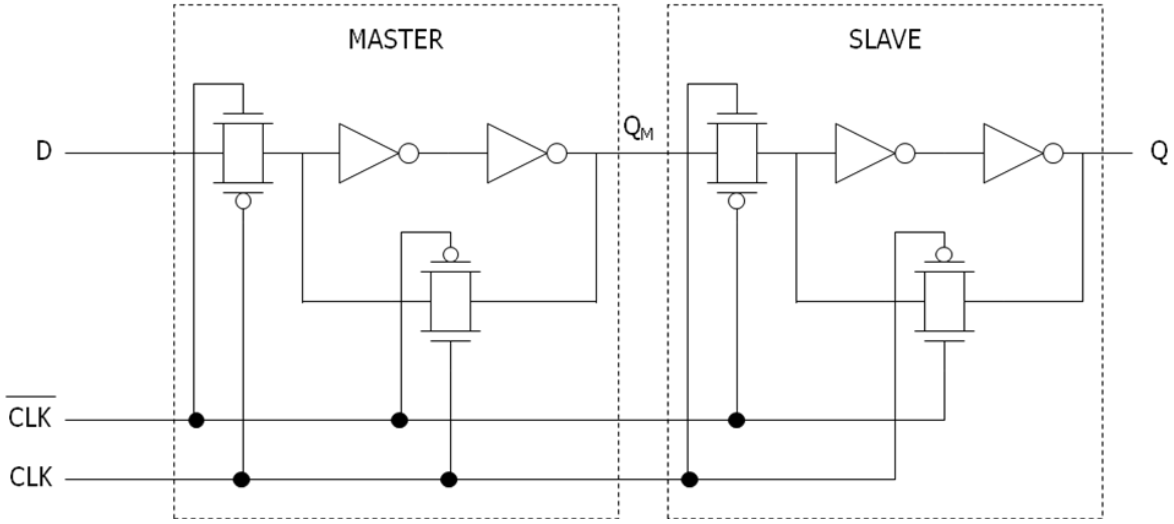
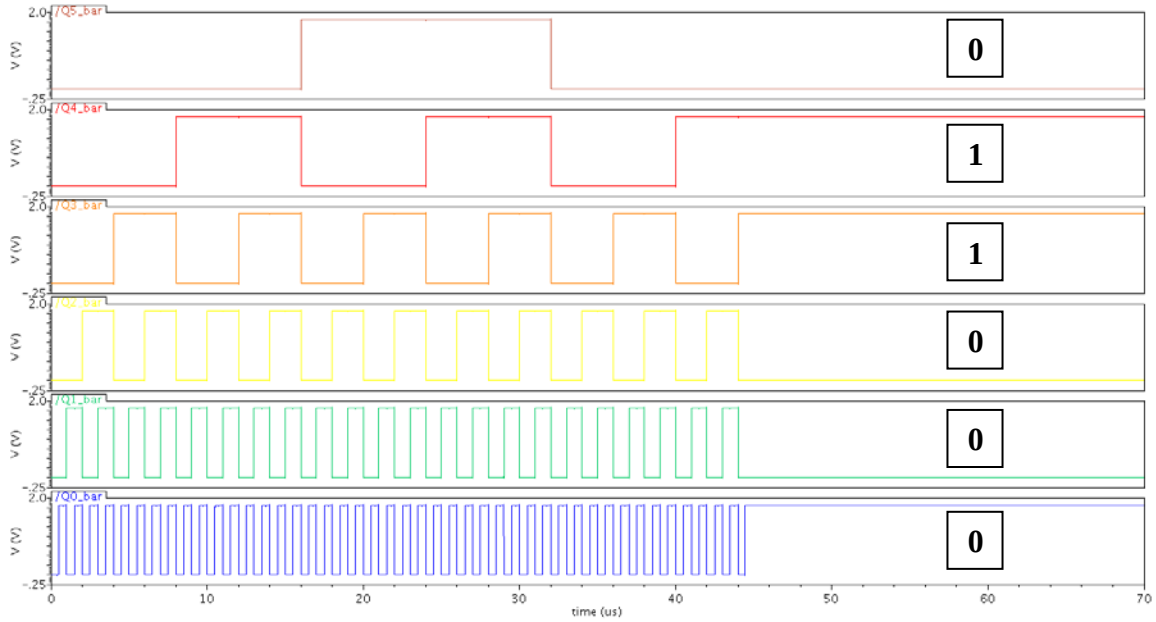


Figure 4.12: a) Parallel connection from Counter to an 8-bit D Flip Flop (DFF) storage and **b)** Transistor level schematic of a single master slave DFF using transmission gate logic architecture [1]

a)

Counter Disabled When Phase Detector Output is Low



b)

8 D Flip Flops Storing the Final Value of the Counter

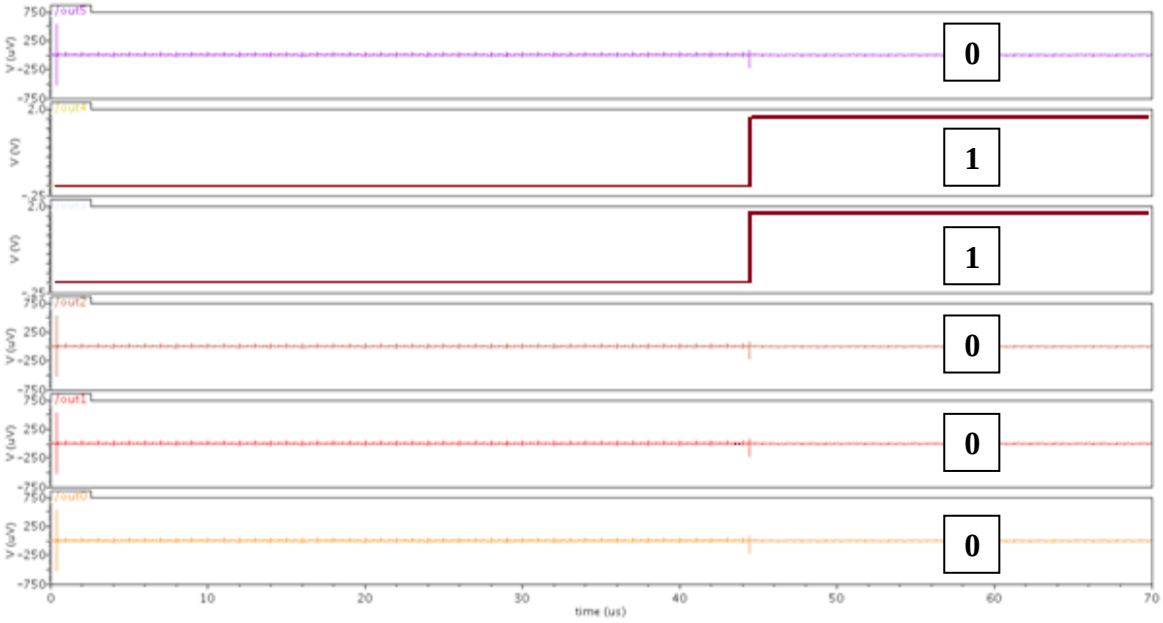


Figure 4.13: a) Counter timing diagram and **b)** Storage timing diagram

4.3 Phase Response Readout System Results

The system described in Section4.2 is integrated and laid out in 0.18um CMOS technology (Figure 4.14). The counter frequency used here was 10MHz. This reduces the need of 3 extra bits and less dynamic power for touch readout. The XOR gate has a glitch so even when there is no touch, the counter counts one bit. Post-layout simulation results at 25ºC are summarized in Table 4-4. Since electronics easily go to temperatures around 40 ºC [1], simulation was also done at that temperature and these results are summarized in Table 4-5. The results are slightly different. This is largely due to the bias change in the CCII final stage amplifier, which can be adjusted with Vbias in our CCII (Figure 4.4). However, in reality, temperature independent biasing is desirable, so a temperature-independent current mirror needs to be used to avoid such effects on the system. For the purpose of proving our concept, our system has successfully shown through simulation that it is capable of detecting the occurrence of touch and its position using a phase response readout scheme on only one layer of metal track.

Table 4-4: Touch for different locations under 25ºC

Touch	x $(k\Omega)$	Bits	Position Number
No	N/A	00000001	1
Yes	0	00011010	26
	13	00011001	25
	26	00010100	20
	39	00010010	18

Table 4-5: Touch for different locations under 40ºC

Touch	x $(k\Omega)$	Bits	Position Number
No	N/A	00000001	1
	0	00010111	23
	13	00010110	18

Yes	26	00010001	17
	39	00001110	14

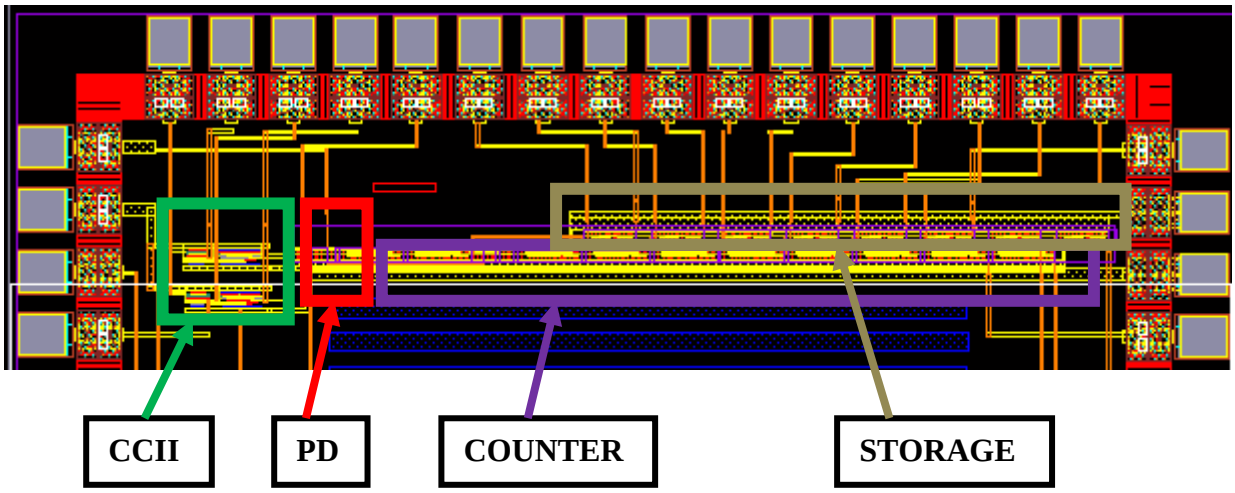


Figure 4.14: System layout

4.4 Future Work

An important step to verify the design would be to test the taped-out chip. Its performance could be compared to conventional voltage response readout schemes. Some possible topics for further research include: optimization of both fabrication and metal track material for touch sensitivity, hihh resistivity and optical transparency; design of temperature independent internal-bias and current mirrors in the CCII; and optimization of the system in terms of robustness and power efficiency.

The research presented here on the novel one-sided touch readout system could perhaps lead to cheaper, less power and brighter integrated touch screen displays for the future.

Chapter 5

Conclusion

Just to summarize, in this thesis we have first explored the drive current and Poole Frenkel emission current of a dual-gate TFT and compared it with a single gate TFT. Thereafter, we compared the instability of dual and single gate TFT and used it to explain the dominant mechanism responsible for the Vt shift. Finally, we proposed a phase response TSP readout scheme that can obtain x and y coordinates of a touch signal using only one metal layer.

First contribution was to show superior drive current capability, and our results showed superior current drive by ~20%. This is different from the expected value of ~50% superior drive current and this was attributed to the ten times higher interface state at the top channel long with a co-planar like TFT structure. This can be improved by passivating the top surface with hydrogen treatment before depositing a-SiNx and using dual-layer a-SiNx deposition.

We also saw a three times increase in Poole-Frenkel emission current under drain voltage of 5V and this was attributed strongly to the increase in gate to drain overlap from the top gate. Further study the effect of top gate on Poole-Frenkel effect, top and bottom gate are needed to be separated. For that, we have provided mask designs that can be used in the G2N Lab at the University of Waterloo. Also provided is a sample MEDICI code for dual-gate TFT in Appendix A for numerical simulation verification of the experimental results.

Finally, we designed, showing post-layout simulation results, a phase response readout scheme that can detect five different locations along a single metal track with a 40kΩ metal track using a CCII running at 200kHz and a Counter running at 10MHz. Further design improvement can be made in the CCII for temperature robustness with temperature independent bias and stacked current mirrors. All these provide possible solutions to make touch screen display cheaper, brighter and more power efficient.

Appendix A

Dual-Gate TFT MEDICI Simulation Code

The following MEDICI code can be used for numerical simulations for a dual-gate TFT. The structure here imitates the dual-gate TFT that is used in Chapters 2 and 3.

```
 COMMENT Start
MESH OUT.FILE=offcurrent.MSH
X.MESH WIDTH=5 N.SPACES=40
Y.MESH WIDTH=0.7 N.SPACES=120


REGION NAME=SINtop NITRIDE Y.MAX=0.2
REGION NAME=nplusS SILICON Y.MIN=0.2 Y.MAX=0.4 X.MAX=1
REGION NAME=nplusD SILICON Y.MIN=0.2 Y.MAX=0.4 X.MIN=4
REGION NAME=SINFILL NITRIDE Y.MIN=0.2 Y.MAX=0.4 X.MIN=1 X.MAX=4
REGION NAME=a-Si SILICON Y.MIN=0.4 Y.MAX=0.45
REGION NAME=SINbot NITRIDE Y.MIN=0.45

ELECT NAME=top_Gate TOP
ELECT NAME=Drain Y.MIN=0.2 Y.MAX=0.4 X.MIN=4
ELECT NAME=Source Y.MIN=0.2 Y.MAX=0.4 X.MAX=1
ELECT NAME=bot_Gate BOTTOM

COMMENT Specify doping
PROFILE  REGION="a-Si"  UNIFORM CONC=4.5*1E15 N-TYPE
PROFILE  REGION="nplusS"  UNIFORM  CONC=1E22   N-TYPE
PROFILE  REGION="nplusD"  UNIFORM  CONC=1E22   N-TYPE

CONTACT  NAME=Source SCHOTTKY VSURFN=1E7 VSURFP=1E7
CONTACT  NAME=Drain  SCHOTTKY VSURFN=1E7 VSURFP=1E7
CONTACT  NAME=top_Gate  SCHOTTKY VSURFN=1E7 VSURFP=1E7
CONTACT  NAME=bot_Gate  SCHOTTKY VSURFN=1E7 VSURFP=1E7

ASSIGN NAME=BNDGP N.VAL=1.8

MATERIAL SILICON  EG300=@BNDGP

MOBILITY MUN0=3 MUP0=0.1

INTERFACE REGION=(SINFILL,a-Si) QF=7*1E11
INTERFACE REGION=(SINbot,a-Si) QF=4*1E11


MODELS SRH

SYMB GUMM CARR=0
```

```
COMMENT SYMB NEWT CARR=0
SOLVE  V(Drain)=0 OUT.FILE=offcurrent.INI

LOAD IN.FILE=offcurrent.INI


ASSIGN NAME=EV N.VAL=-(@BNDGP)/2
ASSIGN NAME=EC N.VAL=(@BNDGP)/2

COMMENT Calculate characteristic length for hole states

COMMENT ASSIGN NAME=PCHR N.VAL=(-0.2-@EV)*LOG(1E18/5E16)
ASSIGN NAME=PCHR N.VAL=0.05

COMMENT Gererate hole traps
TRAP DISTR N.TOT="-(1*1E15+3*1E20*EXP(-(@FENER-@EV)/@PCHR))"
COND="(@FENER<0)" MIDGAP TAUN="1E-9" TAUP="1E-7"
TRAP N.TOT="-(5*1E18)" COND="(@FENER<0)&(@FENER>(-0.25))" MIDGAP
TAUN="1*1E-9" TAUP="1E-7"

COMMENT Calculate characteristic length for electron states
COMMENT  ASSIGN NAME=NCHR N.VAL=(@EC-0.15)*LOG(1E19/1E16)
ASSIGN NAME=NCHR N.VAL=0.020

COMMENT Generate electron traps
TRAP N.TOT="(4.7*1E12+3*1E20*EXP((@FENER-@EC)/@NCHR))"
COND="(@FENER>0)" MIDGAP TAUN="1*1E-9" TAUP="1E-7"
TRAP N.TOT="(5.075*1E18)" COND="(@FENER>0)&(@FENER<0.25)" MIDGAP
TAUN="1*1E-9" TAUP="1E-7"


PLOT.2D GRID FILL

COMMENT SOLVING AND MODELING BEGIN HERE

SYMB GUMM CARR=0
COMMENT SYMB NEWT CARR=0
SOLVE
SYMB NEWT CARR=2
COMMENT SYMB NEWT CARR=1 ELECTRON
METHOD N.DAMP
SOLVE


COMMENT 0-carrier solution with Vd=0.1v
COMMENT SYMB CARRIERS=1  ELECTRON
```

```
COMMENT SOLVE INIT V(Drain)=10 V(bot_Gate)=10 V(top_Gate)=10
OUT.FILE=TEMPSOL

COMMENT LOAD IN.FILE=TEMPSOL

COMMENT PLOT.1D POTENTIA X.ST=0 X.EN=35 Y.ST=0.06 Y.EN=0.06
OUTFILE=POTENTIAL.txt

COMMENT PLOT.1D CONDUC BOT=3 TOP=-3 X.ST=15 X.EN=15 Y.ST=0 Y.EN=0.15
OUTFILE=conduc.txt

COMMENT PLOT.1D VALENC BOT=3 TOP=-3 X.ST=15 X.EN=15 Y.ST=0 Y.EN=0.15
UNCHANGE OUTFILE=valence.txt


COMMENT ID-VG for top gate sweep Vbg=0V
LOG  OUT.FILE=TFT-NT0.IVL
SOLVE  V(Source)=0  V(Drain)=1 V(top_Gate)=-20 V(bot_Gate)=0
ELECTROD=top_Gate VSTEP=.5 NSTEP=80
LOG CLOSE


PLOT.1D   Y.AX=I(Drain)   X.AX=V(top_Gate)  IN.FILE=TFT-NT0.IVL
SYMB=1  Y.LOGARI  OUTFILE=IV_top_0.txt



COMMENT ID-VG for bottom gate sweep Vtg=0V
LOG  OUT.FILE=TFT-NB0.IVL
SOLVE  V(Source)=0  V(Drain)=1 V(bot_Gate)=-20 V(top_Gate)=0
ELECTROD=bot_Gate VSTEP=.5 NSTEP=80
LOG CLOSE


PLOT.1D   Y.AX=I(Drain)   X.AX=V(bot_Gate)  IN.FILE=TFT-NB0.IVL
SYMB=1  Y.LOGARI  OUTFILE=IVbottom_0.txt
```

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