Towards InAs nanowire double quantum dots for quantum information processing

by

Jennifer S. Fung

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

Currently, a major challenge for solid-state spin qubit systems is achieving one-qubit operations on a timescale shorter than the spin coherence time, T_2^*, a goal currently two orders of magnitude away. By taking advantage of the quasi-one-dimensional structure of a nanowire and the strong spin-orbit interaction of InAs, it is estimated that π-rotations can be implemented using electric dipole spin resonance on the order of 10 ns.[1] To this end, a procedure for the fabrication of homogeneous InAs nanowire quantum dot devices is presented herein for future investigations of solid state spin qubits as a test bed for quantum computing.

Both single and double quantum dot systems are formed using local gating of InAs nanowires. Single quantum dot systems were characterized through electron transport measurements in a dilution refrigerator; in one case, the charging energy was measured to be 5.0 meV and the orbital energy was measured to be 1.5–3.5 meV. The total capacitance of the single quantum dot system was determined to be approximately 30 aF. An estimate of the quantum dot geometry resulting from confinement suggests that the quantum dot is approximately 115 nm long. The coupling energy of the double quantum dot system was measured to be approximately 4.5 meV. The electron temperature achieved with our circuitry in the dilution refrigerator is estimated to be approximately 125 mK.

Acknowledgements

On this page and all those that follow, I would like to imprint upon each of them my deepest thanks to and appreciation of all those named and unnamed who have helped me in my journeys. However, that would not be within the regulations.

To my supervisor, advisory committee, teachers, mentors, colleagues, and collaborators: this work would not have been possible without you. To my family and friends: this person would not have been possible without you. To Devin: this adventure would not have been possible without you.

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"Why can't we make them very small, make them of little wires, little elements—and by little, I mean *little*."

— Richard P. Feynman

Chapter 1

Introduction

In the pursuit of more powerful tools with which to improve our understanding of the world and help us solve increasingly complex problems, quantum information processing has revealed itself as an exceptional tool with a staggering breadth of possibilities. Already this relatively young field has yielded many results on the cryptographic, communicational, and computational advantages available when using quantum information.[2]

Within quantum information processing the study of quantum computing is an important, growing field due to its complexity and potential. Even as early as 1992, David Deutsch and Richard Josza demonstrated the potential power of quantum computation with their algorithm for determining whether a function is constant or balanced.[1][3] The Deutsch-Josza algorithm was one of the first demonstrations of a problem that a quantum computer could solve in a single step that would take a classical computer many such steps. These advances, and others, helped accelerate the development of the theory of quantum computation and turn it into the well-developed field it became in the late 1990s.[2]

The progression of quantum computing in the experimental realm has trailed behind its theoretical counterpart, but more recently the development of physical implementations of the quantum bit—or qubit—has begun to accelerate as well. In the many and varied approaches towards a fully realised quantum computer, there are several common fundamental requirements: a scalable system, controlled initialization, long qubit lifetimes, universal computation, and specific measurement capability.[4] Each approach to building a quantum computer has its advantages and difficulties; those of electron spin qubits in quantum dots will be discussed here, as well as the ways in which some difficulties may be overcome in order to test the viability of such a system.

Semiconductor-based approaches towards scalable quantum computing components are promising due to the inherent scalability of these engineered solid-state systems as well as

[1] A constant function is one in which either $f(x) = 0$ or $f(x) = 1$ for all x. A balanced function is one in which $f(x) = 0$ for half of all x, and $f(x) = 1$ for the other half.

the pre-existing wealth of knowledge and experience in semiconductor fabrication techniques inherited from the classical computer industry. Recognizing this, Loss and DiVincenzo put forth a proposal in 1998 for electron spin-based quantum computation using quantum dots, which are semiconductor devices in which electron spins are confined in all three spatial dimensions.[5]

The Loss-DiVicenzo proposal highlighted electron spin qubits in quantum dots, which compared favourably against approaches based on charge states. Firstly, electron spins are natural two-level quantum systems. As well, spin qubits can have longer decoherence times than charge qubits as spins are comparatively weakly coupled to the solid-state environment.[5]

However, a challenge for spin qubits is the creation of a mechanism by which single-qubit operations can be realised on timescales comparable to that of the two-qubit operations and much shorter than that of the spin decoherence time. Recent work has demonstrated that single spin rotations can be accomplished in GaAs two-dimensional electron gas devices by employing a technique known as electric dipole spin resonance (EDSR) via the spin-orbit interaction. However, the timescale demonstrated in these experiments is approximately two orders of magnitude longer than two-qubit exchange operations.[6] In addition to the increased confinement possible in the quasi-one-dimensional structure of a nanowire—a long semiconductor structure with diameters on the order of nanometers—the strong spin-orbit interaction of InAs is hoped to produce faster spin rotations and contribute to the creation of a viable spin qubit system.

A nanowire quantum dot system can be created using depletion regions within the nanowire realised through the use of gates as in a field effect transistor. Electrons are confined radially by the nanowire geometry and axially by these depletion regions, which form barriers to electron tunneling. Additional gates are used to adjust the electrochemical potential within the quantum dots in order to reach the few-electron regime at the cryogenic temperatures needed for EDSR.

1.1 Quantum computing with solid state spin qubits

The five fundamental requirements of quantum computing were outlined by DiVincenzo in 1996:[2] [7]

1. A scalable physical system with well-characterised qubits.

[2]While two more desiderata are often included in discussing a physical system which may also be used for quantum communication, in the case of solid-state electron spin-based quantum computing they are not realistic and so are not germane to this discussion.

2. The ability to initialise qubits in a simple fiducial state, such as $|000\ldots\rangle$.

3. Long decoherence times, much longer than the *gate operation time*.

4. A universal set of quantum gates, such as one-qubit rotations about an arbitrary axis and a two-qubit entangling operation.

5. The ability to measure each qubit specifically.

The way in which a given implementation for quantum computing attempts to fulfill each of these requirements is particular to the capabilities of that system. The electron spin, as an intrinsic two-level quantum system, is a natural choice for a quantum bit. In conjunction with the scalability offered by engineered semiconductor devices, the spin qubit holds promise as a candidate for quantum computing.

A fiducial state can be initialised in an array of single-electron quantum dots by allowing the system to relax into its ground state; this can be accomplished by cooling the device so that distinct energy levels can be resolved, then splitting the spin states through the use of static magnetic fields so that the $|\downarrow\downarrow\ldots\rangle$ state is the ground state, where $|\downarrow\rangle$ indicates the spin-down state.

After a qubit has been initialised or used in computation, measurement of its state is possible by projecting the spin state of the qubit onto the charge basis of the system; taking advantage of the Pauli exclusion principle, the probability of an electron tunneling from one quantum dot into another can be made dependent on the spin state of the electrons in the system, *i.e.* the Pauli spin blockade. The charge state of the quantum dot can then be measured using a quantum point contact, which is a narrow constriction in a wide conductive region that can induce the quantization of conductance and act as a very sensitive electrometer.[8]

In order to implement a generic algorithm on a quantum computer a universal set of quantum gates is required. A complete set of one-qubit rotations together with any two-qubit entangling gate, such as the controlled-not (CNOT) operation, are necessary and sufficient for universal quantum computation.[2] In solid state spin systems, both of these types of quantum operations can be accomplished: one-qubit rotations can be performed conventionally by applying AC magnetic field pulses and by taking advantage of spin precession in the presence of a static magnetic field; two-qubit operations can be achieved by using the tunable exchange interaction between adjacent spin qubits, which occurs when electron wavefunctions overlap, and can be used to swap spin states or perform entangling operations such as $\sqrt{\text{SWAP}}$, which have been demonstrated in as little as 180 ps.[9] However, the magnetic field pulses for one-qubit rotations are infeasible when naïvely scaled down for a quantum dot system.

As a result, a challenge for solid-state spin qubit systems is achieving one-qubit operations on a timescale similar to that of two-qubit operations and, more importantly, much

shorter than the spin coherence time, T_2^*. One method that has shown promise in this regard is EDSR, which uses local electric potentials to excite spin rotations via the spin-orbit interaction. However, while spin coherence in GaAs planar quantum dots has been demonstrated to last several microseconds with the help of refocussing,[9] current implementations of EDSR in these systems have obtained coherent π-rotations, or quantum bit flips, of electron spin qubits only as fast as 55 ns.[10] On the other hand, π-rotations using EDSR in InAs nanowire quantum dots have been estimated to require less than 10 ns, which would allow around 1000 gate operations within the expected coherence time of ~ 3 µs.[1]

1.2 Single-spin rotations

Conventionally, single spin qubit rotations are implemented using pulsed AC magnetic fields. However, due to the physical apparatus necessary for magnetic field generation (*e.g.* solenoid coils or microwave cavities) this method is impractical due to difficulties in scaling down such methods and also due to photon-assisted tunneling. Instead, the spin-orbit interaction combined with small local electric fields can be exploited to generate an *effective* magnetic field to excite the same behaviour using a technique called electric dipole spin resonance (EDSR).

The spin-orbit interaction is a relativistic effect realised when a precessing electron moves through a potential gradient. The potential gradient is created from the semiconductor environment around the electron and includes the effects of confinement, boundaries, external electric fields, and impurities.[11] By causing the electron to translate back and forth across the potential gradient, the electron experiences an oscillating effective magnetic field; when the excitation frequency matches the spin resonance frequency, the electron spin is driven to flip as in a Rabi oscillation. Due to the inherently short spin-orbit lengths in III-V semiconductors, the spin-orbit interaction is enhanced to allow strong coupling of the electron spin to the electric potentials in its environment. The standard Dresselhaus and Rashba spin-orbit terms can both play a role: the Dresselhaus term is non-zero in III-Vs, and can even be enhanced by confinement in some cases; the Rashba term appears when the nanostructure potential possesses lack of inversion symmetry.[12].

In principle, EDSR can be used to implement one-qubit rotations in solid state spin qubits by the application of a static perpendicular magnetic field, B_z, and AC modulation of tunneling barrier potentials, causing the axial position of the quantum dot to oscillate periodically. Recent measurements of the spin-orbit interaction in InAs nanowire quantum dots yielded a spin-orbit length on the order of 200 nm,[13] which is much shorter than in GaAs where it is on the order of micrometres.[12]

In a double quantum dot system, these spin rotations can be observed via spin-to-charge

conversion, which is the process of exploiting the spin-dependent tunneling of electrons into an adjacent occupied quantum dot. This spin-dependent electron tunneling utilises the Pauli spin blockade where electron tunneling can be inhibited due to the Pauli exclusion principle.[14] Thus, spin rotations excited using EDSR can be verified through the observation of coherent Rabi oscillations in transport.

By developing a robust system for the creation of few-electron quantum dots in an InAs nanowire, it is hoped that EDSR can be examined as an effective means of realising one-qubit rotations. Through such investigations, nanowire quantum dots may prove to be a viable test bed for further explorations of spin-based quantum computing and contribute towards a fully realised quantum computer.

Chapter 2

Background

2.1 Quantum dots and nanostructures

Quantum dots are three-dimensional electron confining structures. In fabricated semiconductor quantum dots, electron confinement is possible through the manipulation of electrical potentials in semiconductor structures. While the materials and techniques used in the fabrication of semiconductor quantum dots are similar to those used for other semiconductor devices, quantum effects appear when the size of the confined area is on the order of the Bohr radius of an electron in the material.

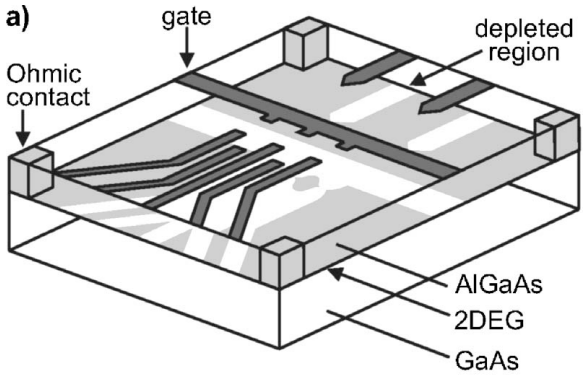


Figure 2.1: An illustration of a planar double quantum dot geometry. One quantum dot is represented by the almond-shaped light grey area visible in the centre of the image. Figure from [15].

In a planar quantum dot structure, as illustrated in Fig. 2.1, one strong direction of confinement is achieved by creating a heterojunction, which allows the formation of a

two-dimensional electron gas (2DEG) at the junction. Confinement in the the other two directions is created by formation of depletion regions due to the application of strong negative voltages to electrodes on the surface of the device. Typically, the size of these types of quantum dots are on the order of hundreds of nanometers in diameter and can be tuned by adjusting the applied voltages.

Such planar quantum dots have been examined extensively and single-electron quantum dots have been achieved[16] as well as single,[17] double,[18] and triple quantum dot systems.[19] In fact, much work has been put into investigating and pushing towards the realisation of the Loss-DiVincenzo proposal for a spin-based quantum computer.[15]

Many of the requirements for a viable realisation of quantum computing have been demonstrated in planar geometry devices. For example, recent work has demonstrated qubit initialization and spin state measurement in a silicon-based quantum dot-based structure. Qubit initialization was performed by creating an energetically preferred ground state through device cooling and Zeeman splitting of spin states. Single-shot measurement—as opposed to ensemble measurement—of the qubit spin state was performed by using Pauli spin blockade to differentiate spin states and then measuring the current through a single-electron transistor integrated into the system.[20]

A universal set of quantum operations have also been demonstrated in planar devices as both two-qubit operations[9] and one-qubit rotations have been executed.[14] The demonstration of one-qubit operations by Nowack, *et al.* utilised EDSR on a planar gallium arsenide quantum dot structure and showed that coherent spin flipping can be achieved on timescales as short as 55 ns. While this demonstration is a factor of four faster than that achieved by pulsed AC magnetic fields, it is still greater than the spin decoherence time measured for the system.[10]

As a result of the limited success of one-qubit rotations in planar quantum dot structures, other geometries have been explored. An alternative geometry that shows promise due to the increased confinement and the structural asymmetry offered by its quasi-one-dimensional geometry is the nanowire quantum dot. In a nanowire quantum dot system, illustrated in Fig. 2.2, two dimensions of strong confinement are achieved by the narrow diameter of the nanowire; the third dimension of confinement is created by applying voltages to local gates in order to manipulate the local potential in the nanowire.[1] A local gate positioned between the gates providing axial confinement is used to change the quantum dot potential; this gate is known as a plunger gate. A global gate, known also as a back gate, may be created using the doped, conductive substrate underneath the nanowire device. The nanowires used in this geometry of quantum dot devices are often less than 100 nm in diameter.[21]

[1] Axial confinement is also possible through the use of heterojunctions, but this variety of nanowire quantum dot is not explored here.

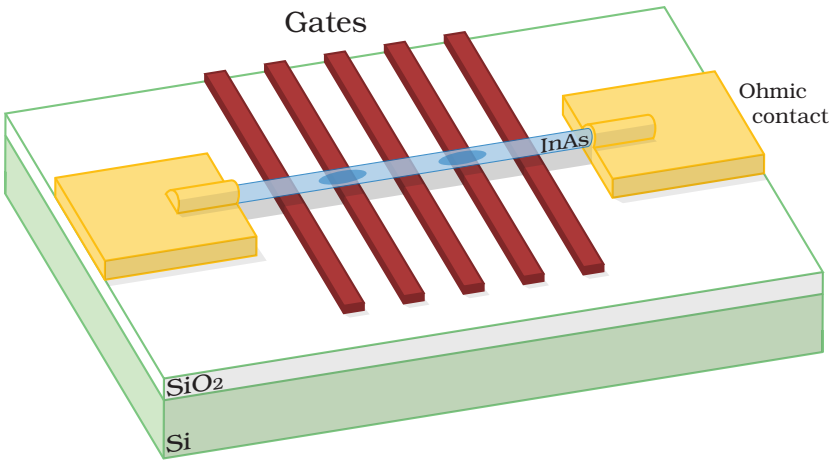


Figure 2.2: An illustration of a bottom-gated nanowire double quantum dot geometry. The two quantum dots (dark blue) are represented in the InAs nanowire (light blue) when confined by tunnel barriers formed using three of the gates (red) with two gates remaining to tune each dot.

2.2 Transport in quantum dots

Electron transport in quantum dots is the sequential tunneling of electrons on and off of a quantum dot as illustrated in Fig. 2.3. At low temperatures, the electron must move to a region of equal or lower electrochemical potential due to conservation of energy at each tunneling event. When an electron makes the complete circuit from the source, through the dots, and into the drain, then a current can be measured. The transport behaviour of a quantum dot is dominated by the Coulomb repulsion between electrons, and the quantum effects that result from the three-dimensional confinement of these electrons.[15]

The Coulomb repulsion between electrons in a quantum dot results in a phenomenon known as Coulomb blockade, wherein an electron is prevented from tunneling into a quantum dot due to the increase in energy required to overcome Coulomb repulsion of electrons already present. This energy increase is known as the charging energy, E_c, and it is assumed in the constant interaction model, described below, that the charging energy can be parametrized by the total capacitance of the system.[22] Coulomb blockade is observable by the formation of diamond-shaped patterns in a two-dimensional intensity plot of the conductance of a quantum dot system, $\frac{\mathrm{d}I}{\mathrm{d}V_\mu}$, where the bias, $V_\mu = V_D - V_S$, is the difference between the potential on the source terminal and the drain terminal, as illustrated in Fig. 2.4. Where Coulomb blockade is in effect, within the diamond shapes, no conductance is measured.

The transport behaviour of a quantum dot can be modeled classically using an electronic

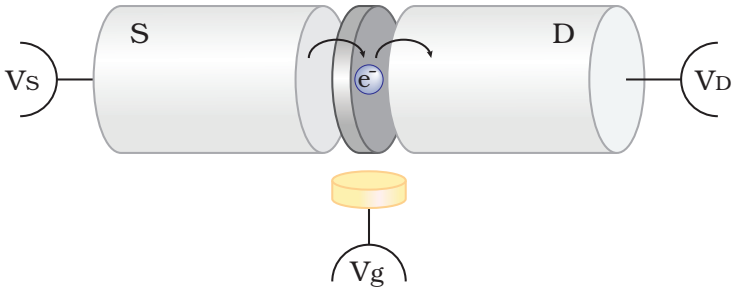


Figure 2.3: An illustration of an electron tunneling through a single quantum dot. The arrangement shown is for a nanowire quantum dot system. The quantum dot (dark grey) is shown with an electron (blue) tunneling into it and out of it again. The source (S) and drain (D) ends of the nanowire (light grey) are labelled. The tuning gate is represented in yellow.

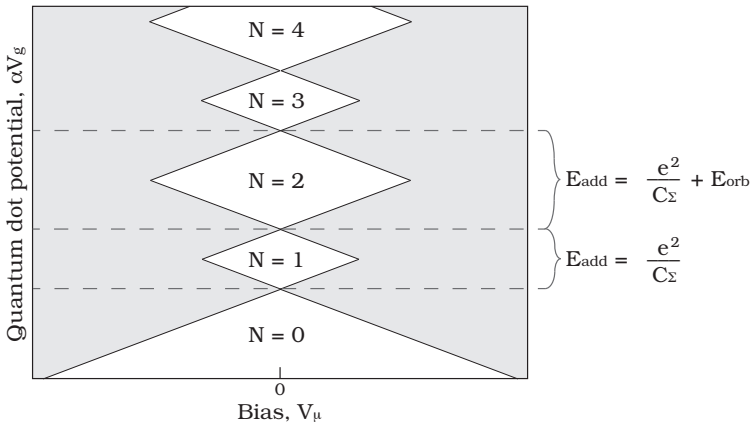


Figure 2.4: A schematic conductance plot for a single quantum dot system. Areas of conductance are shown in grey and areas of no conductance are shown in white. The number of electrons in the quantum dot is labelled in each Coulomb blockade region. When no electrons are in the dot, the region of zero conductance extends downwards and continues to widen.

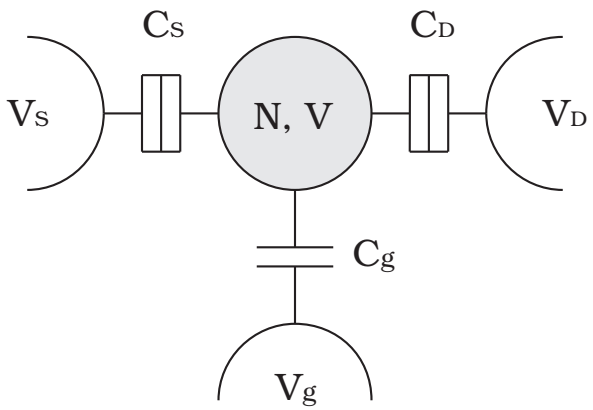


Figure 2.5: A electronic circuit analogue for a single quantum dot system. The quantum dot is represented by the grey node and has a potential V when there are N electrons in it. The source applies a voltage V_S to the system and the drain applies a voltage V_D. The behaviour of the quantum dot can be tuned by adjusting the gate voltage, V_g. The circuit elements labelled C_S and C_D indicate tunneling barriers with capacitive coupling.

circuit analogue. Van der Wiel *et al.* described the behaviour of a single quantum dot using the circuit model shown in Fig. 2.5 to find an expression for the electrostatic potential energy, $U(N)$, of a single quantum dot system carrying N electrons. From this electrostatic potential energy, the work required to change the number of electrons in the quantum dot, known as the electrochemical potential $\mu(N)$, can be found.

Node analysis of the circuit shown in Fig. 2.5 gives the following expression for the potential energy, $U(N)$, of a single quantum dot system with N electrons:

$$\begin{aligned} U(N) =& \frac{1}{2C_\Sigma}\Big(e^2N^2 - 2|e|N\left(C_SV_S + C_DV_D + C_gV_g\right) \\ &+ \left(C_SV_S + C_DV_D + C_gV_g\right)^2\Big) \end{aligned} \tag{2.1}$$

where $C_\Sigma = C_S + C_D + C_g$ and e is the charge of an electron.[23] The electrochemical potential of the dot, $\mu(N)$, can be found by the change in the electrostatic potential energy required to add another electron onto a quantum dot with N electrons:

$$\begin{aligned} \mu(N) &= \frac{U(N+1) - U(N)}{(N+1) - N} \\ &= \frac{e^2}{C_\Sigma}\left(N + \frac{1}{2}\right) - \frac{|e|}{C_\Sigma}(C_SV_S + C_DV_D + C_gV_g) \end{aligned} \tag{2.2}$$

In other words, a change from N electrons to $N+1$ electrons results in the charging energy, $\mu(N+1) - \mu(N) = \frac{e^2}{C_\Sigma}$.

However, the classical treatment of the quantum dot system used above does not capture the full quantum behaviour of the system. The tight confinement of electrons in a quantum dot results in the discretization of its energy spectrum, which is reflected in the electrochemical potential of the dot as an additional term such that

$$\mu(N+1) - \mu(N) = \frac{e^2}{C_\Sigma} + E_{orb} \tag{2.3}$$

where E_{orb} is the splitting between the discretized energy levels.

In order for Coulomb blockade to be observable, the quantum dot must be held at cryogenic temperatures; there are three temperature regimes at which different quantum dot behaviours can be observed:[24]

- $k_B T \gg \frac{e^2}{C_\Sigma}$
  Thermal excitation is too great and so discrete charges cannot be discerned. Coulomb blockade is not observed.
- $\frac{e^2}{C_\Sigma} \gg k_B T \gg E_{orb}$
  Many levels may be excited thermally resulting in electron transport through indistinct levels. Coulomb blockade can be observed, but quantum effects such as energy spectrum discretization cannot.
- $\frac{e^2}{C_\Sigma} \gg E_{orb} \gg k_B T$
  Thermal excitation is low, so only one or a few levels are involved in electron transport. Coulomb blockade and quantum effects can be observed.

By applying the conditions for transport in a single quantum dot system found in Table 2.1 within the quantum Coulomb blockade temperature regime described above, the diamond-shaped features of a characteristic conductance plot can be derived, as seen in Fig. 2.4. These conditions are inequalities comparing the electrochemical potential of the dot with that of the source, $\mu_S = -|e|V_S$, and the drain, $\mu_D = -|e|V_D$, derived from the requirement that at low temperatures electrons can only tunnel into levels in which the electrochemical potential is equal to or below the present electrochemical potential of the electron.

Electron transport in a double quantum dot system can be considered in a manner similar to that of a single quantum dot. A similar circuit analogue can be made: Fig. 2.6 shows the electronic circuit used to describe double quantum dot transport behaviour. Again, node analysis can be used to derive an expression for the electrostatic potential

Nodes	Forward current	Reverse current
Source and dot	$\mu_S \geq \mu(N)$	$\mu_S \leq \mu(N)$
Drain and dot	$\mu(N) \geq \mu_D$	$\mu_N \leq \mu_D$

Table 2.1: The conditions for electron tunneling events between nodes of a single quantum dot system.

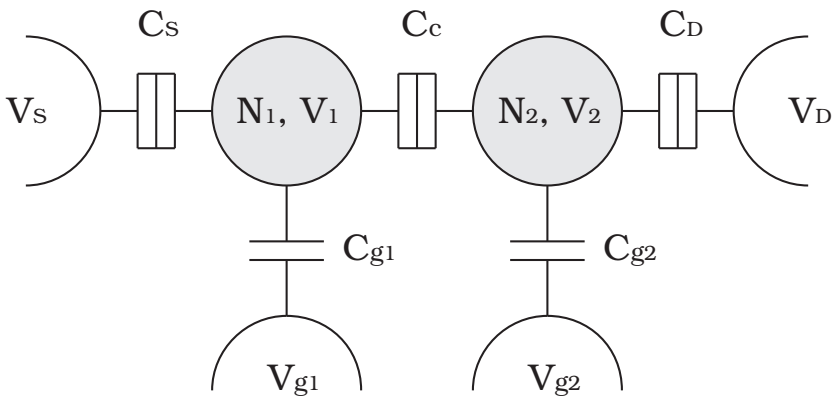


Figure 2.6: A circuit analogue for a double quantum dot system. The quantum dots are represented by the grey nodes. Dot 1 has a potential V_1 when there are N_1 electrons on it, and dot 2 has a potential V_2 when there are N_2 electrons on it. The source applies a voltage V_S to the system and the drain applies a voltage V_D. The number of electrons in dot 1 can be tuned by adjusting the gate voltage V_{g1}, and dot 2 can be tuned using the gate voltage V_{g2}.

energy, $U(N_1, N_2)$, of the system when there are N_1 electrons in quantum dot 1, and N_2 electrons in quantum dot 2.

$$\begin{aligned} U(N_1,N_2) = &\frac{1}{2}E_1N_1^2 + \frac{1}{2}E_2N_2^2 + E_cN_1N_2 \\ &- \frac{1}{|e|}\Big(N_1\big(E_1(C_SV_S + C_{g1}V_{g1}) + E_c(C_DV_D + C_{g2}V_{g2})\big) \\ &\quad + N_2\big(E_c(C_SV_S + C_{g1}V_{g1}) + E_2(C_DV_D + C_{g2}V_{g2})\big)\Big) \\ &+ \frac{1}{2(C_1C_2 - C_c^2)}(C_SV_S + C_DV_D + C_{g1}V_{g1} + C_{g2}V_{g2})^2 \end{aligned} \tag{2.4}$$

where $E_1 = e^2\frac{C_2}{C_1C_2 - C_c^2}$ is the charging energy for dot 1, $E_2 = e^2\frac{C_1}{C_1C_2 - C_c^2}$ is the charging energy for dot 2, and $E_c = e^2\frac{C_c}{C_1C_2 - C_c^2}$ is the charging energy resulting from the capacitive coupling of the two dots. For brevity, the capacitances directly connected to dot 1 are summarized as $C_1 = C_S + C_{g1} + C_c$ and the capacitances directly connected to dot 2 are summarized as $C_2 = C_D + C_{g2} + C_c$. Similarly, the electrochemical potential of the double quantum dot system can be found as:

$$\begin{aligned} \mu_1(N_1,N_2) &= \frac{U(N_1+1,N_2) - U(N_1,N_2)}{(N_1+1) - N_1} \\ &= E_1\left(N_1 + \frac{1}{2}\right) + E_cN_2 - \frac{1}{|e|}\big(E_1(C_SV_S + C_{g1}V_{g1}) \\ &\quad + E_c(C_DV_D + C_{g2}V_{g2})\big) \end{aligned} \tag{2.5}$$

when an electron is added to dot 1, and:

$$\begin{aligned} \mu_2(N_1,N_2) &= \frac{U(N_1,N_2+1) - U(N_1,N_2)}{(N_2+1) - N_2} \\ &= E_2\left(N_2 + \frac{1}{2}\right) + E_cN_1 - \frac{1}{|e|}\big(E_c(C_SV_S + C_{g1}V_{g1}) \\ &\quad + E_2(C_DV_D + C_{g2}V_{g2})\big) \end{aligned} \tag{2.6}$$

when an electron is added to dot 2. As in the single quantum dot system, these expressions for the electrochemical potential indicate the energy required to add another electron to each of the two quantum dots. As a result, the conditions described in Table 2.2 must be satisfied in order for an electron to sequentially tunnel through a double quantum dot device.

Transport phenomena through a double quantum dot system can be characterized using a conductance plot, as in a single quantum dot system, in which the bias, V_μ, is fixed and the effects of the two tuning gates are explored. The effect of changes in the capacitive

Nodes	Forward current	Reverse current
Source and dot 1	$\mu_S \geq \mu_1(N_1, N_2)$	$\mu_S \leq \mu_1(N_1, N_2)$
Dot 1 and dot 2	$\mu_1(N_1, N_2) \geq \mu_2(N_1, N_2)$	$\mu_1(N_1, N_2) \leq \mu_2(N_1, N_2)$
Drain and dot 2	$\mu_2(N_1, N_2) \geq \mu_D$	$\mu_2(N_1, N_2) \leq \mu_D$

Table 2.2: The conditions for electron tunneling events between nodes of a double quantum dot system.

coupling between the two quantum dots is reflected in the shape of the hexagons in the stability diagram as shown in Fig. 2.7. A characteristic conductance plot produced by a double quantum dot system where there exists moderate coupling between the two dots is shown in Fig. 2.7c.

2.3 Indium arsenide nanowires

The experiments using planar quantum dot geometries discussed in Sect. 2.1 showed that solid state spin-based quantum computing may be realizable if one-qubit rotations can be performed on timescales comparable to that of two-qubit exchange operations. As an indium arsenide (InAs) nanowire has a shorter spin-orbit length, on the order of 200 nm, and a larger Landé g-factor than a planar gallium arsenide (GaAs) structure, the spin-orbit interaction is much stronger in InAs, which will contribute to much more effective EDSR and faster spin rotations.[25] For comparison, the spin-orbit length in GaAs is on the order of micrometres.[26]

In its bulk form, InAs has a zincblende crystal structure. It is also possible for InAs to have a wurtzite crystal structure. Unfortunately, the energy difference between these two arrangements is relatively small, on the order of 10 meV per atom, and is affected by surface energies. As a result, the crystal structure can abruptly change from one to another as surface energies and growth conditions alter which crystal structure is more energetically favourable, as shown in Fig. 2.8; this switching of crystal structure forms planar defects. In fact, these planar defects can occur repeatedly to form stacking faults where the crystal structure alternates over length scales as short as several nanometres resulting in a reduction in electron mobility; this is a problem that is shared amongst all III-V semiconductor nanowires.[25]

Despite the difficulties of nanoscale III-V semiconductors, electron mobility in InAs is very high, as much as 18 000 $\mathrm{cm}^2/\mathrm{V} \cdot \mathrm{s}$ in some studies, which implies that the electron mean free path lengths are large.[25] In turn, long mean free path lengthscales indicate that ballistic transport, a regime in which quantum phenomena dominate electron behaviour,

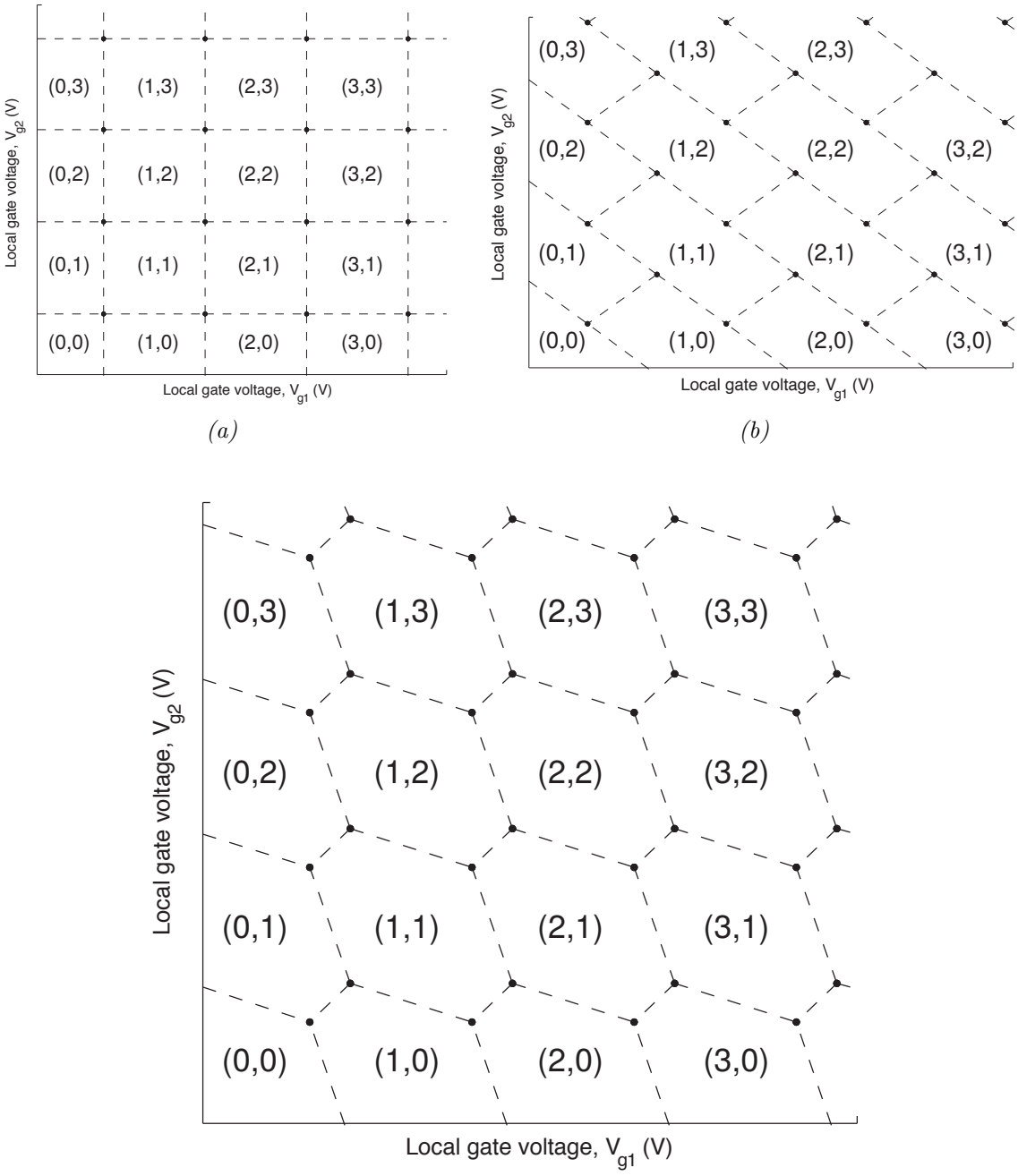


Figure 2.7: Schematic conductance plots for a double quantum dot system generated using Eq. 2.5 and 2.6 where the interdot coupling, C_c, is (a) small, (b) large, and (c) moderate. The number of electrons in each dot is designated by (N_1, N_2). The dashed lines outline the stability diagram regions, and the black dots mark the triple points.

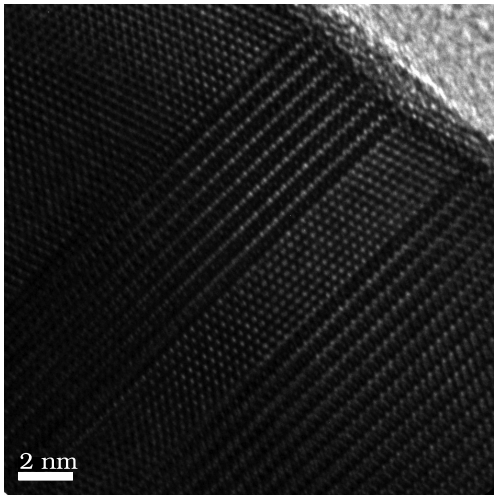


Figure 2.8: A high-resolution tunneling electron micrograph of an InAs nanowire. The bulk of the nanowire (dark grey) is visible in most of the image; the thin surface oxide layer (lighter grey) is visible in the upper right corner in a thin layer less than 2 nm thick. The layers of atoms in the nanowire crystal structure are clearly visible as are the planar defects signaling abrupt changes from wurtzite to zincblende crystal structures and back. Image courtesy of R. R. LaPierre.

in InAs nanowires is possible even over larger structures on the order of micrometres and allowing for easier exploitation of quantum phenomena. In support of the utility of InAs nanostructures, recent work has shown that ballistic transport in InAs nanowires can be demonstrated over length scales on the order of 200 nm.[27]

In addition, InAs is an attractive material for fabrication the creation of an electrical contact exhibiting ohmic behaviour is a relatively simple procedure relative to other semiconductors. In an oxygenated atmosphere, InAs forms a thin native oxide layer, shown in Fig. 2.8, which inhibits the formation of ohmic contacts. However, this oxide layer can be easily etched away using a number of approaches: dilute ammonium polysulfide ($(NH_4)_2S_x$) wet etching, buffered hydrofluoric acid wet etching, or inductively coupled plasma etching for example. A dilute $(NH_4)_2S_x$ solution is favoured here because it also passivates the nanowire surface with sulfur atoms providing a relatively stable surface upon which an ohmic connection can be established.[28] These ohmic contacts are used in a nanowire quantum dot device as the source and drain electrodes.

Chapter 3

Experiments

The quantum dot devices examined in these experiments are electrostatically defined quantum dots in homogeneous InAs nanowires, as illustrated in Fig. 2.2. Quantum dot confinement is accomplished using local gate structures made of unannealed titanium-gold (Ti/Au), fabricated using electron beam lithography, on thermally oxidized silicon (Si) substrates. Ohmic contacts are unannealed nickel-gold (Ni/Au) structures also fabricated using electron beam lithography; for the formation of good ohmic contacts, naturally-occurring oxides on the nanowire are etched away and the exposed surfaces are passivated immediately prior to metal deposition. The Si substrate is p-doped and can be used as a global gate by creating an electrical connection to the back of the device. These nanowires are grown using Au-assisted metal-organic chemical vapour deposition by collaborators at McMaster University in Hamilton, Canada.[29]

Experiments are initially performed at room temperature using a direct current (DC) probe station to verify ohmic behaviour of the devices and also to measure basic electrical characteristics. Promising devices are then selected and installed in a dilution refrigerator for further experimentation at cryogenic temperatures. All experiments are controlled using custom software as detailed in Sect. 3.4.

An example of a device fabricated using the techniques described in Sect. 3.1 is shown in Fig. 3.1. Early devices used a top-gated geometry, where local gates are created over a nanowire instead of under. This approach was favoured due to the theoretically higher capacitance achievable using a gate structure wrapped around the nanowire. However, it was later discovered that fabrication of fine gate structures over a nanowire was very difficult due to excess exposure of the resist along the length of the nanowire causing short-circuiting, and so local gates were then engineered to lie underneath the nanowire. This excess exposure is believed to be a result of electron scattering off of the nanowire due to localization of over-exposure around the nanowire.

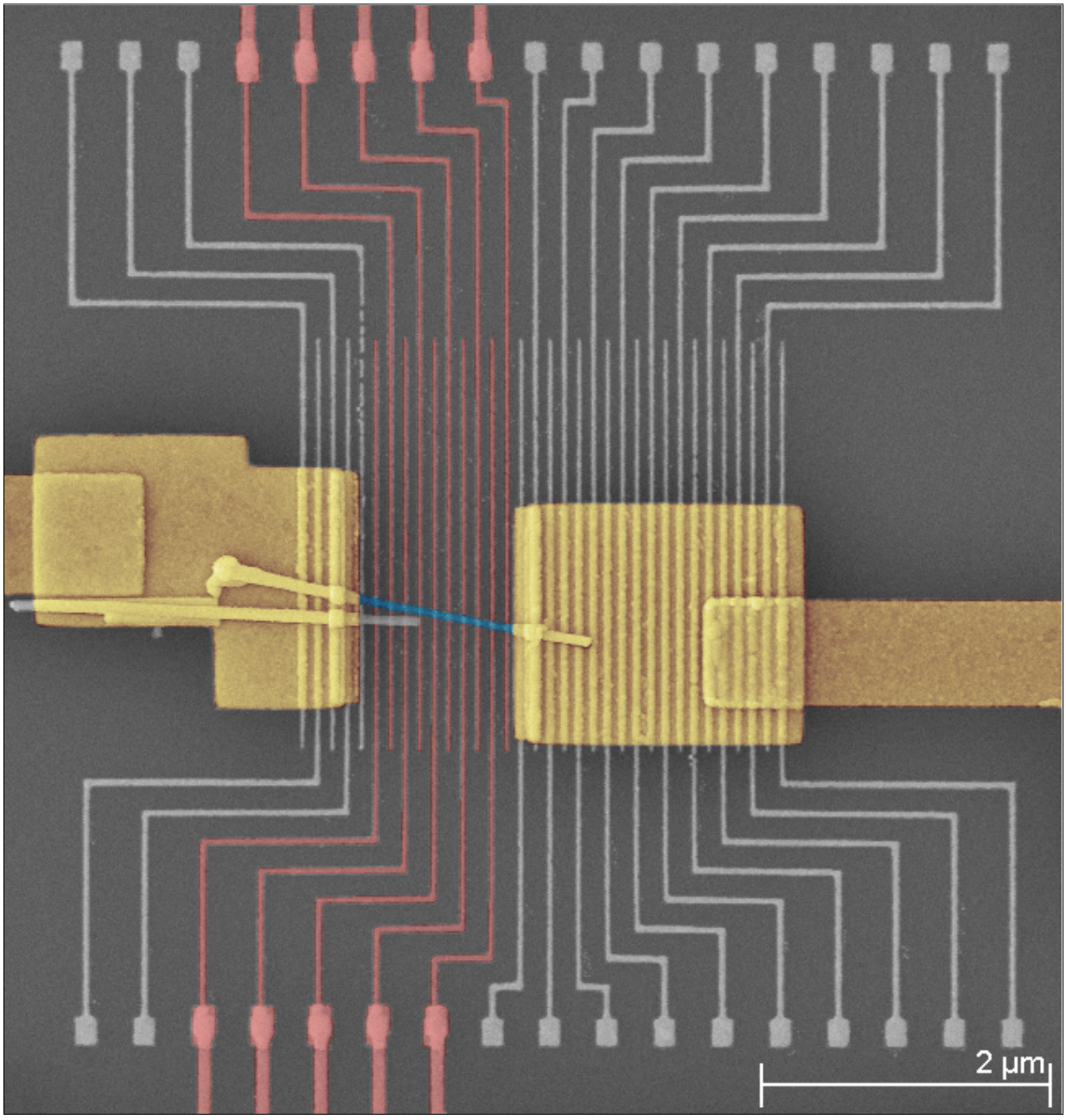


Figure 3.1: A false-colour electron micrograph of a InAs nanowire quantum dot device. The InAs nanowire is highlighted in blue, the source and drain contacts are highlighted in yellow, and the bottom gates for this device are highlighted in red. The diameter of this nanowire is approximately 45 nm.

3.1 Device fabrication

Fabrication of InAs nanowire quantum dots is a delicate process conducted in a controlled Class 10 000 or lower clean room environment in order to prevent contamination. For additional notes on handling and detailed fabrication recipes, see Appendix A.

1. Prepare sample chips

a. *Begin with new p-doped silicon* (Si) *wafers.*

For an effective back gate, very low resistivity Si wafers were used. Early devices, made on Si wafers with resistivities of 0.1–0.4 $\Omega \cdot$ cm, suffered from weak global gates; this was corrected by reducing the resistivity to 0.001–0.005 $\Omega \cdot$ cm through an increase in the doping concentration. This change in resistivity ensures that more charge carriers are present in the global gate creating a stronger effect on the device above it.

b. *Create an insulating silicon dioxide* (SiO_2) *layer.*

Starting with new Si wafers, thermally oxidize the surface of a wafer[1] to create an insulating SiO_2 layer between the device to-be and the conductive region of p-doped Si that will become the back gate.

Early devices used a 200 nm-thick insulting layer, which was initially believed to be the cause of the weak back gates that restricted experimental flexibility in tuning. However, it was later discovered that a more effective back gate could be better achieved by using Si wafers with lower resistivities than by thinning the insulating layer. The devices that yielded the data examined here used a 200 nm-thick insulating layer; however, current devices being produced at the time of this writing possess a 130 nm-thick insulating layer.

c. *Scribe sample chips from an oxidized wafer.*

Using a diamond-tipped scribing tool, scribe an oxidized Si wafer into square sample chips approximate 10 mm $\times$ 10 mm in size. Carefully, blow away any Si fragments or dust using clean and dry N_2 gas.

2. Fabricate bottom gates and alignment markers

a. *Clean sample chip using RCA-1 organics cleaning solution.*

RCA-1 organics cleaning solution:

20 mL ammonium hydroxide (NH_4OH)

[1] Performed by the McMaster Centre for Emerging Device Technologies, McMaster University, Hamilton, Canada

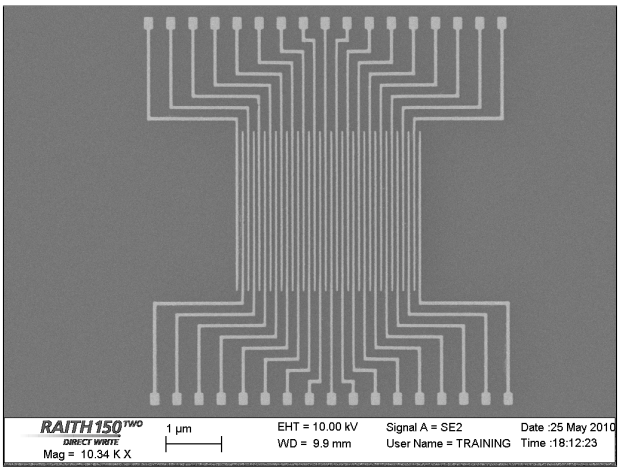


Figure 3.2: An electron micrograph of a bottom gate pattern fabricated using the method outlined in Step 2.

20 mL hydrogen peroxide (H_2O_2)
100 mL deionized water (H_2O)

Soak a scribed sample chip in the above solution for 15 minutes at 60°C. Gently flow deionized water to displace the cleaning solution from the container, then rinse well with fresh deionized water. Carefully, blow dry the sample chip using N_2 gas. Bake the sample chip on a hot plate for 15 minutes at 160°C to ensure proper dehydration prior to further processing. Ensure that sample chips are covered at all times to prevent particle contamination when exposed to air.

This procedure cleans organic contaminants off of sample chips, but does not remove contamination from metal ions or large particle. This step will cause the oxide layer to grow by < 5 nm; however, this oxide growth is insignificant compared to the thermal oxide produced in Step 1b.

b. *Clean sample chip using an oxygen plasma.*

Perform a plasma clean in a reactive ion etcher or other plasma etching equipment using oxygen gas (O_2). If a reactive ion etcher with both inductively coupled plasma (ICP) and parallel plate (RIE) generation capability is used, then an O_2 gas pressure of 100 mTorr introduced at a flow rate of 15 sccm with an ICP power setting of 100 W and a RIE power setting of 30 W will be sufficient when performed for at least 60 s.

This procedure etches away any remaining organic residues from the surface of the sample chip.

c. *Spin coat a 200* nm*-thick layer of 950K PMMA A4*[2].

[2]MicroChem Corp, Newton, USA. http://www.microchem.com

Spin coat polymethyl methacrylate (PMMA) onto a sample chip using the following recipe, then bake the resist onto the sample chip using a covered hot plate for 15 minutes at 180°C.

Bottom gate PMMA spin coating recipe:

i. Speed up for 10 s to 500 rpm.
ii. Spin for 45 s at 4000 rpm.
iii. Slow down for 5 s to 0 rpm.

PMMA is a positive electron beam resist, which means that the areas exposed to the electron beam will be dissolved away when developed in Step 2e.

d. *Write arrays of bottom gate patterns and alignment marks onto the resist layer using an electron beam lithography system.*

Using a 30 kV electron beam through a 10 µm aperture, a dose of 395 $\mu C \cdot cm^2$ was used to create the bottom gate patterns. The beam current during this procedure was measured to be about 43.5 pA on a Raith 150-TWO electron beam lithography system.

This step produces the patterns that will serve as the templates for the metal film-covered areas of the sample chip that will later become the bottom gates. An area dose is used avoid the inconsistent exposure that can result from a line dose, causing lift off problems in Step 2h.[3] The bottom gate lines are written as 30 nm-wide strips with a pitch of 100 nm; however, due to widening of the pattern when exposed, the final gates are approximately 40 nm wide.

e. *Develop the resulting patterns using a solution of methyl isobutyl ketone (MIBK) in isopropanol (IPA) for 60 s.*

Submerge the exposed sample chip in a 1:3 solution of MIBK:IPA for 60 s at room temperature without agitation, then rinse thoroughly in IPA for at least 30 s to stop development. Carefully blow dry the sample chip using N_2 gas.

The above solution was selected in order to produce high resolution detail; however, more concentrated solutions can be used for larger features or thicker resists if resolution of detail is not important. PMMA is a positive resist, so the resulting patterns should be clear where the electron beam has been applied. However, negative resist behaviour can result if the electron beam dose to the PMMA is too high due to cross-linking.

f. *Descum the resist patterns using a weak oxygen plasma.*

Perform an oxygen plasma descum in a reactive ion etcher or other plasma etching equipment using O_2 gas to etch 5–10 nm of PMMA. Using a reactive

[3]Line doses differ from area doses in the manner in which the resist is exposed. A line dose creates a single intense line of exposure, whereas an area dose produces a wider exposure of more uniform intensity.

ion etcher with ICP generation capability, an O_2 gas pressure of 10 mTorr introduced at a rate of 5 sccm with an ICP power setting of 30 W will etch 5–10 nm of PMMA after 20 s.

This procedure ensures that areas of the bottom gate pattern that have been dissolved away will be free of residues prior to metal deposition and improve lift off results.

g. *Deposit a 15 nm-thick layer of titanium* (Ti)*, then a 25 nm-thick layer of gold* (Au).

Titanium and gold are deposited using electron beam evaporation to allow slow and controlled deposition rates in order to improve the quality of the resulting film. Both the Ti and Au films are deposited at a rate of 1 Å/s. Deposition should occur without carousel rotation and the deposition angle should be as small as possible; ideally, the sample chip should be mounted directly above the metal source. Rotation or angled deposition can cause problems when lift off is performed, resulting in excess film adhesion and short circuiting of the pattern due to large areas of remaining metal film.

This procedure creates the thin unalloyed Ti-Au film that will become the bottom gates. Ti is used as an adhesion layer to ensure that the Au film will stay adhered to the substrate surface throughout processing.

h. *Lift off the remaining resist and extraneous areas of metal using Remover PG*[4]*.*

Submerge the sample chip in Remover PG for at least 24 hours at room temperature, then heat to 80°C for 30 minutes with mild agitation. When extraneous pieces of metal film have been removed, rinse thoroughly with IPA. Carefully, blow dry the sample chip using very lightly applied N_2 gas.

Gentle squirting of Remover PG onto the surface of the submerged chip may be necessary to encourage the metal film to tear away from the chip if edges or corners of metal film remain attached to the sample chip. All film must be detached from the sample chip prior to the removal of the sample chip from the Remover PG as a second lift off attempt is not effective due to stiction.

3. Deposit InAs nanowires

a. *Prepare a suspension of* InAs *nanowires in IPA.*

Prepare a new suspension by ultrasonicating a small piece of InAs nanowire growth substrate in IPA for 15 s at a medium setting of ultrasonic agitation.

[4]MicroChem Corp, Newton, USA. http://www.microchem.com

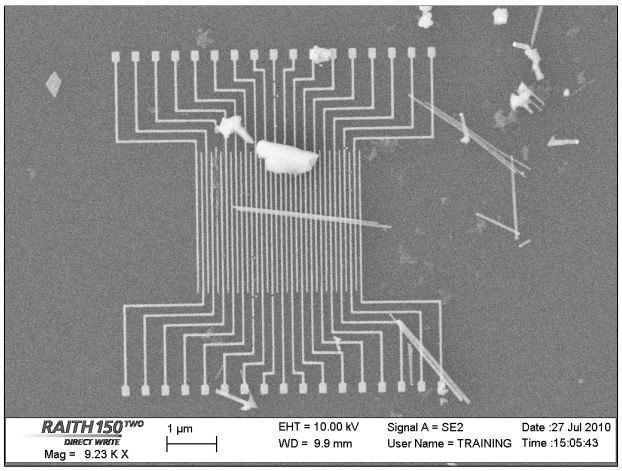


Figure 3.3: An electron micrograph of InAs nanowires deposited, using the method outlined in Step 3, onto a bottom gate pattern.

Remove the growth substrate prior to use or storage. Previously prepared suspension can be used again by ultrasonicating the suspension for 10 s at a medium setting to redistribute nanowires which may have settled into clumps.

A suspension of InAs nanowire in IPA should be clear with a faint dark tint, but not a turbid grey colour. Large particles can contaminate the suspension as a result of the ultrasonication of the growth medium so filtering the suspension using Grade 1 (11 µm pore) filter paper can remove larger particles and drastically improve the quality of the nanowire suspension, but it will also somewhat lower the concentration of nanowires in the suspension.

b. *Disperse* InAs *nanowires across the surface of the sample chip.*

Spin coat the nanowire suspension at low speed over the surface of the substrate as the isopropanol evaporates using the following recipe.

InAs nanowire spin coating recipe:

i. Rest for 90 s at 0 rpm.

ii. Spin for at least 300 s at 500 rpm.

The acceleration for the spin step should be as slow as possible to avoid ejecting nanowires from the surface of the sample chip. The spinning step should continue for at least as long as there remains any droplets of IPA visible on the surface of the sample chip. Continued spinning during the evaporation of the final droplets IPA is important to ensure a good distribution of nanowires on the surface of the sample chip free of clumping.

A good distribution of nanowires is approximately 15–20 evenly dispersed nanowires per 10 000 µm^2.

c. *Examine* InAs *nanowire positioning over bottom gate patterns using a scanning electron microscope.*

Using a scanning electron microscope, find and select suitably positioned nanowires and take detailed micrographs with position measurements for use in designing bottom gate contact electron beam lithography patterns. Thinner nanowires, approximately 20–40 nm in diameter, positioned perpendicular to the bottom gate lines are preferred to allow for the formation of smaller quantum dots. The positioning of the bottom gate patterns relative to position markings should be noted to expedite device location later.

4. Fabricate gate contacts and nanowire fastening strips

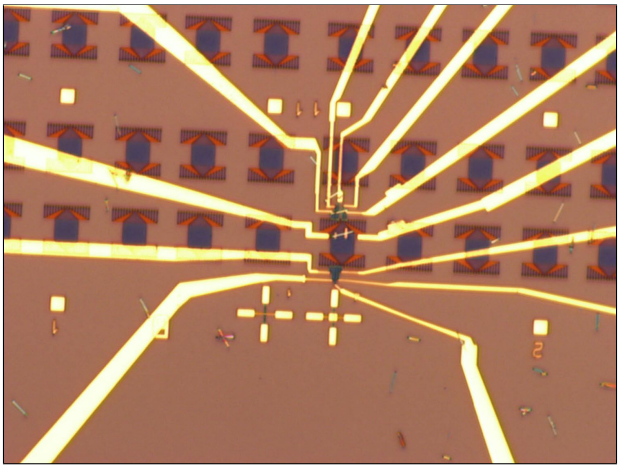


Figure 3.4: An optical micrograph of contacts fabricated to extend the selected bottom gates for integration into a larger circuit using the method outlined in Step 4. Two cross-shaped alignment marks are visible directly below the selected bottom gate pattern, and six small square position markings are also visible towards the edge of the image. As well, two very small strips of gold are visible on the ends of a InAs nanowire located on the selected bottom gate pattern; these strips secure the nanowire in place in preparation for more processing.

a. *Spin coat a 220 nm-thick layer of 950K PMMA A4.*

Spin coat PMMA onto the sample chip using the following recipe, then bake the resist onto the sample chip using a covered hot plate for 15 minutes at 180°C.

Gate contact PMMA spin coating recipe:

i. Speed up for 10 s to 500 rpm.

ii. Spin for 45 s at 3000 rpm.

iii. Slow down for 5 s to 0 rpm.

b. *Write gate contact patterns onto the resist layer using an electron beam lithography system.*

Using a 30 kV electron beam and a 30 µm aperture, a dose of 420 $\mu C \cdot cm^{-2}$ was used; the beam current measured on a Raith 150-TWO electron beam lithography system was about 300 pA. Included in the gate contact patterns are small areas at the ends of the selected nanowire where metal film will firmly affix the nanowire to the substrate in preparation for further processing.

c. *Develop the resulting patterns using a 1:3 solution of MIBK in IPA for 60 s.* (See notes on Step 2e.)

d. *Descum the resist patterns using a weak oxygen plasma.* (See notes on Step 2f.)

e. *Deposit a 25 nm-thick layer of* Ti*, then a 35 nm-thick layer of* Au. (See notes on Step 2g.)

f. *Lift off the remaining resist and extraneous areas of metal using Remover PG.* (See notes on Step 2h.)

5. Fabricate source and drain contacts, and bonding pads

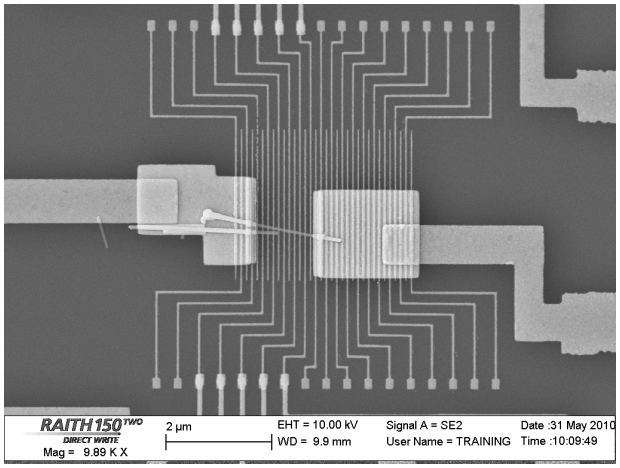


Figure 3.5: An electron micrograph of a nanowire device after source and drain contacts have been fabricated using the method outlined in Step 5.

a. *Spin coat a 350 nm-thick layer of 950K PMMA A4.*

Spin coat PMMA onto a sample chip using the following recipe, then bake the resist onto the sample chip using a covered hot plate for 15 minutes at 180°C.

Source and drain contact PMMA spin coating recipe:

i. Speed up for 10 s to 500 rpm.
ii. Spin for 45 s at 1200 rpm.
iii. Slow down for 5 s to 0 rpm.

b. *Write bonding pads and ohmic contact patterns onto the resist layer using an electron beam lithography system.*

Using a 30 kV electron beam and a 30 µm aperture, a dose of 440 $\mu C \cdot cm^{-2}$ was applied; the beam current measured on a Raith 150-TWO electron beam lithography system was about 300 pA.

c. *Develop the resulting patterns using a 1:3 solution of MIBK in IPA for 60 s.*
(See notes on Step 2e.)

d. *Descum the resist patterns using a weak oxygen plasma.*
(See notes on Step 2f.)

e. *Etch oxides* (InO_x *and* AsO_x) *off of the surface of the nanowires, and passivate nanowire surface with sulfur atoms.*

Submerge the sample chip in a brightly illuminated 0.5% solution of 3M ammonium polysulfide ($(NH_4)_2S_x$) for 30 minutes at 55°C. Flow deionized water to displace the solution from the container, then rinse well with fresh deionized water. Carefully, blow dry the sample chip using N_2 gas. The temperature of the solution should be monitored closely and the container should be sealed to avoid solution degradation.

Sulfur passivation enables a better ohmic contact to be formed between the InAs nanowire and the metal film.

f. *Deposit a 30 nm-thick layer of nickel* (Ni)*, then a 50 nm-thick layer of* Au.

Both the Ni and Au films are deposited at a rate of 1 Å/s.
(See notes on Step 2g.)

g. *Lift off the remaining resist and extraneous areas of metal using Remover PG.*
(See notes on Step 2h.)

3.2 Room temperature experimental setup

Electron mobility experiments were conducted at room temperature using a probe station consisting of a Motic SMZ-168 stereomicroscope[5] with an Amscope HL250-OYS 150 W

[5]Motic, Xiamen, China

halogen light source[6]. Devices are probed using BeCu probes with 10 µm radius tips held by Everbeing EB-700 three-axis micropositioners[7] and connected to an Agilent Technologies E5262A 2-Channel High Speed Source Monitor Unit through a 1 kHz RC filter,[8] and controlled using LabVIEW software created in-house via a National Instruments GPIB controller.

3.3 Low temperature experimental setup

Low temperature experiments were conducted inside an Oxford Instruments DR200 cryogen-free dilution refrigerator system with an integrated 8 T superconducting magnet. The dilution refrigerator has a cooling power of 200 µW at 100 mK and has achieved base temperatures as low as 20 mK. It achieves these low temperatures using the multi-stage cooling approach shown in Fig. 3.6.

The base temperature is measured using a resistive ruthenium oxide (RuO) temperature sensor mounted on the mixing chamber plate. The dilution refrigerator was outiftted for low-noise electronic transport experiments using custom equipment as described below.

3.3.1 Circuitry and filtering

Direct current (DC) signals used for transport measurement and the control of electrostatic potentials in the device must be filtered for electrical noise to avoid uncontrolled excitation of the device. Fig. 3.7 shows a schematic of the low-temperature experiment arrangement.[9]

The first stage of filtering occurs at room temperature and consists of a Π filter (Fig. 3.7) on each DC line enclosed within a breakout box made in-house. These Π filters are effective at removing AC signals in the middle frequency range starting from 10 MHz.

DC signals are transmitted into the dilution refrigerator using a Fischer[10] multi-pin connector fastened to twisted pairs of solid-core manganin wire woven into a ribbon cable. This cable is heat sunk at every cooling stage through compressed contact between heat sinking plates. At the mixing chamber plate, the ribbon cable ends in a 25-pin D-subminiature

[6] American Scope, Chino, USA

[7] Everbeing Int'l Corp, Hsinchu, Taiwan

[8] This RC filter was installed after it was discovered that the Agilent E5262A source output a fast electrical transient when a sweep of voltages was performed. It is suspected that these electrical transients damaged several devices in testing.

[9] Radio-frequency (RF) wiring and components were not used for the experiments described in Ch. 4; for details on the RF circuitry and filtering, see Appendix B.

[10] Fischer Connectors SA, Saint-Prex, Switzerland

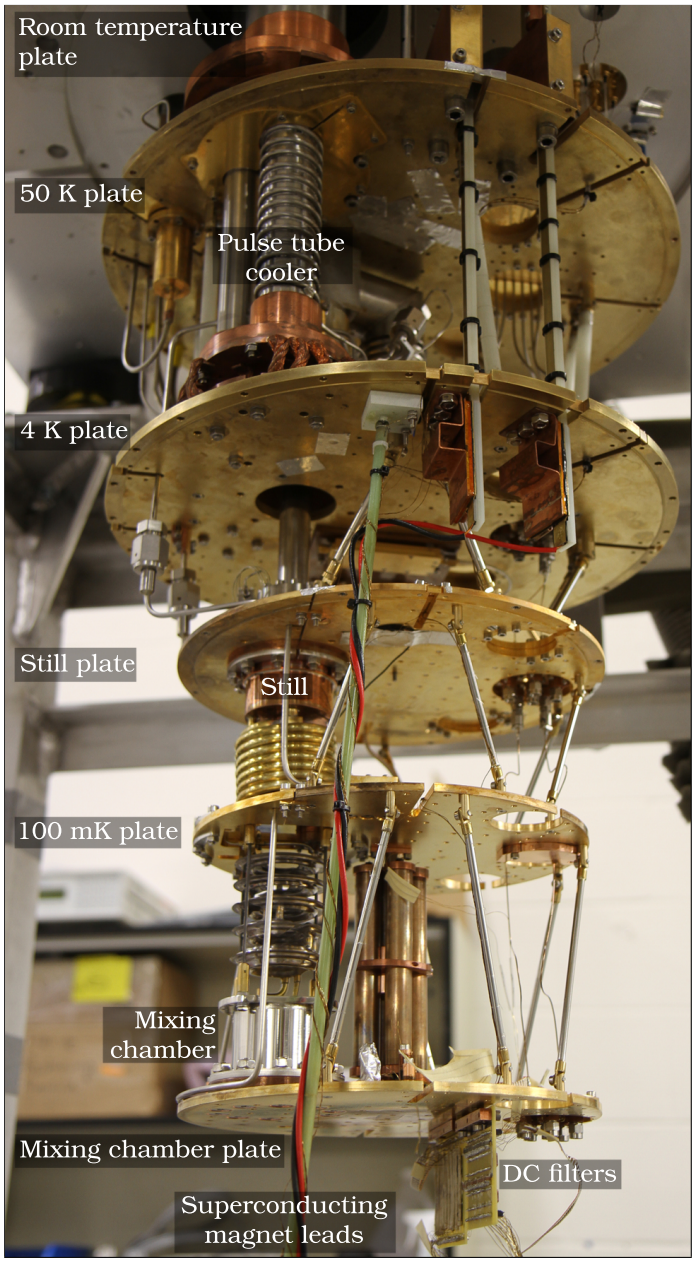


Figure 3.6: A photograph of the interior of the Oxford Instruments DR200 cryogen-free dilution refrigerator used for cooling low temperature experiments. The cooling stages have been labelled.

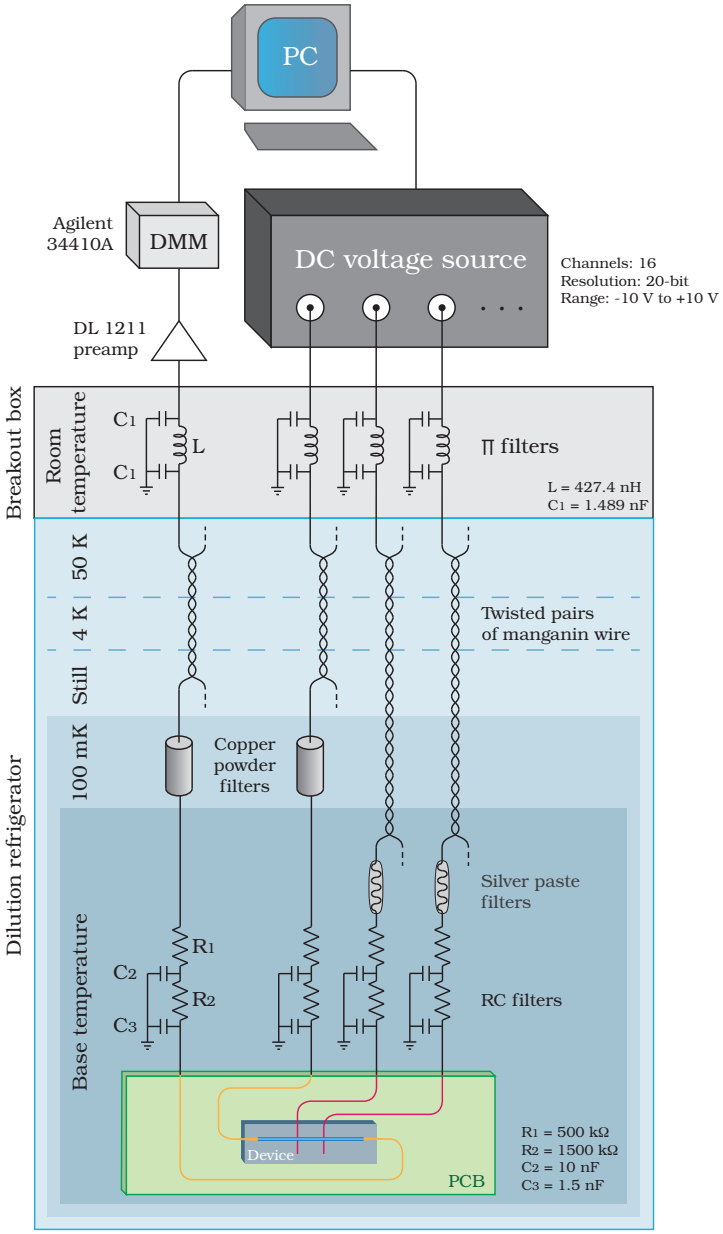


Figure 3.7: A schematic of the DC experiment setup for a single quantum dot with filtering stages shown. The source and drain contacts are shown on the printed circuit board (PCB) assembly in orange, and the bottom gates are shown in red; for clarity, the InAs nanowire of the device is represented in blue. The portions of the setup shown outside of the dilution refrigerator—the breakout box, the DC voltage source, the digital multimeter (DMM), the preamplifier, and the computer (PC)—are at room temperature.

connector. At this point, four DC lines reserved for ohmic contacts are distinguished from the DC lines for gates and filtered separately.

The second stage of filtering consists of a powder filter designed to remove high frequency signals. In the four ohmic contact lines, copper powder filters (Fig. 3.8) are mounted beneath the 100 mK plate and enclose approximately 1.5 m of wire wound in a helix. These copper powder filters have an attenuation of at least 60 dB above 10 GHz. In the gate lines, miniature powder filters (Fig. 3.9) are mounted on printed circuit boards beneath the mixing chamber plate and consist of small helices of wire coated in silver paste. These miniature filters have an attenuation of about 80 dB above 12 GHz.[11]

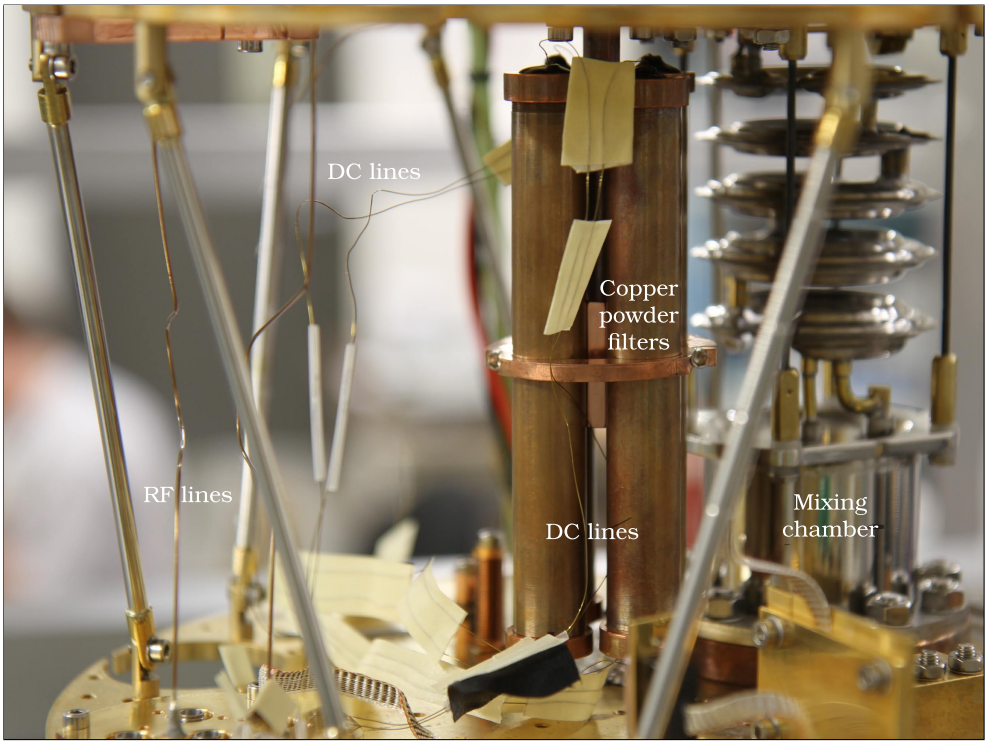


Figure 3.8: A photograph of the copper powder filters, suspended from the 100 mK plate, used in filtering DC lines (labelled) devoted to the ohmic contacts. The remaining unlabelled gate DC lines are shown along the bottom of the image woven into a white ribbon cable. The RF lines (labelled) are semi-rigid 0.086" beryllium copper coaxial cables stretching from the 100 mK plate to the mixing chamber plate and installed for high frequency excitation experiments.

The last stage of filtering consists of two-stage RC filters (Fig. 3.9) on all DC lines in

[11]See Appendix B.1 for attenuation data.

order to remove low frequency noise. The RC filters used on the ohmic contact lines pass signals below 1 kHz;[12] the RC filters used on the gate lines pass signals below 20 Hz.

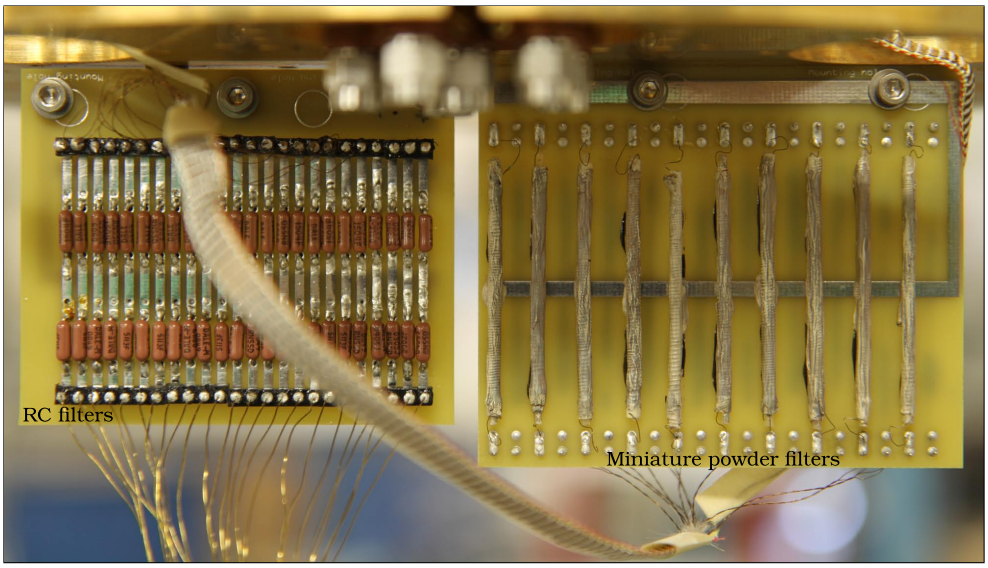


Figure 3.9: A photograph of the miniature powder filters used in filtering DC gate lines and the RC filters used in filtering all DC lines. These filters are mounted to the bottom of the mixing chamber plate.

The DC lines passing through the dilution refrigerator are finally attached to the device through a multi-line DC adapter mating with the printed circuit board (PCB) assembly, all of which were designed in-house.

3.3.2 Device mounting

Devices are installed in the dilution refrigerator using the apparatus shown in Fig. 3.10, which is mounted to the bottom of the mixing chamber plate. Wire bonding is used to electrically connect a device to the PCB assembly, which is enclosed within a shield designed in-house and constructed of oxygen-free high thermal conductivity (OFHC) copper. The PCB assembly consists of a RF-capable PCB connected to a PCB for DC lines fastened to the back; the 24-line DC adapter is a small PCB that mates to the DC PCB as shown in Fig. 3.11. The shield physically protects the device, thermally anchors the PCB assembly to the mixing chamber plate via a OFHC copper support rod designed in-house, and shields the device within from radiative heating from the still shield immediately surrounding it.

[12] A higher cutoff frequency was selected for the ohmic contact lines so that a lock-in amplifier technique can be used to measure differential conductance directly.

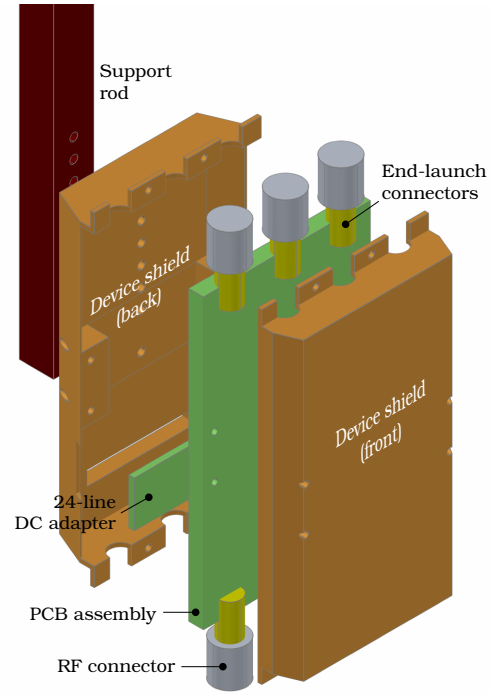
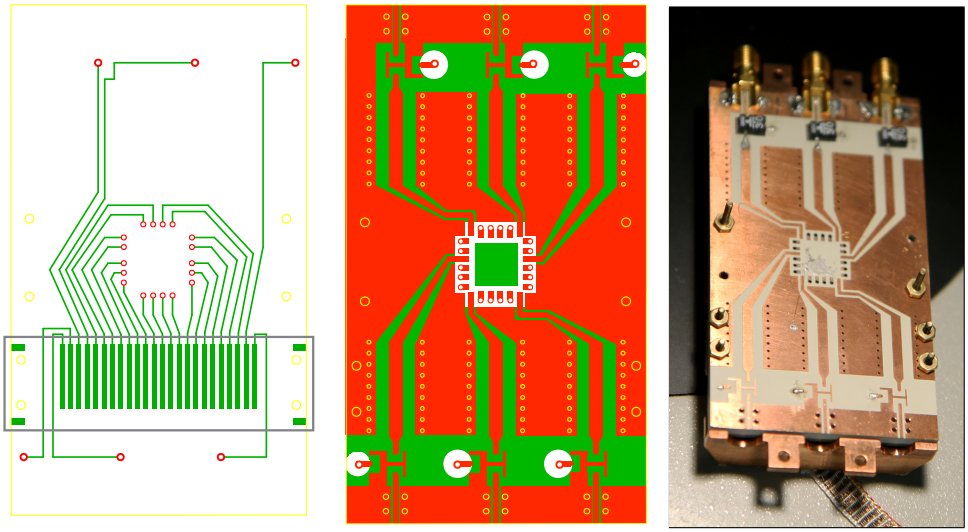


Figure 3.10: A exploded rendering of the lower section of the device mounting assembly including the PCB assembly. The support rod extends upwards to connect the assembly to the mixing chamber plate.



(a) *(b)* *(c)*

Figure 3.11: The PCB assembly is made of two PCBs secured together back-to-back and connected through matching vertical interconnect accesses: (a) a PCB designed for DC lines with a section, outlined in grey, to mate with the 24-line DC adapter, and (b) a PCB for RF signals and device mounting. These images are the PCB design patterns; devices are mounted in the green square in the centre of (b). (c) A photograph of the assembled PCBs in the back half of the device shield. SMA end-launch connectors (gold) and surface-mount bias tees (black) used in RF experiments are visible towards the top of the PCB. The RF PCB can support as many as six high frequency connections using co-planar striplines designed for 50 Ω impedance.

3.3.3 DC experiment components

As shown in Fig. 3.7, devices used in low temperature DC experiments are connected to components outside of the dilution refrigerator. The terminal components of the system—the custom 16-channel DC voltage source designed in-house and made by Science Technical Services[13] and Agilent[14] 34410A digital multimeter—are controlled by a computer. The output of each channel of the DC voltage source is controlled using LabVIEW instrumentation software created in-house. Signals from the device are passed through a DL Instruments[15] Model 1211 current-to-voltage preamplifier and into the Agilent multimeter. The DL 1211 preamplifier has a sensitivity range from 10^{-3} to 10^{-11} A/V, where the input is in the form of amperes of current and the output is in voltage. Measurements from the multimeter are then sent back to the computer for data compilation and analysis.

3.4 Software

As all experiments relied on a large quantity of data and electronic equipment, the experiments were automated so that a computer could be used to control the various components and read the measurements simultaneously.

3.4.1 Probe station software

The probe station used for testing devices at room temperature prior to their installation in the dilution refrigerator used a LabVIEW virtual instrument called OneStep, which was created in-house to control the voltages applied and read the current measurements from the Agilent E5262A Source Monitor Unit. The software is used to perform simple stepped voltage sweeps applied to an ohmic contact terminal, displays and saves the raw data, and calculates the resistance of the nanowire device. An additional voltage source is also used to vary the global gate when the probe station is used to perform measurements to determine the peak room temperature electron mobility of a device. Fig. 3.13 shows the front panel of the probe station software.

3.4.2 Low temperature transport measurement software

Low temperature experiments in the dilution refrigerator were managed using an extensive multi-function LabVIEW software package called FMA, which was adapted from software

[13]University of Waterloo, Waterloo, Canada
[14]Agilent Technologies, Inc, Santa Clara, USA
[15]DL Instruments, Ithaca, USA

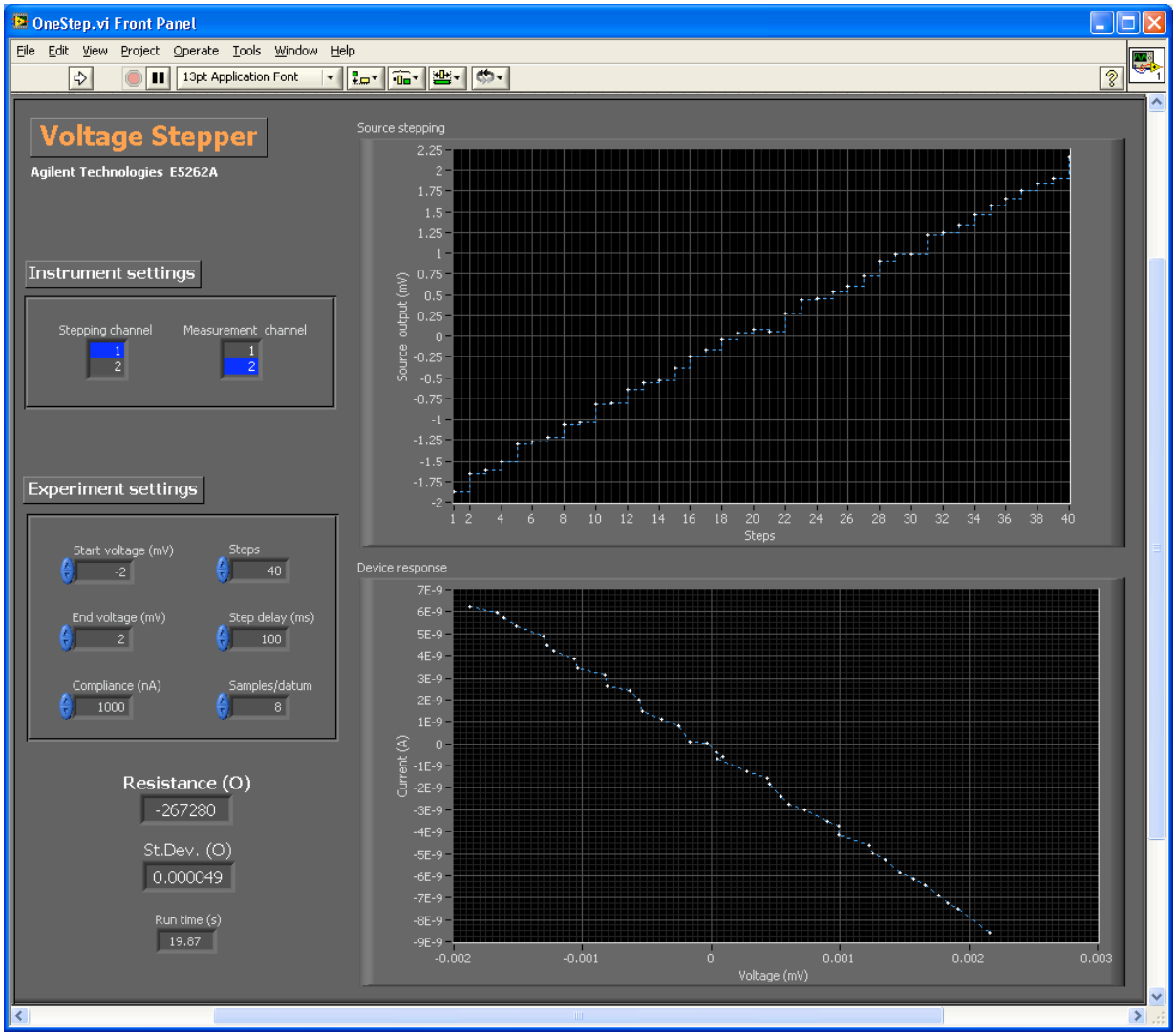


Figure 3.12: The front panel of the probe station LabVIEW software used to test devices at room temperature. The Agilent E5262A source output is monitored in the upper plot. A typical ohmic device response is shown in the lower plot.

developed in the Tarucha lab at the University of Tokyo. Its main functions are the control of the device through the 16-channel DC voltage source, sweeping the magnetic field of the superconducting magnet in the dilution refrigerator, and the extraction of current measurements from the Agilent 34410A digital multimeter. The experiments performed consist of multi-dimensional voltage sweeps applied to the source and gate terminals to obtain the results shown in Chpt. 4. The FMA software can also be used to perform rudimentary data analysis, display, and export functions.

3.4.3 Data analysis software

Most data analysis detailed in Chpt. 4 was performed using MATLAB software. The main analysis program used was called diamondfit.m, which reassembles two-dimensional experiment data and allows users to fit the measured quantum dot conductance data to theory using the single quantum dot model described in Sect. 2.2.

This fitting program is designed so that fit variables can be dynamically adjusted by the user and parameters can be extracted. The fit variables determine the shape of the theoretical lines of conductance plotted on the experimental data. By adjusting the values of these fit variables and by judging the quality of the fit by eye, the user can extract the quantum dot parameters by having the program calculate the relevant parameters when the plotted conductance lines match the lines observed in the experimental conductance plot. The model used assumes that the central vertices of all Coulomb blockade diamonds occur at a bias of $V_\mu = 0$ V. As well, when fitting conductance plots, it is assumed that single quantum dot systems were formed.

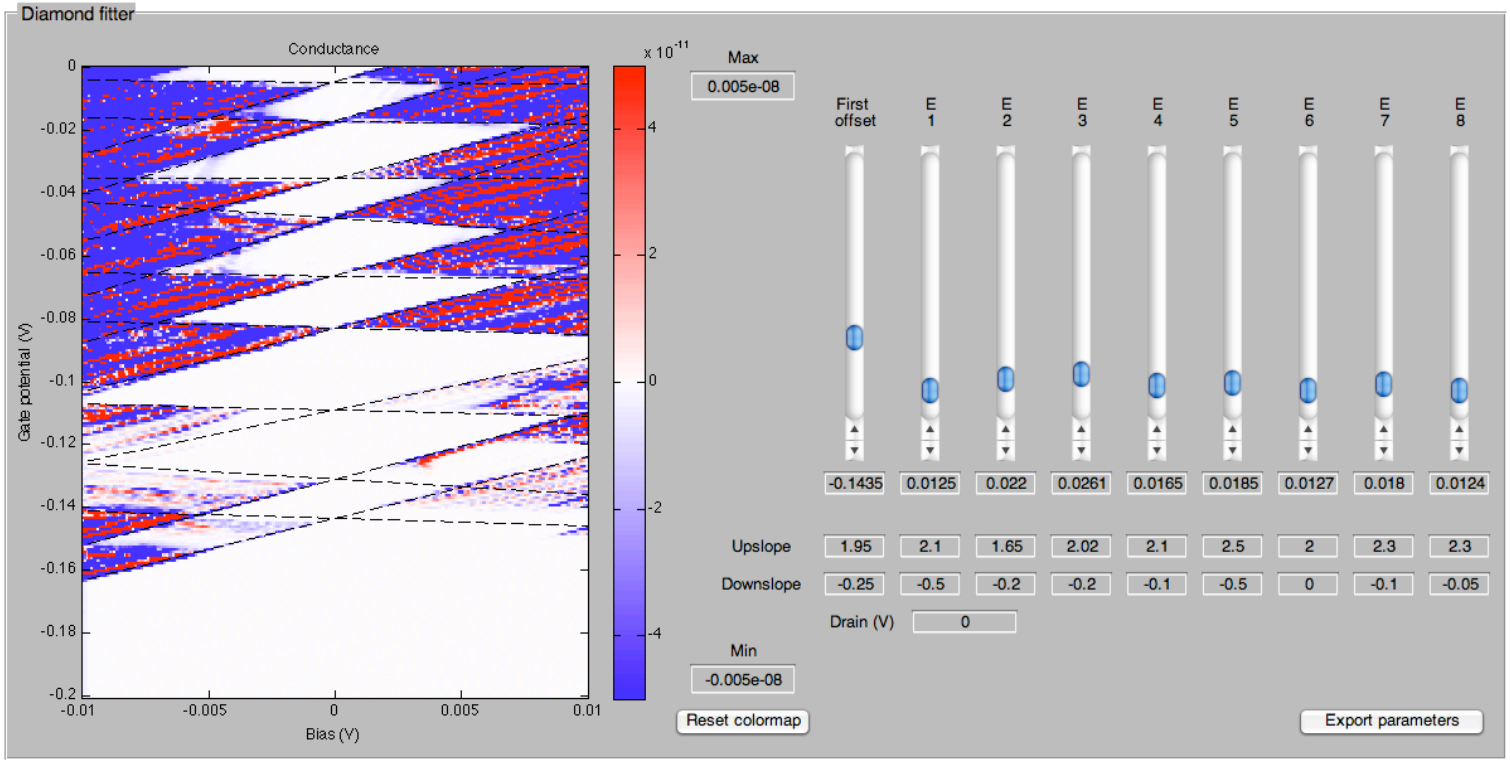


Figure 3.13: The MATLAB data analysis software used to extract the charging and orbital energies, as well as the capacitances for a single quantum dot. Experimental data is displayed in the colour plot to the left with theoretical conductance lines overlaid (dashed lines). In the experimental conductance plot, the colour intensity indicates the differential conductance; red is positive conductance and blue is negative conductance. The sliders to the right are used to fit the conductance model to the image by adjusting the voltage values at which modeled conductance lines meet as well as the slope of the lines overlaid on the plot. The capacitances of the system, charging energies, and orbital energies are derived from these values.

Chapter 4

Results

The following quantum dot results were attained through experiments performed on two samples at cryogenic temperatures. Sample E contained one device: Device 1 which had 8 connected gates. Sample G contained one device: Device 2 which had 6 connected gates. The electron beam lithography patterns are shown in Fig. 4.1. The bottom gates were engineered to be approximately 40 nm wide with a line pitch of 100 nm. The nanowires used had diameters between 30 and 50 nm, with lengths greater than 2 µm.

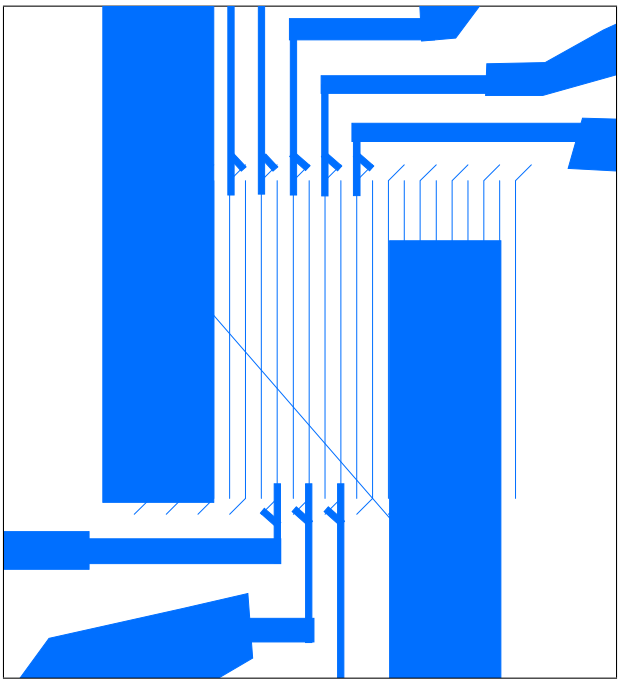
The electron mobility experiments were performed at room temperature using the probe station on an InAs nanowire device with ohmic contacts, a global back gate, and no local gates.

4.1 Electron mobility

Electron mobility is the measure of the ease with which electrons are conducted through a device. Due to its linear relationship with the mean free path length of an electron in a semiconductor, it can be an indicator of ballistic or diffusive transport. In other words, devices with higher electron mobility values have longer mean free path lengths, which, when greater than the confinement length scale, indicates ballistic transport, which is a regime in which quantized conductance can be observed.

The field effect electron mobility, μ_{fe}, can be determined experimentally by observing the current, I, passing through a device while varying the potential applied by a global gate, V_{gg} and maintaining a small fixed bias, V_{μ}, which is the potential difference between the source and drain of a device. Using these measurements, the field effect electron mobility can be found using the expression:

$$\mu_{fe} = g_m \frac{L^2}{C_{gg}} \frac{1}{V_{\mu}} \tag{4.1}$$



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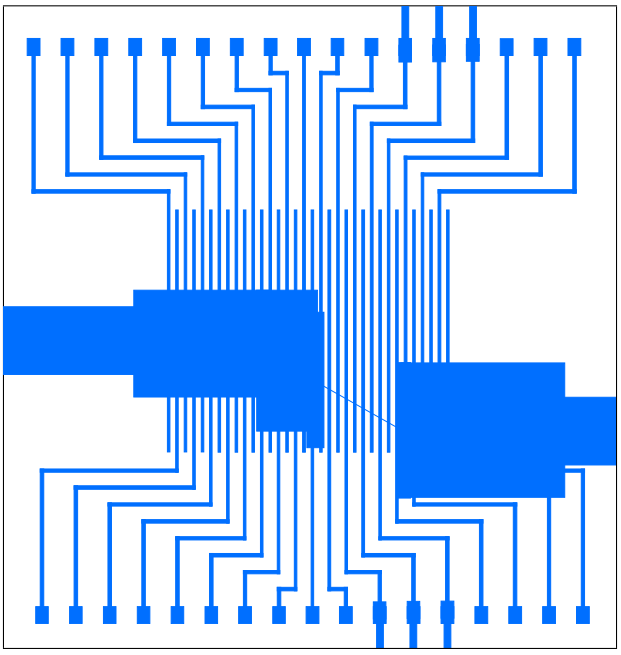


(b)

Figure 4.1: Electron beam lithography patterns of devices used in experimentation. (a) Device 1 was an earlier device design as evidenced by the hockey stick-shaped bottom gate patterns. (b) Device 2 was fabricated using fabrication methods as detailed in Sect. 3.1 and Appendix A. These devices feature a newer device design using area doses, as opposed to line doses, for bottom gates. In all patterns, the nanowire has been drawn as an angled thin blue line stretching between the large ohmic contact structures.

where the transconductance is $g_m = \frac{\mathrm{d}I}{\mathrm{d}V_{gg}}$, the conducting channel length is L, and the capacitive coupling of the nanowire to the global gate is C_{gg}.[21] The capacitance between the nanowire and the global gate is estimated using the expression for a finite cylinder separated from an infinite flat plate by a dielectric:

$$C_{gg} = \frac{2\pi\epsilon_o\epsilon_r L}{\operatorname{arccosh}\left(\frac{r+t}{r}\right)} \tag{4.2}$$

where ϵ_o is the permittivity of free space, ϵ_r is the relative permittivity of the dielectric (SiO_2), L is the length and r is the radius of the nanowire, and t is the thickness of the SiO_2 layer. The device measured had an InAs nanowire that was 110 nm in diameter, measured from a scanning electron micrograph, with a channel length of 1.4 μm on a 120 nm insulating SiO_2 layer. Using Eq. 4.2, the global gate capacitance is estimated to be 167 aF. For comparison, the capacitance between a local gate and a nanowire is usually on the order of 10 aF.[30] While this model is used often in literature to estimate the global gate capacitance in a nanowire system, it has also been shown that the values found using Eq. 4.2 are approximately two-fold larger than capacitances measured using a capacitance bridge method.[21]

The effect of varying the global gate potential on the current passing through a nanowire device was investigated, and the current measurements are shown in Fig. 4.2. By fitting a tangent line to the region with the steepest slope and thereby finding the greatest value for the transconductance, $g_m = \frac{\mathrm{d}I}{\mathrm{d}V_{gg}}$, the peak field effect electron mobility can be calculated using Eq. 4.1. From the line fitted to the data shown in Fig. 4.2, the peak transconductance is $g_m = 1.46$ nA/V; consequently, the peak field effect electron mobility was calculated to be $\mu_{fe} = 86.2\ \mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$.

Compared with results published in [21], our result is two orders of magnitude less than the peak electron mobility of approximately 6000 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ that Ford, *et al.* report for a 35 nm-diameter InAs nanowire. It is suggested that the influence of surface scattering due to interface traps, both at the oxide-semiconductor interface and at the nanowire surface, on electron mobility is enhanced in nanowires, which could cause a severe reduction in electron mobility as observed in the device described above.[21] Planar defects may also cause a reduction in the electron mobility. However, in order to confirm the observed reduction in electron mobility and to deduce a cause more devices need to be examined.

The electron mobility, μ_n, of a semiconductor can allow the carrier lifetime to be estimated as, $\tau = \frac{m^*}{e}\mu$, in which m^* is the effective electron mass and e is the elementary charge. In combination with the diffusion coefficient, $D = \frac{k_B T}{e}\mu$, where k_B is the Boltzmann constant and T is the temperature, the diffusion length of electrons can be expressed

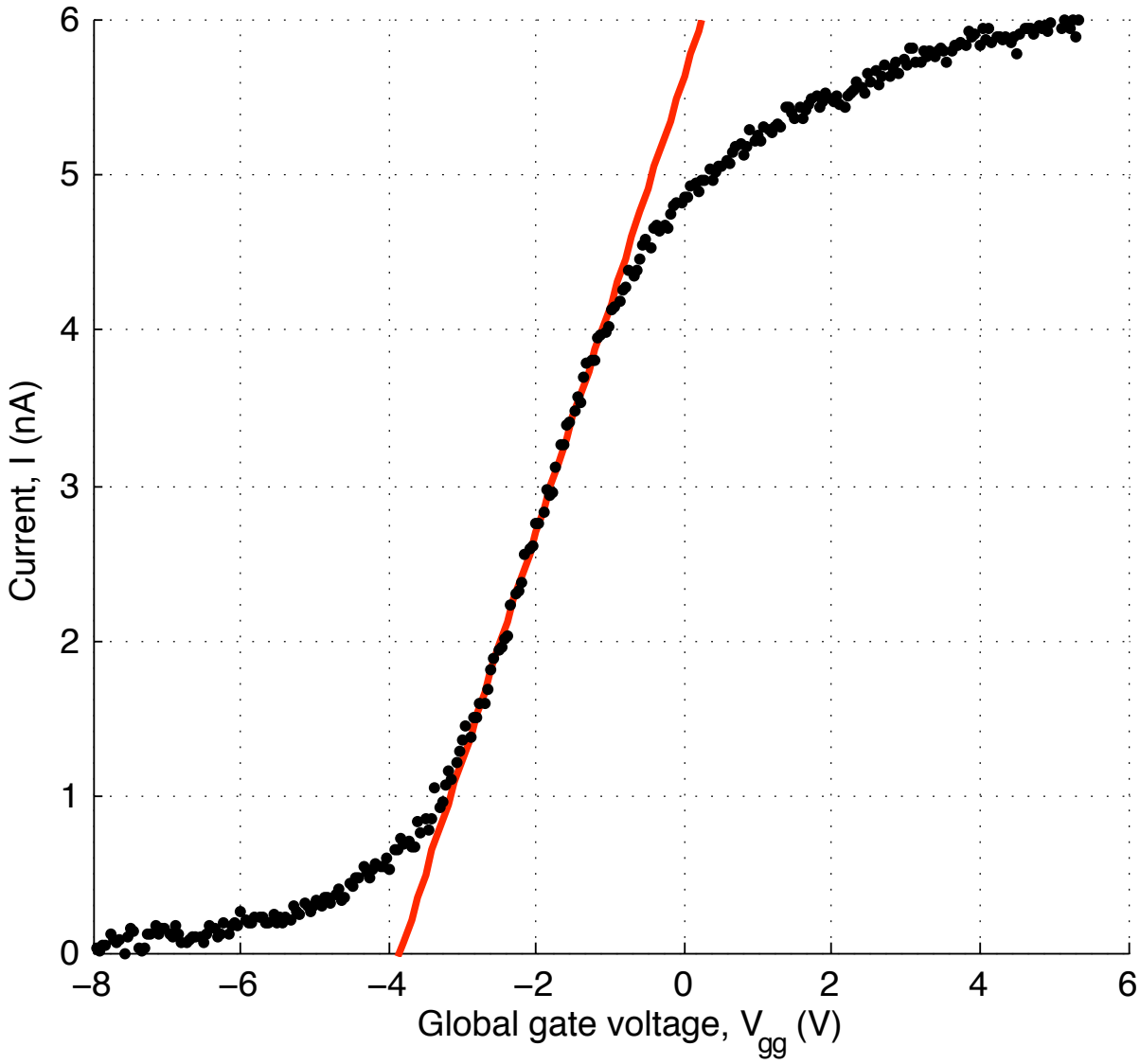


Figure 4.2: Room temperature measurements of current through a InAs nanowire as influenced by a global gate (•) with a tangent fit (red line) to the region corresponding to the peak field effect mobility. The bias is $V_\mu = 2$ mV.

as:[31]

$$\begin{aligned} l &= \sqrt{D_n \tau_n} \\ &= \frac{\sqrt{k_B T m^*}}{e} \mu_{fe} \end{aligned} \tag{4.3}$$

That is to say, as the effective mass of an electron in InAs is $m^* = 0.023 m_e$, Eqn. 4.3 can be used in combination with the previous estimate of the peak electron mobility, $\mu_{fe} = 86.2$ cm^2/V $\cdot$ s, in these InAs nanowire devices, to estimate the equivalent diffusion length as $l = 5.0$ μm, which is larger than the nanowire device thus ensuring that quantum phenomena such as quantized conductance can be observed.[32]

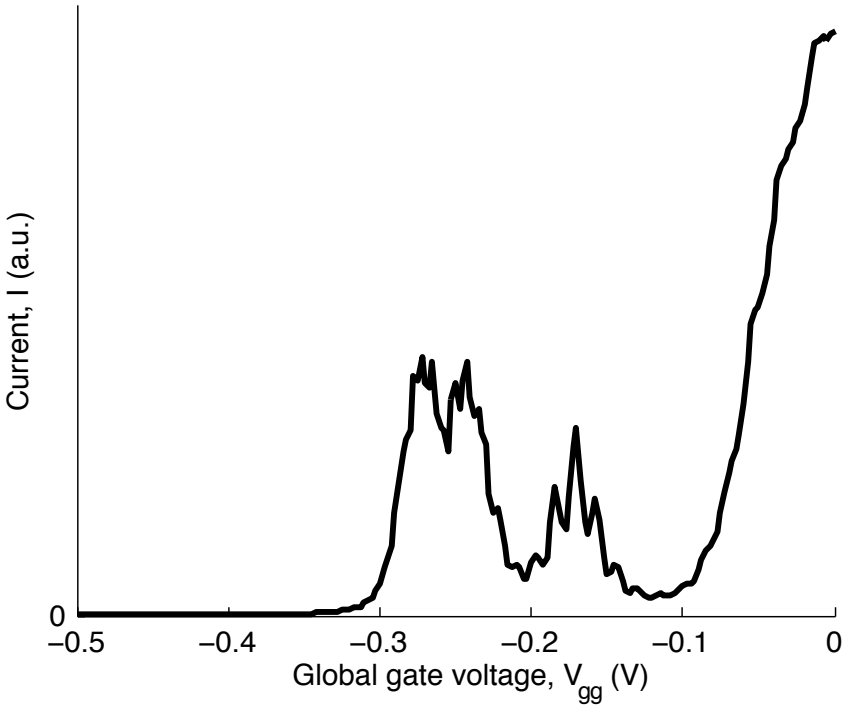
4.2 Single quantum dots

Having demonstrated room temperature global gate control of electron conduction through a nanowire as in Fig. 4.2, the next step towards creating quantum dots is the examination of the effects of this global gate at low temperatures. These experiments are conducted using a small bias usually less than 20 mV.

Pinch-off is the cessation of current through a semiconductor due to a narrowing of the conductive channel caused by applied electric potentials. Fig. 4.3a shows a typical example of pinch-off by global potential adjustment at approximately 25 mK. This information will give an indication of the voltage ranges to be used later when attempting to form quantum dots. As InAs nanowires have n-type conduction behaviour, gate pinch-off in all cases is achieved by applying negative voltages to the gate electrodes.

Local gates also possess the ability to pinch-off a nanowire in a small region, which is essential in forming quantum dots. Fig. 4.3b shows the current behaviour of a nanowire device due only to a local gate. Again, this information will give an indication of the approximate potentials to be applied when forming quantum dots.

While the application of gate potentials at low temperatures can result in an approximately smooth ascent in current with increasingly positive gate potentials as at room temperature, often current oscillations can be observed near pinch-off as in Fig. 4.3a and 4.4. These oscillations hint towards charge confinements effects resulting from the formation of unintentional quantum dots due to local potential variations within the nanowire. These peaks indicate the lifting of the Coulomb blockade as electrons are able to tunnel onto and off of a quantum dot when potentials are aligned, which results in finite conductance. When only one local gate is swept and a quantum dot is not deliberately formed by using other local gates to create tunneling barriers, such oscillations suggest that there may exist local potential variations in the nanowire creating large or weakly confined areas, which behave like many-electron quantum dots.



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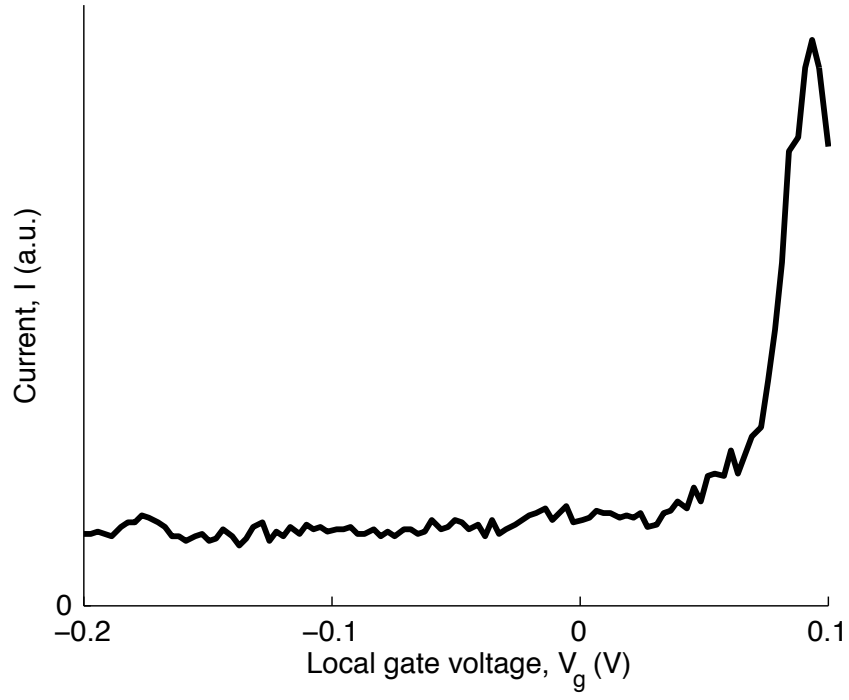
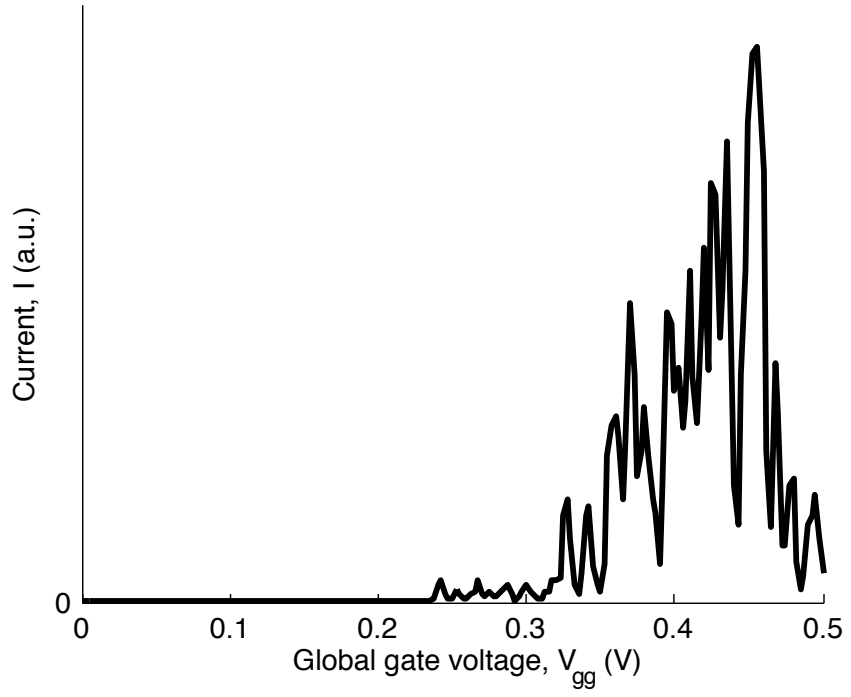


(b)

Figure 4.3: Examples of current measurements showing pinch-off on device 1 through the application of (a) a global gate potential and (b) a local gate potential at 25 mK with a small fixed bias. The current measured is in the range of pA to nA. When the device has been pinched off, the current measured is at or very near zero.



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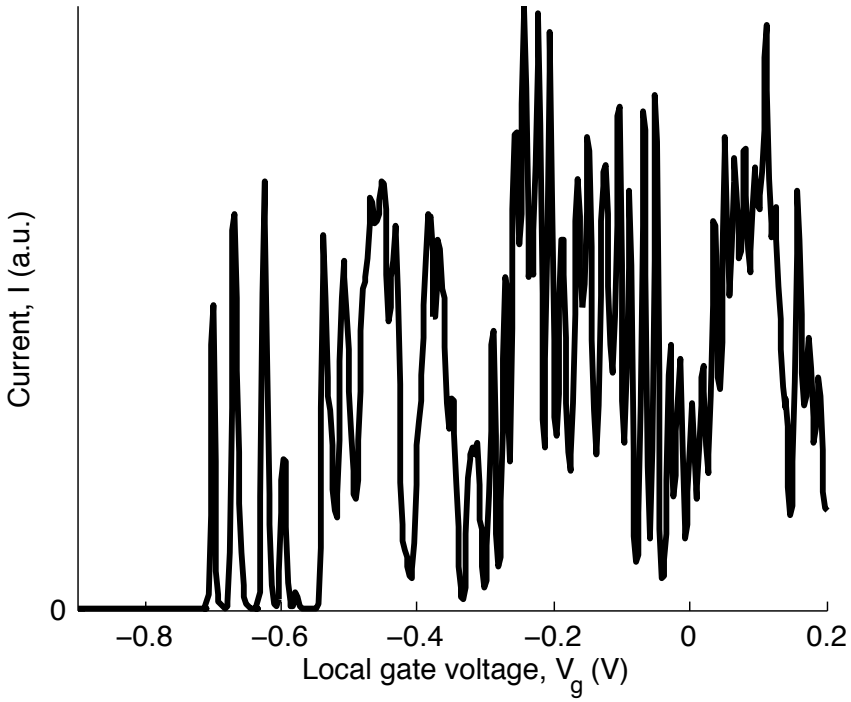


(b)

Figure 4.4: Examples of nanowire current measurements demonstrating Coulomb oscillations in device 1 near pinch-off at 25 mK with 20 mV bias. (a) Coulomb oscillations versus global back gate voltages. (b) Coulomb oscillations versus local gate voltages.

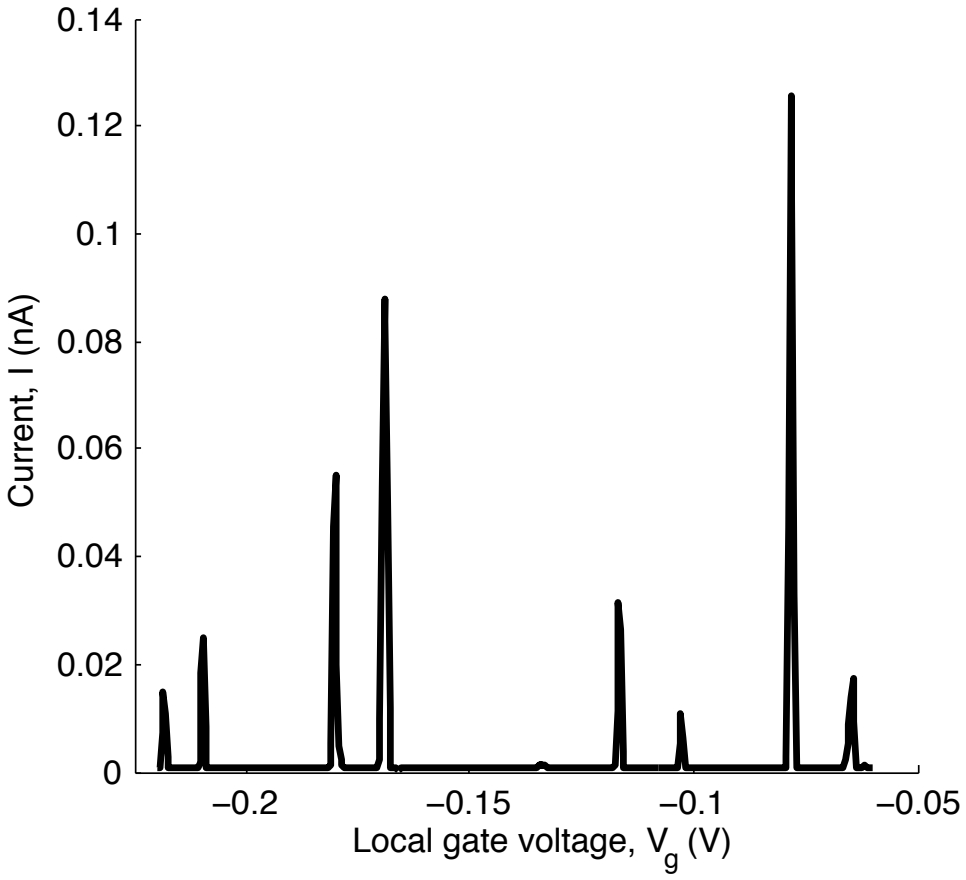


Figure 4.5: An example of current measurements showing single electron charging in device 2 at 25 mK with 30 mV bias. A single quantum dot was made by tuning two local gates to form tunneling barriers. The plunger gate, a third gate between the tunneling barriers, allows the quantum dot electrochemical potential to be tuned and thereby changing the electron number one electron at a time. The uneven spacing between peaks likely indicates that quantum confinement effects are contributing to the addition energy.

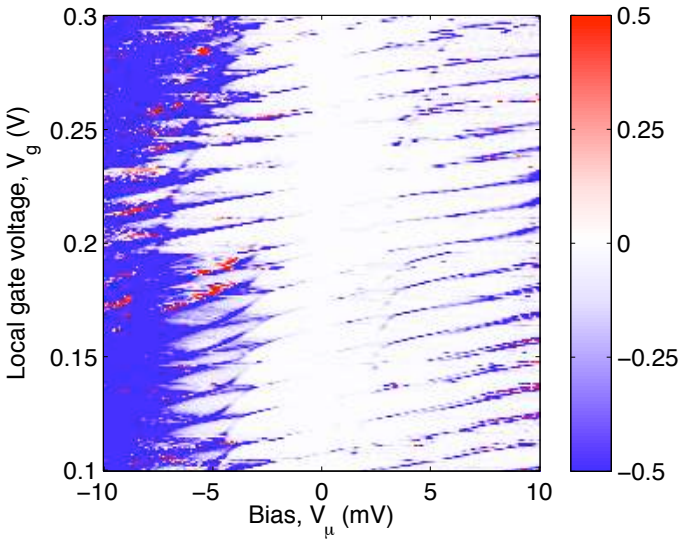
Coulomb peaks can be resolved when a single quantum dot is deliberately formed using local gates, as demonstrated in Fig. 4.5. At a small bias, sweeping through a range of local gate potentials near pinch-off can yield a series of peaks, which occur due to the alignment of source, dot, and drain potentials and thus allowing electron tunneling through the system. In large quantum dots, these peaks are evenly spaced due to smaller contributions of E_{orb}, which scales as the inverse square of the lengthscale, to Eq. 2.3. In small quantum dots, the tight confinement results in an increase in the energy splitting between energy levels, which results in the unevenly spaced peaks shown in Fig. 4.5. A large addition energy indicates that an electron is added to the next orbital state and the energy splitting between orbital states must be overcome in addition to the Coulomb repulsion; a small addition energy indicates that an electron is added to a partially occupied orbital state where only the Coulomb repulsion needs to be overcome.

Single quantum dots are created in InAs nanowire devices by creating tunneling barriers using two local gates set to negative potentials. A third local gate located between the two tunneling barrier gates, known as the plunger gate, is used to adjust the potential of the quantum dot. By measuring the conductance of the system as the plunger gate voltage and bias are swept, a conductance plot can be produced. If a quantum dot is successfully formed, then Coulomb blockade diamond patterns should emerge from the conductance plot, as illustrated in Fig. 2.4 and demonstrated in experimental measurements such as Fig. 4.8.

Similar to the measurement of Coulomb peak spacings in current plots, a conductance plot can show the transport behaviour of a quantum dot through the size and shape of Coulomb diamond patterns. Large quantum dot containing many electrons produce conductance plots with many similarly sized Coulomb diamonds, as in Fig. 4.6a, because orbital energy differences are small. Conversely, in small quantum dots, which have fewer electrons, the orbital energy differences are large and the resulting Coulomb diamond shapes are of different sizes. In addition, the slope of the edges of the diamond shapes can be used to calculate the capacitance of the system.

An example of an early attempt at single quantum dot creation is shown in Fig. 4.6a. It is clear that the quantum dot formed is large due to the regularly-sized diamond-shaped patterns. Smaller quantum dots were created in later attempts as revealed by the differently-sized diamond-shaped patterns similar to those seen in Fig. 4.6b. However, Fig. 4.6b is an example of an unintentional quantum dot, where local gates were not used to create tunneling barriers and any confinement is a product of local potential variations in the nanowire. Unfortunately, this conductance plot exhibits noise, possibly due to poor ohmic contacts to the nanowire, preventing a detailed analysis; as in the electron mobility experiments, oxide-semiconductor interface traps and fixed charges in the oxide layer may be the cause of this noise.

Another example of noise is shown in Fig. 4.7a, where an unstable behaviour known as



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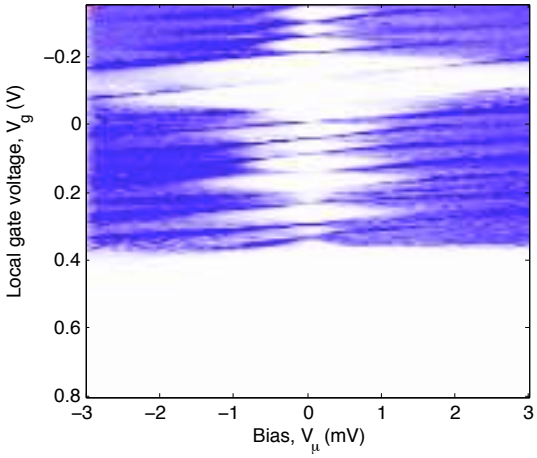


(b)

Figure 4.6: (a) A plot of differential conductance indicating the creation of a large quantum dot with many electrons in device 2 in an early attempt to create a single quantum dot system. The uniformly sized Coulomb diamonds indicate a quantum dot containing many electrons. A color scale is shown to the right with units of nA/mV. (b) A conductance plot of an unintentional quantum dot or multiple unintentional quantum dots (*i.e.* tunneling barriers were *not* created using local gates) in device 2 with fewer electrons than in (a). Many Coulomb diamonds are visible and differences in diamond sizes are clear; however, features are indistinct because $k_B T \approx E_c$ preventing a detailed analysis.

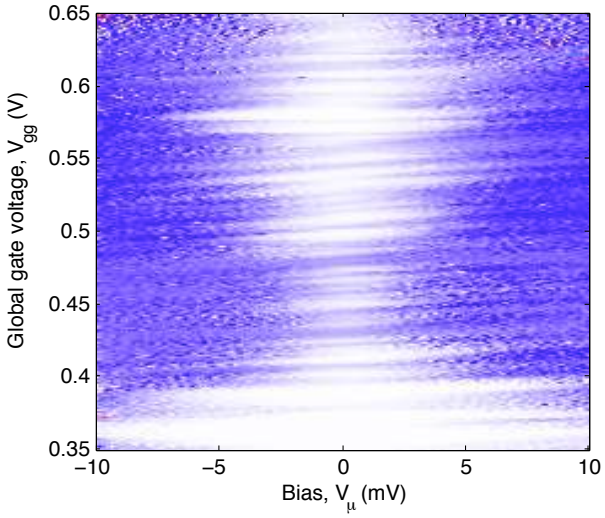
random telegraph noise can be observed. Random telegraph noise is a result of the spontaneous trapping or releasing of charge carriers at semiconductor interfaces or defects. These telegraph noise events are fast local charge fluctuations relative to the long measurement timescale and are manifest as discontinuous changes in the Coulomb diamond pattern. These discontinuous changes can appear as though a potential has suddenly changed causing an abrupt alteration to the shape or size of the quantum dot, or its electrochemical potential.

A quantum dot can also be tuned using the global gate as shown in Fig. 4.7b. However, of greater significance in this figure is the observation of noise suspected to be due to ohmic contacts fabricated in earlier devices. In this example, all local gates are held at fixed potentials and only the global gate is varied. Even so, noise is clearly observable.

The stability of devices is also a problem in experiments as it is clear in comparing earlier and later data, as in Fig. 4.8, device performance does not remain consistent over time. In the measurements presented in Fig. 4.8, device 2 was not removed from the dilution refrigerator between experiments. Only temperature changes had occurred as a result of thermal cycling of the dilution refrigerator. In Fig. 4.8b, it is evident, despite similar conditions resulting in similar quantum dot behaviour, that noise increased over time or due to thermal cycling.

An additional observation from the results shown in Fig. 4.8a is the appearance of fading conductance of the quantum dot as the plunger gate voltage becomes increasingly negative. It is expected that when no electrons remain in the quantum dot, there will be no more tunneling events. As a result, a characteristic of an empty quantum dot is a large area of zero conductance extending downwards and widthwise reflecting the lack of electrons in the system. However, Fig. 4.8a shows that although a large area of zero conductance was measured, there were still very faint areas of non-zero conductance visible on the sides of the lower half of the plot, which indicate that the quantum dot was not empty. These faded areas are a reflection of reduced conductance in the quantum dot system resulting from capacitive coupling of adjacent local gates, causing the tunneling barrier to enlarge and so reducing the electron tunneling rate.

Upon the successful adjustment of local and global potentials, few-electron dots can be achieved as in the measurements shown in Fig. 4.8a. This conductance plot clearly shows a variation in Coulomb diamond sizes indicating a significant contribution by the energy level splitting produced by strong confinement. Reliable and relatively less noisy devices such as these can then be used to characterize both the low temperature measurement system, as in Sect. 4.3, and the properties of the quantum dots, as in Sect. 4.4.



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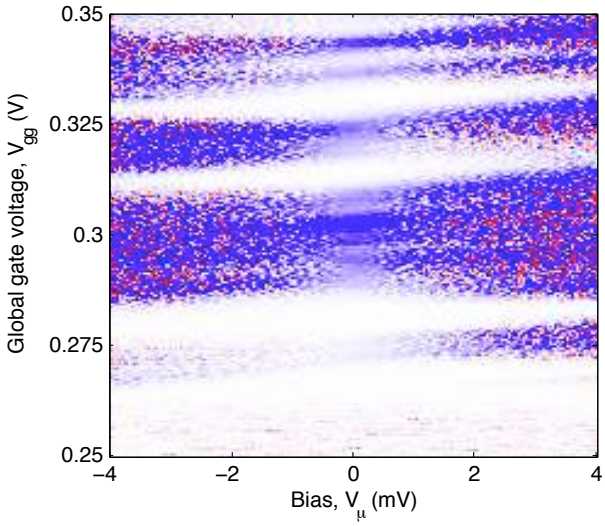
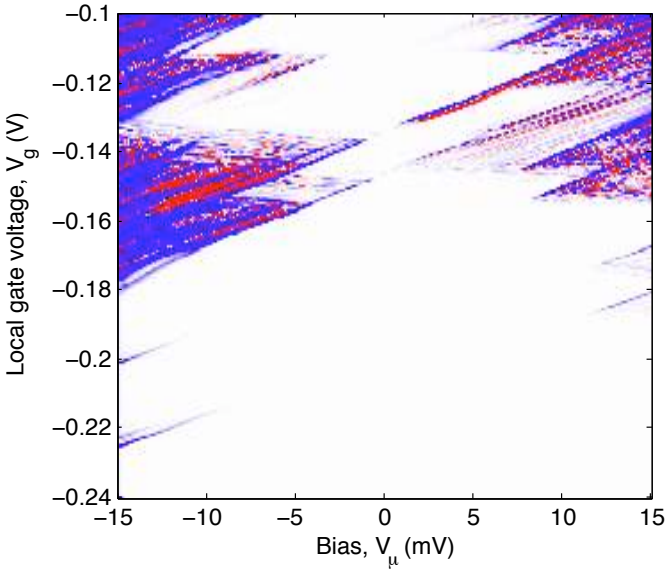


(b)

Figure 4.7: Examples of noise in conductance plots corresponding to measurements of device 1. (a) A conductance plot of an unintentional quantum dot showing the Coulomb diamond size variation typical of few-electron quantum dots. Random telegraph noise-like behaviour can be observed in the form of lines of discontinuity stretching across the plot. (b) A conductance plot showing the tuning of a large quantum dot formed using local gates and tuned using the global back gate. Noise is evident everywhere including areas within the Coulomb blockade diamonds.



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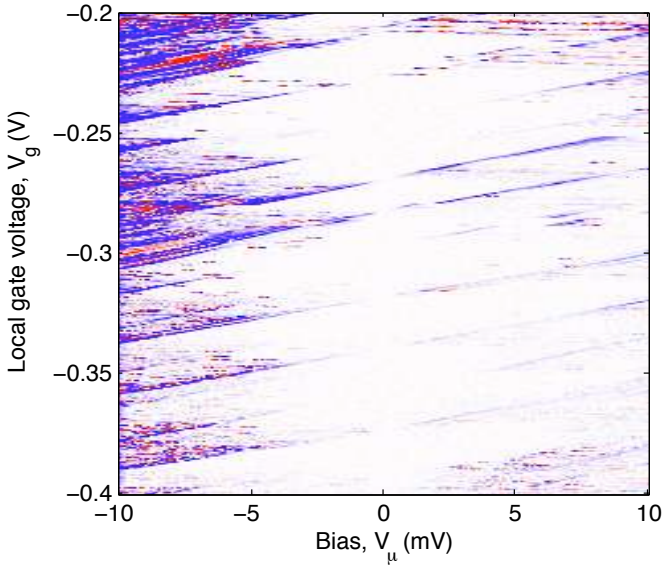


(b)

Figure 4.8: Conductance plots of device 2 (a) upon the initial cooling down of the device, and (b) after cooling again less than two weeks later. Coulomb diamond shapes are clearly visible in both plots, but noise is stronger in the later measurements.

4.3 Electron temperature (T_e)

In order to measure quantum phenomena in these devices, such as electron tunneling into specific orbital states, thermal excitation of electrons must be lower than the energies of the features under investigation. The electron temperature, T_e, is then the temperature corresponding to the minimum thermal excitation, $k_B T$, achievable by electrons in a system.

As thermal excitation can be manifest in the thermal broadening of differential conductance peaks, conductance plots were measured at a variety of temperatures. It is expected that as the temperature of electrons in a device decreases, the width of differential conductance peaks produced will also decrease. However, below the electron temperature, it will not be possible to further reduce the temperature of the electrons due to noise originating from the electrical connection of a device to the warmer stages within the dilution refrigerator, and so the peak width will remain constant.

The shape of a conductance peak at low bias in the quantum Coulomb blockade regime is given as

$$\frac{\mathrm{d}I}{\mathrm{d}V} = G_o \,\mathrm{sech}^2\left(\frac{e\alpha}{2k_B T}(V_g - V_o)\right) \tag{4.4}$$

where $\frac{\mathrm{d}I}{\mathrm{d}V}$ is the differential conductance, V_g is the applied gate potential, and G_o is the conductance peak maximum.[24] The remaining parameters are the charge of an electron, e; the Boltzmann constant, k_B; the dot lever arm, $\alpha = \frac{C_g}{C_\Sigma}$; the temperature, T; and the equivalent electric potential of the electron energy level, V_o.

As the full width half maximum (FWHM) of a $\mathrm{sech}^2(x/b)$ peak is given by FWHM $= 2\,b\,\mathrm{arcsech}(1/\sqrt{2})$, then the FWHM of the differential conductance peak is:

$$\mathrm{FWHM} = \frac{4}{e\alpha}\mathrm{arcsech}\left(\frac{1}{\sqrt{2}}\right) k_B T \tag{4.5}$$

and has a linear dependence on the temperature, T. However, this linear relationship will be disrupted when $T = T_e$.

While the differential conductance in the experiments described here were determined from calculations on direct transport measurements, it is also possible to measure the device conductance directly using a lock-in amplifier and oscillating the plunger gate potential. Using direct transport measurements, the differential conductance is calculated by finding the linear differential of the current measurements averaged over 5 points. Then, measurement noise in the conductance peak is reduced by averaging 5 adjacent peak profiles in the narrowest section of non-zero conductance along the gate potential axis. This procedure is described graphically in Fig. 4.9.

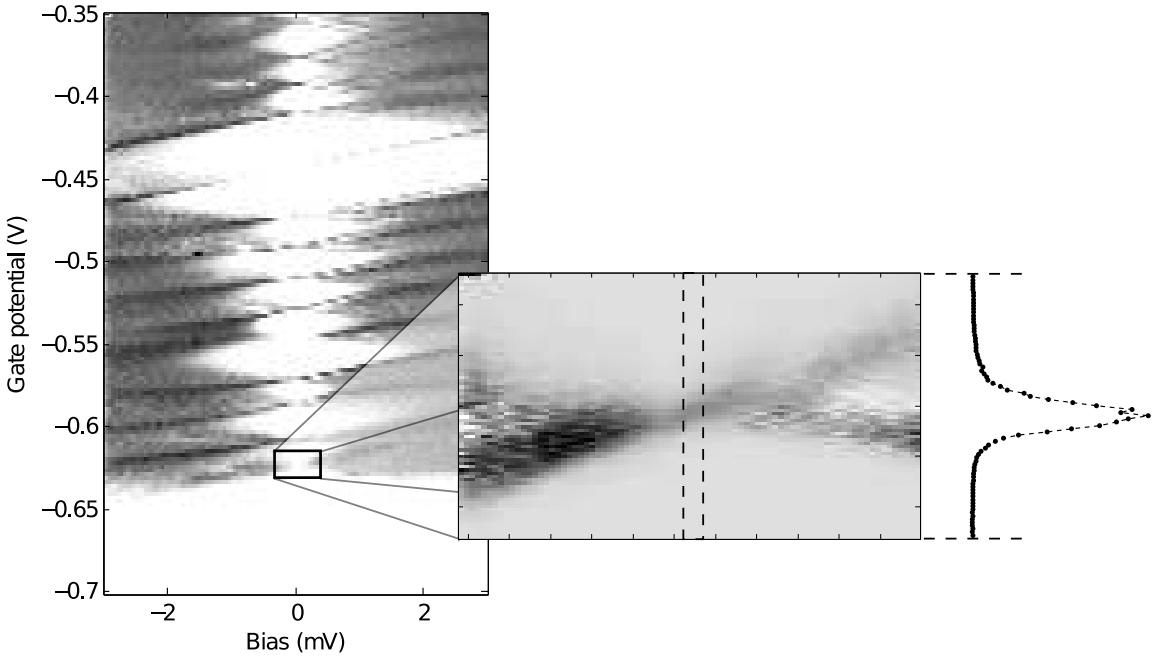


Figure 4.9: The method used for extraction of a conductance peak from differential conductance data of a quantum dot at $T = 25$ mK. The conductance plot shows characteristic Coulomb diamonds of alternating sizes indicating the few-electron regime. At the left is the differential conductance data calculated from current measurements. High resolution measurements of the region outlined by the solid black box were used to characterize a single conductance peak as a function of temperature. This data was measured by varying a local gate without the use of tunneling barriers; a quantum dot was not created using local gates.

The full width at half maximum (FWHM) of each conductance peak was found by fitting the peak profile to Eq. 4.4 using the Levenberg-Marquardt algorithm via the MATLAB Curve Fitting Tool. The data in Fig. 4.10 shows the FWHM measured at each temperature, and suggests a linear dependence above $\sim$ 125 mK, but saturates below, which suggests that $T_e \approx 125$ mK.

The size of the error bars in Fig. 4.10 are estimated from the variation in the FWHM calculated for experiments where measurements were repeated at a fixed temperature. Uncertainty in the fit of the model given by Eq. 4.4 was found to be insignificant when compared to the variation across measurements.

This method for estimating the electron temperature is also corroborated by using Eq. 4.5 to calculate the temperature directly. By using the narrowest measured Coulomb peak widths, the electron temperature can be directly calculated as 170 ± 20 mK.

Additionally, if the electron temperature is assumed to be the temperature of the support rod at the device, the heat load on the mixing chamber can be calculated as

$$\dot{Q} = \frac{\kappa A}{l}(T_{MC} - T) \tag{4.6}$$

where the temperature of the mixing chamber plate is maintained at $T_{MC} = 25$ mK and the temperature of the device is $T = 125$ mK. The cross-sectional area of the support rod is $A = 85 \times 10^{-6}$ m^2, the length of the support rod between the mixing chamber plate and the device is 300 mm, and the thermal conductivity of OFHC copper at temperatures lower than 1 K is $\kappa \approx 50$ W/m $\cdot$ K. Using Eq. 4.6, the heat load of the device on the mixing chamber plate is approximately 150 µW. As this heat load is lower than the cooling power of the dilution refrigerator (200 µW at 100 mK), this estimate of the heat load of the device on the mixing chamber plate seems reasonable. Consequently, it would then appear that the estimate for the electron temperature is plausible.

This estimated electron temperature of 125 mK corresponds to an energy of roughly 10 μeV. In other words, features on the order of 10 μeV or less cannot be faithfully resolved. Larger phenomena, such as the quantization charge and quantum confinement in a nanowire, can be resolved as the charging and orbital energies that result from these phenomena are on the order of meV. However, finer features such as the energy splitting of single electron spin states cannot be resolved as the spin splitting can be as small as tenths of a µeV in weakly coupled double quantum dot systems.[14] As the characterization of spin states will be required in order to attempt coherent spin manipulation, the electron temperature should be reduced further by reducing the thermal noise in the system.

This excess thermal noise could be a result of inadequate thermal anchoring of wiring as well as insufficient shielding of the device from radiative heating from the still shield extension, which surrounds the device area in the dilution refrigerator. A device shield has been created for future devices, as detailed in Sect. 3.3.2. Thermal anchoring greater lengths of wiring may be necessary to ensure a low electron temperature.[33]

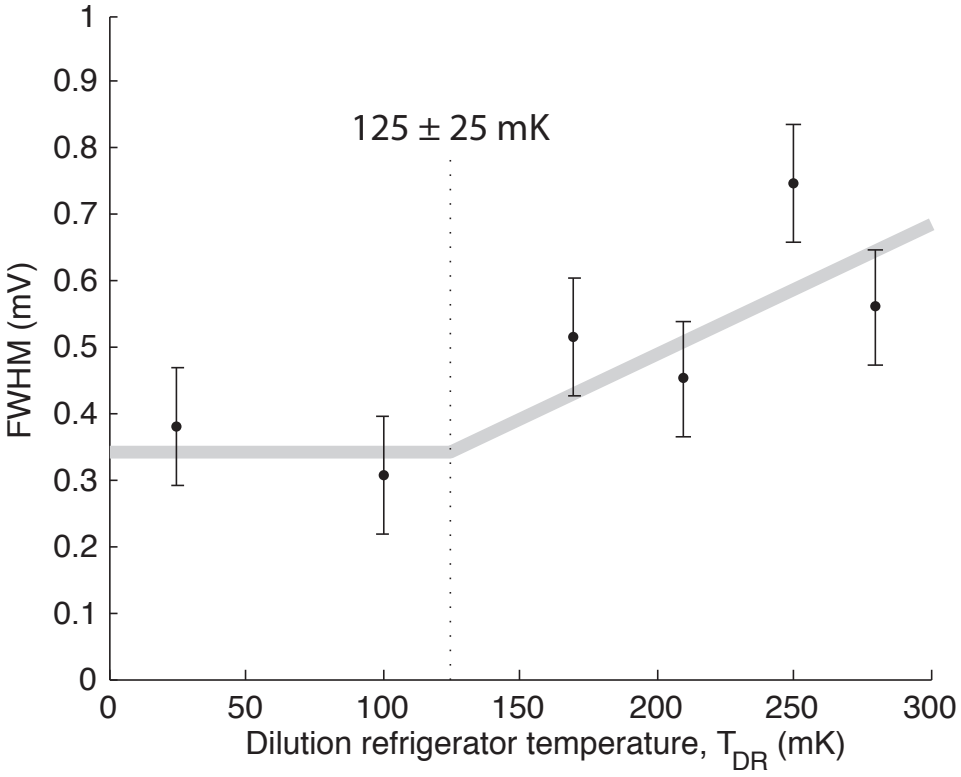


Figure 4.10: The full width at half maximum (FWHM) of the differential conductance peak shown in Fig. 4.4 at various temperatures (•) suggests that the electron temperature is $T_e \approx 105$ mK; the error bars are estimated from the variation in the FWHM found for repeated trials. The grey line is a guide for the eye.

4.4 Quantum dot characteristics

The Coulomb diamond pattern is useful for the characterization of a quantum dot formed by local gating. As shown in Sect. 4.2, it is a two-dimensional intensity plot of the differential conductance, $\frac{\mathrm{d}I}{\mathrm{d}V_\mu}$, of a quantum dot system where the bias $V_\mu = V_D - V_S$ is the difference between the potential on the source and the drain terminal. These characteristic diamonds have dimensions governed by dot parameters such as size, shape, and capacitance.

The addition energy, E_{add}, is the amount of energy required to add another electron to the quantum dot. It is the sum of the charging energy due to Coulomb repulsion, E_c, and the orbital energy due to quantum confinement, E_{orb}.

$$E_{add} = E_c + E_{orb} \tag{4.7}$$

When an electron is tunneling into an incompletely filled energy level then $E_{orb} = 0$, whereas when an electron is tunneling into an empty energy level because the previous level has been completely filled then $E_{orb} = \Delta E$ where ΔE is the energy splitting between the two levels.

Experimentally, the addition energy of each electron can be measured from the conductance plot as the size of each Coulomb diamond along the gate potential axis, where V_g is the potential applied to the gate terminal and α is known as the lever arm. The lever arm is the ratio of the gate capacitance to the sum of all capacitances in the quantum dot system, $\frac{C_g}{C_\Sigma}$. In other words, αV_g is the actual potential at the dot due to the gate.

The charging energy, E_c, of a quantum dot is related to the total capacitance of the system as follows:

$$E_c = \frac{e^2}{C_\Sigma} \tag{4.8}$$

Experimentally, the charging energy can be distinguished from the orbital energy by determining a pattern in the addition energies. The conductance plot used to characterize a single quantum dot system created in an InAs nanowire device is shown in Fig. 4.11. As the orbital energy is only applicable when an electron is added to a new orbital and as the charging energy is a result of the Coulomb repulsion of electrons, there should be a constant minimum addition energy due to the contribution of the charging energy only. These constant addition energies are interrupted by greater addition energies that include the orbital energy as well, as shown in Fig. 4.12. The orbital energy, E_{orb}, of a quantum dot is related to the modes allowed by its geometry. These energies can also be determined by measuring the Coulomb diamonds.

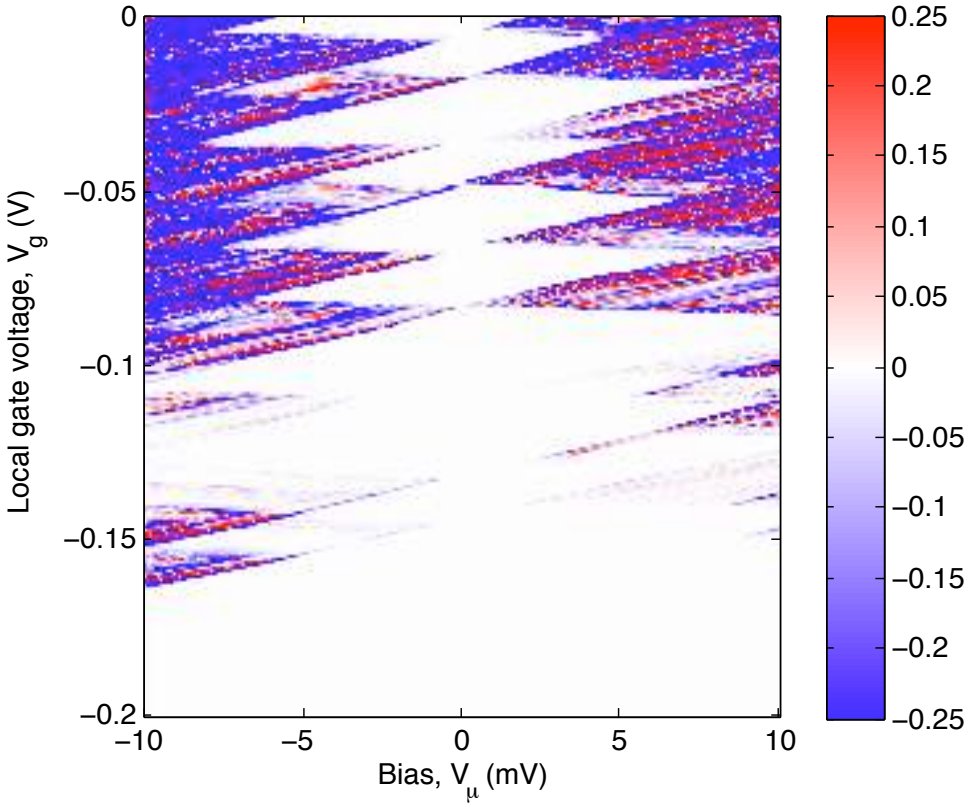


Figure 4.11: A plot of differential conductance data calculated from measurements of a quantum dot system created in device 2 and used for quantum dot characterization. Coulomb diamonds are of visibly varying sizes indicating strong confinement and quantum behaviour. Excitation lines, where electrons are tunneling into excited states of the quantum dot, are visible in areas of non-zero conductance.

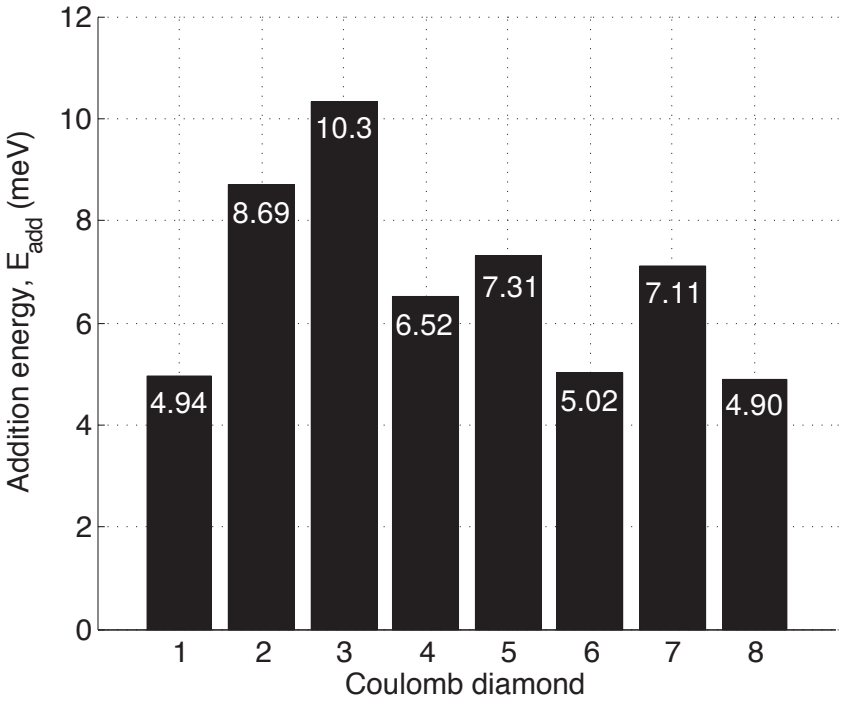


Figure 4.12: A bar plot of the addition energy for each electron as measured from Fig. 4.11. The numeric value of each addition energy is labelled in white on the corresponding bar. The Coulomb diamond at the most negative values of V_g is labelled as the first Coulomb diamond.

4.4.1 Charging energy

The charging energy cannot be directly measured from the conductance plots because the gate voltage, V_g, is related to the quantum dot electrochemical potential, μ, as $\mu = \alpha V_G$ where $\alpha = \frac{C_g}{C_\Sigma}$ is the lever arm.[22] As a result, these values are calculated using the Coulomb diamond fitting software, described in Sect. 3.4, where capacitances are calculated from the slopes of the edges of the Coulomb blockade diamonds.

By examining the experimental conductance plot shown in Fig. 4.11, the charging energy is measured to be approximately 5.0 meV. From this charging energy, a total system capacitance of about 30 aF can be calculated. The lever arm was calculated to be approximately 0.4 eV/V.

As the self-capacitance of a system serves as the upper-limit of its mutual capacitance and by assuming that the capacitances illustrated in Fig. 2.5 constitute the greatest part of the capacitances to which the quantum dot is coupled, then the size and shape of the quantum dot can be estimated if the dot is treated as a solid conducting body. Two simple geometries that can easily be used for comparison are a thin conducting disc and a sphere. The self-capacitance of a thin conducting disc is given by:

$$C_{cir} = 8\epsilon_o\epsilon_r r \tag{4.9}$$

and of a conducting sphere:

$$C_{sph} = 4\pi\epsilon_o\epsilon_r r \tag{4.10}$$

where ϵ_o is the permittivity of free space, $\epsilon_r = 15$ is the relative permittivity of InAs, and r is the radius of the disc or sphere.

The total system capacitance of 30 aF, the diameter of an equivalent thin circular disc is 56.5 nm. As the nanowires used in this device is measured to be approximately 50 nm in diameter, the quantum dot cannot have a greater diameter than the nanowire. On the other hand, an equivalent conducting sphere has a diameter of 35.8 nm, which is too small.

However, a cylindrical model of the quantum dot appears to fit more nicely. The self-capacitance of a right circular cylinder can be estimated as

$$C_{cyl} = 8\epsilon_o\epsilon_r a\left(1 + \frac{2a}{\pi r}\right) \tag{4.11}$$

where r is the radius and a is the length of the cylinder.[34] Using this model and assuming a cylindrical dot diameter of 50 nm, the length of the equivalent cylinder is approximately 10 nm.

4.4.2 Orbital energy

In a nanowire quantum dot system, the dot shape can be approximated as a cylindrical geometry.[35] By solving the time-independent Schrödinger equation for the appropriate geometry the orbital energies can be found. It is easiest to consider that the radial potential as an effectively infinite barrier. The axial potential is approximated as a narrow square well resulting from applied gate potentials.

Due to the cylindrical geometry, the solution to the Schrödinger equation can be separated into its transverse and longitudinal components. As a result, the confinement energy can be expressed as a sum of the confinement energies in the transverse and longitudinal directions. Using the boundary conditions noted above, the transverse confinement energy can be expressed as

$$E_t = \frac{\hbar^2}{2m_e^*}\left(\frac{x_{mn}}{r}\right)^2 \tag{4.12}$$

and the longitudinal confinement energy as:

$$E_l = \frac{\hbar^2}{2m_e^*}\left(\frac{l\pi}{a}\right)^2 \tag{4.13}$$

where $\hbar$ is Planck's constant, m_e^* is the effective mass of an electron in InAs, r is the radius and a is the length of the dot, and x_{mn} is the n^{th} zero of a Bessel function of the first kind, $J_m(x)$.[35] Note that l, m, and n are all quantum numbers and so can only assume non-negative integer values. As n is used to denote the zeroes of the Bessel functions, it is also non-zero.

By applying dot dimensions found in Section 4.4.1 to Eq. 4.12 and 4.13, we find that the longitudinal confinement is much greater than the transverse confinement. Table 4.1 shows the first few confinement energies and the corresponding orbital addition energies.

By again examining the experimental Coulomb diamonds shown in Fig. 4.11, the orbital addition energies can be estimated to be between 1.5 meV and 3.5 meV. The varying orbital addition energies exhibited by the quantum dot suggest that the cylindrical model may be close to the quantum dot shape achieved using local gates in a thin nanowire. However, the magnitude of the orbital energies calculated differ by more than an order of magnitude. In order for the first several orbital energies calculated using Eq. 4.12 to be on the order of 3.5 meV, the cylindrical dot would need to be approximately 130 nm in diameter. This is a large discrepancy between the model and the experimental results, and could be a result of the simplistic model used. Phenomena such as charge screening are not accounted for in the simple treatment used here; a finite element analysis of the device or a detailed three-dimensional quantum dot simulation may provide more insight into the mechanisms involved.

l	E_l (meV)	$E_{orb \cdot l}$ (meV)
0	0	—
1	163.5	163.5
2	654.0	490.5
3	1471	817.5
4	2616	1144
5	4087	1471

(a)

m	n	x_{mn}	E_t (meV)	$E_{orb \cdot t}$ (meV)
0	1	2.40482	15.33	—
1	1	3.83171	38.91	23.59
2	1	5.13562	69.90	30.99
0	2	5.52007	80.76	10.86
3	1	6.38016	107.89	27.13
1	2	7.01559	130.45	22.56

(b)

Table 4.1: The first several confinement energies and orbital addition energies calculated for the (a) transverse and (b) longitudinal dimensions of a cylindrical quantum dot that is 50 nm in diameter and 10 nm in length.

However, it is also clear from the data shown in Fig. 4.11 that the simple model of an idealized single quantum dot system does not suffice as the addition energies are not as neat as this simple model would suggest. For clarity, the addition energies of the system described by Fig. 4.11 are shown in Fig. 4.12.

The pattern of addition energies exhibited in Fig. 4.12 suggests that a more complicated potential profile exists, which might even correspond to more than one quantum dot. It is possible that local potentials due to the nanowire structure has caused the creation of multiple small quantum dots weakly-confined by the local gates instead of a single strongly-confined quantum dot.

Furthermore, simulations of double quantum dot conductance plots exhibit similar qualitative features as seen in Fig. 4.11. These simulations are shown in Fig. 4.13 and created using Eq. 2.5 and 2.6, and the conditions for transport as listed in Table 2.2. Specifically, the Coulomb diamond shapes appear to overlap in a manner atypical of a single quantum dot system (*cf.* Fig. 2.4) and the contribution of the orbital energy does not follow the simple alternating pattern found in single quantum dot systems.

It is plain from a comparison of the charging and orbital energies that the relationship between quantum dot shape and its transport behaviour is not simple as in an ideal conductor as the two approaches do not agree. As well, it is apparent from a comparison of experimental conductance plots with simulated single and double quantum dot conductance plots that the potential within the nanowire is complicated, possibly by point and planar defects, resulting in non-ideal behaviour in the single quantum dots created.

Additional investigations on the characterization of quantum dots need to be conducted

in order to confirm these observations, and shed light on the quantum dot shape as well as the source of the addition energy pattern seen here. Control of the quantum dot potential will be very important in spin manipulation investigations as basic tasks such as loading and measuring a spin qubit will require fine tuned control over the potential of the dot as well as the energy of a spin qubit relative to other spin qubits. The creation of unintentional dots may result in a change in the quantum dot behaviour and inhibit controllability.

4.5 Towards double quantum dots

In order for nanowire quantum dots to be useful for quantum computing, multiple quantum dots need to be created, characterised, and both one- and two-qubit operations must be demonstrated. For both of these purposes, the formation of double quantum dots is a functional beginning. The defining characteristic of a double quantum dot system is the stability diagram, schematically illustrated in Fig. 4.14. Similar to a single-dot conductance plot, the stability diagram is a two-dimensional intensity plot of the differential conductance of a quantum dot device where the two axes are two independently varied local gate potentials.

As with the formation of single quantum dots, creating the proper potential profile to form a serviceable double quantum dot system requires a systematic approach. The following method requires a device with at least 5 functional local gates as the target is to create a double quantum dot system with one plunger gate available for tuning each dot.

1. Set the middle local gate to a negative potential in order to create a weak tunnel barrier. Set all other local gates to a potential that will not result in the creation of another tunnel barrier. (*i.e.* 0 V)

2. Sweep the end gates over negative potential ranges and measure a stability diagram. These end gates are the local gates that will form the outer tunnel barriers defining the double quantum dot system.

3. Locate an area in the previously generated stability diagram in which both end gates are near to pinch-off. Set the end gates to these potentials.

4. Sweep the middle gate to confirm that Coulomb peaks result and that pinch-off can be achieved as though the system was a large quantum dot.

5. Set the middle gate to a negative voltage selected from the results in the previous step. In essence, the goal is to create a large quantum dot and then separate it into two by raising a tunnel barrier in the middle.

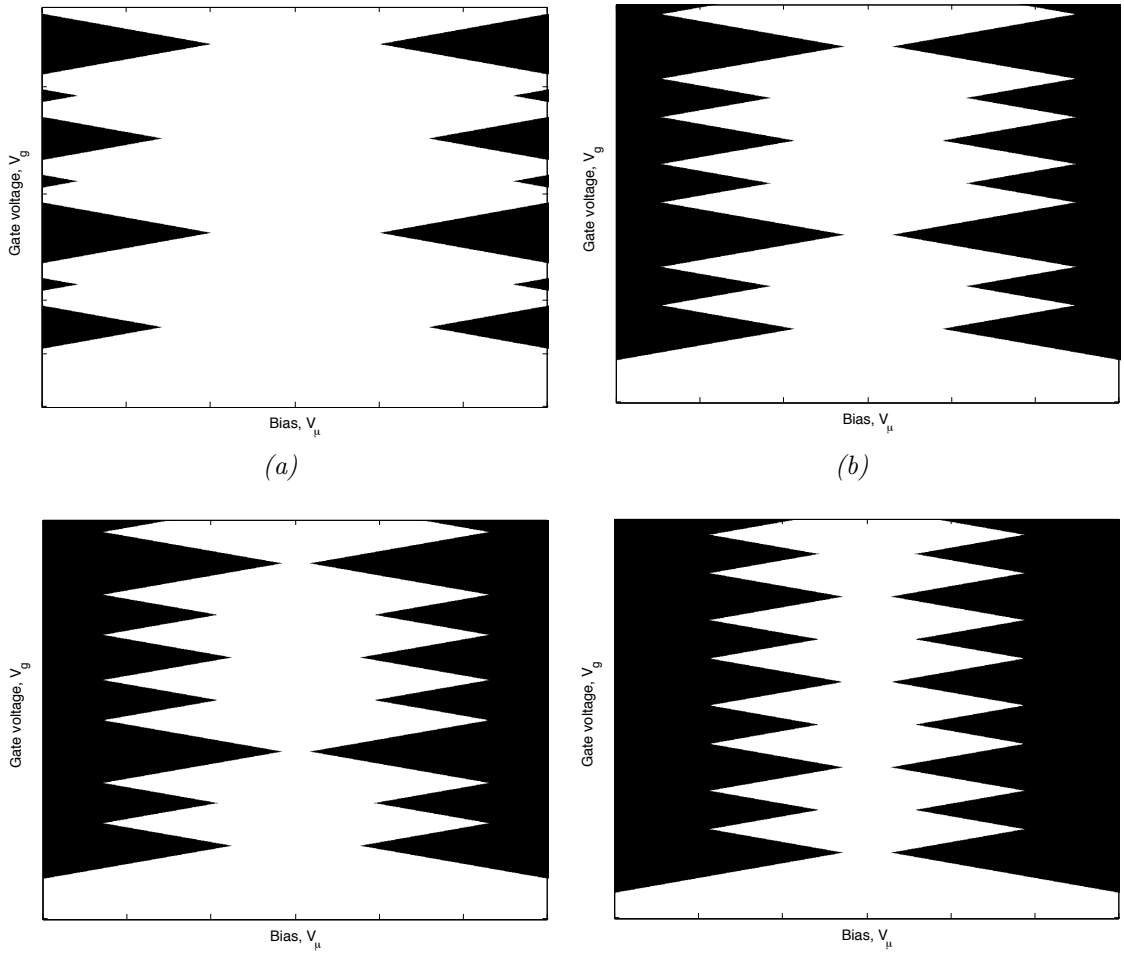


Figure 4.13: Simulations of Coulomb diamond plots for a double quantum dot system. In all plots, $C_S = C_D = 1$ aF and $C_{g1} = C_{g2} = 10$ aF. It is assumed that both quantum dots are the same size, resulting in identical orbital energies.
(a) $\frac{C_c}{C_1} = 0.5$, $E_{orb} = 3$ meV; (b) $\frac{C_c}{C_1} = 0.8$, $E_{orb} = 3$ meV; (c) $\frac{C_c}{C_1} = 0.9$, $E_{orb} = 3$ meV; (d) $\frac{C_c}{C_1} = 0.8$, $E_{orb} = 0$ meV. Black regions represent areas of non-zero conductance.

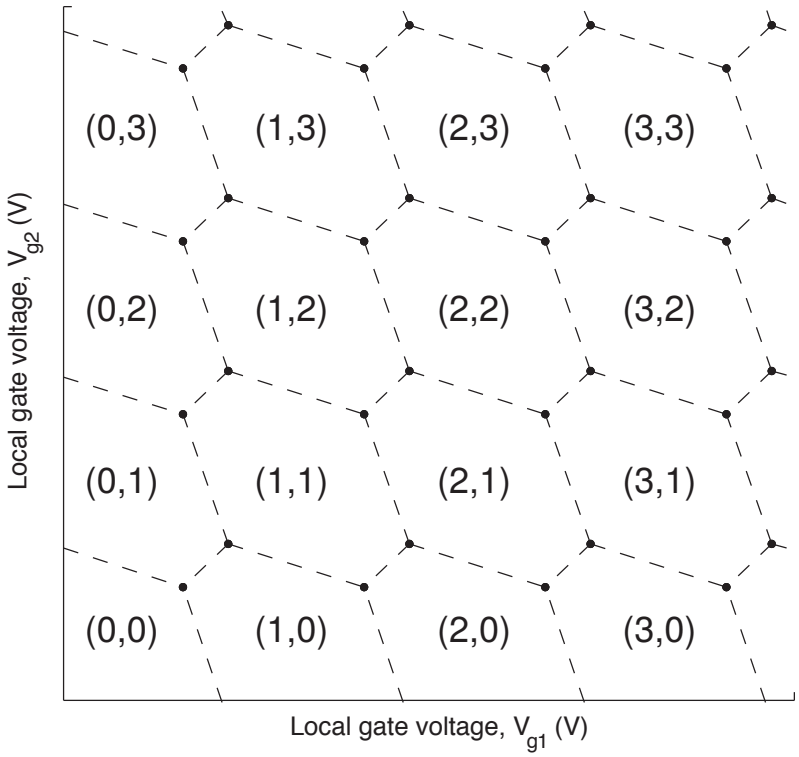


Figure 4.14: A schematic illustration of a stability diagram generated using Eq. 2.4. The dashed lines show the boundaries of the characteristic honeycomb pattern of non-conducting areas; for example, the stable configurations in each area have been labelled. The dots locate the triple points around which electron transport can occur.

6. Carefully sweep the two remaining local gates that have been identified as tuning gates to create a stability diagram that will allow for the characterization of the double quantum dot system.

However, even with this systematic method many early attempts at creating double quantum dot systems were met with only moderate levels of success. Fig. 4.15 is an example of early evidence for a double quantum dot system with suboptimal settings. When the barrier in the middle of the system is not high enough, one single large dot is formed and diagonal ripples can be observed in the resulting stability diagram.

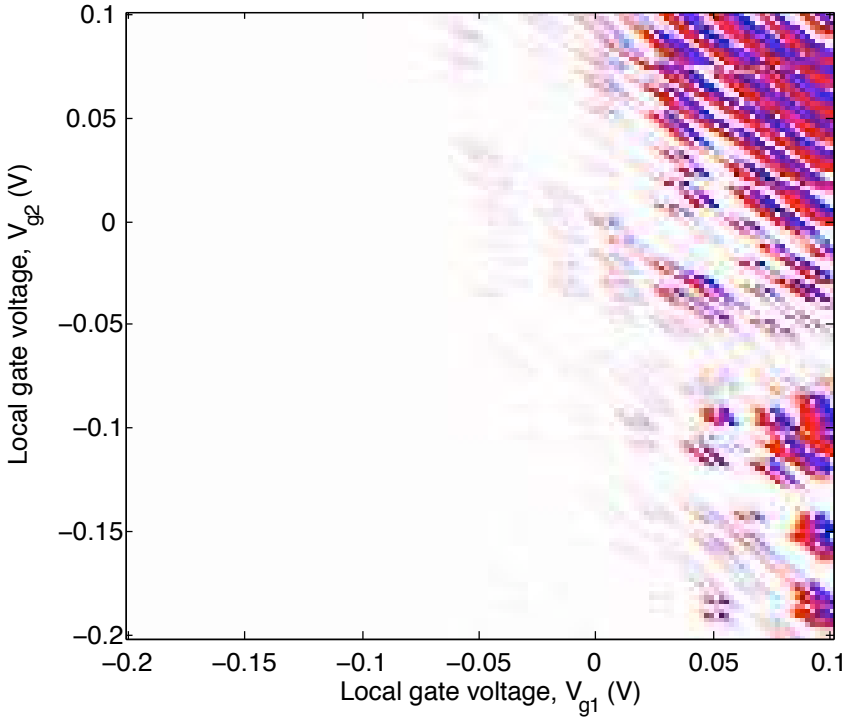


Figure 4.15: An early example of a stability diagram measured to test for the creation of a double quantum dot system. The diagonal ripples are a signature of a single quantum dot.

As in the single quantum dot systems, contact and telegraph noise is also a concern. A more successful example of a stability diagram is shown in Fig. 4.16, but these measurements were marred by telegraph noise. This noise meant that the double quantum dot systems created were not stable enough for detailed testing. On the other hand, results such as those shown in Fig. 4.17a are encouraging even despite the noise as it clearly shows a triple point with good resolution, as highlighted in Fig. 4.17b, as well as expected features such as the anti-crossing located there.

The anti-crossing featured in Fig. 4.17b corresponds to the triple points of a double dot stability diagram, where the separation between the two points corresponds to the inter-dot coupling energy, $E_{cc} = e^2 \frac{C_c^2}{C_1 C_2 - C_c^2}$, where $C_1 = C_S + C_c + C_{g1}$ and $C_2 = C_D + C_c + C_{g2}$. The separation of the two areas, as measured against the axes, corresponds to a coupling energy of $E_{cc} \approx 4.5$ meV, indicative of a moderately-coupled double quantum dot system.

Some examples of double quantum dot systems were created, and one instance of coupling energy was measured. However, in order to properly characterize these double quantum dot systems, a reduction in noise will be necessary in order to resolve the finer details observable in a double-dot conductance plot, such as lines of increased conductance indicating resonant tunneling where the potential of both dots are aligned with each other. The resolution and identification of such features will be necessary when manipulating spin qubits so that spin loading and spin-to-charge conversion can be conducted in a controlled and repeatable manner. In this situation, both ohmic contact noise and telegraph noise will be extremely problematic as they may lead to unintentional lifting of Pauli spin blockade.

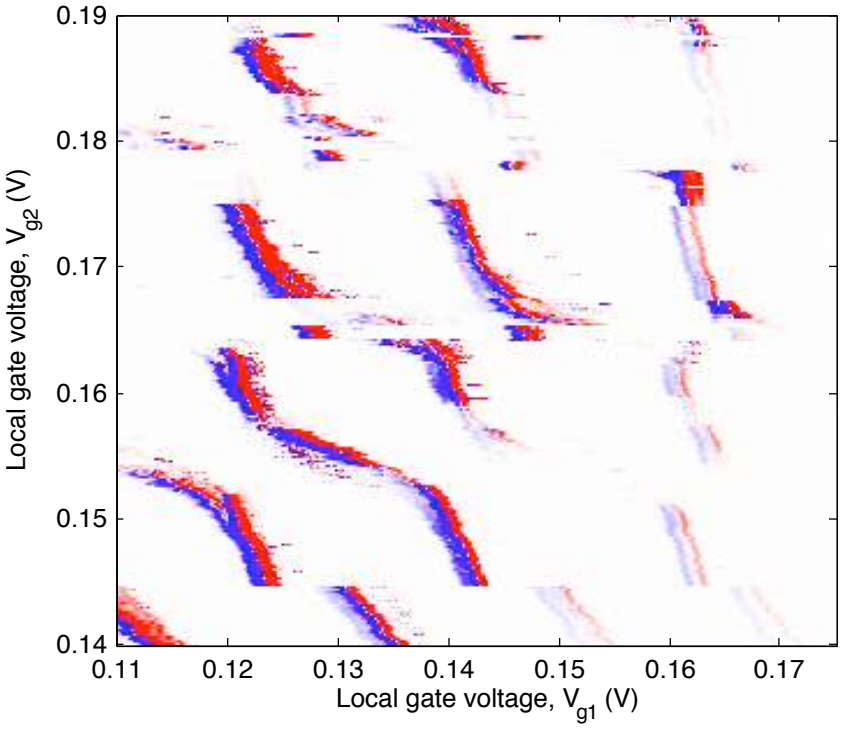
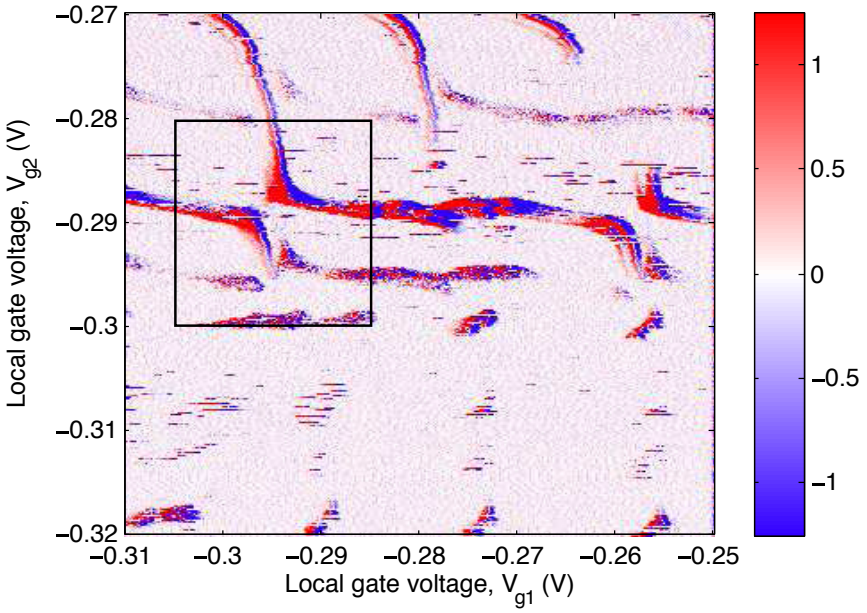
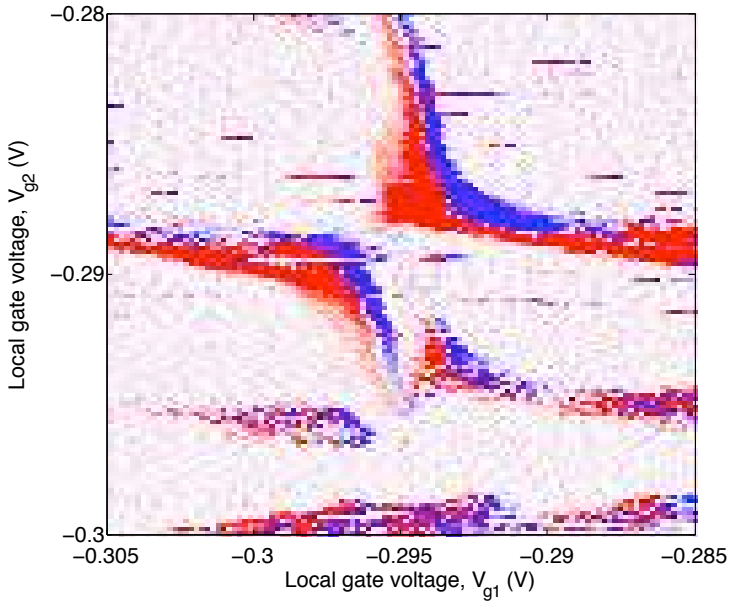


Figure 4.16: An example of a successful but noisy stability diagram measured from an unstable double quantum dot system created in device 2. Random telegraph noise-like behaviour is clearly visible where areas of conductance change discontinuously creating lines of interruption parallel to the horizontal axis.



(a)



(b)

Figure 4.17: (a) A stability diagram of differential conductance data from measurements on device 2. The area framed by the black rectangle is shown in (b) to highlight the anti-crossing.

Chapter 5

Conclusions and the future

Over the course of this work, a procedure for fabricating InAs nanowire quantum dot devices has been developed, but there is room for significant improvement. A peak field effect electron mobility of 200 $cm^2/V \cdot s$ is measured, far less than reported in literature, which can exceed 10 000 $cm^2/V \cdot s$. This electron mobility suggests an electron mean free path length, as calculated using the diffusion model, of 5 μm; this is larger than the size of the device and so suggests that the device functions in the ballistic transport regime. A reduction in the density of stacking faults have been reported to increase the electron mobility by two-fold; however, as the electron mobility in the devices produced are at least an order of magnitude less than that quoted in literature, it must be concluded that poor ohmic contacts and other defects are at issue as well.[25] However, repeated examination of additional devices must be conducted before the reduction of electron mobility can be traced to a cause.

In addition, ohmic contact noise and random telegraph noise is clear and observed to increase over time, or due to thermal cycling, throughout experiments to form and characterize single and double quantum dot systems. This evidence also suggests that poor ohmic contacts and other defects are to blame. As the formation of the native oxide is uncontrolled, it may be surmised that there exist a large number of defect sites along the oxide-semiconductor interface of the nanowire. Defects located at the surface of the semiconductor nanowire are likely to cause problems in InAs devices due to the strong role that surface states play in InAs nanowire behaviour.[27] Such defects may be avoidable by using nanowires that have a deliberately grown shell, such as indium phosphide, in order to avoid the uncontrolled growth of a native oxide. It is as yet unclear whether these defects are a result of the ohmic contact fabrication process or of defects already present in the nanowire. Additional experiments should be performed to investigate the source of the noise, demonstrate the effect of these defects as well as the reduction of the density thereof. As well, device degradation experiments have not been performed and would be

useful in determining the cause of the noise as well as helping to establish best practices for experimentation and handling.

Evidence has been presented supporting the capability of these devices to form single quantum dot systems. In the example investigated, a charging energy of approximately 5.0 meV was observed and the orbital energies were measured to be 1.5–3.5 meV. The total capacitance of the dot created was about 30 aF, which was found to be similar to the self-capacitance of a conducting cylinder 50 nm in diameter and 10 nm thick. While estimates for the orbital energy resulting from the confinement of electrons in a cylinder of these dimensions did not agree, the qualitative pattern in variation of addition energies suggest a potential relationship. It is likely that the model used was too simple and a better approach taking into account complexities, such as charge screening, could be used. A more detailed simulation of the device would be useful and may yield more faithful results.

In examining the single quantum dot systems created, it was also observed that some qualitative features in the experimental differential conductance data did not match that of theory. Comparing with simulations of Coulomb diamond plots generated from double quantum dot systems, it appears that additional quantum dots were inadvertently created. As planar interfaces can create potential barriers, it is believed that the accidental creation of a second quantum dot may be a result of stacking faults creating a low potential barrier within the deliberately created single quantum dot. As previously stated, this may be avoided in future by utilising nanowires with fewer planar defects. Again, additional experimentation is necessary to determine the cause of the complex potential profile as other features, such as point defects, may also contribute.

Double quantum dot systems were also deliberately created. Qualitative characteristics of these systems have been observed, but more experimentation is necessary to quantitatively characterize these systems. As in the single quantum dot investigations, noise is inhibiting detailed study of these systems. A coupling energy of about 4.5 meV was measured, but smaller features could not be resolved.

Lastly, through the examination of single quantum dot systems, the electron temperature in the dilution refrigerator was estimated to be no less than 105 mK. This estimate corresponds to approximately 9 µeV of thermal noise, which means that characteristics of quantum dot transport behaviour suc as charging energies and the orbital energies can be resolved. However, it would be beneficial to further reduce the electron temperature and confirm this conclusion using additional experiments for the purposes of future experiments in spin qubit manipulation in order to prevent inadvertent excitation of spins and thus accidentally lifting Pauli spin blockades. The electron temperature can be improved by increasing thermal anchoring of electrical components within the refrigerator. For example, more electrical wiring and semi-rigid coaxial cable can be wound around cooling posts to increase the amount of area that is directly anchored to the cooling stages. Additional

shielding already incorporated into the device mounting apparatus should also contribute to a reduction in noise in future experiments.

In summary, while it has been shown that the InAs nanowire devices created are functional and can demonstrate basic quantum dot behaviour, there is much room for improvement particularly if these devices will be used to examine coherent spin manipulation.

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Appendix A

Fabrication details

The initial development of these methods was performed in a combination of the Waterloo Advanced Technology Lab,[1] the Centre for Integrated RF Engineering,[1] and the Western Nanofabrication Facility.[2] As electron beam lithography facilities in the University of Waterloo became available, fabrication was moved away from the Western Nanofabrication Facility and into the Institute for Quantum Computing Fabrication Facility[1] when a more advanced electron beam lithography facilities were made available.

A.1 Handling

Important things to remember when fabricating devices:

- Do not expose sample chips to any environment outside of a clean room prior to the completion of processing and use a portable vacuum box for transport.
- Do not hold wafers or sample chips up to one's face, breathe on wafers or sample chips, or bend over wafers or sample chips to examine more closely.
- Always perform any steps involving organic solvents, acids, bases, or other volatile chemicals in a properly ventilated area such as a fume hood.
- Always keep sample chips covered or enclosed to avoid contamination.
- Always clean instruments and containers prior to and after processing by rinsing thoroughly with acetone, then isopropanol, then deionized water. If residue or contamination is visible, then use an appropriate cleaning solution and rinse. Rinse again

[1] University of Waterloo, Waterloo, Canada
[2] University of Western Ontario, London, Canada

with acetone, isopropanol, and deionized water afterwards. Finally, dry instruments and containers using nitrogen gas.

- Always handle wafers and samples using appropriately shaped polytetrafluoroethylene (PTFE) or PTFE-coated metal tweezers.
- Always be gentle when blowing nitrogen gas, spraying liquids, squirting solutions, or applying resist to wafers or sample chips. The device structures are small and delicate so care must be taken to ensure that they remain undamaged.
- Always label all wafers, sample chips, chemicals, and other materials to ensure confusion does not result in mistakes in fabrication.
- Always use tweezers to hold wafers and sample chips flat, firmly, and by an edge or corner far from any structures so that wafers and sample chips are not dropped and any structures are not damaged, dislodged, or scratched by handling.
- Always test fabrication process steps prior to use on a sample chip being used for device fabrication to avoid contaminating, damaging, or destroying potential devices.

A.2 Wafer characteristics

Wafer property	Characteristic
Material	Si
Size	100 mm
Doping	p-type
Dopant	Boron
Orientation	[100]
Resistivity	0.001–0.005 Ω·cm
Thickness	500 µm
Type	Single side polished, prime grade (SSP prime)

Table A.1: Characteristics of wafers used for device fabrication.

A.3 RCA organics clean recipe

The following recipe describes a RCA organics clean using a 1:1:5 solution of NH_4OH:H_2O_2:H_2O. This cleaning process removes large particles and organic contaminants from the surface of

a wafer or sample chip, but does not remove metal ion contamination. This process should only be performed in a fume hood.

1. Clean all instruments and glassware with a progressive and thorough wash using acetone, isopropanol, and then deionized water prior to use.
2. Add 1 part H_2O_2 to 5 parts deionized water.
3. Heat the H_2O_2 solution to 60°C, and monitor temperature. To ensure an accurate measurement, make sure that there is no contact between the thermometer and the container. If possible, use a magnetic stir bar to promote good mixing of the solution and a uniform temperature.
4. When the H_2O_2 solution has reached 60°C, add NH_4OH into the H_2O_2 solution.
5. When the RCA cleaning solution has reached 60°C, soak the sample chip in the RCA cleaning solution for 15 minutes at 60°C. If used, turn off stirring if the sample chip is not protected by a chip holder apparatus. If bubbles are collecting on the surface of the sample chip, agitate the sample chip to ensure that the entire surface is cleaned.
6. After 15 minutes, remove the RCA cleaning solution from the heat source and place it under a gentle stream of deionized water. Allow the deionized water to cascade until the RCA cleaning solution has been completely displaced.
7. Carefully, remove the sample chip from the deionized water, and rinse thoroughly with fresh deionized water.
8. Carefully, blow dry the sample chip using nitrogen (N_2) gas.
9. Perform a dehydration bake for 15 minutes at 180°C. Cover the sample chip to prevent particle contamination if the dehydration bake is performed on an open hot plate.

A.4 Oxygen plasma etching recipe

The following recipe describes an oxygen plasma etching recipe using a reactive ion etcher (RIE) with both conventional parallel plate plasma and inductively coupled plasma (ICP) generation capabilities.

An oxygen plasma etch is used to remove organic materials and resist from wafers and sample chips. If the descum step is being performed, then observe the sample chip colour before and after the descum etch; a large colour change may indicate that too much resist has been etched away. Oxygen plasma etching was performed using a Trion Phantom Reactive Ion Etch system[3]

[3]Trion Technologies, Inc, Clearwater, USA

1. Leaving the RIE chamber closed, pump down the chamber in order to purge any possible toxic or harmful gases remaining from previous uses. Allow the chamber to be pumped down for at least 3 minutes or as long as necessary to achieve a high vacuum.

2. Vent the chamber, then open it.

3. Inspect the chamber for damage or wear, and remove any samples or unnecessary equipment. Finally, wipe away any ash or contaminants using a lint-free wipe.

4. Close the chamber, then pump down.

5. While the chamber is pumping down, input the process settings in Table A.2.

	Cleaning etch	Descum etch
Pressure	100 mTorr	10 mTorr
ICP RF power	100 W	30 W
RIE RF power	30 W	0 W
O_2 flow rate	15 sccm	5 sccm
Time	60 s	20 s

Table A.2: Oxygen plasma etching process settings.

6. When a high vacuum has been achieved, begin the etching process and tune any power or capacitance matching settings as necessary.

7. Extinguish the plasma, then vent the chamber and open it.

8. Place sample chips into place in the chamber.

9. Close the chamber, then pump down.

10. When a high vacuum has been achieved, begin the etching process.

11. When the process is complete and the plasma has been extinguished, vent the chamber and open it.

12. Remove sample chips from the chamber, then close the chamber and set it in the stand-by arrangement.

A.5 Polymethyl methacrylate spin coating recipe

All electron beam lithography used in the fabrication of InAs nanowire quantum dot devices used 950K PMMA A4 as the electron beam resist. 950K PMMA A4 is a 4% solution of 950 000 molecular weight polymethyl methacrylate (PMMA) resin in anisole produced by MicroChem Corp. of Newton, Massachusetts, USA.

After electron beam exposure, the PMMA resist can be developed using methyl isobutyl ketone (MIBK). During lift off, clean up, or otherwise, PMMA can be removed from the sample chip or other surfaces using Remover PG, which is a proprietary MicroChem Corp. solvent containing 99% N-methylpyrrolidone. When PMMA film thickness is selected, it is important to note that metal film lift off is consistently achievable when the ratio of PMMA film thickness to total metal film thickness is 3:1 or greater.

Always test the spin coating process prior to spin coating a sample chip for device fabrication using an extraneous Si chip. Ensure that the spinner and the PMMA is behaving as expected, and check to make sure that the desired film thickness is produced.

1. Pre-heat a baking hot plate or oven to 180°C.

2. Secure the sample chip on the spinner chuck and program the spinner with the process steps in Table A.3 for the desired thickness.

Step	Spinning speed	Duration	Acceleration
Speed up	500 rpm	10 s	4 050 rpm/s
Spin	See Table A.4	45 s	10 125 rpm/s
Slow	0 rpm	5 s	-650 rpm/s

Table A.3: Polymethyl methacrylate spin coating process.

3. Apply PMMA to the sample chip surface and spin coat the sample chip using the programmed process. When applying PMMA to the sample chip surface, use enough PMMA to guarantee coverage of the sample chip surface and do not allow bubbles to form. Bubbles and particles will cause streaking and inconsistency in the resulting film thickness.

4. Remove the sample chip from the spinner chuck and bake it for 15 minutes at 180°C. Cover the sample chip to protect from particle contamination if an uncovered hot plate is used for baking.

Spinning speed	Thickness	Apparent film colour on Si
1200 rpm	350 nm	yellow pink
1700 rpm	300 nm	yellow red
3000 rpm	220 nm	light red
4000 rpm	200 nm	blue

Table A.4: Polymethyl methacrylate spin coating speeds and results including the colour of the film on an unoxidized Si substrate.

5. Allow the sample chip to cool to room temperature before further processing. Failure to cool the sample chip sufficiently can result in the PMMA film becoming crazed with fine cracks when the hot film comes into contact with cool liquids. Cover the sample chip to protect from particle contamination while cooling.

A.6 Electron beam lithography recipe

After a layer of an electron beam resist, such as polymethyl methacrylate (PMMA), has been spin coated onto a sample chip, an electron beam lithographic (EBL) pattern must be written onto the resist in order to fabricate the desired features.

The details of an EBL pattern writing will depend on the scanning electron microscope (SEM) and EBL software used. During earlier work on device development, the EBL writing was performed on a LEO 1530 field emission SEM; the final devices were produced using EBL writing using a RAITH150-TWO EBL system[4].

1. If the EBL system is not on, turn it on and allow parts to warm up.

2. Prepare the sample chip for EBL pattern writing. If a sample stage or sample mount is available, sample chip mounting can be performed before the vacuum chamber is opened. A very small amount of gold particles must be applied to the resist surface along one side or near a corner; these particles will be used to adjust the focus. If features already exist on the sample chip, the gold particles will need to be close to, but not in, the area of interest.

3. Vent and open the EBL system vacuum chamber.

4. Carefully, place the sample stage or mounted sample chip into the vacuum chamber. Be sure to check that the sample stage or sample mount is in the correct position and the sample chip is secure.

[4]Raith GmbH, Dortmund, Germany

5. Close and pump down the vacuum chamber.

6. When the vacuum chamber has reached the required pressure, move the sample chip to an appropriate position. The sample chip should be in a position so that when the electron beam turns on only non-critical areas are exposed. A camera in the vacuum chamber should aid in this maneuvering.

7. Turn on the electron beam and select the appropriate aperture. The beam current should be measured before and after EBL pattern writing to ensure consistency. For recommended aperture sizes and beam currents, see Table A.5.

8. Locate the gold particles and use them to focus on the surface of the resist. In the process of focusing, many settings will need to be adjusted: focus, working distance, image brightness, image contrast, stigmation, and electron beam alignment. As focus is achieved, the magnification should be progressively increased and the other settings iteratively adjusted in order to get the best possible image. These adjustments can be expedited by starting from settings recorded during a previous session. It should be possible to resolve a feature as small as several nanometers.

9. If alignment marks have already been fabricated, then these features should be used to locate the area of interest. Alignment should be performed with as little extraneous exposure to the resist in the areas of interest as possible. This alignment can be performed manually or may be automatically performed using the EBL system software.

10. Write the selected EBL patterns with an appropriate electron beam exposure dose for the resist thickness in use. For recommended electron beam exposure doses, see Table A.5.

11. When EBL pattern writing has been completed, turn off the electron beam, and vent and open the vacuum chamber.

12. Carefully, remove the sample stage or sample mount form the vacuum chamber, and remove the sample chip from the sample stage or sample mount.

13. Close and pump down the vacuum chamber, and set the EBL system in stand-by mode.

Feature	PMMA thickness	Voltage	Electron beam Aperture	Current	Dose
Bottom gate	200 nm	30 kV	10 µm	43.5 pA	395 µC·cm^{-2}
Gate contacts	220 nm	30 kV	30 µm	300 pA	400 µC·cm^{-2}
Ohmic contacts	350 nm	30 kV	30 µm	300 pA	440 µC·cm^{-2}

Table A.5: Recommended specifications for electron beam lithographic pattern writing based on work using a Raith 15-TWO system.

A.7 Electron beam lithography pattern design

A.8 Resist development recipe

After electron beam exposure, polymethyl methacrylate (PMMA) resist can be developed using methyl isobutyl ketone (MIBK). MIBK is soluble in isopropanol (IPA); as a result, IPA is used as both a diluter of MIBK and a developer stop. Large patterns can be developed using full-strength MIBK, but it has been found that fine patterns and details are best resolved using a 25% solution.

1. Clean all instruments and glassware with a progressive and thorough wash using acetone, isopropanol, and then deionized water prior to use.
2. Prepare a 1:3 solution of MIBK:IPA for use as the developer, and a container of IPA for use as the stop bath.
3. Submerge the exposed sample chip in the developer for 60 s without agitation.
4. After 60 s, immediately submerge the sample chip in the stop bath for at least 30 s.
5. Carefully, blow dry the sample chip using nitrogen (N_2) gas. Be particularly careful when blowing dry the sample chip after developing fine patterns such as the bottom gate lines as fine structures are very delicate.
6. Examine the developed pattern using an optical microscope to check for expected results prior to metal deposition.

A.9 Metal deposition recipe

After electron beam lithographic patterns have been written and developed, metal films must be deposited on the sample chip in order to create devices and the conductive circuits

that will connect the devices to experimental apparatus. The metal films are deposited using electron beam evaporation to allow slow and controlled deposition rates in order to improve the quality of the resulting film.

The preferred material for conductive circuits is gold (Au), but Au does not adhere to Si surfaces well; an adhesion layer is necessary and can be achieved by a thin layer of titanium (Ti) or nickel (Ni). In most circumstances, Ti is favoured due to the ferromagnetic properties of Ni; however, Ni is used in the creation of the source and drain contacts as greater success has been achieved when using Ni in creating ohmic contacts to InAs nanowires.

In order to ensure success when lift off is performed, it is important to perform metal deposition without carousel rotation and with the sample chip mounted directly over the metal source. Any angle in the sample chip mounting or rotation during deposition will be reflected in the metal film profile and may cause problems when lift off is attempted. It is also important to ensure that the resist layer thickness has been selected appropriately; lift off is consistently achievable when the ratio of resist film thickness to total metal film thickness is at least 3:1 or greater. Ideally, this ratio should be 5:1.

1. Check that the electron beam evaporator is in stand-by mode and there are no processes running.

2. Vent and open the vacuum chamber. Any vacuum chamber door locks must be released before venting the vacuum chamber.

3. Mount the sample chip on a sample holder directly over the metal source. If the sample chip is not over the metal source, then rotate the carousel to the correct location. If necessary, cover any other deposition sources or open sample holders in order to prevent excess undesired metal deposition. Any viewports that need cleaning should be cleaned as well; Kapton®[5] tape, which is an adhesive-coated polyimide film, can be used to cover viewports that are regularly coated by film depositions in order to facilitate future cleaning.[6]

4. Close the vacuum chamber door and pump down the vacuum chamber to at least 5 µTorr. Vacuum seals should be checked and, if necessary, cleaned prior to closing the vacuum chamber door.

5. While the vacuum chamber is pumping down, program the electron beam evaporator controller with the deposition characteristics in Table A.6 appropriate for the features

[5]DuPont, Wilmington, USA

[6]This step refers specifically to the procedure used at the Centre for Integrated RF Engineering when working with the Intlvac Nanochrome I system manufactured by Intlvac of Georgetown, Canada. Mounting of the sample chip and preparation of the vacuum chamber may vary depending on the electron beam evaporator used.

being fabricated. An adhesion layer and the subsequent Au film should be evaporated during the same deposition session without breaking vacuum to maintain the integrity of the film deposited.

6. When the vacuum chamber pressure is at least 5 µTorr, start the metal film deposition. As heating of a metal source can increase the chamber pressure due to outgassing, waiting for further reduction in the chamber pressure can result in a higher quality film with fewer defects. Monitor the metal film deposition process closely to ensure that the deposition is proceeding as expected.

7. When the deposition is complete, allow the metal sources to cool for at least 5 minutes prior to venting. A hot Ti source can oxidize quickly upon contact with oxygen, the resulting layer of titanium dioxide (TiO_2) is difficult to melt and can render a Ti source useless.

8. When the metal sources have cooled, vent and open the vacuum chamber. Any vacuum chamber door locks must be released before venting the vacuum chamber.

9. Remove the sample chip from the vacuum chamber and unmount it from the sample holder.

10. Close the vacuum chamber door and begin pumping down the vacuum chamber. Set the electron beam evaporator in stand-by mode before leaving it.

	Titanium (Ti)		Nickel (Ni)		Gold (Au)	
Features	Thickness	Rate	Thickness	Rate	Thickness	Rate
Bottom gates	15 nm	1 Å/s			25 nm	1 Å/s
Gate contacts	25 nm	1 Å/s			35 nm	1Å/s
Ohmic contacts			30 nm	1 Å/s	50 nm	1Å/s

Table A.6: Metal film deposition characteristics.

A.10 Lift off recipe

After metal films have been deposited on a developed sample chip, lift off can be performed using Remover PG, which is a proprietary solution of 99% N-methylpyrrolidone produced by MicroChem Corp. of Newton, USA, to remove the resist and extraneous portions of the metal film. It is important to make sure that all extraneous metal film has detached from

the sample chip prior to removal of the sample chip from the Remover PG as a second lift off attempt is rarely effective.

Remover PG is a very effective solvent and care should be used in its handling. Spills should be cleaned up promptly, especially on plastic, painted, or dyed surfaces. The chemical compatibility of instruments and containers should be verified prior to use with Remover PG. Remover PG is a volatile solvent and must be covered or sealed to prevent loss through evaporation.

1. Clean all instruments and glassware with a progressive and thorough wash using acetone, isopropanol, and then deionized water prior to use.

2. Prepare a container of Remover PG. A glass container is recommended because extended exposure to Remover PG does not affect glassware, the container can be easily sealed using a sealing film such as Parafilm M[7], and the container can be heated.

3. Submerge the metal film-coated sample chip in a covered container of Remover PG for at least 10 hours.

4. After at least 10 hours, heat the container of Remover PG to 80°C for 30 minutes.

5. Gently agitate while continuing to heat the Remover PG until all extraneous metal film appears to have lifted away from the sample chip surface. Agitation will encourage flow of Remover PG over the surface of the sample chip and underneath the metal film. A glass pipette can be used to gently squirt Remover PG at the submerged sample chip to further encourage lift off of the extraneous metal film. Care should be taken in squirting or agitating the sample chip when fine patterns are being lifted off to prevent damage to fine structures due to overzealous squirting or agitation. It may be advantageous to use a magnetic stir bar to promote flow of Remover PG over the sample chip if a chip holder apparatus is being used to elevate the sample chip away from the stir bar.

6. Carefully remove the sample chip from the Remover PG. Take care to avoid allowing metal film flakes to reädhere to the surface.

7. Gently rinse the sample chip thoroughly with isopropanol while examining to make sure that all loose metal film flakes have been rinsed off of the surface.

8. Carefully, blow dry the sample chip using nitrogen (N_2) gas.

9. Examine the resulting metal film pattern to check for expected results prior to further processing.

[7]SPI Supplies, West Chester, USA.

A.11 Nanowire suspension recipe

After the bottom gates have been laid down, InAs nanowires must be dispersed over the surface of the sample chip. In order to facilitate nanowire dispersion, a suspension of InAs nanowires in isopropanol (IPA) can be prepared.

1. Clean all instruments and glassware with a progressive and thorough wash using acetone, isopropanol, and then deionized water prior to use.
2. Carefully place a fragment of InAs nanowire substrate into a small bottle.
3. Add approximately 50 µL of IPA for every square millimeter of nanowire growth to the small bottle. The amount of IPA used can be adjusted; this proportion of nanowires and IPA has been found to result in a reasonable number of InAs nanowires on the sample chip surface when used for dispersion by spinning.
4. Sonicate the small bottle for 15 s at a medium power setting. The resulting suspension should be clear with a very faint dark tint; if GaAs nanowires were mistakenly used, the resulting suspension would have a murkier, grey colour instead.
5. Remove the InAs nanowire substrate from the small bottle before storage.
6. If necessary, filter the suspension through Grade 1 (11 µm) filter paper. Filtering can remove some particles and produce a cleaner result when nanowires are dispersed over the surface of sample chips.

A.12 Nanowire dispersion recipe

After the bottom gates have been laid down, InAs nanowires must be dispersed over the surface of the sample chip. A good dispersion of nanowires can be accomplished by using a spinner to spread a suspension of InAs nanowires in isopropanol (IPA) as the IPA evaporates, leaving behind InAs nanowires scattered across the surface of the sample chip. New suspensions can be prepared for use or previously prepared suspensions can be used with similar effectiveness.

1. Clean all instruments and glassware with a progressive and thorough wash using acetone, IPA, then deionized water prior to use.
2. If a previously prepared suspension is being used, ultrasonicate the suspension for 10 s at a medium power setting. When stored for even a short period of time, nanowires can settle out of the IPA and clump together into small dark knots in the solution that are visible by eye.

3. Secure the sample chip on the spinner chuck and program the spinner with the process steps in Table A.7.

	Spinning speed	Duration	Acceleration
Rest	0 rpm	90 s	0 rpm/s
Spin	300 rpm	300 s	100 rpm/s

Table A.7: Nanowire dispersion process.

4. Use a micropipette to drop 150 nL of nanowire suspension for every square millimeter of sample chip surface and spin the sample chip using the programmed process. If more nanowire suspension was used, then the spin duration must be adjusted as it is important that the sample chip continues to spin while the last droplets of IPA are evaporating in order to ensure an even dispersion of nanowires.

5. Remove the sample chip from the spinner chuck.

6. Examine the nanowire dispersion using an optical microscope to check for sufficient dispersion of nanowires over bottom gates. Repeat if necessary.

A.13 Sulfur passivation recipe

After source and drain contact patterns have been written onto the electron beam resist of a sample chip and developed, metal must be deposited onto the InAs nanowires to create ohmic source and drain contacts. However, in order to create successful and reliable ohmic source and drain contacts to the InAs nanowire, it is necessary to first etch away the naturally occurring oxides. (InO_x and AsO_x)

A dilute 0.5% solution of 3M ammonium polysulfide ($(NH_4)_2S_x$) can be used as a slow and controlled selective etch of InAsO, which also passivates the surface of the InAs nanowire using sulfur (S) atoms and improving the quality of the ohmic contacts [XYZ]. An alternative etch that may be used is a dilute hydrogen fluoride (HF) solution; however, an HF etch will not provide sulfur passivation and the ohmic contact quality may vary. A new solution starting from the stock ammonium sulfide ($(NH_4)_2S$) solution should be prepared each time in order to ensure consistently ohmic contacts are produced.

As with many sulfurous compounds, $(NH_4)_2S_x$ emits noxious fumes and must be handled inside a fume hood only. Note that $(NH_4)_2S_x$ may be a source of hydrogen sulfide (H_2S) gas, which is noxious, poisonous, flammable, and smells of rotten eggs. Disposal should be performed carefully and using an adequate dilution to prevent any such hazards.

1. Clean all instruments and glassware with a progressive and thorough wash using acetone, isopropanol, then deionized water prior to use.

2. Add 0.015 mol (0.481 g) of elemental S to a 5 mL volumetric flask. A glass volumetric flask is ideal to ensure that the resulting solution is of the correct molarity, and to aid in mixing.

3. Slowly add 5 mL of 20% $(NH_4)_2S$ stock solution[8] to the volumetric flask to produce a 3M solution of $(NH_4)_2S_x$.The stock solution should be added slowly in small amounts to allow the S to dissolve into the solution. Dissolution of S into $(NH_4)_2S$ should be aided by swirling the solution around the base of the volumetric flask or by ultrasonication. The colour of the solution will change from yellow to a dark orange or red as the S dissolves into the stock solution. Only $(NH_4)_2S$ can be used to dissolve S as it will not dissolve into deionized water.

4. Prepare 200 mL of deionized water in a separate sealable container.

5. Add 1 mL of the prepared 3M solution of $(NH_4)_2S_x$ to the deionized water prepared in the previous step to produce a 0.5% solution of 3M $(NH_4)_2S_x$. Mix this solution well and seal to prevent evaporation and degradation of the etching solution.

6. Heat a small amount of the 0.5% solution of 3M $(NH_4)_2S_x$ in a small rubber-stoppered bottle to 55°C. The rubber stopper should seal the mouth of the bottle and have a hole through which a thermometer or thermocouple can be inserted. The contents of the bottle should be sealed to avoid any water loss through evaporation; water loss will lead to degradation of the etching solution and a S precipitate to form. The temperature should be closely monitored and maintained in order to avoid degradation of the etching solution.

7. When the etching solution has reached 55°C, submerge the developed sample chip in etching solution and reseal the bottle. Soak the sample chip for 30 minutes. The solution should be illuminated brightly with a 100 W incandescent bulb, or a bulb of equivalent luminosity, in a explosion-proof lamp for the entire duration of the etching and passivation step. Monitor the solution temperature closely to avoid degradation of the etching solution.

8. After 30 minutes, remove the rubber stopper from the bottle, and remove the bottle from the heat source and place it under a gentle stream of deionized water. Allow the deionized water to cascade for at least 5 minutes or until the etching solution has been completely displaced.

[8]Fisher Scientific Company, Ottawa, Canada

9. Carefully, remove the sample chip from the deionized water, and rinse thoroughly with fresh deionized water.

10. Carefully, blow dry the sample chip using N_2 gas. Be particularly careful when blowing dry the sample chip at this stage as to avoid dislodging nanowires or damaging fine structures.

11. Proceed immediately to metal deposition. If possible, minimize the amount of time the sample chip spends in an oxygen atmosphere. If possible, transfer the sample chip under decreased illumination, and transfer it to a vacuum chamber as soon as possible.

Appendix B

RF experimental setup

In anticipation of future experiments on one-qubit rotations using electric dipole spin resonance, RF wiring, filtering, and experiment components were incorporated into dilution refrigerator customization as well as device mounting and printed circuit board (PCB) designs. A schematic illustration of the experimental setup for spin rotation excitation with transport measurements is shown in Fig. B.1.

In these experiments, pulsed AC voltages are combined with the existing DC signals used to form the double quantum dot system in order to rapidly translate a quantum dot in the axial direction. The AC signals originate from a room temperature RF circuit designed to create pulsed AC voltages; these signals are then transmitted through the dilution refrigerator using a series of lengths of semi-rigid coaxial cable. Stainless steel (SS outer conductor, BeCu inner conductor, 0.085 in outer diameter) coaxial cable is used in the upper stages of the refrigerator, from the room temperature plate to the 4 K plate, in order to reduce conduction of heat from the room temperature connection. From the 4 K plate to the mixing chamber plate of the refrigerator, beryllium copper (BeCu outer and inner conductor, 0.086 in outer diameter) coaxial cable is used to reduce signal attenuation. Lastly, from the mixing chamber plate down to the PCB assembly, copper (Cu outer and inner conductor, 0.047 in outer diameter) coaxial cable is used, which has the least attenuation of all three varieties of coaxial cable used. At the 4 K cooling stage, the coaxial cables are thermally anchored through +6 dB Aeroflex 40A-06 attenuators; at the still and mixing chamber cooling stages, thermal anchoring of coaxial cables is through +3 dB Aeroflex 40A-03 attenuators. Finally, the AC signals are combined with the DC signals at the RF printed circuit board using Marki BT-0030SM bias tees.

The microwave source used to generate the AC voltages is the Rohde & Schwarz SMF100A source with a quoted maximum power of 15 dBm. The RF switch used to pulse the AC voltages is an ATM SP1T switch. In addition to these components, Marki PD-0220 splitters, which function at frequencies up to 20 GHz, and Marki M2-0220 mixers

are also incorporated.

B.1 Powder filter performance

All low-temperature experiments use filtered DC lines. Among the filters used, the copper powder filters and silver paste filters do not use circuit elements, and were designed and constructed in-house. The attenuation of these filters were tested and the mean results are shown in Fig. B.2 and B.3.

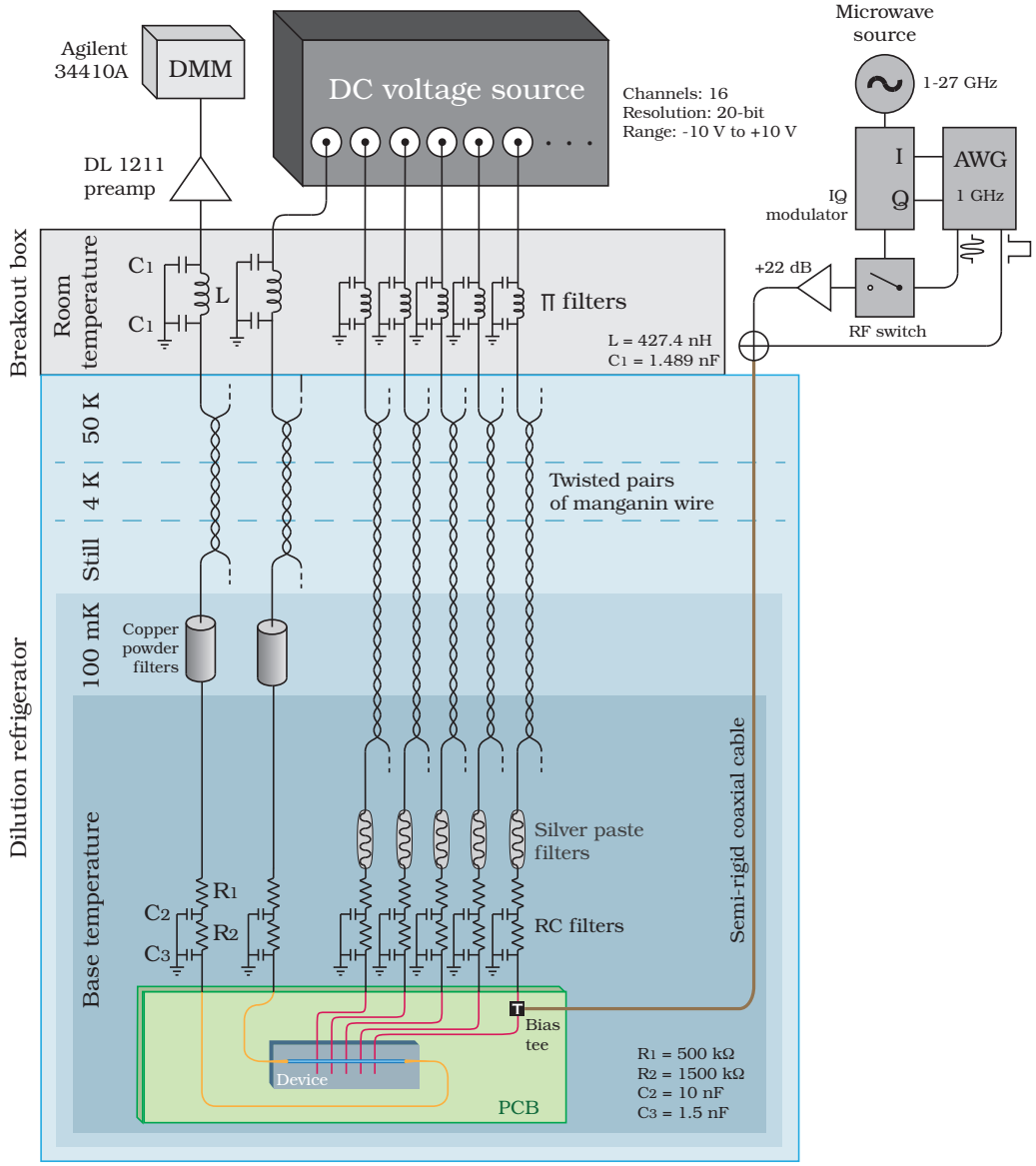

Figure B.1: A schematic illustration of the RF experiment setup for the investigation of electric dipole spin resonance in a double quantum dot system using transport measurements. Spin resonance excitation is performed by the apparatus to the upper right of the image and transmitted to the quantum dot using semi-rigid coaxial cable (brown). Transport measurements are performed by the digital multimeter (DMM) and preamplifier in the upper left.

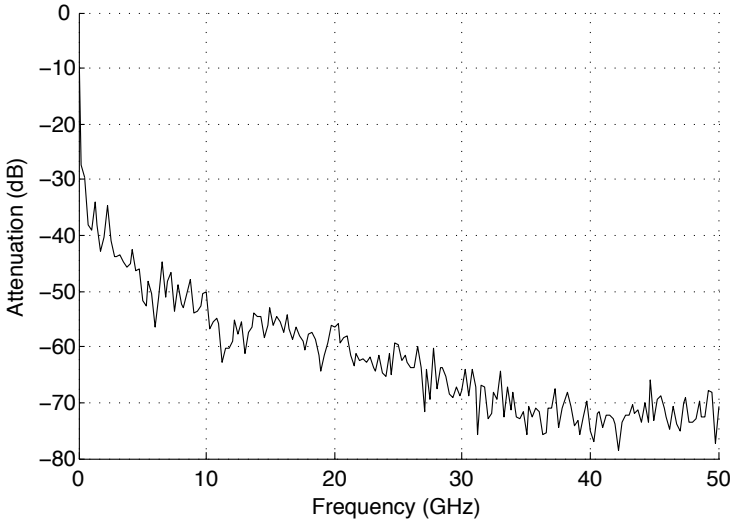

Figure B.2: A plot of the average attenuation of the four copper powder filters created for the experimental setup.

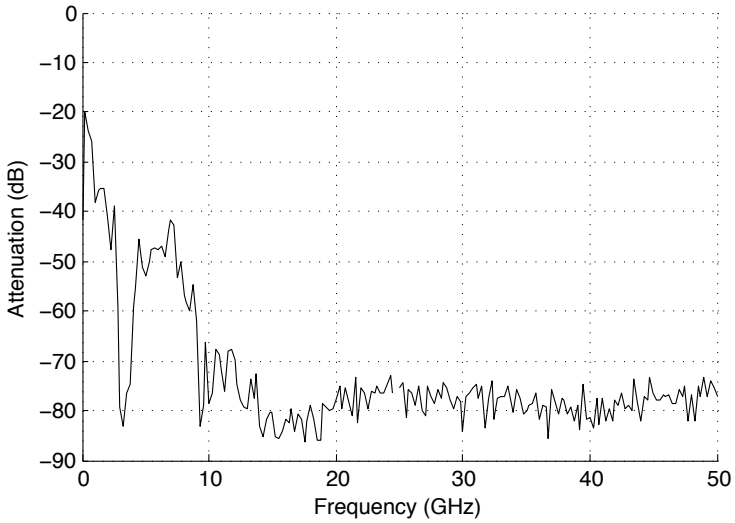

Figure B.3: A plot of the average attenuation of the twenty silver paste filters created for the experimental setup.

"They're just like regular dots, only smaller."

— D. B. Criger