Assessing Au-Al Wire Bond Reliability Using Integrated Stress Sensors

by

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A thesis
presented to the University of Waterloo
in fulfilment of the
thesis requirement for the degree of
Master of Applied Science
in
Mechanical Engineering

Waterloo, Ontario, Canada, 2010
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Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Abstract

Wire bond reliability testing typically consists of aging bonds in a high temperature environment for long time periods, and removing samples at intervals to assess bond shear strength and characterize the bond cross sections. In this way, the degradation of the bond can be monitored at discrete time intervals, and it is determined whether the bond will be reliable during the specific service life. This process can be labour and time intensive. An alternative method is reported using an existing test chip that allows for contact resistance measurements and provides signals from piezoresistive integrated CMOS microsensors located around test bond pads. The sensors are sensitive to radial compressive or tensile stresses occurring on the bond pad due to intermetallic formation, oxidation, and crack formation at the bond interface.

Two sets of identical test chips are bonded with optimized Au ball bonds and aged for 2000 h at 175 ℃. One set is connected to equipment which monitors signals from the stress sensors and the contact resistance of the bonds. The other set is destructively tested by shear tests and cross sectioning. It is found that the stress sensors are capable of indicating which stage of bond aging is experienced by relating the signal to the relative density of the intermetallic compounds (IMCs) and oxide which form during aging.

This research offers a valuable new method for accelerating bond process development. By using the sensors to determine the stage of aging experienced and the magnitude of changes happening to the bond, the initial bond quality and bond reliability can be roughly characterized. A useful application is in comparing large samples of bonds made under varying conditions, and determining relative reliabilities of the bonds. A small sample size is required, as the sensors allow for complete continuous aging histories of individual bonds, which was not previously possible.

A new test chip is designed for use in future studies which allows for contact resistance measurement, and provides stress signals for up to 55 bonds. A multiplexer integrated on the chip allows for measurements from one specified bond pad at a time. The chip is also equipped with x and y-force measurements which can be used to monitor bond process, and a resistive temperature detector for temperature measurement.

A miniaturized bond aging system is designed to facilitate future works where chips are subject to high temperature storage. A heating element fits over the cavity of a microelectronic package containing the test chip, and allows for precise temperature control, while using less power than a conventional oven, and maintaining a low temperature at electrical connections to the package.

Acknowledgements

I wish to thank my supervisor, Dr. Michael Mayer for his assistance and support during my stay as a Masters student. I would also like to thank MK Electron and Microbonds for funding this project. I am grateful for the Ontario Graduate Scholarship and the University of Waterloo President's Scholarship which helped make this work possible. Additional funding was also provided by the Natural Sciences and Engineering Research Council of Canada (NSERC) and Ontario Centers of Excellence (OCE).

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1. Introduction

In microelectronic systems, computer chips are attached to substrates, electrically connected to the substrates, encapsulated, and then affixed to boards. The electrical interconnect between the chip and the substrate is most commonly made by the process of wire bonding where a thin wire is bonded first to pads on the chip and then to pads on the package.

1.1. Reliability

Failure of key interconnections renders entire devices defective. As more than 4×10^{12} wire bonds are made each year [1], it is of vital importance that wire bonds are reliable. Reliability depends on the structure of the bonding pad, the materials of the wire and the bond pad, contamination, and the process parameters used during bonding. When the process is optimized, reliability is greatly improved. Defect rates in industry using optimized bonds are typically 20 to 30 parts per million [1].

1.2. Motivation

As the microelectronics industry evolves, there is an ever present need to increase the performance of devices while decreasing the cost. As integrated circuits become more complex, the I/O density increases, necessitating finer pitch of wire bonds. Due to the high cost of Au, different materials such as Cu are proposed for the wire bonding process as a means of cost savings. As a result, the wire bonding industry is faced with the challenge of optimizing the bonding process with a wide range of different wires so that the bond has a high initial strength and high long term reliability. As the initial strength of a bond is not necessarily related to its long term reliability, the reliability must be assessed by performing accelerated aging tests. In these tests, sample bonds are kept in high temperature storage for an extended period. Sometimes, sample bonds are periodically removed and evaluated for mechanical strength and sectioned in order to observe micro-

structural changes to explain the bond degradation. If the sample bonds are able to maintain an acceptable strength for a minimum time period then the process used is qualified as reliable. This qualification process is expensive and labour intensive, and provides a poor time resolution of results, as samples are destructively examined at discrete time intervals, or at the end of aging only. To learn more about reliability and find ways to increase it, the need exists for an alternative method of observing bond degradation which can monitor the bond interface in real time while providing results at a lower cost. Although standard qualification procedures will not be replaced, such an alternative gauge of reliability could prove useful for accelerating initial bond evaluation, and comparisons of bond materials, processes, and parameter values with respect to reliability.

1.3. Non Destructive Reliability Test Methods

As a wire bond degrades, the interface between the bonded wire and the substrate undergoes various changes before electrically or mechanically failing. Intermetallic compounds (IMCs) form at the interface and on the adjacent pad material. As the pad metallization and bump interdiffuse and are consumed at different rates, the IMCs present at the interface grow and change over time [1]. Due to different interdiffusion rates, Kirkendall voids form both at the interface and in the pad material adjacent to the bond [2]. Due to coalescence of these voids and oxidation of IMCs [3], the bond weakens and cracks may develop.

The two proposed methods of non-destructive bond monitoring are contact resistance measurements and stress measurements. Contact resistance measurements are performed by passing a current of 1 mA through the bond and measuring the voltage drop across the interface. Using Ohm's law, the contact resistance can be calculated. Contact resistance increases as bonds age which is attributed to reduced interface area and high resistance of IMCs [1].

Stress measurements are accomplished by integrating piezoresistive stress sensors around bond pads in custom test chips [4]. As the bond interfaces expand or contract, a differential voltage signal generated by the stress sensor increases or decreases proportionally. These stresses are caused by volume changes due to interdiffusion and formation of IMCs with different densities. Both sensor signals and contact resistance may be monitored continuously and automatically, providing a high time resolution and requiring no additional labour once the aging process has started.

1.4. Objective

The objective of this research is to characterize the usefulness of the integrated stress sensor to monitor bond aging in a typical wire bond product. To this end, multiple stress signals with contact resistance measurements are compared to shear test data and microstructural analysis of Au bonds on multilayer Al pads. Relationships between the non-destructive signals and destructive test data are investigated.

1.5. Thesis Outline

In order to investigate the relationship between the non destructive signals and standard destructive tests, several steps are taken. Appropriate die attach, bonding processes, and accelerated aging regime are selected and setups are built to store the chips at high temperature and measure signals from integrated circuitry. In total, four sets of bonds are made on identical chips. Two sets are made for destructive analysis. One set is made for shear testing at discrete intervals and one set for cross sectioning and examining at the same intervals. Two sets are made for non-destructive testing. One set is made for contact resistance measurement and one for stress measurement. Once the chips are aged, samples from each interval are shear tested and sectioned. It is important to examine the bond cross sections as the microstructural changes occurring at the interface are used to explain the results from all other destructive and non destructive tests. These destructive

measurements are then compared to the non-destructive measurements and it is observed that microstructural changes such as IMC growth or oxide formation can be observed through stress signals and contact resistance measurements. While not enough data is available to directly correlate these results to standard bond failure criteria, the quality of a bond can still be estimated by observing the rates at which microstructural changes occur.

The final section of this thesis is the introduction of new methods to facilitate these measurements for future studies. A new test chip is designed which can take 55 contact resistance and stress measurements for the same bonds, while performing all multiplexing on-chip with integrated circuitry. This reduces the number of chips required and eliminates the need for dedicated multiplexers in the setup. A new miniaturized bond aging device is developed. This device heats the chip more rapidly than conventional ovens, while leaving all package connections at low temperatures and allowing for greater flexibility for setup changes.

2. Literature Review

2.1. Wire Bonding Process

The first level electrical interconnect between an integrated circuit and package or substrate can be achieved by a variety of methods such as flip chip, tape automated bonding (TAB), and wire bonding. The flip chip process involves deposition of solder balls or non-solder bumps onto chip pads, flipping the chip over and mounting it on external circuitry, and then achieving electrical connection through the bumps. This method creates the highest I/O density but is cost intensive and inflexible to process changes [1].

TAB was developed as an alternative to wire bonding in the 1960s when the wire bonding process was much slower and less efficient [1]. TAB uses solder or Au bumps to attach integrated circuits (IC)s to a thin tape which contains the circuitry for attachment to a PCB. Due to advances in wire bonding technology to increase speed and reduce pitch of wire bonds, this method is largely obsolete for mainstream applications, although still has a niche where high production volume and high chip cost make it economical, such as flat-panel displays [1].

Wire bonding is the most common first level interconnect method accounting for approximately 90% of the total microelectronics packaging over the last decade [5]. It is popular due to its relative low costs, high speed, and flexibility of design changes. Wire bonds can be either wedge-wedge bonds or ball-wedge bonds. Both processes use pressure and ultrasonic energy. In the ball bonding process, the device to be bonded is die-attached to a substrate or package and placed on a heater on the wire bonder. A wire is fed through a capillary and clamped in place with the end of the wire protruding from the capillary tip as shown in Fig. 1 a. An electrode then applies a spark known as the electrical flame off (EFO) which melts the end of the wire. Surface tension causes the molten metal to form a free air ball (FAB) which rapidly solidifies at the end of the wire as

illustrated in Fig. 1 b. The capillary presses the free air ball onto the bond pad with an impact

force, deforming it to its final shape (Fig. 1 c). The deformed ball is then held in place with a bond

force which is low enough to ensure that no further deformation takes place, as a transducer

applies ultrasonic energy to the capillary tip creating a solid state bond between the ball and pad.

The clamp holding the wire then relaxes (opens), and the capillary moves to the location of the

second bond while the wire is fed through as shown in Fig. 1 d-e. The capillary presses the looped

wire onto the bond pad of the package, and bonds it using pressure, heat and ultrasound. This

bond is known as the second bond, and is also referred to as the wedge bond, stitch bond, or cres-

cent bond. Then, the capillary and the open clamp move upwards by a certain distance, feeding

out a defined length of wire before stopping. The clamp closes, preventing any more wire from

feeding through the capillary. The capillary and clamp then move upwards again, causing the wire
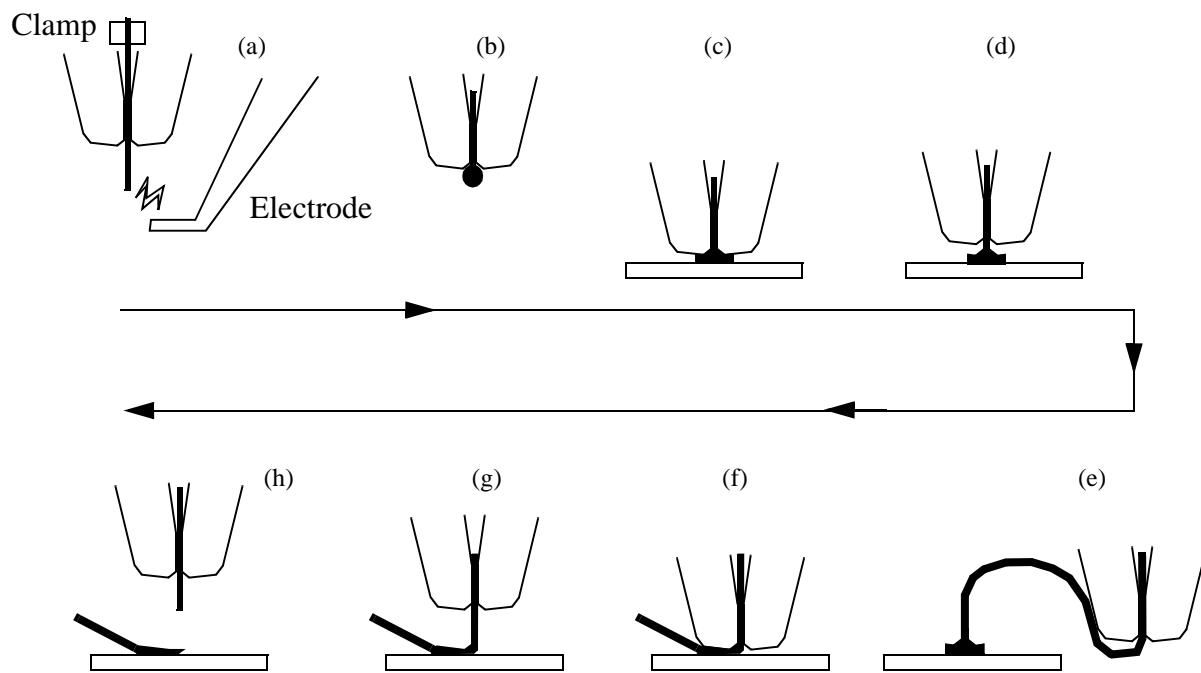
Fig. 1 Wire bonding process. (a) FAB formation. (c) Impact deformation and thermosonic bond-
ing. (e) Looping. (f) Second bond formation through heat, pressure and ultrasound. (g) Wire feed.
(h) Tail breaking.

to break at its weakest point which is located where the wire is pinched after the second bond location as is seen in Fig. 1 h. This leaves a wire tail hanging from the capillary which is available for formation of the FAB of the subsequent bond.

The wedge-wedge wire bond process consists of 2 wedge bonds instead of one ball bond and one wedge bond. In this process the wedge bond loops must be oriented in the same direction as the ultrasonic transducer, requiring a dedicated rotational axis, while the second bond of a ball bonding process may be positioned at any angle. Wedge-wedge bonds are often used for bonding Al wire or ribbons onto Al bond pads, and are generally preferable where extremely low loop heights or room temperature Al bonds are required [1].

2.1.1. Wire Bonding Materials

In a wire bonding process, the wire material must adhere to the bond pad materials for the first and second bonds. The most common wire material is Au due to its absence of oxide and good formability. The degree of purity is expressed as the percentage of Au in the wire. For example wire that is 99% pure Au is referred to as "2N" since the percentage is expressed with 2 nines. Wire that is 99.99% pure Au is referred to as "4N" which is the wire used in the experiments described in this thesis. The remaining 0.01% wire composition includes various dopants such as Cu, Be, Ni and Pd which although supplied in small amounts can greatly improve the wire properties. Interstitial dopants such as Be increase the mechanical strength of the alloy by hindering dislocation movement [5]. Substitutional dopants such as Pd, create much larger stress fields and strengthen the wire even more. With the exception of Pd, however, most dopants significantly reduce the conductivity of the wire [5].

Other wire materials used in industry include Cu wires, and insulated wires. Cu wires have the advantage of being less expensive, but oxidize quickly in air, and form harder FABs. Cu requires

greater bond force and ultrasound, increasing the likelihood of pad damage or chip cratering [6].

To prevent oxidation, the wires must be stored in an inert environment and a shielding gas must be

supplied during bonding [6]. Although Cu oxide is removed from the ball during FAB formation,

it remains on the wire and may interfere with reliable second bond formation.

Insulated wires are coated with a thin organic layer which burns off during the EFO process and

flows out of the bond during ultrasonic application. These wires may touch each other without

short circuiting, and the coating prevents Cu wires from oxidizing. With appropriate process

adjustments, these wires reach standard bond quality by removing the insulation layer from the

bond interface [7].

Wire bonds can be made on many substrates, including Ag metallizations [7], Au, or Al. When

wire bonds are to be made between a chip and a ceramic dual in-line (CerDIP) package, as is the

case for this thesis, the material of the chip bond pad is Al containing small amounts of dopants,

typically Cu and Si [1, 3], and the final surface finish of the package lead is Au. Exact composi-

tions of bond wires and bond pad metallizations are not disclosed by the manufacturers and are

not essentially required for the conclusions of this study.

2.1.2. Bonding Mechanisms

When the crystal lattices of two materials align, a solid state bond is formed. Main impediments

to bond formation are roughness, lattice mismatch, and contamination. For chips manufactured

with standard CMOS processes, surface roughness is not a problem. Roughness which may exist

on bond pad or FAB surfaces is flattened out during the impact deformation of the ball, and during

the application of ultrasound. Au and Al both have FCC crystal structures with lattice parameters

of 4.07 Å and 4.05 Å respectively [8]; therefore lattice mismatch should pose no problem to bond

formation. Contamination risks may be minimized by proper cleaning and storage of chips.

Plasma cleaning is a common method of cleaning chip pads where O_2, Ar, or H_2 are typical plasma constituents. The ionized gas bombards the pad surface and can knock off contaminants by impact. When O_2 is used, it can break down by the reaction $O_2 \rightarrow 2O$. The individual O atoms now react with hydrocarbons on the surface, removing them [1]. Fig. 2 shows the improvement in bond reliability which may be attained through plasma cleaning. Storage in a low humidity nitrogen environment may further protect the chip from contamination between the cleaning and bonding stages.

Plasma cleaning removes foreign contaminants, but the oxide which forms on the surface of the Al bond pad still remains and prevents bonding from occurring. This oxide is removed during the ultrasonic process. The friction of the Au ball breaks the oxide which then disperses away from the interface allowing Au to bond with the pure Al.
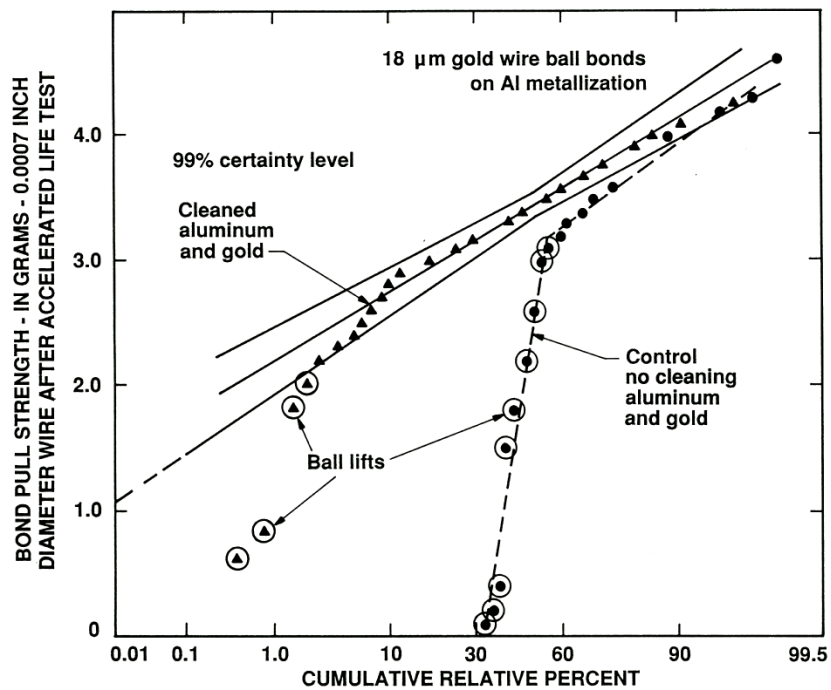
Fig. 2 Pull strength of Au bonds on Al metallizations with and without plasma cleaning after 300ºC high temperature storage for 4 h [1].

An indication of a strong bond is the presence of intermetallic compounds (IMCs) at the interface. While IMC formation is not necessary for a solid state bond to form, IMCs indicate that extensive interdiffusion has occurred resulting in a metallurgical bond [1].

2.1.3. Important Parameters for Wire Bond Optimization

Several process parameters are important for producing a bond of desired shape with optimized strength, which vary depending on the bonding method used. The standard method of ball bonding involves ball deformation through impact with the substrate before ultrasonic bonding begins and is known as the impact deformation process [1, 9]. This is the method used for experiments described in this thesis. An alternative method of ball deformation combines force and ultrasound in a process called ultrasound enhanced deformation (UED) [9]. For the impact force deformation process, the final bonded ball geometry, defined by bonded ball diameter and bond height, is a product of the impact force and the FAB diameter [9]. The FAB diameter in turn is a product of the EFO current, wire tail length, and the EFO time. All process times are typically fixed at standard values, and are not varied between processes. The wire tail length is also held constant, and only the EFO current is modified to optimize FAB size.

Optimized bond strength for a given geometry depends on bond force, bond time, temperature, and ultrasonic power which is varied to achieve the peak strength [1]. Bond temperature is one of the most important parameters for bond shear strength [1]. Typically, bonds are made at temperatures of at least 175ºC in order to ensure formation of a strong bond. Once bond force, temperature, and bond time are established, the bond strength is maximized by optimizing the ultrasound. Maximizing bond strength reduces the chance of bond failure and extends the operating life of the bond. The quality of an optimized ball bond is also expected to vary less between samples than the quality of a non-optimized bond [1].

2.1.4. Bond Evaluation by Pull Test

The pull test is a destructive method of bond strength evaluation developed in the 1960s in which a hook is placed under the wire loop, and pulls the wire upwards until failure occurs [1]. The pull force exerted is measured and indicates bond strength. In order to measure the strength of the wedge bond, the hook is located towards the middle of the loop. To measure the strength of the ball bond the hook is located as close to the ball as possible for a vertical pull direction [3]. While the pull force is an excellent indicator of wedge bond strength, it is not always ideal for evaluating ball bonds. If a minimum of approximately 15% of the interface is bonded, due to the large interfacial area of the ball, failure will occur at the heat affected zone of the ball neck rather than at the pad interface [1], and little information is provided on the ball bond interfacial strength.

2.1.5. Bond Evaluation by Shear Test

The shear test directly measures the strength of the bond interface and is therefore more useful than the pull test in assessing interfacial strength. The shear test is a destructive test where a chisel shaped shearing ram pushes a ball bond off its bond pad at a constant speed, and the force required to break the bond is recorded. Shear strength can be calculated by dividing the required force by the bonded ball diameter to gauge the strength of the bond. Failure may occur according to six distinct modes [10]:

Mode 1. Bond Lift: The entire bond is lifted off the surface leaving only an imprint.

Mode 2. Bond Shear: Intermetallics are left on the bond pad or a large portion of the Au bond is left behind.

Mode 3. Cratering: Pad material and insulating SiO_2 is removed along with the bond.

Mode 4. Bond surface contact: Shearing ram contacts chip and removes metallization

layer.

Mode 5. Shearing skip: Shearing ram is too high and shears top of the bond near the wire.

Mode 6. Bonding surface lift: The bond pad metallization separates from the chip and is

removed with the bond.

Mode 1 failure indicates lack of adhesion between bond and pad. Ideally bonds should exhibit

mode 2 failure.

2.2. Wire Bond Reliability

When a new bond process is developed, reliability is typically assessed by a number of standard

aging tests, e.g. by aging the bonds at elevated temperature while shear testing and/or pull testing

them at periodic intervals. Such high temperature storage (HTS) is performed at various tempera-

tures above 150 ºC. A temperature of 175 ºC is often used because this is the curing temperature

of common moulding compounds which are used in industry to encapsulate bonded dies [5, 3]. If

hermetic package sealing is required, the bonds are exposed to temperatures up to 300ºC for sev-

eral mins; however for applications requiring hermetic packaging, Al wires are generally used

instead of Au [5].

As wire bonds age in HTS, changes occur at the bond interface which over long periods of time

(>1000 h) weaken the bond. This weakening is generally measured by shear tests or pull tests, and

observed through cross sectional analysis. It is possible that the microstructural changes causing

this weakness may be also observed through monitoring the contact resistance [1, 11, 4] and radial

stress fields generated by the aging bonds [4].

2.2.1. Microstructure Evolution

The driving force behind microstructural evolution is the diffusion which occurs between the Au wire bond and the Al pad. IMC formation starts during the bond process and is indicative of strong adhesion. As the metals interdiffuse, IMCs will form according to local availability of each metal. Au_8Al_3 is expected to form first, followed by Au_4Al, Au_2Al, $AuAl$ and $AuAl_2$ [1]. The exact composition of the IMC denoted Au_8Al_3 is debated, and in some phase diagrams is identified as Au_5Al_2 [1, 2].

Conditions of the bonds and environment during HTS influence the rate of microstructure evolution and bond failure. Important parameters are wire composition (2N or 4N), HTS temperature, contamination and atmosphere. 4N wires are used for their low resistivity and large bonding parameter windows, yet readily form IMCs during HTS. 2N wires are doped with Pd, Pt, or Cu which increase strength and slow IMC formation (and therefore bond degradation) [12]. HTS temperature is directly related to the rates of phase transformation and cavity growth. A higher temperature results in more rapid acceleration of the aging process.

Contamination on bond pads and wire reduces reliability. When contamination is severe, and too thick carbon or oxide layers are present on pad surfaces, bonds form less readily and have lower shear strengths. When contaminants are present in lower concentrations, the initial shear strength is unaffected. Koeninger et al [11] report that reliability is unaffected by addition of low levels of contaminants. Harman [1] however, reports that impurities concentrate ahead of the IMC growth and eventually form precipitates. These precipitates attract vacancies resulting from Au and Al diffusion, which eventually coalesce into cavities lowering reliability.

The aging atmosphere can reduce reliability by promoting corrosion or oxidation. Oxidation of IMCs which cannot occur in an inert atmosphere is prevalent in an air atmosphere. In a corrosive atmosphere (35 mbar HCl), failure is greatly accelerated [11].

In this work, 4N wire is used to make bonds aged at 175ºC. Contamination is minimized by plasma cleaning and vacuum storage of chips, and an air atmosphere is used for HTS. The following are case studies from literature which evaluate microstructural evolution of bonds made and aged with similar conditions.

In [13], Noolu observes the formation of 3 intermetallic layers after 2 h of aging 4N Au wire bonds on Al pads at 175 ºC. Underneath the ball there is a layer of Au_4Al. Next is a layer of Au_8Al_3, followed by a layer of Au_2Al, and finally the Al pad metal. After 10 h of aging, the Al pad under the ball bond is almost entirely consumed. Due to a large amount of Au, with decreasing Al supply, the Au-rich phases (Au_4Al and Au_8Al_3) expand down towards the chip surface. After 50 h, the Au_2Al phase has completely converted to Au_8Al_3. After 150 h, the Au_4Al phase has completely replaced all other IMCs and is the only remaining phase. Microstructural evolution as observed by Noolu can be seen in Fig. 3. A minor EDS investigation is pursued to determine the formation of intermetallics lateral to the ball bond. In a cross section of a bond aged 150 h, Au_2Al, $AuAl$ and $AuAl_2$ phases were found between the IMCs under the bond and the remaining Al pad adjacent to the bond.

In Fig 4, a different microstructural evolution is observed in which the Au_5Al_2 IMC eventually dominates and only a thin strip of Au_4Al is present next to the Au ball after 1000 h HTS at 175ºC [2]. In this case the Au_4Al acts as a barrier preventing Au from diffusing into the Au_5Al_2. Another potential microstructural evolution is proposed that involves the oxidation of the Au_4Al [3]. Optimized Au bonds on Al pads are aged at 175ºC for 2000h. By 50 h, IMCs under the bond
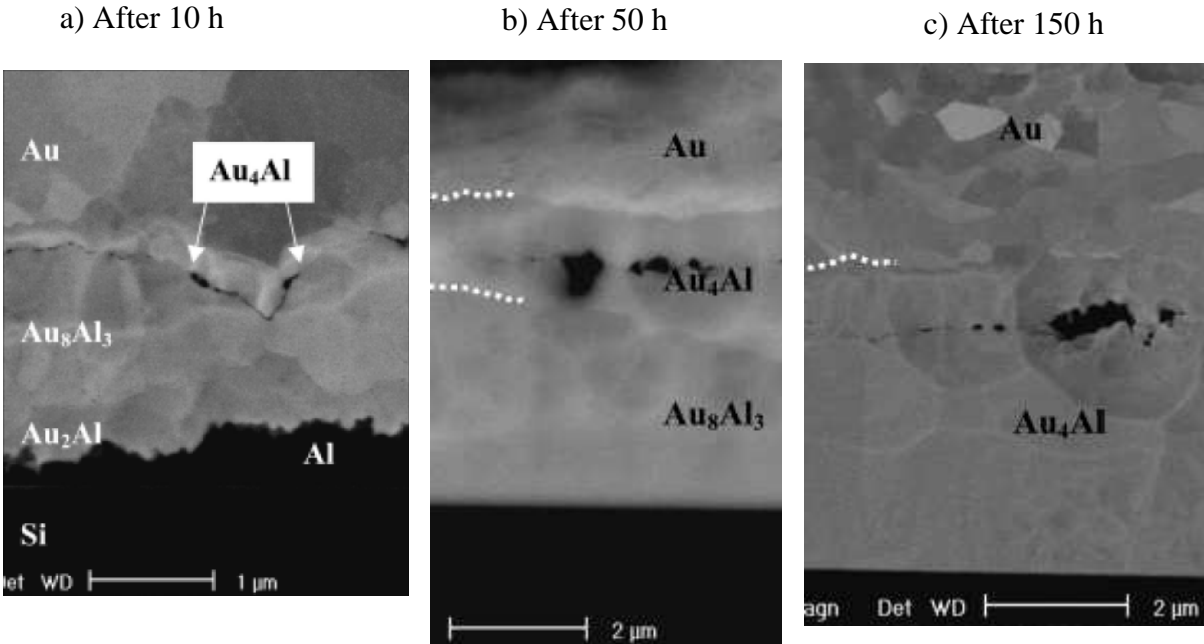
Fig. 3   Microstructure evolution as reported in [13]. (a) After 10h aging at 175 ºC, IMCs have formed at the bond interface. Au_4Al is nearest the ball, Au_8Al_3 comprises the majority of the IMC layer, and Au_2Al forms nearest the pad. (b) After 50 h aging, the entire pad is converted to IMCs. The majority of the IMC layer is Au_8Al_3, and Au_4Al is present near the bond. (c) After 150 h of HTS, the IMC layer has entirely converted to Au_4Al.
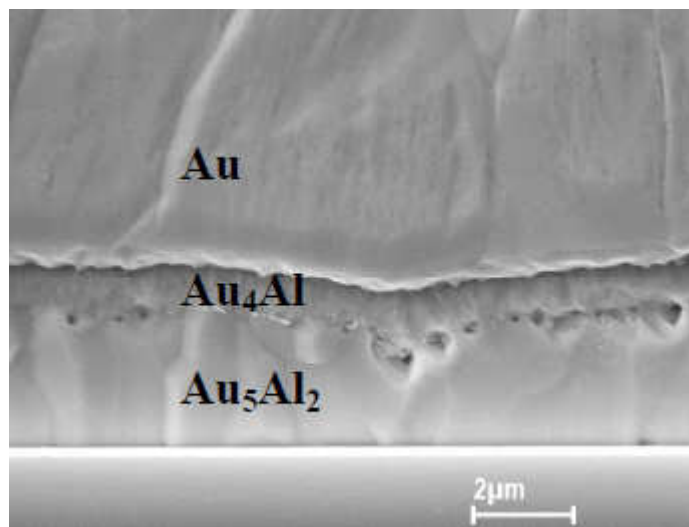
Fig. 4   Microstructure dominated by Au_5Al_2 with only a thin layer of Au_4Al present [2]. Note that the IMC referred to here as Au_5Al_2 is often reported as Au_8Al_3.

consist mainly of Au_8Al_3 with Au_4Al bordering the ball and by 1000 h, Au_8Al_3 has transformed

into a second separate lower layer of Au_4Al. Between 1000 and 2000 h, the majority of the Au_4Al

oxidizes. Oxygen absorbs onto surface of the peripheral Au_2Al and diffuses along the Au-Au_2Al

interface until it reaches the Au_4Al at the bond interface [3]. The original Au_4Al layer next to the

ball forms an oxide layer that is well adhered to the ball. The bottom layer of Au_4Al transforms

into a 2-phase composite with a dark oxide matrix and Au precipitates as shown in Fig. 5. During

pull tests, failure occurs at the crack which forms between the top and bottom oxide layers. Sritha-

ran et al. [14] confirm that the oxidation rate constant, k_p (which defines the increase of oxide

mass per surface area per second [14]), is more than 2.5 times higher for Au_4Al than for any other

IMC or for the base Al, so oxidation should occur more readily in this layer. The proposed oxida-

tion reaction is:

$$4Au_4Al + 3O_2 \rightarrow 2Al_2O_3 + 16Au \tag{1}$$

It is estimated that this reaction will cause a 7% volume expansion [3] which generates stresses

potentially resulting in cracks.
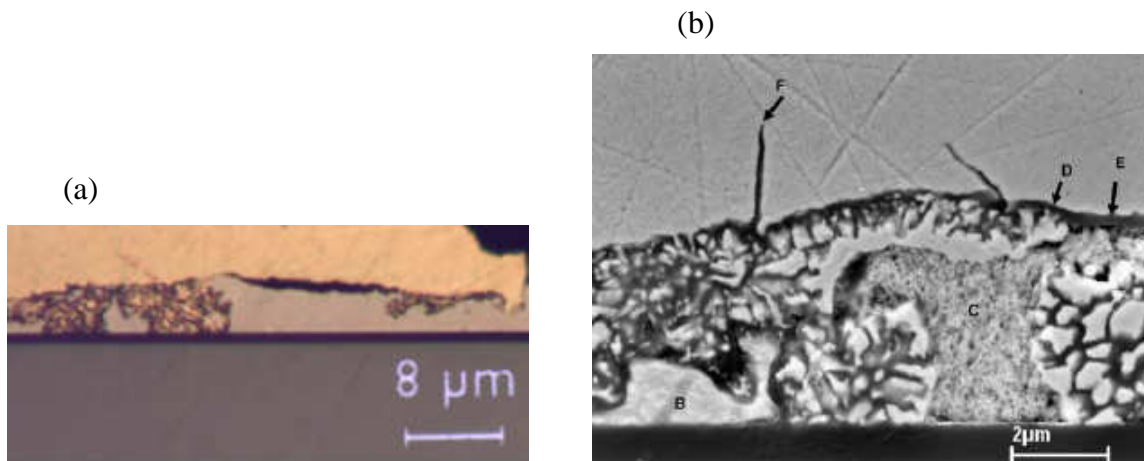
Fig. 5   Oxidized Au_4Al layer [3]. (a) Optical image. (b) SEM image. Light Au precipitates in dark Al_2O_3 matrix

Controversy exists as to whether Au_8Al_3 and Au_5Al_2 reported in [15] and [1] respectively are the same phase, and if so as to which stoichiometry is correct. For simplicity, in this thesis all phases with an Au:Al ratio of 70:30 to 74:26 will be referred to as Au_8Al_3 in accordance with the phase diagram reported by Okamoto [15] shown in Fig. 6.

Multilayer pads designed for increased reliability also include Ti which becomes introduced into the IMC microstructure. During HTS in [16], a 3 layer pad is used which consists of a top Al bonding layer, an intermediate Ti diffusion barrier, and a lower Al conduction layer. The Ti layer prevents diffusion of Al from the lower Al layer to the IMCs which form at the upper layer, and prevents electromigration. During aging at 450 ºC, the Ti layer is broken, and assimilated into the microstructure as a Ti rich diffusion layer. Breaking of the Ti layer has no effect on bond contact resistance.
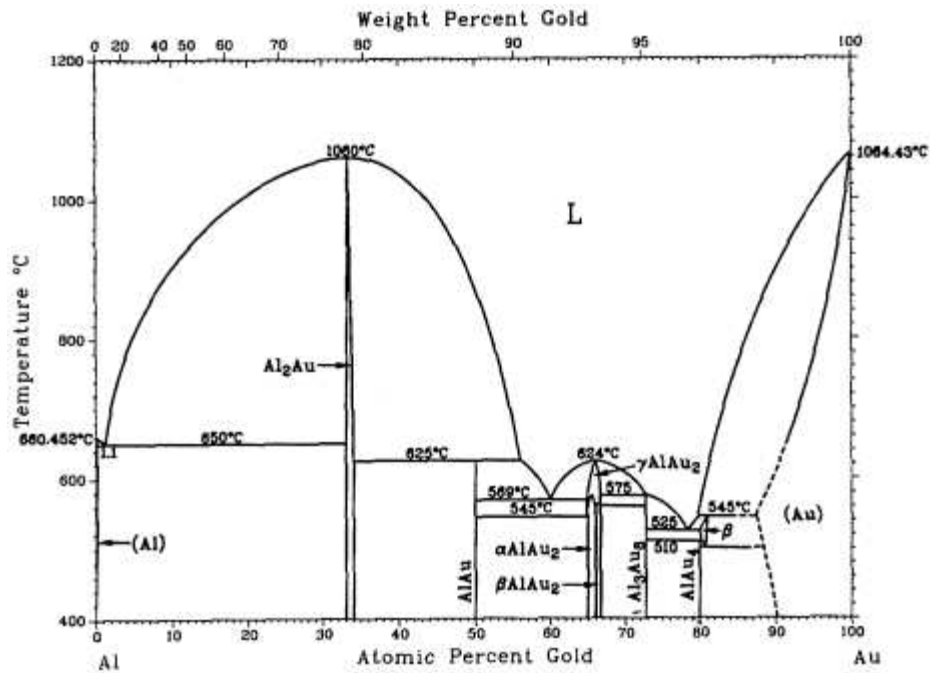
Fig. 6   Au-Al binary phase diagram [15]

2.2.2. Voiding and Cracking

In [13], Noolu observes a row of discontinuous voids between the 4N Au and the small discontinuous regions of intermetallics which form between the Au ball and Al pad metal in unaged bonds. After 150 h aging at 175 ºC, crack propagation due to coalescence of voids starts at the edge of the bonds. As the bond ages further, these cracks propagate towards the center. While it is proposed that the cracking is due to Kirkendall porosity [1, 5, 13], Noolu reports that cavities are formed due to stresses arising from volume changes as different IMCs form. Coalescence of cavities along the void line causes the bond to separate from the chip.

In [2], Breach notices that voids begin to form within 5 µm of the outer edge of the bond within 20 h of aging. After 200 h, the intermetallic layer has grown up in 2 humps at the same location. The Au metal hooks around the outside of the IMC humps, and cracks form around the humps progressing towards the center of the bond pad as shown in Fig.7. Although the cracks are not discussed in detail, it appears that they grow between the IMC layers as opposed to between the Au
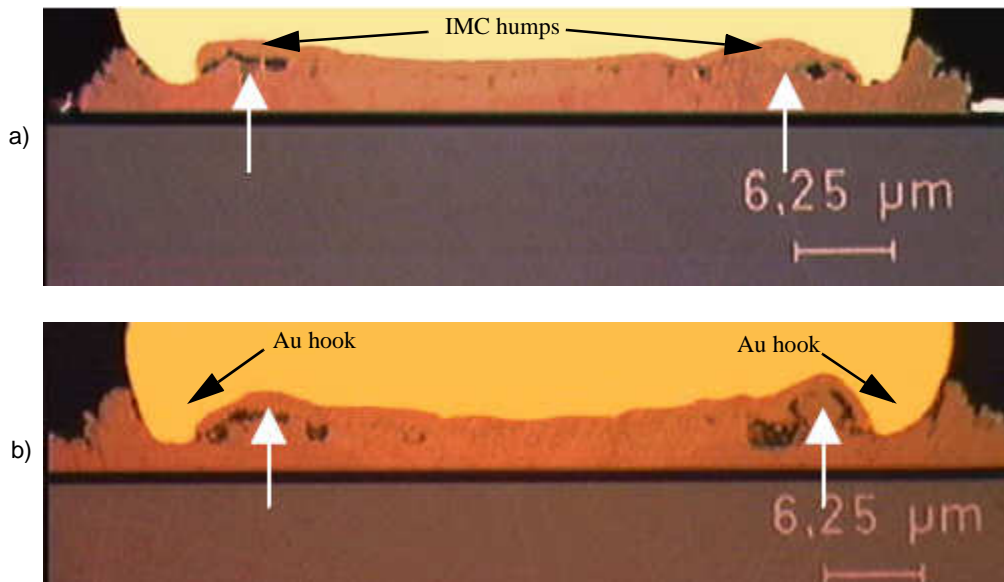
Fig. 7   Crack growth around Au "hook" [2]. (a) Sample after ageing at 175ºC for 500 h. (b) Sample after ageing at 175ºC for 1000 h. Cracking appears to happen between 2 different IMC layers.

and IMC layers as reported by Noolu. Breach proposes that 2 forms of Au_4Al are present: a fine columnar grained cubic alpha phase next to the Au ball, and a thick coarse grained version of the α-Au_4Al phase next to the Au_5Al_2 which forms later. Void formation at the interface between these two layers is credited to either the Kirkendall effect due to Au being transported to the lower Au_4Al layer [2] or by oxidation of the Au_4Al layers [3].

The Au hooking effect shown in Fig. 7 b is explained by Karpel [17] as a lack of bonding at the periphery of the deformed ball. When the bond force is applied, the majority of the force is transferred to the material under the capillary. The peripheral Au is subjected to the ultrasonic energy with a lack of bond force, resulting in minimal bonding and IMC formation in this area. When IMCs that formed under the bond grow upwards, the un-alloyed Au forms a hook with an incipient crack between the ball and substrate which allows oxygen to reach the interfacial IMCs.

2.2.3. Shear Strength During Aging

When a gold wire is thermosonically bonded to a pad, bonding between Au and Al occurs at discrete islands on the bond interface [1, 2]. Therefore, in bonds that have not been sufficiently aged, the weakest point is the bond interface, and during shear testing the bonds lift off, failing in shear mode 1. As the bond ages, the Al pad is consumed as interdiffusion takes place and IMCs form. The interface is now more bonded, and the IMCs provide much higher strengths than either of the base metals [1]. As a result, it is expected that after aging, sheared bonds fail by shear mode 2a: shearing through Au. Upon further aging, IMCs grow up into the Au ball, sometimes in spikes [1]. The samples made for this thesis experiment are bonded at the low temperature of 150°C, to prevent ageing while on the bonder. As a result, it can be expected that the initial bond quality would not be as high as bonds made at over 170°C, and this spiked growth of intermetallics occurs. If the intermetallics grow up to the same height as the shearing ram, much greater shear

force is required to break the bond and the apparent shear strength is very high [1]. As the aging process progresses, voids appear along the intermetallic layer. As these voids coalesce, forming cracks, the interface becomes much weaker. The shear strength drops, and the bonds now fail at the intermetallic layer defined as shear mode 2b. An evolution of expected shear modes over time can be seen in Fig. 8.

In [18], shear and pull strengths of bonds aged at 175° over 1000 h are measured. Shear strength increases up to 200 h and then decreases. As can be seen in Fig. 9, shear strength doubles from as-bonded strength to its peak strength. This is due to the formation of chemically strong bonds by IMCs at the interface. Breach attributes the following decrease in shear strength to chemical degradation of the Au_4Al layer which lies directly below the Au.

longer aging times

(a)   (b)   (c)   (d)

Areas where welding has occurred

Due to interdiffusion and intermetallic formation, a solid bond is formed at the interface.

Spikes of hard intermetallics at shear surface

Porosity plus brittle intermetallics at shear surface.

Direction of ultrasound during bonding
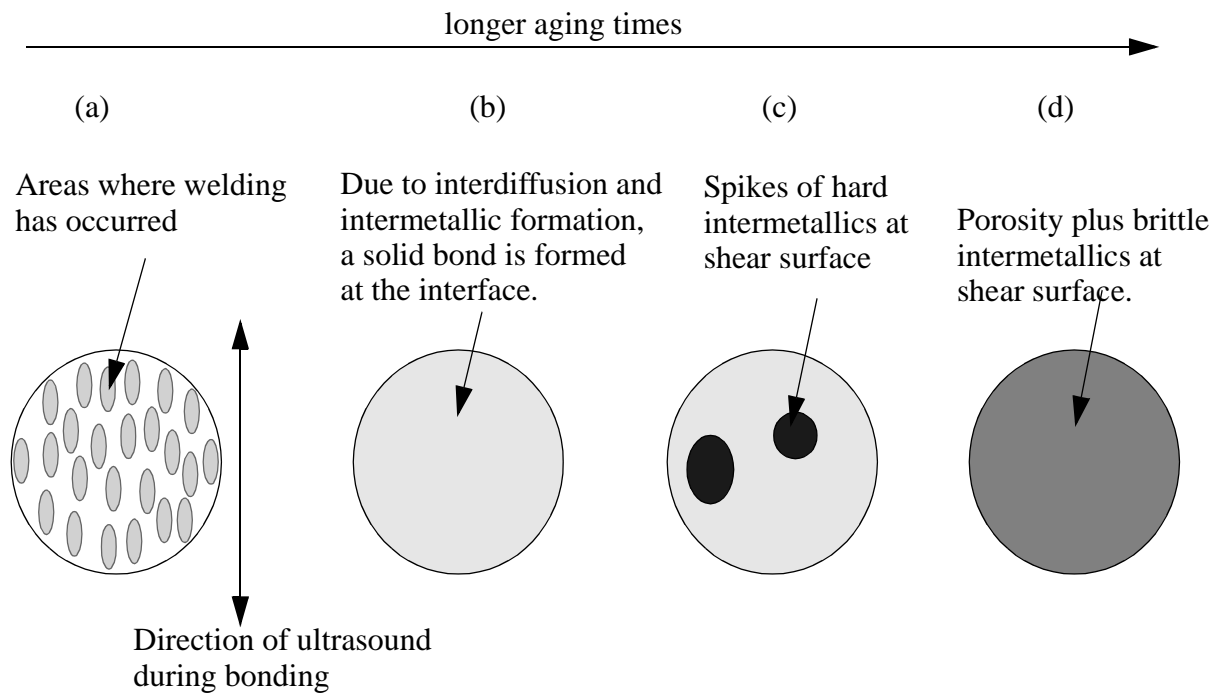
Fig. 8 Interdiffusion and growth of intermetallics at shear interface. (a) Due to poor ball adhesion, ball fails by shear mode 1. (b, c) Ball shears through Au material and fails by shear mode 2a. (d) Shear interface at IMC/oxidation layer reveals shear mode 2b.

2.2.4. Contact Resistance

Although the physical strength of the bond is the most common measure of bond quality, the contact resistance of the bond describes the electrical connection making it an important property. Resistance is measured by passing a current through the bond, measuring the voltage drop, and performing an Ohm's law calculation. Since the contact resistance is very low (~2-3 mΩ [4]) accurate measurement requires the 4-wire method shown in Fig. 10 a, where 2 electrical connec-
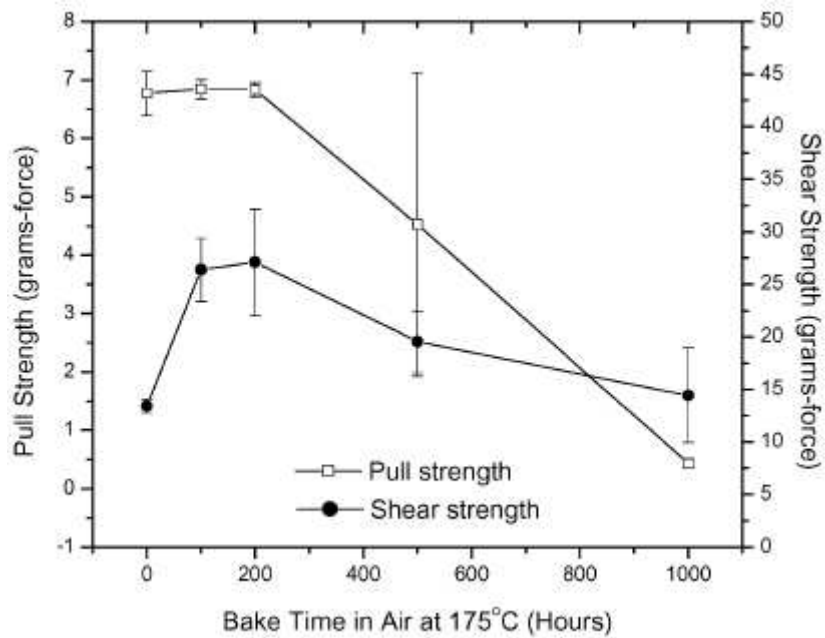
Fig. 9 Shear Test results from [18]. Bonds have diameter of 40 μm. At their peak, the shear stress corresponds to approximately 200 MPa, which is much higher than the shear strength of Au.
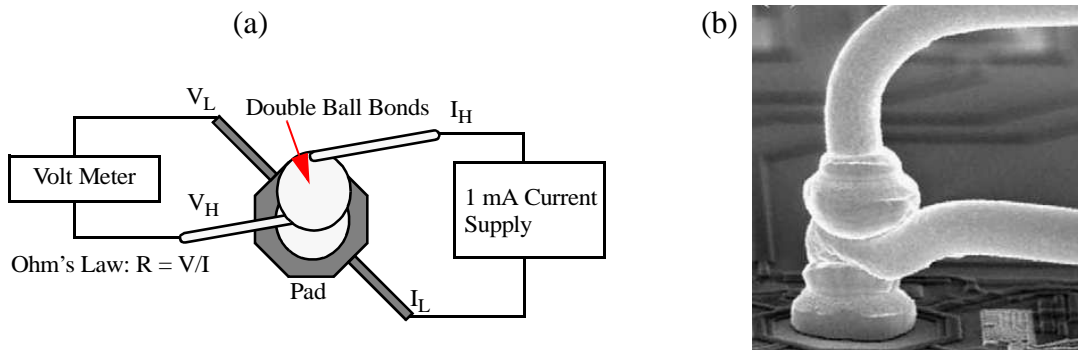
Fig. 10 Four wire connection. (a) Schematic. (b) Double ball bond used for 4-wire measurement [18]

tions are provided to the ball, and 2 connections are provided to the pad. One pair of connections passes a constant current through the bond, while the other pair of connections measures the voltage induced across the bond. Since negligible current passes through the wires measuring the voltage due to the high resistance of the volt meter, only the bond resistance is measured. Existing literature offers cases where the contact resistance is measured at discrete intervals using probes to obtain a 4-wire measurement [18]. A double ball bond can be used to measure contact resistance where a second Au ball is bonded directly on top of a test bond to provide for the V_H, I_H measurements, and a custom test chip is equipped with V_L, I_L measurements [4] as shown in Fig. 10 b. This method is capable of providing real-time contact resistance monitoring during HTS. In [1], it is observed that resistance increases for the first 10,000 hours of a 200 ºC age, afterwards plateauing at a the high value of between 1 and 10 Ω

In [19] it is observed that after excessive aging and before the bond pops off the substrate, the contact resistance will oscillate wildly. The contact between the ball and substrate is reduced to tiny contact areas which connect and disconnect via local electromigration to cause this phenomenon. Electrical failure is often defined as a certain percentage increase of resistance and occurs well before such phenomena are observed [19].

While resistance increase is often blamed on voiding and cracking of the interface resulting in a reduced contact area [1, 2, 19], it has also been attributed to IMC formation [1]. Resistivities of the IMCs are significantly higher than of the base metals, so as the IMC volume increases, so does the contact resistance. Resistance increases of 8 mΩ in the absence of cracks or Kirkendall voids are attributed solely to IMC formation [1].

Electrical failure can occur in one of two ways. Internal voiding either between the Au and the IMC layer, or within the IMC layer can cause the bond contact area to reduce until both mechani-

cal and electrical failure. Alternatively, as IMCs grow lateral to the bond, the surrounding pad Al may deplete due to the Kirkendall effect [1]. This may eventually lead to electrical isolation of the bond, although the bond may remain physically robust as shown in Fig. 11 b.

2.2.5. Integrated Stress Sensors

Integrated stress sensors are introduced in [4, 20, 21]. The sensors are piezoresistive strain gauges made of n+ diffused Si arranged in a Wheatstone bridge configuration around the test pad shown in Fig. 12 a. The configuration is supplied with a voltage of 3V, and outputs a differential voltage which will increase upon experiencing a tensile force caused by the radial shrinking of the bond interface, and decrease when a compressive force (interfacial swelling) is observed as shown in Fig. 12 b.The sensor signal, S, is given by the differential voltage from either side of the bridge:

$$S = (V_2 - V_1)/V_S \tag{2}$$

where V_S is the sensing voltage of 3V. When Kirchoff's circuit laws are applied to the circuit, S can be expressed in terms of the resistance of each element by:
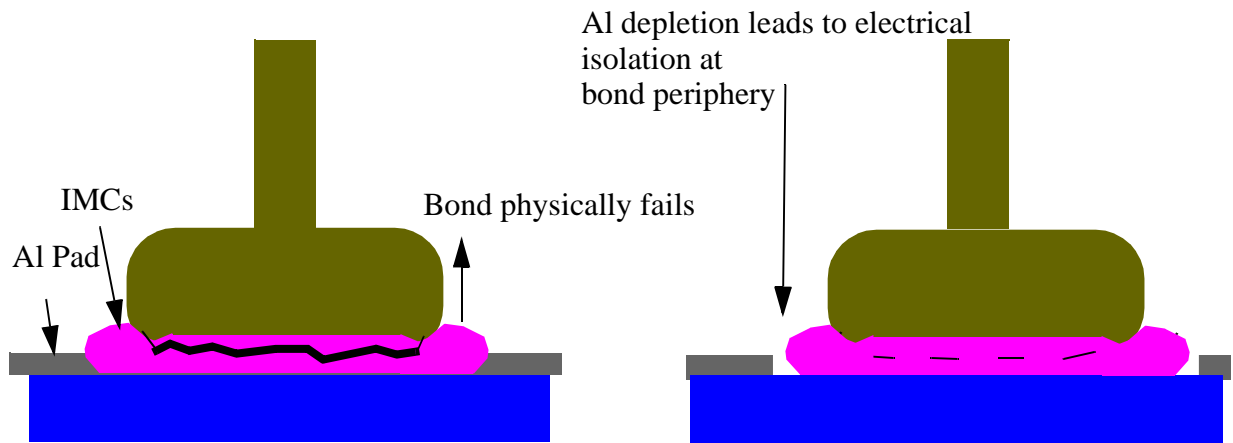
Fig. 11   Contact resistance increases until either (a) the bond fails, or (b) the bond becomes electrically isolated. In case (b) there is no physical failure between the bond and underlying pad. Rather, the pad Al adjacent to the IMCs becomes depleted due to the Kirkendall effect.

$$S = \frac{R_1 \cdot R_4 - R_2 \cdot R_3}{(R_1 + R_3) \cdot (R_2 + R_4)}$$
(3)

By using a Wheatstone bridge configuration, the sensor signal obtained is an average difference of resistance experienced between piezoresistors oriented to experience stresses tangentially (R_1, R_4) and radially (R_2, R_3). Since all resistors experience the same resistance change from an overall temperature change, no overall signal change is caused.

Fig. 13 shows the expected formation sequence of IMCs during aging, with relative IMC volume changes compared to base metal volumes [1]. During aging, sensor signals are measured which have been observed to roughly correspond to the volumetric changes resulting from expected IMC evolution [4].

2.3. Summary

In published studies of Au-Al wire bonds, interfacial IMCs dominated by Au_8Al_3 and Au_4Al typically form at the interface while $AuAl_2$, Au_2Al, and $AuAl$ form lateral to the bond. During HTS
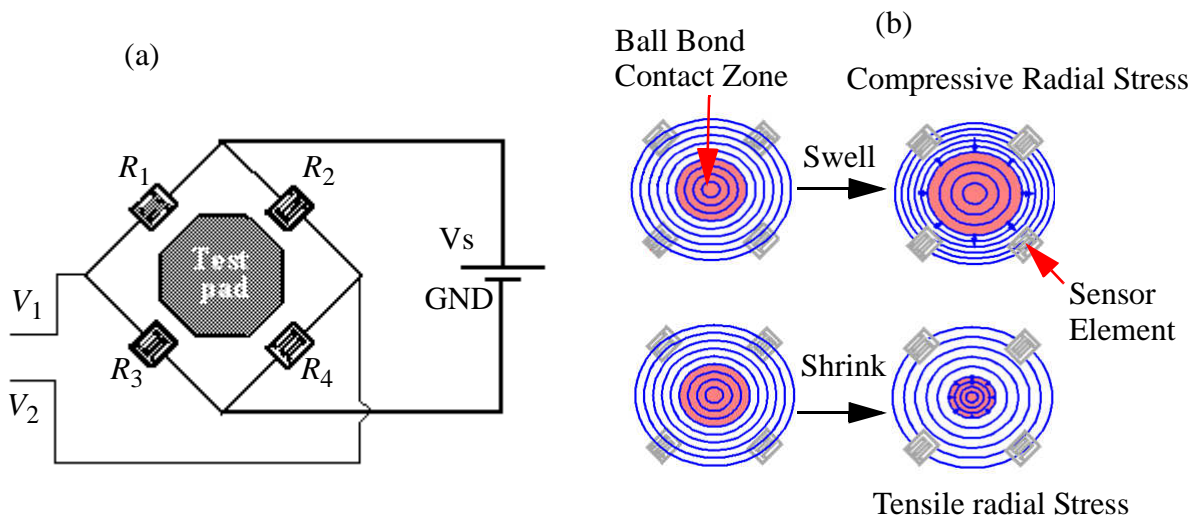
Fig. 12 Stress Sensors. a) A source voltage, Vs, of 3V is applied. The differential voltage between the sides of the Wheatstone bridge is detected [4]. b) When the interface region expands, compressive stresses are generated. When it contracts, tensile stresses result in the radial direction at the sensor element locations [22].

in an air atmosphere the Au_4Al layer is prone to oxidation which results in an Al_2O_3 matrix with Au precipitates. Voiding occurs at the Au-IMC interface, or at the Au_4Al-Au_4Al interface which may result from the Kirkendall effect or from oxidation. These voids coalesces into continuous cracks. This degradation will result in decreased bond strength as measured by the shear tester and increased contact resistance.
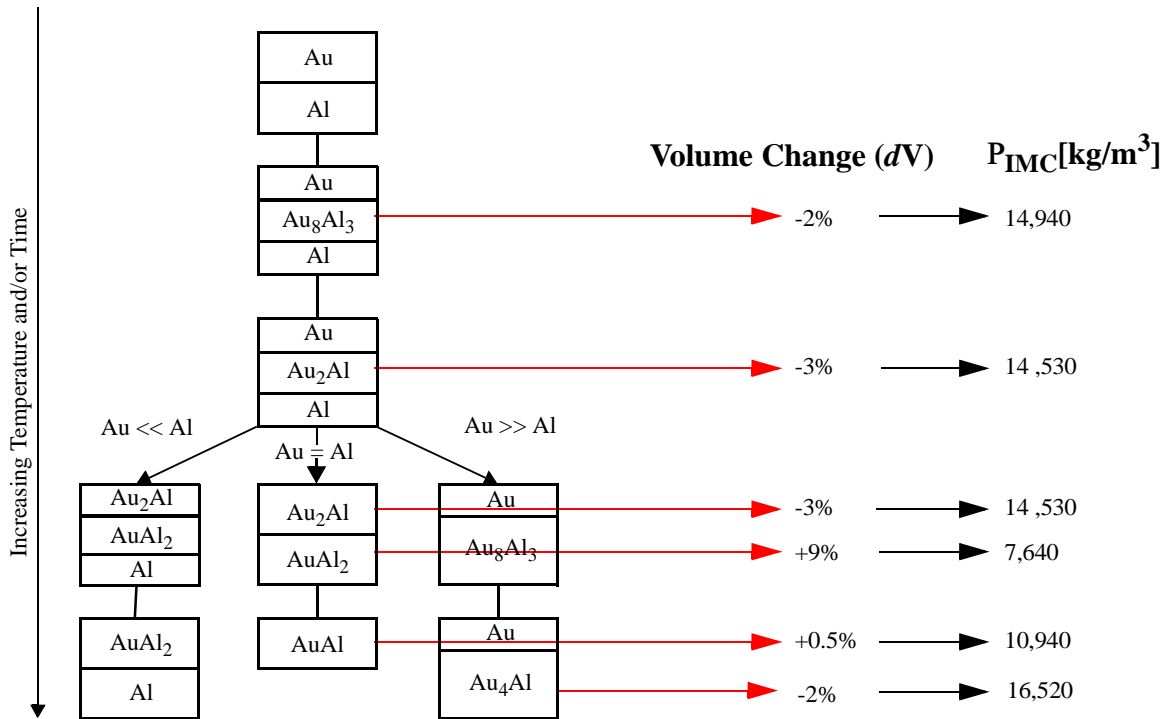
Fig. 13   Intermetallics which are expected to form during aging [1].

3. Experimental Methods

3.1. Overall Experimental Plan

The experiment investigates any relationship that may exist between conventional destructive

bond reliability tests and non-destructive methods of contact resistance (R_C) measurements and

stress sensor measurements (S). The experimental procedure is outlined in Fig. 14.
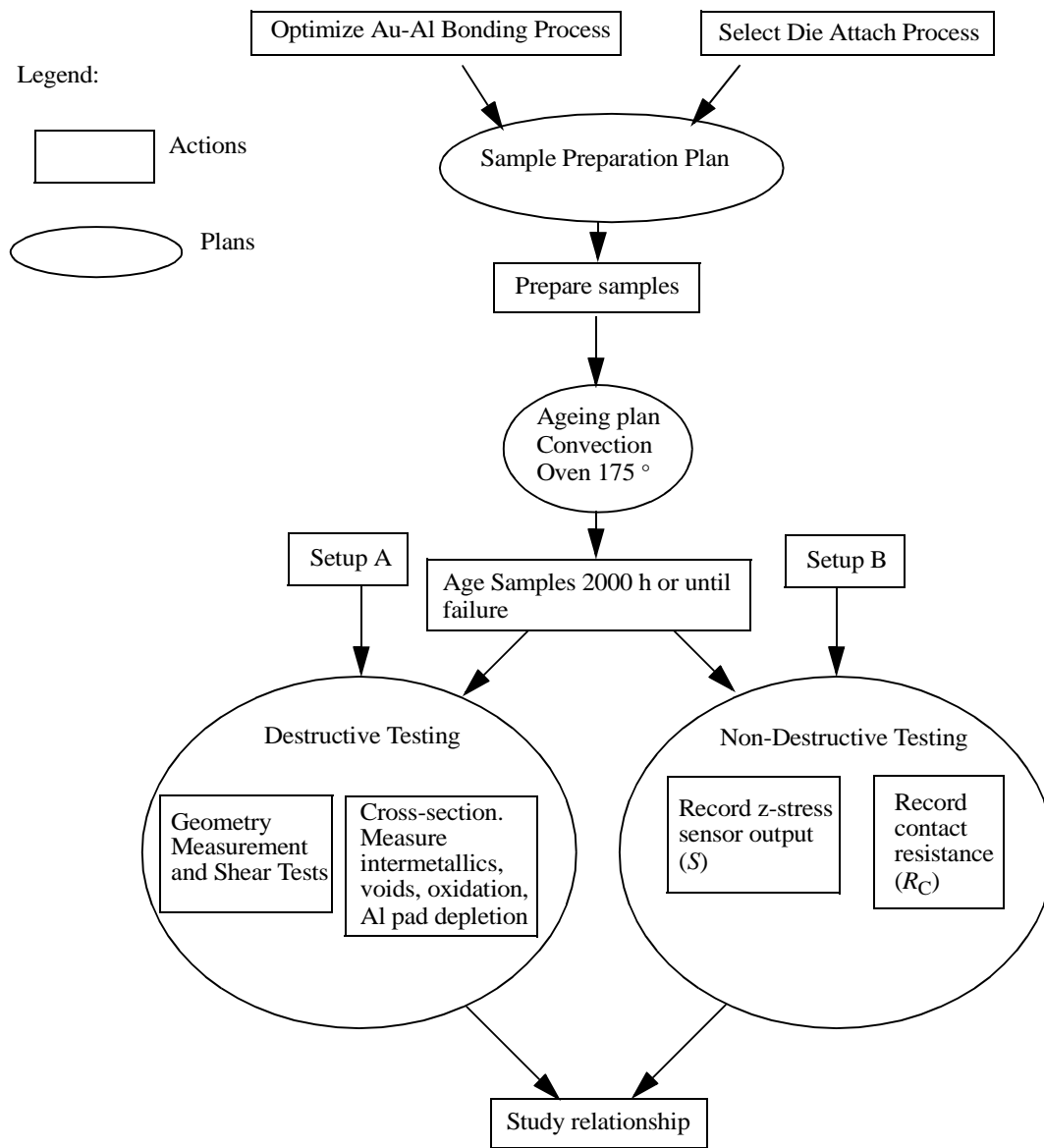
Fig. 14   Experimental procedure

Sample preparation involves selecting an appropriate die-attach process, optimizing the ball bonding process, and bonding the test chips. Setups are constructed for aging chips and monitoring data. Four sets of samples are aged for 2000 h in a pair of Omegalux LMF-3550 ovens (OMEGA Engineering Inc., Stamford, Conneticut) at 175 ºC. Set a contains a total of 380 bonds for shear testing, and set b contains 570 bonds for sectioning. These bonds are equally distributed among 19 chips which are destructively tested at periodic intervals listed in Table 1. Bond sets c and d consist of 61 bonds for R_C monitoring and 82 bonds for continual S monitoring, repectively. Upon aging completion, the results of the destructive analysis are compared to the results of the non-destructive tests to investigate the relationship between all four sets of results. The same test chip is used for all experiments, but is prepared and aged differently for each set of chips as is explained in Sections 3.2-3.7.

Table 1: Plan for Aging and Destructive Testing. The identity of each chip is listed, along with its time of ageing, t_a, the maximum number of shear tests per chip, MS, and the maximum number of cross sections per chip, MC.

Chip	t_a [h]	MS	MC		Chip	t_a [h]	MS	MC
1	0	20	30		11	300	20	30
2	0	20	30		12	300	20	30
3	1/2	20	30		13	600	20	30
4	1/2	20	30		14	600	20	30
5	1	20	30		15	900	20	30
6	1	20	30		16	900	20	30
7	10	20	30		17	1300	20	30
8	10	20	30		18	1300	20	30
9	100	20	30		19	2000	20	30
10	100	20	30		11	300	20	30

3.2. Die Attach

Before chips can be bonded they are die attached to CerDIP packages. A standard die attach

method uses silver filled epoxy (Ablebond 84, Ablestik, Rancho Doniniguez, California) to glue

the chip in place, which is then cured in an oven. For this thesis, a colloidal silver (Pelco 16034

Colloidal Silver, Ted Pella Inc., Redding, California) comprised of 60% ± 1% Ag is used instead

of the silver filled epoxy. The colloidal silver, which cures at room temperature over 24 h, is

reported as reliable at service temperatures of 200 ℃ [23]. It also offers the advantage of being

soluble by isopropanol, allowing for removal of the chip from relatively hard ceramic package for

subsequent cross sectioning. In a preliminary test, a chip die attached with colloidal silver is

removed from a package after 48 h exposure to isopropanol, whereas a chip die attached with sil-

ver filled epoxy is still firmly attached after 72 h of exposure to isopropanol.

After die attach, the chips are plasma cleaned to remove organic contaminants from bond pads

and reduce surface oxide. All samples are placed in a plasma cleaner (plasma cleaner located at

Microbonds, Markham, Canada) which is evacuated to < 90 mtorr, and a gas mixture of 90% Ag,

10% H is pumped into the cleaner until the pressure is increased back up to 270 mtorr. A radio fre-

quency (RF) generator operating at 380W creates the plasma inside the cleaner (Fig. 15) which is

maintained for 15 min. After plasma cleaning, the chips are immediately removed and vacuum

sealed in a container which is placed in nitrogen storage.

3.3. Preparation of Wire Bonding Samples

Prior to bonding the test chips, the bonding process is optimized for two reasons. First, it is desir-

able for the bond to be as strong as possible so that it endures aging for as long as possible. Sec-

ond, the quality of an optimized ball bond is expected to vary less between samples than the

quality of a non-optimized bond as illustrated in Fig. 16.

All bonding is performed on the ESEC 3088 wire bonder (ESEC, Cham, Switzerland). The capillary used is a SBNE-35BD-AZM-1/16-XL (Small Precision Tools, Petaluma, California), which is made for 1 mil wire, and has a chamfer diameter of 51 µm. The wire used is 1 mil 4N Au wire which has a breaking load of 10 gf, elongation of 2.8%, and a Vickers Hardness of 50. Wire bonding test chips used for process optimization are supplied by ESEC and attached to PLCC44 leadframes. The bonding pads for the ball bonds are made of standard bond pad Al (with Si and Cu dopants), and the metallization to which the wedge bonds are made to is Ag.
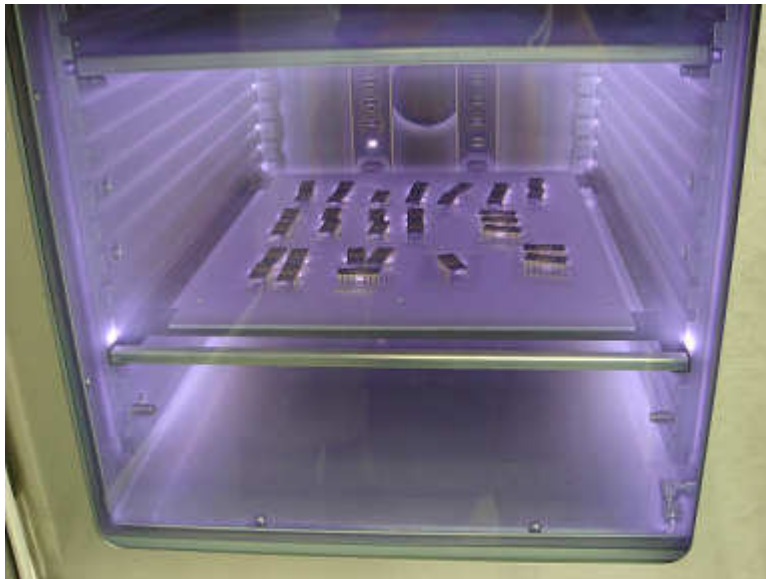
Fig. 15   Chips being plasma cleaned.
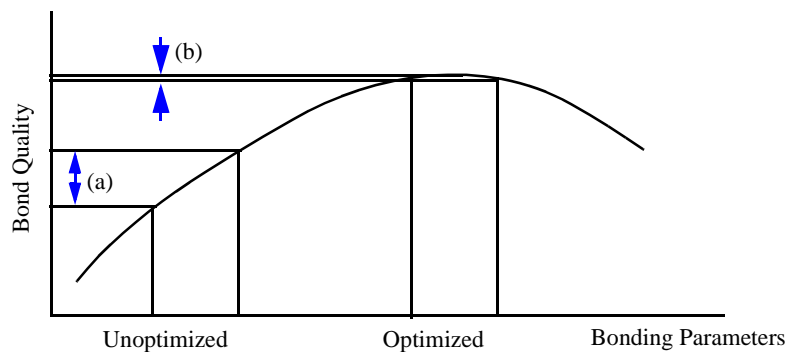
Fig. 16   Optimization results in less variance. Equal variations in bonding parameters will produce greater change in bond quality of (a) unoptimized bonds compared to (b) optimized bonds

A low bonding temperature is desired to minimize any ageing effects while in process. The bond temperature is 150 ºC with an offset temperature of 20ºC and a temperature deviation of 5ºC. Wire loop parameters are shown in Table 2.

The first step of the optimization procedure is to verify the quality of the tail bond. In order to be acceptable, the tail bond should always stick to the material and no fish-tailing (peeling) should be observed. Tail bonds are made with the wedge bond parameters shown in Table 3, and found to be acceptable. The tail bond parameters do not require an extensive optimization like the ball bond parameters because the tail bond is being made between Au wire and Ag metallization on the leadframe used for optimization, and will be made between gold wire and gold leads on the Cer-DIP package for the experiment. Bonds between Au pads and Au wire form easily and are not subject to problems encountered during HTS of dissimilar metals such as interdiffusion, oxidation and intermetallic formation. Since Au is soft and does not oxidize, there are relatively few prob-

Table 2: Wire Loop Parameters

Parameter	Value
Loop Mode 1	Advanced Eng
Arc Path	Standard
Loop Shape	Standard
Loop Height	350 µm

Table 3: Wedge Bond Parameters

Parameter	Value
Wedge Impact Force	700 mN
Wedge Bond Force	400 mN
Wedge Bond Time	25 ms
Wedge Ultrasonic Power	25%
Wedge Adjust Mode	disabled

lems encountered in Au-Au bonding, and a wide range of parameters will result in acceptable bonds.

The second step is the optimization of the ball bond geometry. In order to obtain good signals from the Z-stress sensors on the chip, the bond must be centered on the bond pad. Excess space is left between the outside of the bond and the border of the 70 µm pad to verify bond centering. The bond geometry is chosen as large as possible in order to maximize strength and reliability. These guidelines are met by a bonded ball size between 55 and 60 µm in diameter, leaving between 5 to 7 µm of space between the bond and the pad border to verify bond centering. Thus, the target diameter for the optimization process is 55 µm.

Standard engineering practice for the height to diameter ratio for the bond suggests values between 1:4 and 1:3. A target ratio of 1:3 is chosen for this optimization. The target height is therefore 16.5 µm. Such a ball height value will produce a sufficiently uniform stress distribution at the bond interface.

The bond height and bond diameter are optimized simultaneously by varying the FAB diameter and the impact force, while keeping the bond force constant at 250 mN. The FAB diameter is a function of EFO current, EFO time, electrode-to-wire distance (EWD), and wire tail length. To vary the size of the FAB, the current is varied while other predefined parameters are kept constant. The values of the predefined EFO parameters are listed in Table 4.

Table 4: EFO Parameters

Parameter	Value
Wire Tail Length	400 µm
Electrode to Wire Distance	350 µm
EFO Time	1.30 ms

A target geometry DOE is conducted where the impact force (IF) is varied as either 500 or 800 mN, and the EFO current is varied as either 22 or 24 mA. As can be seen from Table 5, this results in FAB diameters ranging from 47.2 to 55.7 µm. The free air ball diameters are measured in the x and y directions, and the average of these two measurements is taken as the FAB diameter (Fig. 17).

The ultrasonic level (US) is minimized to prevent deformation during bonding. A test bond for each set of parameters is first made at 20% US. Bonds are made at constantly decreasing US until some of the ball bonds no longer stick to the test pad which occurs at 12% US. At this point the US is increased by 1% to 13% US and the test bonds are made. Four to five test bonds are made for each combination of parameters, and the resulting bond height (BH) and ball diameter measured at the capillary imprint (BDC) are measured as is shown in Table 5. The BH is calculated from the different microscope focus required to focus on the bottom or top of the ball bond (Figs. 18 a and b). The BDC is measured twice in orthogonal directions and the average is taken (Fig. 18
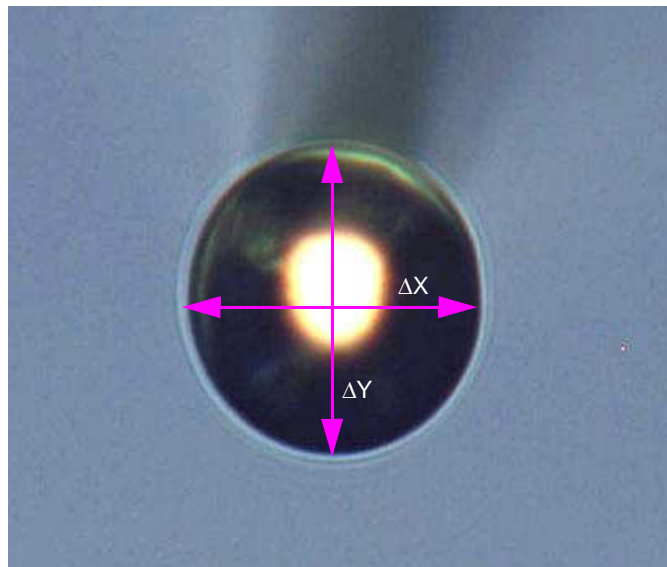
Fig. 17   FAB diameter measurements

b). All bonds are made on the same day with the same capillary, and no changes are made to the machine.

Average values for each set of parameters are taken, and contour plots are made where the *BDC* and *BH* are plotted against the input *IF* and I_{EFO} parameters. The contour plot in Fig. 19 a shows

Table 5: Geometry Results

Parameter	Sample No.	$I = 22$ mA		$I = 24$ mA	
		BH	*BDC*	*BH*	*BDC*
IF = 500 mN	1	13	53	19	53.8
	2	12	51.3	21	54.6
	3	7.5	52	19	55.2
	4	11	52.8	17	55.1
	5	10	53.2	18	54.5
	Average	**10.7**	**52.5**	**18.8**	**54.7**
IF = 800 mN	1	6	58.8	13	62.7
	2	8.5	58.8	11	61.1
	3	6.5	58.7	12	61.6
	4	6	56.6	13.5	63
	5	n/a	n/a	12	60.9
	Average	**6.8**	**58.2**	**12.3**	**61.9**

(a)   (b)
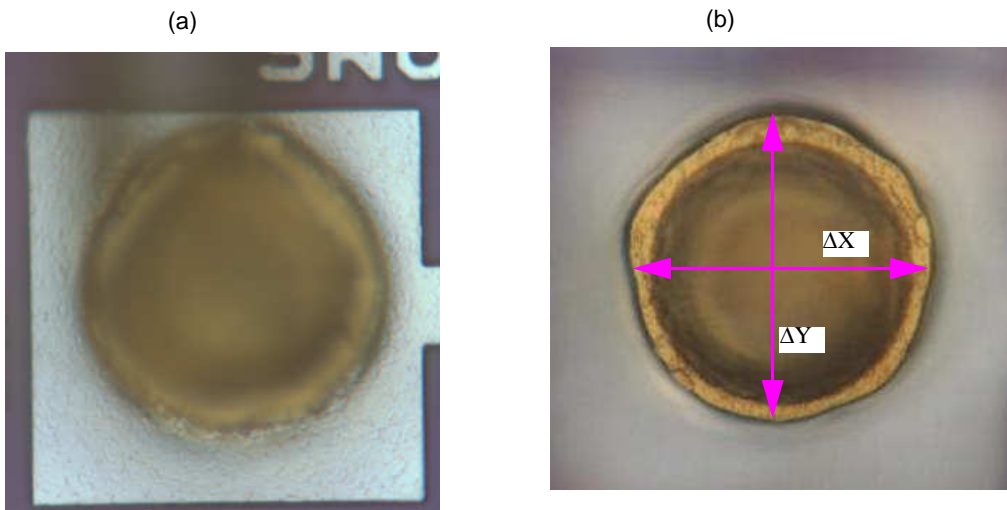
Fig. 18   Ball Bond Measurements. (a) Focus is on bond pad. (b) Focus is on *BDC*. Ball height is measured by the change in focus. *BDC* is calculated as an average of the *BDC* measurements in the x and y directions.

the line which represents the sets of parameters which resulting in the target *BDC*. The contour

plot in Fig. 19 b shows the line which represents the parameter sets resulting in the target *BH*. Fig-

ure 20 shows the intersection of the two lines, representing the individual parameter set which is

expected to result in both target *BH* and *BDC*.

The optimized parameters at the intersection according to this method are $I_{EFO} = 23.63$ mA and

$IF = 536$ mN. These parameters are now tested with minimal *US* parameter (13%). Ten test bonds

are made. The average *BDC* is calculated to be 54.9 µm, and the average *BH* is 16.8 µm. This is

within the acceptable range, and results in a ratio of *BDC* to *BH* of 3.25 which is also acceptable.

The free air ball diameter at the optimized I_{EFO} is 52 µm.

The third step is optimizing *US*. To do this, ten bonds were made on test chips at each of the fol-

lowing *US* values: 15%, 20%, 25%, 30%, 35%, represented as a fraction of the full ultrasonic

amplitude available. The *BH* and *BDC* for each bond are then measured and the bonds are shear

tested with a Dage 4000 shear tester (Nordson Dage, Buckinghamshire, UK) as shown in Fig.
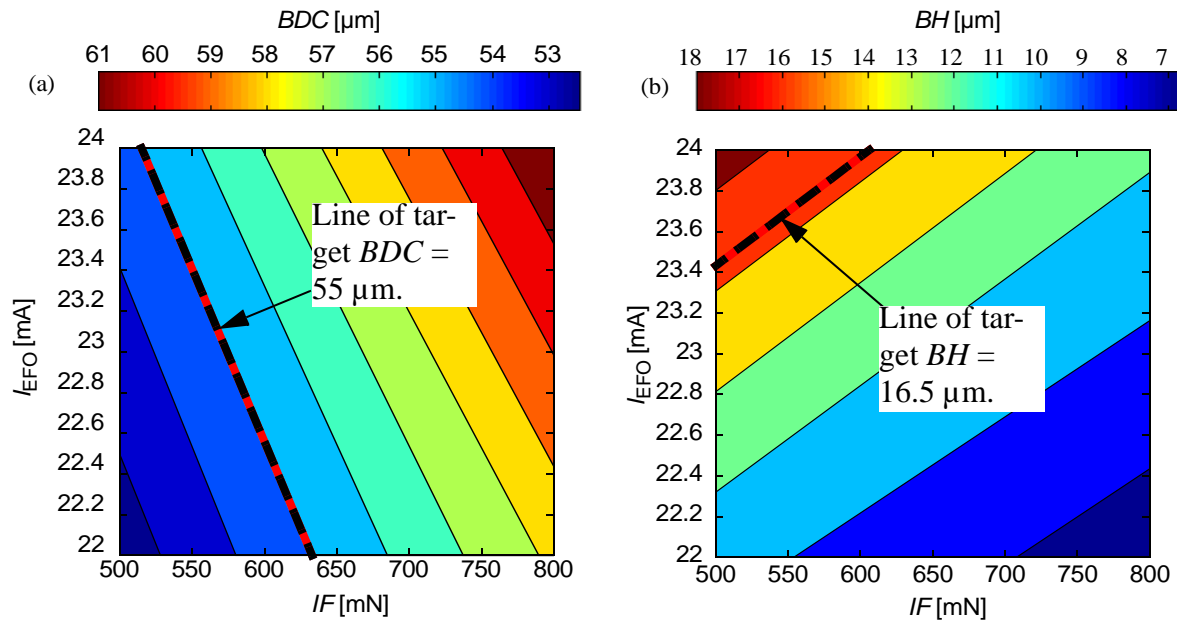
Fig. 19 (a) *BDC* plotted as a function of I_{EFO} and *IF*. (b) *BH* plotted as a function of I_{EFO} and *IF*

21 b. Shear tests are all performed in the direction of ultrasound, and towards the wedge bond (Fig. 21 a). Bonds made with different ultrasonic parameters are randomly alternated on each chip to reduce the effects of systematic variations between test chips if present. The *BH*, *BDC*, and shear force (*SF*) results are tabulated and plotted in Fig. 22 a - d.
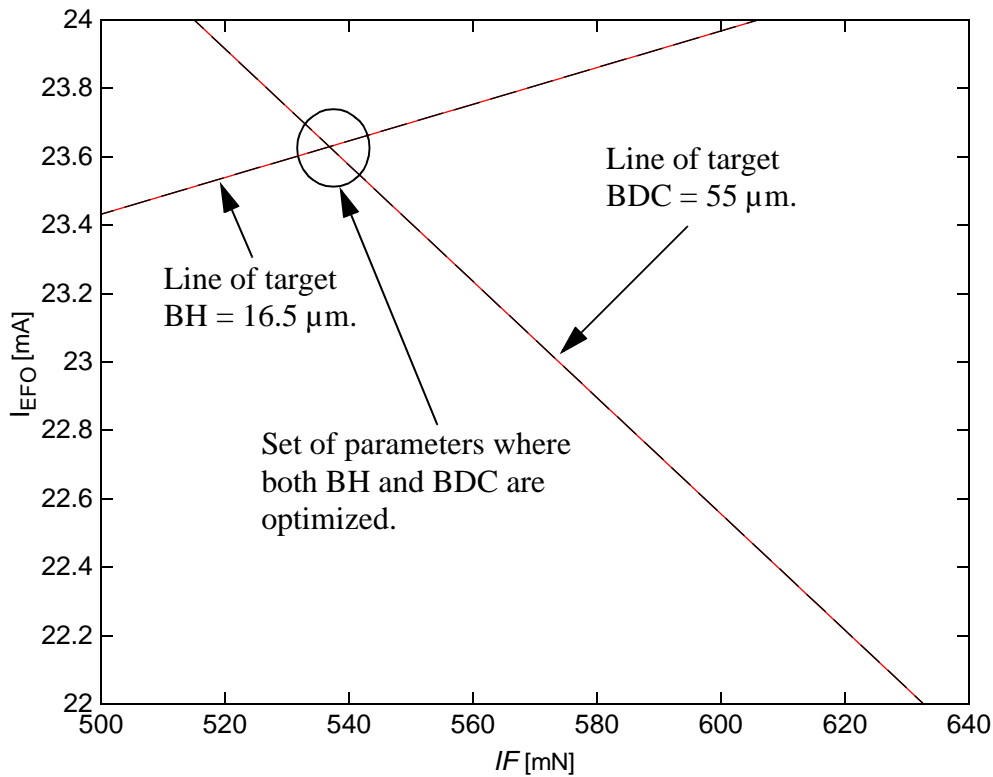
Fig. 20   Optimized parameters for bond geometry
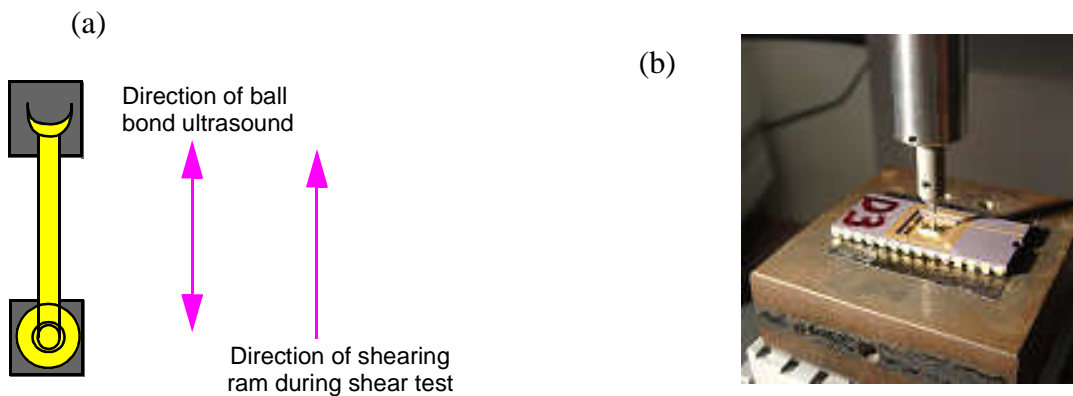
Fig. 21   (a) Direction of shear testing. (b) Bond on chip being sheared.

The shear strength, *SS*, is calculated by converting the shear force from grams force (gf) to Newtons, and dividing by an estimate of the cross-sectional area of the bond which is calculated from the BDC using:

$$SS = (SF \times 4 \times 9.81 \times 10^6) / (1000 \times \pi \times \mathrm{BDC}^2) \qquad (4)$$

The calculated *SS* is plotted against *SS* in Fig. 22 b. When observing this plot, the *SS* is expected to have its maximum between 20 and 25% *US*, so the average value of 23% *US* is taken as the optimized parameter. A total of 32 bonds are produced, measured, and sheared at 23% *US* for verification. These results are also shown in Fig. 22 b, confirming the expectation.

When *US* has been optimized at 23%, it is at a level where it results in slight ultrasonic deformation to the ball bond. As is shown in Fig. 22 a, the average *BDC* at low ultrasound levels is below 55 µm. Below about 20% ultrasound, the ultrasonic parameter is insufficient to deform the bond and deformation is caused by the normal impact force alone. When the ultrasound increases above 20%, the average *BDC* rapidly increases due to *ultrasound enhanced deformation* (UED). This onset of UED corresponds approximately with the peak in shear strength [21].

The process capability index, cpk [24], is verified in order to ensure that the bond process is acceptable and consistent. The cpk value is calculated using:

$$\mathrm{cpk} = (\mu - LSL) / 3\sigma \qquad (5)$$

where μ, *LSL*, and σ are the mean, lower specification limit, and standard deviation of *SS*, respectively. The *LSL* is defined to be 62.3 MPa according to the JEDEC standard 22-B116 [25]. The average *SS* is 130.53 MPa, and σ including outliers is 8.2 MPa. This results in a calculated cpk of 2.77. Since the cpk is greater than 2, the process qualifies as six sigma quality, ensuring that the selected bonding parameters will consistently produce ball bonds that meet the JEDEC standard.

3.4. Test Chip

A layout and photograph of the test chip [4, 20, 21] used for the study are shown in Figs. 23 a and b, respectively. The chip has two main regions. The first region consists of a set of 13 bond pads, each equipped with a set of piezoresistive stress sensors which are linked to a multiplexer. The multiplexer outputs the stress signal of any one pad in the form of a voltage differential between Vz_1 and Vz_2 which is used to calculate S by Equ. 2. The second region of the chip is a large bond pad which accommodates 4-wire contact resistance (R_C) measurements. Multiple bonds can be made on this pad. The test chip also contains additional bonding pads which cannot be used to
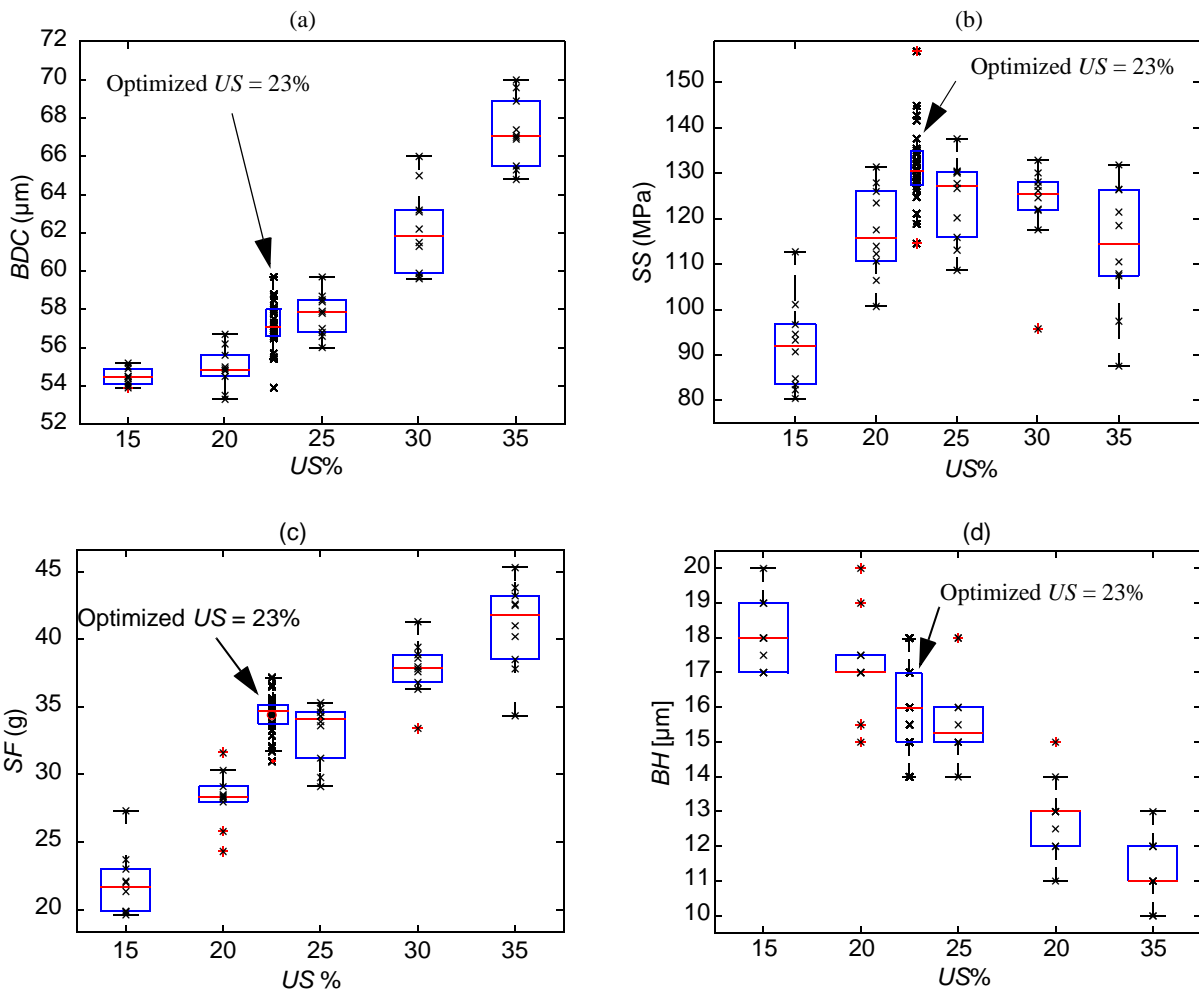
Fig. 22   (a) *BDC* for different *US*%. (b) *SS* plotted against *US* % (c) *SF* for different *US*% (d) *BH* for different *US*%.

record non-destructive data, but can be used to provide additional bond samples for destructive analysis.
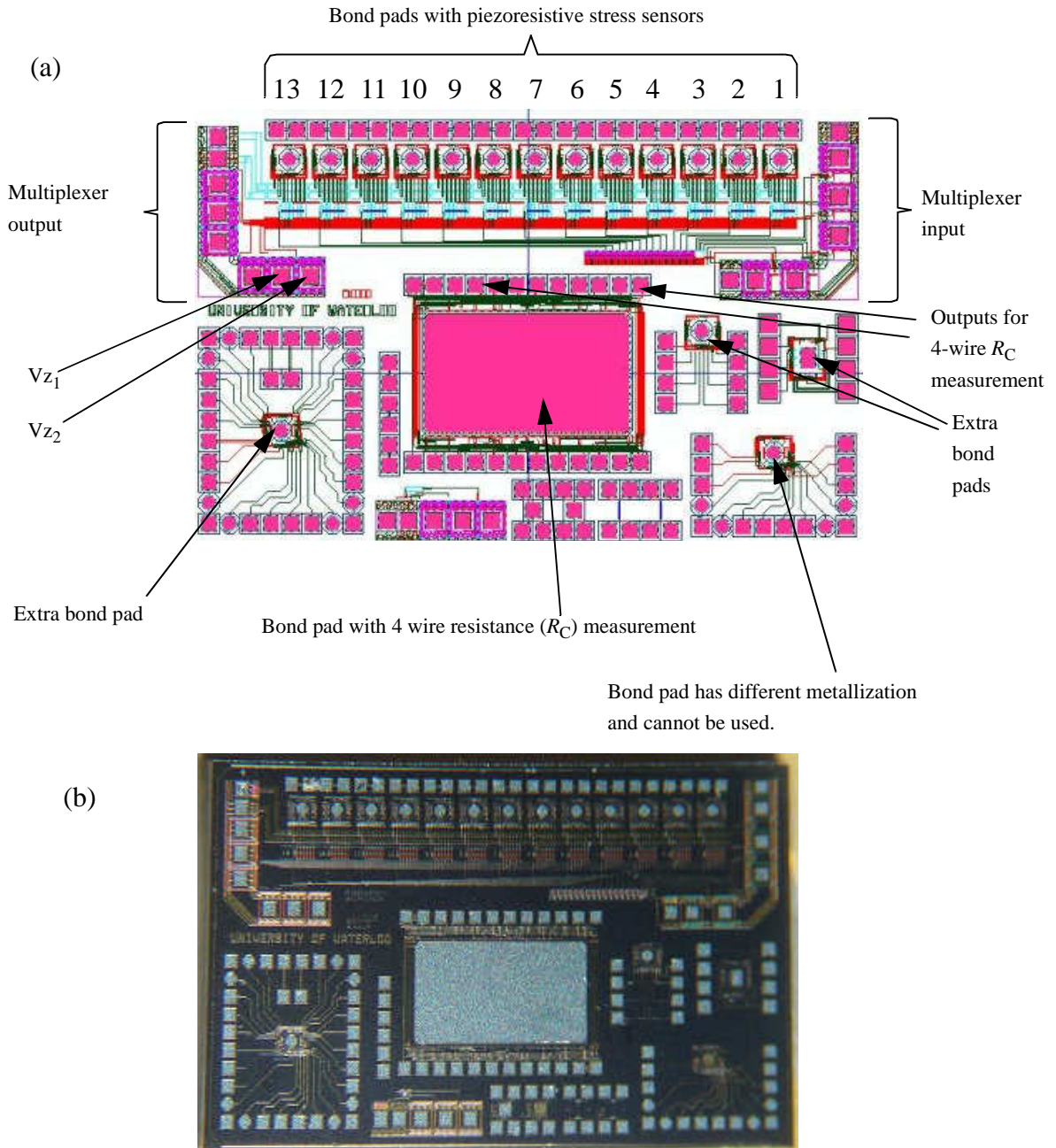
Fig. 23 Test chip [4, 20, 21]. (a) Layout (b) Micrograph

3.5. Destructive Tests

A total of 19 chips are aged for destructive analysis. Figure 24 shows the bonding diagram for the chips used and assigns a number to each wire bond. The bonds which are destructively tested are referred to with 2 subscripts: one denoting the chip and one denoting the bond. For example, $SS_{C4,B16}$ will refer to the shear strength of bond number 16 on chip number 4.
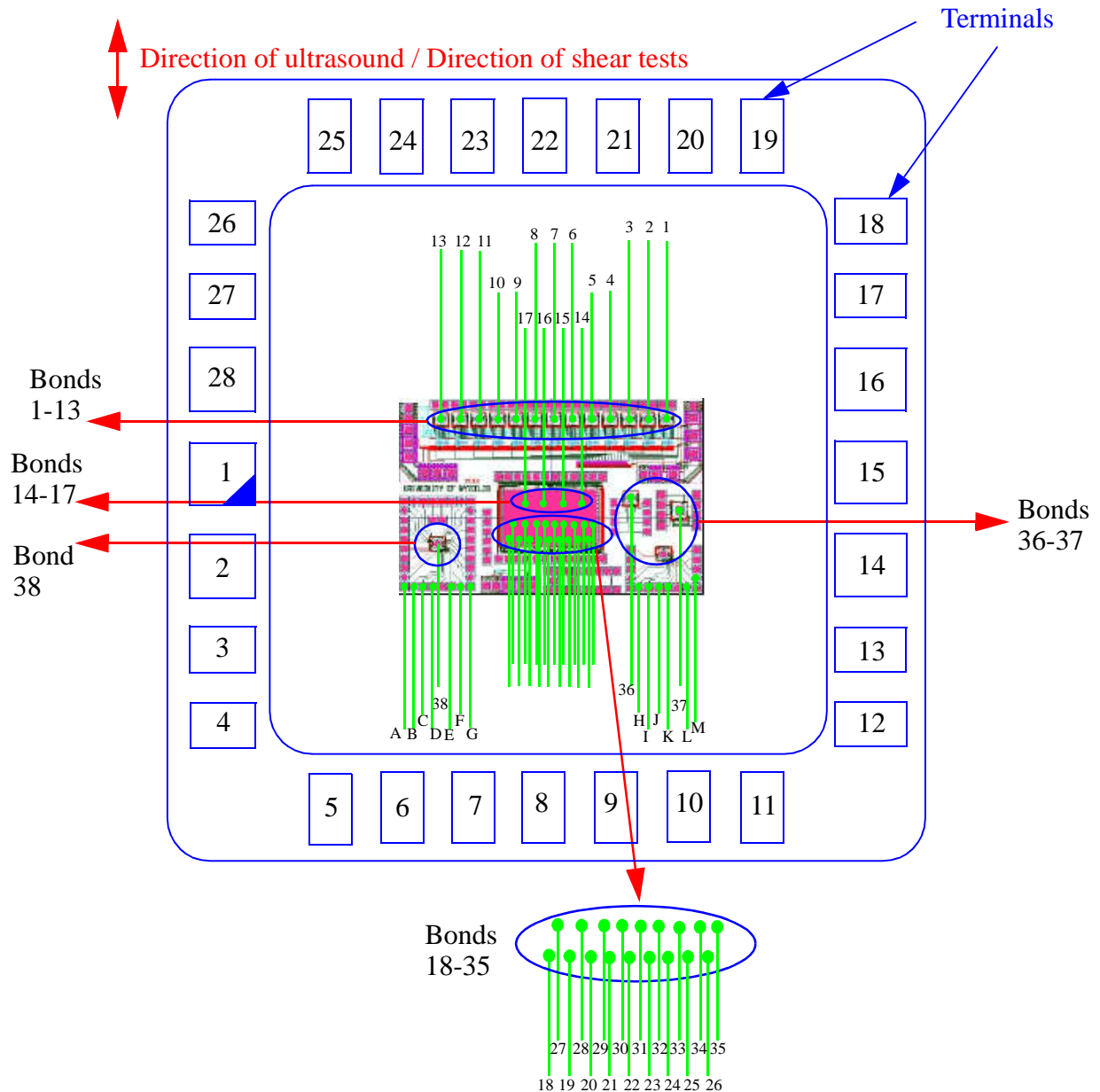
Fig. 24   Wiring Diagram for Destructive Analysis

3.6. High Temperature Storage for Accelerated Bond Aging

The chips are aged in the oven at 175 ºC, and extracted from the oven after 30 min, 1 h, 10 h, 100 h, 300 h, 600 h, 900 h, and 1300 h. One chip is extracted after 2000 h and a pair of chips are destructively tested without any aging to serve as a pair of baseline samples. The allocation of chips for the destructive testing plan is outlined in Table 1.

For each time interval, there is a potential maximum of 40 ball bond samples for shear testing and 60 samples for sectioning.

Bonds 1-17, and 36-38 as shown on Fig. 24 are used for shear tests. The shear tests are performed by the Dage 4000 shear tester at a height of 5µm in the same direction as the applied ultrasound during bonding and towards the wedge bond.

Bonds 18-35, and A-M are used for sectioning in order to characterize voids and intermetallic compounds (IMCs). Prior to sectioning, the exterior of unsheared bonds are examined with optical and scanning electron microscopy to observe lateral IMC growth and Al pad depletion. The surfaces of sheared bonds are examined to study the shear interface. A JEOL JSM 6460 tungsten filament scanning electron microscope (SEM) is used. The chip is removed from the package before grinding and polishing by breaking the wedge bonds and dissolving the colloidal silver with isopropanol as is shown in Fig 25. Reference chips are sectioned with the Al_2O_3 package to verify that package removal does not influence bond structure. The chip is mounted in a puck of slow curing epoxy and cross sectioned by grinding and polishing with 9, 3, and 1 µm diamonds with alcohol based lubricant and 0.25µm colloidal silica solution on silk pads until the center of each row of ball bonds is reached. More details about the polishing method are described in [26]. Cross sections are analyzed with both optical microscopy and SEM. Prior to SEM analysis, the samples are carbon coated. For cross section analysis, a LEO 1530 field emission SEM with

EDAX EDS detector is used, as this provides higher image resolution (as fine as 3µm) than the JEOL SEM.

3.7. Bonding Plan for Contact Resistance and Stress Sensor Signal Monitoring

A total of 9 chips are bonded for continuous non-destructive R_C and S measurement as shown in Fig. 26. Redundant bonds for V_L and I_L connections used in R_C measurement are made from the large Al pad to package leads 14 and 22 to ensure that in the event of bond failure, the chance of signal wires failing before test bonds is reduced.

Stress sensor bonds 1-10 as shown on Fig. 26 are made on sensor pads #3 to #12, respectively, also shown schematically in Fig. 27. A total of 3 pads are left unbonded. The stress signals measured on the unbonded pads serve as a set of baseline stress signals for comparison.

The sensors are connected to an on-chip bus via high temperature switches, and the bus is connected to bonding pads serving as outputs. A multiplexer is built into the chip and is controlled using a 4 digit binary code connected as 0 V and 4 V signals to pads 15 through 18, denoted D0 to D3, respectively, as shown in Fig. 26. The binary signals, as well as the sensing voltage and

(a)

1.4"
35.6 mm

(b)

(c)
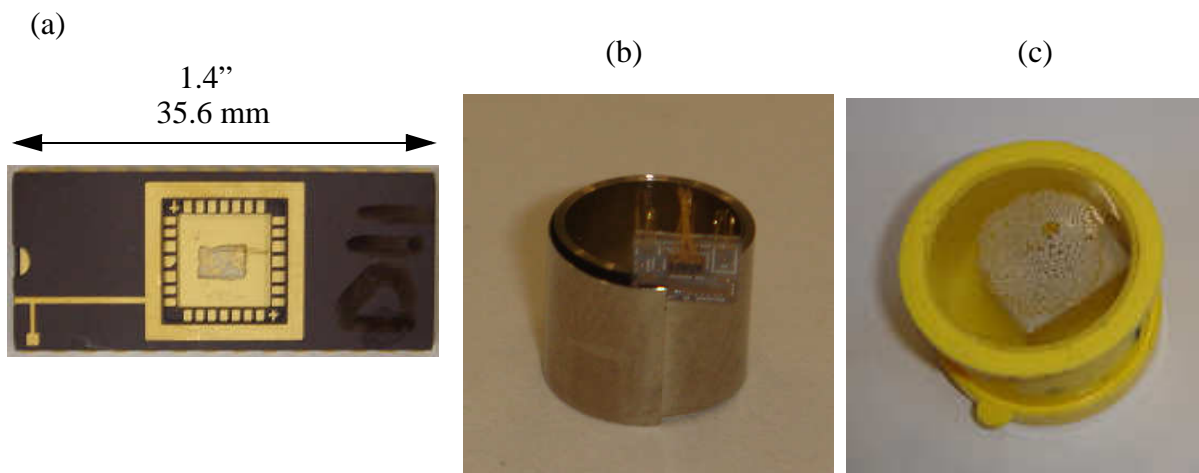
Fig. 25   Mounting of chip for sectioning. (a) Chip is removed from package. (b) Chip is inserted into metal clip to keep bonds perpendicular to grinding surface. (c) Chip is encapsulated in slow curing epoxy which experiences negligible volume change upon curing, minimizing effect on bond quality.

grounding are provided by a data acquisition board (DAQ) (Measurement Computing USB Temp-

AI Data Acquisition Board, Measurement Computing, Norton, Massachussets) which is con-
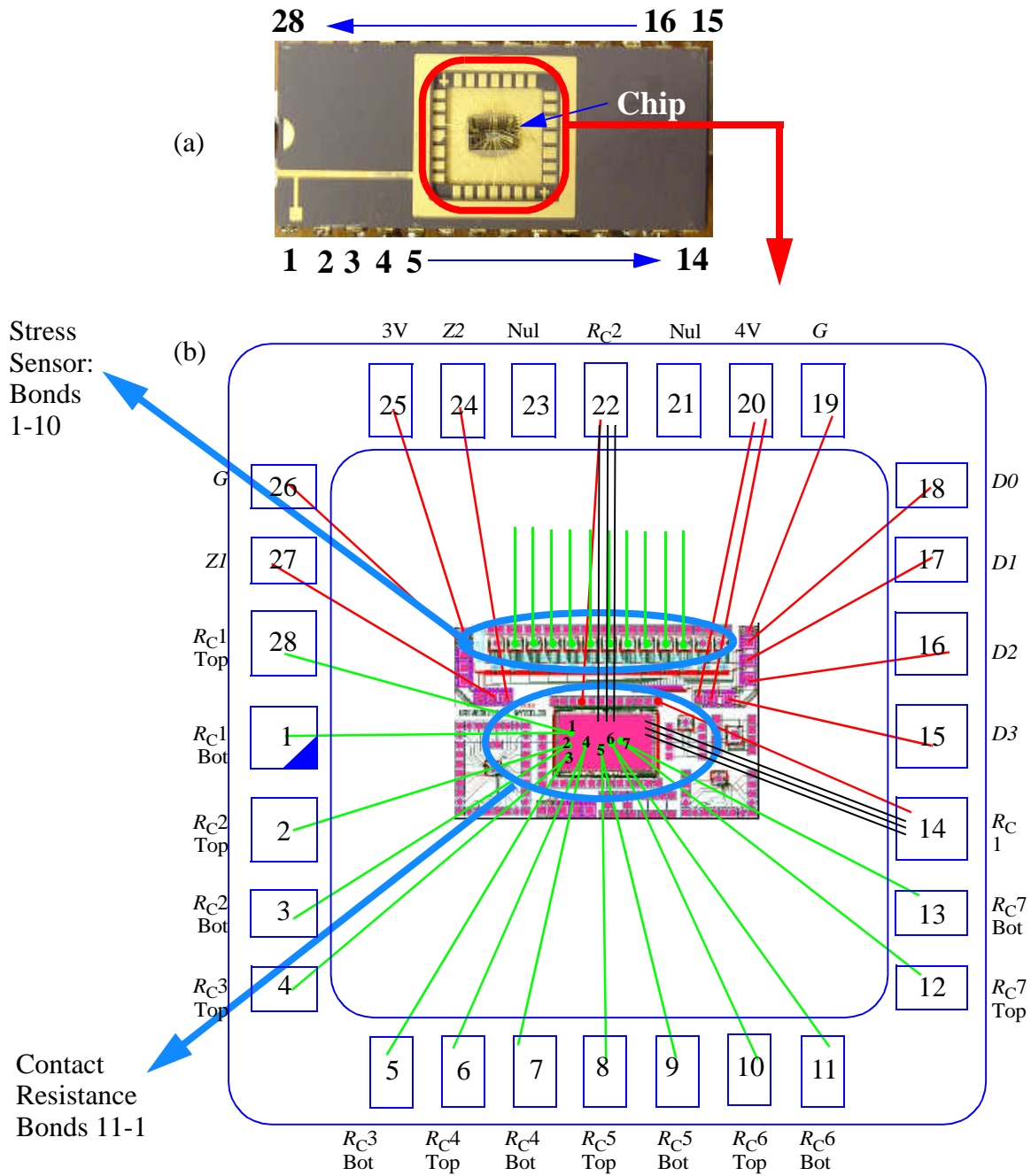
Fig. 26 Non-Destructive Bonded Chip. (a) Chip mounted on package, showing the 28 numbered package pins. (b) Detail of chip on package with bonds from chip to the 28 package leads.
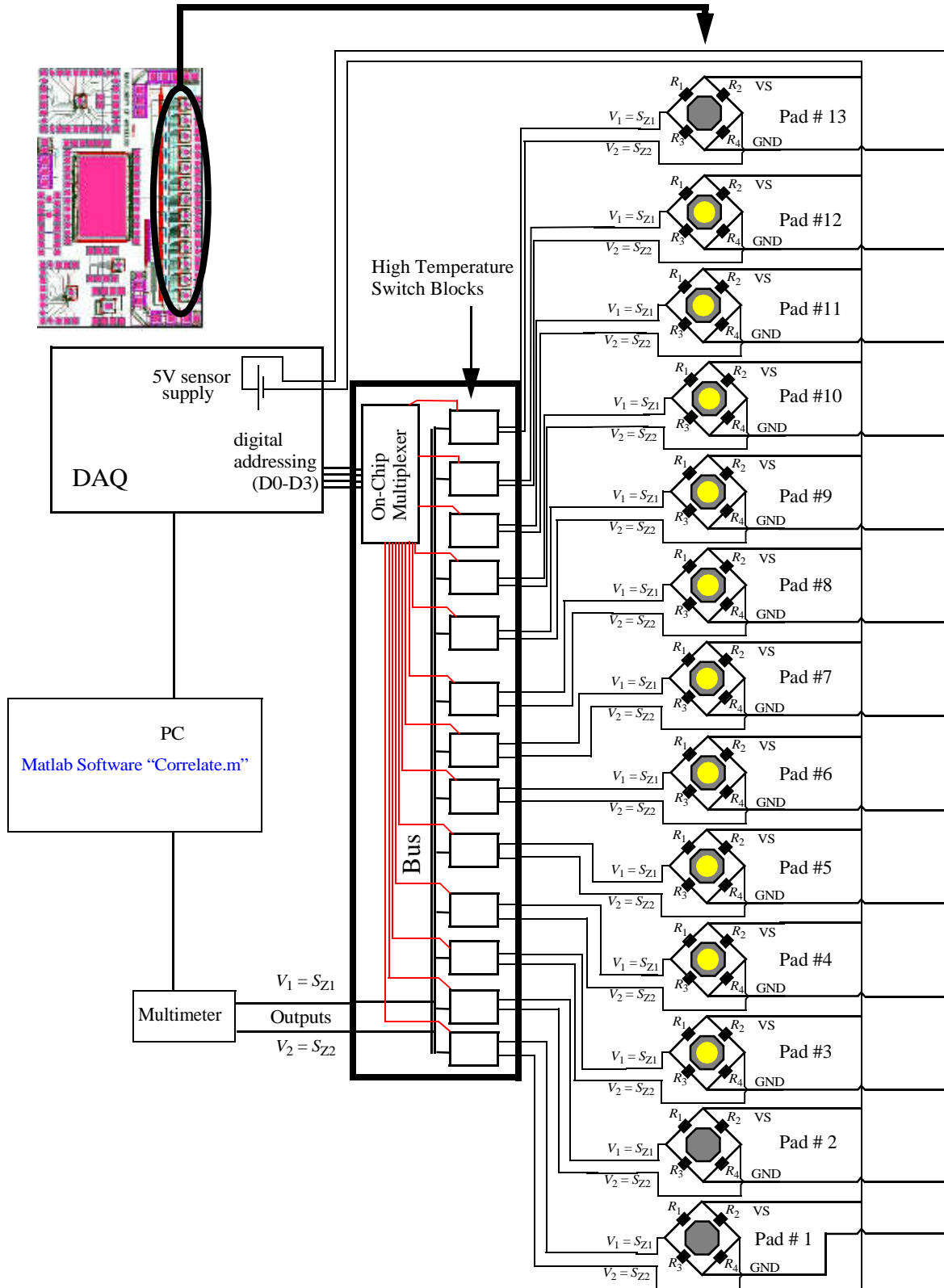
Fig. 27   Z Stress sensors arranged in Wheatstone bridge configuration around each bond pad in MUX'd array for one chip

trolled by the software. The multiplexer is responsible for operating the high temperature switches in a way that the signals of only one test bond are connected to the bus at a time.

R_C measurements are taken for bonds #1 to #7 on the large rectangular pad in the center of the chip as shown in Fig. 26. R_C is measured using the 4-wire method, which requires two electrical connections to the ball bond, and two connections to the pad. For each bond, two connections are provided through the gold wire of the double ball bond, and two connections are provided through the substrate pad which are common to all bonds (see package leads 14 and 22 in Fig. 26). A constant current of 1 mA is fed through the bond interface, while voltage across the substrate and ball bond is measured. R_C is obtained by applying Ohm's law to the known current and measured voltage. A Mainframe (Keithley 2700 Mainframe, Keithley Instruments, Cleveland, Ohio) with a multiplexer (MUX) [Model 7708 40 channel multiplexer, Keithley Instruments, Cleveland, Ohio] is used to select individual ball bonds for R_C measurement. A basic electrical schematic of the multiplexer selection with resistance measurement is shown in Fig. 28.

All bonds which have their contact resistance monitored will be referred to with 2 subscripts: one denoting the chip and one denoting the bond. For example, $RC_{C1,B6}$ will refer to the 6th double bond on chip 1. For bonds on the row of pads equipped with stress sensors, bonds are referred to with 2 subscripts: one denoting the chip, and one denoting the bond pad used as defined in Fig. 23. Therefore, $Vz_{C11,S3-12}$ refers to the stress signals from bonded pads on chip 11, while $Vz_{C11,S1-2}$, and $Vz_{C11,S13}$ refers to the pads which are left unbonded.

4. Experimental Setups for Accelerated Bond Aging

Two setups are used for the experiment. Setup A is used for bonds on chips where R_C and S are monitored. Setup B is used for bonds which are sheared and destructively tested. Setup A which is shown in Fig. 17 consists of an oven operating at 175 ºC, which houses the test chips as well as a Pt100 temperature sensor (Pt100 sensor, Heraeus, Germany). High temperature wires running under the oven door allow the chips to communicate with the monitoring equipment. All equipment interfaces with a computer which selects individual bonds for monitoring, and graphically displays signals from the bonds.

Setup B consists of a second oven operating at 175 ºC which contains the chips to be destructively tested and a Pt100 temperature sensor. These chips are aged in an oven separate from the non-destructive set of chips to avoid possible disturbances to the electrical equipment when the oven is periodically opened for chip removal.
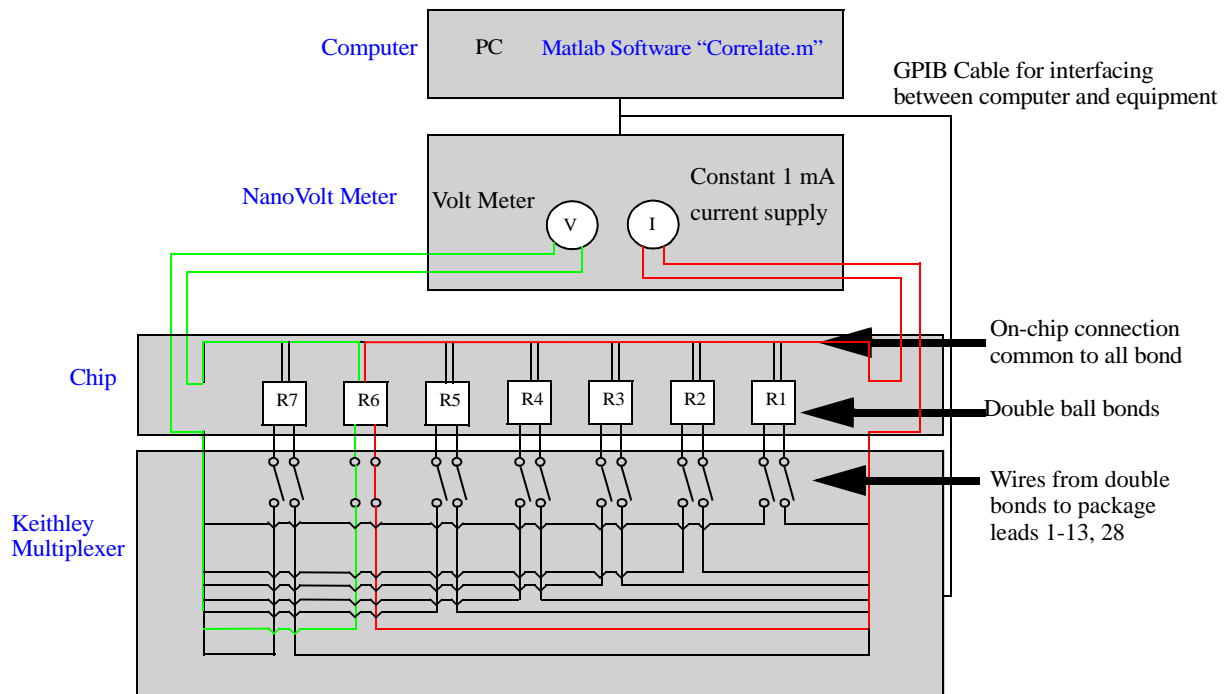
Fig. 28   Multiplexer Selection of Target Ball Bond for one chip. Configuration shown measures R6.

4.1. Setup A

The setup for the non-destructively monitored chips is shown in Fig. 29, and a schematic of the setup is shown in Fig. 30. Chips are stored in an oven. High temperature feedthrough cables described in a following section lead from the chips out of the oven to a switchbox. This switchbox relays instructions from controlling software to the chips via a DAQ. The switchbox transfers output signals from the chips to a set of MUXs described in Section 4.1.5 which select R_C and S signals from individual bond pads as directed by the software. These signals are forwarded to micro-ohm meters (for R_C) and a multimeter (for S) which measures their values. The software stores a record of all readings and displays them graphically in real time. Elements of the setup to be discussed in further detail are the: oven, high-temperature cabling, chip-holding rig, switch box, transistor board, DAQ, multiplexers / measuring equipment / power supplies, and computer software.

Fig. 29   Setup A

Oven

Chip 1 | Chip 2 | Chip 3 | Chip4 | Chip 5 | Chip 6 | Chip 7 | Chip 8 | Chip 9 | Room for 3 more chips

Available connections

Individual R_C connections
14 Wires per Chip:

Rc_{1top}, Rc_{1bot}
Rc_{2top}, Rc_{2bot}
Rc_{3top}, Rc_{3bot}
Rc_{4top}, Rc_{4bot}
Rc_{5top}, Rc_{5bot}
Rc_{6top}, Rc_{6bot}
Rc_{7top}, Rc_{7bot}

R_C

160 Wires:
80 sets of 2

Common connections
2 Wires per Chip

I_L, V_L

24 Wires:
12 sets of 2

Switch Box

Outputs from Chip: $Z1$, $Z2$

Inputs to chip:
G, V for sensors
$D0$, $D1$ 2, $D3$
G, V for on-chip MUX

Z_{stress}

24 Wires: 12 sets of
Voltage Signals

Top-Plexer | Bot-Plexer

Keithley Mainframe

$Rc_{top} = I_H$
$Rc_{bot} = V_H$

Top-Plexer | Bot-Plexer

Keithley Mainframe

I_L
V_L

I_L
V_L

Keithley Multiplexer

$Z1$
$Z2$

DAQ
for digital signals
and voltage supply
for sensors and chip
multiplexer

6 Wires: $D0$
$D1$
$D2$
$D3$
VS
G

Agilent 34401A 7 1/2
Digital NanoVolt /
Micro-ohm Meter

First 40 bonds

Agilent 34401A 7 1/2
Digital NanoVolt /
Micro-ohm Meter

Remaining Bonds

Agilent 34401A 6 1/2
Digital MultiMeter

COMPUTER
for device control
and data
recording

Fig. 30   Setup for non-destructive monitoring during aging

4.1.1. Oven

An identical oven is used for each setup. In each oven, a Pt100 sensor is located next to the test chips to accurately monitor the temperature. During aging, the temperature of the oven in setup A is 175.3 ± 0.49 ℃. The oven in setup B has an average temperature of 174.9 ± 0.14 ℃. The temperature difference between the two ovens is not expected to cause significant differences in bond aging. Figure 31 shows measured temperatures from each oven over a sample period of 1 week.

4.1.2. High Temperature Cabling

High temperature teflon insulated wires (Daburn Electronics & Cable Corp., Dover, New Jersey) are soldered directly on to the pins of the packages for optimal electrical connections using high-temperature solder. The solder used (Farnell Components Ltd., Leeds, UK) is composed of 5% Sn, 93.5% Pb, 1.5% Ag alloy with a melting temperature of 301 ℃. The wires are arranged in flat bands and are fed out of the oven between the oven door and the frame as shown in Figs. 32 a and b.
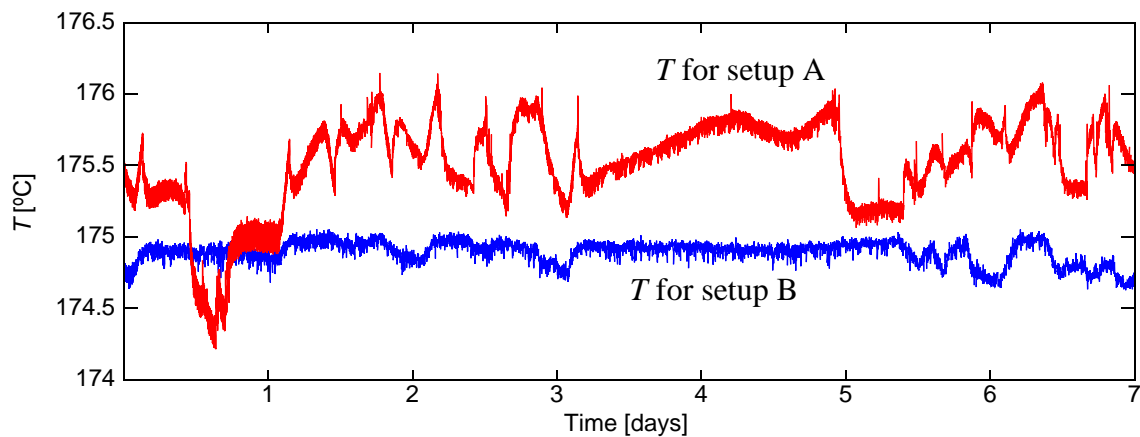
Fig. 31 Temperature measurements from setup A and setup B as measured by Pt100 sensors located in the ovens. Increased variation in setup A is due to small gap in oven door required for wire feed-through.

4.1.3. Rig to Hold Test Chips

An aluminum rig is designed and built to hold the non-destructively tested chips in place while providing space for all required cabling. A more detailed design description is available in [27]. Figs. 33a and b show a schematic and photograph of the rig, respectively. The packages are placed in the rig upside down with the chips containing the test bonds positioned between the sup-

(a)   (b)

Fig. 32   (a) Chips fastened to the rig and placed in oven. (b) Oven door closed over cabling.
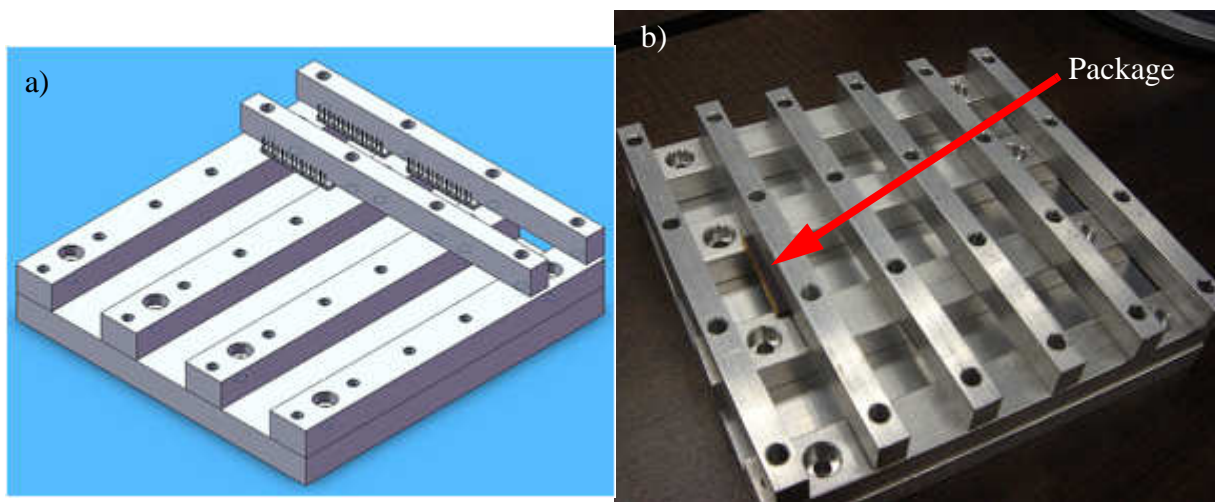
Fig. 33   Package holder for oven. (a) CAD design of holder. (b) Holder with package.

port bars exposed to air. Bars are screwed down to hold the packages in place. Fig. 32 depicts test

chips in the rig with high temperature cabling fed out of the oven.

4.1.4. Switch Box

A switch box shown in Fig. 34 a interfaces between the chips and the measurement devices. The

switchbox is equipped with 36-pin female connectors. The male connectors are attached to the

high temperature wires connected to the chips (Fig. 34 c), and to ribbons of low temperature wires

for all other equipment as shown in Fig. 34 b. The switchbox groups inputs and outputs, so that

R_C measurements from all chips may be accessed by the MUXs from one set of ports, all S mea-

surements from another port, and inputs to the on-chip MUX as well as common grounds and

sensing voltage (V_S) for all chips may be supplied via another individual port. A wiring diagram

for the switchbox is given in Appendix A.
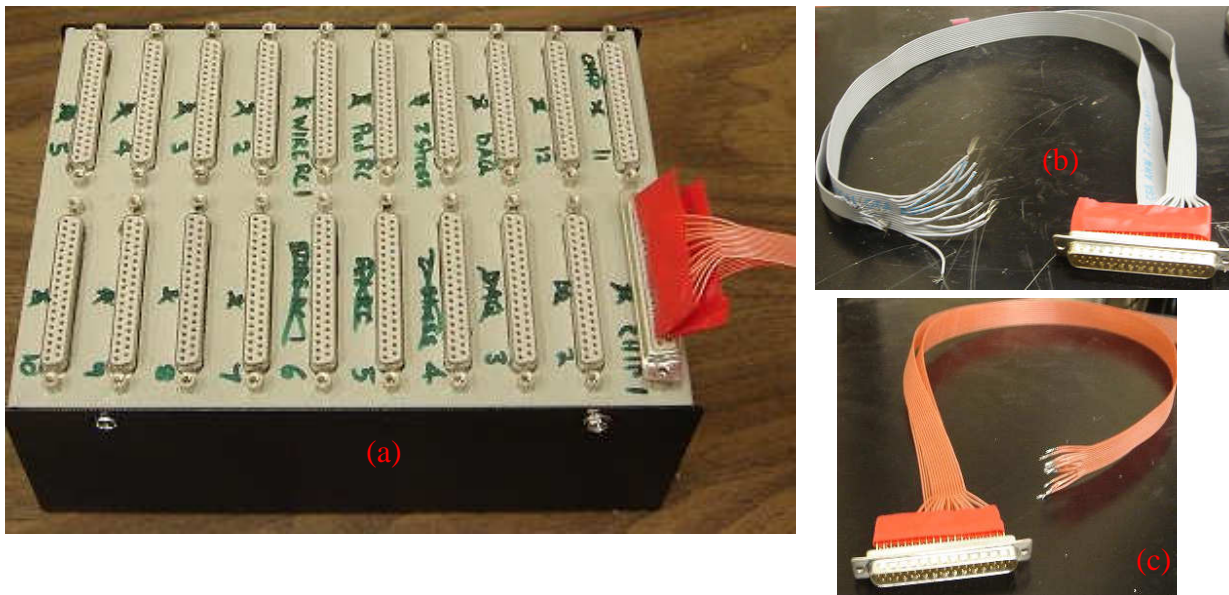
Fig. 34   (a) Switchbox (b) Connector with band of wires (c) Connector with band of high temperature wires.

4.1.5. Devices

A total of 3 Keithley 2700 Mainframes (Keithley Instuments Inc., Cleveland, Ohio) equipped

with Keithley Model 7708 40 channel multiplexer cards are used. Each MUX card has 40 chan-

nels. Since the number of R_C measurements exceeds the available channels on one card, 2 cards

are used to multiplex the top R_C connections (V_H, I_H) supplied by the wire bonds, and another

mainframe with 2 cards is used to select the bond pad connections (V_L, I_L) for 4-wire measure-

ment. A mainframe with one MUX card is used to select a chip from which to read S.

An Agilent 34401A 6 1/2 Digital Multimeter (Agilent Technologies, Santa Clara, California) is

used to measure S and a pair of Agilent 34420A 7 1/2 Digital NanoVolt/Micro-ohm Meters with 6

digit resolution and offset compensation are used to measure R_C.

A set of transistors is used to amplify the signals supplied by the DAQ as described in Appendix

B. The amplified power is provided by a pair of Tekpower 3645A DC power supplies (Tekpower

Inc., Taipei, Taiwan). One power supply will provide a 3V sensing current to the stress sensors.

The other will provide 4V used to operate the on-chip MUXs.

4.1.6. Software

A program called Correlate.m is written using Matlab (The Mathworks Inc., Novi, Michigan) and

is used to record oven temperature and non-destructive data which is displayed graphically in real

time and is stored in a .csv file.

The software cycles through all R_C measurements and all S measurements. At each measurement

interval (Table 1), the program records a single R_C measurement and a single S signal before

switching focus to the next double ball bond and the next set of stress sensors. For the first 9 h, the

program allows an average of 14 s between measurements. This provides a time resolution of 14.2

min between R_C measurements of the same bond or 27.3 min between measurements of the same

sensor signal. As the rate of S and R_C change is expected to slow down over time, the period between measurements is increased to 42.5 s after 17.7 h, to 83 s after 45.3 h, and to 114 s after 99.3 h incrementally reducing the size of the data file created, and reducing the number of data points plotted. If the measurement frequency is not reduced in this way, the program has been observed to crash due to memory overconsumption.

4.2. Setup B

Chips for destructive testing are placed on a shelf inside an oven with a Pt100 temperature sensor as shown in Fig. 35. The temperature sensor signal is recorded by the same DAQ used in setup A.
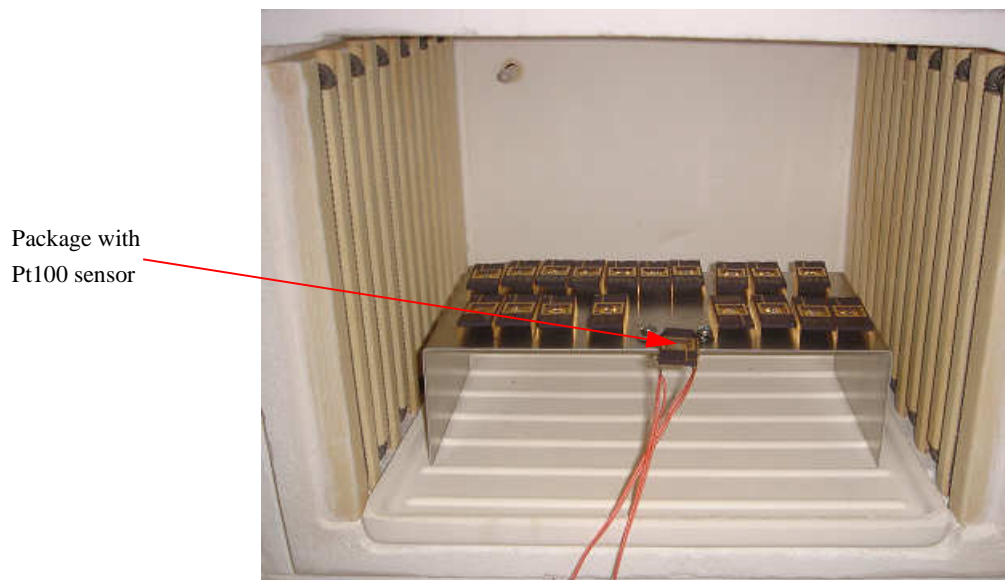
Fig. 35 Chips on shelf in oven in setup B.

5. Microstructural Analysis

A cross sectional analysis and observation of the bond exterior are conducted on samples for each aging duration given in Table. 1. At each time interval, physical quantities (properties) of the bond are measured as described in the following sections. Sample sizes for each measurement are given in Table 6.

5.1. Properties Evaluated

Table 7 lists the quantities evaluated to characterize the bond microstructure during aging. Each of these quantities are described in the paragraphs that follow.

5.1.1. Quantitative Measures

As shown in Fig. 13, IMCs formation lateral to the bond (AuAl, $AuAl_2$) causes a volume increase and results in compressive force felt by the sensing elements. These are Al-rich IMCs, and their formation may result in the depletion of pad Al adjacent to the bond. Formation of $AuAl_2$ is char-

Table 6: Sample sizes

Hours of HTS	Cross Sectional Measurement (AIT, AIC, OCV, PPD, PAC)	Overview Measurement (LIW)
0	12	9
0.5	23	12
1	13	11
10	14	10
100	12	9
300	16	8
600	18	16
900	20	12
1300	36	6
2000	3	18

acteristic of bonds in late stages of aging and is often observed soon before bond failure, earning it the name "purple plague" [5].

The amount of lateral IMC is measured from overhead SEM images, as a SEM allows for wide depth of focus on areas of the bond at different heights, while providing higher resolution than optical microscopy. Overhead images are used as opposed to cross sections, because failure to section the exact center of the bond may misrepresent the width of the lateral IMC ring as shown in Fig. 36 a, and because overhead images show IMC growth for the entire bond periphery as opposed to one specific location. It is also possible that brittle lateral IMCs are damaged during sectioning.

The lateral IMC width is measured in 4 directions for a sample of bonds at each time interval, as shown in Fig. 36 b, and the average of the 4 measurements, LIW for all bonds is determined for each time interval. Due to curvature of the bond as shown in Fig. 37, the actual lateral LIW is approximately 2 µm greater than the measured LIW for all bonds. However, while the overhead measurement does not represent the exact value, it does accurately describe its incremental growth.

Table 7: Bond Properties

Quantity	Abbreviation	Unit
Lateral IMC Width	LIW	µm
Interfacial IMC Thickness	AIT	µm
Average IMC Coverage	AIC	% of interface
Oxide / crack / voids at interface	OCV	% of interface
Penetration of Diffusion Barrier	PPD	% of bonds
Full Pad Conversion to IMC	PAC	% of bonds

The thickness of the interfacial IMCs is measured at 3 random locations at the cross section of each sectioned bond as shown in Fig. 38. Measurements are taken from the top of the IMC layer to the bottom of the IMC layer. The AIT is the average of these measurements.

In the early stages of aging, IMCs do not cover the entire interfacial surface between Au and Al; there are regions of unbonded base metals. To characterize lateral IMC growth under the ball, the
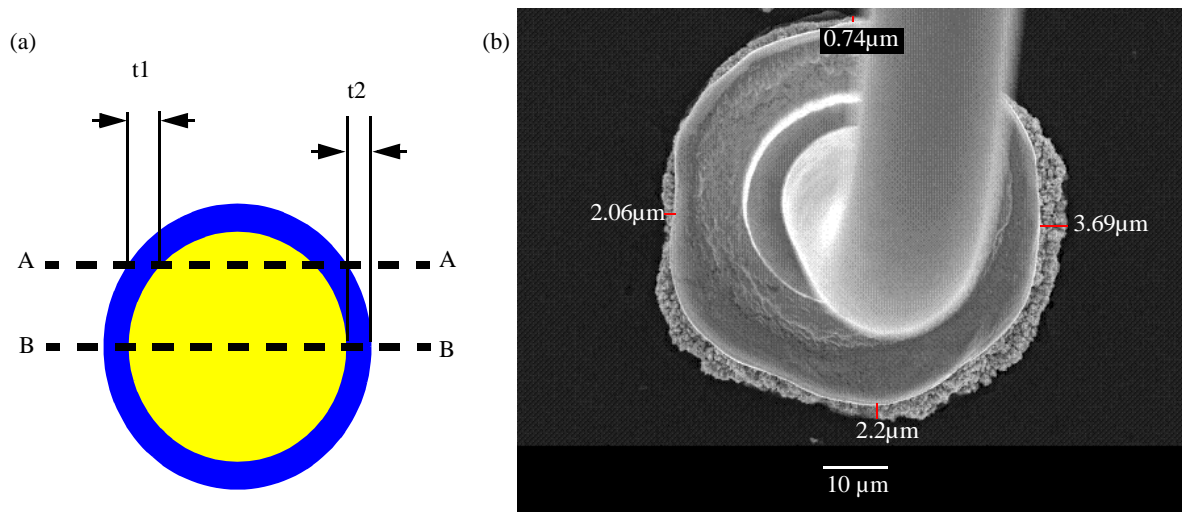

Fig. 36 Lateral IMC measurement. (a) IMC thickness can be misinterpreted if it is measured through sections. Lateral IMCs appear wider if cross section is away from bond center (t1) as opposed to at the bond center (t2). (b) Peripheral IMCs measured at 4 locations on chip 17, bond 20. Average IMC width = 2.17 μm.
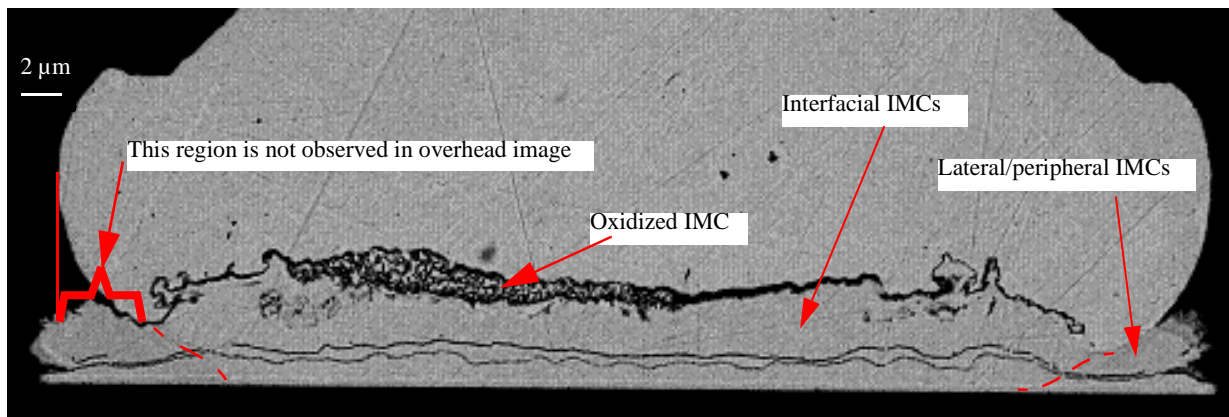
Fig. 37 Some lateral IMCs are not visible due to curvature of bond

percent of the interface covered by IMCs, AIC, is determined at each time interval by dividing

cross sectional area with IMCs by the total cross sectional width of the bond as shown in Fig. 39.

Close-up images are required to identify IMC regions on relatively unaged bonds.

Both voids/cracks and oxide appear as dark regions when examined with both SEM and optical

microscopy. While oxide regions have visible precipitates, it is not always possible to distinguish

them from void regions so they are measured together in this work. Both regions are expected to

lower shear strength of the bond and both regions are expected to increase contact resistance. The

oxide regions are expected to generate compressive stress on sensors as they create a 7% volume

expansion compared to the volume of Au_4Al [3]. Cracking is expected to have a tensile effect

Fig. 38   IMC thickness measurements. Example from chip D19 bond J with average thickness of 4.47μm

Fig. 39   Example measurement of interfacial coverage from chip D3 bond 3.

56

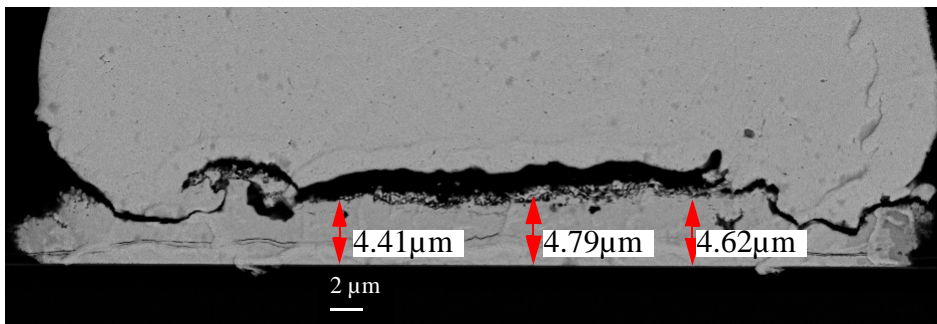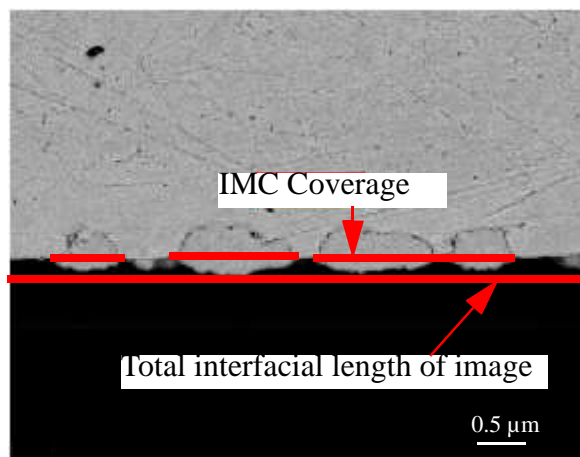radially on the sensor elements as it releases the bonded ball from the pad. The bonded ball compresses the sensor elements due to its thermal expansion.

The degree of cracking/voiding/oxidation at the interface, OCV, is measured in the same way as the interfacial IMC coverage (Fig. 40). The width of the region is measured but the thickness of this region is not taken into account because some bonds with 100% interfacial cracking/oxidation are lifted off the IMC layer during grinding and polishing, making the oxide/crack height unmeasurable for these bonds.

When the DBL separating the 2 layers of Al in the bond pad is broken and penetrated by IMC growth, Au-rich IMCs are given access to a large Al supply from the lower pad layer. This results in a period of rapid IMC growth. To quantify this phenomenon, at each time interval, the percent of examined bonds with penetrated DBL, PPD, is calculated. Figure 41 a depicts a bond with the DBL intact, and Fig. 41 b depicts a bond with the DBL penetrated after 300 h.

When the Al under the pad is fully consumed by IMC growth, the IMCs under the ball (i.e. the interfacial IMCs) may no longer expand downwards, and their growth rate decreases. At each time interval, the percentage of bonds where both Al layers of the bond pad are consumed, PAC, is determined. Figures 41 a and b show bonds with incomplete Al consumption. Figure 42 shows a bond where all Al directly beneath the bond is consumed.
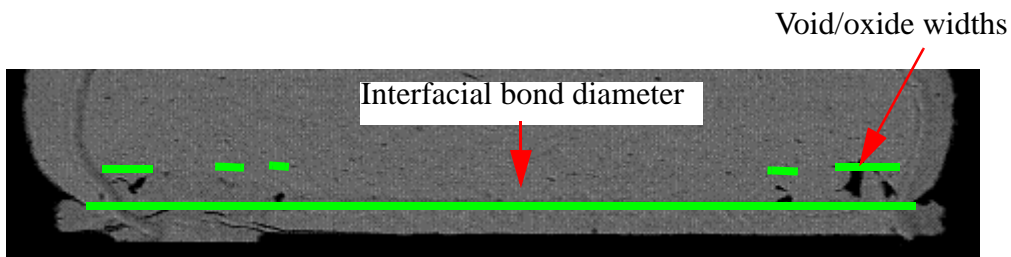
Fig. 40   Example void/crack/oxidation fraction measurement from chip D10, bond B. In this case 19% of the bond diameter is covered by of voids or oxide.

5.1.2. Identification of IMCs

IMCs are identified by EDS analysis and visual analysis. EDS analysis is performed using an

EDAX detector with an accelerating voltage (EHT) of 10 or 15 keV. An Electron Flight Simulator
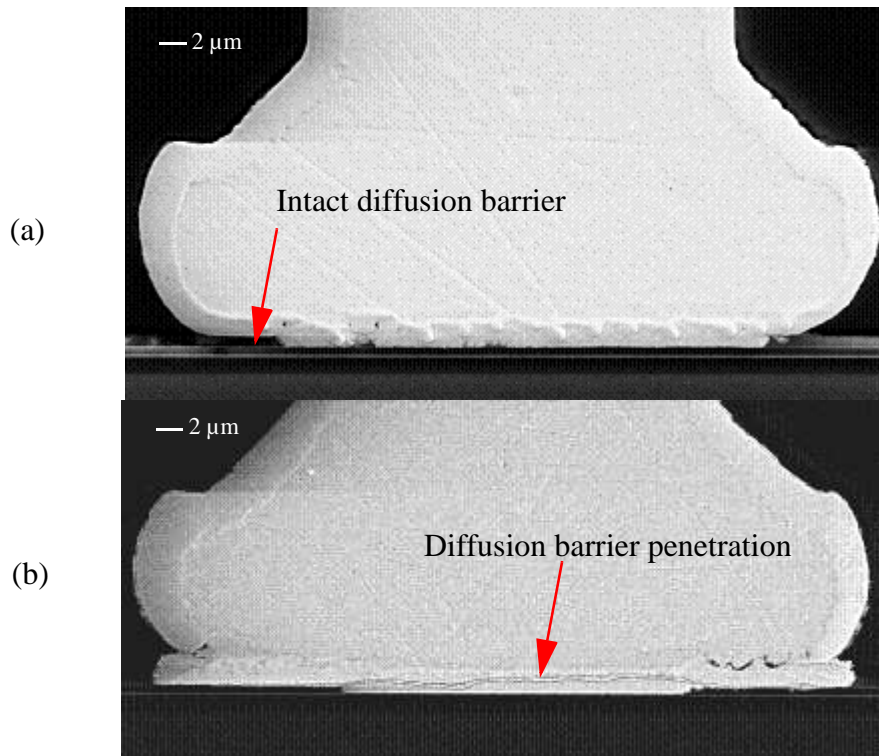
Fig. 41 (a) Bond J from chip D8. IMCs formed on top Al layer. No DBL penetration. (b) Bond F from chip D10. DBL has been broken and IMCs have formed in lower Al layer.
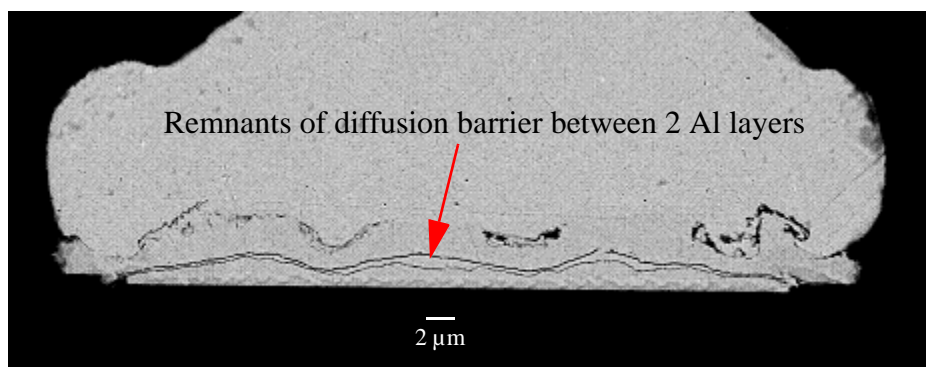
Fig. 42 Bond with All under-pad Al converted to IMCs.

(Small World LLC, Vienna, Virginia) Monte Carlo simulation showing the volume of interaction where x-rays can be generated during EDS with 20 keV EHT is shown in Fig. 43. This reveals a spot size of approximately 0.7µm diameter, which is slightly larger than the interaction volume created with a 15 keV EHT. Therefore, EDS analysis can be considered reliable for IMC regions with larger than 0.7 µm diameter.

Visual identification of different IMC regions is possible due to different IMC colours [28]. $AuAl_2$ may be observed at the ball periphery due to its purple colour (hence the nickname "purple plague"). Au_2Al is slightly darker than Au_8Al_3, which are both grey in colour. Au_4Al is matte yellow, but less bright than Au, and can normally be found at the top of the IMC layer next to the Au ball. In later stages of aging, a yellow phase that possibly is Au_4Al, but may actually be an unidentified ternary Au-Al-Ti phase, is observed near the DBL.
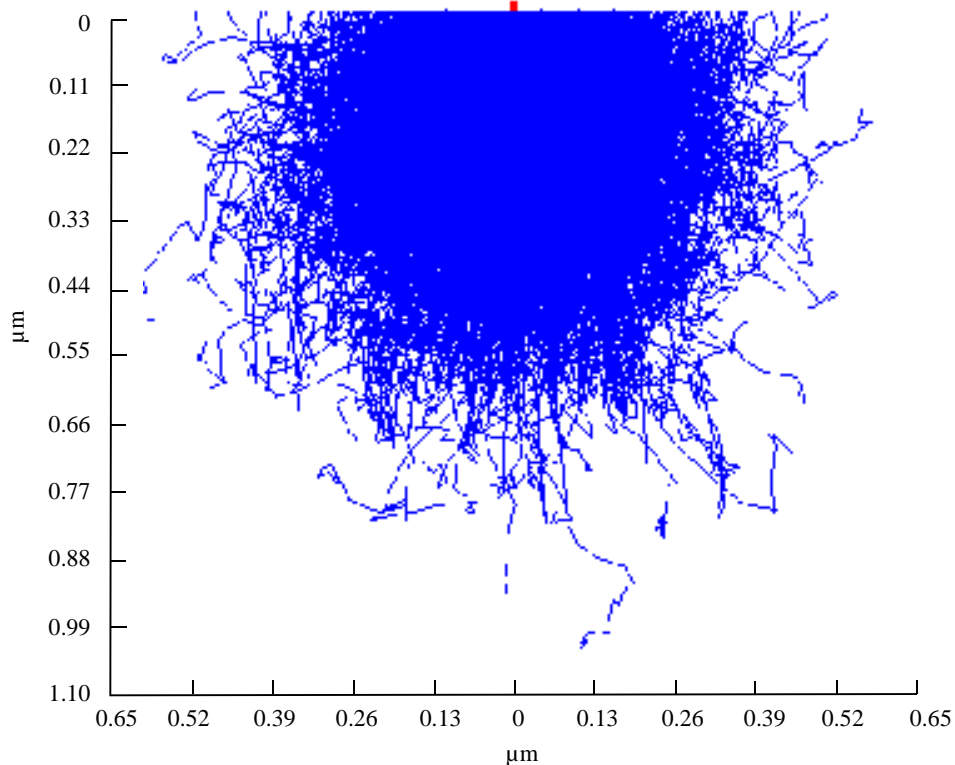
Fig. 43 Monte Carlo simulation of the interaction volume for Au with 20 keV EHT.

5.2. Microstructural Evolution

The microstructural evolution is observed at each time interval, and the physical properties of the bond are measured and quantified. Cross sections of all bonds are found in [29].

5.2.1. Unaged (As-bonded)

Figures 44 a, b, and d show cross sections for a typical bond in the unaged condition. As can be seen, there is very little IMC formation due to the low temperature bond conditions, and the majority of the upper pad layer is still unreacted Al. Interfacial IMCs are less than 1/4 µm thick and cannot be identified by EDS, although it is anticipated that Au_8Al_3 would be the first IMC to form at the interface [1]. No visible pad depletion of lateral IMC formation is present.
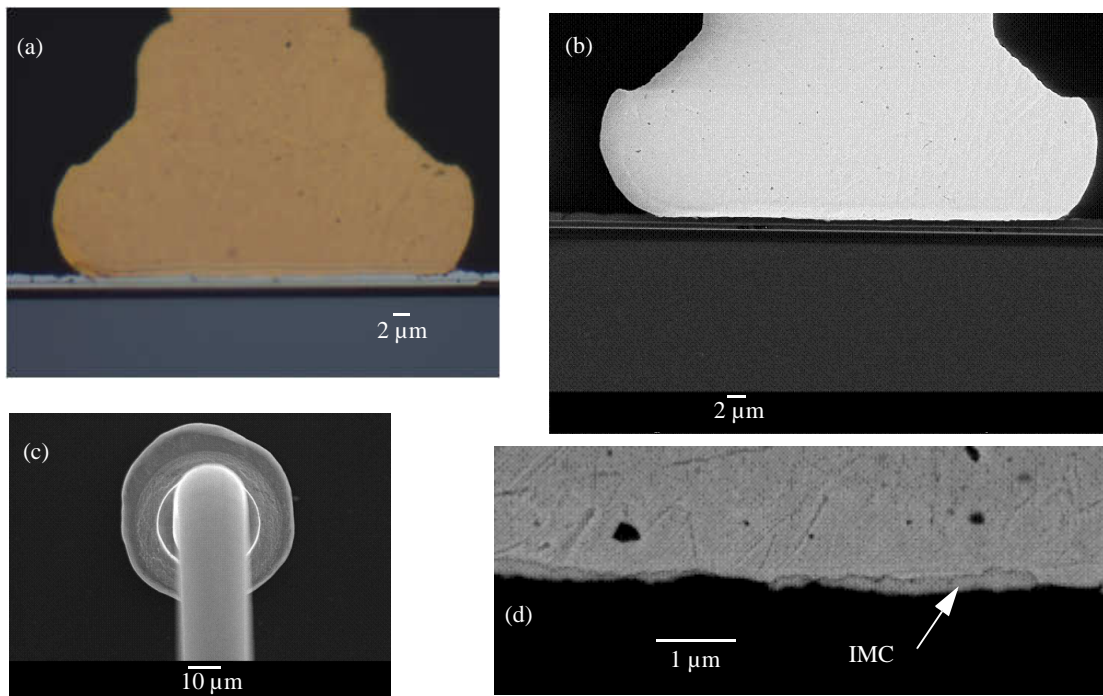
Fig. 44   Unaged bond. (a) Optical micrograph of typical unaged bond. (b) SEM image of the same bond. (c) Overhead view of typical unaged bond. (d) 25000 x magnification of bond inter-

5.2.2. Half Hour Age

Figures 45 a, b, and d depict cross sections of a typical bond aged for 1/2 h. IMCs at the interface have expanded upwards into the Au ball and down into the first Al layer. Some patches are now large enough to be identified by EDS, and are found to be Au_8Al_3. The majority of the first Al layer has not yet been converted to IMCs. No change to the ball periphery or surrounding pad is visible from an overhead view (Fig. 45 c).

5.2.3. One Hour Age

After 1 h, the IMC has consumed the Al down to the first DBL in some spots despite the fact that there are still unbonded regions on the interface as seen in Fig 46 a and b. EDS analysis identifies the columnar IMC grains visible in the IMC layer as Au_8Al_3, and the more equiaxed grains below
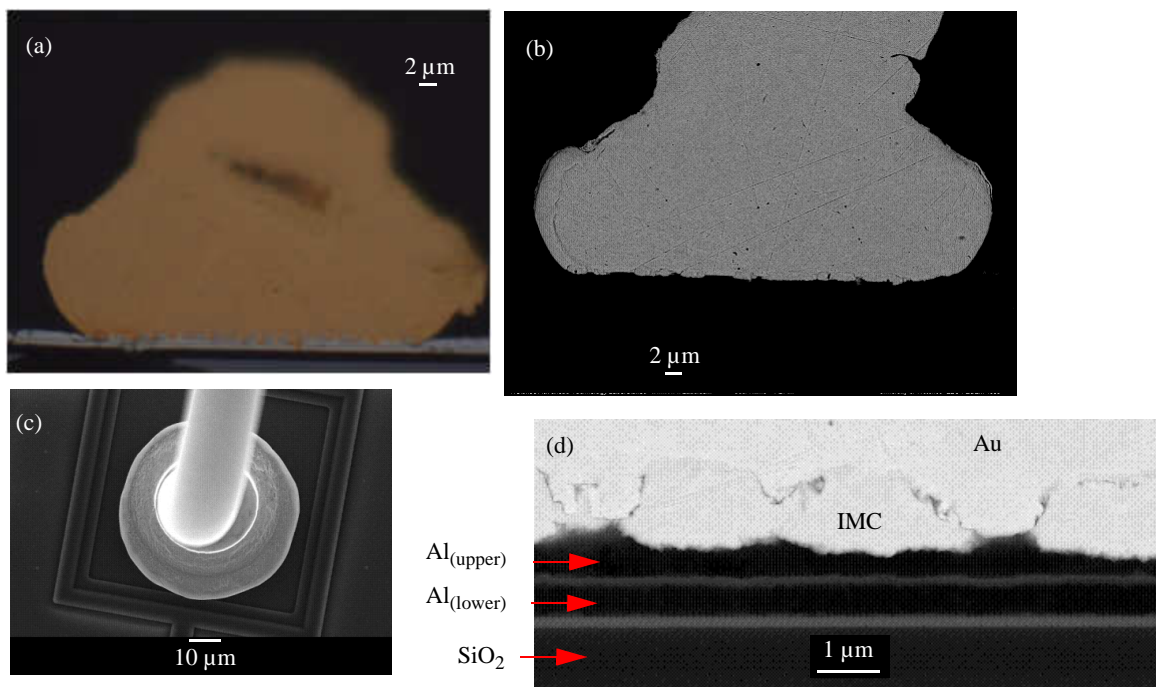
Fig. 45   Bond after 1/2 h age. (a) Optical micrograph. (b) SEM image (c) Overhead SEM image. (d) 20,000x magnification of bond interface. IMC identified as Au_8Al_3 by EDS

them as Au_2Al as shown in Fig. 46 d. It is expected that a thin layer of Au_4Al may exist directly below the Au ball; however this has not been identified by EDS in any of the bonds aged for 1h.

5.2.4. Ten Hour Age

After 10 h, the IMCs cover the entire bonded area in some bonds, and the first layer of Al directly underneath the bond has been consumed. In other bonds, coverage is not lower than 69% with average IMC thickness of $3.22\mu m \pm 0.32\mu m$. It is evident that significant grain growth has occurred in the IMCs, as the Au_8Al_3 grains have grown in size since 1 h as shown in Figs 46 d and 47 d. IMCs have formed directly under the ball center and are growing vertically upward into the ball. The edges of the bonded ball have no IMCs under them. This is the start of the Au hook formation observed by Breach et. al [2]. Au_4Al is now identifiable under the bond by EDS. Lateral
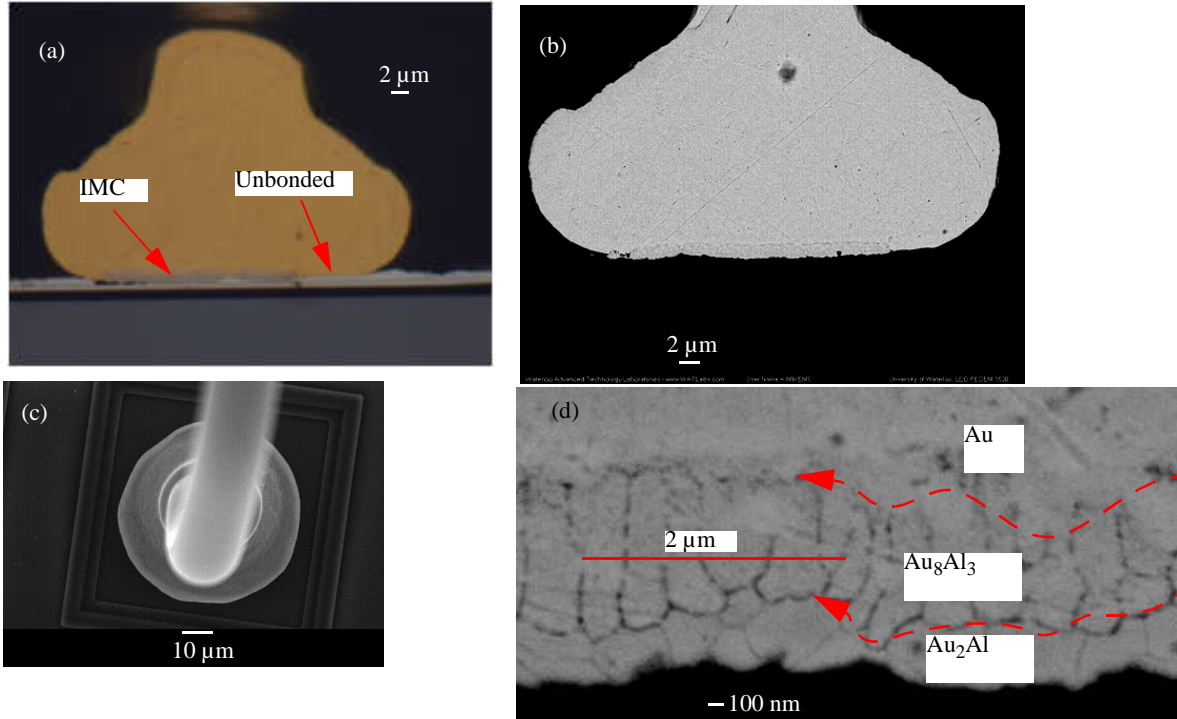
Fig. 46 Bond after 1 h age. (a) Optical micrograph of typical bond. (b) SEM micrograph (c) SEM overview (d) Interfacial IMC region at 20,000x magnification. Au_8Al_3 grain size is small compared to grains after 10h, as 7 Au_8Al_3 grain boundaries are crossed by a 2 μm long line

low density IMCs start to form at the periphery and AuAl is identified at the bond periphery as shown in Fig. 47 e.

5.2.5. Hundred Hour Age

By 100 h, all of the first Al layer has been consumed under all of the bonds. For 7 of the 12 bonds examined, the IMC layer has penetrated the Ti boundary and started to consume small amounts of the second Al layer as shown in Fig 48. As Au penetrates the boundary layer more readily than Al, and a large supply of Al is available for the slow-diffusing Au, Au_2Al forms in the new lower IMC region as shown in Fig. 48.

Dark regions, possibly pores or oxidized Au_4Al, have started to form along the boundary between the base Au and the IMCs as shown in Fig 49. It is theorized that pores are formed as a result of a
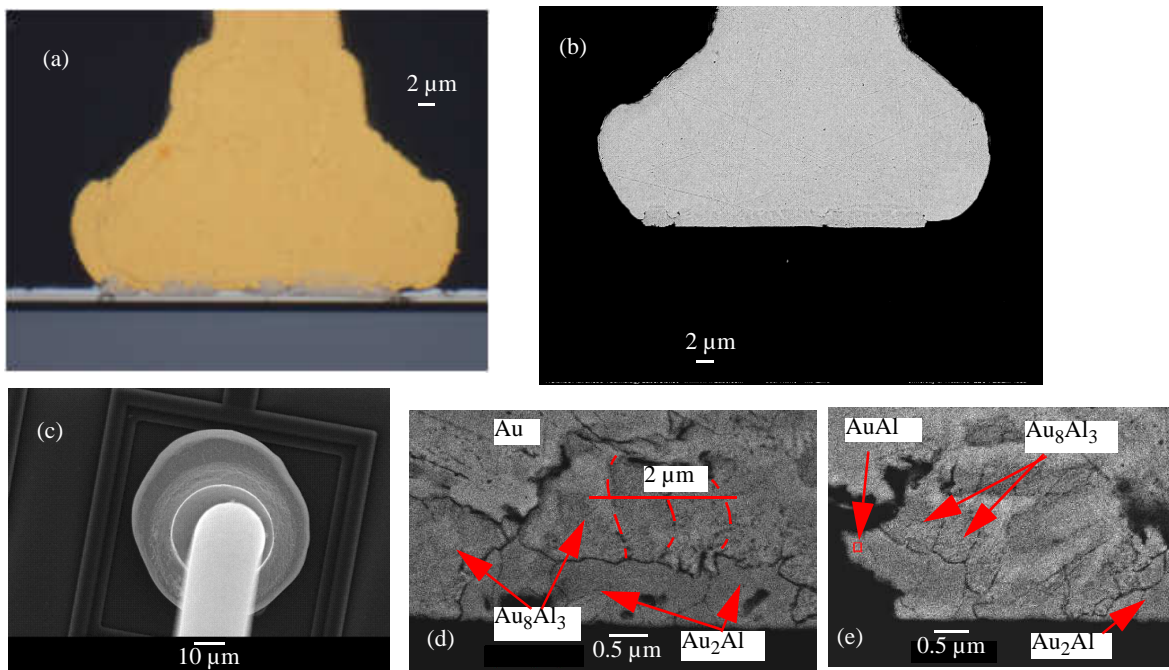
Fig. 47   Typical bond aged for 10 h. (a) Optical micrograph (b) SEM image (c) Overhead SEM image (d) Interfacial IMC region at 20,000x magnification. Large Au_2Al, Au_8Al_3 grains present. 3 Au_8Al_3 grain boundaries are crossed by a 2μm line. (e) IMC region at bond periphery at 20,000x magnification. Note formation of AuAl.

combination of the Kirkendall effect where base Au diffuses into the IMC faster than IMCs can

consume the base Au, leaving voids behind [13]. Volume differences between IMCs may also
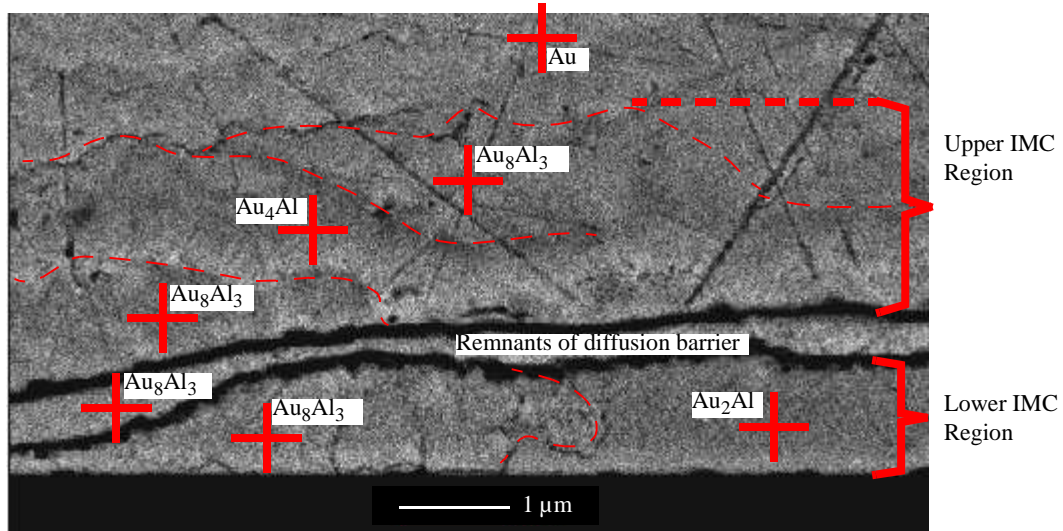
Fig. 48   Initial IMC formation in the lower Al pad layer (after 100 h).
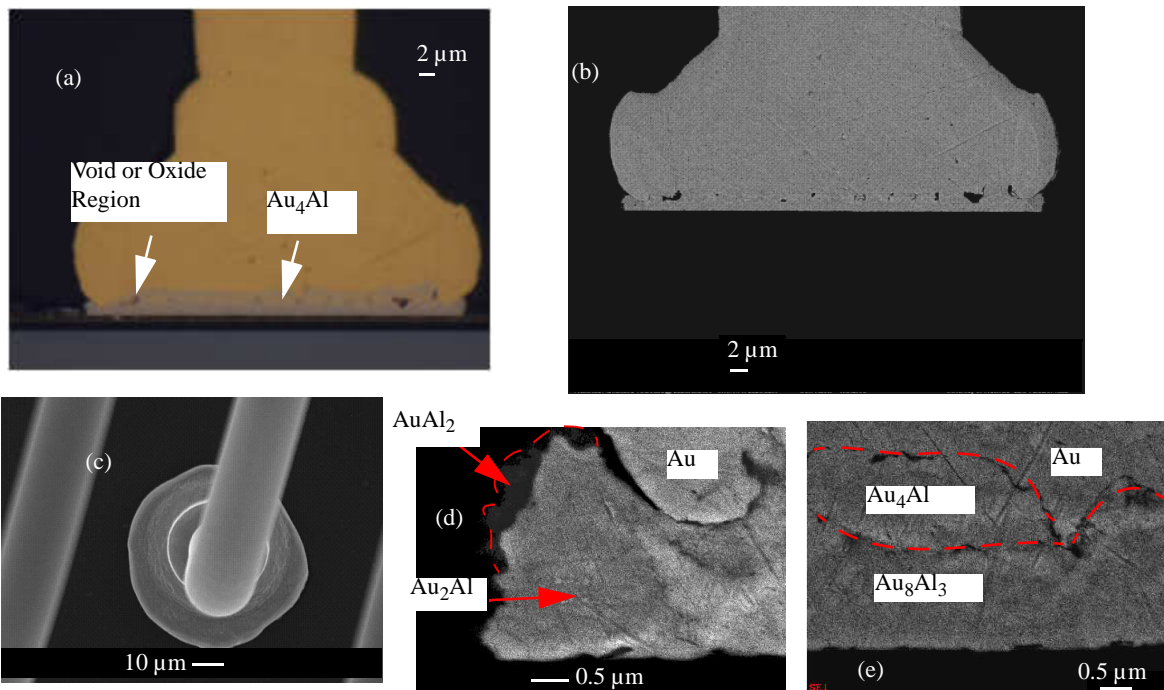
Fig. 49   Typical bond after 100h age. (a) Optical micrograph. Dark regions appear along the yellow line of Au_4Al, which may either be oxidized IMC, or voids/cracks. (b) SEM micrograph. (c) Overhead SEM image (d) Lateral IMCs at 20,000x magnification. IMCs identified by EDS. (d) Interfacial IMCs at 20,000x magnification. IMCs identified by EDS

result in interfacial cracking. IMCs under the bond shrink, while lateral (Al-rich) IMCs adjacent to the bond expand and push the Au ball upwards [13]. Alternatively, evidence of these dark regions being oxidized Au_4Al is given by the fact that all dark regions occur on the yellow line of Au_4Al in Fig. 49 a.

5.2.6. Three Hundred Hour Age

The entire lower layer of Al has been consumed in 9 of the 16 bonds examined. Two lines are now visible where the upper DBL previously separated the Al layers. The composition above, below, and in between the lines is a mixture of mainly Au_8Al_3 and Au_4Al grains. At the interface with the lower DBL which separates the bond pad from the chip, there is a high concentration of Au_2Al as this location is the last IMC region to which Au will diffuse and form Au-rich IMCs. A yellow IMC line is forming at the DBL which is now integrated into the IMC bulk. Ti is detected in varying concentrations in some EDS analyses, and is sometimes not detected at all in this region. The ratio of Au:Al is 4:1; together with the yellow colour, this suggests that this is a layer of Au_4Al forming in the middle of the IMC layer. This could occur because Au can pass through the DBL while Al cannot due to its lower diffusivity in Ti [16]. Where the Au_4Al IMCs, and the Au "hooks" in the upper Al layer contact the DBL, Au diffuses through to the lower Al layer, allowing for the formation of Au_4Al. The result is a layer of Au_4Al sandwiched between two Au_8Al_3 layers as shown in Fig. 50 b (iii). This intermediate Au4Al layer is not present in single-layer bond pads which develop a microstructure similar to that shown in Fig. 50 a.
The dark region at the interface is seen to form between the Au_4Al IMC and the Au_8Al_3 IMC near the unbonded hook region of the ball where oxygen is able to reach the IMCs, indicating that this region is likely oxidized Au_4Al as seen in Fig. 51.

At the periphery, the AuAl and $AuAl_2$ regions have grown since first observed at 100 h. The Au hook now curves in underneath the top layer of IMCs (Fig. 52 a and b). The peripheral IMCs extend in some places further outward than the curvature of the Au ball as shown from above in Fig. 52 c.
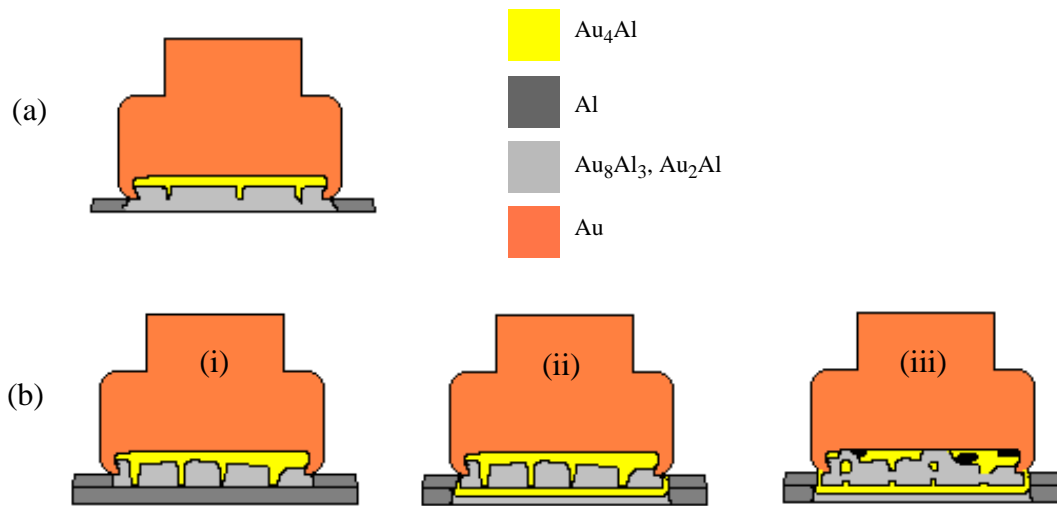
Fig. 50 Development of second Au_4Al layer. (a) In a chip with 1 Au layer typical of most reliability studies, Au_4Al forms near Au ball; Other IMCs form below. (b) (i) Similar microstructure to (a) forms. (ii) Au passes the diffusion barrier, forming another Au_4Al layer in second Al layer. (iii) Due to thickness of Al, a lot of Au diffusion is required for IMC formation resulting in excessive Kirkendall voiding at Au/IMC interface.
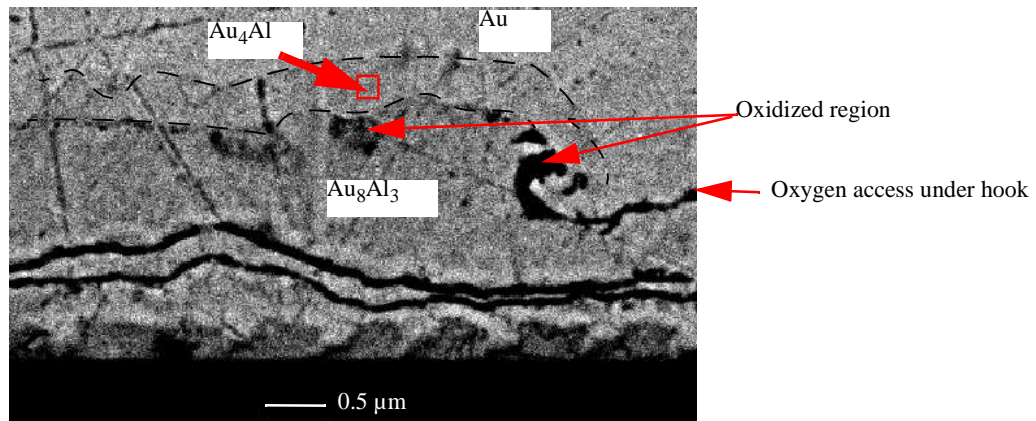
Fig. 51 Dark region next to Au4Al and exposed to air is likely oxide.

5.2.7. Six Hundred Hour Age

The first continuous dark regions (oxide with potentially some cracking) are observed running the whole length of the interface between the Au and the IMC layers. In the thicker parts of these dark regions, Au precipitates can be found as seen in the Fig. 53 b detail, suggesting that Au_4Al oxidizes forming dark Al_2O_3 oxide with Au precipitates. In all bonds, a line of Au_4Al is found in the middle of the IMC layer near the DBL lines, bordered above and below with Au_8Al_3 grains (Fig. 19 a). This lower Au_4Al region has grown since 300h without oxididizing like the upper Au_4Al layer.

At the periphery, significant formation of low density $AuAl_2$ is evident. The IMCs extending past the edge of the ball bond as viewed from an overhead angle shown in Fig. 53 c. The peripheral
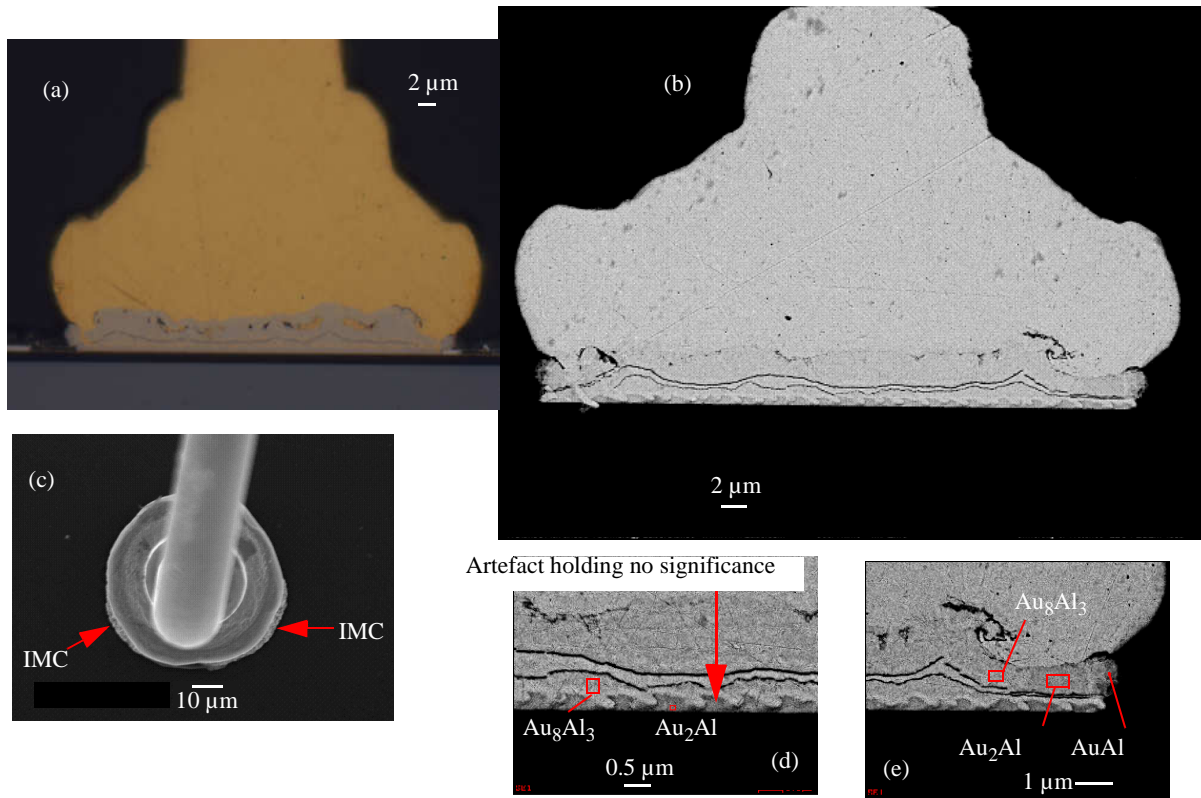
Fig. 52 Bond aged 300 h. (a) Optical micrograph of typical bond. (b) SEM micrograph of bond. (c) Overhead view. (d, e) 25000 x magnification of bond interface at bond center and at periphery. The dark wavy region consists of both Au_8Al_3 and Au_2Al.

IMCs have grown visibly since the 300 h interval, and some Al pad depletion is visible at the

edges of the IMCs extending farthest from the bond.

5.2.8. Nine Hundred Hour Age

The vertical thickness of the IMCs has decreased since 600h from 6.26 µm to 5.13 µm. This is

due to continued oxidation of most remaining upper Au_4Al, and diffusion of Au to the lateral

IMCs where significant growth has occurred. Sample cross sections are shown in Figs. 54 a, b, d,

and e. An overhead view of the bond showing lateral IMC growth is given in Fig. 54 c.
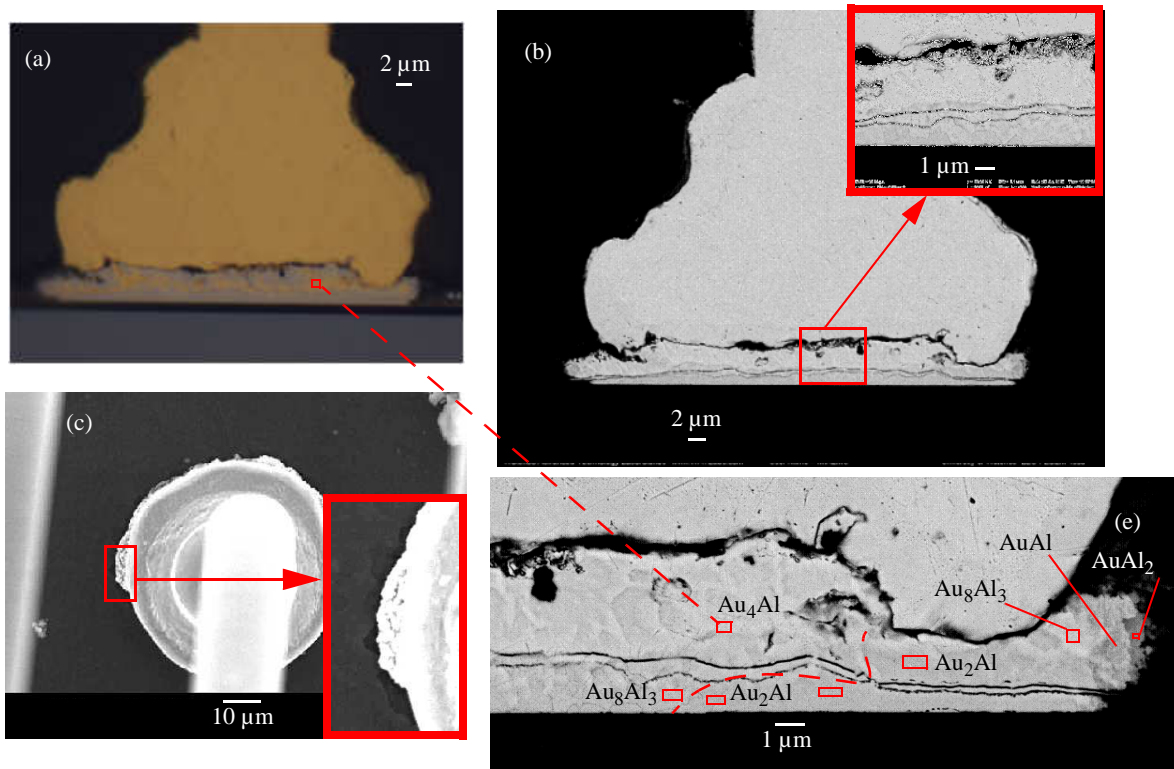
Fig. 53 Typical bond after 600 h age. (a) Optical micrograph (b) SEM micrograph. Detail shows Au precipitates indicating that the dark region is oxide and not a void. (c) SEM overview of bond. Detail shows Al pad depletion in high contrast. (d) IMC region with EDS identification.

5.2.9. One Thousand Three Hundred Hour Age

Little has changed at the interfacial IMC layer. The IMC thickness has slightly decreased due to further Au_4Al oxidation. Oxidation and possibly voids and cracks now cover 100% of the bonding interface at each cross section examined as seen in Fig. 55 a, b, d, and e. Lateral IMCs have increased in volume as seen in Fig. 55 c.

5.2.10. Two Thousand Hour Age

There is very little change at the interfacial IMCs as all under-pad Al has long been consumed, the Au_4Al layer next to the ball has been completely oxidized, and the oxide layer next to the ball has
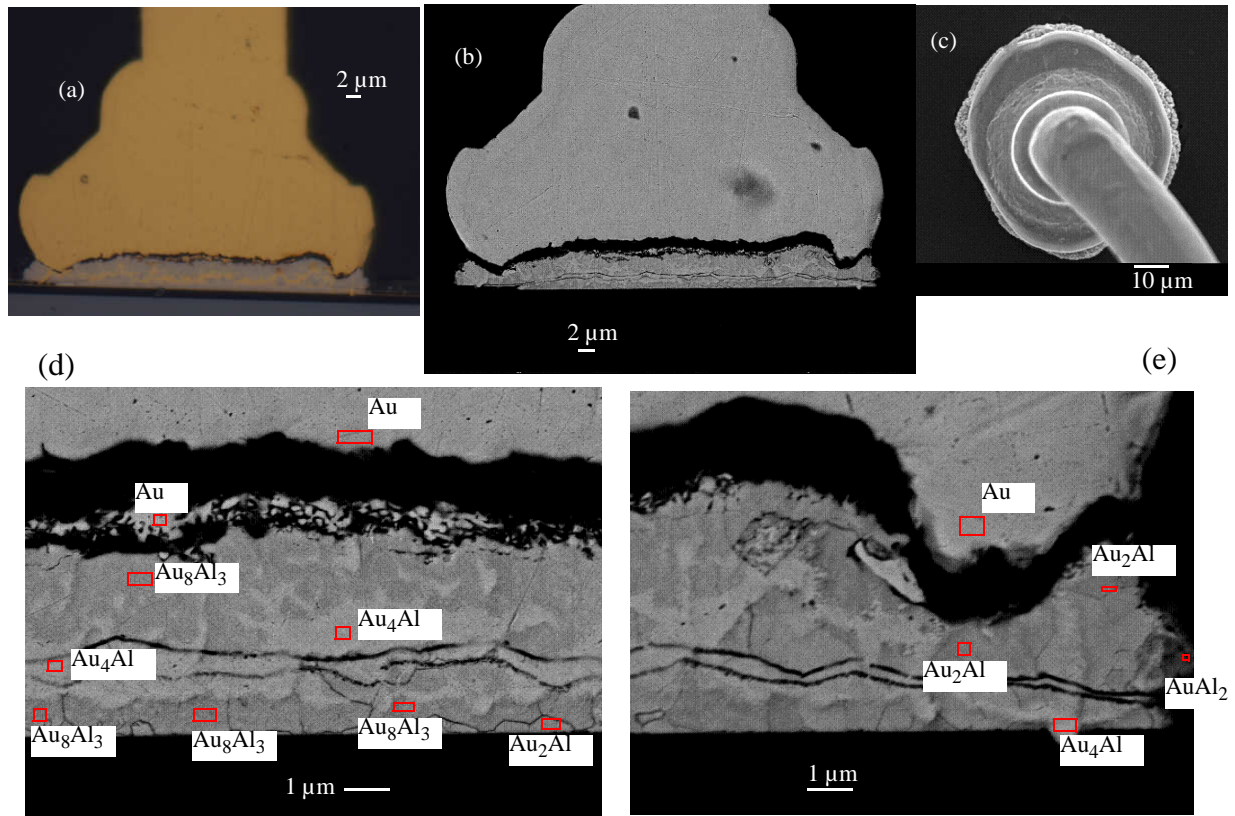
Fig. 54 Bond after 900 h age. (a) Optical micrograph (b) SEM micrograph (c) SEM overview (d) SEM close-up of IMC layer at center of bond with EDS identification. Note some Au_2Al grains remain at the very bottom of the IMC layer. Also note that Au_4Al which appears lighter on SEM images matches locations with yellow IMC from optical micrograph. (e) IMCs at bond periphery with EDS identification

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eliminated the supply of Au required for further IMC development. As the lateral IMCs have

grown, they consumed a lot of the base Al from around the ball bond. As a result, there are

regions of depleted Al (Kirkendall voids [30]) in the pad encircling the bond as shown in

Fig. 56 c. Cross sections of a typical bond, indicating IMCs identified by EDS analysis are shown

in Fig. 56 a, b, d, and f.

5.3. Measurements of Physical Changes

At each interval, values for all variables listed in Table 7 are measured. Fig. 57 plots all of these

properties as a function of HTS time. A discussion of these results in relation to S, R_C, and SS

results is found in Section 9.
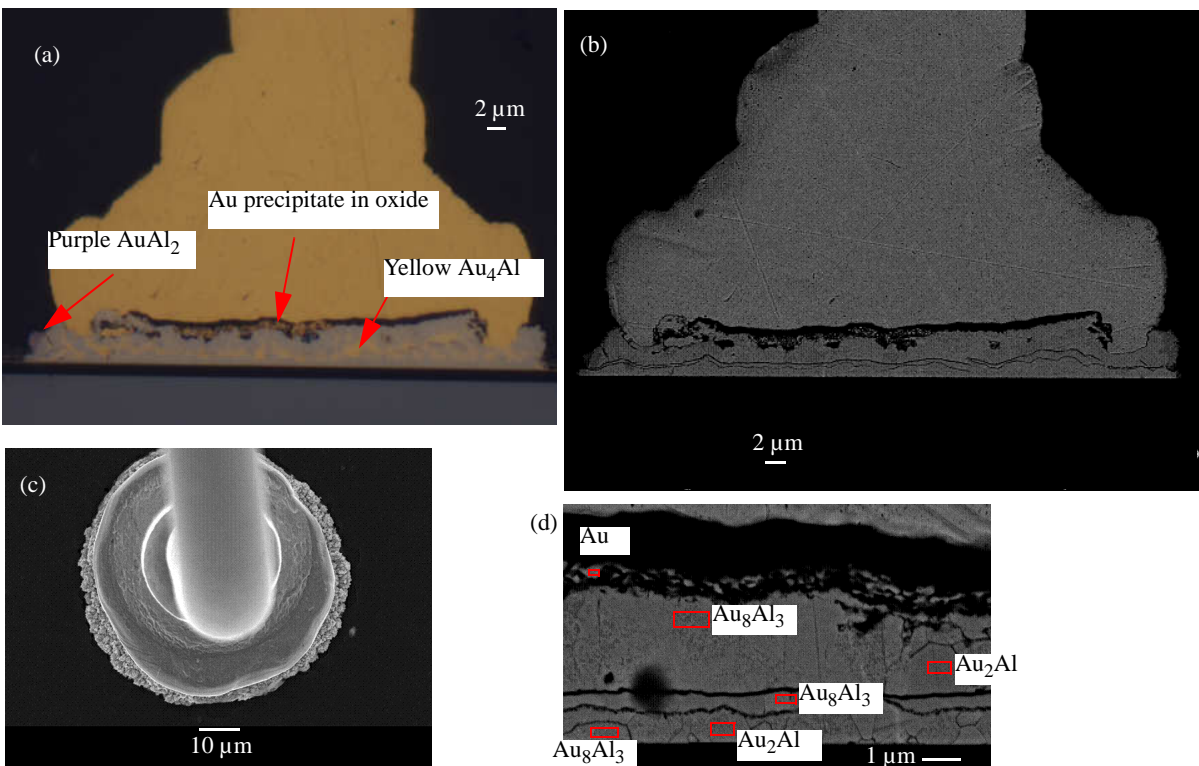
Fig. 55 Typical bond after 1300 h age. (a) Optical micrograph (b) SEM micrograph (c) SEM overview (d) EDS IMC identification

6. Shear Test Results

6.1. Shear Strength of Bonds

Shear strength of bonds over 2000 h HTS at 175ºC is plotted in Fig. 58. Shear strength initially increases, peaks between 10 and 100 h, and then drops. At its peak, the shear strength of the bonds is higher than the shear strength of the as-bonded Au wire.
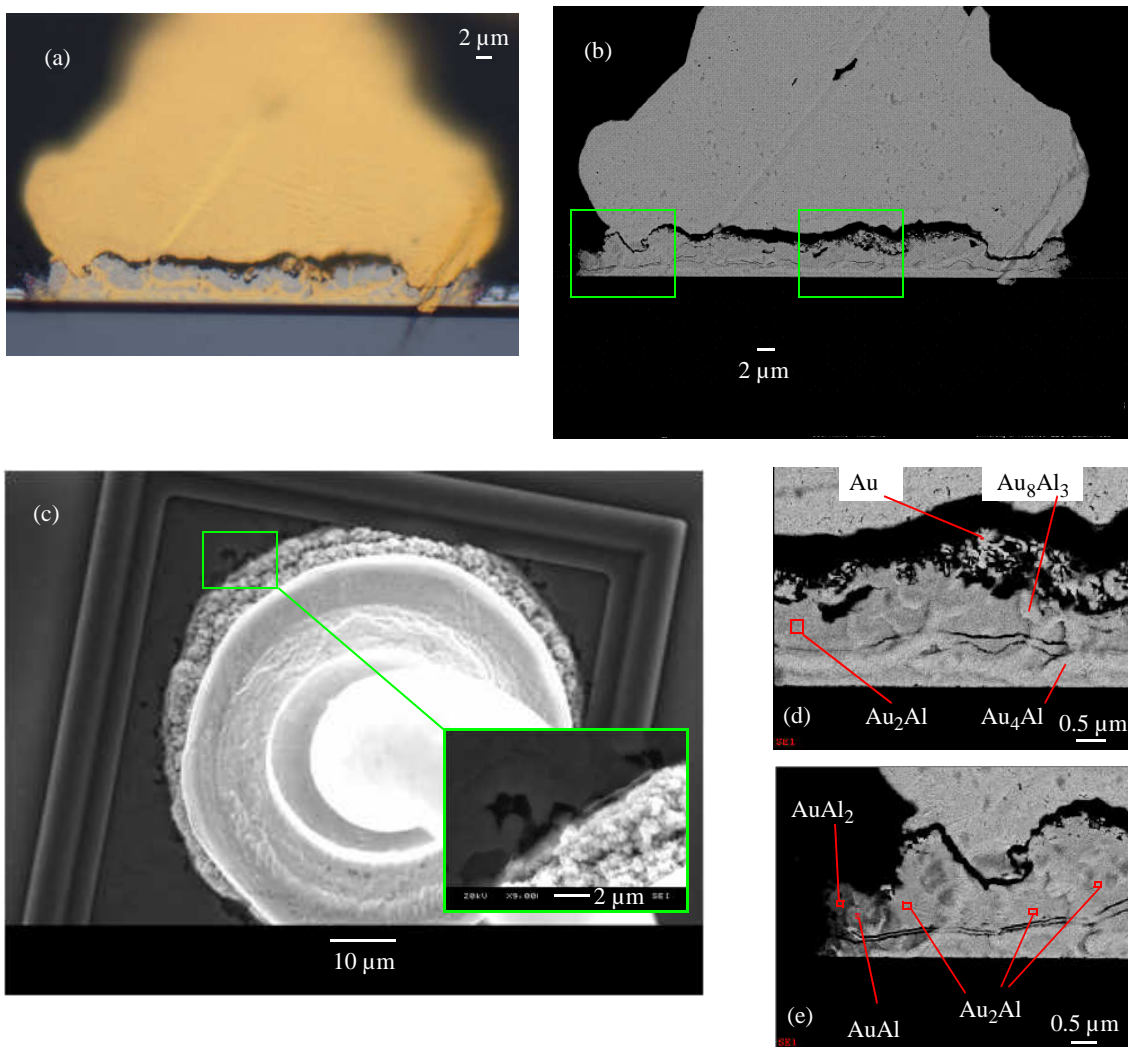
Fig. 56 Typical bond after 2000 h age. (a) Optical micrograph (b) SEM micrograph (c) SEM overview with detail showing high degree of Al pad depletion adjacent to lateral IMCs (d) EDS identification of IMCs under bond center. Note the Au precipitates indicating that the dark region is oxide. (e) EDS identification of IMCs at bond periphery.

The relatively low shear strength initially observed in unaged bonds is explained by the lower adhesion of interfacial regions without IMCs compared to regions with IMCs. During shear testing the bonds lift off, failing in shear mode 1. As the bond ages, the Al pad is consumed by IMC growth as the initial IMC islands grow to cover the entire bond interface. As the IMCs are 3 to 10 times harder than the base Au [1], the bond shears at its weakest point through the Au via shear mode 2a. As spikes of IMC grow vertically into the ball, higher than the 5µm height of the shearing ram, some IMCs are sheared along with the Au. This causes the shear stress to exceed the shear stress of the base Au. As aging progresses, the bond interface degrades due to oxidation of the Au_4Al layer, and formation of Kirkendall voids [13] along the interface between the IMC
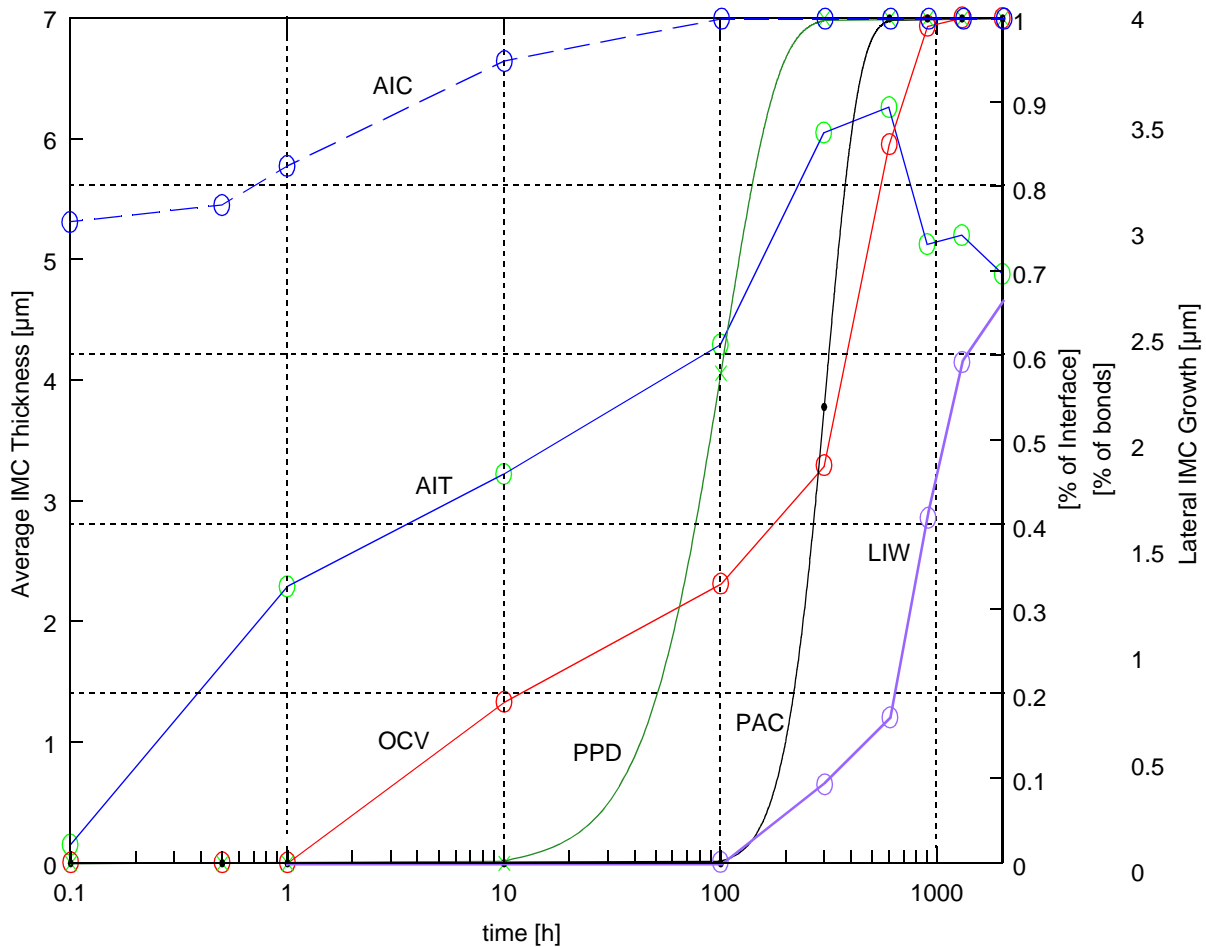
Fig. 57 Physical properties of aging bonds.

layer and the Au bump. After 300 h, a brittle oxide layer forms at the Au_4Al IMC, which may also

result in crack formation due to mechanical stresses [17]. Some bonds are sheared at the layer of

cracks and oxidation, lifting the ball off the IMC region and failing by shear mode 2b; these bonds

have lower shear strengths. The combination of the 2a and 2b failure modes results in an average

shear strength decrease. As time passes, the crack / oxide region between the Au and the IMCs

grows larger, and the percentage of bonds failing due to shear through the separating ball / IMC

interface grows. As a result of this, shear strength drops continuously for the remainder of the

2000 h period. By 1300 h, it is noted that continuous regions of oxidized Au_4Al (and possibly

cracks or voids) run the length of all Au-IMC interfaces as described in Section 5.2.9. The Au_4Al

layer next to the ball is greatly reduced indicating that the supply of Au from the bump has been

cut off. Therefore, there is very little fresh Au diffusion from this point onwards, slowing the

growth of Kirkendall voids. As the Au_4Al layer has been oxidized, there is little further oxide

growth. As a result, the shear strength does not significantly decrease between 1300 and 2000 h.
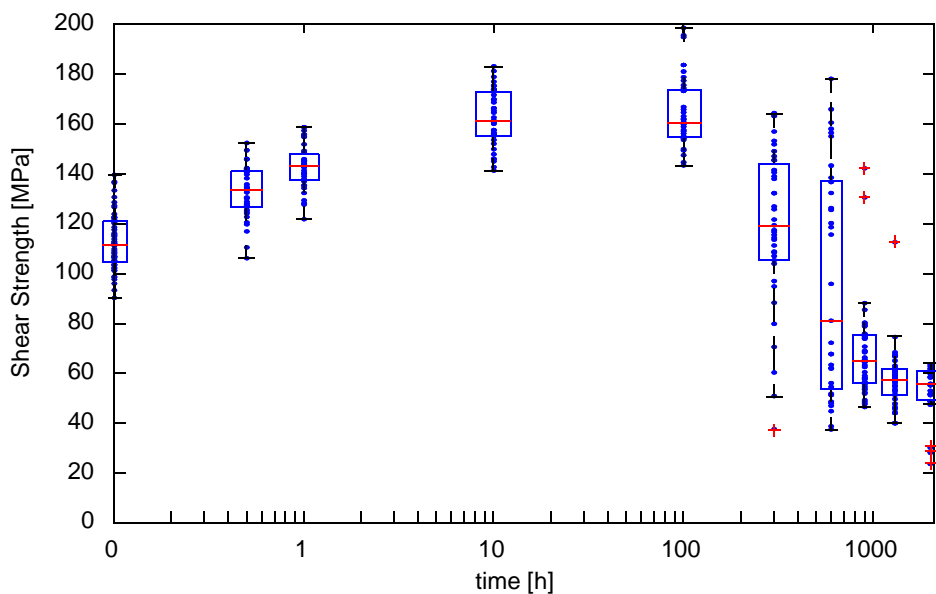
Fig. 58 Shear strength results over 2000 h.

6.2. Shear Interfaces

Examination of the shear interfaces at different points in the aging process verify the causes of shear failure. Figures 59 a, b and c show typical shear interfaces at early, mid, and late stages of the aging process corresponding to respective aging times of 0, 300, and 1300 h. As can be seen, three failure modes are present. The bonds are either lifted off the substrate as in the un-aged bond shown in Fig. 59 a, sheared through the Au as in Fig. 59 b, or sheared through the cracked, brittle, oxidized Au / IMC interface as shown in Fig. 59 c, resulting in brittle fracture. As expected, the majority of lift-off failures occur early on, while failure between the IMC and Au base metal occurs in more heavily aged bonds. In Fig. 60, the percentage of bonds which fail due to each mechanism is plotted against aging time.
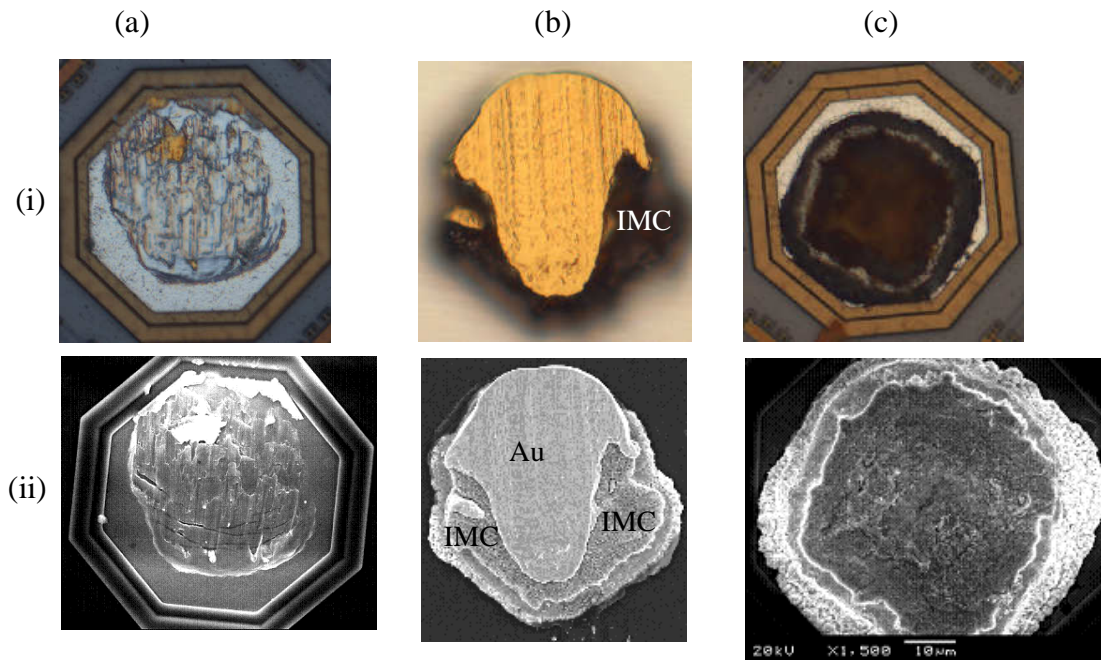
Fig. 59 (a) Typical shear interface of unaged bond. Failure mode 1: bond liftoff. (i) Optical image. (ii) SEM image of the same bond. (b) Typical shear interface of bond aged 300 h. Failure mode 2a: shear through Au. (i) Optical image. (ii) SEM image. (c) Typical shear interface of bond aged 1300 h. Failure mode 2b: shear through interface. Brittle failure. (a) Optical image. (b) SEM image.

7. Contact Resistance Results

The contact resistance (R_C) is measured as described in Section 3.7. Its change over time is shown in Fig. 61 a for all bonds, and in Figs. 61 b and c for one typical sample bond for clarity. Figure 61 a illustrates the strong dependence of R_C on location, as the R_C offset is similar for all bonds of each separate bond location described in Section 3.7. After an initial resistance rise caused by the increased temperature, R_C decreases by an average of 0.4 mΩ due to a pad resistance effect discussed in Appendix C for approximately the first sixty hours before increasing again for the remainder of the experiment. R_C is measured at room temperature of 30 ºC before and after the 2000 h age, and is found to have increased an average of 5.35± 0.52 mΩ during HTS.
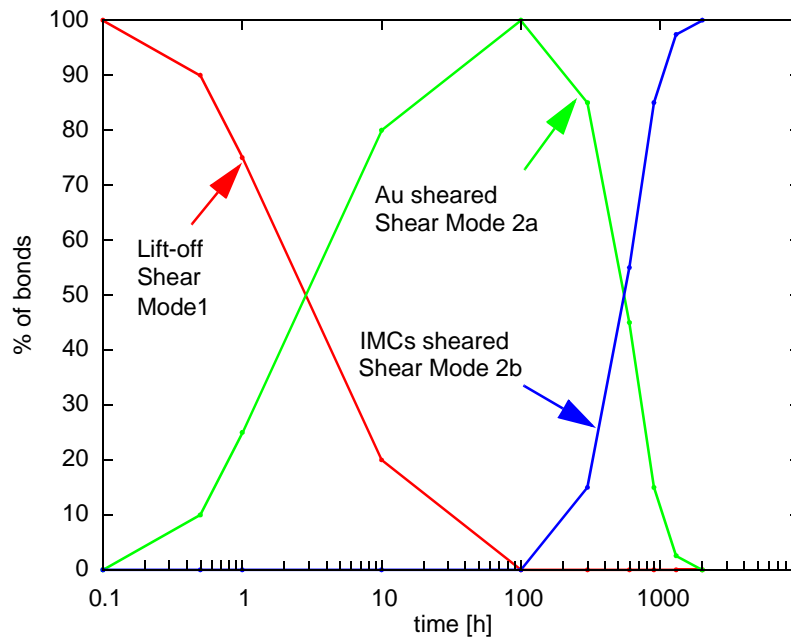
Fig. 60 Shear failure modes vs. time. Unaged bonds fail predominantly by lift-off. Bonds aged between ~ 2 and 300 hours fail in the Au. Bonds aged > 300h fail at the interface between Au and IMCs.

7.1. Factors Distorting R_C Signal

In [4], R_C measured for a 60 µm ball bond on a 70 µm pad is approximately 2 mΩ at 50 ºC. When R_C is measured for bonds on individual pads, only the bond interface resistance is measured as
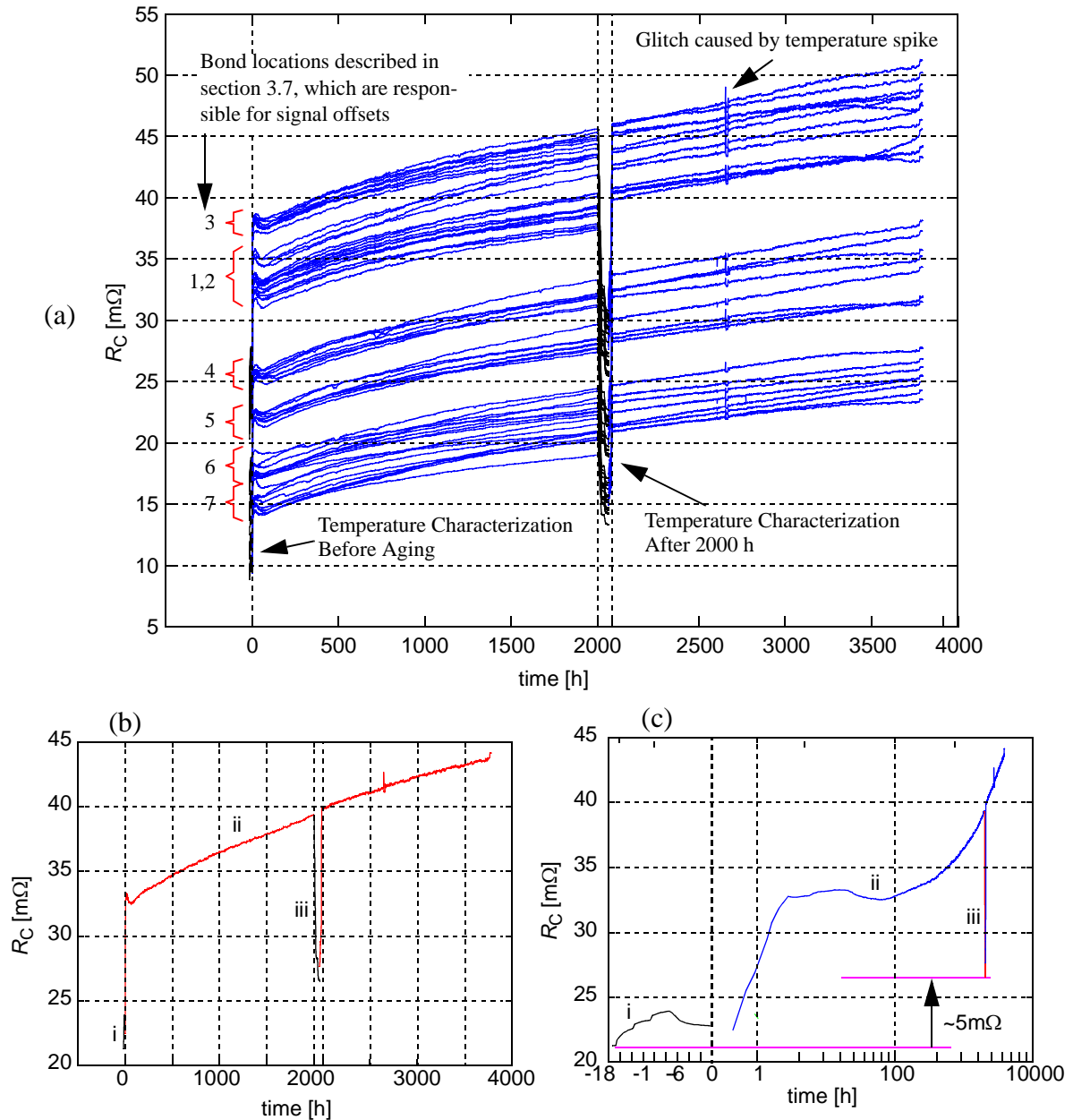
Fig. 61 (a) All R_C measurements during aging. (b) Sample measurement on linear scale including temperature characterization conducted before and after aging (c) Sample measurement on logarithmic time scale. (i) Pre-aging R_C characterization (ii) Aging (iii) Post-aging R_C characterization. (iv) Continued aging after 2000 h experiment is finished. At room temperature after high temperature storage, R_C has experienced a permanent increase.

shown in Fig. 62 a and b. In the present experiment, R_C is measured for bonds on a large thin pad whose area greatly exceeds the interfacial bond area and whose square resistance is greater than the bond resistance. The inclusion of this extra pad resistance as shown in Fig. 62 c provides each bond with a unique, high offset which depends on the bonds' proximity to the 4-wire pad connections. This is explained in more detail in Appendix C.

The resistance of an empty pad is found to decrease about 0.5 mΩ over the first 160 h of aging as described in Appendix C due to grain recovery. The metal anneals and dislocations which hinder electron movement are eliminated, resulting in the resistance decrease. As only a fraction of the pad resistance is included in each R_C measurement, this effect is only partially responsible for the initial R_C drop observed, and does not affect the R_C increase experienced after about 80 h in all bonds.
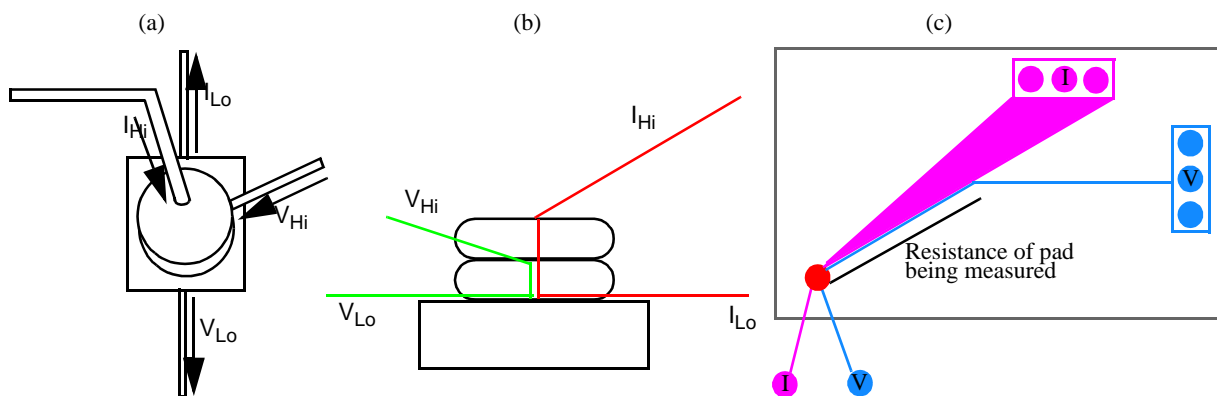
Fig. 62 (a, b) Contact resistance measured from a bond on small bond pad. All of the voltage drop occurs at the wire bond. (c) Contact resistance measured from bond on large rectangular pad used in this experiment. Part of the pad resistance is incorporated into the measurement.

7.2. Average R_C Signal

For all bonds, the times at which the first resistance peak (average occurrence at 16.2 ± 3.9 h),

and first resistance minimum (average occurrence at 58.7 ± 14 h) are calculated, and plotted

along with standard deviations in Fig. 63.

7.3. Initial R_C Decrease

Mechanisms causing R_C decrease are already in effect before the first resistance peak at 16.2 h.

The thermal coefficient of resistance (TCR) for each bond location is calculated from an initial

temperature characterization where R_C is measured for the bonds at 30, 47, 56, and 65 °C (The full

test is explained in Appendix C). The resistance predicted by the TCR is found to be higher than

the actual measured resistance as shown in Fig. 64. This is likely due to pad recovery.
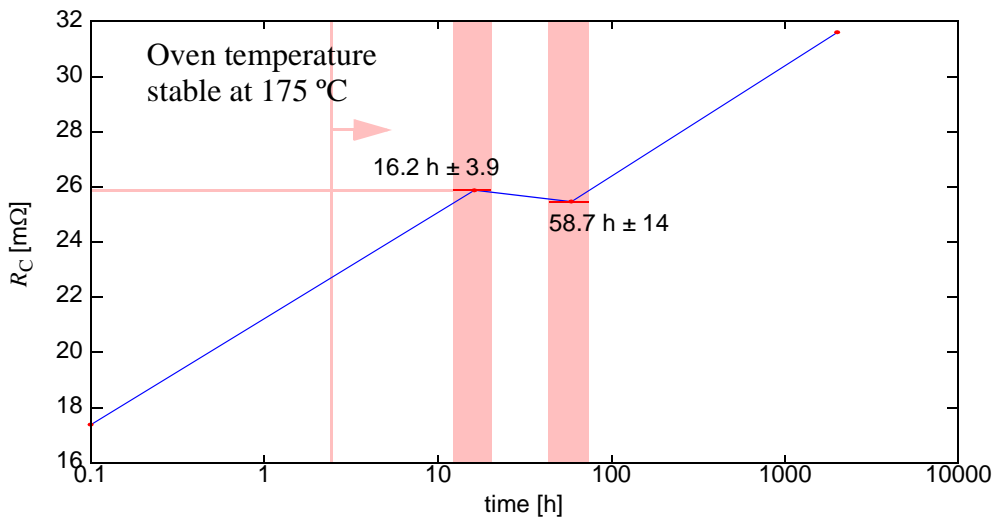
Fig. 63 Average contact resistance for all bond locations. Standard deviations of maximum and minimum R_C which characterize the R_C dip experienced near the start of aging are highlighted. Standard deviations of resistance are not included due to pad effects.

8. Stress Sensor Results

Figure 65 a plots the stress signal over time for all 82 bonds and 8 reference pads. Room temperature offsets, S_O, are removed for all original stress signals, S_{orig}, so that all sensors have a signal $S = S_{orig} - S_O$ that is 0 mV/V at their initial room temperature state (30 ℃). Figures 65 b and c plot S for one typical sample bond, and one reference pad. To more clearly see variations between bonds, all signals from one chip are plotted in Fig. 66. As can be seen in Figs. 65 and 66, after an initial signal decrease caused by thermal expansion mismatch as a result of the temperature increase (wire and pad expand more than Si chip), the stress signal experiences a local minimum and then increases for approximately 6 h. This is followed by a period of relative constant signal with little further signal changes until approximately 56 h. At this point, the stress signal once
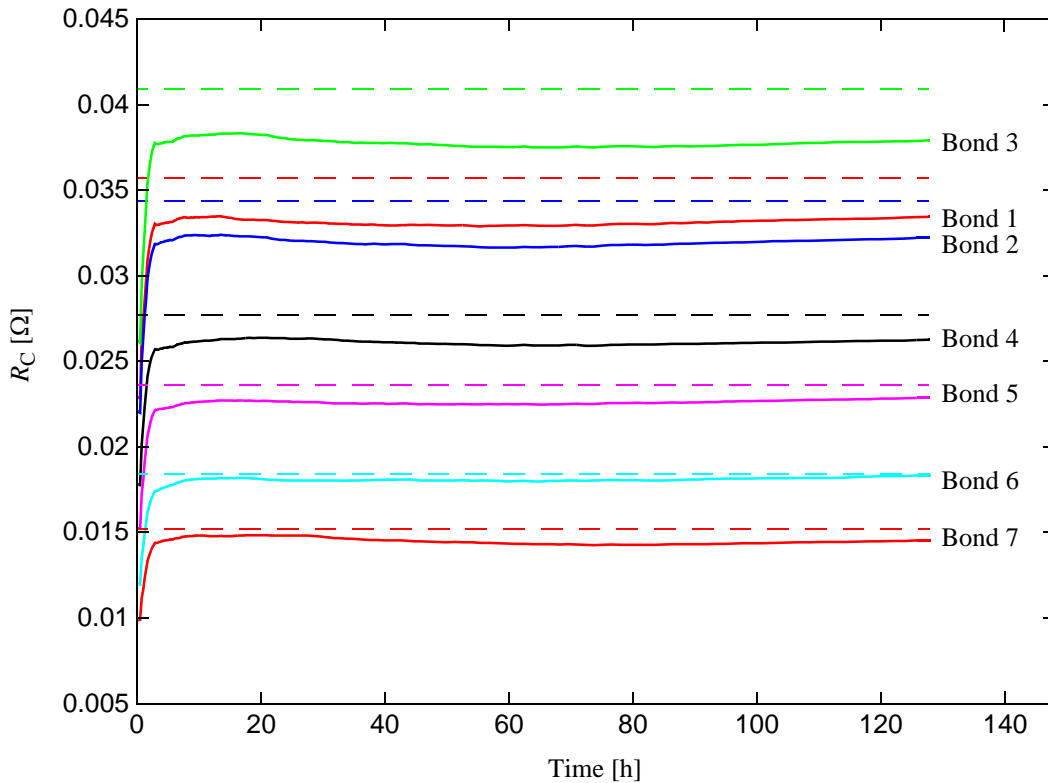
Fig. 64 Experimentally observed R_C vs. TCR predicted resistance. Horizontal dashed lines represent the TCR predicted resistance. Bold solid lines are experimentally observed resistances during temperature increase.

again increases until approximately 221 h. After 221 hours, the stress signal decreases strongly

for the rest of the experiment.
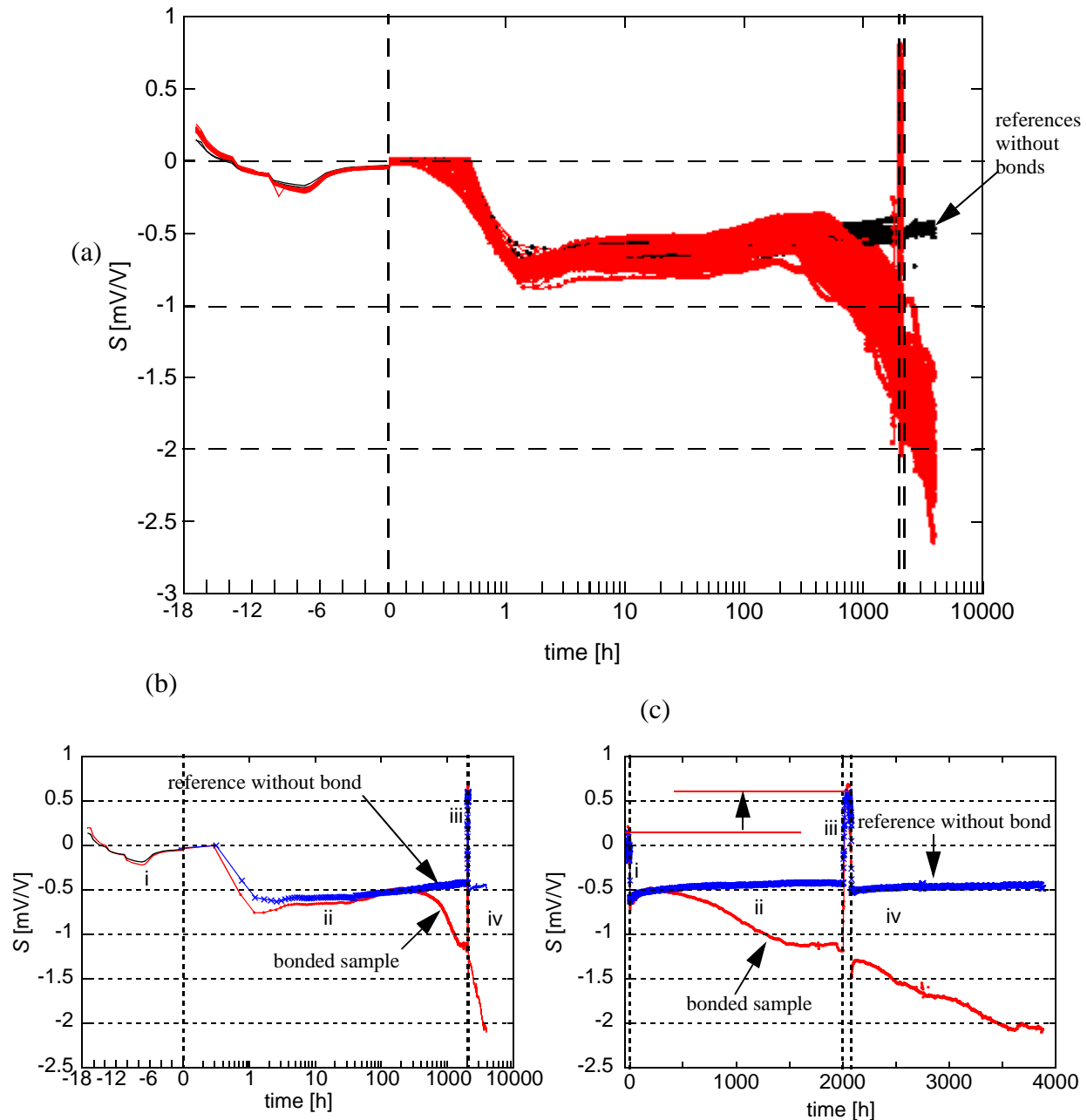
Fig. 65 (a) All sensor measurements during aging (b) Sample measurement on logarithmic time scale (c) Sample measurement on linear time scale. (i) Pre-aging stress signal characterization (ii) Aging (iii) Post-aging temperature characterization. At room temperature, there is a permanent signal increase after aging. (iv) Continued aging after the 2000h experiment has finished.

8.1. Average Sensor Response to Aging

An average sensor signal is constructed from all measured signals by identifying times of pronounced sensor signal changes as are highlighted in Fig. 67, and finding the average occurrences of these changes. As defined in Fig. 67, the maxima and minima are found by sorting the sensor readings to find the lowest point under 10 h (point 1), the lowest point after 10 h (point 6) and the highest point after 10 h (point 4). The point at which the first tensile stress increase finishes (point 2) is defined as the farthest point on the stress curve from the line joining points 1 and 4. The inflection point marking the beginning of the second tensile strength increase is found where the distance between the stress curve and the line joining points 2 and 4 is maximized. Point 5 is defined as the location on the sensor signal curve where the distance from the line joining points 2 and 6 is maximized. In some bonds, there is a large plateau after point 4 before the stress signal
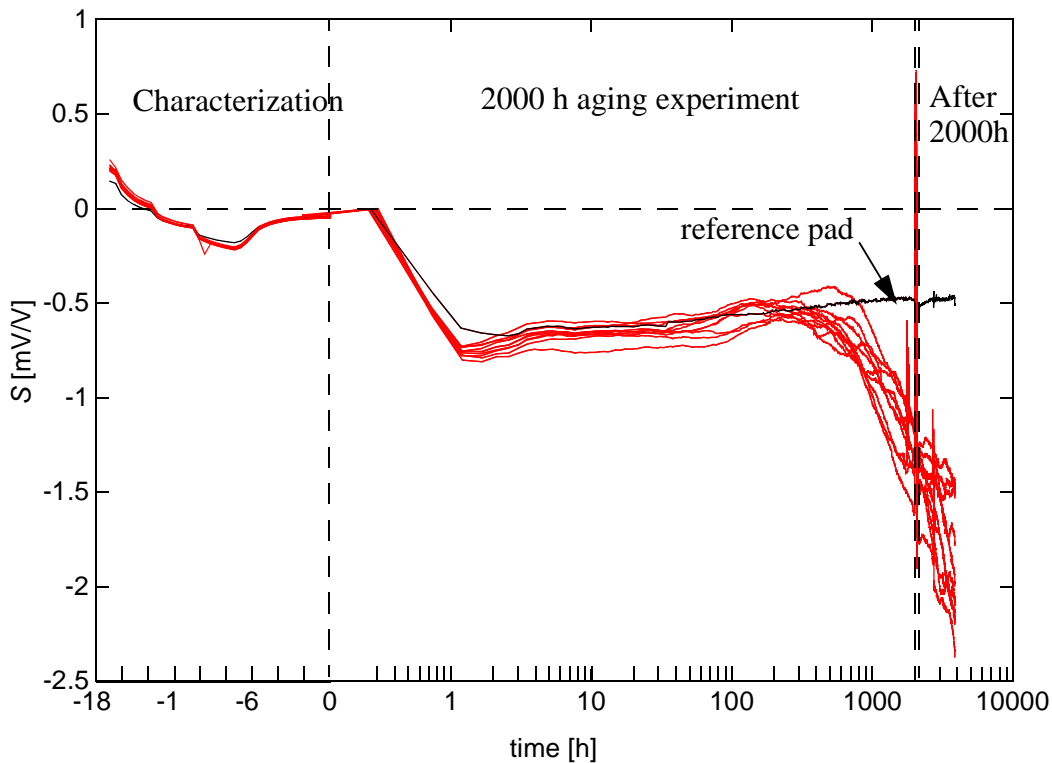
Fig. 66 All sensor signals from one test chip

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drops rapidly. In all bonds, the start of this rapid drop is defined by point 5. At each point of interest, the average time of occurrence and average stress signal are calculated. These values are shown in Table. 8 and plotted in Fig. 68. Standard deviations for *S* and time of each point are plotted as crosshairs at each point.

8.2. Sensor Characterizations Before and After HTS

The stress signal is measured at 30ºC before and after aging. For bonds, it is observed that *S* is 1.03 ± 0.39 mV/V higher after aging, and for reference pads, *S* is 0.928 ± 0.29 mV/V higher. A t-test shows that there is no significant difference in offset increases between sensors at bonded and unbonded pads. This increases indicates a net volume reduction and a net tensile stress experienced.
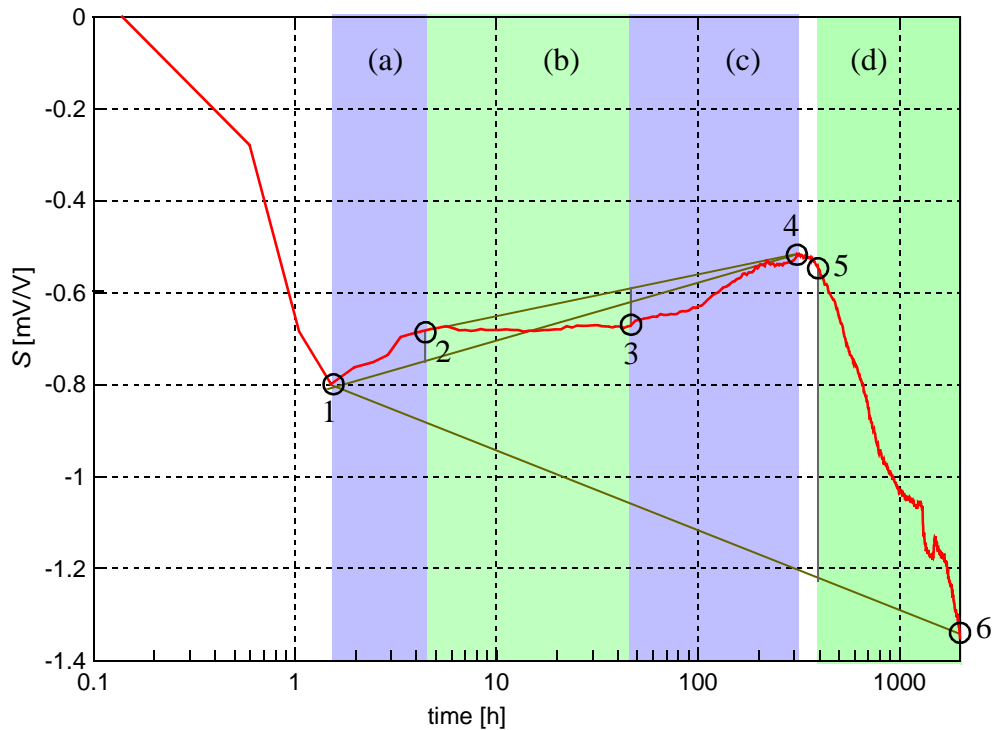
Fig. 67 Key points in stress signal profile. (1) First minimum (2) End of first IMC growth (3) Inflection point where second IMC growth begins. (4) Absolute maximum tensile stress. (5) Drop-off point. (6) Absolute minimum

A temperature characterization of the stress sensors is conducted before and after the aging exper-

iment. Before the experiment is conducted, S is measured at temperatures of 30, 47, 56, and 65 ℃.

The relationship between S and temperature (T) is calculated using the average linear fit equation
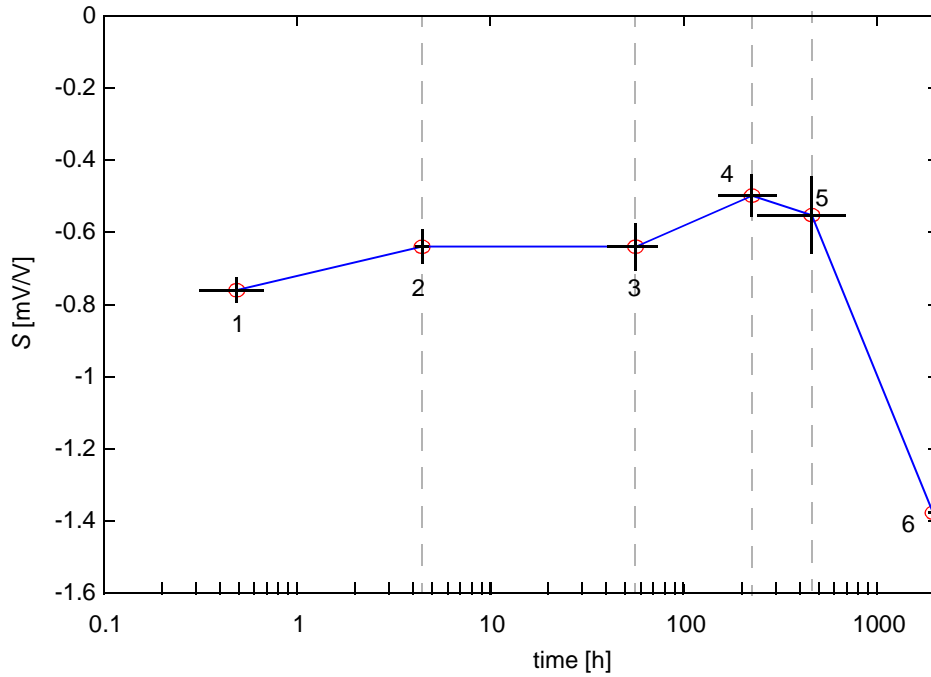
Fig. 68 Stress signal, S, vs. lateral IMC growth. The sensor signal curve is plotted using average values at key points 1-6.

Table 8: Average times and values of key signal changes

Point of interest	Time of occurrence (h)	Outliers (% of measurements)	Sensor signal, S (mV/V)	Outliers (% of measurements)
1	1.49 ± 0.17	3.6	-0.76 ± 0.032	1.2
2	5.44 ± 2.8	2.4	-0.639 ± 0.044	2.4
3	57.6 ± 16	2.4	-0.634 ± 0.056	3.6
4	221 ± 66	3.6	-0.498 ± 0.054	9.7
5	462 ± 210	8.5	-0.554 ± 0.1	12.2
6	1950 ± 77	0	-1.38 ± 0.18	6.1

as calculated from all bonds. Figure 69 shows a typical *S* profile during a temperature ramp-up, and the corresponding linear relationship. After the experiment, the signals are measured at temperatures of 29, 50, 58, 67, and 72 °C. Again, the temperature dependence of *S* is calculated. Average signal temperature relationships before and after bonding are plotted in Fig. 70 and listed in Table 9. After aging, the sensor temperature dependence has increased for both reference pads and
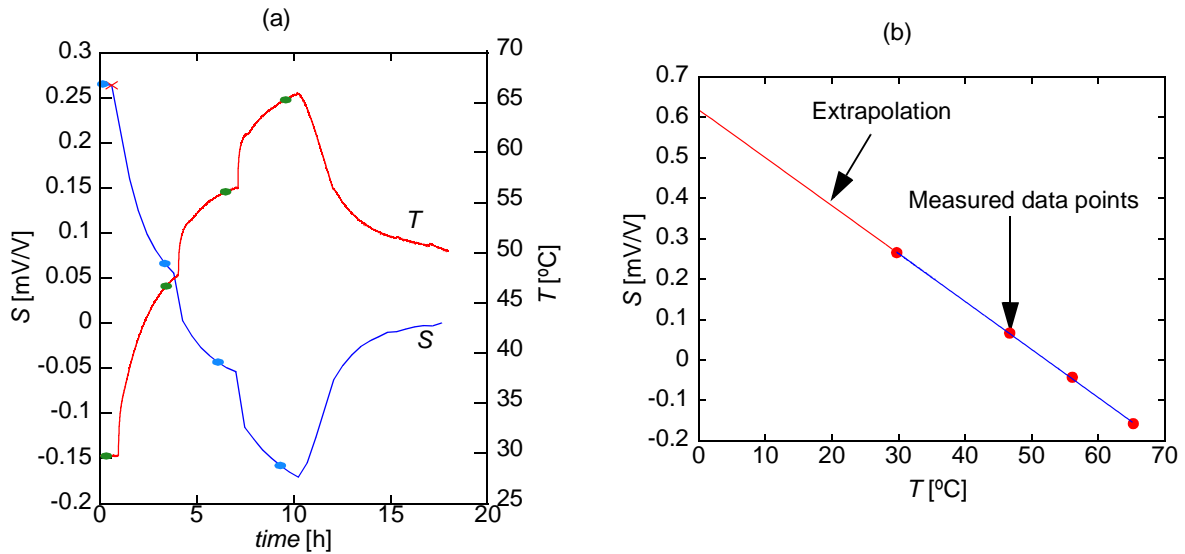
Fig. 69 Typical temperature ramp-up with measured *S*. (a) Temperature profile and *S* profile plotted together. Data points are taken at each temperature plateau. (b) *S* plotted against *T* using a linear fit.

Table 9: Temperature characterization of sensors

	Pre-HTS characterization at t = 0 h	Post-HTS characterization at t = 2000 h
Temperature characterization for reference pad (mV/V/°C)	$-0.00884 \pm 6.6 \times 10^{-5}$	-0.013 ± 0.0061
Number of outliers	0	0
Temperature characterization for bonds (mV/V/°C)	-0.0117 ± 0.00033	-0.0169 ± 0.0018
Number of outliers	2 (2.4% of bonds)	2 (2.4% of bonds)

pads with bonds. The increased CTE of the pads is likely due to removal of dislocations during

the annealing process, allowing for more expansion and contraction.

8.3. Stresses Measured After 2000 h

Although the study concludes after 2000 h, four chips are kept in the oven to observe stresses

experienced after more aging at the same temperature as shown in Figs. 65, 66. For pads with ball

bonds, *S* continues to decrease.
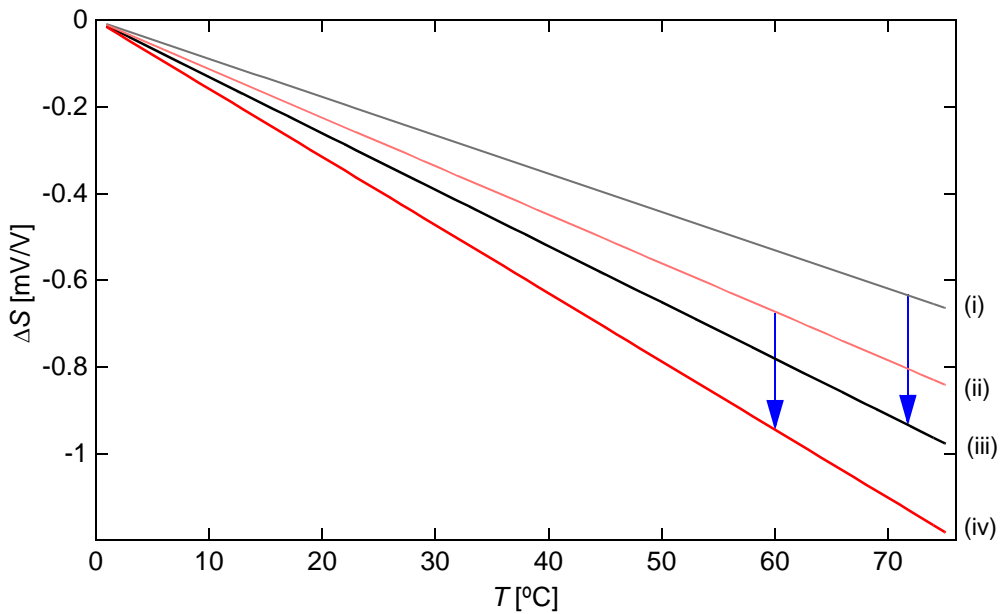
Fig. 70 Average *S*(*T*) before and after aging for reference pads, and bonded pads. (i) Reference pads as received (ii) Ball bond - as bonded. (iii) Reference pad post HTS (iv) Ball bond post HTS

9. Discussion

9.1. The Evolution of Bond Aging

Microstructural changes which are accelerated by HTS result in changes to SS, R_C, and S. By relating changes of these measurements to the evolution of the bond interface, methods are found to evaluate bond quality and predict shear strength changes from non destructive measurements alone.

The HTS history is divided into 5 stages:

Stage (a) 0 - 2 h: Temperature increases to 175ºC

Stage (b) 2 - 5.5 h: Initial interdiffusion and complete conversion of all top Al pad layer into IMCs.

Stage (c) 5.5 - 58 h: Growth of IMC layer

Stage (d) 58 - 300 h: Penetration of DBL and conversion of lower Al layer into IMCs.

Stage (e) 300 - 2000 h: Lateral IMC growth while the region under the bond is relatively static.

All measurements taken are plotted together in Figs. 71 i and ii. Stages are highlighted for clarity.

9.1.1. Stage (a)

The temperature increase is shown in Fig. 72. It takes 1.1 h for the temperature to reach 90% of its final value, and 2 h for the temperature to reach 175 ºC. During stage (a), two mechanisms are affecting measurements: the temperature change and IMC formation. As the temperature increases, the Au and Al expand more than the Si and SiO_2 due to their high coefficients of thermal expansion (CTE) listed in Table 10. The temperature increase also causes an increased electrical resistance due to the temperature dependence of material resistance [4]. Calculated temperature coefficients of resistance (TCRs) of the bonds are found in Appendix C. Diffusion

and IMC formation accelerate as the temperature increases [11]. The IMCs which form at the interface during this time, (Au_8Al_3, Au_2Al, and Au_4Al) all have high densities and result in volume reduction of 2-3%, as listed in Fig. 13.
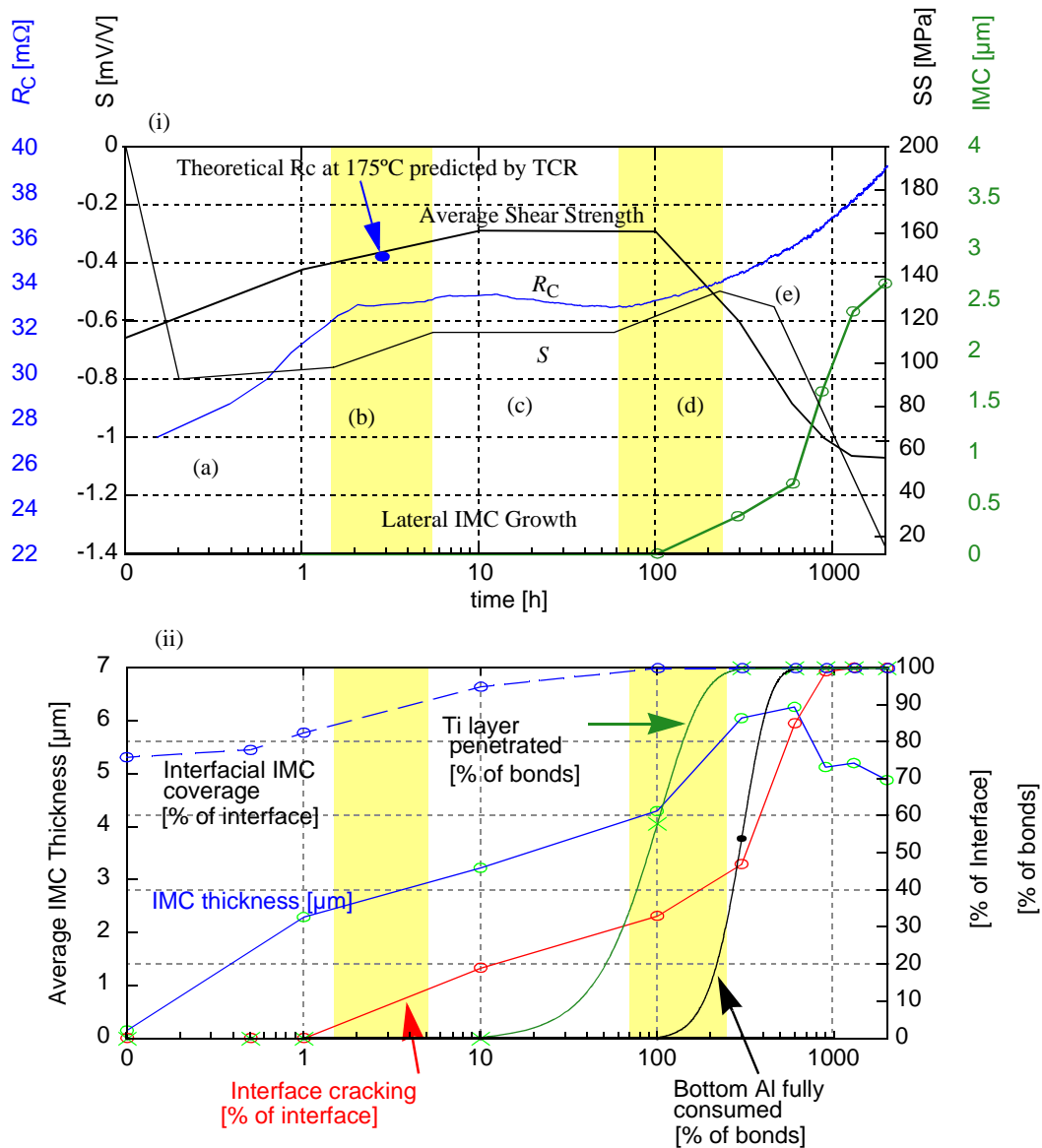
Fig. 71 Destructive and non-destructive measurements. (i) Average shear strength, average lateral IMC growth, average S and typical R_C measurements from different samples. (ii) Average IMC thickness, interfacial IMC coverage, interfacial cracking/oxidation, and times at which diffusion barrier is penetrated and bottom Al layer is fully consumed.

The shear strength increases due to the formation of IMCs at the interface which improve the bonding strength. The stress signal drops indicating a compressive stress caused by the CTE mismatch of chip materials. During the last half hour of this stage, when the temperature is increasing
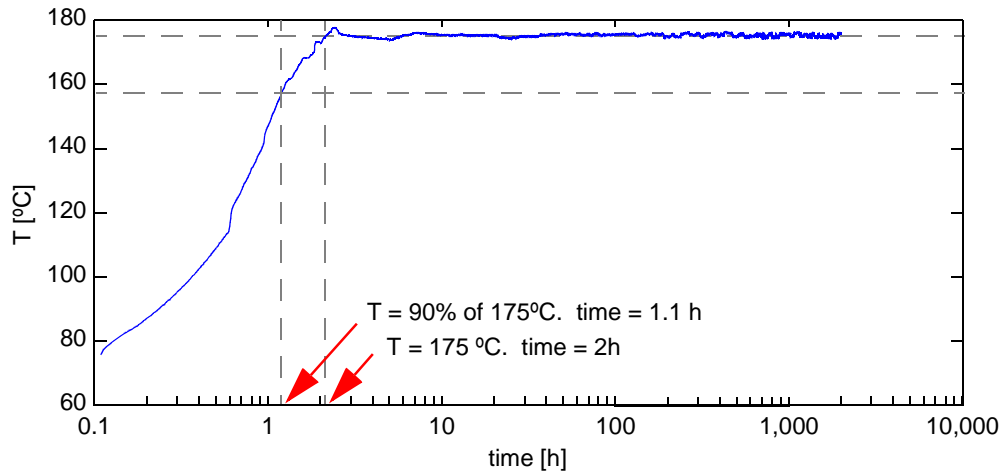
Fig. 72 Temperature profile during aging

Table 10: Material Properties

Material	Linear Coefficient of Thermal Expansion ($\times 10^{-6}K^{-1}$) [30]	Resistivity ($\Omega \cdot cm$) [30]
Au	14.2	2.3
Al	23.1	3.2
Si	2.6	
SiO_2	0.5	
$AuAl_2$	9.4	7.9
AuAl	12	12.4
Au_2Al	13	13.1
Au_8Al_3	14	25.5
Au_4Al	12	37.5

from 110 ℃ to 175 ℃, the tensile stresses caused by growing IMCs outweigh the stress caused by CTE mismatch and the stress signal reaches a local minimum and begins to increase.

The contact resistance in this stage increases with temperature due to the TCR. However, as seen in Fig. 64, R_C does not increase to the level predicted by TCR due to an increase of interfacial bond area and recovery in the Al pad reducing the overall resistance.

9.1.2. Stage (b)

As IMCs consume more of the top Al pad layer down to the DBL, the IMC thickness increases, and the interfacial coverage increases to almost 90%. IMCs grow around the voids formed at the Au-IMC interface during bonding as shown in Fig. 73 a. These initial voids do not grow upon fur-

Fig. 73 Stage b. (a) Voids at Au-IMC interface after 10h. (b) Cross section of sheared bond. Shearing occurs through Au and ball does not lift off. (c) Formation of low-volume IMCs creates a tensile stress felt by the sensor elements.

ther HTS and IMC growth and are distinct from the voids/oxide stages which later form due to solid state reactions, as anticipated by Karpel [17]. IMCs have also grown vertically to the Au ball and Al pad.
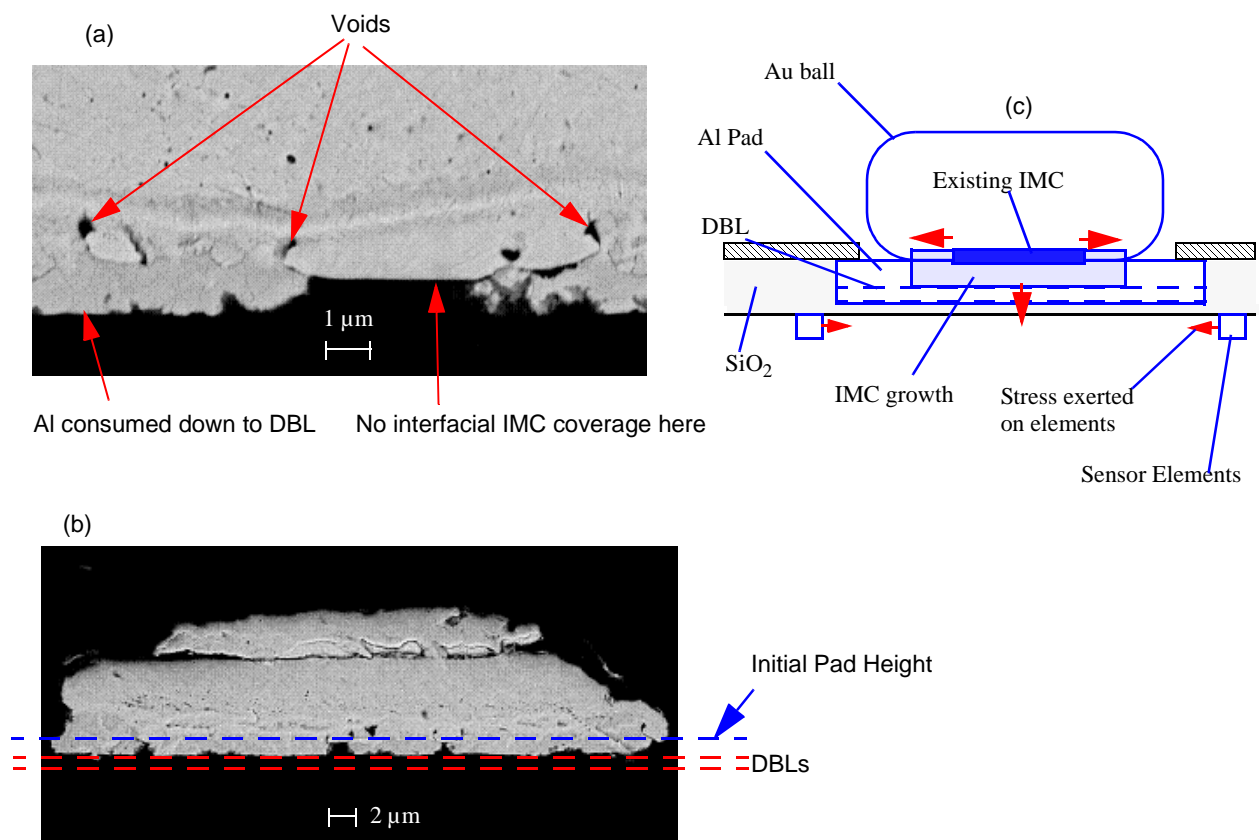
The continued consolidation of the interfacial area results in increased shear strength, as the bonds now shear through the Au layer and do not lift off the interface as shown in Fig. 73 b. The first layer of Al pad is observed through cross sectional micrographs to be almost entirely consumed between 1 and 10 h of HTS. The sensor signal increases until on average 5.44 h, indicating tensile stress caused by the formation of the high density IMCs (Fig. 73 c). Contact resistance also increases on average during this interval, although at a greatly reduced rate. This increase is likely caused by the increased thickness of the IMC stage, as IMCs have higher resistivity than pure Au or Al as listed in Table 10.

9.1.3. Stage (c)

After 5.5 h, the bonding interface is still stronger than the Au ball, and shear strength results remain the same. The tensile stress caused by conversion of the remaining Al to IMC and vertical growth of IMCs into the Au ball is balanced by the compressive stress of AuAl formation at the ball periphery and oxidation of the IMCs which starts in this stage. As a result, S does not change significantly. Conversion of Au ball into IMCs is not expected to affect S as much as downward or lateral growth, as it produces stress on a plane farther from the sensors as illustrated in Fig. 74 a and b. During stage (c), R_C actually decreases on average. This decrease is caused by a combination of the 2 resistances being measured by R_C: the actual contact resistance, R_{bond}, and the resistance of the Al substrate, R_{pad} (See Section 7.1). From Appendix C, it is observed that R_{pad} drops for the first 140 h of aging. R_{bond} is a function of material resistivity, ρ, length, L, and cross sectional area, A, as given by:

$$R_{bond} = \rho \cdot (L/A) \tag{6}$$

Examining bonds at 10 and 100 h shows that the thickness of IMCs has increased. However, the lateral coverage of IMCs, both at the ball periphery and directly under the ball (where IMC formation patches up unbonded base metals) has proceeded at a faster rate. Measuring the ratio of L/A for typical bonds (Figs. 75 a and b) at 10 and 100 h yields ratios of 0.0013 and 0.0008 μm^{-1} respectively, indicating that the increase of R_{bond}, if any, is too small to offset the drop in R_{pad}. Therefore, during stage (c), R_C drops while the interface is consolidated.
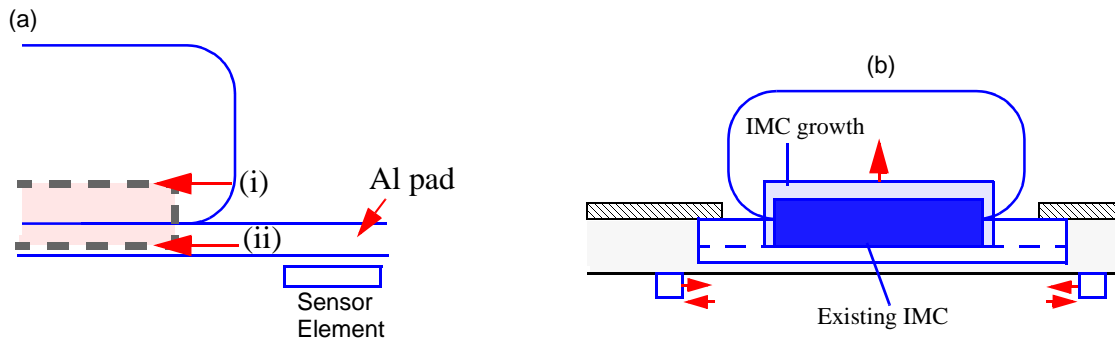
Fig. 74 Stage c. (a) Tensile forces at top of IMC stage (i) are detected by the sensors less than forces at the bottom of the IMC stage (ii) due to their greater distance from the sensing elements. (b) Small tensile forces from vertical IMC growth and small compressive forces from slight lateral IMC growth result in no net force felt by sensors.
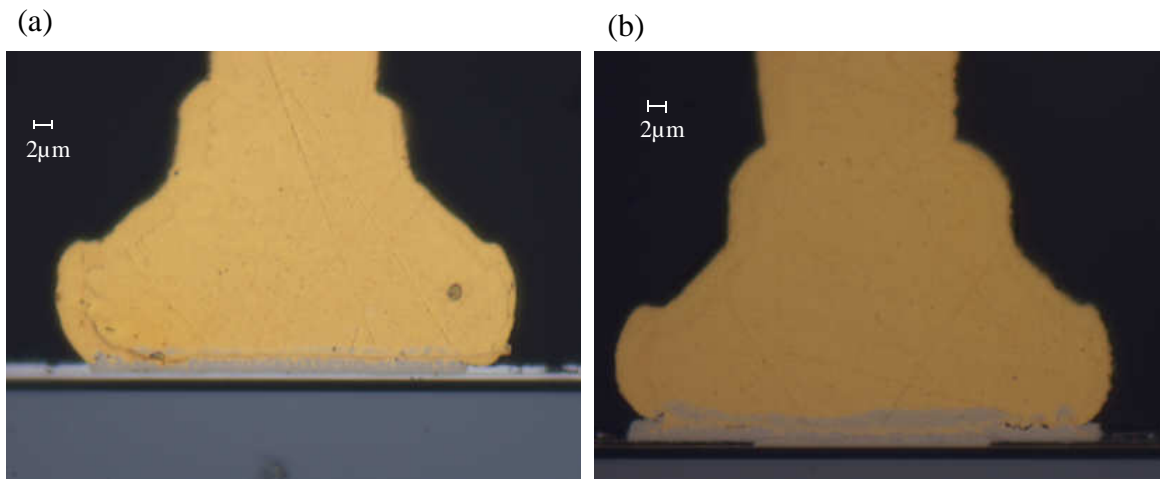
Fig. 75 Typical cross sections. (a) Bond aged 10 h. IMC thickness (L) = 2.07 μm. Diameter of IMCs = 45.5 μm. Ratio of L/A = 0.00127μm^{-1}. (b) Bond aged 100 h. IMC thickness = 2.07μm. Diameter of IMC coverage = 57.5 μm. L/A = 0.00078 μm^{-1}.

9.1.4. Stage (d)

In micrographs taken at 100 h, IMC growth penetrates the DBL in the average bond, providing a large new volume of Al for further IMC growth. In this stage of time, three mechanisms are at work: Au diffuses through the IMC layer and along the DBL converting the Al into IMCs and possibly leaving Kirkendall voids behind due to excessive diffusion; the Au_4Al layer at the IMC/ball interface is oxidized resulting in volume expansion and decreased electrical conductivity; lateral low density IMCs form adjacent to the ball which also result in volume expansion.

The shear strength drops in this stage due to the disintegrating interface. Oxide which forms as shown in Fig. 76 a weakly adheres to Au [3], and reduces strength. In this stage, S increases dramatically due to the rapid conversion of Al into higher density IMCs. Although lateral IMC growth is accelerating in this stage and Au_4Al is oxidizing, causing compressive stress, IMC formation at the pure Al layer occurs very rapidly and tensile stresses dominate. R_C has bottomed out and increases after 58 h due to IMC, oxide and void formation which are observed to increase for the remainder of the experiment.
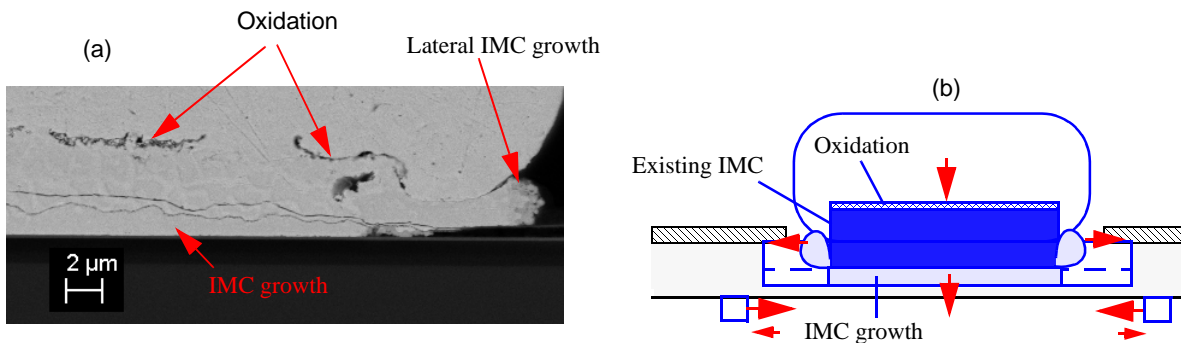

Fig. 76 Stage d. (a) Micrograph showing start of oxidation, and IMC growth. This interfacial oxidation increases bond electrical resistance and decreases shear strength. (b) Tensile forces caused by downwards IMC growth greatly exceed compressive forces caused by oxide formation or lateral IMC growth.

9.1.5. Stage (e)

After the Al under the pad is completely consumed by IMCs, two major phenomena occur for the remainder of observed aging time: the Au_4Al layer at the top of the IMCs is further oxidized causing the overall IMC thickness to decrease (IMC thickness chart in Fig. 71 ii) and IMCs grow lateral to the bond as Au diffuses out to consume the Al pad shown in Fig. 77 b. Shear strength decreases as interfacial oxide forms. After 900 h, an oxide layer is observed to cover the entire bond interface as seen in Fig. 54 a. As the brittle oxide layer cannot spread laterally any further (although it does continue to grow vertically into the Au_4Al), the shear strength decrease greatly slows (average shear strength decrease of 65 to 55.3 MPa between 900 and 2000 h).

As the two major phenomena both result in density reduction and volumetric expansion, S is observed to greatly decrease in this stage indicating high compressive stress at sensor elements. The drop in S appears particularly excessive because the lateral IMCs are located much closer to the sensors than the IMCs under the bond (Fig. 77 b).

R_C continues to increase for the duration of the experiment. This is due to continued oxidation of the Au_4Al and void formation, and may also be due to the depletion of Al around the bond as seen in Fig. 56 c.
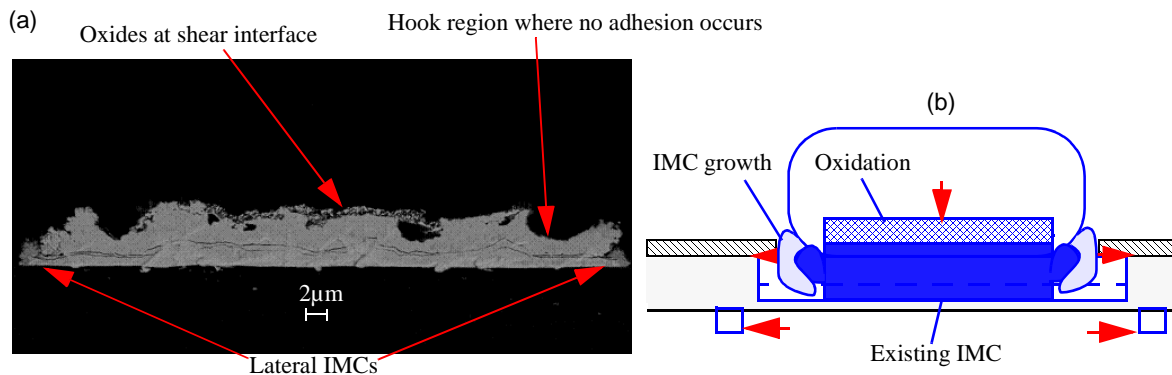

Fig. 77 Stage e. (a) Cross section of sheared bond shows shearing interface at oxide layer verifying that low shear strength is due to oxidation. (b) Compressive stresses are generated by oxidation and lateral IMC growth.

9.2. Evidence of Contact Resistance Increase Primarily Due to Oxide Formation

Harman [1] suggests that R_C increases in the ~8 mΩ range during the first thousand hours is due to IMC formation, as IMCs have higher resistivity than base metals (See Table 10). In this experiment, the resistance drops when the first Al layer is converted to IMCs because the measured R_C decrease caused by a combination of pad resistance decrease and increased bonded area, outweighs the resistance increase caused by IMC formation.

During conversion of the second Al layer into IMCs, R_C increase caused by oxidation of Au_4Al is significantly greater than R_C increase caused by IMC growth. At the end of stage (d), once the entire pad is converted to IMCs and vertical IMC growth is impeded by an oxide layer at the Au ball and by a DBL at the bottom of the pad, IMC expansion stops, and IMC formation can no longer increase R_C. If no oxidation were occurring, it is expected that the rate of R_C increase would abruptly slow after stage (d). From Fig. 71 a, this is clearly not the case, as R_C continues to increase monotonically with no clear features or abrupt slope changes during stage (e). As the other major mechanisms at work to increase R_C are the oxidation of Au_4Al and lateral IMC growth which continue after IMC growth stops, it is concluded that these mechanisms are primarily responsible for the increase of R_C.

When S changes from tensile to compressive, indicating the end of IMC growth under the ball, yet R_C continues to increase at a relatively constant rate, it is concluded that this increase is driven primarily by oxidation.

9.3. Sensor Signal and Contact Resistance as Possible Tools for Predicting Bond Failure

9.3.1. Relation of Stress Sensor Signal to Changes at Microstructure

When S increases, tensile forces are observed at sensing elements which, during aging, are caused by formation of high density IMCs directly under the bond (Au_4Al, Au_8Al_3, and Au_2Al). When S

drops, the sensing elements experience compressive stress due to either growth of low density lateral IMCs or oxidation of Au_4Al. When S is stable for long periods of time, IMCs may be growing vertically into the Au ball as observed between 6 and 58 h, but no significant changes are happening at or below the bond interface. Short periods of S stability occur when 2 counteracting mechanisms are at work, e.g. formation of high density IMCs at the bond interface and formation of low density IMCs at the periphery. However, these periods (in stage (a) and at the transition between stages (d) and (e) as shown in Fig. 71) are very brief.

9.3.2. Relation to Shear Strength

Generally, when the bond is not degrading, S is constant (stable), indicating a static interface with little microstructural change. A stable S indicates no oxidation and low rates of lateral and interfacial IMC growth. As the bond interface weakens and SS decreases, the rate of R_C change increases and S changes. The increase in R_C is caused by lateral IMC growth, vertical IMC growth and oxidation. The changes in S are caused by the same mechanisms. When S is increasing, vertical IMC growth dominates. When S decreases, lateral IMC growth and oxidation dominate. Vertical IMC growth decreases SS by forming Kirkendall voids as base metals diffuse for IMC formation, and by crack formation due to stress induced by volume change [17]. Oxidation reduces SS by lower adhesion of the oxide layer [3], and by possible stress crack formation. Examination of shear interfaces in Section 6.2 and the cross sections shown in Figs. 73 and 77 verify that weakened bonds experience failure at the top of the brittle oxide layer as anticipated.

Through S and R_C measurement, the onset of strength loss may be detected in this way. However, the plateauing of shear strength observed when oxide covers the entire interface (Fig. 71 i, 1300 - 2000 h) cannot be observed using the non destructive signals, as the rate of signal change remains constant, not reflecting this plateauing phenomenon.

9.4. Application of Stress Sensors

The stress sensor signals are related to microstructural changes and strength changes which occur and may be used to compare bonds against each other. When observing signals from several bonds, the shape of the signal curve can be automatically analyzed by custom made software, and it can be determined which bonds have higher initial strengths and reliabilities. Microstructural evolution of bonds with high reliability has a longer duration before cracking, voiding and oxidizing and there is slower lateral IMC formation. If bond pads are made from multiple Al layers separated with diffusion barriers, reliable bonds let the diffusion barriers remain intact for as long as possible. It is shown [16] that the most reliable bonds are on the relatively thin pads. Thick pads allow for more IMC formation, more stresses which may lead to cracking and more voids resulting from increased interdiffusion. Penetration by IMC growth of the DBL will result in a thicker pad and reduce reliability. DBLs may be damaged in a rough bonding process, for example Cu bonding processes which require higher impact and bond forces [21]. DBLs may also be penetrated due to rapid diffusion which may be slowed or accelerated depending on wire chemistry. As a result, sensors adjacent to strong bonds experience a quick initial tensile stress increase which has a low magnitude. This indicates that the majority of the interface is welded to the substrate during the bonding process. In a weak bond, the first signal rise is slow and of high magnitude as the islands of bonded material gradually allow interdiffusion to convert a large amount of unbonded base metal to IMCs. In reliable bonds, the sensors exhibit a second tensile stress increase (due to DBL penetration) later than less reliable bonds. Reliable bonds experience less oxidation [3] and less lateral IMC growth [1] for a given aging time, which results in a slower compressive signal drop. As oxidation is delayed and lateral IMC growth is slower, this compressive drop occurs at a later time. The stress change and increased rate of R_C rise which indicate

voiding and shear strength decrease occur later on, and the overall magnitude of R_C increase is expected to be less. If two bonds denoted bond a and bond b are made and monitored producing the outputs shown in Fig. 78, bond b would be recognized as superior, without the need for extensive testing. This tool becomes relevant when many bonds made with different parameters are to be quickly compared.

In an experiment conducted at the University of Waterloo's Center for Advanced Materials Joining (CAMJ), 11 bonds are made with an ESEC 3100 wire bonder at varying ultrasound levels (all other bond parameters are constant), and aged for 300 h at 200 ºC [31]. The stress sensor profiles are reproduced in Fig. 79 a. Generally, it is expected that bonds made with higher ultrasound have better initial bond quality, and bonds made with exceptionally low ultrasound levels have low initial bond quality and low reliability. From measuring the sensor signals alone, it is evident that the bonds made with higher ultrasound are more similar to bond b in Fig. 78, as the initial tensile stress increase occurs rapidly and reaches a lower magnitude than the low ultrasound samples (Fig. 79 b and c). This is a result of diffusion being able to occur quickly and less Al being available for IMC formation, which indicates that extensive bonding is present before the start of HTS.
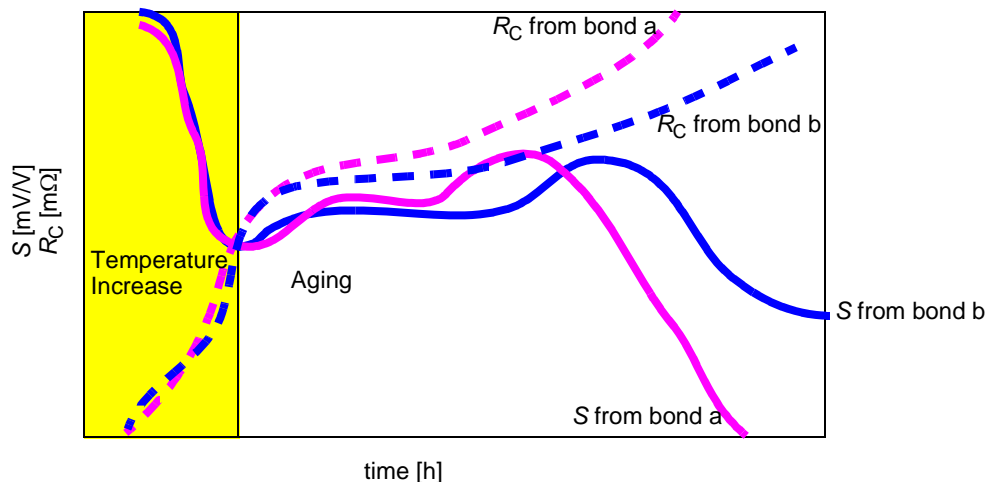

Fig. 78 Example of non-destructive signals for reliable and unreliable bonds

The samples made with low ultrasound can be observed to have lower reliability as they experience prolonged compressive stress, which continues to decrease to relatively high magnitudes after the stress fields around the strong bonds have plateaued.
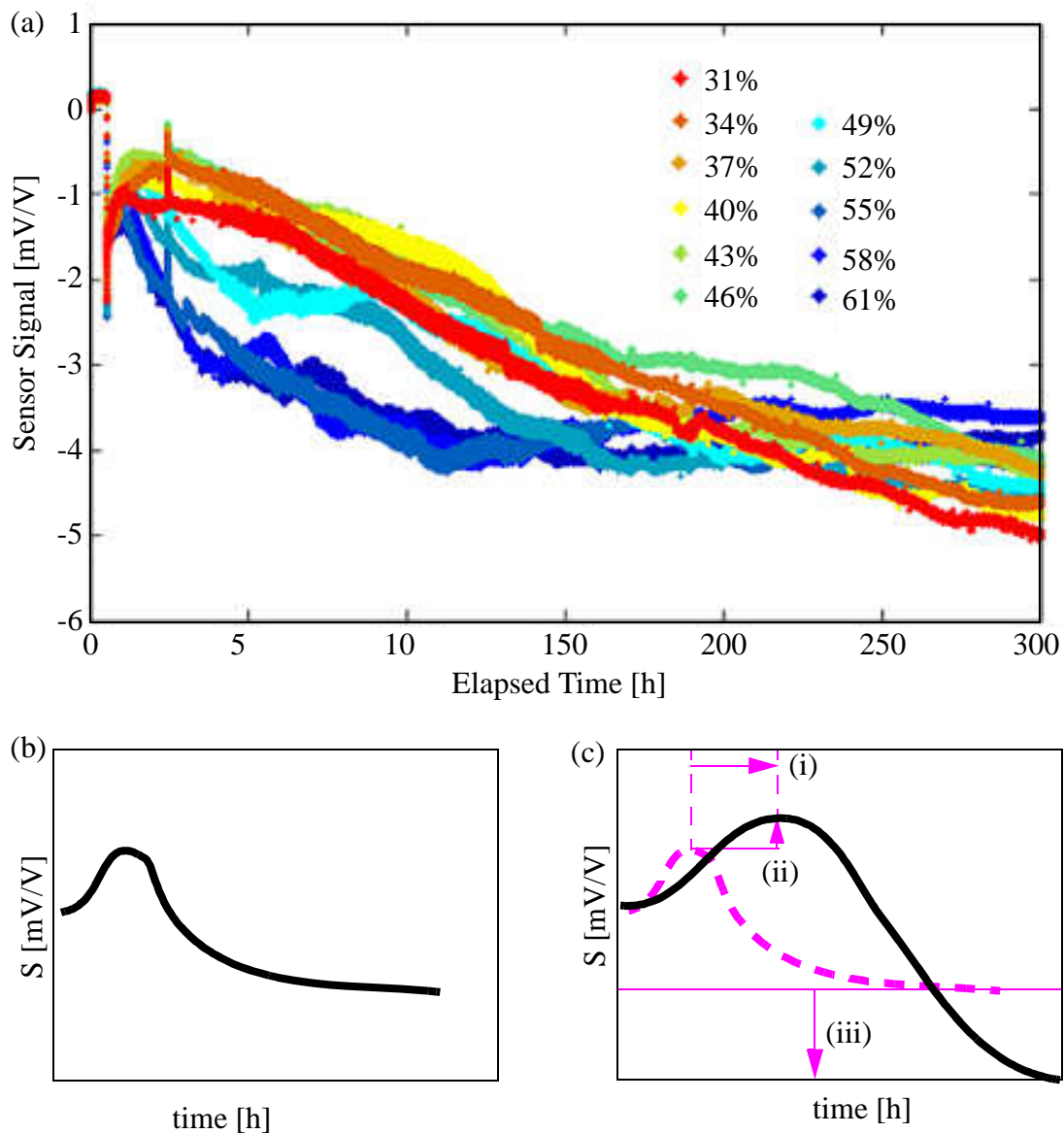

Fig. 79 (a) Bonds made at varying ultrasonic levels expressed as a percentage of maximum transducer amplitude, and aged at 200 ℃ [31]. (b) Typical profile for bond well made at high ultrasound. (c) Typical profile for bond poorly made at low ultrasound. Sensor profile indicates that less adhesion occurred during bonding because (i) Diffusion and IMC formation took more time, (ii) More high density IMC forms during aging which indicates that relatively little IMC must have formed during bonding. Reliability is lower for this bond as S drops much more due to either oxidation or excessive lateral IMC formation.

There is not enough data at this time to correlate the signals directly to standard reliability tests, determining whether bonds pass or fail by monitoring the signals alone, as only one set of identical bonds has been analyzed. In order to directly correlate S to bond shear strength, many sets of bonds made with many sets of parameters would need to be examined.

9.5. Investigation of Additional Potential Correlations

Stress sensor data is analyzed to determine whether any additional correlations exist. For example, in the experiment shown in Fig. 79, bonds with lower US are expected to be weaker and show a peak in S which occurs later. The subsequent compressive force continues for the entire experiment and S reaches lower values than are seen for bonds made with high US. In that experiment, the degree of signal drop could be related to the time of the initial peak, providing a bond quality indicator less than 50 h into the experiment.

For the 2000 h age large sample size experiment, seven parameters shown in Fig. 80 which characterize the S profile are compared to each other to investigate possible correlations. All comparisons are found in Appendix D. No strong correlations are found except for (i) vs. (c), which is irrelevant because (c) comprises the majority of time period (i). Therefore, in this case reliability differences resulting from minor random variations in bond quality cannot be predicted from early S measurements.

10. Chip Design for Future Studies

An upgraded test chip is designed for future non-destructive reliability testing. This test chip has 55 test bond pads which are equipped for S measurement and simultaneous R_C measurement. The chip is also equipped with x and y-force measurements which can be used to monitor bond processes [21], and a resistive temperature detector (RTD) for precise temperature measurement. An on-chip MUX provides for measurements from one specified pad at a time. This chip is shown in Figs. 81 a and b by photograph and design layout, respectively.

Various test structures are included to help troubleshoot. Voltage measurements are available at various locations along the bus to characterize a possible drop in sensing voltage due to resistance
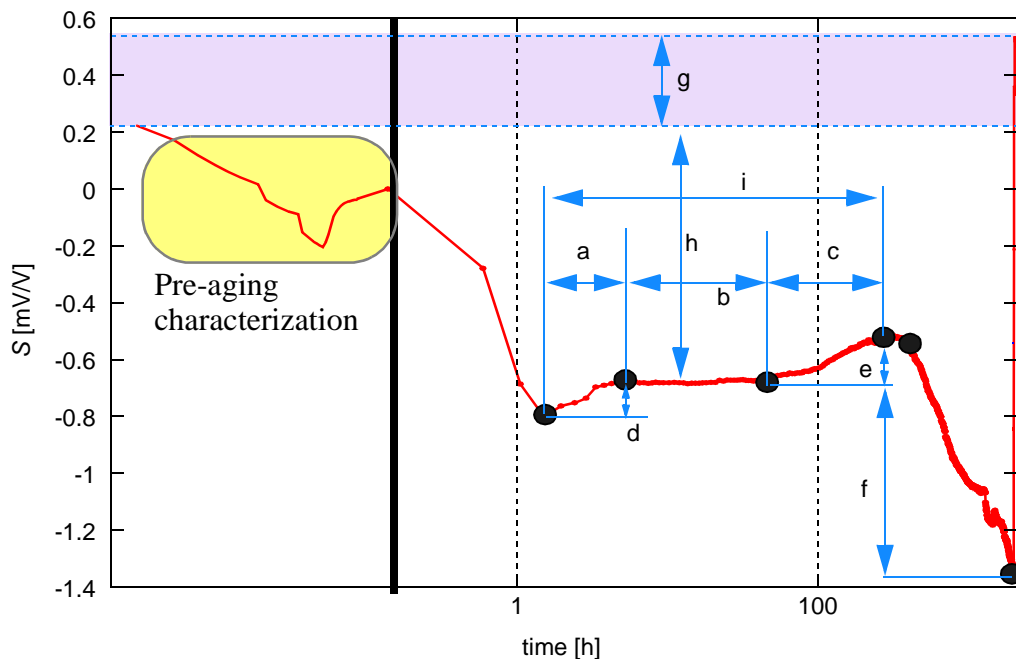

Fig. 80 Parameters used for early indicator correlation test. Parameters are (a) duration of initial tensile stress (b) duration of S plateau (c) duration of second tensile stress (d) magnitude of first S increase (e) magnitude of second S increase (f) magnitude of S decrease (g) change in offset during aging (h) Average signal during the S plateau (i) total time before S peaks

of chip circuitry. Resistance measurements at MUX switches are also provided. Stand-alone x, y, and z direction stress sensors are present for characterization.
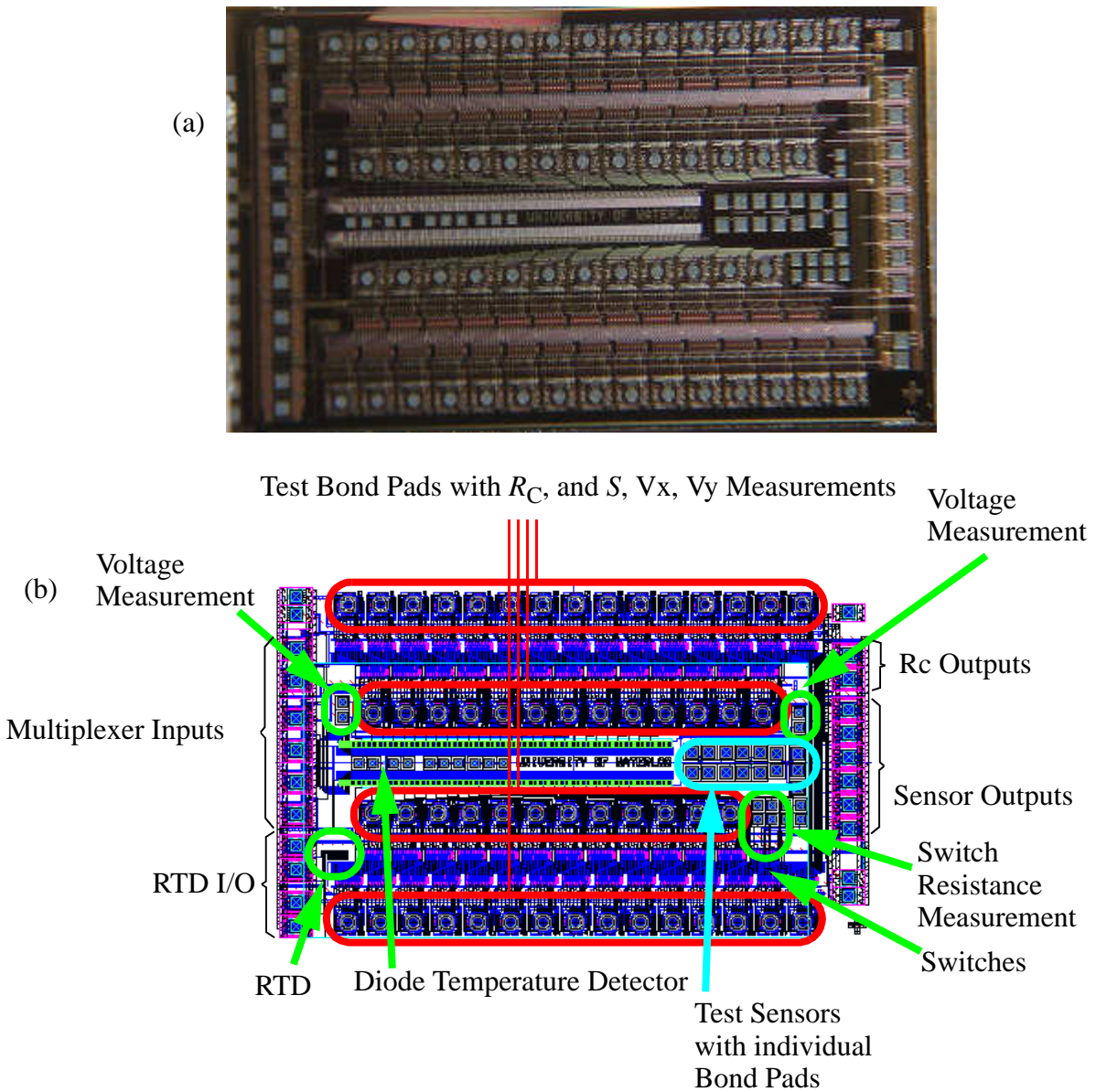

Fig. 81 Upgraded Test Chip. (a) Photograph (b) Design Layout showing chip components

11. Miniaturized Bond Aging System

A miniaturized bond aging system is designed to facilitate future HTS experiments where S and R_C are recorded in real time. For the experiment discussed so far in the thesis, electrical connection between the package and monitoring equipment are located in the oven which may reduce connection reliability and increases the electrical resistance of the auxiliary wire connections. Construction of chip holding rigs and soldering of high temperature wires directly to package connections is time consuming to prepare, especially if multiple devices are tested after each other. To aid in future work, a miniaturized heating system is built which can run on relatively low power and maintains a low temperature at the package pins where electrical connections are located.

11.1. Design

The miniaturized heating system is designed for use with 28-pin CerDIP packages with cavities measuring 1cm or less. Figure 82 shows a schematic of all components in the system. A PC con-
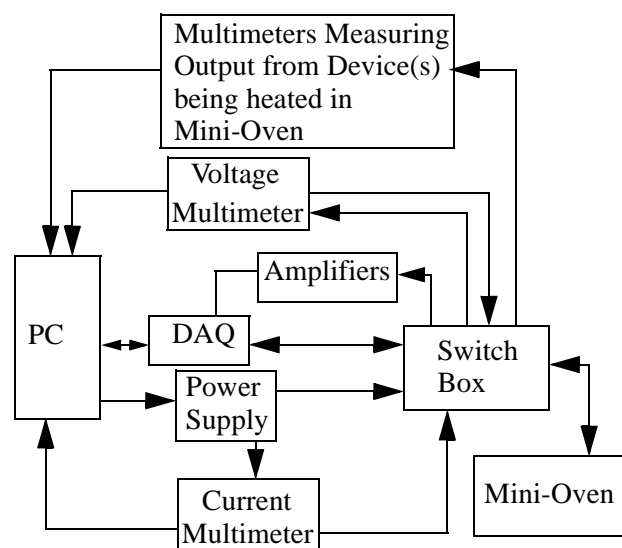
Fig. 82 Schematic of system

tains the software controlling the oven's power supply. The software also sends and receives signals to chips being aged via multimeters, a DAQ and signal amplifiers. The software contains a PID controller which varies the power supplied to the heater to maintain desired temperature. Multimeters measure the actual current and voltage supplied to the heating wire. All signals are organized by a switch box which interfaces between the actual heater device called the "mini-oven" and all other associated equipment.

11.2. Mini-Oven Design

The mini-oven consists of 3 components: the heater, the sockets, and the clamping mechanism. These components are labelled on Fig. 83.

A chip is die-attached to the package which is placed in socket #2. Socket #1 contains a Pt100 temperature sensor that is die attached to a 28-pin CerDIP package. If a temperature sensor is not required, socket #1 may be used to age a second chip.

The toggle clamps are closed, pressing the packages against the open ends of the heating element, which is a hollow square copper tube surrounded by a heating coil. The PID controller in the soft-
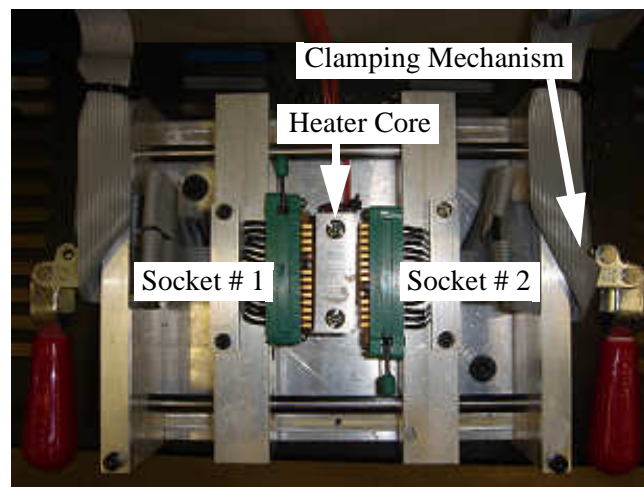

Fig. 83 Overview of mini-oven with components

ware varies the supplied voltage so that the desired set point temperatures are maintained by the oven. Cables attached to the sockets carry signals between the devices being aged and the switch-box. Any number of setpoint temperatures can be programmed to be maintained by the oven for any lengths of time, while any number of signals may be recorded and displayed graphically on the screen. A detailed description of the mini-oven design is found in [32] which includes part descriptions, dimensions, and assembly instructions.

11.3. Thermal Characterization

Thermal characterization of the mini-oven is performed to:

(a) Evaluate how accurately a temperature is maintained

(b) Evaluate how accurately a temperature measurement of one package predicts the temperature of the other package.

(c) Determine the maximum operating temperature of the oven.

(d) Characterize temperature distribution across surface of the mini-oven structure.

For (a) and (b), Pt100 temperature sensors are placed in packages at each side of the mini-oven. The Pt100 sensors are first calibrated to ensure that their measured temperatures differed by < 0.1 ºC. This is done by placing the 2 sensors next to each other in a standard convection oven, and ramping the temperature up to 200 ºC while comparing the measurements of each sensor. The mini-oven is programmed to maintain temperatures of 50ºC, 100ºC, 150ºC, and 200ºC for 40 min per interval. This test is repeated 6 times. Figure 84 shows a visualization of the average temperatures maintained at each package location for these setpoint temperatures. As can be seen in Table 11, the temperatures of the two sides differ by a mean of 0.68ºC at 200ºC. The tests with the smallest and largest temperature differences are plotted in Fig. 85.

The maximum theoretical operating temperature of the oven is 260ºC, as this is the highest temperature which the teflon will withstand. The ceramic coating can withstand up to 1200ºC, and the high-temperature solder connecting the Pt100 temperature sensors to the package can withstand up to 300 ºC.

The upper temperature limits are tested by heating the oven to 225, 250, and 260ºC. Each of these temperatures is successfully reached and maintained for 3 hours.

The temperature is measured at various locations of the mini-oven structure, with the mini-oven operating at 100ºC and 200ºC. The locations are shown and numbered in Fig. 10. Measurements
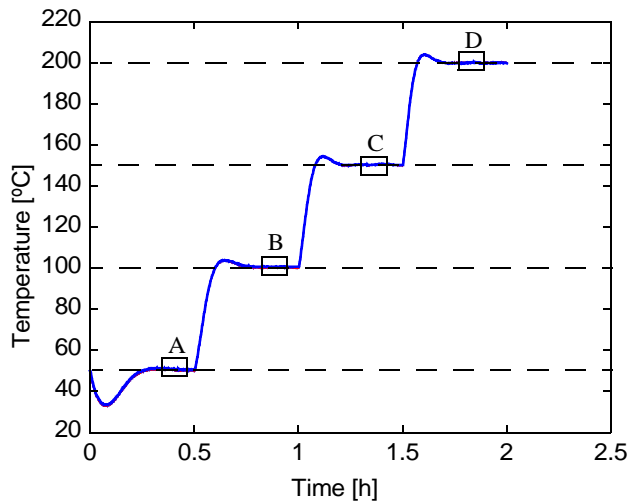

Fig. 84 Temperatures of both sides of the mini-oven during thermal characterization experiment plotted on top of each other. No difference visible on this scale.

Table 11: Temperatures of Each Side of Mini-Oven Averaged over 6 Tests

Setpoint Temp. [ºC]	T1 [ºC]	T2 [ºC]
50	50.23 ± 0.35	50.57 ± 0.42
100	100.17 ± 0.29	100.40 ± 0.31
150	150.19 ± 0.16	149.95 ± 0.40
200	200.13 ± 0.20	199.45 ± 0.53

are taken after maintaining the oven at these setpoint temperatures for at least 3 hours to allow the entire structure to reach a stable temperature. The ambient room temperature is 29ºC. To obtain the distribution, a thermal paste is applied to the surface, and a Pt100 temperature sensor with a 4-wire connection is placed in the paste. The measured temperature is averaged over at least 15 seconds and 5 measurements. The temperature distribution across the oven is shown in Fig. 86 and
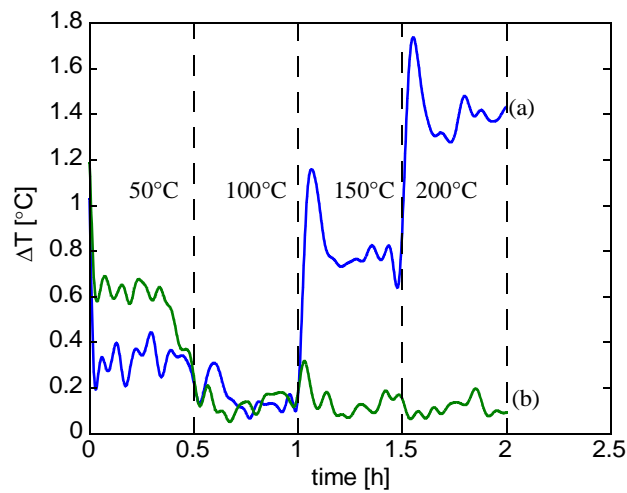

Fig. 85 (a) Largest and (b) smallest temperature differences between the two sides of the mini-oven at setpoint temperatures of 50ºC, 100ºC, 150ºC, and 200ºC. Evaluated from six test repetitions.
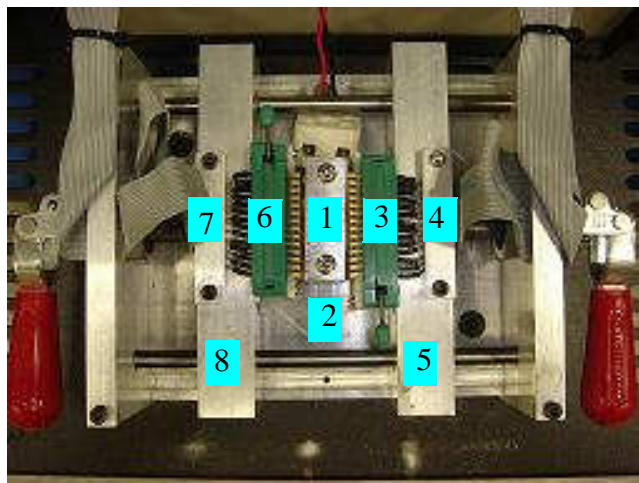

Fig. 86 Locations of temperature measurements on mini-oven.

Table 12. The temperature distribution is slightly asymmetrical, with the left side (points 6, 7, 8) having a slightly higher temperature than the right side (points 13, 4, 5).

11.4. Burn In Test

It is desired that the oven should be able to maintain temperatures of 175-200ºC for extended periods in order to perform standard wire bond accelerated aging tests [3]. To verify that the miniaturized bond ageing system is robust and the upper end of this temperature range, the oven is programmed to maintain a setpoint temperature of 200 ºC for 1120 h. During this burn-in test, the power drawn by the oven and resistance of the heating wire is recorded. As is shown in Figs 87 a and b, the resistance and required power increase significantly in the first 300 h. After 900 h, the rate of increase approaches zero. During the first 300 h, the power required to maintain the temperature increases at an average rate of 4.1 mW/h. This increase might be due to the seal between the hot oven and relatively cool packages degrading when changing room temperature causes thermal expansion and contraction of mini-oven parts ($\Delta T_{room} \sim 9$ºC between day and night). After 900 h, the required power is only increasing by an average of 0.046 mW/h which is negligi-

Table 12: Mini-Oven temperature at various locations on surface

Position	$T_{package} = 100$ºC	$T_{package} = 200$ºC
1	49ºC ± 0.70	75ºC ± 1.14
2	34ºC ± 0.19	46.5ºC ± 0.25
3	39ºC ± 1.76	63ºC ± 0.78
4	37ºC ± 0.20	50.5ºC ± 0.10
5	36ºC ± 0.22	48.5ºC ± 0.53
6	43ºC ± 0.21	63.5ºC ± 1.41
7	38ºC ± 0.93	52ºC ± 0.25
8	36.5ºC ± 0.30	49ºC ± 0.08

ble given that the oven is consuming 28 W of power to operate. Given that the required power fluctuates by ± 0.37mW as the controller adjusts the temperature, and the correlation coefficient, r = 0.048, for the heater resistance data points, this resistance increase is not statistically significant.This indicates that the heating element is not degrading over time, and the mini-oven should be reliable for long term use.

11.5. Thermal Cycling Test

A thermal cycling test is performed to ensure the reliability of the mini-oven when performing temperature cycles. The mini-oven is programmed to cycle the temperature of a Pt100 sensor between 55 °C and 195 °C, for a ΔT of 140 °C, using the temperature profile shown in Fig. 88. The heating part of the cycle lasts approximately 4 min, and the cooling lasts about 7.5 min. After performing 5700 of these cycles, there are no observable changes to the oven or to the heating wires.
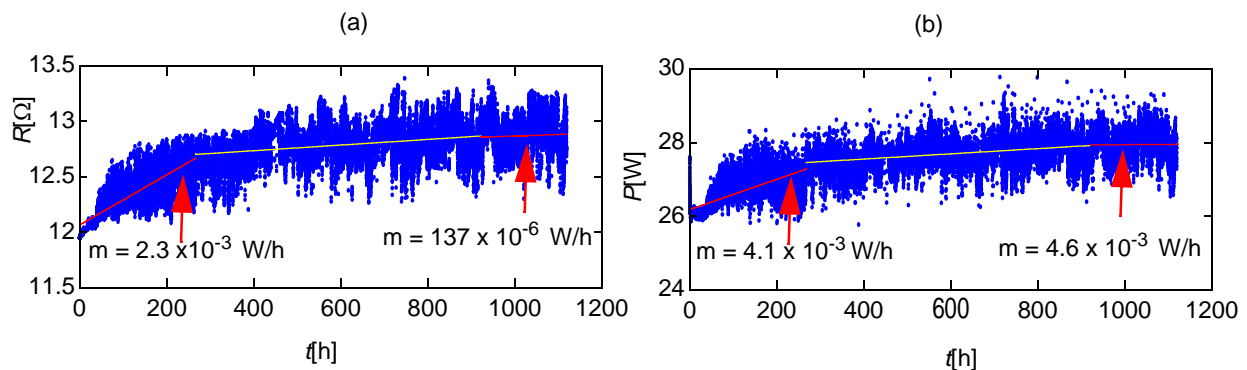

Fig. 87 a) Resistance of heating wire during long term test b) Heating power during long term test. Linear fits provided for i) first 270 h ii) 270 h to 920 h iii) 920 h to 1120 h. Rates of power and resistance increases over time are given as the slopes, m, of the linear fits for the first 270 and last 300 h of the long term test.

12. Recommendations

The integrated stress sensors have proven capable of detecting stress changes associated with microstructural developments. However, here are cases where multiple developments occur simultaneously, and it is unclear what their relative influences are on the sensors. When oxidation and lateral IMC growth are occurring simultaneously, both generate compressive stresses at the sensor elements that cannot be discerned by the sensor signal. To determine the degree to which this stress may be attributed to the lateral IMC growth as opposed to oxidation, it is recommended that similar bonds be made and aged in similar conditions, except one set of bonds should be in an air environment while the other set is in a vacuum or inert environment (e.g. N_2) where oxides cannot form. An experiment such as this could also be used to verify whether a continued contact resistance increase while the stress field changes from tensile to compressive (indicating no more vertical IMC formation) necessarily indicates oxidation of Au_4Al.

In several published studies [2, 11, 13, 17] wire bond microstructures are examined for bonds made on single layer metallizations. While studies exist with bonds made on multi-layer metalli-
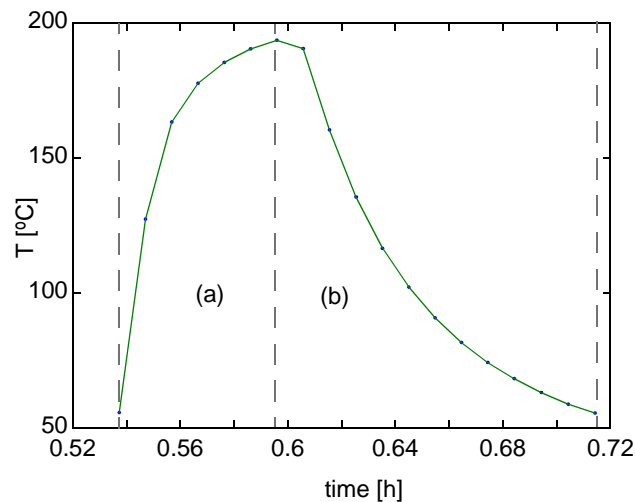

Fig. 88   Temperature profile for thermal cycling test. (a) Less than 4 mins to reach 195ºC. (b) Less than 7.5 min too cool back to 50 ºC.

zations with diffusion barriers [16, 19, 4] there is no in depth analysis on the yellow intermetallic which forms near the diffusion barrier when intermetallic growth consumes the lower Al layer of pad. While EDS analysis identifies this region as Au_4Al, and while Ti is not detected in any constant ratio, it is recommended that this region be more closely examined with transmission electron microscopy to more accurately identify this alloy. If it is discovered that it is in fact a ternary alloy, and is not Au_4Al, then the volume change associated with its formation could be calculated which could help improve the understanding of the stress sensor signal.

While the sensors have demonstrated the ability to identify microstructural changes which indicate bond quality and bond reliability, more research could be done to determine whether the magnitude of signal change can correlate directly with shear and pull strength. To do this, testing a range of bonds with intentionally different reliabilities is suggested. It is also recommended that alternative wire materials be examined such as Cu wire and Al ribbons used for power applications, to discover whether correlations exist between sensor signals and failure modes associated with such other materials.

Contact resistance measurements offer useful supplemental information regarding the state of the electrical connection. In this study, contact resistance measurement is taken from a separate set of bonds than stress measurement which increases the variation when comparing these results. For future reliability studies, it is recommended that the new test chip described in Section 10 is used, where resistance and stress are both measured for each test bond. To facilitate setup and avoid problems which may result from soldering individual wires to every package pin, it is recommended to perform reliability tests with the miniaturized heating system described in Section 11.

13. Conclusions

Observing and analyzing the microstructural evolution and strength degradation of a sample of ball bonds during high temperature storage can be very time and cost intensive if performed with traditional destructive methods. Using custom test chips with integrated stress sensors as described in this thesis allows for automated bond comparisons that can be quick and inexpensive. Where destructive methods require multiple bonds to characterize the aging process at a set of discrete intervals, the custom test chip can give continuous histories of bond evolution for each individual test bond made.

The sensor signals provide more information on bond reliability than contact resistance measurements. Contact resistance can indicate the start of bond degradation when the rate of resistance increase abruptly rises; however, no other features are detected and reliability cannot be assessed by contact resistance measurements alone.

Sensor signals have multiple features and provide insight into the microstructural evolution without the need for sectioning a bond which is otherwise required. The sensors are sensitive enough to observe the effect that a diffusion barrier has in delaying aging, and can differentiate between interfacial and lateral IMC growth which have different effects on the bond.

The practical application for the sensors is as a tool for a quick initial comparison of bonds made with a wide variety of parameters (wire bonder parameters, different wire sizes, different materials, etc...). By comparing different bonds, the signals can characterize the relative degree of initial bonding, the relative reliabilities of the bonds, and the residual stresses in the bonds. With a single test chip, multiple bonds may be quickly compared by automated software, and the bond process development may be accelerated.

It is possible that the sensors might provide an absolute measure of bond quality, and therefore may be suitable as a process qualification tool. To investigate such a possible correlation would require an additional study with multiple sets of bonds with intentionally different reliabilities. If the stress signals of bonds with different aging histories share common features, then a correlation might exist.

It is also suggested to study which respective effects IMC oxidation and lateral IMC growth have on the magnitude of the sensor signal decrease. Both mechanisms generate compressive stresses at the sensor elements. To determine this, it is recommended that identical bonds be aged in both air and vacuum environments, and the signal difference be characterized.

It is possible to customize the design of the required aging oven so that it is miniaturized and allows for more convenient operation (samples can easily be replaced) with low power requirements and rapid heating capability. Such a miniaturized bond aging system allows for more efficient use of laboratory space when multiple miniaturized ovens are stacked, creating a footprint similar to that required for a single conventional oven.

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Appendix A: Wiring Diagram for Switchbox

The wiring diagram for the switchbox is shown in Fig. 89. The switchbox can interface with up to 12 chips, a DAQ which controls the on-chip MUX, an external MUX to switch between chips for S measurements, a MUX to switch between chips for R_C measurements, and 2 MUX for switching between double ball bonds for R_C measurements.

In Fig. 89, connections to the chips are labelled "CHIP 1" through "CHIP 12". For each connection, individual pins are labelled. Pins labelled alphabetically A-X are connections to the stress signals. Each chip has 2 such connections to measure the signal as a differential voltage. All outputs are wired to the port labelled "Z-Stress". For each chip, the lower R_C connection (I_L and V_L) are labelled by a single digit 1-24. Each chip has 2 such connections, one oddly numbered for V_L, and one evenly numbered for I_L. All of these are wired to a single port labelled "Pad R_C". The individual R_C wire bonds on each chip are denoted by a hyphenated pair of numbers, e.g. 2-6. The first number indicates the chip. The second number indicates the bond. Ports shown as white circles indicate the lower ball bond, and hatched circles indicate the upper bond. These connections are wired to the corresponding pins of the 5 output ports named "Wire R_C".

The port labelled "DAQ" provides the same input to all chips simultaneously. Each input is denoted by a colour which is wired to the same coloured pin for each of the 12 chip ports. The red, blue, orange, and green pins correspond to sensor MUX inputs D3, D2, D1, D0 and are controlled by the DAQ. The purple and dark green pins supply the Ground and V_S connections respectively which are supplied by an external power supply, and not the DAQ.
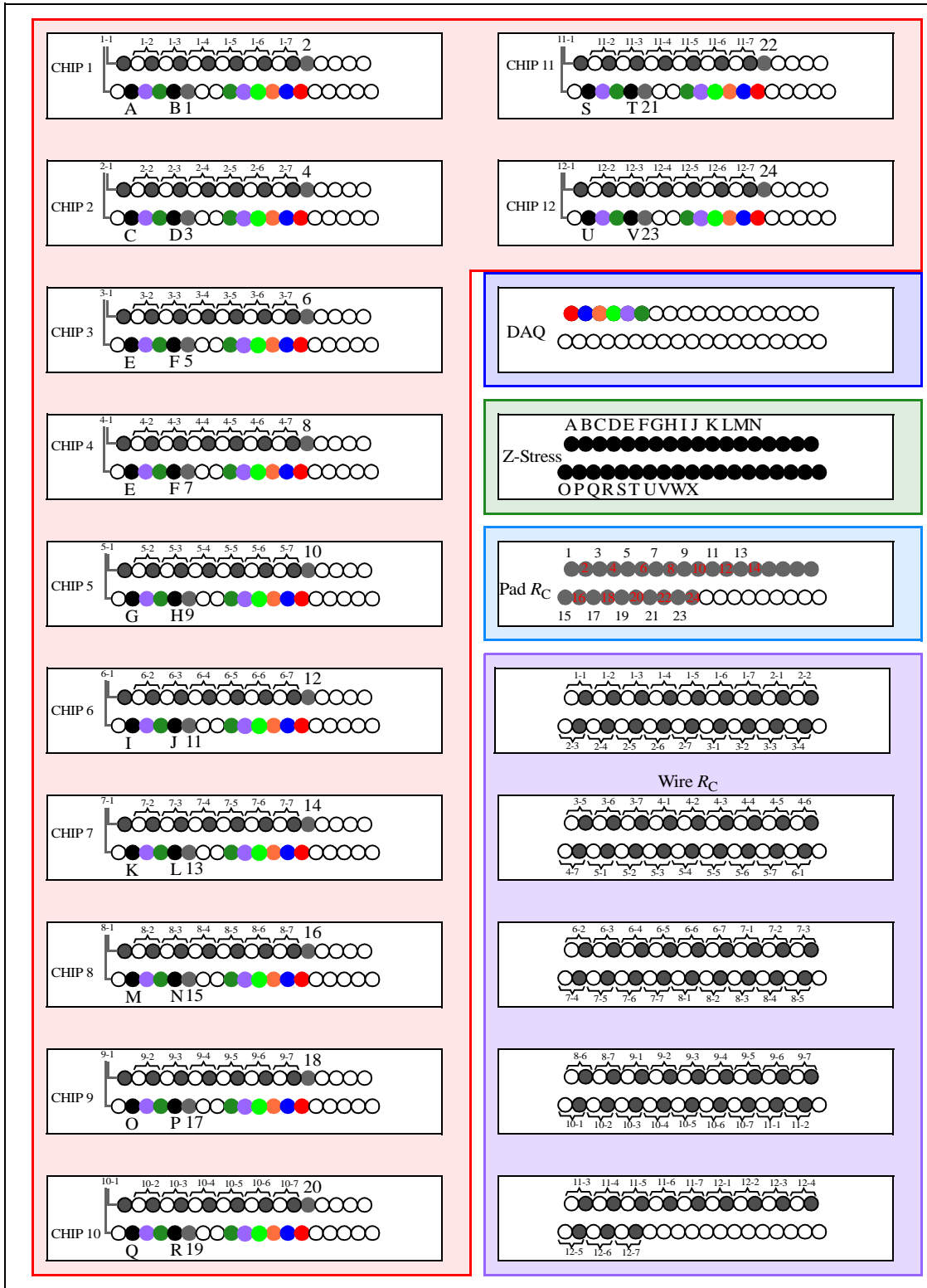
Fig. 89 Switchbox wiring diagram

Appendix B: Transistor Switches

Controlling software uses a DAQ to output signals to the on-chip multiplexer to select an individual stress sensor for signal monitoring. While the DAQ is capable of providing up to 5V output to a chip, connection of multiple chips draws more than the rated amount of current causing the output DAQ voltage to drop. To avoid this problem, a separate power supply provides the power required to operate the MUX switches (4V) and another power supply provides the sensing voltage (3V). The DAQ operates a set of 4 transistor switches corresponding to on-chip MUX inputs D0-D3. The DAQ opens or closes these switches allowing the supplied power to go through to the chips. The default switch condition is open, and the application of voltage causes the switch to close. Therefore, the DAQ output must be inverted. For example, if the desired address is 0,0,0,0, the DAQ should supply signals of 1,1,1,1 in order to close all 4 switches. Figure 90 shows the transistor switch setup.

Input from DAQ

Transistor switches

2kΩ Resistors

V_S (3V), G from

4V input from power

supply to power D0-D3

D0-D3 output to chips
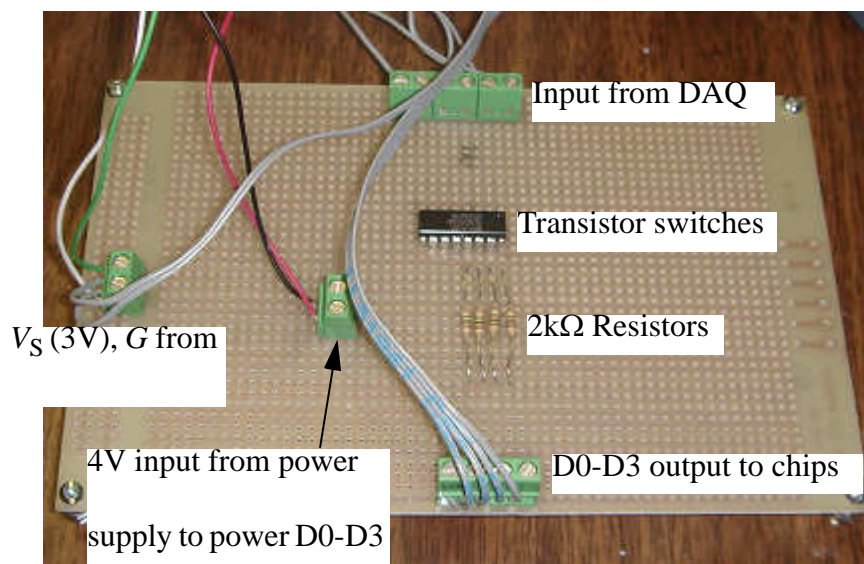
Fig. 90 Power amplification with transistor switches.

Transistor Switch Operation

A ULN2002A Darlington Transistor Array shown in Fig. 90 and 91 is used. Inputs D0-D3 from the DAQ are provided to ports numbered 1B - 4B respectively. A power supply provides 5V to inputs 1C-4C. 2kW resistors are inserted between the power supply and the switches. If a DAQ input of 0 is provided to one of the "B" inputs, the corresponding "C" input is not connected to anything inside the switch as shown in Fig. 91 b. Therefore, the supplied 4V is output to the chips. If a DAQ input of 1 is provided, the corresponding "C" input is grounded in the switch as shown in Fig. 91 c. The majority of the voltage drop will take place over the 2kΩ resistor, so the voltage provided to the chip will be approximately 0V.
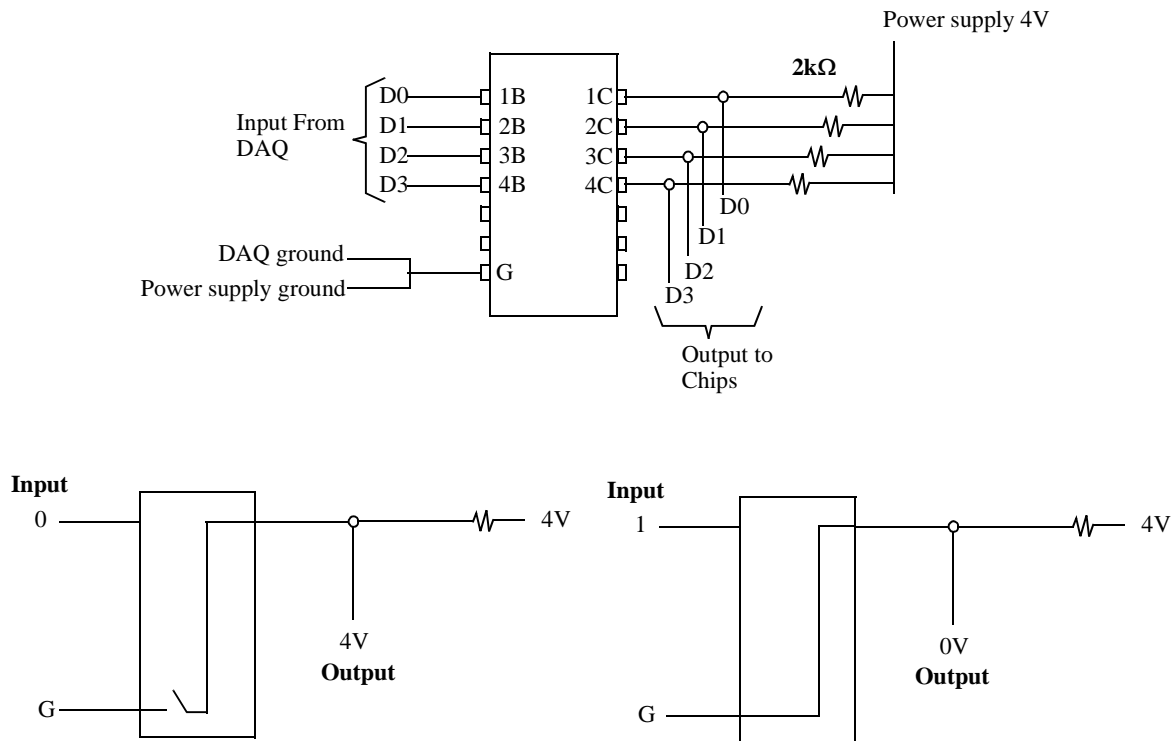
Fig. 91 Transistor Switch Operation. (a) Switch layout. (b) Switch operation with input of 0 (0V). (c) Switch operation with input of 1 (3-5V).

Appendix C: Resistance of Empty Pad

Four wire resistance of the Al pad metallization is measured during aging at 175ºC in order to determine whether the resistance of the pad is changing in a way which might affect the measured R_C of test bonds, and in order to evaluate whether the high R_C values can be explained by the pad resistance.

Measured resistance across length of pad

Ball bonds are made at each corner of the large Al pad as shown in Fig. 92. A sensing current of 1mA is provided along the length of the pad at one side, and the induced voltage is measured on the other side of the pad. An Agilent 34420A 7 1/2 Digital NanoVolt Meter is used to perform the measurements and calculate the resistance of the pad. The temperature is increased to a target temperature of 175 ºC (actual oven temperature as measured by Pt100 sensor is 178ºC) in steps (as shown in Fig.93) to determine the temperature coefficient of resistance (TCR) of the pad which is calculated to be 0.0039 ºC^{-1} from Equ. 7.
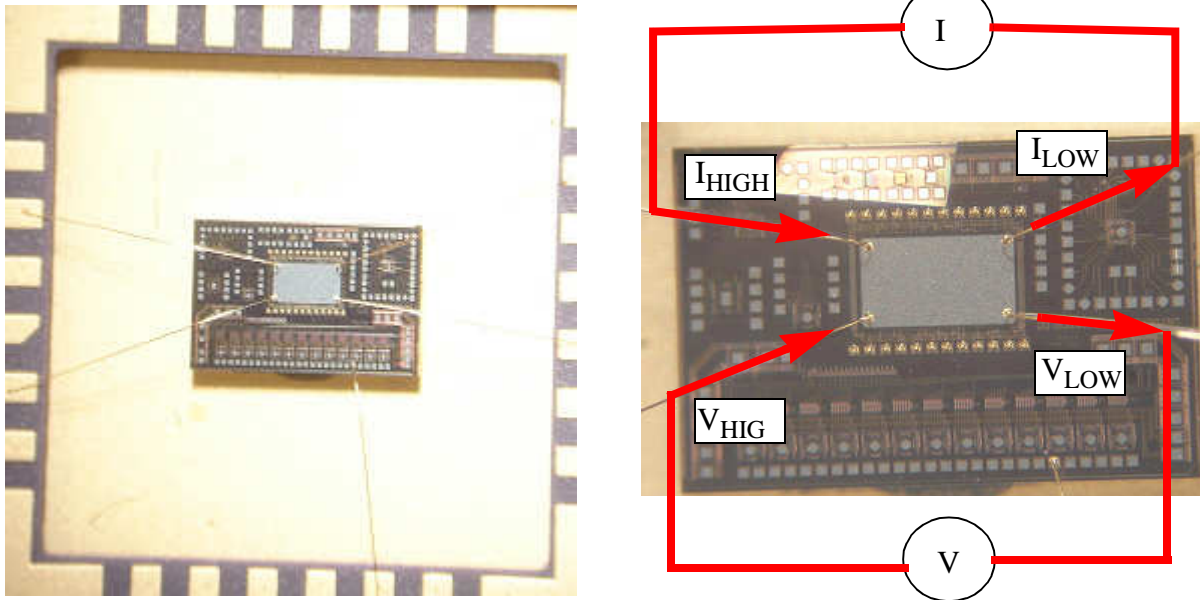
Fig. 92   Wiring for pad resistance measurement.

$$a = m/(m*T_{\text{ref}} + b) \tag{7}$$

where m is the slope of the resistance-temperature curve, b is the intercept at T_{ref}, and T_{ref} is a reference temperature (0ºC in this case).

The sheet resistance of the pad is calculated to be ~13 mΩ per square. The temperature is then maintained for an additional 140 hours as shown in Fig. 94. The resistance of the pad drops by 0.5 mΩ, or 3.2% of its total. This occurs due to Al grain recovery, and helps explain the drop of approximately 0.5 mΩ experienced by the wire bonds during the first 100 hours of aging.

Problems with built-in pads for measuring the overall resistance of large metallization region. As seen in the bond diagram in Fig. 95, the test chip includes bond pads connected to lines which attach to all 4 corners of the large Al pad, and are intended for measuring the resistance of the pad in total. In order to measure resistance with this method, the chip is bonded as shown in Fig. 95
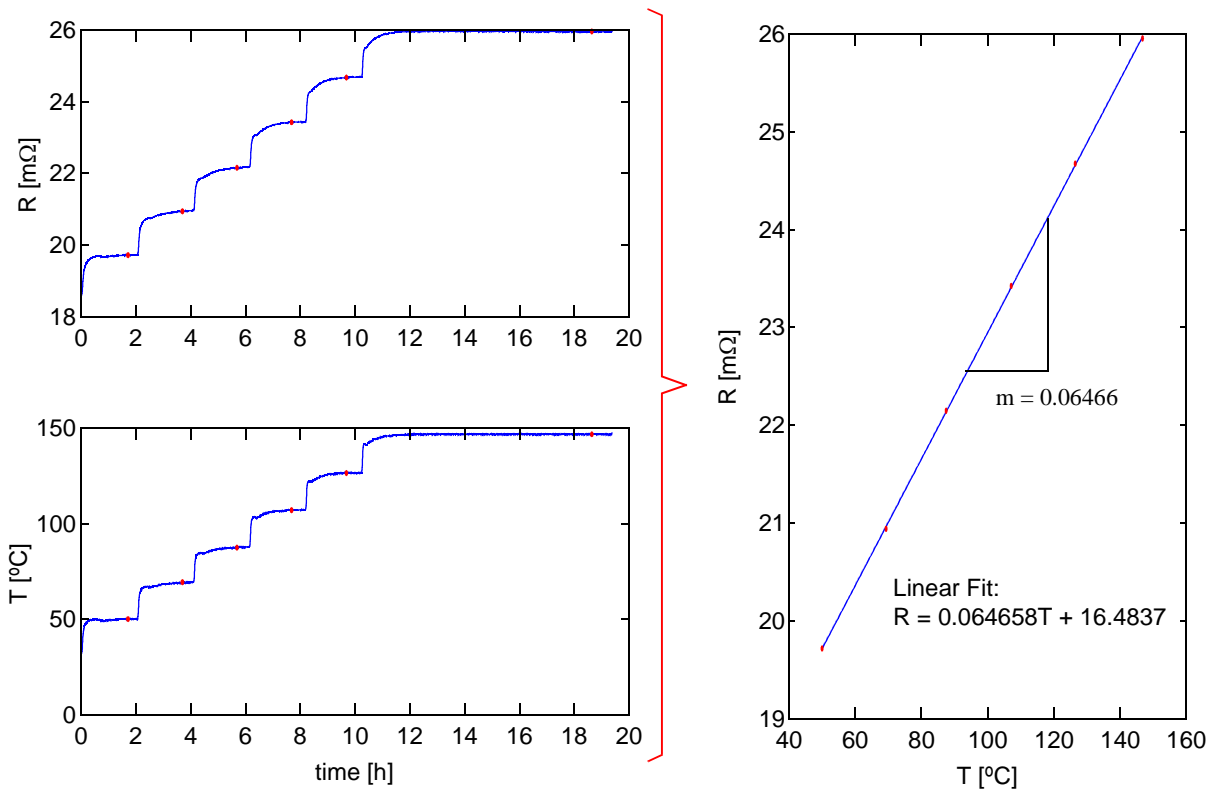
Fig. 93 Resistance-temperature characterization for finding TCR of Al test pad.
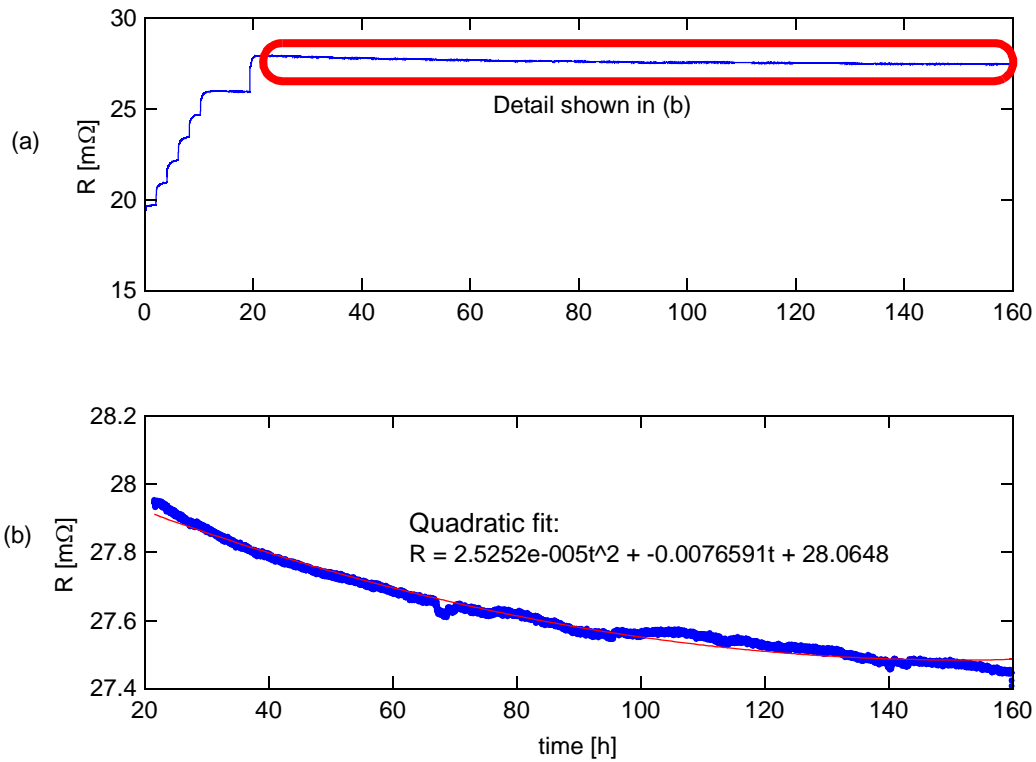
Fig. 94 Pad resistance drop experienced during 140 h of HTS at 175 °C
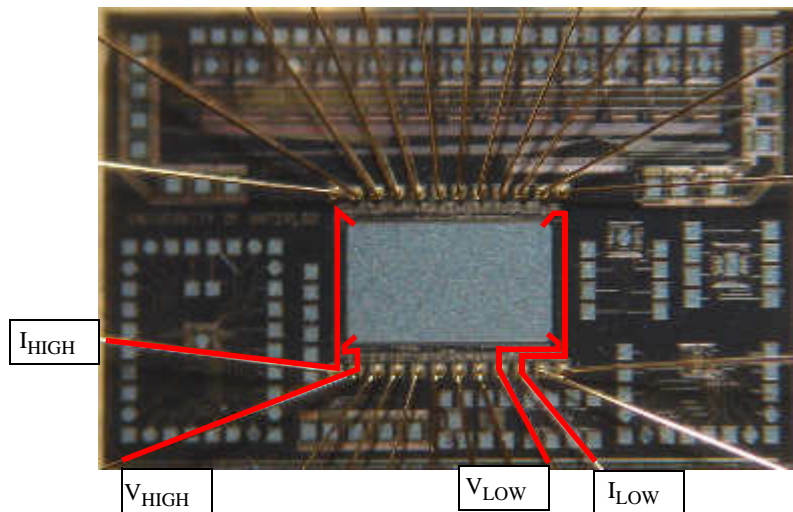
Fig. 95 Wiring diagram for measuring pad resistance using on-chip connections. This method does not work, as the on-chip connections are not reliable

and the resistance measurement is taken as temperature is increased from room temperature to

~100ºC. Figure 96 shows the measured 4-wire resistance of the pad over this time period. As can

be seen, a clear signal is not attainable. Signal breakdown consistently occurred when the temper-

ature reaches 40-50ºC. It has not been determined what design flaw is present which prevents

resistance measurements from being obtained with this method.
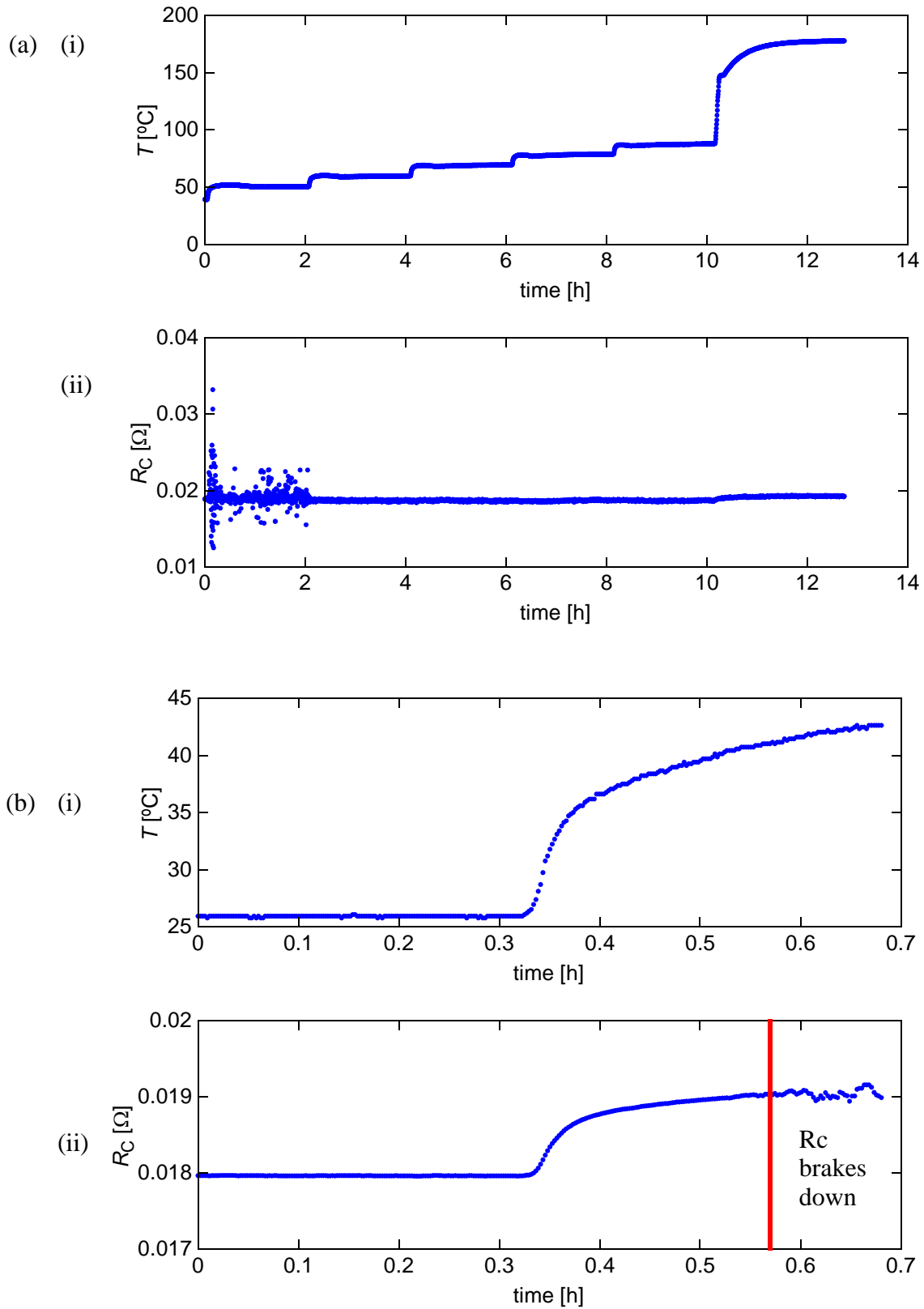
Fig. 96 Resistance cannot be measured using on-chip connections. (a) Typical resistance measurement with on-chip connections. (b) Typical resistance breakdown at ~42ºC.

Appendix D: Effect of Bond Location on Contact Resistance

Fig. 26 shows the bonding plan for chips which measure the contact resistance of test bonds. Seven test bonds are made on the large bonding pad in the center of the chip. The contact resistance (R_C) is measured using the 4-wire method, between the two wires comprising the double bond, and the 4 corners of the bonding pad. As can be seen in Fig. 97, the R_C of bonds on the large bonding pad is very high for an optimized bond, and differs greatly between each bond. This variation is systematic between chips, as bond 3 always has the highest resistance and bond 7 always has the lowest resistance. The reason chip 6 is not included in the analysis is that due to a limited number of multiplexer channels, chip 6 is made with only 5 bonds which have different locations than the other chips. The R_C variation is caused by the size of the large pad, and the placement of bonds with respect to the corners of the pad.
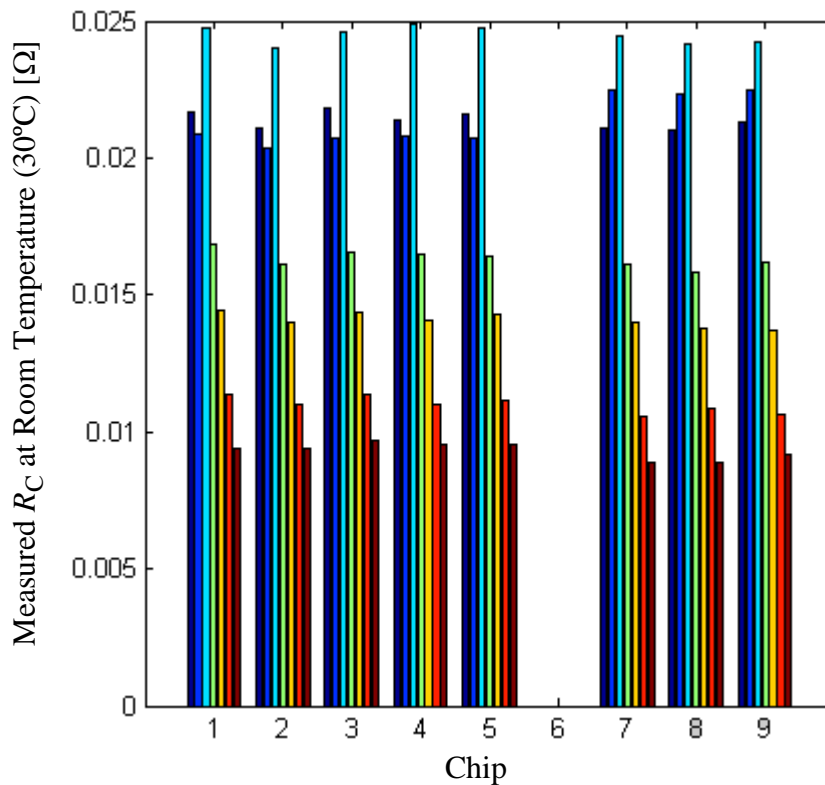
Fig. 97 Contact resistance variation between bonds

Verification of a Systematic Location Effect

Fig. 98 shows the average R_C for each bond location averaged over 8 of the 9 chips. As can be seen, the resistance varies greatly with location. This verifies that the location effect is a real phenomenon.

Evaluated Thermal Coefficient of Resistance (TCR)

Before the aging experiment was started, the TCRs of the bonds on all chips are calculated by heating the bonds in the oven while recording the resistance. The oven was heated in steps from room temperature (30 ºC) to 47ºC, 56ºC, and 65ºC. Higher temperatures were not used because it was important that the bonds are not aged during the characterization step. Figure 99 shows an example of how stabilized temperature and resistance measurements are taken at each temperature plateau to be used for the calculation. The TCR (α) is calculated as shown in Equ. 8.
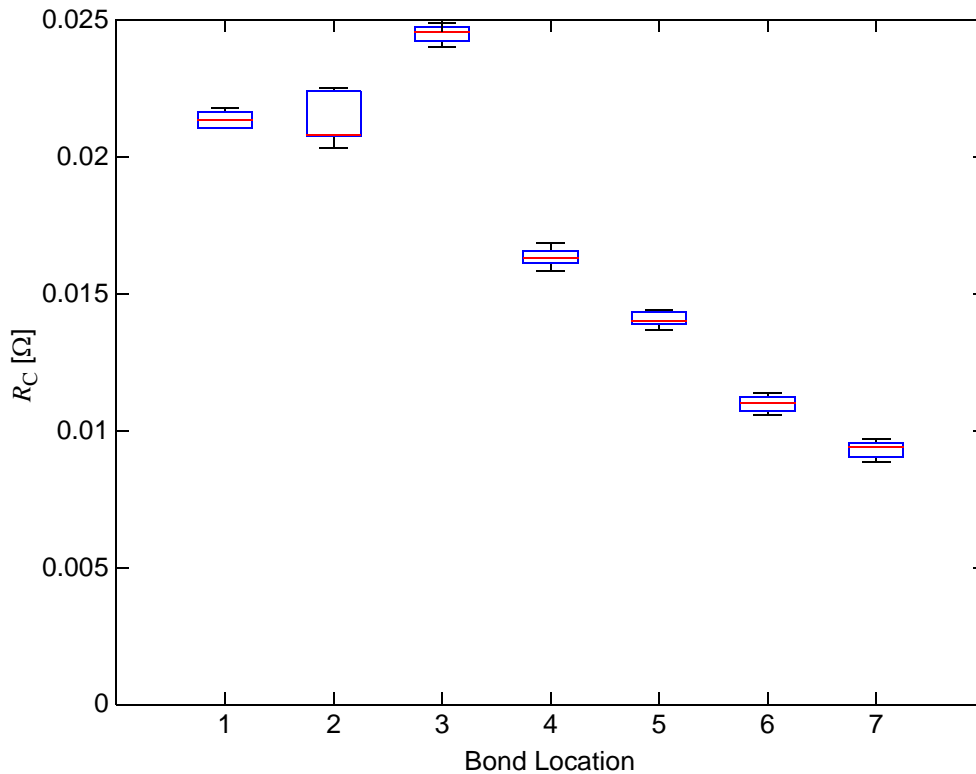
Fig. 98 Average contact resistance for each bond location

$a = m/(m*T_{\text{ref}} + b),$ (8)

where m is the slope of the resistance-temperature curve, b is the intercept at T_{ref}, and T_{ref} is a reference temperature (0 ºC in this case).
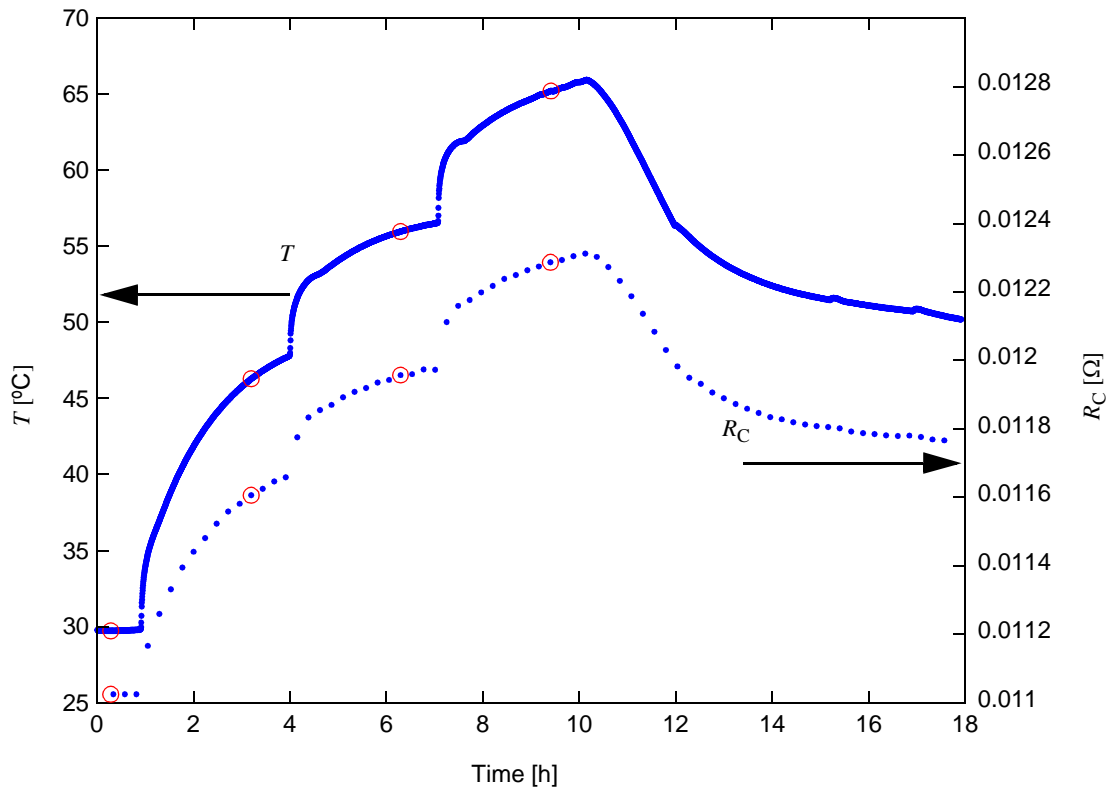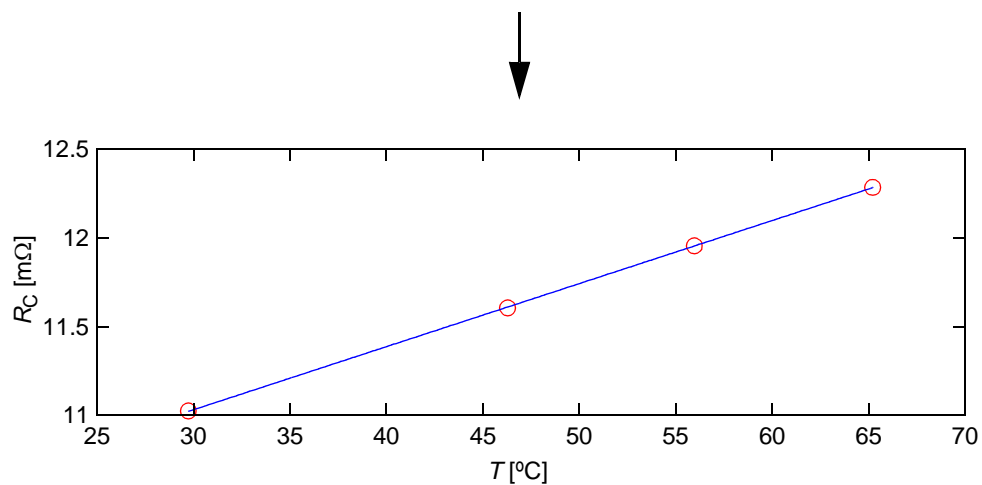

Fig. 99 Temperature ramp-up used for TCR characterization. (a) Temperature ramp-up for finding TCR. (b) Contact resistance plotted against temperature

TCRs of all bonds are plotted against each other in Fig. 100. As can be seen, bonds which were earlier observed to have high R_C values also have high TCR values.

Bond Aging with TCR Effects Accounted for.

The TCR is used to extrapolate the contact resistance to what it would expected to be at 175 ºC, were no metallurgical changes occurring. As can be seen in Fig. 101, the experimentally observed resistances are lower than would be expected. This might be because as the chip heats up, the bond initially strengthens, and the Al in the bond pad undergoes a recovery [8] which causes the resistance in the Al to drop. As can be seen in Fig. 101, the resistance of bonds which are more affected by the Al have measured resistances much lower than would be expected by TCR calcu-
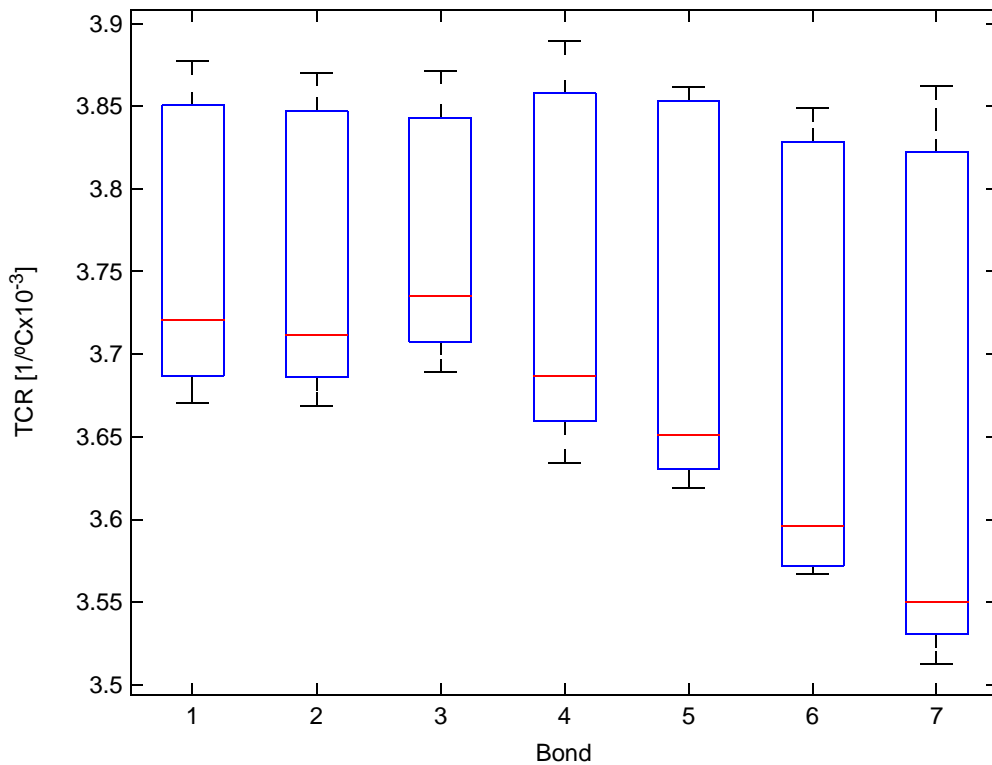
Fig. 100 Comparison of TCRs between bonds

lations alone. Conversely, bonds which are less affected by the Al have resistances only slightly lower than would be expected by TCR calculations.

Figure 102 shows an attempt to compare all data by plotting all measured resistance as an increase above the expected TCR calculated resistance at 175ºC. As expected, the bonds with the highest TCR have the highest resistances. The slopes of all the resistance increases, however, all are similar. This suggests that after an initial heating of the chips, the only mechanism affecting resistance is the interface degradation which is occurring to the same degree in all bonds. Figure 103 shows a comparison of the slopes of resistance vs. temperature for each bond, after 100 hours. As can be seen the same trend is present. The bonds with higher TCRs have higher resistance increases over time.
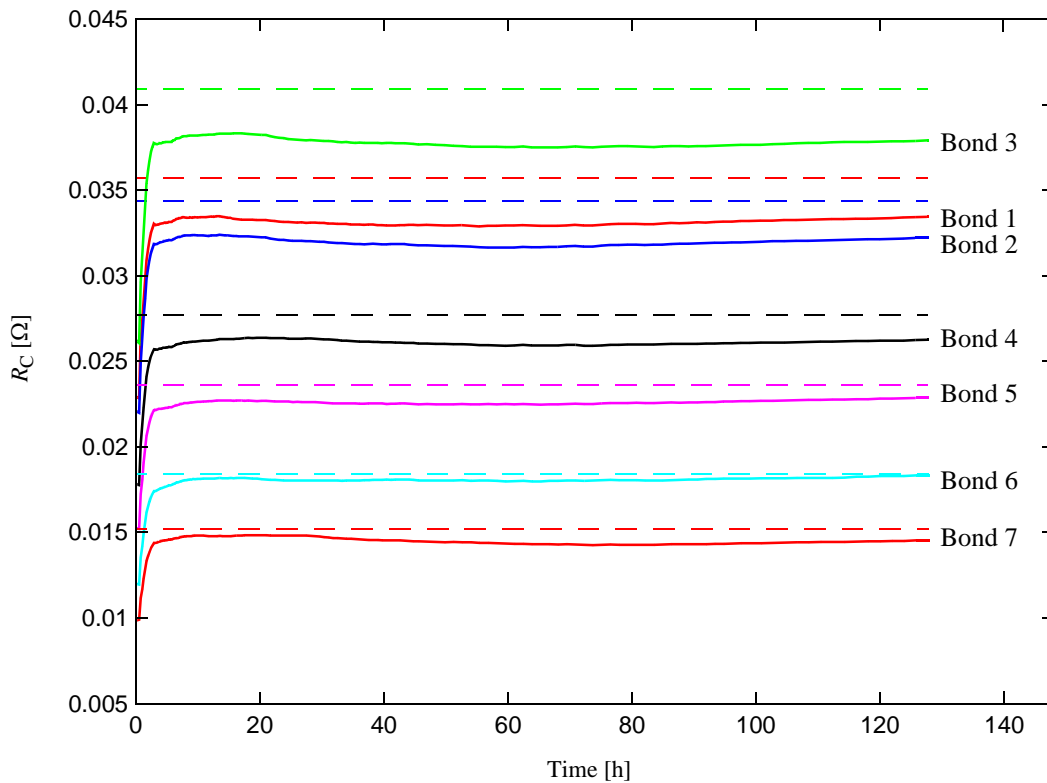

Fig. 101 Experimentally observed R_C vs. TCR predicted resistance. Horizontal dashed lines represent the TCR predicted resistance. Bold solid lines are experimentally observed resistances during temperature increase.
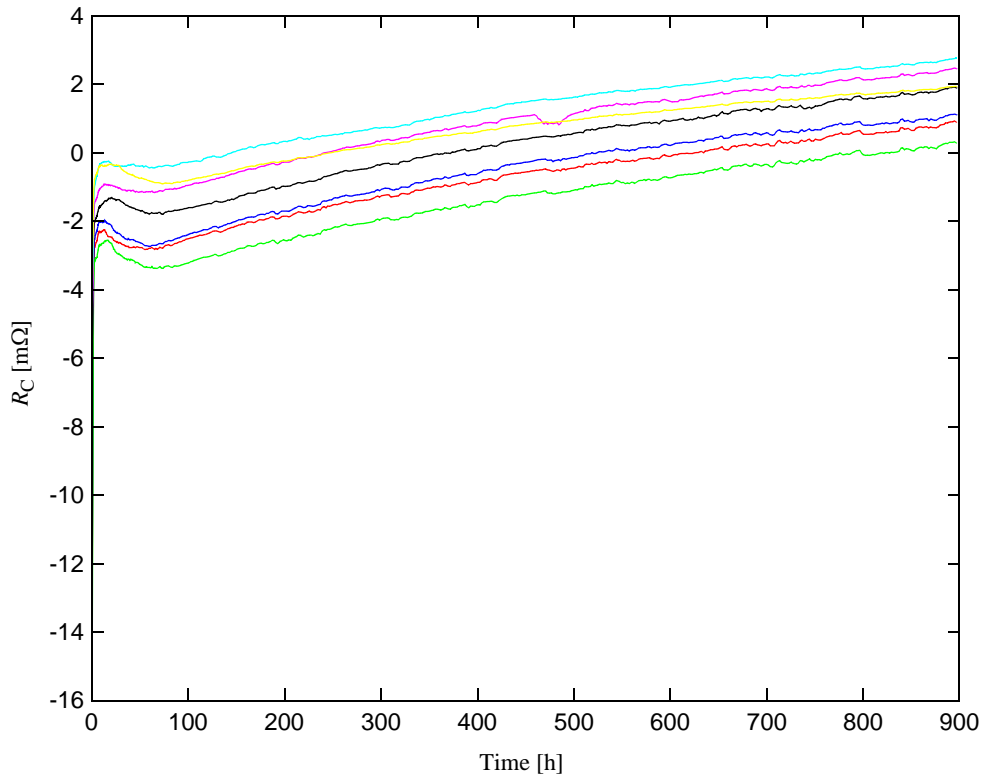
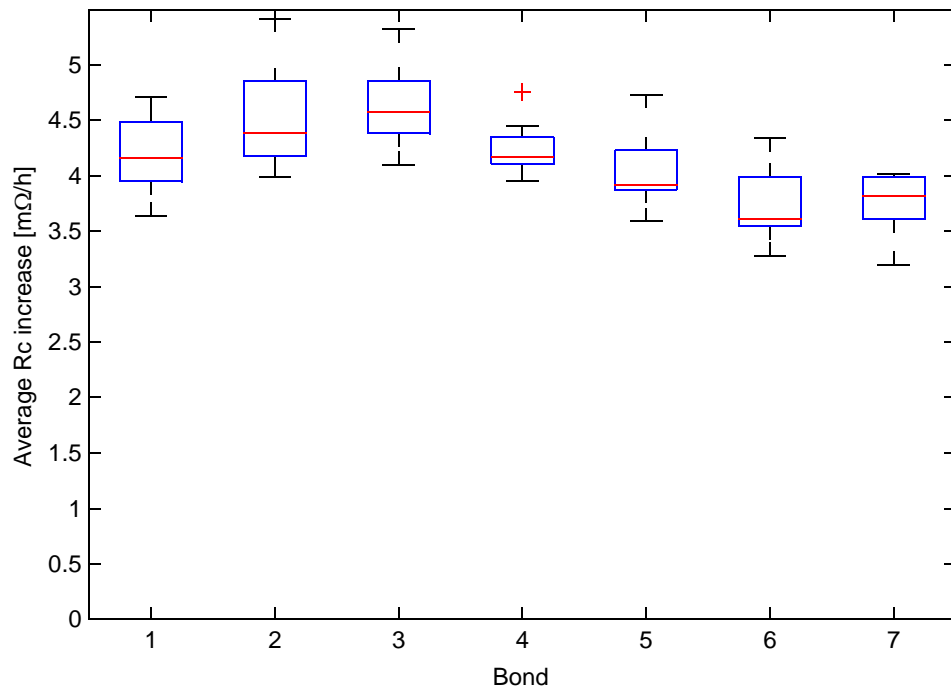Fig. 102 Resistance data minus the TCR-predicted 175ºC resistance

Fig. 103 Comparison of rates of R_C increase for each bond

Appendix E: Investigation of Possible Correlations

Figures 104 to 107 show all combinations of stress signal features described in Fig. 80 plotted

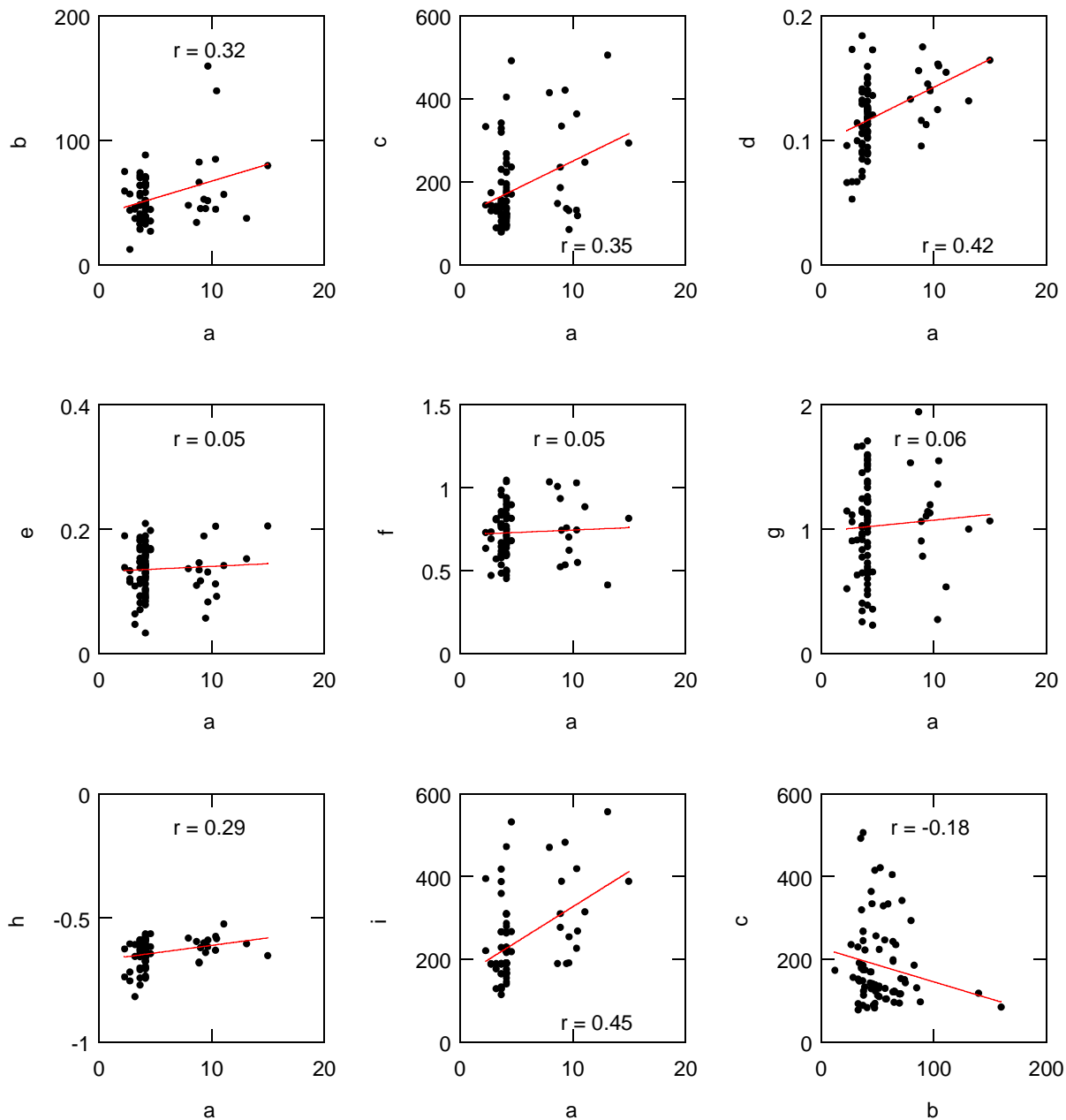against each other with calculated correlation coefficients.

Fig. 104 Correlation tests for stress signal. Parameters are defined in Fig. 80 in Section 9.5. The calculated correlation coefficient, r, is given for each set of parameters.
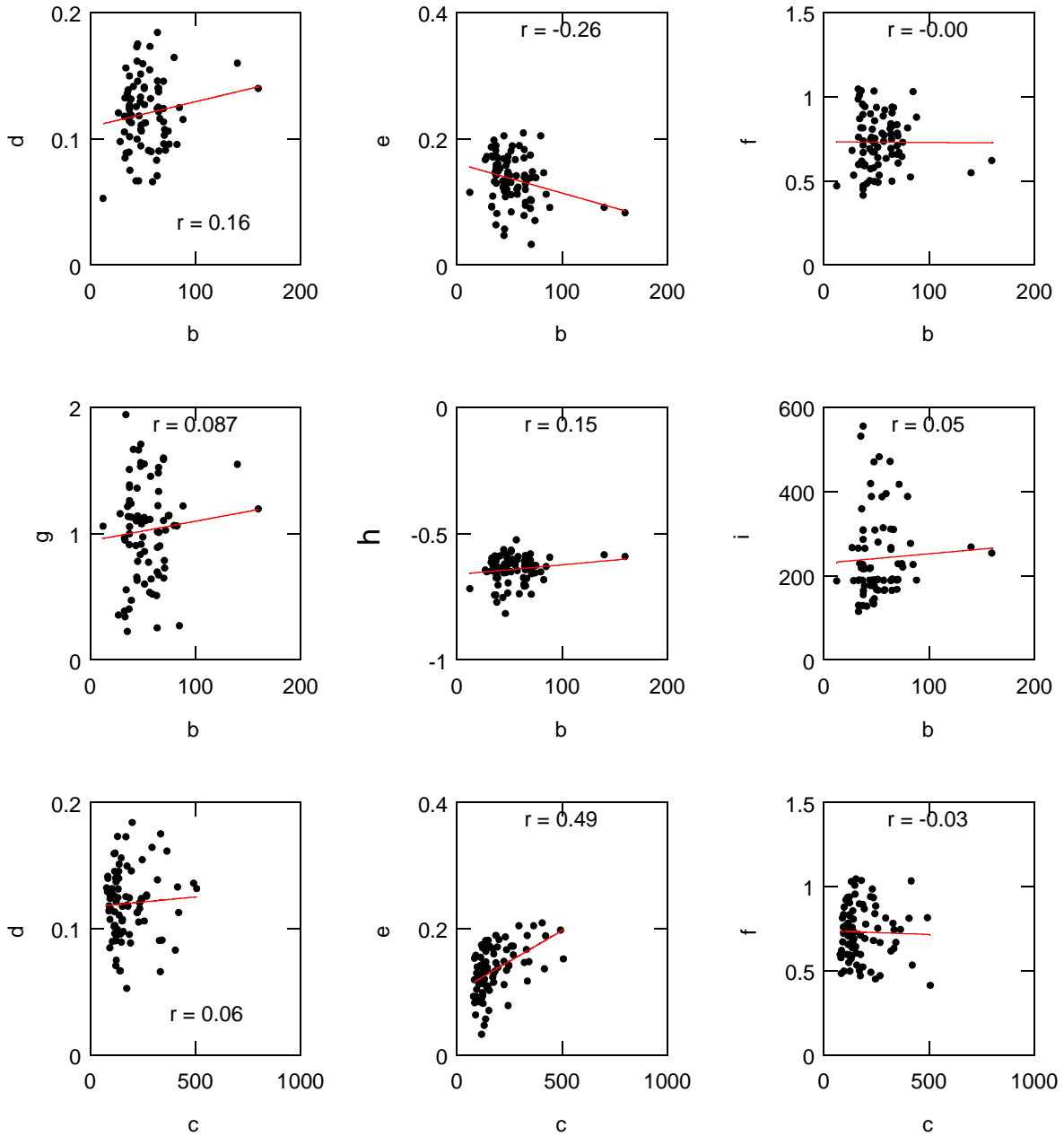
Fig. 105 Correlation tests for stress signal. Parameters are defined in Fig. 80 in Section 9.5. The calculated correlation coefficient, r, is given for each set of parameters. There is a weak correlation between 'e' and 'c'. If oxidation and lateral IMC growth is delayed, vertical IMC will cause tensile stresses to dominate for a longer time, and reach a higher value.
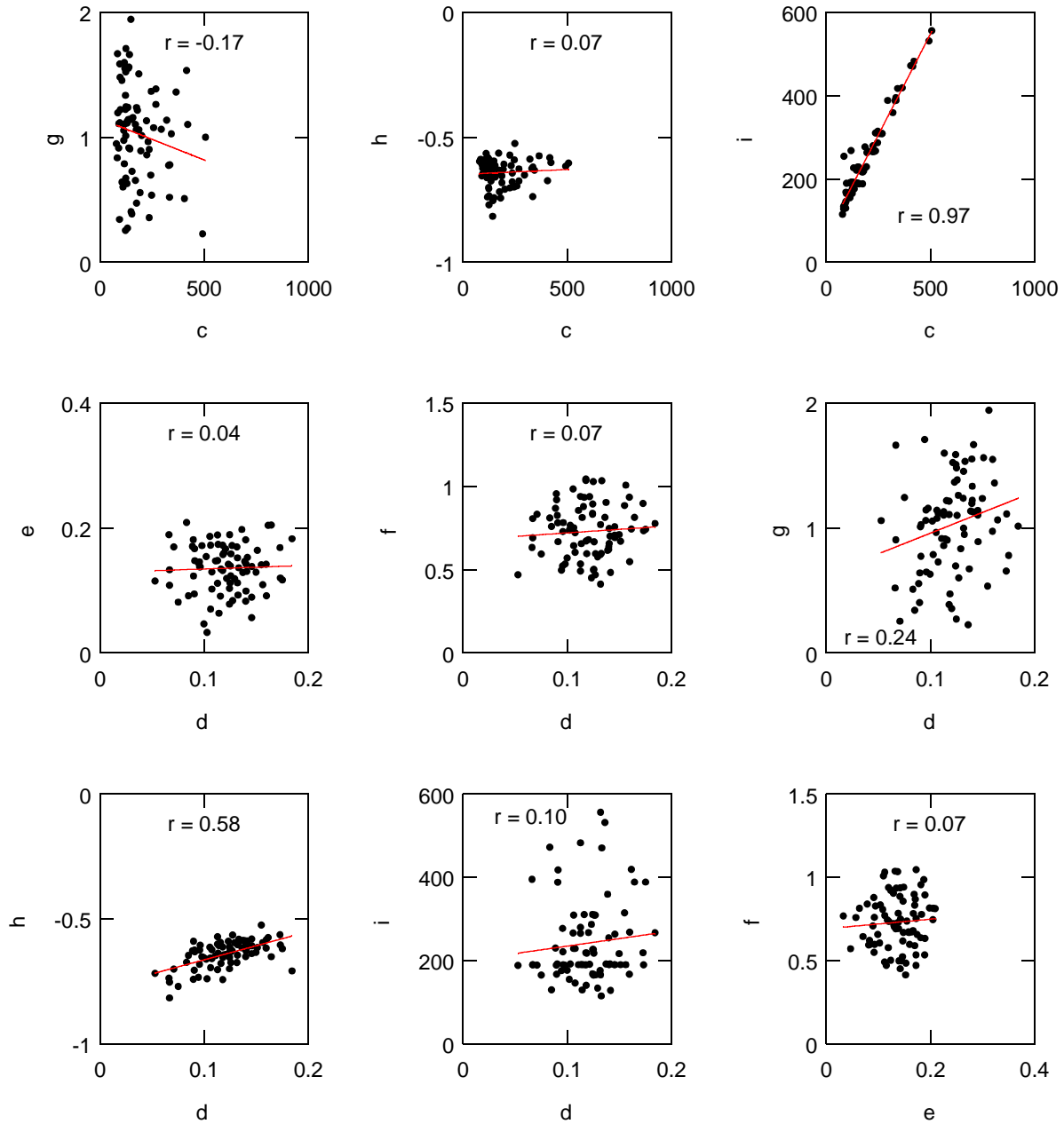
Fig. 106 Correlation tests for stress signal. Parameters are defined in Fig. 80 in Section 9.5. The calculated correlation coefficient, r, is given for each set of parameters. The correlation between 'i' and 'h' only exists because the time interval, 'i', consists mainly of the time interval, 'h'. There is a weak correlation between 'd' and 'h' which is likely due to the some signals being stronger than other signals.
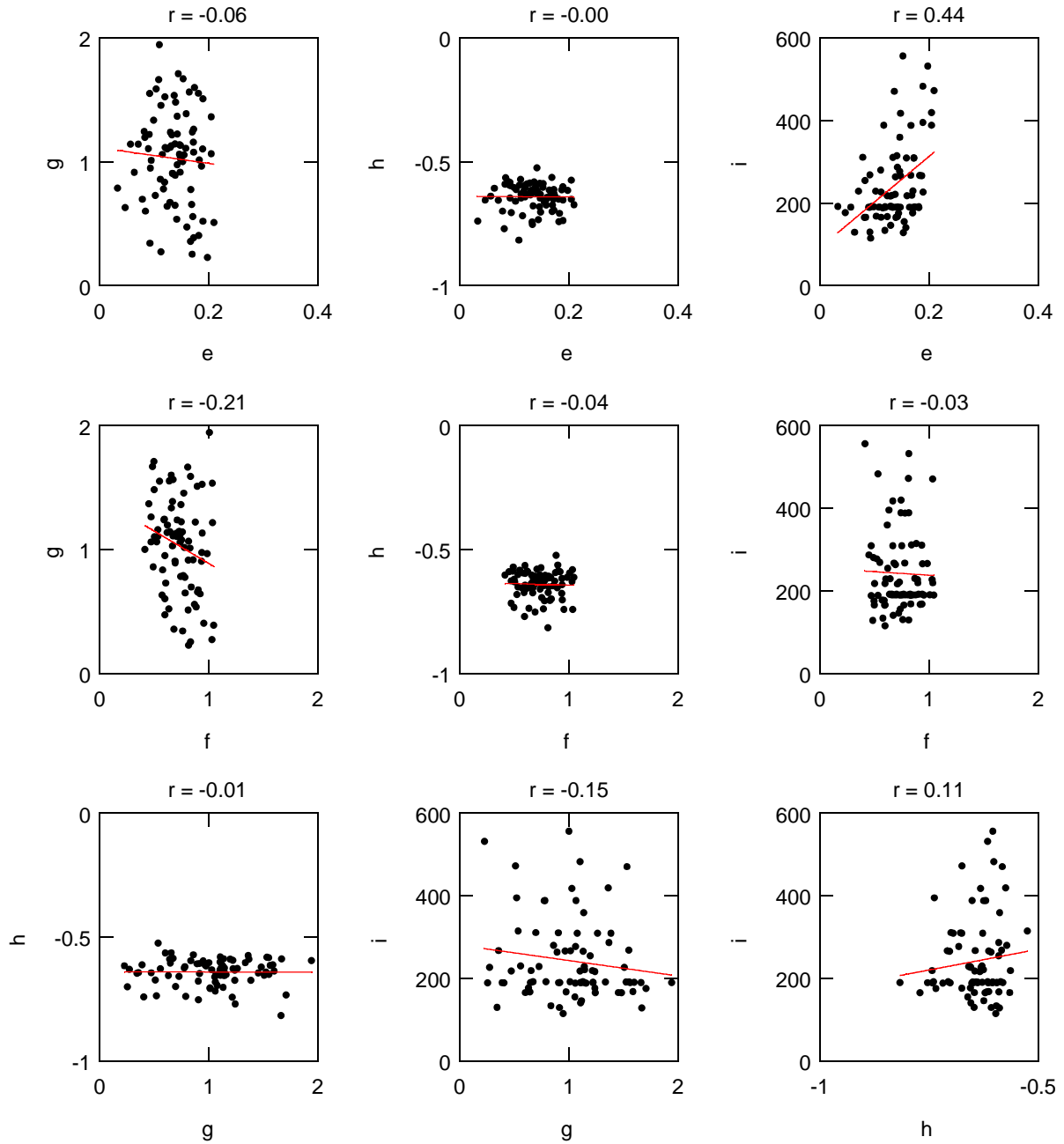
Fig. 107   Correlation tests for stress signal. Parameters are defined in Fig. 80 in Section 9.5. The calculated correlation coefficient, r, is given for each set of parameters.