Evaluation of a Direct Detection Selenium-CMOS 8×8 Passive Pixel Sensor Array for Digital X-Ray Imaging Applications

by

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AUTHOR'S DECLARATION

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

Digital imaging systems for medical applications use amorphous silicon thin-film transistor (TFT) technology due to its ability to be manufactured over large areas, making it useful for X-ray imaging, which requires imagers to be the size of the subject, unlike optical imaging. TFT technology is used to make imaging arrays coated with an X-ray detector called amorphous selenium (a-Se), which can be grown easily over large areas by being evaporated on a substrate. However, TFT technology is far inferior to crystalline silicon CMOS technology in terms of the speed, stability, noise susceptibility, and feature size. Where CMOS technology falls short is its inability to be manufactured in large wafers at a competitive cost, allowing TFT technology to continue to be dominant in the medical imaging field, unlike the optical imaging industry.

This work investigates the feasibility of integrating an imaging array fabricated in CMOS technology with an a-Se detector. The design of a CMOS passive pixel sensor (PPS) array is presented, in addition to how it is integrated with the amorphous selenium detector. Results show that the integrated Selenium-CMOS PPS array has good responsivity to optical light and X-rays, leaving the door open for further research on implementing CMOS imaging architectures going forward. Demonstrating that the PPS chips using CMOS technology can use a-Se as a detector is thus the first step in a promising path of research which should yield substantial and exciting results for the field. Though area may still prove challenging, larger

CMOS wafers can be manufactured and tiled to allow for a large enough size for certain diagnostic imaging applications and potentially even large area applications like digital mammography.

Thesis Organization

Chapter 1 gives general background information on large area digital imaging pixel architectures and amorphous selenium as an X-ray detector, setting up the motivation for this work. Chapter 2 outlines the design of the CMOS PPS array as well as how the a-Se detector was fabricated and integrated with the CMOS chip. Chapter 3 introduces the design of the printed circuit board used to test the PPS array. Chapter 4 discusses the results of testing the PPS array with the a-Se detector on several different fronts. Chapter 5 summarizes the work presented in the thesis and leaves the reader with an idea of where the research path might go from here.

Acknowledgements

It is standard cliché for the acknowledgements section in a graduate-level thesis to begin with the student thanking their supervisor, but after having nearly reached the end of the journey at the time of this writing, I truly understand why. And so I must begin by profoundly thanking Professor Karim S. Karim for his providing his unconditional support, guidance, encouragement, and resources during my time as a master's student and for generally being the best supervisor a graduate student could ask for. From the first time we talked when I was considering graduate studies two years ago, I was immediately taken in by his enthusiasm for research and for taking the time to explain every project the group was undertaking. Over the past two years, under Prof Karim's supervision, I have been able to gain valuable experience and participate in several different research projects through his guidance, all of which were fulfilling, and one of which ended up being this thesis project. I would like to thank Professor Ajoy Opal and Dr. Bill Bishop for agreeing to be readers of my thesis.

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Lastly, I would not be here were it not for my family's loving support – my mom and dad, and my two sisters. I am forever grateful for your never-ending encouragement, which really does make me believe in myself.

As my time at the University of Waterloo winds down, I can look back and say it was the best time of my life and my education, contacts, and experiences were truly invaluable. So I want to thank the University, the Faculty of Engineering, and the ECE Department again. While the time has come to move on, I'll always think of Waterloo as home and I'm extremely proud to be a twice-alumnus of this fine institution.

And with that, I think it's finally time to stop hitting the snooze button…

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Chapter 1

Background

1.1 Introduction to Digital X-Ray Imaging

The field of medical imaging has seen a remarkable evolution in the past two decades. While film screen-based X-ray radiography systems proved resilient over the bulk of the 20th century, the technological advances in the semiconductor industry that allowed engineers to revolutionize so many other fields during this time eventually heralded an elegant solution to allow for the development of a digital X-ray imaging system. Materials that could convert X-ray photons into electric charge had already been identified and once the capability to integrate these detectors with readout electronics became possible, a digital imaging system was developed with wide-ranging advantages over the traditional film-screen system – higher resolution images which result in a smaller chance of false positive and false negative diagnoses, instant access to an on-screen X-ray image, and the elimination of stacks of film archives, all while exposing the patient to lower doses of potentially harmful radiation.

1.1.1 Large Area Medical Imaging

Optical imaging and X-ray imaging have a major difference which has a significant consequence on the architecture of the devices used to capture the respective types of images. The image of a large, beautiful landscape can be projected on and captured with an imaging device the size of a fingernail inside the camera, since light can be refracted through a lens. But X-rays cannot be focused the way light can be, meaning that to take an X-ray image of an object the size of a hand, an imager of the same size is required. This makes it difficult to take advantage of crystalline silicon CMOS technology for the electronic imaging system because large silicon wafers cannot be manufactured while maintaining crystallinity throughout, and their production is extremely costly.

As a result, digital imagers in the medical field use amorphous silicon thin-film transistor (TFT) technology, despite its lower carrier mobility and poorer noise performance compared to CMOS technology. This is because TFT wafers can be manufactured with ease over a large area as the amorphous technology does not need to maintain crystallinity and can be easily deposited on a substrate. The most prevalent imaging system of this type is called a flat panel active matrix array. A typical imager of this type contains an X-ray detector on top of an array of individual pixels of repeated circuitry (fabricated in TFT technology). The circuitry is used to read the electric charge collected by the X-ray detector as a result of the incident X-ray photons, and the pixels' digitized values are put together as part of the array to make up a high-resolution digital image. The conversion of the X-ray photons into electric charge can be done via a direct detection scheme, where the detector converts X-ray photons directly into electric charge, or an indirect detection scheme, where the detector converts X-

ray photons to light photons and uses a photodetector to convert the optical photons into electric charge.

1.1.2 Passive Pixel Sensor Architecture

The passive pixel sensor (PPS), first reported by Rudolph Dyck and Gene Weckler [1] in the late 1960s, is the prevalent pixel architecture standard for flat panel arrays in the medical imaging industry, due to its compact structure and ease of fabrication. The pixel architecture, shown in Figure 1, consists of a photodetector which converts incoming photons into electric charge, accumulating and giving rise to a voltage at the pixel detector node due to the capacitance present there. The detector is connected to the drain of a transistor, which acts as a switch when its gate is asserted to read out the stored charge at the end of each integration cycle. The word *passive* comes from the fact that this transistor acts as a switch and does not provide any on-pixel gain to the signal stored at the detector node.

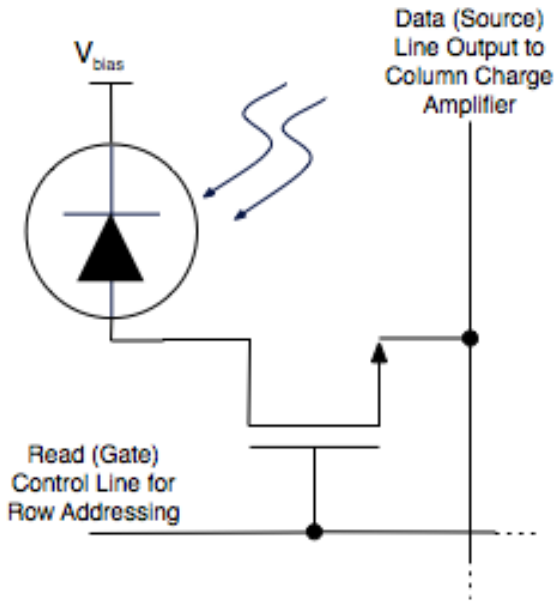

Figure 1: Passive Pixel Sensor (PPS) architecture for general purpose image sensing

In the case of optical imaging, silicon itself can act as the detector due to its photoreceptive properties, and so a simple p-n photodiode is sufficient. However, for X-ray imaging, the detector needs to be thick enough to absorb a large portion of the incoming X-ray photons and convert them into electric charge. Since the detector's capacitance is inversely proportional to its thickness, a thick detector results in a small capacitance. For a typical amorphous selenium (a-Se) panel, the capacitance of the a-Se detector for a pixel is given by the following equation:

$$C_{det} = \frac{\varepsilon_0 \varepsilon_{a-Se} A_{pix}}{t_{det}}, \tag{1}$$

where C_{det} is the effective detector capacitance for each pixel, $\varepsilon_0 = 8.85\text{x}10^{-12}$ F/m, $\varepsilon_{a\text{-}Se}$ is the dielectric constant of amorphous selenium (3.6), A_{pix} is the area of the pixel, and t_{det} is the thickness of the a-Se detector. For a 150 μm x 150 μm pixel with an a-Se detector 500 μm thick, C_{det} is only about 1 fF. This small capacitance means that the photocurrent can result in a buildup of voltages that are large enough to break down the transistor during integration, since the voltage on a capacitor is equal to the charge on it divided by its capacitance:

$$V_{pix} = \frac{Q_{ph}}{C_{det}}. \tag{2}$$

As a result, the PPS architecture used in medical imaging requires the presence of an on-pixel capacitor C_{pix} (typically 1 pF) to store the charge Q_{ph} and ensure that V_{pix} does not exceed the technology's threshold. The effective capacitance at the node is then the sum of C_{pix} and C_{det}, which is effectively C_{pix} due to the fact that it is orders of magnitude larger than C_{det}. A typical PPS architecture using amorphous selenium as a detector is shown in Figure 2.

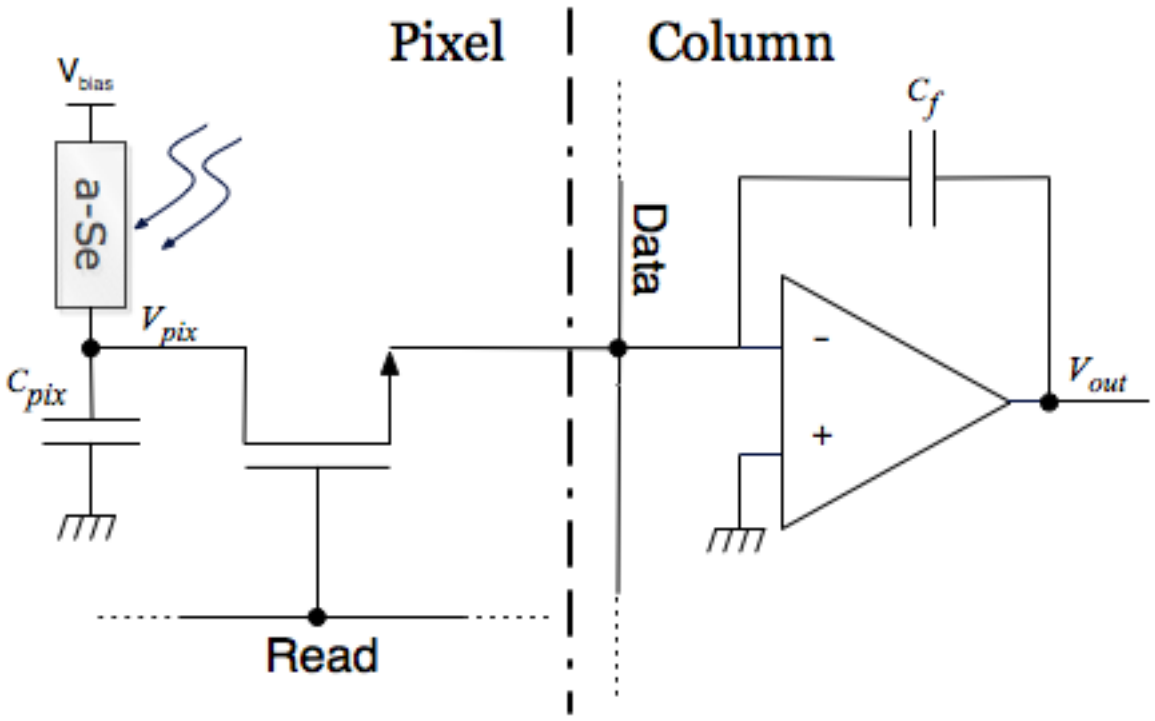

Figure 2: PPS architecture using a-Se detector for digital imaging, with off-array charge amplifier shown

A charge amplifier is used to convert the charge that is read out through the transistor into a stable voltage to allow for digitization and processing externally. The output voltage of the charge amplifier V_{out} is directly due to the charge Q_{ph} accumulated on the pixel capacitor during integration and transferred during readout, and as such can be given by the following equation:

$$V_{out} = \frac{Q_{ph}}{C_f}. \tag{3}$$

Thus, it follows from the two preceding equations that if the feedback capacitor C_f is equal to the pixel capacitor C_{pix}, the charge amplifier output voltage will be equal to V_{pix}, the voltage which is accumulated on C_{pix} during integration.

The operation of a PPS array consists of the two aforementioned cycles – the integration cycle and the readout cycle. The individual pixels in the array are connected in a way that allows for columnar readout of the imaging signals such that during readout, all of the pixels in an addressed column are read out in parallel, with a single charge amplifier per column. The gate of the PPS transistor is connected to a gate addressing or *read* line, shared by every pixel in the same row in the array, and the source of the transistor is connected to a *data* line, shared by every pixel in the same column in the array.

During the integration cycle, the gate line is deasserted such that the transistor is turned off, allowing for charge to integrate on the pixel capacitor proportional to the incident X-ray radiation on that pixel. The integration cycle is followed by the readout cycle, where the gate line is asserted so that the transistor turns on and transfers the stored charge from the pixel capacitor to the data line, where it will be amplified and digitized off-array by a charge amplifier and subsequent readout circuitry. The readout cycle also resets the pixel capacitor node, as its voltage is set to the voltage connected to the positive terminal of the charge amplifier (virtual ground) before the transistor is turned off and the next integration cycle begins. This means that the two cycles can be repeated back-to-back because the PPS architecture has destructive readout, and the pixel capacitor node is reset while readout is done.

The PPS transistor operates in the linear region during readout to provide a low on-resistance and quick charge transfer, and in the cutoff region during integration to provide a high off-resistance and allow for the accumulation of charge on the pixel capacitor. It should however be noted that there exists a leakage current through the channel of the transistor

during integration while it is turned off, which can accumulate charge on the pixel capacitor and result in the presence of noise in addition to the signal integrated on the capacitor.

During readout, the pixel is discharged with a time constant $\tau_{readout}$ which is the product of the capacitance of the pixel and the on-resistance of the transistor (R_{on}):

$$\tau_{readout} = R_{on} C_{pix}. \tag{4}$$

The on-resistance of a transistor operating in the linear region is provided by the following equation:

$$R_{on} = [\frac{W}{L} k'(V_{GS} - V_t)]^{-1}, \tag{5}$$

where W is the width of the transistor, L is its channel length, k' is a process constant which is the multiple of the effective carrier mobility (μ_{eff}) and gate capacitance per unit area (C_G) for a TFT or carrier mobility (μ_n) and gate oxide capacitance per unit area (C_{ox}) for a CMOS transistor, V_t is the transistor's threshold voltage, and V_{GS} is the gate voltage applied to the transistor while it is turned on. Table 1 shows typical values for these constants as well as the resulting R_{on} and $\tau_{readout}$ values for both amorphous silicon TFT technology and 0.18 µm CMOS technology, for two identically sized transistors and a C_{pix} of 1 pF [2,3].

Table 1: Comparing readout time constants using typical process parameters for TFT and CMOS technology

	k'	V_{GS}	V_t	W / L	R_{on}	$\tau_{readout}$
TFT	12.5 nA/V^2	12 V	2 V	10 µm / 5 µm	4 MΩ	4 ms
CMOS	387 µA/V^2	1.8 V	0.48 V	10 µm / 5 µm	979 Ω	4.895 ns

Complete charge readout (99%) requires readout to last five times the time constant ($5\tau_{readout}$), so it can be deduced that pixel readout time here using TFT technology would be 20 ms while it would be about 5 ns for CMOS technology, which is six orders of magnitude faster! The much lower on-resistance of CMOS technology is thus one of its advantages over TFT technology, as it directly results in a much higher frame rate to be realizable for imaging applications, which is a distinct advantage for real-time medical imaging applications like digital fluoroscopy [4].

1.1.3 Active Pixel Sensor Architectures

To address the problems associated with the PPS architecture in terms of its susceptibility to noise, a great deal of research has been done into developing active pixel sensor (APS) architectures, which use additional transistors on the pixel to convert the signal integrated by the detector into a voltage or current at the output. While adding additional circuitry to the pixel decreases the area that is actually used to collect charge generated by the detector (i.e., the *active* area), the performance tradeoffs can be beneficial.

The most basic of the APS designs is the three-transistor (3T) current-mode structure shown in Figure 3, which introduces two additional transistors, one which acts as a source-follower amplifier to buffer the voltage accumulated on the detector node to be read out, and another to reset the detector node at the end of each integration cycle [5].

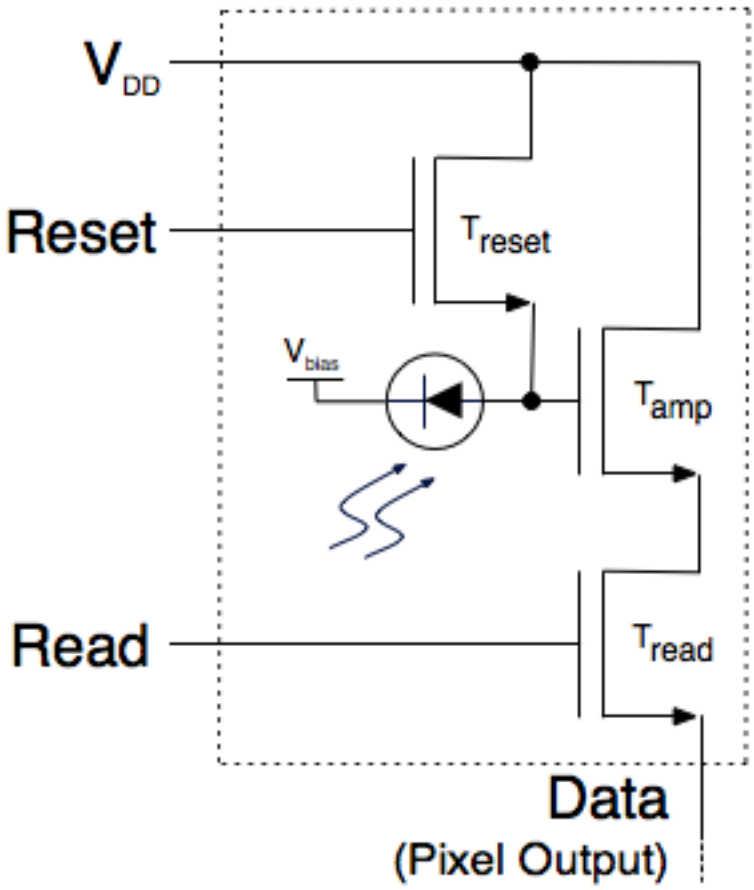

Figure 3: Three-transistor active pixel sensor architecture

The effective capacitance seen at the detector node of the APS structure is the detector's own capacitance in addition to the gate capacitance of the amplifying transistor (T_{amp}), which stores the charge collected by the detector. The operation of the APS pixel is more complicated than the PPS pixel due to the need for an additional timing signal. The operation requires a reset cycle first, where the reset signal is asserted to turn on the reset transistor (T_{reset}) and set the voltage at the detector node to the line voltage V_{DD}. This is followed by the integration cycle, where the reset signal is deasserted, and the incoming photons which generate current in the detector discharge the pixel capacitance by a ΔQ in

charge proportional to the dose, which in turn lowers the voltage at the node by a ΔV that is proportional to the radiation. Following integration, readout is done by asserting the read signal to turn on the read transistor (T_{read}) and read out the current generated by the pixel through the source of the amplifying transistor to the data line, which is connected to a charge amplifier. The source-follower amplifier in the form of T_{amp} plays a key role in improving signal-to-noise ratio because it provides a charge gain while buffering the signal voltage at its gate to its source.

Though APS pixel architectures have shown very promising results, they have for the most part been fabricated and tested as single pixels in amorphous silicon TFT technology for the purposes of noise analysis and comparison of different architectures [6]. Due to their added complexity, it is difficult to fabricate reliable APS arrays and as such there are no commercialized flat panel arrays using APS technology, though as of 2010 there are now reports of results using fabricated APS prototype arrays in academic literature [7]. This is in stark contrast to the optical imaging field, where the PPS architecture has long since been replaced by the APS architecture, which has itself seen advancements. Since its introduction into the optical imaging field, CMOS technology has begun to surpass its competing technology, charge-coupled device (CCD), taking into account cost and performance. The forerunner of pixel architectures in CMOS digital cameras is the four-transistor (4T) APS architecture shown in Figure 4.

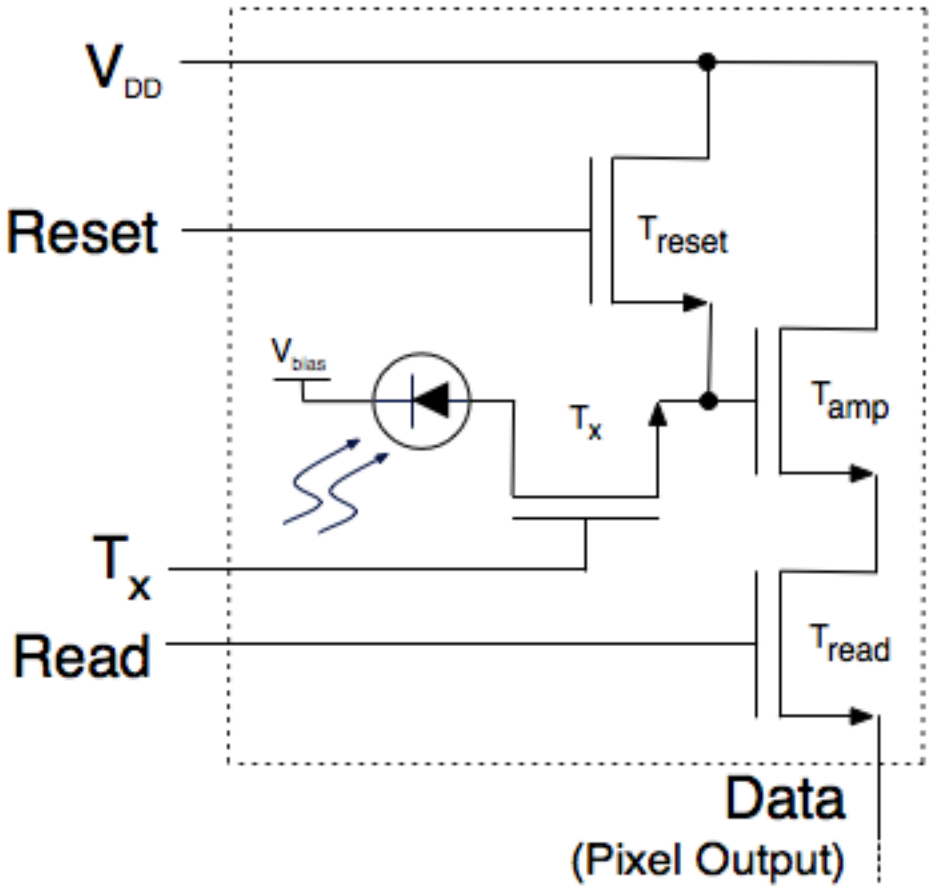

Figure 4: Four-transistor active pixel sensor architecture

The operation of the 4T APS architecture is very similar to the 3T architecture, but it has an additional timing signal which is associated with the additional transistor (T_x). The addition of this transistor helps overcome some of the noise problems suffered by the 3T pixel [8]. By separating the detector node from the pixel node at the gate of T_{amp} via the T_x transistor, the architecture allows for on-pixel correlated double sampling (CDS). CDS eliminates deterministic sources of noise by sampling the signal twice – once before integration and once after – and subtracting the difference to get the true signal and eliminate the reset noise injected at the output. It also allows for the dynamic range/conversion gain

tradeoff to be addressed because the two are now independent of each other as a result of the separation of the detector node and the pixel node. Finally, the 4T pixel also eliminates the problem of kTC noise, a phenomenon which causes a random charge variation on a capacitor that is read out through a switch each time it is sampled. By turning on the T_x transistor as well as the read transistor while readout is done, the problem of sampling a capacitor after a switch is turned off is eliminated.

It is apparent that the medical imaging field would be better served by image sensors that go beyond the simple PPS structure and benefit from the very same ideas that have allowed CMOS APS image sensors to overtake traditional charge-coupled device (CCD) image sensors in cameras. The underlying factor that currently limits this evolution for medical imaging is the amorphous silicon TFT technology in which the large-area arrays are fabricated.

1.2 Amorphous Selenium as an X-Ray Detector

Selenium is a substance that occurs naturally in the earth's crust, as well as being a byproduct of copper refining – meaning it is available in great abundance. The photoconducting properties of amorphous selenium have long been put to use by engineers and scientists – with its ability to be prepared in large areas, a-Se was found to be fruitful as a photoreceptor on the drums of photocopiers as early as the 1970s, which had black powder (toner) adhere to the parts of a surface that remained electrically charged after exposure to light [9]. Selenium's relatively high atomic number (indicating a good level of X-ray absorption) coupled with its photoconductivity made the detector also useful in large-area

xeroradiography, which is in simple terms the photocopying of body parts onto paper by using an X-ray source in place of xerography's light source.

The use of a-Se in both of these applications was doomed, however, for different reasons. In the case of the former, anthropogenic photoconductors of the organic form were found to be more economically advantageous for use as xerographic photoreceptors than a-Se, and as such xerographic photocopying lived on without the use of a selenium-based detector. In the case of the latter, though, the application itself was the root cause of failure, not a-Se and its photoconductive properties. Xeroradiography was simply too problematic due to the difficulties and noise associated with the toner-based method of developing the image [10]. But with the development of electronic readout mechanisms to capture digital images in the form of active matrix flat panel arrays in the 1990s, there was rekindled interest in a-Se as an X-ray detector for reasons that will be evident to the reader shortly.

1.2.1 Operation of Radiation Detectors

There are various properties which are desirable in a radiation detector. A detector generates electron-hole pairs (EHP) when it is given a dose of radiation. The charge carriers of each type are then propelled to opposing electrodes via an electric field, thus creating a net flow of charge, or electric current, which can be stored on a capacitor. It is clear that the detector's sensitivity is directly proportional to the amount of EHPs generated per unit of radiation, which should be as high as possible. But equally as important as sensitivity is the detection efficiency – a high percentage of the incoming X-ray photons should be detected and converted. Further, it is imperative that there is minimal recombination of EHPs during transit through the detector and that the longest carrier transit time is not severely limiting to

the application. The detector should also have a very minimal amount of dark current, meaning when there is no exposure to X-ray radiation, carriers should not be generated and charge not be collected. Detectors are also desired to have a high spatial resolution [11]. Finally, there is a rather important constraint for the use of detectors with flat panels for medical imaging: It is preferable that the detector layer be able to be easily coated onto the panel rather than having to be individually bonded to pixels in the array.

Radiation detectors can generally be split into two categories: direct conversion detectors and indirect conversion detectors (or, simply, direct and indirect detectors).

1.2.1.1 Indirect Radiation Detection

Indirect detectors are named as such because they inherently take an indirect process to convert X-ray radiation to electrical charge, by first using a scintillating screen to convert X-ray photons to photons (light), and then converting the generated light to charge by a photodetector. The scintillator's light intensity is proportional to the light intensity, so the charge is proportional to the X-ray radiation. Thus, the indirect process involves at least two layers of material. There are various implementations of indirect detectors; one such system prototyped by University of Michigan Medical Center researchers uses a thallium-doped cesium iodide (CsI:Tl) scintillator and a hydrogenated amorphous silicon (a-Si:H) p-i-n photodiode as an indirect detector [12].

This design uses, for the photodiode, a patterned n-layer per pixel and continuous i- and p-layers across the array. The photodiode is followed by an indium tin oxide (ITO) metal layer. The CsI:Tl scintillator, grown separately, is then positioned in close contact with the flat panel array using a faceplate. The scintillator converts X-ray photons to light photons,

which then shine on the photodiode to generate EHPs for charge transport. But the fact that the scintillator is placed on top of another rigid surface results in some inevitable air gaps due to non-uniformities, and possible optical coupling and lateral spread between pixels, lowering the spatial resolution of the detector as a result of this crosstalk. It is also apparent that purely from a fabrication and makeup perspective, this is a fairly convoluted solution to the problem of converting X-ray photons to charge when compared to a direct detector like a-Se, which is presented next.

1.2.1.2 Direct Radiation Detection

Unlike indirect detectors, direct conversion detectors use a single layer to convert X-ray photons to electrical charge. This means that the radiation itself generates EHPs which are then propelled by an applied electric field across the detector. Direct detection materials usually have a high resistivity, leading to low dark currents, and are operated at large electric fields. In addition, direct detectors provide the highly desired property of good spatial resolution even at very low pitch pixel sizes, due to their inherent structure producing minimal lateral diffusion and producing high and well-defined electric fields.

Examples of materials that have the characteristics of a direct detector in response to X-rays include cadmium zinc telluride (CdZnTe), mercury iodide (HgI_2), lead oxide (PbO), and amorphous selenium (a-Se). Table 2 shows a comparison of these materials, displaying typical values for the detectors' performance figures of merit, which include electric field operation, resistivity, and charge yield [11].

Table 2: A comparison of different direct radiation detectors' properties

Property \ Detector	a-Se	PbO	HgI_2	CdZnTe
Typical Operating Electric Field [V/μm]	10 to 20	5	1 to 2	0.1
Resistivity [Ω-cm]	10^{14} to 10^{16}	10^{12} to 10^{13}	10^{12} to 10^{13}	3×10^{10}
Charge Yield [e^-/keV of radiation]	20 to 30	60	100	200

As shown, though it has a lower charge yield (also called conversion gain in literature) than the other detectors, a-Se has the highest resistivity, which makes it extremely appealing for low noise tolerance applications such as breast cancer imaging. This is in addition to the fact that a-Se can be vacuum evaporated and deposited as a uniform thick film in large areas over top of the readout electronics in flat panel imagers. Competing detectors are mired in difficulties that don't allow them to be mass-produced or used over a large area. CdZnTe, for example, which has a crystalline structure, suffers from an expensive and poor-yield process and can only be grown in small sizes. These advantages have led to a-Se being the single prevalent direct detector of choice for commercial X-ray imaging.

1.3 Integration of CMOS and Selenium: Motivation for a Selenium-CMOS X-ray Sensor

The discussion so far leads to the conclusion that an imaging solution that integrates CMOS technology for the pixel architecture with amorphous selenium as an X-ray detector would have very promising results for the field of medical imaging. It would allow for pixel architectures such as the APS ones illustrated in this chapter to be fabricated at small pixel

sizes to allow for high-resolution images with fast readout and low noise susceptibility, taking advantage of the reliability and robustness of CMOS technology. Indeed, the purpose of this research is to take the first step towards a CMOS-based array integrated with a-Se serving as a high-performance imager for medical applications.

Chapter 2

Design and Implementation of Integrated Selenium-CMOS PPS Array

This chapter begins by illustrating the design and layout of the 8×8 array fabricated in 0.18 μm CMOS technology. It follows by detailing how the amorphous selenium X-ray detector was deposited on the chip after providing background on how the detectors are fabricated, as well as detailing the final integration steps taken to get the device ready to be tested.

2.1 Design and Layout of CMOS 8×8 PPS Array

To show the feasibility of a CMOS readout array integrated with an a-Se detector, a CMOS chip had to be fabricated. The PPS architecture was chosen for the array due to its simplicity and to serve as a first step in showing that CMOS technology can be integrated with a-Se.

The chip was designed and laid out using Cadence Design Systems's electronic design automation software suite, commonly known as Cadence, and fabricated in the 0.18 µm process through CMC Microsystems, which is the de facto official manufacturer for silicon designs in academia in Canada. Based on the wafer space granted by CMC for this project, the 8×8 array was chosen to have a 40 µm pixel pitch. The 0.3 mm-thick CMOS die would have an area of 1.0 mm × 2.8 mm, which meant an 8×8 array of 40 µm pixels could be nicely laid out at the top portion of the chip, leaving plenty of space for the bond pads.

Like any other large design, a bottom up process was used to create single cells that could then be instantiated repeatedly as part of the overall block. The array design began with the schematic and layout of a single PPS pixel. The screenshot of the Cadence schematic of the cell is shown in Figure 5.

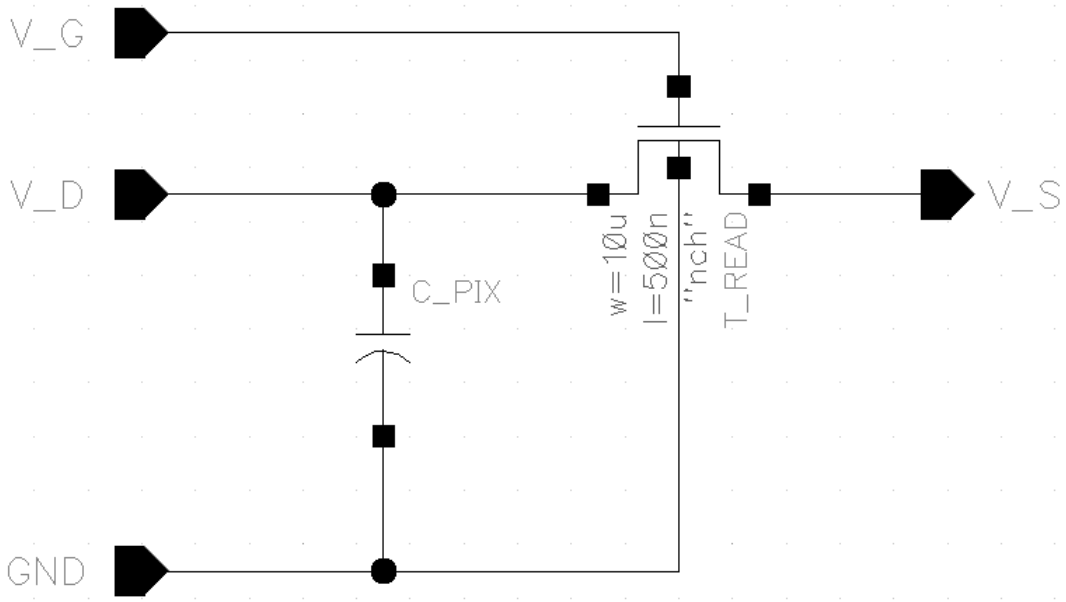

Figure 5: Cadence schematic of a single PPS pixel cell

This block contains the PPS read transistor as well as the pixel capacitor, and has four pins: V_G (the read line, connected to the gate of the PPS transistor), V_S (the data line, connected to the source of the transistor), V_D (the pixel detector node on top of which the detector will be placed), and GND, which is to be connected to ground in order to ensure proper operation of the NMOS transistor by grounding its substrate.

The layout of the single pixel cell is shown in Figure 6. The NMOS transistor was laid out in the bottom right corner of the pixel, with a channel width of 10 µm and a channel length of 5 µm. The drain contact of the transistor was connected to the top metal layer of the CMOS process, the *metal6* layer, which was made to exist over the entire active area of the pixel. This layer, which also made up the top electrode of the pixel capacitor (explained further below), was exposed by forgoing the top layer protective oxide over this area, to allow for the a-Se detector to be deposited on top of it and accumulate charge on the node.

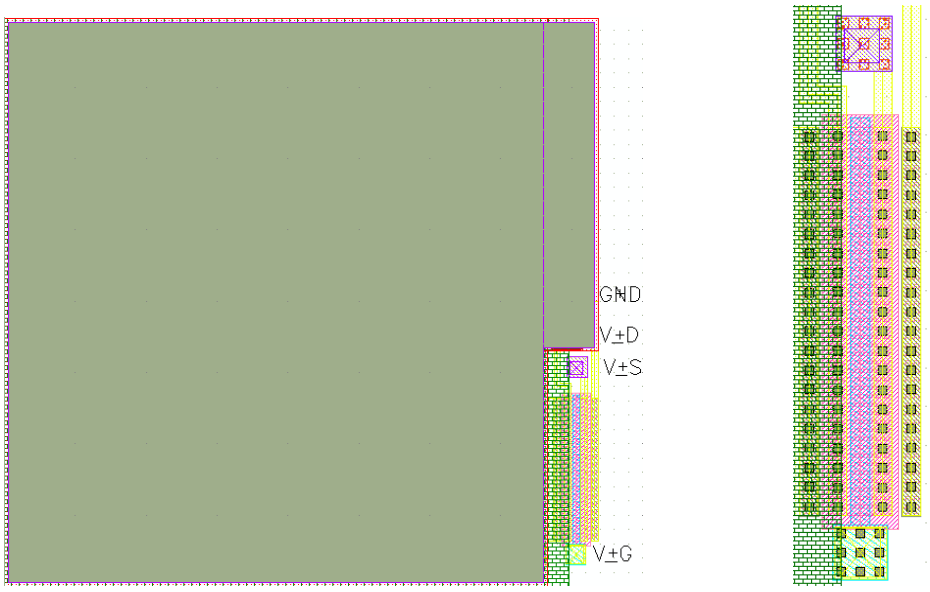

Figure 6: Layout of a single CMOS PPS pixel. A closeup of the PPS transistor in the bottom right corner of the pixel is shown on the right.

The shaded gray area in Figure 6 represents the area for which the *metal6* layer of the CMOS process was exposed, which also represents the actual *active* area of the pixel which collects charge generated by photons striking the detector. Thus, the Fill Factor of the pixel, which quantifies the active area of the pixel in proportion to its total area, can be calculated by the following expression:

$$Fill\ Factor\ (\%) = \frac{Active\ Pixel\ Area}{Total\ Pixel\ Area} \times 100. \tag{6}$$

The total pixel area was $1600\,\mu m^2$, while the active pixel area was $1585.7\,\mu m^2$, since a small portion of the pixel area had to be used for the layout of the PPS transistor. This led to a pixel *Fill Factor* of 99.1%.

The pixel capacitor was made using the CTM layer of the CMOS process, with the area being $30\,\mu m \times 30\,\mu m$. The CTM layer is a special layer exclusively meant for making MIM (Metal-Insulator-Metal) capacitors integrated in the CMOS process. The CTM layer was connected to the *metal6* layer by placing several vias in an array throughout the 30μm x 30μm area, while the *metal5* layer was laid out over the entire pixel area. From here, the *metal4*, *metal3*, *metal2,* and *metal1* layers were only laid out around the perimeter of the pixel, as guard rings, and connected to each layer above through vias, meaning *metal5* was connected down to *metal1*. The *metal1* layer was then routed on the right side to the pixel's ground pin, causing the pixel capacitor to exist between the CTM layer and the *metal5* layer (ground) through the interlayer dielectric separating the two. Figure 7 shows a cross section of a pixel (not to scale) to illustrate how the capacitor was formed between the top electrode and ground. The vias are illustrated by the dark gray oblong vertical sections in between adjacent layers.

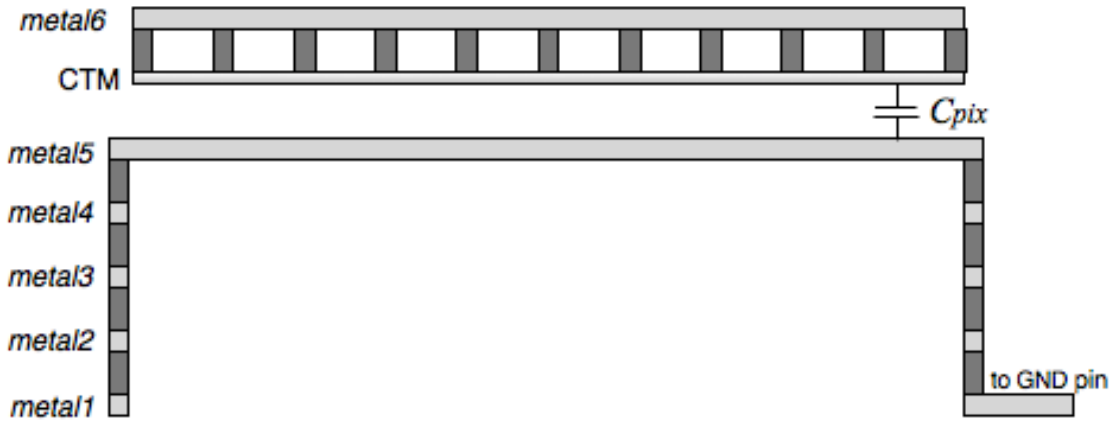

Figure 7: Cross-section illustration of a pixel on the CMOS die showing C_{pix} implemented as an integrated MIM capacitor between the top electrode and ground.

The pixel capacitor was desired to have a value of 1 pF. The capacitance of the pixel capacitor can be calculated by the following formula:

$$C_{pix} = \frac{\varepsilon_0 \varepsilon_{IMD5a} A_{CTM}}{d_{M5-CTM}}, \tag{7}$$

where $\varepsilon_0 = 8.85\text{x}10^{-12}$ F/m, ε_{IMD5a} (3.7) is the dielectric constant of the inter-metal dielectric separating the *metal5* and CTM layers, A_{CTM} is the area of the top electrode of the capacitor (900 μm^2), and $d_{M5\text{-}CTM}$ is the distance separating the two layers (30 nm) [13]. This resulted in an expected capacitance value of 982.35 fF. Following parasitic extraction of the layout view of the pixel cell in Cadence, the capacitance was given to be 951.75 fF.

The single PPS cell was then instantiated 64 times, in eight rows and eight columns to form the 8×8 array. The V_G nodes of every cell in a row were connected to each other while the V_S nodes of every cell in a row were connected to each other, such that the array had eight *read* line inputs – V_G1 through V_G8 – and eight *data* line outputs – V_S1 through V_S8. The array also had 64 V_D inputs, which would be where each pixel

accumulates charge on its pixel capacitor at the drain of the PPS transistor and corresponding to each individual cell's V_D pin. Figure 8 shows the arrangement of the 8×8 array's interconnections. This figure was drawn using schematic software as opposed to taking a screenshot in Cadence, which would not have been legible due to the amount of detail involved. Note that the V_D pins for each cell have been omitted as each pixel had its own, and the GND pins, which are common connected for all 64 pixels, have also been omitted.

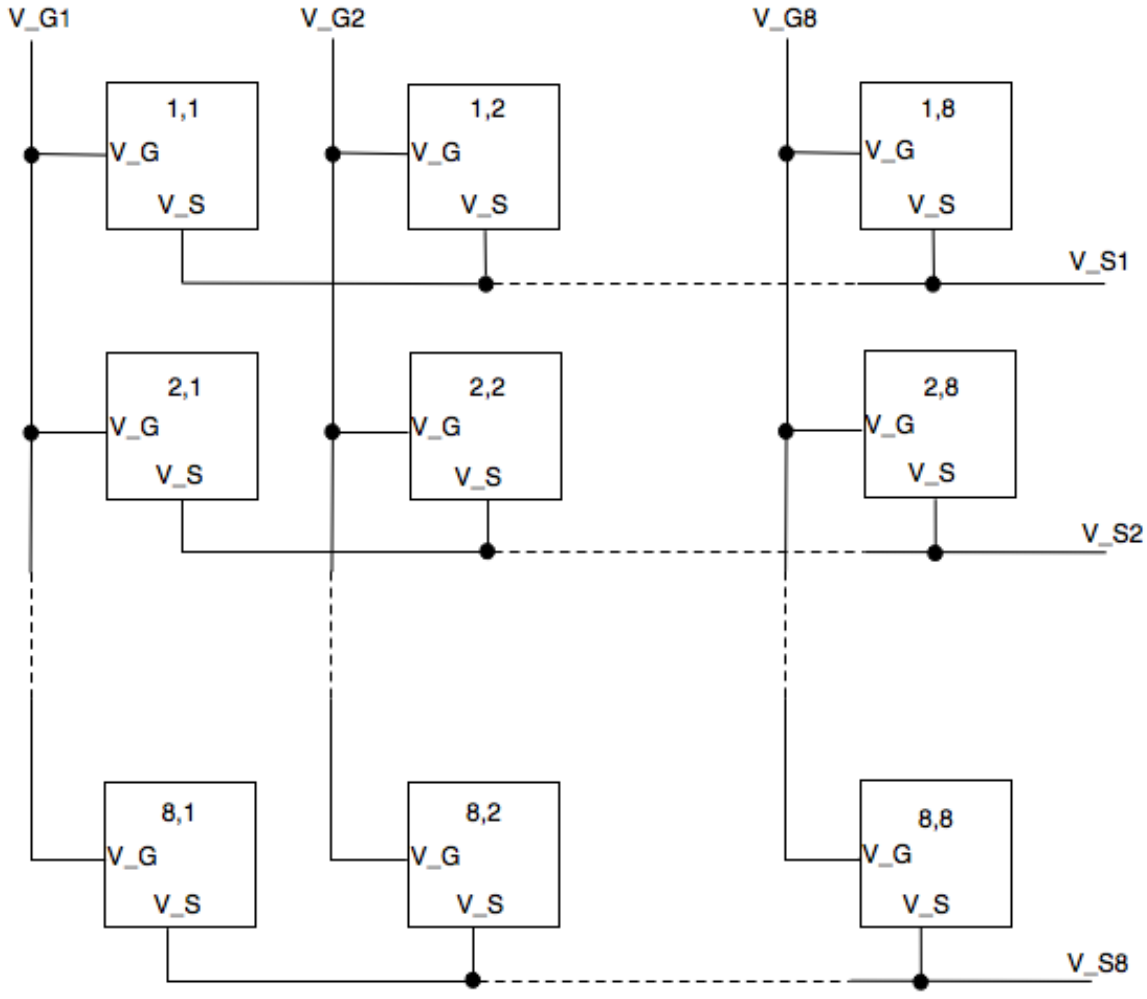

Figure 8: 8×8 PPS array interconnections

The layout of the array was made by instantiating the layout of the single PPS cell 64 times and interconnecting the pins in the same way as was done for the schematic cell. This made up the array cell in the bottom up design approach of the array. The last step was to instantiate this cell in the top level layout, which required bond pads for the input and output pins, and which was required to meet CMC's design rule constraints (DRC) which place minimum and maximum constraints on the density of each layer for proper mask fabrication. Figure 9 shows the top-level layout of the chip with and without the expanded sub-cell views.

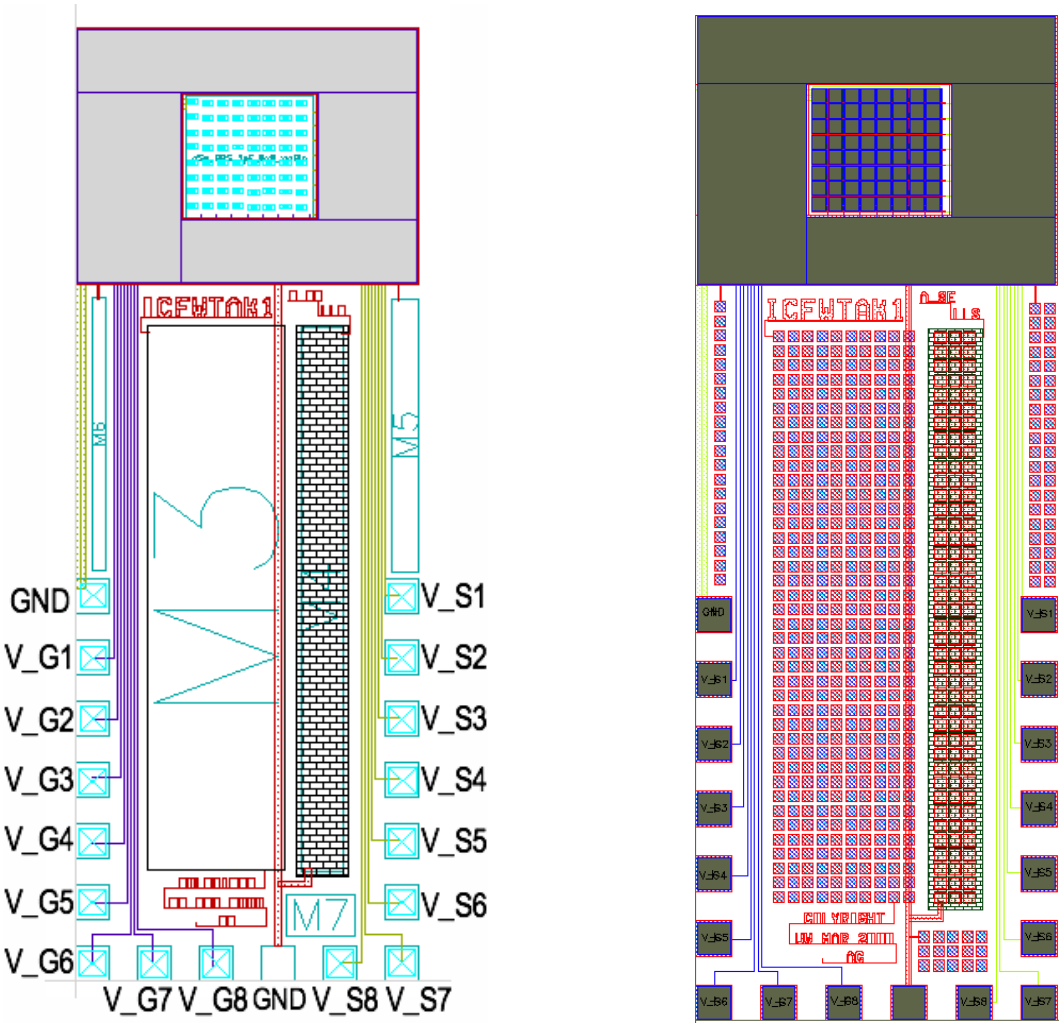

Figure 9: Full layout of PPS chip in Cadence; with expanded sub-cells (right)

The chip required 18 bond pads to be placed around the perimeter of the lower half of the chip, comprising of the eight read lines, eight data lines, and two additional ground bond pads. The *metal1* layer was used for routing the read lines (the gate nodes) to the left side of the chip and the *metal2* layer was used for routing the data lines (the source nodes) to the right side of the chip. The first bond pad on the left side of the chip was connected to the guard ring that was placed around the array area as well as the ground pins of the PPS array, which were connected to the capacitor's bottom electrode and the substrate contacts of the transistors as described earlier and shown in Figure 7.

This was followed around the perimeter by the eight read lines V_G1 through V_G8. A number of metal fills had to be placed in each layer to meet DRC, all of which were connected to the next bond pad, which was to be grounded. This made up a significant portion of the area in the middle of the chip, as seen by the large rectangular boxes comprising of the metal fill cells in the un-flattened cell view in Figure 9 (M3, M5, etc). The remaining eight bond pads were used for the eight data lines V_S1 through VS_8, which were organized with V_S8 on the bottom and V_S1 at the top.

Figure 10 is a die micrograph of the chip fabricated by CMC, taken under a high-magnification microscope at the University of Waterloo Giga-to-Nanoelectronics Lab.

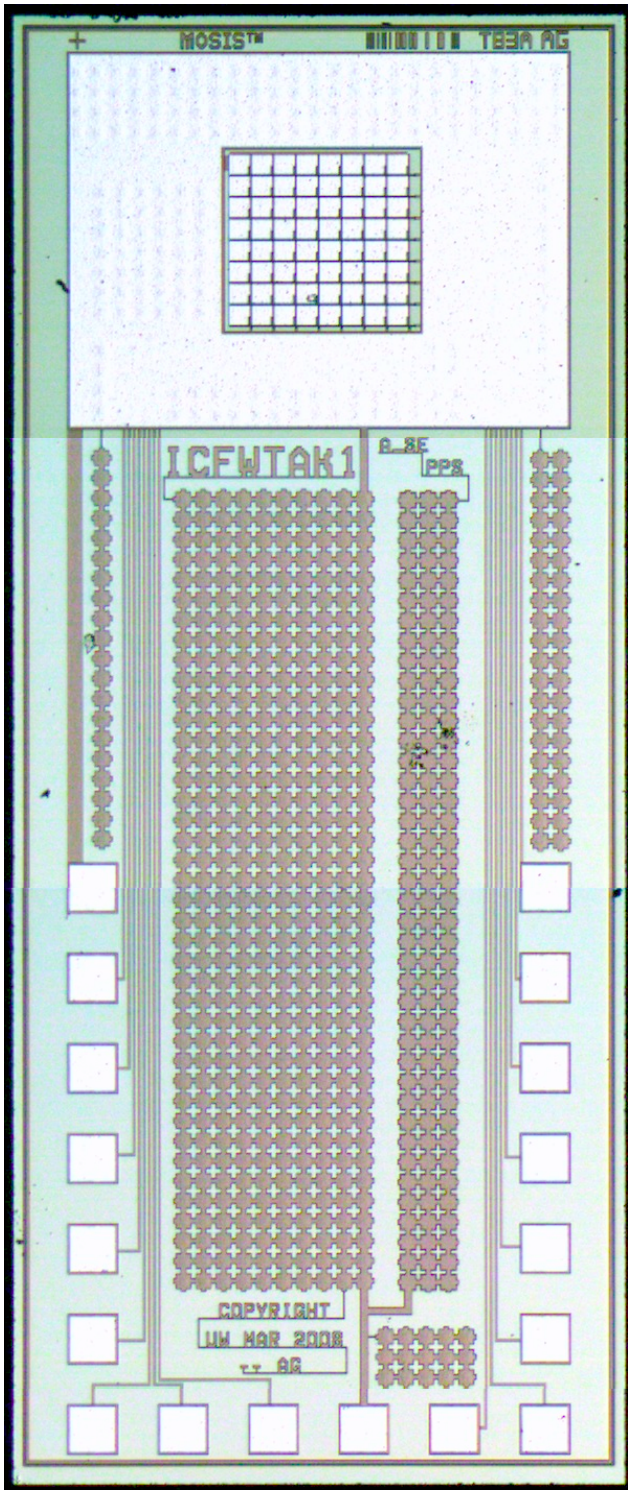

Figure 10: Micrograph of the 0.18 µm CMOS PPS die fabricated through CMC

2.2 Amorphous Selenium: Structure, Fabrication, and Integration with PPS Chip

Amorphous selenium is deposited as a film onto a substrate using vacuum evaporation. When it is struck by X-ray photons, electron-hole pairs (EHPs) are generated inside its structure, which can then be separated via an electric field to generate photocurrent. The following section describes in detail the structure of amorphous selenium, how it is prepared for the vacuum evaporation process, and its integration with the CMOS PPS chip in order to allow for testing of the 8×8 array.

2.2.1 The Structure of a-Se as an X-ray Detector

Amorphous selenium's structure contains under- and over-coordinated charged defects called valence alteration pairs (VAPs), which cause its amorphous nature. These VAPs are illustrated in Figure 11 below.

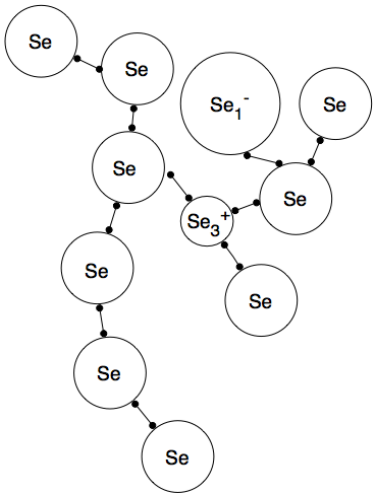

Figure 11: The structure of an amorphous selenium (a-Se) chain, showing its charge defects and amorphous nature (adapted from [14])

The under-coordinated charged defects correspond to a singly bonded negatively charged centre (Se_1^-) and the over-coordinated charged defects correspond to a triply bonded positively charged centre (Se_3^+). These VAPs are present in the absence of dangling bonds and contribute to the optoelectronic properties of a-Se. This is why selenium only maintains its photodetective properties in its amorphous state, and not its crystalline state. Unfortunately, the structure of a-Se, left to itself without encapsulation, is prone to crystallization over time (ranging from months to years based on ambient conditions), causing its performance as a detector to degrade until it loses its photogenerative properties completely [14].

Extensive research has been done in the study of alloying a-Se to prevent this unwanted crystallization, while also improving its charge transport characteristics to prevent trapping of the generated EHPs (thus increasing carrier lifetime) [15]. It has since become established that alloying a-Se with a small amount of arsenic (As) in the range of a few tenths of a percent, and doping it with a few parts per million (a microscopic amount) of a halogen like chlorine (Cl) combine to give the desired performance from the detector. The As and Cl in the specified amounts alter the structure of a-Se to provide the correct balance of VAP charge defects to result in good carrier transport and increased consistency to prevent crystallization. The a-Se structure that is used in flat-panel detectors is referred to as stabilized a-Se and contains 0.2% to 0.5% As doped with 10 to 40 parts per million Cl [14]. The alloying of selenium with these impurities has to be done prior to vacuum evaporation to form solid, stabilized selenium pellets which can then be evaporated and deposited.

2.2.2 Deposition via Vacuum Evaporation

Vacuum evaporation involves heating an evaporant in a vacuum by employing a large current through a container in which it is placed. For the fabrication of amorphous selenium detectors, the evaporant comes in the form of alloyed a-Se pellets which have been refined and alloyed to the desired composition. There are vendors that specialize in making these alloyed a-Se pellets with different compositions to suit their customers' needs. The process of making these a-Se pellets begins with the purification and refinement of selenium, the horizontal zone refining method [16]. A quantity of solid selenium is melted into a continuous solid mass to be vacuum distilled. This is done in a vacuum with the material being heated to over 100°C in order to remove residue water vapour and organic contaminants. The selenium is then melted into an oblong ingot (a metal mold) at a temperature of about 250°C for two hours and stretched over a foot in length, which is then cropped by removing the impure ends mechanically, leaving the purified selenium ready for use in the synthesis of the alloyed a-Se.

The refined selenium is placed with previously synthesized Se-As and Se-Cl alloys and mixed thoroughly within an alloying reactor, which is heated in a controlled manner to well above the melting point of selenium. The melt is homogenized by a rapidly rotating impeller, and then slightly cooled, though still remaining above 300°C. Shotting is then performed on the melt on a cold shotter plate (kept at a few degrees Celcius). This quenches the melt due to the rapid decrease in temperature, which allows it to form an amorphous structure. This produces the alloyed a-Se pellets, which can now be used in the vacuum evaporation deposition process.

Vacuum evaporation converts the solid a-Se pellets from their condensed state to their vaporous phase to be deposited as a film on top of the target surface. This method of depositing a-Se as a thick film using conventional thermal evaporation in a vacuum coater has been used extensively to fabricate a-Se since the 1960s, when it was the photoreceptor of choice in photocopiers [17]. The deposition of a-Se onto flat-panel thin-film transistor flat-panel arrays is done in the same basic way, and in industry, large vacuum reactors are used to coat multiple panels at the same time, making the process highly efficient. Figure 12 below shows the process that takes place inside such a vacuum chamber.

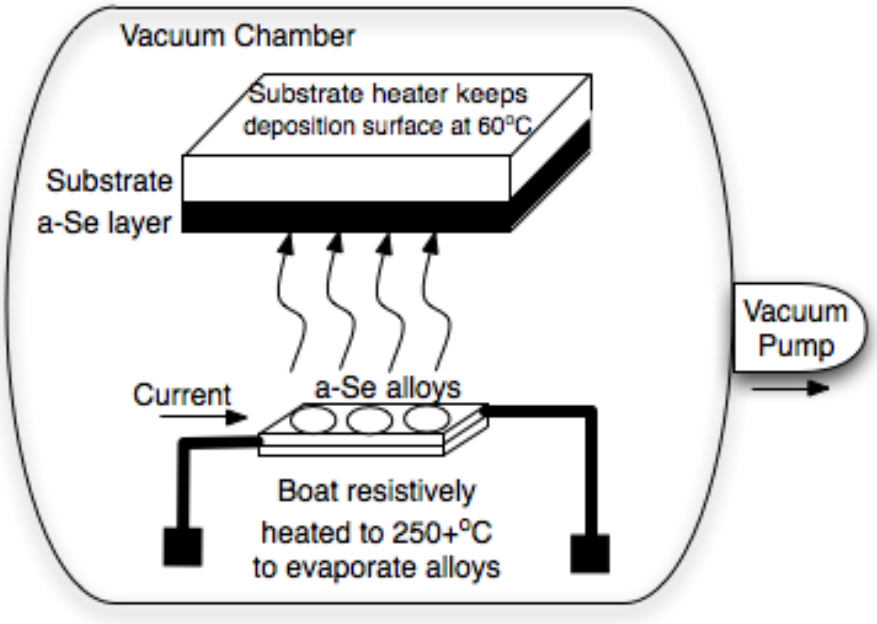

Figure 12: Amorphous selenium is evaporated and deposited as a film on the target substrate, the flat panel imager.

The chamber is kept at a pressure of 10^{-6} torr during this process. Alloyed a-Se pellets are placed into a stainless steel boat which is resistively heated by having current driven through it. The boat is heated to upwards of 250°C while the deposition surface is maintained

at about 60°C to 65°C. The latter condition must be maintained to allow the selenium vapour to form a film, since its glass transition temperature is about 55°C. The vapour from the evaporation of the pellets settles onto the panel acting as the substrate for deposition, forming the a-Se X-ray detecting layer. With the evaporation temperature of a-Se being relatively low at about 230°C, the flat-panel array is not damaged, and furthermore, the process is over with rather quickly, as deposition rates are on the order of 2 μm to 4 μm per minute. This means that a 200μm film can be coated in under an hour. This is one of the advantages of a-Se as an X-ray detector – panels can be manufactured separately and/or independently and then sent for a-Se deposition. While a-Se is not the only photodetector that can be deposited in this manner, other semiconductors often result in polycrystalline films and require high-temperature annealing to eliminate defects.

2.2.2.1 Potential Issues during Deposition

It should be noted that this process is not without its problems. During the evaporation and deposition process, changes take place in the vapour as well as the film composition as the material is continuously evaporated from the boat. Temperature non-uniformities in the boat, finite material thermal conductivity, and limited diffusion in the source material all contribute to a detrimental effect in the deposition called fractionation [14]. Fractionation refers to the fact that the concentration of As is higher at the surface of the photoconductor film than the rest instead of being uniform throughout.

This fractionation effect has been examined and qualitatively explained [18,19]. The source material becomes inhomogeneous as the selenium-rich initial vapour leaves its surface region, leaving behind a surface rich in As. Methods to minimize this effect have also been

proposed through trial and error, with one study showing that when the initial source material (the a-Se pellets) has its surface crystallized by vigorous tumbling, the effects of As fractionation are severely reduced. The fractionation of Cl, however, is not practical to investigate since the concentration is so small, and no studies have been done to directly investigate the doping profile of Cl in the grown a-Se film.

2.2.3 Integration of a-Se Detector with CMOS PPS Array

The fabrication of the a-Se detector on top of the CMOS PPS chips was done at the Electronic Materials and Devices Research Centre at the University of Saskatchewan. The deposition of the a-Se detector was done in two layers. The composition of the alloyed selenium used for the first layer of evaporation was 0.3% As and 2.5 ppm Cl, known to be a very stable composition with good charge transport properties. The substrate temperature was kept at 60°C while the boat temperature for evaporating the alloy was 295°C. Deposition was done for 22 minutes to deposit a layer of a-Se from this alloy that was 67 μm to 68 μm thick. The second layer used a slightly different alloy composition, at 2% As and doped with an Alkali metal as opposed to Cl. This alloy was evaporated for four minutes while the substrate was kept at 60°C and the boat was kept at 310°C, resulting in a layer of about 8 μm to 9 μm being deposited on top of the previous layer. This gave a total thickness for the a-Se detector of about 75 μm. The use of the higher As-rich alloy for the much thinner top layer trades off charge transport in exchange for higher resistivity at the surface, which keeps the leakage current of the a-Se detector low.

Masks had to prepared to ensure that a-Se was not deposited on the entire chip, as only the active array area was the target, and the lower portion of the chip needed to be left

exposed so that the bond pads connected to the read and data lines of the PPS array could be accessed for wirebonding. Additionally, a secondary mask was required to place the 4 µm to 5 µm thin, transparent chromium (Cr) contact on top of the a-Se film, to allow for an electric field bias voltage to be applied on the detector. This mask had to ensure that the electric field was not applied on the entire a-Se surface, as around the edges the thickness of the film was less than 75 µm, which could result in the breakdown of the detector. A mask with a circular opening diameter roughly equal to the array area was used and positioned on top of the array as the Cr contact was deposited over top of the active array surface in a metal evaporator. Figure 13 is a high-resolution micrograph of the sample's active area after the a-Se detector was deposited on the CMOS chip and returned from Saskatchewan.

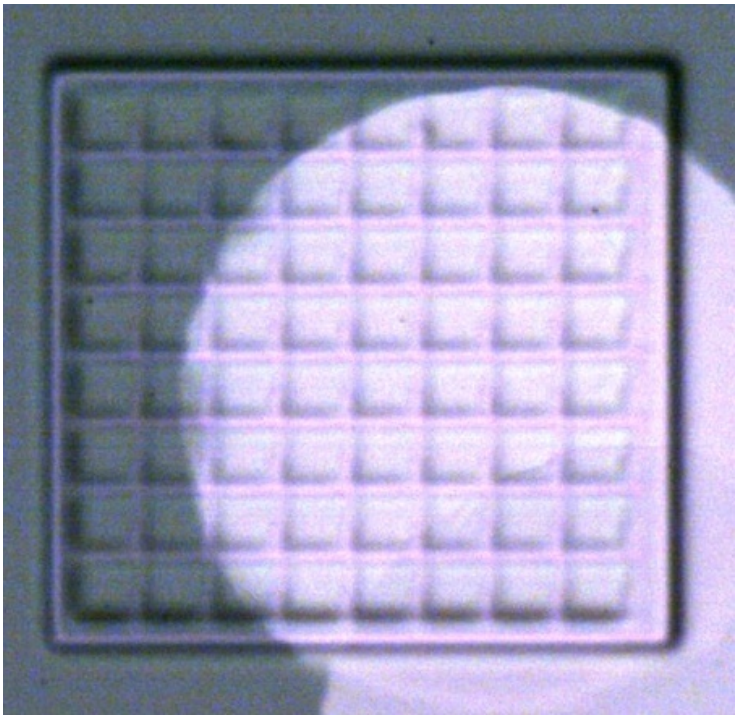

Figure 13: Amorphous selenium on top of the 8×8 active array area. The lighter circular area is the chromium top contact used to apply the electric field bias.

2.2.3.1 Post-Deposition Preparation

Now that the a-Se detector had been coated onto the chip, it had to be placed on a specially designed printed circuit board (PCB) substrate, or daughterboard, such that it could be held in place while being wirebonded and to allow for easy integration with the testing environment. The daughterboard is shown in Figure 14 below, designed and fabricated alongside the test PCB which will be described in Chapter 3. The pads around the edges of the large pad at the centre correspond to the bond pads on the chip, which comprise the read and data lines of the passive pixel sensor array.

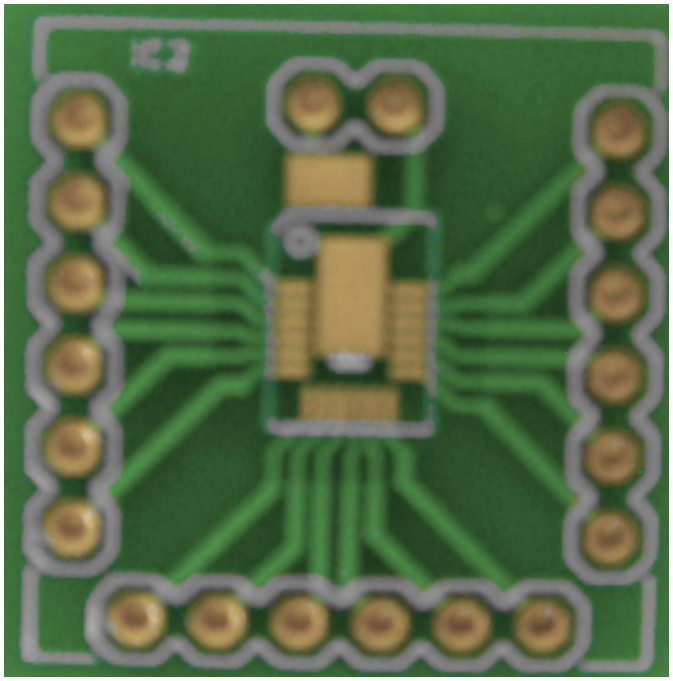

Figure 14: PCB substrate (daughterboard) used to hold the CMOS image sensor.

The contacts on the daughterboard were coated with gold to ensure minimal contact resistance and good adhesion for wirebonding. The large pad at the centre of the daughterboard is the cavity, where the die was placed. To affix the die to the daughterboard,

an epoxy was required which was conductive (to ground the bottom surface, the body of the die) and could cure at room temperature (since a-Se can crystallize at temperatures as low as 45˚C). The solution used was Colloidal Silver Paste made by PELCO, which provides high adhesion while being electrically conductive and curable at room temperature. A small drop of the silver paste was placed using a syringe needle tip in the middle of the cavity and allowed to settle as the die was placed on top of it. The paste was given 24 hours to cure at room temperature, per the manufacturer's instructions.

Once the die was confirmed to have been solidly attached to the daughterboard, it was ready for wirebonding, which was done in the Giga-to-Nanoelectronics Lab at the University of Waterloo. Figure 15 shows the wirebonding diagram used (not to scale).

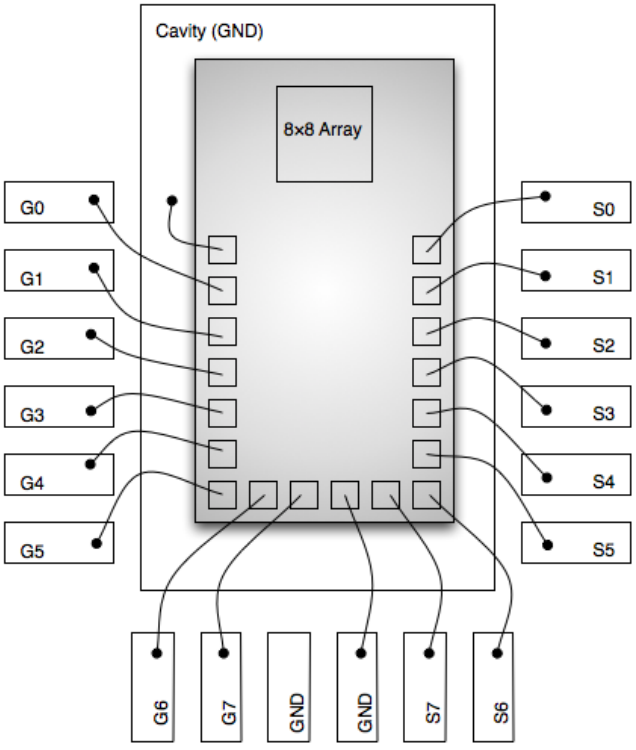

Figure 15: Wirebonding diagram used for connecting bond pads to the daughterboard

The pads labeled G0 through G7 are the eight read lines of the array connected to the PPS gates (V_G1 to V_G8) which need to be asserted for readout, and the pads labeled S0 through S7 are the eight data lines of the array connected to the PPS sources (V_S1 to V_S8), which will be connected to the charge amplifiers externally. The remaining two wirebonds are used to ground the metal guard ring around the array and the substrate contacts (bonded to the grounded cavity) and the metal fills on the chip (bonded to the ground pad at the bottom).

Next, the pad above the cavity had to be connected to the top contact of the a-Se layer on the chip so that a high-voltage contact could be made to bias the detector during operation. This was an intricate process and took several different attempts before an optimal solution was reached. The material used to make the contact could not be too thick or it would block the active area of the array, and once it was placed on top of the array, it had to stay there without drifting from its place or being lifted off the contact.

To accomplish this, a single strand of a solder wick strip was soldered to the daughterboard pad, while the other end was carefully placed on top of the Cr contact using tweezers under a microscope. To ensure it stayed properly in place, a drop of a transparent, non-conductive Lepage epoxy made by mixing a drop of the epoxy's resin and hardener was put on the sample. This encapsulated the top contact wire as well as the wirebonds, effectively protecting the entire sample. Finally, single-strip header pins were soldered to the daughterboard's output connection vias to allow for easy probing of the pins during testing. Figure 16 shows the CMOS chip wirebonded to the daughterboard and encapsulated with the transparent epoxy, ready to be tested.

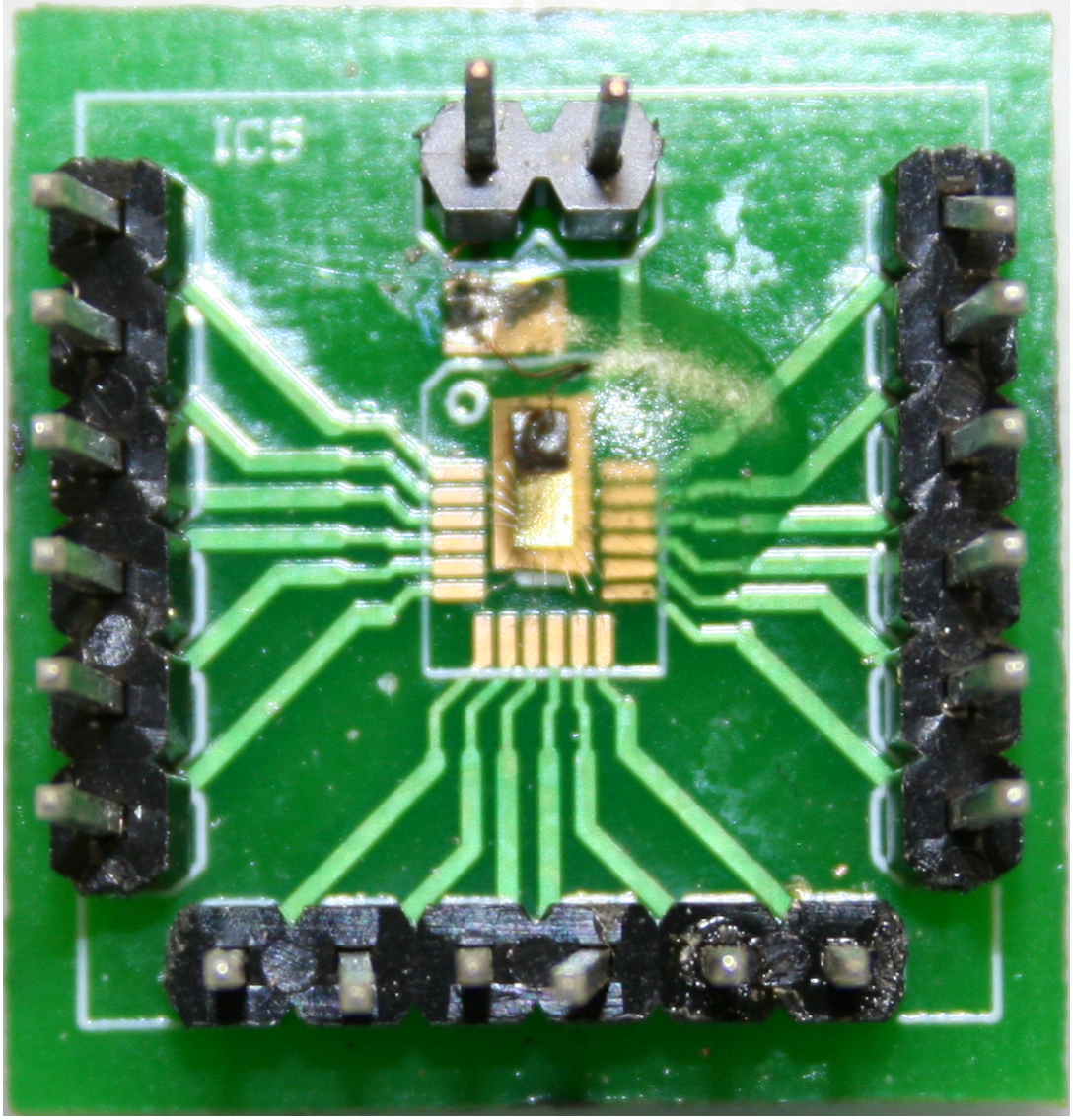

Figure 16: CMOS PPS chip wirebonded to daughterboard and encapsulated in protective non-conductive transparent epoxy

Chapter 3
Design and Assembly of PPS Readout Printed Circuit Board

A printed circuit board (PCB) was designed and fabricated in order to allow for the driving stimulus for the PPS array and to capture its output with readout circuitry. This chapter outlines the parts used in the design and how they were integrated together on the PCB. CadSoft's EAGLE software was used for the schematic design and board layout.

The design process involved outlining the requirements of the test system, selecting the components that were required and creating an EAGLE library to use them, and, following schematic entry, doing the PCB layout and sending it to fabrication. The design used surface mount (SMD) components almost exclusively to allow for a clean and compact layout. Figure 17 shows a generalized top-level block diagram of the PCB to illustrate the major components and how they interact with each other.

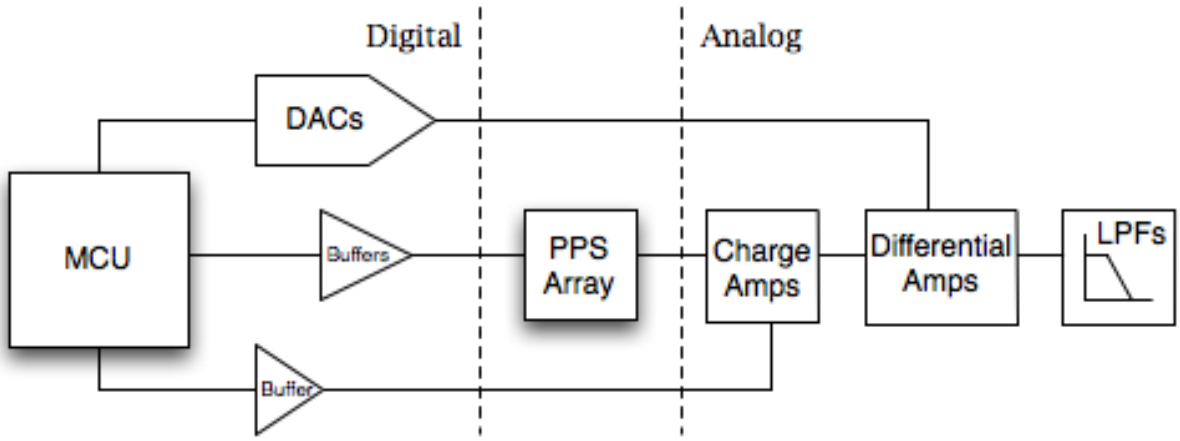

Figure 17: Block diagram of the PCB used for testing the PPS array.

3.1 Voltage Regulators

The operation of chips on the PCB requires the existence of DC voltage sources, implemented by voltage regulators which take a DC input voltage and regulate it at the required supply voltage. Digital parts on the PCB required positive voltages of 1.8 V and 5 V, while analog parts required differential voltages of +/-5 V to allow for signals to swing above and below zero volts. Thus, a DC input to the board of +/-9 V would suffice to allow for the required voltages, utilizing large decoupling capacitors of 220 μF.

Mixed-signal design convention calls for separating analog and digital power supplies and ground planes to isolate noise, current draws, and other crosstalk between the devices. Hence, four voltage regulators were required to generate 1.8 V, 5 V (digital), 5 V (analog), and -5 V. The former two were connected to a digital ground plane which was separated from the analog ground plane serving the latter two. The digital and analog ground planes would

be used for the parts requiring each respective type of power in conjunction with their voltage rail.

3.1.1 5 V Regulator

Since the PCB required 5 V to be generated twice, two instances of the same part could be placed on the board to generate the digital and analog 5 V rails separately. The part chosen was the ADP3303 in the 8-pin surface mount SOIC package, made by Analog Devices, which provides a stable output of +5 V (+/-0.8%) for input ranges 3.2 V to 12 V. A decoupling capacitor of 0.7 µF was used at the 5 V output to keep the voltage stable.

3.1.2 1.8 V Regulator

The 1.8 V supply was required for several of the digital parts. The part used was Texas Instruments's TPS766 in the 8-pin surface mount SOIC package, which provides a stable output of +1.8 V for input ranges 3.3 V to 10 V. A decoupling capacitor of 0.7 µF was used to ensure output voltage stability.

3.1.3 -5 V Regulator

While negative voltage regulators are rarer in existence than their positive counterparts, Linear Technology's LT1175 in the 8-pin surface mount SOIC package was eventually chosen as the solution for providing a -5 V rail for the dual-supply analog parts on the PCB. A decoupling cap of 0.7 µF was placed between its output and ground (with the positive electrode connected to the ground plane).

3.2 Microcontroller

At the heart of the digital side of the PCB is a microcontroller, which governs the operation of the chip by providing the input signals. The microcontroller chosen was the MC68HC908MR32, part of the M68HC08 family of microcontrollers made by Freescale Semiconductor, in the 64-pin QFP package. The microcontroller (MCU) uses an 8 MHz system clock, two separate timer modules comprising of six channels together, and a serial-peripheral interface (SPI) module for easy interfacing. It uses the digital 5 V power supply.

The software running on the MCU was written in assembly using a laptop running the Metroworks CodeWarrior software development kit. Interfacing from the laptop to the MCU on the board was done using the FSICEBASE support board, which connects to the laptop via USB and to the PCB through a 6-pin programming cable. This allowed for assembly code to be written, compiled, and programmed onto the MCU's programmable read-only memory (PROM) for standalone operation, as well as real-time step through debugging while connected to the laptop through the FSICEBASE.

3.3 Buffers

Two buffering chips were used in between the MCU and the targets it was used to drive. The buffers were necessary to protect the MCU from sinking too much current through its output pins. The buffers would also allow for shifting of the high logic level from the MCU's 5 V level to the PPS array's 1.8 V level.

3.3.1 1.8 V Gate Driver Buffer

The PPS array was fabricated using 0.18 μm CMOS technology, for which the high logic level is 1.8 V. As such, the stimulus signals – the read lines connected to the gates of the PPS transistors in the array – needed to be shifted down to 1.8 V logic from 5 V logic, which the MCU uses. This was done via Toshiba's TC74LCX541 chip containing eight buffers in a 20-pin TSSOP package, which used the 1.8 V digital power rail. All eight buffers were used to convert the eight read signals to 1.8 V logic, which could then be connected to the array safely.

3.3.2 5 V Reset Signal Buffer

The other stimulus signal the MCU was responsible for outputting was the Reset signal to the charge amplifiers on the analog readout side, which had to be done after each integration cycle to reset their output level. This signal was buffered using Toshiba's TC74VHC541 chip containing eight buffers in a 20-pin TSSOP package, which used the 5 V digital power rail, one of which was used to buffer the reset signal.

3.4 Digital-to-Analog Converters

The MCU was also responsible for programming eight digital-to-analog converters (DACs) on the PCB through its SPI module. Each DAC would output an independent voltage based on the digital word written to it by the MCU. The use of these voltages, one per line, was to cancel out the deterministic noise injected into the system at the output of the charge amplifier, by feeding the pair of signals into a differential instrumentation amplifier. The DACs used were Maxim MAX5170 chips in 16-pin QSOP packages, which used the 5 V

digital rail. An ADR440BRZ voltage reference chip in an 8-pin SOIC package from Analog Devices was used to provide a reference of 2.048 V to the eight DACs, which provide 14-bit precision in the voltage range from 0 V to 4.096 V at full scale.

3.5 Charge Amplifiers

The operation of the charge amplifier as an integral part of a PPS readout system was covered in an earlier chapter. The purpose of the charge amplifier is to provide a stable output voltage after readout based on the charge that is accumulated on the pixel capacitor during integration. The charge amplifier chip used was Burr Brown's ACF2101 in a 24-pin SOIC surface mount package, each of which contains two charge amplifiers. The chip requires a dual power supply of +/-5 V, and thus made use of the 5V and -5V analog voltage rails.

Because each ACF2101 chip contains two charge amplifiers, four parts needed to be used on the PCB, with each handling two channels of the readout. The feedback capacitor on the charge amplifiers was 1 pF to provide approximately unity charge gain, since the pixel capacitor's value was about 1 pF. The eight 1 pF capacitors used were surface mount with the 0402 footprint. The ACF2101 uses an active low reset signal, which, when asserted, closes a switch across its feedback path. This reset signal needs to be asserted after each integration cycle to close the switch in parallel with the feedback capacitor to discharge it and hence reset the output to 0 V. This signal is provided by the MCU through the 5 V buffer described earlier and shared amongst all eight charge amplifiers, which operate synchronously.

3.6 Instrumentation Amplifier

The output of the charge amplifier has the signal riding on a deterministic noise voltage, due to the fact that when the reset signal is deasserted and the switch across the charge amplifier is opened, an amount of charge is injected onto the feedback capacitor in a phenomenon referred to as charge injection. Thus, through the use of a differential amplifier stage, this constant level can be eliminated by connecting the charge amp output to its positive input and a DAC outputting the measured charge injection level to its negative input. So if the DAC level is calibrated correctly, the gain of the differential amplifier optimally amplifies only the signal part of the charge amplifier output.

The differential amplifier used was Analog Devices's AD8228 instrumentation amplifier, which provides two fixed gain settings, 10 or 100. The AD8228 selected was the 8-pin surface mount SOIC package using the +/-5 V analog rails.

3.7 Low-Pass Filter

The final stage of the analog signal processing was a low-pass filter designed to eliminate high-frequency noise on the signal. This was done with an active RC filter consisting of an opamp with a resistor and capacitor across its negative feedback path to set the cutoff frequency and a resistor at its input to set the filter gain. The opamp used was the Analog Devices AD8655 chip in an 8-pin surface mount SOIC package using the +/-5 V analog rails. The filter circuit is shown in Figure 18.

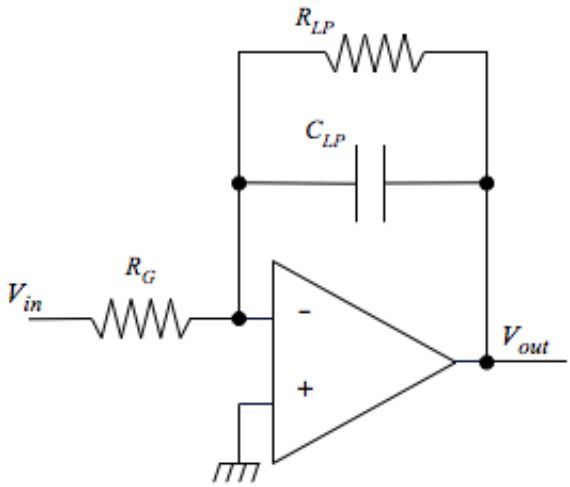

Figure 18: Low-pass filter used to eliminate high-frequency noise

The transfer function of the low-pass filter shown above is given by the following equation:

$$H(s) = -\frac{R_{LP}}{R_G}\left(\frac{1}{1+\frac{s}{1/R_{LP}C_{LP}}}\right), \tag{8}$$

where its cutoff frequency is $1/R_{LP}C_{LP}$ rad/s. Using R_{LP} = 100 kΩ and C_{LP} = 10 pF gave a cutoff frequency of 159 kHz. The value of R_G was also set to 100 kΩ to provide a unity gain low-pass filter.

3.8 Test Circuitry and Miscellaneous Features

To allow for independent testing of the analog readout circuitry from the array, eight 1 pF test capacitors were also added to the design (one per charge amplifier), which could be driven either by the MCU or externally via a function generator through an SMA connector on the board, chosen by a jumper. Figure 19 shows the setup of the test cap and the inputs, with the connection to the PPS array also shown in context.

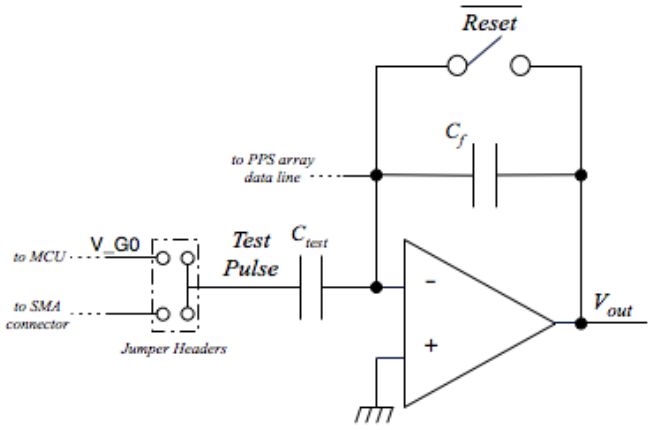

Figure 19: Test capacitor at the input of the charge amplifier, with a jumper choosing the driving mechanism

The jumper can be placed horizontally in the top row or the bottom row of the jumper headers, which would connect the test capacitors to either the input SMA connector or to V_G0, which is the MCU read line output connected to the first row of the array. By putting a voltage pulse at the input of the test capacitor (the node labeled Test Pulse in Figure 19), the output could be probed to show the charge gain (ideally unity) and the charge injection due to the reset switching could be measured for each channel, which would allow for the corresponding DAC to be set to output that same voltage.

The output of the eight charge amplifiers was also routed to a 2×8 connector to allow for easy probing via oscilloscope probes. The output of the analog readout channels, after the low-pass filter, was also routed to a 2×8 connector, and additionally to eight SMA connectors to allow for direct connection to an oscilloscope via an SMA to BNC cable. Finally, an ethernet connector was also placed on the board, to allow for the option of future interfacing with the MCU. Its built-in LEDs were hooked up to the 1.8 V and 5 V digital power rails, to

serve as status lights for quick confirmation that the voltage regulators were functioning correctly.

3.9 PCB Layout

The board was designed with the digital section on the left side, and the analog section on the right side, and the array in the middle. Figure 20 shows the board after it was populated by soldering the components in place, with the major sections labeled.

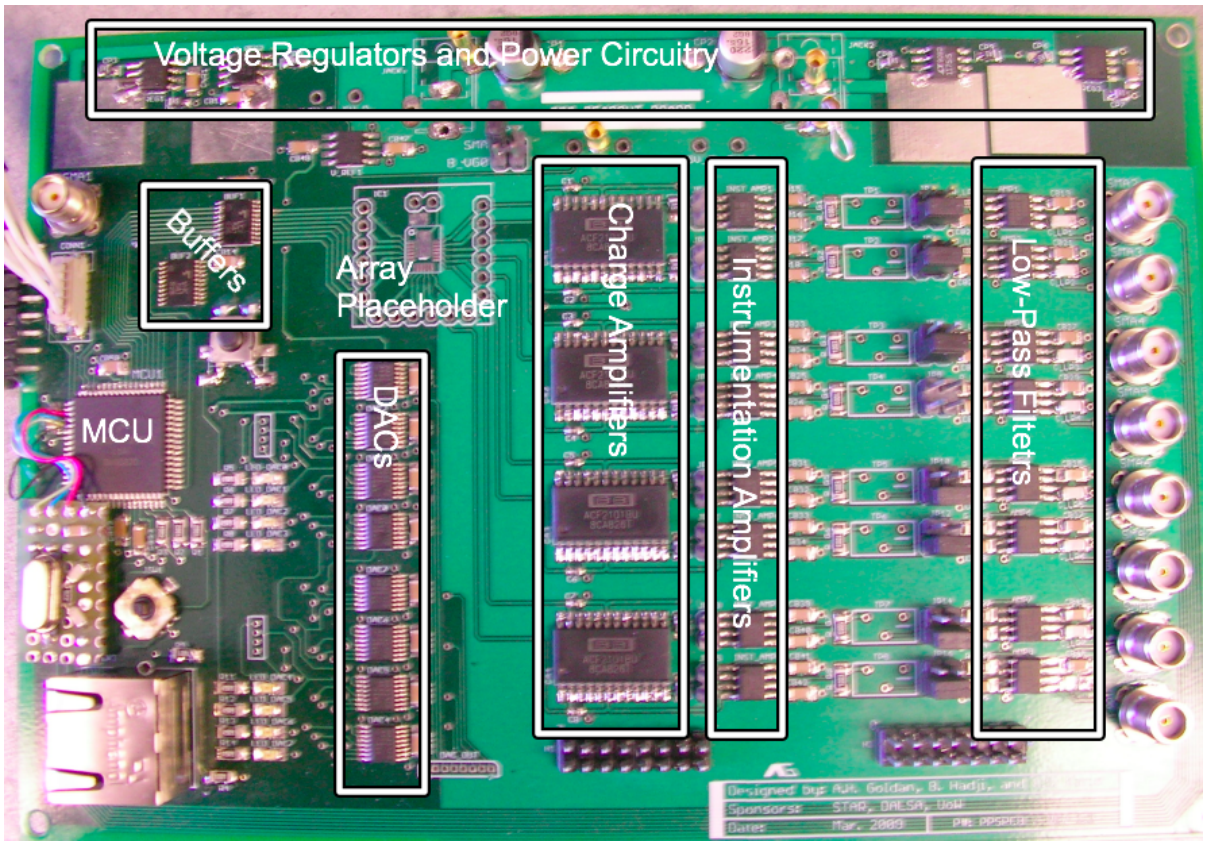

Figure 20: PPS readout PCB after population of components

The voltage regulators were placed at the top, with the two digital voltage regulators on the left side, and the two analog ones on the right. As seen above, each had a large pad at

its input to act as a heat sink. The MCU was placed on the left, with the eight DACs and the two buffers in close proximity. The placeholder for the PPS array was identical to the daughterboard, such that it could sit on top of the board with the header pins making contact with their corresponding vias on the board.

Signal routing was done mostly on the top layer, but rerouted to the bottom layer (the backside of the board) through vias where it was necessary. On both sides of the board, the analog and digital ground planes were filled around the respective components. The eight test capacitors were the only components actually placed on the backside of the board, as it was mostly used for signal routing that had to be rerouted to the bottom. Figure 21 shows the backside of the board. Placeholders were put in to allow for the option of using two 9 V batteries for the dual power supply as opposed to using an external power supply.

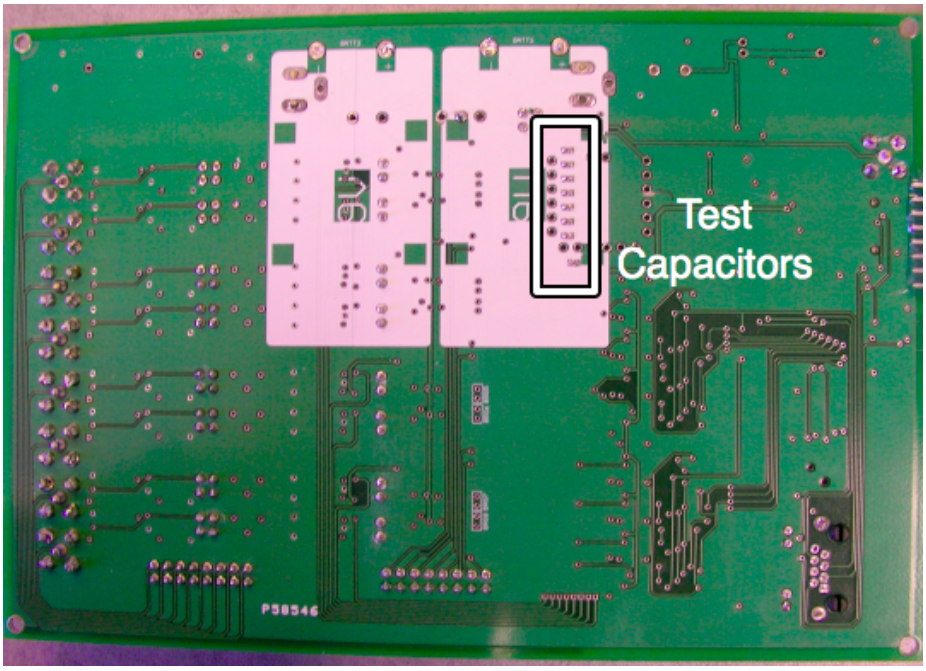

Figure 21: Backside of PCB, with test capacitors labeled

3.9.1 MCU Oscillator and IRQ/RST Modifications

Following the production of the board, it was discovered that an additional piece of circuitry was omitted in the initial design of the PCB, which was required for the proper operation of the MCU. The MCU required an external 8 MHz crystal oscillator to generate its system clock on-chip. The crystal oscillator used was CTS's ATS08ASM 8 MHz crystal oscillator with 20 pF load capacitance. The additional circuitry associated with the crystal is shown in Figure 22, which consists of two capacitors C_1 and C_2 on either side of the oscillator and a biasing resistor R_B in parallel with it, in addition to a third capacitor C_{filt} needed by the MCU's phase-locked loop for stability. C_1 and C_2 were specified to be equal to twice the load capacitance of the crystal, R_1 was specified to be 22 MΩ, and C_s was specified to be 9.625 nF.

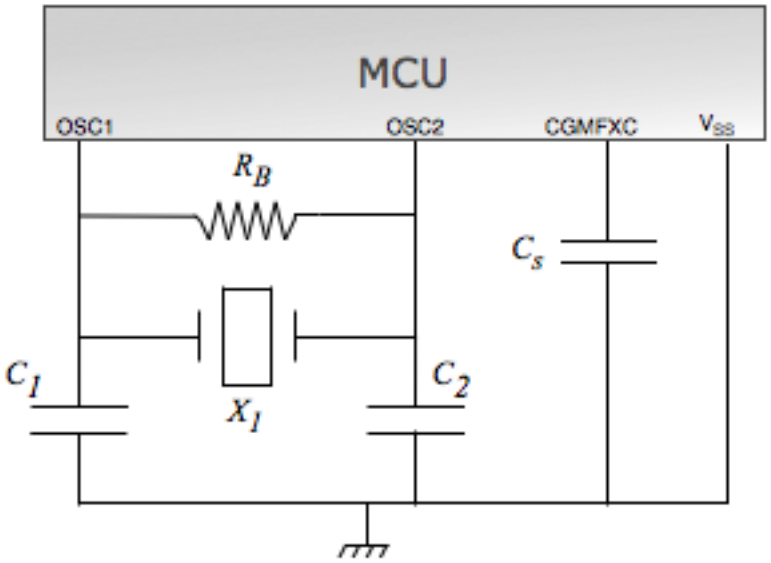

Figure 22: Crystal oscillator and external circuitry, with the MCU's associated pins

The resistor and capacitors chosen were surface mount components with a 1206 footprint, with values of 39 pF for C_1 and C_2, 22 MΩ for R_B, and 10 nF for C_s. The components were

soldered and put together on a small through-hole prototyping PCB, and glued to the PCB in the area between the ethernet connector and the MCU. The four pins (OSC1, OSC2, CGMXFC, and V_{SS}) on the MCU were all adjacent to each other on the left edge of the chip, and four wires were used to make these connections to the mod board.

The only other required post-fabrication modification to the PCB was also associated with the MCU. It has an external interrupt pin (IRQ) and an external reset pin (RST), both of which are active low and routed to the programming connector, as they are signals needed to program the MCU by the laptop through the FSICEBASE. It was noticed during the initial phases of testing that the programs downloaded onto the MCU would work while it was powered through the FSICEBASE board via the programming connector, but after the board was disconnected and powered up independently, the programs would not run properly (i.e., the MCU would be powered up but would not be outputting the signals it was supposed to on its data lines).

By comparing the signals on the board while the FSICEBASE was connected and while the PCB was powered up independently, it was deduced that the problem was due to the fact that the external IRQ and RST active low pins needed to be pulled up when they were not in use (i.e., when the MCU is not being programmed), such that they are deasserted. The FSICEBASE did this properly after programming, but when the PCB was powered up independently, the pins were left floating causing the MCU to permanently have its external reset asserted, halting its processing of the program.

To rectify this design omission, a 2×8 header pin fitting the programming connector was glued onto the edge of the PCB so that when powered independently, the programming connector could be connected to it. The pins on the connector corresponding to IRQ and RST were soldered to the 5 V digital rail on the PCB, and as such, when the programming connector was connected there and the PCB was powered up, the IRQ and RST signals would stay deasserted. Figure 23 shows a close-up of both of the modifications mentioned above, with the parts explicitly labeled.

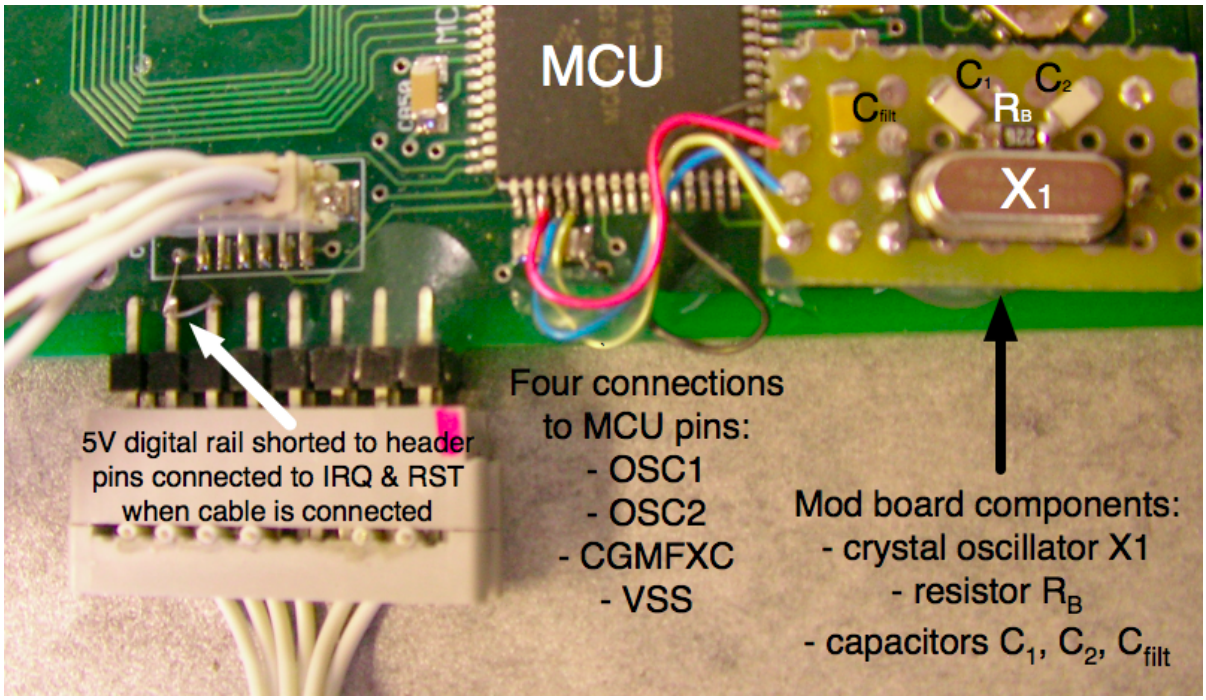

Figure 23: Post-fabrication modifications to the PCB associated with the MCU.

Chapter 4

Testing Results and Analysis

The following chapter outlines the methods and discusses the results of the testing of the CMOS PPS array, beginning with the CMOS die itself, the CMOS die with the integrated a-Se detector, and the tests conducted on the PCB readout board.

4.1 Validation of CMOS PPS Array

After the CMOS dies were returned from fabrication at CMC, before pursuing any further with the project, tests needed to be conducted to ensure that the chip was "alive," a term commonly used in the CMOS design field to mean that the circuits and transistors on a chip behave the way they are supposed to upon powering up for the first time after being fabricated. Since the only transistors on the PPS array were the readout transistors on each pixel, the easiest way to test for this was to perform a test to plot the current versus voltage (I-V) behaviour of a transistor on the die and ensure it was functioning correctly. An Agilent 4156C Semiconductor Parameter Analyzer (SPA) was used to conduct these measurements,

in conjunction with an Agilent 16442A Test Fixture used to probe the sample. A PC running Metrics Technology's Interactive Characterization Software (ICS) was used to interface with and program the SPA and to capture data.

To test a transistor on the PPS array, its gate and drain voltages needed to be swept while its drain current was measured. The gate and source terminals could be accessed using the bond pads for the read and data lines of the array, but there was no bond pad for its drain since that was the top layer of the array, where the a-Se detector was to be deposited. So initially, a bare CMOS die was wirebonded to a daughterboard in the manner shown previously in Figure 15, with an additional wirebond going from the contact meant for the high-voltage electric field bias to a pixel on the array. Because the pitch of the pixels was only 40 μm, the wirebond to the array touched more than one pixel, but the pixel transistor could be isolated by appropriately addressing the gate and source lines (e.g., using V_G1 & V_S8 as the gate and source nodes would be testing the transistor on the pixel at the bottom left corner of the array).

However, upon testing, it was found that the drain and source terminals were shorted for the pixels with which the wirebond made contact (the maximum current limit allowed by the SPA was being conducted through the drain node). This was because the mechanical effect of pressing the wirebond onto the array crushed the MIM capacitor underneath and shorted the *metal6* plane for that pixel to the metal5 plane, grounding the top electrode. This was confirmed because an adjacent pixel which only slightly came in contact with the wirebond's footprint on the array had its transistor work on an initial sweep before also succumbing to the same problem.

To mitigate this problem, a second bare CMOS die was wirebonded, and this time, instead of wirebonding to the array to get access to the drain, conductive silver epoxy was used to short the array to the surrounding metal fills around it, which were routed to the bond pad at the bottom of the array meant to be grounded. Instead, this was used as the drain contact for the transistor, which was actually connected to the drain of every pixel on the array's transistor. Figure 24 shows the I_D-V_{GS} curve obtained from the sample, while Figure 25 shows the same curve with the current plotted logarithmically to show the sub-threshold leakage of the transistor.

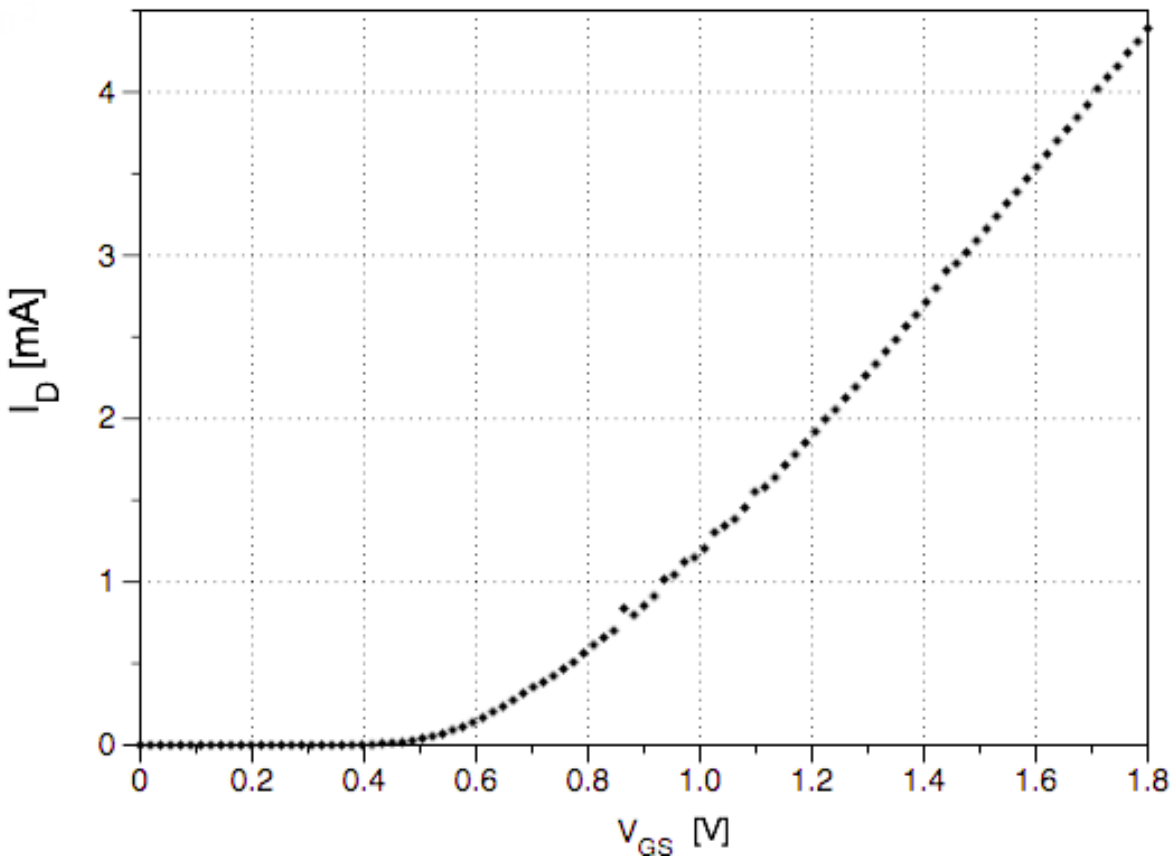

Figure 24: I_D vs. V_{GS} graph for an on-pixel transistor in the CMOS PPS array, with V_D=1.8 V

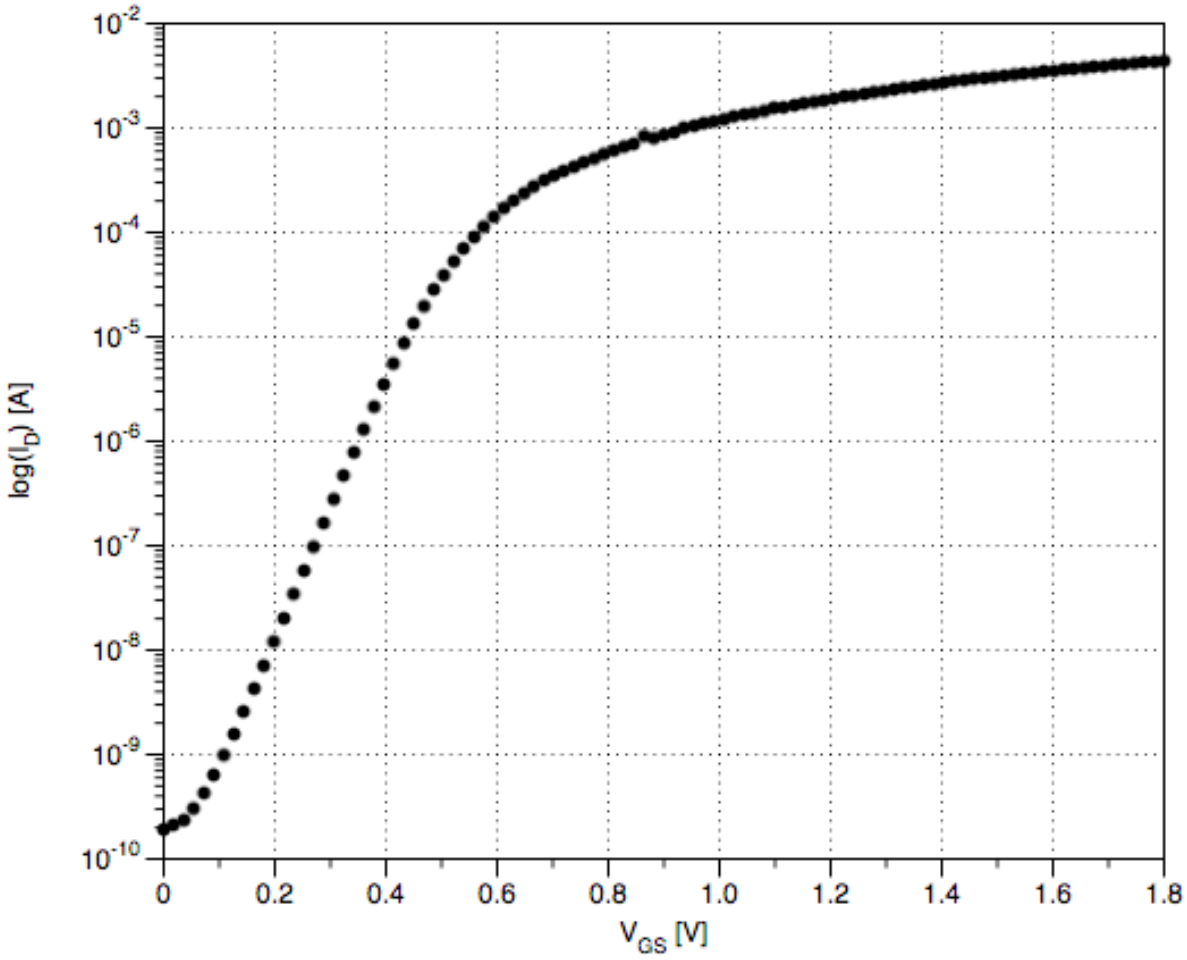

Figure 25: I_D vs V_{GS} curve from Figure 25 with I_D plotted logarithmically to show sub-threshold leakage in the NMOS transistor

Figure 26 shows the I_D-V_{DS} curves obtained from the sample at different V_{GS} values. These graphs correspond to the proper operation of an NMOS transistor in 0.18 µm CMOS technology with a V_t of about 0.5 V.

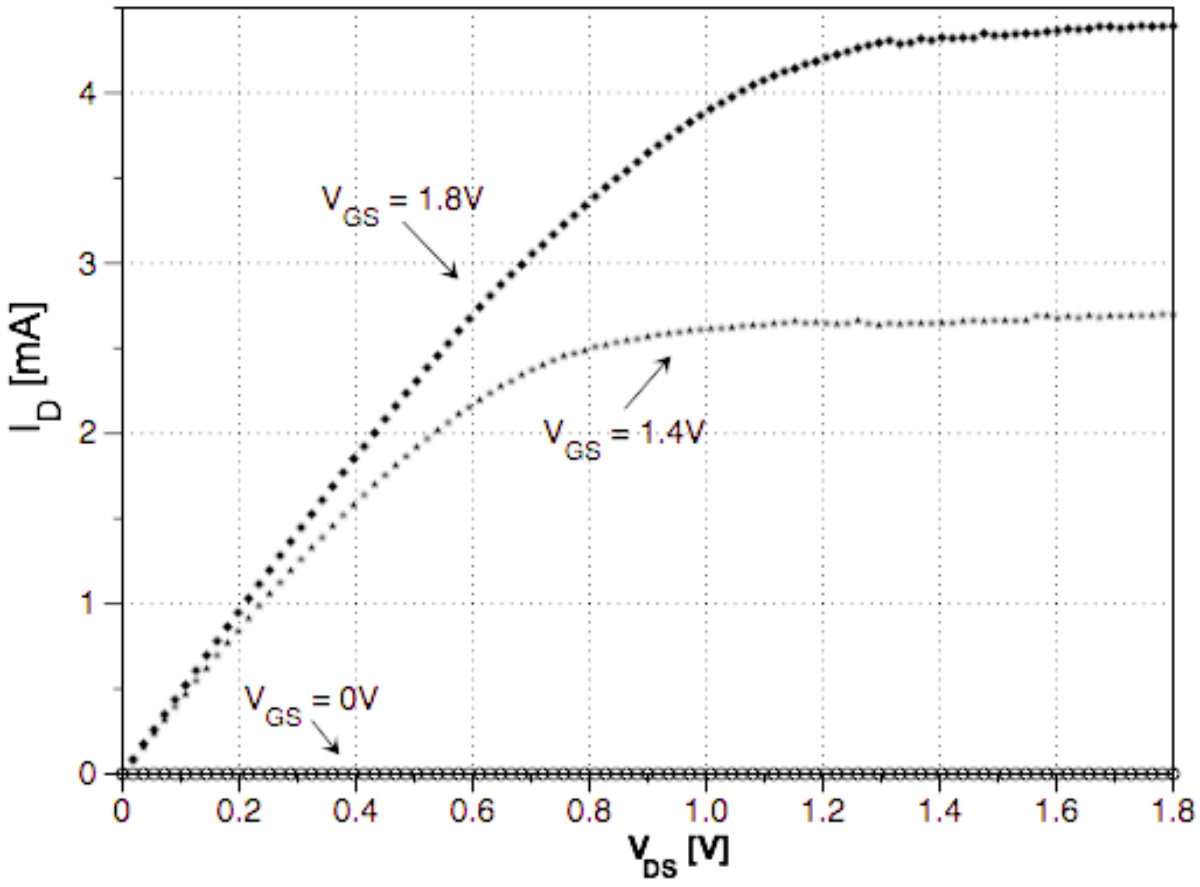

Figure 26: I_D vs V_{DS} graph for an on-pixel transistor in the CMOS PPS array, with varying V_{GS} values

4.2 Testing of Integrated Selenium-CMOS PPS Array

This section describes the results of the tests undertaken with the prepared CMOS PPS array with the a-Se detector wirebonded to a daughterboard as outlined in Section 2.2.3.1. All of these tests were conducted using the same Agilent test setup described in Section 4.1, but with the addition of a Canberra High Voltage Power Supply Model 31060 for tests conducted with a-Se bias voltages of above 100 V (the output voltage limit of the SPA). Figure 27 shows the setup of the test equipment in a rack. For the X-ray tests described in a later

section, the same test fixture was placed inside the X-ray machine with the cables from the SPA routed inside it to be connected.

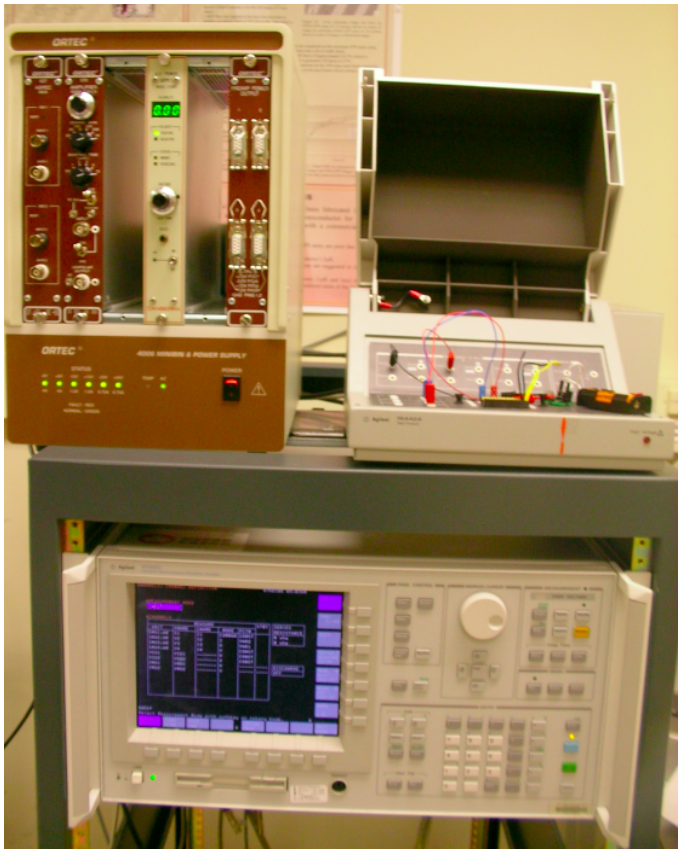

Figure 27: Test equipment setup, with the high-voltage source (top left), test fixture (top right), and Semiconductor Parameter Analyzer (bottom). A PC (out of frame) controls the SPA, which is connected to the test fixture holding the sample.

The prepared sample had all of its gates shorted to each other via jumper connections such that the gate line could be driven via one connection. This was because the tests being conducted in this section would be transient tests measuring current, and as such the gates of the PPS transistors needed to be held high to ensure the transistors were on and that charge buildup did not break down their channels while they were off. This was done using an AA

battery providing 1.3 V. Additionally, the source terminals were all connected to each other such that the current being measured was that of the entire array (i.e., all 64 transistors conducting in parallel the current generated as a result of photogeneration in the detector).

4.2.1 Electric Field Bias

As the voltage put on the top electrode of the a-Se detector (V_{BIAS}) is increased, the electric field across it is increased proportionally, since electric field is directly proportional to voltage. An increased electric field means that charge carriers in the detector are swept more efficiently increasing the charge collection efficiency of the detector when EHPs are generated. However, higher electric fields also result in more leakage current through the detector, not to mention there is a certain threshold above which the detector breaks down.

To illustrate the effect of electric field bias versus charge collection, the detector was relaxed at a zero electric field in a dark environment, followed by a test sequence run by the SPA which measured the current through the detector at three different electric field biases, each being separated by a relaxation period, with the current through the array being measured once a second for the non-relaxation tests.

Table 3 shows the sequence of the tests at different electric field biases and their description, while Figure 28 illustrates the setup of the test. It should be noted that the current being measured henceforth was read through the PPS transistors on the CMOS array, indicating proper integrated operation of the a-Se detector and the CMOS array at the selenium-silicon interface.

Table 3: Electric field bias test sequence

Sequence Number	Test Description	V_{BIAS}	Duration
1	0.27 V/µm Electric Field Bias	20 V	1 hour
2	Relaxation Period	0 V	1 hour
3	0.67 V/µm Electric Field Bias	50 V	1 hour
4	Relaxation Period	0 V	1 hour
5	1.33 V/µm Electric Field Bias	100 V	1 hour

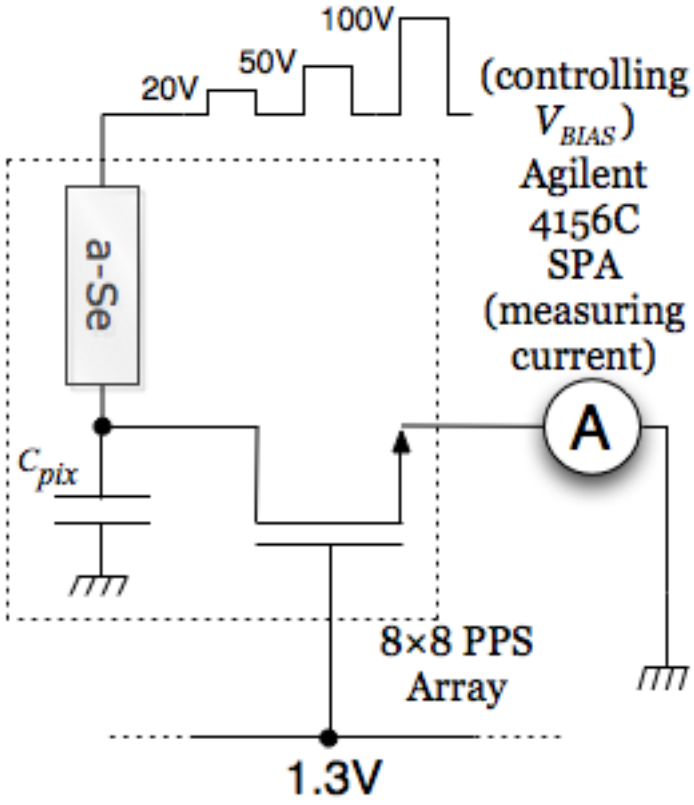

Figure 28: Measurement setup for electric field bias dark current test

The results of the test are shown in Figure 29, with current versus time plotted on a log-log scale. It can be seen that as the electric field bias increases, the dark current through the detector increases such that the settled dark current is about 2 nA, 500 pA, and 200 pA for 1.33 V/µm, 0.67 V/µm, and 0.27 V/µm respectively. The transient behaviour of the a-Se

detector is also apparent, as the current is still on a downward trend at the end of the hour-long measurements.

The established norm for doing tests on a-Se detectors is to allow it to relax for upwards of 14 hours to fully allow the dark current to settle to its true relaxed value. This convention would be followed for the subsequent tests in this section; however, for the purpose of showing a-Se's behaviour at different electric field biases, a shorter relaxation time was sufficient. The shorter relaxation time here also allowed for the tests to be automated by the SPA, as tests 1 through 5 were run automatically after it was programmed via the ICS software.

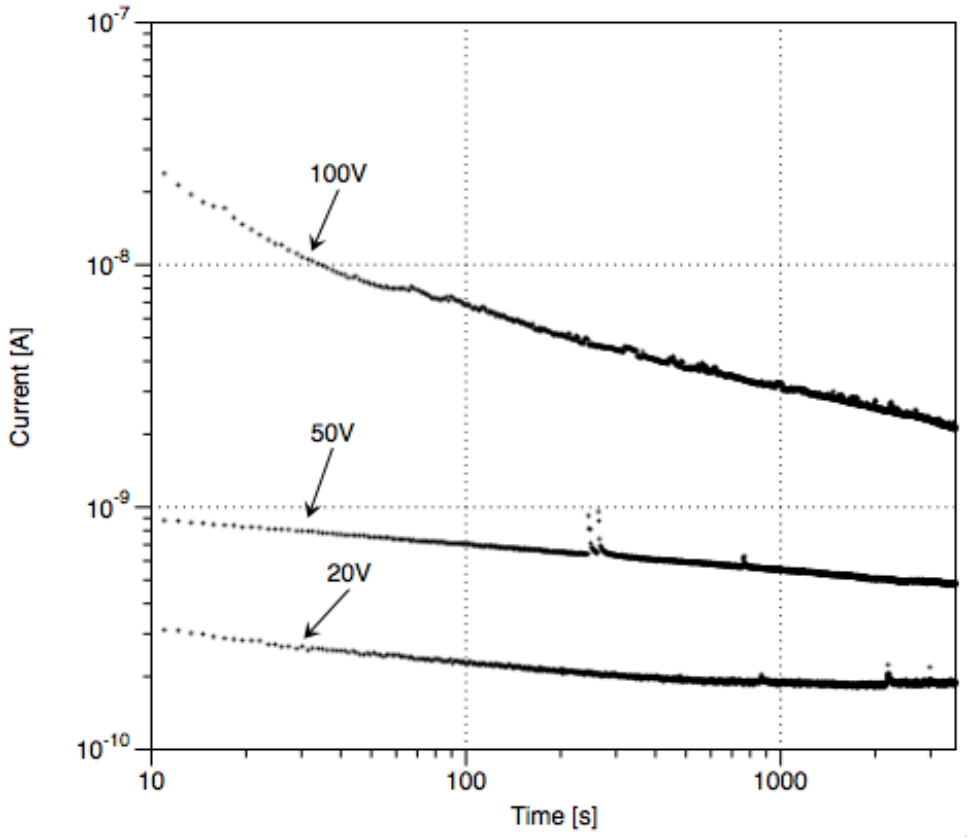

Figure 29: Dark current through Selenium-CMOS array at varying electric field biases

4.2.2 Optical Light

In addition to having photogeneration properties to X-ray photons, selenium's photoresponsivity extends to the optical wavelengths, gradually decreasing as the wavelength approaches red light and beyond. As such, tests were conducted to show the selenium-CMOS PPS array's responsivity to different wavelengths of optical light, using 1 W LEDs. The blue LED made by Lite-On emitted a wavelength of 465 nm, the green LED made by Cree emitted a wavelength of 530 nm, and the red LED made by Lumex emitted a wavelength of 636 nm. In each case, the LED was set up inside the test fixture and positioned directly above (1.5 cm to 2 cm) the sample to ensure good flux – a high number of photons striking the detector. The LED was connected to an external power supply through the test fixture. The sample was allowed to relax for upwards of 16 hours between tests and the electric field bias was set to 3.33 V/um (250 V) using the Canberra high-voltage power supply. Figure 30 shows the setup of the sample and the LED inside the test fixture.

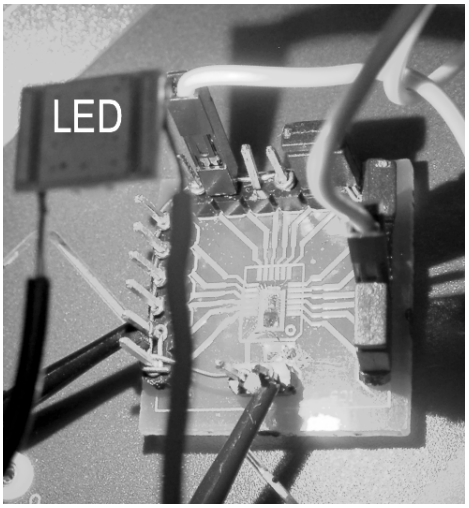

Figure 30: The PPS array was tested inside a test fixture with LEDs positioned above it to test its photoconductivity.

The tests were run as transient current measurements just like the previous section; however, to illustrate the photoresponsivity of the detector, the LED power supply was turned on and off periodically throughout the test to highlight the difference in current in the detector in dark versus light conditions. The on/off timing was two minutes initially and increased to five, ten, and fifteen minutes as time went on in the test in order to show up nicely on the logarithmically displayed transient graph. Figure 31 shows the setup of the test.

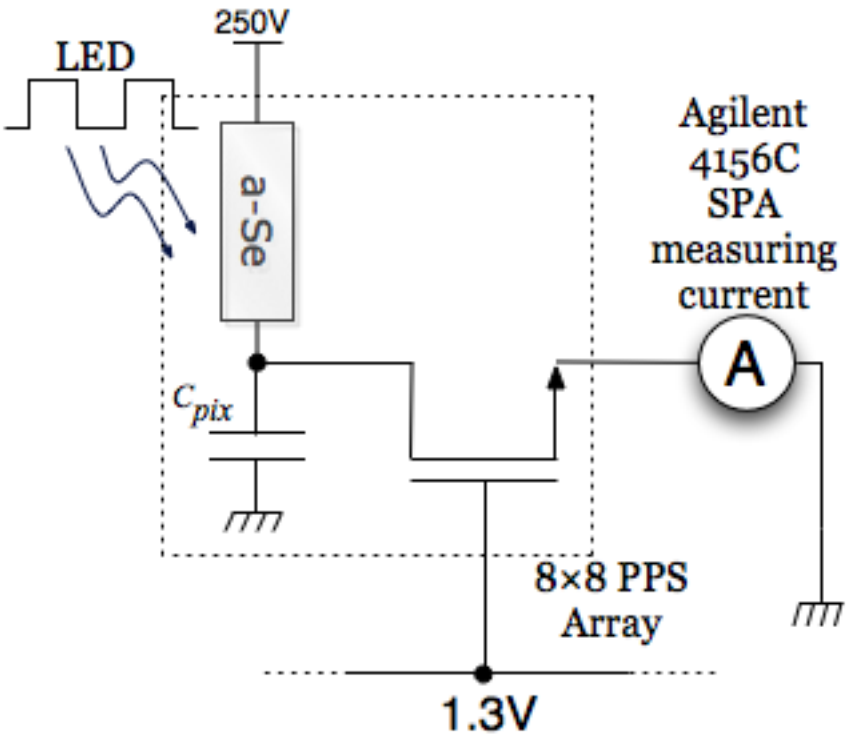

Figure 31: Pulsed optical photocurrent test setup

Figures 32, 33, and 34 show the sample's response to LEDs emitting blue, green, and red light respectively, plotted on a log-log scale of current versus time.

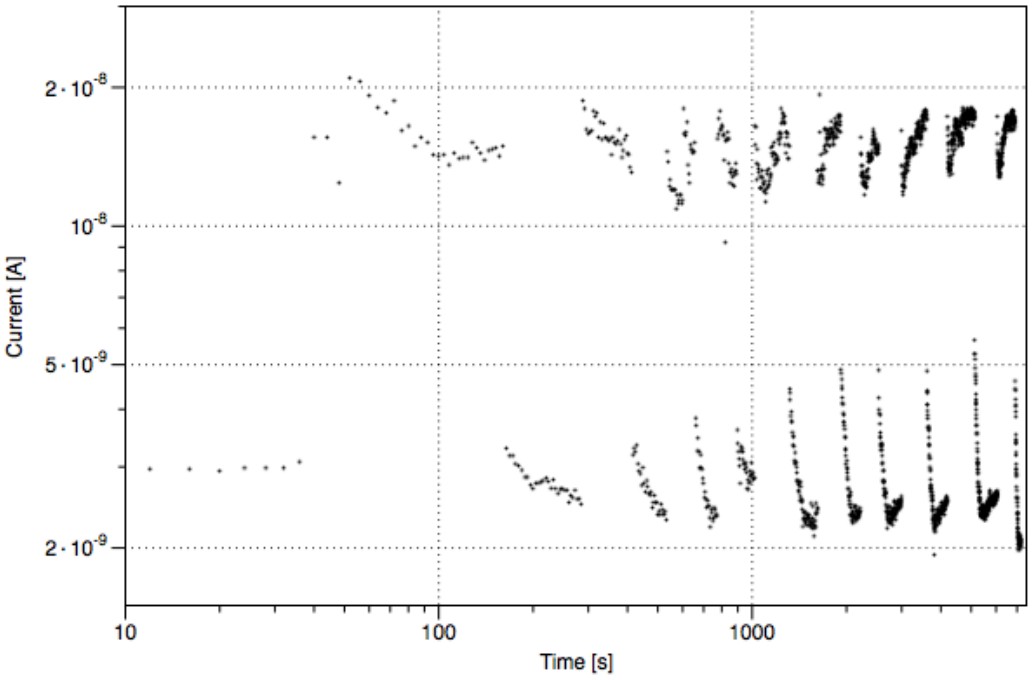

Figure 32: Pulsed photocurrent through PPS array under blue light at 3.33 V/µm

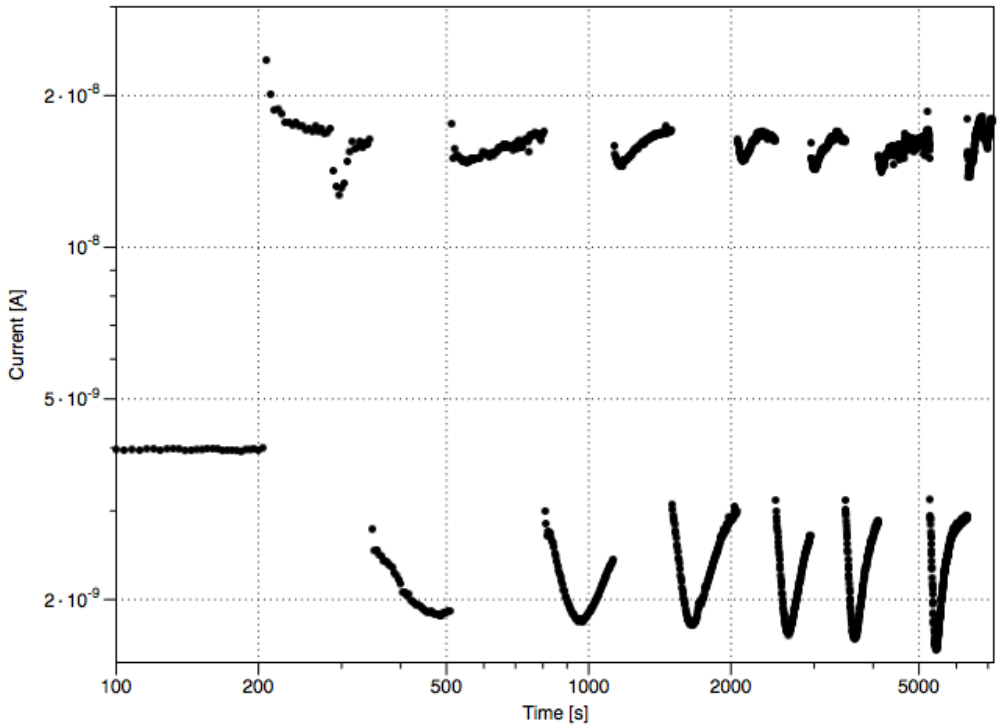

Figure 33: Pulsed photocurrent through PPS array under green light at 3.33 V/µm

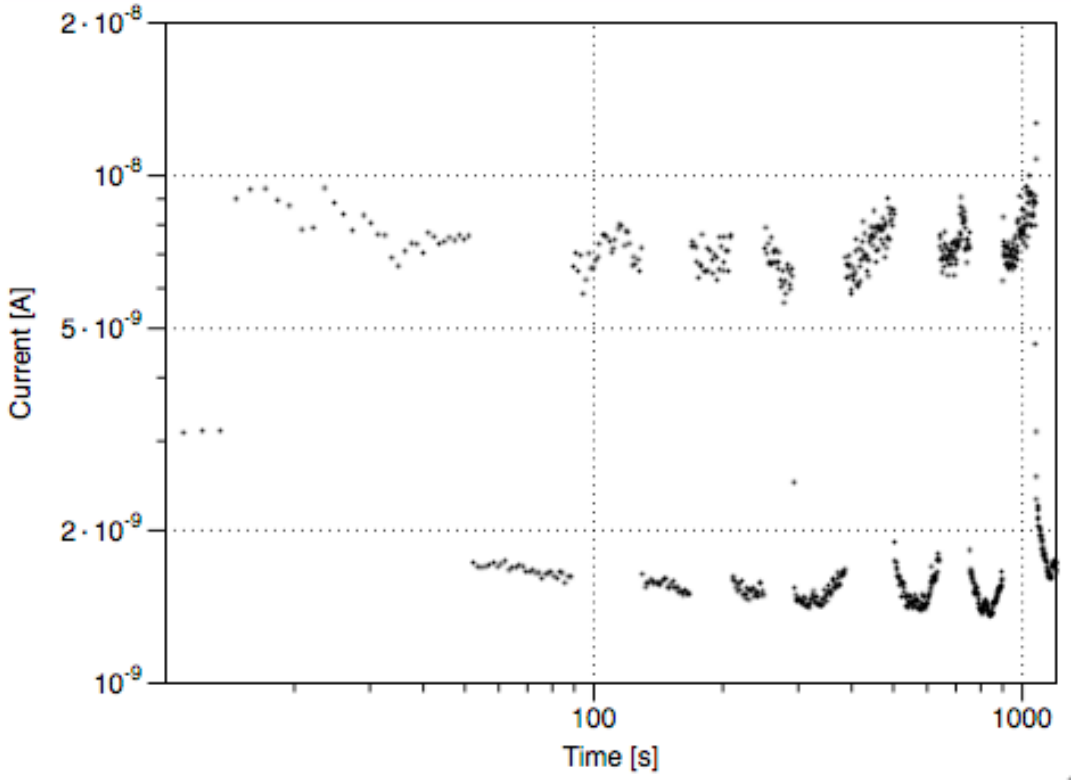

Figure 34: Pulsed photocurrent through PPS array under red light at 3.33 V/µm

From these results, it is immediately apparent that the responsivity of selenium is better to blue and green light than red light. The on-current level for the former two wavelengths is about 20 nA as opposed to the off-current level of about 2 nA, a one order of magnitude difference. With red light, the on level is about 8 nA. The responsivity of selenium has been shown to be poorer with increasing wavelengths in literature as early as 1960 [20], with a dropoff that begins around the 500 nm green wavelength.

The shape of the preceding three graphs raises the question of why there is a fluctuation in current immediately after the "on" and "off" periods (a so-called tailing effect). This can be addressed by noting that the tests were not conducted using a shutter, where hitting the "on" or "off" switch would immediately immerse the array in darkness or light

instantaneously. Instead, the actual LED power supply was turned off, which causes the LED to gradually dim until no current passes through it in the former case and gradually brighten as the power supply starts feeding it current to its current limit in the latter case. The gradual brightening and dimming of the LED can result in charge generation in the detector which causes the transient effect for a time after a steady state of light intensity has been reached.

4.2.2.1 Linearity

With the dark versus light levels established for optical light, the linearity of the detector was also of interest, especially since the pulsing of the LEDs showed drifting of the signal level during the on and off periods. To test for linearity, the sample was allowed to relax and then tested under each of the LEDs turned on for a longer period of time. Figure 35 illustrates the test setup.

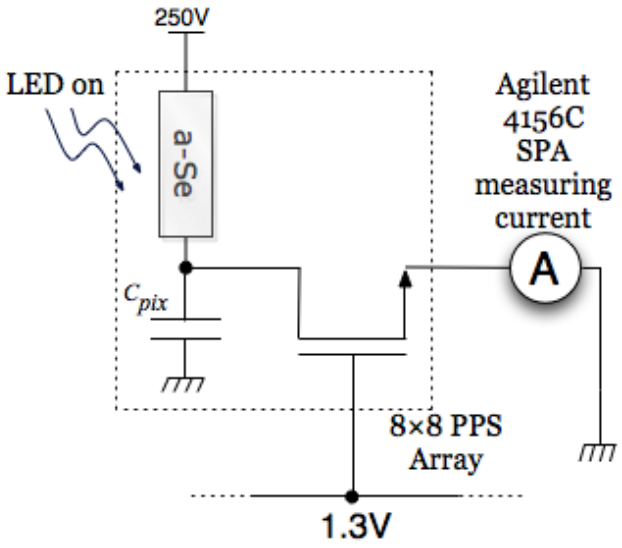

Figure 35: Photoconductance linearity test setup

Figures 36, 37, and 38 show the results of the detector's output, represented as voltage accumulated on a 1 μF capacitor, for the three different wavelengths of light respectively.

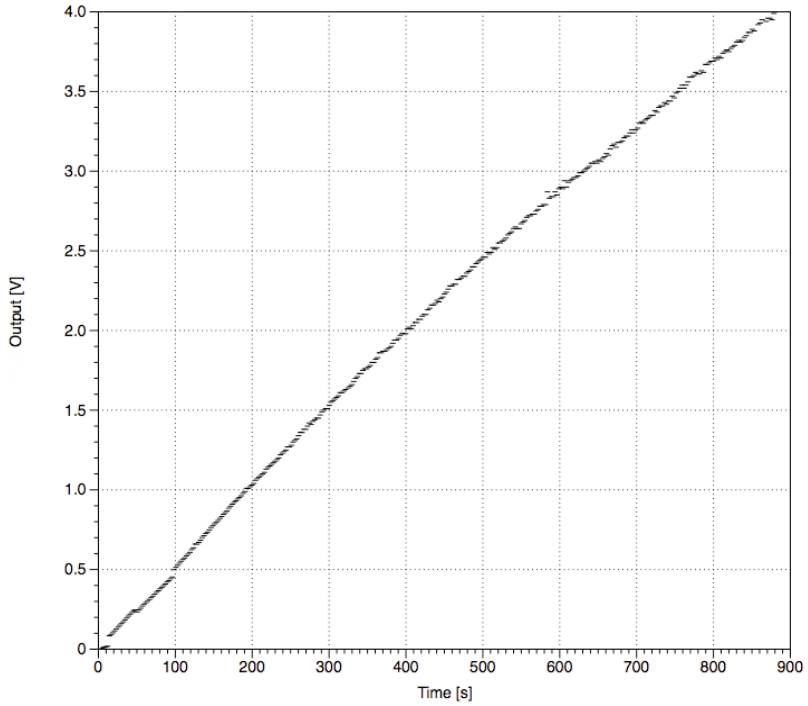

Figure 36: Selenium-CMOS detector linearity under blue light

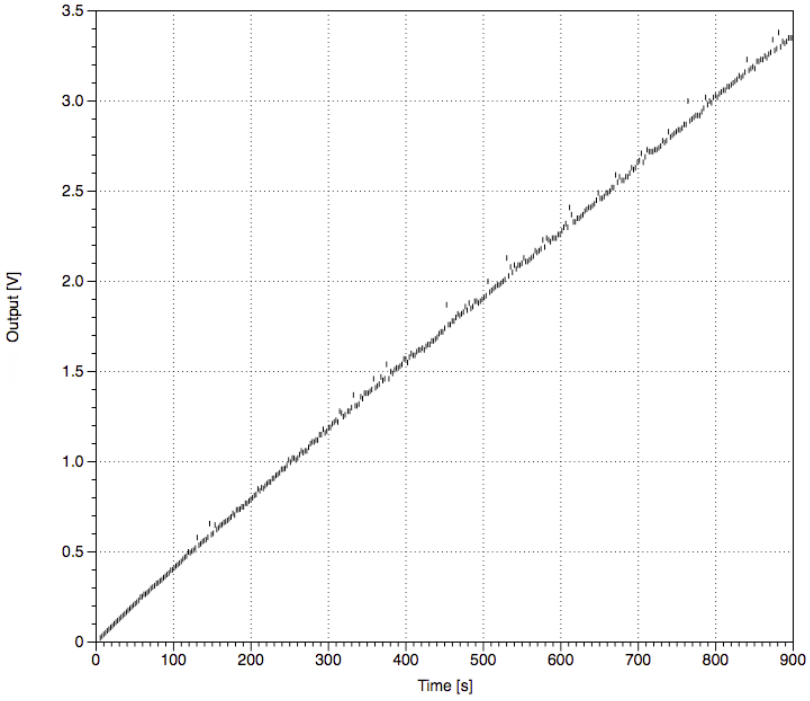

Figure 37: Selenium-CMOS detector linearity under green light

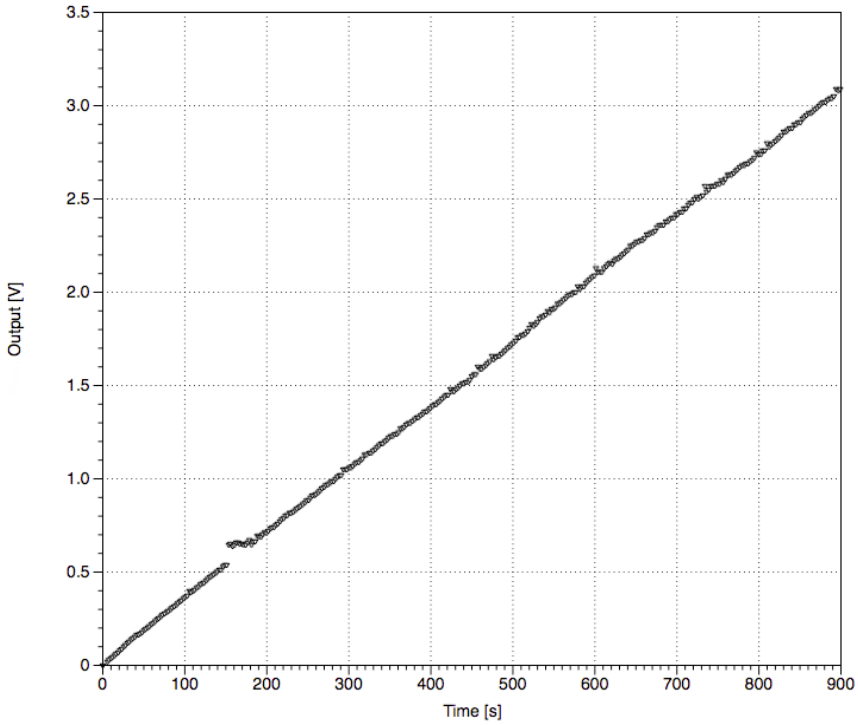

Figure 38: Selenium-CMOS detector linearity under red light

Figure 39 shows the three sets of results from the linearity tests all on one graph, with each set of data points also having a line of best fit. This graph also reiterates the detector's responsivity to the three wavelengths manifested in the slopes of the lines, with the best charge conversion coming with blue light. It should be noted that the detector's response to green light for this test was somewhat diminished, being closer to the response for red than that of blue light, because the green LED had started to dim and after the linearity test it was no longer functional.

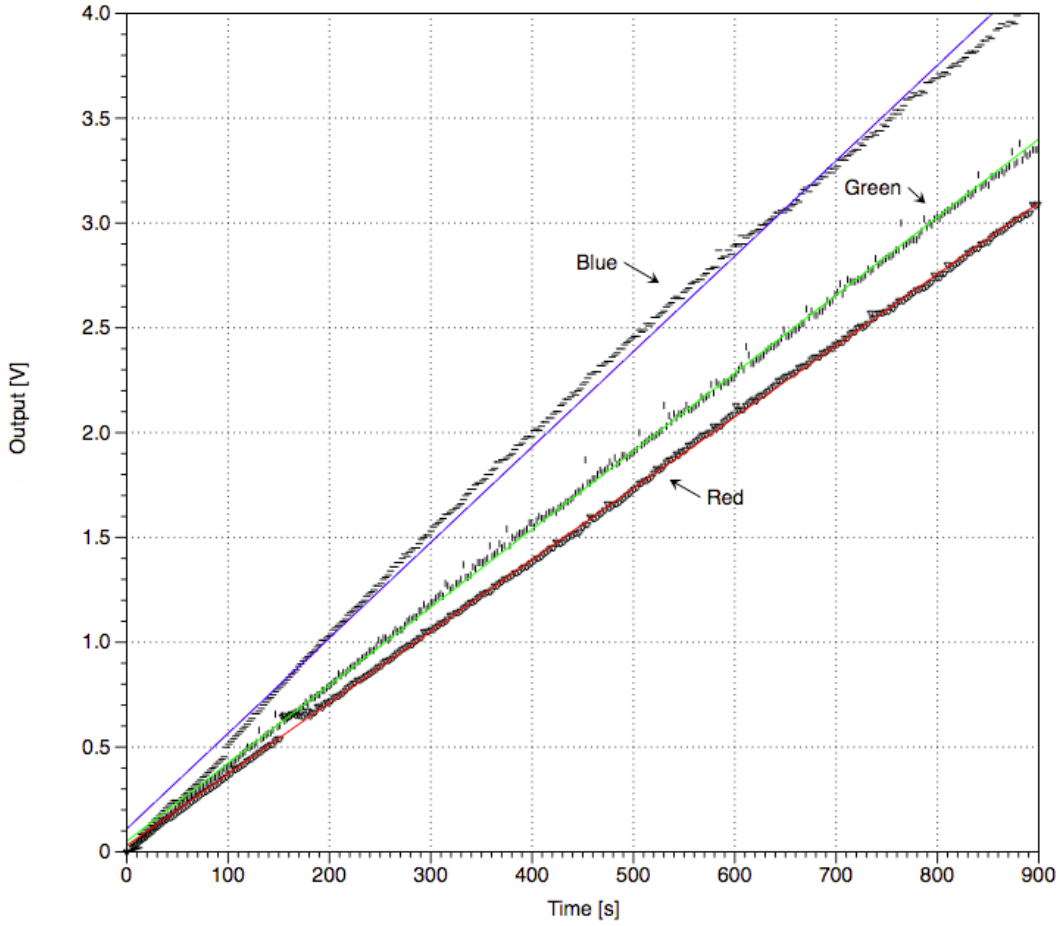

Figure 39: Selenium-CMOS PPS array output linearity under optical light wavelengths

4.2.3 Protective Epoxy Leakage Test

To confirm that the transparent epoxy used to encapsulate the detector, top contact, and wirebonds was not contributing significant leakage current to the system, a test was conducted where a bare daughterboard had the epoxy placed over top of two pads and the transient currents through both pairs of nodes were measured with a voltage of 100 V between the two pads. This was done in conjunction with another two pads which were not connected to each other (i.e., the PCB substrate itself was the only physical connection

between the pads, aside from air). Figure 40 shows the daughterboard PCB, with the connections on the right side having the transparent epoxy over top of them.

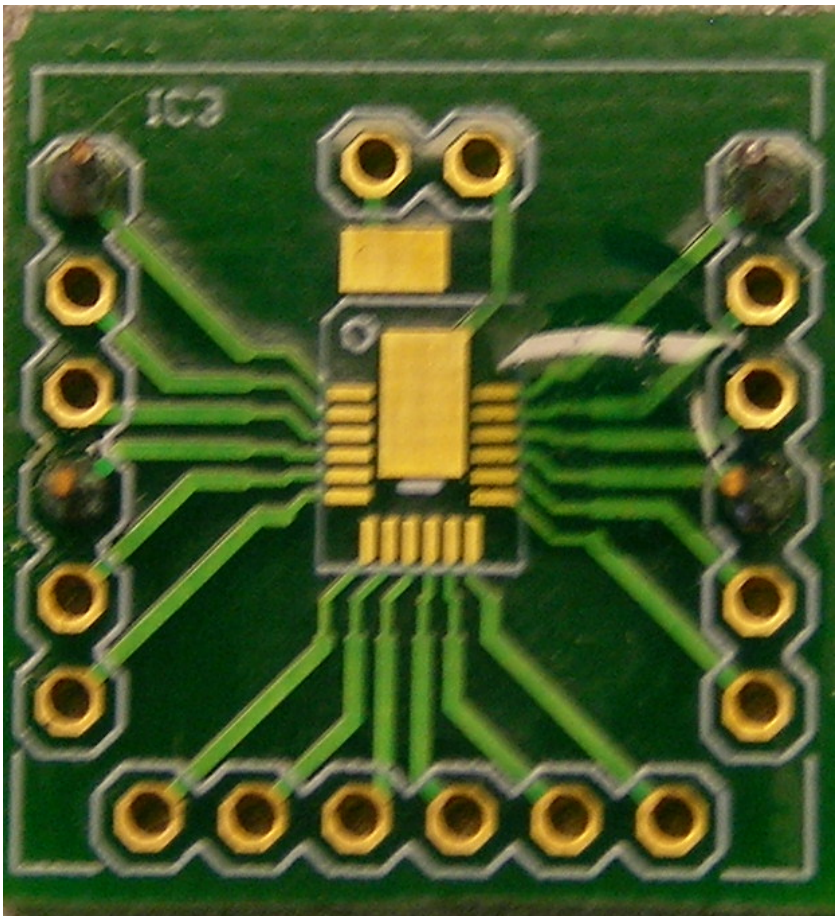

Figure 40: Daughterboard used to measure leakage through PCB and transparent encapsulating epoxy

The transient test was conducted for 60 seconds, with 100 V being applied to the two pairs of nodes on each side and the current being measured via the SPA. The average current level for the left side, leakage through the PCB, was 46.5 fA, while the average current through the right side, with the epoxy, was essentially the same at 45.8 fA, both figures being

near the noise floor of the SPA. This test verified that the encapsulating transparent protective epoxy did not contribute significant leakage in the system and that the leakage levels through both the PCB and the epoxy were orders of magnitude below the signal currents being measured.

4.3 Testing of PPS Readout Board and Array

In order to run the tests on the PPS array using the readout board, the system itself first had to be characterized by focusing on the signal amplification stages. This could be done using the test cap input circuitry described in Chapter 3, but instead of using an external function generator, a program was written so that the MCU could output the signals. Two signals would be required – a pulse at the shared input of the eight test caps going into the charge amplifiers, and an active low reset signal to close the switch across the feedback path of the charge amplifiers.

Assembly code was written to generate a 1 kHz signal using one of the MCU's timer channels and its corresponding counter, so that it had a 75% duty cycle, being low for 250 ns and high for 750 ns. This signal served as the reset signal, so the 750 ns during which it is deasserted each period was when the test cap input pulse was programmed to go high. This would also be a 1 kHz signal, and it was generated by the same timer subroutine by using a counter-decrementing branch structure to make the MCU wait a certain number of cycles after the rising edge of the reset signal before the counter reached zero and it could proceed to the next instruction, which would assert the input pulse signal high. The input pulse was

deasserted by a separate timer counter threshold to allow for easy manipulation of the pulse width. Figure 41 shows the structure of the test characterization timing signals.

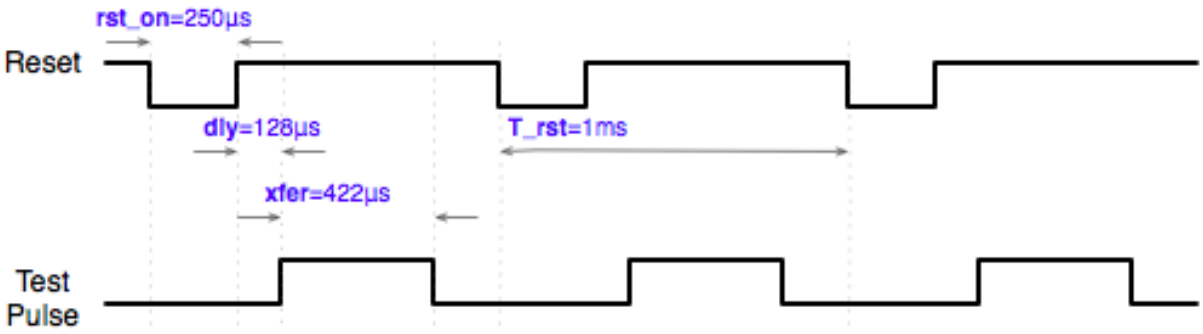

Figure 41: Timing diagram for driving reset signal and test input to charge amplifiers

This program was run and the output of each charge amplifier channel was probed, though the screenshots shown from here on will focus on one channel. Figure 42 shows an oscilloscope screen capture of the reset (Ch1) and input pulse (Ch3) as well as the output of the channel 0 charge amplifier (Ch2).

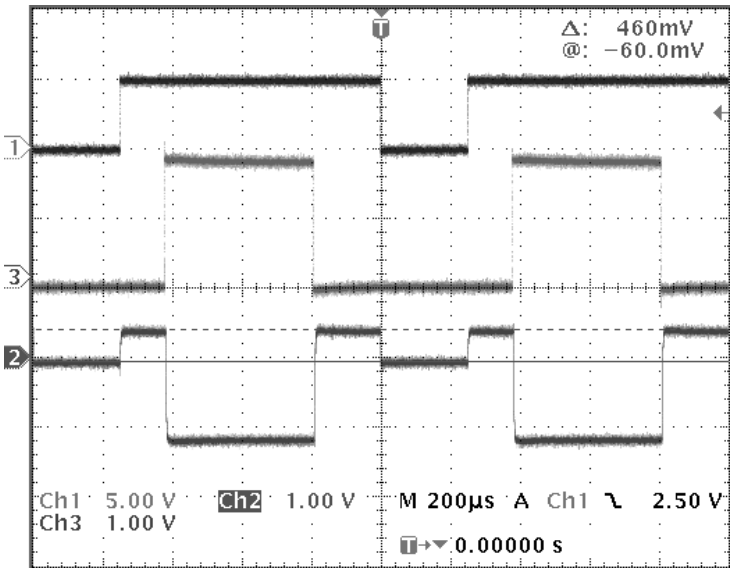

Figure 42: Charge amplifier output being driven by a test pulse from the MCU

The charge amplifier output is reset to 0 V when the reset signal is low (active), since the switch across the feedback path is closed. When the reset signal goes high, charge injection causes the output voltage of the charge amp to rise to 460 mV as shown by the cursor. Then, when the input pulse goes high, the charge amp output decreases by about the same amount (characterized further later) because the gain of the system is $-C_f/C_{test}$, which is approximately -1. Figure 43 is a close-up of the charge amp output at the outset of charge injection, more accurately measuring it to be 456 mV with a settling time of about 10 µs.

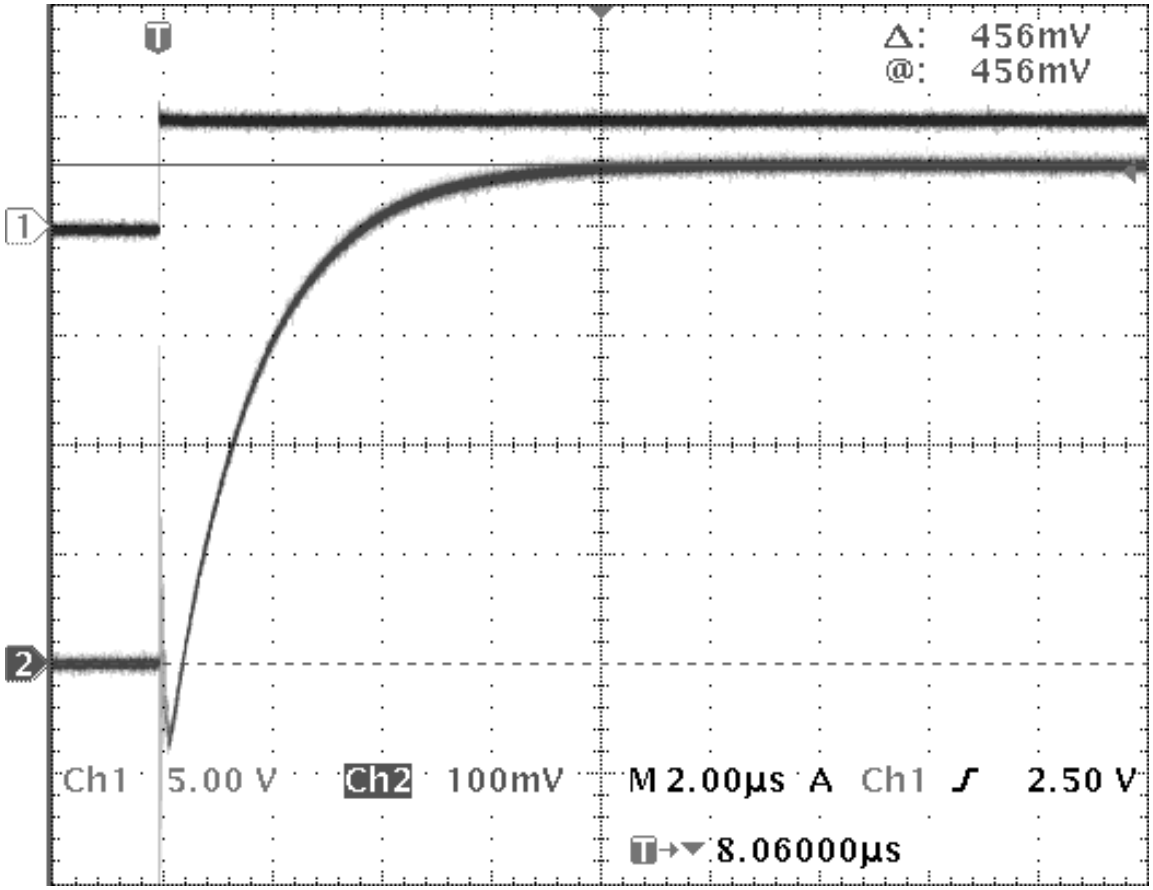

Figure 43: Charge injection due to reset switch toggling at the channel 0 charge amplifier output

The charge gain of the system is characterized in Figure 44. For a 1.8 V input pulse, the charge amplifier output decreases by 1.52 V, giving a charge gain of -0.844. This is slightly below the ideal value of -1 (since $C_f = C_{test} = 1$ pF), as parasitic capacitances in parallel with the test cap cause the charge gain to be lowered.

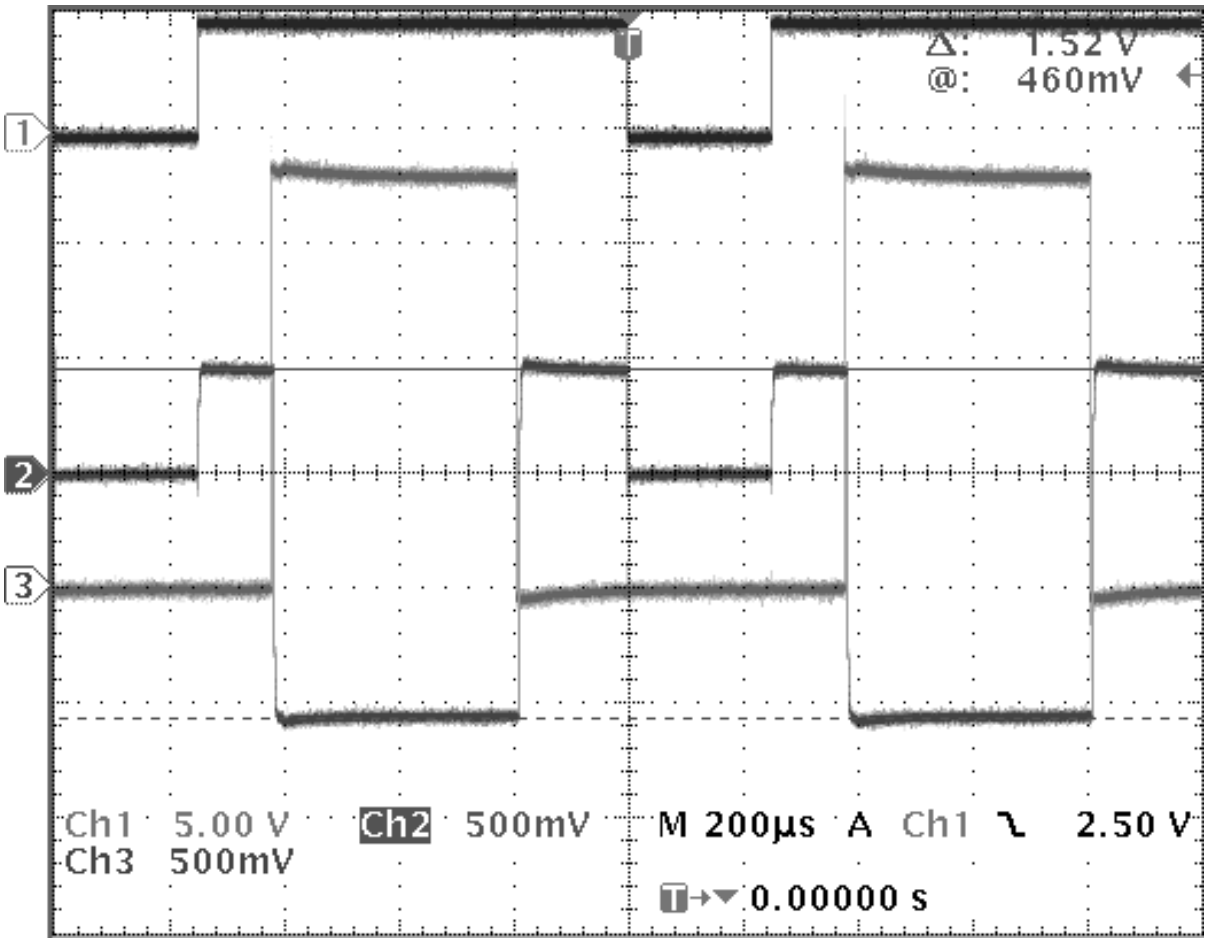

Figure 44: Charge gain of the channel 0 charge amplifier output

A slight "droop" in the charge amp output was apparent from the waveforms, after the test cap input signal was reset to 0 (the charge amp output should have reset to its base level of 456 mV but was going higher and then decaying). Figure 45 is a closer view of the

waveforms that clearly shows that the test cap input signal (Ch3) has an undershoot of about 44 mV when dropping from 1.8 V to 0 V that causes the charge amplifier output level to initially be higher than the eventual settled value by 22 mV.

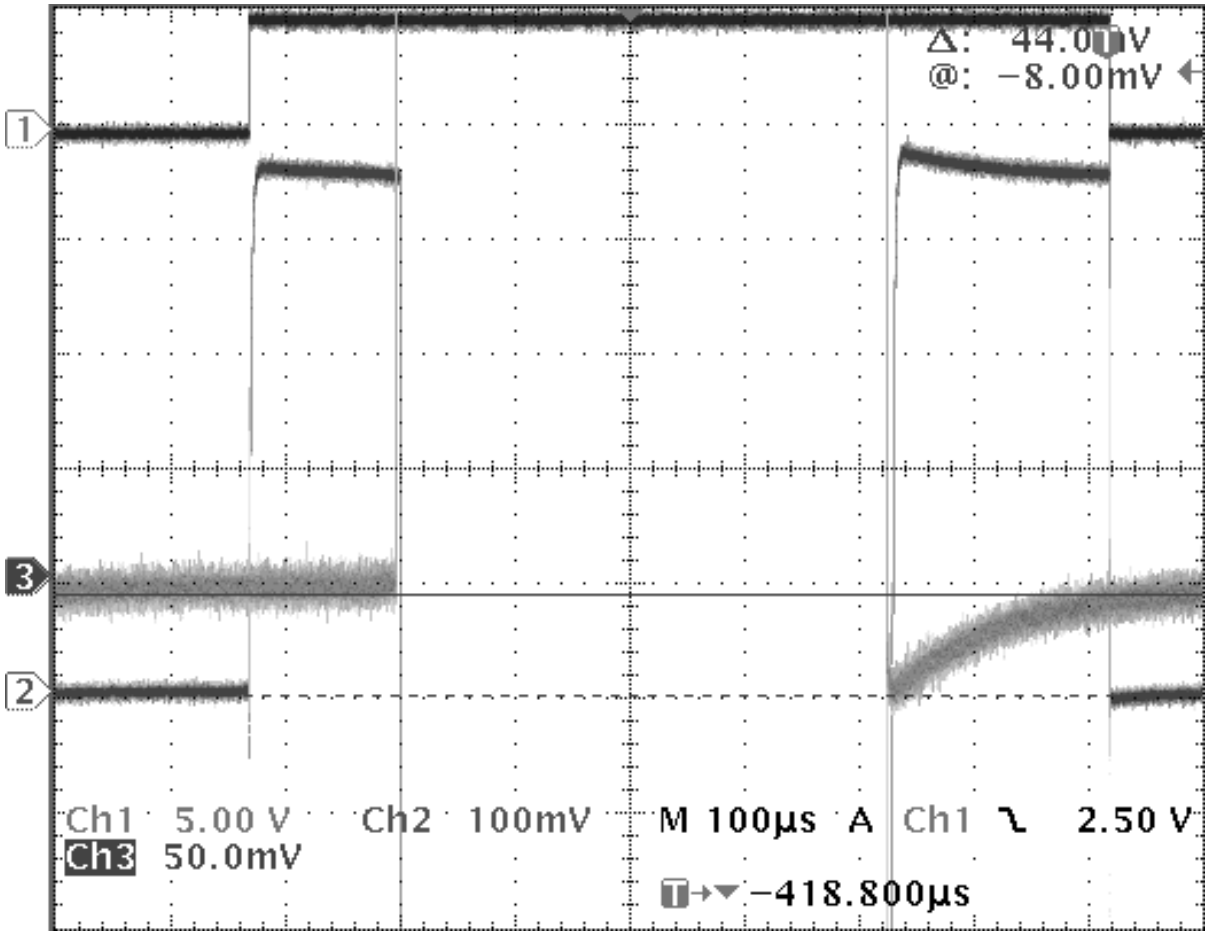

Figure 45: A closer look shows that the charge amplifier output was not decaying due to loss of charge, but because the input signal had an undershoot.

The purpose of measuring the charge injection level for each channel was to use the instrumentation amplifier in the next stage to cancel out this deterministic noise. After measuring the charge injection levels the DAC for each channel was programmed to the

corresponding value (aside from the DAC for channel 3, which, even after extensive debugging, part replacement, and signal probing, would not output a proper voltage level). By probing the output of the channel 0 instrumentation amplifier shown in Figure 46, the effect of eliminating the charge injection can be seen.

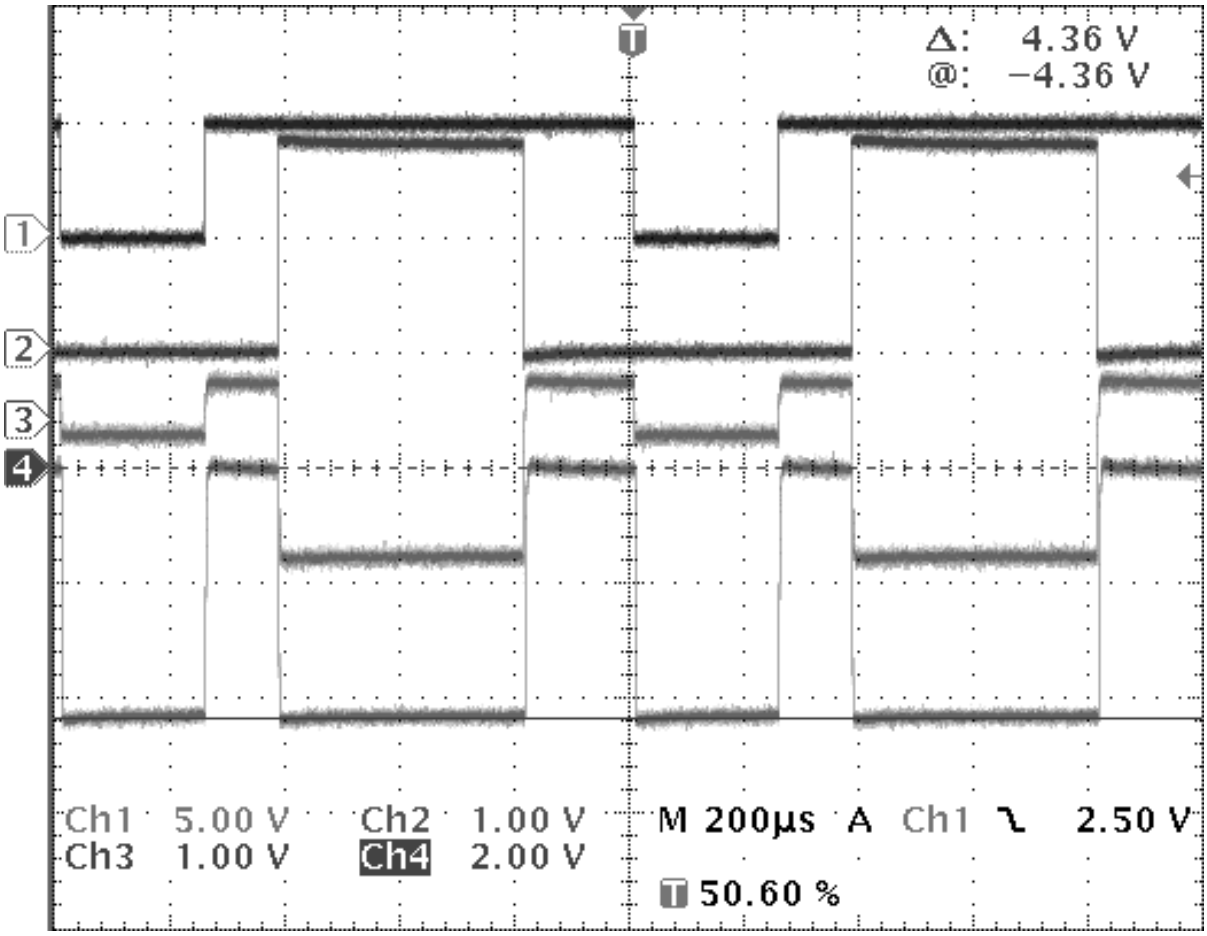

Figure 46: The instrumentation amplifier eliminates the charge injection seen in the charge amplifier output.

Here, Ch1 is reset, Ch2 is the test input pulse, Ch3 is the charge amp output, and Ch4 is the instrumentation amp output, which is at 0 V when the charge amp output is at its charge

injected level of 450 mV, just after reset goes high. When the test cap input rises and the charge amp output decreases, the instrumentation amp output goes down to -4.36 V. Note also that when reset is low (asserted), because the charge amp output goes to 0 V, the instrumentation amplifier output will once again go to its negative saturation level of -4.36 V (since the negative input of the instrumentation amplifier is the DAC output, kept constant at 456 mV). Figure 47 shows the same four signals but focuses in on the instrumentation amp output on Ch4 by adjusting its scale to 50 mV/div.

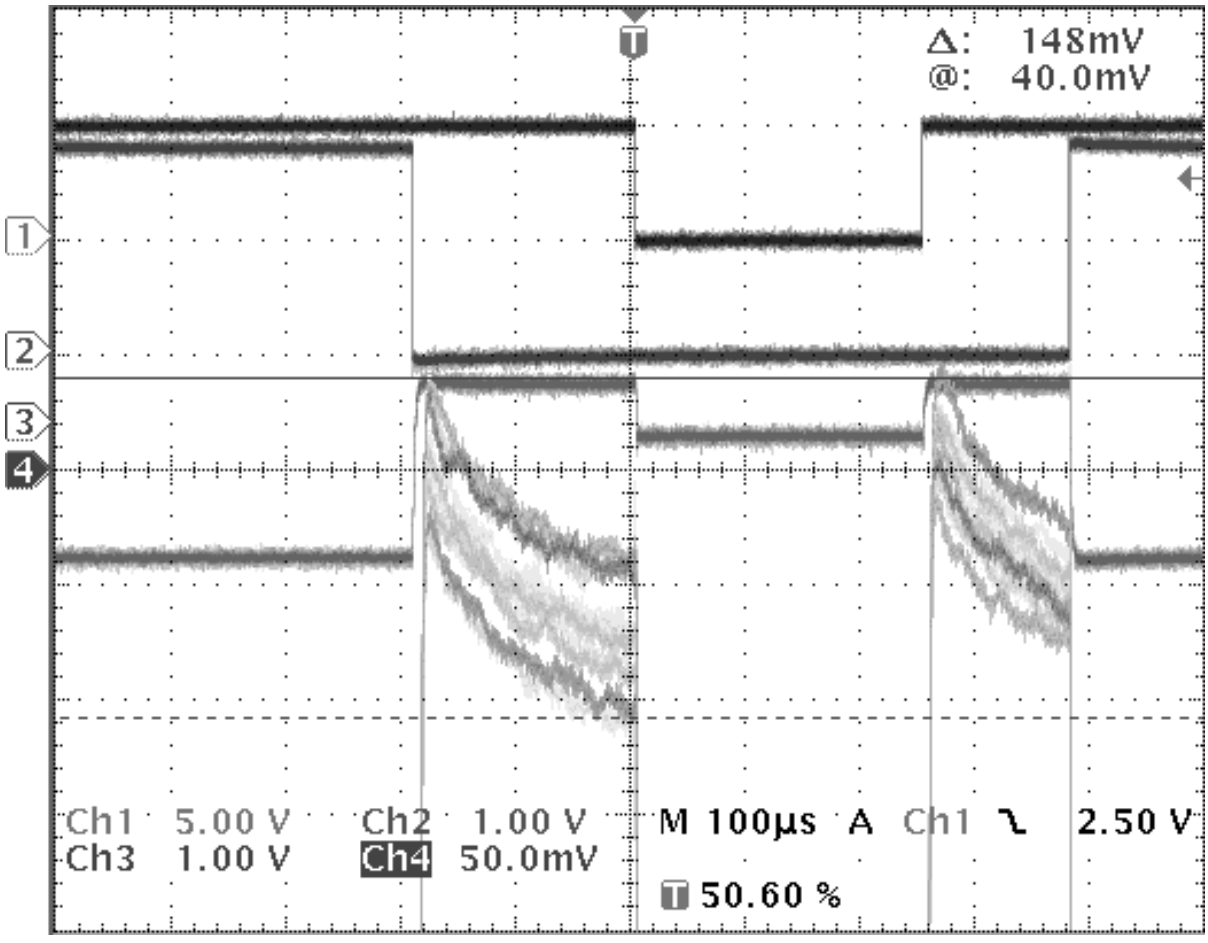

Figure 47: The instrumentation amplifier's 0 V level fluctuates because it tracks the charge amplifier's output.

It is clear that the value is not actually constant at 0 V, but noisy and fluctuating from just above 0 V to just below it. This is due to the droop effect seen in the charge amp output. The instrumentation amplifier is simply behaving as a differential amplifier and tracking the charge amp output, since the instrumentation amplifier's output is its gain (10) multiplied by the difference between the charge amp output and the constant DAC reference. This was verified by adjusting the instrumentation amplifier's gain to 100 by shorting its gain selecting jumper – doing this caused the 0 V level to fluctuate by a much greater degree around 0 V. One last screenshot dealing with this issue is shown in Figure 48, which now just focuses in on the charge amplifier output as well, to show how the instrumentation amplifier tracks the charge amplifier's output, which is fluctuating around 456 mV.

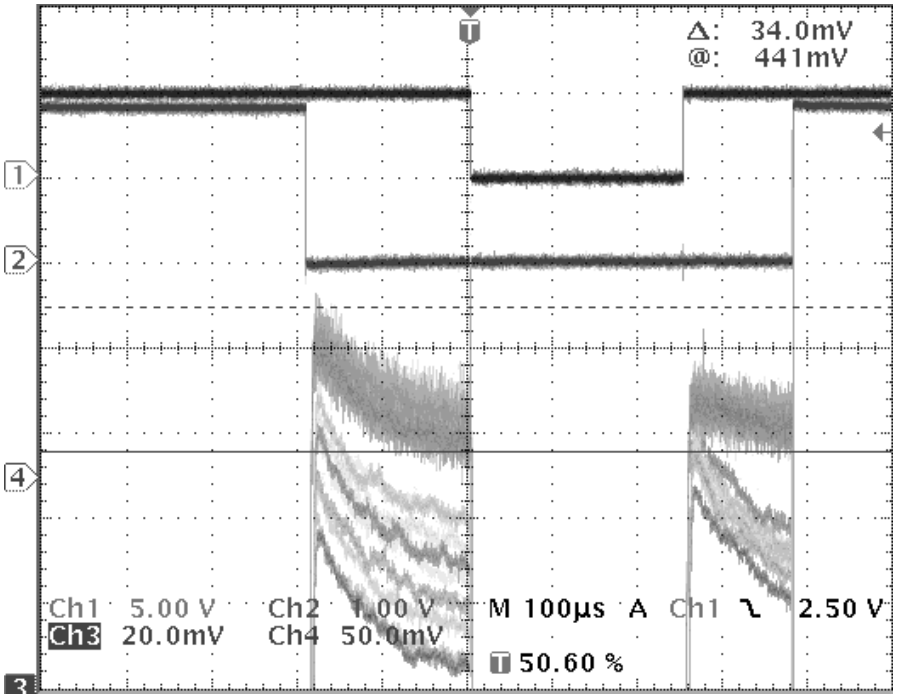

Figure 48: Instrumentation amplifier output shown in perspective with charge amplifier output

4.3.1 PPS Array Testing on Readout Board

To test the PPS array on the PCB, the MCU's program had to be altered. The information gathered in the previous section on the settling time of the charge injection would have to be used to make sure the delay after reset being deasserted before readout was long enough to allow for this settling; this delay was set to be 20 µs. Additionally, there were now eight signals plus reset to deal with – one for each row in the array, as all of the pixels in a row share the same read (gate) line. So each pixel would be integrating for slightly less than eight reset cycles. This was important in the calculation of the timing, as readout had to be done frequently enough that the voltage accumulated on the pixel capacitor during integration did not break down the transistors. From the tests earlier in this chapter, it was found that the array could sink up to 20 nA under photogeneration. Thus, assuming every pixel conducts an equal amount of the total current, the maximum current each pixel could see is the stated total array figure divided amongst the 64 pixels, or 0.3125 nA. Knowing that:

$$Q = CV = It, \tag{9}$$

it can be shown that if the voltage is needed not to exceed a certain breakdown value V_{max}, a restriction for the maximum integration time t_{int_max} can be set as follows:

$$t_{int\_max} = \frac{C_{pix} V_{max}}{I_{pix\_max}}. \tag{10}$$

Using the 0.3125 nA figure and 1 pF for the pixel capacitor C_{pix}, and setting V_{max} to 1.8 V (a conservative estimate, as 0.18 µm CMOS technology is built to withstand even higher voltages), the maximum integration time in this case is 5.76 ms. Figure 49 shows the timing diagram of the program to be implemented on the MCU, with G0 to G7 representing the read

lines for the eight rows in the array. During each cycle where the reset signal was deasserted, only one read line would be activated for readout, which would cause the eight pixels in that particular row to transfer their charge to the eight column charge amplifiers.

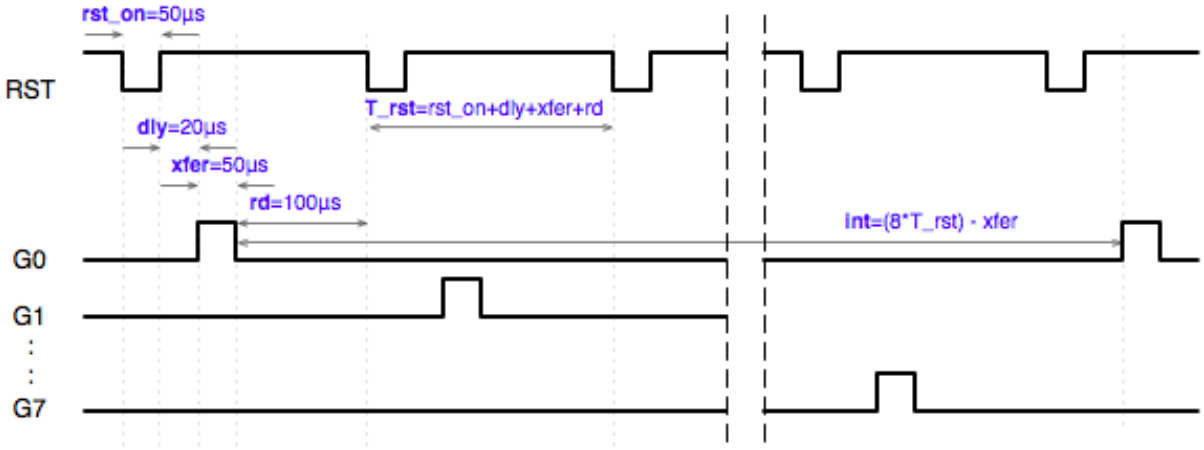

Figure 49: PPS array timing diagram

This timing scheme was set to give an integration time of 1.71 ms, far below the maximum allowable integration time. The algorithm for implementing this set of timing signals was similar to the one used for the previous program. There was still a main reset signal, and after each rising edge, a read signal would rise after a set delay. However, this was not the same signal each cycle. To simplify the problem, the eight read lines were handled as an 8-bit bus. A flag would be used to keep track of which cycle the program was at, and after each cycle, the value of the temporary placeholder storing the value of the 8-bit bus would be shifted left, padded with a zero (allowing the "one-hot" signal to propagate). If the flag showed that it was at the eighth cycle, the value of the placeholder would be reset to 1. Thus, the value of the placeholder could be written to the 8-bit bus after each reset rising edge following the 20 µs charge injection allowance delay. Figure 50 shows an oscilloscope

screenshot of the program running, with Ch1 being reset, Ch2 being G0, Ch3 being G6, and Ch4 being G3.

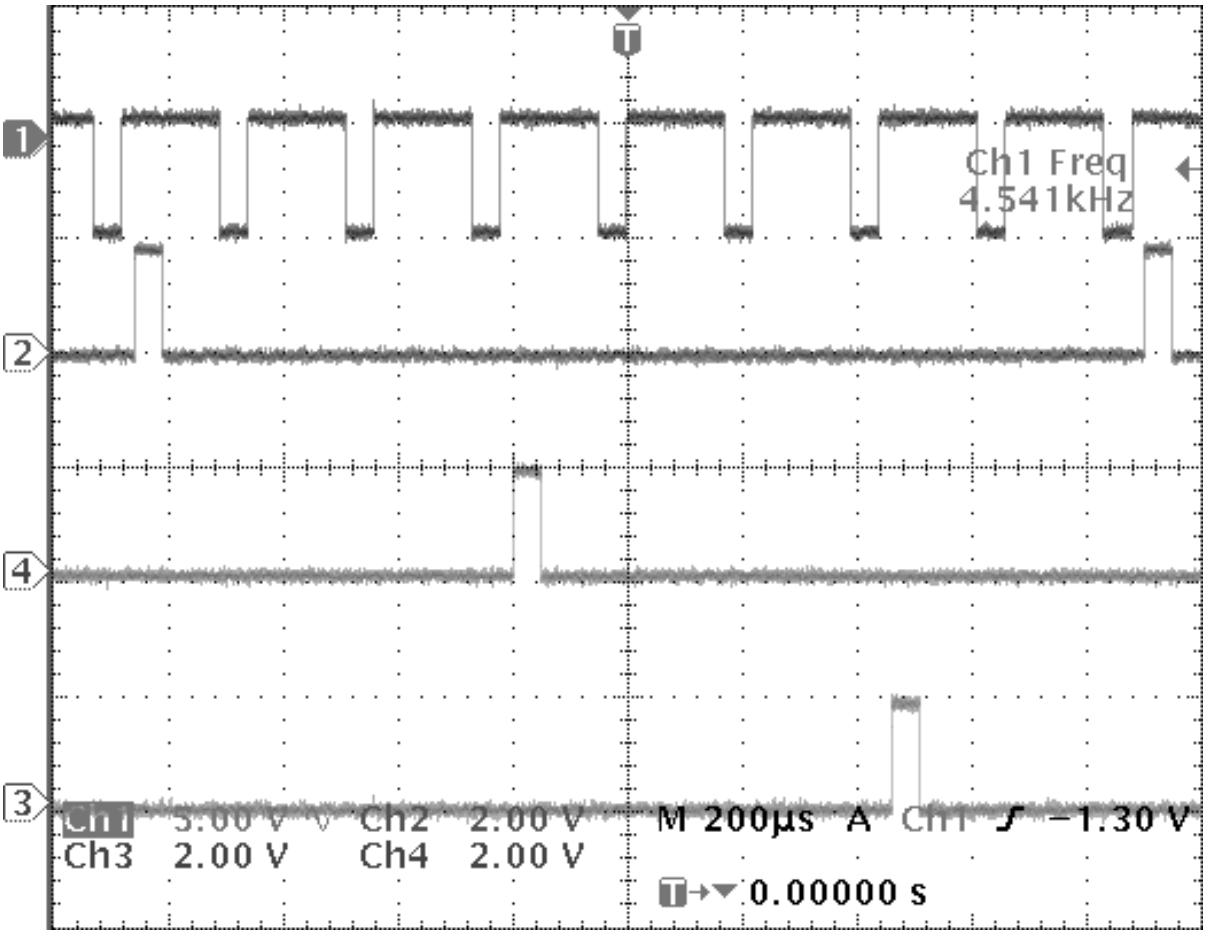

Figure 50: Stimulus for the PPS array, showing the reset signal and three read lines

The Selenium-CMOS PPS array was placed onto the readout board in its place. The blue LED from previous tests was oriented above the array on the readout board, and the board was placed inside a copper box with the required wires being routed inside through the built-in hole. The setup of the board inside the copper box is shown in Figure 51.

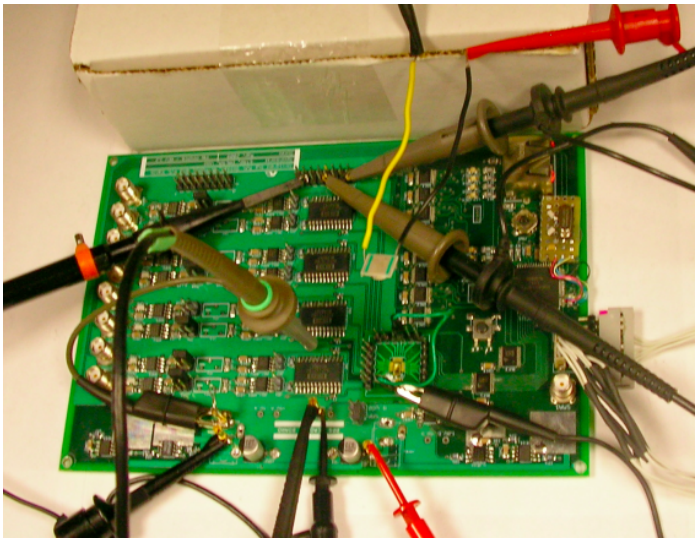

Figure 51: Setup for testing Selenium-CMOS PPS array on readout board

The output of the charge amplifier channels were probed with oscilloscope probes while the LED was turned on to observe the readout of the array. The screenshot in Figure 52 below shows the reset signal on Ch1 and the output of two of the charge amplifiers from the channel 2 and 5 data lines on Ch2 and Ch3 respectively. It can be seen here that these two data lines have noticeably different signal output levels on different readout cycles.

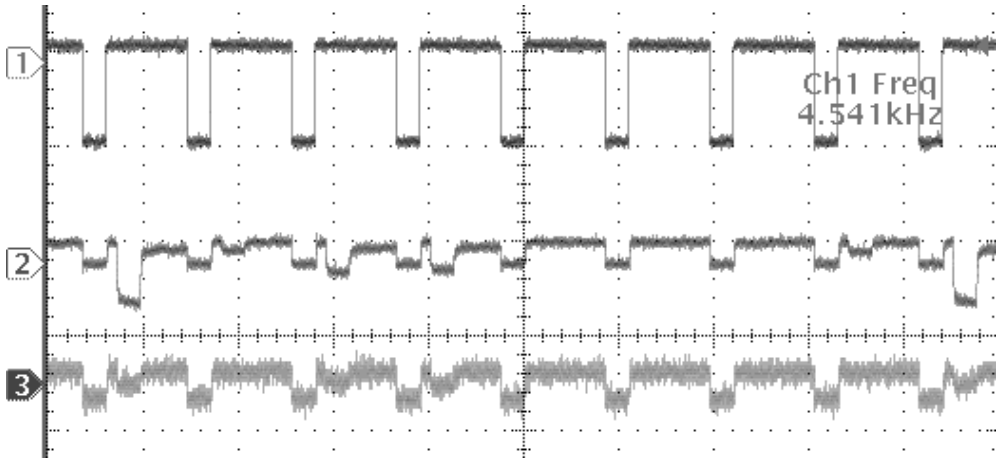

Figure 52: Output for two different channels with PPS array on board

A closeup of the Ch2 waveform is shown in Figure 53 to highlight the signal output difference between two adjacent pixels being read out from the same column on subsequent read pulses.

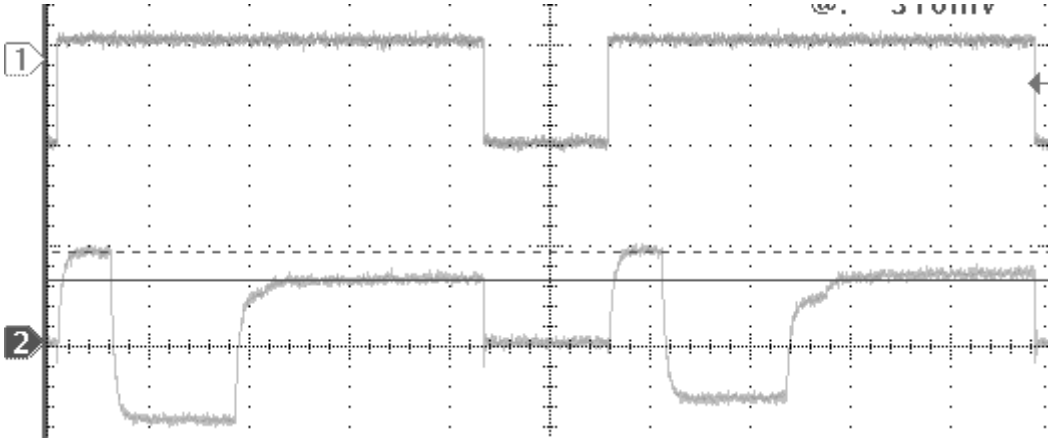

Figure 53: Output showing integration/readout cycles on data line for two adjacent pixels

The results from testing the array with the readout board showed that the output levels were different for pixels across the array after comparing the output levels from different channels and adjacent pixels from the same channel (i.e., pixels in different columns of the same readout row). This was to be expected because several factors came into play affecting the signal level collected by each pixel on the array. While the wire applying the electric field bias to the top contact of the a-Se detector did not block the entire array area, it certainly cast a shadow across the part of the array it was above, having an effect on the number of photons that would strike the a-Se detector there and thus lowering the signal level.

Additionally, the deposition of the Cr top contact on the a-Se detector, using a circular mask, was not even across the entire detector. This would cause the pixels on the

array which did not get the Cr contact deposited directly above them having a smaller electric field bias collecting the charge in the detector to their pixel node. This means that the charge collection there would be lower than that at other parts of the array, since charge collection in a-Se is directly affected by the electric field bias, and the lower charge collection would in turn lead to a smaller pixel output.

4.4 X-Ray Testing of Array

The Hewlett-Packard 43805N X-ray System, which was used to conduct the tests with X-rays, is shown in Figure 54. This machine uses a tungsten target tube to generate X-rays.

Figure 54: X-ray System used to test Selenium-CMOS PPS array

To conduct tests with X-rays, the test fixture was placed inside the X-ray System and positioned in a way so that the sample inside the test fixture was underneath it. A 40 kVp X-

ray energy beam was used with 2 mA of tube current and the test was conducted the same way as the optical tests, with the transient readout measuring the current through the Selenium-CMOS PPS array and the X-ray signal being pulsed on and off during the test for durations of 30 seconds initially, increasing to one minute, then two minutes, and finally five minutes. Figure 55 shows the setup of the test. It should be noted that lead shields were placed over top of the battery supplying voltage to the PPS transistor gates during the test to protect it from getting struck with X-rays.

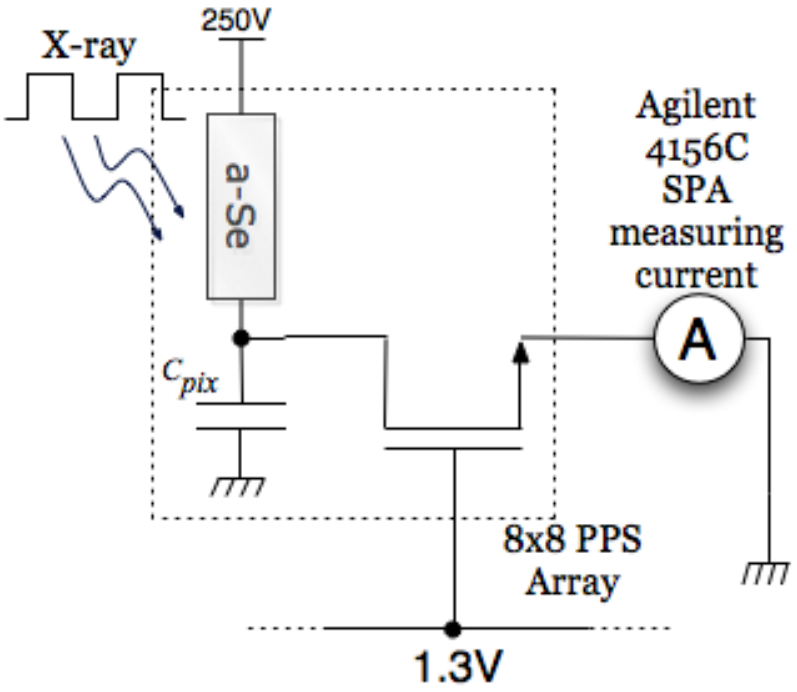

Figure 55: Pulsed X-ray current test setup

Figure 56 below shows the results of the test.

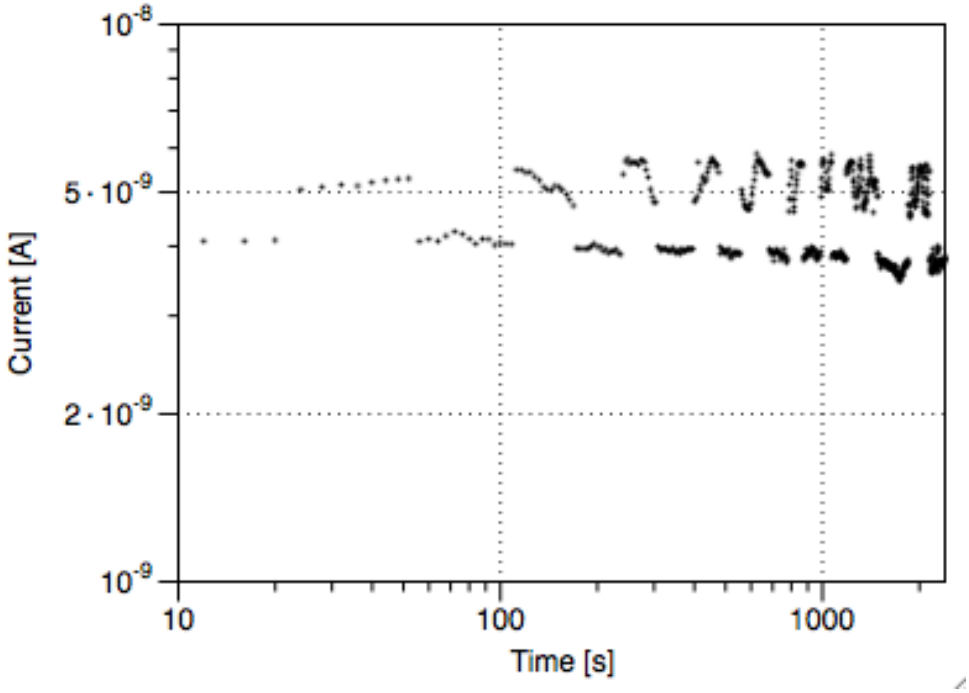

Figure 56: Pulsed photocurrent through Selenium-CMOS array under exposure to 40kVp X-ray beam

The difference between the current level through the detector when the X-ray source is on and when it is off is about 1 nA consistently based on the pulsed test. This clearly shows responsivity to X-rays. To quantify the photocurrent more clearly as was done with the optical tests, another test was run after the detector was allowed to relax again, with the X-ray System being pulsed on (again, 40 kVp at 2 mA of tube current) and being left on to measure the current, which would also allow for analysis of the linearity. Figure 57 shows the transient response of the test.

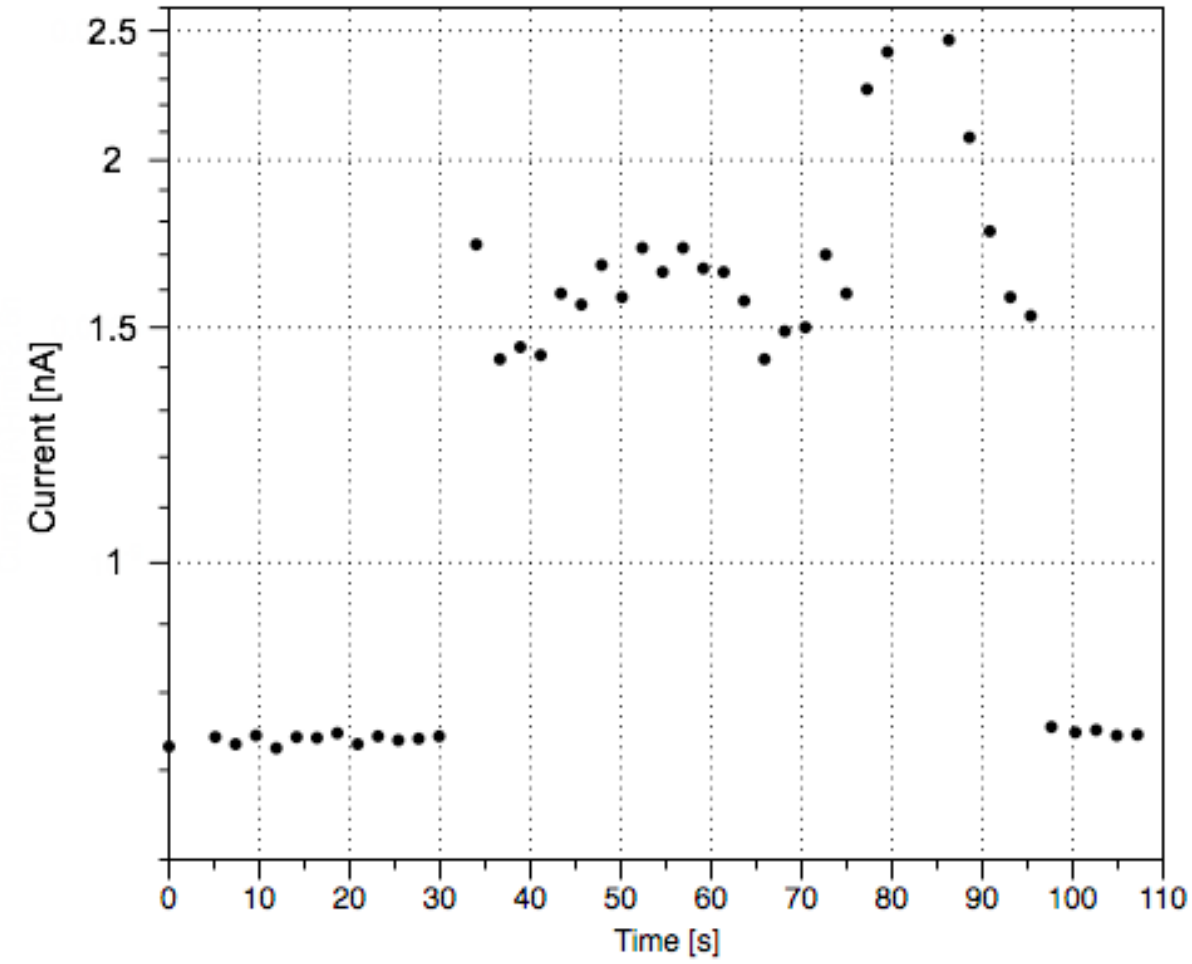

Figure 57: Transient response to single one-minute pulse of 40 kVp X-ray beam

The average relaxed dark current level before X-ray excitation was 0.74 nA, and the the average current that was generated during the minute that the X-ray beam was on was 1.77 nA, giving a photocurrent due to X-rays generated by the detector of 1.03 nA. The response of the detector while the X-ray beam was on is shown represented as voltage accumulated on a 100 nF capacitor in Figure 58 to show the detector's linearity. The dosimeter placed inside the X-ray machine during the X-ray test read dose rates varying from 205 mR/s to 220 mR/s (being on the higher near the end of the minute mark) with a total

integrated dose after the test of 13.71 R. The dose rate variation can account for the deviation from its good linear characteristics towards the end of the test.

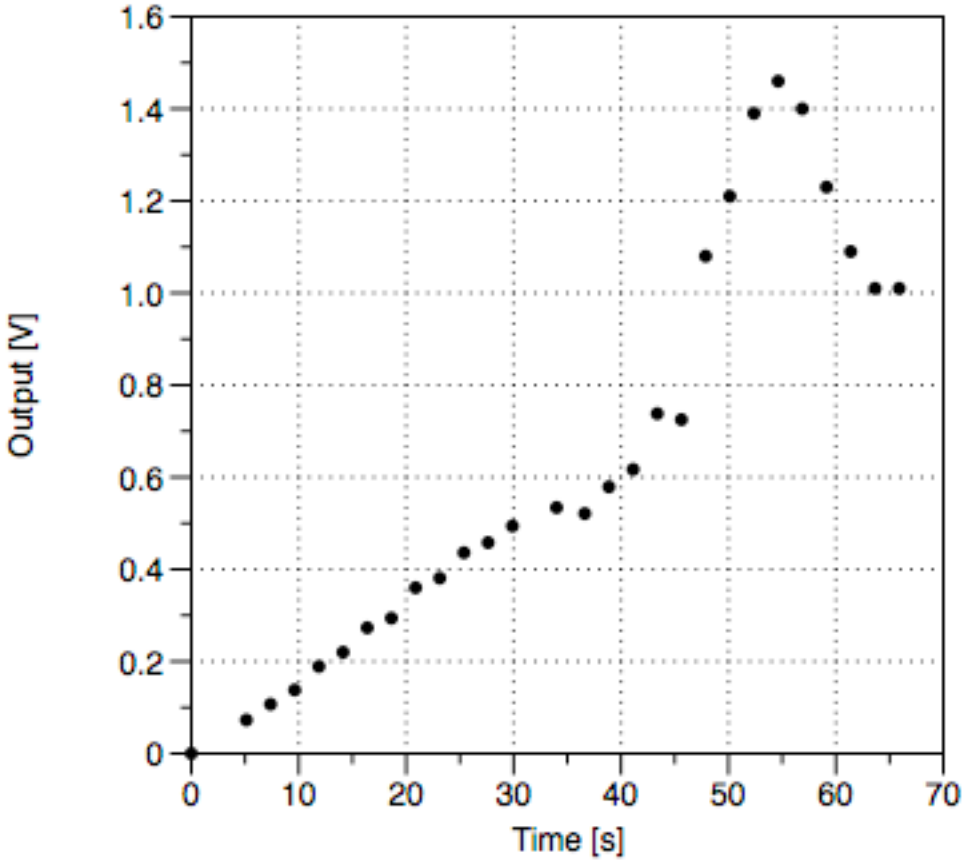

Figure 58: Selenium-CMOS detector linearity under 40 kVp X-ray beam

4.4.1 Analysis of X-ray Photocurrent

It is necessary to do a theoretical analysis to quantify whether the test results yielding a photocurrent of 1.03 nA in the Selenium-CMOS detector due to 40 kVp X-rays are reasonable. The 40 kVp beam has photon energies from 40 keV and below. Knowing that the X-ray System uses a tungsten target tube, the spectrum of the beam can be generated using X-ray spectrum simulation software developed at the J.P. Robarts Research Institute in

London, Ontario, based on a published algorithm from [21]. To get the fluence of X-ray quanta on the detector, the distance from the X-ray tube to the detector needed to be quantified. To extract this parameter, the dose rate was measured at two different distances above the sample. Assuming a $1/L^2$ dependence between exposure and distance from the tube (point source), the dose rate R (R/s) is given by:

$$R = \frac{k}{(L-d)^2}, \tag{11}$$

where k is some constant, L is the distance from the tube to the detector, and d is the distance above the detector. The two pairs of measured values for d and R were ($d_1 = 1.8$ cm, $R_1 =$ 282.5 mR/s) and ($d_2 = 3.7$ cm, $R_2 = 321$ mR/s). Using this data with the equation above, the constant k can be cancelled out, leaving one equation with L as the only unknown, which was solved to be 32.5 cm.

A 40 kVp beam with 2mA of tube current attenuated by the 0.5mm beryllium tube window and the air in the chamber, 32.5cm away from the detector, generates the spectrum in Figure 59, which shows the amount of X-ray quanta per unit area on the detector at each energy level present in the 40 kVp beam.

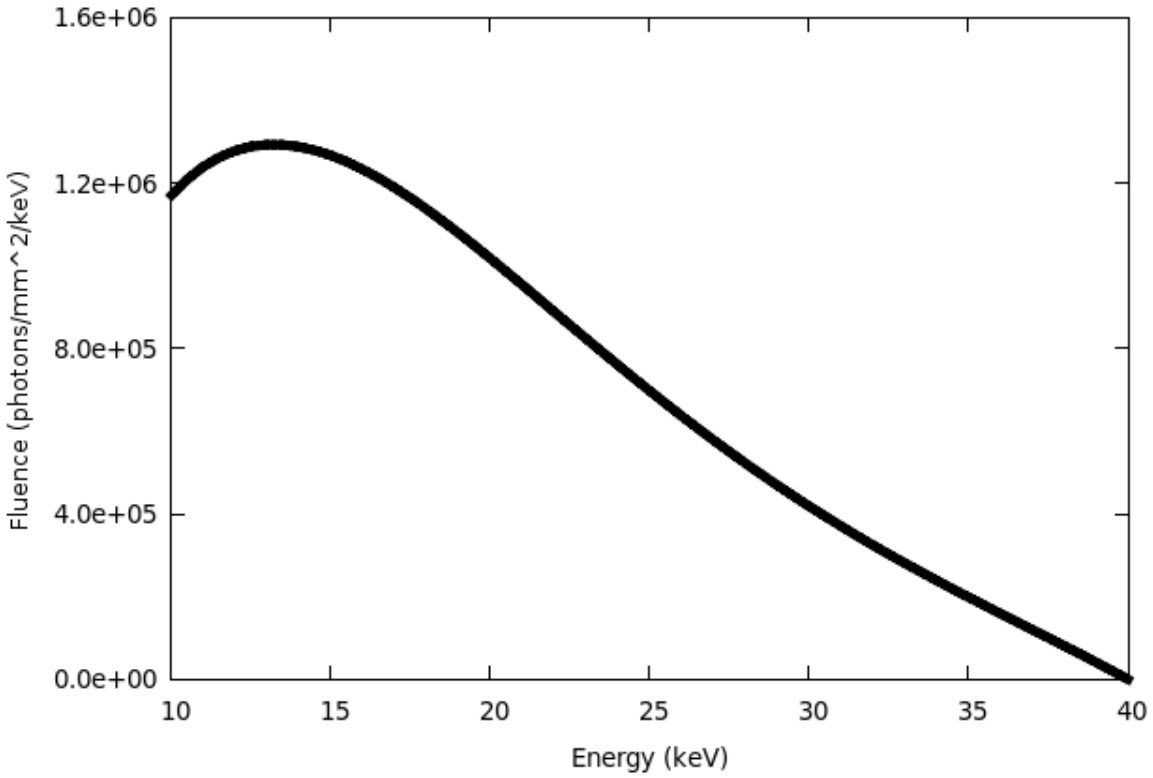

Figure 59: Simulated spectrum of 40 kVp X-ray beam on the Selenium-CMOS detector

A portion of the X-ray quanta hitting the a-Se detector will be absorbed to generate electron-hole pairs, while others go through without getting absorbed or interaction. This is dependent on the quantum detection efficiency (A_Q) of the detector given its thickness and composition. The quantum detection efficiency is given by the following equation:

$$A_Q = 1 - e^{-\alpha(E)t_{det}}, \tag{12}$$

where $\alpha(E)$ is the linear attenuation coefficient of selenium, provided by the PENELOPE Monte Carlo software package from [22], and t_{det} is the thickness of the a-Se detector, 75 µm. Figure 60 shows the quantum detection efficiency of selenium for varying photon energies.

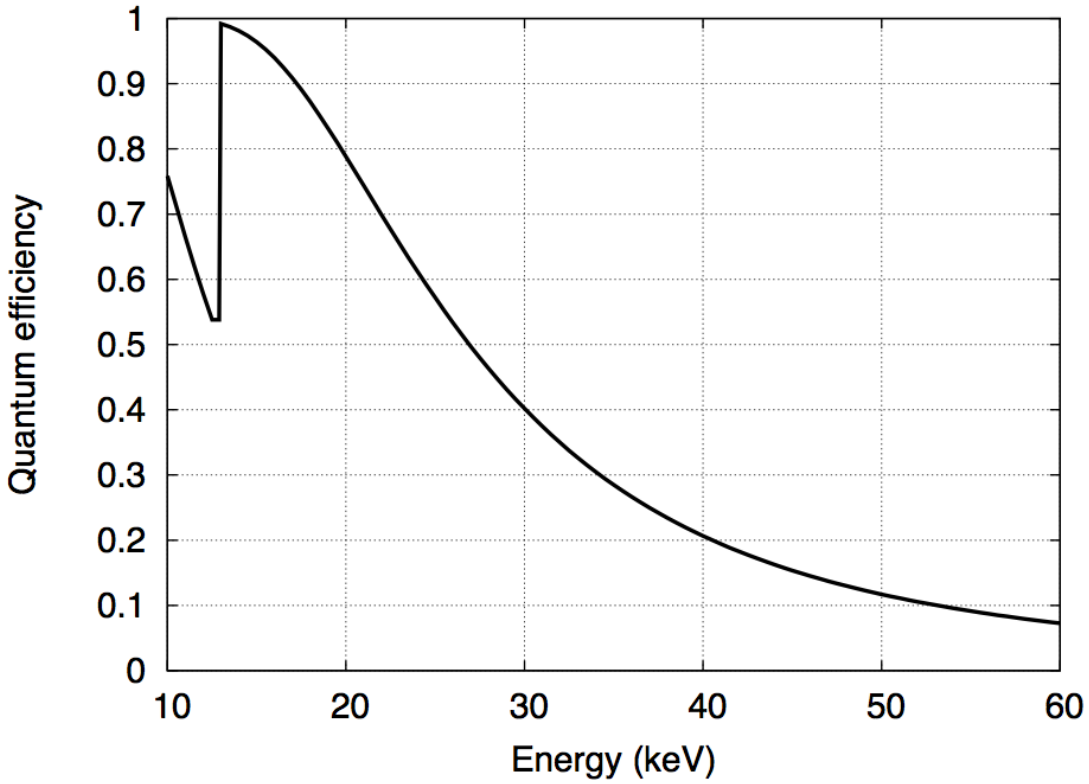

Figure 60: 75 µm a-Se detector quantum efficiency

Given the quantum efficiency and the fluence of X-ray quanta on the detector, the generated charge Q_{ph} is given by the following equation:

$$Q_{ph} = \int_0^{E_{\max}} \frac{\theta(E) A_Q A_p F_p}{W_{\pm}(E,F)} E dE, \tag{13}$$

where $\theta(E)$ is the number of incident X-ray photons of energy E per unit area, A_Q is the detector quantum efficiency, A_p is the area of the pixel, 1600 µm^2, F_p is the pixel Fill Factor, 99.1%, F is the electric field, 3.33 V/µm, and $W_{\pm}$ is the electric field and photon energy dependent energy required to free one electron-hole pair, given by [23]:

$$W_{\pm}(E,F) = (6 + \frac{15 \times 10^6}{0.8F}) \times (0.72 + 0.56e^{-\frac{E}{62.7}}). \quad (14)$$

The result of the integration of the equation for the charge generated in the detector gives Q_{ph}=4052.4 eV. Knowing that the mobility of holes in a-Se is μ_h=0.13 cm^2/Vs and the mobility of electrons is μ_e=0.003 cm^2/Vs, and assuming that the electron-hole pairs giving rise to this charge are generated somewhere in the middle of the detector, a distance of 40 μm from the collecting electrodes, the photocurrent generated by Q_{ph} can be calculated using the following equations:

$$v = \mu F, \quad t = \frac{d}{v}, \text{ and } I_{photo\_pix} = \frac{Q_{ph}}{t}. \quad (15), (16), \text{and } (17)$$

The carrier velocity v for electrons and holes is given by their respective mobility μ multiplied by the electric field F, which can be used to calculate the transit time t through the detector from the point of generation. Assuming holes and electrons each make up half of the total photocurrent, the photocurrent in one pixel is I_{photo_pix} = 359.3pA. So for the 8×8 array, I_{photo} = 64 I_{photo_pix} = 22.995 nA. This calculated value is 22.3 times larger than the measured photocurrent of 1.03 nA.

The discrepancy is likely due to many factors affecting the experimental results that were not taken into account in the analysis. The generated spectrum of the 40 kVp beam is highly dependent on the tube current, which was read as 2 mA on the X-ray System's analog meter but has an error associated with it. Additionally, the error associated with the distance from the sample calculation, whose error is magnified due to the $1/L^2$ relationship, also affects the generated spectrum. The model used to generate the spectrum itself is the relative

best fit to the X-ray System of the available ones, but is not necessarily a precise representation of the makeup of the X-ray beams this particular X-ray machine emits. Finally, the electric field across the a-Se detector on top of the PPS array was not uniform throughout because the Cr top contact was not deposited across the entire array area, and as such pixels on the edges would have a lower electric field bias and thus would conduct less than the calculated I_{photo_pix}. The electric field also has an effect on $W_{\pm}$, which affects the generated charge value, per the Q_{ph} equation.

Chapter 5

Conclusion

5.1 Summary

A passive pixel sensor (PPS) array in 0.18 μm CMOS technology was fabricated in order to serve as the basis for taking the first step towards a CMOS-based medical imaging system which would be able to provide faster readout, higher resolution, and lower noise sensitivity than traditional amorphous silicon thin-film transistor digital imaging systems. Amorphous selenium was deposited on top of the active array area to provide an integrated Selenium-CMOS detector. A printed circuit board was designed to facilitate the testing of the array. The results of the PPS array were promising with optical wavelengths and X-rays from the signal current generated versus the dark current, showing very good linearity as well. Testing the array using the printed circuit board readout system showed that the output of the pixels

from the array varied across it due to shadowing from the bias contact and varying charge collection efficiency across the array, confirming the operation of the array as an image sensor. The X-ray photoconductivity was compared to the expected value in a 75 μm a-Se detector and given the uncertainties associated with the calculation and measurement, it was within a reasonable range.

5.2 Future Research Paths and Recommendations

The work here has shown that the area of Selenium-CMOS integrated imagers indeed is a path worth pursuing. Future work will include fully characterizing the 8×8 PPS array for real-time and static imaging followed by fabricating CMOS arrays with active pixel sensor architectures for faster readout and lower noise susceptibility than their passive pixel architecture counterparts. Another potential path could even involve fabricating a photon-counting based pixel in CMOS technology and integrating it with an amorphous selenium detector as has been proposed [24], since the feasibility of interfacing the two technologies has now been shown.

Improvements can be made to standalone testing of the array by introducing a shutter for optical tests. As well, a more streamlined system of mounting the array on the readout printed circuit board through a socket system should be considered for the next revision. The readout printed circuit board for the array can also be redesigned to allow for easier testing of the array. Using an FPGA to provide stimulus for the array could make it easier to generate timing signals, especially if APS systems with multi-control lines are being tested, and placing analog-to-digital converters on board would allow for easy capture and storage of the

digitized output of the array by the FPGA. This would lead to being able to capture and store the output frames of the array for generation of grayscale images based on the digitized intensity at each pixel output.

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