a-Si:H-Silicon Hybrid Low Energy X-ray Detector

by

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AUTHOR'S DECLARATION

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

Low energy X-ray (< 20 keV) detection is a key technological requirement in applications such as protein crystallography or diffraction imaging. Silicon based optical cameras based on CCDs or CMOS imaging chips coupled to X-ray conversion scintillators have become a mainstay in the field. They are attractive because of fast readout capability and ease of integrated circuit implementation due to modern semiconductor fabrication technology. More recently, hydrogenated amorphous silicon (a-Si:H) thin film technology, that had enabled a huge influx of large area display products into the commercial display market, has been introduced to digital imaging in the form of active matrix flat panel imagers (AMFPIs). Although thin film technology can enable large area X-ray imaging at a potentially lower cost, the existing technology lacks spatial resolution requirements for higher performance crystallography and diffraction imaging applications.

This work introduces a high resolution direct conversion silicon X-ray detector integrated with large area thin film silicon technology for sub-20 keV photon X-ray imagers. A prototype pixel was fabricated in-house using a fabrication facility (G2N) utilizing plasma enhanced chemical vapor deposition (PECVD), reactive ion etching (RIE), photo-lithography, and metal sputtering technologies. Unlike most active matrix display products, top-gate staggered a-Si:H thin film transistor (TFT) were implemented to take advantage of a novel thin film silicon pixel amplification device architecture.

The detector performance was evaluated with an iron 55 isotope gamma ray source to mimic low energy X-ray exposure. I-V and C-V measurement techniques indicate that the hybrid pixel functions as expected and is promising for low cost, high resolution, large area X-ray imaging (< 20 keV) applications. We also performed a noise spectrum investigation to estimate the lowest detection signal level limit and proposed a model rooted in device physics for the pixel output and gain.

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Lastly, I would like to thank Prof. Karim S. Karim as my supervisor and everlasting supporter since my roommate committed suicide in 2010.

Dedication

To my mother and my sister.

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Chapter 1
Introduction

1.1 Digital X-ray Imaging

Since the discovery of X-ray by German physicist, W. K. Roentgen in 1895-6, capturing X-ray intensity information has been performed by various types of phosphors including CsI:Ti, Gd_2O_2S, LaOBr, or Y_2O_2S:Tb and transferred to a photographic films with optical cameras. However, these methods suffered from the following difficulties:

- Lack of data storage and prompt retrieval
- Inability to perform image processing on raw data directly
- Captured images required a multi-step lossy process to transfer
- Chemical waste problems with film developing and associated environmental concerns
- Real-time imaging was not feasible with static images

To address these problems, X-rays went digital starting in the 1960s in the nondestructive testing equipment industry [1]. Later, digitization of X-ray imaging utilized charge-coupled devices (CCD) interfaced to scintillators where the scintillator converted the X-rays into optical signals that were subsequently imaged by a silicon CCD chip [2, 3].

1.2 Detector Technologies

1.2.1 Direct Conversion X-ray Detectors

Direct conversion semiconductor radiation (X-ray, gamma-ray, etc.) sensors saw widespread use in medical, scientific, and industrial systems due to their higher resolution, high sensitivity and fast readout speed. Direct conversion systems eliminated the X-ray to light conversion step enabling higher resolution than their indirect scintillator based X-ray imager counterparts. This enabled a manufacturing cost reduction as well because both expensive scintillators and fiber optics to couple the scintillator to the CCD chip were eliminated. One of the prominent examples of a direct conversion semiconductor X-ray detector is the silicon drift detector (SDD) [4-6] shown in Figure 1.

Due to the relatively low bandgap (1.1 eV) of silicon, X-ray absorption performance of silicon is limited to low energy photons (< 20 keV) as is the case for protein crystallography (as depicted in Figure

2), X-ray spectroscopy [7], medical imaging [8], and archeology [5]. SDD enabled such applications with lower cost, lack of liquid nitrogen cooling, small number of readout channels, low noise, and high readout energy resolution [9].

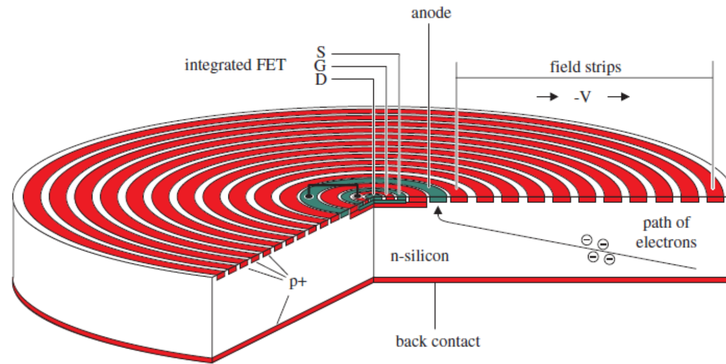


Figure 1 A silicon drift detector example [10].

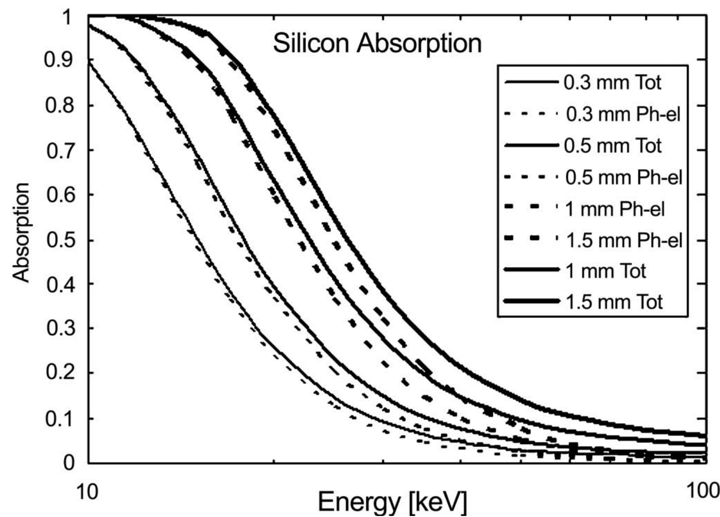
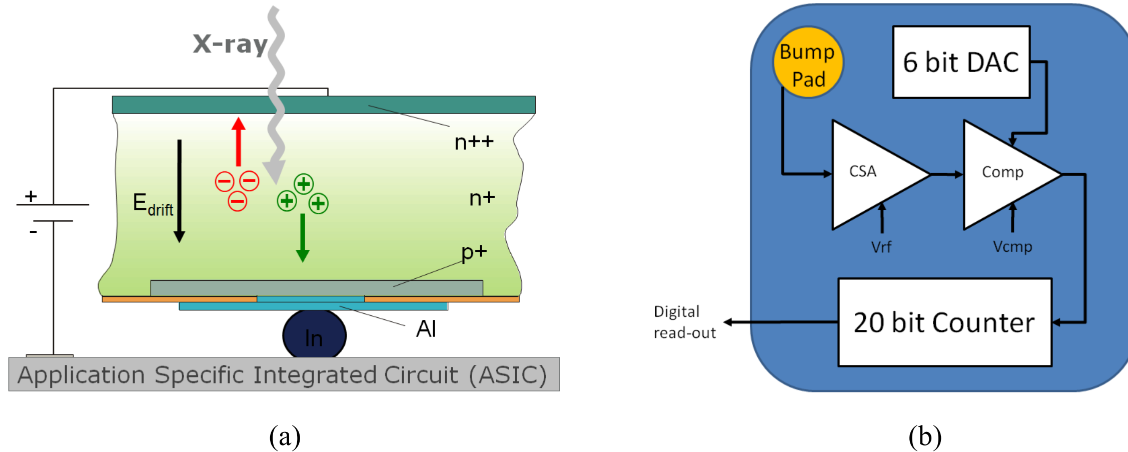


Figure 2 X-ray absorption in silicon adopted from [11].

Another more recent example of the use of direct conversion silicon for X-ray imaging is the Pilatus detector from Dectris^{TM}. This detector is composed of silicon X-ray detector components bump bonded to a very high performance ASIC photon counting circuit as depicted in Figure 3. The readout time for each pixel is reported to be as low as 7 ms (or alternately, a frame rate of 20 images per second) while the minimum capacitance of the photon detector silicon element is kept low to effectively reduce detector

noise. Since the silicon detector thickness defines the detector capacitance and also the maximum photon detection energy, Pilatus is sold with an option to obtain a silicon semiconductor thickness of 320, 450, or 1000 μm. Its resolution is reported to reach 487 by 197 pixels with an active area of 83.8 by 33.5 mm^2 implying a pixel pitch of $170 \times 170\ \mu m^2$ while maintaining the dynamic range of 20 bits, or 1:1048573 [12]. The pixel pitch is presumably large due to the complex circuitry needed for photon counting.



(a) (b)

Figure 3 Schematic of Pilatus from Dectris™. (a) shows the hybrid pixel with silicon detector and (b) shows photon counting circuit ASIC diagram attached to each pixel. Adopted from [12].

1.2.2 Indirect Conversion X-ray Detectors

In contrast to higher performance direct conversion detectors, the method by which X-rays are detected via scintillators is known as indirect conversion imaging since the conversion of X-ray signal to electronic charge involves an intermediate light conversion step in the scintillator. CCD or CMOS digital cameras are commonly used to interface to the scintillator to capture the light photons, however, it is not possible to efficiently capture small quantities of X-ray photons without the use of fiber optics, as depicted in Figure 4 (a) because of large optical losses (for example, if traditional lens based methods are used). A disadvantage of using a CCD camera for image capture is that CCDs can have a lower dynamic range due to the shallow well associated with the MOS capacitor in deep depletion [13, 14]. CMOS imagers, as depicted in Figure 4 (b), utilize silicon photodiodes which provides larger dynamic ranges up to 130,000 even for pixel sizes of 25×25 μm while maintaining a readout speed of 30 frames per second [15].

Detector sizes of up to 20 cm by 20 cm of area can be achieved using both CCDs with optical fiber enhancements as well as using their CMOS counterparts. However, the price range of a scintillator, fiber optic coupling and CMOS backplane is somewhat larger compared to the price of TFT flat panel arrays. More importantly, a scintillator emits the converted photons without any particular direction and causes image blurring. In other words, converted photons may travel to adjacent pixel to generate a false signal. Even if a structured scintillator is used, the image blurring is larger than when direct conversion X-ray imagers are employed.

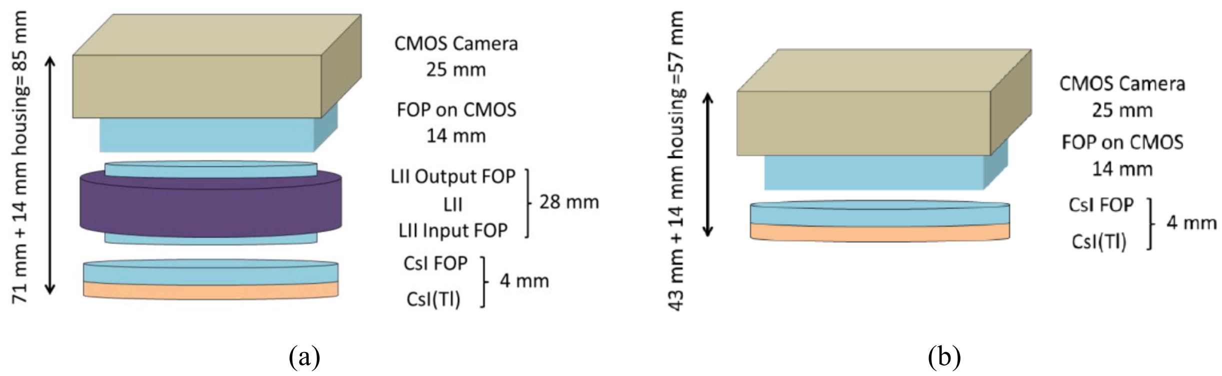


Figure 4 (a) CCD detector and (b) CMOS detector schematics. Adopted from [15].

1.2.3 Large Area Thin Film Silicon X-ray Detectors

The introduction of hydrogenated amorphous silicon (a-Si:H) thin film transistors (TFTs) opened up an opportunity for large area and low cost detectors driven by active matrix pixel driving technology [13]. The active matrix flat panel imager (AMFPI) was also introduced with a phosphor integrated detector, which reads out optically converted X-rays with photodiodes (indirect conversion) and a direct conversion method with amorphous selenium (a-Se), which converts the X-ray directly into electron-hole pairs to be read out by TFTs in the active matrix backplane as depicted in Figure 5.

Although TFT active matrix technology introduced a cost-effective readout for large area applications, AMFPI still requires pricy X-ray conversion layers: scintillators and fiber optic plates for the indirect conversion scheme, and a high quality a-Se layer for the direct conversion method. Also, integration of an additional photodiode in the indirect conversion scheme requires additional process steps, which amplifies production cost. On the other hand, the direct conversion method suffers from reliability issues primarily

the crystallization of the a-Se layer, which leads to an extreme dark current (noise), and extreme care is required to prevent exposure from excessive heat and photons [16].

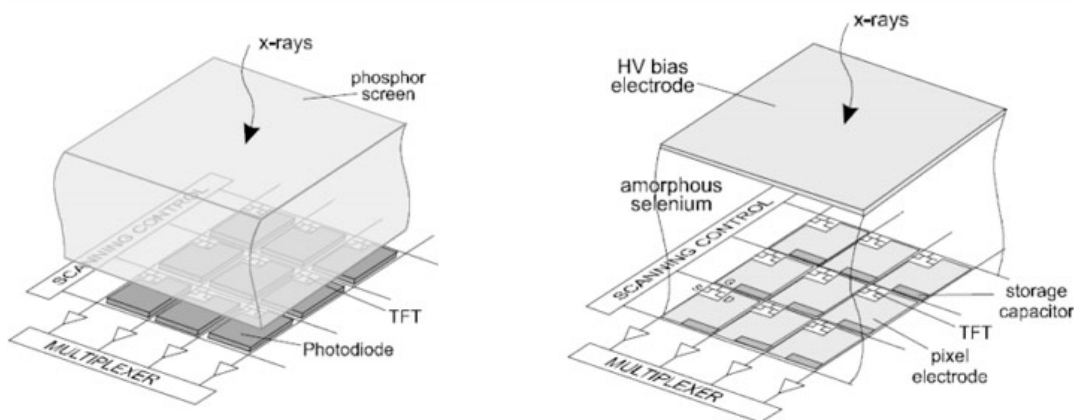


Figure 5 Two types of AMFPI detectors. Indirect (Left) and Direct (Right.) Adopted from [17].

1.3 Protein Crystallography

1.3.1 Overview

One of prime example of low energy (sub 20 keV) X-ray applications is protein crystallography, which plays a great role in molecular biology and pharmaceutical research [18]. So-called molecular medicine research requires investigation of molecule structures (3D structures of protein molecules) because the structure defines the function and characteristic of the molecule and provides insight to negate the functionality of any disease protein.

The basic set up of protein crystallography is shown in Figure 7. To prepare the crystallized sample, the protein must be frozen using cryogenics technology. Meanwhile the X-ray beam must be narrowed with optical elements and the direct path to the detector needs to be blocked to ensure only diffracted spots are detected. Thus, the crystallography system includes not only X-ray sources and detector elements, but also optics for X-ray, cryogenics, and crystal mounting apparatus, as depicted in Figure 6.

From a computational viewpoint, the X-ray beam must be monochromic to ensure protein structure re-construction because diffracted spots (Bragg spots) change as a function of X-ray wavelength and protein structure. Typically, 6 to 20 keV photons (or a wavelength of 0.21 to 0.06 nm) are chosen which is close to the atomic distance of common protein target molecules. To obtain a complete 3D reconstructed image,

the Bragg spots must be obtained from various incident angles. So, the protein sample needs to be turned along the x, y, and z axes [19].

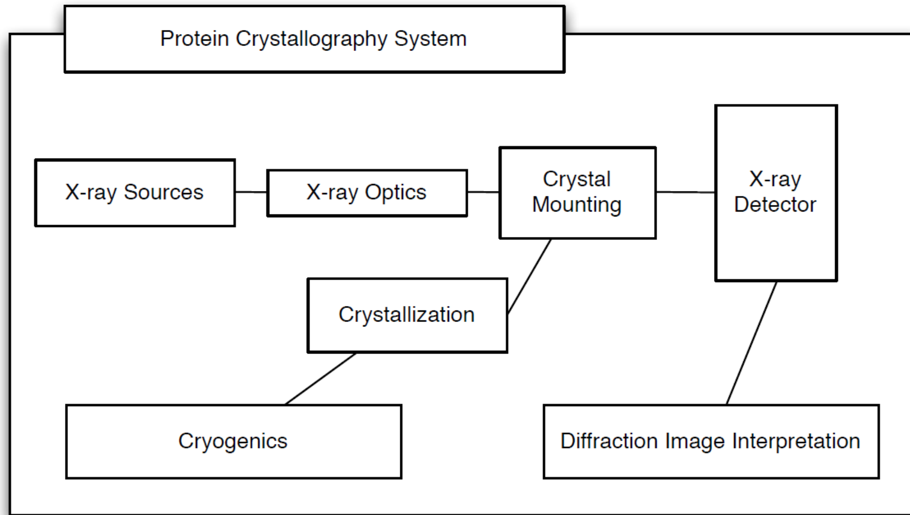


Figure 6 Core components of protein crystallography.

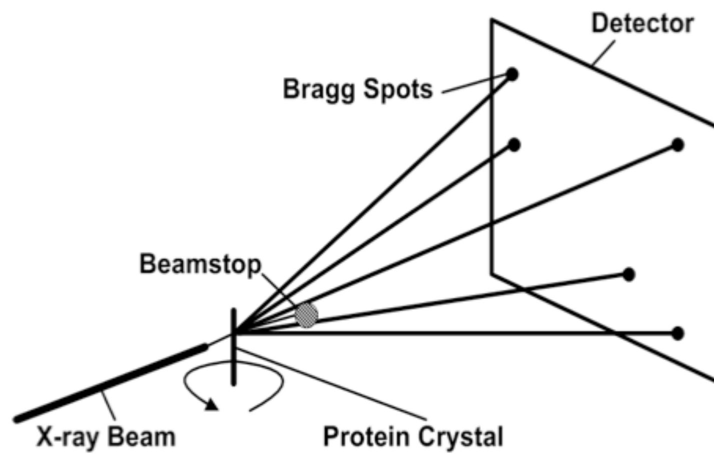


Figure 7 Typical protein crystallography set up. Adopted from [20].

1.3.2 Requirement of digital protein crystallography

At first glance, the size of the detector appears a key requirement for protein crystallography since in the ideal case, the detector must be large enough to capture all Bragg spots effectively [19]. However, collecting the complete set of Bragg spots is not required because the first 100 orders of diffraction data are enough to rebuild the crystalline structure of sample protein. Usually, a detector size of 20 cm by 20 cm is sufficient to cover the first 100 orders [21]. Of course, the imager size depends on the distance from the crystallized protein proportionally. If the detector has sufficiently high resolution, the detector size can be shrunk by closing the gap between the protein sample and the detector itself reducing the requirement on the X-ray source power.

In some applications, the strongest Bragg spots can be as high as 1.2×10^5 X-ray photons per pixel, while non-exposed pixels show almost zero counts as the Bragg spot distribution follows a Gaussian function [22]. Since only 0.1 % of the incident X-ray beam is scattered by the protein and prolonged exposure to X-ray is not preferable due to protein structure degradation, possible solutions are either reducing the intensity of the X-ray beam or to implement a fast readout. Because a fast readout was not feasible with image plate detectors, which required more than 2 to 3 seconds per exposure, the sensitivity of the detector became important to compensate for the reduced X-ray source intensity. However, digital X-ray detectors (scintillator based and direct conversion) could resolve such problems without sacrificing sensitivity because of fast readouts.

The readout time depends on the kind of X-ray source used. Generally, two kinds X-ray sources are relevant to protein crystallography: rotating anode lower power home sources, which usually operate in the 6 to 10 keV range, and much higher power synchrotron sources, which have variable energy, but operate mostly at around 12 keV. For rotating anodes, longer signal charge integration (typically a few minutes [23]) is required compared to synchrotrons (a couple of seconds [23]) because the X-ray intensity is limited. Synchrotron provides a high intensity homogeneous beam, which produces more diffraction spots in a short time interval. The readout time includes the X-ray photon detection time and the detector element to external circuitry transfer time for converted charge.

The sharpness of the X-ray diffraction pattern depends on the spatial resolution of the detector as well as the distance from the protein. Normally, 3 to 5 pixels can hold a single Bragg spot while at least five pixels are required to distinguish between two adjacent Bragg spots [19]. For example, if a 12 keV X-ray photon (wavelength around 0.1 nm) illuminates a protein crystal with a unit cell dimension of 20 nm while crystal-to-detector distance is 20 cm, a typical Bragg spot size would be 100 to 300 µm. Thus,

requiring pixel sizes of 50 to 200 μm [19]. Table 1 shows one set of design consideration factors as applied to the existing, primarily indirect detection detectors.

Table 1 Requirement of digital protein crystallography detectors.

Parameter	Values
Detector area	Larger than 20 cm by 20 cm
Dynamic range	Larger than 10^4
Readout time	Around 1 second but smaller the better.
Pixel size	Smaller than 200 μm
X-ray energy	20 kVp (rotating anode) or 12 keV (synchrotron)
Object size	Around 0.18 nm (Inter-atomic distance of protein)

1.4 Motivation and Chapter Outlines

Direct conversion crystalline silicon layers have the best sensitivity and spatial resolution performance with X-ray photons < 20 keV. Crystalline silicon is one of most widely produced materials due to the emergence of the high volume semiconductor industry since 1980s. Thus, they can be provided with at a lower cost than a comparable scintillator and with much higher reliability than a direct conversion a-Se layers. Silicon wafers currently processed can reach up to 12” (or 300-mm-diameter) in size. If a silicon X-ray conversion layer can be integrated with large area low cost thin film silicon readout, a low cost, high resolution and high sensitivity solution can be realized for low energy X-ray detection applications such as protein crystallography.

Today, large area direct conversion silicon X-ray detectors are already in production but require a process of tiling and bump bonding, which is both expensive and poses yield issues when performed over a large area. Photon counting detectors for protein crystallography such as the Pilatus by Dectris™ employ small four side buttable silicon photon counting pixel arrays bump bonded to high resistivity silicon detectors with a selling price ranging from $150k for a modest sized 1” square imager to around $1M for full-sized large area devices.

In addition, indirect detection thin film amorphous silicon based digital X-ray devices using scintillators suffer from degraded spatial resolution due to the indirect conversion process as well as lower signal levels due to the reduced conversion gains of the scintillator at low energies (as compared to direct conversion crystalline silicon). Amorphous selenium based direct conversion devices integrated with amorphous silicon TFTs offer yet a third alternative that can offer a credible challenge to the higher spatial resolution of direct conversion silicon, however, the selenium detectors have lower conversion gains and are temperature sensitive leading to a tradeoff between manufacturing cost and reliability.

This work implements high resistivity crystalline silicon as a direct conversion X-ray to electron-hole pair converter. The resulting signal is read out using a low-cost, large area capable device: a-Si:H TFTs. Because it is not economical to deposit thick high quality crystalline silicon (where sufficient thickness is required to absorb most of the impinging X-rays) on top of typical TFT devices which are deposited on glass, we propose a novel approach where the a-Si:H TFT readout element is deposited on top of the detector element (crystalline silicon) In Table 2, the benefits of the proposed approach are contrasted with the approaches taken currently by various imager manufacturers operating in the protein crystallography markets. Note that the key advantage of our approach is that it offers the best spatial resolution while maintaining the same signal to noise ratio as its indirect detection CMOS and CCD counterparts. Thus, in principle, our detector could (1) be moved closer to the protein sample, thus enabling a reduction in the X-ray source power necessary to get a quality image which would enable home X-ray sources to complete tasks that are normally the domain of synchrotron sources and (2) investigate new materials that require the higher spatial resolution because of unique molecular structures not visible using traditional imagers. Although the dynamic range of our detector is considerably lower than its counterparts, the smaller pixel size would see a reduced number of photons as compared to a larger sized pixel (assuming the photon fluence is the same for both designs). Here, a 25um pixel would see 64X less incident photons than a 200um pixel counterpart. Moreover, real-time readout can enable an artificial increase in dynamic range, for example, by constantly reading out the detector and summing the frames to obtain the final image.

In Chapter 2, following a brief introduction to thin film silicon transistor operation physics, the novel pixel architecture integrating a crystalline silicon detector with an a-Si:H TFT readout circuit is introduced along with its operation principle, basic device physics and initial simulation results. Two pixel device designs are discussed: one adapted from previous work and a new higher performance design involving a passivation layer to isolate the silicon X-ray conversion layer from the TFT. In chapter 3, following a brief introduction to TFT fabrication processes, the fabrication process developed for the two

pixel designs is presented. The development and characterization steps for each layer employed in the pixel design are discussed along with each process step and condition. In Chapter 4, measurements and discussion on multiple aspects of the pixel designs are provided. These range from basic device operation via I-V sweeps, thin film silicon metastability, and electronic noise characterizations. In addition, measurements on the pixel architecture using an iron 55 isotope source which emits 5.89 keV of energy X-ray photons were taken to verify that the device functions adequately for its intended use with X-rays. In Chapter 5, concluding remarks and the contributions of this work are summarized. The appendices contain fabrication process mask layouts and Medici code for the semiconductor device simulator.

Table 2 Comparison of various X-ray detectors for low energy (~ 6 keV) X-ray photon detection.

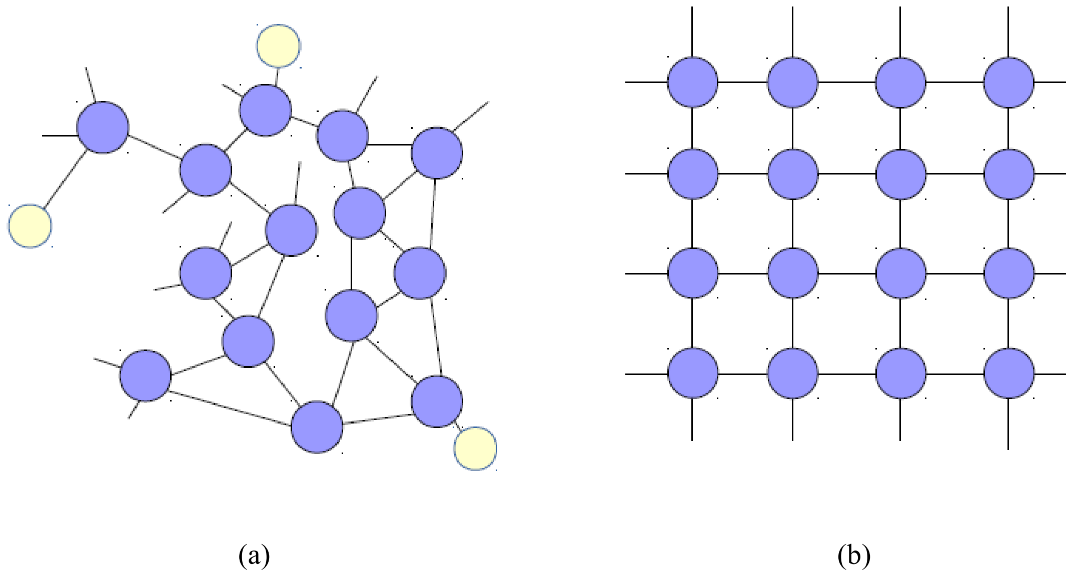
Parameters	Pilatus	Indirect CMOS	AMFPI a-Se	a-Si:H-c-Si Hybrid (Estimated)
Pixel Size	170 μm (down to 75 μm)	50 μm (Indirect)	70 μm	25 μm (direct)
Detector Size	$83.8 \times 33.5\ mm^2$ (four side tileable)	$75 \times 150\ mm^2$ (three side tileable)	$430 \times 350\ mm^2$	$212 \times 212\ mm^2$ (Square area of 12" Wafer)
EHP conversion ($6\ keV/W_{\pm}$)	1667 (c-Si)	167 (CsI:Ti)	125 (a-Se)	1667 (c-Si)
Readout Noise	Negligible	< 150 electrons	< 1500 electrons	< 1500 electrons
SNR	Photon counting	~ 1	0.08	~ 1
Dynamic Range (6keV photons)	1:1,048,573	1:61,750 (0.5 pF cap)	1:120,000 (1 pF cap)	1:3600 (0.03 pF cap)
Readout Speed	20 FPS at max	30 FPS at max	30 FPS	30 FPS
Price per Detector Size ($\$/mm^2$)	51.96	2.00	0.66	0.66

Chapter 2
Hybrid Detector Operation Schema

2.1 Thin Film Transistors

2.1.1 Hydrogenated Amorphous Silicon (a-Si:H)

Figure 8 indicates the atomic bonding structure of a-Si:H in a two-dimensional illustration and is compared to a typical crystalline silicon structure. Figure 8 (a) illustrates the chaotic bonding structure of a-Si:H with a few dangling bonds filled up with hydrogen atoms (bright color.) Such bonding structure is generated from a low temperature (~ 300 ^{o}C) plasma enhanced chemical vapor deposition (PECVD) method where the atomic bonding cannot be controlled separately. However, such low temperature and the use of PECVD enables the fabrication of electronics in a large area format on cheaper alternate substrates, including glass, in an economical manner.



(a) (b)

Figure 8 Two dimensional illustrations on atomic bonding for (a) amorphous silicon and (b) crystalline silicon.

The disorder of the atomic structure illustrates a lot of additional trap states compared to the crystalline silicon layer. The missing atoms at dangling bonds can be interpreted as deep states, depicted in Figure 9,

and the disfigured and irregular atomic bonding leads to tail states where mobility edges need to be defined due to lack of distinct conduction and valence bands [24, 25]. The density of deep defect states in a-Si:H is in the range of $10^{15} – 10^{18}$ $cm^{-3}eV^{-1}$, which is largely dependent on PECVD conditions. Meanwhile, atomic hydrogen (which can be supplied either from a SiH_4 precursor or additional hydrogen dilution) passivates a few dangling bonds to reduce the deep defect states [26].

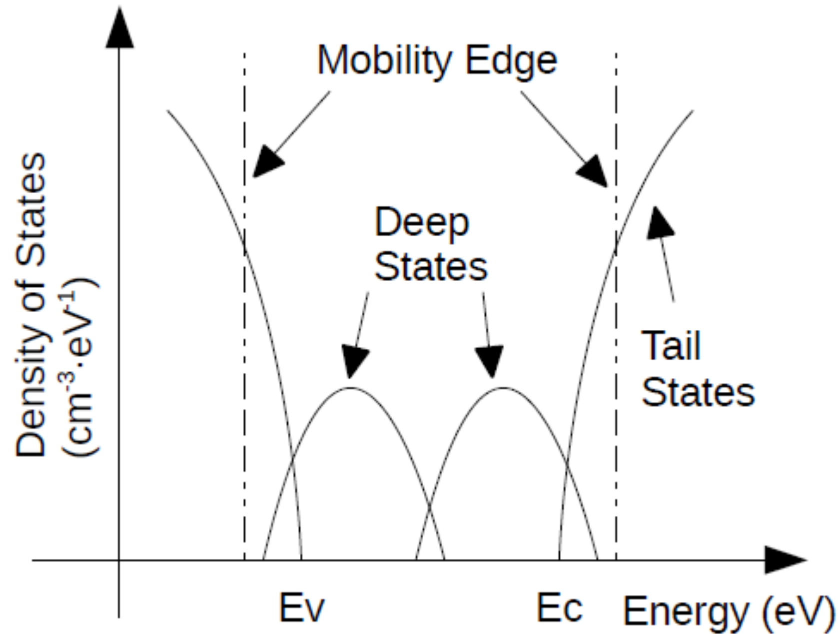


Figure 9 Typical distribution of density of states in hydrogenated amorphous silicon.

Although decreased by hydrogen passivation, such a large deep defect density cannot be ignored in terms of transistor performance. A typical a-Si:H based transistor shows field effect mobility of 0.1 - 1 $cm^2/V \cdot s$, which is dramatically lower than the typical field effect mobility of a crystalline silicon based MOSFETs (~ $400\ cm^2/V \cdot s$) or even polysilicon thin film transistors (~ $200\ cm^2/V \cdot s$). Such low field effect mobility also stems from massive distribution of the band tail states; thus, resulting in frequent trapping of electrons and holes during transport, which leads to extremely low field effect mobility. However, even faced with such challenges, a-Si:H TFTs are a proven technology capable of driving liquid crystal displays and commercially dominate the current flat panel display market [27].

The chaotic alignment of a-Si:H's atomic structure also leads to current drain over time due to threshold voltage increase over time. Carriers propagating through the a-Si:H constantly experience trapping and

de-trapping, inducing more deep states in the a-Si:H channel, resulting in Fermi energy distortion (pushing away from the conduction edge) on the process [26]. This constant creation of states especially under device operation leads to a well-known bias stress induced threshold voltage shift that was first modeled by M. J. Powell [28]:

Equation 1

$$\Delta V_{Th.elec}(t) = A(V_{GS} - V_{Th0})^{\propto}(t)^{\beta}$$

where, V_{GS} is a gate bias, V_{Th0} is the threshold voltage before metastability shift, and A, $\propto$, and β are temperature dependent fitting parameters (obtained empirically) when the electrical stress was applied for a time t.

However, the threshold voltage shift due to electrical bias stress can be reversed by simply applying a reverse bias (again, electrical stress) [29]. Thus, inserting a reverse bias cycle when the TFTs are operating in a constant cycle is usually sufficient to avoid long term performance degradation especially in display applications. However, if the application does not require a constant cycle of operation and mandates a constant bias stress, such as logic circuits, the feasibility of a-Si:H transistors remains questionable.

2.1.2 TFT Structures

Thin film transistors can be manufactured in various configurations, which are determined by gate electrode and source-drain electrode arrangements. Generally, we assume four types of arrangements can be made as illustrated in Figure 10. Top gate structures can be found in Figure 10 (a) and (b) where the channel material is deposited prior to the gate dielectric, while the opposite deposition profile results in bottom gate structures as shown in Figure 10 (c) and (d).

On the other hand, gate electrode and source-drain electrodes are placed across the channel and dielectric layer, or staggered, as seen in Figure 10 (a) and (c). Such is a common structure for a-Si:H TFTs and nanocrystalline silicon TFTs because the channel layers provide additional space to decrease the electric field at the drain area, which prevents excessive off-state leakage. Furthermore, we can reduce process complexity with staggered structures because they only require two masks for TFT formation [30], while additional mask to open contact holes for source and drain electrodes are required for co-planar devices as depicted in Figure 10 (b) and (d).

In fact, a co-planar top gate structure is quite common in MOSFET and polycrystalline silicon TFTs because their contact layers can be prepared with ion implantation and the requirements of contact quality is higher than that of a-Si:H TFTs due to transconductance degradation issues. However, such processes require a post-annealing step to activate the dopants. This increases the production complexity even further beyond the additional contact hole mask. Therefore, to implement cost-effective large area applications, the staggered structure is preferred.

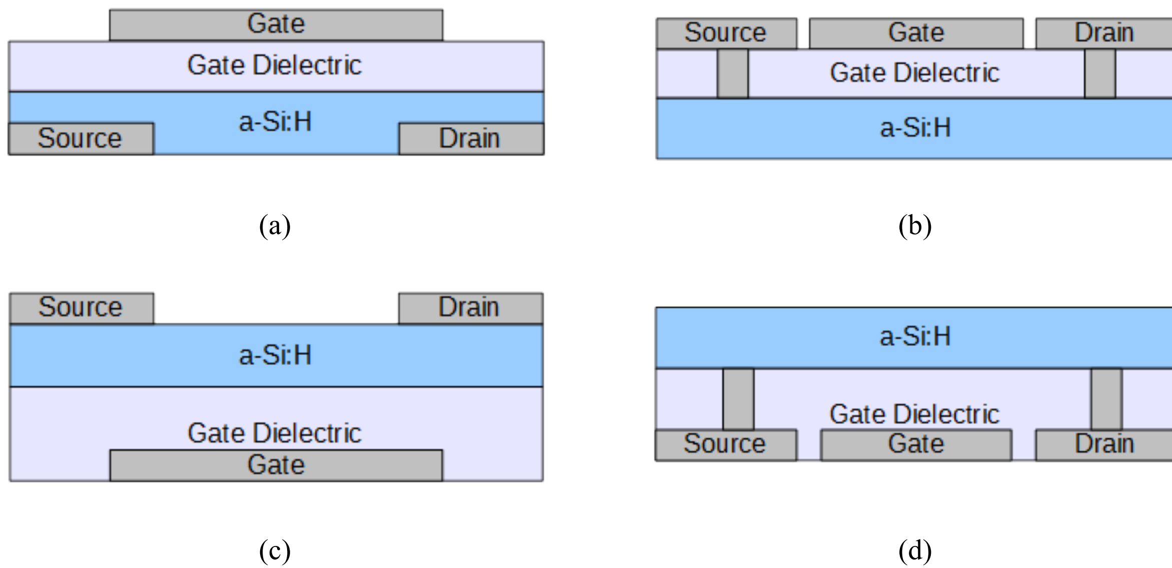


Figure 10 Four types of a-Si:H TFT structures.

In this work, we decided to implement our device readout of X-ray signals with a top-gate staggered structure (Figure 10 (a)) to reduce production complexity and subsequently cost. An inverted-staggered structure (or bottom gate staggered structure, Figure 10 (c)) was not selected because source and drain contact etch-selectivity is hard to control due to the contact layers being a-Si:H based materials. If the etch-selectivity problems are mitigated using a full wet etch process [31], the mask requirements and process complexity is still higher than that of a top-gate staggered TFT process. In contrast, a staggered-top gate structure can be fabricated with only two masks. It requires only one alignment step to finish the pixel and achieve a complete active-matrix TFT array, a remarkable achievement which simplifies the TFT fabrication process dramatically and improves reliability. Moreover, in contrast to a bottom gate

device, a top gate device is naturally suited to have a second gate on the bottom of the active semiconductor layer, a key requirement for operating the silicon X-ray sensitive layer which being the substrate, is naturally beneath the top gate TFT structure.

One drawback of the staggered-top gate structure is the crosstalk problem because the active layer (a-Si:H channel layer) spans through the entire array. However, we can avert this problem by allowing small gate overlaps for source and drain electrodes and etching the active layer and dielectric together, using the gate electrode as a mask. The process will be reviewed in detail in Chapter 3.

2.1.3 a-Si:H TFT Operation Physics

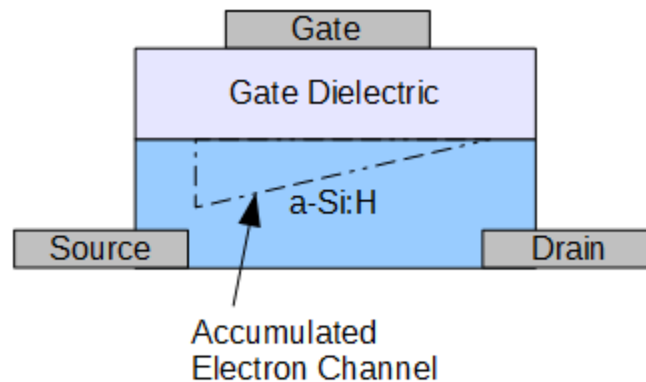


Figure 11 Illustration of top gate staggered thin film transistor.

In short, the a-Si:H TFT operation and current-voltage (I-V) relationship is very similar to MOSFET's. The major difference is that we consider the mobility edges, depicted in Figure 9, to be the conduction and valence band edges, and the extreme amount of defect density of states in these tail states leads to a device best suited for accumulation mode operation. Due to the extreme amount of trap states, the threshold voltage required to cause inversion is much higher than that of MOSFETs, and the hole mobility is 1/10 the level of electrons in a-Si:H [26]. Thus, even though inversion can be theoretically achieved with high threshold voltage, the performance of TFT cannot reach that of electron accumulation channel and the large gate voltages necessary can cause stress on the gate dielectric.

Figure 11 illustrates the operation schema of a top gate staggered a-Si:H TFT. Because an intrinsic a-Si:H is slightly N-type [26], we can consider the device as an accumulation mode N-type MOSFET. Thus, gate and drain bias can be applied positive while source remains at ground. The positive bias at the gate attracts free electrons in the a-Si:H to induce an electron channel at the interface between the a-Si:H and the gate dielectric (mostly a-SiNx:H). When the drain is also biased positively, the electron channel conducts in the way illustrated in Figure 12.

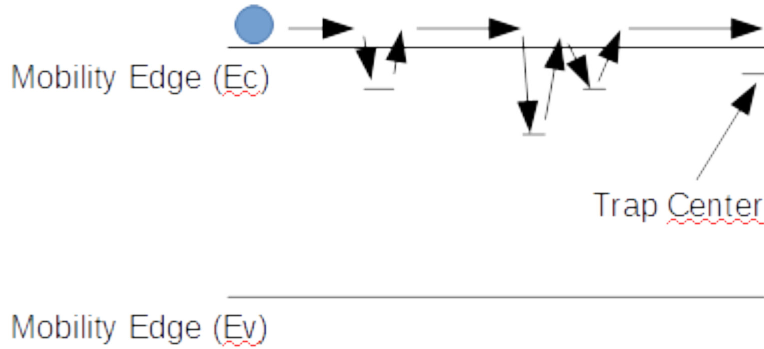


Figure 12 One-dimensional illustration of electron conduction in a-Si:H.

The accumulated electron channel conduction is limited by massive amounts of deep trap states and band tail states, resulting in lower effective mobility than crystalline silicon MOSFETs. Here, electrons will confront a chain of trapping and detrapping mechanics constantly which can be modelled thusly:

Equation 2

$$\mu_{FE} = \mu_0 \frac{\tau_{free}}{\tau_{free} + \tau_{trapped}}$$

μ_0 indicates the band mobility without trapping-detrapping mechanisms, τ_{free} and $\tau_{trapped}$ are the time intervals that electrons are free and trapped, respectively [26]. Because $\tau_{trapped}$ is longer than free time and if the trapped location is a band tail state, then they are called band tail electrons.

Figure 13 shows a typical transfer characteristic of an a-Si:H TFT. Three distinct operation regions can be distinguished: off-state, sub-threshold, and on-state. For small gate biases, the Fermi level lies in the deep defect states (refer to Figure 9) and the energy bands are close to the flat-band condition. As the gate bias increases (positive bias), band bending close to the gate dielectric interface occurs. In other words, the Fermi-level moves up through the deep defect states towards the band tail states [32, 33]. Thus, the threshold voltage of a-Si:H is a function of the density of deep defect states as derived in [24].

Equation 3

$$V_{Th} = qN_T t_S (E_F - E_i)/C_{gate}$$

where $E_F - E_i$ is the energy difference between the Fermi level and the intrinsic level at the threshold, N_T is the density of deep defect states, t_S and C_{gate} are the thicknesses of the channel layer and the gate capacitance per unit area, respectively. It should be noted that Equation 3 is derived with an assumption of uniformly distributed deep defect states in the energy gap.

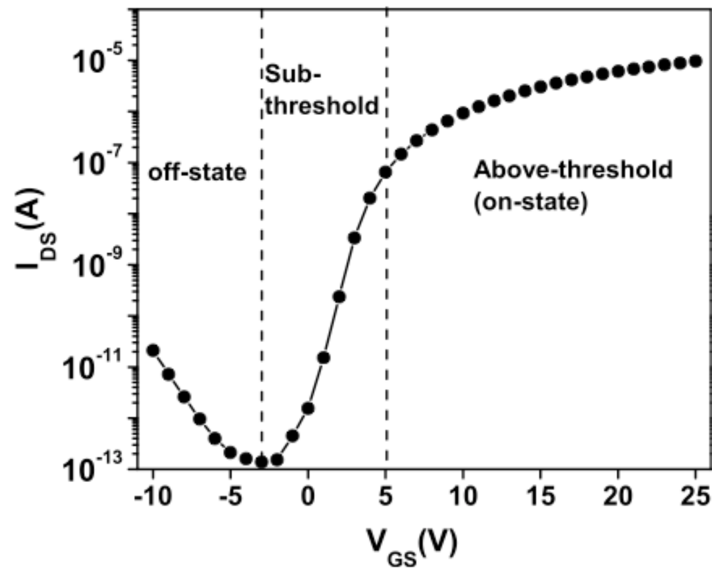


Figure 13 A typical I-V curve of an a-Si:H TFT.

When the gate bias (V_{GS}) exceeds the threshold voltage (V_{Th}), on-state, we can use FET equations to characterize the transfer characteristic. Thus, we can define linear and saturation with comparing $V_{GS} - V_{Th}$ and drain bias (V_{DS}.) Thus, if we take linear region, $V_{DS} \leq V_{GS} - V_{Th}$, the drain-source current (I_{DS}) can be described as [27]:

Equation 4

$$I_{DS} = \mu_{FE} C_{gate} \frac{W}{L}\left[(V_{GS} - V_{Th})V_{DS} - \frac{{V_{DS}}^2}{2}\right]$$

W and L are TFT gate width and length, respectively.

When $V_{DS} = V_{GS} - V_{Th}$, the accumulation channel is pinched off near the drain terminal as depicted in Figure 11 and drain current saturates to be independent of drain bias (V_{DS}). For, $V_{DS} > V_{GS} - V_{Th}$, the TFT enters saturation regime and the output characteristic can be given by:

Equation 5

$$I_{DS} = \mu_{FE} C_{gate} \frac{W}{2L} (V_{GS} - V_{Th})^2$$

Therefore, field effect mobility (μ_{FE}) and threshold voltage (V_{Th}) can be extracted from experimentally obtained I-V curves by using Equation 4 and Equation 5 depending on the regime of operation.

The off-state characteristic mainly depends on ohmic conductivity of the active layer [28] [33]. When negative gate bias is applied, the Fermi level is pushed down to the deep trap states, resulting in a depletion of the band tail states and the effective conductivity of the a-Si:H layer decreases.

However, Figure 13 depicts increasing drain current when the gate bias is negative. In other words, trap-assisted mechanisms may occur in the negatively biased a-Si:H region and intensify with increasing negative gate bias. Especially at the overlap region at the gate-drain electrodes, the gate bias and drain bias are applied additively leading to very high electric fields to encourage trapped electrons to travel by emission mechanisms, including Poole-Frenkel (thermionic emission) conduction [34, 35]:

Equation 6

$$I_{PF} = I_{PF0} e^{(\sqrt{E/E_0})}$$

where E/E_0 is the normalized electric field. Therefore, the Poole-Frenkel current (I_{PF}) increases exponentially with the electric field in the gate-drain overlap region at the reverse gate bias condition. The off-state current is a combination of drain-source ohmic current and the Poole-Frenkel current due to excessive negative gate bias. In other words, the off-current is affected by the gate-drain voltage difference, preventing additional leakage routes between the drain-source.

2.2 Direct Contact Detector

2.2.1 Operation Principle

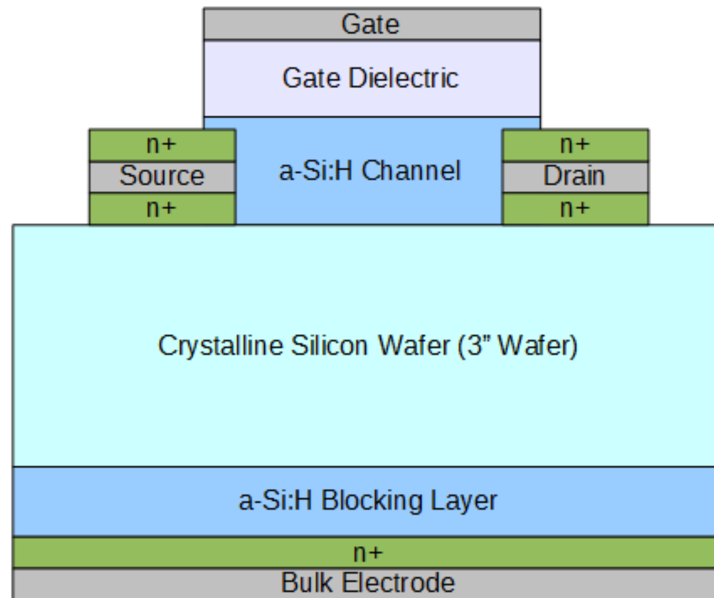


Figure 14 Schematic of a-Si:H-silicon direct contact detector.

The direct contact detector is a combination of an intrinsic crystalline silicon bulk photodiode and a staggered top gate a-Si:H TFT. As depicted in Figure 14, the a-Si:H TFT is deposited on top of a crystalline silicon substrate that forms part of the photodiode. The bottom side of the crystalline silicon substrate is passivated with an additional a-Si:H layer to reduce dark current and a doped diode contact called the bulk electrode.

The crystalline silicon layer provides a direct conversion X-ray to electron-hole pair converter that operates normally under reverse bias (i.e. when a positive voltage is applied to the bulk electrode). The a-Si:H blocking layer is deposited to reduce leakage currents when the silicon diode is placed under reverse bias. Indeed, the TFT side will be positively biased (i.e. the gate and drain electrodes) while the source electrode is tied with ground; thus, resulting in a back to back bias for the entire system. The n+ contacts at the TFT source and drain contacts provide additional depletion regions to temporarily store the photo-generated carriers. For our device with positive bias voltages on the gate, drain and bulk electrodes and the source electrode grounded, holes will reside at the potential minimum of the depletion well created as depicted in Figure 15.

The stored carriers, holes, provide an additional gate bias from the bottom side, which alters the channel conductivity at the a-Si:H and crystalline silicon bulk interface. Thus, the TFT transfer characteristic equation can be adapted to include this effect as follows:

Equation 7

$$I_{DS} = \mu_{FE} C_{gate} \frac{W}{L} \left[(V_{GS} + V_{IG} - V_{Th}) V_{DS} - \frac{{V_{DS}}^2}{2} \right]$$

where V_{IG} represents the induced gate bias resulting from the X-ray photon generated charge in the crystalline silicon substrate, also depicted in Figure 15 as the hole cloud.

Figure 15 Quasi-Fermi level distribution in the crystalline silicon substrate. The dotted line indicates a-Si:H TFT-crystalline silicon interface.

The induced gate bias can be estimated as the following:

Equation 8

$$V_{IG} = \frac{Q_{X-Ray}}{C_D}$$

where Q_{X-Ray} is the X-ray photon-generated charge stored at the potential minimum and C_D is the capacitance per unit area of the intrinsic silicon substrate induced by the TFT gate bias: $C_D = \epsilon_{si}/t_{si}$.

Thus, the thicker the substrate, the larger induced voltage because the capacitance is smaller. Therefore, we can predict the induced current by absorbed X-ray photons using the following equation:

Equation 9

$$\Delta I_{DS} = \mu_{EF} C_{gate} \frac{W}{L} V_{IG} V_{DS}$$

Initial work on this pixel architecture using a bipolar TFT device with $W/_L = {}^{1\,mm}/_{1\,mm}$ was first reported by Kai Wang and Karim S. Karim[36]. However, this device lacked n+ contacts to prevent off-state conduction at the top gate side and the direct contact for source and drain electrodes to the crystalline silicon bulk created an additional off-state current path through the silicon substrate, lowering the TFT's on/off current ratio dramatically. While functional at the pixel level, the high leakage makes the device unusable for a large area active matrix array application such as for protein crystallography. The performance of this direct contact detector will be elaborated on in a later chapter.

2.3 Silicon Dioxide Passivated Detector

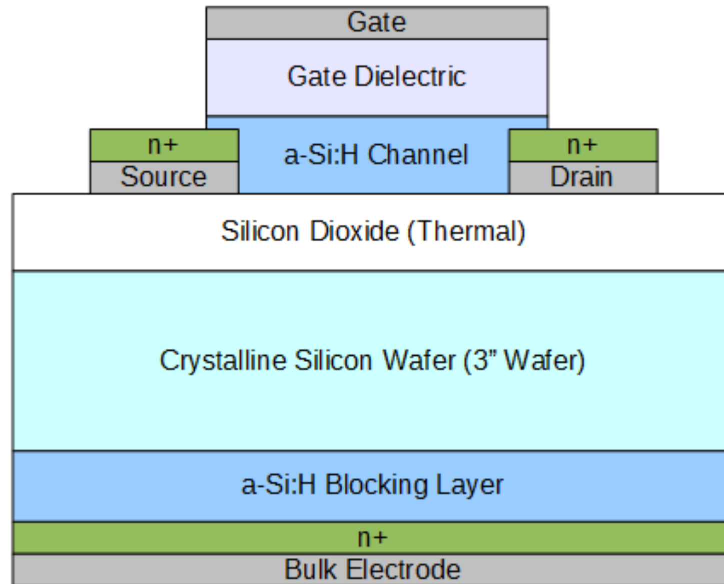


Figure 16 Revised hybrid detector with silicon dioxide blocking layer.

To prevent parasitic off-state current through the crystalline silicon bulk, a thermally grown silicon dioxide layer is implemented as a blocking layer and serve as the dielectric for secondary gate associated

with the X-ray photon-generated charge. The detector operation bias voltages stay similar to that of the direct contact detector. However, due to the passivation layer, the detector capacitance increases marginally. As seen in Figure 17, the energy increases throughout the crystalline silicon layer, resulting the X-ray generated holes concentrated at the silicon dioxide-crystalline silicon interface. Thus, the capacitance of a detector is simply determined by the silicon dioxide itself which is usually 1000 times thinner than the crystalline silicon detector itself. For in-house fabricated device, the silicon dioxide was 300-nm-thick, while the crystalline silicon was 380 µm-thick.

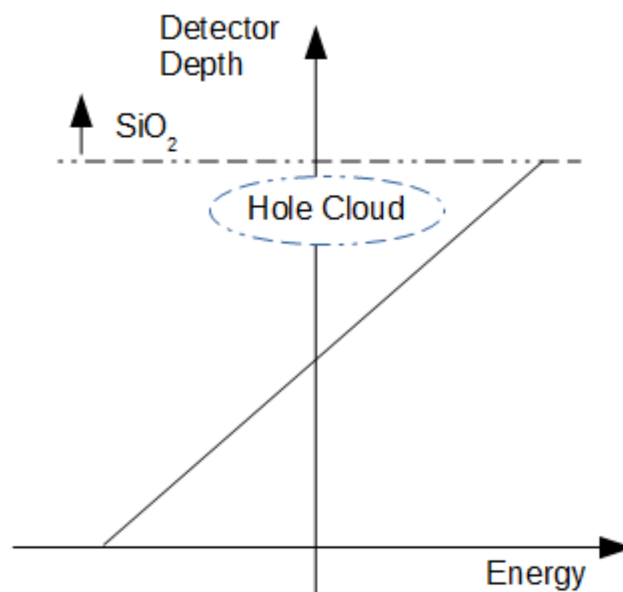
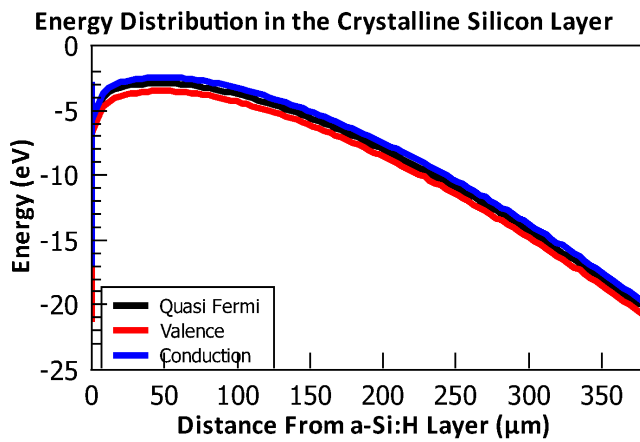


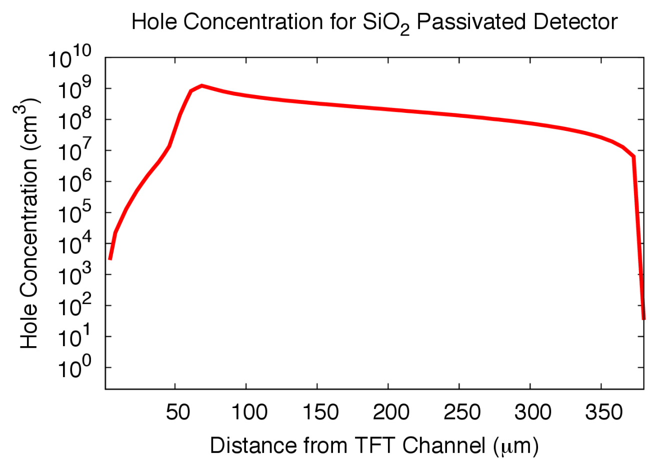
Figure 17 Quasi-Fermi level distribution in the silicon substrate.

Of course, the X-ray generated electrons will be extracted through the bulk diode contact since the electric field within the crystalline silicon detector is constant. Furthermore, the improved capacitance of the detector provides better in-pixel amplification since the larger capacitance provides more hole concentration in a given bulk diode bias voltage at the pixel area. In other words, the ‘virtual gate’ TFT in the silicon dioxide passivated detector has better performance than the direct contact detector. However, due to the cost to grow the silicon dioxide with thermal process, a slight increase in the price per unit area is inevitable. On the bright side, the silicon dioxide process is a common process in current industry standard. Thus, the increase in manufacture price will not affect as a critical factor for the overall unit price.

2.3.1 Energy Distribution Investigation with TCAD

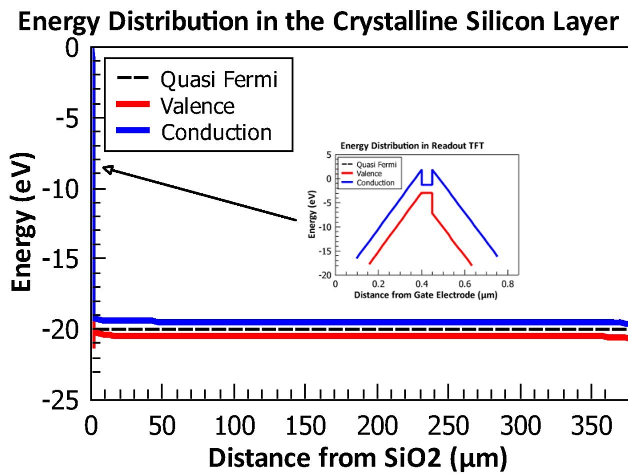


(a)

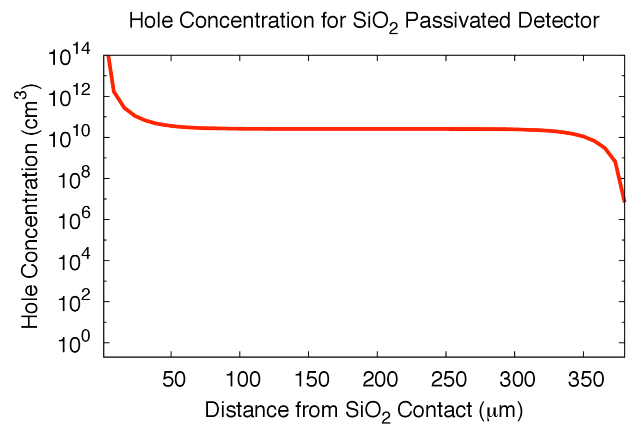


(b)

Figure 18 (a) Energy distribution in the direct contact detector (in the crystalline silicon substrate) and (b) hole concentration under back to back bias condition.



(a)



(b)

Figure 19 (a) Energy distribution in the silicon dioxide passivated detector (in the crystalline silicon substrate) and (b) hole concentration under back to back condition.

Energy distribution in the crystalline silicon detector under back-to-back bias was verified with a Synopsys MEDICI TCAD (Technology Computer Aided Design)[1] simulation tool. The simulation was performed to ensure the feasibility of operation principle which was discussed in previous chapter. As described in earlier sections, hole concentration in a direct contact detector is concentrated in the crystalline silicon bulk, away from the amorphous silicon TFT (Figure 18), while the majority of holes are concentrated in the vicinity of the silicon dioxide and crystalline silicon interface in the passivated detector (see Figure 19). Basically, Figure 18 and Figure 19 are transposed (rotated 90 degrees in counter-clockwise direction) versions of Figure 15 and Figure 17, respectively.

However, simulation results cannot be trusted entirely because trap distribution of a-Si:H and a-SiN_x:H layers was not accurately extracted from fabricated samples. In fact, the trap distribution used was that given in the simulator's default as provided by the MEDICI 2007 manual. These values are provided in the appendix section at the end of the thesis.

2.3.2 Readout and In-pixel Amplification

The pixel readout architecture is based on an active pixel sensor design, but it lacks a read transistor switch because the a-Si:H TFT itself is a switch and signal amplifier. Here, the switching function is controlled by the gate electrode bias while the X-ray photon-generated charge stored in the silicon substrate acts as additional gate bias resulting in an amplification effect in the transistor current. To the best of our knowledge, this is the first report of a single TFT active pixel sensor readout circuit as depicted in Figure 20.

The readout operation consists of three phases: reset, integration, and readout (as shown in Table 3). The reset phase is dedicated for clearing out accumulated photo-generated charges in the silicon substrate where a negative bias is applied to the bulk electrode while the source electrode remains at ground level. The photo-generated charge is evacuated through the forward biased P-N diode (V_{BLK}) and the charge stored in the column amplifier's capacitance, C_{read}, is neutralized by closing the reset switch without reading out any signal from the pixel TFT.

[1] TCAD is a computer aided design tool which simulates device characteristics and fabrication process.

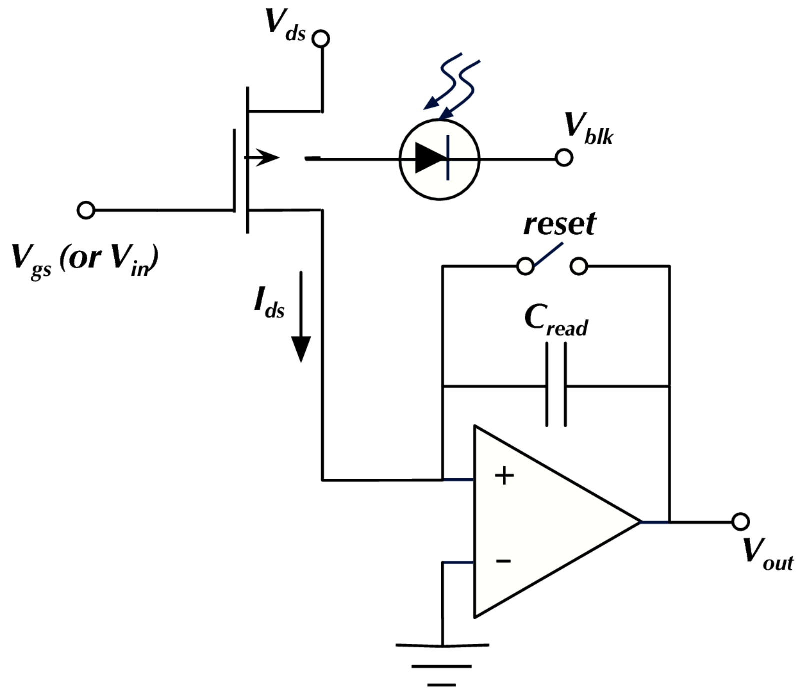


Figure 20 Expected implementation of the hybrid detector readout.

Table 3 Hybrid detector readout schema.

Signal	Reset Phase	Integration	Readout
V_{GS}	Low	Low	High
V_{DS}	Low	Low	High
V_{BLK}	Negative Bias	Positive Bias	Positive Bias

The integration phase is dedicated to accumulating and storing X-ray generated charge in the silicon detector capacitance. Thus, V_{BLK} must be such that the PN diode is under reverse bias and able to accumulate charge. The TFT's gate, drain and source electrodes are held at low potential to minimize metastability related changes.

In the Readout phase, both V_{GS} and V_{DS} are turned on and enable the TFT's I_{DS} to charge up the column amplifier's readout capacitance (C_{read}). Note that the I_{DS} is a function of both the applied gate bias V_{GS} and the X-ray generated charge on the TFT's second gate. The amplification (pixel charge gain, G_p) of the

single TFT active pixel can be described as a function of TFT transconductance (g_m) and the duration of Readout phase (T_s) [37]:

Equation 10

$$G_p = \frac{g_m T_s}{C_{Pix}}$$

The pixel capacitance can be determined as $C_{Pix} = WLC_D$. Thus, the readout gain is dependent on the TFT performance (g_m), the readout time (T_s) and, most importantly, the detector capacitance, C_{Pix}. Additionally, the TFT needs to be operated under linear bias to avoid detrimental effects from threshold voltage change and g_m dependence of the gate bias [38]. It is obvious that transconductance remains a constant when the transistor is operated in the linear region because the output current (I_{DS}) increase is proportional to the input voltage (V_{GS}). Any effects of inadvertent threshold voltage shifts are minimal because the channel is connecting a source to drain path.

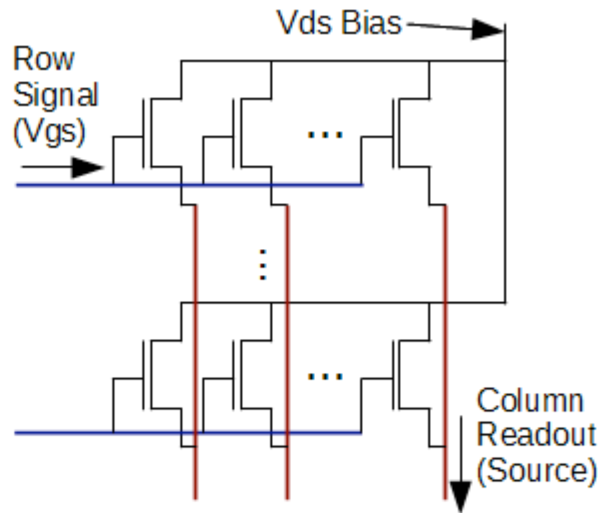


Figure 21 Array readout scheme of the 1T-APS pixel for the hybrid detector.

The detector can be laid out and operated as an active matrix array since only two ports are required for a pixel to operate. The drain electrode can be hooked at a common voltage source while gate bias was provided with a row and the readout at source electrode can be read out as a column. Only difference against a passive pixel sensor is the drain electrode which will be connected to a voltage source, instead of

a detector pixel capacitance. Of course, the bulk diode contact is provided by a single electrode which spans entire detector array at the other side of the wafer, isolated from the readout electronics. Figure 21 illustrates the active matrix array readout for the 1T-APS detector.

Chapter 3
Detector Fabrication

3.1 Overview

Both the direct contact and silicon dioxide passivated hybrid detectors were fabricated in-house using a process comprising only two lithography steps. The process is relatively simple and does not require a negative mask forvia openings as is typically used in TFT fabrication. The detector electrodes were deposited by a sputtering process using an Edwards sputtering system.The a-Si:H, hydrogenated amorphous silicon nitride (a-SiNx:H), and n+ doped a-Si:H films were deposited using a Plasma Enhanced Chemical Vapor Deposition (PECVD) process. These depositions were done using a PECVD cluster tool (multi-chamber system) developed by MVSystems Inc.(refer to Figure 22).

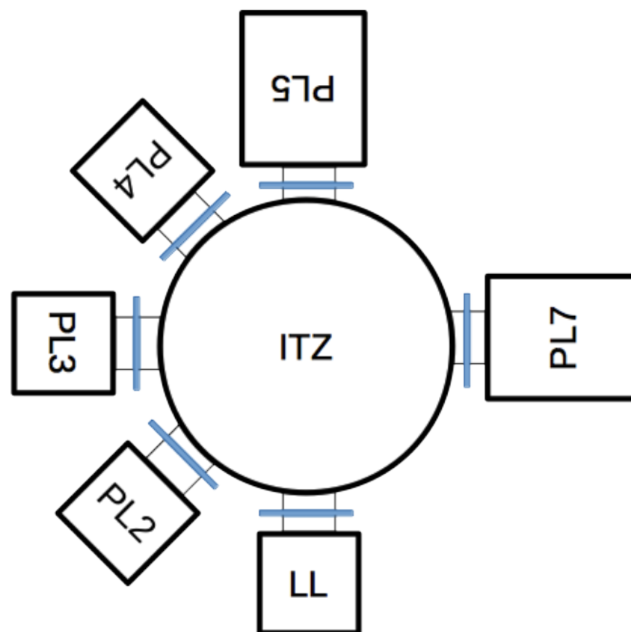


Figure 22 Schematic of the MVSystems multi-chamber PECVD system.

The multi-chamber system is advantageous in film quality and process control over single chamber systems, however their installation and maintenance budget requirements are much higher than simple systems. Because each chamber is dedicated to a certain type of film deposition, integrating different

process steps is easily accomplished with cluster tools. The in-house tool, depicted in Figure 22, has the chamber assignments shown in Table 4.

Table 4 Chamber assignment of in-house cluster PECVD facility.

LL	PL2	PL3	PL4	PL5	PL7	ITZ (Robot arm)
Load/Unload Substrates	Intrinsic silicon materials	Doped silicon materials	Gate dielectric materials	ITO, metal oxide deposition	Laser ablation	Junction for other chambers

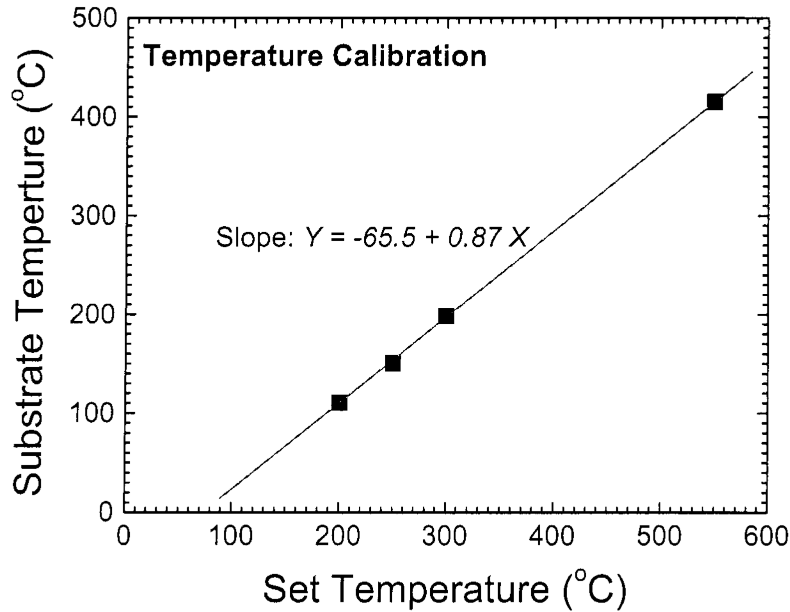


Figure 23 Temperature calibration data of the in-house cluster tool [39].

The substrates onto which the films are deposited are moved around by riding a robotic arm installed in the Interchamber Transfer Zone (ITZ). Therefore, direct contact with the heater element in each chamber is impossible. This leads to a difference between the heater element temperature setting at the control panel and the actual substrate temperature. A thermocouple is installed on top of each chamber for

detection of the chamber temperature. Figure 23 shows the thermal calibration data between the set temperature and the substrate temperature. The process temperature that appear in this thesis are the set values and can be converted to actual substrate temperature using the calibration curve in Figure 23.

3.2 Plasma Enhanced Chemical Vapor Deposition

Various plasma-assisted deposition methods, including radio frequency PECVD, direct current PECVD, very-high frequency PECVD (VHF-PECVD), and electron cyclotron resonance (ECR)-CVD, for silicon-based thin films have been reported since the 1960s [40-42]. Among them, the 13.56 MHz RF PECVD process has been the industrial standard for thin film transistor (a-Si:H and nc-Si:H) fabrication.

A typical RF-PECVD reactor comprises of two parallel electrodes in a vacuum chamber with gas inlet and outlet ports, each connected toa mass flow controller and pump. The electrodes are biased with an RF generator with a frequency of 13.56 MHz in most cases (as illustrated in Figure 24). Additionally, PECVD chambers are typically equipped with a heating element to heat up the chamber. The deposition takes place inside the chamber where the plasma is ignited between the two parallel plates.

In the plasma state, the mobility of electrons is much higher than positive ions due to the smaller mass of electrons (an electron's mass is 5 times that of a proton[42]). Because the electrical force applied to both carriers is the same, the difference in mass of particles results in a difference in mobility. Such large differences generate unbalanced sinusoidal waves, as shown in Figure 25. The excess electrons result in a DC component in the plasma current, which is blocked by the capacitor shown in Figure 24. The voltage bias that appears across the blocking capacitor is known as the self-bias voltage.

The space between the parallel electrodes consists of three major regions: the plasma itself (electrically neutral,) the RF electrode sheath, and the ground electrode sheath, as illustrated in Figure 26. Here, V_{dc}, V_s, and V_p represent the self-bias voltage, sheath potential, and plasma potential, respectively. The plasma potential is always positive and considered as a reference potential, while the potential at the powered electrode ends up as the self-bias voltage. The sheath potential is the potential difference between the plasma and the powered electrode ($V_p - V_{dc} = V_s$). Thus, ions tend to accelerate at the sheath region towards the electrodes, due to the high electric field at the sheath region, resulting in ion bombardment. Because the sheath region electric field (the slope of the potential distribution in Figure 26) is above the ground electrode, one can avoid ion bombardment by placing the substrate close to the ground electrode.

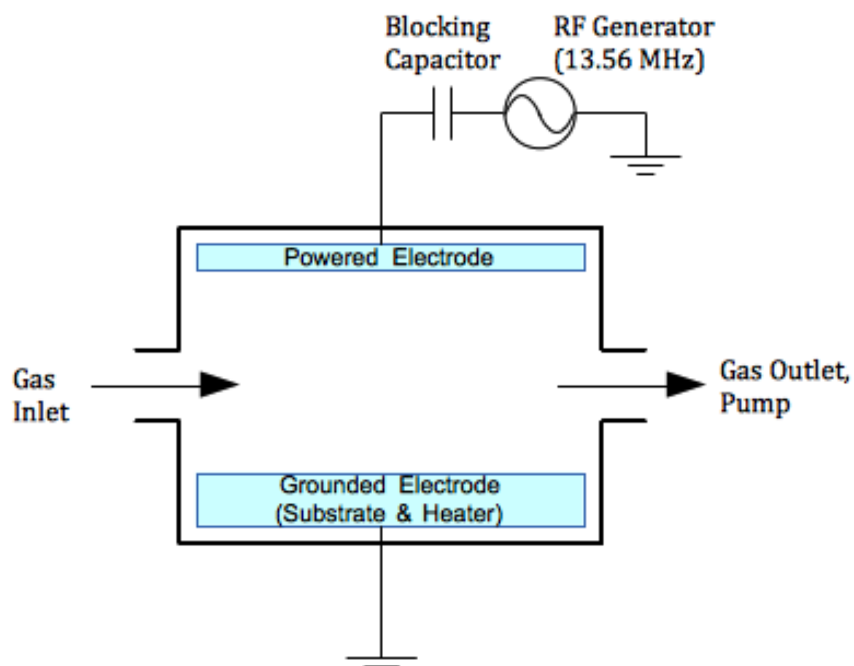


Figure 24 Schematic diagram of a typical RF-PECVD reactor.

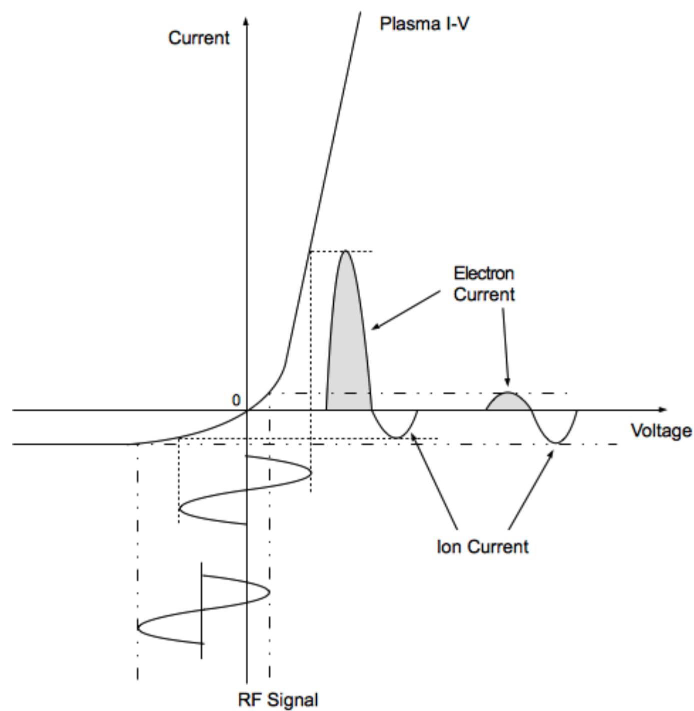


Figure 25 Static current-voltage (I-V) characteristics of a plasma (adopted from[40].)

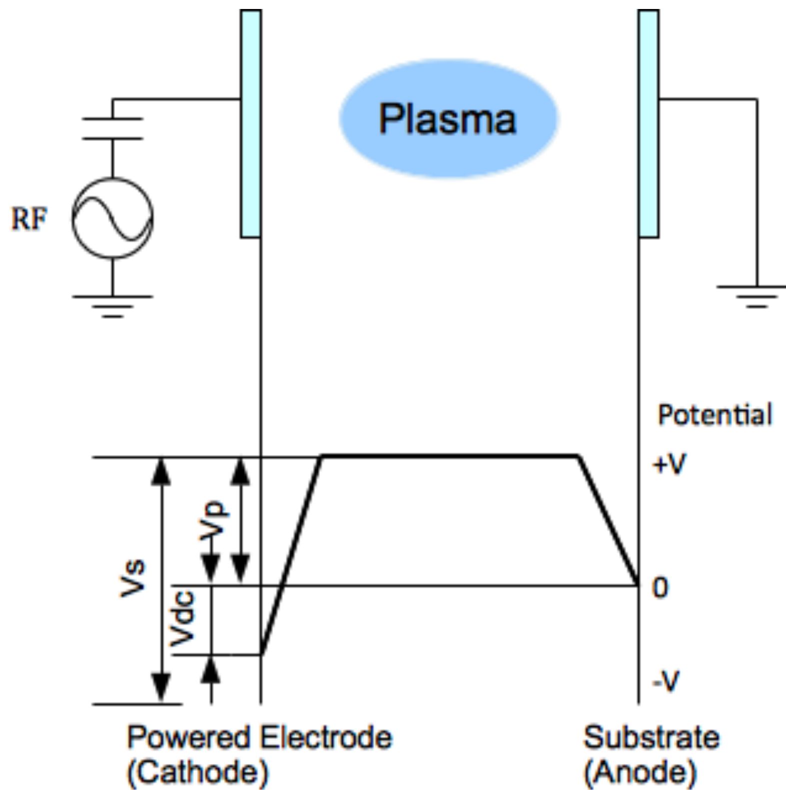
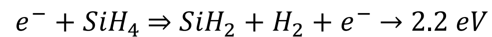


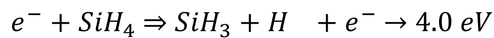
Figure 26 Time-average potential distribution in a plasma reactor (modified from [40, 42].)

The deposition process requires various gas precursors (such as SiH_4 for silicon based materials) to be physically disassembled by the electric bias of the RF plasma. The specific growth mechanism of any deposited film is very difficult to determine since the dominant reactions in a PECVD process can come from a large number of possibilities. For example, the plasma reactions for the SiH_4 precursor for a-Si:H deposition are [26]:

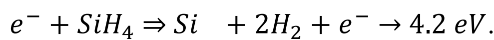
Equation 11



$$e^- + SiH_4 \Rightarrow SiH_2 + H_2 + e^- \rightarrow 2.2\ eV$$



$$e^- + SiH_4 \Rightarrow SiH_3 + H \quad + e^- \rightarrow 4.0\ eV$$



$$e^- + SiH_4 \Rightarrow Si \quad + 2H_2 + e^- \rightarrow 4.2\ eV.$$

The electrons on the left hand side in Equation 11 indicate the electrons generated between the RF biased parallel plates. The radicals and ions collide with each other, or the precursor itself (SiH_4), before reaching the substrate, causing additional reactions. Amongst various radicals, SiH_3 survives for the longest period and becomes a controlling factor in the a-Si:H deposition process. Meanwhile, they also combine themselves, resulting in the formation of large Si_nH_m molecules (or powders) in the reaction chamber, which can pull down the uniformity and mechanical integrity of the a-Si:H film.

Since the exact growth mechanisms for film growth are not known, the film growth parameters are described using the processing conditions, such as gas pressure, reactor temperature, dilution ratio, RF power density, and gas flow rate. The role of each deposition condition is summarized in Table 5.

Table 5 Effect of PECVD parameters.

Parameters	Effect in PECVD process
Pressure	Higher pressure ensures faster film growth speed. However, due to higher chance of collision of ions, powder generation also increases.
Gas flow rate	Provides more precursors in the reactor chamber in a given time. Thus, has a similar effect to the pressure. MFC (Mass Flow Controller) limited.
RF power	Increases the amount of plasma. Increases the deposition rate.
Temperature	Determines chemical reaction rate on the growth surface. Decreases growth rate a bit due to fewer dangling bonds as a result of high mobility of radicals. If SiH_4 was a precursor, hydrogen absorption rate increases.
Gas dilution	Lowers deposition rate and prevents serious powder generation when inert gas is used. Improves interface states (decreases the number of surface states) if the dilution gas was hydrogen.

3.3 Film Characterization

3.3.1 Gate Dielectric

Silicon nitride has been used as a gate dielectric for a-Si:H TFT since the emergence of the LCD industry [26, 43, 44]. The gate dielectric plays a key role in any field effect transistor performance because its main

role is blocking the attracted charges that remain accumulated at the gate-active layer interface, and securing a clear path form source to drain. In this section, the electrical properties of the PECVD hydrogenated amorphous silicon nitride (a-SiN_x:H) layer are presented.

Figure 27 shows the metal-insulator-semiconductor structure used to characterize the silicon nitride film. The substrate was selected based on the purpose of the measurement. For current-voltage (I-V) tests, p+ crystalline silicon (surface resistance < 0.001 Ω · cm) was used to ensure maximum conductivity, while a higher surface resistance (>0.01 Ω · cm) was used in capacitance-voltage (C-V) tests. The dopant type remained as p-type because the main active carrier for a-Si:H TFT is electrons. The top metal electrode was sputtered with a shadow masks as shown in the appendix.

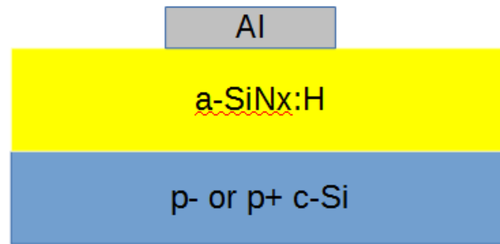


Figure 27 MIS a-SiN_x:H characterization sample cross-section.

The a-SiN_x:H was deposited in the PL4 chamber of the PECVD cluster tool. The chamber was pre-coated with 200 nm of a-Si:H to minimize contamination from silicon dioxide particles from other deposition processes. Table 6 shows the deposition conditions of the film with a gas flow to nitrogen dilution ratio of 1:20 (SiH_4:NH_3). The nitrogen dilution ratio has been shown to give a high quality film for a-Si:H TFTs, with high field effect mobility and low gate leakage current [45-48]. Also, nitrogen rich a-SiN_x:H films tend to sustain metastability effectively [49].

Table 6 Recipe table for a-SiNx:H gate dielectric, PL4.

SiH_4 (sccm[2])	NH_3 (sccm)	N_2 (sccm)	Pressure (mTorr)	Temp. (°C)	RF Power (W)	Growth Rate (nm/sec)
5	100	50	400	350	2	0.1

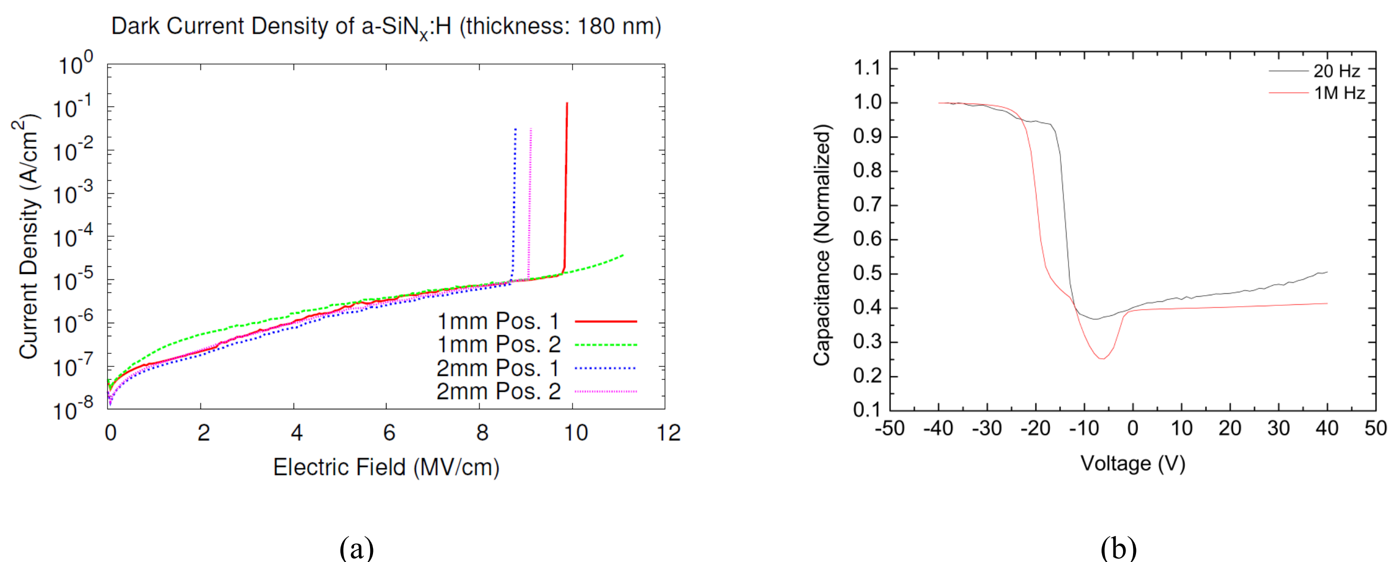


Figure 28 (a) I-V and (b) C-V characteristics of a-SiNx:H prepared by cluster tool PL4 chamber.

I-V characteristics were obtained with a Keithley 4200 system under dark conditions. The electric bias between the top electrode and the silicon bulk was applied via a sweeping profile from 0 to 200 V, and the result was normalized to the electric field, as depicted in Figure 28. The current increases through the continuous sweeping of voltage bias up to 8 MV/cm of electric field, where breakdown occurs and the current hits compliance value[3] of 1 mA.

The current-voltage characteristics (under dark conditions, Figure 28 (a)) provide a useful guide for TFT gate leakage estimation, at the current density around 2 MV/cm (36 V of gate bias for 180-nm-thick

[2] Square Cubic Centimeters per Minute. Unit of precursor gas flow for PECVD deposition.

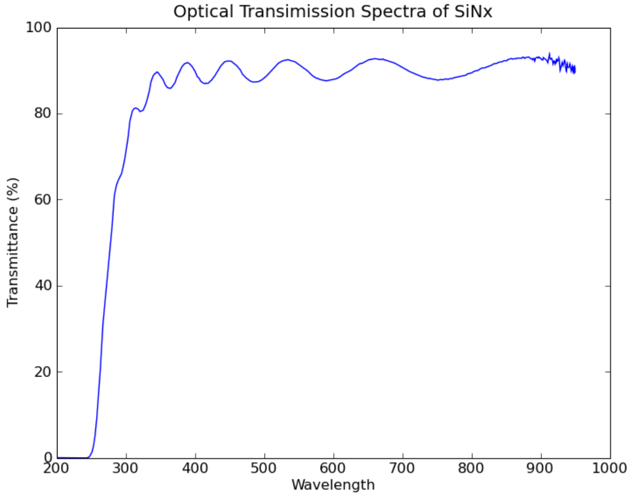
[3] In case of material breakdown, the characterization system contains a failsafe system which prevents excessive current flow. In this case, the breakdown at the thin film sample generates massive current flow through the entire characterization system since the breakdown spot is nothing but a short circuit (or 0 ohm of resistance.)

gate nitride).We can deduce the leakage current of 0.1 $\mu A/cm^2$, then the leakage current for a 1 mm by 1 mm of W/L ratio device will be in the 1 nA, which is close to the off-state current of such large TFT devices. If we take small devices (W/L ratio of 25 μm by 200 μm), the gate leakage becomes around 5 pA, which is also the off-state leakage current range. Thus, the nitrogen diluted silicon nitride is valid for hybrid detector application.

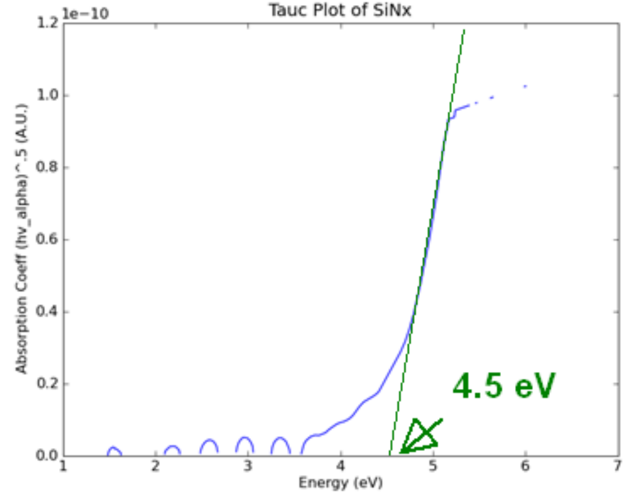
The capacitance-voltage relationship, obtained with Agilent 4284A (Figure 28 (b)), shows the silicon nitride gate dielectric is incapable of drawing the electrons to form the p-type crystalline silicon bulk. The low frequency (20 Hz) data indicates such behavior because the capacitance cannot reach the level of the negative bias condition, while high frequency (1 MHz) data shows normal behavior due to the inability of catching up fast switching bias [50].

The feasibility of silicon nitride gate dielectrics can also be characterized by extracting the optical bandgap via ultraviolet spectroscopy, or optical spectroscopy. The optical spectrum was obtained with a Shimadzu UV-2401PC ultraviolet spectrometer after deposition on a glass wafer. The a-SiNx:H film thickness was 980 nm, to provide as many peaks for transmittance (see Figure 29 (a)) as possible for curve fitting for the Tauc plot method [51, 52]. The curve fitting was performed with a Python language script and open source numerical analysis packages: NumPy, SciPy, and Matplotlib. The curve fitting resulted in 4.5 eV (see Figure 29 (b)) of optical bandgap for nitrogen diluted a-SiNx:H, which was a suitable level for a-SiNx:H films deposited via various methods [53-55]. The Python code can be found at the location below with the assistance of a Subversion version control system.

```
svn co http://taris-personal-docs.googlecode.com/svn/Research%20Documents/tauc/src/
```



(a)



(b)

Figure 29 (a) UV spectra and (b) bandgap estimation via Tauc plot method.

3.3.2 n+ Contact Layer

Contact layers at the source and drain electrodes play an important role in improving the TFT performance. Even though the a-Si:H channel shows optimal conduction characteristic for TFTs, the actual drain current can be suppressed due to parasitic resistance elements at the source and drain. The TFT ON resistance can be characterized as follows [56-58]:

Equation 12

$$R_{ON} = R_{Ch} + R_p$$

The channel resistance (R_{Ch}) can be derived as follows:

Equation 13

$$R_{Ch} = \frac{L}{W\mu_{FE}C_{gate}(V_{GS} - V_{Th})}$$

from Equation 7, by taking the Ohmic relation when $V_{GS} - V_{Th} \gg V_{DS}$. The channel resistance can be reduced by improving μ_{FE} by improving the a-Si:H or implementing nanocrystalline silicon, or even using metal oxide materials. However, excessively large parasitic resistance R_p cannot be ignored if the

contacts for source and drain electrodes are not ohmic. Thus, several deposition conditions for n+ a-Si:H contact layers were investigated as shown in Table 7.

Table 7 PECVD condition for three different contact layer samples.

SiH_4 (sccm)	PH_3 (sccm)	H_2 (sccm)	Power (W)	Temp. (^oC)	Growth Rate (nm/min)	Conductivity (S/cm)
20	20	0	2	350	10	0.01
20	20	150	2	350	2.5	0.0005
5	5	180	2	350	3	0.0003

The n+ a-Si:H samples were characterized by the lateral M-S-M structure shown in Figure 30. The wafer must be an insulator or have very high surface resistance (> 1000 Ω·cm) to prevent additional current paths between the electrodes. If any conductor was deposited prior to n+ a-Si:H (or any other contact layer candidates), then the resulting conductivity is much higher than the deposited film due to the additional path of current flow which was provided by the conductor. In short, the conductor acts as a smaller resistor, forming a parallel connection with the contact layer film (relatively higher resistance to the conductor.)

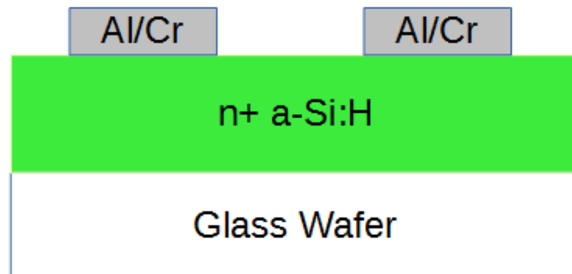


Figure 30 Lateral sample for contact layer conductivity extraction.

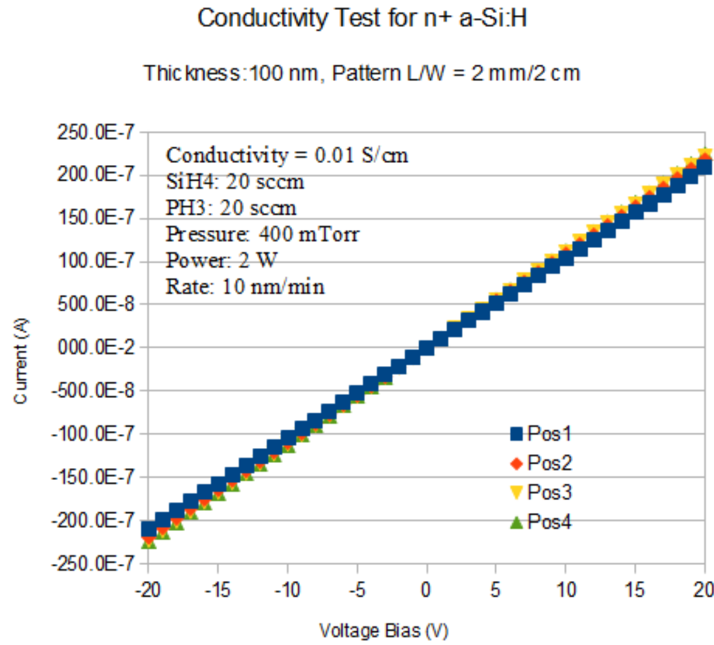


Figure 31 Ohmic contact of n+ a-Si:H contact layer deposited with 49.5 % of hydrogen dilution.

Figure 31 shows the ohmic contact for the given process conditions and conductivity ($\sigma_{contact}$) extracted from the definition of resistance:

Equation 14

$$\sigma_{contact} = \frac{L_R}{RW_R t_R}$$

L_R, W_R, and t_R are length, width, and thickness of the lateral resistance structure, respectively. The resistance can be extracted from inverse slope of the I-V curve, obtained by measurement (see Figure 31).

It is important to reduce the parasitic resistance, improve contact quality, and ensure ohmic contact for source and drain electrodes. Thus, a conductance investigation for different precursor mixtures was performed. Hydrogen dilutions of 49.5 %, 90 %, and 96.8 % were tested and a dilution of 49.5% was shown to give the best conductance as depicted in Figure 32. The conductivity of the n+ a-Si:H film was 0.01 S/cm at this condition. This lowest dilution film was selected as the best candidate for the hybrid detector implementation as this was sufficient to improve the a-Si:H TFT performance from parasitic

resistance [59]. Furthermore, higher dilution conditions could not easily be repeated due to sharing of the PL3 chamber with p+ type film depositions from various projects.

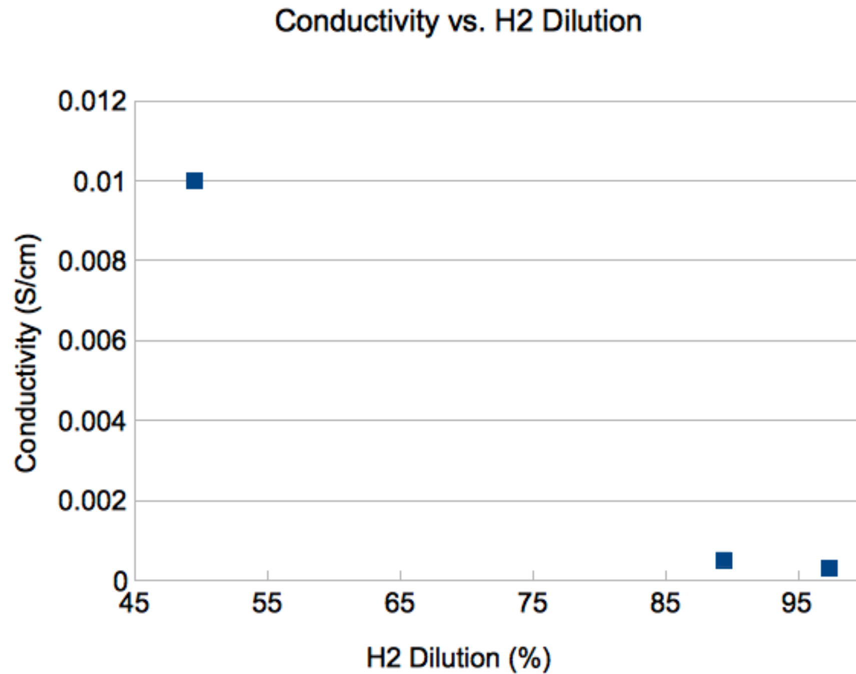


Figure 32 Conductivity comparison of various hydrogen dilution conditions.

The result seems controversial compared to previous results [60-62]. Also, we could not maintain the gas flow constantly for all deposition conditions (especially for 96.8 % sample) due to limitation of the mass flow controller installed at PL4. We believe this problem was induced by mixing of the deposition schedule with p+ films without proper cleaning of the dedicated chamber, which can be averted with a thicker a-Si:H pre-deposition than a 200-nm-thick recipe.

3.3.3 Thermal Oxide

The thermal oxide plays a key role in reducing the source-drain leakage of direct contact hybrid detectors. We procured wet thermal grown oxide with 300 nm thickness from a wafer supplier. The oxide leakage was tested with the MIS structure (see in Figure 27), where the silicon was a highly doped p-type crystalline wafer with a surface resistance of 0.001 $\Omega \cdot$ cm. The leakage results are shown in Figure 32.

The conductivity of the thermal silicon dioxide was 67.2 fS/cm which can be interpreted as $4.96\times10^{16}\ \Omega$ for W/L of 250 μm/25 μm TFT, which exceeds typical R_{Ch} of an a-Si:H TFT (~ 1 MΩ).

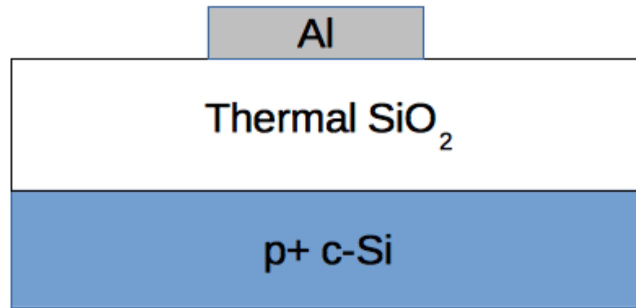


Figure 33 Passivation silicon dioxide I-V test set up. The MIS structure was biased with vertical electric field.

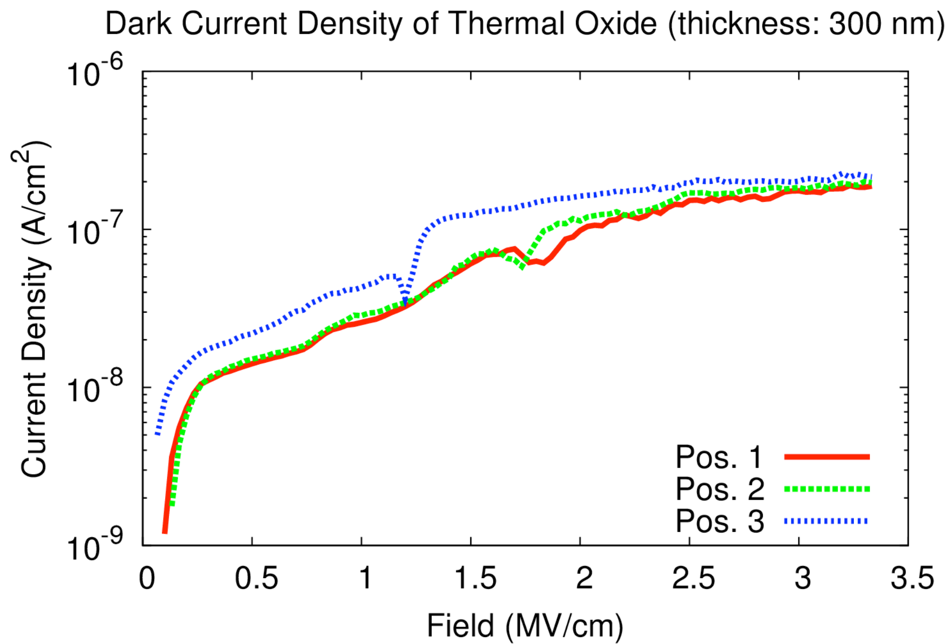


Figure 34 MIS test result of thermal silicon dioxide.

3.4 Direct Contact Detector Process

3.4.1 Mask 1

Figure 35 shows the material stack prior to the first lithography step.

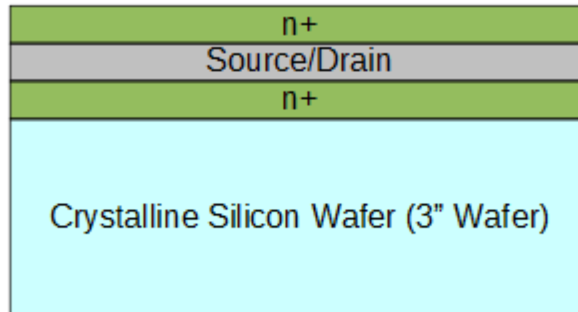


Figure 35 Contact layers deposited on top of an RCA1 and RCA2 cleaned silicon wafer.

A Float Zone technique fabricated silicon wafer (surface resistance higher than 10000 $\Omega \cdot cm$) was prepared with RCA1 and RCA2 cleaning processes to remove any residue. The wafer was then put into the PL3 chamber for n+ contact layer deposition, with the deposition condition shown Table 8 (dilution of 49.5%). The deposition thickness is 50 nm for any n+ contact layers in this work.

A 50-nm-thick chromium source/drain electrode was then deposited using an Edwards sputtering tool. The deposition conditions are shown in Table 8. The sputtering system holds three targets: aluminum, molybdenum, and chromium. Due to the nature of the sputtering operation, the three target materials show the same growth rate for the same deposition conditions. Therefore, deposition conditions for aluminum and molybdenum are the exact same as chromium in this work since only one sputtering tool was used for every metal electrode deposition. Due to the limitation of the machine, the only dominating factor for deposition rate manipulation was the RF Power which can only be manipulated with a digital controller. The chamber pressure had to be manually controlled using a valve handle and varies depending on the user. The argon flow rate was fixed due to the lack of a mass flow controller on this line.

After the source/drain electrode deposition, the wafer was sent into the PECVD chamber (PL3) again to deposit an additional n+ contact layer to form the final layer in the triple stack shown in Figure 35 The source-drain pattern mask (Mask 1) was used to pattern the source and drain as shown in Figure 36.

The reason for the n+ contact layer on top of the source and drain electrodes is to improve the TFT performance by lowering the parasitic resistance at the source and drain electrodes, which cannot be controlled in ambipolar devices. The fabricated triple stack was150-nm-thick: 50 nm of n+ layer, 50 nm of electrodes, and another 50-nm-thick n+ contact layer. At this point, the electrode is encapsulated by the contact layers and cannot be probed.

Table 8 Sputtering condition for Edwards sputtering system.

Ar (sccm)	RF Power (W)	Chamber Pressure (mTorr)	Temperature	Growth Rate (nm/min)
20	220	20	Room	10

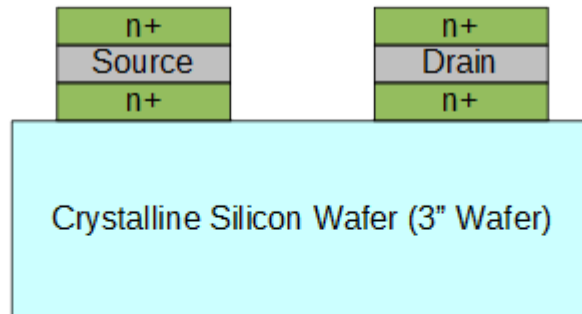


Figure 36 Patterned by mask 1 to form source and drain contacts.

The patterning was performed using a Karl-Suss MA6 mask aligner system and an AZ3312 positive photoresist from AZ Electronic Materials. The UV exposure conditions can be found in Table 9, and photoresist spin coating and curing conditions in Table 10.

Table 9 MA6 mask aligner UV exposure condition for AZ3312 photoresist.

Power (UV Bulb, Ch1)	Contact Type	Align Gap (µm)	Exposure Time (seconds)	Photomask Rack
900	Soft	20	3	4” mask

Table 10 AZ3312 spin coating and curing conditions for mask patterning.

Spin Speed (RPM)	Spin Time (seconds)	Thickness (nm)	Prebake Temperature (^oC)	Post-Bake Temperature (^oC)	Developing Time (seconds)
4000	60	1000	90	120	~ 25

The prebake was performed for 1 minute before exposing the photoresist to UV in the mask alignment system, and the post-bake was performed after developing the photoresist. The photoresist was developed for 25 seconds in an AZ300 MIF developer. The developing time was not fixed due to the nature of the wet chemical process and was determined by visual and microscopic inspection.

The n+ layers were dry etched before stripping photoresist with a Trion Minilock RIE system. The dry etching process used a sulfur hexafluoride (SF_6) and oxygen (O_2) plasma with a DC bias to ignite the plasma. The reactive ion etching (RIE) process is a standard process for etching thin film materials when fabricating TFTs and deep patterns for PECVD deposited a-Si:H films [63, 64]. The RIE conditions can be found in Table 11.

Table 11 RIE process condition for contact layers.

SF_6 (sccm)	O_2 (sccm)	Pressure (mTorr)	DC Bias (V)	Etch Rate (nm/min)	Temperature. (^oC)
45	5	50	-40	~ 6	Room

The chromium was etched using a wet etch process with a (6 wt%) nitric acid and ceric ammonium nitride (16%) solution, which provides an etch rate of ~ 5 nm/min at room temperature and ~ 25 nm/min

when the solution is heated to 70 ^oC on a hot plate. The photoresist is kept on the top n+ layer after RIE to provide additional shielding from the etchant for source and drain electrodes. Subsequently, the bottom n+ layer was dry etched using the same conditions given in Table 11. The photoresist was then stripped away to expose the n+ contact layer before bilayer deposition.

3.4.2 Mask 2

The exposed n+ layer was dipped for 3 to 5 seconds in a 1% buffered hydrogen fluoride solution to remove any oxide formation and protect the n+ layer surface from air [65]. Then the sample was quickly put into the intrinsic channel layer deposition chamber (PL2), followed by 50-nm-thick a-Si:H active layer deposition with the conditions given in Table 12.

The a-SiNx:H silicon nitride deposition was followed by an active layer process without breaking vacuum by transporting the wafer via the ITZ (see Figure 22). The PL4 chamber was coated with 200-nm-thick intrinsic silicon (a-Si:H) prior to sample insertion into the chamber to provide better electric quality of the a-SiNx:H film[66], followed by 300-nm-thick gate dielectric (a-SiNx:H) deposition (using the conditions in Table 4).Then, sputtering of a 150-nm-thick aluminum gate electrode was performed (see Figure 37).

Table 12 a-Si:H channel layer PECVD condition for PL2 chamber.

SiH_4 (sccm)	Pressure (mTorr)	Power (W)	Temperature (^oC)	Deposition Rate (nm/min)
20	400	2	350	10

The gate electrode and bi-layer (a-Si:H active layer and gate dielectric) were patterned using mask 2. The MA6 aligner and photoresist spin coating conditions are the same as in the previous section. The aluminum was etched with a PAN solution, which is a mixture of phosphoric acid (H_3PO_4), acetic acid (CH_3COOH), nitric acid (HNO_3), and de-ionized water (H_2O). The ratio was 16:2:1:1 H_3PO_4: H_2O: CH_3COOH: HNO_3, and its etch rate was around 5 nm per minute when the etch process occurred at room temperature. The etch rate could be speed up to around 80 nm per minute by heating up the PAN solution to 70 ^oC before the etch process. It is crucial to minimize the wet etch process as much as possible

because the etch solutions peel off the post-baked photoresist when the etch process is more than 10 minutes. The photoresist protection is crucial for the bi-layer etch process.

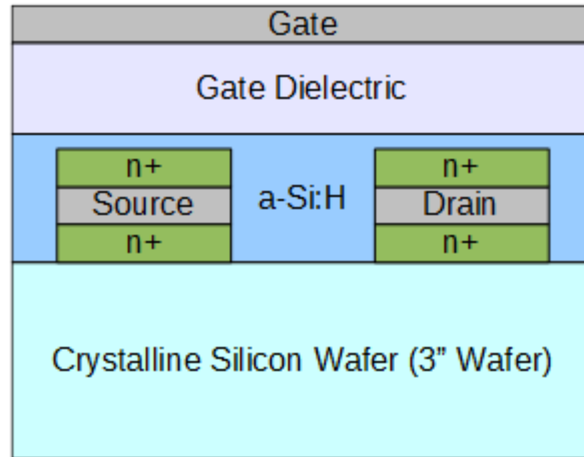


Figure 37 Bilayer deposition with sputtered gate electrode.

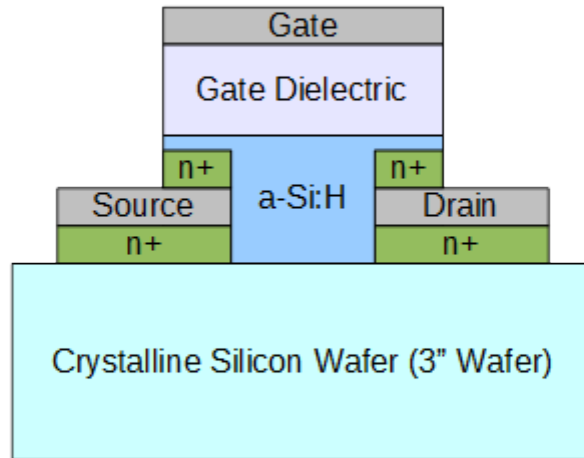


Figure 38 Patterned by mask 2, forming the gate electrode.

Table 13 RIE process condition for bi-layer etch.

SF_6 (sccm)	O_2 (sccm)	Pressure (mTorr)	DC Bias (V)	Etch Rate (nm/min)	Temperature. (^oC)
50	5	50	-80	~ 150	Room

Once the gate electrode was patterned with the PAN solution, the sample wafer was, again, sent intothe Trion Minilock RIE system for gate dielectric and channel layer patterning. During the RIE process, shown in Table 13, the gate electrode was protected by photoresist which was not necessary because the gate electrode was aluminum in this case. However, the photoresist protection could not be neglected when the gate electrode material was molybdenum [67]. Of course, the exposed portion of the n+ contact layer was bombarded by the RIE plasma and etched away to reveal the metal surface for source and drain electrodes, as shown in Figure 38.

Once the bi-layers were completely stripped off after 2 minutes of RIE process, the photoresist was stripped away with the AZ-KWIK solution to reveal the fully functional thin film transistor on the crystalline silicon surface, as depicted in Figure 39.

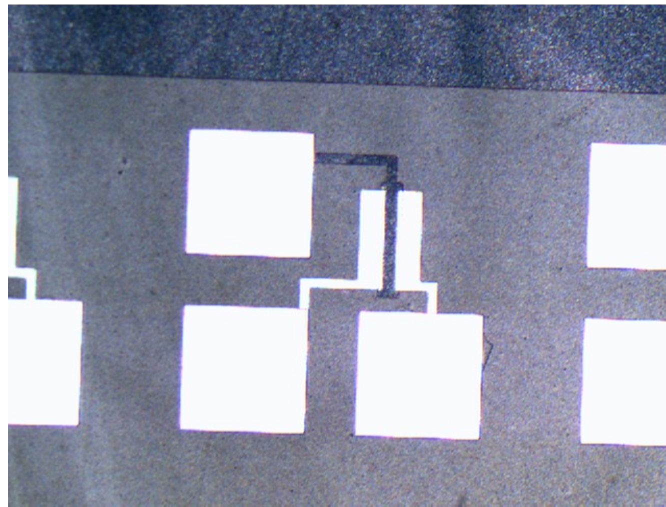


Figure 39 Microscope snapshot of in-house fabricated direct contact detector.

3.4.3 Bulk Electrode

Figure 40 shows the complete direct contact detector including the bulk electrode.

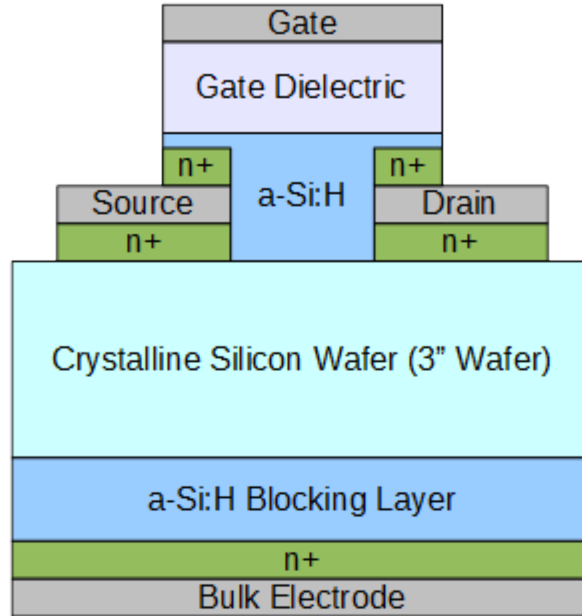


Figure 40 Completed hybrid detector device after bulk electrode deposition.

The bulk contact diode was deposited in the PL2 and PL3 chambers, followed by a 30-nm-thick aluminum bulk electrode sputtered using the Edwards sputtering sytem using the same process conditions as before. The top side, where the a-Si:H TFTs were patterned, was covered by an RCA1 cleaned Corning 1371 glass substrate during any depositions because their process condition was designed for low temperature (< 400 ^{o}C of substrate temperature) processes, while the glass substrate was capable of withstanding over 550 ^{o}C. The 500-nm-thick a-Si:H intrinsic layer was deposited to lower leakage current when the diode was reversely biased, and the n+ contact layer thickness remained the same as that of the source and drain electrodes.

3.5 Silicon Dioxide Passivated Detector Process

3.5.1 Thermal Oxide Etch

The silicon wafer was purchased with the silicon dioxide thermally grown. This processprocess grows silicon dioxide on any surface of the silicon wafers. The silicon dioxide on the back side of the wafer thus

had to be etched away to ensure a direct deposition of the diode contact and bulk electrode. The TFT side thermal oxide was protected with thick AZ3312 photoresist, spin coated using the conditions shown in Table 14. It took 7 minutes and 30 seconds to etch the 300-nm-thick thermal oxide with 10 % BHF solution. The resulting structure is shown in Figure 41.

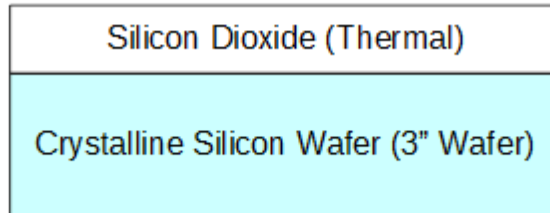


Figure 41 RCA1 cleaned and back side etched with AZ3312 photoresist protection at the top side.

Table 14 Spin coating condition for AZ3312 photoresist to withstand 10 % BHF solution.

Spin Speed (RPM)	Spin Time (seconds)	Thickness (nm)	Bake Temperature (°C)	Bake Time (seconds)
1000	60	> 2000	120	>180

3.5.2 Mask 1

Figure 42 shows the material stack prior to the first lithography step.

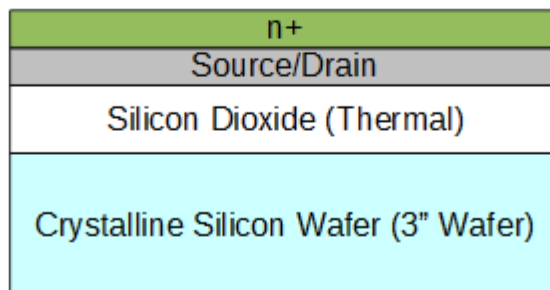


Figure 42 Source-drain contact layer deposition.

Once the bulk electrode side was opened, the process flow was similar to that of the direct contact detector. However, the source and drain electrodes can be deposited directly onto the thermal silicon dioxide because there is no need for another diode contact to the crystalline silicon substrate. 50-nm-thick chromium was sputtered directly onto the thermal oxide surface, followed by 50-nm-thick n+ contact layer with the deposition conditions given in Table 7.

The photoresist was spin coated and patterned following the conditions shown in Table 9 and Table 10, respectively. Figure 43 is a microscope photograph after post-baking the photoresist strip for 1 minute. The photoresist pattern can be easily distinguished by solid outlines because no layers are thicker than the photoresist (1000-nm-thick). The contact layer was dry etched and the metal electrodes were formed using the wet etch process described in the previous section, resulting in the structure shown in Figure 44. Figure 45 shows a microscopic photograph after photoresist stripping.

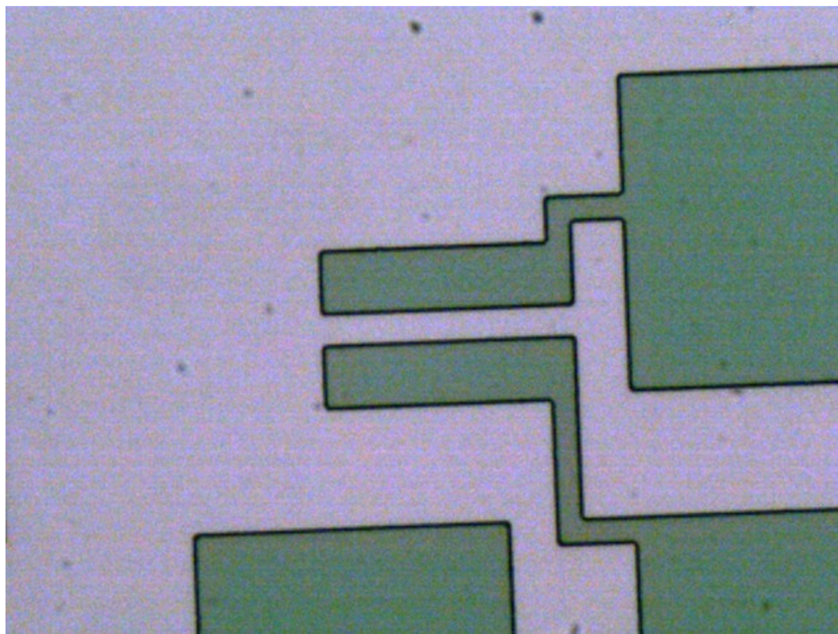


Figure 43 Photoresist developed on top of the source-drain films.

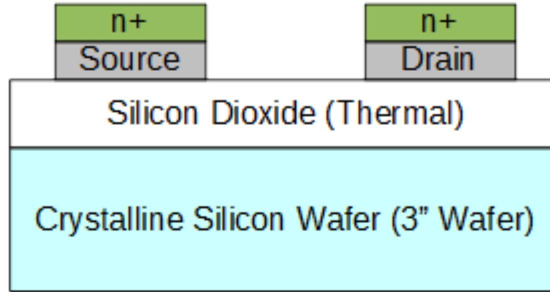


Figure 44 Patterned with source and drain pattern mask (mask 1.)

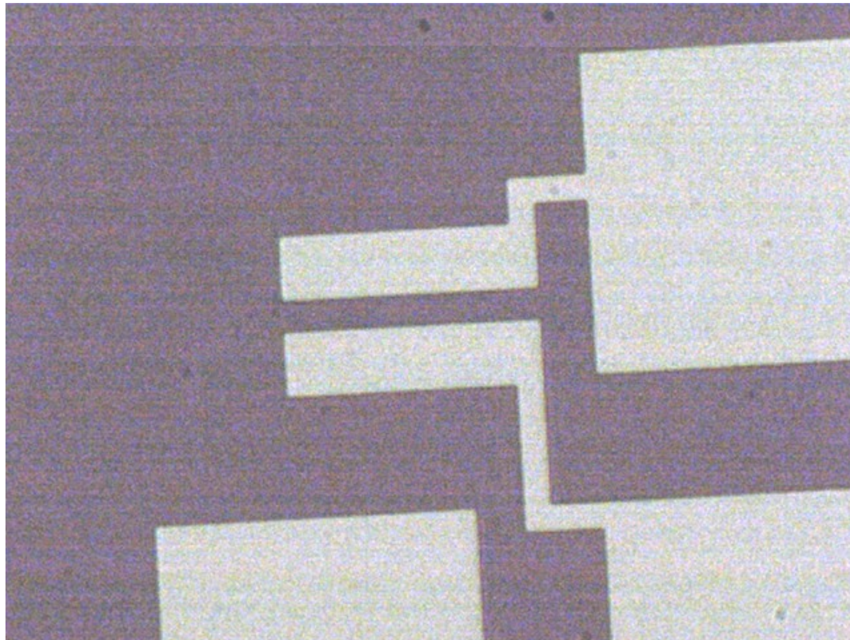


Figure 45 Wafer snapshot after photoresist strip.

3.5.3 Mask 2

Figure 46 shows the material stack of the silicon dioxide passivated detector prior to the bulk electrode deposition.

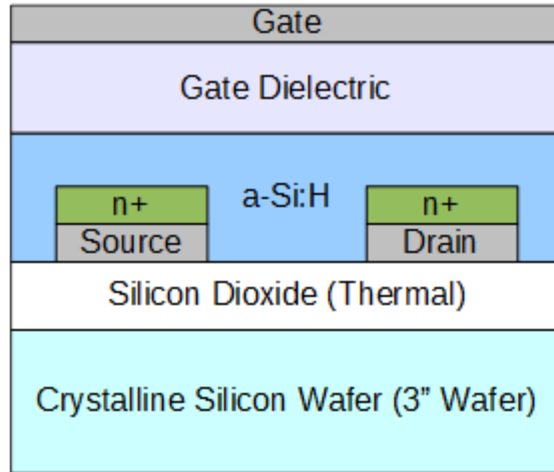


Figure 46 Bilayer and gate electrode deposition.

The exposed n+ source and drain layers were dipped into a 1 % BHF solution for 3 to 5 seconds before sending the wafer into the PL2 chamber for active layer deposition. It can be noted that such short time of 1 % BHF exposure had a minimal effect on the thermal oxide, as it requires more than 7 minutes to completely etch with 10 % BHF solution.

The bi-layer deposition was performed without breaking vacuum with PL2 and PL4, followed by a 150-nm-thick molybdenum gate electrode to improve yield. Because the wafer was supposed to undergo another PECVD deposition for the bulk contact side, the aluminum gate electrode punches through the gate dielectric and ends up with a short circuit to the source or drain electrodes. Thus, replacing the electrode with a metal with a much higher melting point (the melting point of molybdenum is 2200 ^{o}C) than aluminum (660 ^{o}C) prevented such a shortfall in the process.

Figure 47 shows the mask 2 photoresist after developing photoresist, before undergoing the PAN etch for molybdenum gate, which took only a few seconds when the PAN solution was heated to 70 ^{o}C. A RIE process with higher DC bias (see Table 13) was performed for 120 seconds to pattern the a-SiNx:H gate dielectric and a-Si:H active layers, as depicted in Figure 48. The photoresist was stripped away with the AZ-KWIK solution to expose the gate electrode (see Figure 49).

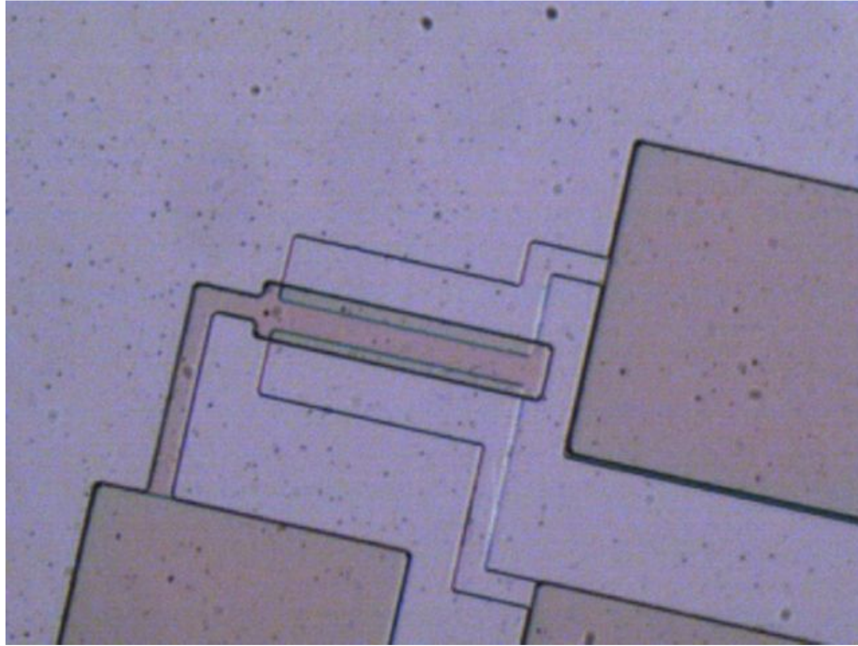


Figure 47 Wafer snapshot of photoresist pattern for mask 2, before etch process.

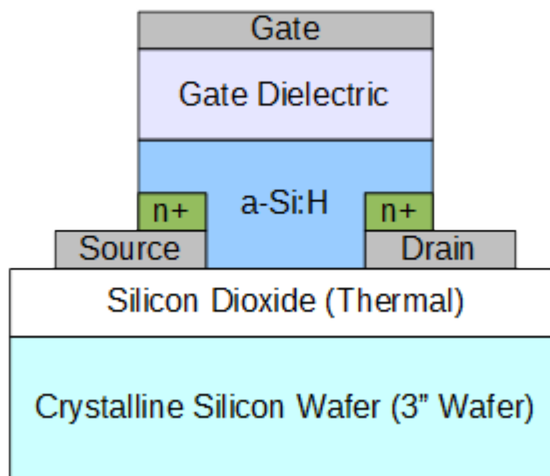


Figure 48 Finished TFT on thermal oxide after Mask 2 etch.

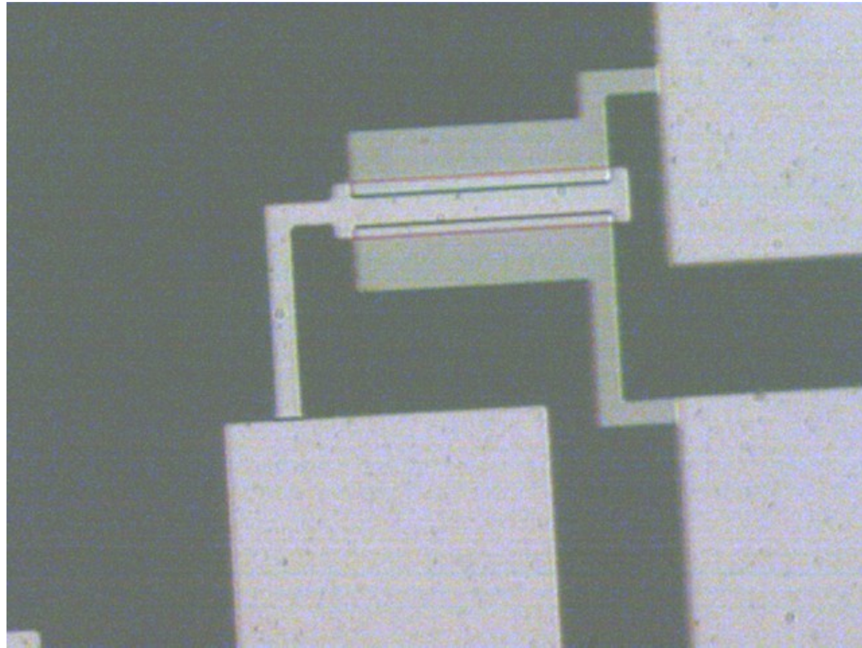


Figure 49 PR stripped after mask 2 etch processes.

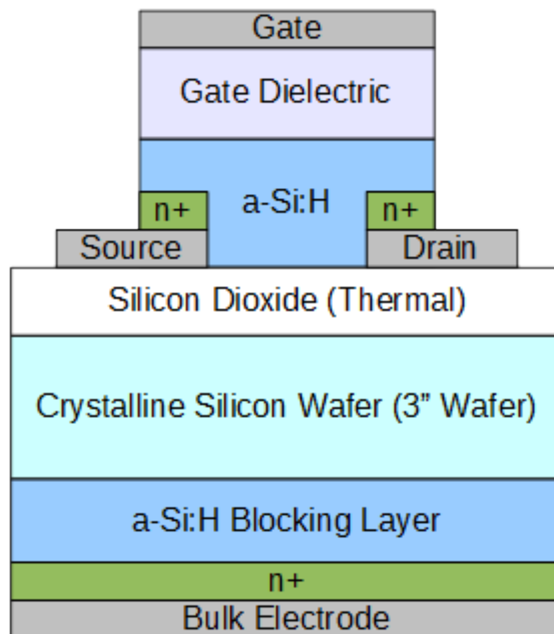


Figure 50 Bulk electrode deposition: finished device.

Lastly, the wafer was flipped to deposit the bulk electrode structure as shown in Figure 50. Again, the intrinsic a-Si:H was 500-nm-thick and the n+ layer was 50-nm-thick, while the bulk electrode was deposited at less than 30 nm of thickness by controlling the sputtering time to less than 3 minutes.
A photograph of the final wafer after bulk electrode deposition is shown in Figure 51.

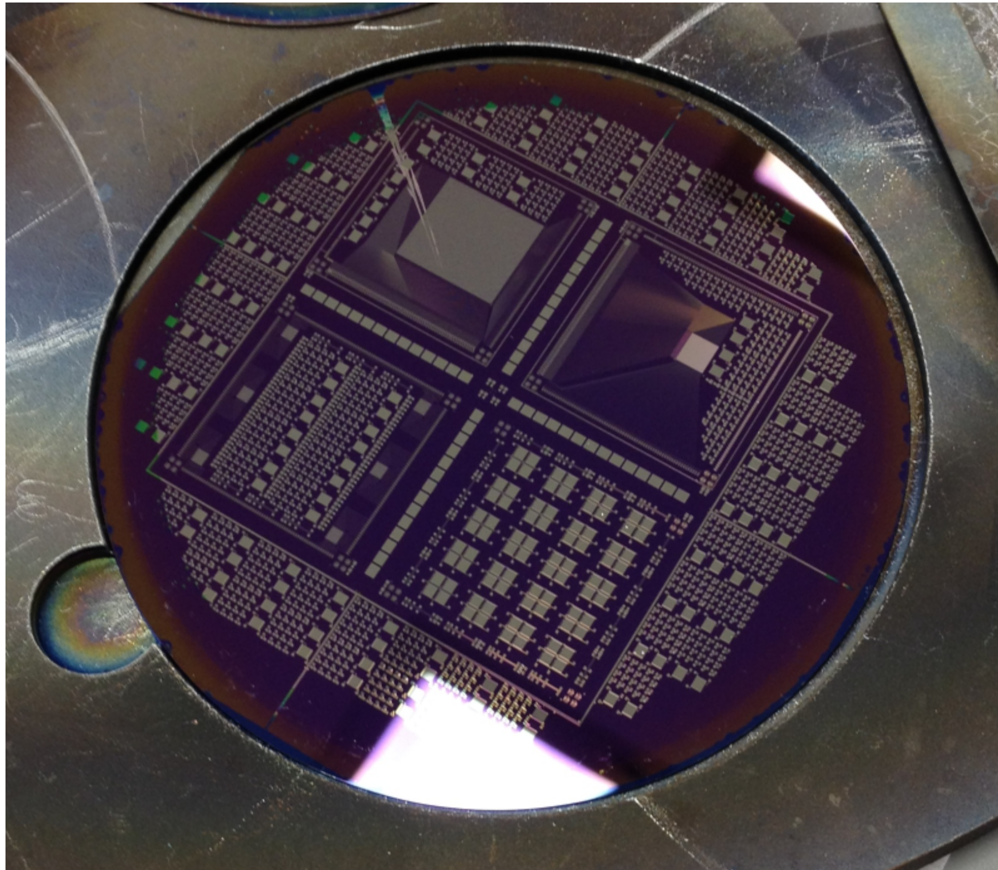


Figure 51Thermal oxide passivated detector after bulk electrode deposition.

Chapter 4
Detector Performance

4.1 TFT Performance

4.1.1 Transfer and Output Characteristics

Electrical characteristics of a TFT device can be investigated via transfer and output curves. The transfer curve shows the on and off ratio, which defines its switching capability and provides information on field effect mobility (μ_{FE}) by fitting the slope of transfer curve (see Equation 15), while threshold voltage can be obtained from the intersection of the fitted curve at the gate bias (V_{GS}) axis. On the other hand, the slope of transfer curve ($\frac{dI_{DS}}{dV_{GS}}$) indicates the transconductance (g_m) of the TFT device, which plays a critical role in in-pixel amplification, as noted in the section 2.3.2.

Equation 15

$$\frac{dI_{DS}}{dV_{GS}} = g_m = \mu_{FE} C_{gate} \frac{W}{L} V_{DS}$$

$$\mu_{FE} = \frac{L \cdot g_m}{C_{gate}\, W \cdot V_{DS}}$$

The transfer curve was obtained using an Agilent 4156C semiconductor characterization system via Signatone Series 720 probe manipulators. As expected, the direct contact detector shows very high off-state current compared to the passivated detector, as seen in Figure 52 and Figure 54. The on/off ratio of the direct contact detector is merely three orders of magnitude at drain bias of 1 V, which ensures linear region operation, and four orders of magnitude at 10 V of drain bias, where the TFT is under the transition from the linear to saturation regions. On the other hand, the passivated detector shows at least five orders of magnitude in on/off ratio of all drain bias conditions (1 – 30 V), which demonstrates effective switching.

The comparison between direct and passivated detectors indicates that such huge leakage in the direct contact detector stems from the crystalline silicon bulk. This occurs because the direct detector allows an ohmic contact path to the silicon bulk from the source and drain electrodes i.e. the buried n+ layer under the source and drain electrodes. Since the conductivity of crystalline silicon is higher than a-Si:H, higher off-current leakage can solely be activated by the drain bias itself. As seen in Figure 52, the off current

increases marginally by increasing the drain bias and reaching almost one order of magnitude of on/off ratio at the drain bias of 30 V.

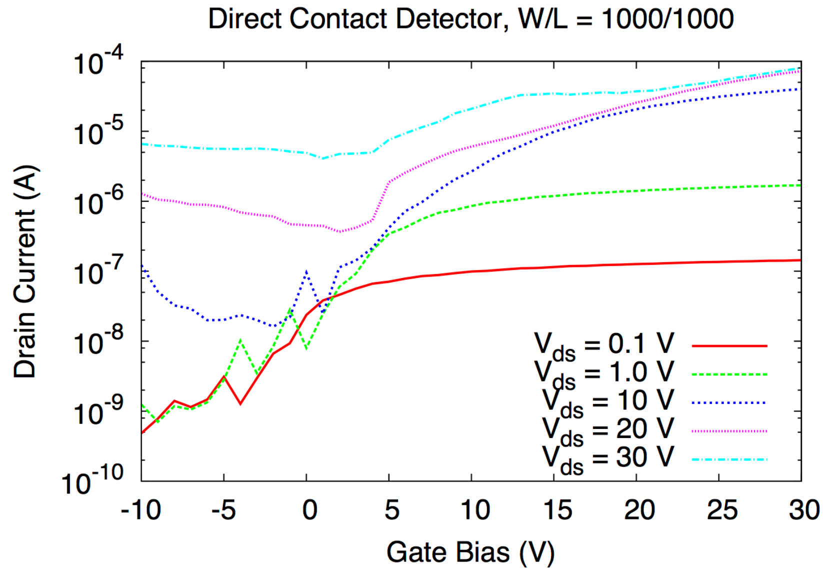


Figure 52 Transfer characteristics of direct contact detector.

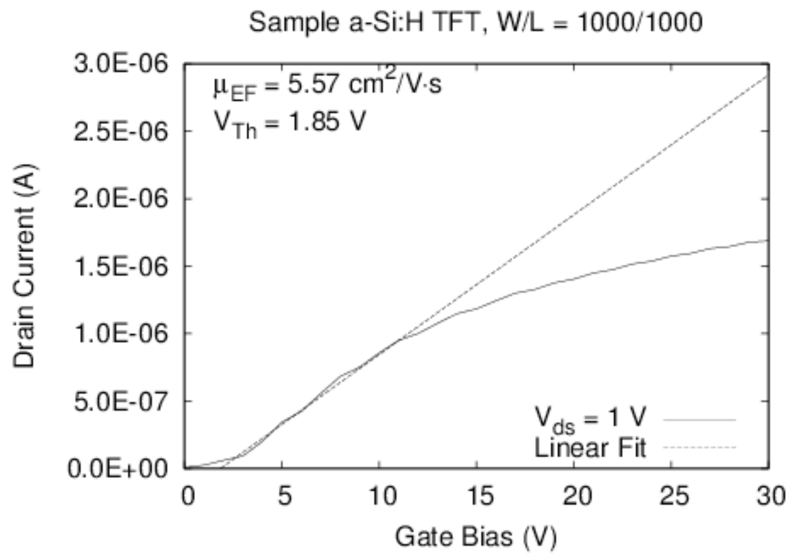


Figure 53 Field effect mobility and threshold voltage extraction of direct contact detector.

Meanwhile, field effect mobility and threshold voltage extraction indicate that the direct contact detector has better field effect mobility due to the additional crystalline silicon pathway, as seen in Figure 53 and Figure 55—where the square root fitting method was applied with Equation 15 under 1 V of drain bias to ensure linear mode of operation. The direct contact detector shows higher field effect mobility and much less threshold voltage due to the current assistance from the crystalline silicon bulk.

However, higher mobility from crystalline silicon bulk leads to a transconductance degradation in contrast to the passivated counterpart. As seen in Figure 53, the slope of transfer curve, i.e. the transconductance, degrades at 10 V of gate bias, while the passivated detector realizes the same detrimental effect at 20 V of gate bias. As noted in the previous chapter, due to the voltage divider formed by the R_p-R_{Ch}-R_p series network, the actual drain bias portion that affects the channel operation decreases when the channel resistance (R_{Ch}) decreases.

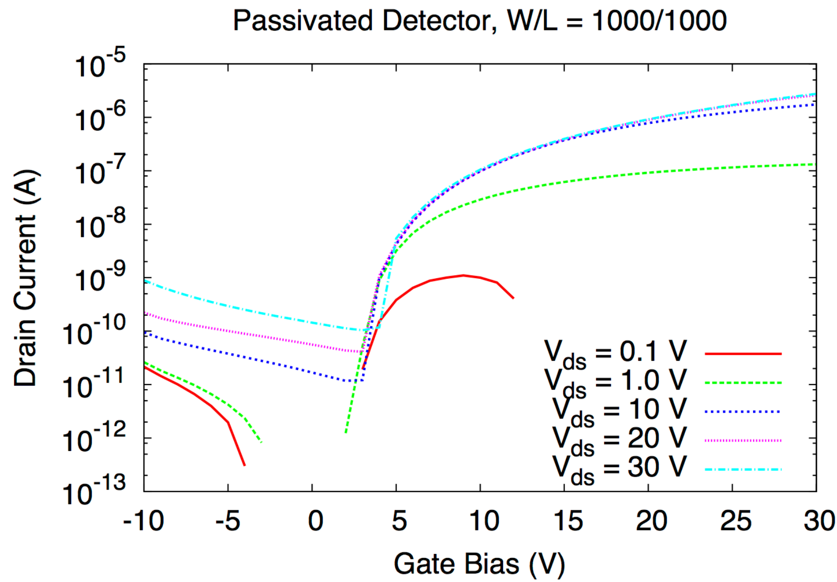


Figure 54 Transfer characteristics of passivated detector.

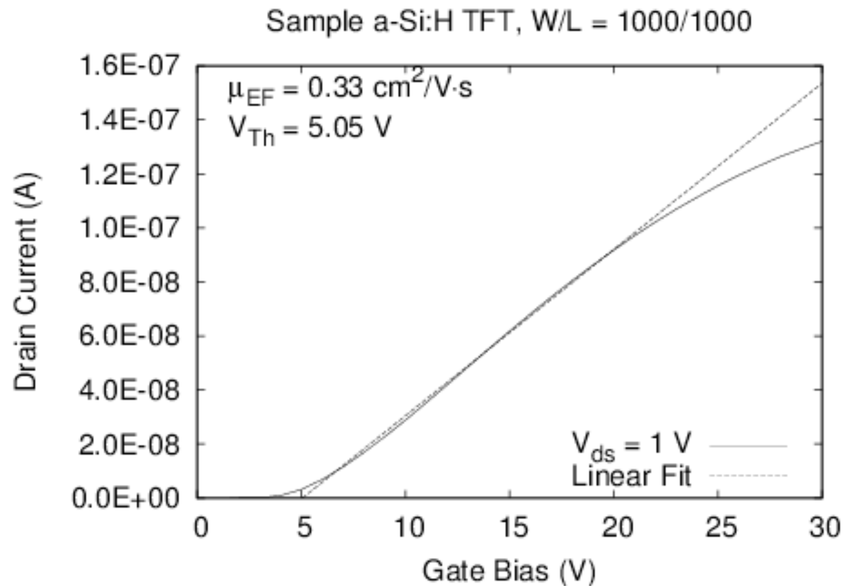


Figure 55 Field effect mobility and threshold voltage extraction of passivated detector.

The detrimental effect from direct contact of the crystalline silicon bulk can also be seen in the output characteristics in Figure 56, where the drain current increases linearly at high drain bias (> 20 V) regardless of gate bias conditions. Such behavior is also seen in MOSFETs as the Kink effect, or floating body effect, which stems from additional charges accumulated in the silicon bulk. It can be averted with silicon insulator technology [68]. In a sense, TFT is an ideal SOI device due to the huge aspect ratio of the channel layer (in this case, it is 1 mm/50 nm) if it were deposited onto an insulator substrate, such as silicon dioxide. However, our direct contact detector also suffers from such a floating body effect due to the crystalline silicon substrate.

In addition, we can confirm that the direct contact TFT is also suffering from a current crowding effect due to the lower channel resistance compared to its passivated counterpart. Figure 56 reveals that the drain current at low drain bias (< 10 V) does not increase linearly, while the passivated detector (Figure 57) shows a linear increase at the same bias condition. The current crowding takes place when the contact resistance plays a critical role against channel resistance in the series network depicted earlier [69]. Although the staggered structure incorporates the channel resistance itself in the parasitic resistance [70], we can decrease the parasitic resistance with increasing conductance of source and drain contact layers. However, in the direct contact detector's case, the Kink effect already deteriorates the on/off ratio by increasing the off-state current.

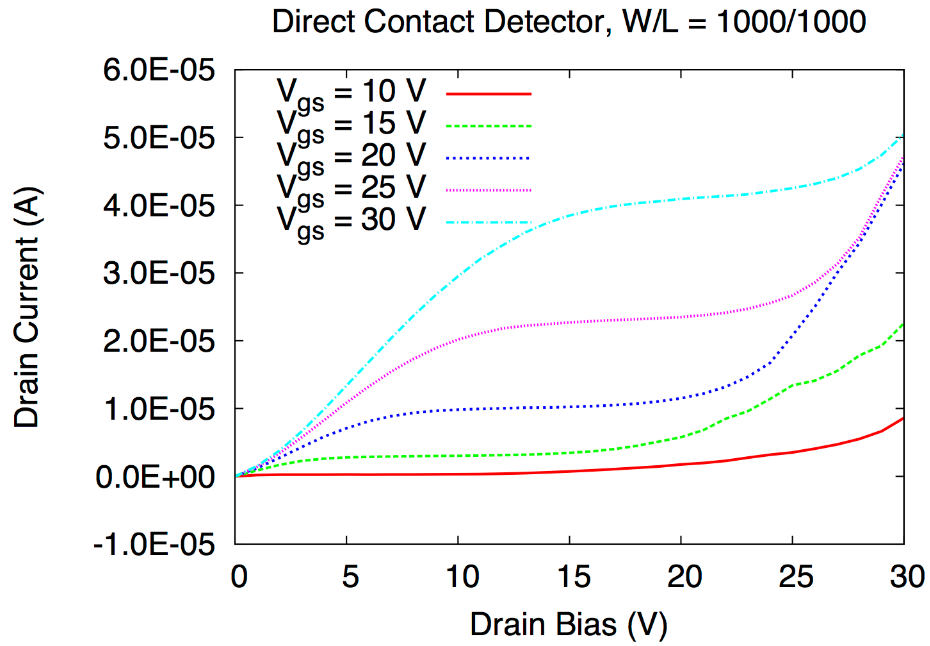


Figure 56 Output characteristics of direct contact detector.

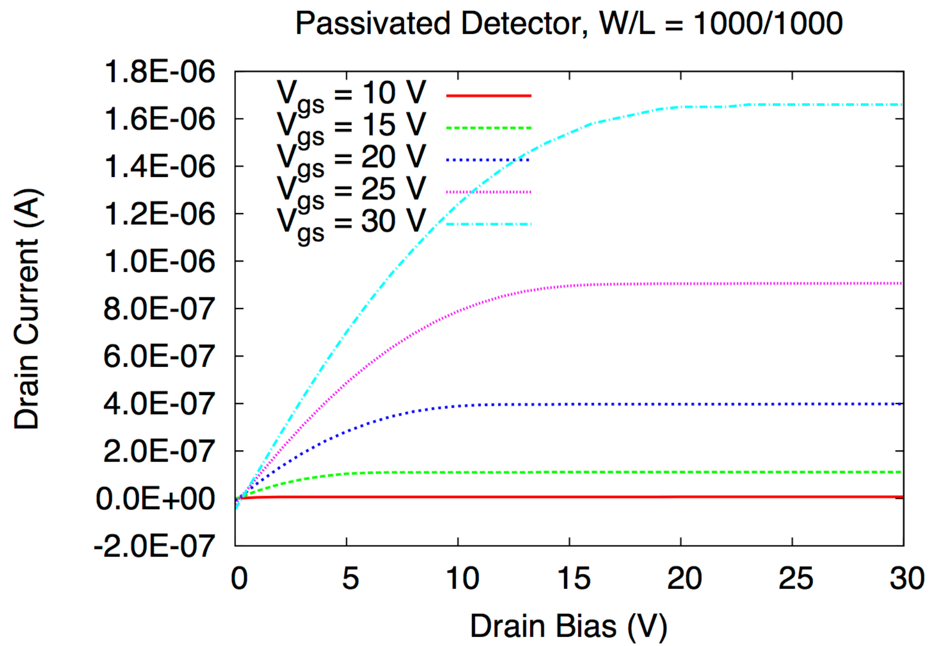


Figure 57 Output characteristics of passivated detector.

4.1.2 Metastability

It is well known that a-Si:H TFTs are prone to threshold voltage shifts due to the metastability of a-Si:H and bias conditions [71]. Therefore, we can assume that the a-Si:H-to-crystalline silicon contact has minimum effects on TFT metastability. However, we were able to confirm that the low threshold voltage observed on a direct contact detector shifted rapidly in response to a prolonged gate bias, as depicted in Figure 58. The detector was stressed with 30 V of gate bias and 10 V of drain bias to ensure maximum on/off current ratio. This resulted in a massive threshold voltage shift, from 3.55 V to 5.92 V. Although the threshold voltage shift can be reversed quickly (less than 1 minute) with the same amount of negative bias (-30 V of gate-source bias), we can confirm that requiring higher bias condition for operation plays a detrimental role in threshold voltage characteristics.

On the other hand, the low bias condition, gate bias of 20 V and drain bias of 1 V, lowers the threshold voltage shift down to a 0.8 V range, as seen in Figure 59, while recovering the threshold voltage with the same amount of negative bias requires the same amount of time. Thus, we can conclude that the TFT device needs to be operated under linear regime and needs to be biased larger than negative 30 V to minimize the recovery duty cycle during readout operation.

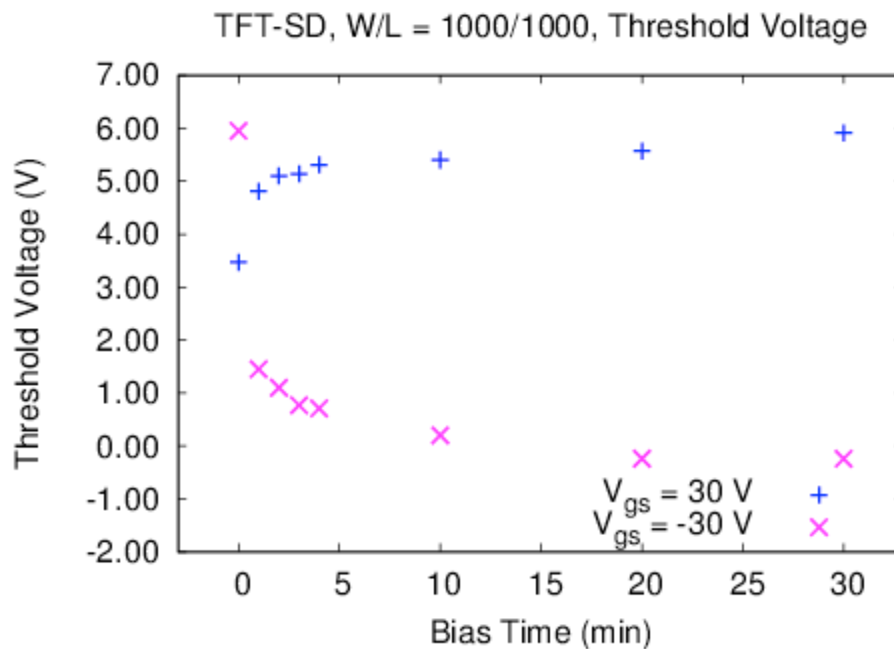


Figure 58 Threshold voltage shift of direct contact detector with 10 V of drain bias.

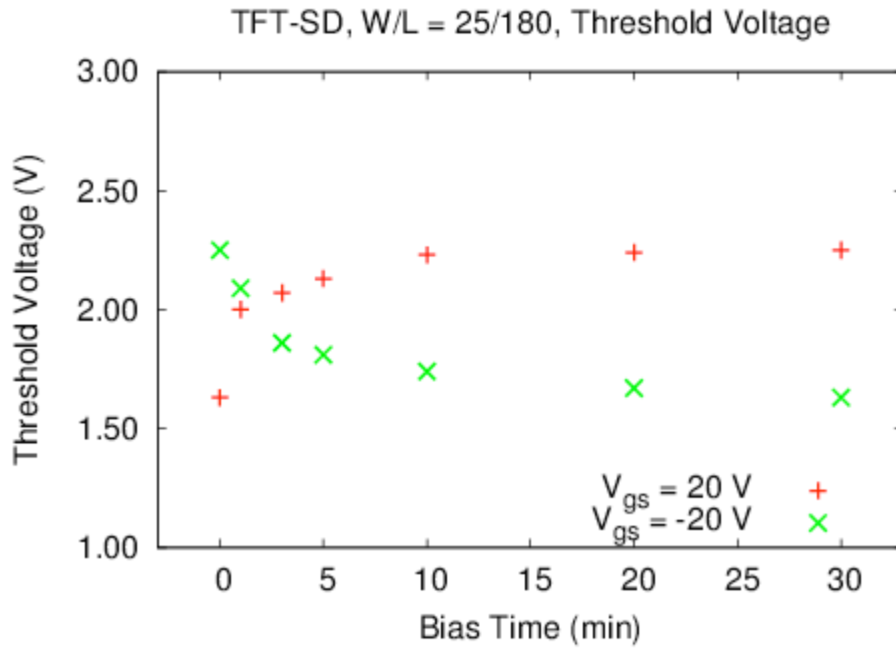


Figure 59 Threshold voltage shift of passivated detector, obtained with 1 V of drain bias.

4.1.3 Time Domain Analysis

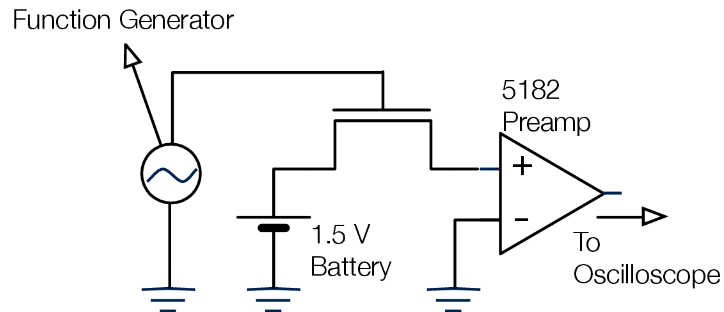
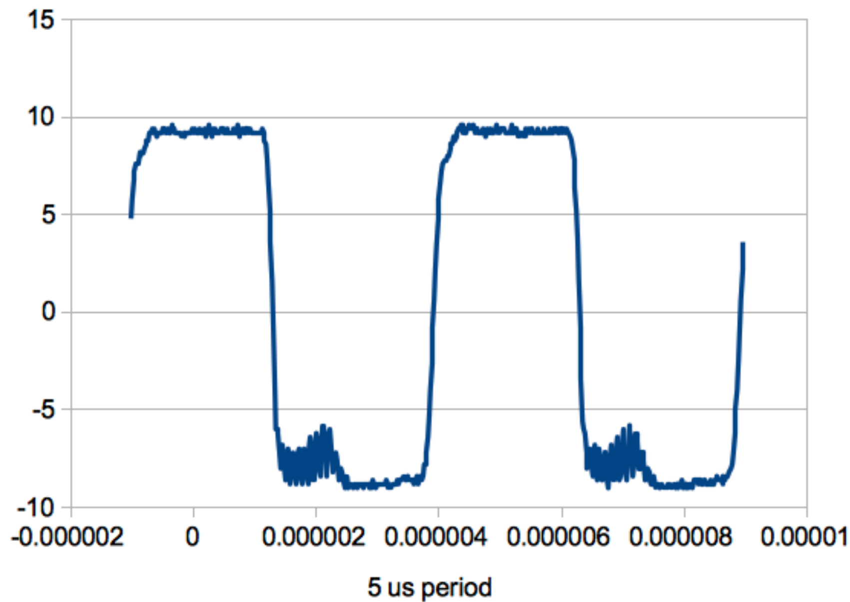


Figure 60 Time domain measurement set up for readout TFTs in passivated detector. The bulk diode bias was grounded.

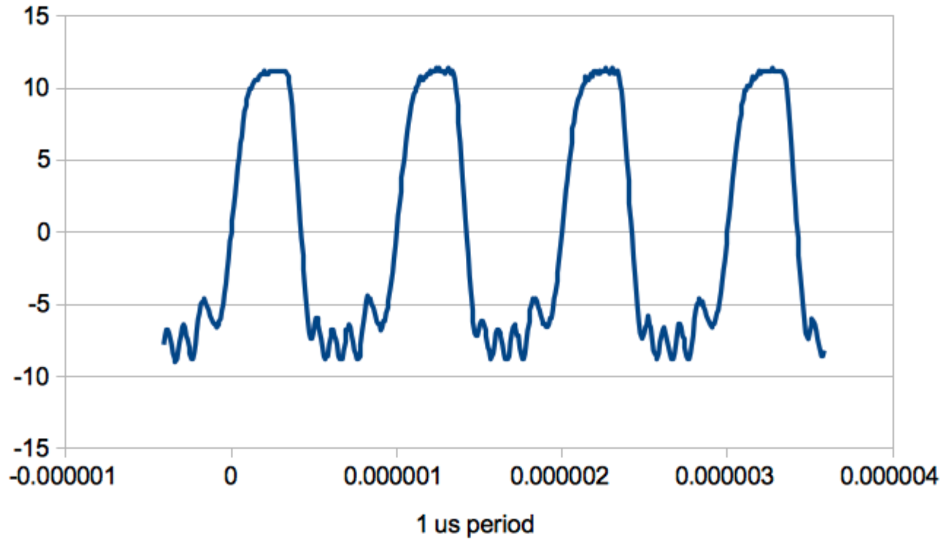
As discussed in the previous section, the readout of the detector array follows that of an active matrix array readout, which requires a fast response time (in the micro second range). Due to the nature of the detector, the active matrix array must be readout constantly prior to X-ray photon exposure. If we assume

a 1000 by 1000 array and a polling rate of 30 Hz, each row only has 33.33 μs for readout, and it decreases if the resolution requirement is larger or if a higher polling rate is required.

The response speed of the TFT readout was validated with a function generator as a gate driver. The drain electrode bias was applied with a battery (1.35 V), while the other biases (source and bulk electrode) have been maintained as ground biases. The drain current was picked up by a PerkinElmer 5182 preamplifier to be converted into a voltage signal which is, again, picked up by an Agilent oscilloscope system. The peak to peak for gate bias was 10 V, with an offset of 10 V, to ensure a 0 to 20 V square pulse input, while the duty ratio was remained at 50%. The preamplifier amplification ratio remained at the amplifier's minimum range (10^4) to ensure high frequency cut-off was prevented at the amplifier stage and to providing enough amplification for oscilloscope sensitivity.



(a)



(b)

Figure 61 Time domain response of a hybrid detector under the bias of 20 V square pulse gate bias and 1.35 V of drain bias.

The raw data from oscilloscope was captured and displayed in Figure 61, revealing the transistor on/off cycle can handle even below 1 μs of operation cycle with around 0.25 μs of rise and fall time. Thus, in theory, the single pixel detector can be integrated into a 1000x1000 active matrix active pixel array, if the polling rate is maintained at 30 Hz, a minimum requirement for real-time X-ray imaging.

4.2 Iron 55 Isotope Response

X-ray detection was evaluated using an iron-55 isotope which emits 5.8 keV gamma photons. The iron-55 X-ray source had 100 μCi of activity when it was obtained in 2008. However, the measurement took place in 2014 and the half-life of the isotope was 2.7 years. Thus, we can assume that the actual activity can be 27.03 μCi for our 2014 experiment. The isotope was a planar iron sheet of 2.54 cm by 2.54 cm square attached on top of a 4 cm diameter plastic surface. Thus, we were able to fit the source under a 3" (7.62 cm) wafer using an improvised method (shown in Figure 62).

The chuck electrode was designed to include nitrogen vacuum vents, which hold everything on top of the bulk electrode firmly and provide contact to the bulk electrode and the stainless steel nuts, as well as the iron-55 isotope. Meanwhile, the TFT device was probed with Signatone series 720 manipulators which were hooked up with a Keithley 4200 semiconductor characterization system. The gate bias was swept from 0 to 30 V, the drain bias was 10 V, and the bulk electrode bias was 30 V.

The direct contact detector shows an increase in the entire current flow of the detector because the photo-generated carriers add up to the drain current of the detector (see Figure 63.) In other words, the photo-generated current (ΔI_{DS}) cannot be amplified with the TFT gate bias, as was discussed in the previous section. Thus, we can conclude that the direct contact detector is not feasible for X-ray detection through in-pixel amplification. It can be noted that the field effect mobility of a direct contact detector is almost the level of nanocrystalline or metal oxide TFTs, but leakage (through the crystalline silicon bulk) assisted on-state current cannot be trusted because the leakage (when the gate bias is less than the threshold voltage) current is still on the same level of magnitude as the on-state current.

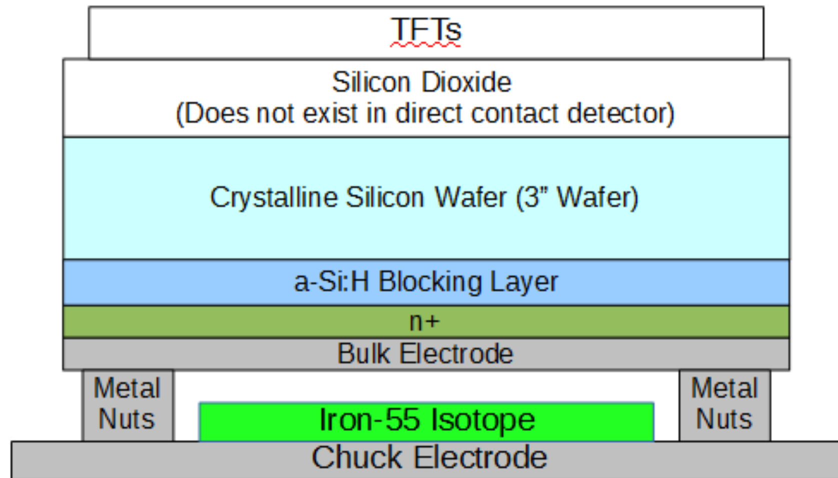


Figure 62 Iron-55 isotope exposure set up for hybrid detectors.

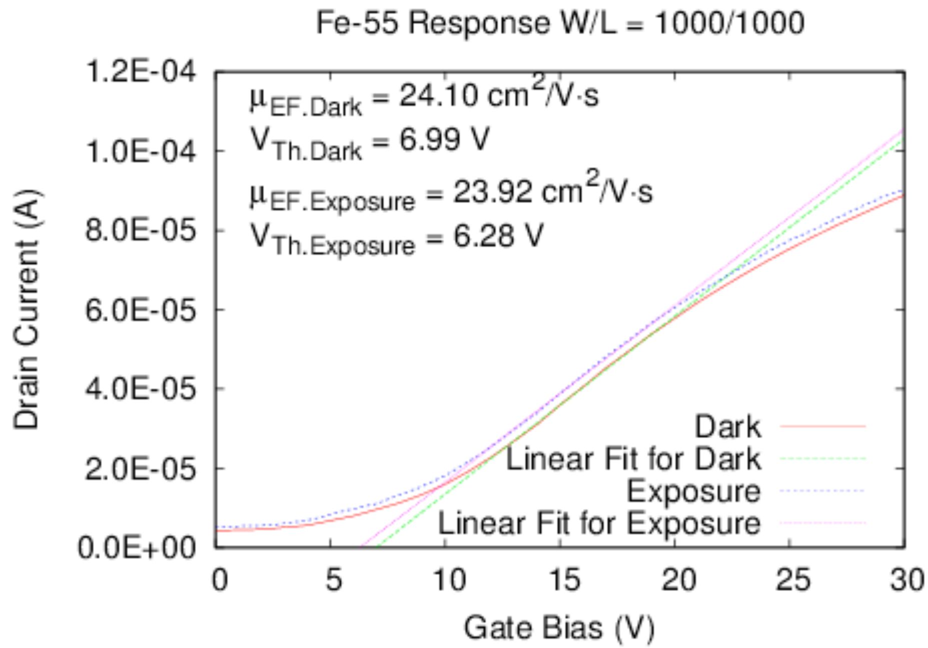


Figure 63 Iron-55 isotope exposure comparison for direct contact detector.

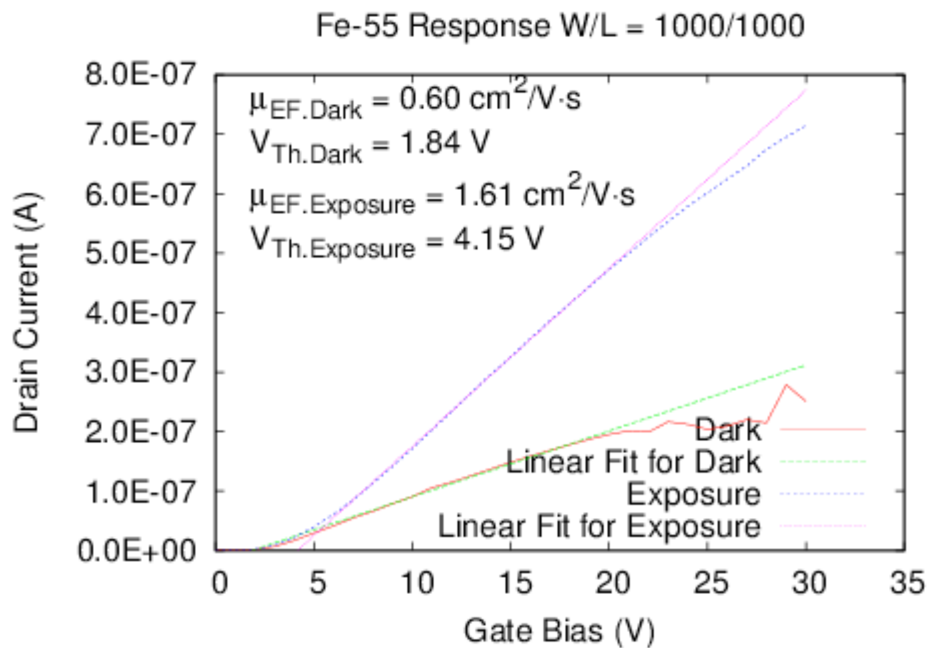


Figure 64 Iron-55 isotope exposure result for 1 mm by 1 mm passivated hybrid detector.

However, the silicon dioxide passivated detector shows promising result for the in-pixel amplification detector operation, as seen in Figure 64. Although the drain current at the on-state bias condition is much smaller than the direct contact counterpart, the ΔI_{DS} of a passivated detector increases as the gate bias strengthens from 0 V to 30 V—an indication of in-pixel amplification. Also, we can note a field effect mobility increase of 167% was achieved with the 5.89 keV X-ray exposure. We can also note the threshold voltage change (2.31 V of increase) under X-ray exposure, which was caused by photo-generated holes (see Figure 17.)

Therefore, we can conclude that the passivation played a critical role in the detector operation mechanism by separating the TFT current and the photo-generated current. The direct contact of the a-Si:H layer not only caused huge off-state leakage and Kink effect, but also deteriorated the detector functionality. Although the direct contact detector provides higher field effect mobility, which is required for high resolution arrays, losing its sensitivity (mobility difference of 0.7%) against passivated counterparts cannot be ignored. To further quantify in detail the performance of the passivated detector, a quantum accounting calculation is necessary which is described in a following section. Specifically, we will seek to answer the question of how much TFT current is generated for each absorbed X-ray photon.

4.3 Detector Noise Investigation

4.3.1 Noise Test Set Up

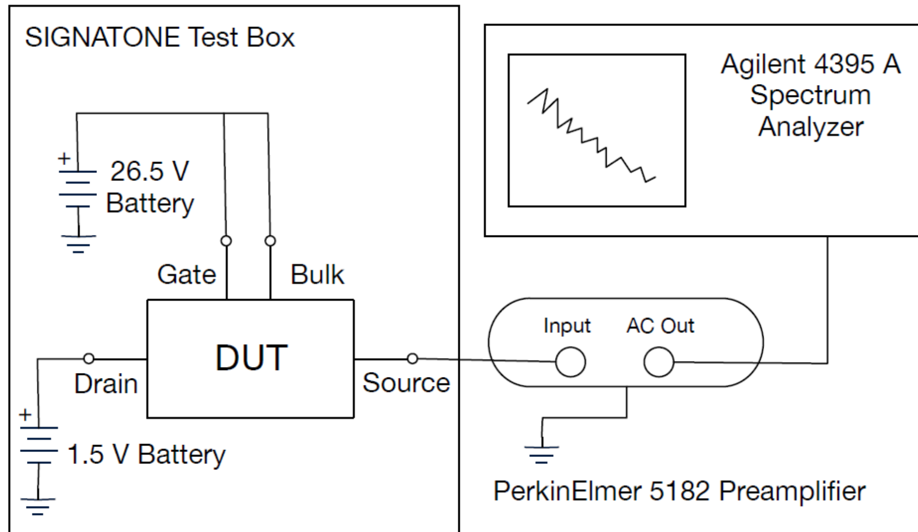


Figure 65 Noise test set up diagram for hybrid detector. External biases for the detector and preamplifier were provided with battery.

Detector noise characterization is a mandatory procedure to figure out the minimum signal that the detector is capable of detecting. The noise comes from various sources and additively combined in every detector system which needs to maximize their dynamic range which can be widened with lowering noise or improving charge collection in the detector. Because the hybrid detector is mainly composed of a-Si:H TFT and the back-to-back diode contacts, we can expect that the main noise sources will be the TFT noise, including thermal and flicker noise (1/f noise) and shot noise from the bulk contacts when the photodiode is placed under its reverse bias condition.

At first, we performed a sanity check for the noise test system with metal resistors. Each of the terminals of resistors were fed into a PerkinElmer 5182 preamplifier and placed in a Signatone test box to prevent any external noise interference. With such a simple resistor check, we were able to find proper shielding conditions for TFT measurements. The verification of the noise test system was accompanied with measuring thermal noises of different metal resistors. The noise voltage, which was fed into an Agilent 4395A spectrometer, can be calculated as follows:

Equation 16

$$\bar{v} = \sqrt{\bar{\imath^2}} A_{preamp} A_{sa} = \sqrt{\frac{4kT}{R}} 10^8 10^{-1}$$

where k is Boltzmann's constant, T is the temperature in Kelvins, R is the resistance, A_{preamp} is transimpedence gain of the preamplifier, and A_{sa} is the gain (attenuation) from the preamplifier to the spectrum analyzer input. The calibration result for six different resistors can be found in Figure 66.

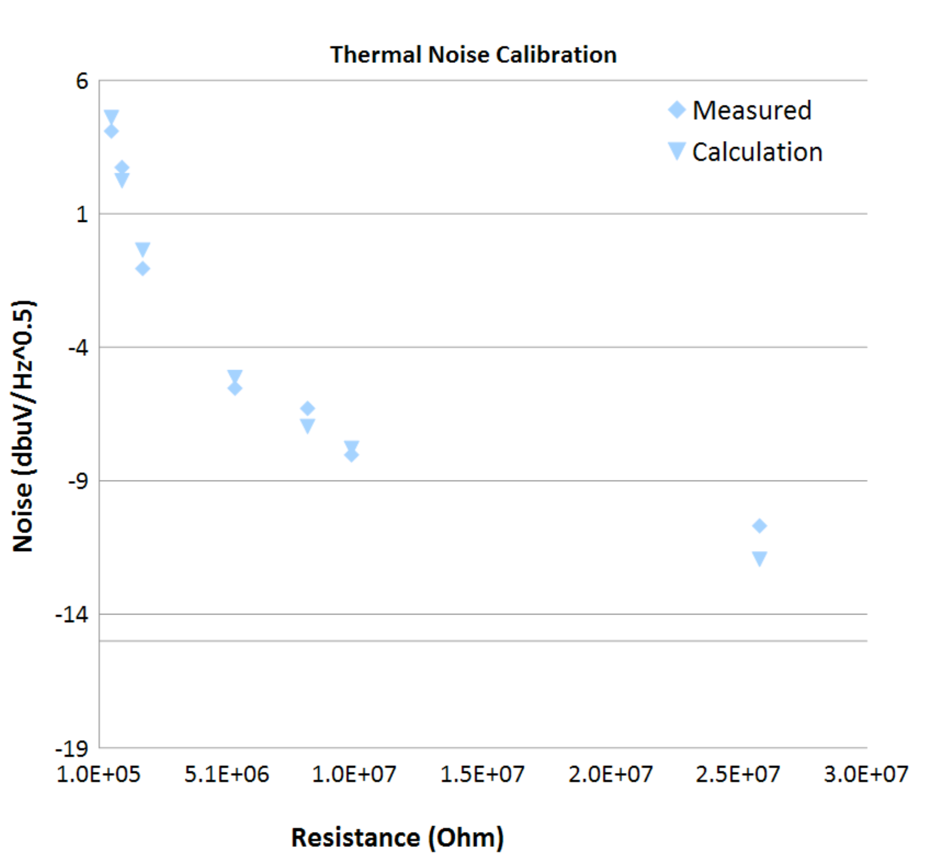


Figure 66 Noise calibration data from resistance thermal noise analysis.

The preamplifier gain setting was the maximum value (10^8 A/V) which results in the lowest bandwidth necessary to ensure minimize noise interference from the preamplifier itself (15 fA/Hz$^{-0.5}$). However, the

setting was limited by the 3 dB frequency of the amplifier itself at 1 kHz. Therefore, the noise measurement was taken at 800 Hz at the spectrum analyzer to avoid a 3dB cut-off frequency effect.

Table 15 Thermal noise calibration table.

Resistance (Ω)	Calculated Thermal Noise ($db\mu V/\sqrt{Hz}$)	Measured Noise ($db\mu V/\sqrt{Hz}$)
5.75×10^{5}	4.60	4.1
9.90×10^{5}	2.24	2.74
1.80×10^{6}	-0.36	-1.04
5.40×10^{6}	-5.13	-5.5
8.24×10^{6}	-6.97	-6.25
9.96×10^{6}	-7.79	-7.97
2.59×10^{7}	-11.94	-10.58

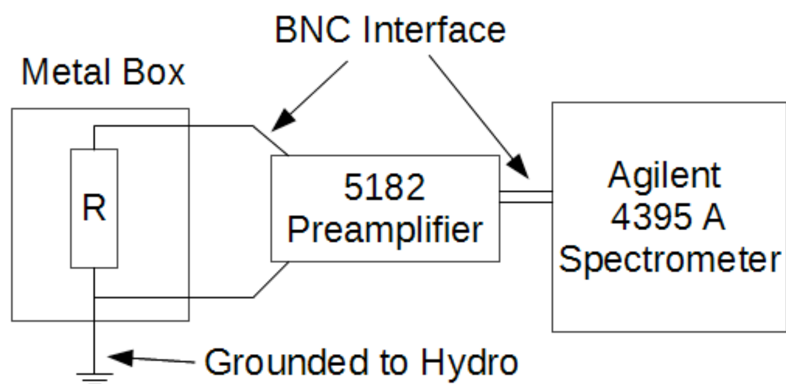


Figure 67 Noise measurement calibration set up. Thermal no

Because the noise voltage difference remained lower than 10 % from calculated data, we decided the noise test environment was feasible for further noise testing for TFTs and established the noise test environment depicted in Figure 65. The biases for TFT operation were provided by alkaline batteries to avoid 60 Hz noise from city electricity and the test was performed at evening to night time to avoid any additional noise from construction and building maintenance crews.

We also concluded that TFT thermal noise can be calculated without measuring the device if its channel resistance (R_{Ch}) and thermal noise power spectral density ($S_{I.Th}$) are extracted via the following equation:

Equation 17

$$R_{Ch} = \frac{L}{\mu_{FE} C_{gate} W (V_{GS} - V_{Th})}$$

$$S_{I.Th}(f) = \frac{4kT}{R_{Ch}}$$

If the TFT was operated in a linear region, then we can evaluate the power spectral density of thermal noise on direct contact and passivated detectors based on experimental values from the previous section.

Table 16 Thermal noise of various sized detectors.

Detector Type	L (μm)	W (μm)	R_{Ch} (Ω)	Thermal Noise Spectral Density (A^2/Hz)
Direct Contact	1000	1000	531997	3.11E-026
	25	180	73889	2.24E-025
	15	50	127679	1.29E-025
	5	25	106399	1.56E-025
Passivated	1000	1000	5710307	2.90E-027
	25	180	793098	2.09E-026
	15	50	1370474	1.21E-026
	5	25	1142061	1.45E-026

It is obvious that the thermal noise spectra from drain current are inversely proportional to the channel resistance and channel length. Also, we can note that the thermal noise spectra stays around 10^{-25} for a-Si:H based hybrid detectors at most. This can be interpreted as 26 electrons of noise current when the pixel gain is set to a 1 for 33.33 μs readout time frame for a L/W = 5/50 direct contact detector. Thus, we can assume that the contribution of thermal noise in a-Si:H TFT based detector is fairly limited compared to other noise sources as will be discussed in following sections.

4.3.2 Flicker Noise Investigation (Detector Size)

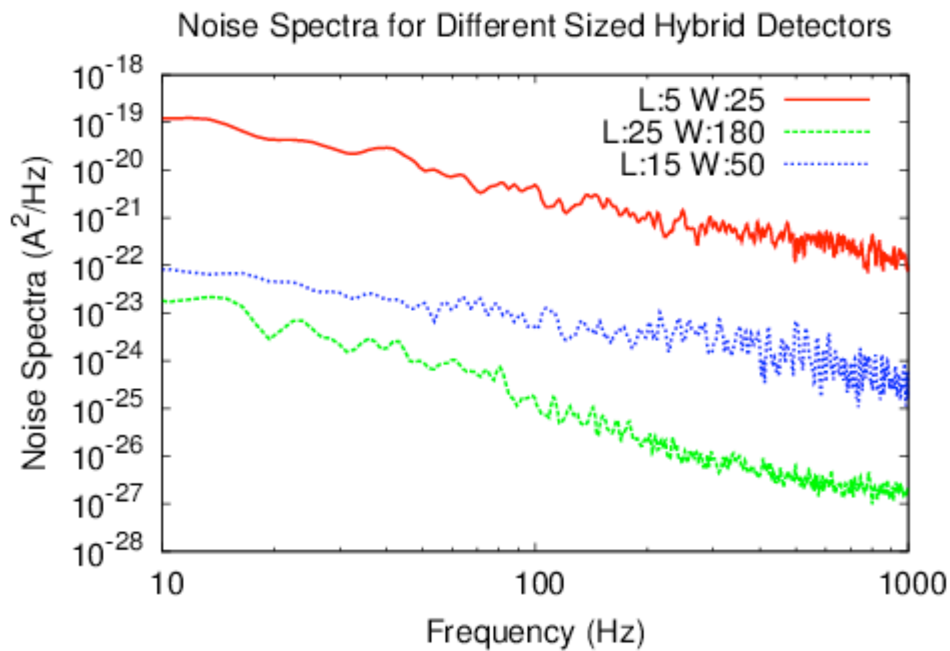


Figure 68 Noise power density spectra for various sized passivated detectors. Bulk bias was maintained at 0 V.

The flicker noise of a TFT is reported to stem from the hopping conduction of carriers and a charge trapping-detrapping situation causes the drain current to fluctuate over time as described in [72, 73]:

Equation 18

$$S_{I.1/f}(f) = \frac{1}{f}\frac{\alpha_H q {I_{DS}}^2}{WL(V_{GS} - V_{Th})C_{gate}}$$

α_H is a fitting parameter (coulomb scattering coefficient) and considered as 0.05 for a-Si:H TFT operating in linear region [74]. According to the noise data depicted in Figure 68, the α_H can be derived as 0.007 at 100 Hz for W/L = 25/180 device when it was biased under 26.5 V of gate bias.

The flicker noise was extracted with the same set up depicted in Figure 65, while the bulk bias remained as ground bias (0 V). Due to the low frequency nature of the flicker noise, the noise sample acquisition was performed at a very slow rate. The sweep/sample rate for the spectrum analyzer was ~ 11 s, and the frequency bandwidth was 1 Hz to 1000 Hz while frequency resolution was set to 1 Hz. Tests were run for more than 15 minutes (> 20 samples) with constant bias provided by alkaline batteries.

As depicted in Equation 18 and Figure 68, the flicker noise is a physical property that is dependent on the TFT size itself. In Equation 18 (Hooge's Model), the drain current (I_{DS}) also includes W/L term as discussed in the section 2.1.3 where the device under test is operating under liner mode of operation. Thus, flicker noise spectra, $S_{I.1/f}$ is heavily dependent on channel length: $S_{I.1/f} \propto {}^{W}/_{L^2}$. Such dependence is also shown in Figure 68, where the shortest gate length device (5 μm) shows even four orders of magnitude larger than 15 μm of gate length device. The largest device, 25 μm of channel length, even shows up thermal noise at 1000 Hz of frequency. Since our measurement scope was limited under 1000 Hz due to the pre-amplifier limitation, we have taken the 25 μm device for further characterization on the shot noise from the bulk diode contact.

4.3.3 Shot Noise Investigation (Bulk Bias)

It is possible to obtain a noise electron per given frame time if the detector was composed only with a TFT. However, the bulk bias also provides a noise current from the negative biased contact as depicted in Figure 69. We can define the shot noise spectra for reverse biased PN junction photodiode as follows:

Equation 19

$$S_{I.Shot} = \sqrt{2qI_{dark}},$$

As depicted in Figure 69, the noise from the bulk diode contact cannot be ignored during the operation. The shot noise itself provides an order of magnitude of higher power spectral density where the similar range of 15 µm gate length device.

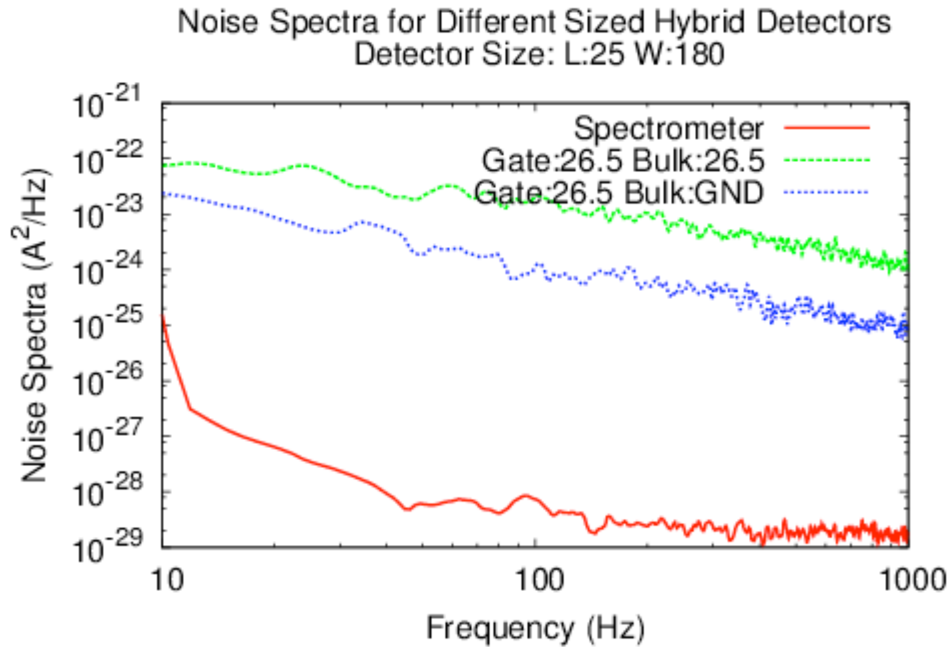


Figure 69 Noise power density spectra for passivated detector on bulk bias and without bulk bias conditions.

The increase in the poser spectral density with the bulk diode contact bias shows a flat increase for throughout the entire noise spectra. In this case, we can suspect the thermal noise as well. However, the thermal noise for 0.86 nA of leakage is as low as $1.67\times10^{-27}\ A^2/Hz$ which is not even close to any noise contributors under 1000 Hz range. Therefore, the dominating factor of the flat increase is the shot noise from reverse bulk diode contact.

The shot noise can be resolved by implementing industrial quality contact layer for the bulk contact since the doping efficiency for the n+ a-Si:H layer was questionable with the in-house fabrication facility. However, the reverse bias current of a P-N junction diode comes from electron diffusion and generation current, cooling the device in operation will be an excellent workaround to minimize the effect of shot noise.

4.3.4 Total Noise Estimation

To verify the how well the fabricated device stacked up to the initial performance prediction shown in Table 2, the noise spectra shown in Figure 69 was curve fitted. A square root method using a residual function of $f(x) = Ax^{-B}$ was employed since the dominant noise source under 1000 Hz was the flicker noise. Each condition, bulk bias of 26.5 V and 0 V, was fitted separately and the given residual function was integrated from 1 to 30 kHz to account for the 30 frame per second (FPS) operation of a hypothetical 1000 by 1000 pixel array.

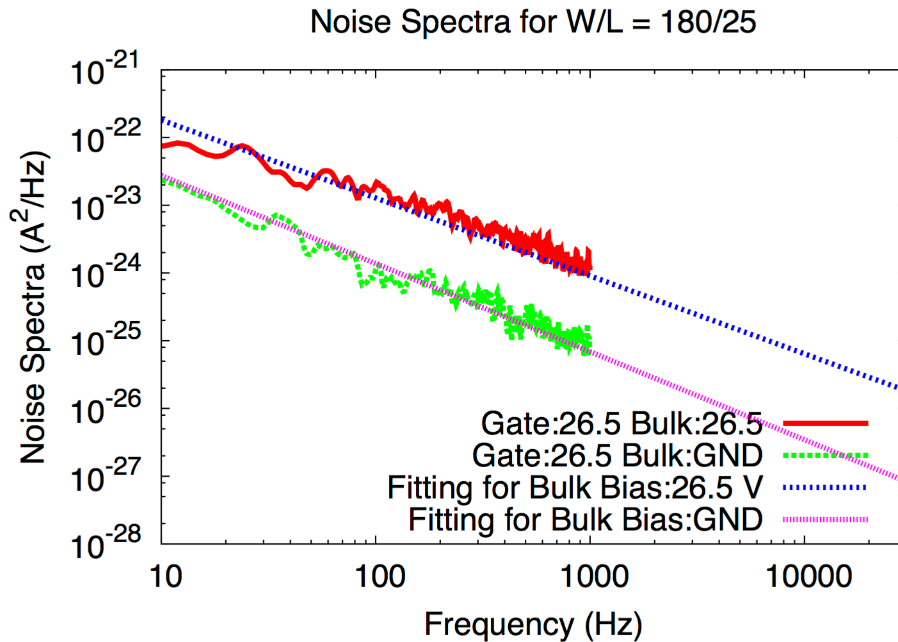


Figure 70 Square root fitting for the noise spectra of 25 by 180 (μm/μm) pixel up to 30 kHz.

The integrated noise value is the noise at the output of the 1T APS TFT, or alternately, the drain electrode current. Thereafter, input referred noise was obtained by dividing the output referred noise current with transconductance of the readout TFT. The transconductance was obtained as the derivative of the transfer curve of 1 mm by 1 mm passivated detector (see Figure 54) at 1 V of drain bias. Figure 71 shows the transconductance curve of the 1 mm by 1 mm detector. Since the noise characteristic was obtained from a smaller device, the transconductance value observed at 26.5 V, i.e 3.0 nA/V, was translated to 24 nA to account for the different W/L of the device under X-ray test based on the equation below.

Equation 20

$$g_m = \frac{dI_{ds}}{dV_{gs}} = \mu_{FE} C_{gate} \frac{W}{L} V_{ds}$$

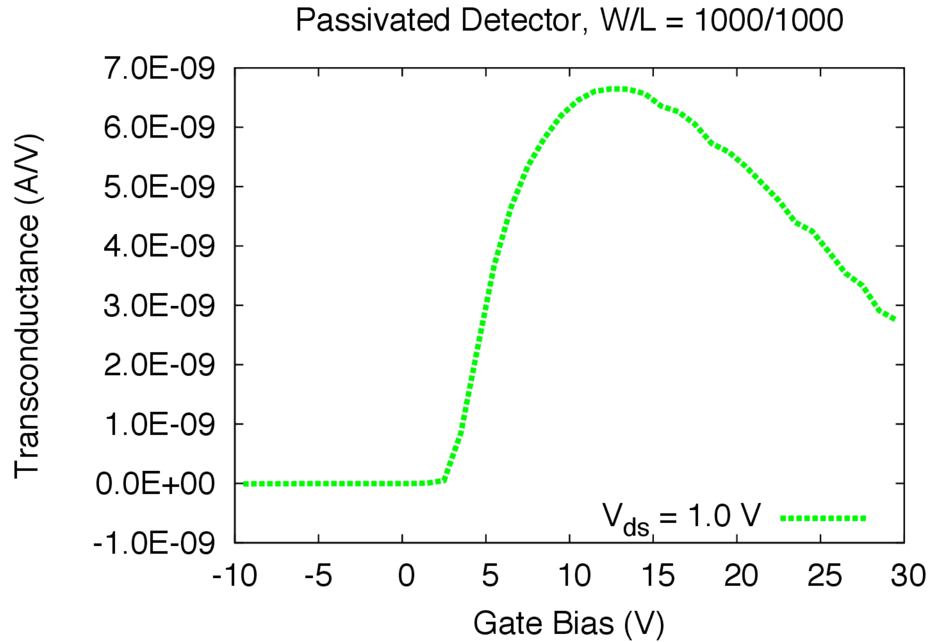


Figure 71 Transconductance curve of 1 mm by 1 mm pixel at drain bias of 1.0 V.

The input referred noise calculated from the measured noise spectra was determined 19590 electrons when the bulk diode contact was biased and 7059 when the bulk contact was grounded. Such a large noise value when the bulk diode is biased indicates that the majority of noise is supplied by the bulk diode contact (when biased reversely) while the TFT itself also shows a significant flicker noise component.

Even though the flicker noise was large, it is in principle manageable using good circuit design techniques on the active pixel as reported in the past [75]. However, the bulk diode contact shot noise is at least 3 times larger than the TFT noise itself. Therefore, pixel noise is dominated by the shot noise from the bulk diode contact and the first consideration before any industrial implementation requires an improvement of the bulk diode contact or alternately, improving the detector operation by using low temperatures to suppress the dark current.

Table 17 summarizes the noise test results with the expectations originally anticipated in Table 2. As expected in 2.3, the dynamic range of the passivated detector is higher than the direct contact detector due to higher pixel capacitance, which was provided with thermally grown silicon dioxide. However, due to the unexpected bulk diode contact shot noise and flicker noise, the signal to noise ratio was an order of magnitude lower than expectation. In terms of price, the passivated detector can in theory, be fabricated at the similar price point as amorphous selenium detectors.

Table 17 Detector performance comparison with the original expectation.

Parameters	Original Expectation (direct contact detector)	Measured (passivated detector)
Pixel Size (μm^2)	25 x 25	25 x 180
Detector Size (mm^2)	212 x 212	212 x 212
EHP Conversion ($6\ keV/W_{\pm}$)	1667	1667
Readout Noise (30 FPS, 1000 by 1000 array)	< 1500	19590
Dynamic Range	1:3600 (Direct Contact Detector)	1:110000 (Passivated Detector)
SNR	Around 1	Around 0.1
Readout Speed (1000 by 1000 array)	30 FPS	30 FPS
Price (USD) per Detector Size (1 mm by 1 mm)	0.66	0.66

4.4 X-ray Sensitivity

4.4.1 X-ray Absorption Investigation

To clarify the relationship between electron-hole pair generation rate and impinging X-ray photon flux, the photocurrent generation was investigated via the Monte-Carlo simulation method as follows. At first, we need to determine the number of X-ray photons impinging on the detector area from the iron-55 isotope source. The main problem is, unlike medical purpose X-ray generators, the isotope X-ray emission is not collimated but isotropic. To get a rough estimate, we decided to use the Monte-Carlo method to determine the number of X-ray photons actually being absorbed in the detector area.

For such purpose, we adopted a Monte-Carlo simulation package from Open Gate Collaboration [76]. The system was defined to mimic the isotope exposure situation depicted in Figure 62, where the distance between the isotope and the back contact electrode was 1 mm because the thickness of the metal nuts were 2 mm and the plastic substrate for the isotope was 1 mm. The isotope activity was defined as 27.03 μCi, as depicted in Appendix C. The simulation system can be found in Figure 72 for a typical detector pixel size of 250 μm by 250 μm, including the area of source and drain electrodes.

The Monte-Carlo simulation was performed for 1000 seconds within the simulation setting to capture as many events as possible because the X-ray activity of 27.03 μCi was defined on a per second basis, resulting in 45000 captured events, as shown in Figure 73. Thus, we can safely conclude that 45 X-ray photons were impinged into the detector pixel area. If we convert the detector area to 1 mm by 1 mm, we can assume that around 720 X-ray photons were impinged per second.

Once the X-ray photons reached the surface of the bulk electrode, they need to travel through 30 nm of aluminum, 50 nm of n+ a-Si:H contact layer, and 500 nm of intrinsic a-Si:H layer to be absorbed in the crystalline silicon photodiode detector and then be converted into electron-hole pairs. Thus, we investigated X-ray photon transmission with an external source [77] for 5.89 keV photons, as depicted in Table 18. Thus, we can conclude that 0.96, or 96%, of isotope-generated X-ray photons are actually being absorbed into the crystalline silicon layer. This converts to 43 photons for a typical detector pixel size of 250 um x 250 um and 691 photons for 1 mm by 1 mm pixel detector. We also confirmed via simulation that the low energy X-ray photon cannot penetrate the crystalline silicon layer to affect TFT performance.

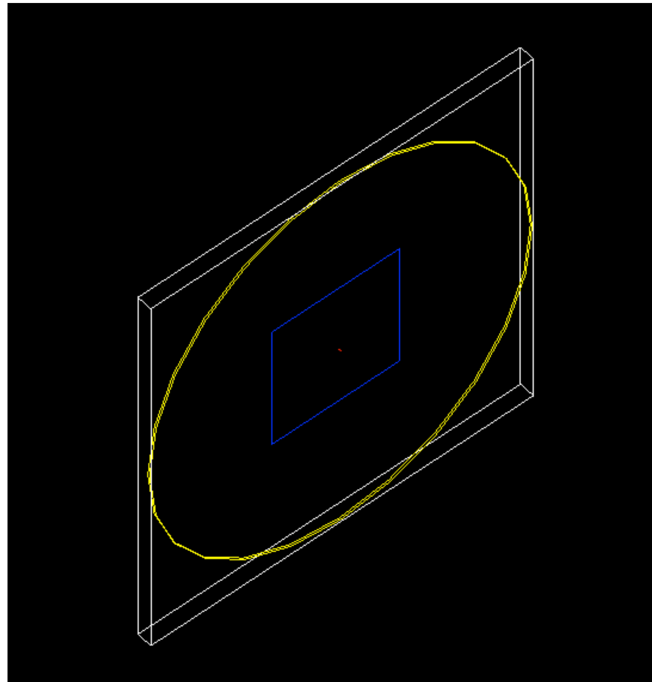


Figure 72 Monte-Carlo simulation system set up to depict the X-ray exposure from iron-55 isotope. The yellow ring is the 3" wafer, the blue square is the 1" by 1" isotope, and the small red dot is the detector pixel area.

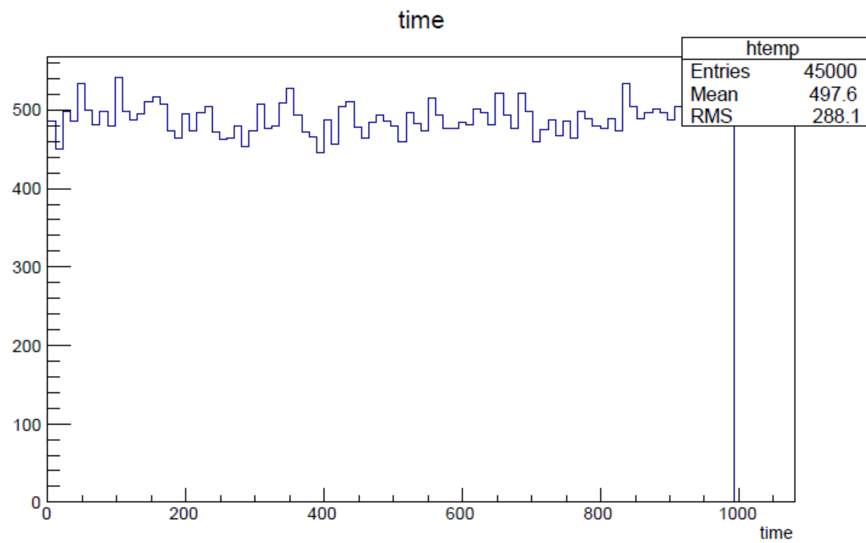


Figure 73 X-ray photon absorption counts for 1000 seconds of operation.

Table 18 5.89 keV X-ray transmission ratio information for bulk electrode penetration.

Material	a-Si:H (50 nm, n+)	a-Si:H (500 nm, leakage barrier)	Aluminum (30 nm)	Crystalline Silicon (380 um)
Transmission Ratio	0.99	0.98	0.99	0.00000403

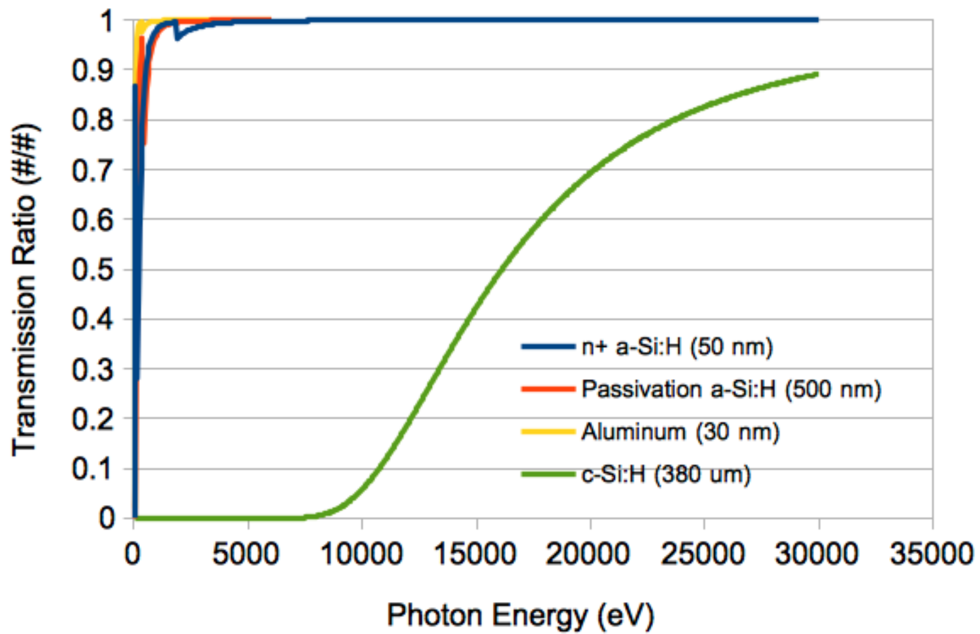


Figure 74 Photon transmission ratio for various materials. Obtained from [77].

4.4.2 EHP Conversion and Signal Amplification

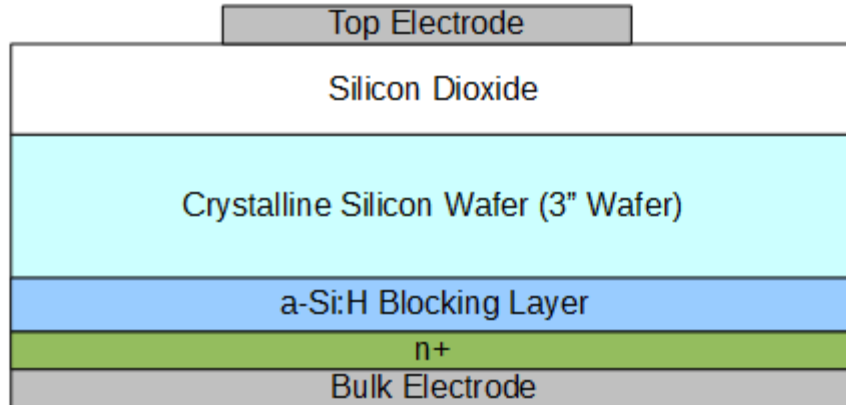


Figure 75 MIS structure setup for iron-55 isotope photo-generation evaluation.

To confirm the photo-generation caused by the iron-55 isotope, we measured current-voltage characteristics of a MIS structure (depicted in Figure 75). The bulk electrode was biased to the ground electrode, while the top electrode bias was swept from 0 to 100 V to prevent carrier loss at the a-Si:H based layers (blocking layer and n+ contact layer). The current-voltage sweep indicates that the photo-generation from the 27.03 μCi isotope source remains at 10 to 30 pA for a 1 mm by 1 mm area (top electrode dimension). It was kept at the same size as the passivated detector itself (as depicted in Figure 76 and Figure 77). Thus, we can assume that 691 absorbed photons generated 187.5×10^6 electron-hole pairs per second.

We then confirmed that the current increment of the detector stays at a 10 nA range as a minimum, but increases linearly as the gate bias increases (see Figure 78). The photo-current (ΔI_{DS}) behavior under gate bias indicates that the TFT amplification provided at least three orders of magnitude of amplification for photo-generated electron-hole pairs in the crystalline silicon substrate. Thus, we can conclude that the 619 photons generate 62.5×10^9 electrons for readout per second. Henceforth, to achieve 27.95×10^6 of signal electron generation for 30 Hz polling time, we need 5.89 keV X-ray photons arriving at a rate of 1 every 100 seconds to achieve SNR > 5.

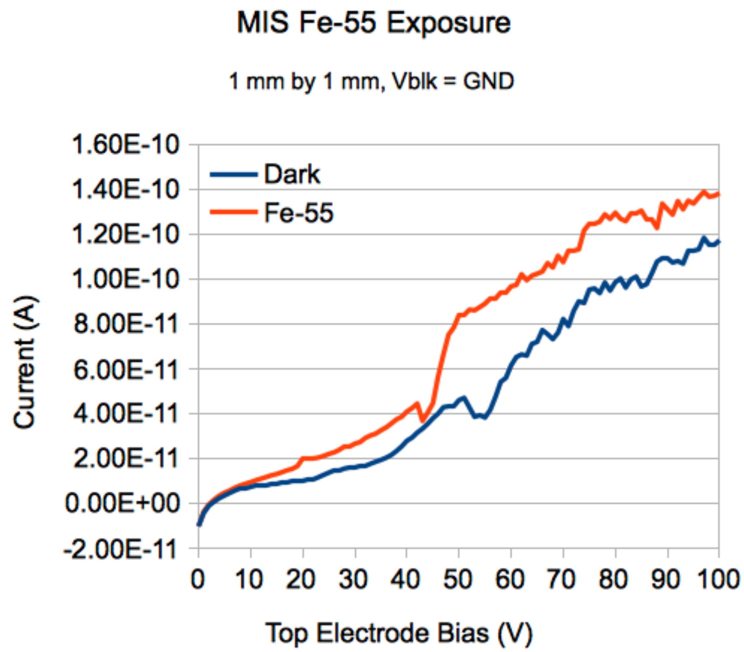


Figure 76 MIS structure I-V test result.

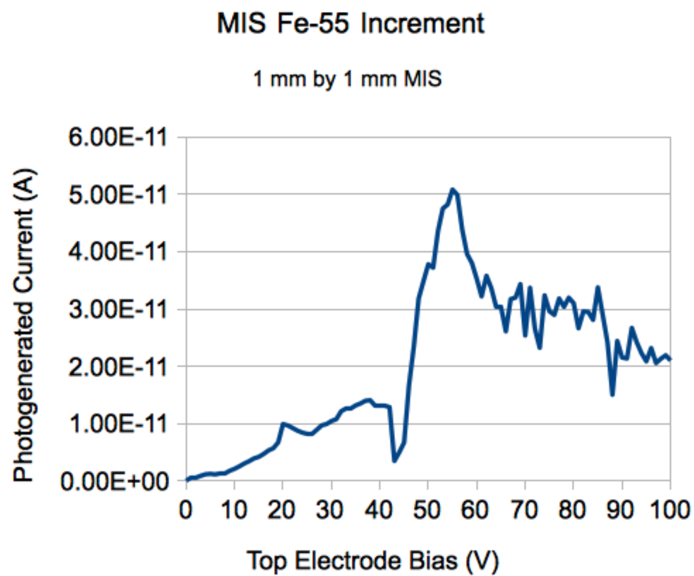


Figure 77 Current increment from the MIS exposure results.

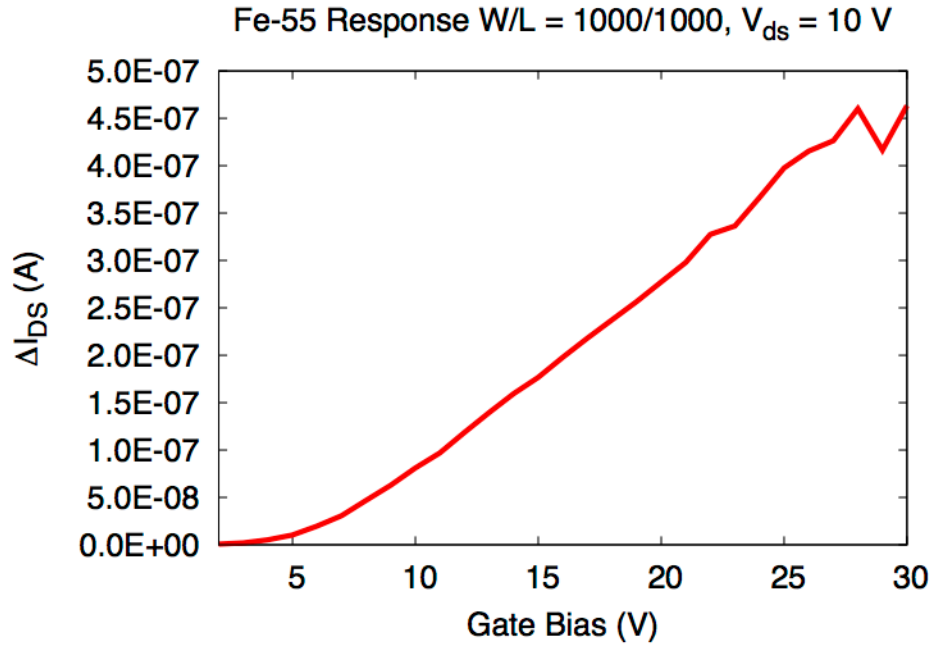


Figure 78 Drain current increment from X-ray (iron-55) detection.

However, Figure 78 also indicates that the photo-current relation depicted in Equation 9 because it does not convey the effect of the TFT gate bias and the field effect mobility leap in any case. Because the photo-conversion gain is dependent to the gate bias of TFT, we can suggest the ΔI_{DS} to photo-generated charge (Q_{photo}) relation as:

Equation 21

$$\Delta I_{DS} = \mu_{EF.Dark} C_{gate} \frac{W}{L} (A \cdot \frac{Q_{photo}}{C_D} + B \cdot V_{GS}) V_{DS}$$

A and B serve the role of fitting parameters on photo-conversion gain of the crystalline silicon substrate and field effect mobility modulation constant due to the X-ray exposure. In short, the photo-generated current is affected by the photo-generated 'virtual' gate underneath the silicon dioxide passivation layer and the gate bias. In the passivated detector's case, we can assume that $C_D = 7.87 \times 10^{-9}\ C/cm^2$from the measurement of the MIS structure as depicted in Figure 79 at the top electrode voltage bias of 20 V, which shows neither inversion or accumulation regions of a MIS capacitor, showing the total capacitance

of thermal oxide-crystalline silicon substrate series capacitance. On the other hand, the field effect mobility ratio from X-ray exposure can be given by the difference of the dark and X-ray exposure conditions ($\frac{|\mu_{EF.Exposure}-\mu_{EF.Dark}|}{\mu_{EF.Dark}}$) which is 1.68 in the current passivated hybrid detector as depicted in Figure 64. In short, A and B represent the 'virtual gate' threshold voltage constant and mobility modulation factor, respectively.

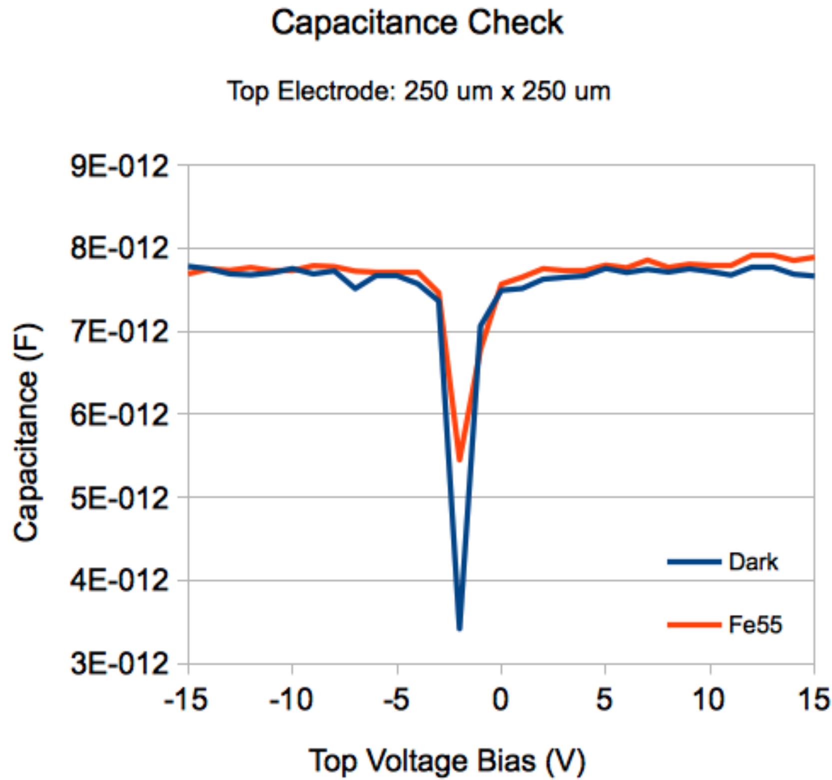


Figure 79 Capacitance sweep of the passivated detector.

Therefore, we can derive the 'virtual gate' threshold voltage constant, A, from a square root fitting of the X-ray induced current, which was 5.85 in the current device under the drain bias of 1 V. Ideally, the fitting parameter must remain at the same amount of the mobility modulation factor (B) because the X-ray generated charge is supposed to provide additional amplification via the 'virtual gate' provided charges. However, constant recombination and leakage through the bulk bias compromised the charge storage in

the crystalline silicon substrate. Also, the surface charge contribution of thermal oxide-crystalline silicon interface and the interface between the thermal oxide and a-Si:H channel layer are not negligible due to the nature of a-Si:H material.

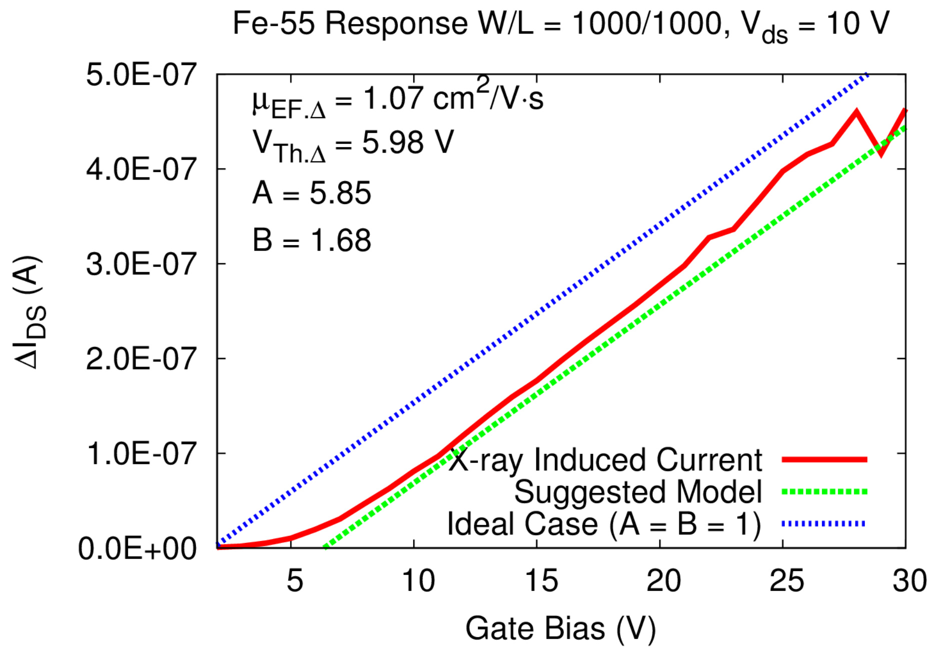


Figure 80 Comparison of suggested model and extracted data.

4.5 Closing The Loop

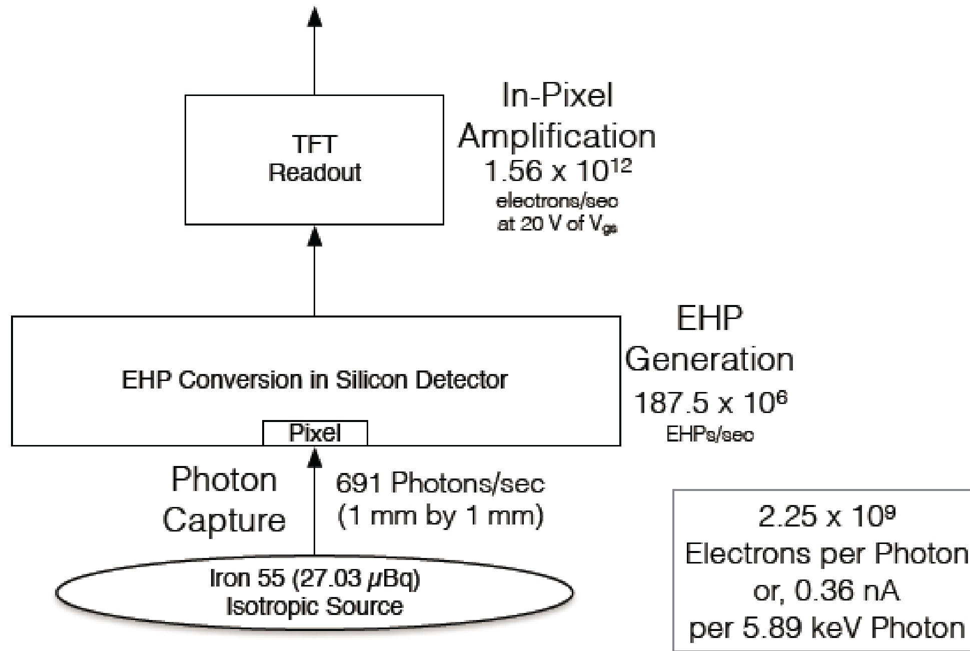


Figure 81 Determining the number of electrons generated per absorbed photon.

Figure 81 describes the process by which the number of electrons generated for each photon absorbed in the passivated detector is calculated. Monte-Carlo simulation was used to estimate the number of impinging 5.89 keV photons onto a 1 mm by 1 mm single pixel for the given Fe-55 gamma source: i.e. 691 photons per second. As the photon are converted into electron-hole pairs in the silicon detector, the photo-generated holes provided the 'virtual gate' effect for the 1T APS TFT, yielding 0.36 nA of photo-current when the device was biased under 20 V of gate bias while the drain bias was 10 V. Alternately, 2.25×10^9 electrons are detected at the output of the single-TFT APS for each absorbed photon.

The noise measurement investigation in section 4.3 showed that a single pixel was affected a large amount of noise due to the shot noise from silicon detector bulk bias. Since the flicker noise measurements were performed on a $25\ \mu m \times 180\ \mu m$ pixel, the noise had to be scaled for the larger pixel $1\ mm \times 1\ mm$ pixel used for X-ray sensitivity measurements. Flicker noise for the larger device with W/L of ${}^{1\ mm}/_{1\ mm}$ was much smaller than for the smaller device and this is to be expected. Silicon detector dark current was measured at the diode contact and the shot noise for the $1\ mm \times 1\ mm$ device

was estimated based on the measured dark current value. Thus, we estimate the total noise for the 1 mm by 1 mm detector as being 12551 electrons for a 30 FPS, 1000 by 1000 array set up. Thus, it requires at least 7.52 photons to overcome the detector noise for a $1\ mm \times 1\ mm$ detector.

The above noise measurements were obtained at the pixel level. In an array, external readout electronics and array parasitic elements such as line capacitance will affect the total noise although it is not expected to be significant because we have employed a 1T APS. In addition, our estimate has focused exclusively on electronic noise and has neglected photon shot noise and any other relevant modular transfer function effects, both of which are important to the overall image quality.

Chapter 5
Conclusions

5.1 Summary and Conclusion

In this work, we proposed a silicon detector with a-Si:H TFT readout, enhanced with in-pixel amplification using a one transistor active pixel sensor. We developed a cost-effective simple two mask fabrication procedures. Because of the abundance of silicon substrates and large area fabrication capabilities of PECVD, our device can expect to realize a large manufacturing cost reduction for X-ray detectors for low energy X-ray detection applications.

An investigation into two types of in-pixel amplification detectors uncovered the fact that allowing direct contact from the a-Si:H channel to the crystalline silicon detector layer causes detrimental effects not only to the performance of X-ray detection itself, but also to the a-Si:H TFT switching capability due to the floating bulk effect. However, this problem was mitigated by growing a silicon oxide passivation layer on the silicon substrate before initiating the TFT deposition process.

Although the passivated detector shows much lower performance than the direct contact type due to lack of additional driving current, the in-pixel amplification overcame the noise limitation of a-Si:H TFT itself and even showed promising results for photon counting detectors by reducing the photon flux requirement to overcome the TFT noise and the bulk bias shot noise.

Furthermore, such a simple pixel structure (a single TFT acts as a readout switch, an amplifier and the detector) enables maximizing the fill factor and minimizing pixel size without considering additional capacitors or amplification/reset transistors. Such a simple pixel structure provides flexibility to the array design when it comes to the array size and the resolution requirements that need to be met simultaneously.

Therefore, we discovered that even with a simple SOI-like structure, we can provide cost effective and large area capable X-ray detectors without implementing any complex and expensive fabrication methods, such as laser ablation or controlled RIE etching. Also, we discovered that simply growing another insulator on crystalline silicon solves many fundamental problems for the detector itself. We hope the new hybrid detector will contribute to low energy X-ray applications such as X-ray diffraction and protein crystallography.

5.2 Further Improvements

Although we proposed a simple and economic way to detect low energy X-ray, the limitation of a-Si:H TFT performance bottlenecks array size and resolution. In fact, current industrial flat panel displays show that a-Si:H TFTs cannot be used anymore to drive the resolution higher than 1080p applications. In other words, the resolution of the hybrid detector we proposed will also be affected. Thus, we can improve the TFT channel material for higher performances. Possible candidates are nanocrystalline silicon, metal oxide, and even low temperature polysilicon if its production cost can be contained to an economic level. The paradigm shift of depositing readout electronics on the sensor (as opposed to the conventional sensor on electronics or multi-chip module integration) enables this improvement.

Furthermore, assessment of modular transfer function for hybrid detectors is required to verify spatial resolution claims. It is possible that excess X-ray photon generated carriers will not exit the crystalline silicon bulk and will diffuse to adjacent pixels causing blurring and even ghosting in captured images. Such a problem would be most prominent in small pixel systems.

Also, we can investigate cheaper solutions for passivation because thermal oxide growth requires dedicated oxidization chambers. We suggest polymer materials which can be easily spin-coated. They provide reasonable insulation without requiring backside BHF etch processes to open the back contact for bulk electrode. Even high quality PECVD deposited a-SiN_x:H that is already available in a TFT fabrication facility can be suitable option for passivation.

Lastly, we can also implement a co-planar structure for readout transistors which would reduce the parasitic resistances. The lack of need to punch through the channel layer reduces the parasitic resistance effect, which is even seen in the X-ray amplified curve in Figure 64. The X-ray exposure can be explained simply by reducing the channel resistance, the parasitic resistance effect cannot be ignored when the gate bias increases to obtain more amplified current. In that sense, LTPS (low temperature polysilicon) are the optimal candidate for industrial quality detectors.

5.3 Academic Contributions

- Cadmium zinc telluride detector for low photon energy applications, SPIE Medical Imaging 2010: Physics of Medical Imaging, March 23, 2010

  Authors: Kyung-Wook Shin, Kai Wang, Karim S. Karim

- Novel silicon x-ray detector with TFT readout, SPIE Medical Imaging 2012: Physics of Medical Imaging, March 9, 2012

  Authors: Kyung-Wook Shin, Karim S. Karim

- Fabrication and characterization of a novel x-ray silicon detector, SPIE Medical Imaging 2013: Physics of Medical Imaging, March 19, 2013

  Authors: Kyung-Wook Shin, Karim S. Karim

- a-Si:H TFT-Silicon Hybrid Low Energy X-ray Detector, IEEE Transactions on Electron Devices, Preparing submission, September, 2014.

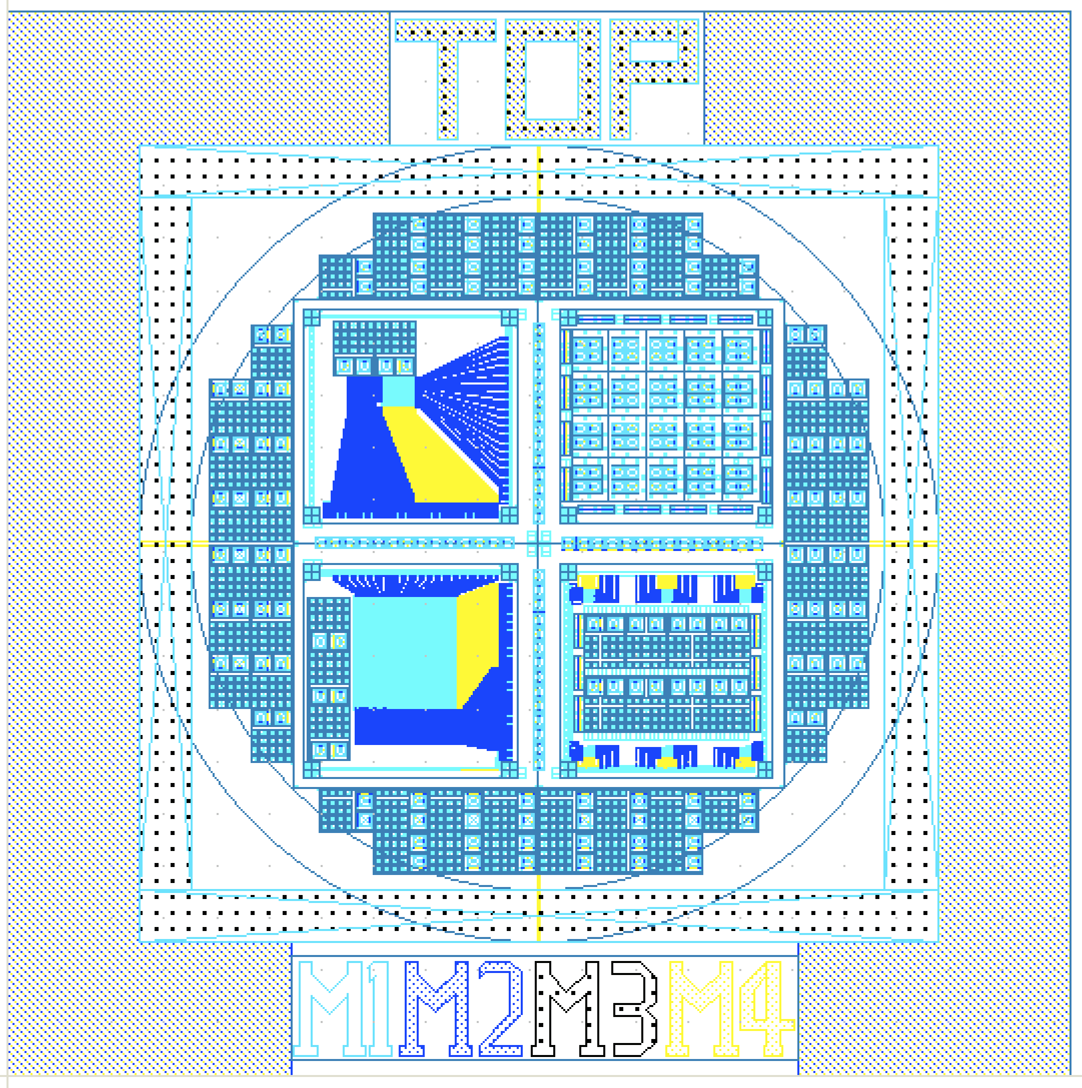
  Authors: Kyung-Wook Shin, Karim S. Karim

Appendices

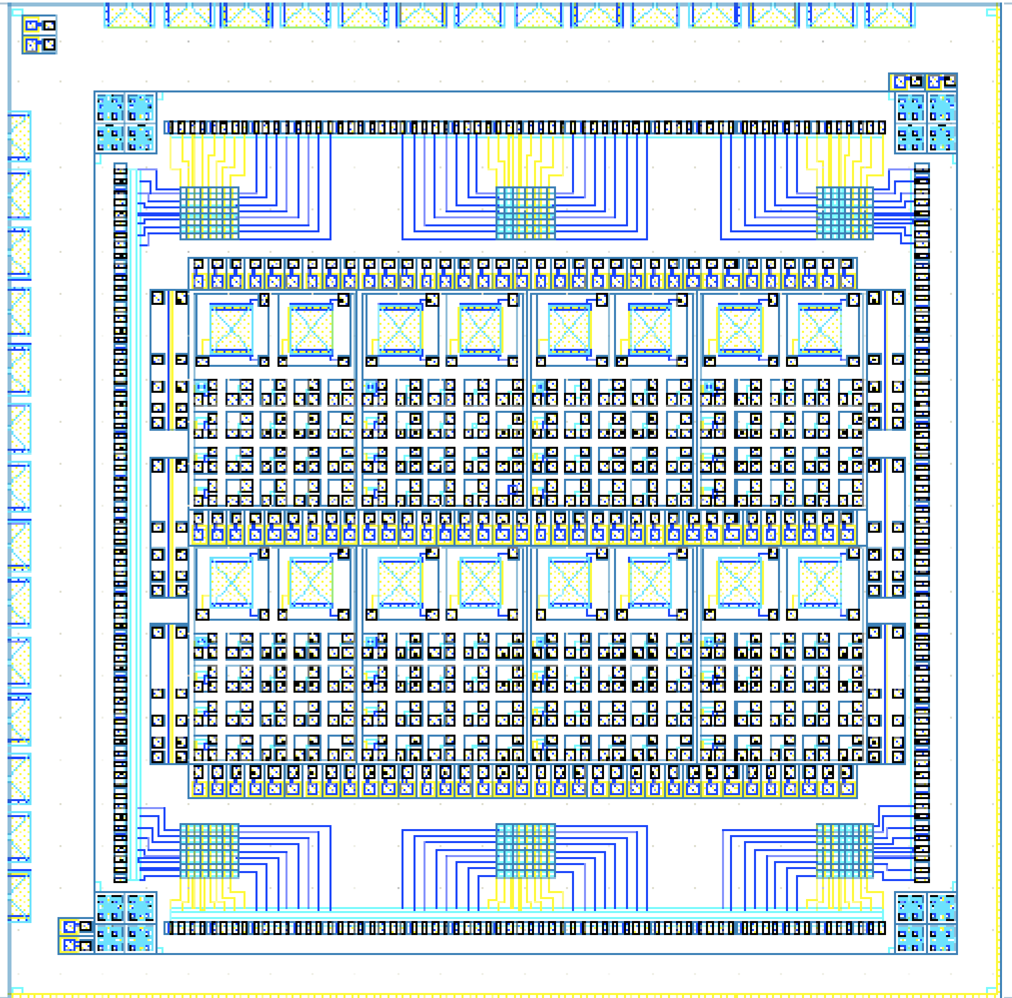
Appendix A

Hybrid Detector Mask Layout

A.1. Entire Wafer Layout



A.2. Sample Device Layout



A.3. Shadow Mask

3 inch (76.2 mm), 0.5 mm thick
20 mm
4 mm
3 mm
1 mm
2 mm
3 mm
Center
4 mm
20 mm
2 mm
2 mm
40 mm
1 mm
18 mm
4 mm
40 mm

Appendix B
TCAD Input Deck

B.1. Mesh Definition

```
TITLE               Si Drift Detector Mesh

COMMENT        Assigning Variables

COMMENT   Bandgap Definition
ASSIGN         NAME=EGSI N.VAL=1.05
ASSIGN         NAME=EV N.VAL=-1
ASSIGN         NAME=EC N.VAL=.7
ASSIGN         NAME=EGaSI N.VAL=@EC-@EV

COMMENT   Device Demension Definitions
ASSIGN         NAME=TCON N.VAL=0.050
ASSIGN         NAME=TSI N.VAL=380
ASSIGN   NAME=TSUBDI N.VAL=.300
ASSIGN         NAME=TOX N.VAL=0.300
ASSIGN      NAME=TBLOCK N.VAL=0.500

ASSIGN         NAME=WL N.VAL=10
ASSIGN         NAME=GTH N.VAL=0.100
ASSIGN         NAME=SDTH N.VAL=0.018


COMMENT        Mesh Generation
MESH          OUT.FILE="SiTFTDetector.msh"
X.MESH         WIDTH=45 N.SPACES=45
Y.MESH         Y.MIN=@GTH
+        Y.MAX=@GTH+@TOX N.SPACES=10
```

```
  Y.MESH         Y.MIN=@GTH+@TOX
  +        Y.MAX=@GTH+@TOX+@TCON N.SPACES=25
  Y.MESH         Y.MIN=@GTH+@TOX+@TCON
  +        Y.MAX=@GTH+@TOX+@TCON+@TSUBDI N.SPACES=10
  Y.MESH         Y.MIN=@GTH+@TOX+@TCON+@TSUBDI
  +        Y.MAX=@GTH+@TOX+@TCON+@TSUBDI+@TSI N.SPACES=50
  Y.MESH    Y.MIN=@GTH+@TOX+@TCON+@TSUBDI+@TSI
  +   Y.MAX=@GTH+@TOX+@TCON+@TSUBDI+@TSI+@TBLOCK N.SPACES=10
  Y.MESH         Y.MIN=@GTH+@TOX+@TCON+@TSUBDI+@TSI+@TBLOCK
  +        Y.MAX=@GTH+@TOX+@TCON+@TSUBDI+@TSI+@TBLOCK+@TCON
N.SPACES=15

  COMMENT        Regions
  +        1:Silicon Substrate, 2:Channel,
  +        3:Bottom Contact, 4:Gate Dielectric
  +        5:Substrate Dielectric
  REGION         NUM=1 Y.MIN=@GTH+@TOX+@TCON
Y.MAX=@GTH+@TOX+@TCON+@TSI SILICON
  REGION         NUM=2 Y.MIN=@GTH+@TOX Y.MAX=@GTH+@TOX+@TCON A-
SILICO
  REGION         NUM=3 Y.MIN=@GTH+@TOX+@TCON+@TSUBDI+@TSI
Y.MAX=@GTH+@TOX+@TCON+@TSUBDI+@TSI+@TBLOCK+@TCON A-SILICO
  REGION         NUM=4 Y.MIN=@GTH Y.MAX=@GTH+@TOX NITRIDE
  REGION         NUM=5 Y.MIN=@GTH+@TOX+@TCON
Y.MAX=@GTH+@TOX+@TCON+@TSUBDI OXIDE

  COMMENT        Electrodes
  +              1:Gate, 2:Bottom Electrode
  +              3:Source, 4:Drain
  ELECTR         NUM=1 Y.MIN=0.0 Y.MAX=@GTH X.MIN=10 X.MAX=35
  ELECTR         NUM=2 Y.MIN=@GTH+@TOX+@TCON+@TSI+@TBLOCK+@TCON
  +
     Y.MAX=@GTH+@TOX+@TCON+@TSUBDI+@TSI+@TBLOCK+@TCON+0.020
X.MIN=0.0 X.MAX=45
```

```
  ELECTR         NUM=3 Y.MIN=@GTH+@TOX+0.025
  +              Y.MAX=@GTH+@TOX+@TCON X.MIN=0.0 X.MAX=15
  ELECTR         NUM=4 Y.MIN=@GTH+@TOX+0.025
  +              Y.MAX=@GTH+@TOX+@TCON X.MIN=30 X.MAX=45

  $$ELECTR NUM=5 X.MIN=0 X.MAX=0 Y.MIN=15 Y.MAX=20
  $$ELECTR NUM=6 X.MIN=45 X.MAX=45 Y.MIN=120 Y.MAX=130

  COMMENT        Doping Specification
  $$PROFILE      P-TYPE Y.MIN=@GTH+@TOX+@TCON
  $$+                       Y.MAX=@GTH+@TOX+@TCON+@TSI UNIFORM
N.PEAK=1.5e10
  PROFILE        N-TYPE Y.MIN=@GTH+@TOX
  +                         Y.MAX=@GTH+@TOX+@TCON
  +                         X.MIN=0.0 X.MAX=15 UNIFORM N.PEAK=1e18
  PROFILE        N-TYPE Y.MIN=@GTH+@TOX
  +                         Y.MAX=@GTH+@TOX+@TCON
  +                         X.MIN=30 X.MAX=45 UNIFORM N.PEAK=1e18
  PROFILE        N-TYPE Y.MIN=@GTH+@TOX+@TCON+@TSI+@TBLOCK
  +                         Y.MAX=@GTH+@TOX+@TCON+@TSI+@TBLOCK+@TCON
UNIFORM N.PEAK=1e18

END
```

B.2. Simulation Input Deck

```
TITLE      Si Hybrid Detector

COMMENT          Simulation Settings
COMMENT          Potential Extraction Mode (ON:1, OFF:0)
ASSIGN           NAME=PEXT N.VAL=0

COMMENT          2D Plot Mode (ON:1, OFF:0)
```

```
ASSIGN          NAME=2DPLOT N.VAL=1

COMMENT         Plot Dark Condition (ON:1, OFF:0)
ASSIGN          NAME=PLOTDARK N.VAL=1

COMMENT         Plot Band Diagrams? (ON:1, OFF:0)
ASSIGN          NAME=PLTBAND N.VAL=1

COMMENT         Setting up Bias Condition
ASSIGN          NAME=BGATE N.VAL=19
ASSIGN          NAME=BDRAIN N.VAL=1
ASSIGN          NAME=BBACK N.VAL=19

CALL       FILE=./SiTFTDetectorMesh.inp
IF              COND=(@2DPLOT=1)
     PLOT.2D    BOUNDARY REGION JUNCTION FILL LABELS CLEAR
     +          TITLE="Si TFT Detector"
     PLOT.2D    BOUNDARY REGION JUNCTION FILL LABELS CLEAR
     +          TITLE="Si TFT Detector TFT Side"
  +   X.MIN=0.0 X.MAX=45.0 Y.MIN=0.0 Y.MAX=@GTH+@TOX+@TCON+@TSUBDI

IF.END




COMMENT    Calculate characteristic for holes/electron

ASSIGN     NAME=PCHR N.VAL=(-0.25-@EV)*LOG(1E22/8E13) PRINT
COMMENT    Generate hole traps.
TRAP  DISTR N.TOT="-(8E13+1E20*EXP(-(@FENER-@EV)/@PCHR))"
```

```
+
      COND="(@FENER<0)&(Y>@GTH)&(Y<@GTH+@TOX+@TCON)&(Y>@GTH+@TOX+@TC
ON+@TSUBDI+@TSI)&(Y<@GTH+@TOX+@TCON+@TSUBDI+@TSI+@TBLOCK+@TCON)"
+   PRINT
+           X.PLOT=0.38 Y.PLOT=4 OUT.FILE=HOLETRAP.IVL
+           TAUN="1E-5" TAUP="1E-6"
ASSIGN      NAME=NCHR N.VAL=(@EC-0.4)*LOG(1E20/1E13) PRINT
COMMENT     Generate electron traps.
TRAP  DISTR N.TOT="(1E13+1E17*EXP((@FENER-@EC)/@NCHR))"
+
      COND="(@FENER>0)&(Y>@GTH)&(Y<@GTH+@TOX+@TCON)&(Y>@GTH+@TOX+@TC
ON+@TSUBDI+@TSI)&(Y<@GTH+@TOX+@TCON+@TSUBDI+@TSI+@TBLOCK+@TCON)"
+   PRINT
+           X.PLOT=0.38 Y.PLOT=4 OUT.FILE=ELECTRAP.IVL
+           TAUN="1E-5" TAUP="1E-6"

COMMENT          Specify Electrode Workfunctions
CONTACT          NUM=1 MOLYBDENUM
CONTACT          NUM=2 ALUMINUM
CONTACT     NUM=3 WORKFUNC=4.5
CONTACT     NUM=4 WORKFUNC=4.5

COMMENT          Specify Optical Parameters
MATERIAL   A-SILICON EG300=@EGaSI
MATERIAL   SILICON EG300=@EGSI

COMMENT          Solving initial conditions
MODELS  CONMOB CONSRH AUGER BGN
SYMB  NEWTON CARR=0
SOLVE   V1=0.0 V2=0.0 V3=0.0 V4=0.0 OUT.FILE="SiTFT.INI"

SYMB        NEWTON CARR=2 ELECTRON HOLES
```

```
IF              COND=(@PLOTDARK=1)
     COMMENT    Dark Current Evaluation
     COMMENT    Electrodes
     +          1: Gate, 2: Bulk Electrode, 3: Source, 4: Drain
     LOG        OUT.FILE="SiTFT.IVL"

    SOLVE V2=0.0
$$   SOLVE V2=0.0 VSTEP=0.1 NSTEP=5 ELEC=2
$$   SOLVE V2=1 VSTEP=1 NSTEP=@BBACK ELEC=2

     SOLVE V3=0.0

     SOLVE V4=0.0 VSTEP=0.1 NSTEP=9 ELEC=4
     SOLVE V4=1
$$   SOLVE V4=1 VSTEP=1 NSTEP=@BDRAIN ELEC=4

     SOLVE V1=0.0 VSTEP=0.1 NSTEP=5 ELEC=1
     SOLVE V1=1 VSTEP=1 NSTEP=@BGATE ELEC=1

     SOLVE OUT.FILE="SiTFTDK.INI"
     LOG        CLOSE

     COMMENT    Transfer Characteristic (Dark)
     PLOT.1D    IN.FILE="SiTFT.IVL" X.AX=V1 Y.AX=I4
     +          POINTS PRINT
     +          TITLE="Transfer Characteristic (Dark)"
     +          OUT.FILE="SiTFTTRNSDK.dat"

     IF         COND=(@2DPLOT=1)
          COMMENT         2D Plots for device estimation
```

```
            PLOT.2D         BOUNDARY REGION JUNCTION LABELS FILL
DEPLETION
            +               TITLE="Potential"
            CONTOUR         POTENTIAL
            $$PLOT.2D       BOUNDARY REGION JUNCTION LABELS FILL
DEPLETION
            $$+             TITLE="Electric Field"
            $$CONTOUR       E-FIELD
      IF.END

      IF          COND=(@PLTBAND=1)
            COMMENT         Potential at Source (Dark)
            LOAD       IN.FILE=SiTFTDK.INI
            PLOT.1D
            +               X.ST=10 X.EN=10 Y.ST=0
Y.EN=@GTH+@TOX+@TCON+@TSI+@TBLOCK+@TCON+@GTH
            +               COND NEG PRINT
            +               TITLE="Band Diagram at Source (Dark)"
            +               OUT.FILE="CONDataAt10um.dat"
            PLOT.1D         X.ST=10 X.EN=10 Y.ST=0
Y.EN=@GTH+@TOX+@TCON+@TSI+@TBLOCK+@TCON+@GTH
            +               VAL UNCH NEG PRINT
            +               OUT.FILE="VALDataAt10um.dat"
            PLOT.1D         X.ST=10 X.EN=10 Y.ST=0
Y.EN=@GTH+@TOX+@TCON+@TSI+@TBLOCK+@TCON+@GTH
            +               QFN UNCH NEG COL=2
            +               OUT.FILE="FermiDataAt10um.dat"

            COMMENT         Potential at Channel (Dark)
            PLOT.1D
            +               X.ST=22.5 X.EN=22.5 Y.ST=0
Y.EN=@GTH+@TOX+@TCON+@TSI+@TBLOCK+@TCON+@GTH
```

```
          +              COND NEG PRINT
          +              TITLE="Band Diagram at Channel (Dark)"
          +              OUT.FILE="CONDataAt22.5um.dat"
          PLOT.1D        X.ST=22.5 X.EN=22.5 Y.ST=0
Y.EN=@GTH+@TOX+@TCON+@TSI+@TBLOCK+@TCON+@GTH
          +              VAL UNCH NEG PRINT
          +              OUT.FILE="VALDataAt22.5um.dat"
          PLOT.1D        X.ST=22.5 X.EN=22.5 Y.ST=0
Y.EN=@GTH+@TOX+@TCON+@TSI+@TBLOCK+@TCON+@GTH
          +              QFN UNCH NEG COL=2 PRINT
          +              OUT.FILE="FermiDataAt22.5um.dat"

          COMMENT        Potential at Channel TFT Side (Dark)
          PLOT.1D
          +              X.ST=22.5 X.EN=22.5 Y.ST=0
Y.EN=@GTH+@TOX+@TCON+@TSUBDI
          +              COND NEG PRINT
          +              TITLE="Band Diagram at Channel TFT Side
(Dark)"
          +              OUT.FILE="CONDataAt22.5um.dat"
          PLOT.1D        X.ST=22.5 X.EN=22.5 Y.ST=0
Y.EN=@GTH+@TOX+@TCON+@TSUBDI
          +              VAL UNCH NEG PRINT
          +              OUT.FILE="VALDataAt22.5um.dat"
          PLOT.1D        X.ST=22.5 X.EN=22.5 Y.ST=0
Y.EN=@GTH+@TOX+@TCON+@TSUBDI
          +              QFN UNCH NEG COL=2 PRINT
          +              OUT.FILE="FermiDataAt22.5um.dat"

          COMMENT        Potential at Drain (Dark)
          PLOT.1D
```

```
          +               X.ST=35 X.EN=35 Y.ST=0
Y.EN=@GTH+@TOX+@TCON+@TSI+@TBLOCK+@TCON+@GTH
          +               COND NEG PRINT
          +               TITLE="Band Diagram at Drain (Dark)"
          +               OUT.FILE="CONDataAt35um.dat"
          PLOT.1D         X.ST=35 X.EN=35 Y.ST=0
Y.EN=@GTH+@TOX+@TCON+@TSI+@TBLOCK+@TCON+@GTH
          +               VAL UNCH NEG PRINT
          +               OUT.FILE="VALDataAt35um.dat"
          PLOT.1D         X.ST=35 X.EN=35 Y.ST=0
Y.EN=@GTH+@TOX+@TCON+@TSI+@TBLOCK+@TCON+@GTH
          +               QFN UNCH NEG COL=2 PRINT
          +               OUT.FILE="FermiDataAt35um.dat"
     IF.END

     COMMENT          Carrier Concentration (Dark)
     PLOT.1D
     +                X.ST=22.5 X.EN=22.5 Y.ST=0
Y.EN=@GTH+@TOX+@TCON+@TSUBDI+@TSI+@TBLOCK+@TCON+@GTH
     +                ELECTRON COL=4 PRINT
     +                LEFT=@GTH+@TOX+@TCON
RIGHT=@GTH+@TOX+@TCON+@TSUBDI+@TSI+@TBLOCK+@TCON+@GTH Y.LOG
     +                TITLE="Electron Concentration (Dark) at 22.5"
     +                OUT.FILE="ELECCAt22.5um.dat"
     PLOT.1D
     +                X.ST=22.5 X.EN=22.5 Y.ST=0
Y.EN=@GTH+@TOX+@TCON+@TSUBDI+@TSI+@TBLOCK+@TCON+@GTH
     +                HOLES COL=3 PRINT
     +                LEFT=@GTH+@TOX+@TCON
RIGHT=@GTH+@TOX+@TCON+@TSUBDI+@TSI+@TBLOCK+@TCON+@GTH Y.LOG
     +                TITLE="Hole Concentration at (Dark) 22.5"
     +                OUT.FILE="HOLECAt22.5um.dat"
```

```
      PLOT.1D
      +                X.ST=35 X.EN=35 Y.ST=0
Y.EN=@GTH+@TOX+@TCON+@TSUBDI+@TSI+@TBLOCK+@TCON+@GTH
      +                ELECTRON COL=4 PRINT
      +                LEFT=@GTH+@TOX+@TCON
RIGHT=@GTH+@TOX+@TCON+@TSUBDI+@TSI+@TBLOCK+@TCON+@GTH Y.LOG
      +                TITLE="Electron Concentration (Dark) at 35"
      +                OUT.FILE="ELECCAt35um.dat"
      PLOT.1D
      +                X.ST=35 X.EN=35 Y.ST=0
Y.EN=@GTH+@TOX+@TCON+@TSUBDI+@TSI+@TBLOCK+@TCON+@GTH
      +                HOLES COL=3 PRINT
      +                LEFT=@GTH+@TOX+@TCON
RIGHT=@GTH+@TOX+@TCON+@TSUBDI+@TSI+@TBLOCK+@TCON+@GTH Y.LOG
      +                TITLE="Hole Concentration (Dark) at 35"
      +                OUT.FILE="HOLECAt35um.dat"
IF.END


COMMENT          Extracting Potential from entire device
IF               COND=(@PEXT=1)
      LOOP       STEPS=46
            ASSIGN     NAME=XPOS N.VAL=0 DELTA=1
            ASSIGN     NAME=CONNAME C.VALUE=CONDat.000 DELTA=1
            ASSIGN     NAME=VALNAME C.VALUE=VALDat.000 DELTA=1
            ASSIGN     NAME=FERNAME C.VALUE=FERMIDat.000 DELTA=1

            PLOT.1D    PRINT CLEAR
            +          X.ST=@XPOS X.EN=@XPOS Y.ST=0
Y.EN=@GTH+@TOX+@TCON+@TSUBDI+@TSI+@TBLOCK+@TCON+@GTH
            +          COND NEG
```

```
          +          OUT.FILE=@CONNAME
          PLOT.1D    PRINT
          +          X.ST=@XPOS X.EN=@XPOS Y.ST=0
Y.EN=@GTH+@TOX+@TCON+@TSUBDI+@TSI+@TBLOCK+@TCON+@GTH
          +          VAL UNCH NEG
          +          OUT.FILE=@VALNAME
          PLOT.1D    PRINT
          +          X.ST=@XPOS X.EN=@XPOS Y.ST=0
Y.EN=@GTH+@TOX+@TCON+@TSUBDI+@TSI+@TBLOCK+@TCON+@GTH
          +          QFN UNCH NEG COL=2
          +          OUT.FILE=@FERNAME
     L.END
IF.END

END
```

Appendix C

OpenGateCollabration Monte Carlo Simulation Macro

C.1. Main Macro

```
# Visualization
/vis/open OGLSX
/vis/viewer/reset
/vis/viewer/set/viewpointThetaPhi 60 120
/vis/viewer/zoom 1
/vis/viewer/set/style surface
/vis/drawVolume
/tracking/storeTrajectory 1
/vis/scene/endOfEventAction accumulate -1
/vis/viewer/update

# Settig up Materials
/gate/geometry/setMaterialDatabase ./GateMaterials.db

# World
/gate/world/geometry/setXLength 7.62 cm
/gate/world/geometry/setYLength 7.62 cm
/gate/world/geometry/setZLength 3.0 mm
/gate/world/setMaterial Air
/gate/world/vis/forceWireframe
/gate/world/vis/setColor white

# Detector Definition
# Setting up SiHDetector System(scanner)
/gate/world/daughters/name scanner
/gate/world/daughters/insert cylinder
/gate/scanner/setMaterial Silicon
```

```
/gate/scanner/geometry/setRmin 0 cm
/gate/scanner/geometry/setRmax 3.81 cm
/gate/scanner/geometry/setHeight 0.381 mm
/gate/scanner/placement/setTranslation 0. 0. 1. mm
/gate/scanner/vis/forceWireframe
/gate/scanner/vis/setColor yellow
/gate/scanner/describe

# Detector Pixel
/gate/scanner/daughters/name Pixel
/gate/scanner/daughters/insert box
/gate/Pixel/setMaterial Silicon
/gate/Pixel/geometry/setXLength 0.250 mm
/gate/Pixel/geometry/setYLength 0.250 mm
/gate/Pixel/geometry/setZLength 0.381 mm
/gate/Pixel/placement/setTranslation 0. 0. 0. mm
/gate/Pixel/vis/setColor red
/gate/Pixel/describe

# Isotope Source Mount(Phantom)
/gate/world/daughters/name phantom
/gate/world/daughters/insert box
/gate/phantom/setMaterial Air
/gate/phantom/geometry/setXLength 2.54 cm
/gate/phantom/geometry/setYLength 2.54 cm
/gate/phantom/geometry/setZLength 0.001 mm
/gate/phantom/placement/setTranslation 0. 0. 0. mm
/gate/phantom/vis/setColor blue
/gate/phantom/vis/forceWireframe

# Attaching Sensitive Sensors
/gate/Pixel/attachCrystalSD
```

```
/gate/phantom/attachPhantomSD

# Digitizer
/gate/digitizer/Singles/insert adder
/gate/digitizer/Singles/insert readout
/gate/digitizer/Singles/readout/setDepth 3

# Physics
/control/execute ./SiHDet_Physics.mac

# Initialize
/gate/run/initialize

# Source Definition
/control/execute ./SiHDet_Source.mac

# Output format
/gate/output/root/enable
/gate/output/root/setFileName SiHDet
/gate/output/root/setRootHitFlag 1
/gate/output/root/setRootSinglesFlag 1
/gate/output/root/setRootSinglesReadoutFlag 1

# Simulation profile
/gate/application/setTimeSlice     1.  s
/gate/application/setTimeStart     0.  s
#/gate/application/setTimeStop      1.  s
/gate/application/setTimeStop      1000.  s

# Start the Acquisition
/gate/application/start
```

C.2. Source (Iron 55) Definition

```
#######################################
#  SiHDet Source definition           #
#######################################
# The data came from 4 year old Fe-55 #
# source with 100 uCi, yeilding 27 uCi#
# as of April 2014.                   #
#######################################
/gate/source/addSource Fe55
/gate/source/Fe55/setActivity 999000.0 Bq
/gate/source/Fe55/gps/particle gamma
/gate/source/Fe55/gps/energytype Mono
/gate/source/Fe55/gps/monoenergy 5.8 keV
/gate/source/Fe55/gps/angtype iso
/gate/source/Fe55/gps/type Plane
/gate/source/Fe55/gps/shape Rectangle
/gate/source/Fe55/gps/halfx 1.27 cm
/gate/source/Fe55/gps/halfy 1.27 cm
/gate/source/Fe55/gps/centre 0 0 0 cm
/gate/source/Fe55/visualize 250000 green 0.5
/gate/source/list
/gate/source/Fe55/gps/confine phantom
```

C.3. Physics Definition

```
#######################################
#  SiHDet Physics Definition          #
#######################################

/gate/physics/setEMin 0.1 keV
```

```
/gate/physics/setEMax 100 keV

/gate/physics/addProcess PhotoElectric gamma
/gate/physics/processes/PhotoElectric/setModel StandardModel

/gate/physics/addProcess Compton gamma
/gate/physics/processes/Compton/setModel StandardModel

/gate/physics/addProcess RayleighScattering gamma
/gate/physics/processes/RayleighScattering/setModel PenelopeModel

/gate/physics/addProcess GammaConversion
/gate/physics/processes/GammaConversion/setModel StandardModel
```

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