Top-Gate Nanocrystalline Silicon Thin Film Transistors

by

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AUTHOR'S DECLARATION

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

Thin film transistors (TFTs), the heart of highly functional and ultra-compact active-matrix (AM) backplanes, have driven explosive growth in both the variety and utility of large-area electronics over the past few decades. Nanocrystalline silicon (nc-Si:H) TFTs have recently attracted attention as a high-performance and low-cost alternative to existing amorphous silicon (a-Si:H) and polycrystalline silicon (poly-Si) TFTs, in that they have the strong potentials which a-Si:H (low carrier mobility and poor device stability) and poly-Si (poor device uniformity and high manufacturing cost) counterparts do not have. However, the current nc-Si:H TFTs expose several challenging material and devices issues, on which the dissertation focuses.

In our material study, the growth of gate-quality SiO_2 films and highly conductive nc-Si:H contacts based on conventional plasma-enhanced chemical vapor deposition (PECVD) is systematically investigated, which can lead to high performance, reproducibility, predictability, and stability in the nc-Si:H TFTs. Particularly to overcome a low field effect mobility in the p-channel transistors, the possibility of $B(CH_3)_3$ as an alternative dopant source to current B_2H_6 is examined. The resultant p-doped nc-Si:H contacts demonstrate comparable performance to the state of the art with the maximum dark conductivity of 1.11 S/cm over 70% film crystallinity.

Based on the highest-quality SiO_2 and nc-Si:H contacts developed, complementary (n- and p-channel) top-gate nc-Si:H TFTs with a staggered source/drain geometry are

designed, fabricated, and characterized. The n-channel TFTs demonstrate a threshold voltage V_{Tn} of 6.4 V, a field effect mobility of electrons μ_n of 15.54 $cm^2/V \cdot s$, a subthreshold slope S of 0.67 V/decade, and an on/off current ratio I_{on}/I_{off} of 10^5, while the corresponding p-channel TFTs exhibit V_{Tp} of -26.2 V, μ_p of 0.24 $cm^2/V \cdot s$, S of 4.72 V/ decade, and I_{on}/I_{off} of 10^4. However, the TFTs show significant non-ideal behaviors that considerably limit device performance: high leakage current in the off-state, transconductance degradation under high gate bias, and threshold voltage instability in time.

Quantitative insight into each non-ideality is provided in this research. Our study on the off-state conduction in the nc-Si:H TFTs reveals that the responsible mechanism for high leakage current, particularly at a high bias regime, is largely due to Poole-Frenkel emission of trapped carriers in the reverse-biased drain depletion region. This could be effectively suppressed by proposed offset-gated structure without compromising the on-state performance. A numerical analysis of the transconductance degradation shows that the parasitic resistance components that are present in the nc-Si:H TFTs strongly degrade transconductance and thus a field effect mobility. Correspondingly, strategies for reduction in parasitic resistance of the TFT are presented. Lastly, the threshold voltage shift in the nc-Si:H TFT is attributed to the flatband voltage shift, which is mainly due to charge trapping in the PECVD SiO_2 gate dielectric.

Material and device study, and physical insight into non-ideal behaviors in the top-gate nc-Si:H TFTs reported in the dissertation constitute an arguably important step towards

monolithic integration of pixels and peripheral driving circuits on a versatile active-matrix TFT backplane for high-performance and low-cost large-area electronics. However, the gate dielectric and the highly doped nc-Si:H contacts, still imposing considerable challenges, may require entirely new approaches.

Acknowledgements

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To My Wife, Yoo Mi Lee, for her unconditional love and sacrifice

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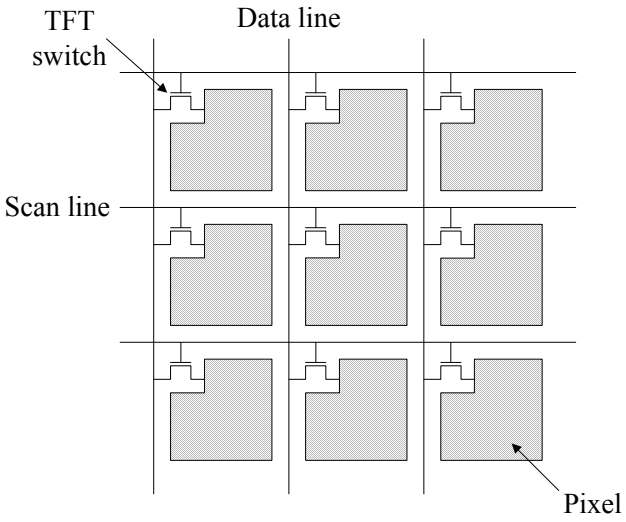
Chapter 1
Introduction

1.1 Research Motivation

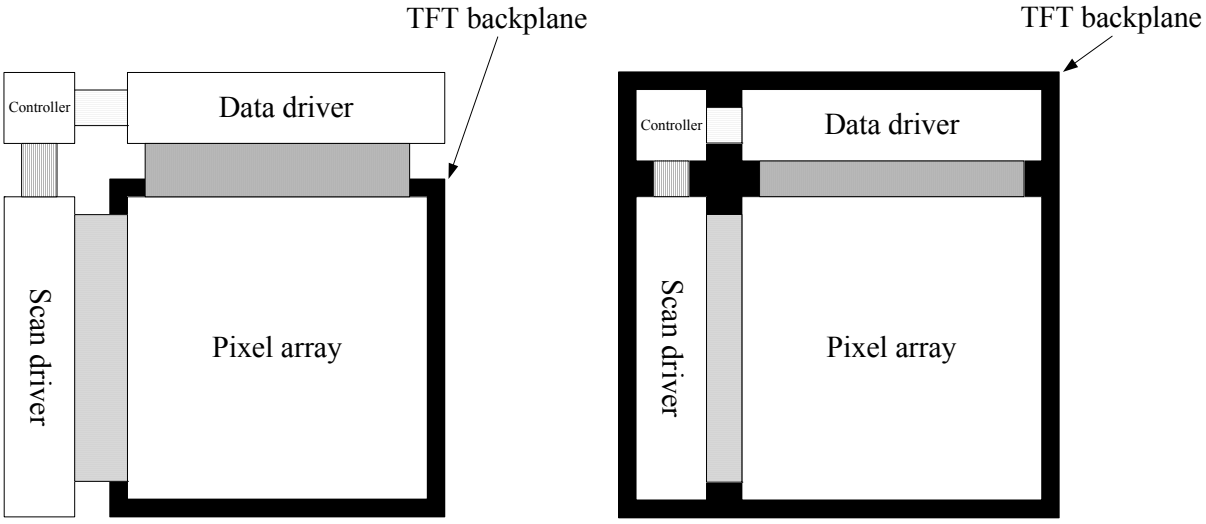
Active-matrix backplanes are essential to the various applications of large-area electronics, currently including liquid crystal displays (LCDs) [1], solar cells [2], and sensors [3], and also showing tremendous promise for emerging applications such as organic light-emitting diode (OLED) displays [4], electronic skins [5], radio-frequency identification (RFID) tags [6], and much more. A key element here is a thin film transistor in each pixel of the backplane as depicted in Fig. 1.1 (a), containing intelligence capability of addressing, amplification, and multiplexing of an information signal. In traditional a-Si:H TFT technology, an array of pixels is driven by higher performance circuits externally connected to the backplane as illustrated in Fig. 1.1(b). However, total integration of pixels and peripheral drivers as in poly-Si TFT technology presented in Fig. 1.1(c) is desirable not only for high functionality, ultra-compactness, and versatility, but also for low packaging cost and high manufacturing yield. This requires that TFTs based on non-crystalline silicon

technology should perform comparably to complementary metal-oxide-semiconductor field effect transistors (MOSFETs) made of crystalline silicon (c-Si).

Since a-Si:H TFTs, the current industrial standard, suffer from low carrier mobility, poor CMOS capability, and poor device stability, poly-Si TFTs fabricated by laser crystallization of a-Si:H have been developed to achieve these [7]. However, their industrial implementation over large area is faced with high manufacturing cost, complex fabrication process, and poor device uniformity [8]. Recently, there has been growing interest in nc-Si:H TFTs in view of their potentially high performance and low cost [9] as compared in Table 1.1. Nanocrystalline silicon has many useful advantages over a-Si:H, one being that it is expected to have increased stability due to its lower hydrogen concentration [10]. One of the most important advantages, however, is that it can have higher mobility due to the presence of silicon crystallites [11]. It also shows increased doping efficiency [12]. Additionally, device non-uniformity in the nc-Si:H TFTs is expected to be less significant compared to the poly-Si counterparts due to fine but uniformly-distributed silicon grains in nc-Si:H. Although the nc-Si:H TFTs currently may not attain the mobility that the poly-Si TFTs can, they are lower cost and easier to fabricate because the TFT channel layer can be deposited directly from the glow discharge of silane highly diluted in hydrogen [9]. This can enable us to switch the same fabrication lines which today produce the a-Si:H TFTs to nc-Si:H TFT production without additional investments, for instance, laser annealing or high temperature process required in poly-Si TFT fabrication. This is the motivation that we have actively been pursuing TFT technology based on nc-Si:H [13],[14].



(a)



(b) (c)

Fig. 1.1. (a) Schematic of active-matrix TFT backplane structure, and a-Si:H versus poly-Si backplane technology: (b) in the a-Si:H case, driving circuits are connected externally, while they are integrated on the TFT backplane (c) in the poly-Si case.

Table 1.1. Comparison of different silicon TFT technologies [15].

	a-Si:H TFT	poly-Si TFT	nc-Si:H TFT	
Status	Mature	Development	Research	
Structure	Bottom-gate	Top-gate	Top-gate	Bottom-gate
CMOS capability	Poor	Good	Good	Unknown
Mobility ($cm^2/V \cdot s$)	~0.1	~100	~40	~3
Uniformity	Good	Poor	Expected good	Expected good
Stability	Poor	Good	Expected good	Good
Cost	Low	High	Low	Low

1.2 Applications

In the following two subsections, we briefly describe two emerging applications of active-matrix TFT backplanes: OLED displays and RFID tags.

1.2.1 Organic Light-Emitting Diode Displays

OLED displays have been attracting much attention in recent years [16],[17]. They are lightweight, thin, and compact, since they do not require a backlight unit, polarizers, color filters, and alignment layers as LCDs do. They do not also exhibit limitations in

viewing angle as in LCDs. The response time of OLEDs is much faster (typically in the range of 10^{-9} sec) than that of twisted nematic (TN) LCD (~2 msec now being commonplace) [18].

Figs. 1.2(a) and (b) show the schematic diagram of OLED energy band and the simplified structure of the OLED displays, respectively [19]. The operational principle is simple; electrons are injected into the lowest unoccupied molecular orbital (LUMO) from the cathode having a low work function (typically Ca), while holes into the highest occupied molecular orbital (HOMO) through the anode with a high work function (transparent indium-tin-oxide, ITO). They recombine in the organic layer generating excitons which then decay radiately, producing the light. Since ITO deposition by sputtering damages the organic layer [19], ITO is first deposited on the glass substrate. This is followed by successive evaporation of the organic layer and the top electrode. Here, the solvents used in photolithography process can dissolve the organic layer, so the top electrode is usually patterned by lift-off process.

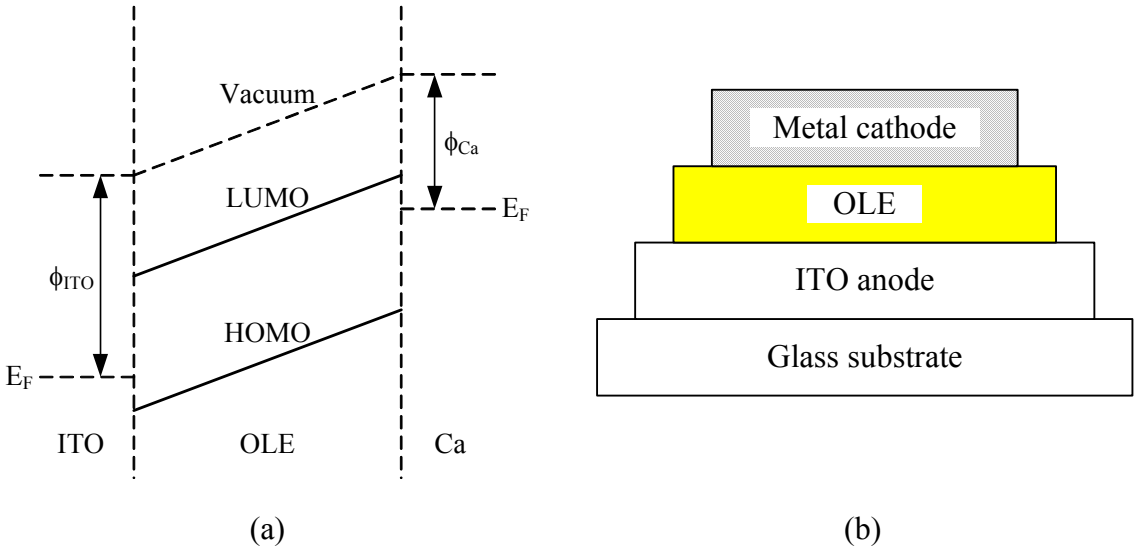


Fig. 1.2. (a) Schematic diagram of OLED energy band, and (b) simplified structure of the OLED displays.

In Fig. 1.3, two basic pixel configurations of the AMOLED displays are presented, along with the corresponding emitting structures. Here, the row lines are sequentially selected to turn on 'select' TFTs (denoted by T_1 in the figure) over a frame period. When one line is addressed, a voltage signal is transferred through the column lines to the gate of driver TFTs (denoted by T_2 in the figure). This signal is stored when the select TFT is switched off. Here, the leakage current in the select TFTs is critical. If it is too high, the signal cannot be maintained until the next line is selected. A storage capacitor can be added in each pixel to compensate this, but a sacrifice in pixel aperture ratio is inevitable in this case.

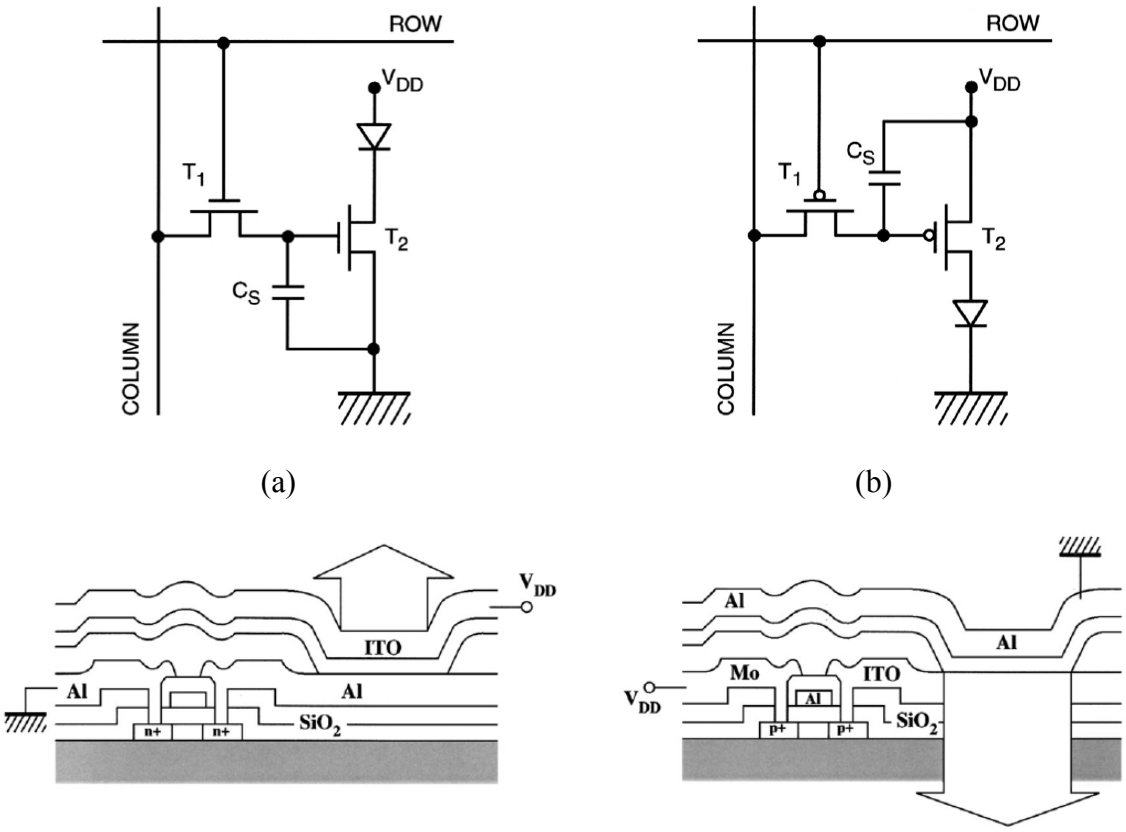


Fig. 1.3. Basic pixel configurations of AMOLED displays: (a) with n-channel and (b) with p-channel TFTs, and the corresponding emitting structures: (c) top-emitting and (d) bottom-emitting [19].

It should be emphasized that there are several constraints in OLED pixel structure to obtain good image quality. First, the OLED must be fed with a constant current, which implies that the diode has to be connected to the drain terminal of the driver TFT operating in the saturation regime [4]. By doing so, voltage variations across the OLED (accordingly, V_{DS}

of the driver TFT) do not affect the current passing through it, since $I_{DS,sat} \sim (V_{GS} - V_T)^2$. Next, the anode of the OLED is ITO as mentioned earlier. These restraints enable only two possible configurations of pixel architecture as shown in Fig. 1.3: (a) with n-channel and (b) with p-channel TFTs. If n-channel TFTs are used, ITO should be sitting on top of the organic layer (top-emitting structure). However, in this case, ITO sputtering damages the organic layer as mentioned before, and oxygen penetration from ITO into the organic layer degrades the lifetime of the OLED [19]. Therefore, p-channel TFTs with bottom-emitting structure depicted in Figs. 1.3(b) and (d) are preferred in the OLED displays. As hole mobility in a-Si:H TFTs is extremely low (< 10^{-2} $cm^2/V \cdot s$) [20], poly-Si TFTs are the only possible candidate for the OLED pixel.

Assuming that the n-channel a-Si:H TFTs with top-emitting structure are possible, there is still a remaining issue, i.e., the threshold voltage shift in the a-Si:H TFTs under prolonged bias stress [21]. The a-Si:H TFTs have been able to be used in AMLCDs, since the pixel duty cycle is short and the line addressing can be inverted during the TFT off-state to compensate the threshold voltage shift. However, in OLEDs, the situation is completely different because the duty cycle of the driver TFTs, being in the on-state during most of the frame period, is almost unity. However, the poly-Si TFTs also have a serious problem, i.e., device non-uniformity over large area, as mentioned in Section 1.1.

1.2.2 Radio Frequency Identification

In recent years, automatic identification procedures have become popular in many industries. The application area is not only limited to current passports, transportation payments, product tracking, and animal identification, but will also be extended to telemetry, patent identification, security, and the replacement of traditional barcodes in the near future [22]. RFID is an automatic identification method, relying on storing and remotely retrieving data using devices called RFID tags or transponders as shown in Fig. 1.4.

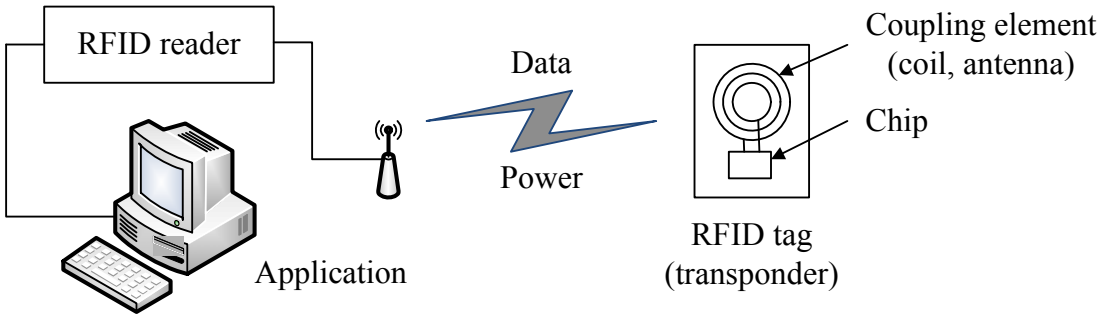


Fig. 1.4. Main components of the RFID system [22]: the RFID tag represents a data-carrying device, normally consisting of a coupling element and a microchip.

RFID tags are generally classified into two types: active and passive tags. Active tags have their own internal power source which is used to power ICs and broadcast the signal to the reader [22]. However, passive tags require no internal power supply. The minute

electrical current induced in the coil by the incoming RF signal provides enough power for ICs in the tag to power up and transmit a response. Philips demonstrated a 13.56 MHz tag using organic TFTs in 2006 [6]. However, complementary devices are required for the integration of microprocessors and memories in a tag, which is out of reach of the organic TFTs because they are inherently p-type [23].

1.3 Objectives of the Doctoral Research

The dissertation focuses on the following material and device issues in the development of high-performance and low-cost nc-Si:H TFTs for large-area electronics.

- Gate-quality SiO_2 dielectric: the first issue is the development of high-quality PECVD SiO_2 for a TFT gate dielectric. The quality of SiO_2 films grown by conventional PECVD at low temperature is generally poor, and the leakage current across the oxide and hysteresis associated with charge trapping in the oxide cause irreproducibility, unpredictability, and instability in TFT performance. Therefore, producing gate-quality SiO_2 films has been regarded as one of the most challenging issues in TFT research.
- Highly conductive nc-Si:H contacts: the capability to prepare heavily doped n- and p-type nc-Si:H contacts is critical for complementary operation of the TFTs. In the TFTs, these layers are required to provide sufficiently low series resistance (high on-current) and to block the injection of carriers with the opposite sign (low off-current) so as to achieve

high on/off current ratio. Especially in nc-Si:H, much lower conductivity (~1 S/cm) achieved by p-doping than that (> 20 S/cm) obtained by n-doping must be addressed.

- Complementary nc-Si:H TFTs: the development of high-performance n- and p-channel nc-Si:H TFTs is the third area of emphasis in the dissertation. While the n-channel mobility over 40 $cm^2/V \cdot s$ is reported, the p-channel counterpart is quite low (~0.2 $cm^2/V \cdot s$), which is unsuitable for CMOS operation.
- Non-idealities in TFT behavior: lastly, non-idealities generally observed in the top-gate nc-Si:H TFTs are the third issue of study. It is desirable that the TFTs provide high field effect mobility and low leakage current along with high electrical stability. However, deviations from the ideality are usually observed in the TFTs. Therefore, physical insight into their mechanisms is imperative for further improvement in transistor performance, which can aid the design of the TFTs to maximize device performance. In this research, the three most important non-idealities are discussed. These are:
    - High leakage current in the off-state,
    - Transconductance degradation under high gate bias,
    - Threshold voltage shift in time.

1.4 Organization of the Dissertation

The work here introduces the use of a conventional parallel-plate PECVD system with a 13.56 MHz RF power source. Indeed, PECVD has been the only successful large area

and low temperature method with high throughput for the growth of the gate dielectric and the channel layer for TFT production. In this work, the process temperature is kept below 260°C in consideration not only of the current glass substrates such as Corning 1737 but also of the future employment of plastic substrates such as Kapton.

Chapter 2 starts with the formation of gate-quality SiO_2 films. The physical and electrical properties of PECVD SiO_2 are presented for the optimization of growth process for TFT gate applications. The effects of N_2O plasma pre-treatment and post-metallization thermal annealing are also discussed for further improvement in the dielectric properties.

Chapter 3 describes the evolution of structural and electronic properties in the nc-Si:H material with doping in order to overcome a low carrier mobility in the highly p-doped films. Here, we examine the possibility of $B(CH_3)_3$ as an alternative p-type dopant source for the growth of high-quality contact layers by investigating the film crystallinity, grain size, dark conductivity, and activation energy of the films.

In Chapter 4, the structure, fabrication process, and electrical characteristics of n- and p-channel nc-Si:H TFTs are presented. Here, top-gate structure is employed to take advantage of the highest carrier mobility available at the top of the nc-Si:H films. Device parameters governing TFT performance are extracted. The output characteristics of the TFTs are described to evaluate source/drain contact integrity. The transfer characteristics along with gate leakage properties are presented to discuss the effect of the leakage current on transistor performance. The impact of TFT leakage current is emphasized by implementing

inverter circuits. Finally, the influence of post-fabrication thermal annealing on device performance is investigated.

In Chapter 5 is described one of the major goals in the dissertation. The off-state conduction mechanisms underlying high leakage current in the top-gate nc-Si:H TFTs are quantitatively investigated. Offset-gated structure is proposed and examined to suppress the leakage current based on the studied mechanisms. The effect of channel compensation doping on TFT performance, which is also introduced to reduce the leakage current, is discussed. The transconductance degradation in the TFTs, which significantly limits the on-state performance, is analyzed numerically using device simulations. Finally, the threshold voltage shift associated with SiO_2 charge tapping is studied.

Chapter 6 finally concludes the implications of this research and suggests future work related to this work.

Chapter 2
SiO_2 Gate Dielectric

In this chapter, we report the preparation, characterization, and optimization of gate-quality SiO_2 grown by conventional PECVD at low temperature. Strong emphasis is placed on the leakage current across the oxide and hysteresis associated with oxide charge trapping.

2.1 Introduction

Nature has endowed the silicon microelectronics industry with an excellent material, silicon dioxide (SiO_2, referred to as simply oxide), whose properties are summarized in Table 2.1 [24]. SiO_2 is not only native to silicon but also the only stable phase on silicon, and with it forms a low defect density interface. It also has high resistivity (~10^{15} Ω·cm), excellent dielectric strength (~10 MV/cm), and a large band gap (~9 eV). These properties of SiO_2 are ascribable to the microelectronics revolution. Indeed, other semiconductors such as Ge or GaAs were not the first choice of the semiconducting material, mainly due to their lack of a stable native dielectric and a low defect interface. Indeed, the Si/SiO_2 interface, which forms

an integral part of MOSFETs, is arguably the world's most economically and technologically important materials interface.

The quality of dielectrics depends strongly on the temperature of formation. In crystalline silicon MOSFET technology, oxide is generally grown by thermal oxidation, a high temperature (~1000°C) process that uses O_2 (dry) or H_2O (wet) ambient [25]. The elevated temperature provides the sufficient energy for reactions to occur between the silicon surface and gaseous oxygen atoms, and the resultant oxide typically has an exact stoichiometric ratio (SiO_2). However, TFTs fabricated on either glass or plastic substrates must use gate dielectrics grown at low temperature. This imposes another challenge, since a reduction in processing temperature causes deterioration in the device characteristics due to the poor properties of the dielectrics [26],[27].

Table 2.1. Selected properties of thermal SiO_2 [24].

Low interfacial (Si/SiO_2) defect density (~10^{10} $cm^{-2}\cdot eV^{-1}$, after H_2 passivation)
Energy gap: 9 eV
Resistivity ~10^{15} $\Omega\cdot cm$
Dielectric breakdown field ~10 MV/cm
Dielectric constant = 3.9

At low temperature, oxide has been formed by LPCVD [28], PECVD [26], sputtering [29]. LPCVD requires temperature over 350°C, which is incompatible with the plastic substrates currently available. Sputtering can be done at room temperature, but the interface quality is typically poor and impurities from the chamber walls can easily be incorporated into the films. Low-temperature PECVD SiO_2 in these contexts has been developed. The major advantage of the PECVD technique is that highly active species such as ions, radicals, and neutrals generated by glow discharge promote deposition process at lower temperature, thus minimizing thermal budget required to film deposition [26]. High density plasma (HDP) processing such as electron cyclotron resonance (ECR) [30] and inductively coupled plasma (ICP) [31] are also good choices of attaining high-quality interface at low temperature, but it is difficult to achieve uniform ion density over large area [32].

PECVD silicon nitride (SiN_x, referred to as simply nitride) has been used for a-Si:H TFTs. This is because differences in band-bending and alignment at the a-Si:H/dielectric interface favor the nitride dielectrics, since the unbiased interface is either flat or in slight accumulation, as compared to the SiO_2 dielectric which has depletion regions in a-Si:H, therefore causing a larger threshold voltage [33]. However, SiO_2 is preferred for nc-Si:H TFTs because it provides a higher field effect mobility [9],[34]. Nevertheless, it should be noted that various types of traps and charges exist in the bulk SiO_2 film and at the Si/SiO_2 interface: mobile charges Q_m, bulk trap charges Q_{ot}, fixed charges Q_f, and interface trap charges Q_{it} [35]. These charges have a profound effect on the characteristics and performance

of the TFTs by inducing equivalent negative charges in the channel, which requires negative gate bias to achieve flatband condition V_{FB} as depicted in Fig. 2.1.

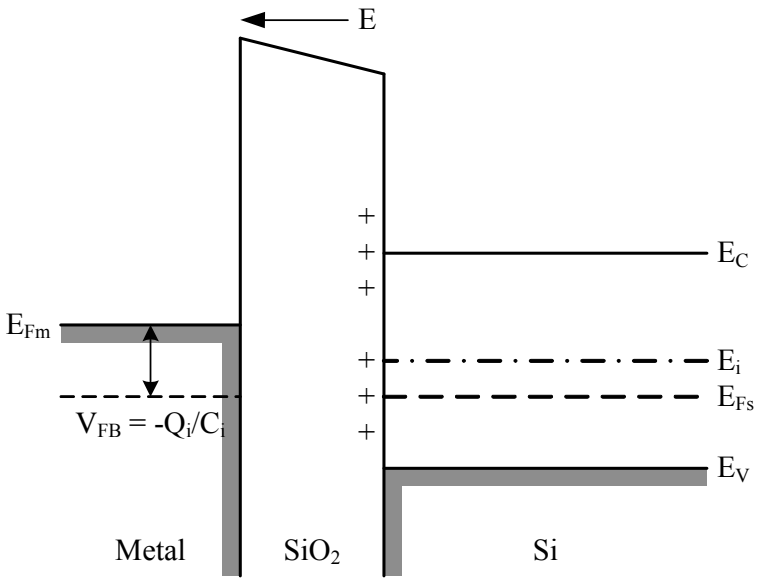


Fig. 2.1. Effect of trap charges in the bulk SiO_2 and at the Si/SiO_2 interface: an equivalent sheet of positive charges Q_i at the interface induces an equivalent negative charge in the silicon channel, which requires negative gate bias to achieve the flatband [35].

In addition, PECVD SiO_2 contains much hydrogen, especially one grown at low temperature. H is bonded with the Si–O network as hydride (Si–H), silanol (Si–OH), and water (H_2O), and can be incorporated not only during film deposition [36] but also by post-deposition exposure to the atmospheric moisture [37]. Although the relative concentration of

hydrogen in the three bonding sites depends on deposition conditions, the total concentration varies usually between 2 and 9 at. % [25], which is much higher than that in thermal SiO_2. These hydrogen-related contaminants yield a silicon-rich film (i.e., SiO_x, $x < 2$) [27], and therefore, the oxygen vacancies are inevitable. This center forms a neutral hole trap, which becomes positive by losing the non-bonding electron, while an unpaired electron of a silicon atom (i.e., a dangling bond) acts as an electron trap because it easily captures an electron to complete the covalent bond as illustrated in Fig. 2.2. These hydrogen atoms have been attributed to cause the leakage current across the oxide and the flatband voltage shift in the TFTs [38]. However, good-quality oxides have been obtained from the glow discharge of a mixture of SiH_4 and N_2O highly diluted in He at a substrate temperature of 275°C [38]. It is reported that He leads to the reduction of unwanted Si–H and Si–OH bonds, thus enhancing the tendency toward a stoichiometric composition [38]. In addition, high He dilution can provide good film uniformity for low growth rate process, which will be discussed later, by maintaining a sufficient gas residence time in the PECVD reactor [39].

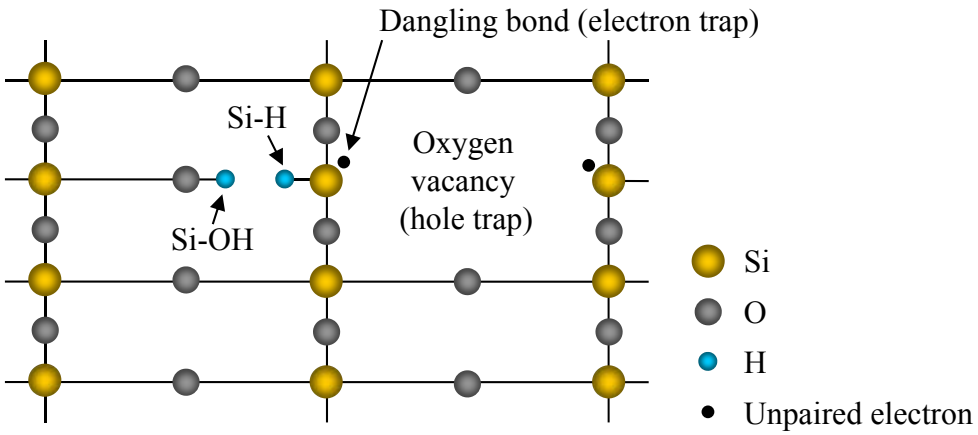


Fig. 2.2. Schematic diagram of PECVD SiO_2 network showing electron and hole trapping [38].

2.2 Film Deposition and Characterization

Since the existing oxide deposition recipe in our group listed in Table 2.2 yielded an electrically leaky film [40], our first aim is to improve the bulk properties of the PECVD oxide. Indeed, when the oxide deposited by the existing recipe was incorporated into the TFT, the device was destroyed under the drain bias of 10 V during test as shown in Fig. 2.3.

Table 2.2. Existing process parameters for PECVD SiO_2 deposition.

Process parameter	Value
Substrate temperature (°C)	260
RF power (W)	150
Pressure (mTorr)	100
He flow rate (sccm)	500
N_2O-to-SiH_4 flow ratio (N_2O/SiH_4)	25 (N_2O: 100 sccm, SiH_4: 4 sccm)

The starting point for the experiment is to keep the deposition process in a low growth rate regime (~10 nm/min). Indeed, a deposition rate much lower than that used in conventional PECVD process (~50 nm/min) has been reported to be crucial in obtaining the gate-quality SiO_2 films [26]. In our experiments, the oxide films were deposited on 3-inch crystalline silicon wafers. All substrates were cleaned using standard RCA process followed by a HF dip to remove a native oxide from the silicon surface prior to film deposition. Fig. 2.4 shows a conventional PECVD system (PlasmaTherm 790 Series) with 14 × 14 in^2 parallel-plate electrodes (1-inch separation between electrodes) used in film deposition. The physical and leakage properties of the oxide films were studied while the RF power, pressure, He flow rate, and N_2O/SiH_4 were varied with 3 levels as summarized in Table 2.3. The substrate temperature was maintained at 260°C during deposition.

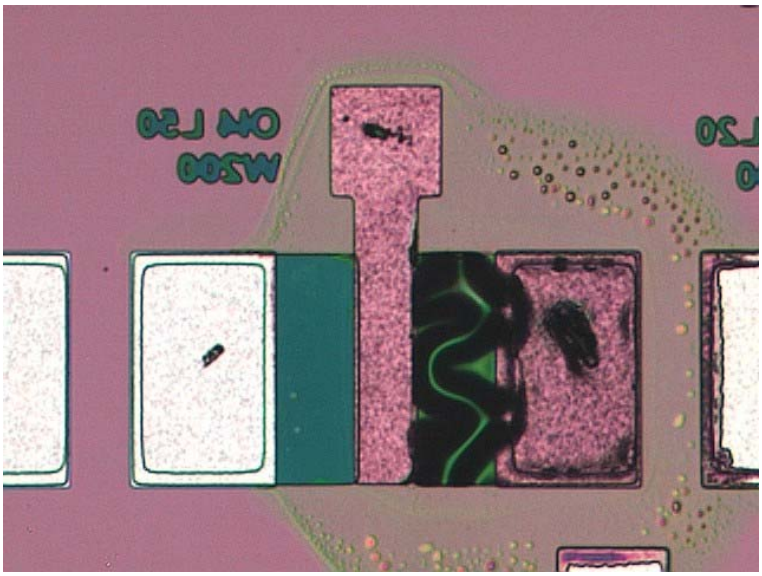


Fig. 2.3. Optical micrograph of a destroyed TFT under the drain bias of 10 V due to the poor SiO_2 gate dielectric.

Table 2.3. Process parameters and their selected levels for the optimization of SiO_2 deposition.

Process parameter	Level		
	0	1	2
RF power (W)	100	125	150
Pressure (mTorr)	100	450	800
He flow rate (sccm)	300	400	500
N_2O/SiH_4	25	50	100

The growth rate was calculated from the film thickness measured with a Dektak 8 surface profiler. The refractive index was measured at wavelengths ranging from 400 to 750 nm using a WVASE32 spectroscopic ellipsometer. The film composition was studied from infrared absorption spectra measured in the range from 400 to 4000 cm^{-1} by a Shimadzu 8400S FTIR and from photoemission spectra by VG Scientific ESCALab 250 with a 1253.6 eV Mg-Kα X-ray source. For electrical characterizations including current-voltage (I-V) and capacitance-voltage (C-V) measurements, MOS capacitors were fabricated on p-type crystalline silicon wafers with a resistivity of ~10 Ω·cm. Here, 200-nm thick SiO_2 was grown, which is the same thickness as that of the gate dielectric in the fabricated TFTs. Then, 300-nm thick Al gate was deposited onto the SiO_2 film through a shadow mask shown in Fig. 2.5 using an Edwards E306A RF sputtering system. The I-V characteristics were measured with a ramp rate of 1 V/s by a Keithley 4200 semiconductor characterization system connected to a Cascade 11000 probe station. The C-V data were taken using an Agilent 4284A LCR meter. All of the measurements were carried out at room temperature in a dark and dry environment.

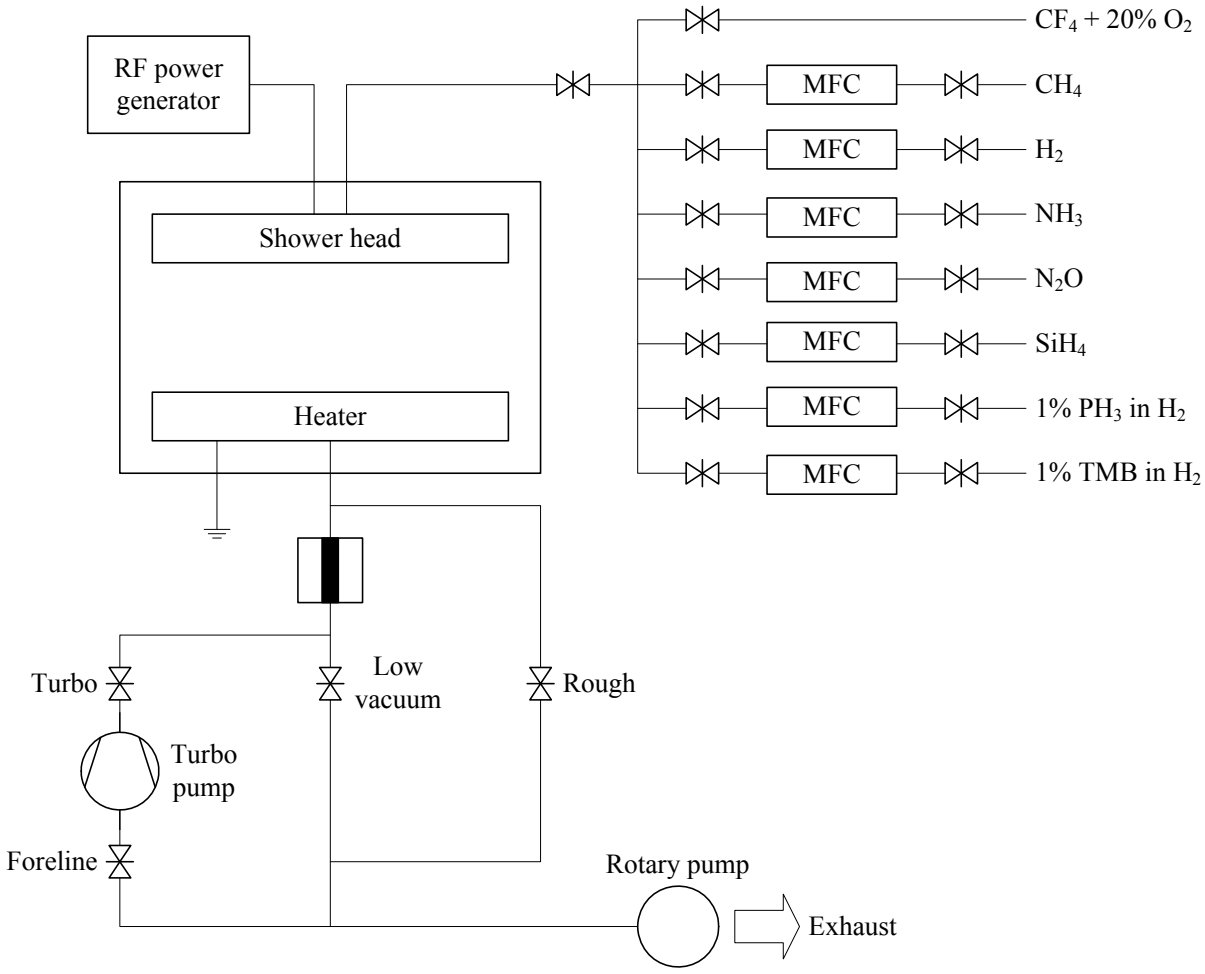


Fig. 2.4. Schematic diagram of the PECVD system used in this research.

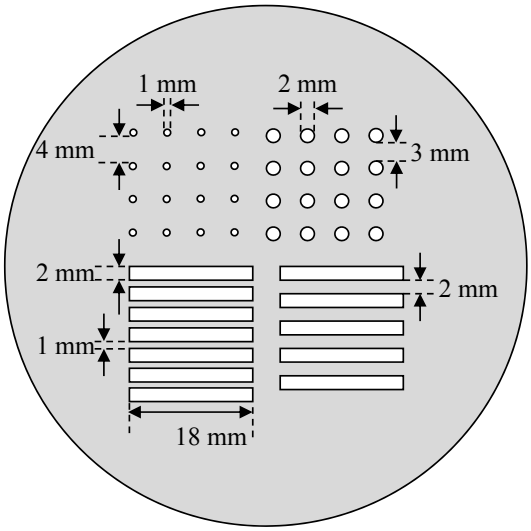


Fig. 2.5. Shadow mask used to fabricate MOS capacitors for electrical characterization.

2.3 Physical and Electrical Properties

The effect of various deposition conditions on the growth rate of the SiO_2 films is discussed first for the optimization of deposition process. In the determination of principal parameters and their optimal values, we select parameters and their values that yield the lowest deposition rate for denser, thus less porous film leading to the lowest leakage current. From the dependence of the film growth rate on the RF power, pressure, He flow rate, and N_2O/SiH_4 shown in Fig. 2.6, we can infer that the pressure and N_2O/SiH_4 are the principal factors, and their optimal condition are 100 mTorr and 100, respectively. Although the

effects of the RF power and He flow rate on the growth rate are relatively smaller than those of the pressure and N_2O/SiH_4, their optimal values are 100 W and 400 sccm, respectively.

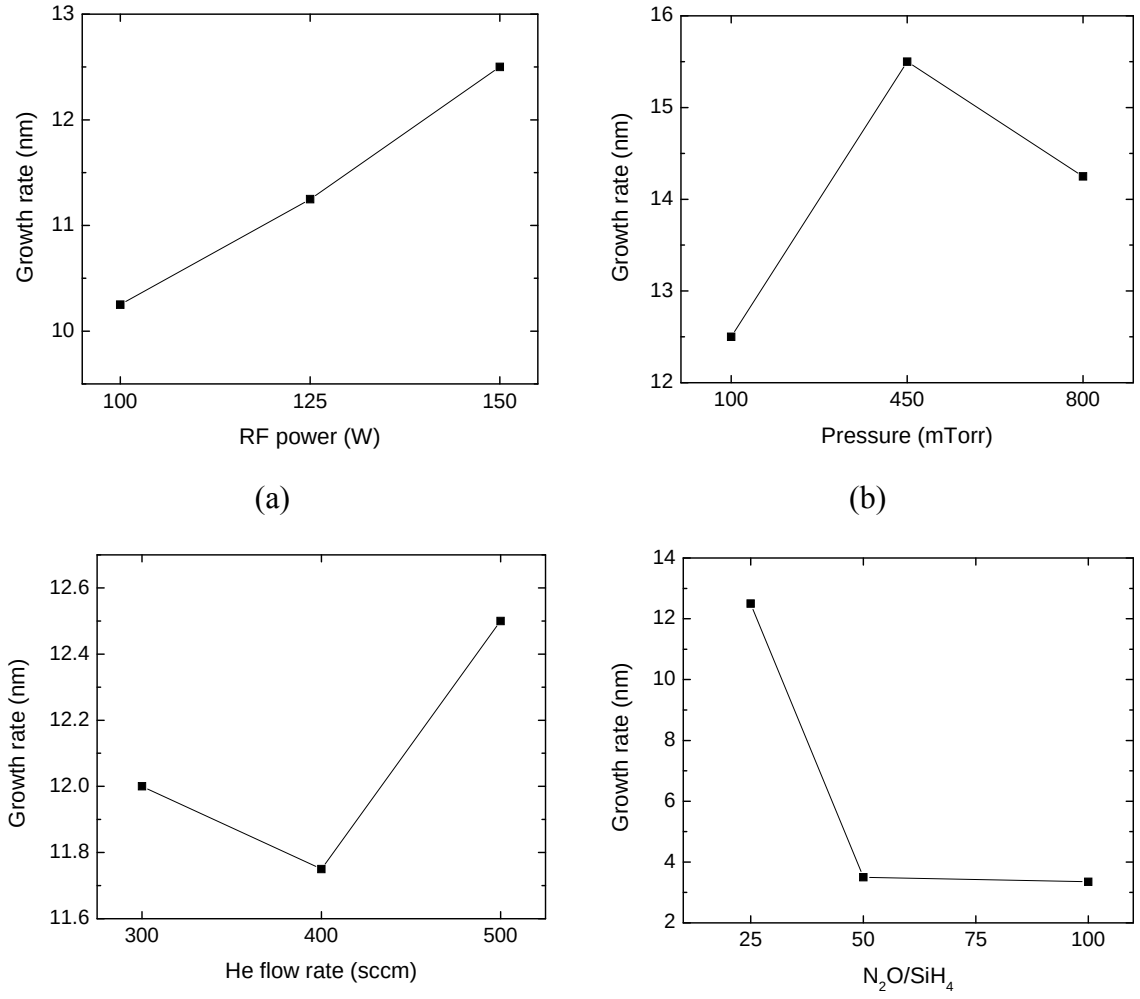


Fig. 2.6. Effects of (a) the RF power, (b) pressure, (c) He flow rate, and (d) N_2O/SiH_4 on the growth rate of the SiO_2 films.

The most important bulk property of the SiO_2 dielectric as a gate material is electrical integrity, specifically the leakage current and hysteresis associated with charge trapping [26]. These properties can be evaluated in detail from the I-V and C-V characteristics of the MOS capacitors. Fig. 2.7 shows the leakage current as a function of the RF power, pressure, He flow rate, and N_2O/SiH_4. As observed here, the optimal levels of the process parameters yielding the lowest leakage current are the RF power of 100 W, pressure of 100 mTorr, and He flow rate of 400 sccm, which are in good agreement with those yielding the lowest deposition rate previously discussed. However, reduction in the SiH_4 flow rate is not helpful to suppress the leakage current. This is possibly because the SiH_4 flow rate below 4 sccm in our case is too low to provide a sufficient amount of the precursor molecule (SiH_3) for SiO_2 deposition [38].

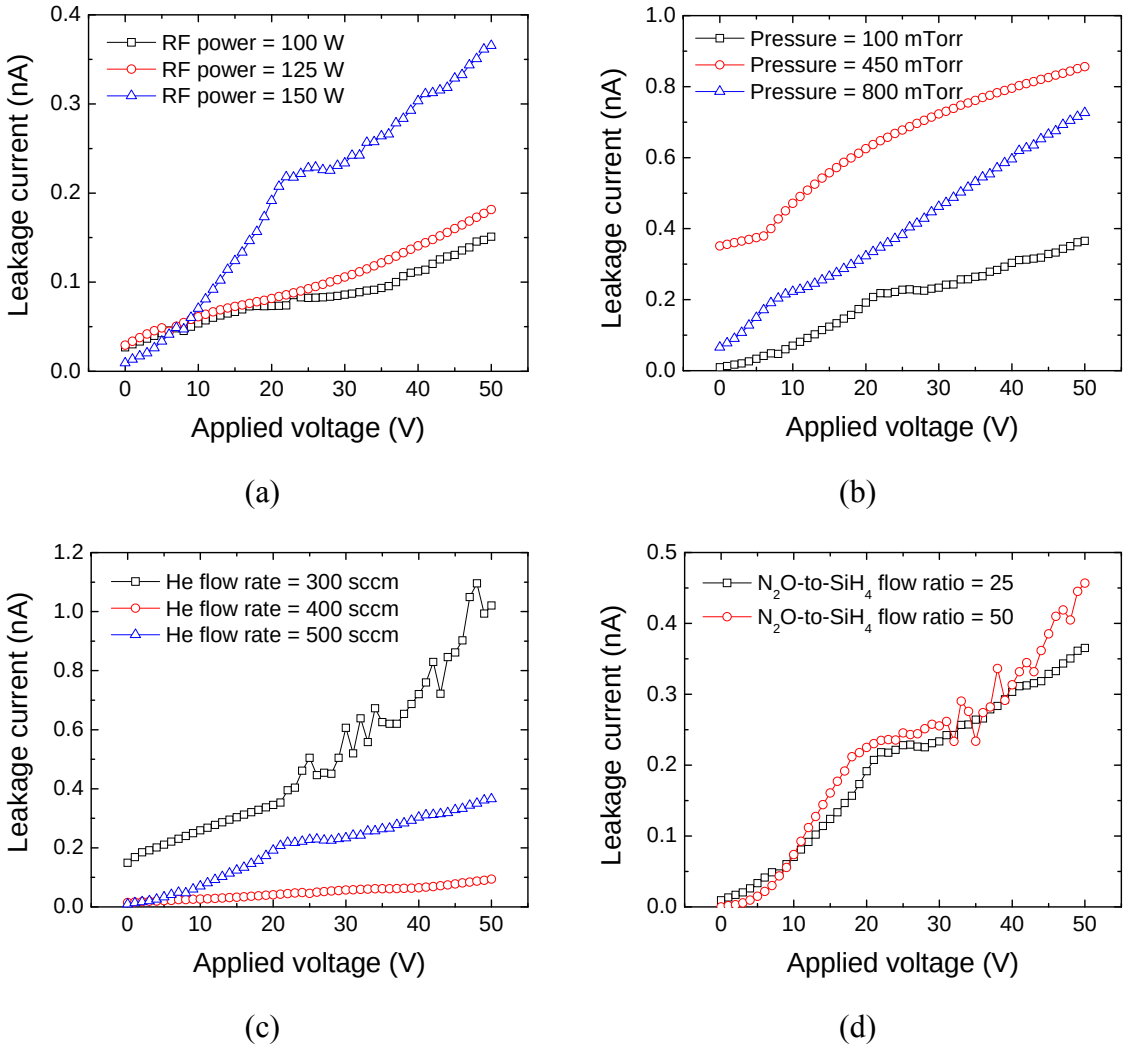


Fig. 2.7. Leakage current as a function of (a) the RF power, (b) pressure, (c) He flow rate, and (d) N_2O/SiH_4.

Table 2.4 summarizes the optimized process conditions for our PECVD SiO_2 deposition. The SiO_2 film deposited by using this new recipe exhibits a growth rate of 10.7 nm/min. The ellipsometric data and infrared absorption spectra of the optimized SiO_2 were

compared for the study of the chemical composition of the film. Fig. 2.8 shows the refractive indices in the wavelength range 400 to 750 nm. The refractive index at 632.8 nm is ~1.46. Indeed, this value of the refractive index is very close to that of thermal SiO_2, which can indicate that the optimized film is nearly stoichiometric. However, this interpretation should be supported by other complementary data because the ellipsometric measurements are strongly model-dependent. In Fig. 2.9, the infrared absorption spectra plotted in the range 400 to 1400 cm^{-1} feature three principal absorption peaks related to the Si–O groups: the rocking mode near 450 cm^{-1}, the bending vibration mode at ~810 cm^{-1}, and the asymmetric stretching mode at about 1060 cm^{-1} [36],[39]. In addition, we observe a broad shoulder at the high wavenumber side of the asymmetric stretching mode centered at around 1200 cm^{-1}. This is typical of the SiO_2 films deposited at low temperature [36],[39]. The infrared spectra ranging from 3000 to 3800 cm^{-1} are also shown in the inset. Here, a peak related to the Si–OH asymmetric stretching vibration is observed at ~3630 cm^{-1} [39]. It is important to note that the shift of Si–O asymmetric stretching towards lower wavenumbers than ~1078 cm^{-1} in thermal SiO_2 correlates with an increase in Si–Si bonds (therefore, the corresponding decrease in Si–O bonds) [39], indicating that the film is possibly deviated from the stoichimetic composition.

Table 2.4. Optimized process parameters for PECVD SiO_2 deposition.

Process parameter	Value
Substrate temperature (°C)	260
RF power (W)	100
Pressure (mTorr)	100
He flow rate (sccm)	400
N_2O/SiH_4 flow	25

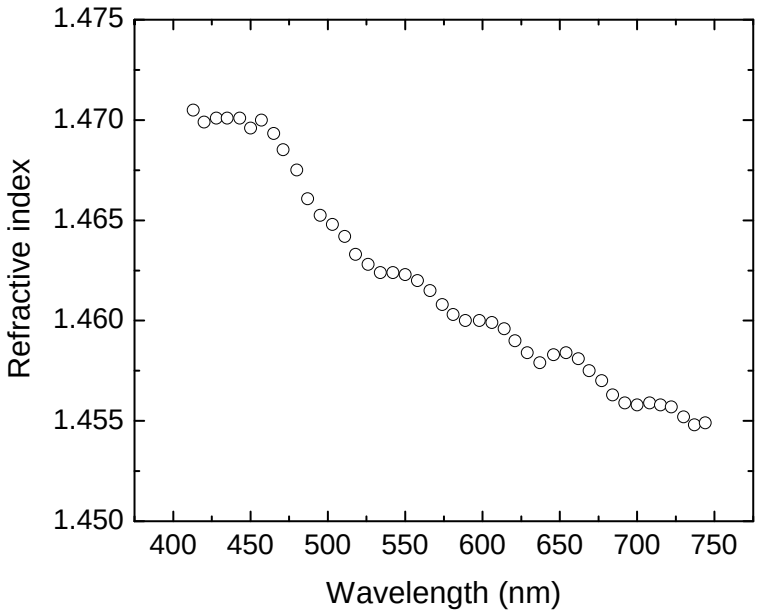


Fig. 2.8. Refractive indices of the optimized SiO_2 film. The refractive index at a wavelength of 632.8 nm is ~1.46.

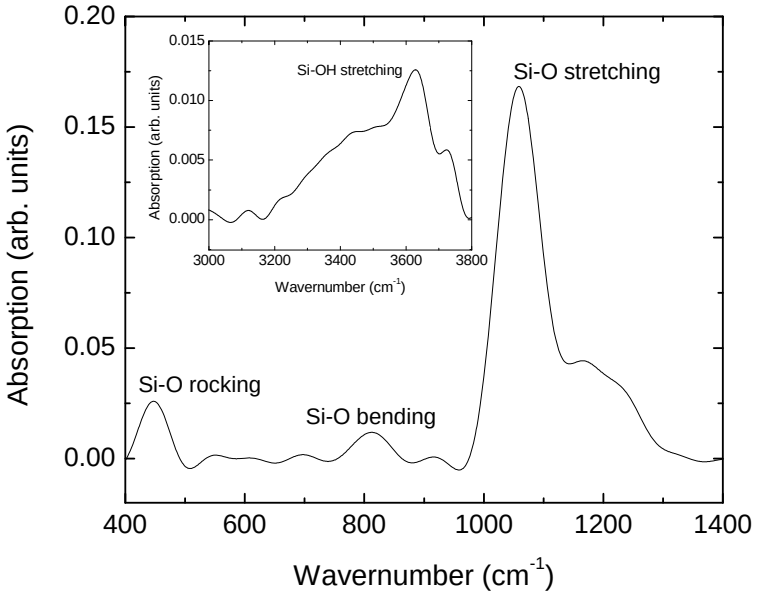


Fig. 2.9. Infrared absorption spectra of the optimized SiO_2 films showing Si–O rocking, bending, and stretching at 460 cm^{-1}, 808 cm^{-1}, and 1075 cm^{-1}, respectively. In addition, a broad shoulder at the high wavenumber side of Si–O stretching is observed. Inset: infrared spectra ranging 3000 to 3800 cm^{-1} showing Si–OH asymmetric stretching at ~3630 cm^{-1}.

The I-V characteristics of the optimized film presented in Fig. 2.10 demonstrate characteristics typical of PECVD SiO_2 [26]. The characterization sequence was as follows. First, a test capacitor was swept up from 0 V to the breakdown field. Then, a new capacitor was selected, and the first I-V trace was retrieved as the applied voltage was ramped up from 0 to 50 V. On the same capacitor, the voltage was then ramped down from 50 to -50 V, and the second I-V trace was appended. In our case, the second trace resulted in a significant reduction in the measured current, which indicates a considerable amount of traps present in

SiO_2 [39]. This sequence was repeated until the hysteresis associated with SiO_2 charge trapping was fully minimized. As observed here, carrier injection at low bias level is greatly reduced after the third sweep. Here, the leakage current density is 9.64 nA/cm^2 at 20 V. Therefore, it is crucial that the TFT characteristics should be measured after fully saturating charge trapping in SiO_2 by repeated sweeps so as to minimize the hysteresis effect of the dielectric on TFT performance.

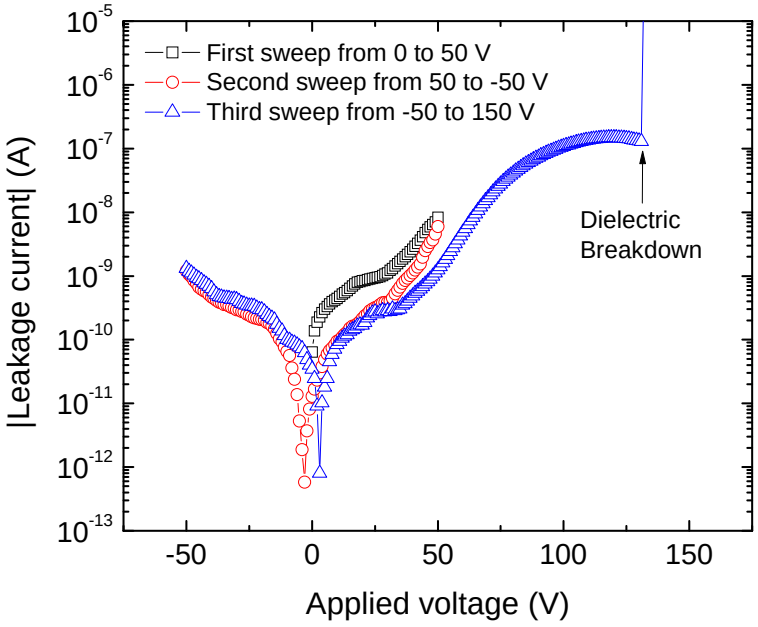
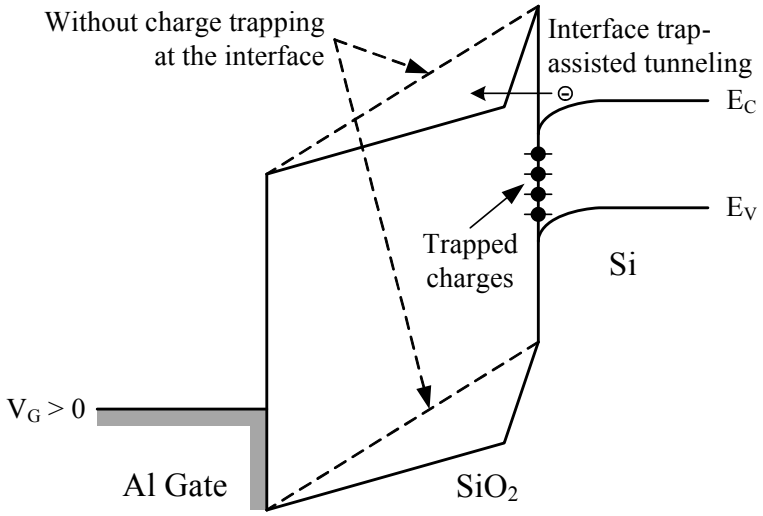
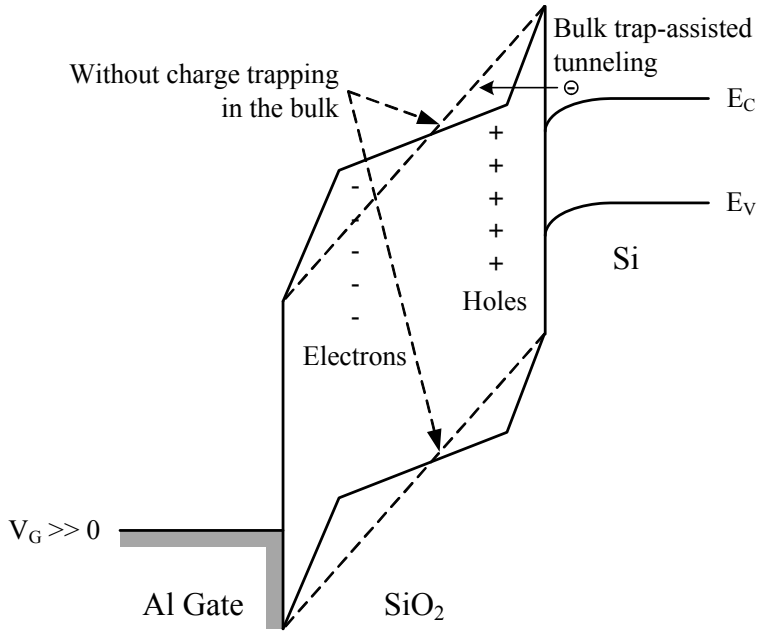


Fig. 2.10. I-V characteristics of the MOS capacitors fabricated by using the optimized SiO_2 films, in which a hysteresis associated with charge trapping in SiO_2 is observed.

For low applied voltages (≤ 20 V), the displacement current is predominantly enhanced by premature injection of carriers, whose origin has been attributed to interface traps [26], as depicted in Fig. 2.11(a). Here, trapped charges at the Si/SiO_2 interface distort the band edge, thus thinning the width of the tunneling barrier. Then, current injection from the silicon substrate occurs through the barrier corresponding to the conduction band discontinuity between Si and SiO_2. As the current increases through the oxide by Fowler-Nordheim (FN) tunneling [41], some electrons captured into the traps create space charges as shown in Fig. 2.11(b). At a sufficiently high bias (> 30 V), the space charge opposes the applied voltage, and therefore a trapping ledge is observed on a logarithmic plot [27]. After all of the traps are filled, the curve undergo the ledge (at ~100 V) and then a new Fowler-Nordheim injection before breakdown. In our case, dielectric breakdown is observed at 6.17 MV/cm, which is lower than that of thermal SiO_2 (~10 MV/cm).



(a)



(b)

Fig. 2.11. Band diagrams of the MOS capacitor showing (a) interface trap-assisted tunneling and (b) bulk trap-assisted FN tunneling.

Fig. 2.12 shows the C-V characteristics of the optimized film. The dielectric constant ε_r extracted from the measurements is 4.51. This is slightly higher than that of thermal SiO_2, which indicates that the films are silicon-rich [27]. From the fact that the interface states can follow low frequency variations of the applied bias but not at high frequency, the density of interface states D_{it} can be calculated from the stretch out between high and low frequency C-V curves,

$$D_{it} = \frac{1}{q}\left(\frac{C_{OX}C_{LF}}{C_{OX}-C_{LF}} - \frac{C_{OX}C_{HF}}{C_{OX}-C_{HF}}\right), \quad (2.1)$$

where C_{OX} is the oxide capacitance, and C_{LF} and C_{HF} are the capacitance values measured at the onset of strong inversion at low and high frequencies, respectively [42]. In our case, D_{it} is ~1.5×10^{11} $cm^{-2}\cdot eV^{-1}$, which is an order of magnitude higher than that of thermal SiO_2 (~10^{10} $cm^{-2}\cdot eV^{-1}$).

It should be also noted that an upward tilt is observed in the quasi-static C-V characteristics as the MOS capacitor is swept from accumulation to depletion. This skewing effect at negative gate bias can result from shunt resistance across the MOS capacitor. Indeed, shunt resistance of the order of 10^{12} Ω is known to have visible effects [42]. This shunt resistance, which can originate from a leaky oxide [42], occurs as an ohmic current opposed to the displacement current in the MOS capacitor. As the gate bias becomes less negative, the opposing shunt current decreases, thus causing an upward skew in the C-V characteristics [42].

The mobile ion content, particularly water-related ions such as positive H^+ and negative OH^-, can be determined by the bias-temperature stress (BTS) test [43]. Basic idea of this technique is that the positive bias at elevated temperature repels positive mobile ions to the Si/SiO_2 interface so that they fully contribute to the flatband voltage, while the negative bias at low temperature attracts positive ions to the gate electrode so that they are too far away to affect the flatband condition. In Fig. 2.13, the high frequency C-V characteristics under positive and negative BTS are shown. Here, an electric field of 1 MV/cm and a temperature of 120°C were applied. From the difference of two flatband voltages, the mobile ion content can be calculated using,

$$Q_m = C_{OX}(V_{FB}^+ - V_{FB}^-), \tag{2.2}$$

where V_{FB}^+ and V_{FB}^- are the flatband voltages measured under positive and negative BTS, respectively. In our case, Q_m is 3.4×10^{11} #/cm^2, which is higher than that in well-controlled thermal SiO_2 process (< 10^{10} cm^{-2}·eV^{-1}). It is also noted that since the mobility of H^+ is much higher than that of OH^-, H^+ ions requires more negative gate bias to achieve flatband condition than OH^-. Table 2.5 summarizes the physical and electrical properties of the optimized SiO_2 film.

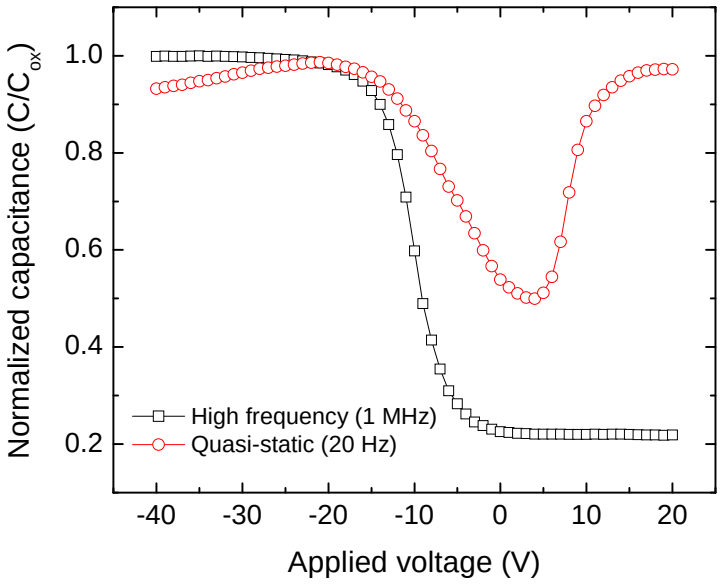


Fig. 2.12. C-V characteristics of the optimized SiO_2 film. The upward skew at negative bias in the quasi-static C-V characteristics can originate from a leaky oxide.

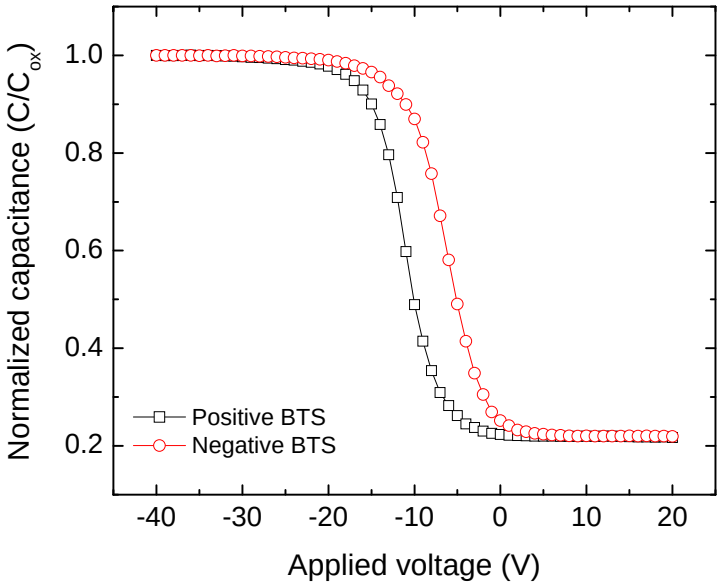


Fig. 2.13. C-V characteristics under positive and negative BTS.

Table 2.5. Summary of physical and electrical properties of the optimized SiO_2 films.

Property	Value
Growth rate (nm/min)	10.7
Refractive index	1.46
Breakdown field (V/cm)	6.17
Dielectric constant	4.51
Interface trap density ($cm^{-2}\cdot eV^{-1}$)	1.5×10^{11}
Mobile ion concentration ($\#/cm^2$)	3.4×10^{11}

2.3.1 N_2O Plasma Pre-Treatment

One may think that plasma treatment at the silicon surface (or plasma oxidation of silicon) prior to bulk oxide deposition and post-metallization annealing (PMA) can further improve the electrical properties. Fig. 2.14 shows the effect of N_2O plasma pre-treatment at the Si/SiO_2 interface. Steeper slope observed in the C-V characteristics, indicating less interface traps [44], suggests that the interface quality can be improved by employing N_2O plasma treatment. However, its benefit here is observed to be small.

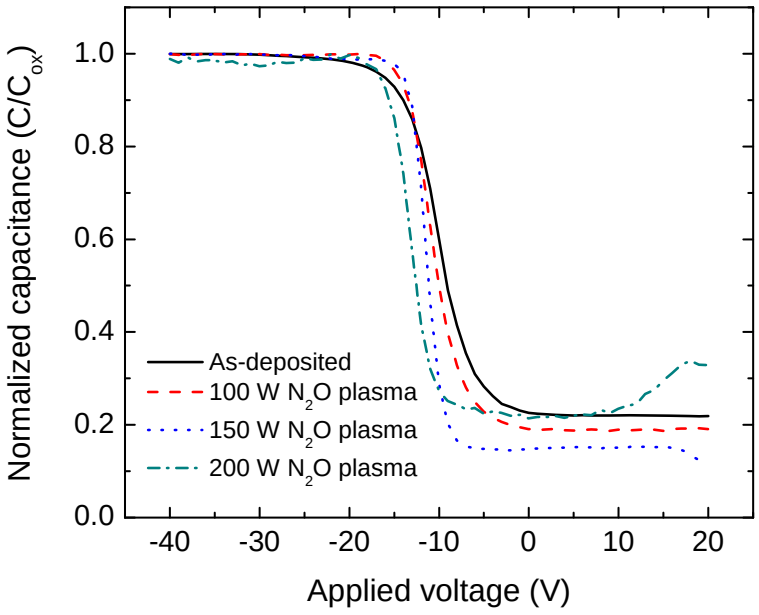


Fig. 2.14. Effect of N_2O plasma treatment at the Si/SiO_2 interface on the C-V characteristics.

This is possibly because a sufficiently thick oxide, which can significantly improve the interface quality, has not been grown. In Fig. 2.15, the Si 2p photoemission spectra of the SiO_2 film grown by 150 W N_2O plasma is presented. Here, the strong peak at ~99 eV corresponds to element silicon in the substrate, while the very weak peak at ~103 eV indicates about 4 eV chemical shifts of silicon in the very thin oxide film grown by 150 W N_2O plasma [45]. The thickness of the SiO_2 film is ~0.2 nm, calculated using the following equation [46],

$$t_{ox} = \lambda_{SiO2} \sin\theta \ln(\alpha/\beta + 1), \quad (2.3)$$

where, λ_{SiO2} is the attenuation length of the Si 2p photoelectrons in SiO_2, being set to be 2.9 nm here [47], θ is the angle between the sample surface plane and the entrance to the electron analyzer, $\alpha = I_{SiO2}^{exp}/I_{Si}^{exp}$ is the ratio of Si 2p intensities from the grown film, and $\beta = I_{SiO2}^{\infty}/I_{Si}^{\infty}$ is the ratio of Si 2p intensities from pure Si and pure SiO_2, being set to be 0.89 here [47]. Indeed, it is reported that greater than 2-nm thick films having the quality comparable to thermal SiO_2 (thus probably a few nm thicker films having low quality) can significantly reduce the interface trap density [48]. In our case, however, further increase in the RF power up to 200 W to grow thicker films rather causes deterioration in the interface quality as shown in Fig. 2.14. This is possibly because energetic ion bombardment beyond the sputtering threshold (~90 eV) of silicon damages the Si/SiO_2 interface [49].

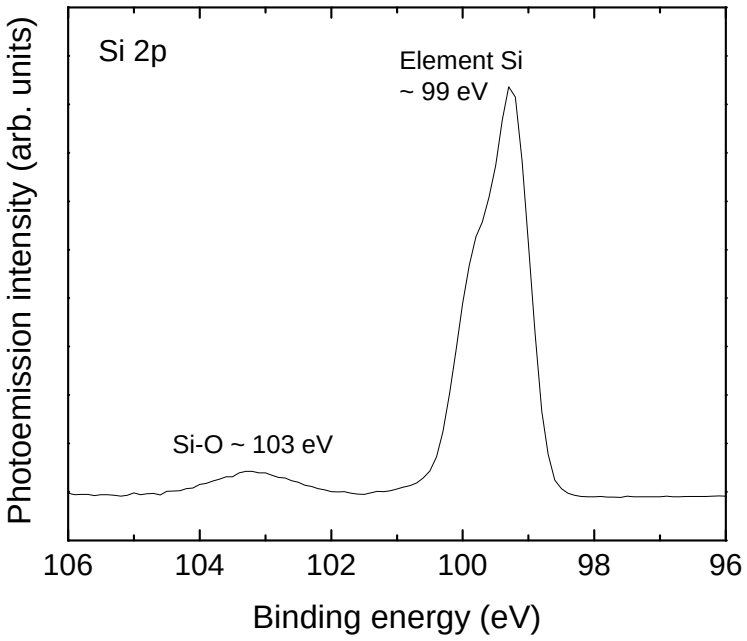
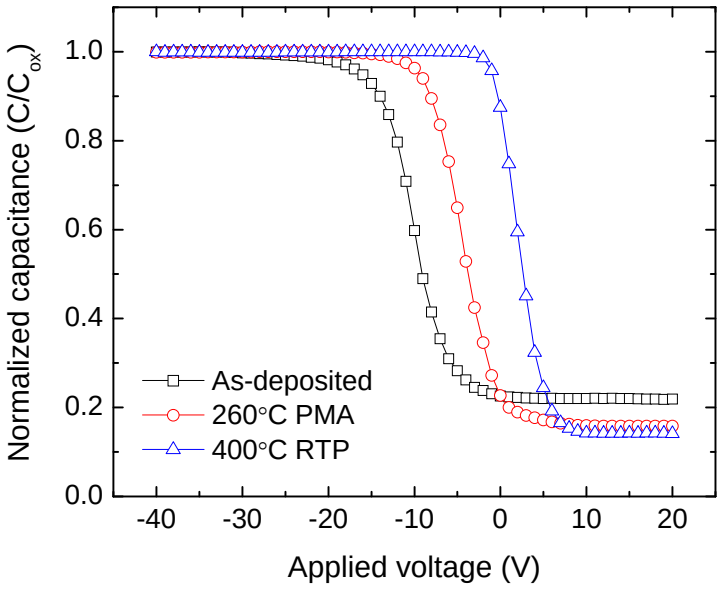


Fig. 2.15. Si 2p photoemission spectra of the SiO_2 film grown by 150 W N_2O plasma. The strong peak at ~99 eV indicates silicon in the substrate, while the weak peak at ~103 eV corresponds to Si–O in the thin oxide film (~0.2 nm).

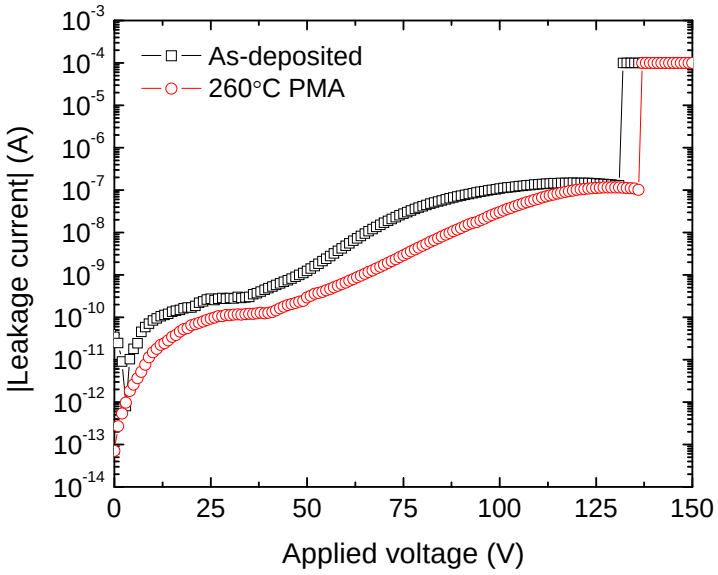
2.3.2 Post-Metallization Thermal Annealing

Post-metallization thermal annealing may not be helpful to reduce the trap states in the film in consideration of the allowable maximum processing temperature of the plastic substrates [50]. In order to investigate the effect of annealing treatment, the MOS capacitors were subjected to PMA as follows: (1) thermal annealing in a N_2 ambient at a temperature of 260°C for 60 min and (2) rapid thermal annealing (RTP) in a N_2 ambient (10 slpm) at a

temperature of 400°C for 10 min, respectively. The resultant C-V and I-V characteristics are shown in Figs. 2.16(a) and (b), respectively. As observed in Fig. 2.16(a), annealing at deposition temperature reduces the flatband voltage from -15 to -10 V. Especially when the film is annealed using RTP, the flatband voltage is found to be nearly 0 V. As a result of 260°C PMA, the dielectric constant is decreased from 4.51 to 3.82 (3.8 in thermal SiO_2), and the dielectric breakdown field is slightly increased from 6.17 to 6.4 MV/cm as shown in Fig. 2.16(b). However, prior to employing PMA process (particularly RTP) for TFT fabrication, thermal damage to the underlying substrate should be carefully investigated first.



(a)



(b)

Fig. 2.16. Effects of post-metallization annealing on the electrical properties of the optimized SiO_2 films: (a) C-V and (b) I-V characteristics.

Chapter 3
Highly Conductive nc-Si:H Contacts

In this chapter, we demonstrate the evolution of structural and electronic properties in the nc-Si:H material with doping to particularly improve its p-type properties, which is one of the most critical issues for the development of complementary nc-Si:H TFTs.

3.1 Introduction

Disordered materials contain a large number of defect states within the band gap of the material. Fig. 3.1 illustrates a typical density of defect states (DOS) distribution for a-Si:H, poly-Si, and nc-Si:H materials [51]. Here, each half of the gap is broken into two sections: deep and tail states. Again, states in the upper half of the band gap are acceptor-like (i.e., positive when unoccupied and neutral when occupied by electrons), and states in the lower half of the gap are donor-like (i.e., neutral when unoccupied and negative when occupied by electrons) [51].

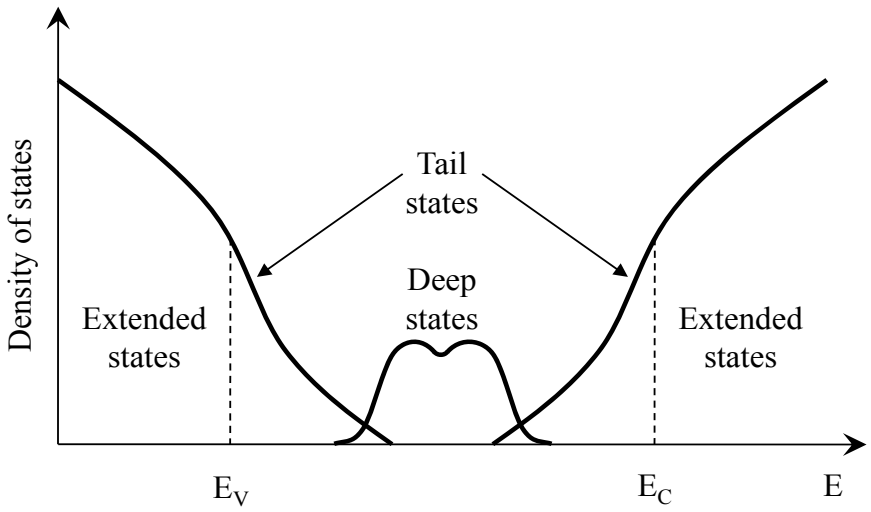


Fig. 3.1. Illustration of the density of defect states within the band gap of disordered materials such as amorphous, polycrystalline, and nanocrystalline silicon [51].

To accurately describe behavior of the TFTs made of the disordered materials, two deep states are modeled using a Gaussian distribution expressed by,

$$g_{GA}(E) = NGA \exp\left[-\left(\frac{EGA-E}{WGA}\right)^2\right], \tag{3.1}$$

$$g_{GD}(E) = NGD \exp\left[-\left(\frac{E-EGD}{WGD}\right)^2\right], \tag{3.2}$$

where E is the trap energy, and the subscripts G, A, and D stand for Gaussian, acceptor, and donor states, respectively. For Gaussian distributions, the density of defect states is described by its total density of states (NGA and NGD), its characteristic decay energy (WGA and

WGD), and its peak energy/peak distribution (EGA and EGD) [52]. Two tail states are modeled using an exponential distribution, in which,

$$g_{TA}(E) = NTA \exp\left(\frac{E-E_C}{WTA}\right), \tag{3.3}$$

$$g_{TD}(E) = NTD \exp\left(\frac{E_V-E}{WTD}\right), \tag{3.4}$$

where the subscript T stands for tail states, E_C is the conduction band energy, and E_V is the valence band energy. For exponential tail distributions, the density of defect states is described by its conduction and valence band edge intercept densities (NTA and NTD), and by its characteristic decay energy (WTA and WTD) [52]. Therefore, the total density of defect states in the band gap is given by

$$g(E) = g_{GA}(E) + g_{GD}(E) + g_{TA}(E) + g_{TD}(E). \tag{3.5}$$

Table 3.1 summarizes typical values of these parameters for amorphous and polycrystalline silicon materials.

Table 3.1. Summary of typical values for the density of defect states in amorphous and polysilicon materials [52].

Parameter	a-Si:H	poly-Si
NTA (cm^{-3})	1×10^{21}	1.12×10^{21}
NTD (cm^{-3})	1×10^{21}	4×10^{20}
NGA (cm^{-3})	4.5×10^{15}	1×10^{18}
NGD (cm^{-3})	4.5×10^{15}	3×10^{18}
EGA (eV)	0.62	0.4
EGD (eV)	0.78	0.4
WTA (eV)	0.033	0.025
WTD (eV)	0.049	0.05
WGA (eV)	0.15	0.1
WGD (eV)	0.15	0.1

It is widely known that nc-Si:H film growth undergoes four stages: (1) incubation, (2) nucleation, (3) growth, and (4) steady state as follows [10]. In the incubation stage, hydrogen diffuses into the a-Si:H network and forms the hydrogen-rich layer. Once the film is fully modified by hydrogen, nucleation of crystallities takes place. After the formation of stable nuclei, the crystallities grow until the crystalline fraction reaches steady state. Accordingly, this leads to the inhomogeneous structure of the film along the growth direction, consisting

of an amorphous incubation layer, regarded as a remnant of the nucleation process, and a bulk layer with the highest crystalline fraction as shown in Fig. 3.2.

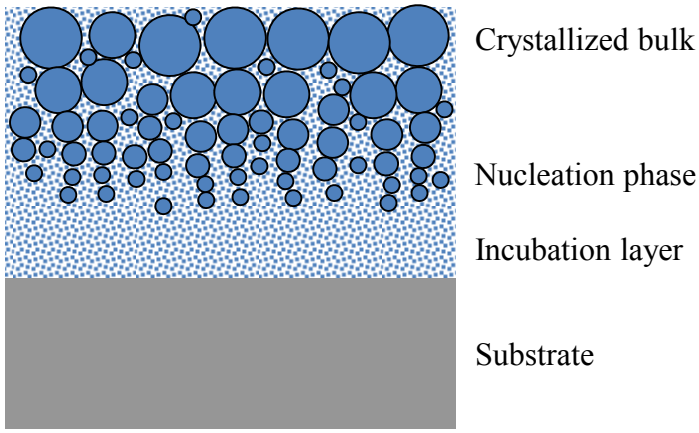
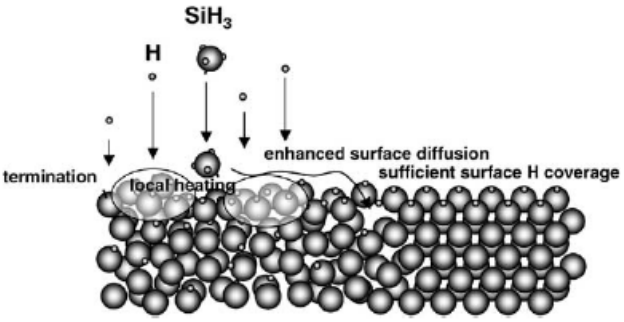


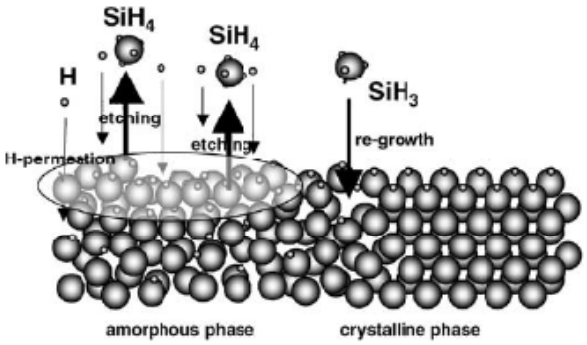
Fig. 3.2. Inhomogeneous growth of the nc-Si:H material. The incubation layer can be considered as a remnant amorphous phase of nucleation process, and a bulk layer at the top has the best crystalline properties.

Here, hydrogen atoms play a key role for the growth of the nc-Si:H films. There have been three predominant models for the role of H proposed to account for the growth process of nc-Si:H: (1) surface-diffusion model, (2) etching model, and (3) chemical-annealing model as presented in Fig. 3.3 [11]. In the surface-diffusion model, large amount of hydrogen atoms fully covers the film-growing surface and also produces local heating through hydrogen exchanging reactions, enhancing the surface diffusion of film precursors (SiH_3). SiH_3 adsorbed on the surface finds energetically favorable sites, leading to the nucleus

formation. As a result, epitaxial-like crystal growth takes place with an enhanced surface diffusion of SiH_3. In the etching model, atomic hydrogen preferentially breaks weak Si–Si bonds, in the amorphous network. The resultant site is replaced with a new film precursor SiH_3, creating a strong Si–Si bond, and leading to crystalline structure. The chemical-annealing model has been proposed to explain a layer-by-layer growth of the nc-Si:H films (repetition of an alternating sequence of a-Si:H growth and H-plasma treatment). During H-plasma treatment, many hydrogen atoms are permeating into the film, leading to a crystallization of amorphous phase through the formation of a flexible network without remarkable removal process of silicon atoms.



(a)



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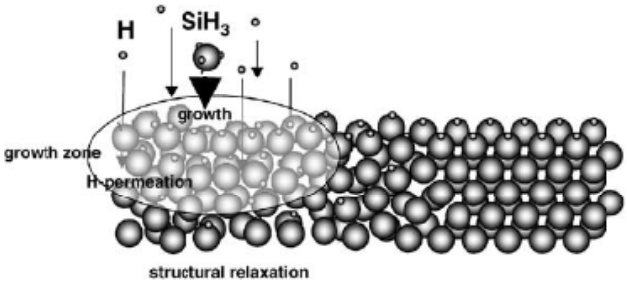


(c)

Fig. 3.3. Growth models for nc-Si:H: (a) surface-diffusion model, (b) etching model, and (c) chemical cleaning model [11].

High-quality nc-Si:H films are indispensable for high-performance TFTs. High crystallinity giving rise to high field effect mobility and low dark conductivity minimizing the leakage current are two primary targets for intrinsic nc-Si:H film growth. It should be noted that the as-deposited (undoped) nc-Si:H material shows slightly n-type properties possibly due to oxygen impurities incorporated during film growth as shown in Fig. 3.4 [53]. Therefore, there have been many attempts to grow nearly intrinsic films from the mixture of SiH_4 and SiH_2Cl_2 [34] or by adding a small amount of p-type impurities such as B_2H_6 to the source gas, so-called 'compensation doping' [54].

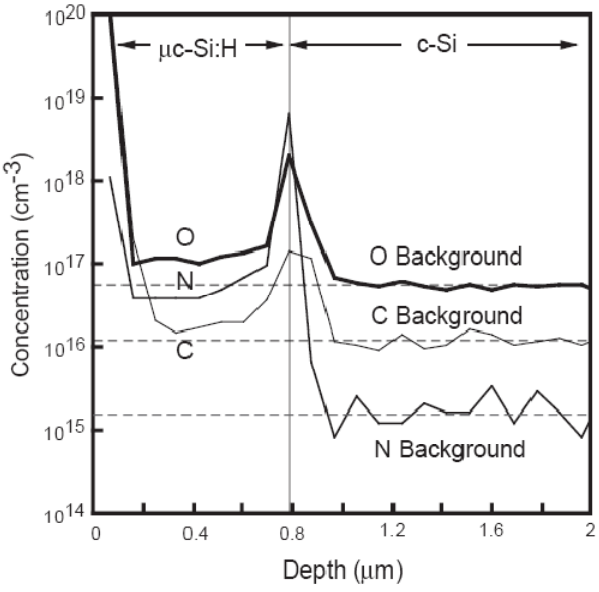


Fig. 3.4. Depth profiles of O, C, and N impurities in the nc-Si:H film characterized by secondary ion mass spectrometry (SIMS) [53].

The capability to prepare heavily doped n- and p-type nc-Si:H layers is also critical for high-performance TFTs, since these layers are required to make good ohmic contact with the intrinsic channel layer and to block the injection of carriers of the opposite sign [12]. If these contacts are not able to provide sufficient carrier injection and collection, they definitely increase series resistance and thus limit TFT performance. One of the most challenging issues in the growth of the highly doped nc-Si:H material is an asymmetry observed in n- and p-type doping. Highest conductivity (~1 S/cm) achieved by p-doping is found to be much lower than that (> 20 S/cm) obtained by n-doping [12],[55]. Here, PH_3 and B_2H_6 have been used as n- and p-type dopant sources, respectively. However, further improvement especially in the p-type properties is crucial.

Several methods have been proposed to grow the high-quality nc-Si:H films including sputtering [56], hot-wire (HW) CVD [12],[57], very high frequency (VHF) glow discharge [54], ECR [58], ICP [59], and conventional PECVD [10]. Compared to other methods, PECVD is widely used due to its high potential to prepare high-quality materials uniformly over large area.

3.2 Film Deposition and Characterization

The starting point for the experiment is to investigate $B(CH_3)_3$ (trimethylboron, referred to as simply TMB) as an alternative dopant source for the growth of high-quality p-type nc-Si:H films. In Table 3.2, the relative advantages and drawbacks of B_2H_6 and TMB

are summarized. TMB is known to have better thermal stability (therefore, longer gas shelf life) due to higher dissociation energy of B–C bonds than that of B–B bonds in B_2H_6 [60]. In addition, TMB doping can produce less defective films if doping process is carefully controlled, while B–H bonds remaining in the films doped by B_2H_6 can generate high defects [60]. However, if the films are too highly doped using TMB, more C incorporated into the films may not only suppress crystalline growth process [57] but also widen the electrical band gap [60], thus causing a decrease in the conductivity of the films.

Table 3.2. Comparison of B_2H_6 and TMB as dopants for p-type nc-Si:H deposition.

	B_2H_6	$B(CH_3)_3$
Decomposition process	By forming BH_3 at low temperature: - B–B bonding energy: 27 kcal/mol - B–H bonding energy: 99 kcal/mol	Via sequential loss of CH_3: - B–C bonding energy: 87 kcal/mol - C–H bonding energy: 99 kcal/mol
Thermal stability	Poor due to low dissociation energy of B–B bonds.	Better due to high dissociation energy of B–C bonds.
Crystallinity	Better	Can be worse due to the incorporated C suppressing crystal growth.
Defect density	B–H bonds remaining in the films can result in high defect density	More C incorporation by high doping may result in the amorphization of films (a-SiC formation).
Conductivity	Better	Wide E_g due to C incorporation may result in low conductivity.

In our experiments, the films were grown on Corning 1737 glass substrates using the same PECVD system as in oxide deposition previously described. The evolution of the structural and electronic properties in n- and p-type (also compensated) nc-Si:H films are studied by gradually varying a PH_3-to-SiH_4 flow ratio (PH_3/SiH_4) from 0.1 to 2% and a TMB-to-SiH_4 flow ratio (TMB/SiH_4) from 0.5 to 3% to cover the full range of doping. Here, 1% PH_3 and 1% TMB both diluted in H_2 were used. The substrate temperature, RF power, pressure, and hydrogen dilution ratio $H_2/(H_2 + SiH_4) \times 100\%$ were fixed at 260°C, 90 W, 900 mTorr, and 99 %, respectively.

The growth rate r_d was calculated from the film thickness measured with a Dektak 8 surface profiler. The film crystallinity X_C was determined from Raman spectra measured in the backscattering geometry using a Renishaw micro-Raman 1000 spectrometer with a 633 nm He-Ne laser source. The power of the incident beam was kept below 50 mW to avoid the crystallization of the nc-Si:H films. The crystallinity was deduced from the integrated Raman intensity ratio,

$$X_C = \frac{I_{520}}{(I_{520}+\eta I_{480})}, \tag{3.6}$$

where I_{520} and I_{480} are the deconvoluted intensities of the Raman spectra in crystalline silicon transverse optical (TO) (~520 cm^{-1}) and amorphous silicon TO (~480 cm^{-1}) peaks, respectively, as shown in Fig. 3.5, and η is the ratio of the back scattering cross-sections, being set to be 0.8 here [61]. X-ray diffraction (XRD) peaks were measured with a

PANalytical X'Pert PRO x-ray diffractometer using Cu-Kα_1 line (λ = 1.54056 Å) at a grazing incidence (0.5°). The grain size d_g was calculated by the Scherrer formula [55],

$$d_g = \frac{k\lambda}{B\cos\theta_B}, \tag{3.7}$$

where k ~0.9, B is the full width at half maximum (FWHM) of the peaks (in units of 2θ), and θ_B is the angular position of the peak.

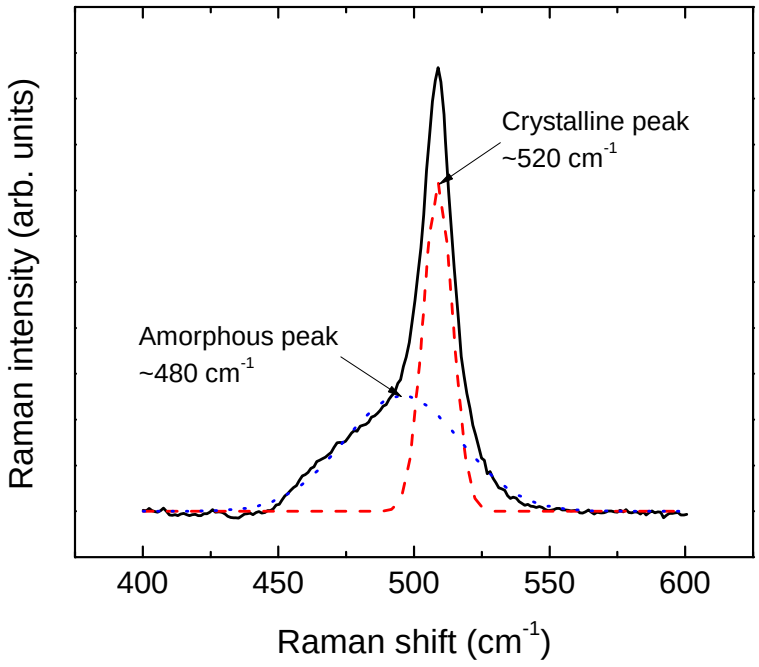


Fig. 3.5. Determination of the crystallinity from deconvoluted Raman spectra: the 520 cm^{-1} peak corresponds to the scattering by crystalline silicon TO mode, while the 480 cm^{-1} peak indicates amorphous silicon TO.

For dark conductivity σ_d measurements, 18-mm long and 1-mm apart coplanar chromium contacts were deposited through a shadow mask shown in Fig. 2.5 by an Edwards E306A RF sputtering system. The dark conductivity was then retrieved from the slope of the film I-V characteristics as shown in Fig. 3.6. The activation energy E_a was calculated from the temperature dependence of the dark conductivity expressed by

$$\sigma_d = \sigma_0 \exp\left(-\frac{E_a}{kT}\right), \tag{3.8}$$

where k is the Boltzmann constant. For all measurements, the film thickness was ~50 nm, which was the same thickness as that of source/drain contacts in the fabricated TFTs.

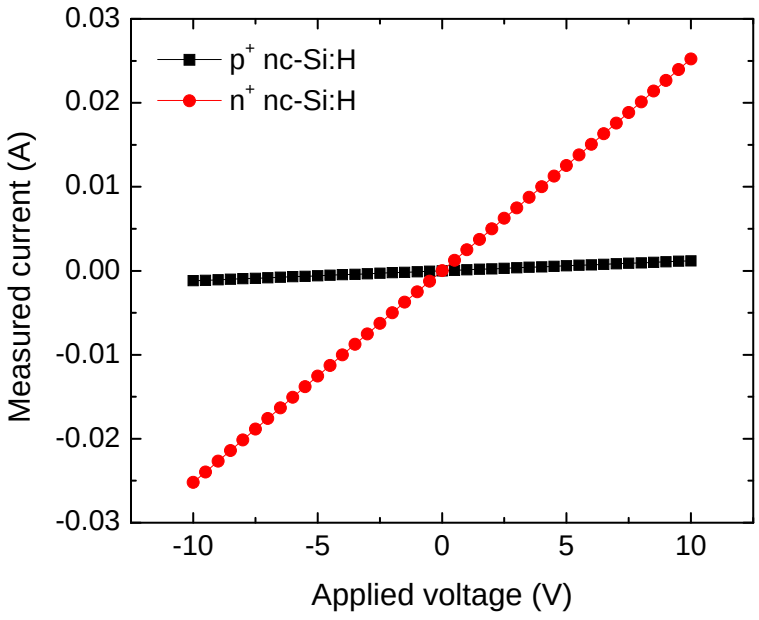


Fig. 3.6. Dark current-voltage characteristics of nc-Si:H films: the dark conductivity is retrieved from the slope.

3.3 Structural and Electronic Properties

In this section, we discuss the evolution of the structural and electronic properties in the nc-Si:H films with doping, with emphasis on p-type properties. Table 3.3 summarizes the structural and electronic properties of selected n- and p-doped nc-Si:H films. In Fig. 3.7, the evolution of the film growth rate as a function of a doping gas-to-SiH_4 flow ratio is presented. Here, a sharp increase in the growth rate is observed as both n- and p-doping increase. As TMB/SiH_4 increases from 0 to 0.7%, the growth rate of the p-type films increases by a factor of 1.6, while the growth rate of the n-type films increases by a factor of 1.5 as PH_3/SiH_4 increases from 0 to 0.5%. Indeed, a dramatic increase in the growth rate of the n- and p-doped films observed here is in agreement with that previously reported for PH_3 and B_2H_6 doping, respectively [55],[62]. Especially for the p-type films prepared by using B_2H_6 as a doping gas, the increase upon addition of B_2H_6 has been explained by the catalytic effect of BH_3 radicals that abstract hydrogen atoms from the film-growing surface, thus enhancing the sticking probability of SiH_3 precursors [62]. From a similar trend in the growth rate observed in our case, CH_3 radicals from TMB are attributable to hydrogen removal process from the surface, hence promoting the growth process as depicted in Fig. 3.8.

Table 3.3. Structural and electronic properties of selected n- and p-doped nc-Si:H films.

Dopant	Doping ratio (%)	r_d (nm/min)	X_c (%)	d_g (nm)	σ_d (S/cm)	E_a (meV)
PH_3	0.5	4.17	68	Unmeasured	5.56	35.6
	1.0	4.18	69		14.17	25.5
	2.0	3.68	64		25.30	20.0
	3.0	4.04	58		9.33	26.9
TMB	0.2	3.50	72	8.15	9.45×10^{-9}	540
	0.4	3.75	73	9.56	0.24	70.4
	0.5	3.97	71	7.4	1.11	36.7
	0.7	4.51	51	5.75	0.47	45
	2.0	4.83	Amorph.	N/A	1.94×10^{-7}	530

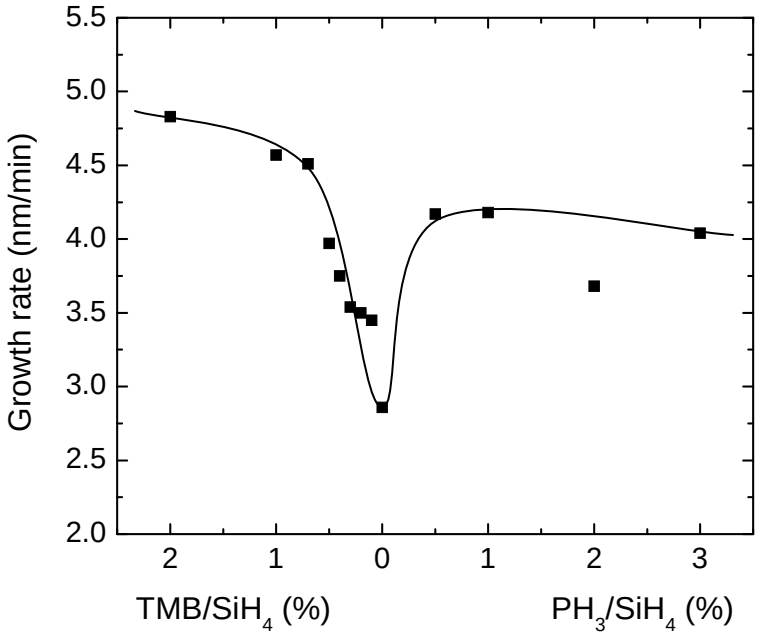


Fig. 3.7. Growth rate of the nc-Si:H films as a function of doping level. The line drawn is meant only as a guide for the eye.

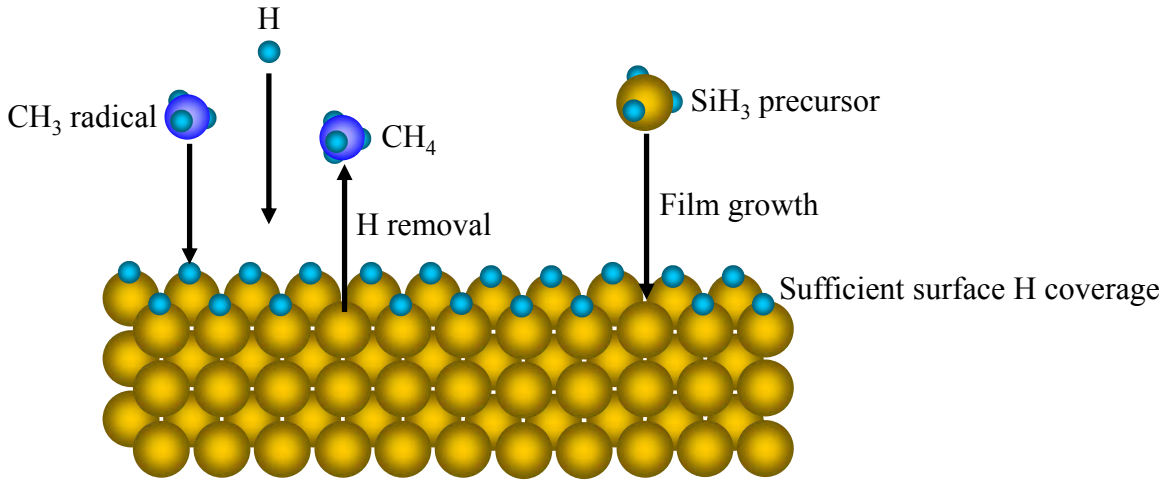


Fig. 3.8. Proposed model for CH_3-assisted nc-Si:H growth: the catalytic effect of CH_3 radicals that abstract hydrogen atoms from the film-growing surface promotes the growth process by enhancing the sticking probability of SiH_3 precursors.

With respect to the crystallinity of the doped films, high crystallinity over 70% is observed when the doping gas-to-SiH_4 flow ratio is low (≤ 0.5%). However, the crystallinity of the films significantly drops as doping increases as shown in Fig. 3.9. Here, as TMB/SiH_4 increases from 0.5 to 0.7%, the crystallinity of the p-type films decreases by a factor of 1.4, while the crystallinity of the n-type films decreases by a factor of 1.2 as PH_3/SiH4 increases from 0.5 to 3%. Especially, it is observed that the p-type films undergo a phase transition from nanocrystalline to amorphous as TMB/SiH_4 increases up to 1%, which is in agreement with previously reported data [57]. In Fig. 3.10, the evolution of Raman spectra in the p-doped films as a function of TMB/SiH_4 is presented, in which the films are observed to be

gradually amorphized by increased doping. We also investigated detailed micro-structural properties of the p-doped films using XRD, and the resultant X-ray diffraction spectra are shown in Fig. 3.11, in which the grains are oriented at (111), (220), and (311) planes. A sharp (111) diffraction peak along with two relatively broader (220) and (311) peaks indicates the good quality of the nc-Si:H material. However, the width of the (111) peak increases as TMB/SiH_4 increases, and the grain size calculated from the (111) peak decreases by a factor of 1.7 as TMB/SiH_4 increases from 0.4 to 0.7%. This also implies the amorphization of the nc-Si:H material by increased doping.

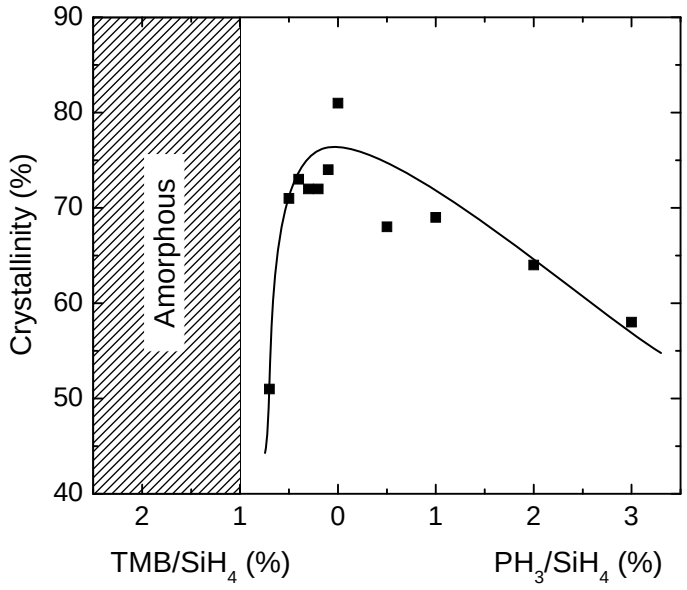


Fig. 3.9. Film crystallinity as a function of doping level. A phase transition from nanocrystalline to amorphous is observed in the p-type films as TMB/SiH_4 increases up to 1%. The line drawn is meant only as a guide for the eye.

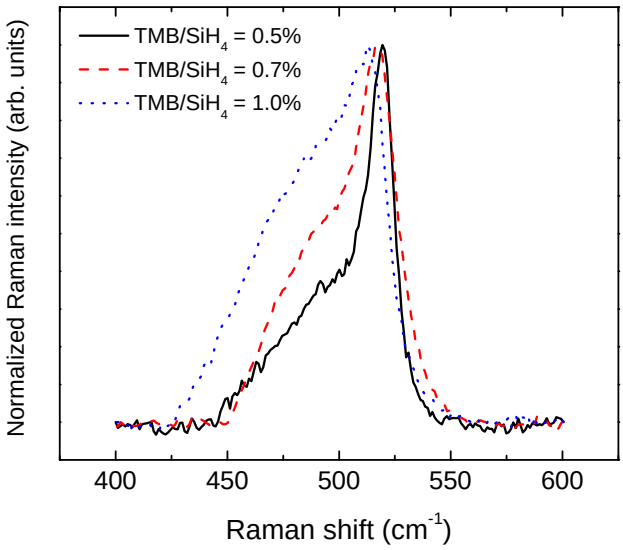


Fig. 3.10. Evolution of the crystallinity in the p-type nc-Si:H films as a function of TMB/SiH_4. The films are gradually amorphized by increased p-doping.

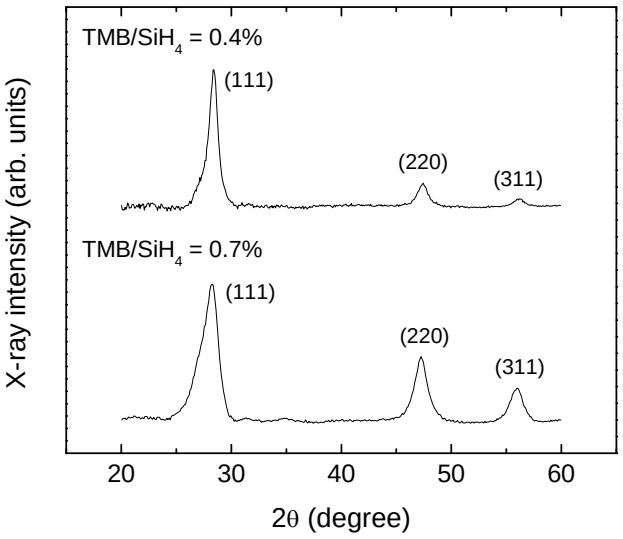


Fig. 3.11. XRD spectra of the p-doped nc-Si:H films. The grain size calculated from the (111) peak decreases by a factor of 1.7 as TMB/SiH_4 increases from 0.4 to 0.7%.

As discussed earlier, one of the most challenging issues in the development of the highly doped nc-Si:H material is to remove an asymmetry particularly in the electronic properties of n- and p-doped films by improving p-type properties. Indeed, Fig. 3.12 illustrates the asymmetry in the dark conductivity of n- and p-doped nc-Si:H films. In Fig. 3.13, the temperature dependence of the dark conductivity and the corresponding activation energy are presented. While n-doped nc-Si:H demonstrates the maximum dark conductivity of 25.3 S/cm (E_a = 20.0 meV) at a PH_3/SiH_4 of 2%, p-type nc-Si:H exhibits much lower value of the maximum dark conductivity of 1.11 S/cm (E_a = 36.7 meV) at a TMB/SiH_4 of 0.5%. The trend in the dark conductivity and activation energy of the doped film is found to be very sensitive to that in the crystallinity of the films. As a phase transition from nanocrystalline to amorphous occurs at a TMB/SiH_4 of 1% in our case, a further increase in TMB/SiH4 to 2% reduces a dark conductivity to 1.94×10^{-7} S/cm (E_a = 0.53 eV) due to the amorphization of the nc-Si:H films, whereas a further increase in PH_3/SiH_4 to 3% shows a slight reduction in the dark conductivity (9.33 S/cm and the corresponding E_a = 26.9 meV) while the crystallinity ~60% is still mantained. In this case, it is highly possible that the p-type nc-Si:H contact layers are not capable of providing sufficient carrier injection and collection. Accordingly, they may increase series resistance and thus limit TFT performance, which will be discussed in detail in the following chapters.

It should be also noted that when TMB/SiH_4 is below 0.2%, a small amount of boron atoms added to the films compensates oxygen impurities incorporated during deposition, and nearly intrinsic films can be grown. As TMB/SiH_4 increases up to 0.2%, the dark

conductivity is reduced to ~10^{-8} S/cm by two orders of magnitude from that of the as-deposited (undoped) film. However, the process window of compensation doping here is observed to be very narrow.

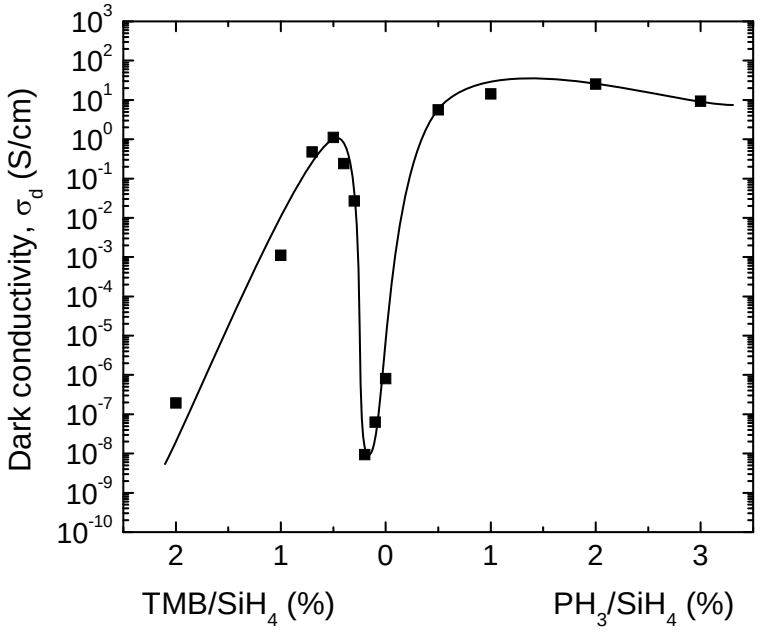
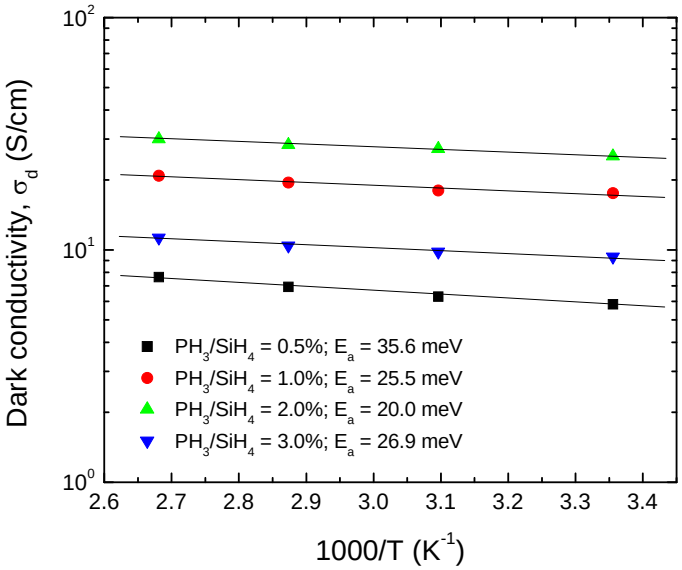
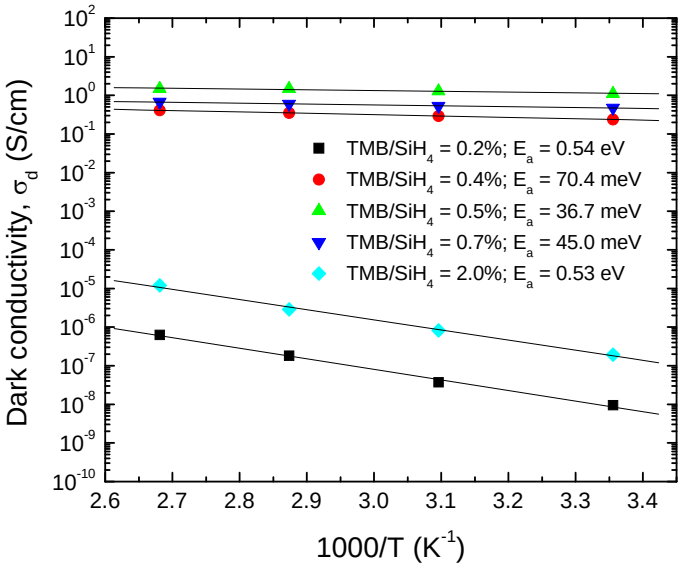


Fig. 3.12. Asymmetry in the dark conductivity of the n-doped ($\sigma_{d,\,max}$ ~25.3 S/cm) and p-doped ($\sigma_{d,\,max}$ ~1.11 S/cm) nc-Si:H films. In addition, σ_d is reduced to ~10^{-8} S/cm by two orders of magnitude from that of the undoped film using compensation doping (TMB/SiH_4 ~0.2%). The line drawn is meant only as a guide for the eye.



(a)



(b)

Fig. 3.13. Temperature dependence of the dark conductivity and corresponding activation energy for (a) n-doped and (b) p-doped nc-Si:H films.

Chapter 4
TFT Fabrication and Characterization

High field effect mobility and low leakage current (therefore, high on/off current ratio), and small threshold voltage along with small subthreshold slope are primary goals for the achievement of high-performance TFTs. Not only the quality of materials incorporated into TFTs but also the structural factors of TFTs strongly influence device performance. In this chapter, we describe the structure, fabrication process, and electrical characteristics of top-gate nc-Si:H TFTs.

4.1 Introduction

TFTs generally operate in accumulation mode, while MOSFETs operate in inversion mode. This is because the thin channel material contains higher defect states within its band gap as previously described in Section 3.1. Application of small positive gate bias yields band bending at the interface, but trap states near the interface capture most of the free electrons generated as shown in Fig. 4.1 [63]. At least for small gate voltages, the conduction

band is not very close to the Fermi level, and as a consequence, the number of electrons in the conduction band is not enough to provide a sufficient drive current. It is not until larger gate bias is applied that the Fermi level becomes close to the conduction band and a significant number of free electrons are induced. Therefore, operating TFTs in inversion mode requires much higher gate bias. This is because TFTs use an intrinsic (undoped) layer as an active channel. The transistor type is then determined by the doping of the source/drain contacts, rather than that of the semiconductor channel.

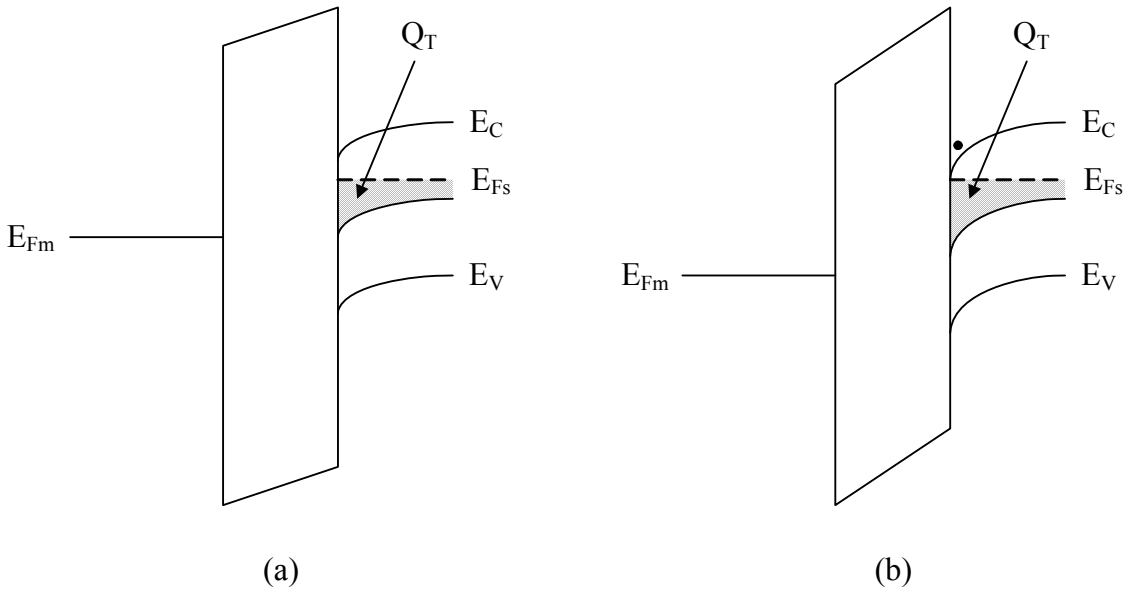


Fig. 4.1. Band diagrams of TFTs having high trap states in the channel: (a) small positive bias in which most of free electrons are captured, and (b) larger positive bias in which a significant number of free electrons are induced in the conduction band [63].

There are four possible TFT structures as depicted in Fig. 4.2. These are categorized into top and bottom gate structures, and each of them is classified again into coplanar and staggered structures. Basically, these structures are very similar to those of crystalline silicon MOSFETs. However, the main difference is that the bulk of the TFT channel layer is electrically being floated because they are fabricated on glass or plastic substrates. Generally, the bottom gate-staggered structure has been adopted for a-Si:H TFT fabrication due to its excellent interface properties between the channel and the gate dielectric, since these layers can be successively deposited without breaking vacuum. In the meantime, the top gate-coplanar structure has generally been employed in the poly-Si TFTs because the good quality of the poly-Si films can be obtained by laser crystallization. In addition, the implementation of fully self-aligned structure is possible, in which the TFTs have low parasitic capacitance.

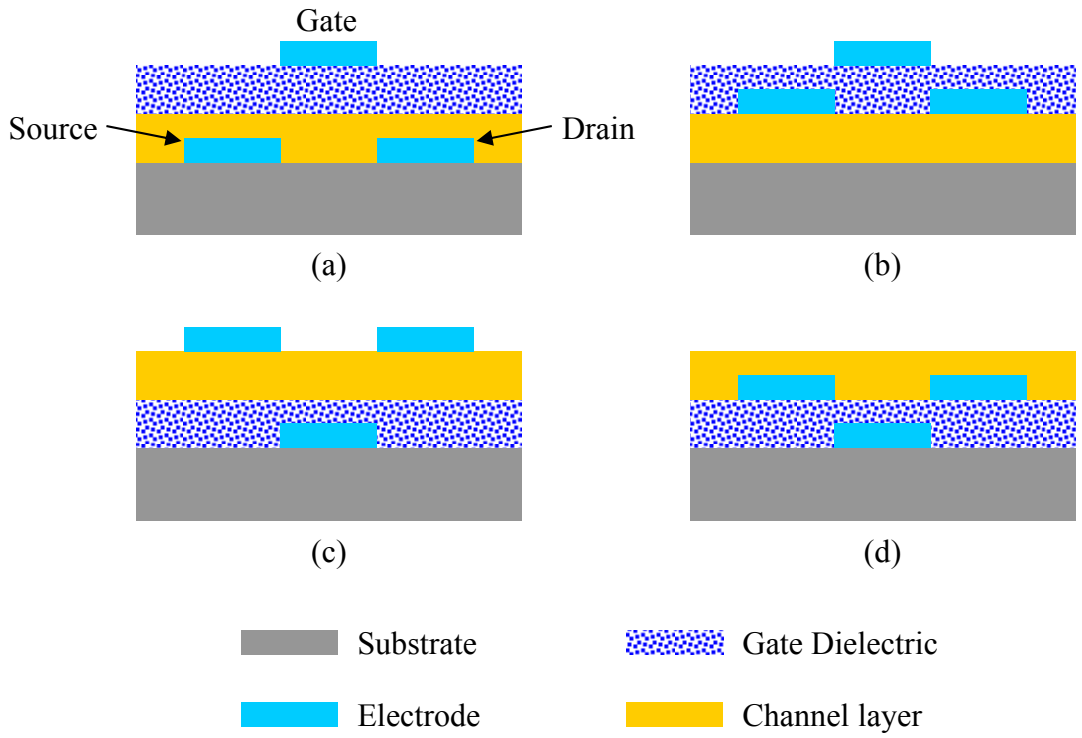


Fig. 4.2. Simplified cross-sectional view of basic TFT structures: (a) top gate-staggered, (b) top gate-coplanar, (c) bottom gate-staggered, and (d) bottom gate-coplanar.

It is desirable to select top-gate structure for the fabrication of nc-Si:H TFTs to take advantage of the highest carrier mobility available at the top of the nc-Si:H film as discussed in Section 3.1. Either coplanar or staggered source/drain contacts can be used. The coplanar structure is simple, but the etch selectivity between a highly doped nc-Si:H contact layer and an intrinsic nc-Si:H channel is small, so over-etching is difficult to prevent, thus causing etch-damage to the surface of the channel layer [64]. On the other hand, the staggered

geometry provides a wider process window for source/drain patterning and therefore, the damage-free interface. In addition, the deposition of the gate dielectric can successively follow the growth of the channel layer without breaking vacuum so as to preserve high electrical integrity at the nc-Si:H/SiO_2 interface. However, the series resistance of the intrinsic nc-Si:H channel layer can limit TFT performance in the staggered structure, since carriers must travel through an intrinsic nc-Si:H region on their way to/from the channel [65], which will be discussed in Section 5.3.

4.2 Fabrication Process

By using the highest-quality SiO_2 and nc-Si:H films previously discussed in Chapter 2, n- and p-channel top-gate nc-Si:H TFTs with staggered source/drain electrodes were fabricated as follows. First, 50-nm thick Cr was sputtered on a Corning 1737 glass substrate at room temperature. Then, highly n- and p-doped nc-Si:H contact layers of the same thickness were deposited by PECVD at 260°C for n- and p-channel TFT fabrication, respectively. After the nc-Si:H contact layer and Cr were patterned to form source/drain regions by reactive ion etching (RIE) and wet chemical etching, respectively, a 100-nm thick nc-Si:H channel layer and a 200-nm thick gate SiO_2 were successively deposited using PECVD at 260°C. Finally, contact holes were opened to the bottom Cr layer, and a 300-nm thick Al electrode was sputtered and patterned by wet chemical etching. Fig. 4.3 shows the cross-sections of the TFT fabrication sequence using 3 photomasking steps. Details regarding

the design of test chips for the evaluation of the nc-Si:H films, TFT devices, and circuits are presented in Appendix A.

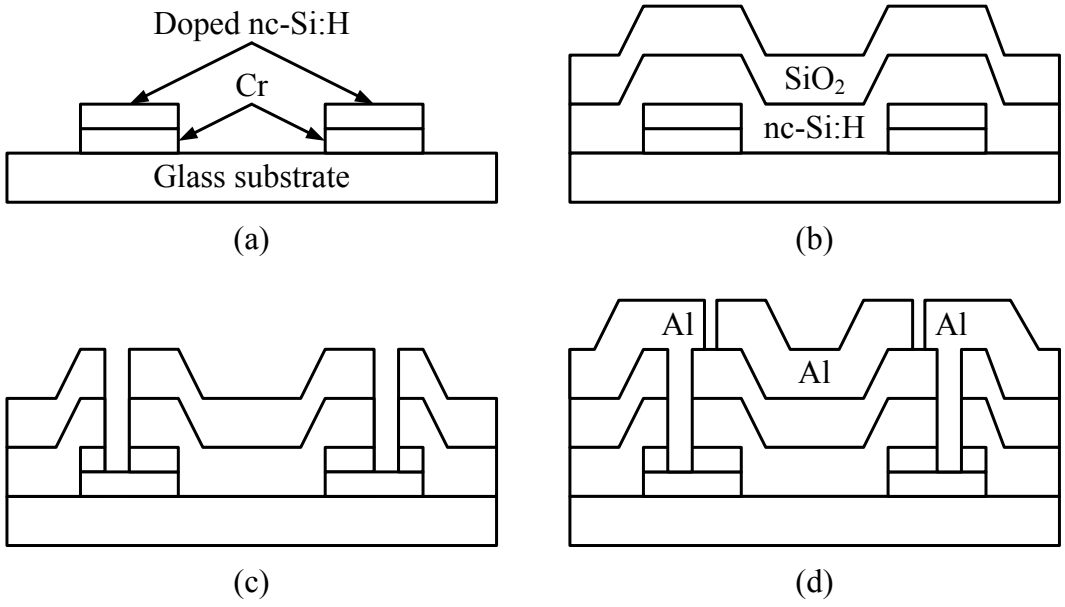


Fig. 4.3. Schematic cross-sections of the fabrication sequence of the top gate-staggered nc-Si:H TFTs using 3 photomasking steps: (a) source/drain contacts (mask 1), (b) bilayer deposition, (c) contact hole formation (mask 2), and (d) metallization (mask 3).

The nc-Si:H channel layer was deposited using 99% H_2 dilution of SiH_4. The RF power and pressure were 90 W and 900 mTorr, respectively. For the growth of n^+ and p^+ nc-Si:H contacts, 1% PH_3 and 1% $B(CH_3)_3$ (trimethylboron, TMB) both diluted in H_2 were used as the source gas with 2% flow ratio of PH_3-to-SiH_4 and 0.5% flow ratio of TMB-to-SiH_4,

respectively. The other process parameters, such as the RF power and pressure, were the same as in the channel layer deposition.

4.3 Electrical Characteristics

The TFT characteristics were measured using a Keithley 4200 semiconductor characterization system. The channel width W and length L of all the TFTs described here were 200 and 50 μm, respectively. In order to minimize the hysteresis effect of the SiO_2 gate dielectric on TFT performance as previously discussed in Section 2.3, the TFT characteristics were measured after the third sweep to saturate charge trapping in SiO_2. Device parameters governing TFT performance were extracted from the saturation characteristics based on conventional MOSFET theory,

$$I_{DS,sat} = \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_{GS} - V_T)^2, \tag{4.1}$$

where $I_{DS,sat}$ is the drain current in the saturation region, μ is the field effect mobility of carriers, C_{OX} is the oxide capacitance, V_{GS} is the gate voltage, and V_T is the threshold voltage. The threshold voltage of the TFTs is extracted from the intercept of the $\sqrt{I_{DS}}$-V_{GS} line on the V_{GS} axis as shown in Fig. 4.4. The field effect mobility of carriers are then calculated from the transconductance relationship expressed by

$$g_{m,sat} = \frac{\partial I_{DS,sat}}{\partial V_{GS}} = \mu C_{OX}\frac{W}{L}(V_{GS} - V_T), \tag{4.2}$$

where $g_{m,sat}$ is the transconductance in the saturation region. The subthreshold slope S is retrieved using the expression,

$$S = \frac{dV_{GS}}{d(\log I_{DS})} = \ln 10 \frac{dV_{GS}}{d(\ln I_{DS})}. \quad (4.3)$$

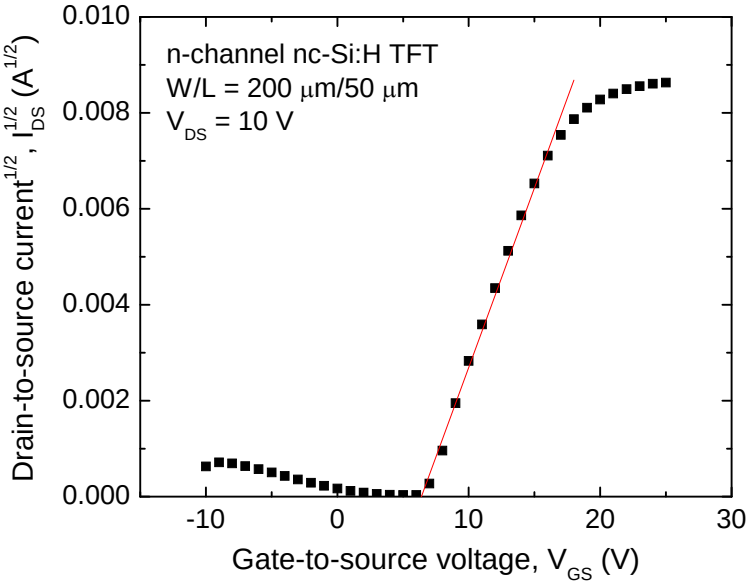
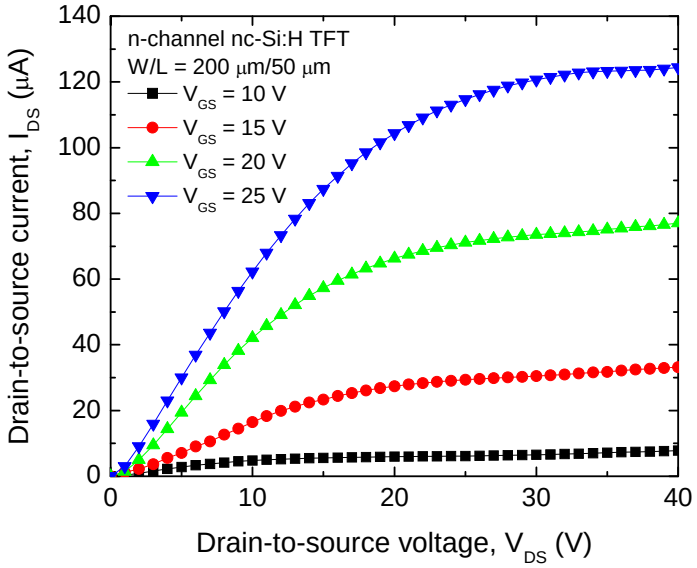


Fig. 4.4. Plot of square root of the drain current versus gate voltage for the extraction of TFT parameters.

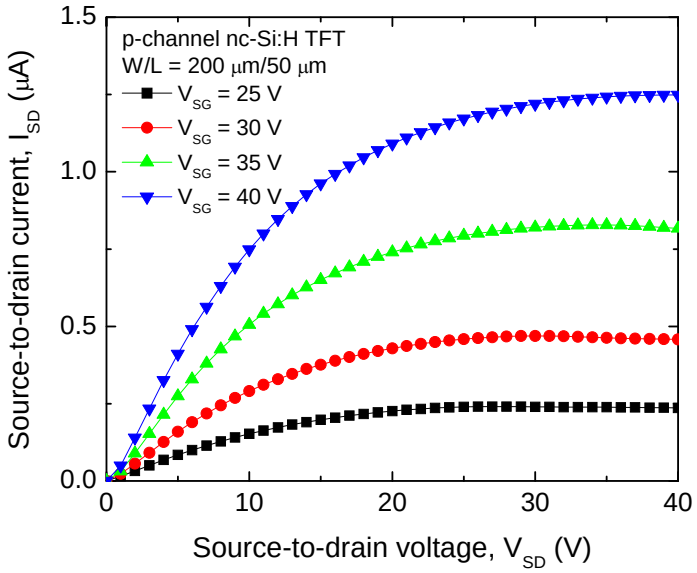
The n-channel TFTs demonstrate a threshold voltage of 6.4 V, a field effect mobility of electrons of 15.54 $cm^2/V{\cdot}s$, a subthreshold slope of 0.67 V/decade, and an on/off current ratio I_{on}/I_{off} of 10^5, while the corresponding p-channel TFTs exhibit a threshold voltage of -26.2 V, a field effect mobility of holes of 0.24 $cm^2/V{\cdot}s$, a subthreshold slope of 4.72 V/

decade, and an on/off current ratio of 10^4. It should be noted that a deviation from the linearity of $\sqrt{I_{DS}}$-V_{GS} is observed at high gate bias regime, mainly due to high parasitic resistance at source/drain terminals, which will be discussed in Section 5.3.

The output (drain current versus drain bias) and transfer (drain current versus gate bias) characteristics along with the gate leakage current of the fabricated n- and p-channel nc-Si:H TFTs are presented in Figs 4.5 and 4.6, respectively. Obviously, current crowding near the origin of the output characteristics is not observed here, which indicates that the highly doped n- and p-type nc-Si:H layers provide good ohmic contact with the intrinsic layer. The effect of the gate leakage on TFT performance is also found to be minimal as the gate leakage is below 0.1 nA, which is at least an order of magnitude lower than the drain leakage for the measurement range considered here. However, the drain leakage current is observed to be in the range of several nanoamperes, and significantly increases with increasing gate and drain bias. These high values not only cause poor image display quality but also high power consumption in the driving circuits [66].

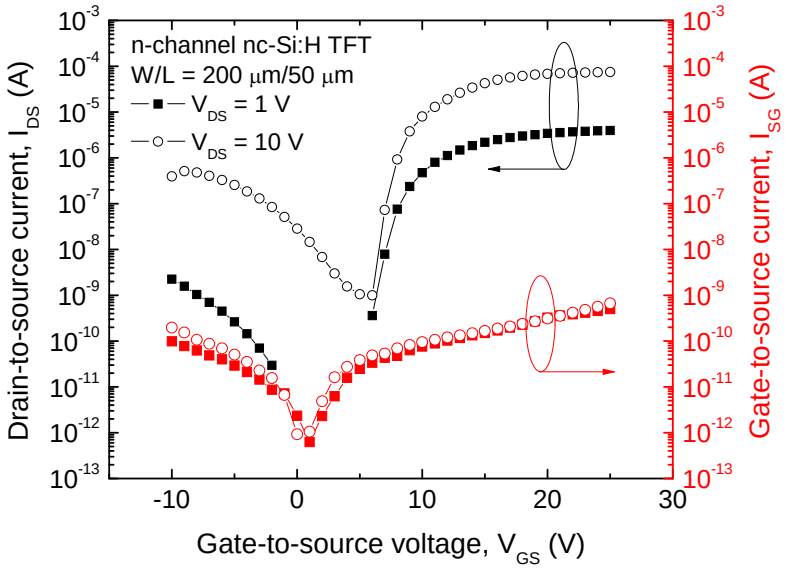


(a)

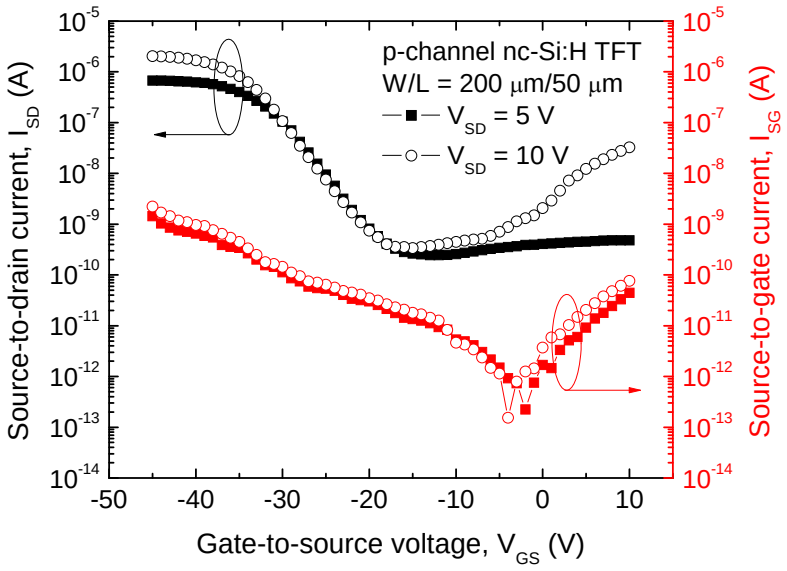


(b)

Fig. 4.5. Output characteristics of the fabricated nc-Si:H TFTs: (a) n-channel and (b) p-channel.



(a)



(b)

Fig. 4.6. Transfer and gate leakage characteristics of the nc-Si:H TFTs: (a) n-channel and (b) p-channel.

4.3.1 Circuit Implementation

In order to investigate the impact of the leakage current on TFT performance, nc-Si:H TFT inverters with a diode-connected n-channel TFT load have been implemented. Here, the channel width W and length L of pull-down and pull-up transistors are 200 and 50 μm, respectively. The schematic diagram, optical micrograph, and voltage transfer characteristics (VTC) of the TFT inverters are presented in Figs. 4.7(a), (b), and (c), respectively. Here, the applied supply voltages are V_{DD} = 20 V and V_{SS} = 0 V. The inverter demonstrates a reduced output swing, with the output high voltage V_{OH} of 19 V and output low voltage V_{OL} of 6.88 V, which are slightly lower than the applied V_{DD} and far higher than V_{SS}, respectively. The reduction in the output swing of the inverter is due to the high leakage current in the TFTs. While the leakage current in the driver TFT slightly pulls down V_{OH} from V_{DD} = 20 to 19 V, the leakage in the load TFT prevents V_{OL} from reaching V_{SS} = 0 V. Therefore, a good understanding of the off-state conduction mechanisms in the nc-Si:H TFTs is imperative, which will be discussed in Section 5.1.

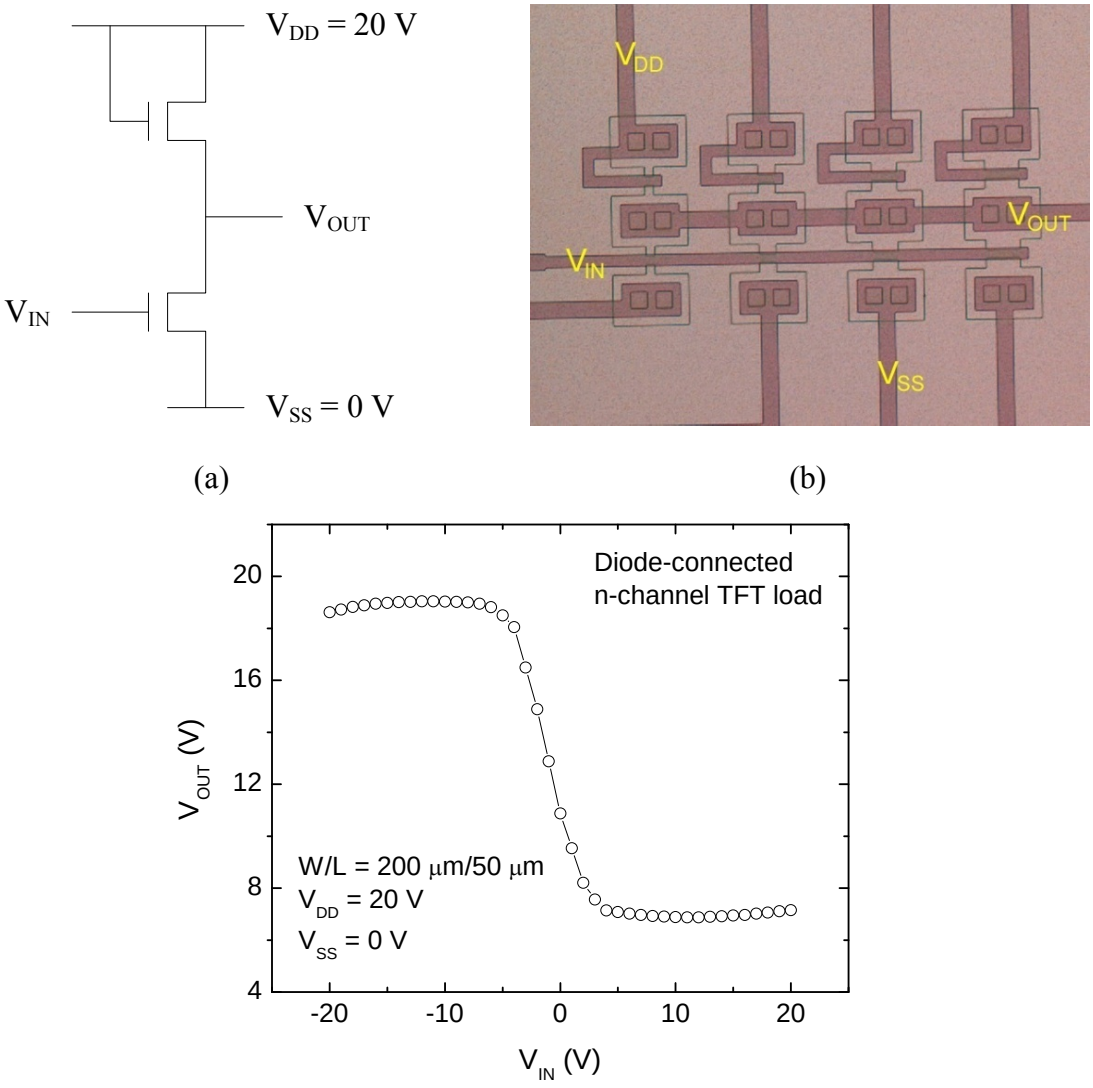


Fig. 4.7. nc-Si:H TFT inverters with a diode-connected n-channel TFT load: (a) the schematic diagram, (b) optical micrograph, and (c) voltage transfer characteristics (VTC) of the inverters.

4.3.2 Post-Fabrication Thermal Annealing

Lastly, the influence of post-fabrication annealing on transistor performance is presented. Here, the annealing temperature slightly lower than the deposition temperature of the nc-Si:H films was chosen because hydrogen effusion from the nc-Si:H channel layer, could generate defects. The n-channel TFTs were annealed in a N_2 ambient at a temperature of 240°C for 60 min. After annealing, the threshold voltage is reduced by a factor of 1.3 from 6.4 to 4.9 V, the field effect mobility of electrons is increased by a factor of 1.7 from 15.54 to 26.13 $cm^2/V \cdot s$, the subthreshold slope is decreased by a factor of 1.3 from 0.67 to 0.52 V/decade, and the on/off current ratio is increased by an order of magnitude from 10^5 to 10^6. The resultant transconductance curves before and after annealing are compared in Fig. 4.8. Although the TFTs received thermal annealing, the transconductance still shows a significant reduction at high gate bias. The transconductance degradation, which significantly limits the on-state performance of the TFTs [67], will be discussed in Section 5.3.

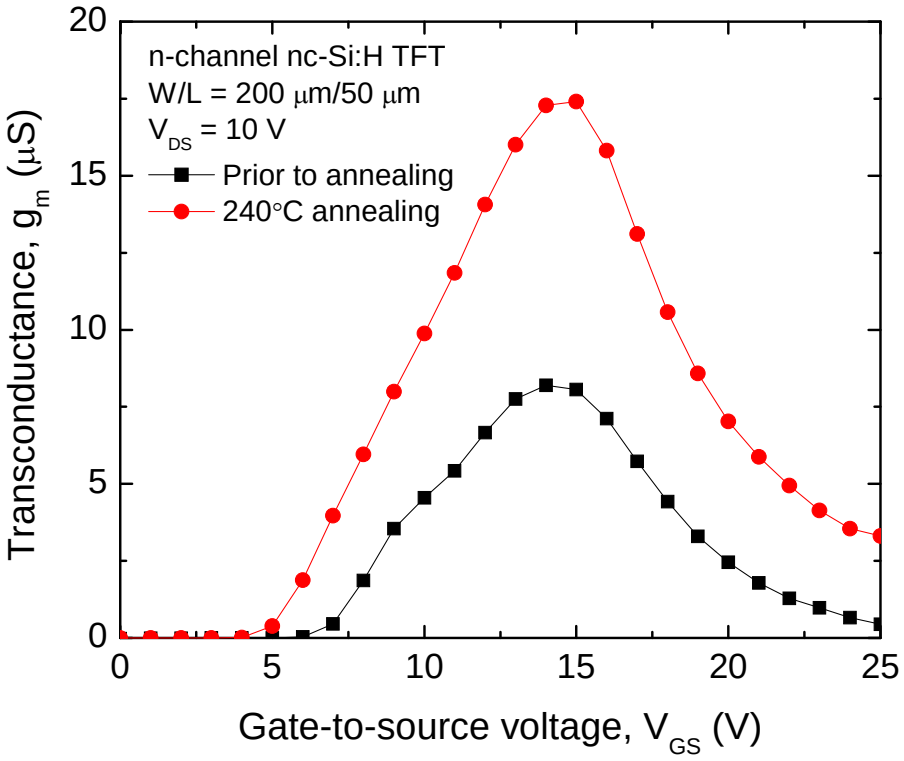


Fig. 4.8. Transconductance of the n-channel nc-Si:H TFTs before and after thermal annealing. In both cases, transconductance significantly degrades at high gate bias.

Chapter 5
Non-idealities in TFT Behavior

Ideal TFTs provide high field effect mobility and low leakage current along with high electrical stability. However, as previously discussed, departures from the ideal case, i.e., the high leakage current, transconductance degradation, and threshold voltage instability which significantly limit TFT performance, are generally observed in the top-gate nc-Si:H TFTs. Therefore, physical insight into these mechanisms is crucial; a good understanding of the anomalous mechanisms are expected to aid the design of the nc-Si:H TFTs so as to improve the performance of the active-matrix backplane. In this chapter are described the mechanisms responsible for non-ideal TFT behaviors. Strategies for their possible solutions are also discussed.

5.1 Leakage Current Mechanisms

As previously discussed in Section 4.3, the top-gate nc-Si:H TFTs currently fall short of their poly-Si counterparts, particularly in terms of the leakage current I_L which is in the

range of several nanoamperes and has a strong dependence on gate and drain bias as observed. In the active-matrix TFT backplanes, these high values not only cause signal loss in pixels over the frame period, but they also lead to large power consumption in driving circuits. Thus a good understanding of the off-state conduction mechanisms is imperative; unfortunately, very little attention has been paid to address this issue to date [68].

In general, significant leakage current mechanisms in poly-Si TFTs have been attributed to (1) resistive current at low gate bias and to (2) junction leakage current at high gate bias [69]. For example, in p-channel TFTs, the former arises when the applied gate bias is not positively larger enough to form an n-layer in the channel; in other words, when the gate bias is larger than flatband condition but smaller than some equivalent threshold voltage for electron accumulation, in which the gate bias is high enough to deplete accumulated holes but not enough to accumulate electrons to form an n-channel. In this case, the leakage current can be ascribable to the ohmic current through the bulk channel layer. This resistive component is controlled by the diffusion of holes in the bulk channel, and therefore the minimum level of the resistive current is determined by the peak concentration of holes [70].

As the gate bias increases further, i.e., when the gate bias is larger than the threshold voltage for electron accumulation, there is formation of an n-channel and consequently, a reverse-biased p-n junction between drain and channel as depicted in Fig. 5.1.

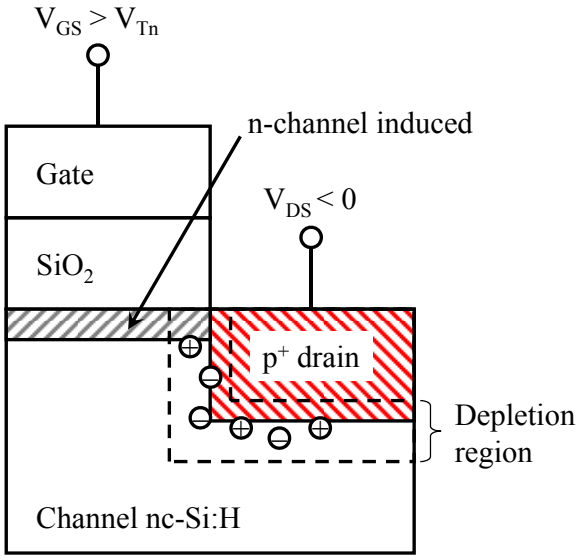


Fig. 5.1. Reverse-biased p-n junction showing the generation of carriers trapped at grain boundaries in the drain depletion region.

In this case, holes trapped at grain boundary states in the drain depletion region can be excited to the valence band by (a) thermal emission [71], (b) field emission [72], and (c) thermionic-field (Poole-Frenkel) emission [73] as illustrated in Fig. 5.2. The thermal emission current I_{TE} is nearly independent of the applied bias,

$$I_{TE} = I_{TE0}\exp(-E_a/kT), \tag{5.1}$$

where I_{TE0} is a constant independent of temperature, k is the Boltzmann constant, and T is temperature [74]. Here, E_a is the activation energy of the thermal emission current, which measures the difference between the edge of the valence band and the energy of the grain boundary states within kT of the Fermi level, since there are fewer free carriers in the off-

state and therefore, the Fermi level in the TFT channel is pinned at mid-gap states [74]. For this reason, the activation energy of the thermal emission current is expected to be approximately half the band gap of the channel material.

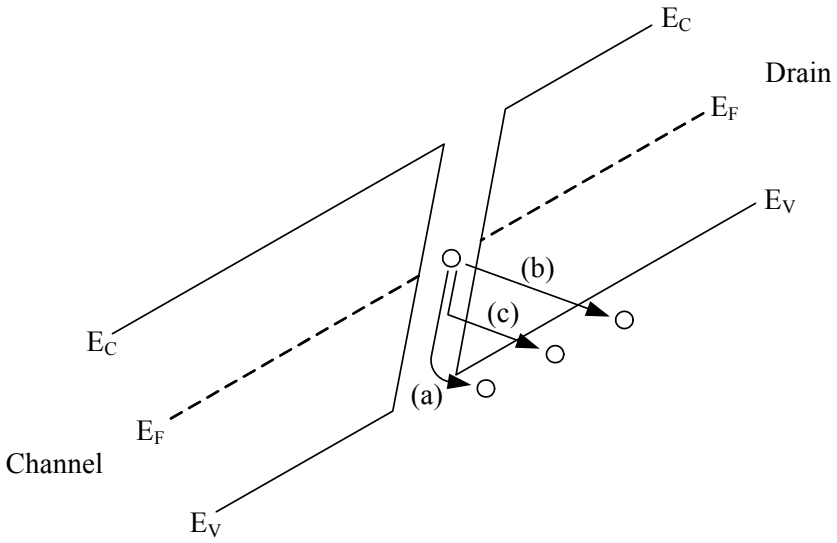


Fig. 5.2. Schematic illustration of the leakage mechanism model: (a) thermal emission, (b) field emission, and (c) Poole-Frenkel emission [74].

The field emission current I_{FE}, which is due to the field ionization of trapped holes tunneling through the potential barrier into the valence band, has the strongest dependence on the applied field but is essentially independent of temperature. Therefore, it dominates at low temperature and high field conditions [71]. The field emission current is given by

$$I_{FE} = AE \exp(-B/E), \tag{5.2}$$

where A is a constant in $cm \cdot V^{-1}$, E is the electric field, and B is a positive constant independent of the electric field or temperature [68].

Poole-Frenkel emission is due to field-enhanced thermal excitation of trapped holes in the valence band [73]. In this case, the applied field causes the barrier to become low and thin enough so that thermal emission prior tunneling can easily occur. The Poole-Frenkel mechanism gives an emission current of the form

$$I_{PF} = I_{PF0}\exp\left(\beta\sqrt{E_{pk}}\right), \tag{5.3}$$

where I_{PF0} is the generation current at zero electric field, E_{pk} is the peak electric field given by $E_{pk} = |V_{GS} - V_{DS} - V_{FB}|\varepsilon_{OX}/t_{OX}\varepsilon_{Si}$, and β is the Poole-Frenkel coefficient given by $\beta = q^{3/2}/\sqrt{\pi\varepsilon_{Si}}kT$ [70].

In order to identify the underlying off-state conduction mechanisms in the top-gate nc-Si:H TFTs, we examined the behavior of the leakage current in the p-channel TFTs at different temperatures: 23, 50, 75, and 100°C. The resultant Arrhenius plot and the corresponding activation energies for different gate and drain bias are depicted in Figs. 5.3 and 5.4, respectively.

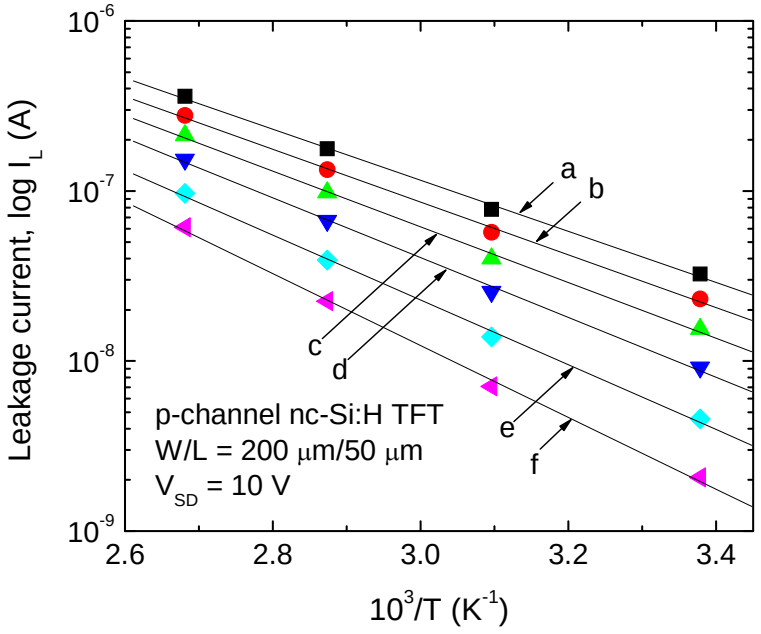


Fig. 5.3. Temperature dependence of the leakage current: Arrhenius plot at V_{SD} = 10 V for different V_{GS} (along with the extracted E_a values), a: V_{GS} = 10 V, E_a = 0.32 eV, b: V_{GS} = 8 V, E_a = 0.33 eV, c: V_{GS} = 6 V, E_a = 0.35 eV, d: V_{GS} = 4 V, E_a = 0.37 eV, e: V_{GS} = 2 V, E_a = 0.40 eV, and f: V_{GS} = 0 V, E_a = 0.45 eV.

First, the temperature dependence of the leakage current in Fig. 5.3 can rule out field emission from the possible mechanisms [71]. Two different regimes of operation can also be identified based on the dependence of the activation energy on gate and drain bias observed in Fig. 5.4; i.e., the subthreshold and electron accumulation regions with a demarcation of around V_{GS} of 0 V.

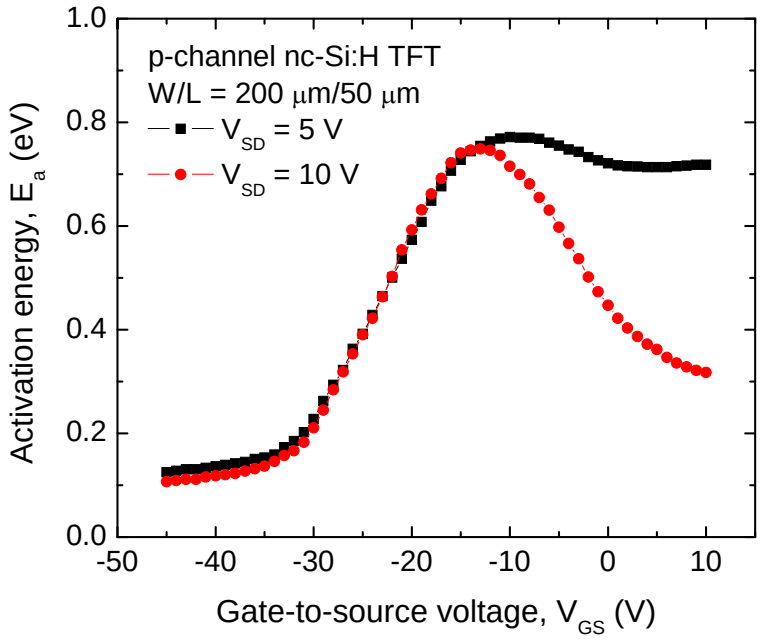


Fig. 5.4. Dependence of the activation energy on V_{GS} at V_{SD} = 5 V and 10 V. The activation energy continues to decrease at high drain bias (= 10 V), while it becomes virtually independent of gate bias at low drain bias (= 5 V), suggesting that two different leakage mechanisms exist.

In the electron accumulation region (high gate bias regime), the activation energy at high drain bias (= 10 V) continues to decrease as gate bias increases up to 10 V, which is reminiscent of Poole-Frenkel (PF) emission in Eq. (5.3). If Poole-Frenkel emission prevails, it is expected that the leakage current versus $\sqrt{E_{pk}}$ will show a linear relationship as in Fig. 5.5. Here, a straight line fits the data reasonably well, and its slope $\beta = 0.0098\ cm^{1/2}\cdot V^{-1/2}$ is close to the theoretical Poole-Frenkel coefficient of $0.0085\ cm^{1/2}\cdot V^{-1/2}$ [75]. Therefore, there

is strong evidence to suggest that Poole-Frenkel emission is predominant at high gate and drain bias regime.

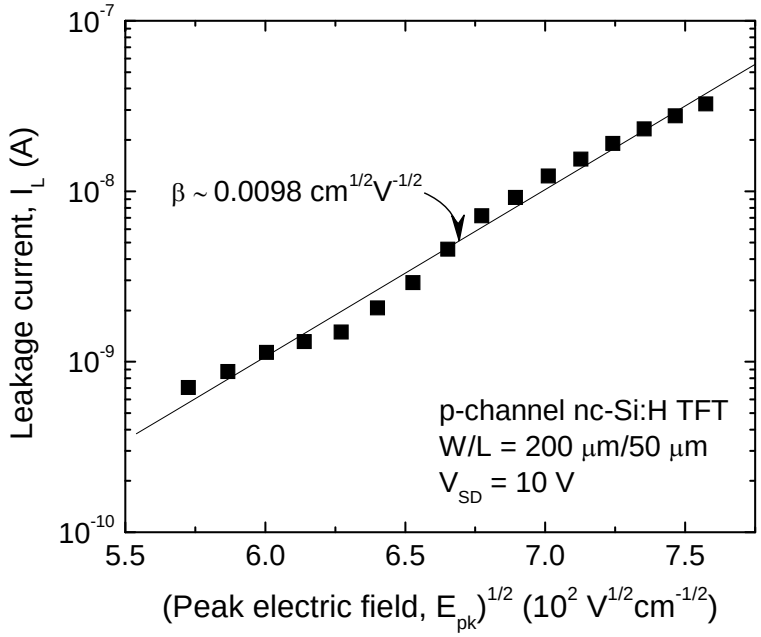


Fig. 5.5. Leakage current versus $\sqrt{E_{pk}}$ at V_{SD} = 10 V for the fabricated TFT. A straight line fits the data reasonably well, and its slope $\beta = 0.0098\ cm^{1/2}\cdot V^{-1/2}$ is close to the theoretical PF coefficient of $0.0085\ cm^{1/2}\cdot V^{-1/2}$, which is strong evidence that PF emission is predominant in this bias region.

To the contrary, the activation energy at low drain bias (= 5 V) becomes virtually independent of the gate bias, i.e., 0.72 ± 0.002 eV, which is retrieved from the average and

standard deviation of the activation energy values between V_{GS} = 0 and 10 V. This behavior is reminiscent of thermal emission in Eq. (5.1). The observed range of values for the activation energy is indeed about half the band gap of the nc-Si:H channel material, albeit with small variations of the order of kT around the position of the Fermi level. Here, the band gap of nc-Si:H is slightly larger than that of crystalline silicon and can range from 1.3 to 1.6 eV depending on the crystalline volume fraction [76].

In the subthreshold region (low gate bias regime), the leakage current has a weaker gate and drain bias-dependence as observed in Fig. 4.6(b), suggesting that it is determined by the intrinsic resistivity of the channel layer. In this case, the dependence of the TFT channel dimensions on the leakage current can help distinguish the resistive and junction leakage components, in which the former is proportional not only to 1/ L but also to W [77]. Indeed as we observe in Fig. 5.6, the leakage current increases linearly with the channel width. As previously mentioned, this resistive component is controlled by diffusion of holes in the bulk channel. Therefore, the increase in the resistive leakage with gate bias can be attributed to the increase in the peak concentration of holes. This can explain the decrease in the activation energy from 0.77 to 0.72 eV for V_{SD} = 5 V, observed in Fig. 5.4.

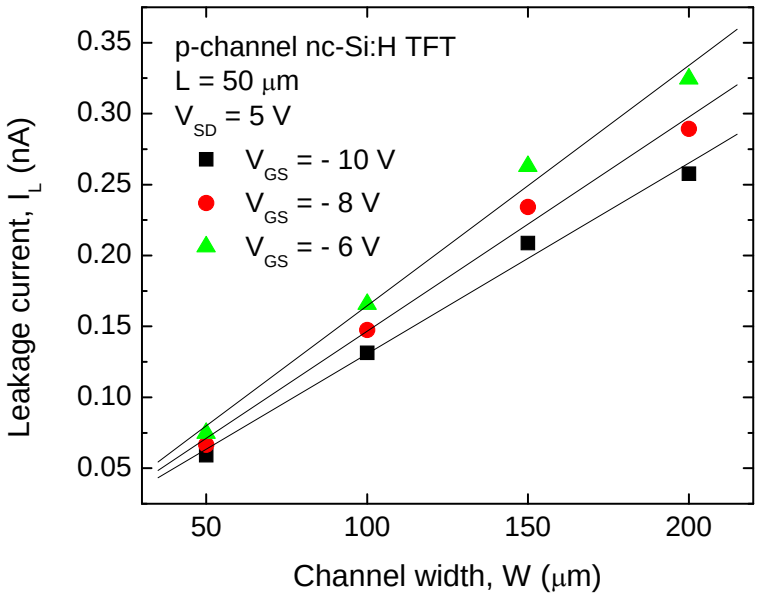


Fig. 5.6. Linear dependence of the leakage current on various W with a fixed L = 50 μm for different V_{GS} = -10, -8, and -6 V, which indicates that the leakage current in this bias region can be attributed to the resistive current.

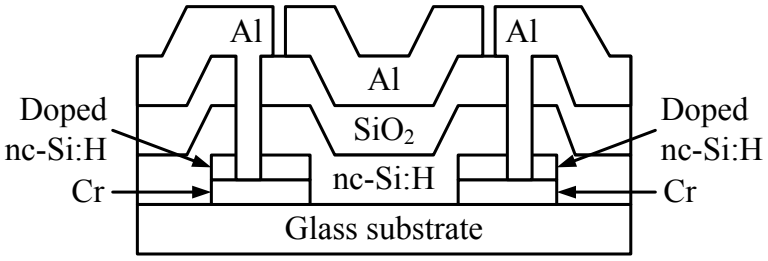
In summary, the mechanisms responsible for the off-state conduction in the top-gate nc-Si:H TFTs are (1) ohmic conduction flowing through the bulk nc-Si:H channel, which appears to be prevalent under low gate bias, and the junction leakage current under high gate bias, which can be attributed to (2) thermal emission of trapped carriers at low drain bias and to (3) Poole-Frenkel emission at high drain bias.

5.2 Leakage Suppression

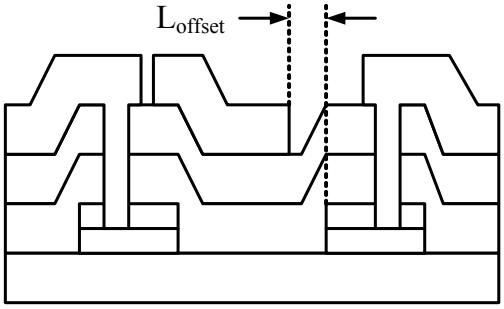
5.2.1 Offset-Gated Structure

It is clear from the previous analysis that to suppress the leakage current in the top-gate nc-Si:H TFTs, particularly at a high bias regime, a reduction in the peak electric field at the drain vicinity is critical. It might be possible to achieve this by employing offset-gated [78] or lightly-doped drain (LDD) [79] structure as in poly-Si TFTs. It is along these lines that we examine offset-gated nc-Si:H TFTs, where an undoped region is introduced between gate and drain electrodes, and study the effect of the offset region on TFT performance.

n- and p-channel nc-Si:H TFTs with various offset lengths were fabricated. Their fabrication process was the same as described in Section 4.2. The channel width and length of all the TFTs were 200 and 50 μm, respectively. The length of offset L_{offset} was varied from 0 (non-offset) to 4 μm. Schematic cross-sections of the non-offset and offset-structured TFTs are compared in Fig. 5.7, along with an optical micrograph of a fabricated TFT with 4-μm offset region. Here, the effective length of the offset measured is 3.8 μm.



(a)



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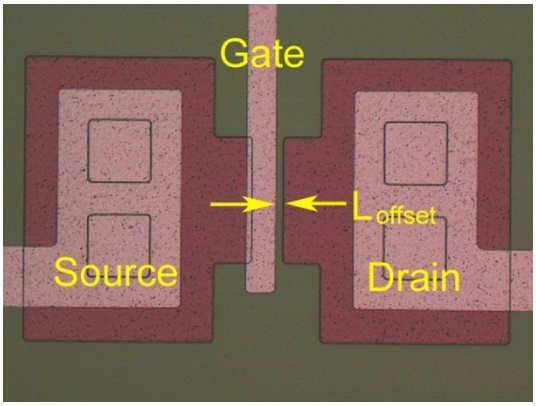


(c)

Fig. 5.7. Schematic cross-sections of (a) the non-offset and (b) offset-structured TFTs, and (c) an optical micrograph of a fabricated 4-μm offset-gated TFT.

In order to evaluate the impact of the offset region on transistor performance, the transfer characteristics of the non-offset and offset-gated TFTs are compared in Fig. 5.8. In both n- and p-channel devices, the non-offset TFTs show a strong increase in the leakage current with increasing gate bias. To the contrary, this increase in the offset-gated structure is drastically reduced, while the on-current is not significantly affected. In particular, the leakage current remains virtually independent of the gate bias in the p-channel TFT having a 4-μm offset as observed in Fig. 5.8(b).

Further detailed analysis of the offset-length dependence on TFT performance was performed, and the result is summarized in Table 5.1. Here, we extracted the values of series resistance R_s for different offset lengths by subtracting the channel resistance R_{ch} from the TFT on-resistance R_{ON} [80],

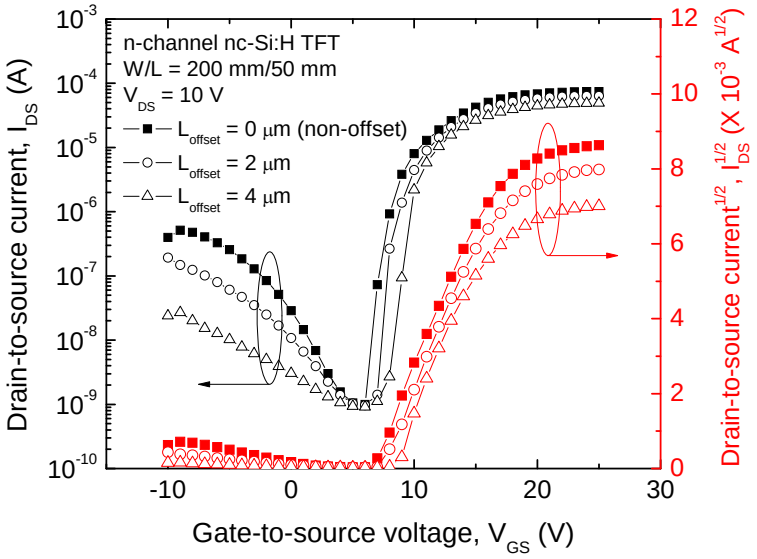
$$R_{ON} = \frac{\partial V_D}{\partial I_D} = R_{ch} + R_s, \tag{5.4}$$

where R_{ch} is given approximately by,

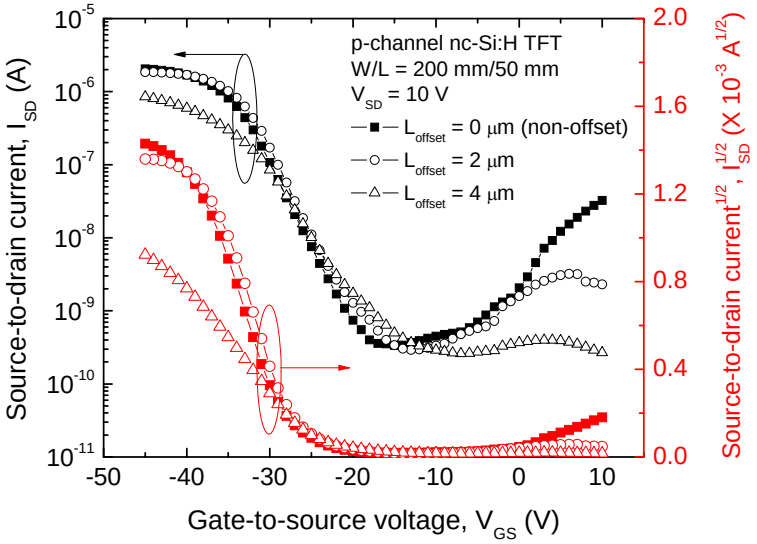
$$R_{ch} = \frac{L}{W\mu C_{OX}(V_G - V_T)}. \tag{5.5}$$

We also define a leakage current increase ratio as a measure of the increase in the leakage current with increasing V_{GS}, in which we have used the ratio of maximum to minimum leakage current [78]. The maximum leakage current here was taken at V_{GS} = -10 V for n-channel and at V_{GS} = 10 V for p-channel devices. Correspondingly, the minimum leakage current was taken at V_{GS} = 5 V for n-channel and at V_{GS} = -15 V for p-channel

devices. As the offset length increases, series resistance increases, which can lead to an increase in the threshold voltage and to a decrease in the field effective mobility. However, except for the p-channel 4-μm offset case, these values are slightly changed, while the leakage current increasing ratio is dramatically reduced for all cases. Compared to the non-offset TFTs, the leakage current is reduced by more than a factor of 2 for the n-channel with 2-μm offset and substantially more in the TFTs with a larger offset. The same is observed for the p-channel TFTs. This result indicates that the offset region between gate and drain electrodes is quite effective in suppressing the leakage current without significant compromise of the on-state performance.



(a)



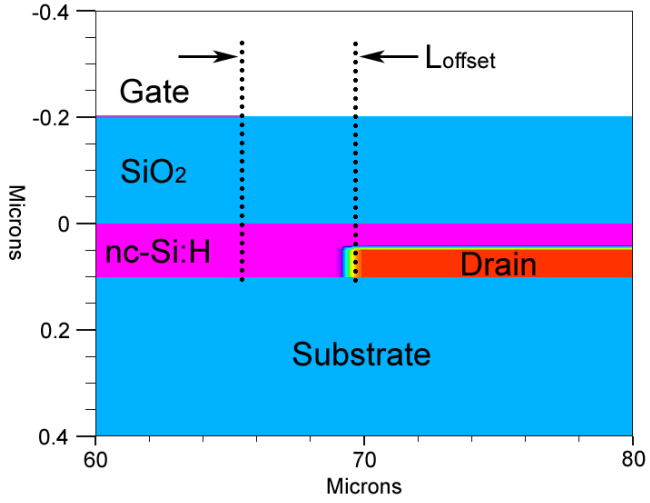
(b)

Fig. 5.8. Comparison of the transfer characteristics of the non-offset and offset-gated TFTs: (a) n-channel and (b) p-channel.

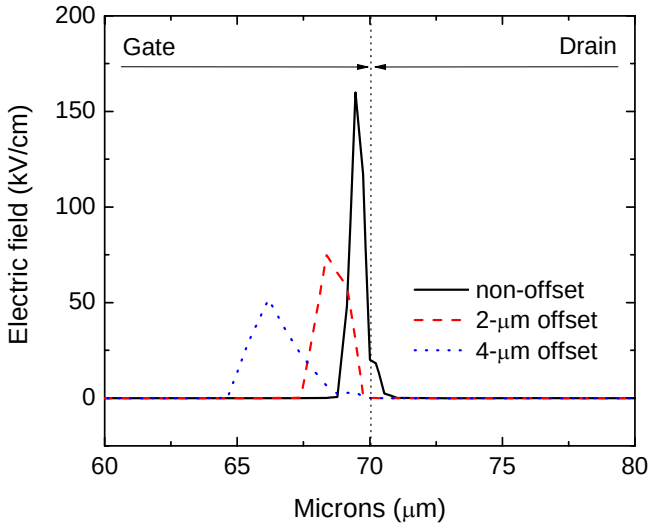
Table 5.1. Effect of various offset lengths on TFT performance.

TFT	L_{offset} (μm)	R_s (Ω)	V_T (V)	μ ($cm^2/V{\cdot}s$)	I_L increase ratio
n-channel	0	89 k	6.5	16.6	515
	2	112 k	7.2	15.9	200
	4	158 k	8.0	15.5	29.7
p-channel	0	2.46 M	-26.6	0.31	96.4
	2	2.98 M	-25.8	0.31	11
	4	9.31 M	-23.8	0.06	1.53

For deeper insight into the main factors that result in high leakage current, the electric field along the channel of off-state n-channel TFTs (biased at V_{GS} = -10 V and V_{DS} = 10 V) with various offset lengths was computed using ATLAS [52]. The test structure with staggered source/drain configuration and the simulated electric-field profiles along the channel are depicted in Figs. 5.9(a) and (b), respectively. As observed here, the maximum electric field in both 2-μm and 4-μm offset-gated TFTs is less than half of that in the non-offset structure. This is expected since the drain bias drops across the highly resistive undoped (i.e., offset) region. The resulting decrease in the peak electric field reduces carrier emission from grain boundary traps in the drain depletion region, thus effectively suppressing the leakage current.



(a)



(b)

Fig. 5.9. Electric-field computation in the non-offset and offset-gated TFTs: (a) TFT test structure used in simulations, and (b) simulated electric-field profiles along the channel. The n-channel TFTs with L = 50 μm were biased in the off-state (V_{GS} = -10 V and V_{DS} = 10 V).

5.2.2 Channel Compensation Doping

As discussed in Section 3.1, the as-deposited (undoped) nc-Si:H material shows slightly n-type properties (high dark conductivity) due to oxygen impurities incorporated during film growth, which can cause high minimum leakage current (i.e., high resistive current) in the TFTs. In our case, at TMB/SiH_4 of 0.2%, a small amount of boron added to the films compensated oxygen contaminants and nearly intrinsic films could be grown with a dark conductivity of ~10^{-8} S/cm, which is two orders of magnitude lower than that of the as-deposited films.

The influence of the channel compensation doping on n-channel TFT performance is shown in Fig. 5.10. It is observed that the leakage current at high negative gate bias (= -10 V) is suppressed more than an order of magnitude in the compensated TFT. However, the compensated TFT shows a higher threshold voltage of 9.2 V and a lower field effect mobility of 8.11 $cm^2/V \cdot s$ with a slightly reduced on-current compared to the TFT having the undoped channel. This is possibly because compensation doping by TMB might result in higher defect densities in the channel layer [60], which can be supported by a higher subthreshold slope of 1.11 V/decade observed in the compensated TFTs. However, in this case, the leakage current should increase according to the increased defect states.

Another possible reason could be that the channel layer was over-compensated due to the narrow process window of the compensation doping as mentioned in Section 3.3. This is deduced from the fact that the minimum leakage current of the TFTs, which is related to the

intrinsic resistivity of the channel layer, has not decreased by the compensation doping. If the channel was over-compensated, the TFTs might operate in inversion-mode, which is known to show lower on-current but also have lower leakage current [66]. Therefore in our case, it would be reasonable to conclude that the channel layer was more p-doped by compensation than desired. As Platz et al. pointed out [81], the need to tailor the level of boron doping to the case-by-case oxygen contamination in the nc-Si:H films and to precisely control doping within such a very narrow window make this method unfeasible.

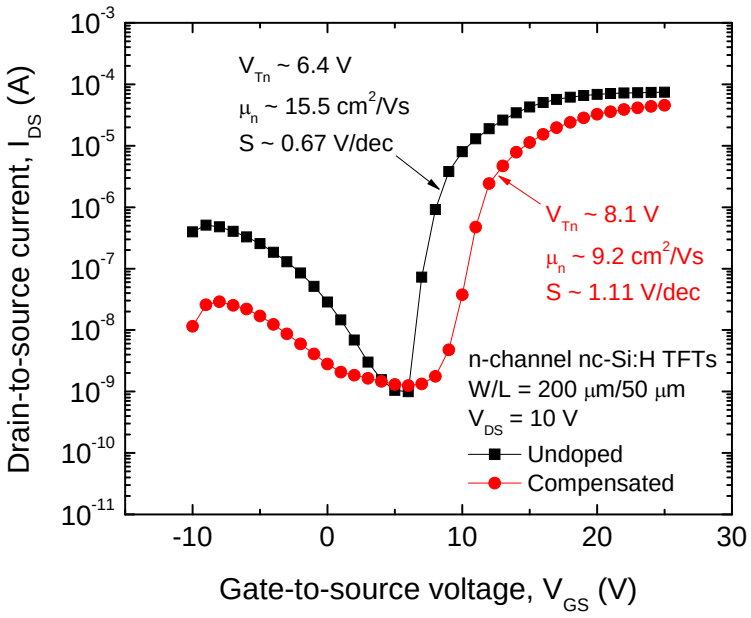
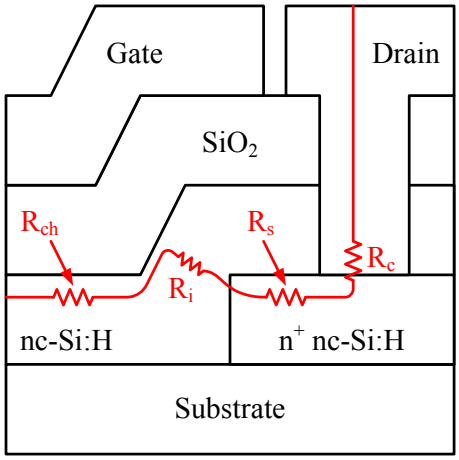


Fig. 5.10. Effect of compensation doping on the transfer characteristics of the n-channel nc-Si:H TFTs.

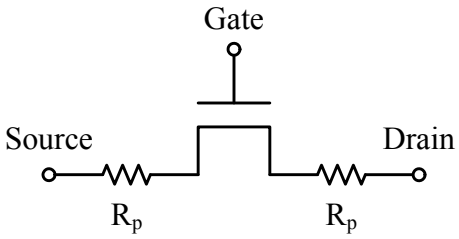
5.3 Transconductance Degradation

As discussed so far, TFT performance can be strongly affected by the quality of the gate dielectric, the channel layer, and their interface. Many geometrical or extrinsic factors including the channel length, nc-Si:H thickness, and the quality of the source/drain nc-Si:H contacts can also influence transistor performance [80]. These factors disclose themselves as parasitic resistance in the TFTs. If parasitic resistance is too large, ohmic contact cannot be obtained and the crowding behavior of the drain current is usually observed near the origin of the TFT output characteristics [82]. As discussed in Section 4.3, we have not observed the current crowding behavior in our TFTs, which indicates that the developed n^+ and p^+ nc-Si:H layers provide good ohmic contact with the channel layer. However, parasitic resistance can still affect transconductance to a large degree as we observe in Fig. 4.8; the transconductance shows a considerable reduction at high gate bias, which significantly limits the on-state performance of the TFTs [67]. Therefore, it is crucial to reveal the effect of parasitic resistance for further improvement in device performance.

Fig. 5.11(a) illustrates the parasitic resistance components that are present in the n-channel TFTs. These include contact resistance between n^+ source/drain nc-Si:H contacts and metal electrodes, series resistance of the contact layers, and series resistance of the nc-Si:H channel layer. The latter can be strongly influential, particularly in staggered structure like our TFTs, since carriers must travel through an intrinsic nc-Si:H region on their way to/from the channel [65].



(a)



(b)

Fig. 5.11. (a) Parasitic resistance components of the n-channel top-gate nc-Si:H TFTs with staggered source/drain structure, and (b) the equivalent circuit of the TFTs used for device simulation.

In our numerical analysis, we treat all these components as a single lumped parasitic resistance R_p at each source/drain terminal. In Fig. 5.11(b), the equivalent circuit of the TFTs

used for ATLAS simulation is shown. By iterating the material properties of nc-Si:H and the values of parasitic resistance, we achieved the best fit between the computed and experimental transconductance data for the n-channel TFTs with W/L = 200 μm/50 μm as presented in Fig. 5.12. Here, the values of parasitic resistance deduced are 50 ~ 100 kΩ, depending on the drain bias. This is in good agreement with that previously reported for the top-gate nc-Si:H TFT having the n^+ layer with a dark conductivity of ~20 S/cm [83].

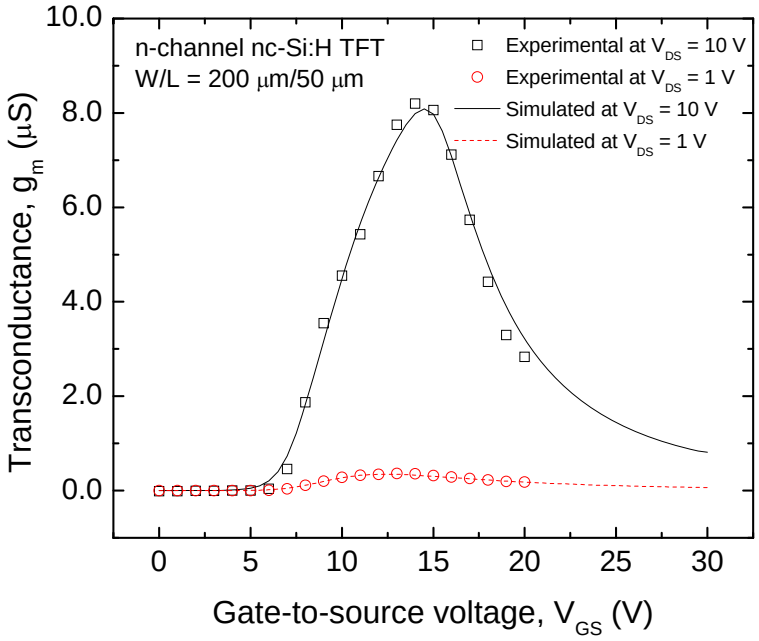
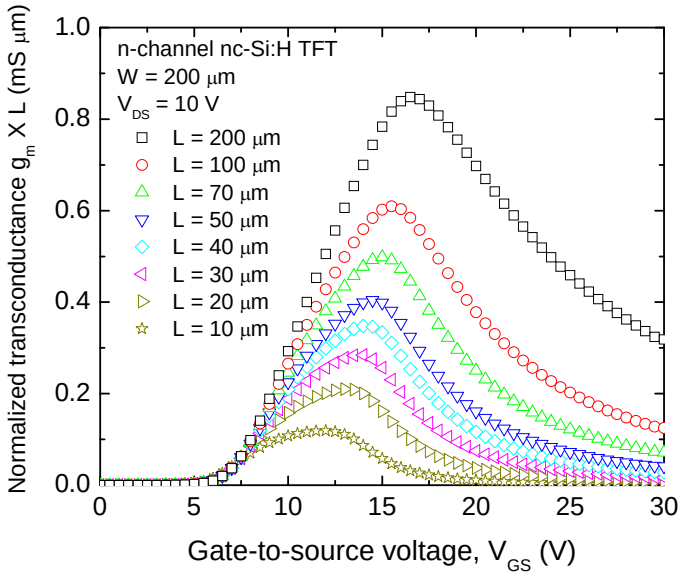
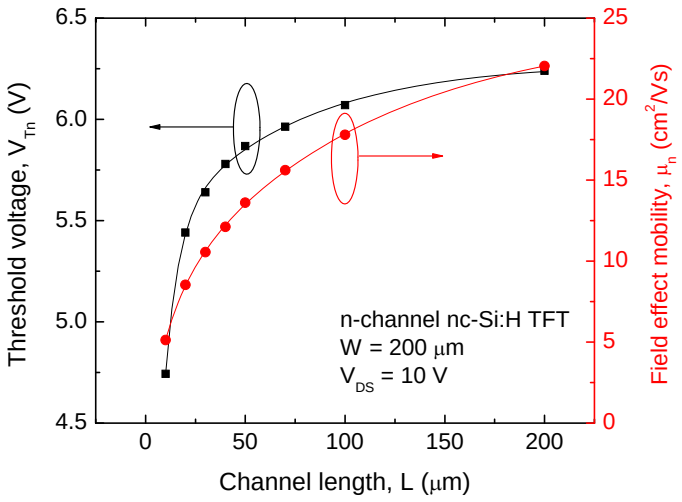


Fig. 5.12. Experimental and simulated transconductance of the n-channel TFTs at V_{DS} = 1 and 10 V.

We then studied the dependence of the channel length on TFT transconductance by numerical simulations. The results are depicted in Fig. 5.13(a). Here, the normalized transconductance significantly degrades as the channel length decreases. The maximum value of the normalized transconductance drastically decreases by a factor of 7.1 from 0.85 to 0.12 mS/μm as the channel length decreases from 200 to 10 μm. As a result, the threshold voltage and field effect mobility decrease as presented in Fig. 5.13(b). 24% reduction in the threshold voltage and 77% in the field effect mobility are observed as the channel length is reduced from 200 to 10 μm. This is because the weight of parasitic resistance increases as the TFT channel length decreases [80].



(a)



(b)

Fig. 5.13. (a) Simulated channel-length dependence on transconductance, and (b) variation in the threshold voltage and field effect mobility as a function of the channel length, which is deduced from the simulated transconductance.

For a better understanding of the impact of parasitic resistance upon transconductance, the TFTs having various values of parasitic resistance were simulated. The results are presented in Fig. 5.14. As seen here, when parasitic resistance is sufficiently low, 1 kΩ in our case, virtually no transconductance degradation (~32 μS) is observed. However, as parasitic resistance increases to 1 MΩ, the maximum transconductance drastically decreases to 0.73 μS.

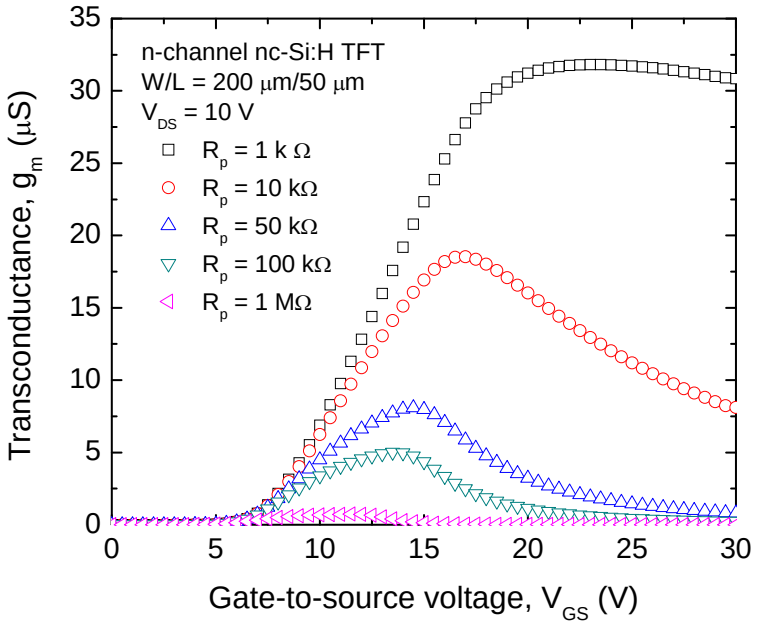
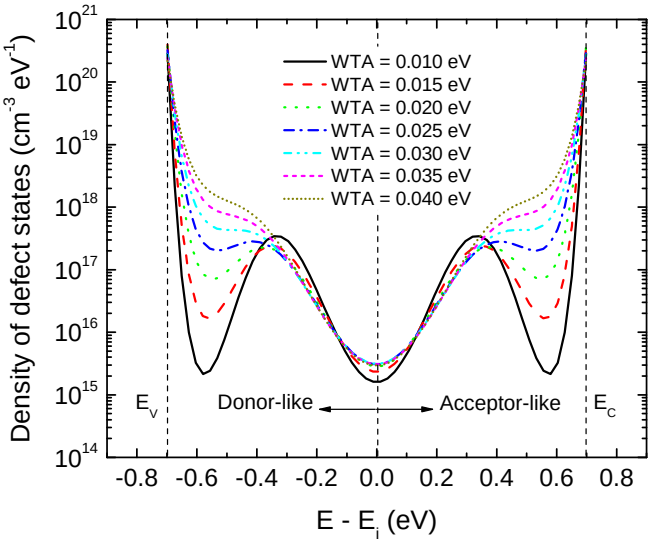
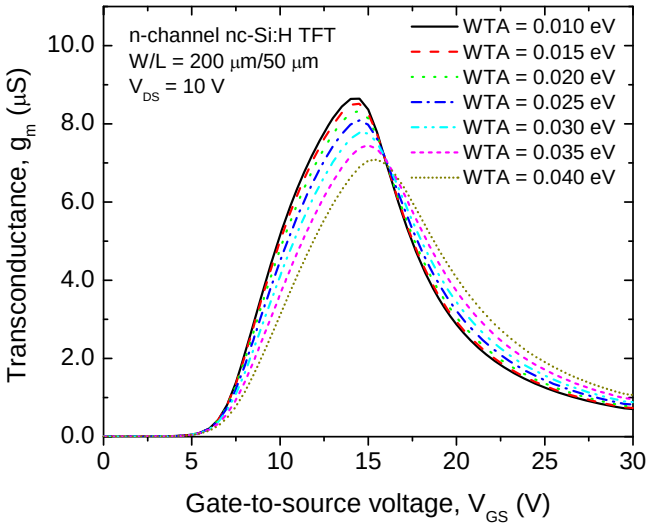


Fig. 5.14. Effect of parasitic resistance on TFT transconductance. Virtually no transconductance degradation is observed when the parasitic resistance value is sufficiently low (= 1 kΩ).

Material properties of nc-Si:H, i.e., the density of defect states within the band gap of the nc-Si:H material, can also strongly affect the series resistance of both the highly doped contacts and the intrinsic channel, and thus parasitic resistance. As presented in Section 3.1, the defect states are modeled by the sum of Gaussian deep states and exponential tail states. Here, wider tail corresponding higher characteristic decay energy WTA in Eq. (3.3) indicates that the film has more amorphous properties [84], thus resulting in higher series resistance of the film. Therefore, we investigated the influence of the nc-Si:H properties on the transconductance degradation by varying the values of characteristic decay energy. In Fig. 5.15(a), polynomial fits of the discrete energy levels of defects used in simulations are shown for various WTA values. As WTA increases from 0.01 to 0.04 eV, i.e., the films become more amorphous-like, the transconductance slightly degrades from 8.65 to 7.08 μS as observed in Fig. 5.15(b).



(a)



(b)

Fig. 5.15. (a) Polynomial fit of the density of defect states for various WTA values, and (b) the effect of WTA on transconductance. As WTA increases, in other words, the film becomes more amorphous-like, transconductance degrades more.

It is known that the transconductance degradation can also be due to the mobility reduction induced by high transverse electric field across the gate oxide [85]. In the TFT channel region, the high electric field forces carriers to interact strongly with the semiconductor/dielectric interface, and thus the carriers are subjected to scattering with surface roughness [85]. In Fig. 5.16, the simulated electric field in the nc-Si:H channel layer of the n-channel TFT is presented, in which the TFT is biased at V_{GS} = 25 V and V_{DS} = 10 V. As observed here, the intensity of the vertical electric field in the channel increases as it is closer to the nc-Si:H/SiO_2 interface, and shows the maximum value of around 10^5 V/cm underneath the interface.

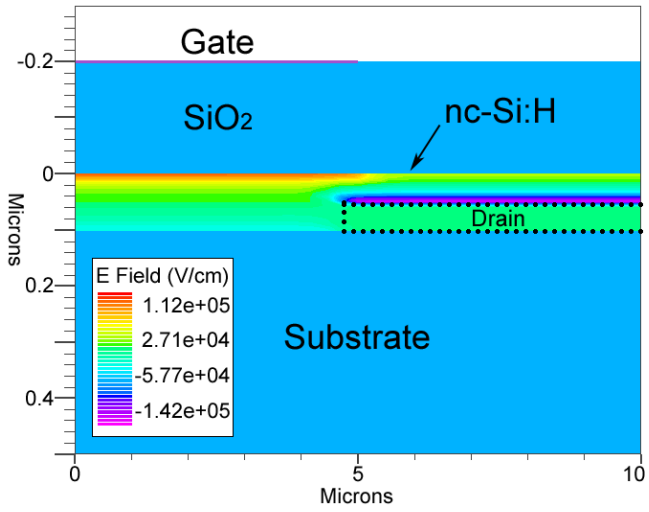


Fig. 5.16. Simulated transverse electric field in the channel layer of the n-channel TFT biased at V_{GS} = 25 V and V_{DS} = 10 V. The strong transverse electric field beneath the interface can induce the mobility degradation in the TFT.

Lombardi et al. have modeled the scattering effect on the carrier mobility by the sum of three terms for device simulation purpose [85],

$$\frac{1}{\mu} = \frac{1}{\mu_b} + \frac{1}{\mu_{sr}} + \frac{1}{\mu_{ac}}, \tag{5.6}$$

where μ_b is the carrier mobility in the bulk channel, and μ_{sr} and μ_{ac} are the carrier mobility limited by scattering with surface roughness and with surface acoustic phonons, respectively, having the following expressions,

$$\mu_{sr} = \left[\frac{(F_\perp/F_{ref})^2}{\delta} + \frac{F_\perp^3}{\eta}\right]^{-1}, \tag{5.7}$$

and

$$\mu_{ac} = \frac{B}{F_\perp} + \frac{C}{TF_\perp^{1/3}}, \tag{5.8}$$

where $F_\perp$ is the electric field perpendicular to the semiconductor/dielectric interface, F_{ref} is the reference field (= 1 V/cm), T is temperature, and B, C, δ, and η are constants. In Fig. 5.17, the adjusted values of μ_b, μ_{sr}, and μ_{ac} for the nc-Si:H channel material are depicted.

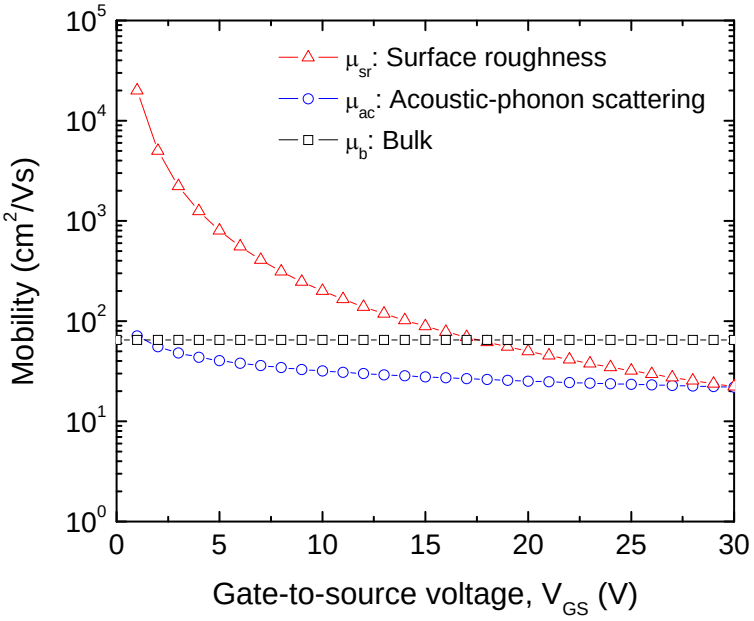


Fig. 5.17. Values of the Lombardi's mobility terms adjusted for the nc-Si:H channel material.

It should be noted that there is a possibility that the transconductance degradation by the parasitic resistance effect is too large so that the mobility degradation by high transverse field can be swamped. Therefore, in our numerical analysis, the parasitic resistance value is set to 1 kΩ, in which no transconductance degradation by parasitic resistance is observed as discussed earlier. The simulation results are shown in Fig. 5.18. As seen here, when the constant mobility model is employed, no mobility degradation is observed, whereas there is the mobility degradation when the effect of surface scattering or acoustic phonon scattering is considered.

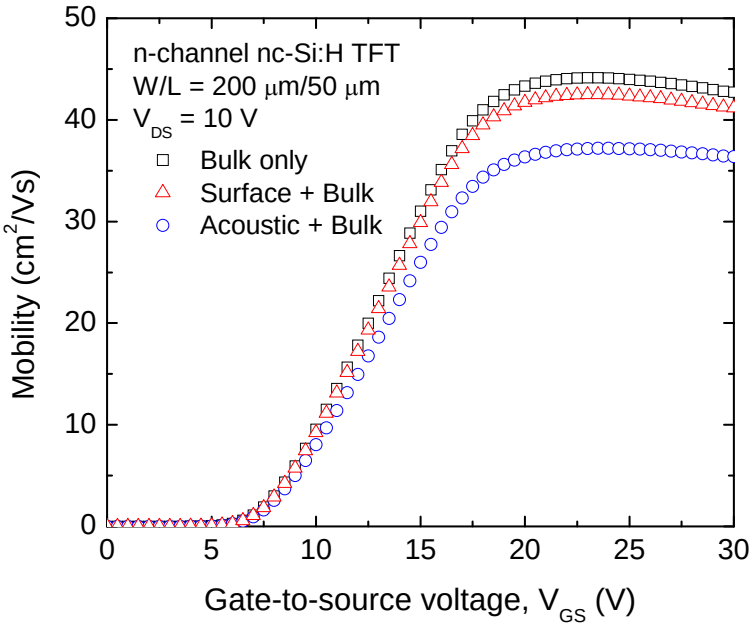


Fig. 5.18. Simulated field effect mobility as a function of gate bias, which shows the effect of each Lombardi's mobility term on the mobility degradation. When the constant mobility model (squares) is employed, no mobility degradation is observed, while the mobility degradation is observed when the effect of surface scattering (triangles) or acoustic phonon scattering (circles) is considered.

It is clear from the above numerical analysis that the on-state performance of the TFTs can be significantly improved by reducing parasitic resistance. One might think that higher level of doping could be effective. However, further doping can significantly reduce the dark conductivity and increase the corresponding activation energy due to the amorphization of the nc-Si:H material as discussed in Section 3.3. In order to reduce the

series resistance of the nc-Si:H channel layer, the coplanar structure might be more effective. However, as discussed in Section 4.2, since the etch selectivity between the nc-Si:H highly doped layer and the intrinsic channel is small, over-etching problem is inevitable. Indeed, a lower field effect mobility was reported for top-gate TFTs with coplanar source/drain electrodes [64]. To avoid this, self-aligned TFTs, in which ion implantation is employed, can be considered. However, a costly process step such as laser annealing is additionally required for the dopant activation in this case [59].

5.4 Threshold Voltage shift

One of the most important issues in the current amorphous silicon technology is material metastability. In the a-Si:H material, prolonged illumination causes defect creation and consequently, a decrease in both dark and photoconductivities, which is known as the Staebler-Wronski effect [20]. The effect is of particular importance for solar cells, in which the light exposure is the working condition. When it comes to TFTs, the threshold voltage shift ΔV_T is observed under prolonged gate bias stress, which has been attributed to defect creation in the a-Si:H channel and to charge trapping in the nitride gate dielectric [21]. In general, defect creation in the channel is predominant at low gate bias, while charge trapping in the nitride is at higher gate bias even though it can dominate at low electric field if the nitride dielectric is silicon-rich [21].

Several researchers have modeled both defect generation and charge trapping mechanisms to provide quantitative insight into instability in the a-Si:H TFTs. According to Powell et al. [21], the creation of metastable states in the a-Si:H channel has been reported to have a common origin related to the breaking of weak Si–Si bonds and the dispersive diffusion of hydrogen, which is given by a power law,

$$\Delta V_T = (V_{GS} - V_T)(t/t_0)^{\beta}, \tag{5.9}$$

where t_0 and β are a time constant and fitting parameter (being about 0.5), respectively. To the contrary, the threshold voltage shift where charge trapping in the nitride gate dielectric dominates shows a logarithmic dependence in time expressed by,

$$\Delta V_T = \gamma_d \log(1 + t/t_0), \tag{5.10}$$

where γ_d is a constant. In the meantime, Libsch et al. [86] have modeled the threshold voltage shift due to charge trapping with a stretched-exponential time dependence,

$$\Delta V_T = (V_{GS} - V_T)\left\{1 - \exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right]\right\}, \tag{5.11}$$

where $\tau = \tau_0 \exp(E_a/kT)$ represents the characteristic trapping time. Here, τ_0 is a constant ($\sim 10^{-10}$ sec) and E_a is the activation energy. A disagreement between the two charge trapping models is that Powell's model speculated no further redistribution of the charges trapped at the interface deeper into the bulk dielectric [21], whereas Libsch's model hypothesized the emission of trapped charges toward deep states in the bulk dielectric for longer stress time ($t > \tau$) and larger stress field [86].

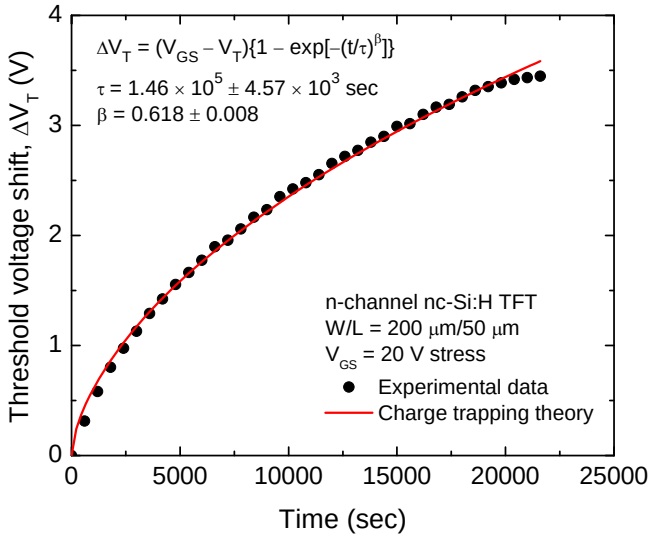
Nanocrystalline silicon is expected to have higher material stability due to the presence of silicon crystallites and lower concentration of hydrogen. Indeed, it is reported that the bottom-gate TFTs with the nitride gate dielectric shows improved stability over the a-Si:H counterpart [87]. However, the threshold voltage shift in the top-gate nc-Si:H TFTs with the SiO_2 gate dielectric has not been reported yet. In nc-Si:H, the dispersive motion of hydrogen atoms that are present in its amorphous matrix is also expected to play a key role as in the a-Si:H material. In addition, Nicollian et al. [88] have attributed charge trapping in the oxide of the MOS capacitors to water-related traps as discussed in Section 2.1, and modeled the flatband voltage shift due to charge trapping with the same stretched-exponential dependence in Eq. (5.11). Gaspare et al. have also modeled the threshold voltage shift in poly-Si TFTs with the SiO_2 gate dielectric using the same stretched-exponential expression [89]. Therefore, a careful speculation of the aforesaid facts led us to the conclusion that the existing models can be effectively applied to the stability analysis of our nc-Si:H TFTs with the SiO_2 gate dielectric.

Fig. 5.19(a) shows the measured time dependence of the threshold voltage shift in the n-channel TFTs with the channel width of 200 μm and length of 50 μm. The threshold voltage was retrieved every 10 minutes during 6-hour positive gate bias stress of 20 V. The drain bias V_{DS} of 1 V was throughout stressing to exclude any effects which might result from high drain current. Here, a threshold voltage shift of approximately 3.45 V is observed in $t \sim 10^4$ sec. The simulation using Eq. (5.11) is shown by a solid line in the figure. As observed here, the stretched-exponential model fits experimental data very well. This is

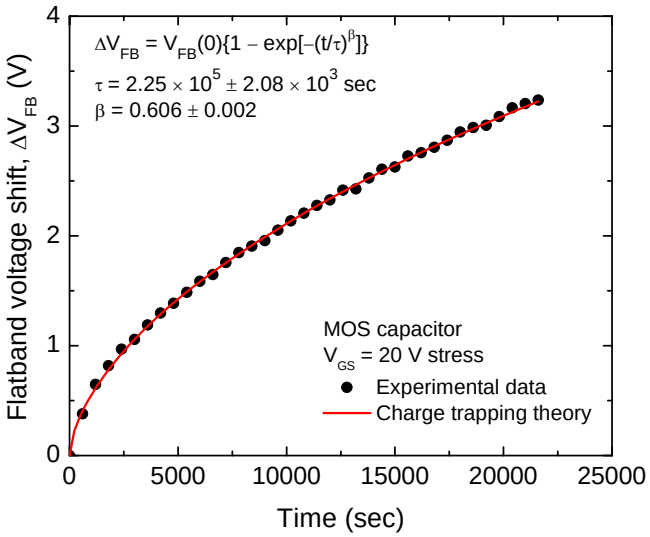
strong evidence to suggest that charge trapping in the SiO_2 gate dielectric is a predominant mechanism for the threshold voltage shift in our TFTs. Assuming the primary instability in our TFTs is associated with SiO_2 charge trapping, then the flatband voltage shift ΔV_{FB} in the MOS capacitors must correctly account for the threshold voltage shift in the TFTs under the same stress conditions. The measured data (circles) and simulation results (a solid line) using Eq. (5.11) are overlaid in Fig. 5.19(b). Here, a flatband voltage shift of about 3.24 V, which is also reproduced by the stretched-exponential dependence, well describes the threshold voltage shift in the TFTs. It is clear from these facts that the threshold voltage shift in the top-gate nc-Si:H TFTs with SiO_2 gate dielectric can be attributed to the flatband voltage shift, which is mainly due to charge trapping in SiO_2.

In our case, the oxide-related instability mechanism occurring in the TFTs is expected to be mostly involved with interface charge trapping but not with mobile ion drift effect for the following reasons. First, as predicted by the I-V and C-V characteristics of PECVD SiO_2 presented in Fig. 2.10 and Fig. 2.12, respectively, injection and trapping of carriers at the nc-Si:H/SiO_2 interface (recall high $D_{it} \sim 1.5 \times 10^{11}$ $cm^{-2} \cdot eV^{-1}$) occurring at around 20 V are believed to be predominantly responsible for the threshold voltage shift in our TFTs under the same level of gate bias stress (= 20 V). In addition, if the instability mechanism is due to mobile charges (i.e., positive H^+ ions), the negative threshold and flatband voltage shifts must occur as previously reported [90]. However, this is contradictory to our measurement results, which show positive threshold and flatband voltage shifts as presented in Fig. 5.19.

Thus, this strongly suggests that oxide-related instability is due to charge trapping at the nc-Si:H/SiO_2 interface.



(a)



(b)

Fig. 5.19. (a) Threshold voltage shift in the top-gate n-channel nc-Si:H TFT and (b) flatband voltage shift in the MOS capacitor. Both shifts were measured every 10 minutes during 6-hour positive gate bias stress of 20 V.

Chapter 6
Conclusions

The dissertation has covered issues pertaining to the material and device aspects of the top-gate nc-Si:H TFTs for high-performance and low-cost large-area electronics.

In our material study, a conventional PECVD system with a 13.56 MHz RF power source has been used. First, low temperature SiO_2 growth process has been optimized to yield the lowest leakage current across the oxide for TFT gate applications. The optimized film has exhibited the refractive index of 1.46 at a wavelength of 632.8 nm, dielectric breakdown field of 6.17 MV/cm, dielectric constant of 4.51, interface trap density of ~10^{11} $cm^{-2}\cdot eV^{-1}$, flatband voltage of -15 V, and mobile ion concentration of 3.4×10^{11} #/cm^2 before post-metallization thermal annealing. After 260°C annealing treatment, the films have demonstrated the improved dielectric breakdown field of 6.4 MV/cm, dielectric constant of 3.82, and flatband voltage of -10 V. N_2O plasma pre-treatment has been introduced for further improvement in the interface properties. However, its benefit in a conventional PECVD system has been observed to be small, since a sufficiently thick oxide, thus significantly improving the interface qualities, has not been grown as confirmed by photoemission spectra.

Next, the structural and electronic evolution of the nc-Si:H material with doping has been studied to surmount a low field effect mobility in the p-channel TFTs. In our study, the possibility of $B(CH_3)_3$ as an alternative dopant source for the growth of high-quality p-type nc-Si:H contacts has been examined. The p-doped films have demonstrated a dramatic increase in the growth rate, which has been attributed to the catalytic effect of CH_3 radicals promoting growth process. The films have also demonstrated comparable performance to the state of the art doped by B_2H_6 with the maximum dark conductivity of 1.11 S/cm (E_a = 36.7 meV) over 70% film crystallinity. Here, the electronic properties of the films have been found to be very sensitive to the crystallinity of the films. We have observed a phase transition from nanocrystalline to amorphous occurring at increased p-doping, thus causing degradation in a dark conductivity.

By selecting the highest-quality SiO_2 and nc-Si:H films developed, complementary top-gate nc-Si:H TFTs with staggered source/drain structure have been designed, fabricated, and characterized. The n-channel TFT has demonstrated a threshold voltage of 6.4 V, a field effect mobility of electrons of 15.54 $cm^2/V \cdot s$, a subthreshold slope of 0.67 V/decade, and an on/off current ratio of 10^5, while the corresponding p-channel TFT has exhibited a threshold voltage of -26.2 V, a field effect mobility of holes of 0.24 $cm^2/V \cdot s$, a subthreshold slope of 4.72 V/ decade, and an on/off current ratio of 10^4. Here, the effect of the gate leakage on TFT performance has been found to be minimal. However, the drain leakage current has been observed to significantly increase with increasing gate and drain bias. This high leakage current has manifested its effect as a reduction in the output swing of the inverters which

have been implemented by the nc-Si:H TFTs. After 240°C post-fabrication annealing, the n-channel TFTs have demonstrated improved performance; the threshold voltage has been reduced to 4.9 V, the field effect mobility of electrons has been increased to 26.13 $cm^2/V \cdot s$, the subthreshold slope has been decreased to 0.52 V/decade, and the on/off current ratio has been increased to 10^6. However, the TFTs still show the transconductance degradation under high gate bias, which significantly limits transistor performance.

Non-idealities observed in TFT behavior, including high leakage current, transconductance degradation, and threshold voltage shift, have been systematically investigated. Our study on the off-state conduction in the TFTs reveals that the responsible mechanisms for the leakage current are, under low gate bias, ohmic conduction flowing through the bulk nc-Si:H channel, and under high gate bias, thermal emission at low drain bias and Poole-Frenkel emission at high drain bias. In order to suppress the leakage current, particularly at a high bias regime, offset-gated structure has been examined. It has been confirmed that the undoped offset region between gate and drain electrodes is quite effective in suppressing the leakage current without significant compromise of the on-state performance. For further reduction in the resistive current, a small amount of boron has been added during nc-Si:H channel deposition in order to compensate oxygen contaminants. However, the compensation doping has been found to be unfeasible due to its narrow process window.

The transconductance degradation in the TFTs has been numerically analyzed. It has been confirmed that the parasitic resistance components existing in the TFTs strongly

degrade transconductance and thus significantly limit the on-state performance; 24% reduction in the threshold voltage and 77% in the field effect mobility have been observed as the channel length is reduced from 200 to 10 μm, which is due to the increased weight of parasitic resistance for short channel devices. However, if parasitic resistance was sufficiently low (~1 kΩ), virtually no transconductance degradation has been observed. Accordingly, strategies for reduction in parasitic resistance in top-gate structures have been discussed.

Lastly, the threshold voltage shift in the TFTs under prolonged bias stress has been quantitatively studied. The threshold voltage shift of approximately 3.45 V is observed under constant gate bias stress of 20 V in $t \sim 10^4$ sec. Under the same stress conditions, the flatband voltage shift in the MOS capacitors is 3.24 V, which well describes the threshold voltage shift in the TFTs. The stretched-exponential time dependence model, previously introduced to account for metastability due to charge trapping in the gate dielectrics, also fits our experimental threshold and flatband voltage shifts very well. This strongly suggests that the flatband voltage shift due to charge trapping in the SiO_2 gate dielectric is a predominant mechanism for the threshold voltage shift in the nc-Si:H TFTs. In our case, the oxide-related TFT instability has been attributed to injection and trapping of carriers at the nc-Si:H/SiO_2 interface.

The research presented in the dissertation has significant implications and contributions to the development of high-performance and low-cost nc-Si:H TFTs for highly functional, ultra-compact, and versatile active-matrix TFT backplanes as follows:

- First, our systematic study on PECVD SiO_2 has provided quantitative insight to leakage and charge trapping behaviors in the gate dielectric of the top-gate nc-Si:H TFTs. This has led us to an understanding of the oxide-related TFT instability, which will benefit reproducibility, predictability, and long-term reliability of the nc-Si:H TFTs. Indeed, this work is the first report on the instability mechanism in the top-gate nc-Si:H TFTs with the SiO_2 gate dielectric.
- Next, p-type nc-Si:H contacts grown by using $B(CH_3)_3$ have been applied to TFT fabrication for the first time. The corresponding p-channel TFTs developed in this work, demonstrating comparable performance to the state-of-the-art TFTs fabricated using B_2H_6, can be considered to be an alternative to the current a-Si:H and poly-Si TFTs in OLED pixels, which suffer from device instability and non-uniformity, respectively. In addition, the p-doped nc-Si:H films reported here are not limited to TFT applications but can also be extended to a wider range of applications including solar cells and image sensors.
- In addition, leakage current mechanisms in the top-gate nc-Si:H TFTs have been reported for the first time. Physical insight afforded by this research has enabled us to design the offset gate structure in order to suppress the leakage current. This will certainly lead not only to signal integrity in pixels but also to low power consumption in driving circuits of

the active-matrix backplanes. While further optimization of the TFT geometry can add to improvement in device performance, the n- and p-channel nc-Si:H TFTs reported here constitute an arguably important step towards monolithic integration of peripheral driving circuits on the active-matrix backplane.

- Lastly, our analysis on the transconductance degradation in the top-gate nc-Si:H TFT has quantitatively revealed the effect of parasitic resistance for further improvement in transistor performance. Such insight will enable us to enjoy the full benefits of higher carrier mobilities in nc-Si:H over the current industrial a-Si:H, eventually leading to the short channel nc-Si:H TFTs for faster active-matrix backplanes with higher resolution.

Although this dissertation has addressed several critical issues aforementioned, some process steps, particularly the growth of high-quality gate dielectrics and highly conductive nc-Si:H source/drain contacts which are still posing considerable challenges, may require completely new experimental approaches.

Appendix A

Test Chip Layout

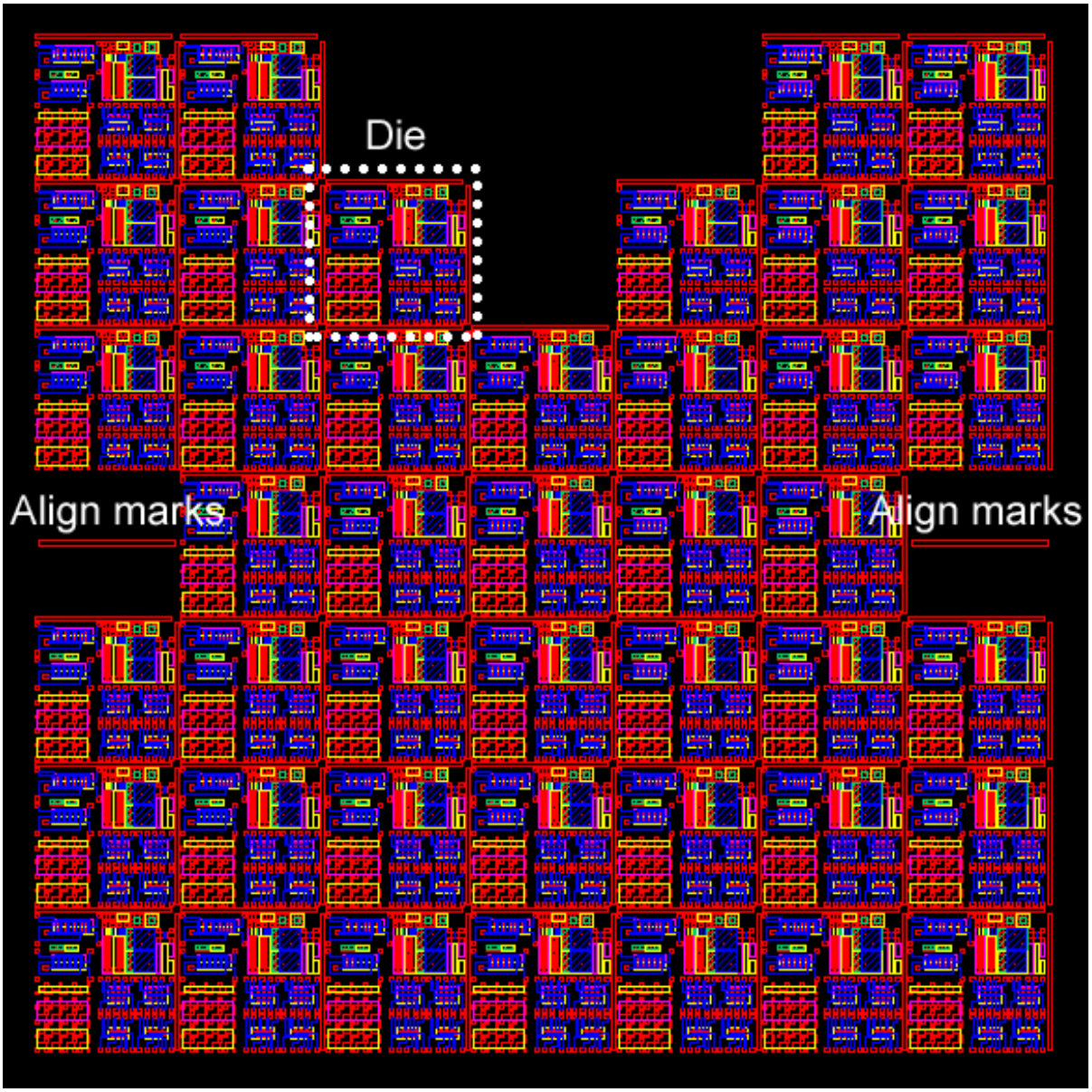


Fig. A.1. Top cell.

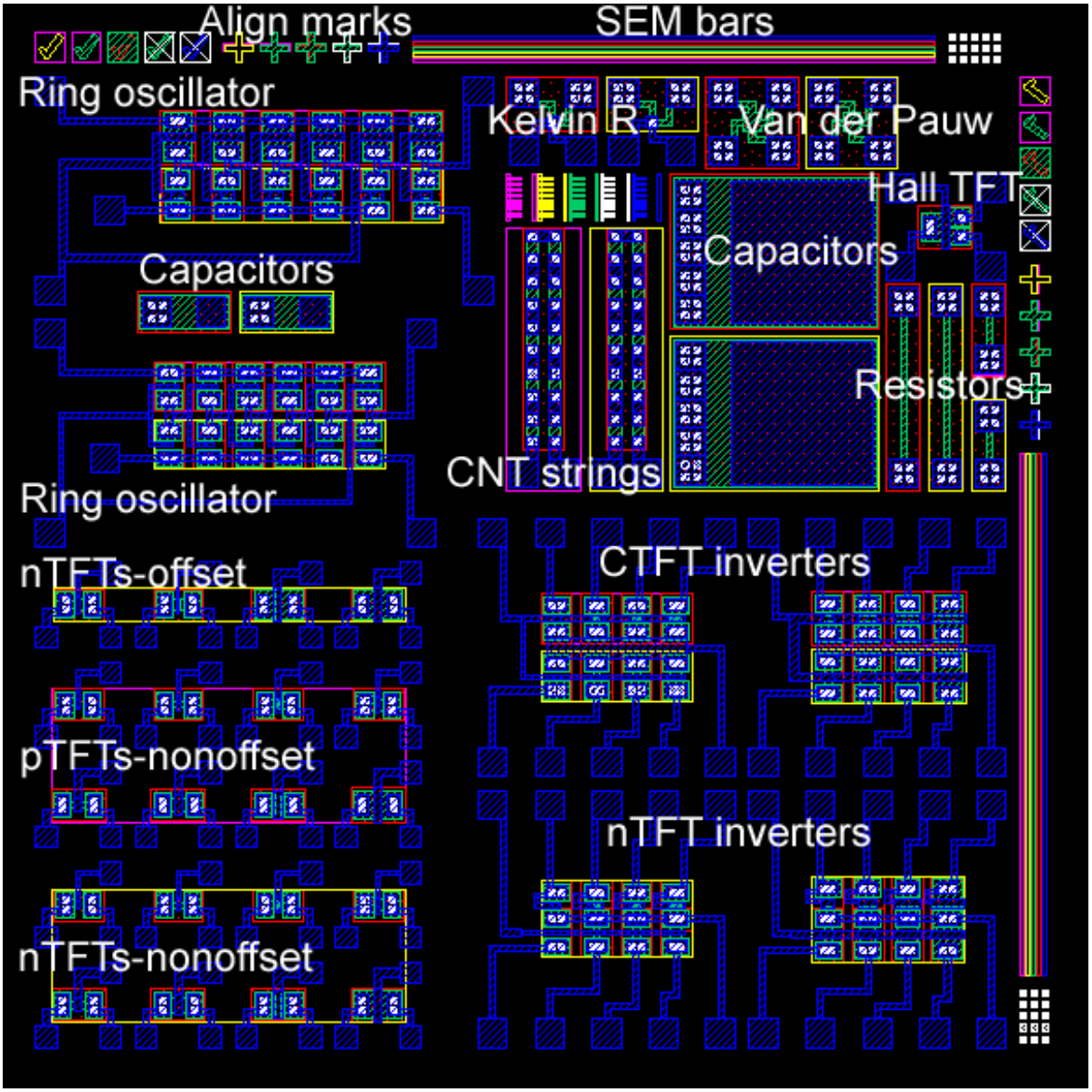

Align marks
SEM bars
Ring oscillator
Kelvin R
Van der Pauw
Hall TFT
Capacitors
Capacitors
Resistors
CNT strings
Ring oscillator
nTFTs-offset
CTFT inverters
pTFTs-nonoffset
nTFT inverters
nTFTs-nonoffset

Fig. A.2. Die.

Appendix B

TFT Process Recipe

Table B.1. Metal deposition conditions:

Cr and Al			
Ar	RF power	Pressure	Growth rate
30 sccm	400 W	5 mTorr	17 nm/min (Cr) 10 nm/min (Al)

Table B.2. PECVD process conditions:

Intrinsic nc-Si:H					
SiH_4	H_2		RF power	Pressure	Growth rate
5 sccm	500 sccm		90 W	900 mTorr	2.86 nm/min
n^+ nc-Si:H					
SiH_4	H_2	1% PH_3	RF power	Pressure	Growth rate
5 sccm	490 sccm	10 sccm	90 W	900 mTorr	3.7 nm/min
p^+ nc-Si:H					
SiH_4	H_2	1% TMB	RF power	Pressure	Growth rate
5 sccm	498 sccm	2.5 sccm	90 W	900 mTorr	3.97 nm/min
SiO_2					
SiH_4	N_2O	He	RF power	Pressure	Growth rate
4 sccm	100 sccm	400 sccm	100 W	100 mTorr	10 nm/min

Table B.3. RIE process condition

Intrinsic and n^+/p^+ nc-Si:H				
SF_6	O_2	DC bias	Pressure	Etch rate
45 sccm	5 sccm	-40 V	50 mTorr	5 nm/sec

Appendix C

Simulation Input Deck

```
go atlas
TITLE  Generation of top gate-staggered source/drain TFT structure.

# Define TFT structure: standard (L_off = 0), L = 50 um, t_ch = 100 nm, t_ox = 200 nm
mesh
x.m     l=0     spac=2.
x.m     l=20    spac=3.
x.m     l=35    spac=5.
x.m     l=50    spac=0.25
x.m     l=75    spac=3.
x.m     l=100   spac=0.25
x.m     l=115   spac=5.
x.m     l=130   spac=3.
x.m     l=150   spac=2.

y.m     l=-0.2  spac=0.05
y.m     l=0     spac=0.0075
y.m     l=0.05  spac=0.01
y.m     l=0.1   spac=0.0075
y.m     l=0.5   spac=0.25
y.m     l=10.   spac=5.

# Define regions: 1=oxide, 2 and 3=silicon, 4=oxide
region          num=1           y.max=0.        oxide
region          num=2           y.min=0.        y.max=0.05      silicon
region          num=3           y.min=0.05      y.max=0.1       silicon
region          num=4           y.min=0.1       oxide
```

```
# Define electrodes: 1=gate, 2=source, 3=drain
# To give gate offset, change x.max of gate
elec    num=1 x.min=50      x.max=100     y.min=-0.2    y.max=-0.2    name=gate
elec    num=2 x.min=0.      x.max=20.     y.min=0.1     y.max=0.1     name=source
elec    num=3 x.min=130.    x.max=150.    y.min=0.1     y.max=0.1     name=drain

# Define doping
doping  reg=2   uniformconc=1.e11     n.type
doping  reg=3   uniformconc=1.e11     n.type
doping  reg=3   gauss       conc=1.e20    n.type      x.right=50    char=0.3
doping  reg=3   gauss       conc=1.e20    n.type      x.left=100    char=0.3

save outf=std_str_l=50.str
tonyplot std_str_l=50.str

quit

go atlas
TITLE Simulation for the transconductance degradation in nc-Si:H TFTs

mesh inf=../../str/std_str_l=50.STR

# Set nc-Si:H material parameters
material        material=silicon mun=65 mup=3
defects         nta=1.e20 ntd=1.e20 wta=0.025 wtd=0.025 \
                nga=3.7e17 ngd=3.7e17 ega=0.4 egd=0.4 wga=0.1 wgd=0.1 \
                sigtae=1.e-16 sigtah=1.e-14 sigtde=1.e-14 sigtdh=1.e-16 \
                siggae=1.e-16 siggah=1.e-14 siggde=1.e-14 siggdh=1.e-16 \
dfile=donors.dat afile=acceptors.dat \
numa=36 numd=36
```

```
interface qf=1.5e11

# Define contact parameters
contact num=1 alum
contact num=2 alum resistance=1.e7
contact num=3 alum resistance=1.e7

# Define models
models srh print trap.coulombic

# Enable the following parameters for study of scattering effects
# mobility en.cvt=1 dn.cvt=0.333 ep.cvt=1 dp.cvt=0.333 kn.cvt=2 kp.cvt=2

method newton
solve init
solve prev vdrain=0.1
solve prev vdrain=0.2
solve prev vdrain=0.5
solve vdrain=1 vfinal=10 vstep=1 name=drain

log outf=forward_10.log
solve vgate=0 vstep=0.5 vfinal=30 name=gate

extract name="forward_10" curve(v."gate", i."drain") outf="forward_10.dat"
extract name="gm_10" curve(v."gate",dydx(v."gate", i."drain")) outf="gm_10.dat"

tonyplot -overlay forward_10.dat ../../target/target_forward_10.dat
tonyplot -overlay gm_10.dat ../../target/target_gm_10.dat

quit
```

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