

Integrated MEMS-Based Phase Shifters

by

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A thesis
presented to the University of Waterloo
in fulfillment of the
thesis requirement for the degree of
Doctor of Philosophy
in
Electrical and Computer Engineering

Waterloo, Ontario, Canada, 2008

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Author's Declaration

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This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

I understand that my thesis may be made electronically available to the public.

Reena Al-Dahleh

Abstract

Multilayer microwave circuit processing technology is essential in developing more compact radio frequency (RF) electronically scanned arrays (ESAs) for the next generation radar and space-based systems. ESAs are typically realized using the hybrid connection of four discrete components: the RF manifold (combining network), phase shifters or Butler matrices, antennas and T/R modules. The hybrid connection of these separate and conventional components increases the system size, packaging cost and introduces parasitic effects that result in higher losses. In order to eliminate these drawbacks, there is a need to integrate these components on the same substrate, forming a monolithic phased array. With the recent advancements in the field of microelectromechanical systems (MEMS) and micromachining technology, miniaturized RF MEMS components including switches and phase shifters have been demonstrated with superior performance. RF MEMS technology enables the monolithic integration of the ESA components into one highly integrated multifunctional module, thereby enhancing ESA designs by significantly reducing size, fabrication cost and interconnection losses.

In passive ESAs, the RF combining network and phase shifters are placed between the T/R module, which contains low noise amplifiers (LNAs) and power amplifiers (PAs), and the antenna elements. The insertion loss of the phase shifter and of the combining network is a key design consideration as it directly impacts the transmitted power and the receiver's noise figure. Conventional wide-band digital true-time-delay phase shifters are mostly built using switches made of p-i-n diodes, MESFETs or high electron-mobility transistors (HEMTs), and the insertion loss is usually in the range of 4 to 6 dB at X-band for a 4-bit design. The use of high loss phase shifters necessitates that the T/R module compensates for this loss with a higher transmit RF power. This in turn results in more DC power consumption and the use of a larger size and a higher cost T/R module. MEMS switches exhibit a lower loss and lower DC power consumption in comparison to their semiconductor counterparts. Therefore, they can be used for the realization of a MEMS phase shifter with a performance that is far superior than that of existing commercial semiconductor phase shifters.

For the first time, a novel capacitive shunt MEMS switch design is presented that utilizes warped beams to enhance its RF performance without drastically influencing the mechanical performance. Various capacitive switch spring configurations using the proposed warped beam concept are investigated both theoretically and experimentally. A dual-warped beam MEMS switch with an off-to-on capacitive

ratio of almost 170 is achieved without the need for thin dielectrics or high dielectric constant materials. It exhibits excellent RF performance and mechanical reliability with isolation better than 40dB and switching speeds as low as 6 μ s. These MEMS switches are implemented into single pole three throw (SP3T) and single pole four throw (SP4T) configurations.

A novel 3-bit finite ground coplanar (FGC) waveguide switched delay line MEMS phase shifter is developed with four cascaded SP3T dual-warped beam capacitive switches to achieve low-loss performance and simplify the ESA design. The fabricated prototype unit for the MEMS phase shifter exhibits an insertion loss of 2.5 \pm 0.2dB with an rms phase error of \pm 6 $^\circ$. Moreover, a compact 4 x 4 Butler matrix switchable with the use of a MEMS single-pole four-throw (SP4T) switch is investigated as an alternative passive beamforming method. The overall beam-switching network is monolithically integrated within a real-estate area of only 0.49cm². Air-bridge crossovers are implemented to maintain compatibility with the MEMS fabrication process utilized for the SP4T MEMS switch. This technique provides a unique approach to fabricate the entire beamforming network (BFN) monolithically. It also demonstrates the potential for scalability to larger more complex systems.

An 8-mask fabrication process is developed that allows the monolithic integration of the MEMS phase shifters and the RF combining network on one substrate. This modular approach integrates the capacitive-coupled interconnects, a 3-bit MEMS phase shifter and a power divider, thereby achieving a significant breakthrough in size, weight and cost while maintaining good RF performance. This novel monolithic integration process reduces fabrication costs in offering low packaging and assembly complexity. The wafer-scale three-dimensionally integrated ESA prototype unit has an area of 2.2cm². It serves as the basic building block to construct larger scanning array modules and introduces a new level of functionality previously achieved only by the use of larger, heavier and expensive systems.

Acknowledgements

I wish to express sincere appreciation and gratefulness to my advisor Professor Raafat Mansour for his knowledge, insight, valuable guidance and contagious enthusiasm throughout this research. Indeed, my gratitude to him cannot be expressed in a few words and it was an honor to be his student. I have gained a life-long role model to which I look up to and hope to follow in his footsteps. I am also grateful to Professor Sivoththaman and Professor Nieva for sharing their expertise and knowledge in processing and mechanical modeling. I would like also to thank Professor Antar, Professor Chaudhuri, Professor Sivoththaman, and Professor Nieva for serving on my committee and for their constructive criticism and feedback. Financial support was provided by the Natural Science and Engineering Research Council of Canada (NSERC) and COMDEV. Their contribution is greatly appreciated.

I would like to recognize my officemate Paul Laforge for putting up with me for those four years; I will forever remember the many great conversations we've had about all subjects in life. He will make an excellent professor and mentor one day. Thanks to Bill Jolley, Roger Grant and Stella Chang for their constant support and guidance, and for giving me those laughs when I needed them the most. I would like to especially thank Siamak Fouladi for his laid back attitude and for admitting that I'm always right! My eternal gratitude to KarMun Cheng, Tiana Robinson, Cherilyn Carrara and Amira Aker, whose humor, unconditional support and strength made every day enjoyable, and I am profoundly thankful.

Last but certainly not least I have to express my everlasting gratitude to my Dad and Mum who have inspired me to be the best that I can be. They gave me all the tools in life to be able to succeed, and taught me never to stop achieving, and to never settle for less than best. I derive my strength from the strength they exuded through all their battles in life. I am eternally indebted to my brother, my best friend and rock throughout the grueling past few years; he made me believe that I can be a great professor one day. Thank you to my sister for bringing in one of my biggest joys into this world, my nephew Jad, which I hope I will one day inspire to be the best that he can be. I would also like to recognize my fiancé Fareed who made the last tough stages a breeze.

Dedication

I would like to dedicate this thesis to my mother Narrivana Al-Dahle and my father Jihad Al-Dahle for their infinite love and support.

I would also like to dedicate this thesis to my biggest inspiration, my cousin Mohammed Dahleh, who was robbed of reaching his full potential of being an excellent researcher and engineering professor at the young age of 39 by colon-liver cancer. I hope I can follow in his path of being a wealth of knowledge, a dynamic and creative personality with a calming presence.

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Chapter 1

Introduction

1.1 Motivation

Next generation electronically scanned arrays (ESAs) aim to reduce both deployment and operational expenses by employing scalable, lightweight arrays assembled using low-cost, monolithically-integrated modules [1]. ESAs are an integral part of space-based radar systems and are realized with the hybrid connection of the RF feed network (transmission lines and power dividers), phase shifters, antennas and T/R modules, as shown in Figure 1.1. ESAs steer the beam electronically by controlling the relative phase shift in each radiating array element. This enables the system to track fast-moving and multiple targets, necessary for radar applications such as surface detection, tracking and satellite communication. Electronic scanning also eliminates mechanical complexity and reliability issues involved with conventional mechanically scanned arrays. Current integrated ESA technology has several disadvantages such as high assembly and integration cost and high DC power consumption, preventing its implementation in many phased array applications.

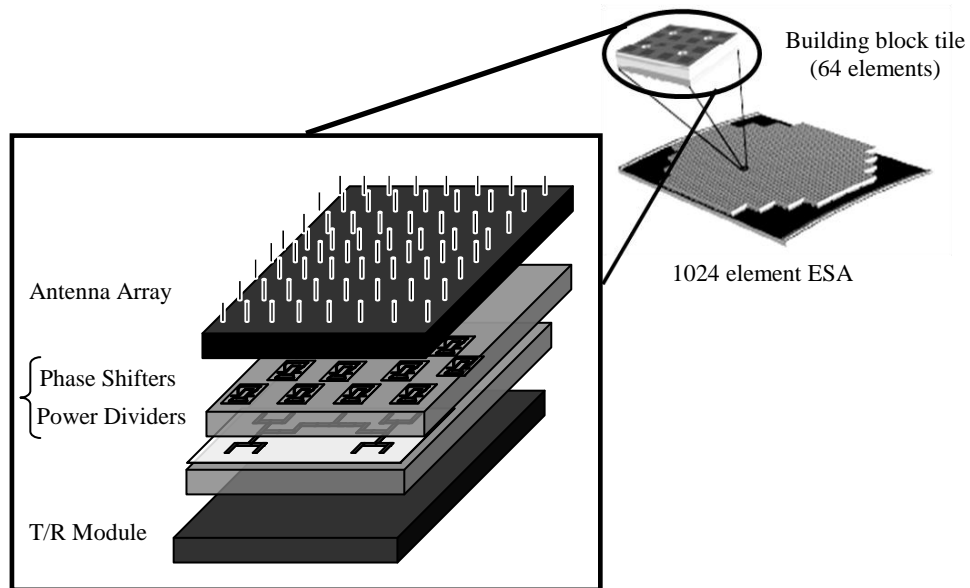


Figure 1.1: Proposed 3-D integrated ESA module. A 1024 element ESA can be subdivided into an array of tiles. Each tile consists of the hybrid connection of the RF feed network (transmission lines and power dividers), phase shifters, antennas and T/R modules.

With the recent exciting advancements in the field of microelectromechanical systems (MEMS) and micromachining technology, miniaturized MEMS phase shifters have shown to offer a superior RF performance in comparison to their semiconductor counterparts. The main objective of this research is to develop a new technique for integration at the module level that combines the MEMS phase shifters and feed networks into a highly integrated multifunctional chip, which can then be connected to the antenna array and T/R modules, as illustrated in Figure 1.1.

In today's large sized phased arrays for radar systems the key attributes include low insertion loss and drive power as well as light weight and low production cost. Consider a space-based radar system which consists of 182,400 phase shifters. The ESA can be subdivided into an array of tiles. Each tile consists of an array of 64 elements integrated into one module, serving as the building block for the entire system. Traditionally the phase shifter networks and the power divider networks are integrated as shown in Figure 1.2(a) and Figure 1.2(b). In the first technique illustrated in Figure 1.2(a), the MEMS phase shifter networks and the power divider networks are processed on two separate substrates and connected using gold connectors.

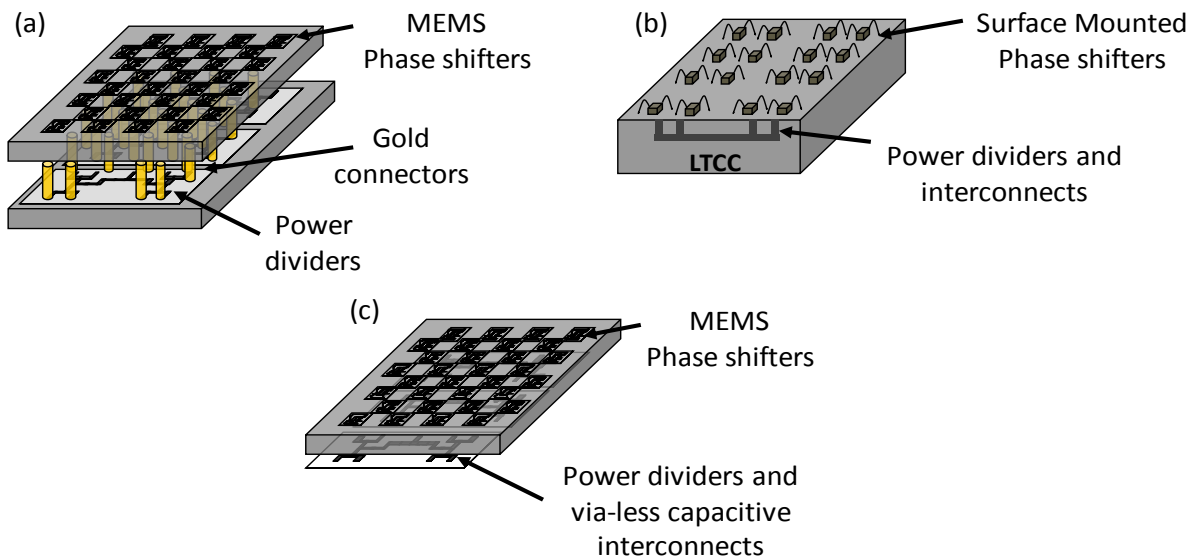


Figure 1.2: Comparison of the different integration methods. (a) Hybrid integration using two processed substrates and gold connectors. (b) Hybrid integration using an LTCC-processed substrate and surface mounted phase shifters. (c) The proposed integration method using a single substrate and capacitive interconnects.

The second method uses Low Temperature Co-fired Ceramics (LTCC) processing where the hybrid phase shifters are surface mounted to the LTCC-processed substrate and connected to the power divider networks using gold interconnects. If 8-way power dividers are integrated with these phase shifters monolithically, the 64 phase shifters and the associated feed network can be potentially integrated on a single 6 inch wafer. The proposed integration method shown in Figure 1.2(c) uses the double side of a single wafer with via-less capacitive interconnects to connect the two networks. These via-less capacitive interconnects use capacitive coupling through a thin substrate to connect the circuits on either side of the wafer. In space-based systems mass is a critical factor and a saving of 1gram per phase shifter by using monolithic and via-less integration can translate to a significant mass cutback.

Recently, MEMS switches implemented in phase shifters have demonstrated exceptional performance at microwave frequencies including low insertion loss (less than 1dB), high isolation and low DC drive power consumption. Although a FET phase shifter consumes low power, its insertion loss is at least 4dB higher than that of a MEMS phase shifter. The signal would require amplification to correct this loss. To demonstrate, consider a simple transmitter module that consists of a phase shifter terminated with a radiating antenna element as shown in Figure 1.3. The FET phase shifter exhibits an insertion loss of about 6dB, whereas a MEMS phase shifter exhibits an insertion loss of about 2dB.

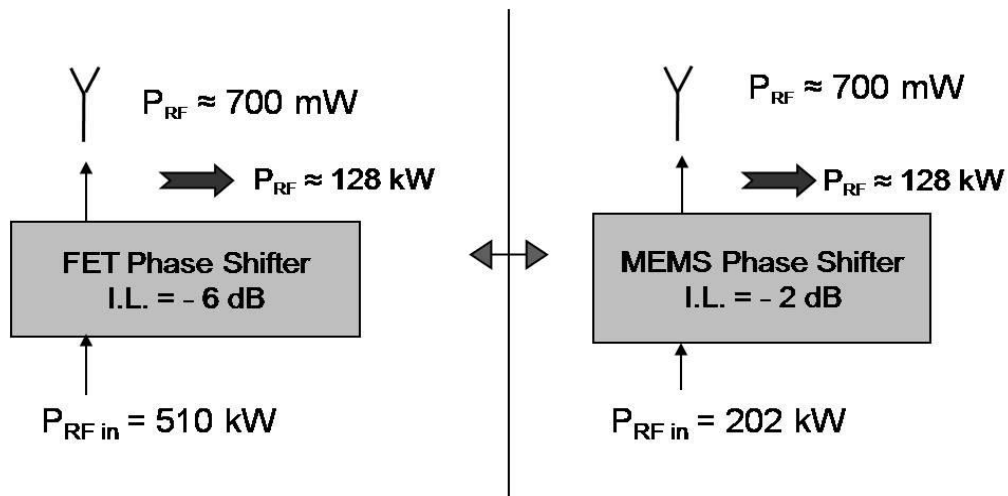


Figure 1.3: Comparison of the power requirements of a system designed with a FET phase shifter and a system designed with a MEMS phase shifter. Both phase shifters consume very little DC power.

As mentioned earlier, typical implementations of space-based radar systems have an excess of 182,400 antenna elements. Therefore, to deliver about 700mW to each of the antenna elements, the system with the FET phase shifter would require 510kW of RF power. In comparison, the MEMS phase shifter would only require 202kW. Assuming that the power amplifiers have 50% efficiency, the DC power required for the semiconductor-based system would be 1020kW, while that required by the MEMS-based system would be 404kW. That calculates a saving of 50% in DC power consumption.

The final and often deciding factor in ESA fabrication is the cost of hybrid integration of the devices. Monolithic integration of these components into one substrate will reduce cost of assembly and integration which typically contributes to a large part of the phased array cost. RF MEMS technology enables the monolithic integration of the ESA components into one module, thereby enhancing ESA designs by significantly reducing size, fabrication cost, and interconnection losses and enhancing overall system performance.

In this research, a MEMS-based phase shifting network (tunable 3-bit MEMS phase shifter and passive 4 x 4 Butler beam forming network) and feed network are integrated into one versatile compact prototype chip that can then be connected to the antenna array and T/R modules. In addition to saving in assembly and integration cost as well as a reduction in DC power consumption, this integration concept offers high yield as well as low packaging and assembly complexity.

1.2 Objectives

The objective of this thesis is to design and fabricate a novel integrated module with RF MEMS components into one feasible prototype chip using micromachining technology. This innovative module introduces a new level of integration, previously achieved only by the use of larger, heavier and expensive systems. The stages of research and design include:

- **Development, modeling and fabrication of novel n-throw dual-warped beam capacitive MEMS switches**

A novel MEMS capacitive shunt switch is developed to meet array system requirements with high isolation and low actuation voltage (~26V). By introducing warped bimetallic beams within the switch's geometry, the effective capacitive area is optimized to fine-tune the switch's RF performance in the 'off' state without influencing the switch's 'on' state performance. As a result, measurements show a drastic improvement where the 'off' state capacitance is doubled and the 'on' state capacitance is halved. Using this technique, a dual-warped switch with an off-to-on capacitive ratio of almost 170 is achieved without the need for thin dielectrics or high dielectric constant materials, exhibiting excellent RF performance and mechanical reliability. The mechanical and electrical modeling of this switch is examined in detail. This switch is also implemented in a three-throw (SP3T) and four-throw (SP4T) switch configuration for signal routing in the beam forming networks.

- **Development of the 3-bit MEMS Phase Shifter and the feed network**

Using the switches conceived in the previous stage of research, a 3-bit switched delay-line MEMS phase shifter is developed. Critical parameters such as low insertion loss and phase linearity are the focus of this design. FGC lines are employed in the design of the phase shifter to incorporate the shunt capacitive MEMS switches that have higher power handling capabilities than their metal-to-metal series switch counterparts. Two-way power dividers are designed to meet criteria such as low insertion loss and compact size. Integrated Butler matrices designed using FGC waveguides are also examined and tested as a passive beamforming network alternative to the active phased array.

- **Fully Integrated ESA Module**

A wafer-scale integration technique using micromachining processes is developed to combine the ESA's RF components to form novel and versatile ESA modules on one chip, taking into consideration discontinuities and interconnection losses. Using an 8-mask process, X-band 3-bit MEMS phase shifters, Wilkinson power dividers and via-less capacitive interconnects are integrated on a double-sided wafer to produce the prototype module. In this monolithic approach, the choice of

substrate, alignment and circuit component layouts are explored. Several design and processing challenges are encountered and circumvented in integrating these RF components onto one substrate. This integration technology offers high yield and low cost batch fabrication as well as low packaging and assembly complexity. The wafer-scale three-dimensionally integrated ESA prototype unit has an area of 2.2cm^2 and is an enabling building block of integrated sub-system arrays for lightweight large space-based phased arrays.

1.3 Outline

Following the motivation and objectives given in Chapter 1, Chapter 2 presents an overview of the different technologies available to realize integrated ESA modules. ESA module component technology is also examined where the most current RF MEMS switches and MEMS phase shifters are surveyed. In Chapter 3, a novel dual-warped capacitive MEMS switch is reported. Several configurations and designs are presented including a single-pole three-throw (SP3T) and single-pole four-throw (SP4T) switch. The monolithic fabrication of these designs along with mechanical analysis and measured data is presented. Other ESA components designed for the integrated module including the 3-bit MEMS switched delay-line phase shifter, power dividers, via-less capacitive interconnects, and 4x4 Butler matrices are introduced in Chapter 4. Chapter 5 presents the integration process used to fabricate the designed integrated ESA module on one chip. Finally, a brief summary of the contributions of the thesis with an outline of proposed future research is given in Chapter 6.

Chapter 2

Background

The roadmap given in this chapter will describe the extensive work documented on each individual component of ESAs and the different integration and assembly techniques developed to meet the changing demands of radar and satellite systems. The first part of this chapter describes the different methods of phase scanning in ESAs and presents the most current work reported on integrated ESAs. In the second part of this chapter, a review of the ESA active and passive components including MEMS switches, phase shifters and Butler matrices is given including the use of RF MEMS technology from the perspective of its enabling technologies including fabrication.

2.1 Integrated ESAs

An ESA's beam is electronically scanned by varying the relative phase shift in each radiating array element with the use of phase shifters and switches. There are two main electronic scanning techniques: phase scanning and electronic feed switching. The electronic feed switching method uses multiple fixed directional beams with narrow beam widths, whereas the phase scanning technique positions the beam electronically by adjusting the differential phase between elements of an array in a predetermined manner, continuously steering the beam towards the desired direction, as illustrated in Figure 2.1. Comparing the two systems, a phase-scanning array system can cover an expansive, more uniform area with the same power levels as a simple switched beam system at a higher cost and increased system complexity due to the necessity of tunable active phase shifters [1]. Whereas the electronic feed switched system consists of switches, interconnecting Butler matrices and fixed phase delays. The disadvantage of Butler matrices is that with larger arrays, the interconnecting requirements and layout gets increasingly complex.

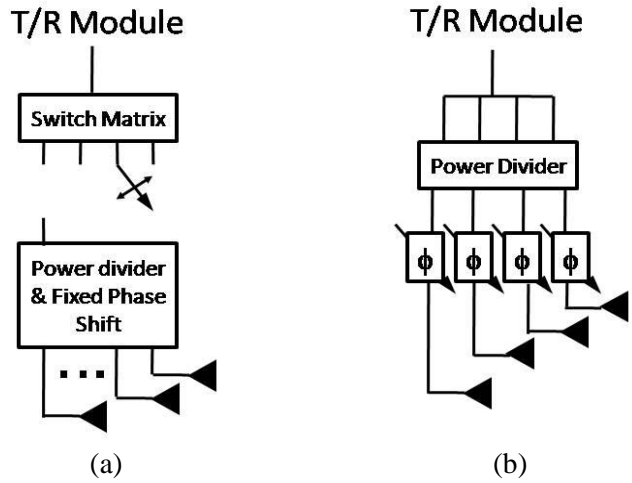


Figure 2.1: Functional block diagram of electronic scanning methods. (a) The electronic feed switching method. (b) The phase scanning method [1].

Moreover, the different types of ESAs can be classified as active and passive. The block diagram in Figure 2.2 shows the architectural differences between both systems [1]. While the active ESAs use a T/R module containing a low noise amplifier (LNA) and power amplifier (PA) for each radiating element to minimize the contribution of RF losses to the system noise figure and transmitting efficiency, the passive ESA uses a single PA and LNA for all radiating elements. In this thesis, the design is based on the passive ESA approach where the use of MEMS low-loss phase shifters allows the design to migrate towards a passive ESA.

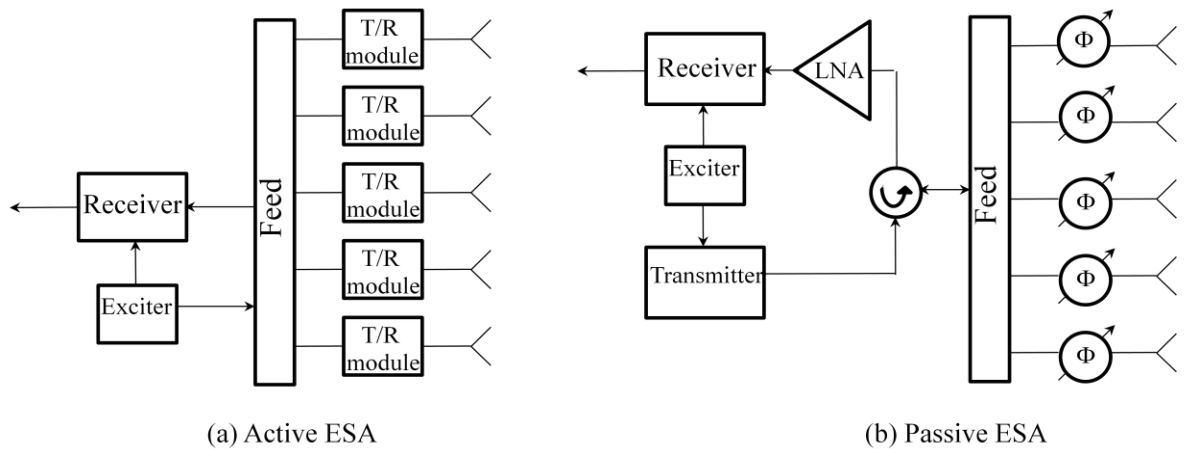


Figure 2.2: There are two types of ESAs (a) Active ESA. (b) Passive ESA [1].

2.1.1 Integrated Electronic Feed Switched ESAs

The Butler matrix (BM) is one of the most commonly used beamforming networks (BFNs) and uses passive hybrids and fixed phase delays to produce successive multiple beams. An $N \times N$ BM produces N beams directed in different paths with an N -element array. When a signal approaches the input port of the Butler matrix, it produces a set of progressive inter-element phase shifts between output ports given by:

$$\Delta\phi = \pm(2k - 1) \frac{\pi}{2N} \quad k \in [1, N] \quad (2.1)$$

where N is the number of ports of the matrix. Consider the 4×4 BM array shown in Figure 2.3(a) that consists of four 90° hybrids and two fixed phase shifters. When one of the input ports is excited by an RF signal, all output ports feeding the array elements are equally excited with an increasing phase difference, resulting in a beam at a specific angle as shown by the radiation pattern in Figure 2.3(b). If multiple beams are required, two or more input ports need to be excited simultaneously.

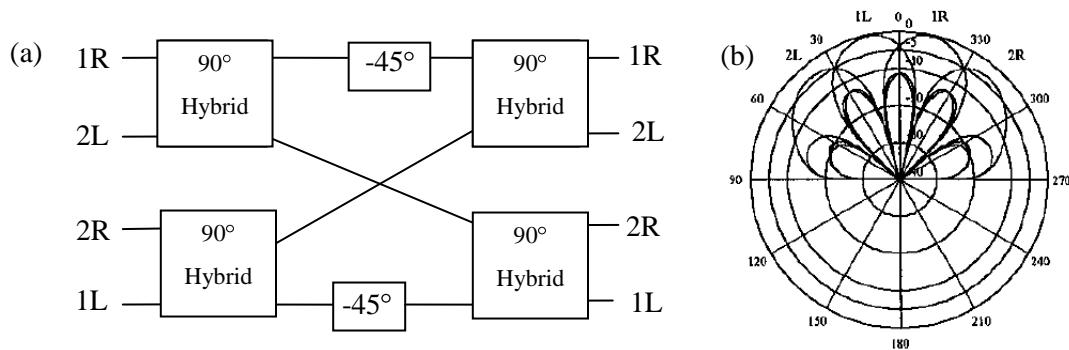


Figure 2.3: The BM consists of four 90° hybrids, two 45° delay lines and crossover lines. (a) The 4×4 BM layout. (b) The associated radiation pattern of a 4×4 BM.

A high-power handling routing multiplexer or switch matrix is required to select the different inputs of the BFN, resulting in a switchable phased array system. Most common implementations for routing the signal into the matrix use coaxial or multi-throw MMIC switches. Savium Technologies

uses a single-pole eight-throw (SP8T) PIN diode switch matrix to route signals through the Rothman beamforming lens as shown in Figure 2.4 [2].

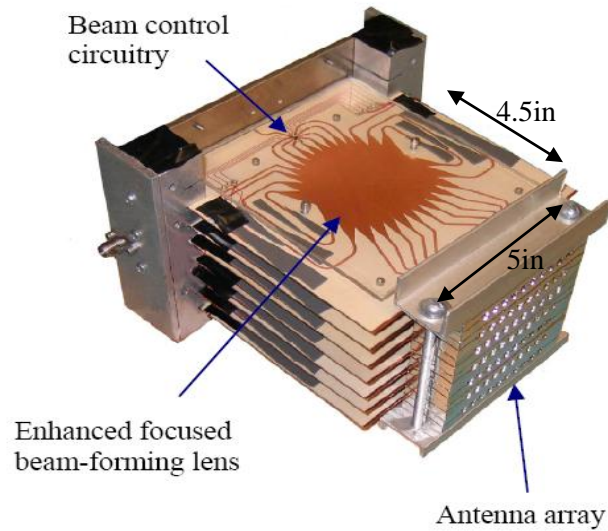


Figure 2.4: Switched beam phased array with an SP8T PIN diode routing switch by Savium Technologies [2].

Another system is presented [3] in which a hybrid 8 x 8 BM is connected to an 8 x 2 microwave switch matrix. The resultant system is bulky and large in nature, as shown in Figure 2.5.

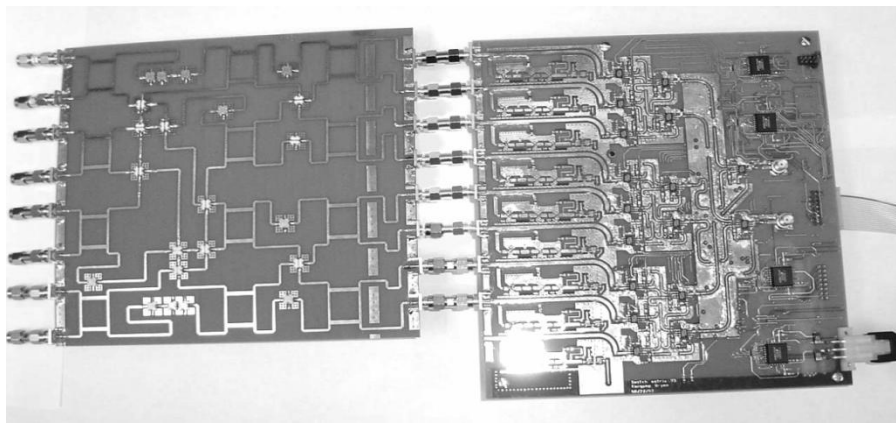


Figure 2.5: Hybrid 8x8 Butler matrix connected to the 8x2 microwave switch matrix [3].

To our knowledge, there has been no report of integrating a MEMS routing switch to the Butler matrix input for input port selection. The use of a multi-throw SPNT switch can allow for the design and fabrication of a purely monolithic, switchable BFN that requires very little driving DC power.

2.1.2 Integrated Phase Scanning ESAs

There have been many notable attempts to develop planar, integrated phased array antenna systems employing phase shifters for beam steering. Some technologies have used hybrid integration of the ESA components; however more current reports use multilayer processes and organics for the monolithic integration of these RF components.

Romanofsky et al. reported a prototype K-band linear 16-element scanning phased array based on thin ferroelectric film coupled microstripline phase shifters and microstrip patch radiators as shown in Figure 2.6, with bias voltages up to 350 V and is 11.9 cm long [4].

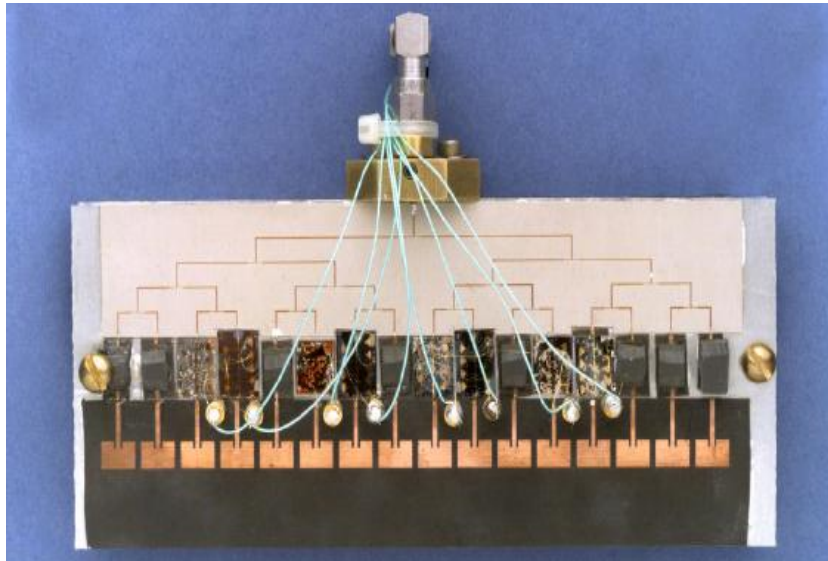


Figure 2.6: 16-element phased array antenna using $Ba_{0.6}Sr_{0.4}TiO_3$. This ferrite-based phased array requires actuation voltages of up to 250V and is 11.9cm long [4].

These hybrid systems however may not be appropriate for constructing a large phased array antenna system since they generally require several thousand elements fed by a phase shifter as well as a switch for every antenna element. This can complicate assembly, not to mention the parasitic losses introduced and increase in size.

Monolithic systems using single and multilayer processing have recently been reported to meet current phased array system demands such as lighter weight and compact size. How et al. also presented a steerable phased array antenna using single-crystal yttrium-iron-garnet (YIG) phase shifters, illustrated in Figure 2.7. This array antenna tuned the input phases to the antenna elements by varying the bias magnetic field [5].

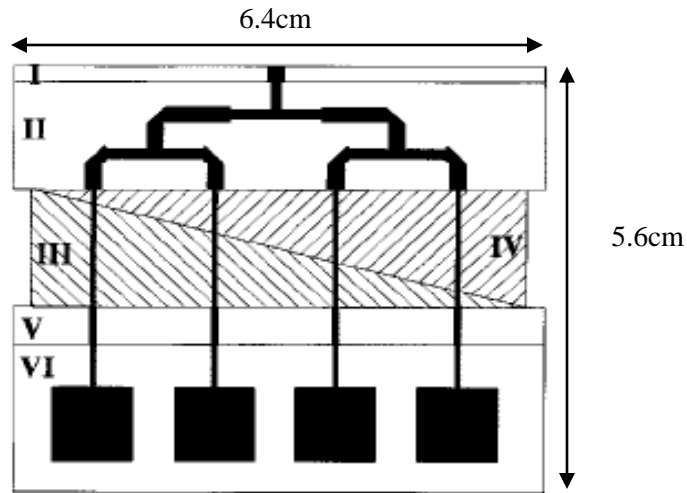


Figure 2.7: Layout of a phased array antenna using single-crystal YIG phase shifters [5].

Shown in Figure 2.8 is a four element array monolithically implemented on single high resistivity silicon (HRS) substrate, and consists mainly of Wilkinson power dividers, $\text{Ba}_x\text{Sr}_{1-x}\text{TiO}_3$ (BST) true time delay (TTD) phase shifters, and microstrip radiating patches. In this case, DC bias voltages of up to 300V were required to vary the phase. The phased array has a total area of 4.6cm x 5.3cm and an operational bandwidth of 8.7% [6].

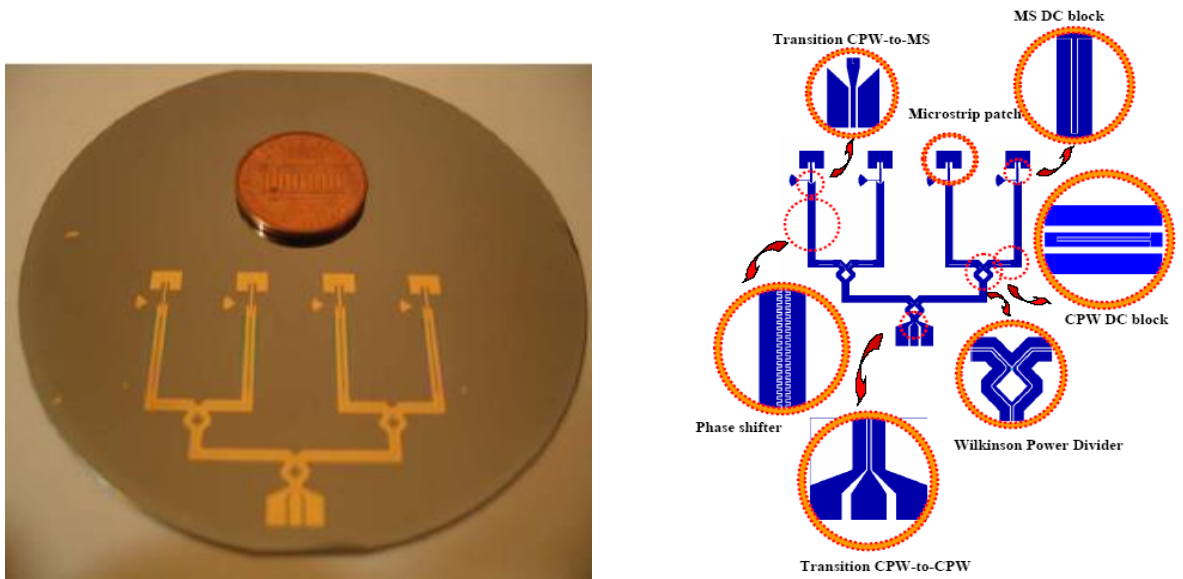


Figure 2.8: Four-element phased array integrated monolithically on a silicon substrate [6].

Three-dimensional Microwave Monolithic Integrated Circuits (MMICs) involve stacking multiple layers of functional modules in a limited estate. With the rising need for more compact ESA modules, this technology can be extended to multilayer ESAs. The array’s components are processed and interconnected through the several layers to obtain shorter path lengths. One of the most common multilayer processes used to produce integrated ESAs is the Low Temperature Co-fired Ceramics (LTCC) process. LTCC is a high temperature process that produces multilayer circuits from ceramic substrate tapes or sheets. Conductive, dielectric, and resistive pastes are applied on each sheet or tape as needed, and the sheets are then laminated together and fired at temperatures up to 850°C in one step. The drawbacks of this technology are significant including poor thermal conductivity and shrinkage during the firing process which results in inherent feature size limitations especially at higher frequencies [7]. An LTCC-processed module consisting of single sheets with specific functions such as phase shifting, polarization, and grounding all have to be laminated together and fired in one step, as shown in Figure 2.9(a) [8]. Spin-on organics such as Benzocyclobutene (BCB) and Polyimide (PI) have also been used in designing vertically integrated ESA modules. Figure 2.9(b) illustrates a proposed 3-D vertically integrated phased array module where the layers consist of 22µm thick PI layers that are isolated with trenches and ground plane layers [9]. The issues that arise in forming this integrated module include “outgassing” defects, edge-bead effects, as well as the

planarity and leveling of polyimide over deep-via structures and layer-delaminating as a result of multi-layer stress.

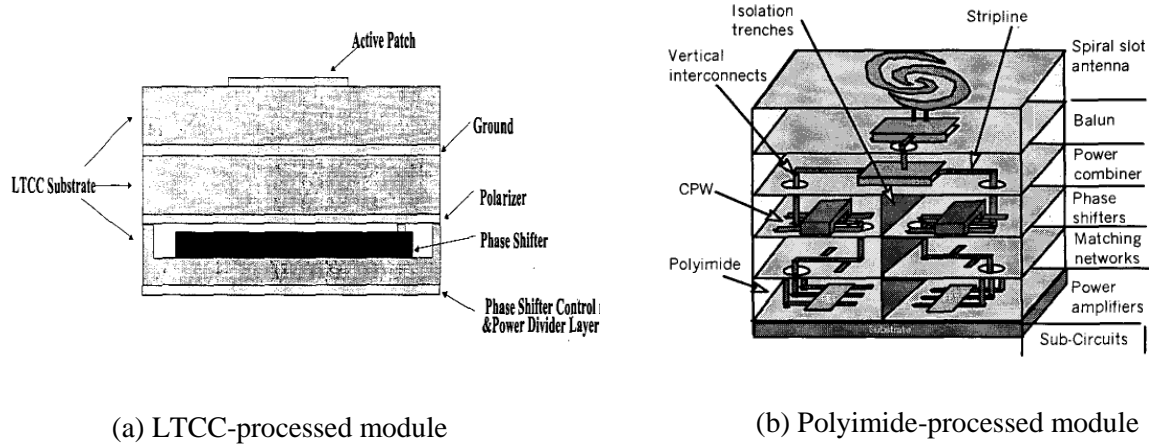


Figure 2.9: Examples of 3-D multilayer 'stacked', monolithically integrated phased array modules. (a) An LTCC processed substrate with stacked functional layers [8]. (b) A 3-D phased array module vertically integrated with 22 μ m thick polyimide layers [9].

In [10], a MEMS-based ESA fabricated using printed circuit processing is reported. The loaded-line phase shifters and feed network are monolithically integrated on a Duroid substrate and operates at 9.1GHz. The ESA is composed of three stacked layers of Kapton tape, RT/Duroid substrate and a Polyflon bonding film that are laminated with thermocompression bonding to obtain the ESA prototype, as illustrated in Figure 2.10. The total area of the ESA is about 29cm².

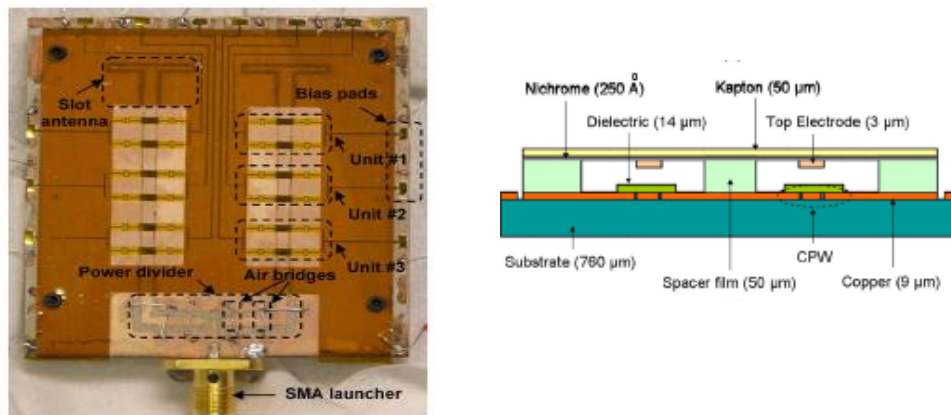


Figure 2.10: Top view and cross-sectional view of the PCB MEMS-based ESA [10].

Therefore, the conventional methods used to integrate ESA components have several disadvantages such as wasted area and volume, outgassing of organics and limited feature resolution. There is a need to develop a new approach for integration that will achieve breakthroughs in size, weight and cost and minimize any process variations.

2.2 MEMS and Micromachined ESA Components

This section will present in detail the most current developments and designs in ESA module components including RF MEMS capacitive switches, MEMS phase shifters and Butler matrices.

2.2.1 RF MEMS Switches

RF switches are used in a wide array of commercial, aerospace and defense application areas including satellite communications systems, wireless communications systems and radar systems. In this thesis, capacitive RF MEMS switches are designed and optimized for their implementation in an X-Band 3-bit phase shifter, and are a vital component of the final integrated phased array module. In order to choose an appropriate RF switch for this application, the required performance specifications must first be considered. These include the switch's capacitance ratio, isolation and insertion losses, power handling capabilities, switching speed, and cost of fabrication.

Traditional switches such as waveguide and coaxial switches show low insertion loss, high isolation, and good power handling capabilities but are power-consuming, slow and unreliable for prolonged applications. Current solid-state RF technologies such as the PIN diode and FET are favored for their high switching speeds, commercial availability, low cost and ruggedness. Some commercially available RF switches can support high power handling, but require large, massive packages and high power consumption. In spite of their design flexibility, two major areas of concern with solid-state switches persist: nonlinearity and bandwidth limits at higher frequencies. When operating at high RF power which is the case in satellite space-based radar systems (SBR), nonlinear switch behavior leads to spectral re-growth; this interferes with the energy outside of its allocated frequency band and causes adjacent channel jamming. An additional strong driving mechanism for

pursuing new RF technologies is the fundamental degradation of insertion loss and isolation at signal frequencies above 1-2 GHz.

The development of MEMS technology enables the fabrication of electromechanical and microelectronics components in a single chip with enhanced RF performance. MEMS RF switches combine the advantages of traditional electromechanical switches (low insertion loss, high isolation, high linearity) with those of solid-state switches (low power consumption, low mass, long lifetime). These devices are typically operated with electrostatic forces and they draw no current other than a very small leakage current. The low loss dielectrics and high conductivity metals used to construct these switches enable them to have low losses. Table 2.1 shows a comparison of MEMS, PIN diode and FET switch parameters. A disadvantage of RF MEMS switches is their actuation voltages (30-80V) which necessitate the use of CMOS up converters to raise the input 3-5V control voltage to the actuation voltage [11]. Despite that, all the advantages exhibited by RF MEMS switches as well as their potential for high reliability long lifetime operation make them a promising solution to existing low-power RF technology limitations.

Table 2.1: Performance comparison of FETs, PIN diode and RF MEMS Electrostatic Switches [11].

Parameter	RF MEMS	PIN-Diode	FET
Voltage (volts)	20-80	\pm 3-5	3-5
Current (mA)	0	0-20	0
Power Consumption (mW)	0.5-1	5-100	-0.5 – 0.1
Switching speed	5-60 μ s	1-100ns	1-100ns
C _{off} (series) (fF)	1-6	40-80	70-140
R _s (series) (Ω)	0.5 – 2	2-4	4-6
Capacitance Ratio	40-500	10	n/a
Isolation (1-10GHz)	Very high	High	Medium
Isolation (10 – 40GHz)	Very High	Medium	Low
Isolation (60 – 100GHz)	High	Medium	None
Power Handling (W)	<1	<10	<10

The primary goals of the capacitive MEMS switch performance for ESAs include: low actuation voltage, low insertion loss and high isolation, high power handling capability and fast switching speed. By manipulating the switch dimensions and parameters, these parameters can be fine-tuned, however there are tradeoffs. In ESA design, the two essential design requirements include fast switching speed and high power handling capability. In the design of the integrated ESA module, each switch would have to be capable of handling up to 700mW of power. Capacitive switches have a large contact area that allows them to handle more RF power typical of radar systems than metal-to-metal contact switches [11].

The capacitive switch typically consists of a metal bridge suspended over a driving electrode, typically coated with a thin dielectric for DC isolation when the bridge is actuated in downstate. The switch has two states – with no bias applied, the bridge remains in the upstate and is referred to the ‘on’ state because it allows the signal to pass through. However, when a DC voltage is applied, the switch membrane is pulled down, introducing a high capacitance and resulting in a reflective switch where the signal is not allowed to pass through; also referred to as the ‘off’ state. In order to obtain high isolation switches, large ‘off’ state capacitances and small negligible ‘on’ state capacitances are required to produce large capacitive ratios (C_{off}/C_{on}). Moreover, to lengthen the switch’s lifetime, it is necessary to try to reduce the actuation voltage required to pull-down the membrane into ‘off’ state. There has been extensive work done on MEMS switches specifically the capacitive shunt and series switches. Switch research and development focus is on different design parameters including high isolation (large capacitance ratios), lower actuation voltages, faster switching speed or enhanced power handling capability.

Raytheon’s capacitive low-loss shunt switch, also referred to as the Texas Instrument’s switch, has been used in X-band and K-band phase shifters as shown in Figure 2.11. Its performance included actuation voltages ranging between 30-50V, switching speeds as low as 3-5 μ s, with a loss of only 0.07dB at frequencies ranging between 10 – 40GHz [12]. The capacitance ratio observed was approximately 80 with isolation better than only -20dB at 10GHz.

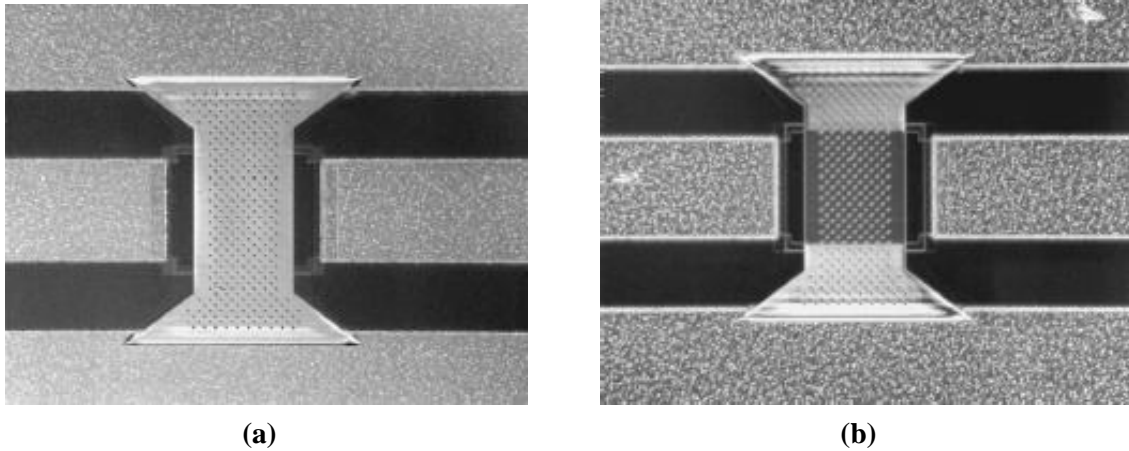


Figure 2.11: SEM image of the switch designed by Raytheon. (a) The switch in 'on' state with no DC bias applied. (b) The switch in 'off' state with a DC voltage applied [12].

The University of Michigan has developed a shunt capacitive switch with a lower spring-constant membrane. In Figure 2.12, the membrane is connected using a folded spring to the anchors lowering the spring constant to about 1-3N/m, and resulting in a pull down voltage of about 8-15V [13].

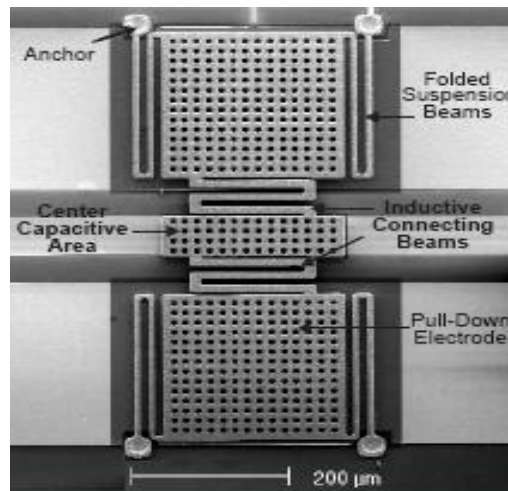


Figure 2.12: University of Michigan's low spring-constant MEMS switch [13].

In terms of high power handling, the University of Michigan improved their design further by introducing a top electrode [14], as shown in Figure 2.13. These electrodes are 2-2.5 μm above the

actuation pads and were used to pull the switch from the down state to the up state. These electrodes improved switch stability and substantially increased the RF power range over which the switch can withstand during hot switching.

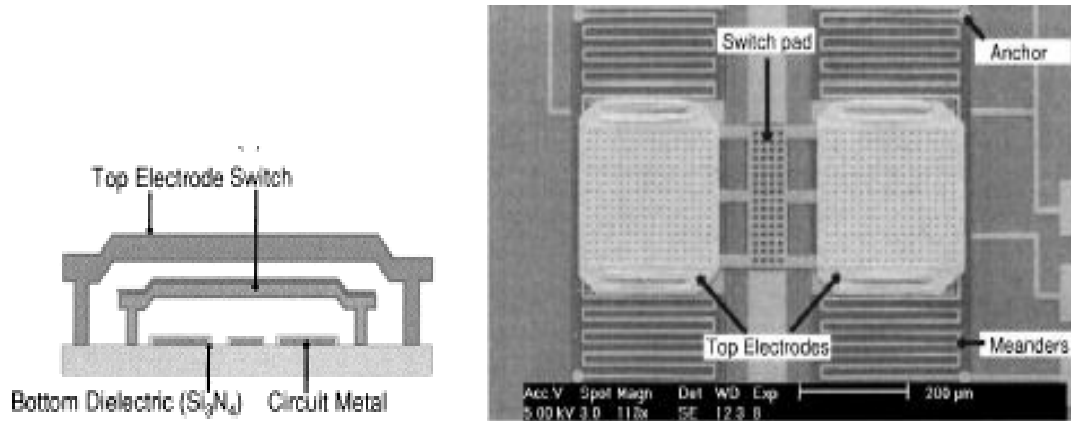


Figure 2.13: Side view and top view of the University of Michigan's switch with enhanced power handling capabilities [14].

Several attempts have been reported to achieve high isolation such as using complex tuned switches [15] or by placing several MEMS switches in series [16], limiting miniaturization capabilities. Researchers have also proposed the use of high dielectric-constant ceramics such as strontium-titanate oxide to achieve high isolation performance with a capacitance ratio of 600 [17]. Fabrication methods such as reducing the dielectric thickness and increasing the dielectric constant are limited due to effects such as dielectric breakdown, charge trapping and pin-hole defects.

A corrugated cantilever arm in [18] is used to design a metal-to-metal contact switch as well as a capacitive coupling switch. Figure 2.14 denotes the structure of the corrugated beam. This switch is relatively small ($55\mu\text{m}$ by $45\mu\text{m}$) and the pull-down electrode is in the RF path directly beneath the cantilever. To minimize the parasitic effects of the pull-down electrode, it is constructed from a high sheet resistivity metal. In the 'off' state, this switch curls up creating a relatively large separation distance of approximately $10\text{-}15\mu\text{m}$, which results in a high isolation and at the same time creates an increase in the pull-in voltage. It has been reported that about 80V is required for a good contact resistance whereas the primary actuation voltage is around 35V . The capacitance ratio achieved with this design is 141:1.

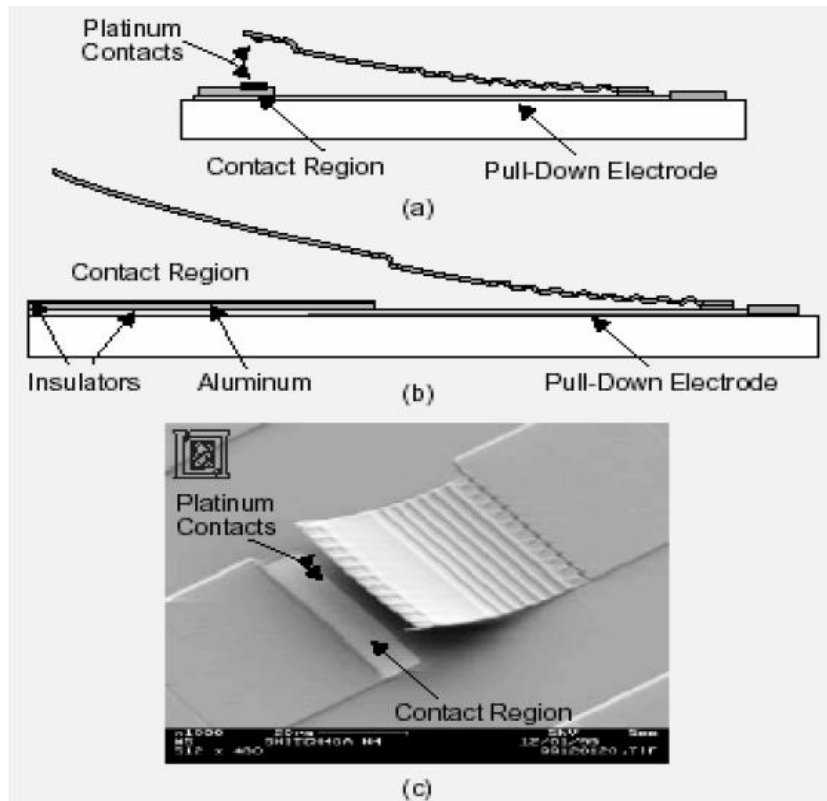


Figure 2.14: Lincoln Laboratories in-line MEMS-series switch in (a) metal-metal contact, (b) capacitive configuration and (c) SEM of the metal-metal contact switch [18].

2.2.2 MEMS Phase Shifters

Phase shifters are critical components in the electronic steering of antenna beams in phased-array antennas. In the passive ESA, each T/R module usually feeds several phase shifters, which are each placed directly behind the radiating element, thus directly contributing to the noise figure of the system. The transmit power is also directly reduced by the loss of the phase shifters. The advantage is that a simpler and lower cost system results due to the smaller number of T/R modules and other components required. However, this is feasible only if the phase shifters are of very low loss since the T/R modules must compensate for the loss in the phase shifters. A high loss in the phase shifters means that the T/R module needs to be much higher in transmit power, larger in size and more costly,

thus defeating the purpose of achieving a simplified design with a passive array. The phase shifter's performance can be greatly enhanced with reduced complexity and cost using RF MEMS technology.

The MEMS switch's desirable characteristics have led to their implementation in phase shifters. There are several approaches to MEMS-based phase shifters such as the switched-line circuit (also referred to as the true-time delay circuit), the distributed-line circuit, and the reflected-line circuit. There has been widespread work done on phase shifters based on MEMS by organizations such as Raytheon, Rockwell and many others.

For ESAs, the three choices for phase shifters are ferrite, PIN diode or MEMS-based phase shifters. Table 2.2 shows a comparison of loss and approximate cost of a 4-bit phase shifter [16]. Ferrite phase shifters contribute very low RF losses but can add significantly to weight and cost. PIN diode phase shifters have higher RF loss and require significant driving power. MEMS phase shifters are an attractive alternative to the conventional options since they are small, lightweight, inexpensive, and contribute smaller RF losses. Moreover, since MEMS phase shifters are electrostatically actuated, they require essentially no DC current, minimizing power consumption. The average loss of MEMS phase shifters is 2dB. This in turn translates to improvements in radar or a two-way telecommunication system. Therefore, one can eliminate an amplifier stage in the T/R chain, also resulting in a power reduction of 20-100mW per element at X-band frequencies.

Table 2.2: 4-bit Phase Shifter Loss and Cost Comparison [11].

Phase Shifter	Loss (dB)	Cost (\$)
Ferrite	0.5	75
PIN Diode	3.0	40
MEMS	2.0	2

The aforementioned capacitive switches have been implemented in a 2-bit and 4-bit microstrip X-band MEMS phase shifter using Lange couplers integrated on a silicon substrate. An average loss of 1.3dB is observed between the frequencies of 8-10GHz and a limited bandwidth of 7 – 11GHz due to the use of Lange couplers in the design. The phase shifter described is illustrated in Figure 2.15 [19].

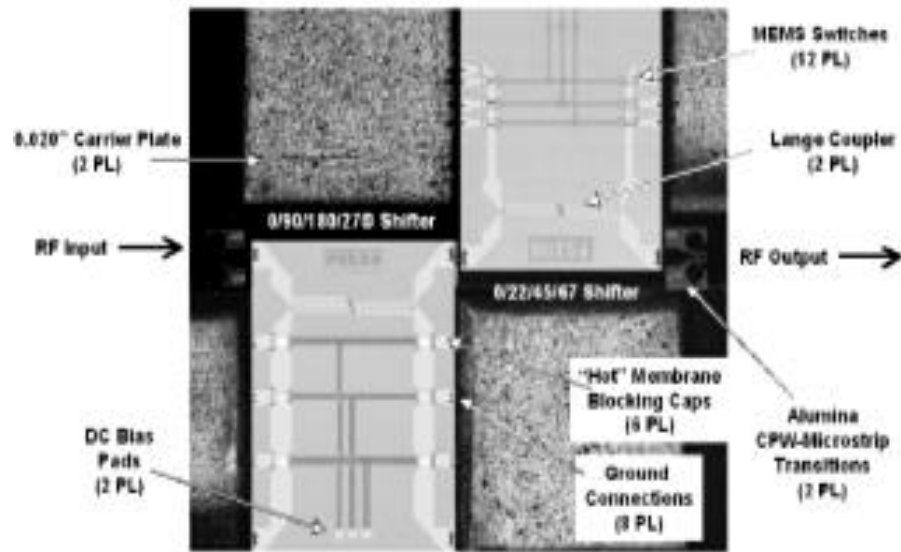


Figure 2.15: Raytheon's 4-bit X-band MEMS phase shifter designed using 3dB Lange couplers integrated on a silicon substrate [19].

Rockwell Science Center created a wideband 4-bit switched-line phase shifter using a SP4T (single-pole four-throw) MEMS switch shown in Figure 2.16. The switches used in this case are series capacitive switches in a microstrip line configuration. This phase shifter represents the smallest area (4.9mm by 4.25mm) MEMS phase shifter developed to date with very low insertion loss performance (0.25 – 0.35dB/bit at X-band) [20, 21].

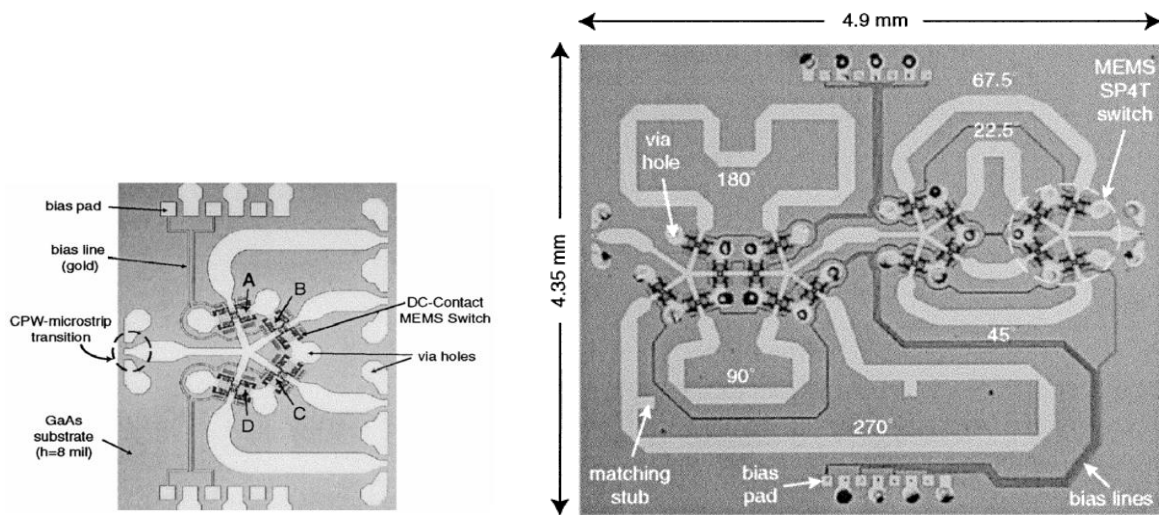


Figure 2.16: Rockwell Scientific/ University of Michigan 4-bit MEMS phase shifter [21].

2.2.3 Butler Matrices

Design challenges faced when designing and fabricating Butler matrices include the realization of the crossover lines and the minimization of matrix real estate without jeopardizing circuit performance and complicating circuit fabrication. Several efforts have been reported to achieve compact Butler matrices with simple crossover lines. A microstrip-slot-microstrip approach is used in [22, 23] where the matrix is printed on two distinct substrate layers with a ground plane in between, as shown in Figure 2.17. The crossover lines are realized by coupling through the slot from one layer to the next. This technique introduces fabrication complexities and requires accurate substrate alignment.

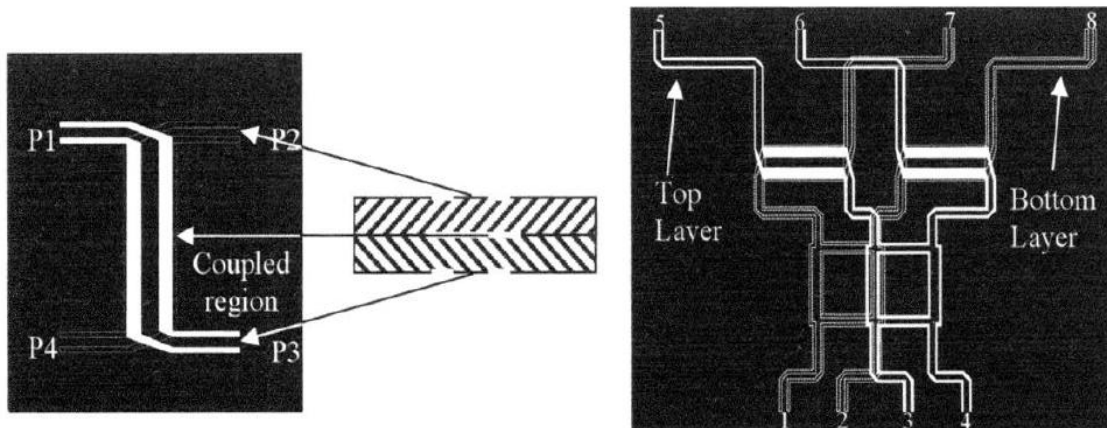


Figure 2.17: Layout of the slot-coupled coupler and 4 x 4 Butler matrix. The crossover lines are realized by coupling through the slot from layer to the next [23].

In [24 and 25], the need for crossovers is eliminated by replacing the crossing with a 0dB branch-line coupler as shown in Figure 2.18. Even though this design greatly simplifies the fabrication and assembly of the BM, the circuit's real estate is drastically increased.

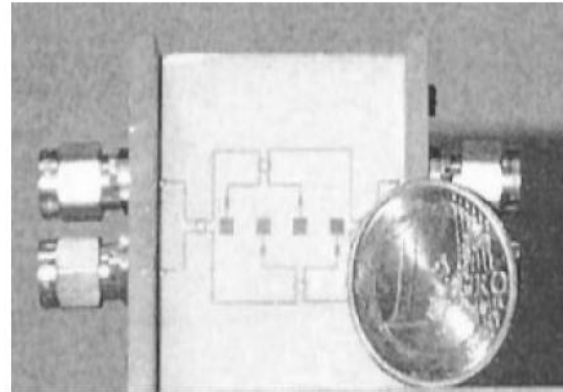
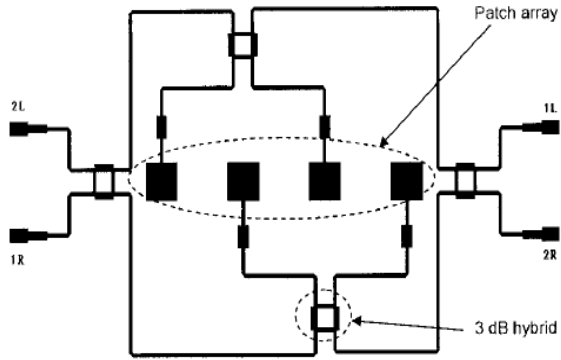


Figure 2.18: Layout and photo of the 4 x 4 Butler matrix network without any crossovers using a 0-dB branch-line coupler in order to reduce circuit fabrication complexity [24].

A 4 x 4 compact BM developed in [26] uses a new bi-layer structure and is illustrated in Figure 2.19. The structure is low-loss and compact using foam-suspended strip line. Transitions between the two layers were achieved using contact-less coupling and the crossovers occur on the opposite sides of the suspended substrate with increased characteristic impedances lines to reduce the coupling capacitance between the overlapping lines.

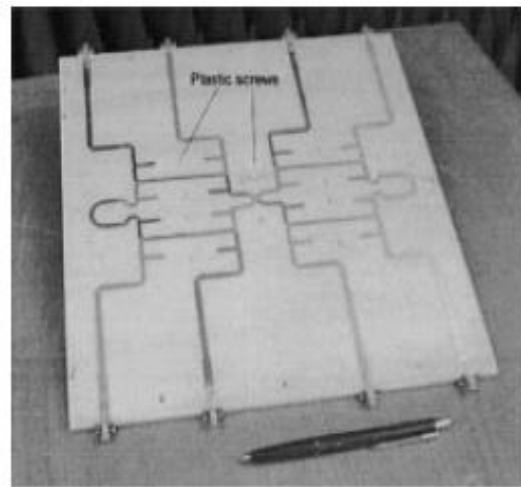
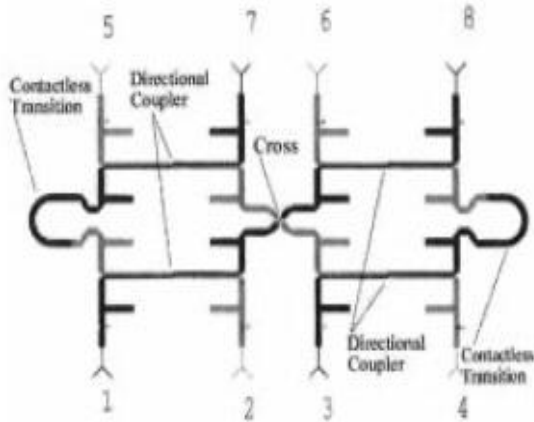


Figure 2.19: 4 x 4 compact Butler matrix layout and realized structure. The structure is low-loss and compact using low-loss foam-suspended strip line [26].

Current research shows that there is a need to develop a process to achieve a compact integrated Butler matrix reducing the complexity of crossover design and matrix fabrication without compromising wafer real estate and matrix RF performance.

Chapter 3

SPNT Capacitive Shunt Dual-Warped Beam Switches

Space-Based Radar (SBR) systems applications require single-pole n-throw (SPNT) switches with reduced actuation voltages, fast switching speeds, compact size, high isolation and low insertion loss. This section will introduce a novel design approach to capacitive MEMS switches using warped bimetallic beams with low-loss and high isolation over X-band frequencies. The fabrication process flow for attaining such a switch structure will also be presented. Mechanical modeling obtained of this structure will be discussed followed by a detailed description of the measured results.

3.1 SPST Dual Warped-Beam Capacitive MEMS Switch

In general, MEMS switches can be classified into two main categories: metal-to-metal and capacitive switches. Shunt capacitive switches are chosen for the design of the integrated ESAs because their large contact area can handle more RF power than metal-to-metal contact switches [11], an essential requirement for space-based applications. The electrostatically actuated MEMS switches outperform solid state switches such as FETs, HEMTs and PIN diodes [15]. MEMS switches have low insertion loss and do not exhibit the nonlinearities associated with semiconductor junctions in PIN and FET devices. This improves their distortion characteristics and power handling capabilities, an important consideration in phased array systems that contain a large number of switches and limited power resources.

The physical structure of the electrostatic-type shunt capacitive MEMS switch in its two states, ‘on’ and ‘off’, is shown in Figure 3.1. In this thesis, the terms ‘on’ and ‘off’ states, which correspond to the switch in “upstate” and “downstate” respectively, will be used to describe and characterize the switch’s behavior. The MEMS switch is electrostatically actuated with fixed-fixed metal bridges suspended over the center conductors of the FGC transmission line. When no DC bias is applied, the switch presents a very small shunt capacitance between the center conductor and ground planes. This state is referred to as the ‘on’ state and the switch behaves as a through switch allowing the RF signal to propagate through with negligible loss. When a DC voltage is applied

between these two metal layers, the electrostatic force starts to pull the bridge towards the lower conductor. The bias is then increased until a threshold voltage is reached at which point the bridge's spring force is overcome and the bridge collapses down on top of the signal line separated by a thin dielectric isolation layer. The switch emulates a short circuit by introducing a large capacitance and reflects the signal back. This state is referred to as the 'off' state.

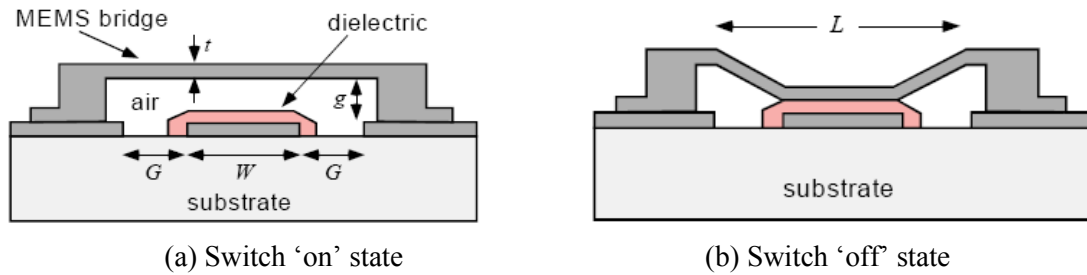
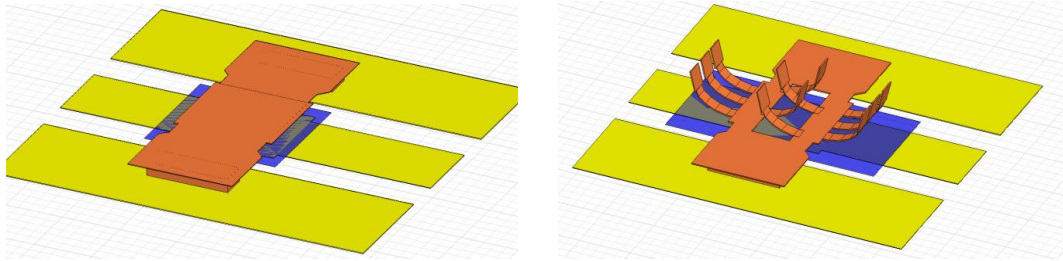


Figure 3.1: Shunt capacitive MEMS switch structure in its two states. (a) Capacitive shunt switch in 'on' state. (b) Capacitive shunt switch in 'off' state.

Electrostatically actuated capacitive MEMS switches have been developed and optimized in various applications due to their low-loss and high-linearity [11]. Several attempts have been reported to achieve high isolation such as using complex tuned switches [15] or by placing several MEMS switches in series [16], limiting miniaturization capabilities. A high isolation switch was achieved in [13] by reducing the switch's spring constant using serpentine springs and increasing the gap height. However, a reduced spring constant may limit the switching speed as well as reliability of the switch to return to its initial state after actuation. Researchers have also proposed the use of high dielectric constant ceramics such strontium-titanate oxide to achieve high isolation performance [17]. Enhancing the switch's performance in one state comes at the expense of the switch's performance in the reverse state, a trade off faced when designing capacitive MEMS switches. In order to enhance the switch's isolation in the 'off' state, the electrode area beneath the beam must be increased, resulting in an increase in the 'off' state capacitance and thereby enhancing the isolation. However, by increasing the overlapping area, the switch's 'on' state capacitance is also increased, compromising the switch's return loss in the 'on' state. Fabrication methods such as reducing the dielectric thickness and increasing the dielectric constant are limited due to effects such as dielectric breakdown and charge trapping. This thesis proposes a simple and novel design of the capacitive

shunt switch that optimizes the switch's performance in 'off' and 'on' states without the aforementioned tradeoffs. The overall electrode-beam overlapping area is increased by adding Au-Cr beams to the edge of the MEMS switch. These beams warp upwards due to the residual tensile stress. On the other hand, by adding these beams to the center of the switch, the overlapping capacitive area is effectively decreased for improved 'on' state performance, as shown in Figure 3.2.



(a) Conventional Switch

(b) Proposed Dual-Warped Beam Switch

Figure 3.2: (a) Conventional switch. (b) Proposed dual-warped beam switch.

A summary of the capacitive switches reported in literature are listed in Table 3.1 to compare the proposed dual warped-beam design to the current technology available.

Table 3.1: Summary of capacitive shunt switches reported in literature compared to the proposed design.

Switch Dimensions L x W (μm)	Dielectric (\AA)	Actuation Voltage (V)	Switching Time (μs)	C_{off} (pF)	Capacitive Ratio	Reference
350 x 200	Si_3N_4 (1000)	30-50	3	1-6	80-120	[12]
700 x 250	Si_3N_4 (1500)	6 – 20	20-40	1-3	30 - 50	[13]
350 x 140	Si_3N_4 (1000)	12 – 25	6 – 15	0.5-3	20-40	[15]
300 x 100	SrTiO_3^* (1000)	8 – 15	N/A	50	600 – 700	[17]
300 x 80	SiO_2 (5000)	110	N/A	4	N/A	[27]
160 x 90	Si_3N_4 (2500)	20	250	2-6	N/A	[28]
400 x 150	Si_3N_4 (1800)	25-27	6-17	10	170	[30]

* A high dielectric constant material requiring special processing.

The proposed dual-warped beam switch design offers a competitive switching speed and a large off-to-on capacitance ratio in comparison to the switches reported in literature, and achieves this without the use of a high dielectric material or complex tuning circuits. An RF model of the switches is used to analyze the effects of the switch design parameters and RF performance. The optimization of the switch mechanical design is discussed where the pull-in voltage can be lowered to 27V. Measured results are presented for several variations of the dual-warped beam switch, demonstrating good performance over a wide range of frequencies (5 – 30GHz).

3.1.1 Electrical Design

The capacitive shunt switches are implemented on a 50Ω finite ground coplanar (FGC) waveguide. The FGC line dimensions are shown in Figure 3.3. The FGC signal line's width is increased at the center to a width of 152μm to maximize the overlapping electrode area of the switch. Moreover, a larger FGC line is used to implement a longer switch structure with a smaller spring constant thereby effectively reducing the actuation voltage. The input of the CPW line with dimensions W/S/G is set to 60/25/120 to accommodate 150μm pitch ground–signal–ground coplanar RF probes. The signal line width is adjusted to be 60μm at the FGC line input and 120μm at the line's center by Sonnet[®] [46] to yield characteristic impedance close to 50Ω.

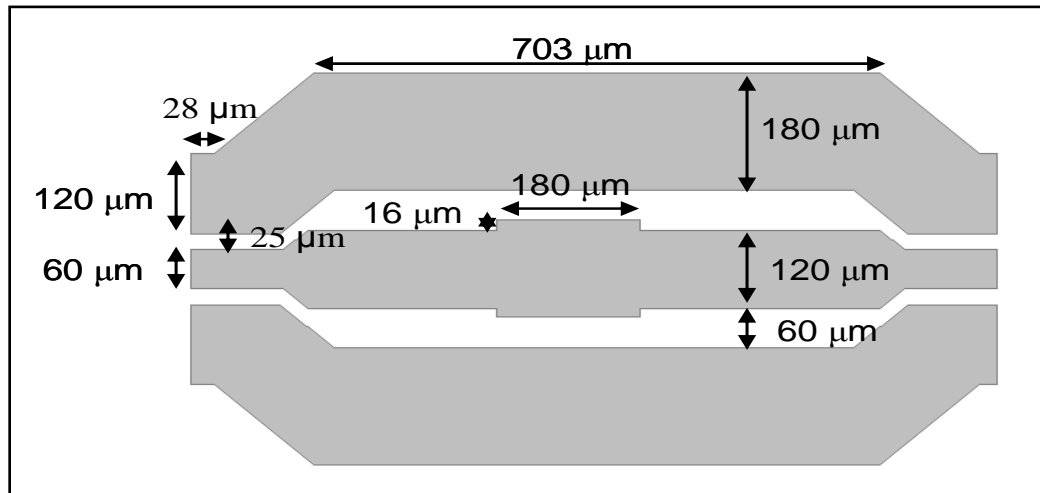


Figure 3.3: CPW layout and dimensions.

The schematic view of the four capacitive MEMS shunt switches designed is shown in Figure 3.4. Figure 3.4(a) shows the traditional switch design. It is referred to as Switch 1 and will be used as the reference to which any changes in RF performance will be compared. Figure 3.4(b) illustrates Switch 2, with additional warped beams incorporated to its borders in order to enhance the downstate capacitance in ‘off’ state by increasing the overlapping capacitive area. Figure 3.4(c) illustrates Switch 3; the switch with warped beams introduced to the center of its geometry, in order to reduce the upstate capacitance. Figure 3.4(d) illustrates the dual-warped switch, Switch 4, with warped beams incorporated to the structure’s center and borders. All geometry labels and switch dimensions are provided in the top view of the switch in Figure 3.4(e) and Table 3.2.

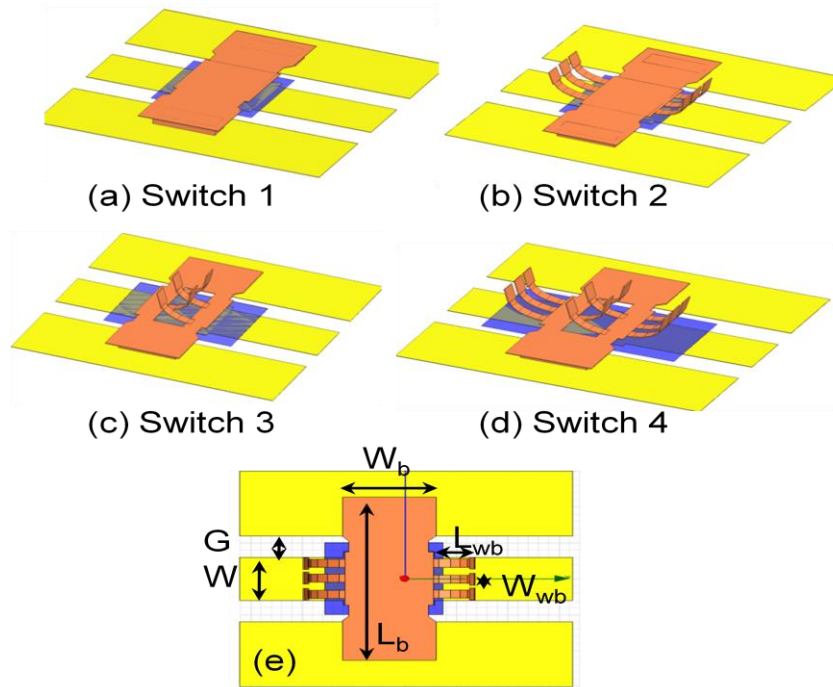


Figure 3.4: Schematic views of (a) Switch 1, (b) Switch 2, (c) Switch 3, (d) Switch 4 and (e) the top view of Switch 2.

The bimorph beams added to the switch’s geometry are designed at lengths varying from $25\mu\text{m}$ to $110\mu\text{m}$ and widths varying from $10\mu\text{m}$ to $25\mu\text{m}$. The beams are spaced out by $10\mu\text{m}$, limited by switch geometry and fabrication tolerances. The dimensions of these beams were set from RF simulations in order to achieve optimum RF performance at 10GHz. Implementing these beams to the

outline of the basic switch geometry effectively increases the overall overlapping switch-electrode area and therefore capacitance by an additional 40 - 130%.

Table 3.2: Dimensions of MEMS switch and circuit in μm .

Parameter	Value	Parameter	Value
W_b	150	W	120
L_b	450	S	60
L_{wb}	55 – 110	G	180
W_{wb}	25	t	1.25
g_0	2.6		

The switch's 'on' state performance is primarily determined by the 'on' state capacitance (C_{on}) presented by the switch. C_{on} is a function of the overlapping area between the switch beam, the driving electrode size and the switch gap height. The switch's 'off' state RF performance depends on the off-state capacitance (C_{off}) determined by the overlapping area, and the series inductance (L_s) determined by the geometry of the switch's supporting beams. The combination of these two terms increases the isolation and tunes the resonant frequency as governed by the equation:

$$f_r = \frac{1}{2\pi\sqrt{C_{off}L_s}} \quad (3.1)$$

Therefore there are two methods to enhancing the switch's performance in the 'on' and 'off' states. One is to increase the capacitive ratio, the off-to-on ratio of capacitances, by maximizing the 'off' state capacitance and minimizing the 'on' state capacitance. The second method is to increase the series inductance of the switch by introducing high inductance springs into the switch's structure. However, the trade-off, purely inductively resonant MEMS shunt switches result in less bandwidth than standard shunt switches but with higher isolation around the resonant frequency [15]. As will be seen, by simultaneously increasing the 'off' state capacitance and increasing the series inductance, wider bandwidth capacitance switches with good isolation performance can be obtained. The switch capacitances are typically between 20-60fF in the 'on' state, and 2-7pF in the 'off' state, depending on the size of the bridge [15].

Several high inductance spring designs are considered to further enhance the switch's performance and reduce the actuation voltage. Shown in Figure 3.5 are the various springs designed, fabricated and tested. All supporting spring beam widths are set to $10\mu\text{m}$.

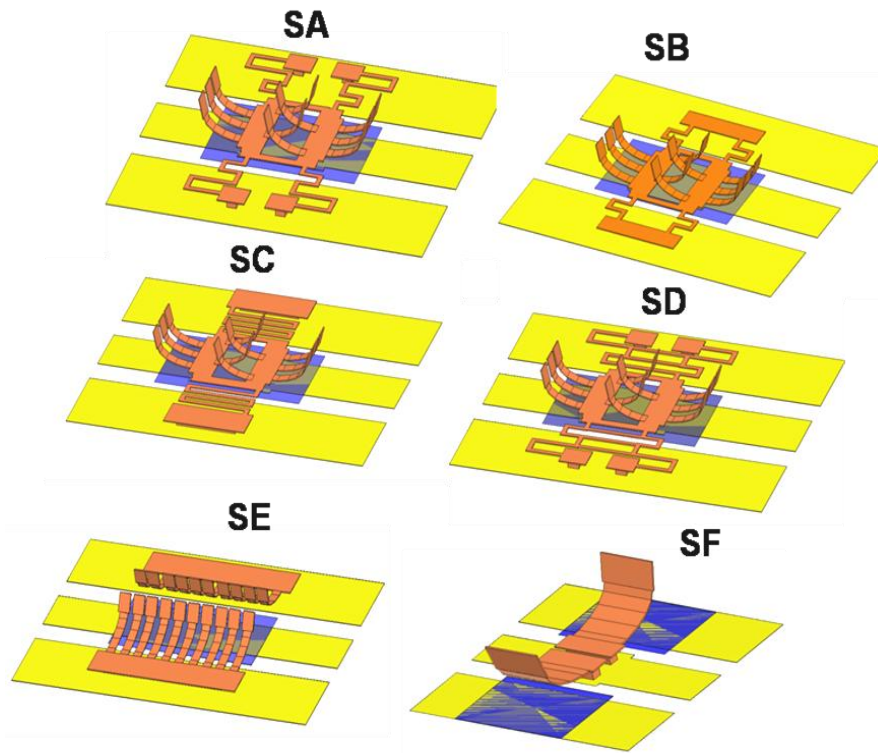


Figure 3.5: Different capacitive switch spring designs using the warped-beam concept.

Several meandered spring designs are considered including spring A, spring B, spring C and spring D. Spring D is very similar in design to spring A with reinforcing beams implemented across the meanders in an effort to minimize any warping that can occur in the supporting meandered beams. Spring B employs meandered fixed-fixed flexures into the switch's geometry. Spring E uses warped cantilevers instead of a fixed-fixed beam structure because cantilever beam structures require lower actuation voltage and exhibit higher isolation than the fixed-fixed beam [29]. The purpose of Switch F's design is to isolate the dielectric and pull-down electrode from the RF signal line thereby isolating any induced RF voltage resulting from high RF powers. As a result, this may enhance the power handling capabilities while introducing flexibility in terms of actuation voltage and other design parameters. Moreover, by placing the electrodes along the ground plane, the RF performance of the switch is dissociated from its voltage requirements.

A balance between the switch's mechanical and RF performance is needed when selecting the spring design. The best switch with ideal series inductance, mechanical performance and RF performance within the X-band frequencies according to simulated and measured results is Switch C as will be discussed in the following sections.

3.1.2 Fabrication Process

Using these designs, a set of MEMS capacitive switches have been fabricated. The MEMS switches are based on a 5-mask batch process developed at the University of Waterloo and built in CIRFE labs [30]. An alumina substrate is selected for the base substrate since it retains its intrinsic properties during the process and exhibits a good RF performance at high frequencies. In Figure 3.6(a), 400Å of Cr and 1200Å of Au are e-beam deposited and patterned on a 10mil thick alumina wafer. These layers include the FGC waveguide line, electrode and high resistivity bias line.

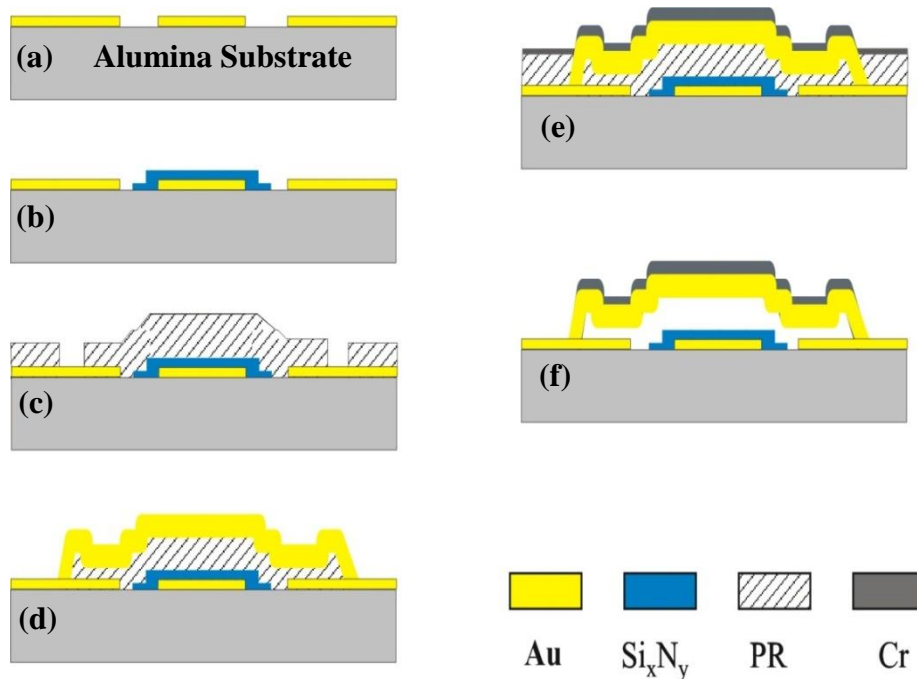


Figure 3.6: The 5-mask fabrication process for all the switch designs.

Next an 1800Å silicon nitride layer (Si_3N_4) is deposited using a Trion Plasma Enhanced Chemical Vapor Deposition (PECVD) system at 250°C and patterned over the electrode area. It is also deposited over the bias lines to isolate the ground lines from the applied DC voltage. To provide good adhesion between the silicon nitride and Au layer, a very thin film of TiW is sputtered onto the gold layer before depositing the nitride. The nitride and TiW layers are patterned with the nitride mask and etched using buffered hydrofluoric acid (BHF) and 30% diluted hydrogen peroxide, respectively. In Figure 3.6(c), the sacrificial layer is then spun cast to a thickness of 2.6µm. The sidewalls are sloped positively for good sidewall metal coverage for anchors by hard baking the resist at 120°C for about 2 minutes to re-flow and bake out any solvents. The MEMS air bridge is then fabricated by depositing a thin seed layer of 2000Å of Au, and by electroplating it up to 1.2µm. A thin layer of Cr is then deposited on top of the electroplated Au layer, patterned and etched to form the bimetallic structure. After etching the top metal in a similar manner as the first step, the wafer is released. This process involves a two-fold approach – a partial dry and partial wet release. First, the partial dry etch is performed in the Trion Reactive Ion Etch (RIE) system using a pure oxygen plasma recipe with high pressure, high ICP (Inductive Coupled Plasma) power and low RF power. This reduces etch directivity, resulting in a more isotropic etch to help partially release the devices.

To enhance and accelerate the isotropic etch, the wafer is raised into the field of the ICP plasma using a 3.5 inch high Quartz tube, essentially recreating a plasma asher's environment. The setup is shown in Figure 3.7 along with a microscope picture of the devices after performing a 300 second partial dry etch.

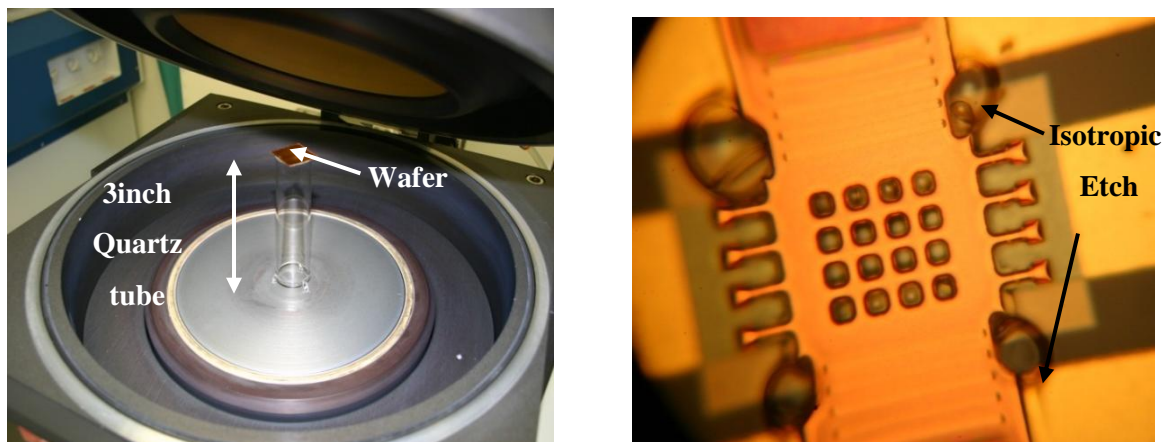


Figure 3.7: Dry release set-up and captured image of the isotropic etch.

The RF power is maintained less than 150W to prevent the substrate from heating up and affecting the switch structures. More information on this fabrication process is included in Appendix A.

The ‘off’ state capacitance is highly dependent on the roughness of the dielectric material used, where a roughness of 40Å results in a degradation of 50% in the total capacitance [11]. A TiW electrode is used as an adhesion layer so as to result in a very smooth dielectric layer (1800Å of nitride). The average roughness of the electrode is below 12.3Å and is characterized using a Veeco profilometer, where the average roughness across the wafer surface is shown in Figure 3.8.

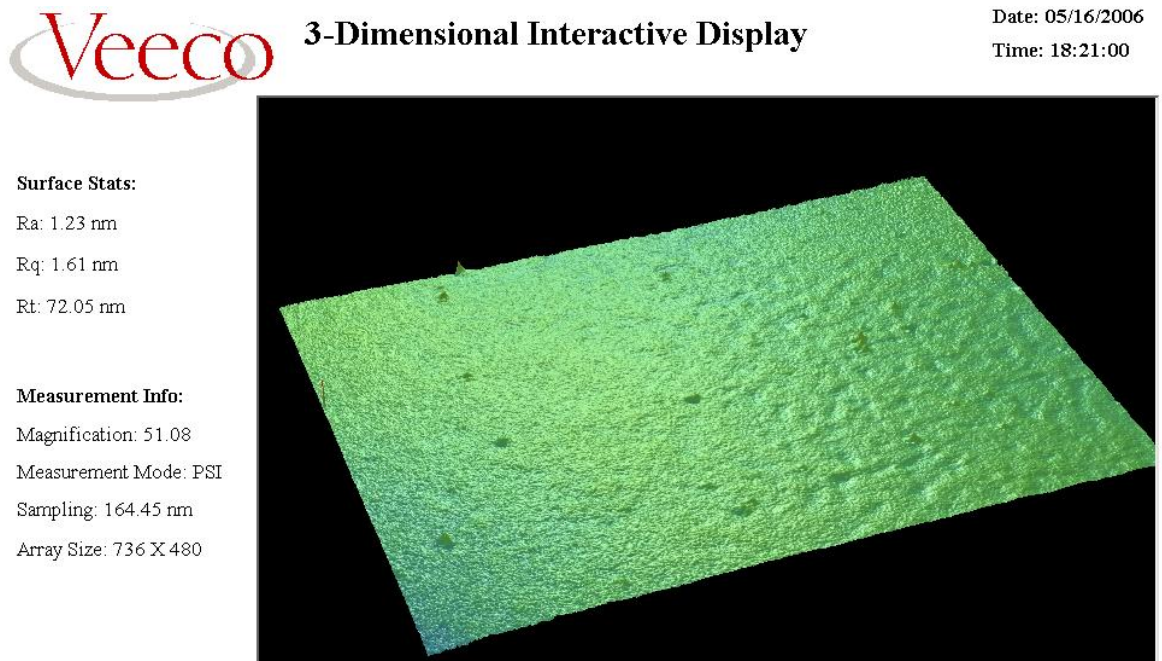


Figure 3.8: Surface profile for the 1800Å thick Nitride layer PECVD deposited at 250°C.

The footprint of each switch fabricated is about $0.6 \times 0.4 \text{ mm}^2$. A SEM picture of the released capacitive MEMS switch with deflected beams is shown in Figure 3.9. In the ‘on’ state, the built-in intrinsic stresses due to the bilayer warp the switch upwards away from the FGC line providing a large separation distance and therefore a very small ‘on’ state capacitance. The fabricated beams depicted in Figure 3.9 warp up to approximately up to a 35° angle from the switch’s surface plane when depositing a 150Å thick Cr layer.

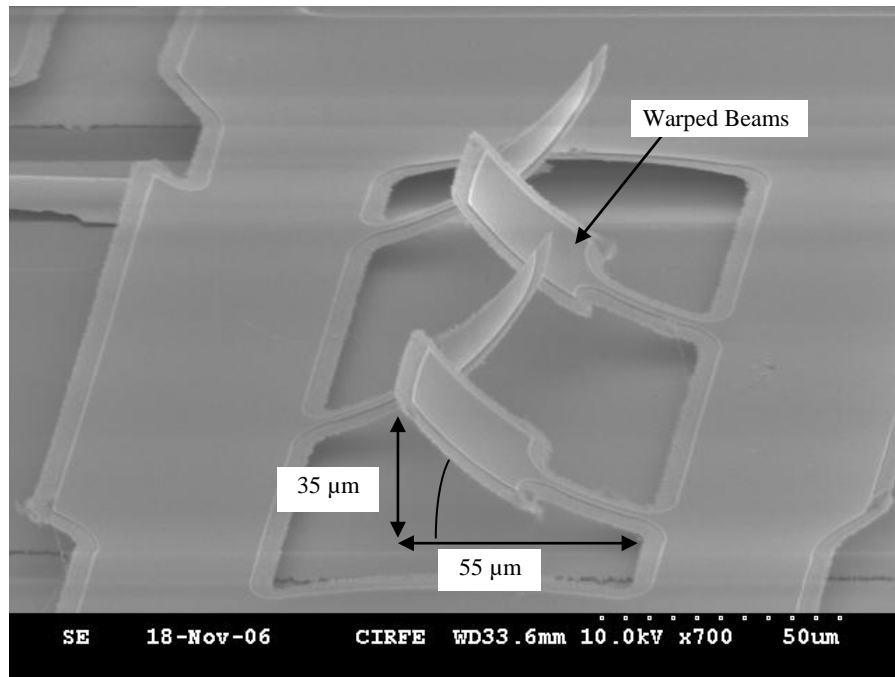


Figure 3.9: SEM of Switch 3 with center warped bimetallic beams. These center beams warp up to approximately a 35° angle from the switch's surface plane when depositing a 150Å thick Cr layer.

Several metals and dielectrics as well as film deposition methods are considered to achieve the bimorph structure; however, e-beam deposited Cr is the most compatible with the 5-mask fabrication process. A reasonable median is required to achieve the right amount of warping in the beams. Figure 3.10(a) shows the beams with only e-beam deposited Au as a structural layer. Figure 3.10(b) and Figure 3.10(c) show the MEMS switches with a 150Å and 400Å thick Cr layer on top of the Au respectively. The 400Å thick Cr layer results in warping the switch structure as well as the beams, an undesirable effect that may influence the switch's ability to come down flat in contact with the electrode. The nominal thickness with a reasonable amount of warping without drastically influencing the switch's performance is achieved with a Cr thickness of 90 - 150Å.

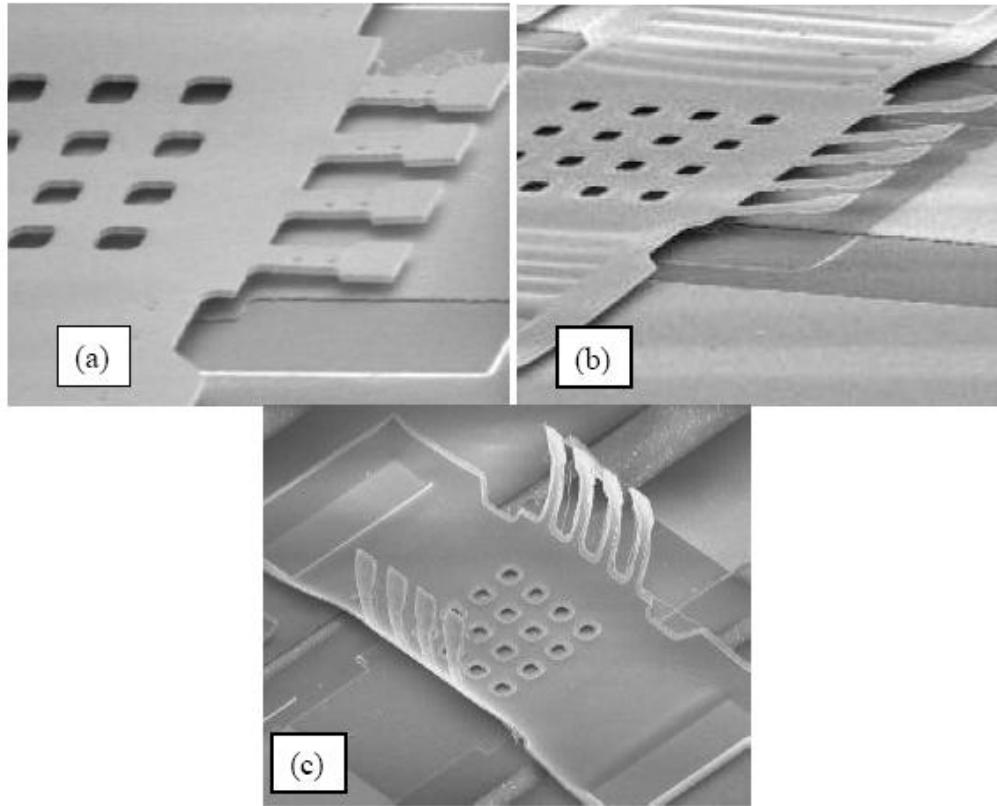


Figure 3.10: SEM photos of the different degrees of beam curling as a function of metal thickness and effective residual stress. (a) E-beam deposited gold results in flat beam structures. (b) 150Å thick Cr results in a reasonable amount of warping. (c) 400Å thick Cr results in warping the switch structure.

Figure 3.11 clearly shows the Au - Cr layers used to produce the bimorph structures. The release holes are set to a diameter of 10µm determined and limited by fabrication and resolution tolerances, and are a critical requirement for the switch's release. The perforation pattern is characterized by the ligament efficiency μ , defined as the ratio of the remaining link width, l , and the pattern pitch. In this case, the ligament efficiency is set to 67%. The holes release some of the residual stress in the beam making the materials effectively orthotropic and results in a more populated elasticity matrix [31].

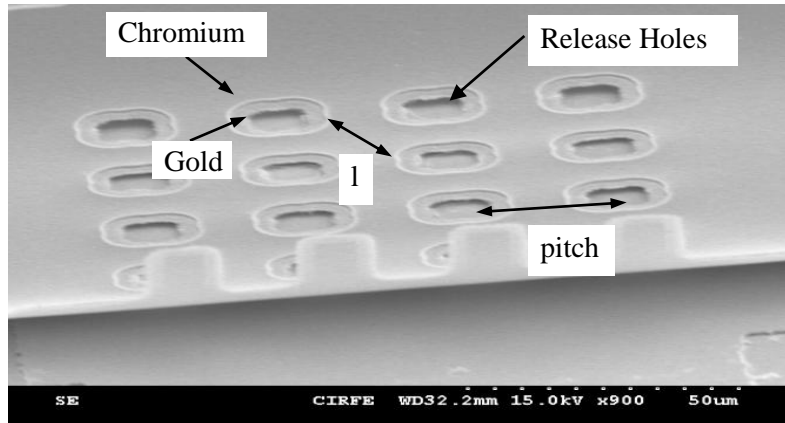


Figure 3.11: SEM of the fabricated capacitive MEMS switch with bi-layer of Au – Cr.

The MEMS switch is biased using an external DC probe. A $30\mu\text{m}$ wide high resistance Cr line 200\AA thick is routed to the switch's electrode, as shown in Figure 3.12, providing enough RF isolation for the RF signal line. This bias line is isolated from the ground plane to which the switch beam is anchored using a dielectric layer. The sheet resistance of chromium is $64\Omega/\text{sq}$.

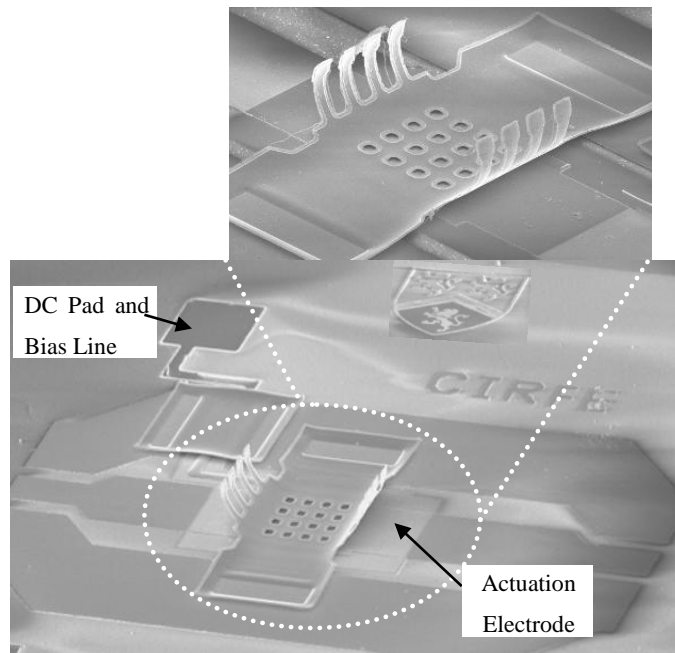


Figure 3.12: A SEM of the capacitive MEMS Switch 2 using 400\AA of Cr as a top layer. A $30\mu\text{m}$ thick high resistivity Cr line is routed to the switch electrode in order to isolate the RF signal and to bias the switch externally using a DC probe.

SEM pictures of the fabricated switches with various support designs are shown in Figure 3.14.

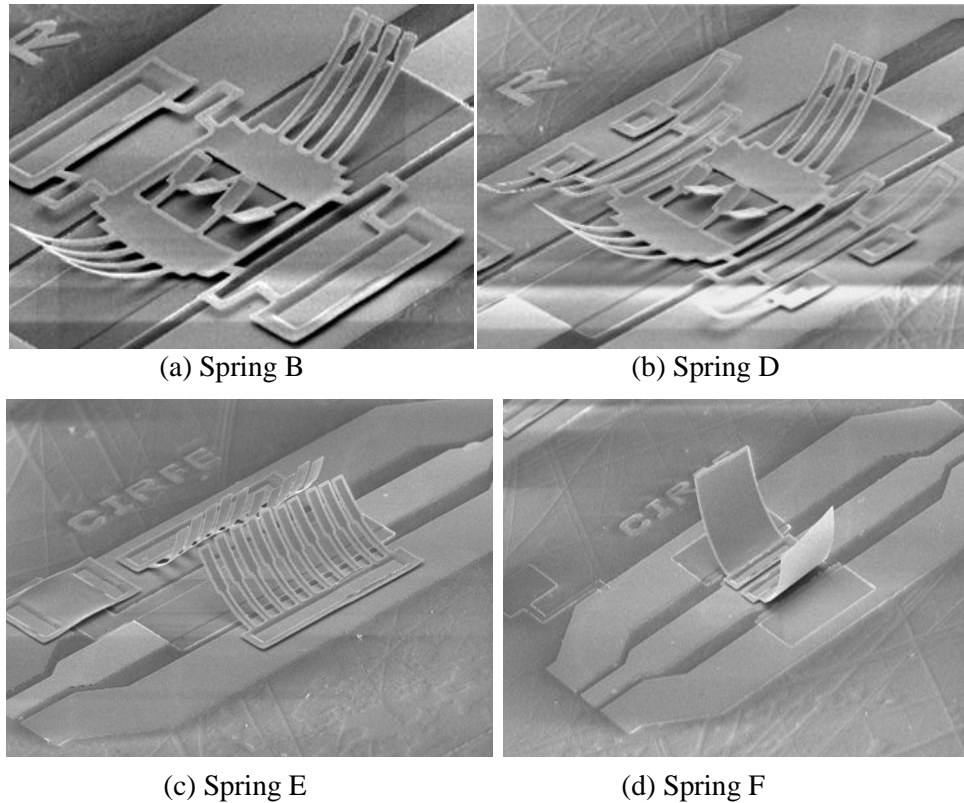


Figure 3.13: SEM photos of the fabricated bimetallic warped-beam switches. (a) Spring B, (b) Spring D, (c) Spring E and (d) Spring F.

3.1.3 Mechanical Design

Finite Element Method (FEM) simulations were performed using CoventorWare's [32] coupled electro-mechanical solver to determine the pull-in voltages of switches 1 to 4. The mechanical and electrical properties of gold required for coupled electro-mechanical solver set up are listed in Table 3.3, and the switch dimensions were obtained from Table 3.2.

Table 3.3: Material variables and their respective values.

Variable	Description	Value	Dimension
E	Au Young's Modulus	80	GPa
ρ	Mass Density	1.93×10^{-14}	$\text{Kg}/\mu\text{m}^3$
ν	Au Poisson's ratio	0.44	none
t	Au layer thickness	1.25	μm
σ_c	Conductivity	4.4×10^{13}	$\text{pS}/\mu\text{m}$
g_0	Initial Gap Height	2.6	μm

Introducing warped beams into the border of the switch slightly varies the actuation voltage. Figure 3.14 illustrates the pull-in voltage simulations of the four switches. A variation of 10V between the different switch geometries can be a result of the altered overlapping area and hence the switch's capacitance.

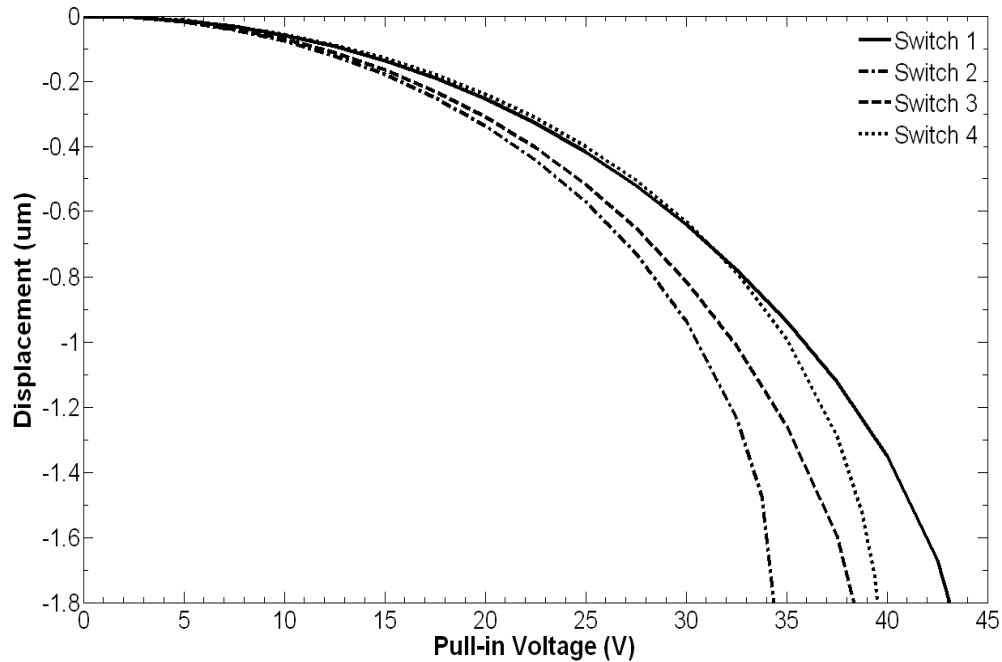


Figure 3.14: Comparison of the simulated pull-in voltages of Switches 1 to 4.

This can be explained by examining the relationship between the pull-in voltage and switch capacitance given by Equation (3.2);

$$V_p = g \sqrt{\frac{8k}{27C}} \quad (3.2)$$

where g is the switch bridge's height above the driving electrode, k is the bridge's spring constant and C is the overlapping capacitance present between the beam and driving electrode. If the capacitance is increased by 40% as a result of including 30 μ m long warped beams to the border of the switch, the voltage is expected to decrease by approximately 15% from the original 43V to 34.5V, close to the simulated results. The slight variation between the predicted and simulated changes in pull-in voltage can be due to the 10 μ m spacing between the dual warped beams that are not taken into account in the calculations. All four switches have pull-in voltages close to 40V. These simulations however did not take into account the intrinsic stress due to plating and the presence of the thin layer of Cr. Actual pull-in voltages ranged between 45V to 65V. These discrepancies can also be attributed to fabrication tolerances and variations.

The mechanical design of an electrostatic switch is primarily focused on the required DC actuation voltage and the deflection. These quantities are calculated by treating the MEMS switch as a mechanical spring. For parallel plate electrostatic actuation, when the gap reduces to 2/3 of the original gap, the beam becomes unstable and experiences a 'pull-in' effect, and collapses down on top of the thin insulating dielectric layer. The equation used to calculate the pull-in voltage of a fixed-fixed beam is given in Equation (3.3):

$$V_p = \sqrt{\frac{8K_z g_0^3}{27\epsilon_0 A}} \quad (3.3)$$

where K_z is the bridge's equivalent spring constant, g_0 is the gap between the switch and the actuation electrode, and A is the overlapping electrode area where the electrostatic force is applied. When designing switches with low actuation voltage, the choice of the membrane material and of the support design is critical. In order to lower the pull-in voltage of the structure, three different methods can be used [33]:-

- (1) increasing the area of the membrane or electrode
- (2) reducing the gap between the switch and driving electrode
- (3) designing a structure with a low spring constant.

In this design, both methods (1) and (3) are used to reduce the actuation voltage. For the second approach, the isolation associated with the RF signal restricts the value of the gap. For a given material, the spring constant of the membrane is reduced by using meander shaped supports for air-bridge structures. When designing for low actuation voltage and high isolation, choice of the membrane material and support design is critical. The effective spring constant, K_{eff} , for the entire MEMS switch can be determined by combining the simple spring equations in a fashion similar to capacitors. That is, springs in parallel add directly and springs in series add as the inverse of the sum of the reciprocals [34]. Table 3.4 lists the different supporting spring designs considered and their associated dimensions and estimated spring constant.

Table 3.4: Simulated switch pull-in voltages and spring constants.

Switch	Pull-In Voltage (V)	Spring Constant (N/m)
Original	42.5	69.3
A	6	1.6
B	22	22
C	12	6.4
D	24	25.76

The calculated pull-in voltage and spring constant of the final optimum design chosen, Switch C, are 12V and 6.4N/m, respectively. There is a discrepancy between the measured and simulated results. The actuation voltage of Switch C is measured at 27V, 2.25 times higher than the theoretical values, comparable to the values observed in [40] reported for a guided-end cantilever type switch with simultaneous axial tension and concentrated transverse loading. Therefore, it is predicted that our measured discrepancies should indeed be mainly due to intrinsic stress induced during fabrication and are not accounted for in the theoretical values.

The existence of a residual stress in the normal plane of a fixed-fixed beam or cantilever beam is an inevitable consequence of thin film deposition. These stresses are present due to a gradient in the material properties through the structure's thickness; in this case the sputtered seed gold layer followed by the electroplated gold layer, and due to the deposition of a different material, in this case the thin layer of Cr on top of the gold. Several studies have been performed to theoretically explain the mechanism of these stresses [35 - 37] and to experimentally measure their effects [38, 39]. Thin-film stress characterization is complicated and highly depends on the fabrication process parameters and specifics. Using the same approach presented in [36], the effective stress of the bimetallic layers is roughly approximated with the use of test cantilever beams and clamped-clamped bridges. Captured images of Switch 2 as well as some of the test structures used to characterize and extract the stress information using an optical profilometer are shown in Figure 3.15.

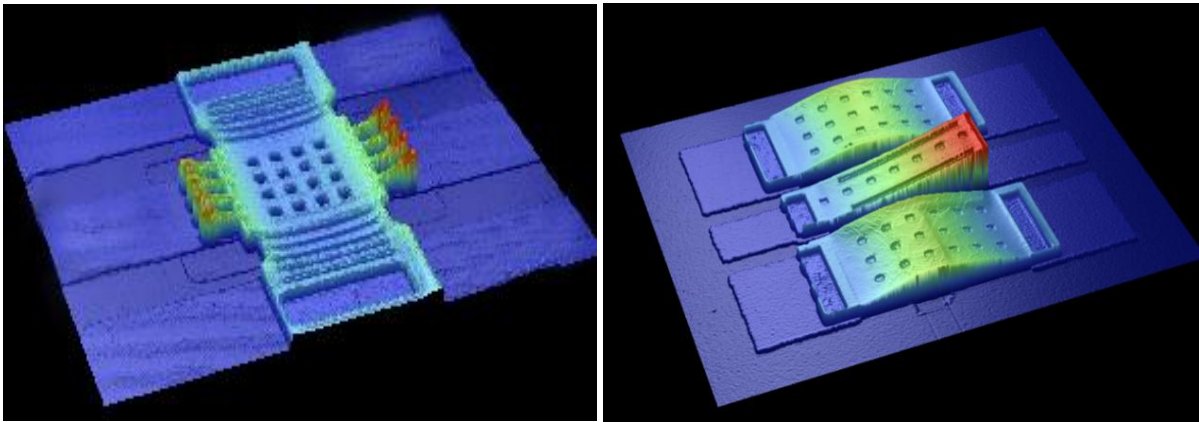


Figure 3.15: Optical profilometer captured image of the Switch 2 and the some of the cantilever and fixed-fixed beam structures used to measure deflection and curvature.

The general uniaxial residual stress field in a thin film can be represented as [33]:

$$\sigma_x = \sum_{k=0}^{\infty} \sigma_k \left(\frac{y}{h/2} \right)^k \quad (3.4)$$

where h is the film thickness and $y \in (-h/2, h/2)$ is the coordinate across the film thickness, with its

origin at the mid-plane of the film. For a first order approximation, the total stress can be calculated as:

$$\sigma_{total} = \sigma_0 + \sigma_1 \left(\frac{2y}{h} \right) \quad (3.5)$$

Equation (3.5) implies that the total stress can be expressed as a superposition of the constant in-plane mean residual stress σ_0 (negative since the film is in tension) and a gradient stress about the mid-plane. The residual gradient stress causes out-of-plane deformation for cantilever beams. The photoresist AZ3330 sacrificial layer and sputtered gold (2000Å) seed layer contribute to such a stress. The switches are then electroplated in a gold plating solution (Techni-gold solution by Technic Inc) with a steady current density of 2mA/cm² for approximately 35 minutes, followed by the electron beam deposition of a very thin Cr layer. Each deposited layer is characterized using the measured deflection, Δz , and radius of curvature, ρ , obtained from the optical profilometer profiles of the cantilever beams and fixed-fixed beams. The stress gradient due to bending is extracted using the equations obtained from [11] for a deflected cantilever and the critical buckling stress for a fixed-fixed beam given by Equation (3.6) and Equation (3.7), respectively.

$$\Delta\sigma = \frac{(\Delta z)4tE_e}{3L^2 \left(\frac{1-(t_2-t_1)}{t^2} \right)} \quad \text{Cantilever} \quad (3.6)$$

$$\Delta\sigma = \frac{E_e t}{2(1-\nu)\rho} \quad \text{Fixed-fixed Beam} \quad (3.7)$$

where z is the amount of vertical tip deflection, E_e is the effective Young's modulus, t is the film thickness, ρ is the radius of curvature of the cantilever beam and L is the beam length. Initially, the gradient stress values from the multilayer cantilever beams were calculated using Equation (3.6). Since the gradient stress has been found insufficient to generate large deflections of the fixed-fixed beam, total stress is first measured and the gradient stress values obtained from the cantilever beams are de-coupled from the total stress values, in order to obtain the in-plane residual stress values. Stress measurements for the seed gold layer and electroplated gold layer were provided by Frederic Domingue and King Yuk Chan from CIRFE labs. The measured approximated residual in-plane stresses for each of the layers in the switch structure are listed in Table 3.5.

Table 3.5: Measured residual in-plane stress for the switch's structural layers.

Layer Material	Measured Stress (MPa)	Thickness (μm)
Sputtered Au	98.1	1
Electroplated Au	109.1	0.2
E-beam deposited Cr	1758	0.015

It is experimentally found that the effective residual in-plane tensile stress of the three layers is on the order of 120MPa. This explains the discrepancy between simulated and measured pull-in voltages. This residual stress has a considerable effect on the pull-in voltages of the switch, where a residual tensile stress of 150MPa can increase the switch's pull-in voltage by a magnitude of three times [40]. More thorough mechanical analysis is required in order to determine how each of the stresses influences the pull-in voltage and 'on' state capacitance values.

3.1.4 Results

HFSS™ software [41] is used to simulate the RF performance of the proposed designs. A comparison of the simulated and measured results is presented in this section. The substrate thickness is set to 254 μm with microwave properties $\epsilon_r = 9.9$ and a loss tangent of 0.001. The FGC waveguide line is set to a thickness of 1.2 μm to account for gold conductor losses. The radiation box with outer edges excluding the wave port surfaces are all set to perfect conductor radiation properties and to 2000 μm in height. The solution method used is the driven modal solution with a center frequency set to 10.5GHz for an X-Band range of frequencies (8-12GHz).

The switches are all first simulated in "on" state with a gap height of 2.6 μm above the dielectric. In this case, the target optimum behaviour is a very small S_{11} value ($S_{11} < -20\text{dB}$), low insertion loss ($S_{21} < -1\text{dB}$) and a very small upstate capacitance (~10-60fF). In the 'on' state, the switch ideally allows the signal through with a minimal amount of reflections. In 'off' state, the switch ideally presents a large capacitance (4-9pF) and target optimum behaviour is a very small value of S_{21} ($S_{21} < -25\text{dB}$) for high isolation. The capacitance values in the 'on' state and 'off' state

are determined from the switch's reflection coefficient and insertion loss, respectively. They can be calculated using Equation (3.8) and Equation (3.9).

$$|S_{11}|^2 \cong \frac{\omega^2 C_{on}^2 Z_0^2}{4} \quad \text{'on' state capacitance} \quad (3.8)$$

$$|S_{21}|^2 \cong \frac{4}{\omega^2 C_{off}^2 Z_0^2} \quad \text{'off' state capacitance} \quad (3.9)$$

Switch 2 shows a notable improvement in its 'off' state isolation performance due to the presence of the external beams added to the structure's border, thereby resulting in increased effective 'off' state capacitance. HFSS simulation results illustrated in Figure 3.16 predicts an 'off' state capacitance of 9.12pF at 10GHz, two times the 'off' state capacitance of the basic switch, Switch 1. The switch's insertion loss is less than 0.1dB for X-band frequencies.

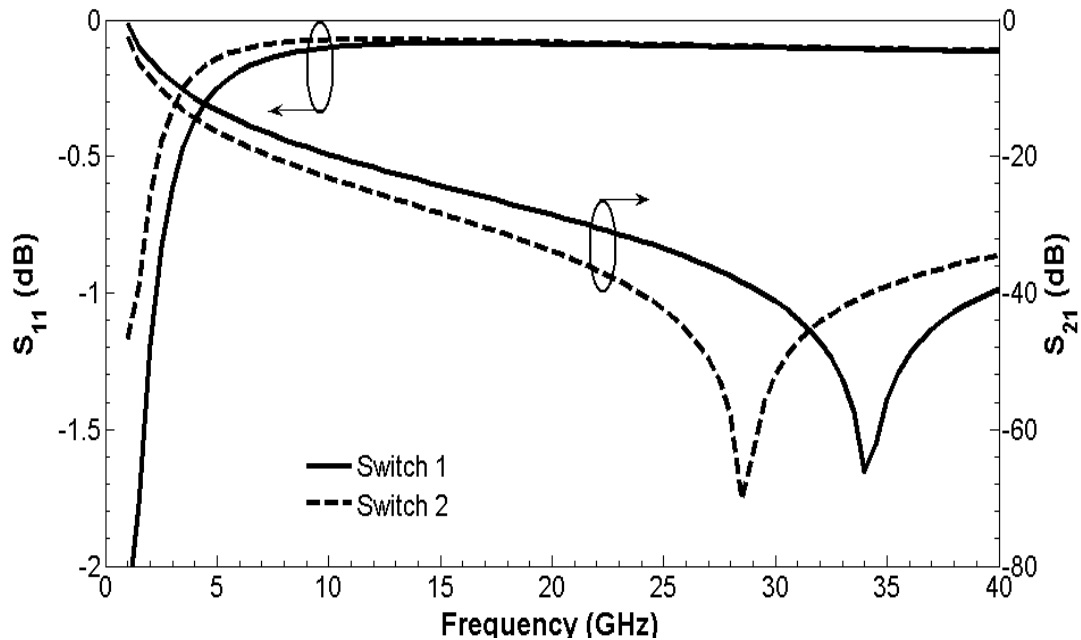


Figure 3.16: Comparison of the simulated responses of Switch 1 and Switch 2 in 'off' state. An 'off' state capacitance of 9.12pF at 10GHz is measured; two times the 'off' state capacitance of the basic switch, Switch 1.

The presence of these beams on the border of the switch has a small contribution to the ‘on’ state capacitance. To compensate for this, Switch 3 with warped beams at its center is modeled and simulated. This switch exhibits an improved return loss of better than 20dB at 10GHz, as shown in Figure 3.17. The presence of these warped beams reduces the ‘on’ state capacitance by 20% to 63.6fF at 10GHz due to the reduced overlapping area between the switch structure and driving electrode, resulting in a smaller effective capacitance when the switch is in its ‘on’ state.

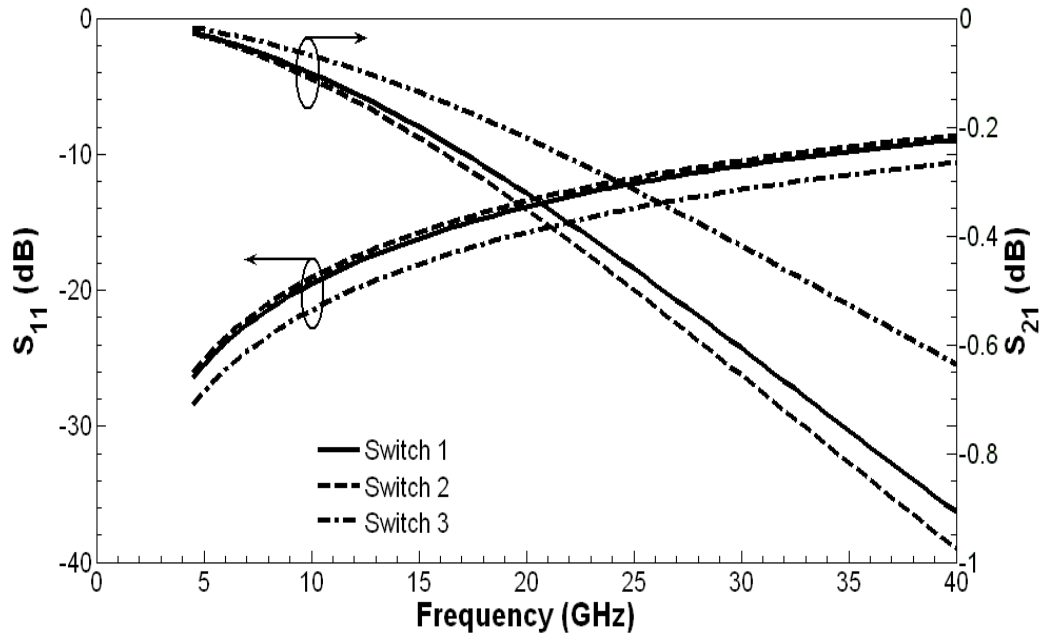


Figure 3.17: Comparison of the simulated responses of Switch 1, Switch 2 and Switch 3 in ‘on’ state. The presence of these warped beams reduces the ‘on’ state capacitance by 20% to 63.6fF at 10GHz

The circuit is modeled using HP ADS[®] [42]. The model shown in Figure 3.18 consists of two sections of physical transmission line to represent the input and output sections of the FGC line and a capacitor-inductor-resistor series combination shunted across the transmission line to represent the MEMS switch. In this approach, the line impedance Z_0 , line length l , and effective dielectric constant ϵ_{eff} , are determined from the physical dimensions of the FGC line. The switch capacitances on, C_{on} and off, C_{off} , inductance L_s , and series resistance R_s are all varied to fit the model to the measured data. The attenuation in the physical transmission line model is specified at 10GHz and then follows a \sqrt{f} variation.

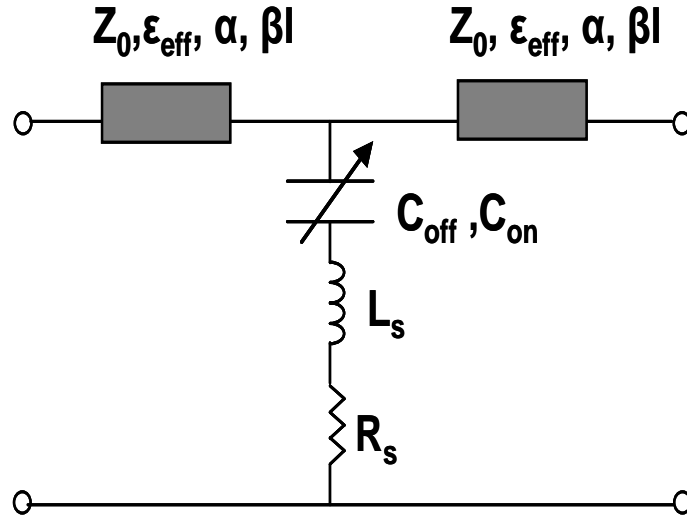
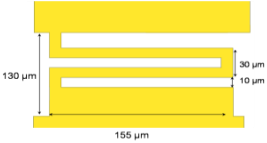
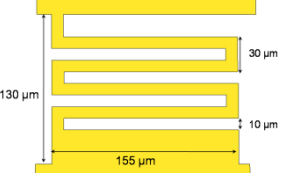
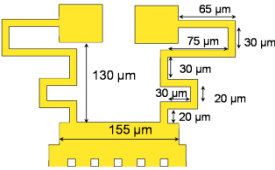
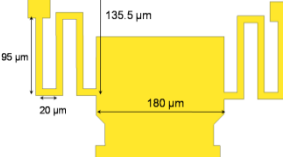
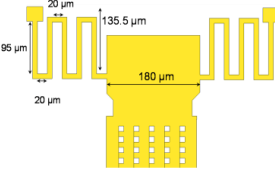


Figure 3.18: Equivalent circuit model used to extract the switch's on and off capacitances, C_{on} and C_{off} , series inductance L_s and series resistance R_s parameters.

The simulated responses obtained were fitted to a C-L-R (Capacitance-Inductance-Resistance) circuit and the extracted capacitance, inductance and resistance at the resonance frequency in the 'off' state are listed in Table 3.6 for the various spring designs included in the basic Switch 1 model.

Table 3.6: Fitted simulated parameters using the equivalent CLR model.

Connecting Beam	Resonant Frequency (GHz)	Inductance (pH)	Resistance (Ω)	'Off' State Capacitance (pF)
	13.8	35	0.48	3.8
	5.8	70	0.6	10.8
	23	5	0.03	9.3
	11	23	0.3	9.1
	8.43	39.7	0.4	8.9

A two-port on-wafer measurement of the MEMS switches is performed from 5GHz to 40GHz using an HP8722ES vector network analyzer. S-parameter measurements are de-embedded to remove any parasitic effects and losses of the RF probes and FGC waveguide lines, and are referenced to 20 μ m from either side of the MEMS bridge. The capacitance values are extracted by fitting an equivalent series C-L-R circuit to the measured S parameters. The measured test results of Switch 2 shown in Figure 3.19 in ‘off’ state show great improvement in S_{21} and S_{11} over the basic switch, Switch 1. The ‘off’ state capacitance improves from 4.25pF to 10pF, with a capacitance ratio of 89. Isolation measurements are shown with the fabricated switches pulled to downstate with 45 - 60V. Among the many samples fabricated and tested variations less than 10% from the average value are observed, ensuring that the switch pull-in voltages can be relatively repeatable with the 5-mask fabrication process used.

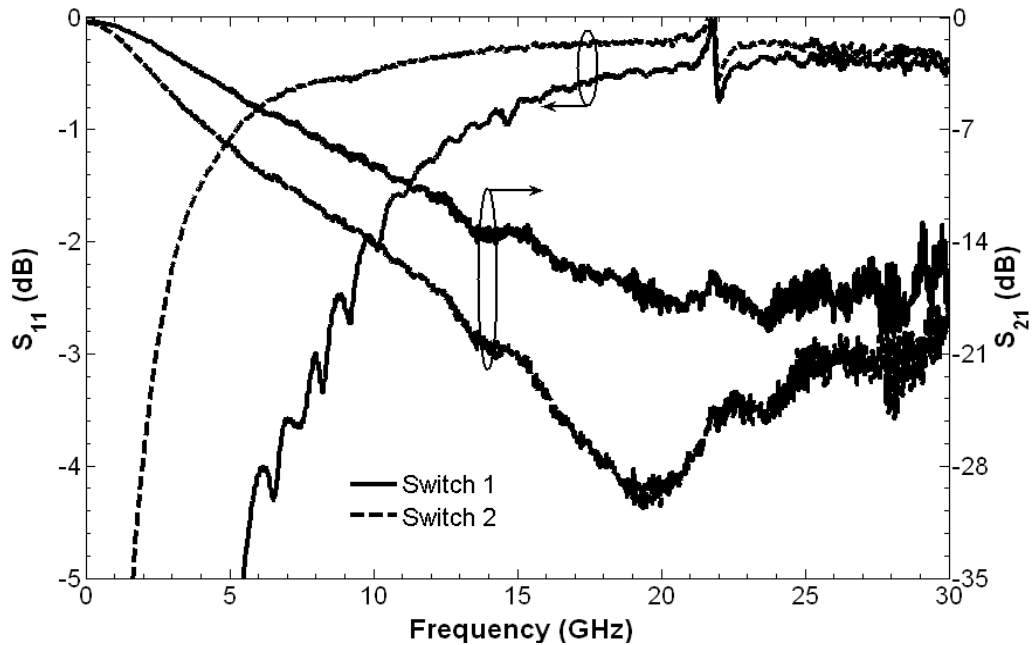


Figure 3.19: Comparison of the measured responses of Switch 1 and Switch 2 in ‘off’ state. The ‘off’ state capacitance improves from 4.25pF to 10pF.

Figure 3.20 shows the measured response of Switch 3 compared to that of the traditional switch, Switch 1. Return loss in the ‘on’ state is enhanced to better than 20dB at 10GHz. The measured ‘on’ state capacitance decreases from 121fF to 59.5fF, half the original ‘on’ state

capacitance. The performance of Switch 3 with its center warped beams does not differ significantly from that of Switch 1 in ‘off’ state, with an ‘off’ state capacitance of 3.92pF, comparable to that of Switch 1 at 4.25pF. Discrepancies found between the measured and simulated results can be attributed to several sources. Metallic loss, release holes, wet etch undercut, dielectric roughness and fabrication tolerances such as residual stress all contribute to these differences and are not considered in the EM simulation.

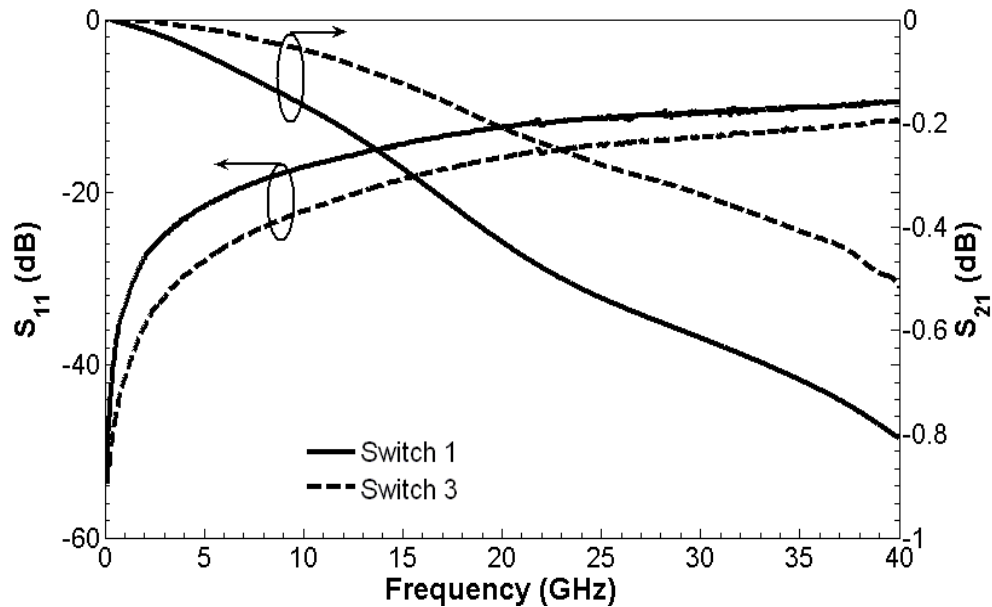


Figure 3.20: Comparison of the measured response of Switch 3 and Switch 1 in ‘on’ state. The measured up-state capacitance decreases from 121fF to 59.5fF, half the original ‘on’ state capacitance.

The ‘off’ state capacitance and ‘on’ state capacitance can therefore be simultaneously enhanced by fully implementing the warped beam concept. This gives an off-to-on capacitive ratio of 170 for the dual-warped switch without the use of a thinner dielectric or a high dielectric constant material. However, by adding these beams to the center of the switch, a resonance is introduced that allows current to pass through the switch at a specific frequency in the ‘off’ state. To compensate for this, Switch 2 with warped beams at its center is modeled and simulated, exhibiting an improved return loss of better than 20dB at 10GHz, as reported in [30]. However, in ‘off’ state, the presence of these center-warped beams results in a resonance at 20GHz.

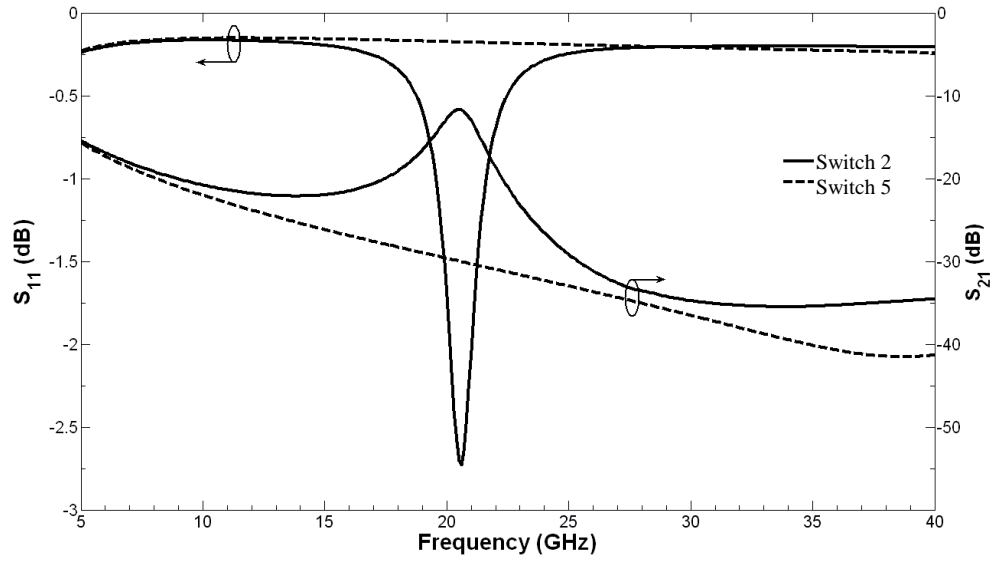
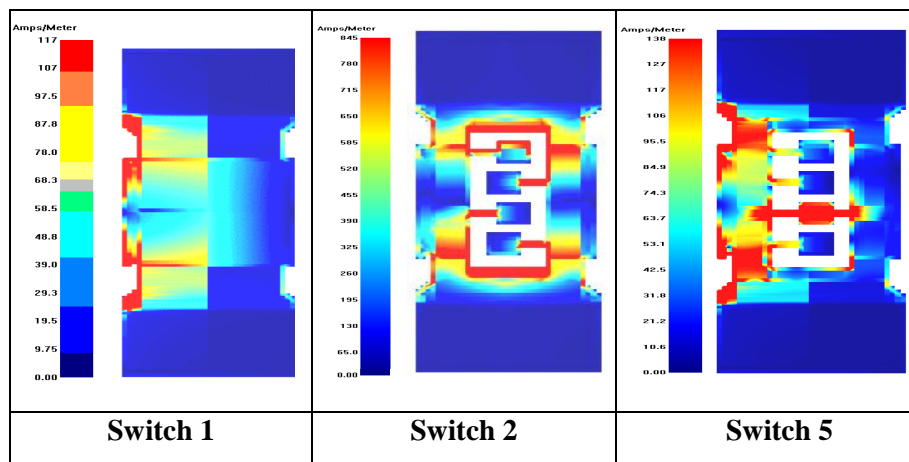


Figure 3.21: Comparison of the simulated responses of Switch 2 and Switch 5 in ‘off’ state. The presence of these center-warped beams results in a resonance at 20GHz.

After modeling several designs, the current can be redirected by connecting one of the center beams straight across the switch structure, thereby eliminating the resonance as shown in Figure 3.21. The occurrence of this resonance can be better understood by examining the normalized current distribution along the surface of the switch in the ‘off’ state at 20GHz, as shown in Table 3.7.

Table 3.7: Normalized current distribution along the surface of Switches 1, 2 and 5 in ‘off’ state at 20GHz.



In the traditional Switch 1, the signal is shorted when the bridge is pulled down, and therefore the current is dramatically reduced at the right hand side of the switch and mostly localized along the sides of the coplanar slots on the switch's left side. The current is concentrated on one edge of the MEMS bridge since this edge presents a short circuit to the incoming wave. For the center warped-beam Switch 2, the signal appears to couple across the beams and passes through at 20GHz. After several iterations, it was found that by connecting the center beam as shown in Switch 5, the signal is given a high inductance path to redirect it back to the left hand side of the switch without greatly influencing the RF performance of the switch. The equivalent circuit of Switch 2 is shown in Figure 3.22 and appears as two smaller capacitive switches in parallel with a inductances and coupling capacitances present between the warped bimetallic beams.

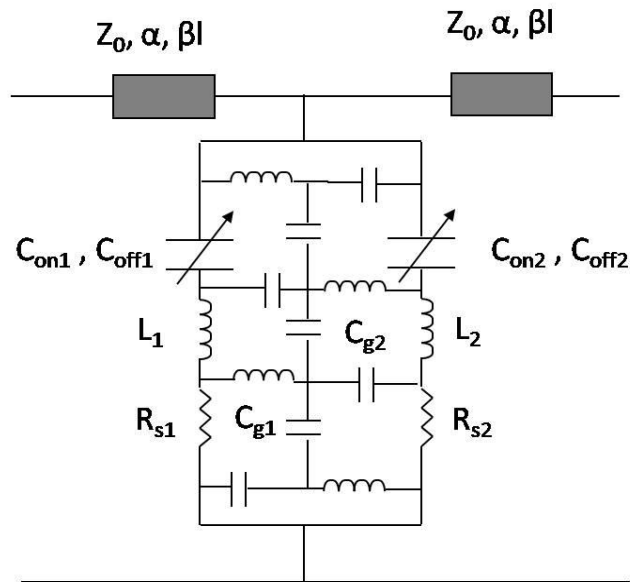


Figure 3.22: The equivalent CLR circuit of the center warped-beam Switch 2.

The capacitance and inductance values are extracted by fitting an equivalent series C-L-R circuit to the measured S parameters. The model consists of the characteristic impedance, Z_0 , of the input and output sections of the FGC waveguide transmission line, the series resistors, R_{s1} and R_{s2} , of the switch beam, the series inductors, L_1 and L_2 , switch shunt capacitances, C_1 and C_2 (in both states), and inductances to represent the step change in the warped-beam width, and finally the coupling capacitors, C_g present between the warped beams. The switch inductances, capacitances and series resistances are varied and optimized to fit the model's response to the measured S-parameters using

HP ADS. Figure 3.23 shows the measured results and equivalent C-L-R circuit simulated response of Switch 2, in the ‘off’ state. There is a fairly good agreement between those results. Any discrepancies present can be a result of fabrication tolerances and switch conformity with the electrode when actuated to ‘off’ state.

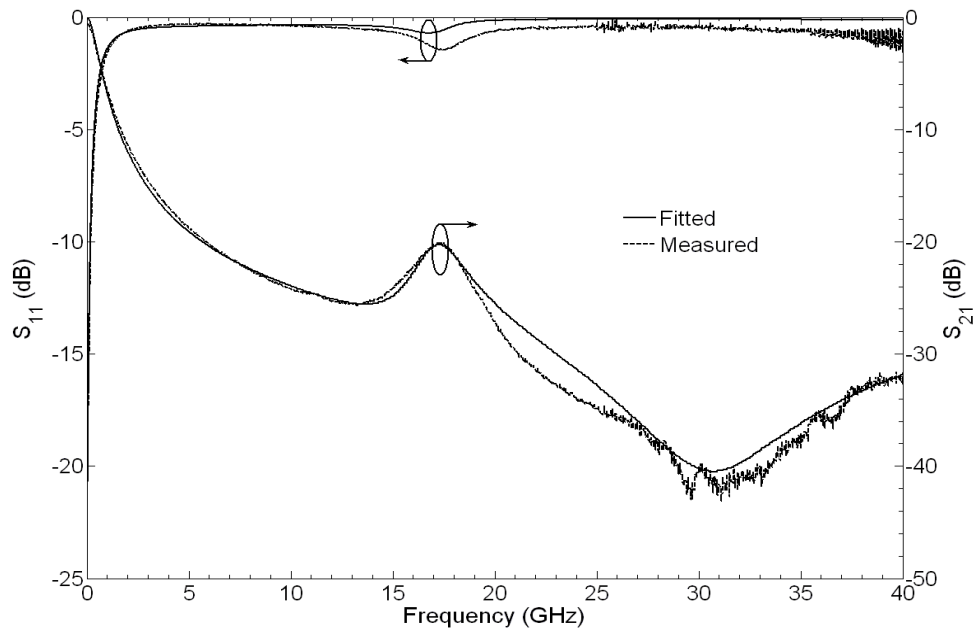


Figure 3.23: A comparison between the measured response and the equivalent CLR circuit simulated ADS response of Switch 2 in ‘off’ state. Any discrepancies present can be a result of fabrication tolerances and switch conformity with the electrode.

There is a capacitance present that couples between the warped beams. This capacitance behaves as band pass filter allowing the signal to couple through at 20GHz. By connecting one of the center beams straight across the switch, the current can be routed back to the ground line, and effectively sees a whole capacitive switch, removing the presence of a the resonance at 20GHz, as illustrated in Figure 3.21. The final design, Switch 6, is shown in Figure 3.24, with the dual-warped concept implemented, along with a center connected beam and meandered supporting springs 10 μ m wide.

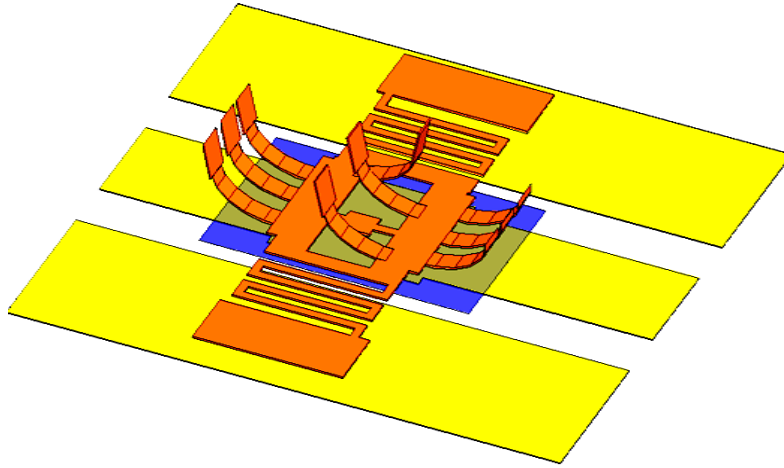


Figure 3.24: Switch 6 improved dual-warped beam switch with meandered springs and center connected beam.

Two-port on-wafer measurements of the revised and improved MEMS switches are performed from 5GHz to 40GHz using an HP8722ES series vector network analyzer. The measured test results of Switch 5 presented earlier in Table 3.7 are illustrated in Figure 3.25. The ‘off’ state performance measured closely agrees with the performance predicted by the simulated results presented in Figure 3.21. Slight discrepancies such as the location of the resonance frequency could be a result of fabrication tolerances such as gold over etch and switch conformity when actuated in ‘off’ state. Figure 3.26 shows the measured responses of Switch 3 and Switch 6 compared to that of the traditional switch, Switch 1. Return loss in the ‘on’ state is improved to better than 20 dB at 10GHz.

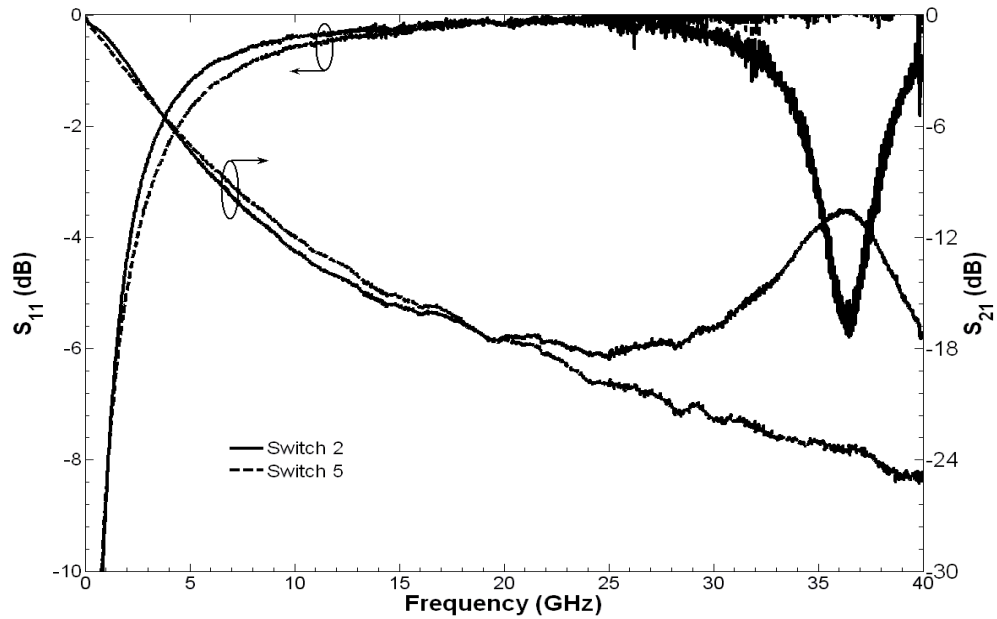


Figure 3.25: Comparison of the measured responses of Switch 2 and Switch 5 in 'off' state. Connecting the center beam across the width of the switch removes the resonance.

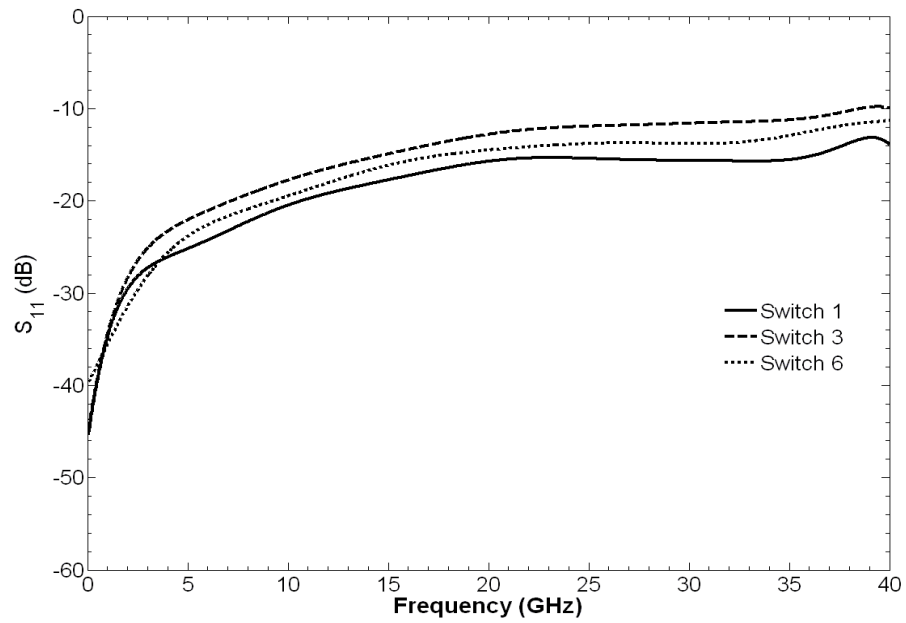


Figure 3.26: Comparison of the measured responses of Switch 1, Switch 3 and Switch 6 in 'on' state.

Shown in Figure 3.27 to Figure 3.30 are the measured results obtained for the spring design variations combined with the warped beam design approach in ‘off’ state. As mentioned earlier, a balance between the switch’s mechanical and RF performance is needed when choosing the spring design. The inductance of the supporting beams determines the location of the resonance frequency, governed by Equation (3.1).

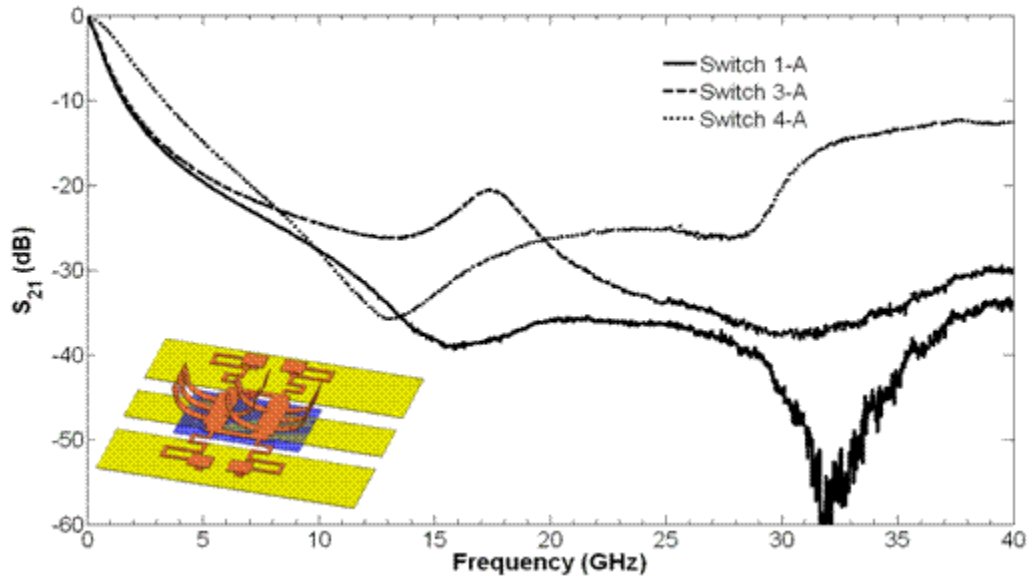


Figure 3.27: Comparison of the measured results of Switch A in ‘off’ state.

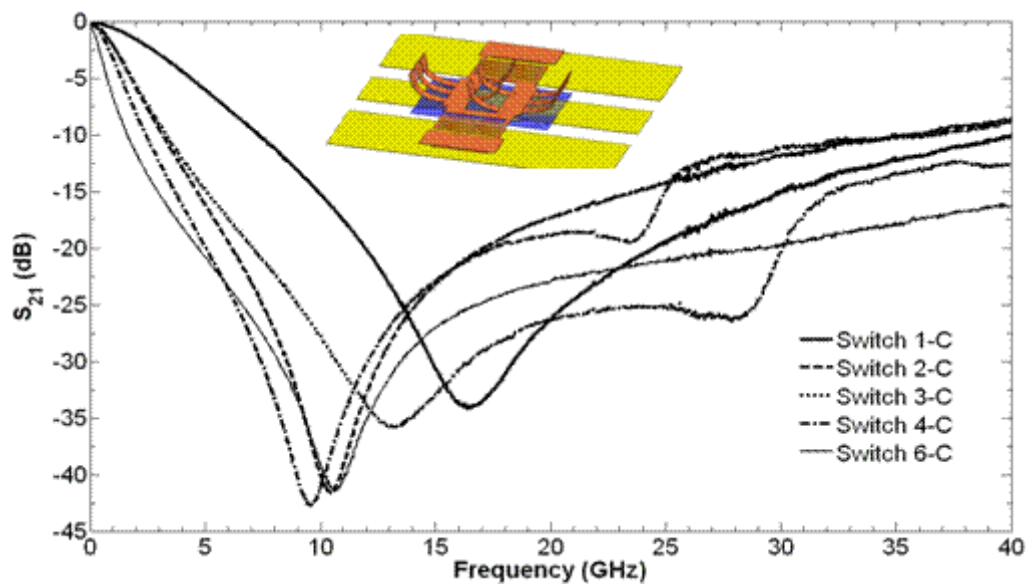


Figure 3.28: Comparison of the measured results of the 5 variations of Switch C in ‘off’ state.

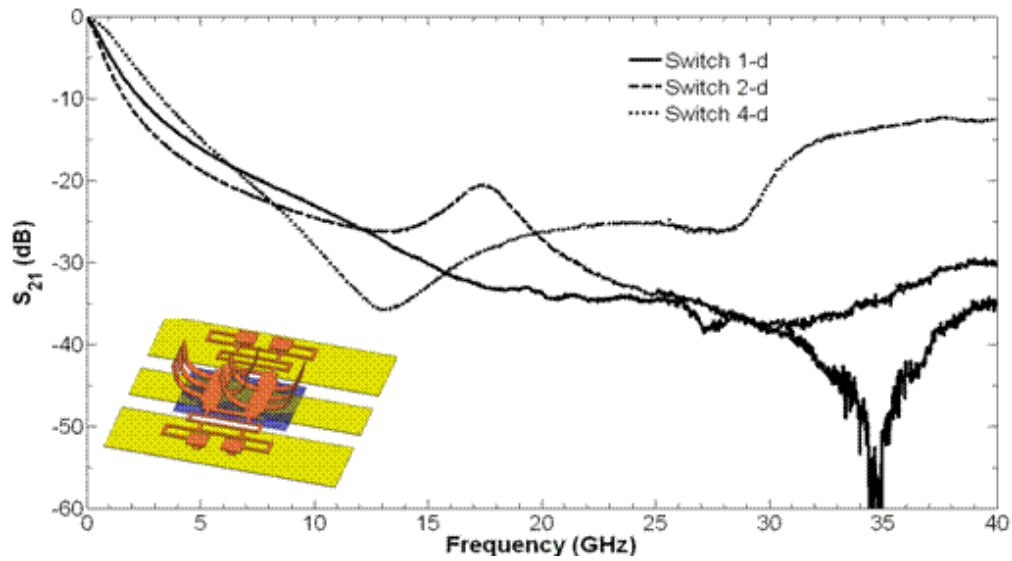


Figure 3.29: Comparison of the measured results of the 3 variations of Switch D in 'off' state.

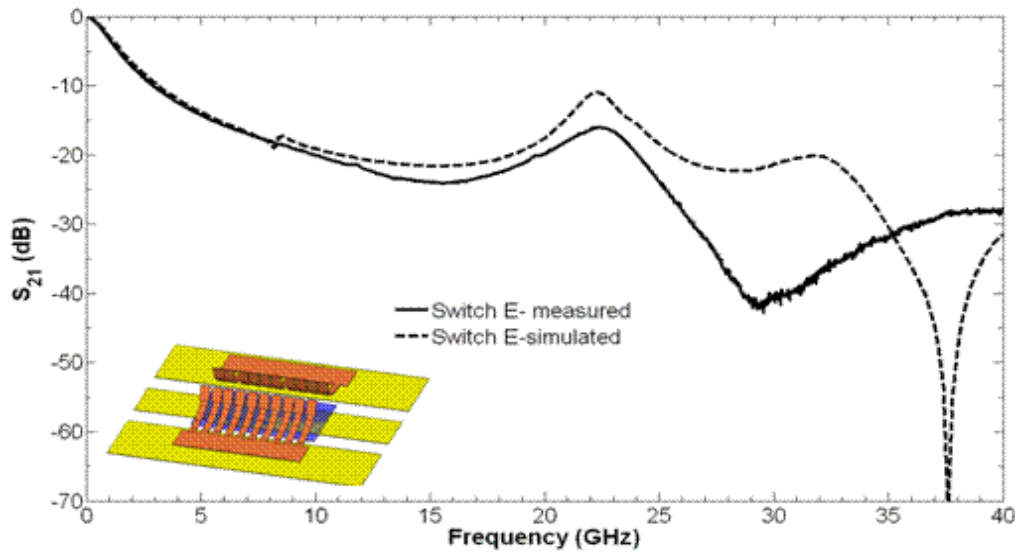


Figure 3.30: Comparison of the simulated and measured results of Switch E in 'off' state.

Results indicate that for optimum performance centered at a frequency of 10.5GHz, the spring design C in Figure 3.28 offers the best performance with a wide bandwidth and excellent isolation. Switch D's measured response is very similar to that of Switch A as expected with a slightly higher resonance frequency since it's supporting beams have a lower effective inductance than that of Switch A. Switch E results in Figure 3.30 demonstrate the flexibility of the warped beam

design, illustrating how this approach can be used to tune the performance of any switch design. Improving the switch's isolation by increasing its series inductance results in a very narrow operating bandwidth, however enhancing the switch's RF performance by manipulating its off-to-on capacitance ratio does not drastically influence the switch's bandwidth. This can be further explained by modeling the capacitive shunt switch in 'off' state as a band-stop resonator that prevents the RF signal from passing through within a specific frequency band.

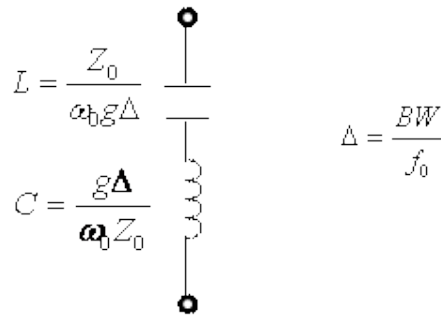


Figure 3.31: The equivalent circuit of a bandstop resonator.

Consider two switches designed at two frequencies, f_{01} and f_{02} . Shown in Table 3.8 is a comparison of the first case where the inductance of the second switch is quadrupled while maintaining the same capacitance, and the second case where the capacitance is quadrupled and the same inductance for the two switches is maintained.

Table 3.8: Comparison of switch bandwidth when varying its inductance and capacitance.

$L_2 = 4L_1$ and $C_2 = C_1$	$L_2 = L_1$ and $C_2 = 4C_1$
$\left(\frac{g}{2\pi Z_0}\right) \frac{BW_1}{f_{01}^2} = \left(\frac{g}{2\pi Z_0}\right) \frac{BW_2}{f_{02}^2}$ $\frac{BW_1}{f_{01}^2} = \frac{BW_2}{f_{02}^2}$ $\frac{BW_1}{4f_{02}^2} = \frac{BW_2}{f_{02}^2}$ $BW_1 = 4BW_2$	$\left(\frac{Z_0}{2\pi g}\right) \frac{1}{BW_1} = \left(\frac{Z_0}{2\pi g}\right) \frac{1}{BW_2}$ $BW_1 = BW_2$

Therefore, it is expected that by simultaneously tuning the series inductance L_s and the downstate capacitance C_s a wider bandwidth with good isolation is obtained for the MEMS shunt switch as is shown in the measured switch's response. A two-port on-wafer measurement of Switch 6, the final design, is performed from 5GHz to 40GHz. Figure 3.32 and Figure 3.33 summarize the measured response of Switch 6 compared to its simulated response for the 'off' state and 'on' state, respectively.

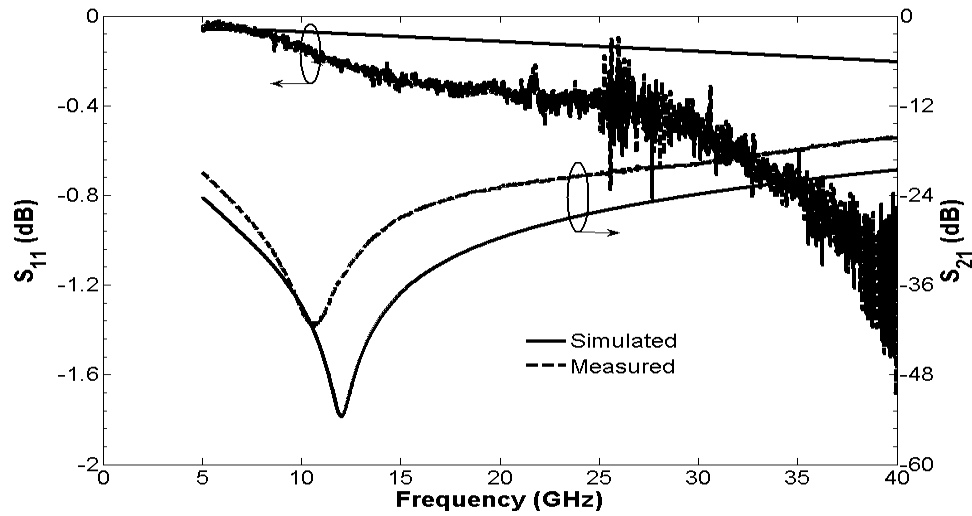


Figure 3.32: Comparison of the simulated and measured response of Switch 6 in 'off' state.

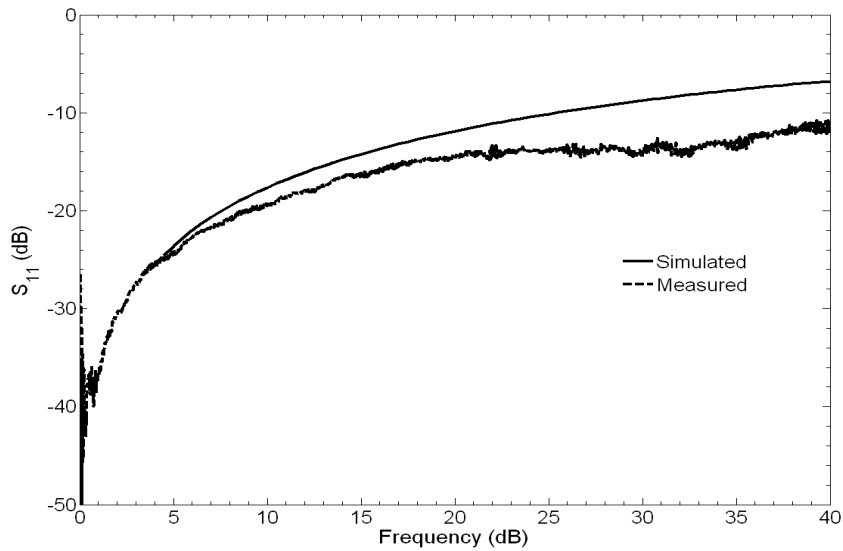


Figure 3.33: Comparison of the simulated and measured response of Switch 6 in 'on' state.

The performance of Switch 6 with its center warped beams and meandered springs results in an isolation better than 40dB at 10.5GHz and an insertion loss less than 0.2dB. Using an equivalent CLR circuit, the equivalent downstate capacitance is 10pF and a series inductance of 23pH. The actuation voltage required by the switch is reduced to 27V with the use of meandered springs. There is about a 1.5GHz shift in resonance frequency between simulations and measurement. This shift toward lower frequencies can be due to the higher capacitance value that the switch presents in ‘off’ state. Other discrepancies found between the measured and simulated results can be attributed metallic loss, wet etch undercut and fabrication tolerances such as residual stress, all which contribute to these differences and are not considered in the EM simulations.

In summary, the downstate capacitance and upstate capacitance can therefore be simultaneously enhanced by fully implementing the warped beam concept, Switch 6, as illustrated in Figure 3.24. Measured responses in ‘off’ state and ‘on’ state show enhanced ‘on’ state and ‘off’ state capacitances of 59.5fF and 10pF respectively. This gives an off-to-on capacitive ratio of 170 for the dual-warped switch without the use of a thinner dielectric or a high dielectric constant material.

3.1.5 MEMS Switch Dynamic Behavior

Fast switching speed is essential for phased array applications and is one of the design challenges and disadvantages faced when designing MEMS components. The fastest switch designed to date was by MIT Lincoln Laboratory [18] with a speed of approximately 1 μ s, primarily due to its compact size. However, the disadvantage of this switch is that it requires high voltages of up to 70 – 80V to achieve such fast speeds. Low voltage switches however tend to be slower because they typically have a larger actuation area. Low-height switches have a relatively high mechanical resonant frequency and a fast switching time [11]. The switching speed measurement setup is shown in Figure 3.34. A Continuous Wave (CW) RF input signal of 5dBm at 10.5GHz as a center frequency is applied to the switch. The biasing signal is provided by a DC power supply that outputs voltages up to 200V. One output is fed into the oscilloscope to use as a reference signal and the second output is fed into the biasing switching circuit. The biasing switching circuit uses a transistor connected to the DC power voltage supply to switch high voltage square waveforms to the switch’s input. For the measurement, a HP 33220 function generator is used to generate a square wave of 5volts. The DC

bias is applied to the switch through an external high resistivity Cr line routed to the driving electrode. The switches are probed using a Cascade probe station where the output RF probe is connected to a HP 420A n-type crystal detector. The crystal detector provides a DC voltage proportional to the modulated RF envelope and captures the switching behavior of the device under test, which is then viewed on the oscilloscope. The frequency of the RF signal is limited and determined by the operating frequency band of the detector. The crystal detector modulates the RF power recorded from the switch's output, providing a DC voltage output that can be measured on an oscilloscope and in this case is selected over X-band.

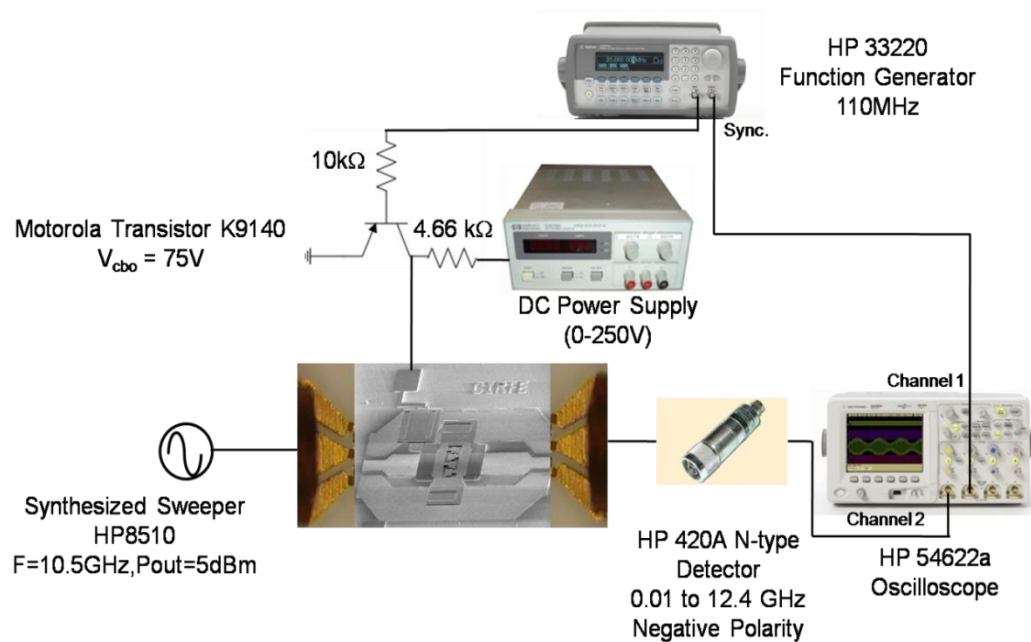


Figure 3.34: Switch speed measurement setup.

The switching time of the switch is primarily determined by the squeeze film damping when the switch is actuated, and limited by the time it takes the membrane to release itself from the dielectric layer. In the DC testing of Switch 6, a driving voltage of 25-30V is required to achieve a 2.6 μ m in-plane displacement. Figure 3.35 plots the rising-edge response time and the falling edge response time. A 10Hz 50% duty cycle square-wave signal with a hold-down voltage of 34V is used to measure the frequency response of the switch. The square wave signal is applied to the switch as the excitation source, and the modulated output of the switch is monitored on an oscilloscope. Switch

'on' and 'off' time can be determined by measuring the elapsed time during the signal from the input ports requires to reach the output ports through the transmission line. The biasing transistor contributes a switching speed of $4\mu\text{s}$ and is determined by the value of the resistors placed at its collector and base junction inputs. This value is de-embedded from the switch's switching time measurements as shown in Figure 3.35.

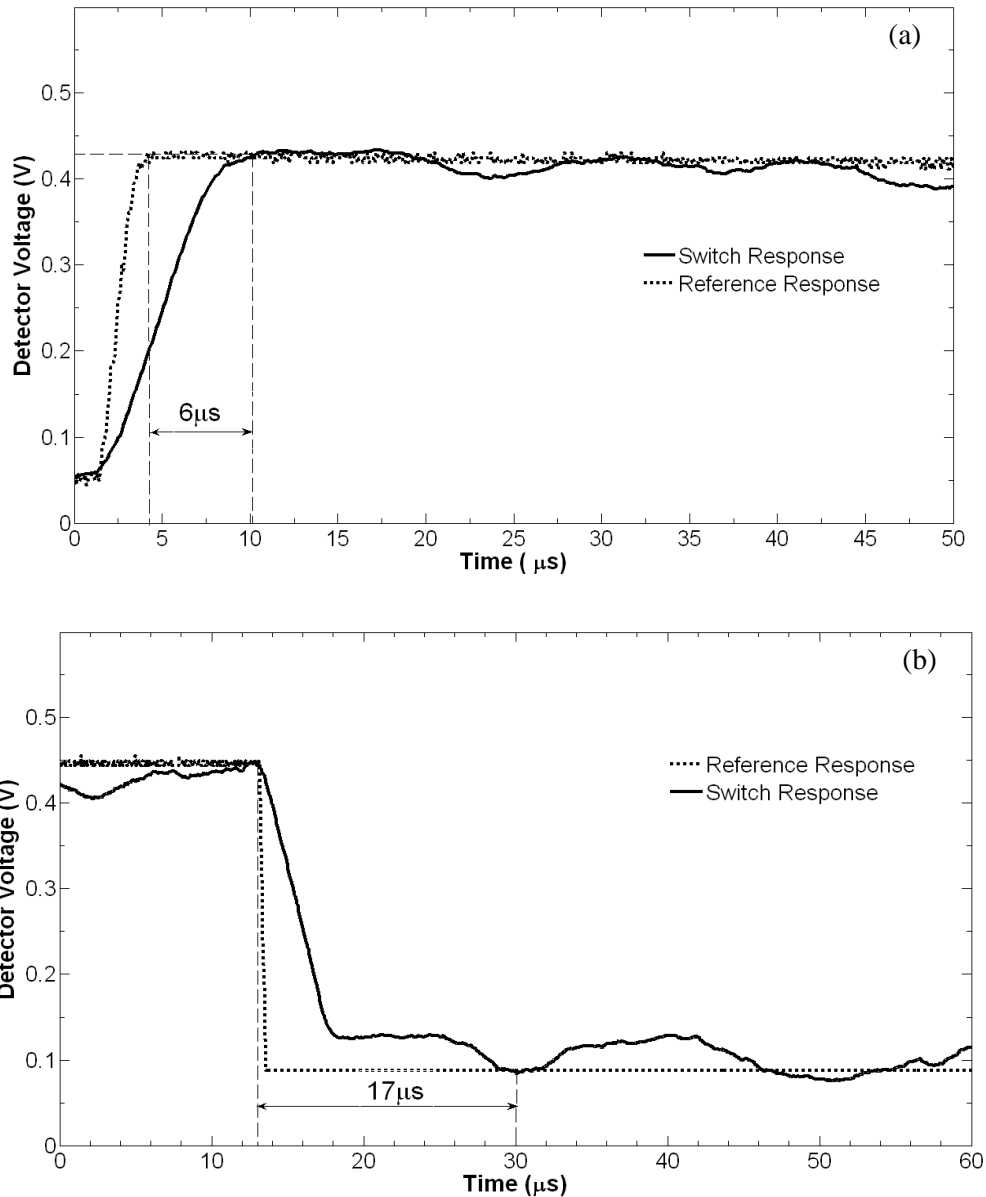


Figure 3.35: Switch's measured (a) rising-edge and (b) falling-edge response time. The $4\mu\text{s}$ delay contributed by the transistor switching circuit is de-embedded from the results.

The switch needs an average of $6\mu\text{s}$ to switch to ‘off’ state and less than $17\mu\text{s}$ to switch release back to ‘on’ state. The mechanical resonance frequency is measured as 22 KHz. It is measured by monitoring the output signal when increasing the exciting signal frequency until the switch fails to deliver the signal efficiently.

3.1.6 Switch Power Handling Capability

The maximum RF power that MEMS switches can successfully handle is an equally important issue for space-based applications such as transmitters in satellite and earth-based communications stations. RF power handling of a capacitive RF MEMS switch is defined as the power at which the MEMS devices fails to operate properly. The two types of failures are RF latching and RF self-actuation. RF latching occurs when the input RF power generates a force large enough to pull down the switch to ‘off’ state even when the DC bias applied is removed. This situation occurs when the RF power is continuously (CW) applied to the MEMS circuit. Such a failure means that once a device is actuated, the switch will not release until the RF power level is lowered below its threshold point. Once the power is lowered, the device is no longer in a failure mode and will continue to operate normally.

RF self-actuation is a situation in which the high RF power actually creates enough potential to pull down the membrane down into the actuated position without applying a DC bias across the switch. Similar to the latching failure condition, if the RF power level is reduced, the switch will return to its normal behavior.

Although a DC voltage is applied to bias the electrostatic switches, these structures respond to any voltage with frequencies lower than the switch self-resonance [11]. For example, a harmonic RF voltage of $V(t) = V_0 \cos(2\pi t)$ applied between the switch beam and driving electrode induces an electrostatic force. This force has a high frequency and low frequency component. The high frequency component will not influence the switch’s behavior; however, the low-frequency force is equal to the force that would have been experienced by the switch structure if an equivalent DC voltage has been applied to them. Therefore, the switch will be actuated if the voltage V_{eq} , given by Equation (3.10), is higher or equal to the pull-in voltage [11].

$$V_{eq} = \frac{V_0}{\sqrt{2}} = V_{RF}^{rms} \quad (3.10)$$

This phenomenon is called self-actuation and occurs with high RF powers. The minimum amount of RF power required to cause the switch to self actuate is given by Equation (3.11) [11].

$$P_{act} = \frac{8K_z g_0^3}{27\epsilon_0 A_{RF} Z_0} \quad (3.11)$$

where A_{RF} is the overlapping switch area that interacts with the applied RF power.

The power handling capabilities of the switches were characterized using the measurement set-up shown in Figure 3.36. The RF signal generated by the synthesized sweeper is amplified using an X-band Travelling Wave Tube (TWT) with a 30-35dB gain, and is then passed through a 10dB coupler to the switch being tested. The output signal is then recorded using a power meter.

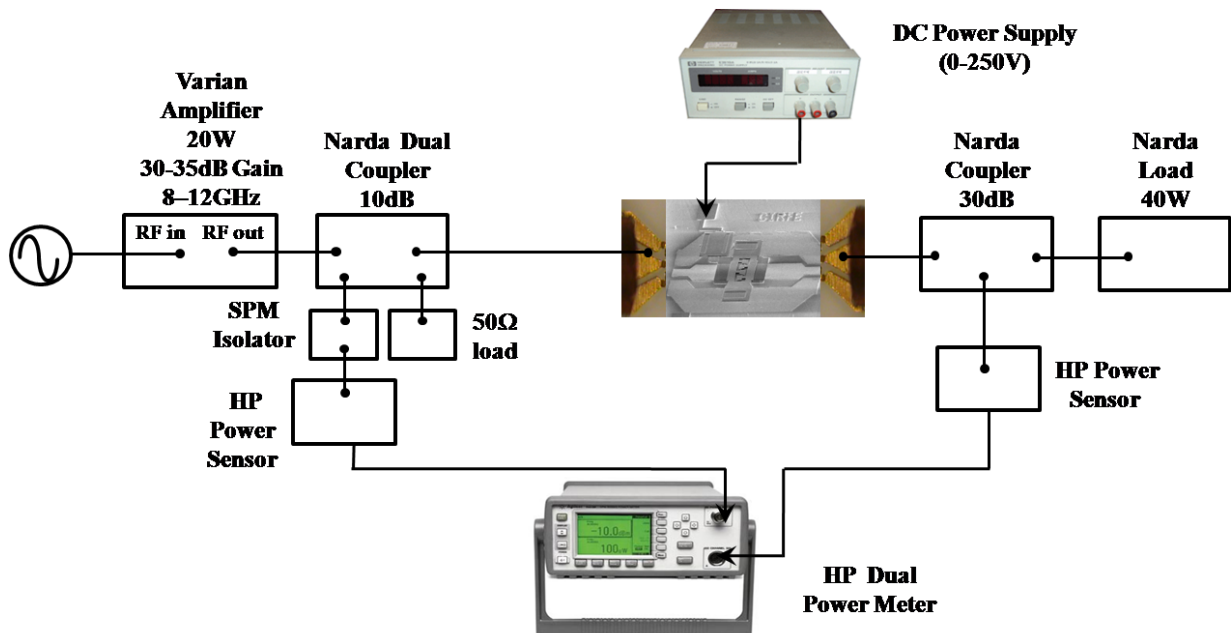


Figure 3.36: High power measurement setup. The switch is biased during ‘hot switching’ using a DC power supply. Output power levels are measured using a dual power meter.

An isolator is placed at one of the outputs of the coupler in order to protect the HP power sensor. A dual power meter is used to observe the RF signal at the input and output of the test devices and is also used to measure and account for losses contributed to from the connecting cables. The measurements were performed at 10.5GHz because of the limitations imposed by the TWT amplifier. The power coming out of the MEMS switch was coupled to a 30dB coupler and fed into the power meter.

The switches were initially tested in the ‘on’ state with no applied bias voltage and an input RF power of approximately 0.7mW in order to observe for the self-actuation failure. The power was then steadily increased until the switch actuated. The switch demonstrated power handling capabilities of up to 6W for continuous RF power before self-actuating, also referred to as ‘cold switching’ testing. The switch was then tested under ‘hot switching’ conditions, where the switch was actuated continuously while slowly increasing the RF power tested the latching failure. The latching failure was observed at 560mW.

In conclusion, the capacitive-contacted dual-warped beam switches have an impedance ratio of 170:1 from the open to closed state with a shunt ‘on’ state capacitance of 59fF and an ‘off’ state capacitance of 10pF. It exhibits isolation better than 40dB at the resonant frequency of 10.5GHz, and exhibits an insertion loss of less than 0.2dB.

3.2 SP3T Dual Warped-Beam MEMS Switch

Traditionally, solid-state components such GaAs MESFETS and PIN diodes have been used to implement single-pole multi-throw switching networks that are required for switched line phase shifters in phased arrays. Although these conventional components have been used for several years, they have several disadvantages. They rely on control of current through a semiconductor junction or a metal-semiconductor junction, and there is a resistive loss associated with charge flow that consumes substantial DC and RF power [21]. This consumed power generates heat that must be dissipated which adds to the system size and complexity. Lastly, linearity is required for modern, wide band communication systems that must process signals with a wide dynamic range, but transistors and diodes are nonlinear devices. Implementing the SPNT configuration is very difficult

to accomplish using semiconductor devices especially if wide PIN diode or FET switches are used, which result in off-path resonances that greatly reduce the bandwidth [43].

Single-pole n-throw (SPNT) switches are an integral part of many microwave systems such as transceivers, where they are used to switch a device between receive and transmit modes, and receiver front ends for diversity application. While most of the research has been focused on developing SPST switches, very limited work has been reported on multi-throw switches. In [44], an SP3T switch is reported with the use of three resistive series switches with an insertion loss of 0.45dB and isolation of 20B from DC to 25GHz. Authors in [45] presented an SP3T switch realized with a hybrid approach, where the switches are affixed to the circuit surface with the use of flip chip technology. Electromagnetic simulations in addition to circuit modeling are used to design and optimize the switch. Three-throw and four-throw capacitive-configured RF MEMS switches based on the dual warped-beam design are used to construct the complete SP3T and SP4T switches. Measurements indicate an insertion loss of 0.6 ± 0.25 dB and 0.69 ± 0.15 dB at 10.5GHz and 14.6GHz for the SP3T and SP4T switches, respectively and isolation better than 30dB.

3.2.1 Design

Figure 3.37 illustrates the single-pole three-throw (SP3T) RF MEMS switch structure. The SP3T is a four-port device designed in FGC waveguide environment so that it is easily integrated with other circuits. The circuit consists of a three output T-junction with SPST switches monolithically integrated at each of the output arms. The input port is a 50Ω characteristic impedance line with dimensions $G/W/G$ of $32\mu\text{m}/60\mu\text{m}/32\mu\text{m}$. The switch is placed a quarter-guided wavelength ($\lambda_g/4$) from the input port so when the switch is in the ‘off’ state, the virtual RF short is transformed to an open at the junction. At X-band, the switches are therefore placed approximately $2400\mu\text{m}$ from the tee junction, which corresponds to $\lambda_g/4$ at 10.5GHz. In order to achieve the highest isolation, the resonant high inductive warped-beam MEMS switches presented earlier are placed at the designated locations on each arm of the SP3T.

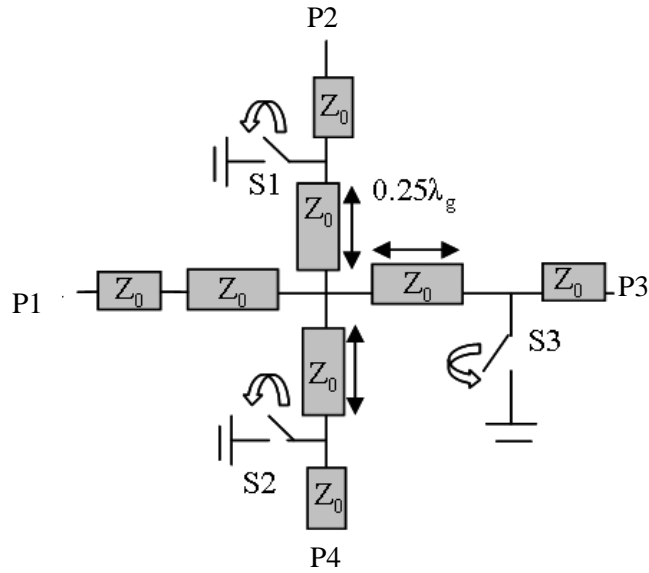


Figure 3.37: Equivalent circuit layout of the SP3T capacitive shunt switch.

Figure 3.8 illustrates the fabricated SP3T switch with a total circuit area of approximately 0.25cm^2 . Gold air bridges are used to connect all the ground planes within the vicinity of a discontinuity or junction to suppress any unwanted coupled-slot line modes.

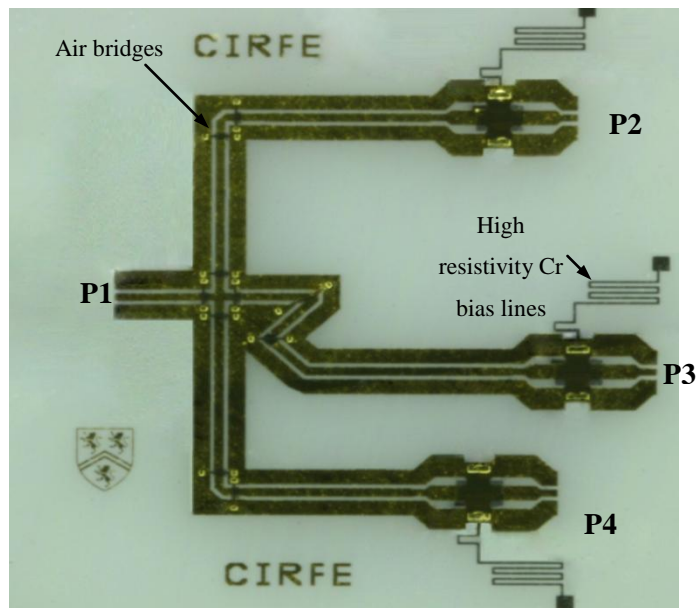


Figure 3.38: The fabricated Single-Pole Triple-Throw (SP3T) circuit.

Moreover, meandered FGC lines are used to reduce the switch's intrinsic circuit area and minimize radiation. The switches are DC-biased using high resistivity Cr lines routed externally to the switch's anchor. The T-junctions are optimized to provide the best possible impedance match and delay flatness over the X-band frequencies. Because the SP3T utilizes quarter wavelength lines for matching, the bandwidth is limited to $\pm 10\%$.

The circuits are modeled and optimized using Agilent's HP ADS circuit simulator. Figure 3.39 shows the equivalent circuit model of the SP3T switch set up in ADS in which port 2 only is in the 'on' state mode. In order to include RF effects, the capacitive MEMS switches, the tee junction and each CPW section is modeled in Sonnet and simulated to obtain its S-parameter matrix. These S matrices are then imported into ADS and cascaded to obtain the simulated response shown in Figure 3.40 for a more accurate prediction of the circuit's performance.

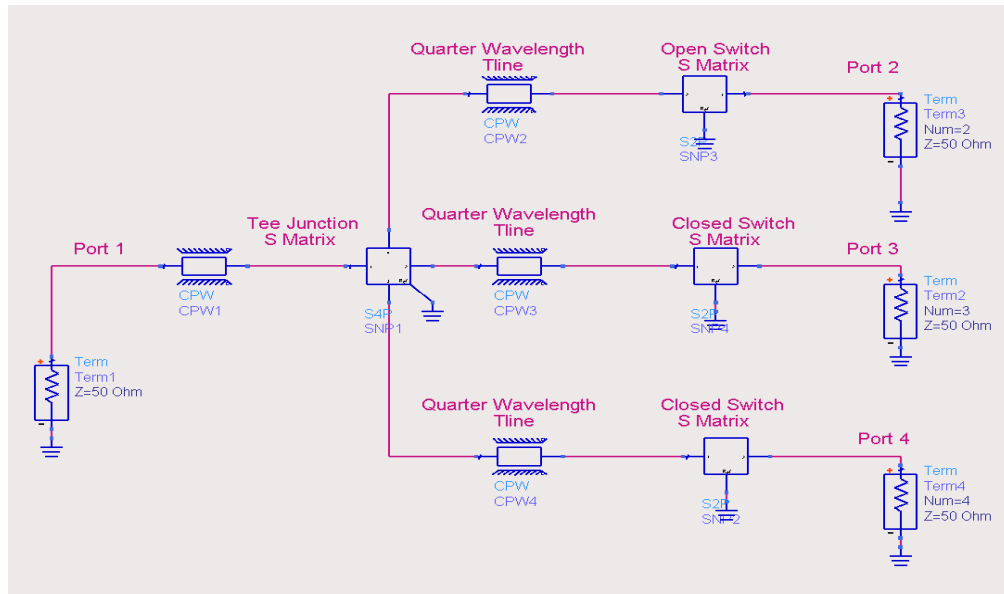


Figure 3.39: Equivalent circuit set-up in HP-ADS[®]. The EM simulated S matrix of the T-junction, quarter wave transmission lines and 'on' and 'off' states of the switch obtained from Sonnet and HFSS simulations are used in the ADS circuit simulator to optimize and obtain the simulated response of the SP3T switch.

Simulated results for the case where port 2 is in the ‘on’ state and both ports 3 and 4 are in the ‘off’ state are shown in Figure 3.40. The results predict isolation better than 40dB across the X-band range of frequencies with an insertion loss of less than 0.2dB at port 2. The switch’s return loss is better than 20dB over the frequency range of 9.5GHz to 11.25GHz.

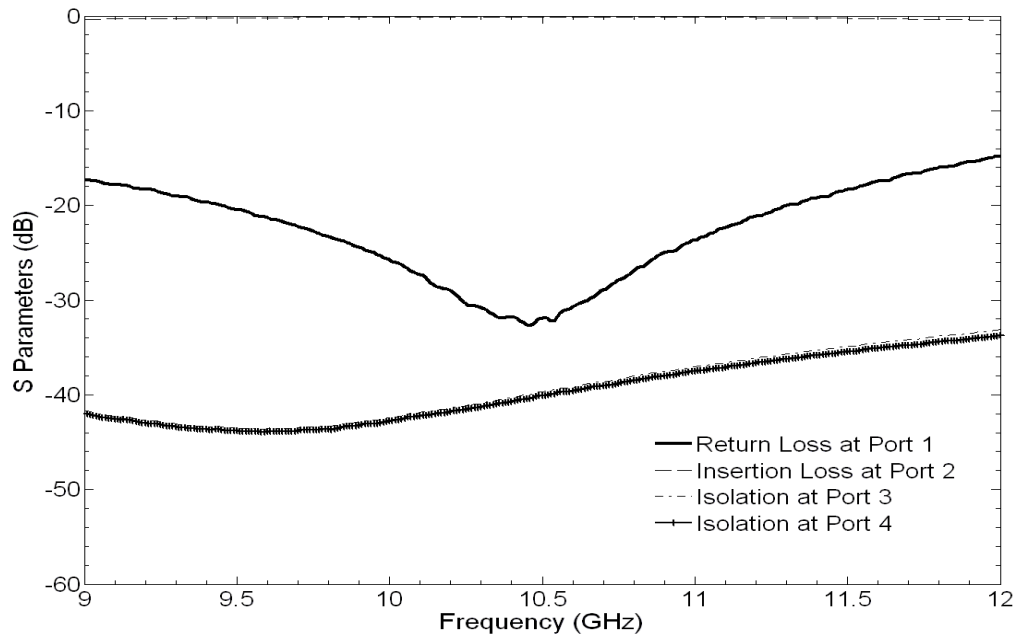


Figure 3.40: Simulated results of the SP3T switch circuit with Port 2 open (switch is un-actuated to remain in ‘on’ state) and Ports 3 and 4 are closed (switches are actuated to ‘off’ state).

3.2.2 Measured Results

The SP3T switch has been fabricated using the same 5-mask process as that employed for the SPST MEMS switch presented in the previous section. In the ‘off’ state mode, the measured isolation characteristic of the SP3T switch between the input port and ports 2 and 3 is better than 30dB, as illustrated in Figure 3.41. The switches placed at Ports 2 and 3 in ‘off’ state present an isolation better than 30dB over the frequency band of interest.

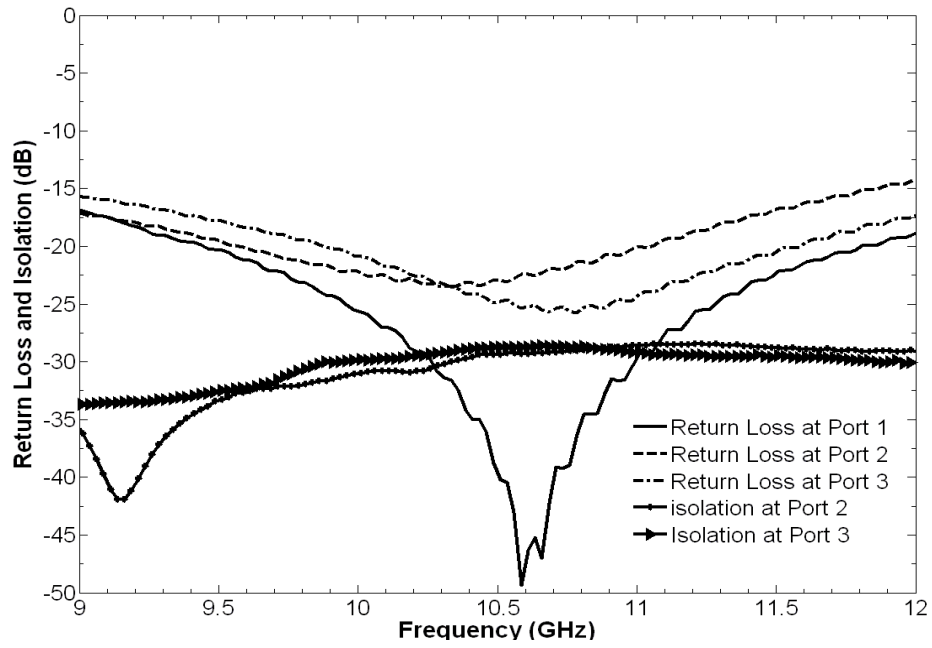


Figure 3.41: Measured return loss and isolation across the SP3T output ports for the different activated ports.

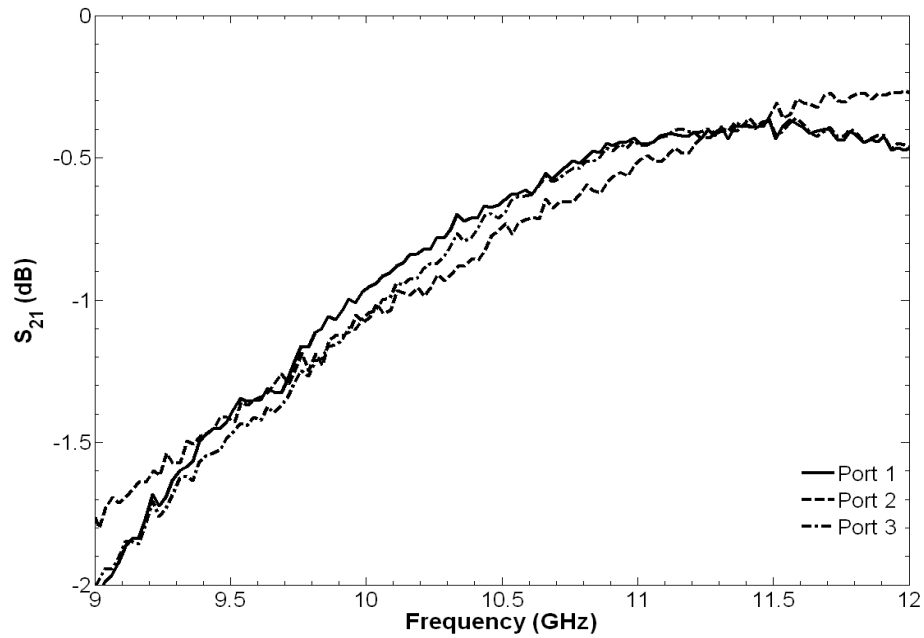


Figure 3.42: Measured insertion loss across the SP3T output ports when each switch is kept in 'on' state.

The measured insertion losses between the input port and each output port (P2, P3 and P4) at 10.5GHz are shown in Figure 3.42 ranging around 0.6 ± 0.25 dB. Return loss for all three of the output ports are measured better than 15dB for the frequency range between 9GHz to 12GHz. Isolation for the measured switches are approximately 5dB to 10dB lower than the simulated switches and can be attributed to fabrication errors and switch conformity to the signal line in 'off' state.

3.3 SP4T Dual Warped-Beam MEMS Switch

This switch is designed in parallel with the SP3T to operate over the Ku band, and its purpose is to select the different input ports of the 4 x 4 Butler matrix allowing for the design of a fully integrated passive switchable phased array.

3.3.1 Design

Figure 3.43 illustrates the SP4T switch circuit design. Similar to the SP3T switch circuit design, the circuit consists of a four-junction symmetric tee with a MEMS switch integrated at each of the output arms. The arms of P3 and P4 are branched out at about 25° from the center input port.

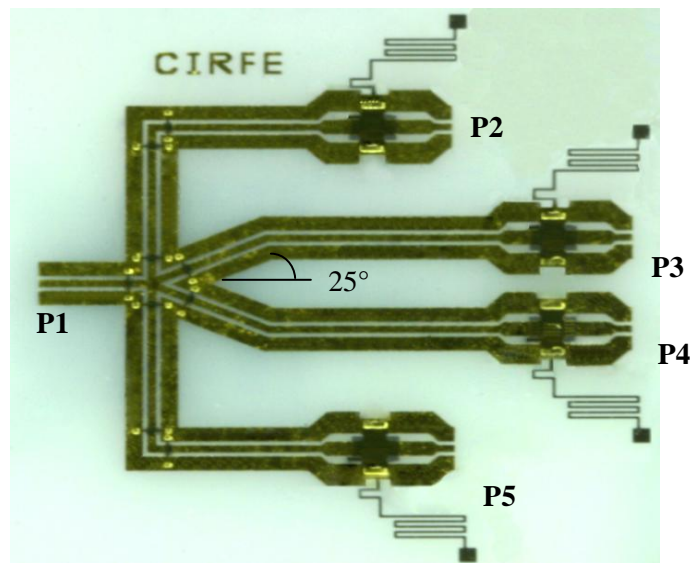
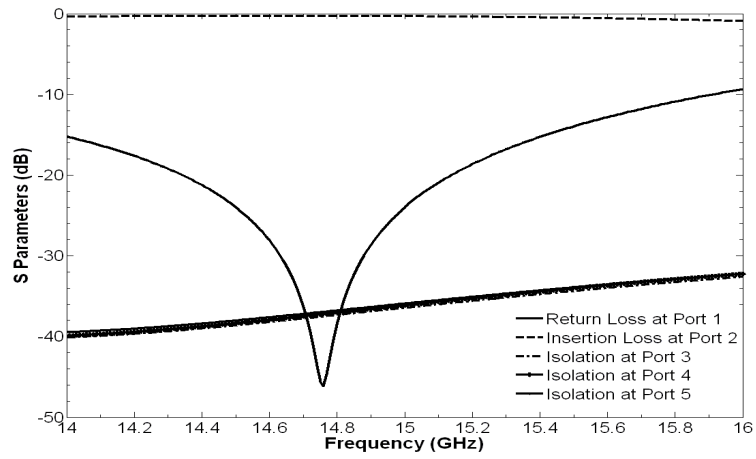
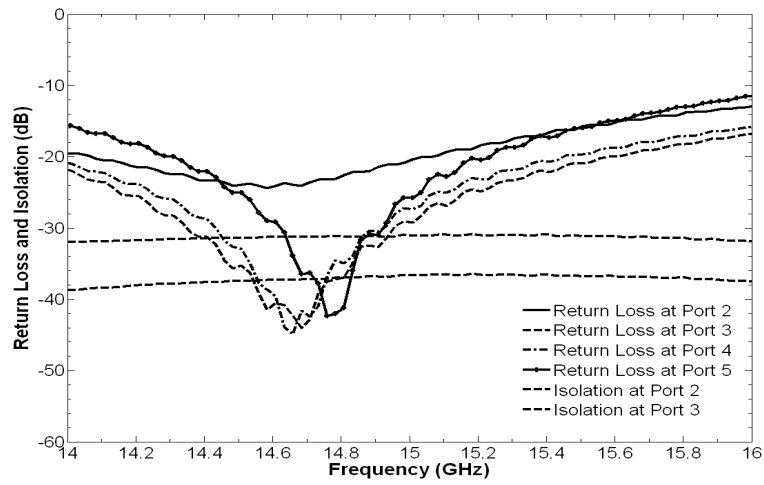


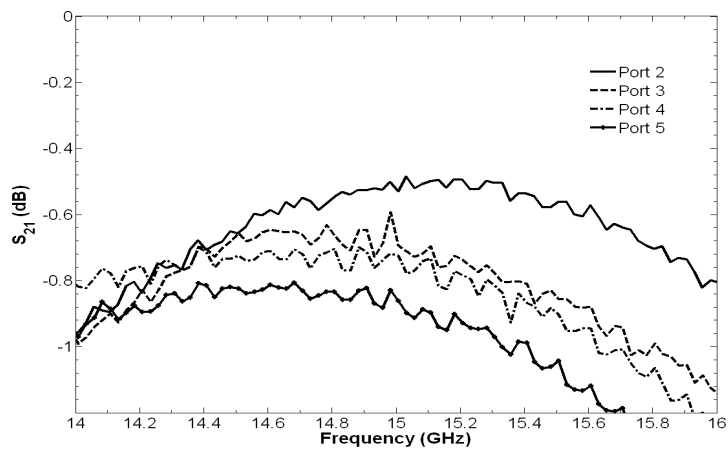
Figure 3.43: The Single-Pole Four-Throw (SP4T) circuit.



(a)



(b)



(c)

Figure 3.44: (a) Simulated, (b) measured return loss and (c) insertion loss for the SP4T.

3.3.2 Measured Results

In the 'off' state mode, the measured isolation characteristic of the SP4T switch between the input port and ports 2 and 3 are less than 30dB, as illustrated in Figure 3.44(b). The measured insertion loss between the input port and each output port approximates around 0.69 ± 0.15 dB.

The design, fabrication and characterization of a SPST, SP3T and SP4T switch based on low-loss dual-warped beam switches have been presented. By introducing warped bimetallic beams into the switch structure, measured results show a significant improvement where the downstate capacitance is doubled and the upstate capacitance is reduced by half. The SPST switch RF and mechanical performance can be further enhanced by means of serpentine springs to achieve lower actuation voltages and better isolation. The SP3T and SP4T switches show good results with insertion losses of 0.6dB and 0.8dB, minimum return losses of 20dB, and isolation of less than 30dB, respectively. These multi-throw switches are implemented into the beam forming networks including the MEMS phase shifter and passive 4 x 4 Butler matrix for signal routing.

Chapter 4

ESA Individual Components

4.1 Introduction

The ESA components must be developed to meet typical SBR system specifications such as a 10% bandwidth and high isolation, as listed in Table 4.1 [47].

Table 4.1: Phase shifter target specifications [47].

Parameter	Specification
Nominal frequency	X-Band (8 – 12GHz)
Percentage bandwidth	10 % (1GHz)
Insertion loss	1.5dB
Return loss	< -20dB
Switching time	10 μ s
Max peak power	700mW

To achieve the performance specifications listed and simplify the design simultaneously, some design choices have to be made. These include the phase shifter design and layout (including phase shifter type, number of phase shifter bits, size), the power divider design and layout and the ESA component integration method. The following sections summarize the parametric analyses for the ESA components designed including the MEMS 3-bit phase shifter, the power divider and the capacitive interconnects developed over X-band. A Ku-band 4 x 4 Butler matrix is also examined as a passive phase scanning alternative to the MEMS phase shifter. The fabrication processes used to produce these components in CIRFE labs will be described in detail. Finally, the measured results obtained are presented. The monolithic integration of these ESA components will then be presented in detail in Chapter 5.

4.2 MEMS Integrated Phase Shifter

One of the key elements in the array design is the MEMS phase shifter. RF MEMS phase shifters possess many advantages such as low loss, improved power handling capability and can also be used to realize high density packages to reduce the size and weight components. 50-75% of the T/R modules can be eliminated in large phased arrays by using MEMS phase shifters [48]. The majority of MEMS switched-line phase shifters reported to date have been designed using microstrip lines. However, the proposed phase shifter in this thesis is designed using FGC waveguide lines in order to maintain consistency with the rest of the module components, and to avoid the use of inter-level ground planes and vias typically required for microstrip line designs.

4.2.1 Design

In a distributed MEMS transmission line (DMTL) phase shifter, up to eight switches are used to generate a 90° phase shift, and therefore up to sixteen switches are needed for a 180° phase shift. Lange couplers in reflected line phase shifters in the X-Band can take up a large chip area. The switched-line technique is used to realize a 3-bit digital phase shifter shown in Figure 4.1, which can result in a more compact structure, small size and relatively low insertion loss. The effective phase shift is the difference in electrical length between the 0° length (reference length) and the delay line. The phase shift in degree of each bit is given by:

$$\Delta\Phi = \frac{2\pi(l_d - l_r)}{\lambda} \quad (4.1)$$

where l_d and l_r are the lengths of delay lines and reference lines, respectively. These sections of lines are switched ‘on’ and ‘off’ using shunt capacitive MEMS switches. A compact phase shifter with lower losses can be achieved by folding the transmission lines, setting the reference line electrical length close to zero and using SP3T switches instead of SPST switches. Implementing these switches into the phase shifter circuit is a difficult task because several design problems may arise. Using a shunt capacitive switch requires an additional quarter-wave transformer from the junction to the switch, which can make the overall phase shifter larger with narrow bandwidth characteristics.

Therefore, the layout of the phase shifter is extremely important during design, because it can simplify the integration process and enhance RF performance.

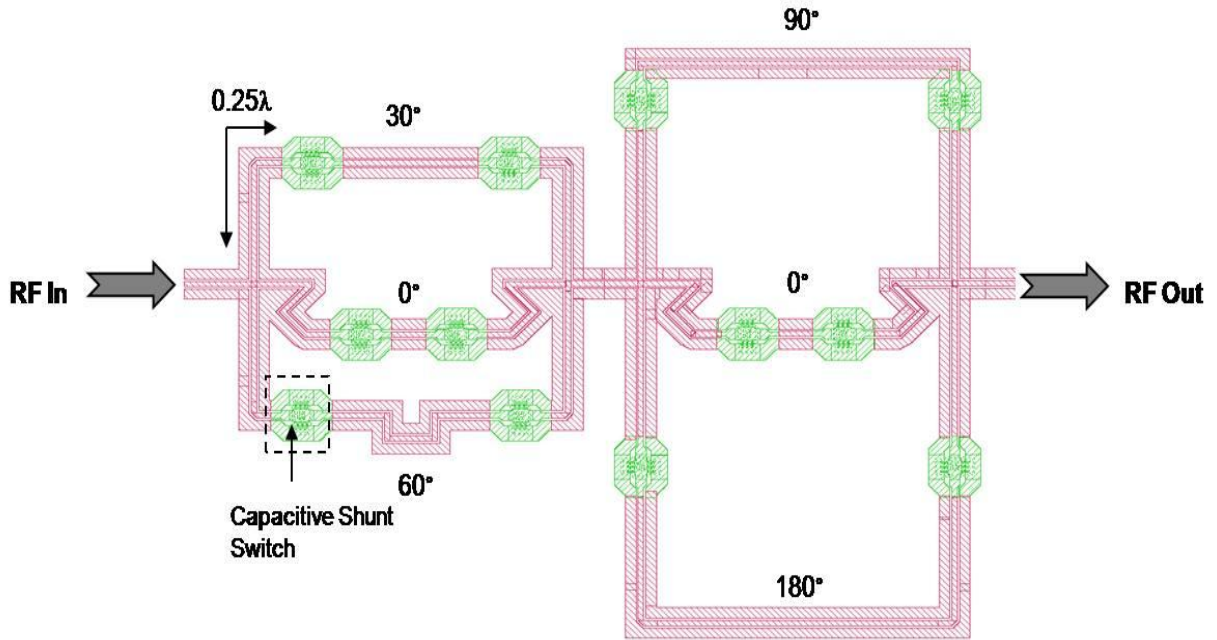


Figure 4.1: Proposed digital phase shifter. It consists of four cascaded SP3T capacitive shunt switches with varying delay line lengths. The phase shifter has nine switchable.

The size of the switched-line phase shifter is dependent on the center frequency. Figure 4.1 shows a schematic of the 3-bit time delay phase shifter with various line lengths that are interconnected using RF MEMS switches. Any differential phase value from 0° to 240° can be achieved in 30° increments by appropriate settings for the 12 switch positions. Since the insertion loss of the phase shifter is primarily determined by metal loss and switch loss, a fewer number of switches can result in a lower overall system insertion loss. The impedance of delay lines is designed at 50Ω . The length of delay lines is determined by Equation (4.1). To achieve a compact configuration of the phase shifter, some delay lines are folded with bends $M=0.6$.

4.2.2 Fabrication Process

The RF MEMS phase shifter is based on the same 5-mask batch process developed for the capacitive MEMS switches and are fabricated in CIRFE labs. The footprint of the phase shifter fabricated is about 1.42cm^2 . A captured image of the released fabricated RF phase shifter is shown in Figure 4.2.

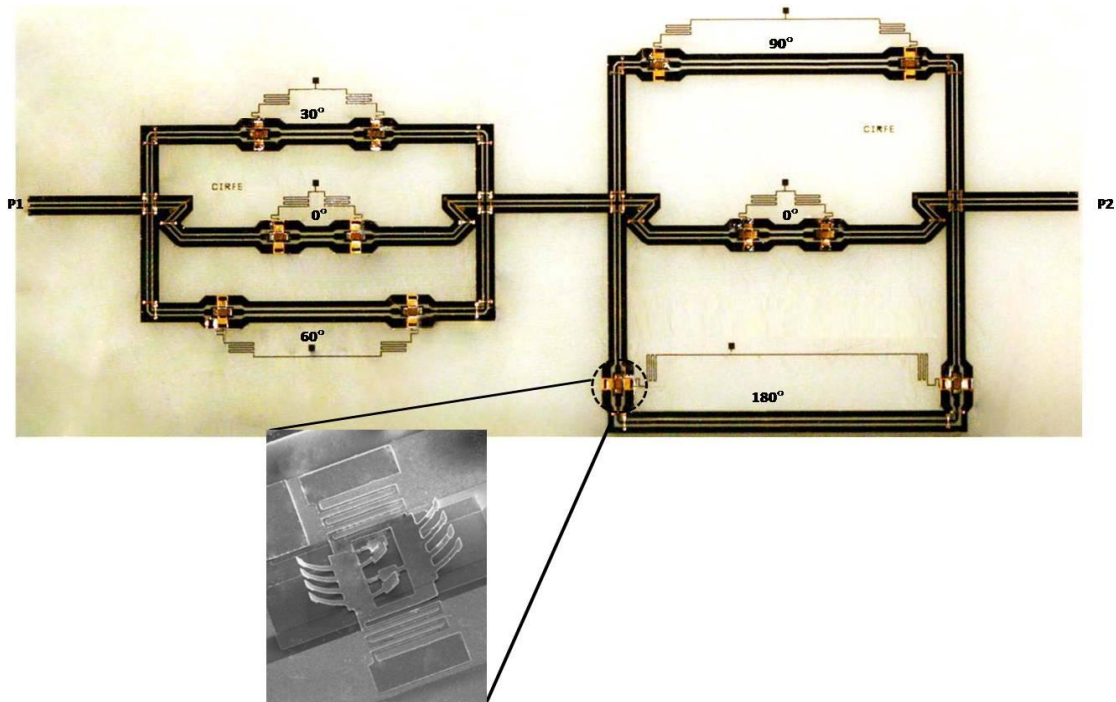
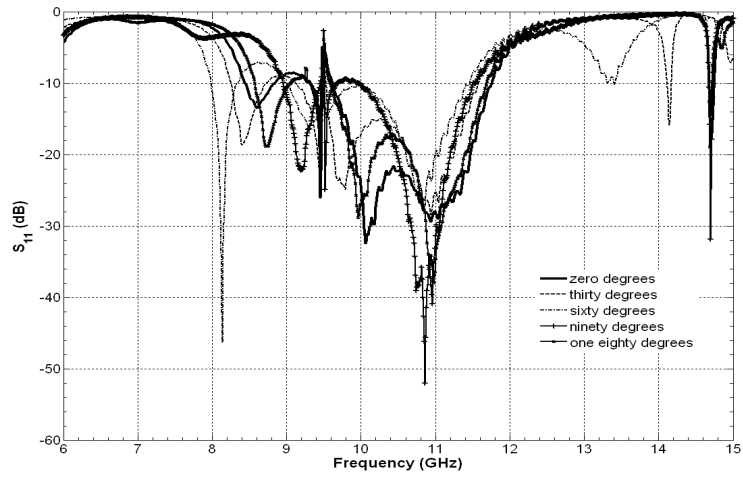


Figure 4.2: Fabricated MEMS integrated phase shifter.

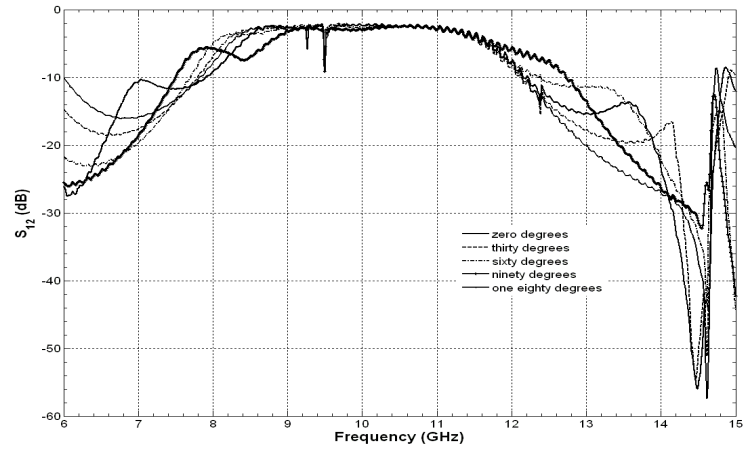
The phase shifter circuit is processed on a 10mil thick alumina wafer and features a via-less topology using FGC lines. This layout is set up in HP ADS and optimized at 10.5GHz by cascading the exported S-matrices of the EM simulated lines and the S-parameters obtained from the measured SP3T switches. The line lengths are optimized to account for changes in phase velocity as a result of the capacitive effect introduced by the MEMS switches. The delay sections are designed separately for the desired phase shift and then combined. Each section is designed to achieve a low insertion loss and a good return loss over the X-band frequency range. Careful attention is given to minimize

coupling between the signal lines. An EM simulation using Sonnet[®] is performed to determine the amount of coupling that would result between two 50Ω FGC lines 1mm long at 10.5 GHz. As long as the spacing between the FGC lines is maintained to more than 400μm, the coupling between the lines is less than 60dB. In this design, the smallest distance between the delay signal lines exists between the 0° and 60° lines and is 1300μm.

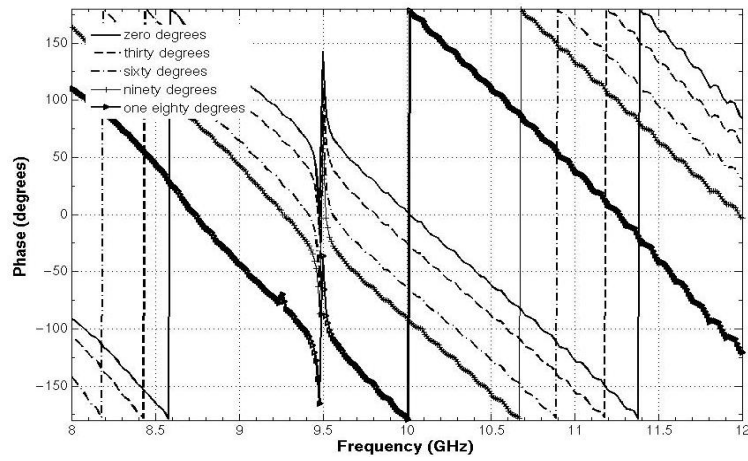
The simulated return loss of the phase shifter plotted in Figure 4.3(a) is better than 15dB for the phase states of 0°, 45°, 90° and 180° at 10.5GHz. The theoretical insertion loss from 8GHz to 12GHz for all 5 states is shown in Figure 4.3(b). Gold and alumina substrate loss properties are used in the analysis with 1.95±0.3dB insertion loss predicted at 10.5GHz and rms phase error of 3°. Typically, the combined isolation of the switches in ‘off’ state must exceed 20dB in the design’s frequency band or there will be ripples in the amplitude and phase response due to leakage in the ‘off’ arm [49]. There are some resonances present in the simulation response close to 9.5GHz and those are believed to be a result of the dual-mode nature of ground CPW. An ideal CPW does not have a ground plane under the substrate, but Sonnet analysis is performed inside a six-sided metal box so the substrate’s bottom side is grounded by default.



(a)



(b)



(c)

Figure 4.3: 3-bit phase shifter's simulated (a) return loss, (b) insertion loss and (c) phase.

4.2.3 Measured Results

A two-port on-wafer measurement is performed using a Cascade probe station to evaluate the phase shifter's performance, and the results are plotted in Figure 4.4. The measured results show a return loss better than 20dB and an insertion loss of about 2.5 ± 0.2 dB. Figure 4.4(c) indicates a measured phase error of about $\pm 6^\circ$. The phase shift increases linearly with frequency, as is typical of all delay-line techniques with minimal transmission line dispersion. Due to capacitive loading effects of the MEMS switches, a slight shift in the resonant frequency is observed when the different phase shifter line sections are actuated. The loss figure of merit is 0.6dB/bit. Since phase shifter losses are mainly due to the metal and switch losses [21]; increasing FGC waveguide metal plated thickness may further reduce insertion losses.

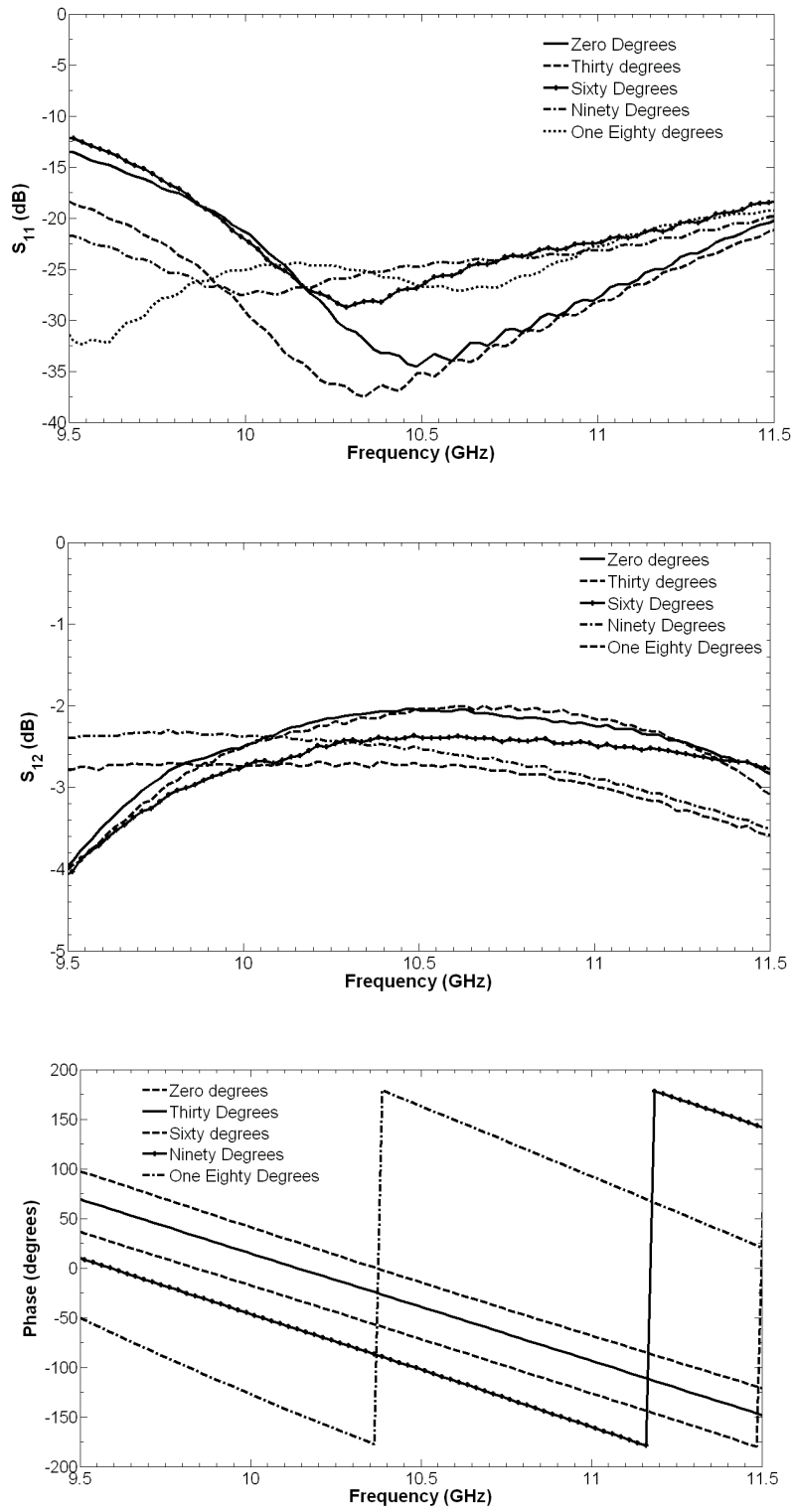


Figure 4.4: 3-bit phase shifter measured (a) return loss, (b) insertion loss and (c) phase.

4.3 Power Dividers

One of the basic passive components found in phased array systems are the power dividers used for RF power division or power combining. There are several critical parameters in selecting a power divider for an ESA system including: operating bandwidth, output port isolation and insertion loss, amplitude balance, power handling capability, size and ease of fabrication. As an indication of high performance, a power divider has a typical isolation of 20dB, and with higher isolation there is a smaller chance of leakage between the output ports. Amplitude balance, sometimes referred to as amplitude tracking, is also an important indication and is simply the amplitude difference between the powers at the output ports. In addition, the power handling capability is of high importance and is dependent upon the internal resistors used. The following sections discuss the design approach and results obtained for the power divider proposed.

4.3.1 Design

A power divider is ideally a lossless reciprocal device which can perform vector division and summation of two or more signals and thus is sometimes called a power combiner [50]. There are several components used for power division including the traditional Wilkinson power divider, the microstrip T-junction, the tapered-line divider, and a rat-race coupler divider. Wideband power dividers are typically desired in a phase shifting network for space-based systems. The type of power divider initially considered for the proposed integrated 3-D module is a simple microstrip T-junction power divider, optimized to operate in wideband. These T-junctions consist of three transmission lines and do not have a matching resistor across the junction. The output 100Ω lines for a two-way divider for instance, require a quarter-wave transformer to transform the resistance seen at these 100Ω lines to 50Ω. The power dividers are designed to operate within 8-12GHz (X-band frequency range). In comparison, a Wilkinson divider is a lossy three-port network and consists of quarter-wave length arms of impedance $1.414Z_0$ with an isolation resistor of impedance $2Z_0$ connected across ports 2 and 3.

EM Sonnet is used to model and simulate the two and eight-way microstrip power dividers. Figure 4.5 illustrates the power dividers with strip-line tuning stubs and coupled parasitic tuning

elements. The circuit is modeled on a 25mil thick Alumina wafer with dielectric constant of 9.9 and loss tangent of 0.0001. The power dividers are optimized to have a wideband performance by implementing open-circuited stubs and parasitic elements along the divider's output branch lines. Using the optimization tool in sonnet, these elements are fine tuned in terms of width, length, spacing and location along the output lines. The tuning elements are assumed to have open-ended terminations.

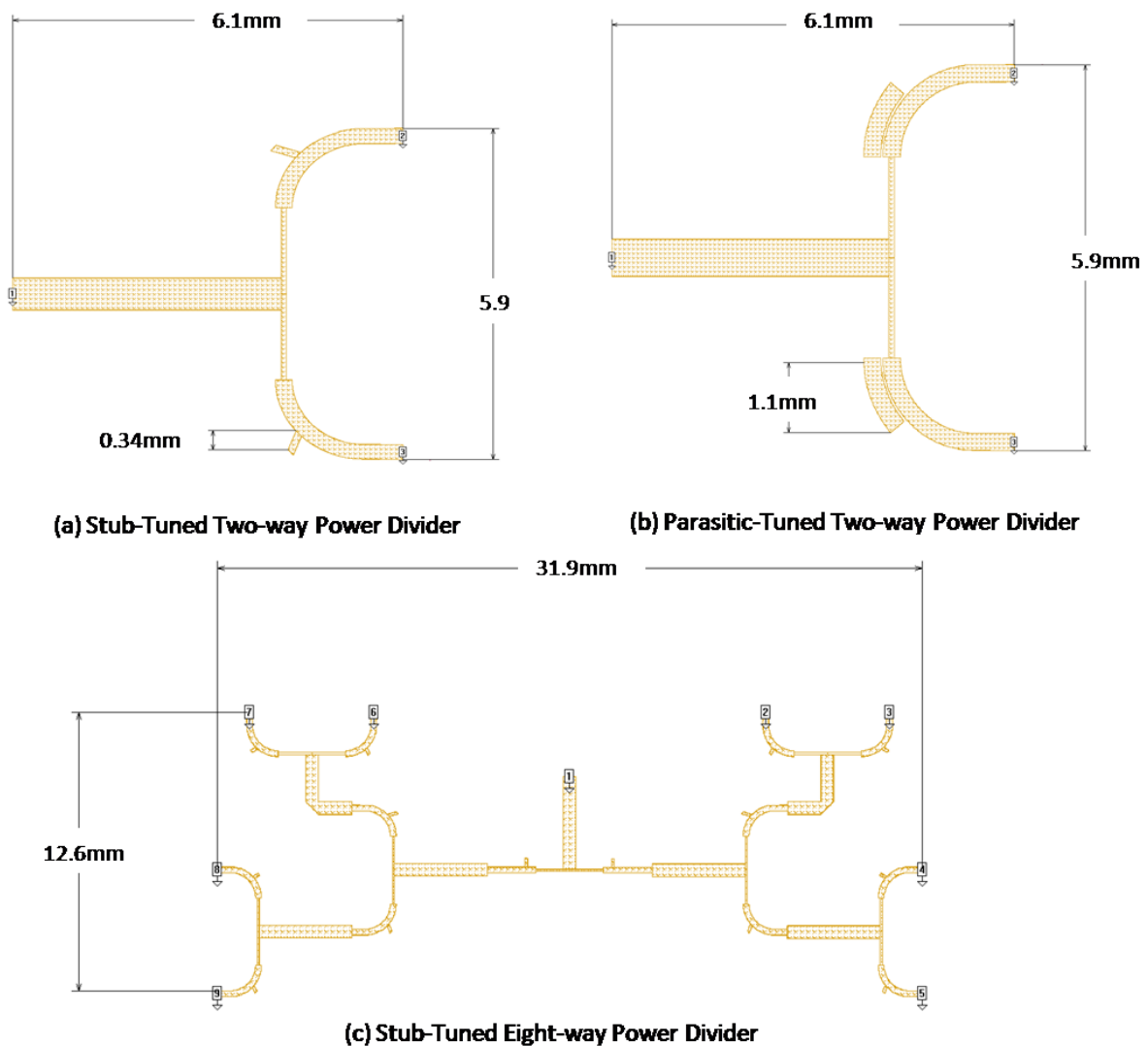


Figure 4.5: The two proposed designs of the T-junction power divider. The power dividers are optimized to have a wideband performance by implementing open-circuited stubs and parasitic elements along the divider's output branch lines.

Several parameters are optimized for the two configurations of power dividers, parasitic and stub-tuned, to obtain the best performance. The simulated results obtained for the two-way power dividers in comparison to a standard two-way power divider without any tuning elements are illustrated in Figure 4.6. Return loss is improved to better than 40dB, the insertion loss is slightly improved by 0.02dB, and the -20dB bandwidth is increased to 84%, with a center frequency of 10.4GHz.

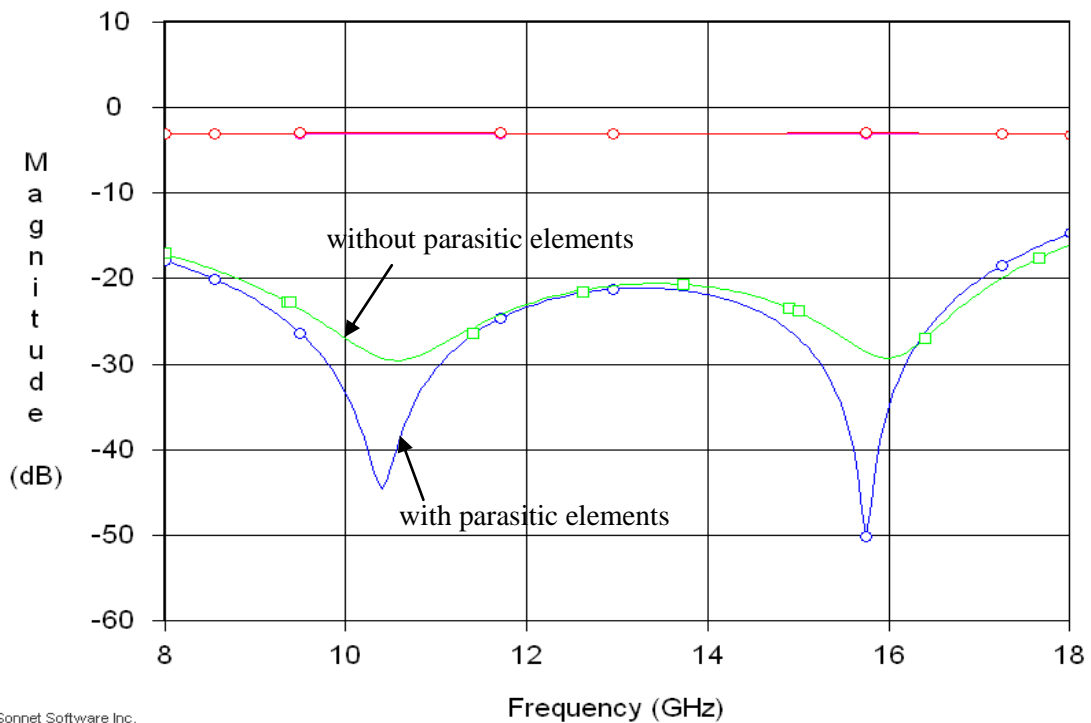


Figure 4.6: Reflection and insertion loss responses of the two-way power divider with parasitic elements. Return loss is improved to better than 40dB, the insertion loss is slightly improved by 0.02dB, and the -20dB bandwidth is increased to 84%.

However, looking at the results obtained with the tuning stubs, the power dividers are found to decrease in bandwidth with improved matching. In Figure 4.7, increasing the length of the stubs are found to enhance the matching of the higher frequency resonance (15.9GHz) and deteriorate the lower frequency resonance at 10.5GHz. The bandwidth for S_{11} less than -20dB is about 70%.

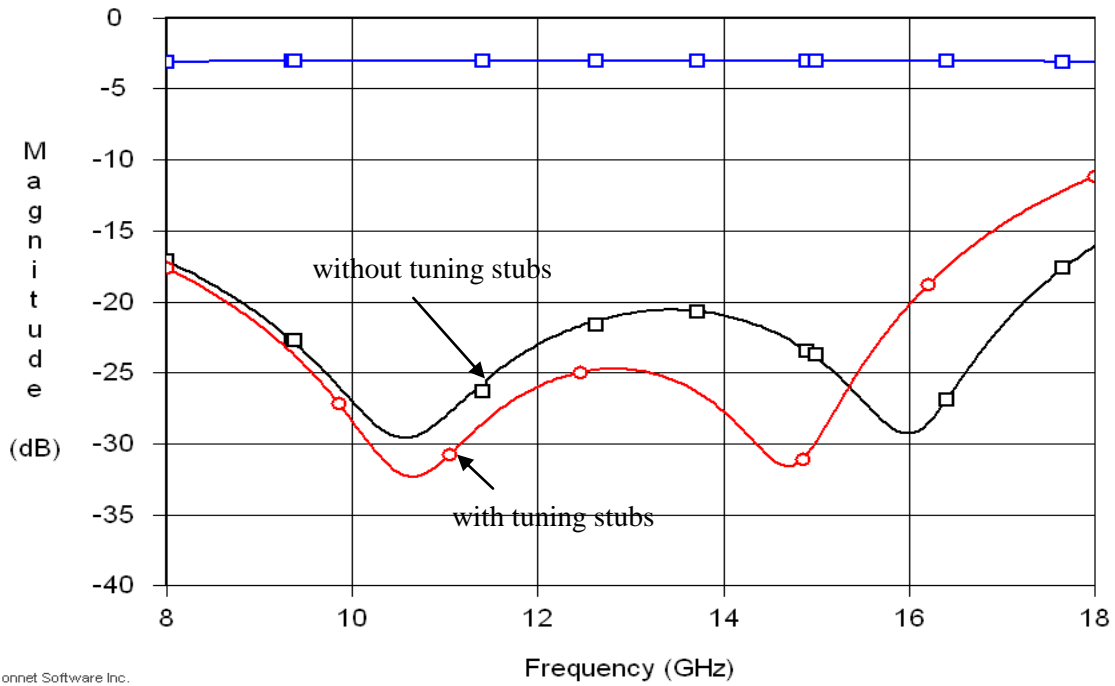


Figure 4.7: Reflection and insertion loss of the two way power divider with tuning stubs. Increasing the length of the stubs is found to enhance the matching of the higher resonance frequency and deteriorate the lower resonance frequency.

A summary of the bandwidths and sizes achieved for all the power dividers designed are listed in Table 4.2.

Table 4.2: Summary of the power divider simulated results obtained.

	Stub-Tuned		Parasitic-Tuned	
	BW (%)	Size (cm ²)	BW (%)	Size
2-way	70	0.36	84	0.056
4-way	25	1.15	7	0.109
8-way	25	4.13	8	0.629

Including stubs or parasitic elements into the T-junction design can improve their performance. The advantage of such configurations is their simplicity, planar configuration and flexibility in comparison to Wilkinson power dividers. Their design parameters such as stub or parasitic element length, width and location can all be adjusted to fine tune the performance to the desired bandwidth and frequencies. However, a disadvantage of this structure is the reflections present at the output ports. For instance, the stub-tuned 8-way power divider exhibits reflections at its output ports of about -11dB with 13% bandwidth.

One of the main advantages of Wilkinson power dividers is that the three port network can be finely matched to obtain good isolation at its output ports. Because of this advantage over the other types of power dividers such as T-junction dividers and resistive dividers, there have been many efforts to optimize the Wilkinson structure [51-53]. The typical Wilkinson power divider consists of a three port passive network, as shown in Figure 4.8. The input signal at port 1 can be divided between the two output ports comprised of quarter-wave transmission line transformers that transform the single input impedance of 50Ω to the impedance associated with the parallel output ports.

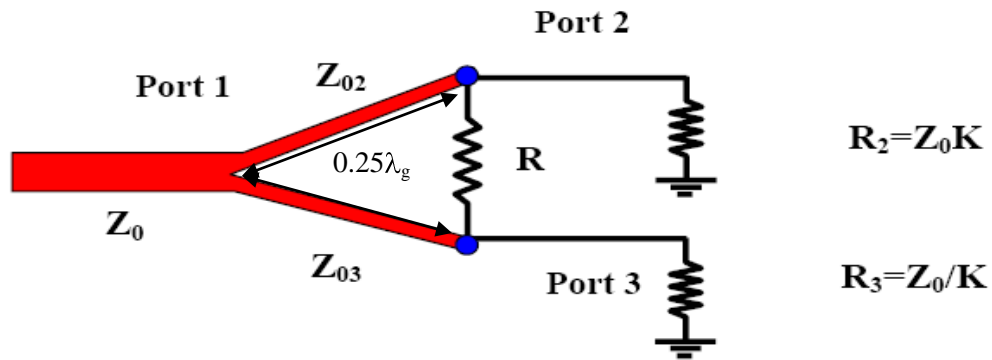


Figure 4.8: Schematic of a typical Wilkinson power divider [50].

If the divided power between ports 2 and 3 is defined with a ratio of $K^2 = P_3/P_2$ then the divider design can be accomplished by using the following equations [50].

$$Z_{03} = Z_0 \sqrt{\frac{1+K^2}{K^3}} \quad (4.2)$$

$$Z_{02} = K^2 Z_{03} = Z_0 \sqrt{K(1+K^2)} \quad (4.3)$$

$$R = Z_0 \left(K + \frac{1}{K} \right) \quad (4.4)$$

where Z_0 , Z_{02} , and Z_{03} are the characteristic impedances of port 1, 2, and 3, respectively, and R is the shunt resistor for isolation between port 2 and 3. Therefore, for the equal-split power divider ($K=1$) with a 50Ω -impedance input line, Z_{02} , Z_{03} and R should be 71Ω , 71Ω , and 100Ω , respectively. The input VSWR of this divider is primarily influenced by the quality of the impedance transformers and the VSWRs of the loads which terminate the outputs of the device.

The Wilkinson power divider is designed to operate in the X-band, centered at approximately 10.5GHz. Using Sonnet, the dimensions are optimized and fine-tuned. The equal-split Wilkinson power divider is designed using FGC lines to maintain consistency with the rest of the phased array components. FGC lines are similar to CPW lines with electrically narrow ground planes, with the added advantage of not supporting parallel-plate modes, thus eliminating the need for via holes between upper and lower ground planes and reducing radiation loss [54]. Values of $50\mu\text{m}$, $68\mu\text{m}$, $80\mu\text{m}$ and $40\mu\text{m}$ are chosen for $W1$, $G1$, $W2$, and $G2$ respectively, in order to realize a 71Ω and 50Ω FGC waveguide line on alumina. Figure 4.9(a) illustrates the power divider with two Vishay 0402 thin film resistors and has a total area of 0.065cm^2 . The resistors consist of NiCr deposited on high performance 99.5% Alumina substrates with a temperature coefficient of resistance (TCR) of $\pm 50\text{ppm}/^\circ\text{C}$. Gold wrap-around parts on either end of the chip resistors are mounted with the resistor facing upward to allow for silver epoxy application and gold wire bonding. Fabricated thin film resistors (TFRs) can be easily integrated with the 5-mask fabrication process to obtain a fully monolithic power divider. Initially, isolation TFRs were designed and tested with the use of Cr and TiW for the Wilkinson power divider. 200\AA e-beam Cr and 340\AA sputtered TiW layers were examined for use as the resistive material. Standard four-probe sheet resistivity measurements are performed on the two deposited materials to obtain $64\Omega/\text{sq}$ and $32\Omega/\text{sq}$ for Cr and TiW respectively. Varying width resistors were then designed on FGC lines to obtain resistances of 50Ω and 100Ω for matched load and isolation resistors, respectively. However, due to the high TCRs of Cr and TiW, the

resistances values were found to vary after placing the wafer through the multi-layer process with several high temperature cycles, proving unreliable for use in designing these power dividers. More temperature stable materials such as NiCr or TaN with lower TCR values are recommended for use in designing Wilkinson power dividers. Details on the characterization and process of producing TFRs can be found in Appendix B.

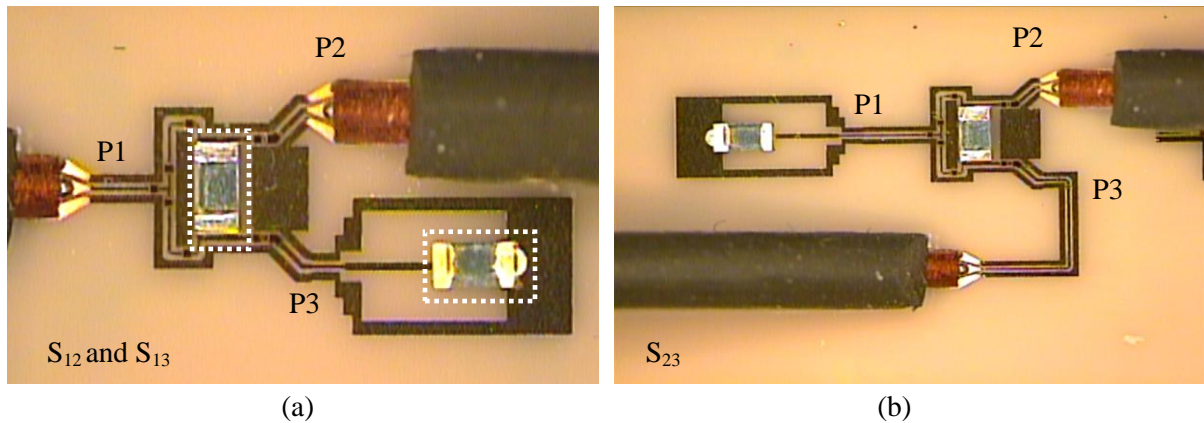


Figure 4.9: Fabricated equal-split two-way Wilkinson power dividers. (a) The first layout is for measuring the power divider's insertion loss and return loss. (b) The second layout is for measuring the power divider's isolation at the output ports.

Since the network analyzer is a two port system, several layouts of the Wilkinson power divider are fabricated. The first layout in Figure 4.9(a) is for measuring the power divider's insertion loss and return loss, where one resistor serves as the isolation resistor, and the second layout is used to terminate one of the output ports and allow for a two-port measurement at ports 2 and 3 (S_{12} and S_{13}). In Figure 4.9(b), the matching load is placed at the input port P1 for the isolation measurement (S_{23}).

4.3.2 Results

The measured response is fairly similar to the simulated response, where most of the losses can be sourced directly to the FGC conductor losses and hybrid resistor assembly. Insertion loss is

about 0.3dB at port 2 and 0.5dB at port 3, and the isolation is better than 15dB over the X-band. The return loss is found to be better than 20dB, and a flat 3-way equal power-split property is achieved over the bandwidth of interest. Its power-split amplitude imbalance is less than 0.2dB and the bandwidth nearly 13%.

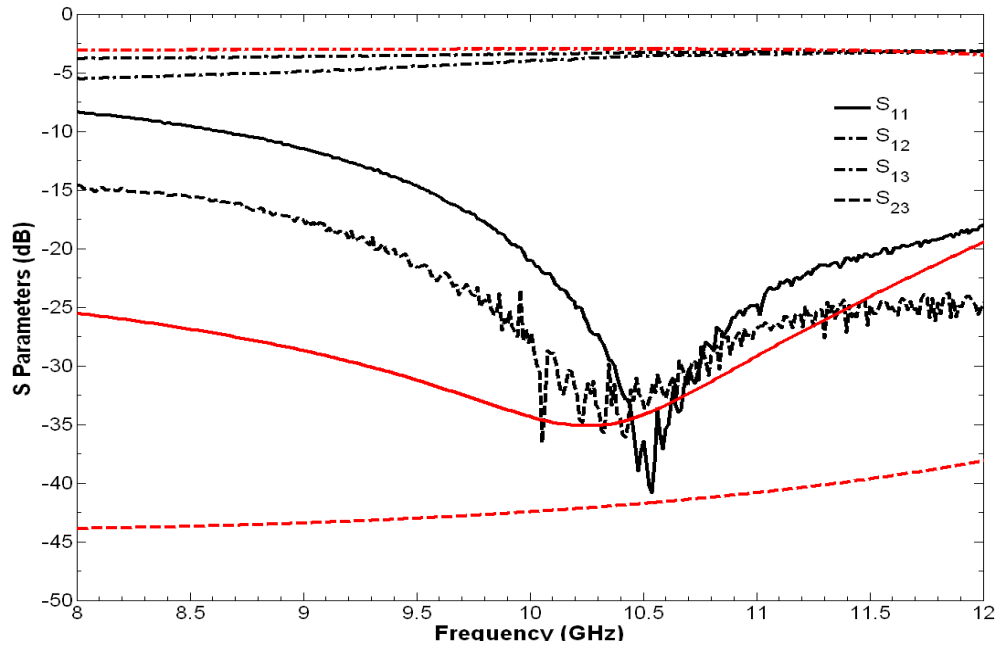


Figure 4.10: Comparison between simulated and measured response of the two-way Wilkinson power divider.

The Wilkinson's power divider has a low Voltage Standing Wave Ratio (VSWR) at all ports and high isolation between output ports. This planar power divider configuration can easily be implemented in the modular concept of the proposed ESA unit.

4.4 Capacitive Coupled Interconnect

The monolithic integration of the RF MEMS phase shifter with the power divider involves the implementation of an interconnect network compliant to the 5-mask fabrication process used to produce the capacitive switches described earlier. Since the phase shifter and switches are fabricated on the wafer's front side, high isolation crossovers can be implemented on the backside without the

loss of wafer estate. The interconnect proposed here is an electromagnetically-coupled junction designed and presented in [55]. Using the novel compact interconnect proposed eliminates the need for a multilayer manufacturing process and provides excellent RF performance. The interconnects are integrated monolithically with the rest of the ESA module onto a single chip.

4.4.1 Design

The interconnects are designed also using FGC waveguide lines, maintaining uniformity with the rest of the ESA components. The major advantage of the FGC waveguide is that its lowest surface mode is TE_0 , therefore leakage and coupling occurs at much higher frequencies compared to that of the infinite ground CPW line [55]. This is important to minimize the amount of unwanted coupling and crosstalk for overlapping circuits processed on opposing sides of the wafer. An additional advantage of this design is that it eliminates the need for interconnect vias, thereby simplifying the fabrication process, increasing reliability and repeatability, and avoiding fabrication errors such as blind vias and shorts. The layout of a dual-path interconnect is shown in Figure 4.11 and has a total circuit area of 0.15cm^2 .

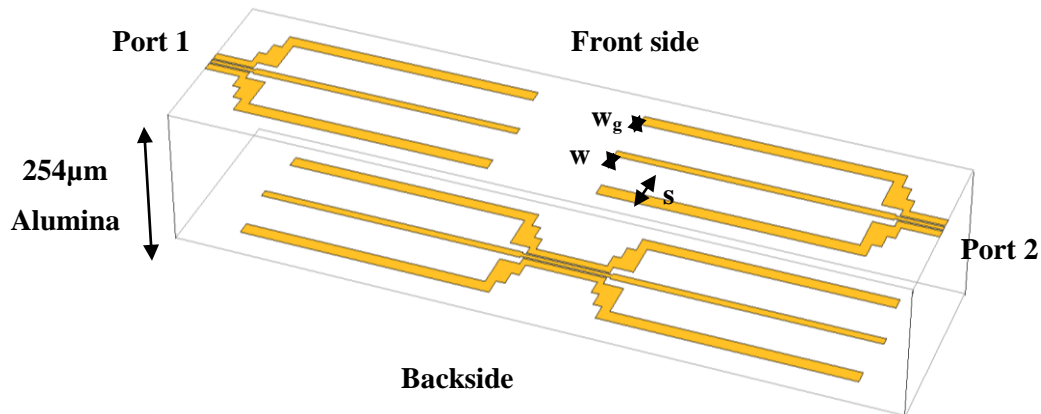


Figure 4.11: Layout of a dual-path EM interconnect with a total circuit area of 0.15cm^2 .

It consists of two superimposed FGC waveguide lines at either side of the substrate where electromagnetic coupling transfers the RF signal from one side to the other. The overlapping area of the two lines is set to a quarter wavelength to produce a pass band where the even and odd

impedances are perfectly matched. The wafer thickness is chosen to be 254 μm and the signal line width and ground line width is 224 μm and 184 μm , respectively. In addition to the substrate thickness, the spacing S between the signal line and ground line also controls the coupling and is set to 550 μm . The vertical CPW coupled interconnects are matched to a 50 Ω FGC line via a stepped optimized junction [55].

4.4.2 Results

Figure 4.12 illustrates a comparison of the simulated and measured results obtained for the dual-path EM interconnect. A full wave analysis using Sonnet is performed to optimize the interconnects' performance, and a two port on-wafer probe measurement is performed to evaluate the interconnect performance over X-band. Measured results indicate a return loss of better than 20dB over the frequency range of 9GHz to 11GHz. The insertion loss of the lines is approximately 0.62dB, which leads to the conclusion that each vertical transition contributes about 0.31dB in loss. Losses can be due to the conductor losses, any parasitic radiation present as well as front side misalignment with the backside layer during fabrication. The bandwidth is almost 1GHz.

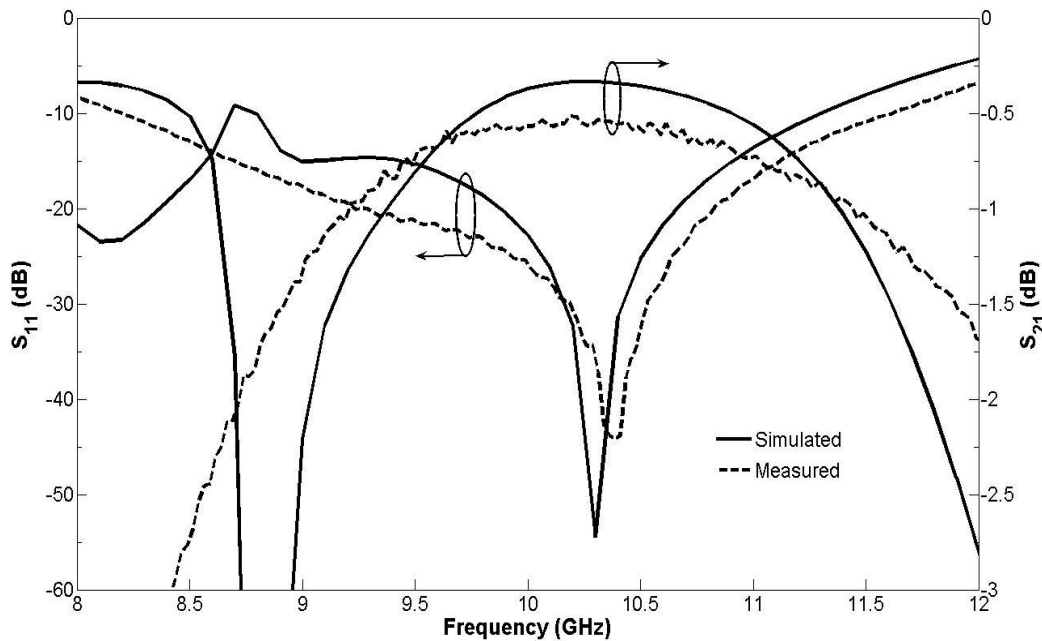


Figure 4.12: Comparison between the simulated and measured results for the dual-path interconnects.

This design is very versatile and can be easily tuned to the frequency of interest by adjusting the overlapping area. Therefore, by laser trimming the underlying lines in length, the overlapping area is reduced thereby increasing the frequency of operation.

4.5 FGC 4 x 4 Butler Matrix

The Butler Matrix (BM) is investigated as an alternative to the phase shifting method proposed in earlier sections. A compact 4 x 4 BM consisting of meandered FGC waveguide branch-line couplers is presented. The following sections entail the design and fabrication of the 4 x 4 integrated MEMS BFN and its constituting components designed to operate over the Ku-band. In order to minimize the space occupied by the passive network and simplify its fabrication and design, a biplanar topology using folded FGC waveguide lines has been chosen. The folded FGC waveguide lines implemented in the matrix design allow for high-density integration. The two designs propose the use of polyimide and gold air bridges for crossover design in a MEMS compatible process to fabricate the Butler matrix monolithically onto one substrate. This compact BFN network is then integrated in Chapter 5 with a monolithic SP4T capacitive MEMS switch to produce a MEMS-tunable BFN. This enables the user to switch from one input port to the next, or to select more than one port at a time. The proper input of each input port is chosen using digitally controlled MEMS SP4T switches, introduced in Chapter 3. One advantage of this system is that it is passive and thus preserves the system dynamic range and does not cause any gain instability [56].

4.5.1 Design

The BM is a microwave network normally employed in BFNs and scanning networks for linear and circular arrays. The matrix components including the directional 90° hybrids, crossover lines and fixed phase shifters are designed using a modular approach. Each component is optimized separately and implemented using FGCs. They are then integrated to form the final 4 x 4 BM. FGC waveguide lines are chosen for the design of the BM because of their many advantages including balanced signal propagation, ease of fabrication and lower losses. Another main advantage of FGC

lines is that they do not support parallel-plate modes, thus eliminating the need for via-holes between upper and lower ground planes reducing radiation loss [57].

The 90° hybrid takes up over 50% of the area in a BM, so a significant reduction of the hybrid can result in a significant reduction in the overall BM size [58]. Hybrid couplers have been reduced in area using lumped elements [59] resulting in narrower bandwidths, and high impedance transmission lines with shunt stubs [60] that are difficult to realize using FGC lines. In this design, the hybrid coupler area is reduced by 50% via folded FGC lines shown in Figure 4.13. The EM simulated response is given in Figure 4.13. The meandered lines that form the 45° fixed-delay phase shifters are also simulated and optimized. The best performance for the mitered bend was obtained for a mitering of 60% with a return loss less than 30dB.

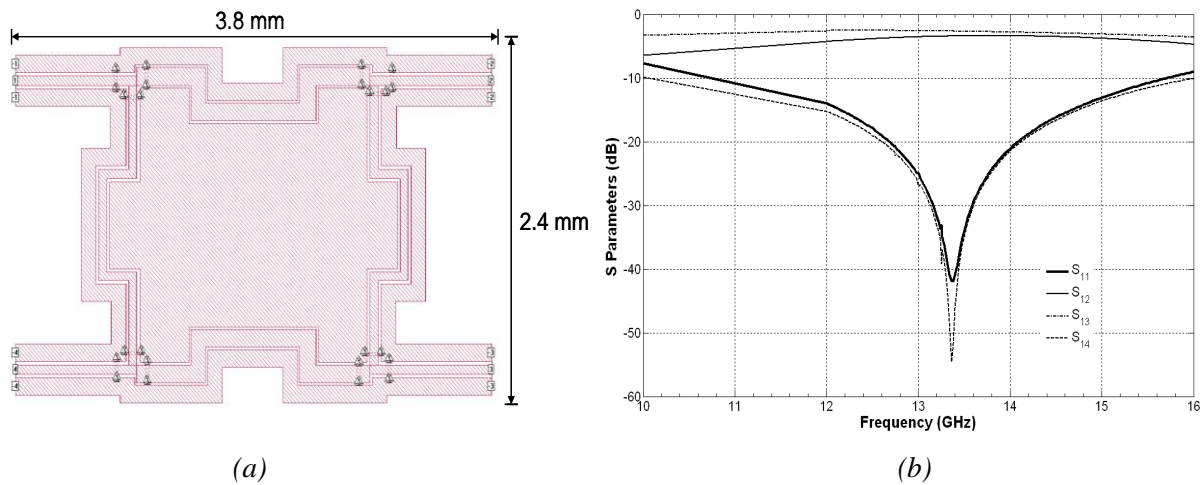


Figure 4.13: (a) The FG-CPW folded coupler and (b) the EM simulated response [74].

Line crossovers are one of the main obstacles in designing the Butler matrix and can lead to increased insertion loss, mismatched junctions, additional line cross couplings and poor power handling [61]. There are several techniques available in designing crossover lines including:-

- Coupler doubling design. In [24], two hybrid couplers are connected in cascade to work as a crossover. The resulting element is rather big however the structure's symmetry is maintained.

- Coupled two-layer design. A non-planar strip requires an expensive laminate and an aperture through which the signal is coupled leading to alignment difficulties [23].
- Non-planar design. A crossover using an air bridge or dielectric transition between the Butler matrix elements [62].

It is desirable to design a crossover that has good return loss and isolation. Since the isolation is directly dependent on the mutual capacitive coupling, it can only be increased by narrowing the overlapping strips or varying the dielectric layer thickness if adjustable. The 4 x 4 BM is constructed by linking four of the folded hybrids presented earlier, two mitered 45° delay lines and crossover lines. Primarily, the crossover lines are realized by evaporating a gold layer under the polyimide, which serves as an isolation layer, as shown in Figure 4.14. The HD Microsystems PI-2611 [63] average dielectric constant is measured as 3.34 at 1MHz and a loss tangent of 0.002 measured at 1kHz [52]. Appendix A has a detailed description of the electrical characterization of PI-2611 and the process developed to pattern this polyimide. The polyimide thickness is varied between 6µm to 18µm to minimize coupling between the crossover lines and reduce insertion loss. Simulated results show a return loss of less than 20dB and isolation better than 35dB for a polyimide thickness of 18µm, as illustrated in Figure 4.15.

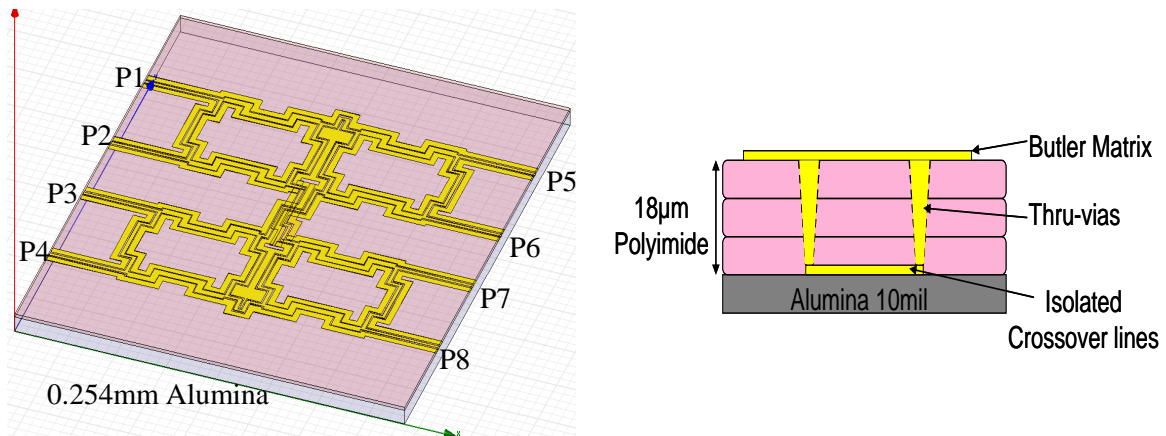


Figure 4.14: Proposed 4 x 4 Butler matrix layout and cross section [74].

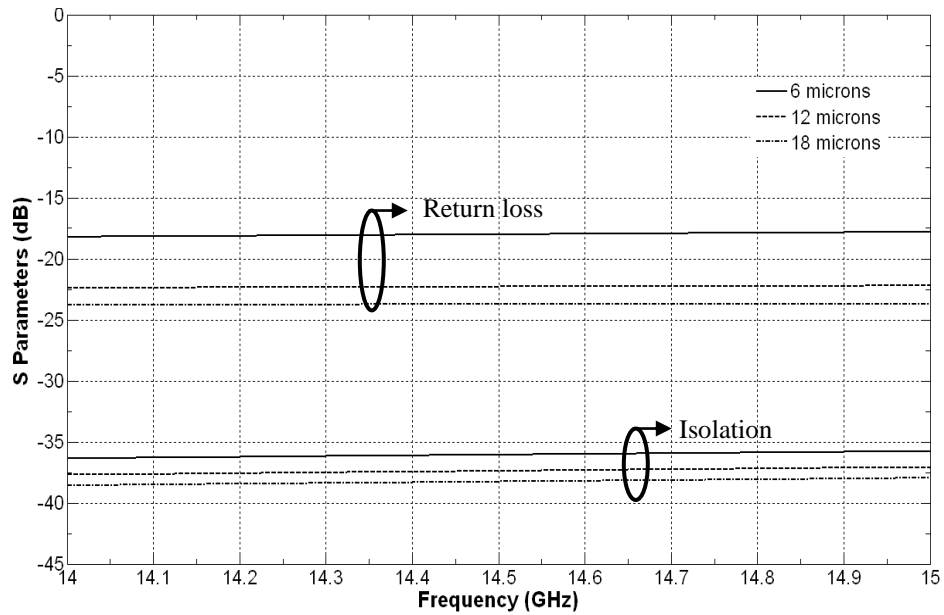


Figure 4.15: Crossover lines return loss and isolation as a function of polyimide thickness [74].

In order to develop a prototype that integrates the BM with the SP4T switch monolithically without re-characterizing the SP4T performance, a second BM with a different set of crossover lines is developed using gold air bridges. A complete layout of the 4 x 4 Butler matrix is shown in Figure 4.16. The overall size of the beam-forming network is 0.49cm^2 . The air bridge crossover lines are realized by evaporating a gold layer over the sacrificial photoresist and released with the switches, as shown the cross section in Figure 4.16. Air bridges are also included at all the discontinuities and bends in the design to suppress the unwanted coupled slotline modes excited at discontinuities.

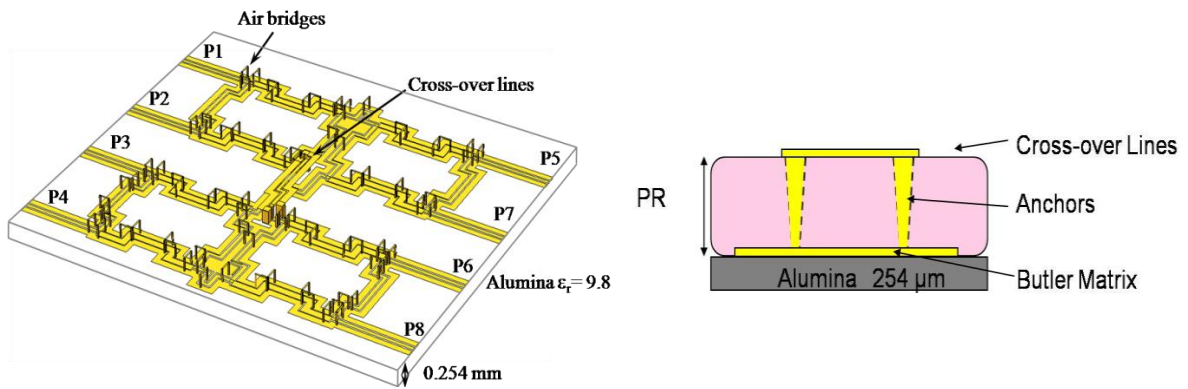


Figure 4.16: 4 x 4 Butler matrix layout and cross-section.

The bridge crossover designed is shown in Figure 4.17(a) and is optimized in terms of isolation, coupling and input reflection coefficient. FGC crossover junctions have approximately 15dB lower coupling than CPW crossover junctions and do not excite the parasitic slotline mode [13]. This represents another advantage of using FGCs for this structure. Simulation results in Figure 4.17(b) reveal an almost constant performance over the design frequency band with cross coupling less 25dB and an insertion loss of 0.412dB.

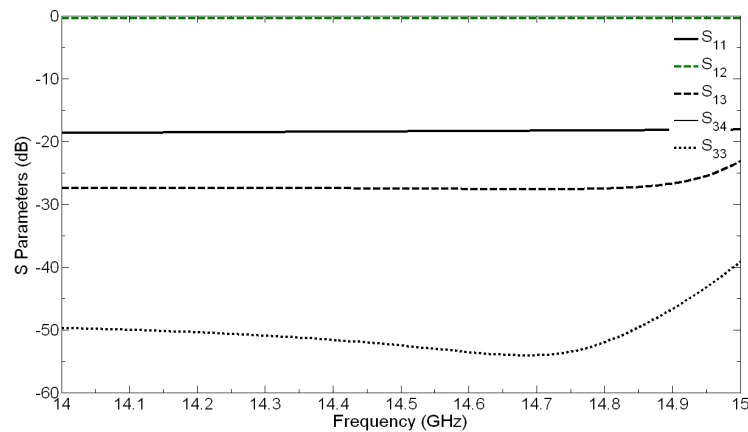
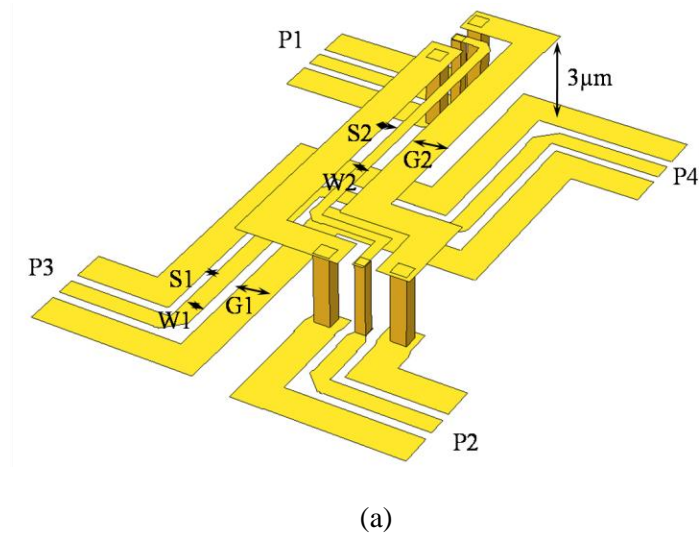


Figure 4.17: (a) The layout of the FGC bridge crossover bridge in Sonnet and (b) the simulated EM response. The overlapping FGC air bridge lines (S2, W2, G2) are at an impedance slightly higher than that of (S1, W1, G1) to improve matching and reduce reflections.

4.5.2 Fabrication Process

The fabrication process of the 4 x 4 Butler matrix starts with a 10mil thick, highly polished alumina wafer. The process steps are outlined in Figure 4.18.

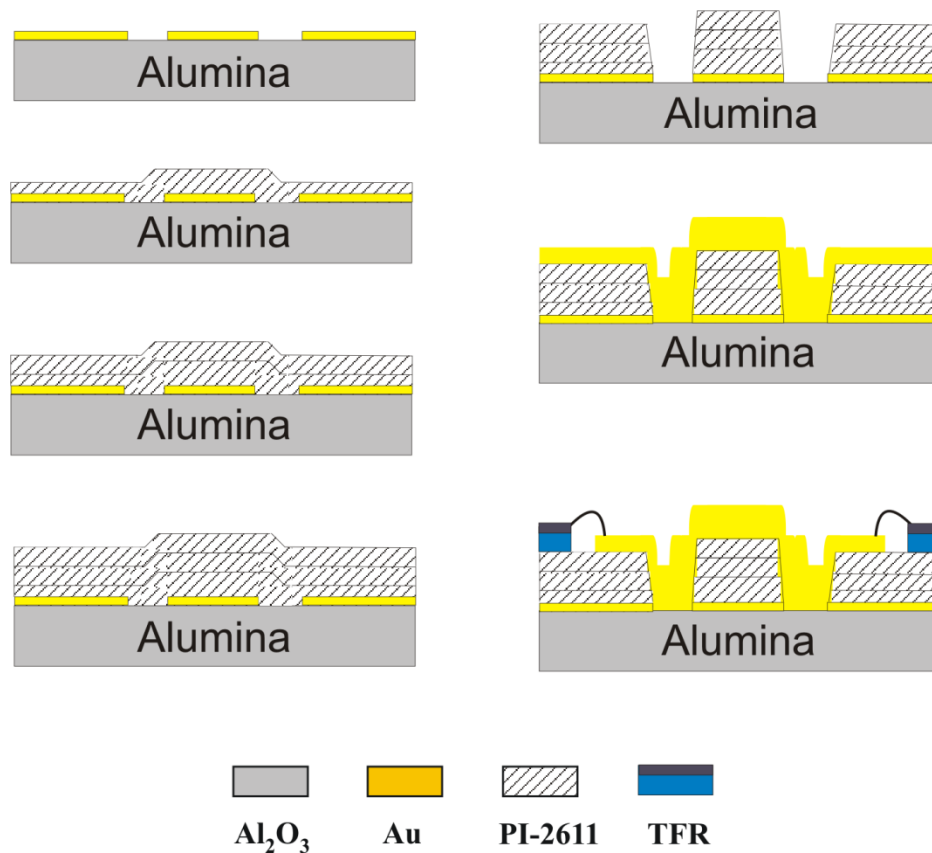


Figure 4.18: 4 x 4 polyimide-integrated Butler matrix fabrication process.

The alumina substrate is cleaned in a standard RCA solution for 15 min at 70°C prior to processing. The crossover lines are deposited with e-beam evaporation where 400Å of chromium is used as an adhesion layer between the 1µm of gold and the alumina wafer. The Cr/Au crossover lines are then patterned and etched using iodine and 40% diluted ceric ammonium nitrate based solutions, respectively. HD Microsystems Polyimide PI-2611 is then spun to a thickness of 6µm and cured for 3 hours to bake out any present solvents. Adhesion promoter is spun on between the multiple layers of polyimide in order to enhance the layers adhesion to each other. Aluminum is then deposited using

DC sputtering to a thickness of $0.5\mu\text{m}$, used as a metal mask for etching the polyimide. The three-layer $18\mu\text{m}$ thick polyimide is then etched using a pure oxygen plasma recipe developed at CIRFE labs. Low pressure of 10mtorr with low ICP power is used to achieve highly anisotropic via wall profiles. The vias have a total area of $25 \times 25\mu\text{m}^2$.

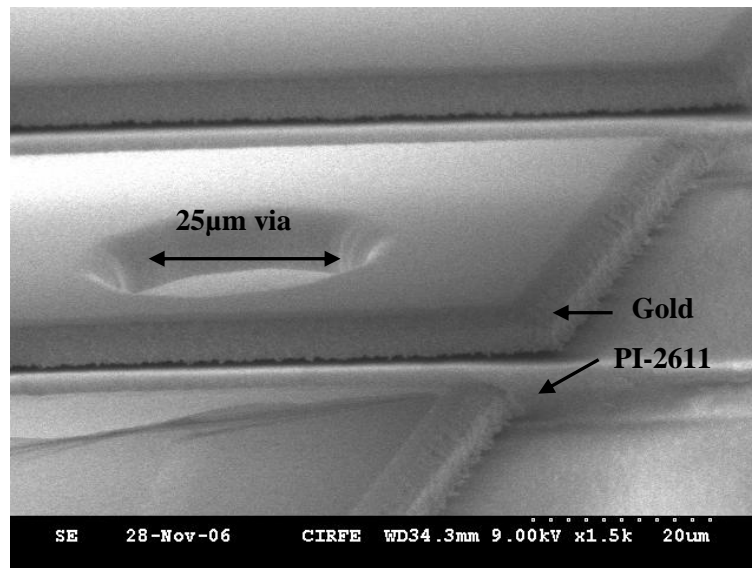


Figure 4.19: SEM of the Butler Matrix's etched via profile. The vias have a total area of $25 \times 25\mu\text{m}^2$.

In relatively deep vias, the problem in polyimide etch is the residue at the bottom, typically as a result of re-deposited sputtered metal present on the circuit or mask. One of the most important requirements is excellent etching selectivity between polyimide and the mask. Aluminum is used as an etch mask because it was found to produce the least amount of residual grass during the plasma etch, is economically feasible and easy to pattern and etch. Gas flow of 4sccm of CF_4 is added in the last 60 seconds of the etching process to remove any remnant etch residue. A captured SEM image of a via wall profile is shown in Figure 4.19. The etch recipe produces smooth anisotropic sidewalls with good sidewall coverage achieved. A warmed up Phosphoric – Acetic – Nitric (PAN) solution mixture is used to etch off the aluminum metal mask. The polyimide is then placed in the furnace at 150°C for an hour-long dehydration bake. The polyimide surface is then roughened in oxygen plasma for 50seconds to enhance gold adhesion. A second layer of gold is then evaporated, electroplated, patterned and etched to form the top passive BFN. More information on process details and optimization is given in Appendix B.

It is necessary to choose an inter-dielectric that is thermally stable at a given temperature. Thermal stability for an interlayer needs to be in excess of the temperatures to be encountered during subsequent processing steps of fabrication of the multilayer structure. Polyimides exhibit high thermal stability and are stable up to 400°C. Moreover, PI2611 is specifically chosen because it is characteristically lower stress than the other line of polyimides provided by HD Microsystems. Moreover, film adhesion is very sensitive to surface preparation. The use of a chromium layer and an oxygen plasma “roughening” recipe has proven to be effective in improving interlayer adhesion. Bake out cycles are employed during the fabrication of the multilayer circuit due to polyimide that exhibits significant moisture absorption. Since alumina has a high dielectric constant, dielectric layers such as polyimide can be used on top of alumina substrate to create an interface layer that can host wider bandwidth.

For the integrated Butler matrix with gold air bridges for crossovers, the fabrication process of the switched BFN is based on the same five-mask process developed at CIRFE labs in [14]. Starting with a 254 μm thick alumina wafer, the first gold layer defining the majority of the circuit is first deposited, patterned and etched. Next, an 1800 \AA silicon nitride layer (Si_3N_4) is PECVD deposited and patterned over the switch electrode area and under the air bridges for isolation. In Figure 4.20(c), the sacrificial layer is then spun cast to a thickness of 3 μm . The sacrificial layer is hard baked at 120°C for four minutes to ensure positive sidewalls for good metal anchor coverage. The MEMS switches, air bridges and crossover lines are then fabricated by depositing a thin seed layer of 2000 \AA of Au, and by electroplating it up to 1 μm . The electroplated gold layer is then patterned and etched. The crossover lines are anchored via square anchors with a total area of 25 x 25 μm^2 , as shown in Figure 4.21. Gold air bridges are used to connect all ground planes within the vicinity of a discontinuity or junction. Moreover, during the assembly of the network, three of the four output ports that are not in use during testing are terminated with 50 Ω Vishay thin film resistor loads using gold wire bonds and silver epoxy. As a result, the network is measured and characterized as a two-port network.

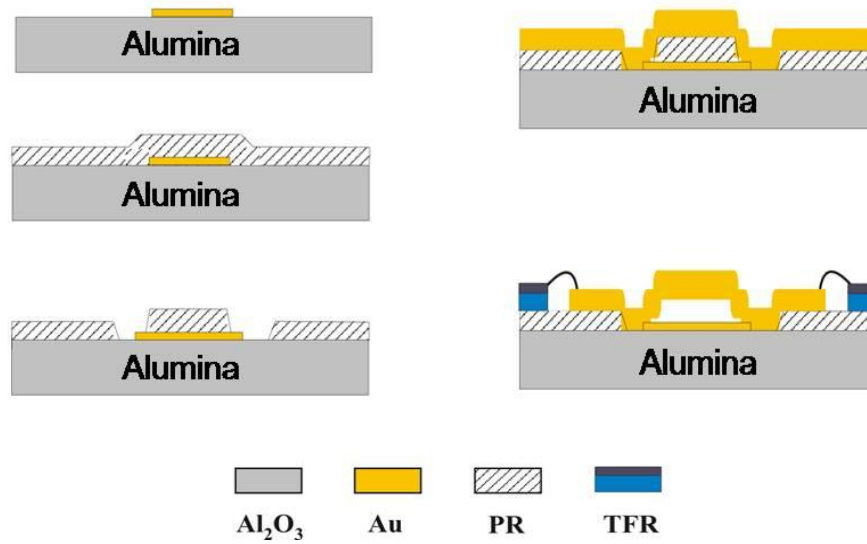


Figure 4.20: 5-mask fabrication process of the 4 x 4 MEMS integrated Butler matrix circuit.

The crossover lines are fabricated in conjunction with the switches to be released as air bridges. A captured SEM image is shown in Figure 4.21 of the released crossover lines. The crossover lines were anchored down with 25 μm square anchors. One of the advantages of this monolithic design is that the crossovers can be packaged simultaneously along with the MEMS switches within the same process. However, a disadvantage is the slight warping the crossover lines can experience due to intrinsic stresses.

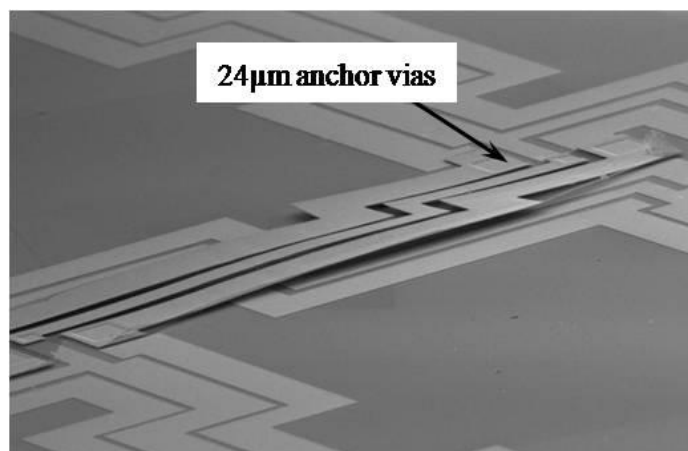


Figure 4.21: SEM image of the crossover lines suspended 3 μm above the wafer.

4.5.3 Results

The polyimide-based folded FGC fabricated Butler matrix is presented in Figure 4.22 and has been reported in [74]. Gold wire bonds are used to connect all ground planes within the vicinity of a discontinuity or junction to suppress any unwanted CPW line modes. Moreover, during the assembly of the network, six of eight input and output ports that are not in use during testing and measurement, are terminated with hybrid 50 Ω thin film resistor loads. As a result, the network is measured and characterized as a two-port network.

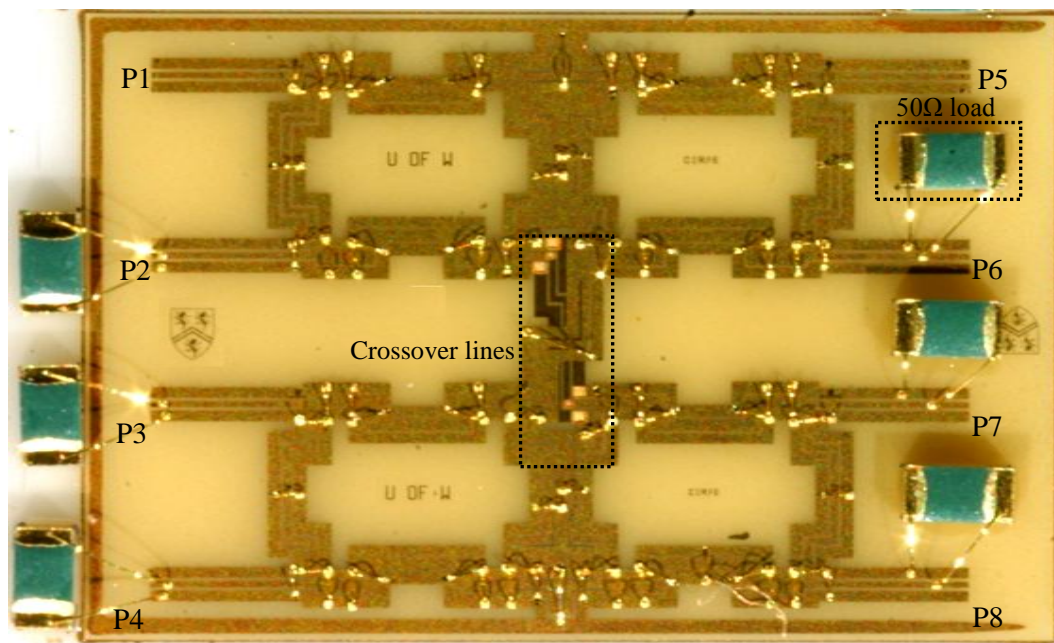
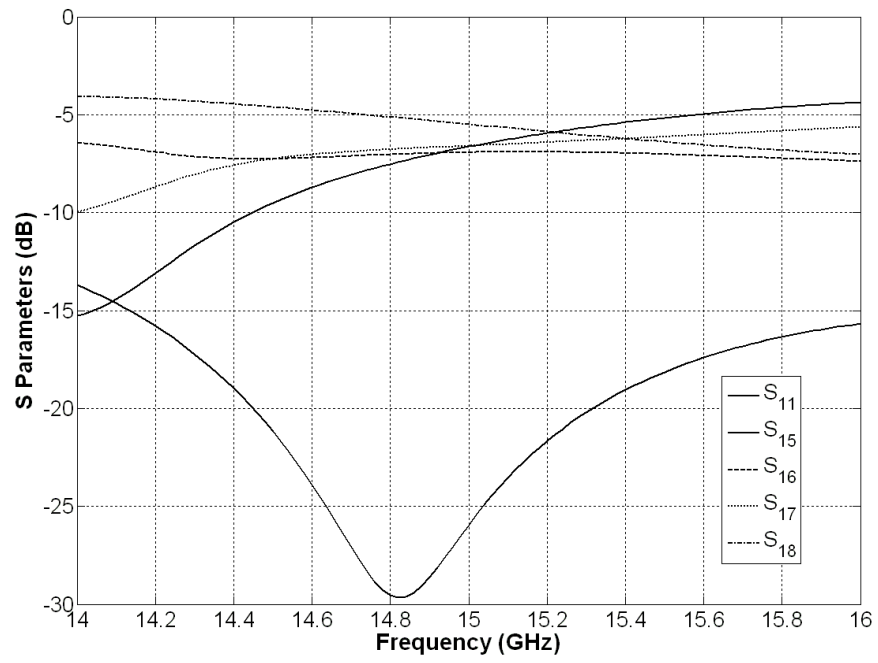
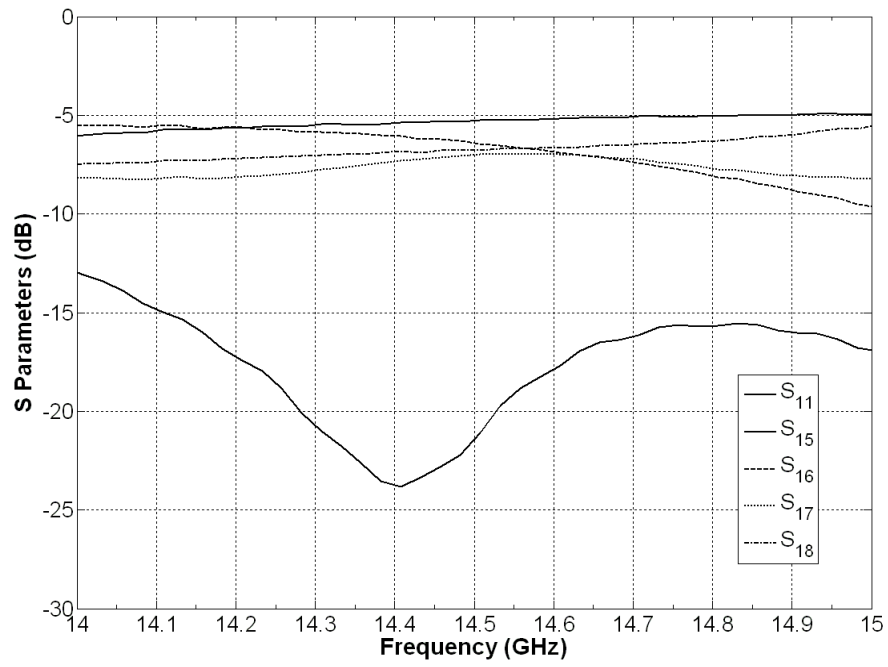


Figure 4.22: Fabricated Butler matrix with hybrid integrated thin film resistors.

The simulated and measured magnitude and phase results are shown in Figure 4.23. The output ports measure close to -6dB with magnitude errors of about ± 1.5 dB. The operational bandwidth is about 400MHz. The differences between measurement and simulation can be attributed to inaccuracies in bond-wire, dielectric and conductor modeling and fabrication tolerances.

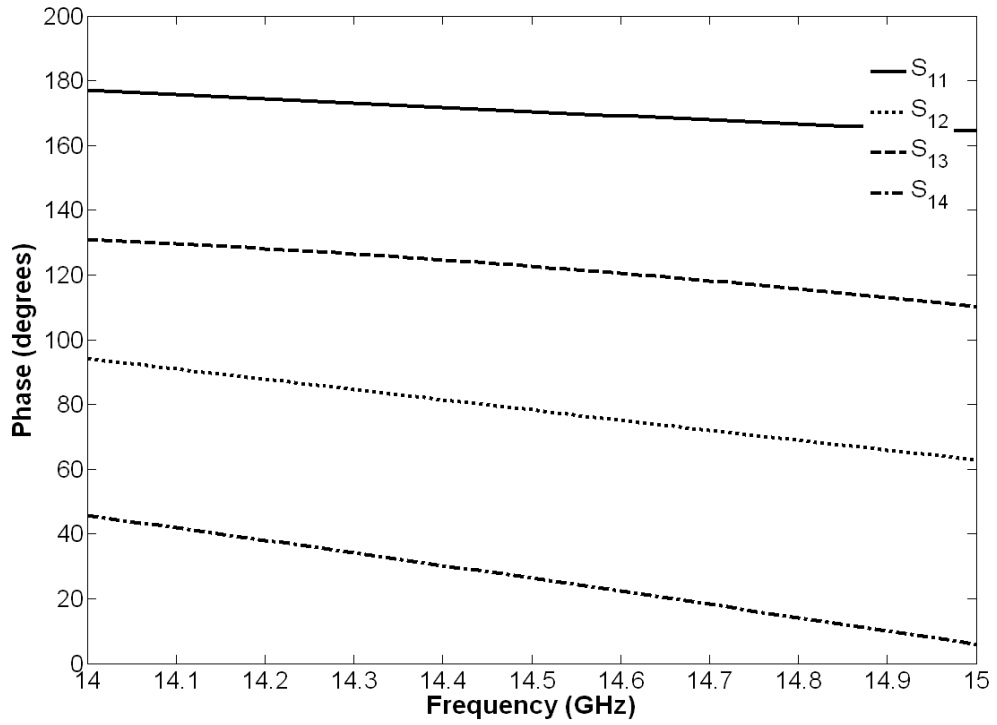


(a)

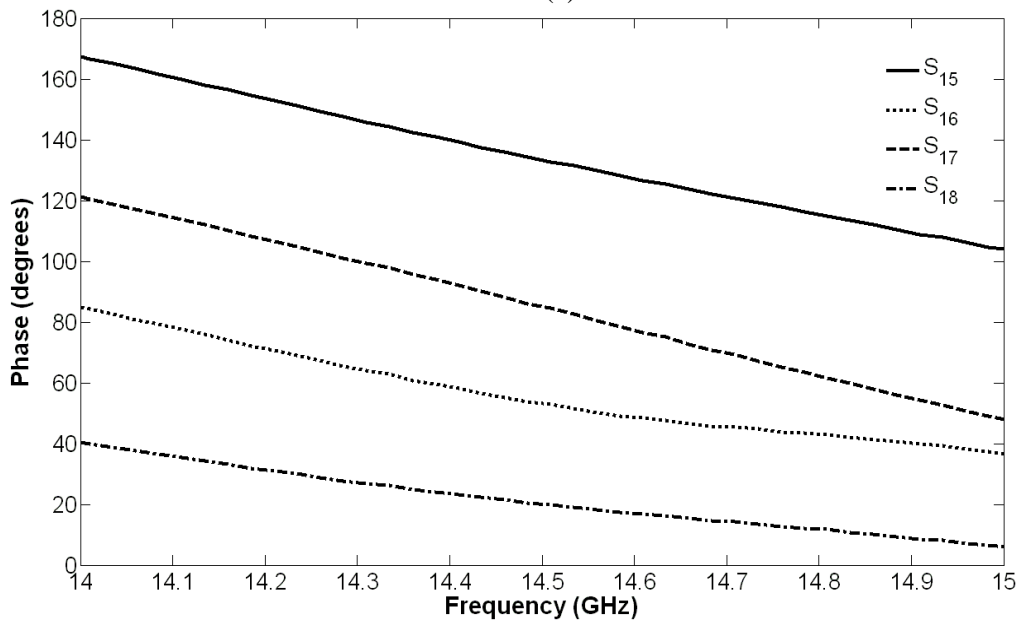


(b)

Figure 4.23: Comparison of the polyimide-integrated S-parameter results. (a) Simulated S-parameters. (b) Measured S-parameters.



(a)



(b)

Figure 4.24: Comparison of the polyimide-integrated BM phase results. (a) Simulated phase. (b) Measured phase.

The folded FGC fabricated BM is presented in Figure 4.25. Similarly, gold wire bonds are used to connect all ground planes within the vicinity of a discontinuity or junction to suppress any unwanted CPW line modes.

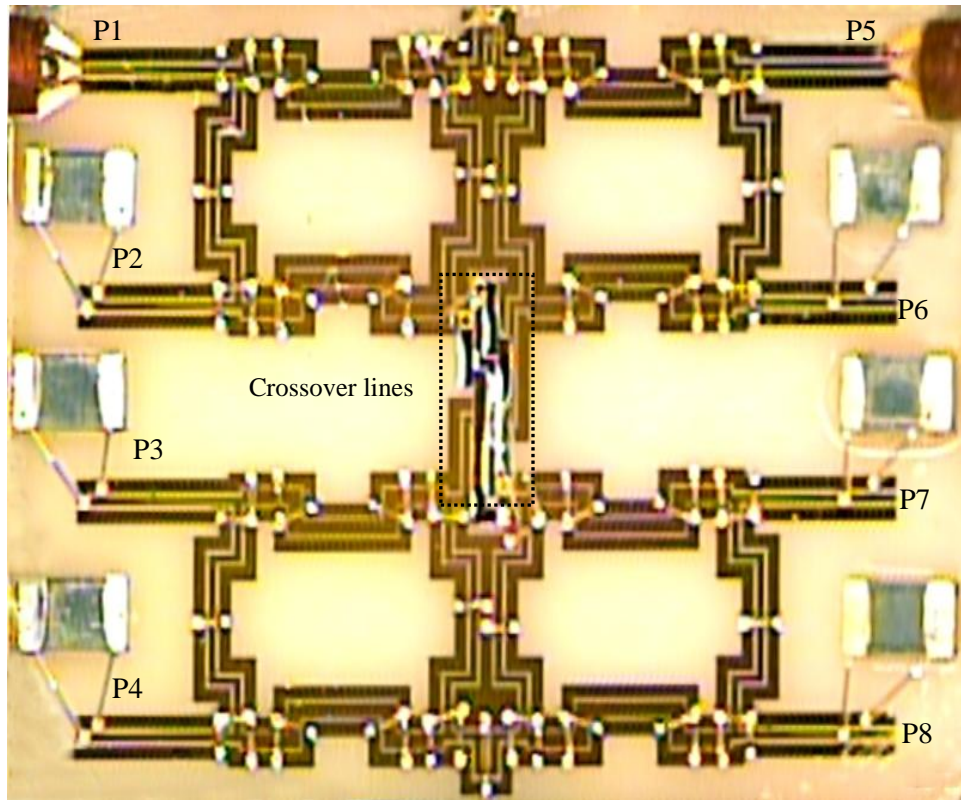


Figure 4.25: Fabricated Butler matrix with gold air bridge crossovers.

The measured RF performance of the 4 x 4 fabricated Butler matrix with gold air bridge crossovers are shown in Figure 4.26 and Figure 4.27. The output ports measure close to -6dB with magnitude errors of approximately ± 1.65 dB and phase errors of 12° . The operational bandwidth is about 280MHz.

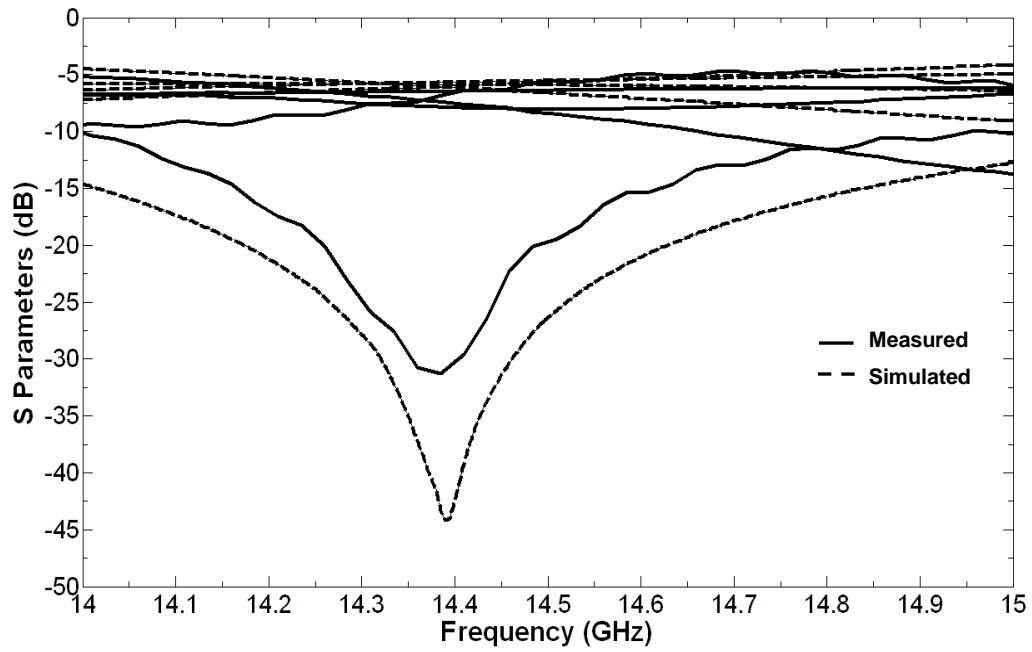


Figure 4.26: 4 x 4 Butler matrix simulated (dashed line) measured (solid line) return loss and insertion loss when input is at Port 1.

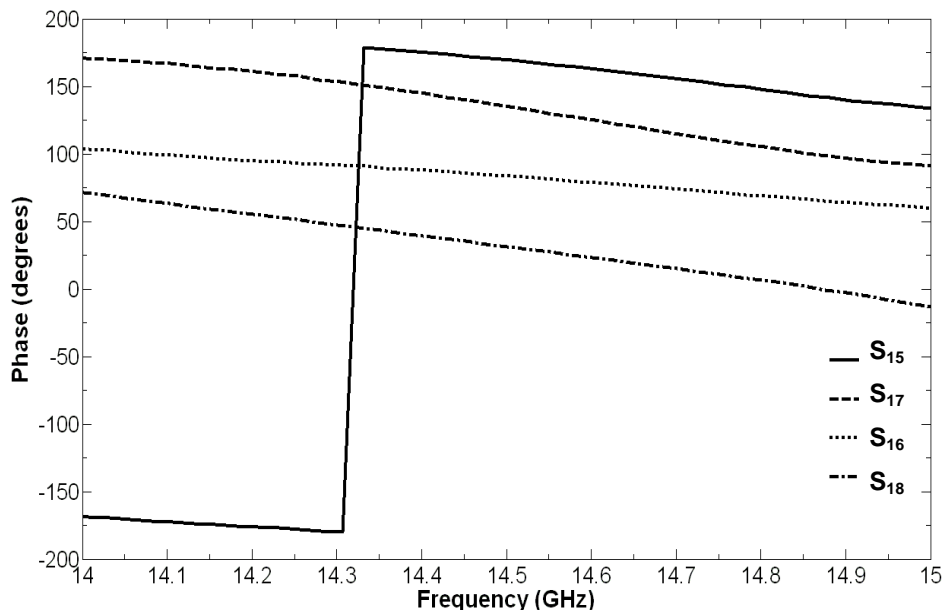


Figure 4.27: 4 x 4 Butler matrix measured phase response.

The phase variation can be attributed to fabrication errors and tolerances of the air bridges, where the realized crossover lines air gap may be larger than the $3\mu\text{m}$ they were originally designed at and experience slight warping due to intrinsic stress. Moreover, the performance of this integrated Butler matrix has a narrower bandwidth than that of the polyimide due to the high dielectric constant of alumina.

In summary, a compact folded 4×4 Butler matrix has been designed and tested. This BFN is made compact using folded FGC lines and is monolithically integrated into one substrate with the use of a thick polyimide inter-dielectric layer. The proposed matrix with a footprint of only around 0.46cm^2 demonstrates a great potential for all-planar integration of switched BFN network is also integrated with the use of gold air bridges for crossover lines, a process amenable to the 5-mask MEMS fabrication process. Using gold air bridges is a space-effective method for producing small Butler matrices despite the phase errors and insertion losses they introduce.

Chapter 5

MEMS Integrated Phase Shifter Modules

5.1 Introduction

The main components of the ESA include the antenna elements, the phase shifters, the feed network and the T/R module. While improving the RF performance of the components is important for the next generation ESAs, the tight integration of these components will enable radar to extend their functionality and ubiquity. By employing wafer-scale heterogeneous integration, these sub-array building blocks may be combined to form arbitrarily large arrays with no sacrifice in system performance. The optimum level of integration is usually a trade-off between component yield versus packaging and assembly complexity. Multilayer substrates are attractive for areas with a high density of interconnections to minimize the packaging area needed and coupling between microwave and control signals. Co-fired ceramic (HTCC), low-temperature (LTCC), or thin-film packaging can be used as a multilayer substrate. HTCC is generally considered the lowest cost of these technologies but will have more insertion loss than LTCC or thin film. The thick film conductors used in HTCC provide lower line resolution than thin-film materials and are difficult to process [64]. The low costs of LTCC and the ability to stack multiple layers are both attractive features. However, the drawbacks of this material are significant and include poor thermal conductivity and shrinkage variance larger than contact pad and via holes sizes. Moreover, HTCC or LTCC circuits are not amenable to monolithic integration with MEMS phase shifters and their application is limited only to hybrid integration.

The Defense Advanced Research Agency (DARPA) Microsystems Technology Office (MTO) is driving development of integration techniques at the module level with a program called SMART that was initiated in 2006 [65]. This program is focused on developing integrated, multi-layer modules for three-dimensionally integrated surface-emitting panels. The challenges faced fall into three categories including mechanical integrity, electrical integrity and thermal management. Mechanical challenges result from the integration of multiple layers with different functions within a single stack, including incorporation of high-frequency active devices, wafer-to-wafer alignment and

resolving coefficient of thermal expansion mismatches between the layers. Electrical challenges include making reliable and low-loss vertical interconnects at high interconnect density while maintaining good isolation and thermal management including reduction of DC power consumption and heat removal. Our proposed integration technique proposes solutions to circumvent some of these challenges.

5.2 Integrated Electronically Scanned Phase Shifter Module

A highly integrated passive ESA module using an innovative tile construction integration approach with MEMS processing technologies is presented. X-band monolithic 3-bit MEMS phase shifters, Wilkinson power dividers and via-less capacitive interconnects are integrated on a double-sided wafer to produce a prototype module that can be easily extended to construct a sub-array (tile) on a single substrate. The 2.2cm² integrated module has a bandwidth of 11% and is an enabling building block of integrated sub-system arrays for lightweight large space borne phased arrays. This novel integration concept offers high yield and low cost batch fabrication as well as low packaging and assembly complexity.

5.2.1 Design

The design of the integrated MEMS module is approached in two stages. The initial stage involves the individual design, fabrication and characterization of the different components in the module including the MEMS phase shifter, power divider and vertical via-less interconnect, all presented in detail in Chapters 3 and 4. The 3-bit switched-line phase shifter employs the dual warped-beam capacitive MEMS shunt switches presented in Chapter 3. The power divider is a Wilkinson power divider that distributes the power to the sub-array module elements presented in Chapter 4. FGCs are used as the transmission line type for all of the components in the module to eliminate the need for ground planes or vias when transitioning from one layer to the next. Two layouts were designed when fabricating these devices: one layout contained all the components disconnected to allow for the separate and accurate characterization of each device, as illustrated in Figure 5.1(a). Access is provided for the input and output ports of all three components: the phase shifter PS1 and PS2, the power divider PDR1 and PDR2 and the interconnect IC1 and IC2. Once the

components are optimized, they are then integrated using MEMS processing and vertical capacitive interconnects as illustrated in Figure 5.1(b). The vertically interconnected unit module consists of the input port P1 printed on the front side of the wafer. The signal is then coupled through an interconnect to the wafer's backside and is split halfway in power through the Wilkinson power divider. The signal then returns to the front side of the substrate through a second capacitive interconnect to the input of the phase shifter, finally exiting at port P2.

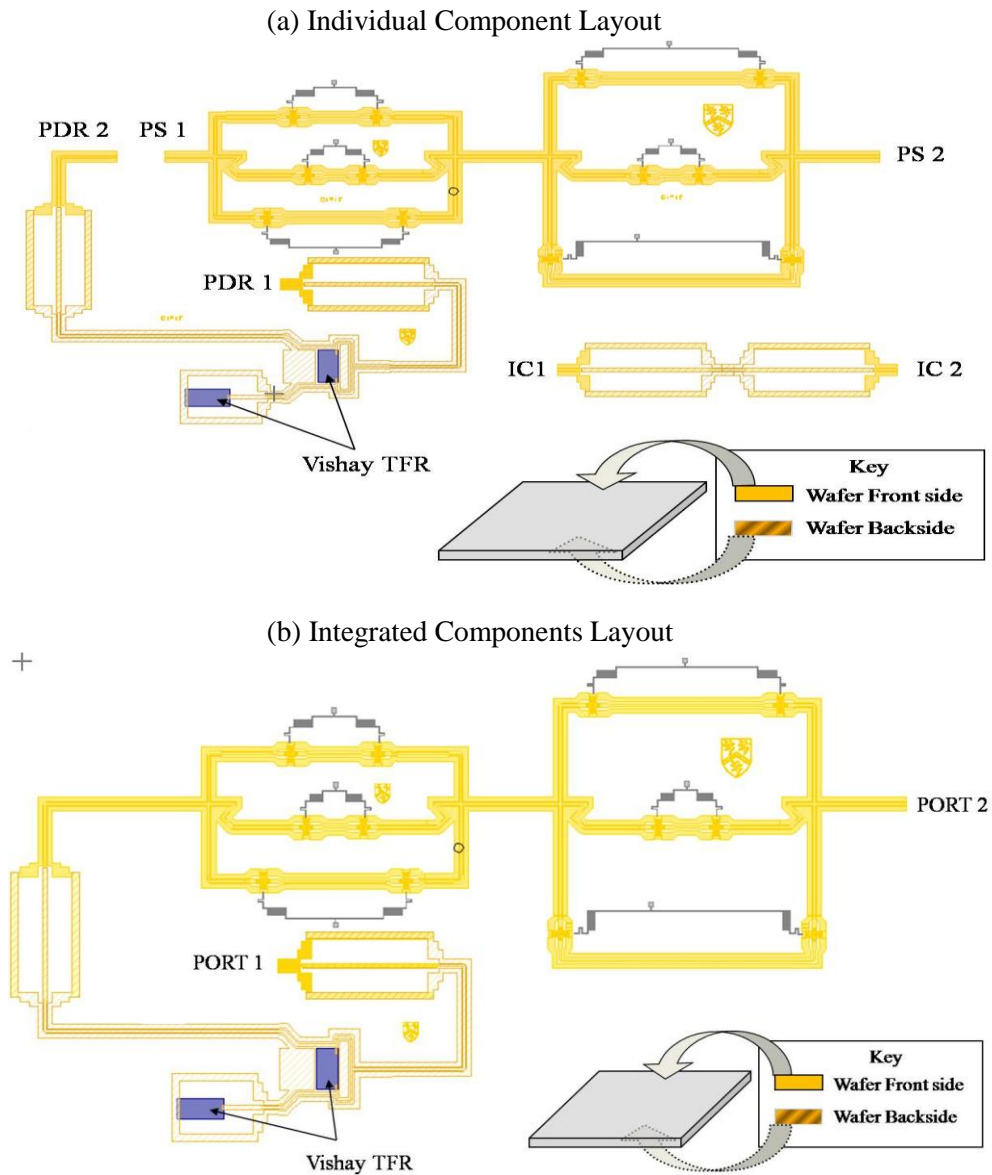
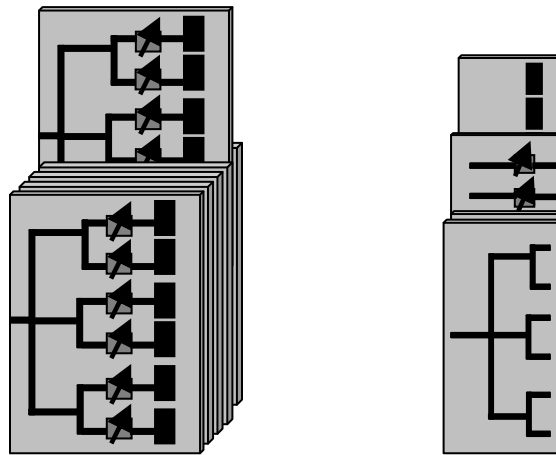


Figure 5.1 ESA component layouts.

The fact that all the components of a sub-array are fabricated and assembled on one common substrate makes the cost substantially lower than fabricating all the components individually and connecting them together with cables and connectors. This integrated sub-array module becomes the basic building block of an ESA. There are two basic types of ESA architectures to choose from; in-line and layered sub-array architectures, as illustrated in Figure 5.2 [66]. The in-line ESA consists of stacked, flat monolithic substrates, where each substrate/layer performs a number of functions such as: phase shifting, power division and signal distribution. Whereas the layered ESA consists of several layers, each layer with only one specific function such as phase shifting. The components are arranged in a “layered” sub-array architecture where each layer performs a specific function such as power division or phase shifting. The layered sub-array arrangement is selected for the design of the integrated ESA module because it results in a much thinner and compact package in comparison to the inline layout.



(a) In-line sub-array architecture (b) Layered sub-array architecture

Figure 5.2: Two basic types of ESA sub-array architectures. (a) The in-line sub-array architecture consists of stacked substrates where each substrate/layer performs a number of functions. (b) The layered sub-array architecture consists of several layers where each layer with only one specific function.

5.2.2 Fabrication Process

The integrated module is fabricated using an 8-mask batch process developed at the University of Waterloo and is built in CIRFE labs shown in Figure 5.3.

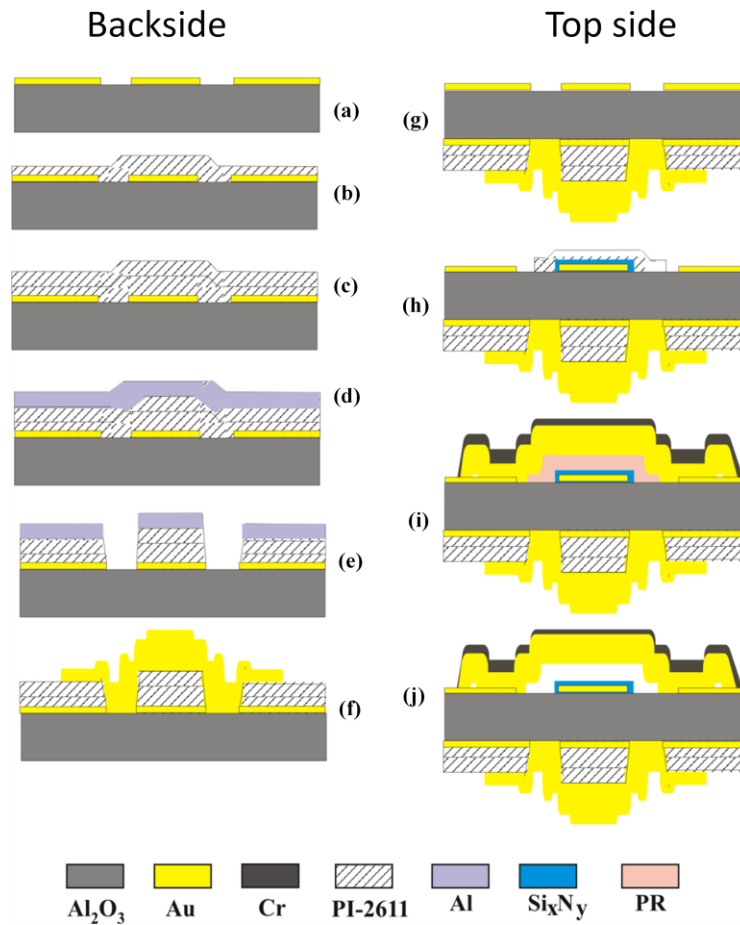


Figure 5.3: 8-mask integrated module fabrication process for the backside and top side of the wafer.

In Figure 5.3(a), 400\AA of Cr and 1200\AA of Au are deposited and patterned on the backside of a 10mil thick alumina wafer to define the power divider circuit. Two layers of polyimide are then spun on and cured to isolate the air bridges from the power divider circuitry. The polyimide is then patterned and etched in the RIE with the use of an aluminum layer as a hard mask and the air bridges are defined with a second gold layer. Next, the front side of the wafer is then processed by depositing 400\AA of Cr and 1200\AA of Au. Next an 1800\AA silicon nitride layer (Si_3N_4) is PECVD deposited and

patterned over the switch electrode area. In Figure 5.3(i), the sacrificial layer is then spun cast to a thickness of $2.6\mu\text{m}$. The MEMS air bridge is then fabricated by depositing a thin seed layer of 2000\AA of Au, and by electroplating it up to $1\mu\text{m}$. The MEMS switches are finally released using a critical point drying process.

The wafer pattern on the backside is aligned with the pattern on the front side with the use of alignment marks included in the chrome mask that utilize the outer edge of the alumina wafer, as shown in Figure 5.4. The alumina wafers used have a 1.25inch square surface area, and the chrome masks are designed with 1inch square windows to allow for resist edge bead, wafer handling and other fabrication tolerances.

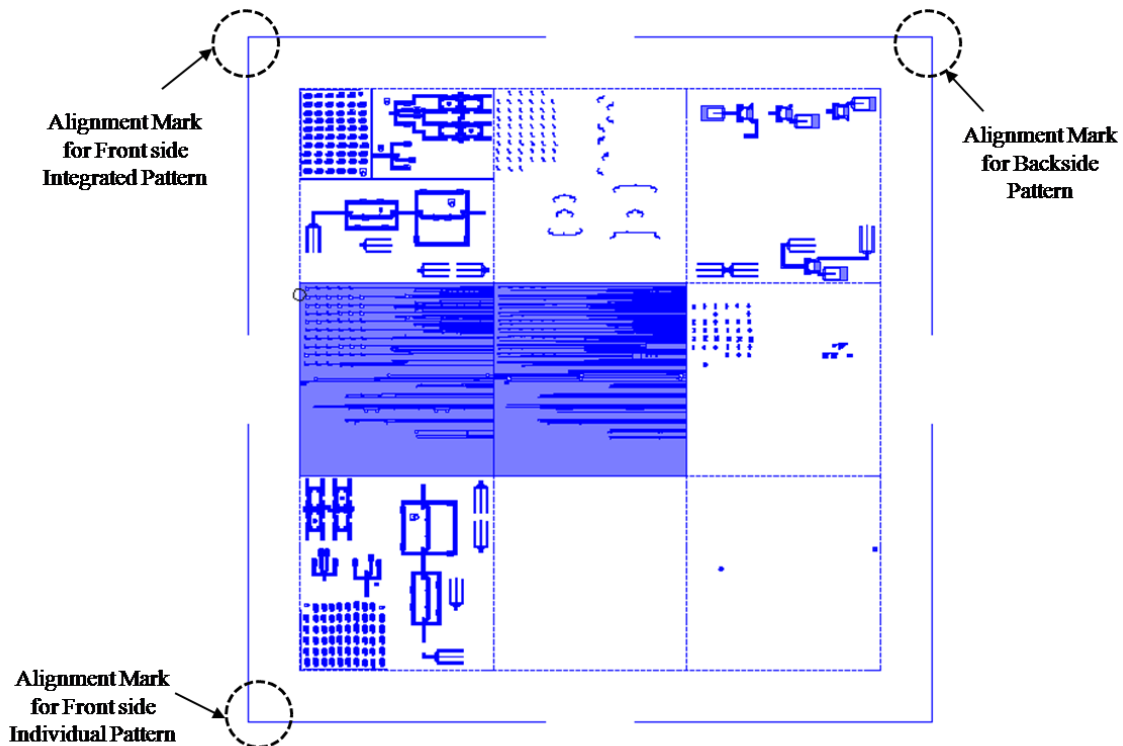


Figure 5.4: Mask layout with alignment marks required for backside to front side alignment.

5.2.3 Results

The footprint of the fabricated ESA module prototype is 2.2cm^2 . A 6 inch wafer ‘tile’ can accommodate 64 of these integrated modules. Pictures of the front and backside view of the fabricated chip are shown in Figure 5.5.

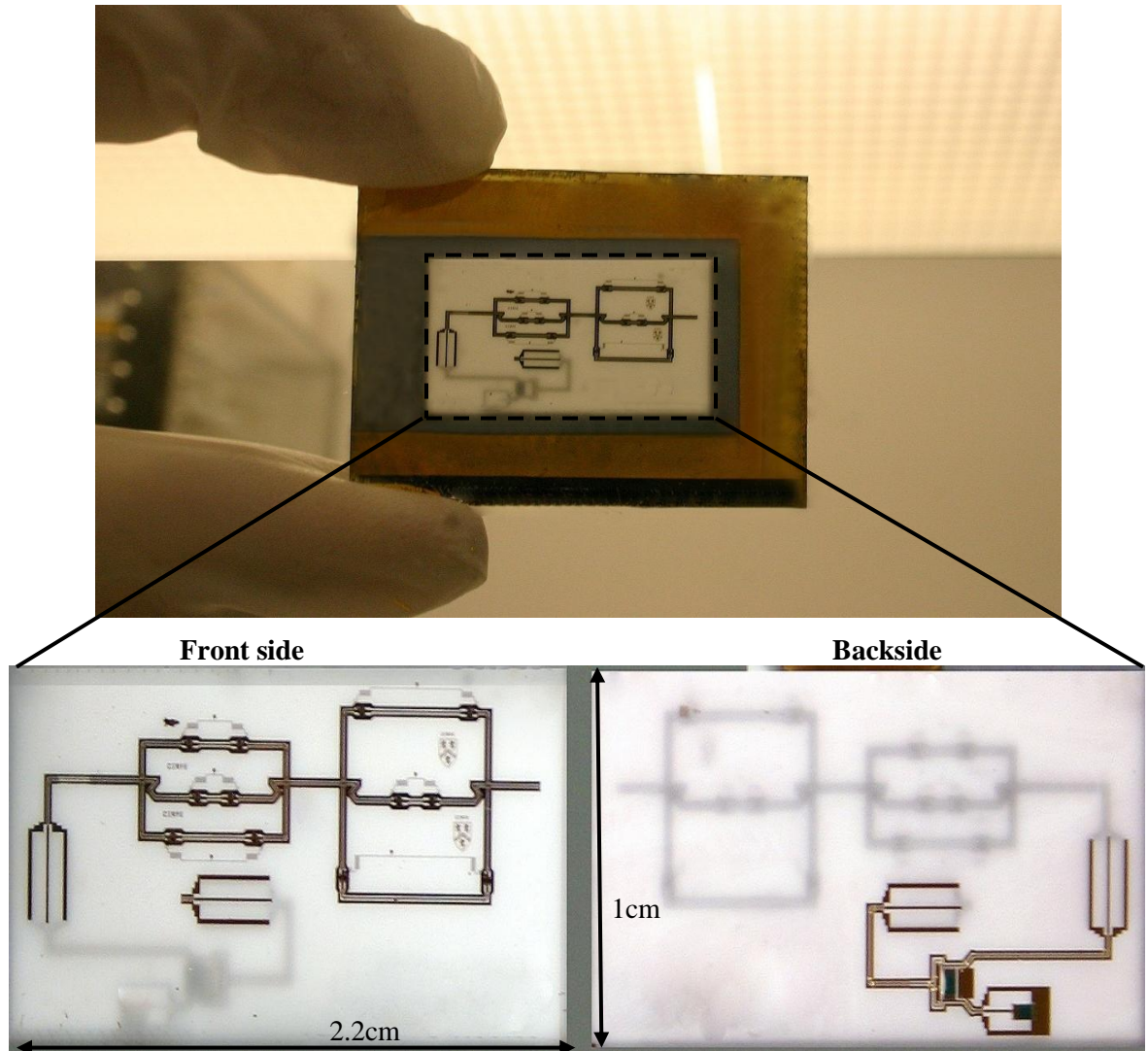


Figure 5.5: Fabricated integrated ESA module.

When held up to the light, the 10mil thick alumina wafer is thin enough to distinguish the coupled circuit on the module’s backside. The wafer is tested in a raised aluminum machined holder

illustrated in Figure 5.6, in order not to short the circuit on the backside of the wafer on the cascade wafer chuck during measurements.

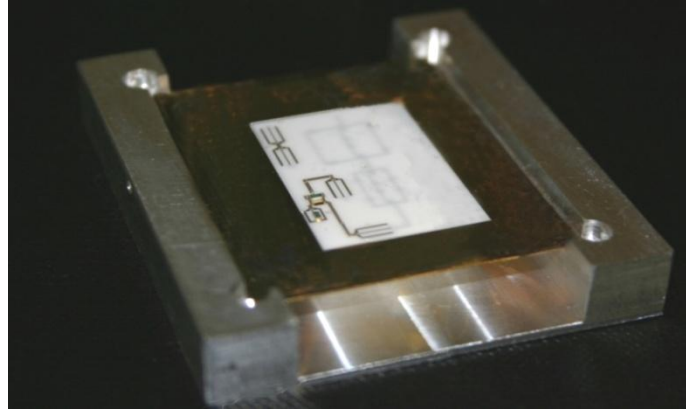


Figure 5.6: Aluminum machined holder used in order not to short the circuit on the backside of the wafer during measurements on the cascade wafer chuck.

The measured results of the integrated module switched through different delay line lengths are shown in Figure 5.7. The measured insertion loss for the integrated module at different states averages at $6.6\text{dB} \pm 0.23$; this includes the 3dB power split emerging from the power divider. Return loss is better than 20dB over an 11% bandwidth.

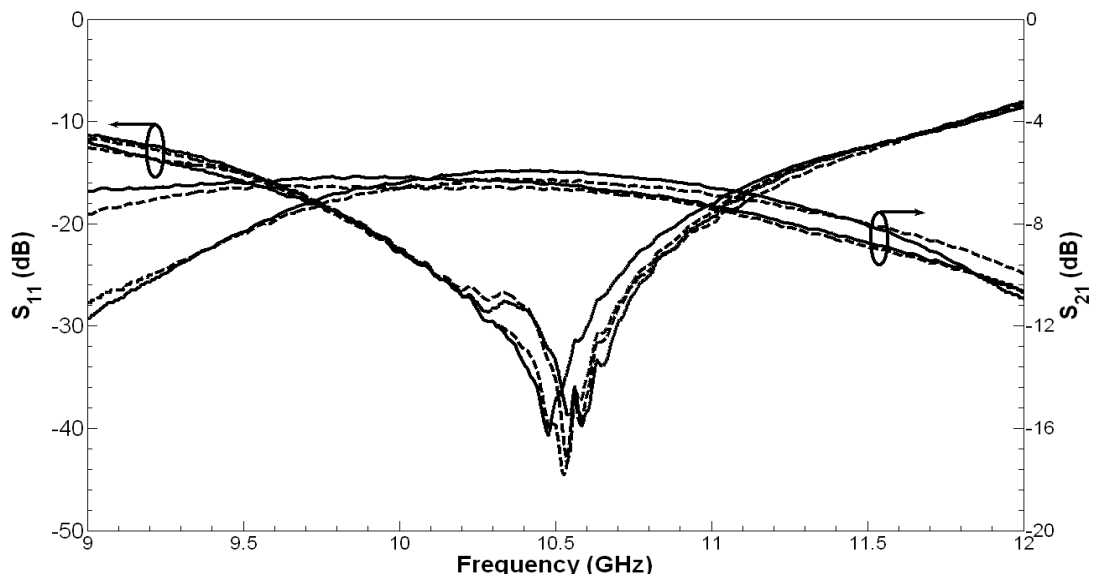


Figure 5.7: Measured return loss and insertion loss for the fully integrated MEMS ESA module.

Table 5.1: A summary of total measured insertion loss of the individual ESA components compared to the total insertion loss of the integrated module [75].

Individual Components		Integrated ESA	
<i>Component</i>	<i>Insertion Loss (dB)</i>	<i>Component</i>	<i>Insertion Loss (dB)</i>
Wilkinson Power divider	0.3		
Dual-Path Interconnect	0.62		
3-bit MEMS Phase Shifter	2.5		
Total Loss	3.42	Total Loss	3.6

The losses contributed by each system are extracted, and the individual components sum up to a total insertion loss of 6.42dB. Discrepancies found between the measured discrete and integrated losses can be attributed to several sources including connecting line conductor losses and fabrication tolerances such as front-to backside interconnect misalignment. The integrated module operates in X-band with an operational bandwidth of 11%. Shown in Table 5.1 is a summary of all the losses from each individual component to lead to the final integrated structure.

The integration properties of the capacitive switch, phase shifter, power dividers and capacitive interconnects make this packaged sub-array module very compact and attractive as a basic building block for a large low cost phased array. The presented integration technology provides for a new approach to ESA design. This technology also addresses stringent reliability and maintainability as well as electrical requirements. The result is a packaging and interconnect technology that reduces life cycle cost and achieves improved performances and reduces assembly issues.

5.3 MEMS Integrated Phase Scanned Phased Array Module

A compact 4 x 4 BM switchable with the use of a MEMS single-pole four-throw (SP4T) switch is presented. The overall beam-switching network is monolithically integrated within a real-estate area of 0.78cm². Details of the simulated and measured results are presented for a 4 x 4 Butler

matrix prototype unit developed at Ku band. Air-bridge crossovers are implemented to maintain compatibility with the MEMS fabrication process utilized for the SP4T MEMS switch. This technique not only eliminates the need for an expensive multi-layer process or larger wafer real estate but also provides a unique approach to fabricate the entire BFN monolithically. This prototype also demonstrates the potential for scalability to larger more complex systems. The phase error and couplings are within 14° and -6 ± 2.4 dB respectively. Large phase and error coupling are primarily due to the air bridge crossovers and can be reduced by implementing a 0dB crossover similar to that implemented in [25].

5.3.1 Design

This section details the design and fabrication of the switched beam system and its components designed to operate over the Ku band. The proposed system uses the BM network for beam forming procedure and consists of a 4×4 printed BM producing 4 orthogonal beams in the azimuth direction. The proper input of each matrix is chosen using a digitally controlled MEMS SP4T switch. The block diagram of the system is presented in Figure 5.8. In many applications, it is desirable to radiate several independent beams simultaneously from an array. That is the radiation resulting from a simultaneous excitation of two or more input ports should be a simple linear superposition of the radiation obtained when the ports are excited separately.

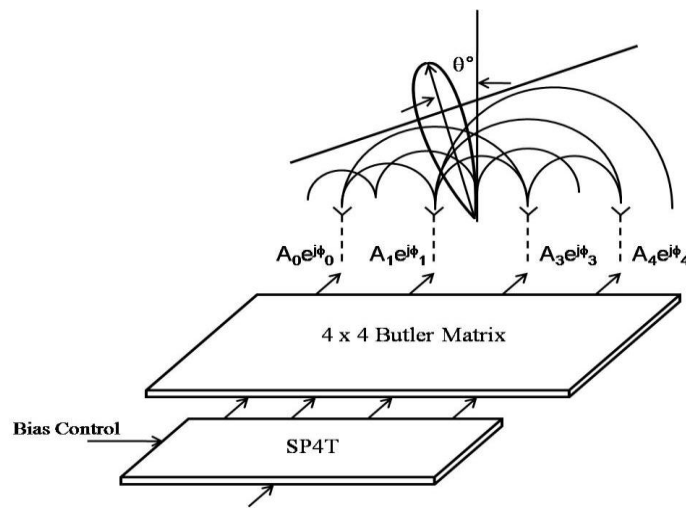


Figure 5.8: Block diagram of the proposed MEMS-switched integrated beamforming network.

In order to minimize the space occupied by the passive network and simplify its production, a bi-planar topology using FGC waveguide lines has been chosen. The folded FGC waveguide lines implemented in the BM design allow for high-density integration. Crossovers are implemented with the use of an air bridge suspended in air in a MEMS-compatible process to fabricate the Butler matrix and SP4T simultaneously and monolithically onto one substrate. The experimental results demonstrate the simplicity and flexibility of this novel approach. The realized integrated MEMS Butler matrix is shown in Figure 5.9 with a total real estate area of 0.78cm^2 . The NiCr Vishay thin film resistors (TFRs) are placed at the Butler matrix's four output ports and wire bonded to the ports not being measured as a matched 50Ω load.

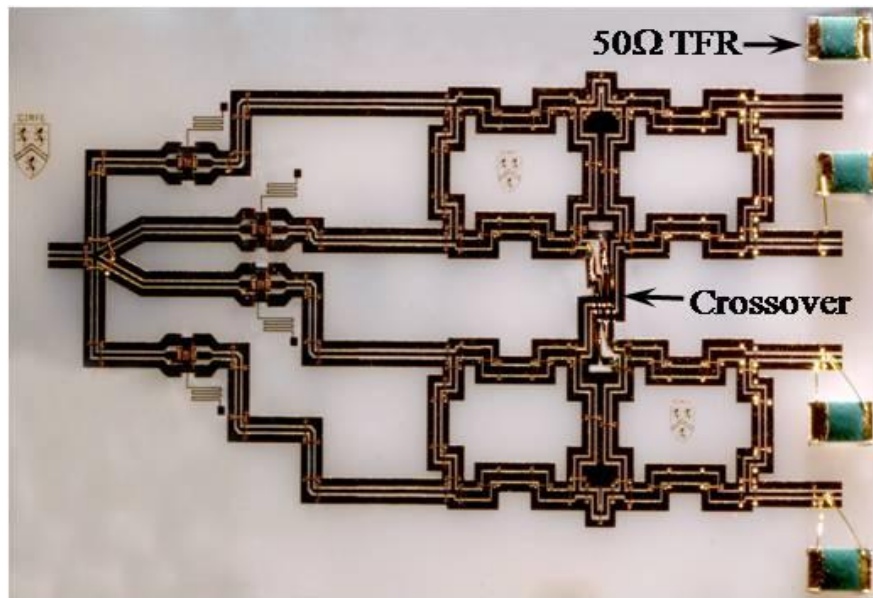


Figure 5.9: Realized integrated MEMS 4x4 Butler matrix. NiCr Vishay thin film resistors (TFRs) are placed at the Butler matrix's four output ports and wire bonded to the ports not being measured as a matched 50Ω load.

5.3.2 Results

A two-port on-wafer measurement of the integrated circuit is performed from 14GHz to 15GHz using an HP8722ES vector network analyzer. The measured magnitude results are shown in

Figure 5.10. The Butler matrix exhibits couplings and phase errors within -6 ± 2.4 dB and 14° over a 200MHz bandwidth with a center frequency at 14.45 GHz.

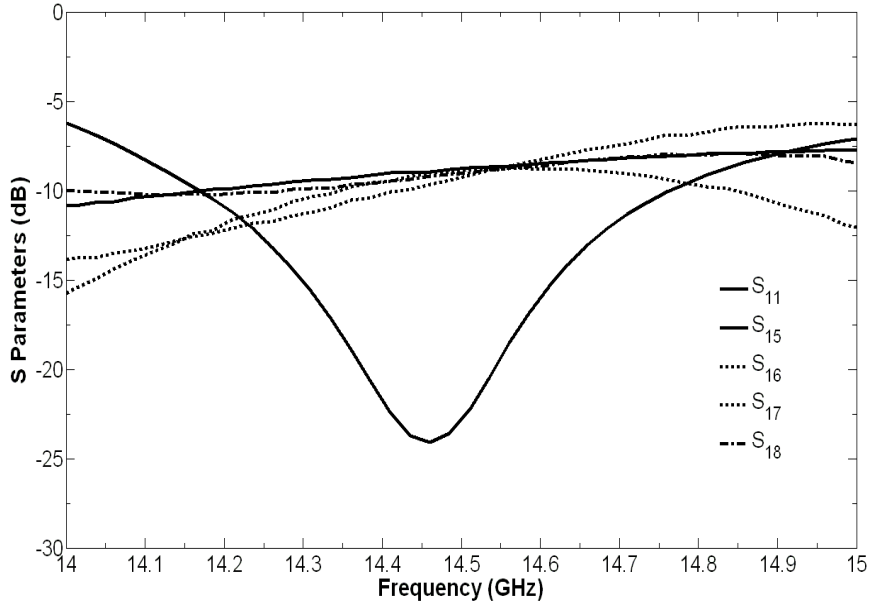


Figure 5.10: Measured S-parameters when Port 1 is selected in the MEMS 4x4 Butler matrix. The switch at Port 1 is kept in 'on' state whereas the switches at Port 2, Port 3 and Port 4 are actuated to 'off' state.

The disadvantage of using a high permittivity substrate like alumina can result in a reduced and narrow bandwidth and higher insertion loss as observed in the results. This can be perhaps compensated for by implementing the crossover design in the method proposed in [25]. The SP4T switch would have to be redesigned and characterized, but a monolithic implementation can still be achieved.

An advantage of the MEMS switchable 4x4 BM is its potential for scalability to larger more complex matrices. The MEMS integrated matrix prototype developed can represent a basic building block that is implementable to larger switchable matrices such as the 8x8 MEMS integrated BM illustrated in Figure 5.11. Using an SP2T switch, the SP4T MEMS integrated Butler matrix unit cell and simple crossover air bridge lines are simply cascaded and scaled to achieve the larger matrix.

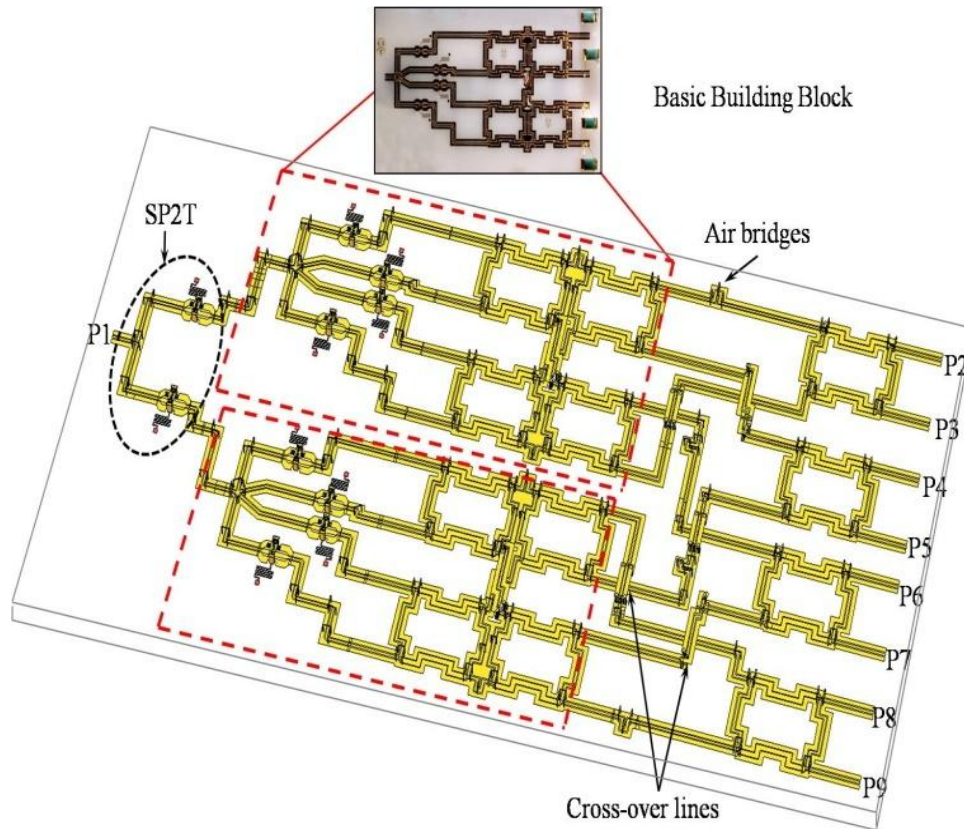


Figure 5.11: 8x8 folded Butler matrix layout.

In summary, a MEMS-based switched beam system designed using a compact folded 4x4 Butler matrix and MEMS SP4T has been introduced. The BFN is made compact using folded FGC lines and is monolithically integrated into one substrate via air bridges for crossover lines. The proposed matrix demonstrates a great potential for monolithic integration of switched beam phased arrays and compatibility with MEMS fabrication processes. This matrix prototype also demonstrates the potential for scalability to larger more complex systems.

Chapter 6

Conclusions and Future Work

This thesis deals with the use of RF MEMS technology to develop a high performance integrated ESA module. The first part of this thesis has focused on the development of novel capacitive switches with optimum performance. Specifically, a warped-beam bimetallic capacitive shunt switch with an insertion loss of less than 0.2dB and isolation better than 40dB at X-band has been demonstrated. These switches are then implemented in three-throw and four-throw configurations for signal routing. The three-throw switch is then used to design a 3-bit digital phase shifter and the four-throw switch is used to develop a MEMS switchable integrated Butler matrix prototype. This research has introduced novel capacitive MEMS switches that offer the potential for low-loss high-isolation capacitive switches for not only phase array applications but for other RF applications. Moreover, a modular monolithic design for ESAs has been presented. The design uses via-less micromachining and MEMS technologies for the integration of the ESA components into a single 2.2cm² unit. The prospect of integrating these devices can result in improved RF performance and low DC power consumption, offering exciting possibilities for the development of highly miniature low cost ESAs.

6.1 Thesis Contributions

The major contributions of the thesis can be summarized as follow:

- A novel dual-warped beam concept that enhances the RF performance of capacitive shunt MEMS switches has been developed. A capacitance ratio of up to 170 has been achieved with an isolation of 40dB at X-band and actuation voltages as low as 27V. These switches have also been implemented in compact three-throw and four-throw configurations in an FGC implementation.

- A novel 3-bit finite FGC waveguide switched-delay line MEMS phase shifter is developed with four cascaded SP3T dual-warped beam capacitive switches to achieve low-loss performance and simplify the ESA design. The phase shifter has a total chip area of 1.4cm^2 and exhibits an insertion loss of $2.5\pm 0.2\text{dB}$ with an rms phase error of $\pm 6^\circ$. Compact meandered FGC lines are employed in the design of the phase shifter to incorporate the high-isolation shunt dual-warped beam capacitive MEMS switches proposed. Implementing the FGC lines also eliminates the need for vias and ground planes typically required by microstrip line phase shifter designs.
- A novel compact 4×4 Butler matrix (BM) consisting of meandered FGC waveguide branch-line couplers is designed. The BM is monolithically integrated with the use of polyimide as an inter-dielectric layer, and is compatible with standard MEMS fabrication processes. Optimized micromachined crossovers isolated with the thick polyimide layer or air bridges are used to realize the bi-planar structure.
- A highly integrated ESA module using an innovative integration approach with MEMS processing technologies is presented. An 8-mask process is developed and optimized at CIRFE labs. Processing challenges such as thin film resistor design and fabrication, material compatibility as well as polyimide adhesion to metal layers have been addressed and circumvented. In order to fully integrate these components, FGC waveguide MEMS components are employed for the very first time without the use of interconnect vias or complex multi-layer processing. The 2.2cm^2 integrated module has a bandwidth of 11% and is an enabling building block of integrated sub-system arrays for lightweight large space-based phased arrays.

In summary, the focus of this thesis has been on developing integrated ESA modules. A new integration technology has been developed to create a vertically interconnected MEMS FGC module for lightweight conformal phased array technology advancement. The design uses MEMS processing, FGC MEMS components and via-less interconnects to obtain a compact and versatile integrated module. This modular design for active phased arrays based on building blocks of integrated sub-arrays offers significant reduction in size, mass, DC power consumption and cost.

6.2 Future Work

Although the research for this thesis has been extensive, there are still several unexplored issues. Moreover this work opens up many avenues of research that can be explored.

- An interesting project would be to investigate the use of corrugations rather than bimetallic layers to achieve the warped-beam effect in the proposed capacitive shunt switches. Using corrugations, the beams would curl up achieving lower upstate capacitance without significantly contributing to the switch's stress. This in turn may reduce actuation voltages due to reduced intrinsic stress and result in a higher reliability switch.
- Further mechanical modeling and analysis of the warped-beam switch would be useful to better understand the stresses and their influence on the switch's pull-in voltage and 'on' state capacitance values. This project can be a collaborative effort with the mechanical engineering department.
- The reliability of MEMS switches is of major concern for long-term applications [11]. Therefore, it would be worthwhile to perform reliability tests to further characterize the switch's performance. Moreover, developing a low cost hermetic packaging technique can also be explored. This packaging can provide mechanical support, environment protection, electric interconnection, thermal dissipation, power management and stable reliable performance characteristics [67]. Reliability and packaging are two important issues of MEMS switches that can primarily determine their cost.
- In order to reduce the insertion losses exhibited by the 3-bit delay-line phase shifter and further enhance RF performance, a microstrip line phase shifter design can be explored with the implementation of the proposed high isolation low-loss dual-warped beam switches. By eliminating the need for quarter-wave transformers, the phase shifter exhibits less conductor line loss.

- Another approach to the integrated 4x4 MEMS Butler matrix would be the possibility of designing and fabricating the integrated Butler matrix using a 0dB coupler for the crossover rather than air bridges. This may achieve a wider bandwidth performance with lower amplitude and phase variations.
- Achieving a fully monolithic integrated ESA module by implementing processed thin film resistors than hybrid Vishay resistors with materials such as TaN, poly-Si or NiCr.
- Investigating the use of spin-on inter-dielectric organics such as polyimide to obtain the integrated ESA module. This involves redesigning the FGC waveguide RF components and building the module upwards from the surface of the substrate. There are some challenges that may be faced such as adhesion problems, organic layer shrinkage, however this approach allows for easy implementation of the antenna components.

Appendices

Appendix A

Integrated Module Fabrication Process

8 mask process step-by-step process description:-

(1) Gold 2 Backside Layer Patterning – Mask 3

- AZ3330 Positive Resist (Program S)
- Spin at 4000rpm for 30sec, acl =15
- Soft bake at 90°C for 60sec
- Exposure for 12 sec
- Post exposure bake at 110°C for 60sec
- Develop for 45sec (new 6 mask process developer)

(2) Etch the Gold 2 Backside Layer

- Wet etching for 2min and 45sec with 100% diluted Transene gold etchant
- Cr etch took 20-25secs with 40% diluted etchant
- Stripping the resist 60-70°C

***TAKE OUT PI2611 to DEFROST the day BEFORE PI and book furnace*

(3) Deposit 400Å Cr adhesion layer on Backside

- E-beam 400Å of Cr at 3Å/sec

(4) Deposit almost 12micron PI 2611 on Backside

- VM652 in a 10mL syringe onto the wafer
- Let it sit for 20 secs
- Spin @ 5000 rpm for 30 sec
- Bake on hotplate @ 120 C for 30 sec
- Pour PI onto centre of wafer (i.e. 0.375” drop for 2” wafer) and let sit for 15 sec
- Spin (Program ‘P’) 15 sec, 500 rpm, acl: 15 and 35 sec, 1500 rpm, acl: 15 (~11 microns)
- Soft bake - 2 min, 90 C and 2 min, 150°C
- Make sure the local temperature is at 150°C – load program1 and make sure it’s in Res then hold down the run button to run the program
(150°C load, 350°C for 0.5hr, hold 0.3hr, 150°C for 0.4hr, 90 for 0.15hr, t=0 at 90°C).

(5) Deposit almost 12micron PI 2611 on Backside

- VM652 in a 10mL syringe onto the wafer
- Let it sit for 20 secs
- Spin @ 5000 rpm for 30 sec
- Bake on hotplate @ 120 C for 30 sec
- Pour PI onto centre of wafer (i.e. 0.375” drop for 2” wafer) and let sit for 15 sec
- Spin (Program ‘P’) 15 sec, 500 rpm, acl: 15 and 35 sec, 1500 rpm, acl: 15 (~11 microns)
- Soft bake - 2 min, 90 C and 2 min, 150 C
- Make sure the local temperature is at 150°C – load program1 and make sure it’s in Res then hold down the run button to run the program
(150°C load, 350°C for 0.5hr, hold 0.3hr, 150°C for 0.4hr, 90 for 0.15hr, t=0 at 90°C).

- VM652 in a 10mL syringe onto the wafer
- Let it sit for 20 secs
- Spin @ 5000 rpm for 30 sec
- Bake on hotplate @ 120 C for 30 sec
- Pour PI onto centre of wafer (i.e. 0.375" drop for 2" wafer) and let sit for 15 sec
- Spin (Program 'P') 15 sec, 500 rpm, acl: 15 and 35 sec, 1500 rpm, acl: 15 (~11 microns)
- Soft bake - 2 min, 90 C and 2 min, 150 C
- Make sure the local temperature is at 150°C – load program1 and make sure it's in Res then hold down the run button to run the program
(150°C load, 350°C for 0.5hr, hold 0.3hr, 150°C for 0.4hr, 90 for 0.15hr, t=0 at 90°C)

(6) Deposit Aluminum 0.5micron Metal Mask

- Sputter 0.5 microns of Aluminum @ 180Å/min (28mins)

(7) Pattern Aluminum on Backside

- AZ3330 Positive Resist (Program S)
- Spin at 4000rpm for 30sec, acl =15
- Soft bake at 90°C for 60sec
- Exposure for 12 sec (check what others have used)
- Post exposure bake at 110°C for 60sec
- Develop for 45sec (6 mask process developer)
- Hard bake 120 °C for 120 secs

(8) Etch Aluminum Layer

- Warm up the PAN etch at knob 3 and it should take about 45 secs
- Strip the patterning resist

(9) Etch PI 2611 layer

- Etch rate of recipe is about 0.013microns/sec
- Estimated time of etch ~ 1800secs
- Trionimide recipe – ICP P=500W, RF=35W, P=10mT, O₂=35ccm

(10) Etch the Aluminum Mask

- Warm up the PAN etch at knob 3 and it should take about 45 secs

(11) Pattern Gold 2 backside Layer for lift-off

- Lor15A @ 2000rpm for 30 secs, acl=10
- Soft bake at 150°C for 5 minutes
- AZ3312 @ 3000rpm for 30secs
- Soft bake at 90°C for 60sec
- Exposure for 12 sec
- Post exposure bake at 110°C for 60sec
- Develop for 2min – 2mins10secs

(12) Deposit Gold 2 backside

- Deposit 400Å Cr adhesion layer followed by 1micron sputtered gold @ 300Å/sec (time=33minutes)

(13) Remove the LOR 15A

- Warm up two beakers of PG Remover to about 65 -70°C (PG Remover A and PG Remover B) and place the wafers in each beaker for about 20mins.
- Rinse off gently with IPA.

(14) Gold 1 Front side Layer Patterning

- AZ3330 Positive Resist (Program S)
- Spin at 4000rpm for 30sec, acl =15
- Soft bake at 90°C for 60sec
- Exposure for 12 sec (check what others have used)
- Post exposure bake at 110°C for 60sec
- Develop for 55sec (6 mask process developer)
- Gently flip wafer over and use syringe to drop resist on backside and bake @ 120°C for 2mins to protect backside

(15) Etch the Gold 1 Front side Layer

- Wet etching for 2min and 45sec with 100% diluted Transene gold etchant
- Cr etch took 20-25secs with 40% diluted etchant
- Stripping the resist 60-70°C (both front side and back side resist removed)

(16) Pattern Cr front side Layer for lift-off

- LOR 15A Lift Off Resist
- Spin at 2000rpm, acl. = 10, for 30 secs on the LHS spinner
- Soft bake @ 150°C for 5 mins
- AZ2035 Negative Resist
- Spin at 4000rpm for 30sec on the RHS spinner
- Soft bake at 110°C for 60sec
- Exposure for 9 sec
- Post exposure bake at 110°C for 60sec
- Develop between 1min 45sec and 2 mins

(14) Deposit 150A Cr in Intel Vac

(15) Remove the LOR 15A

- Warm up two beakers of PG Remover to about 65 -70°C (PG Remover A and PG Remover B) and place the wafers in each beaker for about 20mins.
- Rinse off gently with IPA – do not overdo.

(16) Dielectric Patterning

- LOR 15A Lift Off Resist
- Spin at 2000rpm, acl. = 10, for 30 secs on the LHS spinner
- AZ3312 Positive Resist
- Spin at 4000rpm for 30sec on the RHS spinner
- Soft bake at 90°C for 60sec
- Exposure for 12 sec

- Post exposure bake at 110°C for 60sec
- Develop between 1min and 1 min 10sec until you can see the edge of the LOR line up with the patterning resist edge.

(16) Deposit 350A Ti adhesion layer on Front Side

(17) Deposit 0.2micron PECVD nitride on Backside

Table II. Recipe for PECVD Nitride

Pressure	625mtorr
RIE Power	40W
Temperature	250°C
SiH ₄	12 sccm
NH ₃	10 sccm
N ₂	200 sccm
Time	500sec

(18) Remove the LOR 15A

- Warm up two beakers of PG Remover to about 65 -70°C (PG Remover A and PG Remover B) and place the wafers in each beaker for about 20mins.
- Rinse off gently with IPA – do not overdo.

(19) Sacrificial Layer Spin-on and Patterning

Do a test wafer first to see exposure time for 3 and 4micron gap

- AZ3330 Positive Resist
- Spin at 2400rpm for 30sec acl =15 / spin @ 2000rpm – test wafer first
- Soft bake at 90°C for 3min
- Exposure (a) Anchors for 18sec
- Post exposure bake at 110°C for 60sec
- Develop for 1min and 15sec
- Hard bake at 120°C for 120secs

Table III. Spin Speeds and associated exposure times

Spin Speed (rpm)	1300	2400	2000
Thickness (µm)	4	2.7	3
Exposure time Anchor (sec)	20	16	17

(21) Deposit final Gold Layer

- E-beam 0.2 microns gold layer
- Electroplate the following thickness:-
 - Current =0.02A, plating time=0.72A.min for ~1.3µm (time = 36mins)

(22) Deposit Cr Layer

- E-beam 150Å Cr layer

(23) Pattern Cr and Gold Final Layers

- AZ3330 Positive Resist (Program S)
- Spin at 4000rpm for 30sec, acl =15
- Soft bake at 90°C for 60sec
- Exposure for 12 sec (check what others have used)
- Post exposure bake at 110°C for 60sec
- Develop for 45sec (6 mask process developer)

(24) Etch the Cr and Gold 2 Front side Layer

- Cr etch took 20-25secs with 40% diluted etchant
- Wet etching for 2min and 30sec with 100% diluted Transene gold etchant

(26) Etch the Cr and Gold 2 Front side Layer

- Place in the RIE for a partial dry etch using Release 2 recipe with the following settings:-

Pressure	600mtorr
RIE Power	10W
ICP Power	150W
O₂	50 sccm
Time	1200sec

- Wafer must be removed after every 180sec interval to prevent it from warming up and to check on the progress.
- Wet etching of the sacrificial photo resist layer using Kwik Strip for 3-4hrs warmed up to 65°C.
- 5min IPA or any other alcohol (3 times, each time in a fresh batch)
- CO₂ critical point drying using a purge time of 15 min. 6 pounds of CO₂ is required.

(27) Affix TRFs on the back side AFTER releasing the wafer. It was found if the TFRS are affixed on the wafer before dry and wet release; the resistive NiCr layer on the resistors is etched as seen in the Figure A.1.

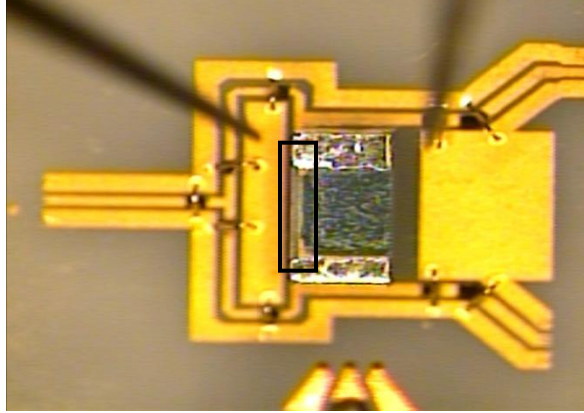


Figure A.6.1: RIE etch result of the hybrid Vishay thin film resistor.

Appendix B

Polyimide Characterization and Processing

Included in this section is a detailed description of the characterization of the HD Microsystem's PI-2611 polyimide. The dielectric constant and the dry etch process developed to obtain high aspect ratio vias are described. Methods to improve the polyimide's adhesion to gold are presented as well as methods to eliminate residual polymer grass after dry etching in the RIE.

The polyimide is first characterized to determine the dielectric constant using a standard C-V measurement setup shown in Figure B.1. An emulsion mask with varying size metal-insulator-metal (MIM) capacitors is used with a $6\mu\text{m}$ polyimide layer as the inter-dielectric. The metal used was aluminum for the capacitor plates. Varying capacitor areas were also included to characterize the 250°C PECVD deposited silicon nitride used in the capacitive switch design ($0.2\mu\text{m}$ thick layer was used). In the measurement setup, a voltage applied across the capacitors with DC probes generates charge and a proportional capacitance across the plates. The dielectric constant can then be extracted given the MIS capacitor area and plate-to-plate separation, or insulator thickness.

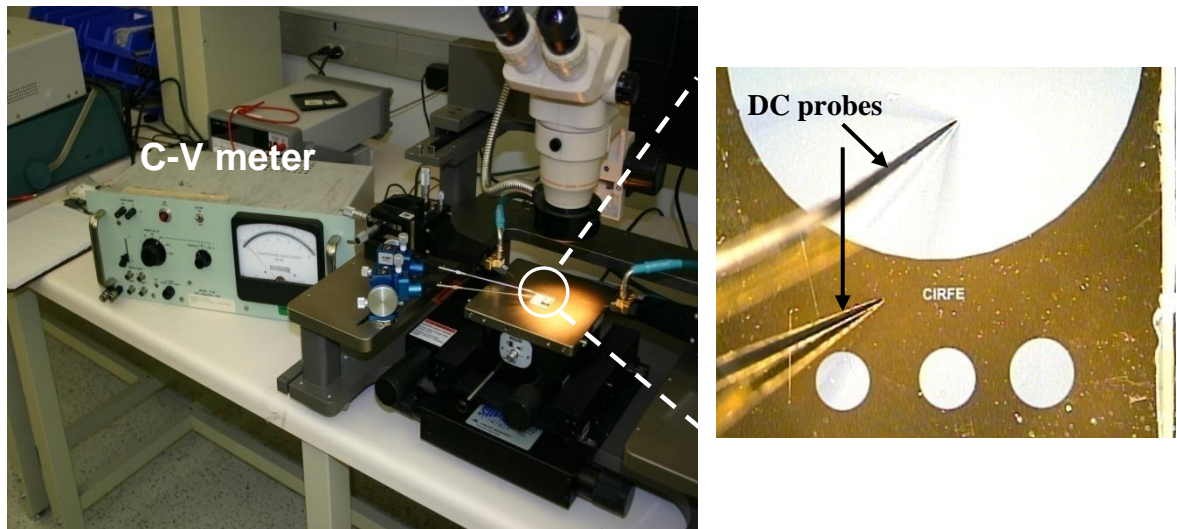


Figure B.6.2: C-V measurement setup.

Disc capacitors with areas ranging from $1.42\mu\text{m}^2$ to $89.3\mu\text{m}^2$ were measured using the C-V meter and the results are plotted in Figure B.2. The average dielectric constant of PI-2611 is calculated as 3.34 at 1MHz. The silicon nitride layer's average dielectric constant is calculated as 6.02.

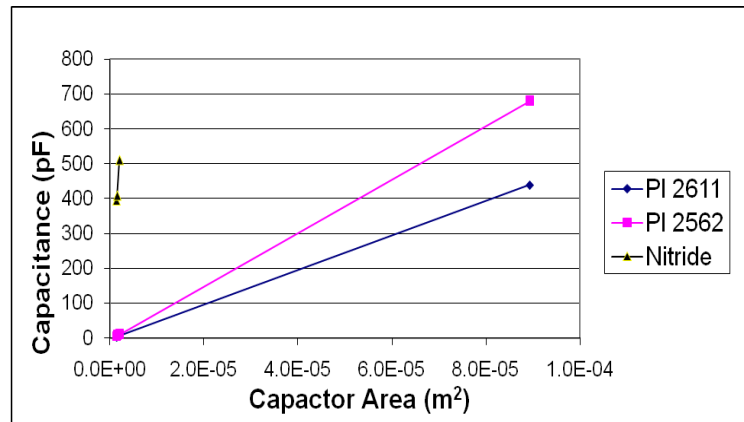


Figure B.6.3: Capacitance versus area for PI-2611, PI-2562 and PECVD Silicon Nitride.

Moreover, the coupling behavior between two overlapping lines separated by PI-2611 has been modeled. Shown in Figure B.3 are some transmission lines designed with varying overlapping areas and their RF performance was measured.

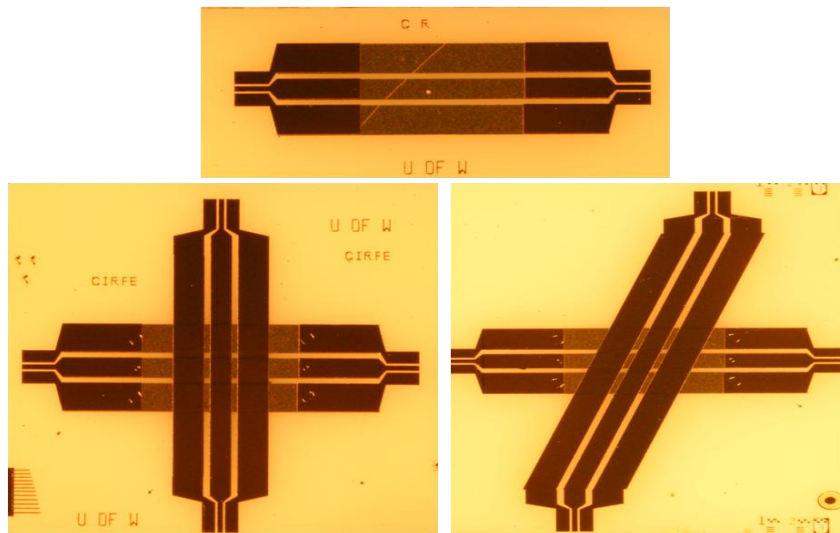


Figure B.6.4: Overlapping circuits designed with a $6\mu\text{m}$ thick PI-2611 inter-dielectric layer.

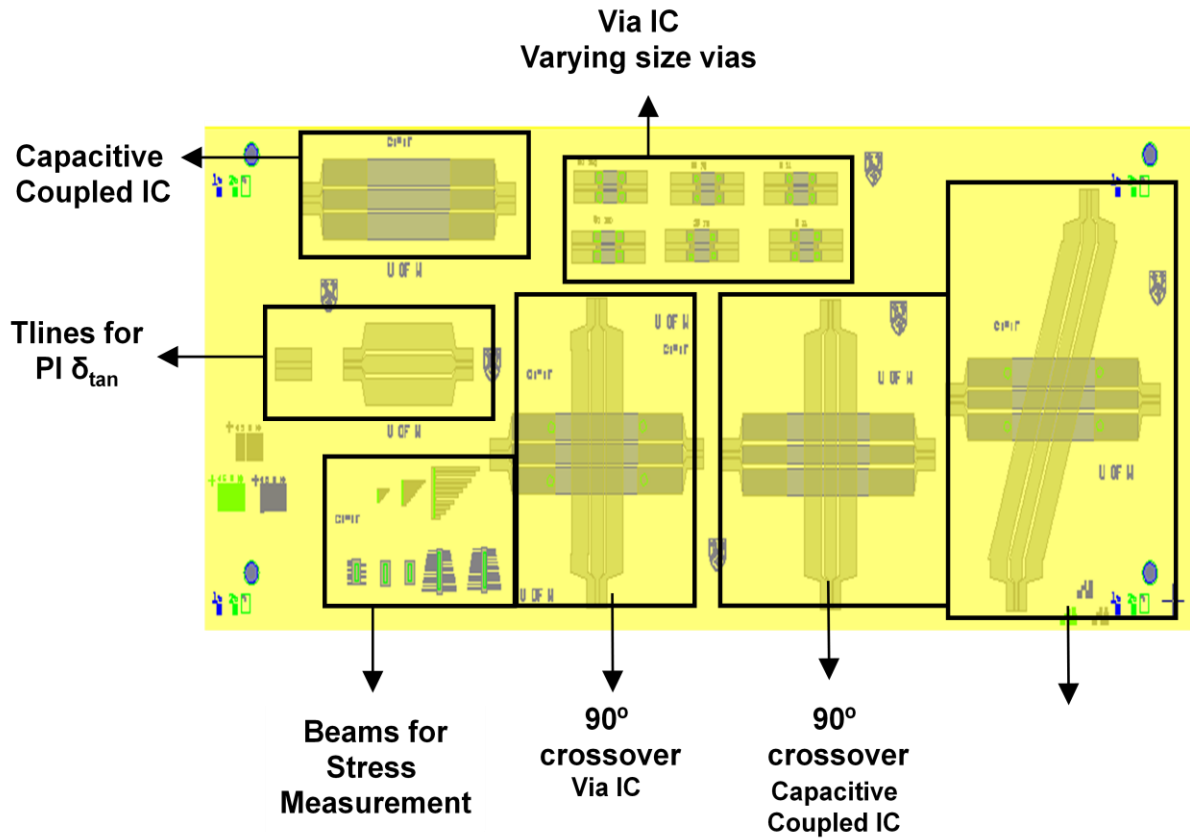


Figure B.6.5: Chromium mask layout for PI-2611 characterization.

The application of the PI-2611 required optimization and several iterations and the flow diagram is shown in Figure B.4. Starting off with a dehydration bake, the wafer is coated with HD Microsystems adhesion promoter to better enhance the polyimide's adhesion to the wafer. The wafer is soft baked for 5 minutes and is then coated with the second polyimide layer. These steps are repeated to achieve the desired multiple stack thickness. Once the appropriate number of PI layers are spun on, the wafer is then placed into the furnace for a 5-6 hour cure.

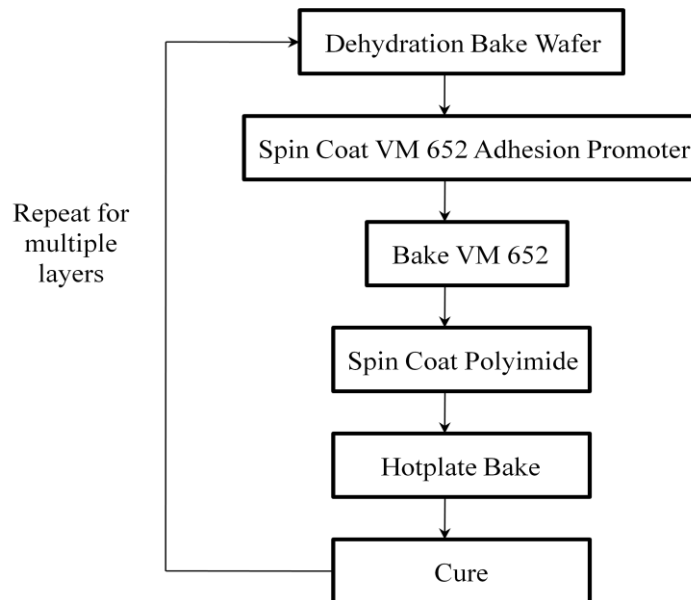


Figure B.6.6: Flow chart of the polyimide application process.

Step-by-step details of the polyimide application process and etch recipe is listed below along with several processing problems faced.

Step 1: RCA clean process

- 750ml DI water, 130ml Ammonium Hydroxide (27%), 130ml Hydrogen Peroxide at 70°C for 15min
- Rinse in DI water
- Dehydration bake at 120°C for 2min

Step 2: Application of the adhesion promoter VM 652

- Bake wafer at 150 °C for 15-30 min for dehydration
- Coat entire wafer surface with VM 652 and let stand for 20 s
- Spin at 3000 RPM for 30 s
- Hotplate bake at 120°C for 30

Step 3: Application of the Polyimide PI 2611

- Centre wafer on vacuum chuck of spinner
- Slowly pour polyimide onto centre of wafer from Nalgene bottle, enough so that the spun film completely covers wafer
- Spin 500 rpm for 10s
- Spin 3000 rpm for 30s

- On hotplate, bake PI 2611 at 90 °C for 2min then 150 °C for 2min, bake PI 2562 at 120°C for 5min
- Clean spinner with AZ PG Remover

Step 3: Cure the Polyimide

Polyimide must be cured after the hotplate bake to completely remove solvents.

- Load at 150°C
- Ramp to 350°C at 4 °C/ min
- Cure for 30min
- Switch oven off and allow cooling
- Unload at 150°C

Polyimide is commonly etched using inductively coupled plasma/reactive ion etch (ICP RIE) systems using O₂ or O₂/CF₄ [68 – 70]. We have attempted etches with each of these gases, as well as O₂/SF₆, with mixed results. As a starting point we used the O₂/SF₆ polyimide etch recipe recommended by the manufacturer of the RIE, Trion. However, the etch process was highly non-uniform and left residue on the wafer stage and on the wafer itself as illustrated in Figure B.8. The most effective etch that we have developed uses pure O₂ at low pressure and high ICP power. Low pressure increases the mean free path of the accelerated ions which improves the anisotropy of the etch. The RIE etch recipe parameters are listed in Table B.1.

Table B.1: Parameter settings for the RIE PI etch.

Pressure	10mtorr
ICP Power	500W
RIE Power	25W
O ₂ flow	35sccm ³

The procedure for etching using the Trion system begins by first pumping out the chamber without a sample and tuning the ICP and RIE variable capacitor pairs to minimize the reflected RF power. With the above etch recipe, the reflected ICP power can be brought to between 1 and 10W and the RIE power to between 0 and 1W. Once the tuning is completed, the chamber is vented and loaded with the sample. The etch rate for PI 2611 is about 1µm/ min. While the bulk of the polyimide is being etched, the plasma has a dull pink glow which fades to a dim grey once the etch stop (gold and

wafer surface) is reached. At this point, the wafer is left in the RIE an additional 30s to remove the remnant polyimide. Once etching is complete, the Al mask is etched in warmed PAN etch solution.

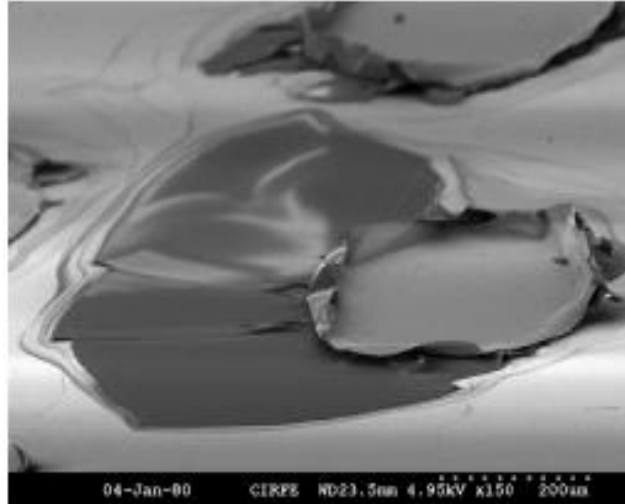


Figure B.6.7: SEM image of PI 2562 after etching in KOH with an Al mask [70].

Polyimide can be etched using KOH however the process is highly non-uniform and isotropic, and cannot be used to form high aspect ratio, anisotropic via features. The result is a softened film that delaminates, and a residue that is difficult to remove is produced.

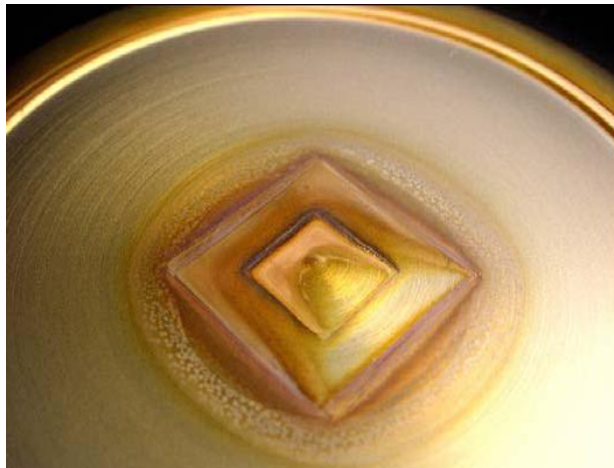


Figure B.6.8: Photograph of remnant residue left on the RIE's electrode after etching polyimide PI 2611 with SF_6 and O_2 . This residue was extremely difficult to remove and did not appear with CF_4/O_2 and pure O_2 recipes.

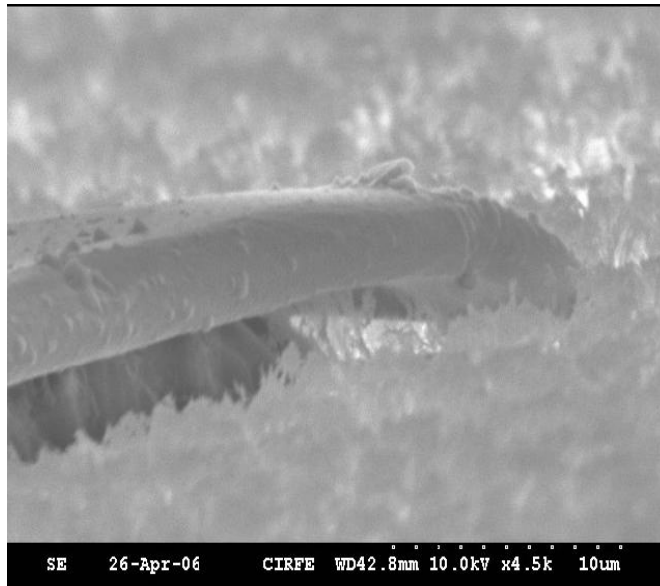


Figure B.6.9: SEM image of the residue referred to as “grass” as a result of re-deposited unetched polyimide during RIE etching PI 2611 in O_2/CF_4 . This etch recipe left considerably more residue than a pure O_2 etch.

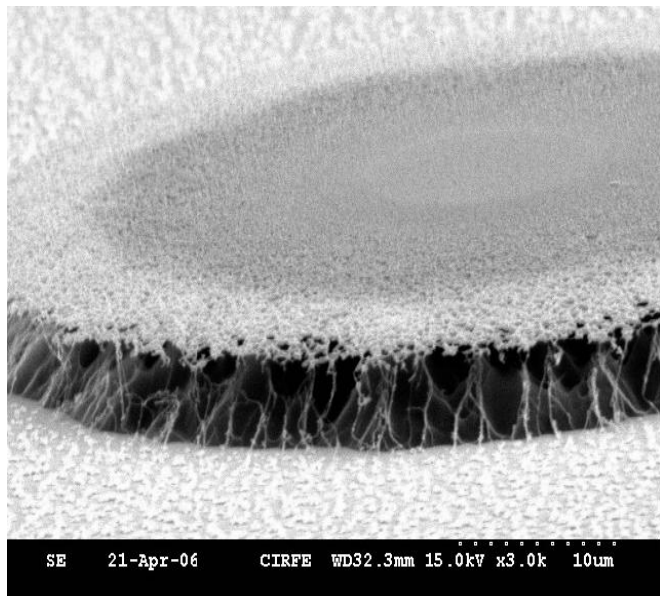


Figure B.6.10: SEM image of a $6\mu\text{m}$ -thick polyimide PI 2611 film etched in O_2 using a $1\mu\text{m}$ -thick SiO_2 mask. Pinholes developed in the SiO_2 due to a low selectivity RIE etch recipe causes a highly undercut film with rough edges. An Al etch mask consistently gives smooth edges with less undercut.

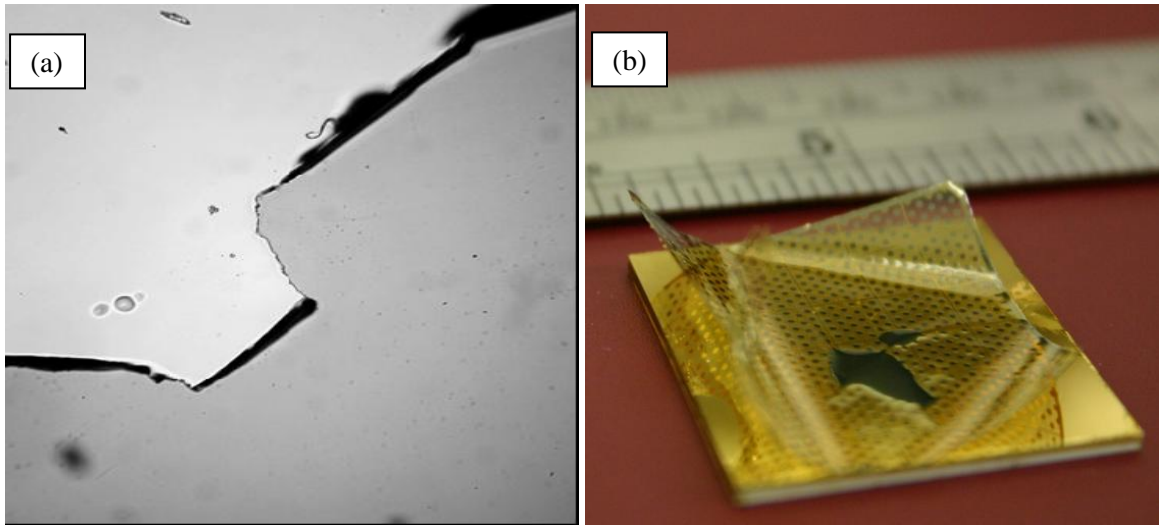


Figure B.6.11: (a) SEM image of a 1 μ m thick gold layer lifting off the polyimide PI 2611 film due to poor adhesion. (b) Photograph of a polyimide PI 2611 layer lifting off the gold again due to poor adhesion and absence of an adhesion layer.

Appendix C

Thin Film Resistor Characterization and Processing

Resistors are an essential part in any electrical circuit requiring current regulation, voltage division or a matched termination load. Implementing resistors with thin film metallization results in a physical structure with high power dissipation capability, small size, and optimal operating characteristics for both DC current and microwave signals. In general, there are four parameters of concern to the engineer when designing a resistor; the resistor value, its change in value over time, its change in value with temperature, and its power handling capability. Secondary considerations include the choice of resistor material and sheet resistivity.

As with any type of resistor, total resistance is determined by the Equation (C.1), where R is the total resistance (Ω), ρ is the bulk resistivity of the resistor material (Ωcm), L is the resistor length (cm), W is the resistor width (cm) and the t is the resistor thickness (cm).

$$R = \frac{\rho L}{wt} \quad (\text{C.1})$$

With thin film resistors, sheet resistance in units of ohms per square (Ω/\square) is often used to specify a film and is calculated using Equation (C.2).

$$R_{sheet} = \frac{\rho}{t} \quad (\text{C.2})$$

Where \square refers to the unit surface area of equal length and width. This approach permits easy calculation of the thin film resistor values as follows:

$$R_{total} = R_{sheet} \times \frac{L}{W} \quad (\text{C.3})$$

In general, sheet resistance can vary by 25% within a lot of material as a function of deposition environment, surface quality, substrate material and other factors. This reality dictates that resistors be laser trimmed to final values and is a preferred approach over “fired-to-value” requirements. Standard laser trimming achieves 10% tolerances on completed resistors while

tolerances of $\pm 1\%$ of design value are routinely achieved with proper resistor layout. Moreover, the deposition process, intrinsic material properties, and film stoichiometry all contribute to changes in resistance values as a function of temperature, a “dynamic” property. These changes are quantified by the temperature coefficient of resistance (TCR) given by Equation (C.4).

$$TCR = \frac{(R_2 - R_1)}{R_1(T_2 - T_1)} \times 10^6 \quad (C.4)$$

where R_2 and T_2 are the final resistance and temperature and R_1 and T_1 are the initial resistance and temperature, respectively. The thin film resistivity also highly depends on the surface roughness. Surface roughness of alumina substrates dominates the scattering of the electrons reducing their mean free path lengths and thus increasing the electrical resistivity of thin metallic films. As the thickness of the film increases, the effect of surface roughness on the resistivity decreases. Moreover, electron-beam deposited films have lower resistivity compared to the sputter deposited films because there is less oxygen and carbon contamination in the e-beam deposited films [71].

In EM simulations executed in Sonnet[®] and HFSS[™], the resistor was set to a metal type with sheet resistance equal to about 32ohms/square for 400Angstroms. Dimensions were determined and various resistor designs and areas were placed in an emulsion mask for characterization shown in Figure C.1. CIRFE’s thin film resistors are formed by lithographically patterning the high-resistance e-beam deposited Cr on the surface of an alumina substrate.

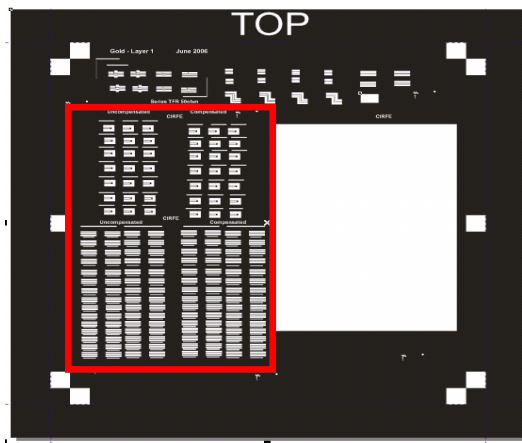


Figure C.6.12: Emulsion mask used for the design of series and shunt TFRs.

Initially two processes were considered for the formation of the Cr thin film resistors as shown in Figure C.2. The first process involved the wet etching of the adhesion layer to form the resistor outline. However, wet etching variation resulted in very ragged resistor outlines resulting in uncertainty in resistance values. The second process examined in Figure C.2(a) uses lift off of a second additional layer and is found to produce more reliable resistor geometries.

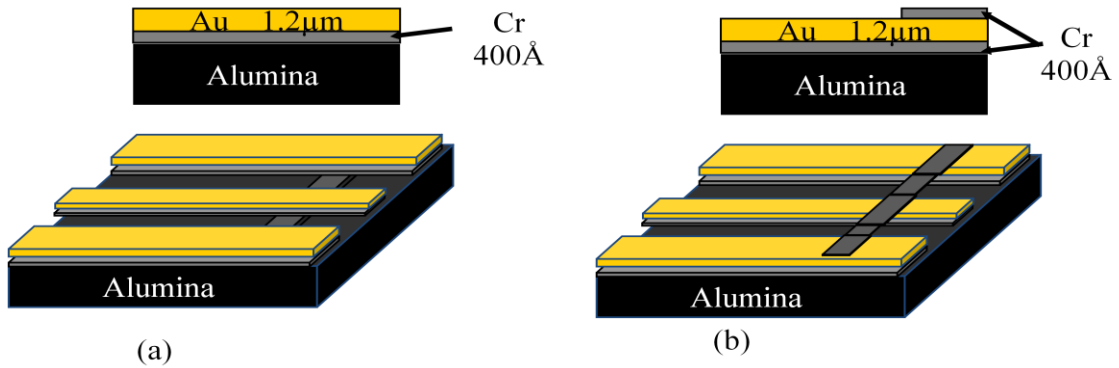


Figure C.6.13: Two types of resistors tested using (a) a wet etch process and (b) using lift off for higher reliability and repeatability.

Figure C.3 depicts the process flow used to produce the thin film resistors using lift off resist.

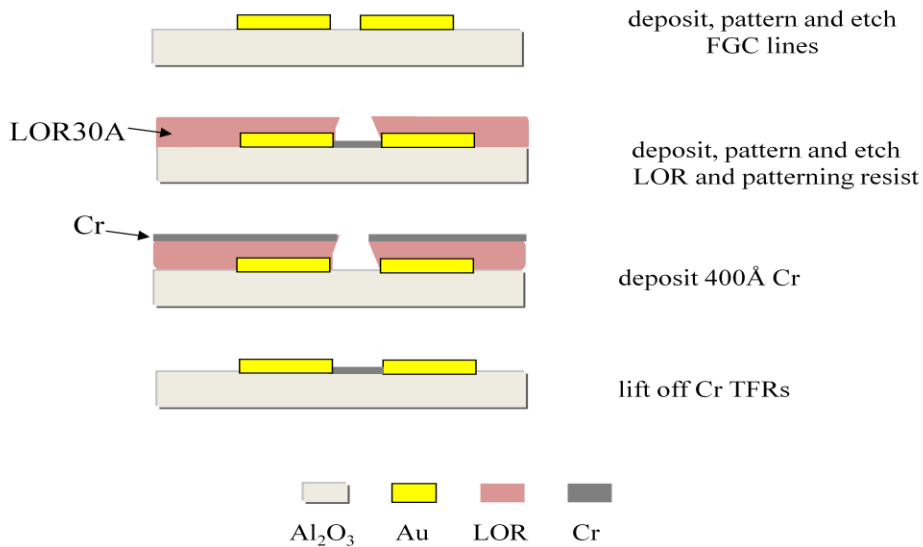


Figure C.6.14: Process flow for fabricated Cr thin film resistors.

Moreover, two types of resistors configurations were investigated. A resistor in series with the transmission line and a resistor shunt with the FGC line, as shown in Figure C.4 (a) and (b), respectively. The series thin film resistors were investigated to determine the correct dimensions for the isolation resistor to be used for the Wilkinson power divider designed. The series resistor configurations were investigated for use as termination loads to measure circuits with more than two ports using the Cascade prober station.

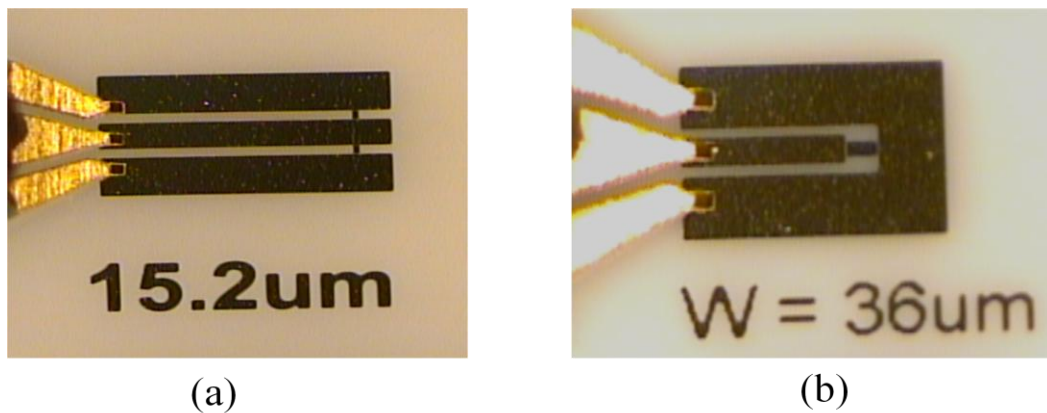


Figure C.6.15: Two types of resistors tested (a) a shunt parallel resistor, (b) a series resistor.

One port measurements are done using the cascade prober, where the transmission line effects were de-embedded from the measured results, for a better approximation of the resistor's resistance value. Figure C.5 shows the equivalent circuit and equation used to extract the resistor's approximate value.

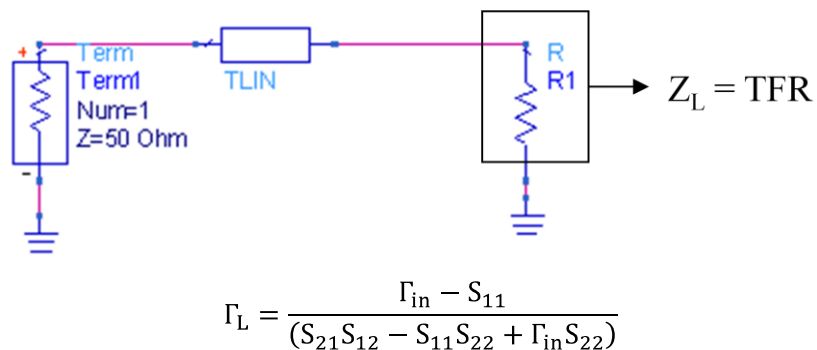


Figure C. 6.16: Equivalent circuit and equation used to extract the TFR resistance value.

The resistors were designed for their value over the X-band and the results obtained are listed in Table C.1 and a comparison of the simulated and measured response of the series resistor in Figure C.6.

Table C.1: Fabricated Cr thin film resistors.

100Ω Resistor			
Resistor Layout	Resistor Dimensions	FGC Dimensions	Resistor Value
Series	18um by 90um	S = 85um Gap = 24um Ground = 180um	R = 100.1Ω
Parallel	26um by 90um	S = 85um Gap = 24um Ground = 180um	R = 70.7 Ω
50Ω Resistor			
Resistor Layout	Resistor Dimensions	FGC Dimensions	Resistor Value
Series	12um by 32um	S = 80um Gap = 32um Ground = 120um	R=50.5Ω
Parallel	12um by 32um	S = 80um Gap = 32um Ground = 120um	R=52.37Ω

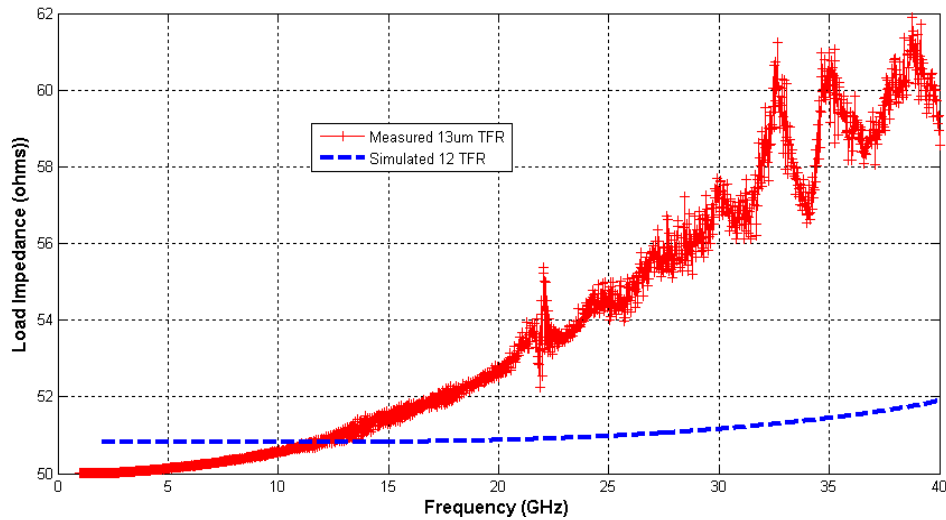


Figure C.6: Comparison of the simulated and measured series Cr 12μm wide TFR.

Cycling the CIRFE fabricated resistors through high temperature cycles, the resistance values varied. Placing a Cr resistor through 1 high temperature bake cycle at 250°C results in a increase in resistance by almost 2 times the original resistance. Placing the resistors through two high temperature cycles results in an increase 2.3 times of the original resistance. It is possible that the resistance increases as a result of oxidation of Cr during the high temperature cycles. Therefore, the use of Cr for thin film resistors is not applicable for this process because of the high temperature cycles highlighted in the 8-mask process shown in Figure C.7.

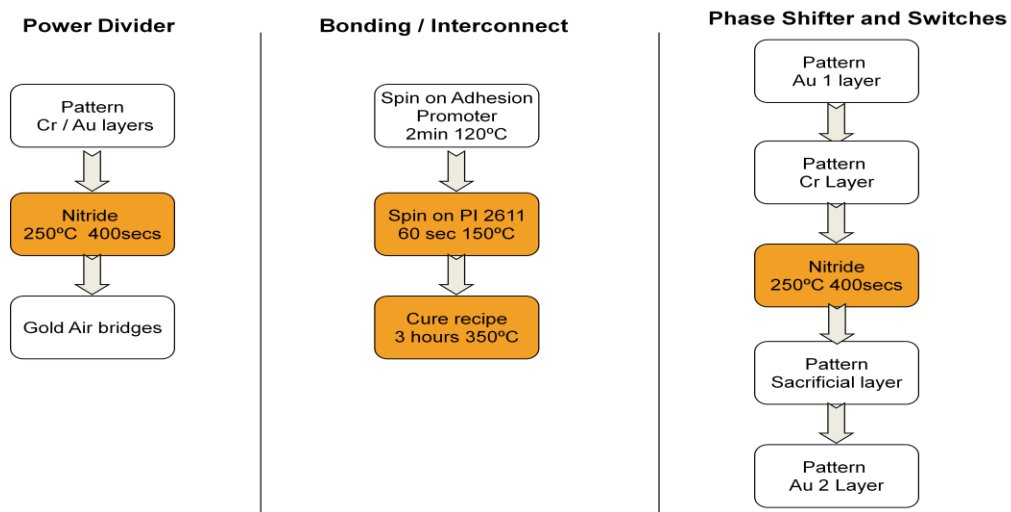


Figure C.6.17: High temperature steps present in the 8 mask process.

Both tantalum nitride (TaN) and nichrome (NiCr) resistor films are well characterized and their limitations are understood. Likewise, the deposition processes used to create these films have been described extensively in the literature. High frequency response thin film chip resistors from Vishay made of passivated NiCr material with a TCR ± 50 ppm were considered. An optimized laser trim is used to provide a balanced resistor with low internal parasitic effects. The resistor element is protected with overcoats designed for electrical, mechanical and environment protection. Deposition and integration of the films are well controlled to produce high precision resistors and the TCR characteristics of the film make it ideally suited for applications across a large temperature range, a requirement for the 8 mask process. This is the reason we decided to use hybrid chip thin film resistors.

The processing step details is as follows:

Step 1: RCA Clean Process

- 750ml DI water, 130ml Ammonium Hydroxide (27%), 130ml Hydrogen Peroxide at 70°C for 15min
- Rinse in DI water
- Dehydration bake at 120°C for 2min

Step 2: Gold and Chromium Deposition

- 400A Cr (e-beam evaporation)
- 1.2um Au (e-beam evaporation)

Step 3: Chromium Patterning

- AZ2035 Negative resist
- Spin at 4000rpm for 30sec
- Soft bake at 90°C for 2mins
- Exposure for 9sec
- Post exposure bake at 110°C for 60sec
- Develop for 45sec for 1mins
- Hard bake at 120°C for 4mins
- No descum
- Wet etching using 100% new Gold etchant 2mins 30 secs slight agitation
- Stripping the resist 65°C with EKC Dupont Stripper for 30mins
- Warm acetone 47 degrees ultrasonic bath agitation for 20mins

Step 4: First Gold Patterning

- LOR15A Spin at 2000rpm (2µm) for 30secs
- Soft bake at 150°C for 5 minutes
- AZ3312 Positive Resist
- Spin at 3000rpm for 30sec
- Soft bake at 90°C for 2mins
- Exposure for 10sec – with the new bulb
- Post exposure bake at 110°C for 60sec
- Develop for at least 3.5mins

Step 5: Deposit the Chromium layer

Note: the time between LOR hard bake and loading the samples into the Intel Vac for evaporating the resistive chromium layer must be minimized so no moisture uptake can occur. Therefore it is recommended Steps 4 and 5 be done on the same day. The Cr is deposited at 3Å/sec, therefore set the thickness to 0.04microns (i.e. 400Anstroms) and the time taken will be about 2mins 15secs for deposition.

Step 6: Lift Off to remove the LOR15A and AZ3312

- Follow the same steps as developed by CIRFE for Lift off
- Set hot plate to 75°C (between notch 3 and 4 on knob)
- Using two beakers for PG Remover A and B, warm up. Place the sample in Beaker A for 15mins with slight agitation.
- Then Place into Beaker B for 10mins with slight agitation
- Then take the sample and place in a Petri dish with IPA for a few mins (about 4mins)

List of Acronyms

RF	Radio Frequency
MEMS	Microelectromechanical Systems
ESA	Electronically Scanned Arrays
SPNT	Single-Pole N-Throw
FET	Field-effect Transistor
HRS	High Resistivity Silicon
MMIC	Microwave Monolithic Integrated Circuits
TTD	True Time Delay
DMTL	Distributed MEMS Transmission Line
PECVD	Plasma Enhanced Chemical Vapor Deposition
RIE	Reactive Ion Etch
ICP	Inductively Coupled Plasma
TFR	Thin Film Resistor
BFN	Beamforming Network
BM	Butler Matrix
PA	Power Amplifier
LNA	Low Noise Amplifier
LTCC	Low Temperature Co-fired Ceramics
HTCC	High Temperature Co-fired Ceramics
BCB	Benzocyclobutene
PI	Polyimide
SBR	Space-Based Radar
TCR	Temperature Coefficient of Resistance
CW	Continuous Wave
CPW	Coplanar Waveguide
FGC	Finite Ground Coplanar waveguide

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