Retrofit Control to Prevent ASD Nuisance Tripping Due to Power Quality Problems

by

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I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

Since the onset of automation, industry has relied on adjustable speed drives to accurately control the speed of motors. Recent advances have increased the number of adjustable speed drives hitting the market. The proper operation of the speed drives requires electrical supply with relatively high power quality which is not the case in most industrial facilities. Power quality problems such as harmonic, sag, swell, flicker, and unbalance can trip the speed drive with a wrong message, which is referred as a premature tripping. Although the power quality problems can be mitigated by using custom power devices, they are bulky and costly. Moreover, they themselves might adversely affect the operation of the adjustable speed drive. A comprehensive study done in this thesis presents the overlooked effect of the custom power devices on the speed drive stability. It is found that the speed drive system might trip due to its interaction with custom power devices. Obviously, it is vital to increase ASD immunity to premature tripping because of poor power quality or custom power.

This thesis offers fast, efficient and robust algorithms to achieve this immunity by retrofitting the ASD control unit and integrating the power conditioning function with the adjustable speed drive. Therefore, the power quality problem is mitigated and the drive system performance is significantly enhanced. Such integration requires the modification of the control unit by considering various elements such as envelope tracking, phase-locked loop, symmetrical component extraction, and the controller. Simple but robust and fast algorithms are proposed for such elements based on a newly developed energy operator algorithm. The developed energy operator and the developed algorithms overcome the drawbacks of the existing algorithms.

Acknowledgements

Looking back on my days at Waterloo, I realize that I am tremendously blessed by God Almighty to have the ability to withstand the pressure of graduate studies and to be able to complete this dissertation. I have been also blessed to have had teachers, friends, colleagues, and a family who have been providing me with guidance and support. I am fortunate to have had Prof. Magdy Salama and Assoc. Prof. Ehab El-Saadany as my research advisors. This thesis would have been difficult without their encouragement, support, and listening to my ideas even when they did not make sense. In Waterloo, many other professors motivated me on both the academic and the personal levels. In particular, I would like to acknowledge M. Aagaard, K. Bhattacharya, C. Gebotys, Y. Hegazy, and M. Kazerani.

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Having a work experience at Honeywell Aerospace has had a profound impact on my engineering track. I still remember the warm welcome from V. Le, L. Cheng, and their system team at Honeywell. I would like to thank C. Angel, S. Cino, R. Paton, and V. Nikolic for the tremendous help during my first steps at Honeywell. Thanks to Venky, I can speak Indian now. I am at a loss of words to express my gratitude to my Canadian mother, Betty Anne for the love and the support during my first days in Canada. Spending years away from home would have been hard without Bettey's love. I am lost of words to describe Huda and Amin, my mother and father, but the best description for them is my mum and my dad. Mahmoud and Ahmed, my wonderful brothers, have been there for me whenever I needed them. I feel fortunate to have them always standing by my side. Samira and Dr. Abdel Hamid are the best sister and brother in law.

Dedication

This thesis is dedicated to my parents, my grand pararents and my family, whose encouragement have meant so much to me during the pursuit of my graduate degree and the composition of this thesis.

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Chapter 1

Introduction

1.1 Background

Typically, industrial machinery is driven by electric motors that have provisions for speed adjustment. An Adjustable Speed Drive (ASD), also known as a Variable Speed Drive (VSD), is nomenclature for the power electronic equipment used to control the speed of machinery. The incorporation of incremental features and functions in digitally-controlled drives is here to stay as suppliers attempt to further exploit the potential of the technology. This situation is increasing the number of ASD hitting the market, that boost the performance of the drives. However, overlooking the effect of the electric service source quality on the ASD, culminate substantial financial losses in terms of defected products, process shutdown, or system reset [4].

An ASD consists of a power electronic circuit for adjusting the magnitude and the frequency of the voltage applied to the motor [2]. The most popular circuit is the rectifier-inverter topology, which is connected to the three-phase utility supply through a rectifier circuit [3].

Most nonlinear loads interfere with the utility supply and cause Power Quality (PQ) problems which, in turn, affects the ASD operation. A PQ problem is any deviation of voltage, applied to the equipment, that results in damage or misoperation of electronic

equipment or other electrical devices. Some common symptoms of PQ problems in ASD systems are [4], [5], [6], [7], [8]:

- The ASD prematurely trips or shuts down.
- The ASD resets or restarts.
- The motor, operated by the ASD, requires frequent repairs or replacements.
- The erratic control of process parameters.
- The unexplained fuse blowing and/or component failures.
- The frequent motor overheating trip and/or continuous operation of the motor cooling system.

If the ASD is detrimentally affected by those symptoms, PQ monitors are usually installed to monitor the distribution system to assess the PQ level in it and to analysis the PQ problem. Although, the entire distribution system monitoring is costly, it is essential to determine whether or not the ASD trips are due to PQ problems.

One approach to avoid ASD tripping is to mitigate the PQ problems by using custom power devices such as DSTATCOM [9]. However, they are bulky as well as costly and can affect the ASD operation [10], [11], [12].

Another approach is to use the forced commutated rectifier of the ASD itself to mitigate the PQ problems at the Point of Common Coupling (PCC) [13], as the forced commutated rectifiers will allow a bidirectional power flow. This requires retrofitting the ASD control to accommodate tracking and to mitigate the PQ problem. Instantaneous, fast, stable, and robust algorithms, including envelope tracking, PLL, symmetrical component extraction, to track the PQ problem are essential to ensure robust operation of the ASD.

Although the use of the forced commutated rectifier to mitigate only the harmonics at the PCC has been discussed [14], [15], [16], the use of the ASD rectifier to mitigate voltage sag, swell, flicker, and unbalance has not addressed yet.

1.2 Objective

The primary objective of this thesis is to immunize the ASD structure against the premature tripping due to PQ problems by retrofit control algorithms of the ASD. Three tasks are undertaken as follows:

1. Develop a method to monitor the distribution system at minimum cost to accurately assess the PQ in the distribution system
2. Study the effect of the DSTATCOM on the ASD stability limits to highlight the overlooked effect of the DSTATCOM on the ASD operation.
3. Define and design the control unit of the ASD rectifier to integrate the mitigation of sag, swell, flicker, and unbalance function by doing the following:
   (a) Develop a voltage envelope tracking algorithm, based on an energy operator, to track sag, swell and flicker
   (b) Apply the developed energy operator to build PLL circuitry and study its digital implementation
   (c) Introduce an unbalance tracking algorithm and unbalance mitigation technique
   (d) Derive a robust controller in terms of system uncertainties, and motor speed and torque variation
   (e) Integrate the novel algorithms in the control unit of the rectifier with a power conditioning function

1.3 Outline of The Thesis

The outline of the thesis is illustrated in Fig. 1.1. This thesis consists of ten chapters.

Chapter 2 presents a survey on the effect of PQ problems on the ASD and survey the rectifiers circuit topologies used in the ASD. .

Chapter 3 provides an economic method to monitor the distribution system with optimized the number of the PQ monitors.

Chapter 4 examine the effect of the DSTATCOM on the ASD stability boundaries along with a mathematical analysis of the results.

Chapter 5 provides a description of a new computational method for the Energy Operator (EO) that is used for envelope tracking, PLL, and symmetrical component extraction. The theory and mathematical derivation of the algorithm as well as the design steps for the hardware and software implementation are detailed.

Chapter 6 purposes a PLL circuit, based on the EO introduced in Chapter 5. The idea behind the proposal and its advantages over existing PLL techniques are outlined. The digital implementation of the PLL using FPGA is discussed and the laboratory tests to validate the outstanding performance of the proposed circuit is presented.

Chapter 7 provides an algorithm for fast Symmetrical Components Extraction (SCE), used in unbalance mitigation, utilizing the energy operator algorithm. In addition, a new control technique for unbalance mitigation using voltage control rectifier is introduced.

Chapter 8 consists of the application of the sliding mode control theory as a robust controller for the rectifier. The controller overcomes the uncertainties in the system model.

Chapter 9 proposes a Self Immune Rectifier (SIR) which combines the rectification function and power conditioning function. The SIR is more friendly to the distribution system regarding to PQ and saves the cost of custom power devices. The circuit topology as well as the previously developed algorithms and the operation of the SIR are elaborated in this chapter. In addition, a simple study of the SIR economics are provided.

Chapter 10 summarizes the work presented in this thesis and provides a road map for future work.

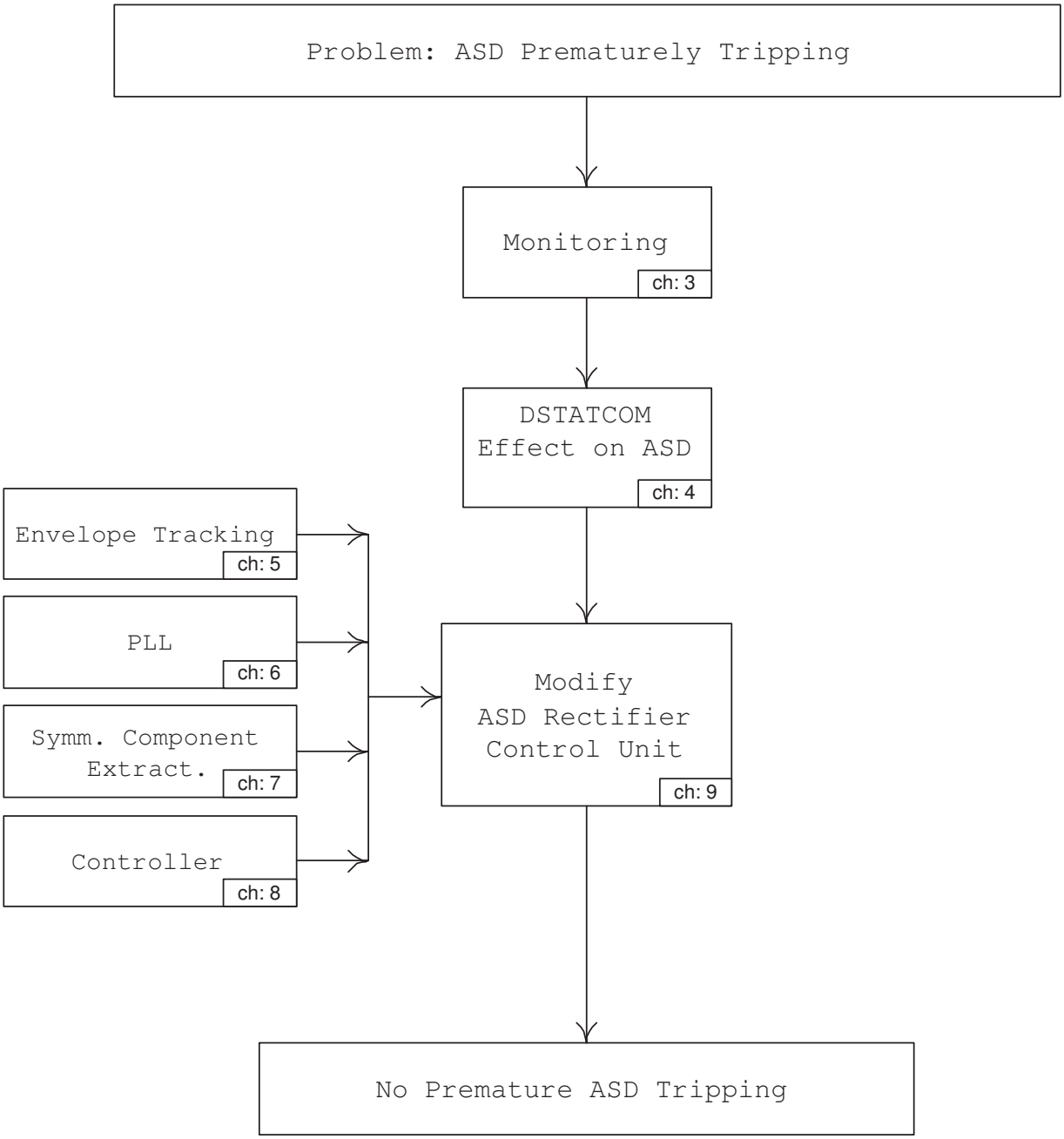

Figure 1.1: Thesis outline

Chapter 2

Background

2.1 Introduction

In this chapter, the effect of the PQ problems on the operation of the ASD will be briefed. Since the ASD is interfaced with the utility via its rectifier, the rectifier circuit topologies used in the ASD are included to demonstrate their effect on PQ problem mitigation.

2.2 Effect of the PQ on the ASD Operation

PQ problems such as sag, swell, harmonic, flicker, and unbalance can instigate premature tripping of the ASD. Voltage harmonics cause motor heating, resulting in the continuous operation of the motor cooling system. If the cooling system is unable to cool down the motor, the ASD trips due to overheating.

Voltage sag and swell, at the AC side, will create a voltage dip and swell, at the DC bus of the ASD [17]. As a result the drive trips, stoping a process no matter what the torque-speed profile of the load is. The result is the need for a restart [18].

Steady-state voltage unbalance has a significant effect on the current unbalance and harmonics of PWM based ASDs. The research to determine the PQ characteristics of ASDs demonstrates that, given a small voltage unbalance, the input current unbalance

of the ASD can be high [19]. Generally, the findings indicate that as the electric service supply voltage unbalance increases, the ASD input current unbalance increases from a nominal 10% up to 50%, depending on the ASDs internal reactance and the electric service impedance. This results in a pulsating torque which triggers the ASD protection leading to ASD tripping [20].

The system in Fig. 2.1 is used to illustrate the effect of the voltage sag and flicker on the operation of the ASD. This system consists of a nonlinear load and an ASD connected at the PCC.

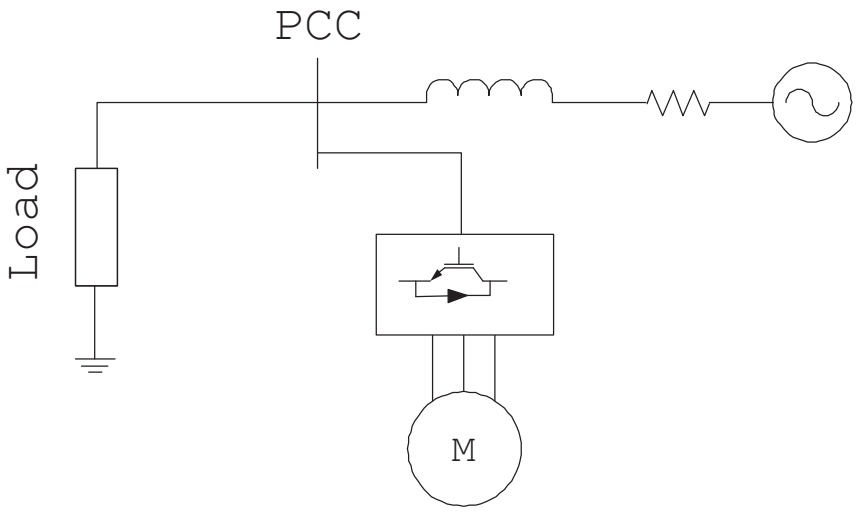

Figure 2.1: System used to study the effect of PQ problems caused by a load at the PCC

2.2.1 Effect of the Voltage Sag

A study of voltage sag effect can be done analytically or in the time domain, by using dynamic load models mainly designed for stability analysis. Keeping the motor connected to the supply during voltage sags and short interruptions, rather than disconnecting and re-starting the motor, is advantageous from the system operation prospective point view [21]. Consequently, examined in this thesis, the is not disconnected during a voltage sag.

The system, Fig. 2.1, is subjected to a voltage sag that is simulated as a load increase causing a voltage dip of 30% for 100ms starting after 1.5 second. Figure 2.2 exhibits that as the voltage drop at 1.5 second, the speed begins to decay and drop. When the speed drops, within a short time, the entire production process can be disrupted. Depending on the set-point of the under speed protection, the ASD drops, interrupting the industrial process. Usually, the speed drop is a function of the sag level, duration, motor inertia, DC link capacity, and mechanical load at the moment of sag [6].

A closer look at the ASD current (I_{ASD}) and the motor stator current (I_{stator}) in Fig. 2.2, conveys that the stator current begins to decay, eventually causing the speed to decay as well. However, the ASD current is zero because the DC voltage at the DC link is higher than the equivalent input AC voltage. Therefore, the voltage sag is usually followed by an instantaneous DC overvoltage and a AC over-current which can destroy the devices in the power path. In fact, the overvoltage level can even trigger the overvoltage protection of the ASD causing the premature tripping.

2.2.2 Effect of the Voltage Flicker

The system, in Fig. 2.1, is subjected to voltage flicker simulated as a nonlinear loads causing a voltage variation of 10% with a modulation frequency of 4 Hz. As Fig. 2.3 illustrates, the speed fluctuates due to the variation of the DC link voltage, caused by the flicker at the PCC. The speed variation is a function of the voltage magnitude variation and modulation frequency; both vary randomly. These variations in the speed affect the process in terms of defective products. For example in the textile industry, variation in the speed deteriorates the fibre roll resulting in substantial economic losses [18]. Printed Circuit Board (PCB) industry is particularly affected by voltage variations; in fact, voltage flicker is one of the most known causes of defective products that require rework.

Another effect of voltage flicker is an unwanted pulsating torque due to the fluctuation of the speed. Figure 2.3 shows the electromagnetic torque (T_{EM}) of the motor, pulsating as the speed varies.

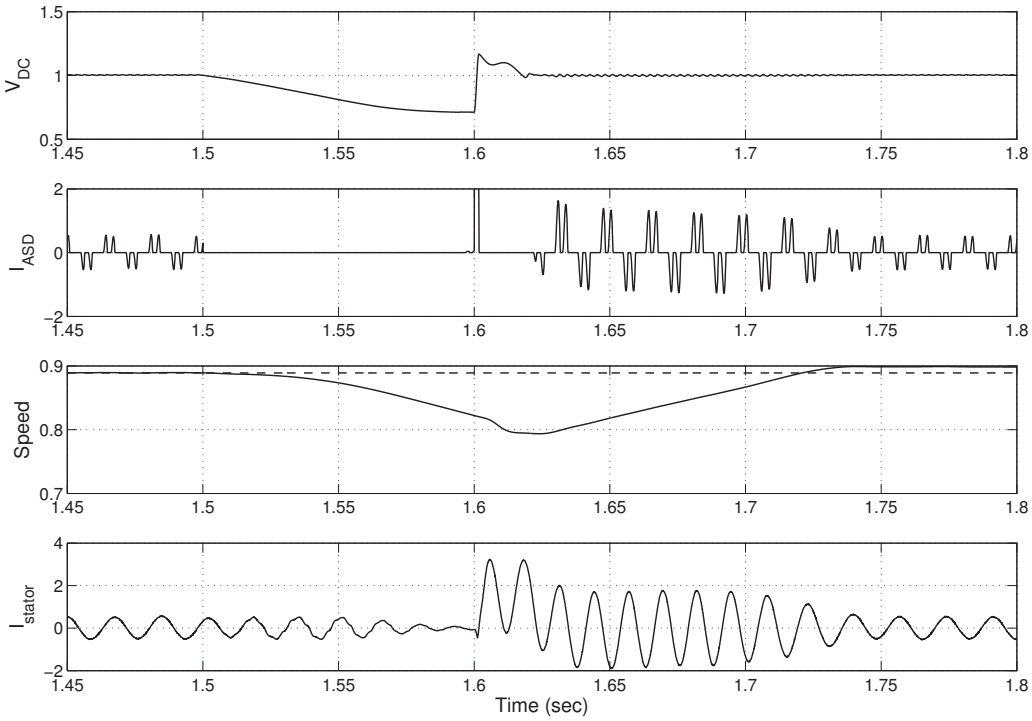

Figure 2.2: Effect of voltage sag on the ASD

Since the ASD is connected to the PCC through the ASD's rectifier, the following sections describe the ASD circuit topology and to mitigate the PQ problems.

2.3 Adjustable Speed Drive

The ASD circuit consists of four parts: rectifier, DC link, inverter, and motor. ASDs can be categorized in different ways. Based on the driven motor, ASD can be categorized as DC ASDs and AC ASDs [22]. Since the majority of ASD in the industry is the AC ASD, this study will focus on AC speed drives. In terms of the chosen topology, the ASD can be categorized as a current source ASD or voltage source ASD, as shown in Fig. 2.4 and Fig. 2.5, respectively. Since the ASD interfaces with the utility by a rectifier, its controller

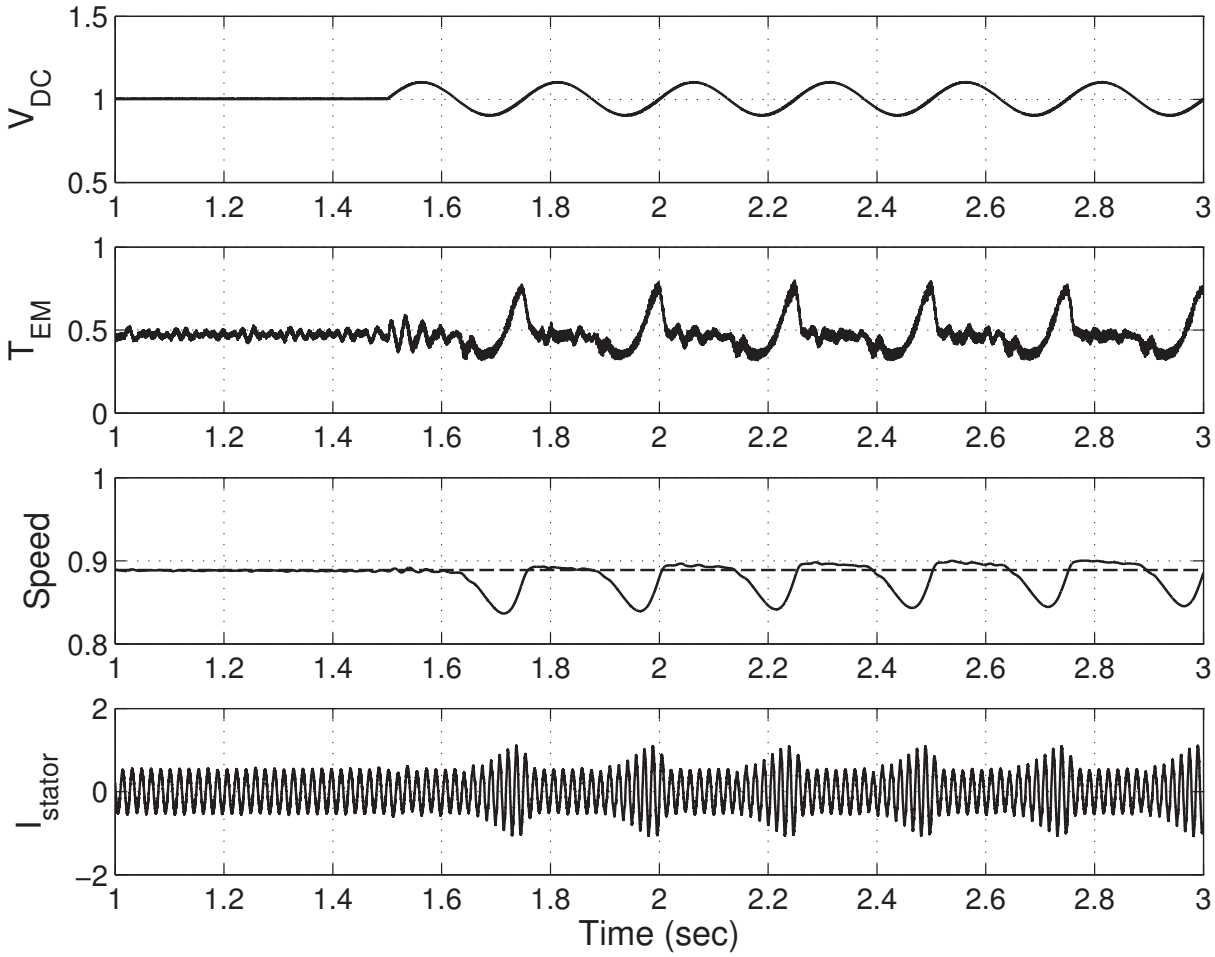

Figure 2.3: Effect of voltage flicker on the ASD

will be retrofitted to mitigate the PQ problems. Therefore, it is essential to highlight the rectifier circuit topology and control topology in the following sections.

2.3.1 Rectifier Circuits Topology

Voltage source ASD uses a voltage source rectifier in the rectifier circuit, while current source ASD uses a current source rectifier in their rectifier circuit.

The Voltage Source Rectifier (VSR), in Fig. 2.4, consists of six power switches to rectify the voltage at the DC link to the inverter. The inverter chops the DC voltage at the DC

link to supply an AC voltage to the motor.

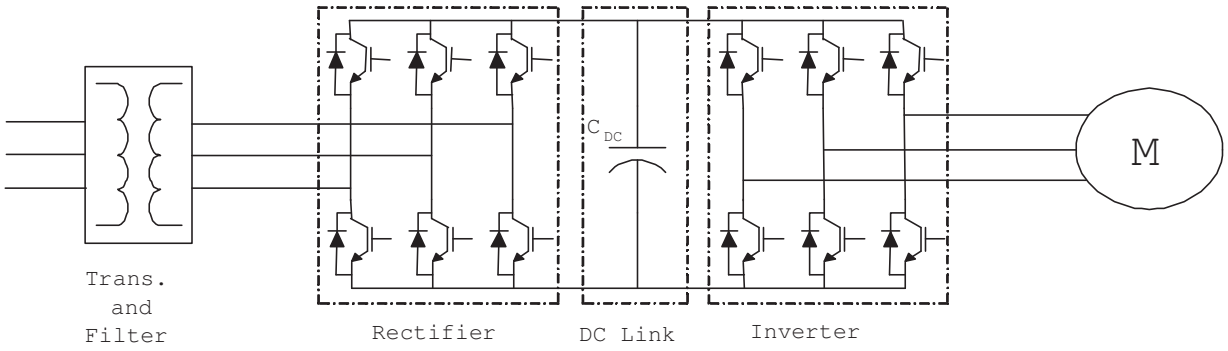

Figure 2.4: Voltage source rectifier and ASD

The current source rectifier, exhibited in Fig. 2.5, also consists of six power switches along with a DC inductor as the DC link. The inverter chops the DC current from the DC link to supply the current to the motor.

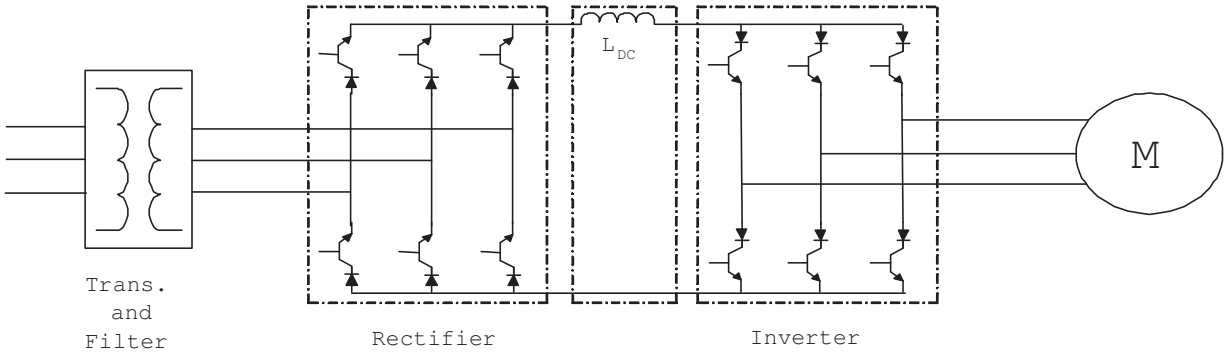

Figure 2.5: Current source rectifier and ASD

The practical implementation of current source drive systems with on-line control capabilities is more complex than the implementation of VSR, due to the gating requirements of the current source [23], [24]. In addition, the bulky size and heat dissipation of the DC link inductor are higher than those of the capacitor [25]. This has resulted in the widespread use of the voltage source topology rather than the current source topology. Consequently, this study focuses on the VSR.

2.3.2 Control Algorithms of the VSR

The conversion from AC voltage to DC voltage can be achieved if the IGBTs in the rectifier circuit are switched based on PWM [26]. PWM requires pattern signals that can be compared carrier triangle signals to determine the switching of the power electronics [23]. Three pattern signals are required for the three phases. If the pattern signals have the same frequency as the utility frequency, the power flow between the utility and the rectifier can be achieved with harmonic free current [27]. As a result, a control unit is required to generate the three pattern signals, u_{abc}, for the PWM.

The idea of the VSR is to maintain the DC link voltage at a desirable reference value by using a feedback control loop, as denoted in Fig. 2.6. This is accomplished by controlling the active power flow of the PWM rectifier [28]. In fact, the reactive power flow does not affect the DC voltage, so that there is no need to draw reactive power from the utility, and the rectifier can work at the Unity Power Factor (UPF) [16], [29].

As shown in Fig. 2.6, the control unit consists of the five blocks:

1. The measurement block that receives the current signals from the Current Transformers (CTs) and the voltage signals from the Potential Transformer (PT) at the PCC. The block extracts the required signals, such as the Power Factor (PF), Reactive Power (Q), or any other signals as required.

2. The controller block which computes the command signals to maintain a constant DC voltage and UPF operation of the rectifier.

3. The abc-conversion block generates the pattern signals, u_{abc}, from the output of the controller.

4. The PLL circuit synchronizes the pattern signals with the voltage at the PCC.

5. PWM circuit block.

The VSR can be controlled in either a Current Control (CC) mode or a Voltage Control (VC) mode [25]. In both modes, the control unit measures the voltage at the DC bus,

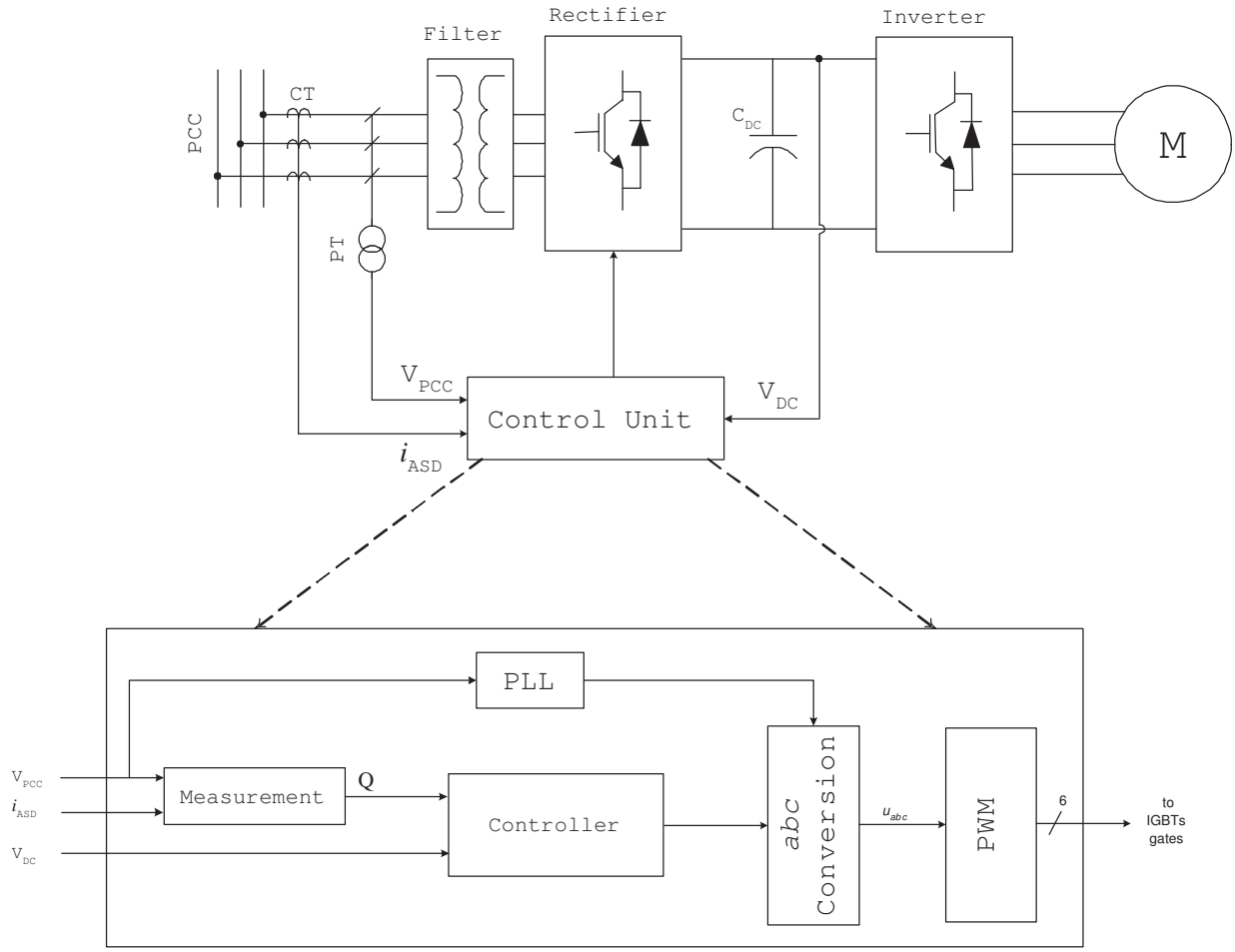

Figure 2.6: Block diagram of the PWM rectifier control unit

and controls the active power flow accordingly; while the reactive power is kept zero to maintain the UPF. However, the idea of controlling the power in both topologies is different as discussed in the following subsections.

2.3.2.1 Voltage Control Rectifier (VCR)

The concept behind the voltage controlled mode is to control the VSR as a voltage source. It is characterized by the voltage magnitude, frequency and shift-angle; therefore, it is necessary to determine these parameters [16]. The idea is to control the power flow between

two voltage sources, namely the VSR and the utility, connected together through a filter inductance. The filter resistance is neglected, since it is too small, compared with the inductance.

It is well known that the active power flow between two voltage sources is controlled by the shift-angle between them, whereas the reactive power flow is controlled by the voltage magnitudes [24]. If the voltage at the PCC is used as a reference, the VSR voltage angle and magnitude can be used to control the power flow. Consequently, two controllers are required, the first to regulate the voltage at the DC bus by controlling the VSR voltage angle, and the second to maintain a null reactive power.

A function block diagram of the voltage control VSR control unit is denoted in Fig. 2.7. Two Proportional-Integral (PI) controllers are required to control the power factor,PI_{PF}, and to regulate the DC voltage PI_{DC}, respectively [28]. The output signals are the voltage shift angle and the magnitude, which are employed to control the PWM indices (ϕ_{PWM} and m_{PWM}). The two indices are required to compute the *abc* pattern signals, u_{abc}, in the abc-Conversion block, which must be synchronized with the PCC through a PLL. The signal, u_H, is related to the harmonic mitigation, which is discussed in Section 2.3.3.

2.3.2.2 Current Control Rectifier

Since the VSR must be controlled as a current source, the currents injected by the VSR must also be managed. This task is readily achieved, if the rectifier is modeled in a rotating frame of reference (dqz) rather than a fixed frame of reference (abc) [23]. If the voltage at the PCC is adopted as a reference and a constant value, then the d-component and the q-component of the rectifier current indicate the active and reactive power, consequently [30].

Two controllers are required to control the current d-component (i_d^*) and q-component (i_q^*) of the VSR, as signified in Fig. 2.8. The abc-currents are computed by using the dqz-currents from the controllers. The abc-currents are converted to voltage signals in the Current-Compensator block since the PWM receives the pattern signals as a voltage signals only. The signal, adopted i_H, is related to the harmonic mitigation and elaborated

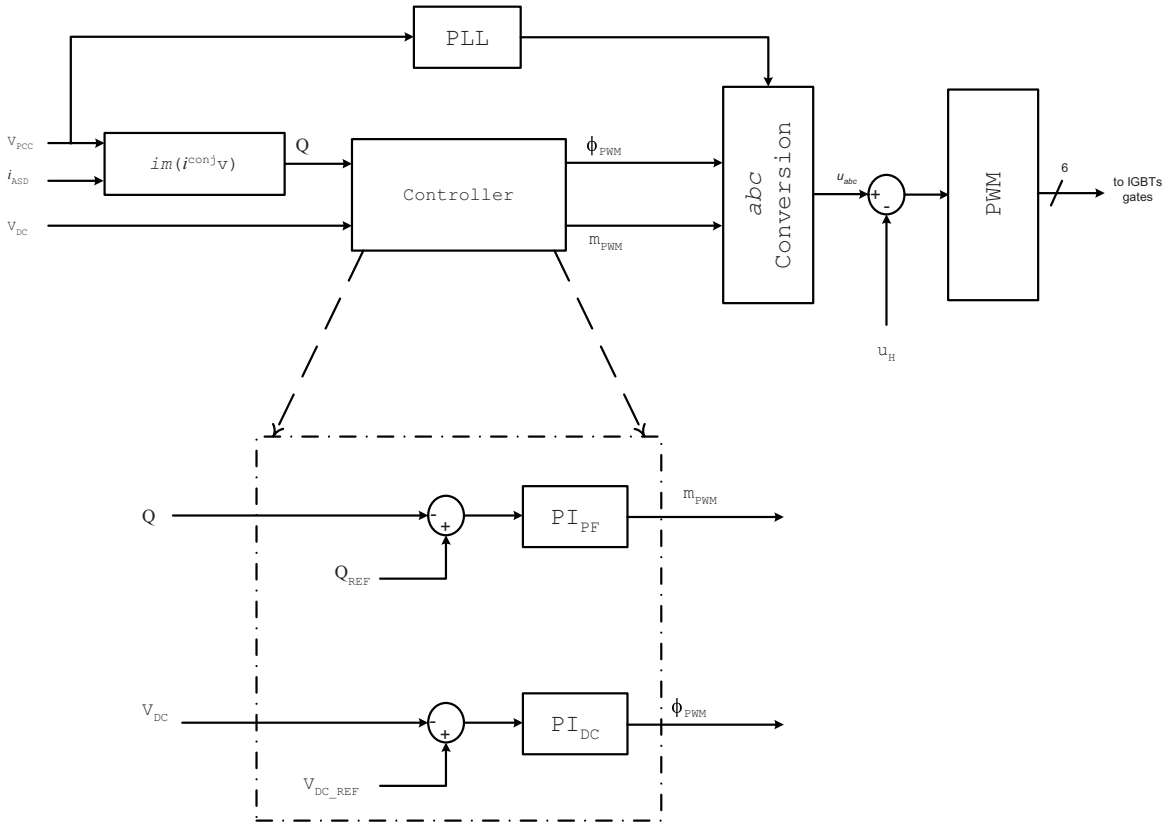

Figure 2.7: Voltage control rectifier

on Section 2.3.3.

2.3.3 Harmonic Mitigation Using The Rectifier

Figures 2.7 and 2.8 show signals u_H and i_H, respectively. They are used to reshape the PWM-reference signals to inject harmonics into the system. As‘a result, it has been suggested to inject harmonic currents by the VSR in such a way that the injected harmonics cancel the harmonics, caused by the nonlinear loads connected at the same PCC [14], [15], [31], [32]. In this case, the harmonics are mitigated by the VSR, and there is no need for an Active Power Filter (APF). In fact, the harmonic mitigation is carried out by injecting a reactive power, which does not affect the control loop of the DC voltage.

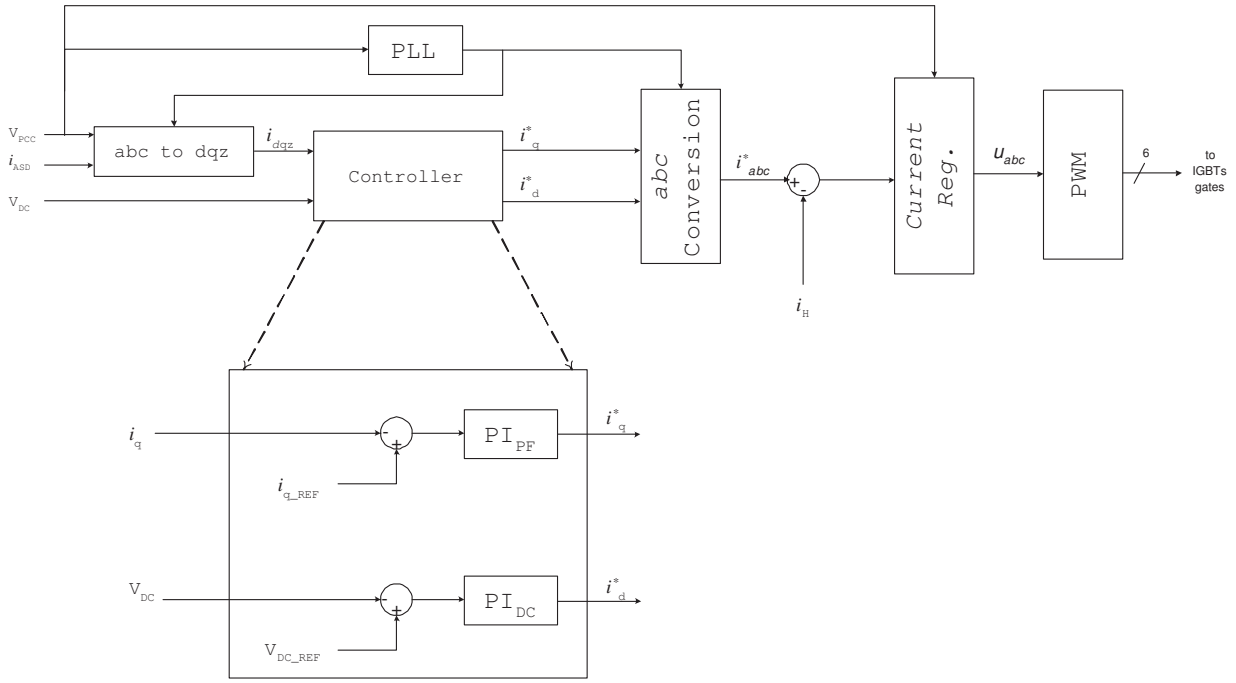

Figure 2.8: Current controlled rectifier

When the rectifier behaves as an APF, the current transformers must be located to measure the utility supply current, not the rectifier current. Since the rectifier does the filtering, there is an increase in the power electronic rating, as well as in the DC capacitor.

2.3.4 Rectifier with The Lead Power Factor Operation

Figures 2.7 and 2.8 show that the rectifier is working at the UPF by equating Q_{REF} to zero and i_{q-REF} to zero, respectively. However, the lead power factor operation of the rectifier can be achieved by equating Q_{REF} or i_{q-REF} to a positive value to allow the rectifier to supply a reactive power to the utility [33], [32], [31], [34].

2.4 Proposal of The Rectifier with Power Conditioning

Active filtering has been integrated successfully to the PWM rectifier, where the algorithms used in the APF have been adapted and implemented to the rectifier. Other PQ problems, such as sag, swell, flicker, and unbalance, can be mitigated by the rectifier due to its capability to inject reactive power, but this has not been addressed yet.

The basic elements of the Rectifier Control Unit (RCU) with the power conditioning function are depicted in Fig.2.9. Although harmonic mitigation is not addressed in this work, extra signals can be added for harmonic mitigation as shown in Chapter 9. The RCU shall mitigate voltage at the PCC and maintain the DC voltage constant by controlling the PWM reference signals. Therefore, the RCU senses the voltage at the PCC and at the DC bus.

The first step in the control is to extract the PQ problem sag, swell, flicker, and unbalance. After the required reactive power is determined by the controller, the PWM is synchronized with the voltage at the PCC by PLL.

For extraction purposes, a new algorithm has been developed for the Envelope Tracking (ET) by using an EO and is utilized for the PLL circuit, and the Symmetrical Component Extraction (SCE). Due to the nonlinearities and uncertainties in the power system, a robust controller based on the Sliding Mode Controller (SMC) is proposed. The pattern signals to the PWM circuit are produced by a Pattern Signal Generator (PSG). These algorithms will are examined in details in the following chapters.

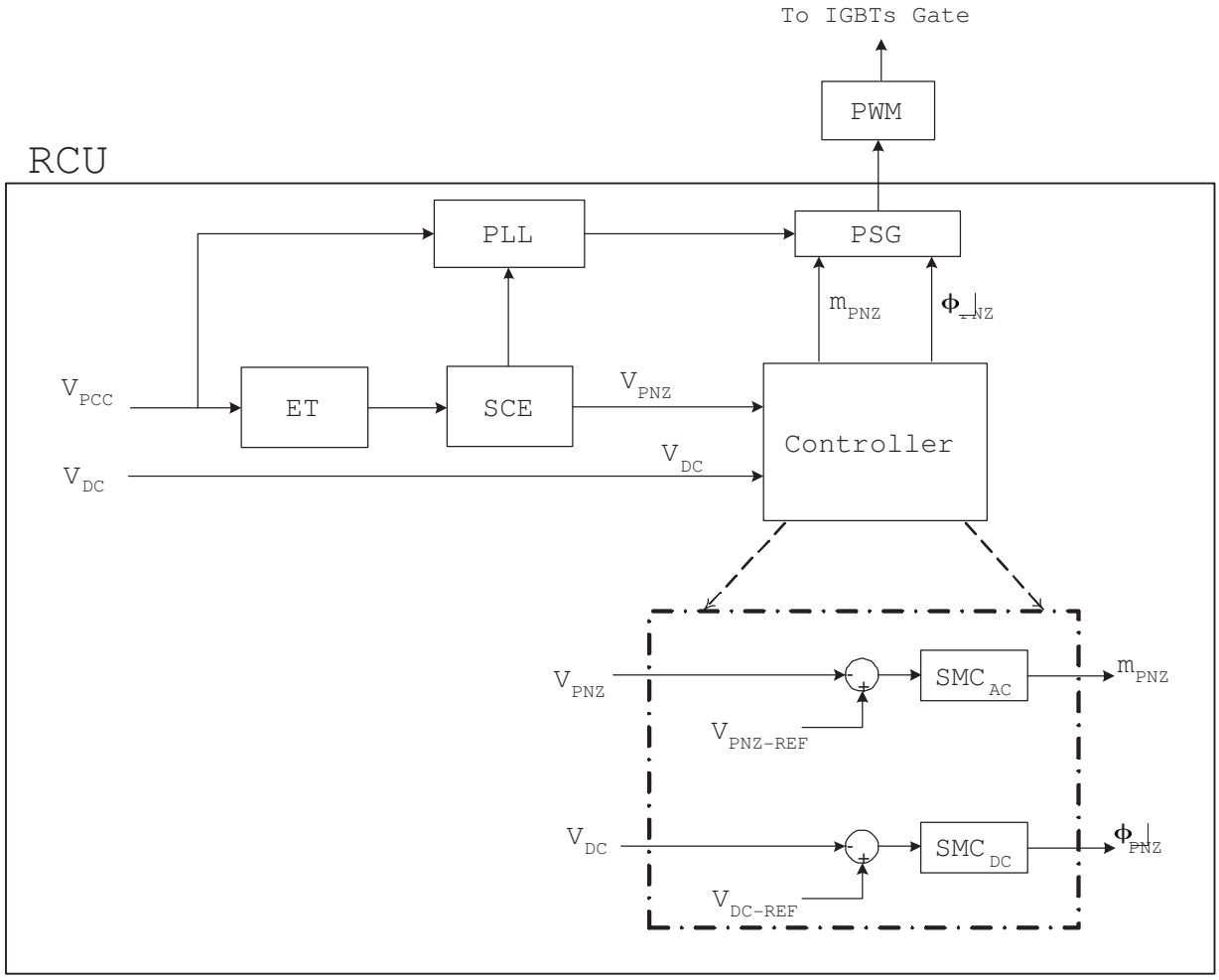

Figure 2.9: Rectifier Control Unit (RCU)with the power conditioning function

Chapter 3

Optimum Power Quality Monitoring Allocation

The first step in this thesis is to monitor the entire distribution system to assess the PQ problems. Since this is costly, there is a need to optimize the number and location of the PQ monitors.

3.1 Introduction

Although the voltage and the current can be monitored at a single bus at a reasonable cost, the recent trend is to move away from monitoring one bus to monitoring the whole system [35]. Such monitoring system can aid in many applications such including system diagnosis, locating the events, sharing information among remote sites, studying the propagation of the problems in the system, evaluating the PQ cost effect, and enhancing predictive maintenance programs [36].

Monitoring a system faces two key problems. The first is the communication among the remote sites while the second is the high cost of the monitoring system itself. To solve the first problem, recent advances in Internet communication and real-time applications have been adapted to monitor the entire power system. Reducing the cost associated with

the monitoring procedure can be achieved by three different methods: 1) reducing the cost of the PQ monitors, 2) optimizing the number of PQ monitors to be installed, and 3) combining both. Although the first aspect is addressed in a number of publications that try to reduce the cost by using the Distributed Monitoring Scheme [37], [35], [38], [39], the second and the third aspects have not been thoroughly addressed. This chapter concentrates on reducing the cost associated with the monitoring system through the reduction of the number of installed monitors.

A novel algorithm is introduced to determine the optimum allocation of the PQ monitors to reduce the cost of the distributed monitoring system, taking into account data redundancy. The algorithm depends on installing a number of Power Quality InfoNodes (PQINs) to measure a pre-determined number of currents and voltages, so that the remaining currents and voltages can be calculated. As a result, all the system currents and voltages are observable. The optimization problem is formulated as a covering and packing one, which can be manipulated by integer linear programm algorithms. The appropriate constraints are deduced from the electrical circuit topology, independent of the load parameters. In addition, the problem is adopted to a general form which can be implemented by any optimization package.

3.2 Distributed Power Quality Monitoring (DPQM)

To carry out the PQ analysis of a system, the instantaneous waveforms of all the voltages and the currents throughout the network should be available [40], [39]. Therefore, PQ monitors should be installed at each bus to measure its currents and the voltages at each bus. Then, the captured data are sent to a server for further analysis [41]. The design of such a system requires the analysis of two schemes: the centralized and the decentralized measurement systems. Although the central system is simpler to implement, it is unreliable due to a dependency on the central unit. Therefore, it is preferable to utilize the decentralized system, where the control is distributed among a number of units and the

central unit plays a smaller role [38], [42].

3.2.1 Proposed Method

Distributed measurement architecture depends on monitoring some voltages and currents by using a Power Quality InfoNode (PQIN), and on computing the other voltages and currents. The problem of determining the number and the location of the measuring devices, which are the PQINs, is known as observability analysis. To conduct such an analysis, the entire system parameters, the transmission line, the transformer, and load parameters need to be known in advance [43]. In an electrical power system, although the transmission line and transformer parameters are known the load parameters are not. It is logical, then, that for the observability analysis of the power system, the circuit topology is relied on to avoid a dependency on the load parameters [43]. In this chapter, the optimization problem is formulated in the form of covering and packing, where the density matrix is deduced in relation to the circuit topology.

Although the models accuracy of the power system's elements, such as the transformers and transmission lines, will not affect the allocation of the PQIN, it does have influence on the accuracy of the estimation method. From a practical point of view, accuracy is important to monitor the bus voltage either by direct measurement or by estimation regarding an acceptable accuracy level. The voltage at the non-measured buses can be accurately estimated by using one of the estimation methods that deals with system uncertainties such as the Weighted Least Square method or Kalman's Filter [44], [45]. Typically, the models and estimation method should be chosen to ensure accuracy.

Since during and after a short circuit, the circuit topology changes, the observability of the system will change as well. This situation is known as a power system observability contingency [46]. Different methods are suggested to deal with it and can be adopted in the new method [47], [48].

3.2.2 PQIN Description

The PQIN depicted in Fig. 3.1, consists of the appropriate transducers, depending on the voltage or current levels, that capture the voltage or the current signal in the analogue form. The analogue signal is digitalized by a Data AcQuisition (DAQ) at a suitable sampling rate and resolution [49], [50]. The components of such a setup are divided into the hardware and software. The hardware consists transducers, DAQ card, computers or signal processor setup, and facility to send this data to the server. The software consists of dynamic state estimation, PQ events detection, classification, location etc., and Graphical User Interface (GUI).

According to this configuration, the cost of PQIN is defined as

$$C(j) = C_{tran} + C_{DAQ} + C_{PC} + C_{com} + C_{sw} \tag{3.1}$$

where C_{tran} is the cost of the transducers, C_{DAQ} is the cost of the DAQ, C_{PC} is the cost of the computer, C_{com} is the cost of the communication facility and C_{sw} is the cost of the software divided by the number of PQINs.

The cost of a PQIN varies according to the following

- The number, sensitivity and the accuracy of the transducers.
- The sample rate. and the resolution of the DAQ.
- The communication method.
- The cost of the software, for the system.

3.2.3 Communication Between The PQINs

Different power system communication methods and protocols have been used to transfer data and information through the power system. These methods can be wireless such as

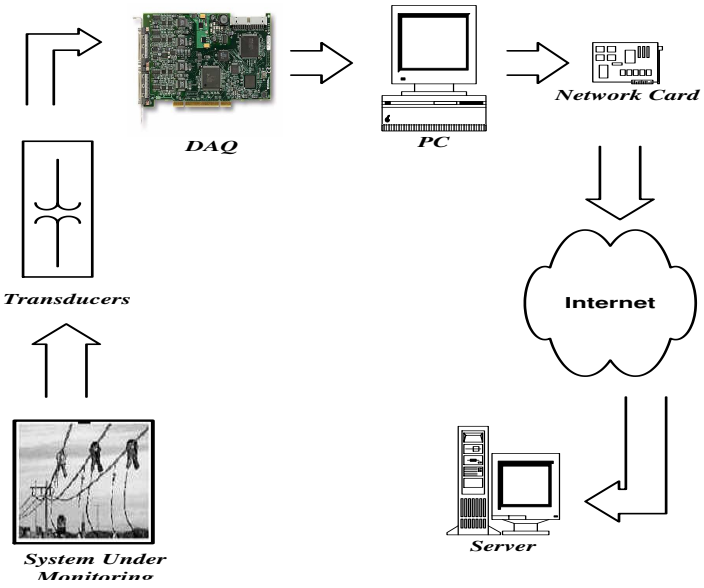

Figure 3.1: The PQIN configuration.

satellite, wired such as fiber-optic, or even rented public communication lines [51]. As a result of the advances in Internet communication, it has been more reliable, more secure and cheaper than the aforementioned methods. The use of Internet as a communication environment for both on-line and off-line measurement has been addressed in a number of publication with great success [38], [52]. By using the appropriate protocol, the real-time synchronization of the data can be accomplished [41], [53], [54]. Therefore, the of use the Internet to communicate among PQINs is convenient.

3.3 Covering and Packing Problem

For a given family of subset S of finite set X, the problem of covering is to find a subfamily with the minimum number of members of subsets S such that the union is X [55]. The problem of packing is to find a subfamily of disjoint subsets that includes the maximum number of members.

The density of covering or packing is the mean number of subsets that covers the

elements of the basic set. By definition, the density of any covering is not less than 1, and the density of any packing is not more than 1. The case where the density is equal to 1 is ideal. In this case, the covering is at the same time as the packing; such objects are usually called perfect.

The problems of covering and packing can be represented by reducing them to problems of Integer Linear Programming (ILP) [55], where X is the optimization variable, C be the cost of each variable and D be a binary matrix called density matrix. The inner product of two vectors $C = (c_1 \ ... \ c_n)^t$ and $X = (x_1 \ ... \ x_n)^t$, is equal to

$$\sum_{i=1}^{M} c_i \ x_i \ = \ C^t \ X \tag{3.2}$$

and constitutes the objective function. The covering problem is defined as minimizing (3.2) subject to $DX \geq 1$, whereas the packing problem is to minimize (3.2) subjected to $DX \leq 1$. The columns of the density matrix represent the subsets S and the rows represent the elements of X to be covered. For example, consider $X = \{x_1, x_2, x_3, x_4, x_5, x_6, x_7, x_8, x_9\}$ and subsets $S_1 = \{x_1, x_2, x_3, x_4\}$, $S_2 = \{x_4, x_6, x_8, x_9\}$, $S_3 = \{x_3, x_5, x_6, x_8\}$ and $S_4 = \{x_1, x_5, x_7, x_9\}$. The density matrix is given as

$$\mathbf{D} = \left(\begin{array}{c|cccc} \frac{X}{S} & S_1 & S_2 & S_3 & S_4 \\ \hline x_1 & 1 & 0 & 0 & 1 \\ x_2 & 1 & 0 & 0 & 0 \\ x_3 & 1 & 0 & 1 & 0 \\ x_4 & 1 & 1 & 0 & 0 \\ x_5 & 0 & 0 & 1 & 1 \\ x_6 & 0 & 1 & 1 & 0 \\ x_7 & 0 & 0 & 0 & 1 \\ x_8 & 0 & 1 & 1 & 0 \\ x_9 & 0 & 1 & 0 & 1 \end{array}\right) \tag{3.3}$$

The ILP problem is to find the minimum number of subsets S that cover all elements.

The problem of the allocation of the PQ monitors can be formulated as a covering and packing concept as follow:

Given: the available locations of PQINs are $X = (x_1...x_n)^t$, and the cost of these PQINs is given as: $C = (c_1...c_n)^t$.

Problem: Find the locations of PQINs to minimize the total cost?

Constraint: All the state variables, *i.e.* the voltages and the currents of the system, must be covered by at least one PQIN "$DX \geq 1$". By saying that PQIN covers a state variable, it means that the PQIN is capable of observing this state variable either by direct measurement or calculation.

Generally, density matrix D is a binary matrix that depends on the circuit parameters, and requires a prior knowledge of the load parameters. Knowing all the loads' parameters is not a realistic assumption. Therefore, the density matrix needs to be built independently on knowing the load parameters. In this work, the density matrix will be built depending on the power system circuit topology. Generally, the density matrix is the mathematical representation of the constraints.

3.4 Mathematical Formulation

Consider an electrical power system of n busses, l lines, and m state variables. Some variables that are used in the mathematical formulation are then defined.

Definition 1 "*Existence Vector*" :

The existence vector, X, is defined as a vector of n-binary elements which represents the existence of the PQIN and are expressed as

$$x(j) = \begin{cases} 1 & if\ PQIN\#j\ is\ installed \\ 0 & if\ PQIN\#j\ is\ not\ installed \end{cases} \tag{3.4}$$

Definition 2 "*Cost Vector*":
The cost vector, C, is defined as a vector of n-elements that expresses the cost of each PQIN, where

$$c(j) \; = \; the \; cost \; of \; PQIN\#j \tag{3.5}$$

The total cost of the monitoring system is the summation of the cost of the installed monitors and is given in (3.2). This objective function should be minimized subjected to the observability constraints which are deduced by applying Kirchof's Current Law (KCL) and Ohms's Law (OL) resulting in two groups of constraints.

3.5 Ohm's Law Constraints

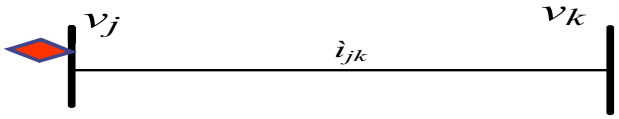

Figure 3.2: Part of the power system consists of a transmission line, represented by a series inductance and resistance, running between two buses.

Figure (3.2) shows two buses connected by a transmission line. By applying Ohm's law to the circuit, the relation between the current and the voltages can be written in the time domain (3.6).

$$v_j \; - \; v_k \; = \; Ri_{jk} \; + \; L\frac{di_{jk}}{dt} \tag{3.6}$$

There are three state variables: i_{jk}, v_j,and v_k, in this equation, knowing two variables leads to the calculation of the third variable. From this equation, the following lemmas are true.

Lemma 1: If the voltage at one bus of the line and the current through it are observable, then the voltage at the other bus is observable.

Lemma 2: If the voltages across the line are observable, then the current through this line is observable.

These two lemmas form two constraints: voltage constraints and current constraints, respectively.

3.5.1 Voltage Constraints

Definition 3 "*Connectivity Matrix*":

The connectivity matrix, A, is defined as a binary (mxn)-matrix with column $\#k$ representing the PQIN at bus $\#k$ and the row v_j representing the state variable v_j (the voltage at bus #j). The elements of this matrix are defined as

$$a(v_j, k) = \begin{cases} 1 & if\ v_j\ is\ observed\ by\ PQIN\#k \\ 0 & otherwise \end{cases} \tag{3.7}$$

Note that; $A(v_k)$ points to the row corresponding to the state variable v_k and $A(j)$ points to column corresponding to the PQIN#j at bus number j.

From the definition of A, the condition of observation of v_j is the installation of PQIN#k , $x(k) = 1$, and the ability of PQIN#k to observe v_j, $a(v_j, k) = 1$, in other words, $a(v_j, k)x(k) = 1$. Since the goal is to observe v_j by at least one PQIN, then the following condition should be valid

$a(v_j, 1)x(1) + a(v_j, 2)x(2) + ... a(v_j, n)x(n) \geq 1$

In other words,

$$\sum_{k=1}^{n} a(v_j, k)x(k) \geq 1 \tag{3.8}$$

Definition 4 "*Observability Vector*" :

The observability vector, U, is defined as an integer vector of n-elements, representing how many times the state variable is observed, and is

$$U = AX \tag{3.9}$$

Note that, $u(k) = T$ indicates that the state variable k is observable at T times, where $T = 1$ is the ideal case. However, some state variables can be observed by more than one PQIN, and data redundancy can occur.

The condition of observing all the state variables is that all the elements in vector U must be equal to at least one. Since the observability vector, U, depends on the locations of the PQINs, the vector X, and the circuit topology of the transmission line, matrix A, the system observability is built without knowing of the load parameters.

As mentioned before, the task of a PQIN is to measure voltages and currents at the installed bus. Since, both the voltage and the current are known, the voltage at a connected bus is observed according to *lemma* 1. Therefore, a PQIN at any bus will be able to observe the voltage at all the buses connected to it.

For a line running between bus $\#j$ and bus $\#k$, the state variables are v_j, v_k and i_{jk}. It is obvious that installing PQIN#j yields $a(v_j, j) = a(v_k, j) = a(i_{jk}, j) = 1$ whereas installing PQIN#k yields $a(v_j, k) = a(v_k, k) = a(i_{jk}, k) = 1$. Accordingly, the stamp of A-matrix for a transmission line is shown in Fig. 3.3.

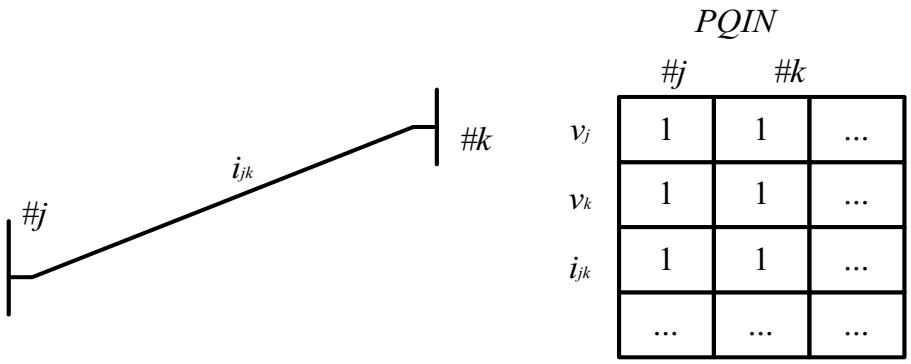

Figure 3.3: The stamp of matrix A for a transmission line

3.5.2 Current Constraints

Consider Fig. 3.4 where a part of a power system consists of four buses and two PQINs is illustrated.

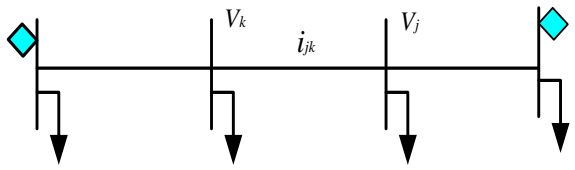

Figure 3.4: Four buses are connected by lines as a part of the power system

If the two PQINs are installed as shown, by a rhombus, then the voltages ($v_j,\ v_k$) will be observed by these two PQINs, according to *lemma* 1; and consequently the current through this line, i_{jk}, is observable, according to *lemma* 2, . Typically, the following is true

If v_j *and* v_k *are observable, then* i_{jk} *is observable*

Since the U-vector is the observability vector, then

If $u(v_j) \geq 1$ *and* $u(v_k) \geq 1$ *then* $u(i_{jk}) \geq 1$

To formulate this constraint mathematically, a definition of the co-connectivity matrix is needed.

Definition 5 "$Co-connectivity\ Matrix$" :

The co-connectivity matrix, B, is defined as a binary (mxn)-matrix that is expressed as:

$$B(i_{jk}) = \begin{cases} A(v_k) & if\ bus\ \#j\ and\ \#k\ are\ connected \\ 0 & otherwise \end{cases} \tag{3.10}$$

With the last constraint, the formulation is

If $B_j x \geq 1$ *and* $B_k x \geq 1$, *then* $u(i_{jk}) = 1$.

By replacing the *and*-operator by the multiplication-operator

If $(B_j.x)^t.(B_k.x) \geq 1$, *then* $u(i_{jk}) = 1$.

This equation defines the co-observability vector.

Definition 6 "*Co − observability Vector*" :

The co-observability vector W, is defined as an integer vector if n-elements expressed as:

$$w(i_{jk}) \;=\; (B_j.x)^t.(B_k.x) \quad \forall i_{jk} \tag{3.11}$$

For a line carrying current i_{jk} between bus #j and #k, B-matrices are built according to *lemma* 2 as follow:

1. Read the data file.
2. Build A-matrix.
3. Set $B_j(i_{jk}) = A(v_j)$ and $B_k(i_{jk}) = A(v_k)$

The flowchart in Fig. 3.5 summarizes the steps of building the A and B matrices.

3.6 Kirchof's Current Law (KCL) Constraints

For the previous constraints, it is assumed that the loads at all the buses are unknown. However, there is enough information about some loads may be available, so that the allocation problem can benefit from this information. The buses whose load parameters are known are called the known buses, whereas the bus that has no loads connected to it is called the connecting bus. These buses should be introduced in the allocation problem to reduce the number of PQINs. To introduce these two buses into the optimization problem, as constraints, Kirchof's Current Law (KCL) will be used.

KCL states that "the incoming and the outgoing currents at any bus are equal". By applying this law on these two types of buses, the result is that there are two extra constraints that reduce the number of the installed PQINs.

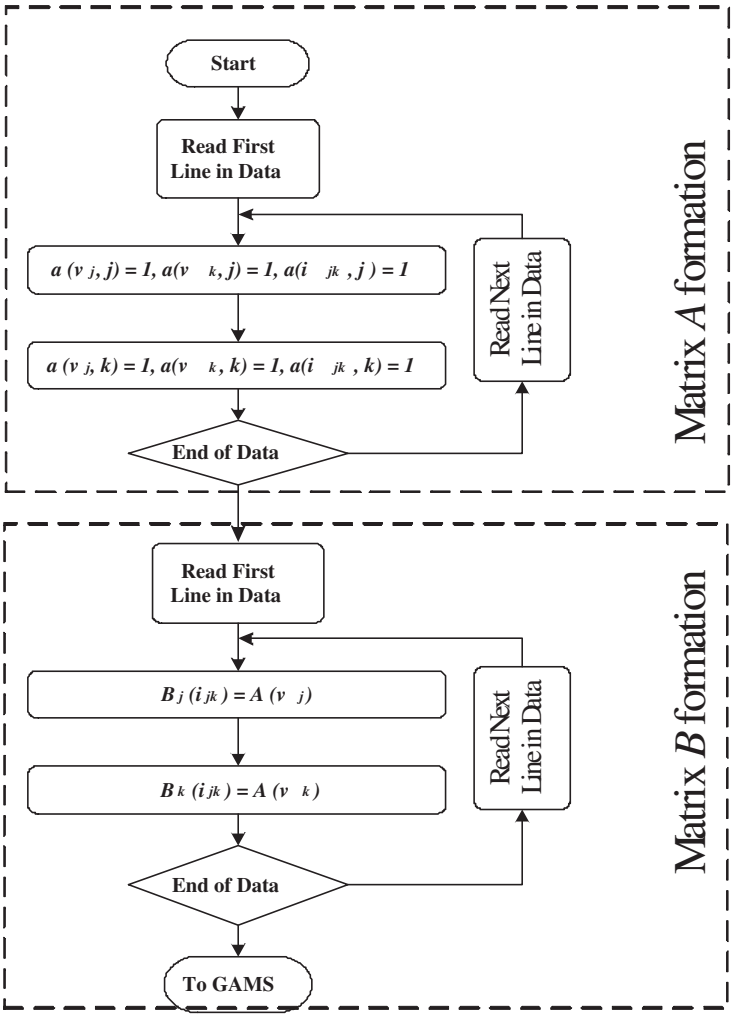

Figure 3.5: Flowchart of generating the A and B matrices

3.6.1 Known Busbar

Definition 6 "*Known Bus*" :

The known bus is defined as the bus whose relation between its load's current and voltage is known; *i.e.* $f(v, i) = 0$ is known.

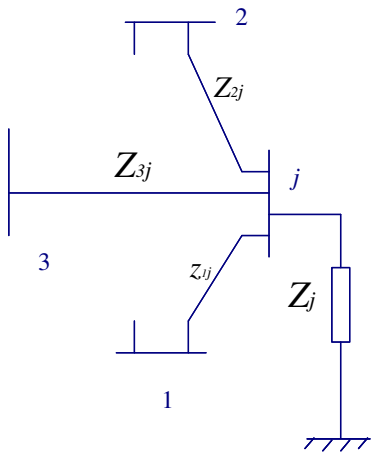

Figure 3.6: The known bus, the load is represented by the impedance to indicate that $f(v,i)=0$ is known.

Consider a part of the power system in Fig. 3.6, with KCL applied at bus #j such that:

$$i_{j1} + i_{j2} + i_{j3} = i_j \tag{3.12}$$

if the transmission line and the load impedance are known, then

$$\frac{v_1}{z_{1j}} + \frac{v_2}{z_{2j}} + \frac{v_3}{z_{3j}} = \frac{v_j}{z_{jj}} \tag{3.13}$$

where $\frac{1}{z_{jj}} = \frac{1}{z_j} + \frac{1}{z_{1j}} + \frac{1}{z_{2j}} + \frac{1}{z_{3j}} \ldots$

Therefore, if v_1, v_2, and v_3 are observable, and $f(v_j,i_j) = 0$ is known, then v_j is observable. In this example, it is assume that the load is represented by an impedance z_j, *i.e.*

$$f(v_j,i_j) = v_j - z_j.i_j = 0 \tag{3.14}$$

As a result, the following lemma is valid.

Lemma 3 :

If all the voltages of the buses, connected to a known bus, are observable, then the voltage at the known busbar is observable.

By applying this lemma in the circuit in Fig. 3.6, the expression is

$If\ u(1) \geq 1\ and\ u(2) \geq 1\ and\ ...\ u(J) \geq 1,$

then v_j *is observable*

By replacing the *and*-operator by the multiplication-operator, the observability condition of v_j is

$$u(1).u(2)\ ...\ u(J) \geq\ 1 \tag{3.15}$$

By replacing u in (3.8),

$$\prod_{J} \sum_{k=1}^{n} a(j,k).x_k\ \geq\ 1 \tag{3.16}$$

This condition leads to a definition of the KCL Co-observability Vector

Definition 7 "KCL Co − observability Vector" : The co-observability vector y, is defined as an integer vector of n-elements, expressed

$$y(v_j)\ =\ \prod_{J} \sum_{k=1}^{n} a(j,k).x_k \tag{3.17}$$

The Y-vector is written for only the known buses and it depends on knowing the load parameters in advance. It is noteworthy that the more that is known about the buses, the fewer the PQINs are required.

3.6.2 Connecting Busbar

Define the connecting bus as the bus that is connected to neither the load nor the generator. Figure 3.7 shows a part of the power system, where bus #j is called the connecting busbar. This constraint is considered as a special case of the known bus. The reason for considering it to be a different constraint is that it requires different treatment in the estimation

method. The mathematical formulation is the same as in (3.17).

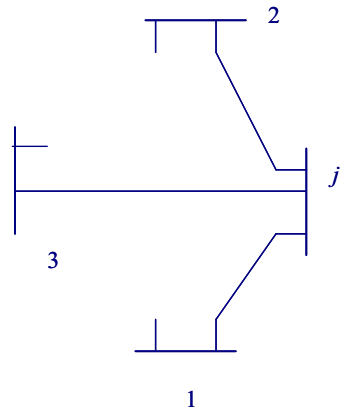

Figure 3.7: Connecting bus with no generation unit and no load.

3.7 Solution Algorithm

The optimization problem is stated as

$$\begin{cases} min \ \sum_{j=1}^{n} c_j.x_j \\ subjected\ to: \ U \ + \ W \ + \ Y \ \geq \ 1 \end{cases} \tag{3.18}$$

As seen in the previous sections, X is a binary vector so that there is a non-linear optimization problem caused by vectors W and Y. To overcome the non-linearity caused by W, the constraints are restated as:

$$\begin{cases} U \ + \ W_j \ + \ Y \ \geq \ 1 \\ U \ + \ W_k \ + \ Y \ \geq \ 1 \\ where: \ W_j = B_j.X \ and \ W_k = B_k.X \end{cases} \tag{3.19}$$

The same concept can be applied to linearize the vector y. Solving the problem of

covering and packing by the ILP is beyond the scope of this chapter, and more details can be found in [55]. In this chapter, it is adequate to formulate the problem and solve the ILP problem by utilizing the Branch and Bound method [56]. During the formulation of the equation, the mathematical equations are formulated in a general form that can be manipulated by any general purpose optimization software. For a large electrical system, TOMLAB is used as the optimization software since TOMLAB has proven its efficiency with dealing in large scale optimization problems [57], [56].

The last point to be considered here is related to the cost of the PQIN. In some systems, there will be PQIN installed already to monitor either the bus or the transformer, therefore the cost due to such PQIN is zero. However, the cost of such PQIN should be set to very small value in the optimization cost function (3.18), otherwise the optimization will consider the cost of this PQIN as a dummy variable.

3.8 Data Redundancy

It is always anticipated in monitoring problems that there is data redundancy, which means that some of the network voltages or currents can be measured or calculated from two or more different monitors. Yet, it is desirable to limit this redundancy. In this context, the data redundancy is defined as: how many times the state variables are measured or calculated, and the Data Redundancy Factor (DRF) is defined as

$$DRF = \frac{sum\ of\ numbers\ of\ observing\ state\ variables}{number\ of state\ variables} \tag{3.20}$$

When there is no redundancy in the data, the DRF is one, and the higher the DRF, the higher the redundancy is.

Equation (3.18) shows that, $u(j) + w(j) + y(j) = T$ indicating that the state variable

j is observed T times. So, DRF could be written in terms of u, w *and* y as:

$$DRF = \frac{\sum_{j=1}^{N} u(j) + w(j) + y(j)}{N} \tag{3.21}$$

where: N is the number of state variable.

The main concern with the optimization problem is to optimize the number of PQINs, and consequently, the cost of the monitoring system. Moreover, different PQIN allocation configurations have the same value as a cost function. However, the DRF differs from one configuration to another. Therefore, the criteria of selecting among those configurations will rely on the data redundancy. The benefits of less data redundancy are the reduction of the bandwidth of sending and receiving the data between the different PQINs as well as reducing the media to store these data. However, reducing the redundancy in the data reduces the system reliability.

3.9 Applications

The proposed method is applied to different systems, where TOMLAB is used as the optimization package. The first study case is a simple 6-bus system to illustrate the proposed method. The second study case reveals the effect of the known and connecting buses. The effect of data redundancy and the criteria of choosing between the different configurations is illustrated by the third study case. Here, a more realistic system is studied in which the emphasis is on the effect of the number of transmission lines on the PQIN allocation. It should be pointed out that, whenever series device is installed in the system between buses $\#j$ and $\#k$, it is considered as a load connected at both bus $\#j$ and bus $\#k$. However, if the dynamic model of the series device is known, it can be dealt with in the same way as the transmission line case.

3.9.1 Study Case (1)

A 6-bus system with eight transmission lines is shown in Fig. 3.8. The state variables are the bus voltages and the transmission lines currents as indicated in the figure. In this case, it is assumed that no information is available about either the loads or the generation units, *i.e.* there is neither known busbars nor connecting busbars. The A and B matrices are built and the system is solved by TOMLAB.

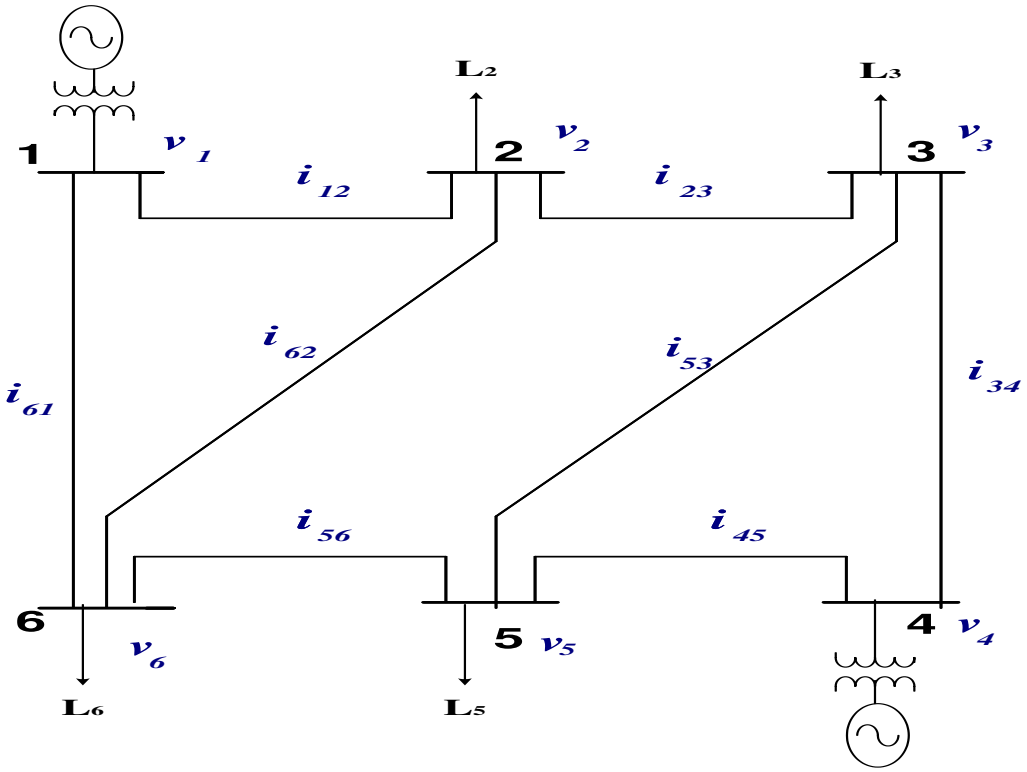

Figure 3.8: The 6-bus system

Appendix E details the formulation of A-matrix and B-matrix. Although the cost of the PQIN at each bus depends on the number and the types of the sensors as well as the bus location, equal cost for all PQINs is assumed in this study case for simplicity. The optimum number of monitors is found to be 2 PQIN. The different locations of the PQIN and the associated DRF are listed in Table 3.1.

Table 3.1: Optimum locations and DRF of the 6-bus system

PQIN Location	DRF
#1 *and* #3	1.57
#1 *and* #4	1.28
#1 *and* #5	1.5
#2 *and* #4	1.57
#2 *and* #5	1.78
#3 *and* #6	1.78
#4 *and* #6	1.5

In this allocation, #1 and #4, it is obvious that PQIN#1 will measure v_1, i_{12}, and i_{61} and the voltages v_2 and v_6 will be calculated by knowing the line resistance and inductance. Also, PQIN#4 will measure v_4, i_{34}, i_{45} and v_3 and v_5 will be calculated. The current in lines between busbars 2 and 6, i_{62}, will be calculated, as v_2 and v_6 are observable and the line parameters are known. The same concept will be applied for currents i_{23}, i_{53}, i_{56}. Having all transmission line currents observable, the load current at all busbars will be observable.

To verify the ability of the two nodes to observe the system accurately, the system is simulated using EMTDC/PSCAD. The system is supplied by two source connect at buses #1 and #4. To simulate different PQ problems, non-linear loads are connected at buses #3 and #6. The nonlinear loads are simulated by harmonic current sources with third, fifth and seventh harmonic. Moreover, a sudden large load is connected at bus #5 after 0.5 second to simulate a voltage sag. The linear loads are connected at buses #2 and #5. The voltages at buses #3 and #6 are given as:

$$\begin{cases} v_3 = (L_{34}\frac{d}{dt} + R_{34})i_{34} + v_4 \\ v_6 = (L_{61}\frac{d}{dt} + R_{61})i_{61} + v_1 \end{cases} \tag{3.22}$$

By substituting $\frac{d}{dt}$ by Euler backward approximation,

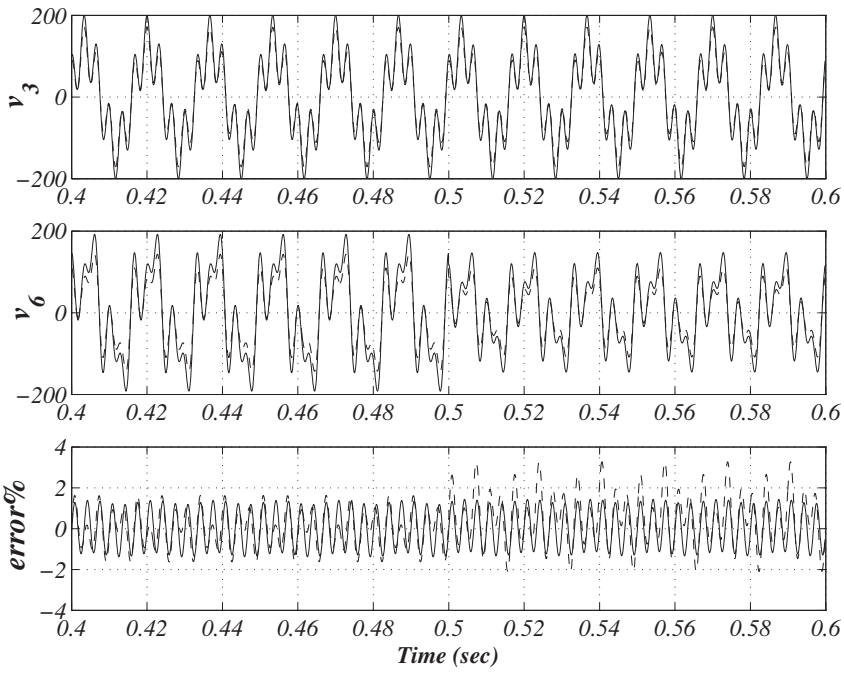

Figure 3.9: Voltage at bus #3 and #6 and error

$$\begin{cases} v_3(t) = L_{34}\frac{i_{34}(t) - i_{34}(t-1)}{T_s} + R_{34}i_{34}(t) + v_4(t) \\ v_6(t) = L_{61}\frac{i_{61}(t) - i_{61}(t-1)}{T_s} + R_{61}i_{61}(t) + v_1(t) \\ where: \ T_s \ is \ sampling \ time \end{cases} \tag{3.23}$$

The voltages at buses #3 and #6, v_3 and v_6, are calculated according to (3.23) and compared with the actual values from the simulation. Figure 3.9 displays the actual waveforms of v_3 and v_6 which are distorted due to the existence of nonlinear loads with a voltage sag in v_6. The error is found to be less than 2% as shown in the Fig. 3.9.

3.9.2 Study Case (2)

To show the effect of the KCL constraints, the second study case will be utilizing the same 6-bus system, but with assuming that buses #5 and #4 are known busbars. A and B matrices will not differ from the previous case and two extra constraints will be added,

namely KCL constraint, at busbars #4 and #5. The optimum number of PQIN is found to be 1 at busbar #2. This study case shows that known busbars will reduce the number of required PQINs.

It is clear that PQIN#2 will measure $v_2,\ i_{12},\ i_{23},\ i_{26}$ and the voltages $v_1,\ v_3,\ v_6$ will be calculated by knowing the line impedance. To calculate the voltages at bus #4 and #5, consider KCL at busbar #4, such that

$$\frac{v_3}{z_{34}} + \frac{v_5}{z_{45}} = \frac{v_4}{z_{44}} + f_g(v_4) \tag{3.24}$$

where: f_g is a dynamic function that models the dynamics of the generator and $z_{ij} = R_{ij} + L_{ij}\frac{d}{dt}$.

KCL at busbar #5 yields

$$\frac{v_3}{z_{35}} + \frac{v_4}{z_{45}} + \frac{v_6}{z_{56}} = \frac{v_5}{z_{55}} \tag{3.25}$$

Since v_3 and v_6 are observable, then (3.24) and (3.25), can be solved to obtain the two unknowns voltages, v_4 and v_5.

3.9.3 Study Case (3)

For a more realistic study, the proposed algorithm is applied to the IEEE 30-bus. It is assumed that there is no information about either the generation units or the loads. It is assumed here that all the PQINs have equal costs. The results are shown in Fig. 3.10, where the PQINs are indicated by the rhombus. In this system, it is noticed that the redundancy factor DRF is a bit higher than the one in the previous study due to the fact of heavy connectivity of the system. However, removing any of these PQINs will result in loosing the observability of another state variable.

As mentioned earlier, in some cases a higher DRF is needed to obtain a higher reli-

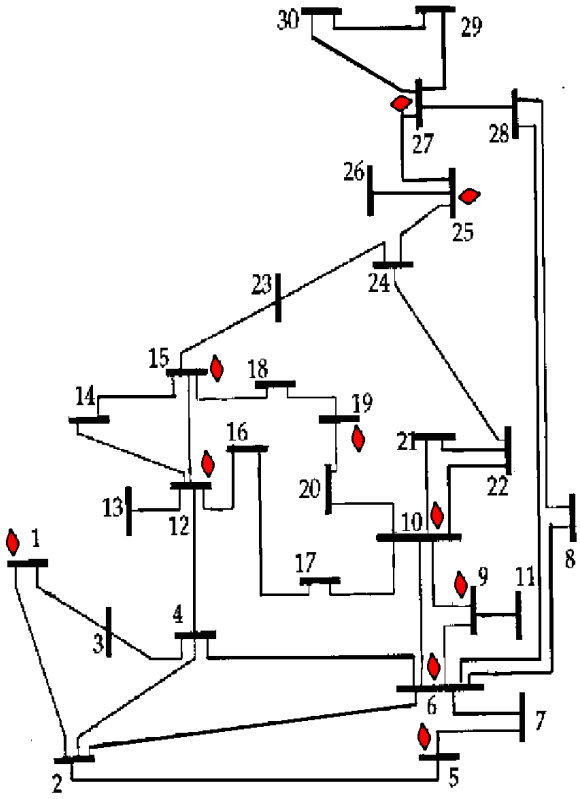

Figure 3.10: The IEEE 30-bus system with the location of the PQIN indicated by the rhombus in case of equal PQIN cost

ability. Consequently, it is required to list all the locations of the PQIN that have the same cost function value, then choose the highest or the lowest DRF depending on the required monitoring reliability. Table 3.2 indicates different locations of the PQINs with the associated DRF. Although the optimum PQINs number of all the configurations is ten PQINs, the DRF is found to vary between 1.643 and 2.155.

Since the cost of the PQIN is not equal at all the buses, it is beneficial to study the case of unequal PQINs cost. For that sake, the PQIN cost in the system under study will vary and the optimization process will be conducted to determine the optimum configuration that gives the minimum overall cost.

Equation (3.1) shows that the cost of the PQIN is a function of the different factors

Table 3.2: Optimum locations and DRF of the IEEE 30-bus system

	Configuration Number							
bus	#1	#2	#3	#4	#5	#6	#7	#8
#1	1	0	1	0	1	0	1	0
#2	1	1	0	0	1	0	1	1
#3	0	0	0	1	0	1	0	0
#4	0	1	0	0	0	0	0	1
#5	0	0	1	1	0	1	0	0
#6	1	1	0	0	1	0	1	1
#7	0	0	0	0	0	0	0	0
#8	0	0	0	0	0	0	0	0
#9	1	1	1	1	1	1	0	1
#10	1	1	1	1	1	1	1	1
#11	0	0	0	0	0	0	1	0
#12	1	1	1	1	1	1	1	1
#13	0	0	0	0	0	0	0	0
#14	0	0	0	0	0	0	0	0
#15	0	0	0	0	1	1	0	0
#16	0	0	0	0	0	0	0	0
#17	0	0	0	0	0	0	0	0
#18	1	1	1	1	0	0	1	1
#19	0	0	0	0	0	0	0	0
#20	0	0	0	1	1	1	0	0
#21	0	0	0	0	0	0	0	0
#22	0	0	0	0	0	0	0	0
#23	0	0	0	0	0	0	0	0
#24	1	1	1	1	0	0	1	1
#25	1	1	1	1	1	1	1	1
#26	0	0	0	0	0	0	0	0
#27	1	1	1	0	0	0	1	0
#28	0	0	1	1	0	1	0	0
#29	0	0	0	0	1	1	0	1
#30	0	0	0	0	0	0	0	0
DRF	1.97	2.12	1.64	1.64	2.01	1.67	1.81	2.15

where the number of transducers plays the major role in the cost. More transducers means: 1) wider communication bandwidth is needed which increases the communication cost (C_{com}), 2) more DAQ analogue channels are required which rises the cost of the DAQ (C_{DAQ}), and 3) escalating the transducers cost it self (C_{tran}). Therefore, PQIN cost is

chosen to proportionate with the number of transducers, in other words the PQIN cost is proportional to the number of connected lines to that bus.

Based on the aforementioned discussion, the PQIN cost of the IEEE 30-bus system has been chosen based on the number of transducers. For example, bus #2 requires three potential transformers to measure the three-phase voltages and fifteen current transformers to measure the currents of the four lines and the load connected at the bus. As a result, the $c(2)$ is set be 18 in (6.4).

The optimum number is found to be twelve-PQIN at buses number 3, 5, 8, 11, 13, 14, 17, 19, 21, 23, 26, and 29. Although, the number of the PQIN has been increased from ten to twelve compared to the case of equal cost, the actual cost of the chosen twelve is less than the ten.

3.9.4 Study Case (4)

In this case, larger systems are tested to study the effect of the circuit topology. The first system is the IEEE-118 bus system with 186 connecting lines. Because the system is heavily connected, the optimum number of the PQIN is found to be 32 out of 118 available locations, so saving of 72.88% is achieved.

The second case is the IEEE 300-buses system which has 411 connection lines. The optimum number of the PQIN is found to be 41. Table 3.3 summarizes these results.

Table 3.3: IEEE 118 and 300-bus systems

System	No. of Lines	No. of PQIN	%Saving	DRF
IEEE-118	186	32	72.88%	1.45
IEEE-300	411	41	86.33%	1.52

3.10 Summary

This chapter introduces a novel algorithm to determine the optimum number and location of PQ monitors and also keep the system state variables, currents and bus voltages, observable. The problem is formulated in covering and packing concept, and is transferred to the problem of integer linear programming which can be manipulated by any general purpose optimization program, such as TOMLAB. Introducing this technique solves the high cost problem associated with monitoring the entire electrical power system.

The proposed algorithm is applied to a simple 6-bus system and reduces the number of PQIN by 66%. Moreover, utilizing the concept of the known buses results in a further reduction of installed monitors and increased the savings to 83%. However, applying the newly devised algorithm to the IEEE-30 bus system results in a saving of 66.6%, and a number of solutions have the same minimum cost. Therefore, a data redundancy factor is used in choosing the solutions. With heavily connected systems such as IEEE-118 and IEEE-300 systems, the saving is increased to 72.8% and 86.3%, respectively.

Chapter 4

DSTATCOM Effect on The ASD Stability

Although, a DSTATCOM is installed in electrical power distribution systems to mitigate the PQ problems, the device affects the stability of the ASD. This and what can be done about it, is debated in this chapter.

4.1 Introduction

A DSTATCOM utilizes either voltage or current source inverters along with reactive power storage elements, either a capacitor or an inductor respectively [58]. However, voltage source inverters are popular due to their smaller size, lower heat dissipation and the less expensive than the capacitor compared to the inductor for the same power rating [59]. Different control techniques for the DSTATCOM based on Voltage Source Inverters (VSI) are found in the literature [60], [61]. Typically, DSTATCOM control techniques can be categorized into Voltage Control-DSTATCOM (VC-DS) or Current Control-DSTATCOM (CC-DS) [62]. Therefore, both control techniques of the voltage source inverter based, DSTATCOM, VC-DS and CC-DS, are considered in this study.

ASDs rely on power electronics inverters to control the speed of the electric machines.

Those inverters can be either VSI or Current Source Inverter (CSI). Since both inverter schemes are utilized in the ASD, both are investigated. Moreover, this study focuses on scalar-based speed controllers, known as a constant V/f control [63]. The system, including the ASD and DSTATCOM, is modeled in a rotating frame of reference known as *dqo*, and the eigenvalues of the system are calculated to determine the stability limits of the system.

4.2 System Under Study

The system under study, depicted in Fig. 4.1, consists of an ASD and a DSTATCOM. The system is fed from substation at node number 1. The ASD, connected at the third node, is comprised of an AC/DC/AC converter which feeds an induction motor. The induction motor works at different speeds and mechanical loads, drawing different amounts of active and reactive currents. Consequently, the voltage at the second node fluctuates. The DSTATCOM is installed at the second node to mitigate the voltage fluctuation at this node and, thus, protect the sensitive loads at the second node. The impedances z_{12}, z_{23}, and z_{31} are used to present the mutual impedance of the nodes.

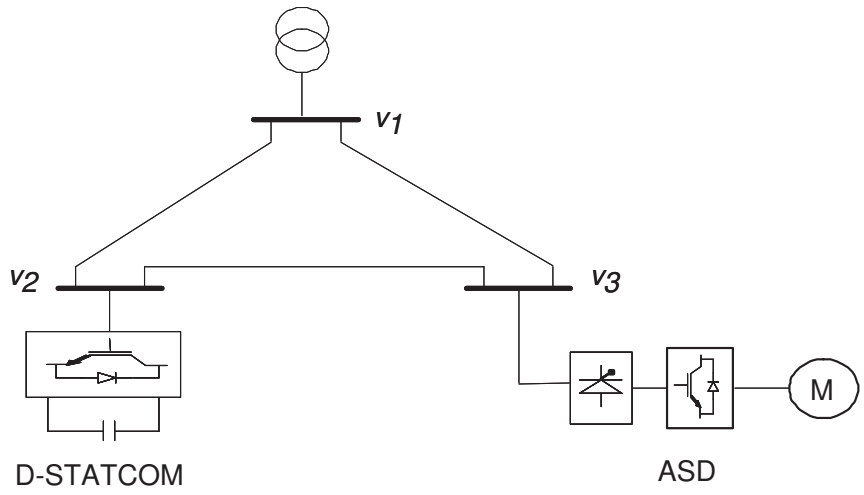

Figure 4.1: System studied

For the stability evaluation, the eigen domain offers a fast method to predict the stabil-

ity of linear and time-invariant systems. Since the system under study is nonlinear, it has to be linearized around the operating point, before the eigen domain analysis is conducted. Moreover, the system is modeled in a time-invariant stationary reference frame, the *dqo* notation, rather the time-variant rotating frame, *abc* notation. The system equations are linearized and written in the form given in (4.1), so the eigenvalues can be computed.

$$\begin{aligned} \dot{x} &= A\ x\ +\ B\ u \\ y &= C\ x\ +\ D\ u \end{aligned} \tag{4.1}$$

In the following sections, models of the DSTATCOM and the ASD are presented. Two circuit model topologies for the ASD and two control techniques of the DSTATCOM are explored.

4.3 DSTATCOM Model

The heart of the DSTATCOM is the power electronic inverter which allows the exchange of power between both sides, *ac* and *dc*. Figure 4.2 reflects the components of the DSTATCOM which is based on the VSI circuit topology. The primary task of the DSTATCOM in the distribution system is to supply reactive power to the system in order to regulate the voltage at the PCC. When the source of active power is available on the *dc* side of the DSTATCOM such as a storage battery or a fly-wheel, the DSTATCOM can be used to supply active power.

Since the VSI is the most common circuit topology for the DSTATCOM, as discussed in the introduction, it is good candidate for this study. VSI-DSTATCOM can be used as a VC-DS or as a CC-DS. Based on the control technique, two models are realized and are discussed in the following subsections.

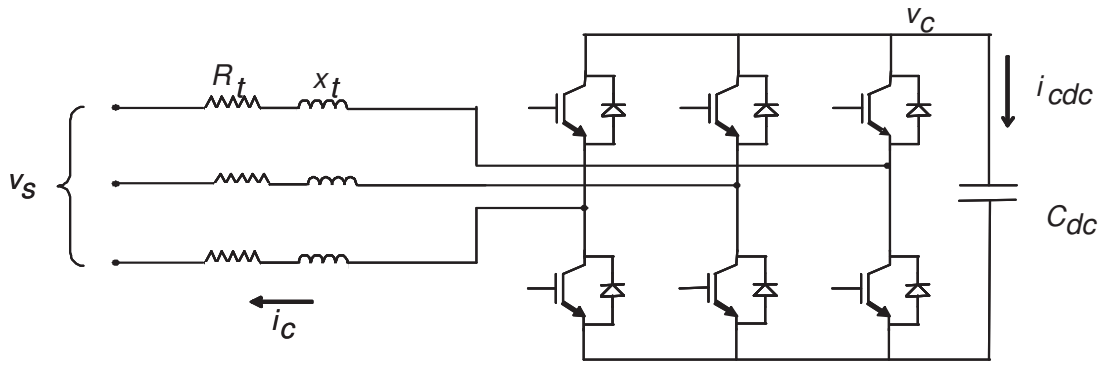

Figure 4.2: DSTATCOM

4.3.1 Voltage Control DSTATCOM

The key idea behind the VC-DS is to control the flow of active and reactive power in the inverter by using the DSTATCOM as a voltage source. This is realized by controlling both the modulation index, m, and the modulation angle, ϕ, which are the inputs to the Sinusoidal Pulse-Width Modulation, SPWM. In such a way, the DSTATCOM is modeled as a control voltage source. By using the Generalized Averaging Model (GAM) introduced in [64], the dynamic equations of such a system in the *dqo* reference frame are

$$\frac{d}{dt}\begin{pmatrix} i_{dc} \\ i_{qc} \\ v_c \end{pmatrix} = A_{VC}\begin{pmatrix} i_{dc} \\ i_{qc} \\ v_c \end{pmatrix} - \begin{pmatrix} \frac{v_{sd}}{x_t} \\ \frac{v_{sq}}{x_t} \\ 0 \end{pmatrix} \tag{4.2}$$

and

$$A_{VC} = \begin{pmatrix} -\frac{R_t}{x_t} & 1 & -mcos(\phi) \\ -1 & -\frac{R_t}{x_t} & -msin(\phi) \\ \frac{3m}{2C_{dc}}cos(\phi) & \frac{3m}{2C_{dc}}sin(\phi) & \frac{G_{dc}}{C_{dc}} \end{pmatrix} \tag{4.3}$$

where ϕ and m are the modulating angle and index of the SPWM, respectively. Equation (4.2) shows that three state variables are needed to model the voltage control based DSTATCOM, which are $[i_{dc},\ i_{qc},\ v_c]^t$.

4.3.2 Current Control DSTATCOM

Another common method to control the power flow of the DSTATCOM is to control its active and reactive current. Such a configuration is known as the current control DSTATCOM which is modeled as a dependent current source [65]. Controlling the *abc* current of the DSTATCOM is accomplished by Hystersis Current Control (HCC), a common technique [66]. The input signals are the reference direct current signal, $i_{ref,d}$, and quadrature current signal, $i_{ref,q}$.

By applying the GAM [64], the dynamic equation of this system is

$$\frac{d}{dt}\begin{pmatrix} v_{cd} \\ v_{cq} \\ i_{dc} \\ i_{qc} \end{pmatrix} = A_{CC}\begin{pmatrix} v_{cd} \\ v_{cq} \\ i_{dc} \\ i_{qc} \end{pmatrix} + \begin{pmatrix} \frac{1}{C_{dc}}\ i_{ref,d} \\ \frac{1}{C_{dc}}\ i_{ref,q} \\ \frac{1}{x_t}\ v_{sd} \\ \frac{1}{x_t}\ v_{sq} \end{pmatrix} \tag{4.4}$$

and

$$A_{CC} = \begin{pmatrix} -\frac{Gdc}{C_{dc}} & 1 & \frac{1}{C_{dc}} & 0 \\ -1 & -\frac{G_{dc}}{C_{dc}} & 0 & \frac{1}{C_{dc}} \\ -\frac{1}{x_t} & 0 & -\frac{R_t}{x_t} & 1 \\ 0 & -\frac{1}{x_t} & -1 & -\frac{R_t}{x_t} \end{pmatrix} \tag{4.5}$$

4.4 Adjustable Speed Drive (ASD)

A simplified diagram of an ASD is shown in Fig. 4.3. The ASD consists of a six pulses rectifier with a filter, an inverter, and a three-phase induction motor. The *ac* voltage, v_s,

is rectified to yield a *dc* voltage with a value, depending on the firing angle α computed as

$$v_r = \frac{3\sqrt{2}}{\pi} V_s cos(\alpha) \tag{4.6}$$

where V_s is the rms of the supply voltage v_s and is given by

$$V_s = \sqrt{v_{sd}^2 + v_{sq}^2} \tag{4.7}$$

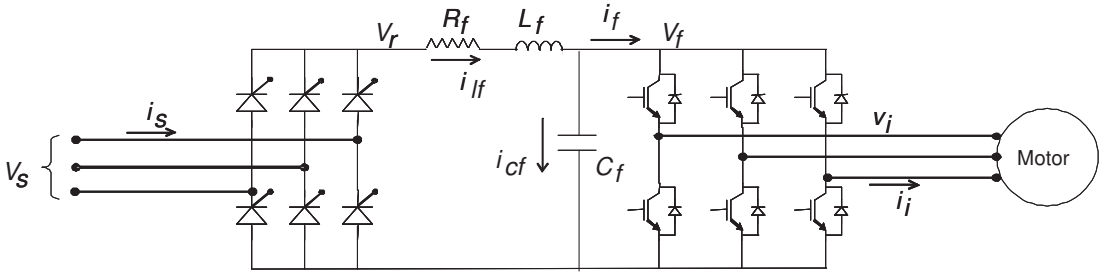

Figure 4.3: ASD system

The rectified voltage, v_r, is then filtered to yield v_f, according to

$$L_f \frac{d}{dt}(i_{lf}) = -R_f i_{lf} + (v_r - v_f) \tag{4.8}$$

and

$$C_f \frac{d}{dt}(v_f) = i_{lf} - i_f \tag{4.9}$$

Equations (4.8) and (4.9) describe the dynamics of the low-pass filter in the time domain, where C_f and L_f are the capacitance and the inductance of the used filter, respectively.

The filtered voltage, v_f, is then converted to a three-phase *ac* voltage with the desired frequency and voltage level by using a voltage inverter. The inverted voltage, v_i, is fed to the induction machine.

The induction motor is modeled by using a technique reported in [67]. The equations

which describe the induction motor in an arbitrary frame are expressed

$$x_{im}\frac{d}{dt}\begin{pmatrix} i_{qi} \\ i_{di} \\ i'_{qr} \\ i'_{dr} \end{pmatrix} = -A_{im}\begin{pmatrix} i_{qi} \\ i_{di} \\ i'_{qr} \\ i'_{dr} \end{pmatrix} + \begin{pmatrix} v_{iq} \\ v_{id} \\ v'_{rq} \\ v'_{rd} \end{pmatrix} \tag{4.10}$$

Matrices x_{im} and A_{im} are given in Appendix B.

Based on the aforementioned discussion, the ASD state variables are $x = [i_{qs},\ i_{ds},\ i_{qr},\ i_{dr},\ v_f,\ i_{lf}]^t$. Since the rotor circuit of the induction machine is usually short-circuited, the values of the rotor voltage are zeros, *i.e.* $v_{qr} = v_{dr} = 0$ [68]. Equations (4.8) to (4.10) model the ASD in the *dqo* frame of reference. In the following sections, these equations are updated to represent the VSI and CSI.

4.4.1 Voltage Source Inverter Based ASD

The VSI based ASD (VSI-ASD) converts the filtered voltage into a 3-phase voltage given by

$$\begin{aligned} v_{ia} &= \tfrac{2\sqrt{3}}{\pi}v_f[cos(\omega_e t) - \tfrac{1}{5}cos(5\omega_e t) + \tfrac{1}{7}cos(7\omega_e t) + ...] \\ v_{ib} &= \tfrac{2\sqrt{3}}{\pi}v_f[cos(\omega_e t - 120) - \tfrac{1}{5}cos(5\omega_e t + 120) + \tfrac{1}{7}cos(7\omega_e t - 120) + ...] \\ v_{ic} &= \tfrac{2\sqrt{3}}{\pi}v_f[cos(\omega_e t + 120) - \tfrac{1}{5}cos(5\omega_e t - 120) + \tfrac{1}{7}cos(7\omega_e t + 120) + ...] \end{aligned} \tag{4.11}$$

where ω_e is the electrical fundamental frequency.

Converting these equations into the rotating frame of reference gives

$$\begin{aligned} v_{iq} &= \tfrac{2}{\pi}v_f[1 - \tfrac{2}{35}cos(6\omega_e t) - \tfrac{24}{143}cos(12\omega_e t) + ...] \\ v_{id} &= \tfrac{2}{\pi}v_f[0 - \tfrac{12}{35}cos(6\omega_e t) - \tfrac{2}{143}cos(12\omega_e t) + ...] \end{aligned} \tag{4.12}$$

Although the fundamental component of the applied stator voltages, and the harmonics

combine to produce a steady-state operating point, the contribution of the voltage harmonics on the electromechanical behavior of the IM is small in most operating conditions. Therefore, the change in the average steady-state operating point and the perturbation about this operating point due to the harmonics are neglected [2].

By neglecting the harmonics, and taking the q-axis as the reference of the *dqo* of the induction machine, the voltage equations can be written as

$$\begin{aligned} v_{iq} &= \tfrac{2}{\pi} v_f \\ v_{id} &= 0 \end{aligned} \tag{4.13}$$

By assuming that the inverter is lossless, at a steady-state, the input and the output power of the inverter will be constants. In other words, the following relation is valid

$$v_f i_f = \frac{3}{2}(v_{iq} i_{iq} + v_{id} i_{id}) \tag{4.14}$$

Equation (4.14) provides the general formula for the power exchange between the *dc* side and the *ac* side of any inverter, which can be applied for the VSI by substituting v_{id} by zero. This substitution leads to

$$i_f = \frac{3}{\pi} i_{iq} \tag{4.15}$$

By using (4.13)-(4.15) and substituting then into (4.8) to (4.10), the complete model of the VSI-ASD is realized.

4.4.2 Current Source Inverter Based ASD

The CSI can be realized if the capacitance of low pass filter, C_f, in Fig. 4.3, is removed. Thus, the task of the inverter is to convert the filtered current to a 3-phase current, calculated by

$$\begin{aligned} i_{ia} &= \tfrac{2\sqrt{3}}{\pi} i_f [cos(\omega_e t) - \tfrac{1}{5} cos(5\omega_e t) + \tfrac{1}{7} cos(7\omega_e t) + ...] \\ i_{ib} &= \tfrac{2\sqrt{3}}{\pi} i_f [cos(\omega_e t - 120) - \tfrac{1}{5} cos(5\omega_e t + 120) + \tfrac{1}{7} cos(7\omega_e t - 120) + ...] \\ i_{ic} &= \tfrac{2\sqrt{3}}{\pi} i_f [cos(\omega_e t + 120) - \tfrac{1}{5} cos(5\omega_e t - 120) + \tfrac{1}{7} cos(7\omega_e t + 120) + ...] \end{aligned} \tag{4.16}$$

By converting these equations into the rotating frame of reference,

$$\begin{aligned} i_{iq} &= \tfrac{2}{\pi} i_f [1 - \tfrac{2}{35} cos(6\omega_e t) - \tfrac{24}{143} cos(12\omega_e t) + ...] \\ i_{id} &= \tfrac{2}{\pi} i_f [0 - \tfrac{12}{35} cos(6\omega_e t) - \tfrac{2}{143} cos(12\omega_e t) + ...] \end{aligned} \tag{4.17}$$

By neglecting the harmonics, and using the reference of the *dqo* of the induction machine locked to the q-axis, the current equations are

$$\begin{aligned} i_{iq} &= \tfrac{2}{\pi} i_f \\ i_{id} &= 0 \end{aligned} \tag{4.18}$$

Since the filter capacitance is removed, (4.9) is no longer included in the system dynamics. Therefore, the current supplied to the inverter is the current in the inductor, *i.e.*, $i_f = i_{lf}$.

By assuming that the inverter is lossless, at the steady-state, the input and the output power of the inverter is constant, therefore, (4.14) is valid. Typically, the d-axis current is zero during both the steady state and transient conditions due to locking in the synchronously frame reference with i_{ia} [69]. Equation (4.14) is updated for the CSI by substituting i_{id} by zero. This substitution leads to

$$v_f = \frac{3}{\pi} v_{iq} \tag{4.19}$$

Another consequence of equating i_{id} by zero is the elimination of the d-axis dynamic equation from (4.10) which will result in (4.20).

$$x_{im,csi}\ \frac{d}{dt}\begin{pmatrix} i_{qi} \\ i'_{qr} \\ i'_{dr} \end{pmatrix} = -A_{im,csi}\begin{pmatrix} i_{qi} \\ i'_{qr} \\ i'_{dr} \end{pmatrix} + \begin{pmatrix} v_{iq} \\ v'_{rq} \\ v'_{rd} \end{pmatrix} \tag{4.20}$$

where

$$x_{im,csi} = \begin{pmatrix} x_s & 0 & 0 \\ 0 & x'_r & 0 \\ 0 & 0 & x'_r \end{pmatrix} \tag{4.21}$$

$$A_{im,csi} = \begin{pmatrix} r_s & 0 & \frac{\omega}{\omega_b}x_m \\ 0 & r'_r & \frac{\omega-\omega_r}{\omega_b}x'_r \\ -\frac{\omega-\omega_r}{\omega_b}x_s & -\frac{\omega-\omega_r}{\omega_b}x'_r & r'_r \end{pmatrix} \tag{4.22}$$

4.4.3 Mechanical Equation

The electromagnetic torque, produced by the IM, is given by

$$T_e = x_m\left(i_{qs}i'_{dr} - i_{ds}i'_{qr}\right) \tag{4.23}$$

The acceleration equation which governs the mechanical dynamics is mathematically expressed as

$$\frac{2H}{\omega_b}\omega = T_e - T_m \tag{4.24}$$

where H is the inertia of both the mechanical load and the motor and T_m is the mechanical load torque.

4.5 The Interaction Case Studies

Since this investigation focuses on the dynamic effect of the DSTATCOM on the ASD stability boundaries, it is crucial to establish these boundaries before connecting the DSTATCOM to the system. Therefore, the stability boundaries of both the VSI and the CSI based ASD are set out first. Then, the DSTATCOM is connected to the system and two control techniques are tested.

Since the ASD can be either a VSI or a CSI and the DSTATCOM could be controlled as either VC or CC, four cases are examined in the following subsections. These cases are:

1. VSI-ASD with VC-DS
2. VSI-ASD with CC-DS
3. CSI-ASD with VC-DS
4. CSI-ASD with CC-DS

Since the motor inertia varies, the effect of the motor inertia variation is studied. The DC-capacitor of the DSTATCOM can vary as well, and so its variation effect is taken care of as well.

4.5.1 Stability Boundaries of the ASD Only

It is important to know the stability limits of the ASD at different speeds and loads before installing the DSTATCOM . For this sake, a graph of the mechanical load versus the mechanical speed of the ASD is plotted to show the stability limits [70].

To obtain such a plot, the mechanical speed, ω_m, is set to a certain value and the mechanical torque, T_m, is increased staring from the small values. The eigenvalues are calculated at each operating point. When the system is sustained oscillating, at least one eigenvalue has zero real part, this operating point is recorded and plotted. This procedure

is summarized in Fig. 4.4 and repeated for all the cases. Figure 4.5 shows the plot for the system without the DSTATCOM.

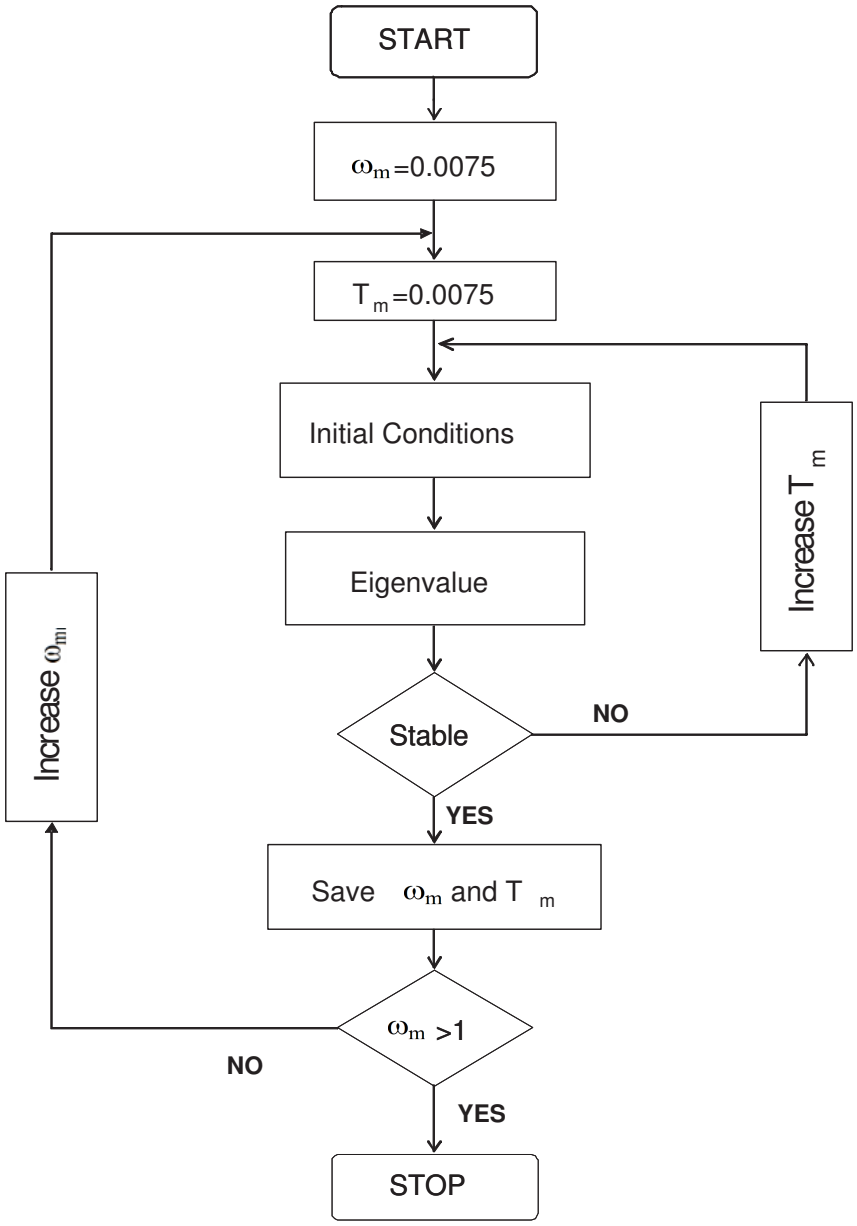

Figure 4.4: The flowchart to determine the stability boundaries of the system

Two regions are shown in Fig. 4.5. Region A, where the real part of the eignvalue are all negative which means that the system is stable. At Region B, at least one real part of

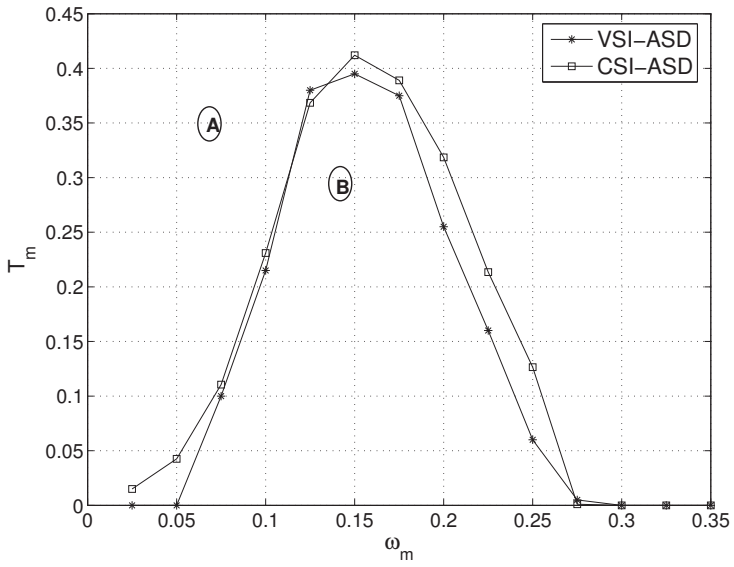

Figure 4.5: ASD Connected to the system without DSTATCOM

the eigenvalues is positive, which indicates that the ASD is unstable [71]. On the curve, at least one of the real part of the eigenvalues is zero, or the system is working in a sustained oscillating mode.

4.5.2 Effect of DSTATCOM Control Technique on The ASD

In this section, the effect of the DSTATCOM control technique on the CSI based ASD and the VSI based ASD will be studied. Figure 4.6 portrays the stability curves of the ASD for the two operating strategies of the DSTATCOM. The first (top) row in Fig. 4.6 exhibits the stability curves for a VC-DS, whereas, the second (bottom) row shows those curves for CC-DS.

It is evident that the stability limits for the VSI-ASD and CSI-ASD are enhanced by the installation of the VC-DS. Although the CC-DS can improve the voltage quality, it barely has an effect on the stability curves of the ASD, the CSI and VSI. It can be concluded from Fig. 4.6 that the VC technique is recommended to control the DSTATCOM when it is installed near an ASD.

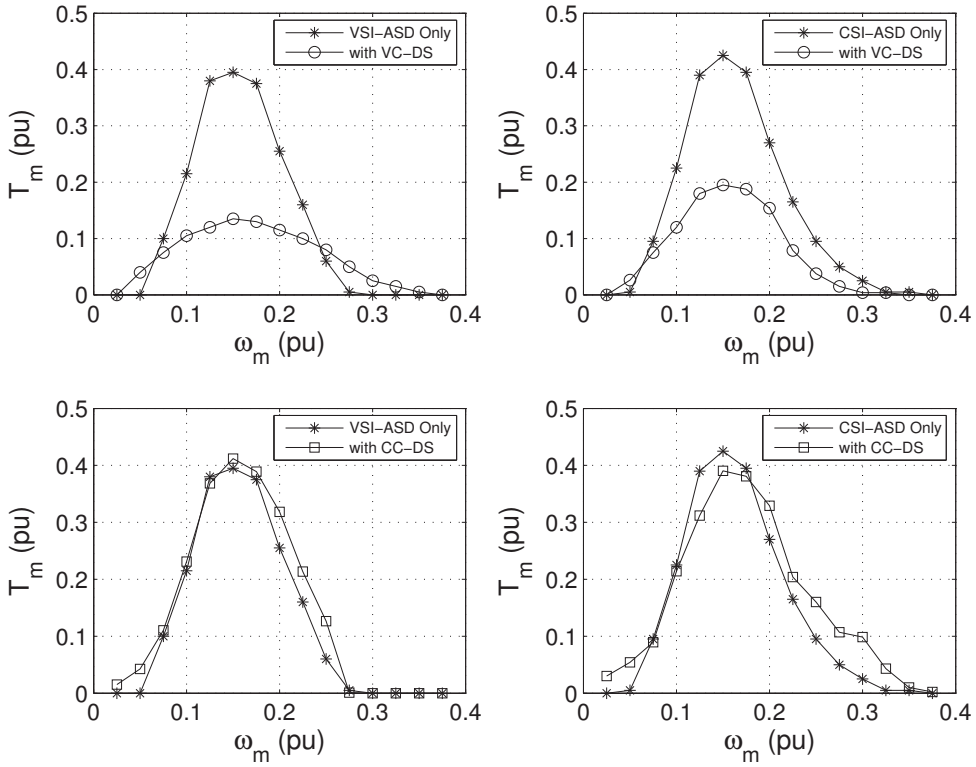

Figure 4.6: Effect of the DSTATCOM controller on the ASD stability curve

4.5.3 Effect of the induction motor inertia

During the operation of the IM, the load varies widely and so does the inertia of the load. Therefore, it is beneficial to study the effect of the inertia variation on the studied system. In this study, the inertia of the IM mentioned in Appendix A, takes values of 2, 1, and 0.5 times of the value mentioned in Appendix A.

Figure 4.7 shows the stability curve of the ASD while the DSTATCOM is controlled as the VC. No doubt that the larger the inertia, the better the stability limits of the ASD are. This improvement in the stability limits is mainly due to the increase of the IM inertia.

The stability curves of the ASD with different IM inertia, while the DSTATCOM is controlled as the current source, are plotted in Fig. 4.8. These curves verify that the increase in the machine and load inertias improve the stability curves.

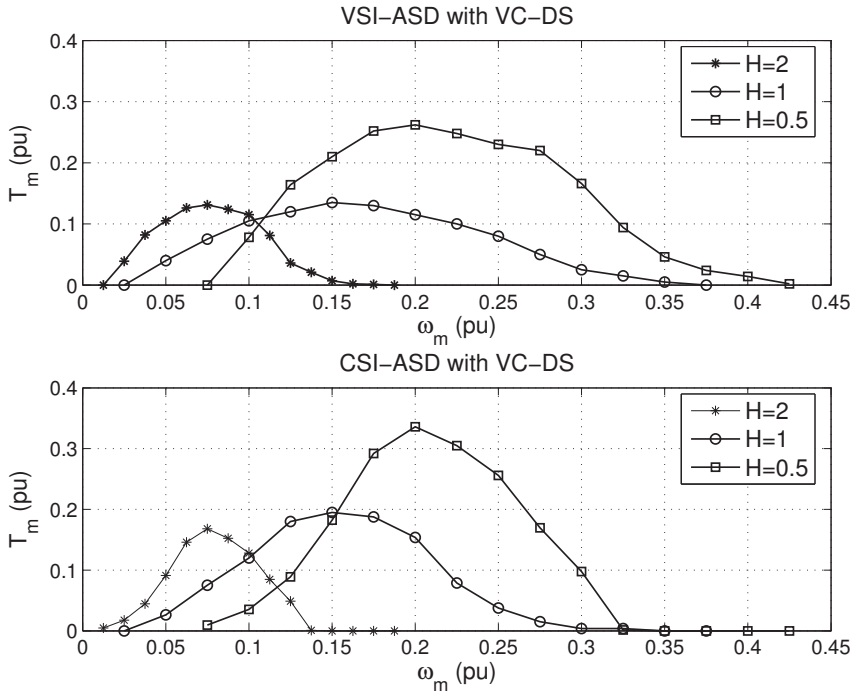

Figure 4.7: Effect of the IM inertia on stability of ASD in existence of VC-DS

4.5.4 Effect of The DSTATCOM Capacitor

The choice of the DC-capacitor of the DSTATCOM depends on a particular design and can have different values, therefore this section is dedicated to study the effect of the variation in this capacitance value. The value of C_{dc} varies by 2, 1 and 0.5 of the the value mentioned in Appendix A. Figure 4.9 displays the stability curves of the VSI-ASD when the DSTATCOM is controlled as VC with different values of C_{dc}. It is evident that the capacitance value has a slight effect on the stability curve. However, the CC-DS exhibits sharp irregularities on the stability curve.

Figure 4.10 illustrates the stability curves of the CSI-ASD. From this figure, it is clear that the VC-DS is less affected by the value of C_{dc}. However, it is obvious that the stability curves are extremely affected by the capacitance value when the DSTATCOM is controlled as CC.

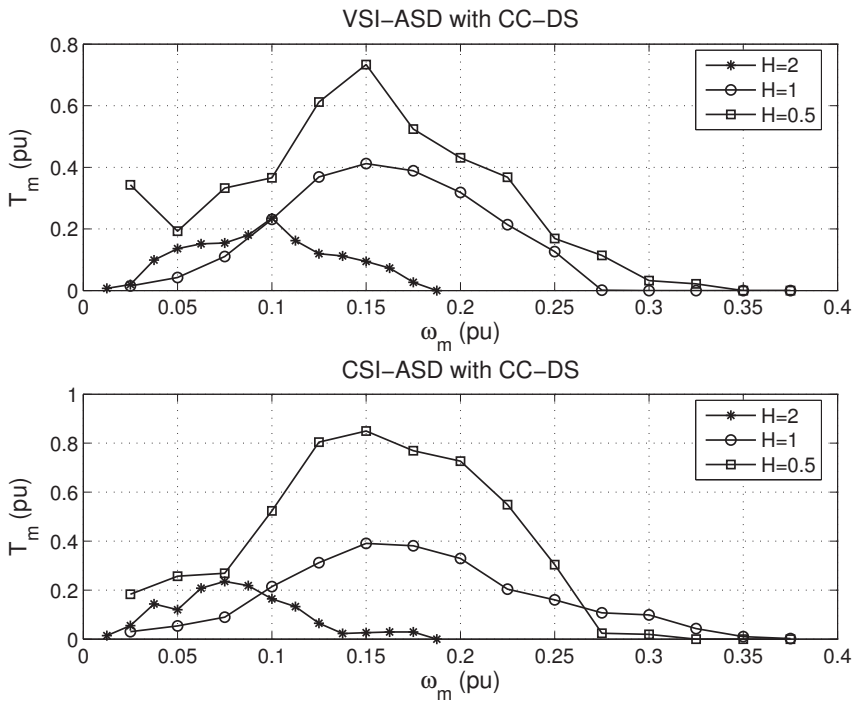

Figure 4.8: Effect of the IM inertia on the stability of the ASD with an CC-DS

It can be concluded from Fig. 4.9 and Fig. 4.10 that the ASD stability is less influenced by the capacitance value of the *dc* side when the VC-DS is installed in the distribution system. To study this phenomenon analytically, the characteristic equation of the DSTATCOM system is explored in this section. The Characteristic Equation (CE) of the dynamic system given in (4.1) is written as [72]

$$CE \;=\; \|A\| \tag{4.25}$$

To carry out the investigation, the DSTATCOM is considered to be connected to Thevenin's equivalent circuit as shown in Fig. 4.11 where R_{th} and x_{th} are the equivalent Thevenin impedance seen by the DSTATCOM. Thevenin's equivalent impedance depends on the equivalent impedance of the ASD which is a function of the operating conditions of the induction motor, *i.e.* the operating speed and the mechanical torque. Therefore,

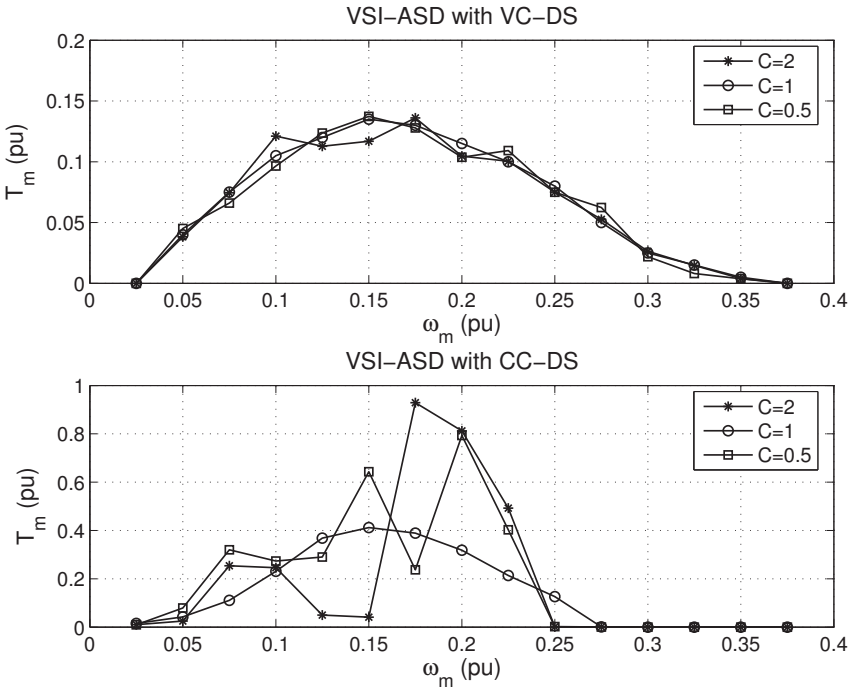

Figure 4.9: Effect of the C_{dc} on the VSI-ASD

Thevenin's equivalent impedance is also a function of ω_m and T_m which vary widely.

4.5.4.1 Characteristic Equation Analysis of the Voltage Control DSTATCOM

Figure 4.12 shows the equivalent circuit of the DSTATCOM shown in Fig. 4.11, when it is controlled as a voltage source, where $x_e = x_t + x_{th}$ and $R_e = R_t + R_{th}$.

For an ideal capacitor, the shunt conductance can be neglected, and the CE is given by

$$CE_{VC-DS} = \frac{-3}{2} \times \frac{R_e m^2}{x_e^2 C_{dc}} \tag{4.26}$$

Equation (4.26) shows that the characteristic roots of the VC-DS depend on the system parameters, x_e, R_e, and C_{dc} as well as the control signal of the amplitude, m. Solving the CE with respect to one of those parameters determines the critical value for each parameter.

It is obvious that the only value of C_{dc} that makes the CE equal to zero is at $C_{dc} = \infty$.

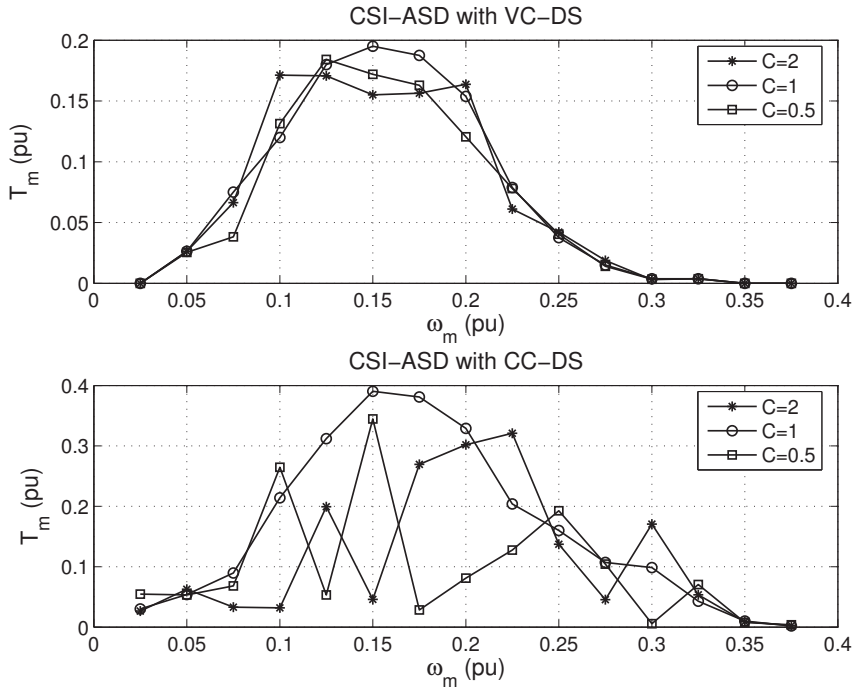

Figure 4.10: Effect of the C_{dc} on the CSI-ASD

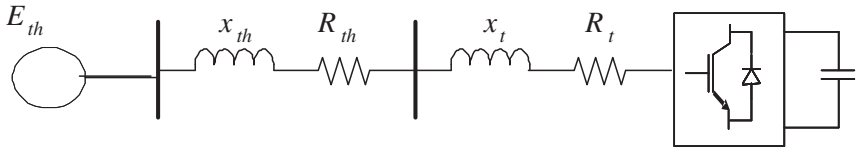

Figure 4.11: Thevenin's equivalent circuit of DSTATCOM

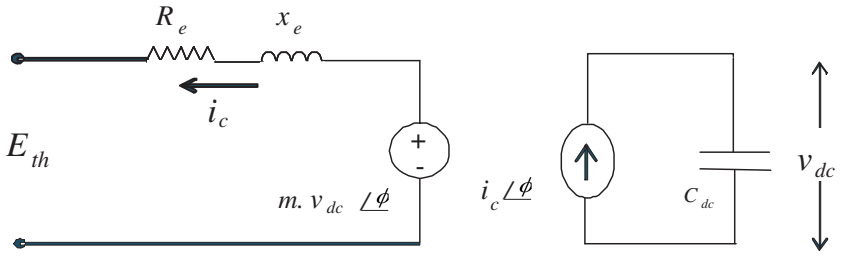

Figure 4.12: Equivalent circuit of VC-DS

This means the capacitor is disconnected or an open circuit. In addition, at $m = 0$, the CE is zero too. However, the $m = 0$ condition means that the capacitor is a short circuit. Neither of those two conditions are considered to be normal operating condition and the protection of the DSTATCOM is activated and disconnects the DSTATCOM upon the initiation of the either conditions.

In general, the stability limits of the VC-DS are neither affected by the *dc* link capacitance value nor by the operating conditions of the ASD. It can be concluded that the system is stable for all the operating points of the ASD.

4.5.4.2 Characteristic Equation Analysis of The Current Control DSTATCOM

The DSTATCOM in Fig. 4.11 can be controlled as a current source, and the equivalent circuit is given in Fig. 4.13.

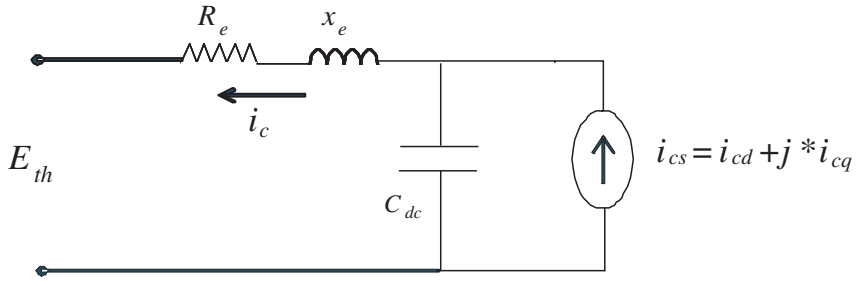

Figure 4.13: Equivalent circuit of CC-DS

If the shunt conductance of the dc-capacitor is neglected, the CE of the CC-DS is computed by

$$CE_{CC-DS} = \frac{(R_e^2 - x_e^2)C_{dc}^2 + 2x_e C_{dc} - 1}{{C_{dc}}^2 {x_e}^2} \tag{4.27}$$

By solving this equation with respect to C_{dc}, the two critical values of the *dc* side are

$$C_{dc,\ critical} = \frac{x_e \pm R_e}{{x_e}^2 - {R_e}^2} \tag{4.28}$$

Equation (4.28) indicates that the critical values of the capacitance depend only on the equivalent impedance of both the Thevenin and the filter. However, the Thevenin equivalent impedance depends on the system connected loads including the loading and speed of the IM. During the operation of the ASD, its equivalent circuit varies widely and so does the Thevenin's equivalent impedance. It is possible that the equivalent impedance, seen by the DSTATCOM along with the filter impedance, is equal to the critical value of the *dc* capacitance, therefore ASD will be unstable. This explains the irregularities that appear, when the DSTATCOM is controlled as a current source.

From the aforementioned analysis, it can be concluded that the CC-DS is affected widely by the operating condition of the system.

4.6 Summary

In this chapter, the DSTATCOM effects on the ASD stability boundaries are investigated. The study reveals that the VC-DS can improve the stability limits of both the VSI based ASD and CSI based ASD at lower speeds.

The stability boundaries are found to be less affected by the variation in the capacitor value of the *dc* side of the DSTATCOM, when it is controlled as a voltage source. On the other hand, the stability limits are found to be extremely affected by the capacitance value when the DSTATCOM is controlled as current source. This result is investigated analytically by using the characteristic equation of both the CC-DS and the VC-DS.

The characteristic equations of both the voltage and the current source control DSTATCOM are solved to compute the critical capacitance that brings the system to the unstable region. The critical value for the VC-DS is either zero or infinity, *i.e.* when the capacitor is faulted by either an open circuit or a short circuit. Under normal operation conditions, there are no critical values of the capacitor as far as it is able to supply adequate reac-

tive power. On the other side, the critical value for the CC-DS depends on the operating conditions of the system, *i.e.* depends on the loading condition of the IM and on its speed.

Chapter 5

Energy Operator: Theory and Design

Chapter 2 establishes the fact that the RCU requires a fast and accurate method to track the voltage envelope of the voltage at the PCC. In this chapter, a novel algorithm, based on calculating the EO of a sinusoidal waveform for Envelope Tracking (ET) purpose, is presented. The mathematical derivation of the proposed algorithm as well as the various circuit designs required to realize it, are described. The novel algorithm is fast and robust, and requires only few samples to calculate the envelope of a given signal.

5.1 Introduction

The sag, swell, and flicker mitigation depends on injecting a certain amount of reactive power, defined by the difference between, the reference-voltage and the measured-voltage amplitudes. As a result, the measurement accuracy and robustness are crucial. Voltage amplitudes measurement depends principally on the accuracy of the ET algorithm. The envelope tracker should be accurate, robust, and fast with the least mathematical burden.

The voltage envelope is either calculated or estimated. Different signal processing algorithms, such as, the Fast Fourier Transform (FFT) [73], [74] and the Wavelet [75], [76] are adopted to calculate the voltage envelope. However, these algorithms introduce a lag in the envelope tracking that is equal to the length of the used window. It is this delay

that imposes some limitations on the on-line application of these algorithms.

The envelope of the voltage signal can be estimated by various estimation methods such as the Kalman Filter (KF) [77], the Least Absolute Value (LAV) [78], the Simulated Annealing (SA) [79], and the ADAptive LInear NEuron (ADALINE) [80]. Although the KF is fairly accurate, it has a high mathematical burden which limits its use for on-line tracking. The LAV and SA algorithms require that the flicker waveform is known in advance which is not a realistic assumption. Although the ADALINE is efficient and has a fast convergence, compared to other estimation algorithms, the ADALINE is still considered mathematically cumbersome.

In [81], it is proven that the energy contained in a sinusoidal signal is proportional to the square of the signal amplitude. Thus, it is proposed in [82] to use the energy operator to track the envelope by tracking the amplitude of the signal. The Teager Energy Operator (TEO) is successfully applied to achieve this task since the TEO calculates the energy, and in turn, the amplitude, by only three samples [83]. Since, the algorithm does not depend on any kind of estimation or optimization, the algorithm is considered suitable for on-line tracking. Moreover, the delay between the actual envelope and the tracked envelope is within two samples only. However, the algorithm's practical application indicates that large spikes are embedded in the tracked envelope which is a fatal drawback in using these measurements for flicker mitigation techniques. In addition, these spikes reach very high values when the level of the amplitude is suddenly changed [82], [84].

In this chapter, tracking the fluctuation in the voltage waveform is achieved by a novel algorithm to calculate the energy operator. The proposed algorithm attains the same TEO advantages; simple, fast, robust, and independent of estimation techniques. Yet, the new algorithm overcomes TEO drawbacks; insensitive to noise and immune to severe spikes in voltage magnitude.

5.2 Voltage Amplitude Variation

Ideally, the voltage magnitude should be a constat value, but practically it is characterized by slow changes in the root mean square (rms) of the voltage due to several loads switching or loading conditions. These changes can be represented by either a modulated signal or generated experimentally by utilizing nonlinear or switching loads.

5.2.1 Computer Simulation

The slow changes in the rms are represented by the following amplitude modulation:

$$v = [A_o + f(t)]sin(\omega_o t) \tag{5.1}$$

where A_o is the amplitude of the fundamental, ω_o is the fundamental frequency and $f(t)$ is the modulating signal that can have different shapes such as a square wave, sinusoidal wave, triangle wave, or even random wave.

5.2.2 Laboratory Simulation

Figure 5.1 depicts a simple PQ generator which consists of two loads, connected at the PCC. The first load is a linear load which is represented by a resistance, whereas the second load is a nonlinear load, composed of a resistance series with a bidirectional power electronic switch such as a triac.

When the triac is ON, the voltage at the PCC drops and recovers again when the triac is turned OFF. If the triac is kept triggered at a constant frequency, less than the power frequency, the voltage at the PCC will fluctuate and generate voltage flicker at the PCC. While the amplitude of the voltage drop is determined by the value of the resistance, the frequency of the fluctuation is controlled by the switching frequency. Switching a resistance of 2/3 of the load at 16 Hz results in the voltage fluctuation that is represented in Fig. 5.2. A full description of the PQ generation in the lab is given in [84].

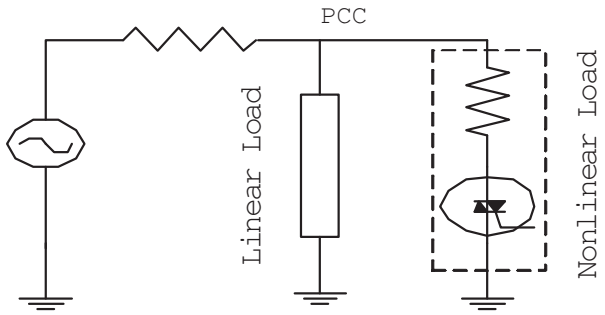

Figure 5.1: Laboratory PQ generator

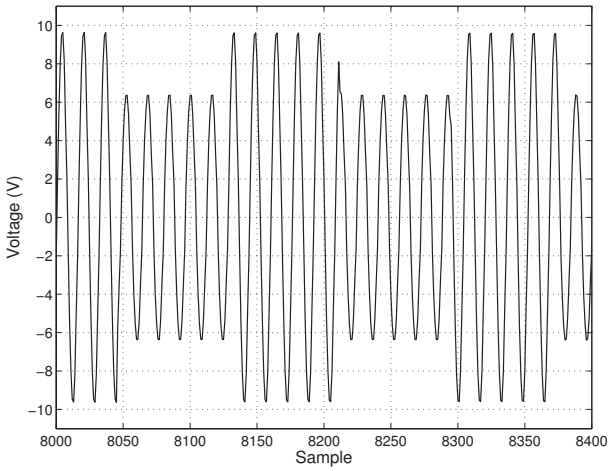

Figure 5.2: Voltage at the PCC using the PQ generator

5.3 Energy Operator (EO)

5.3.1 Teager Energy Operator (TEO)

The EO of any signal, v, is given as the summation of kinetic energy, $(\frac{dv}{dt})^2$, and potential energy, $(v\frac{d^2v}{dt^2})$, of the signal. In [81], Teager proves that the Energy, E, in a simple harmonic oscillation is proportional to the squares of the amplitude, A, and the frequency, ω. The TEO can be computed as follows:

$$TEO = (\frac{dv}{dt})^2 - v(\frac{d^2v}{dt^2}) = A^2\omega^2 \tag{5.2}$$

Later, Kaiser proved in [83], that, TEO can be calculated by using three consequent samples as follows:

$$TEO \;=\; E \;=\; A^2\omega^2 = v_k^2 - v_{k-1}v_{k+1} \tag{5.3}$$

where v_{k-1}, v_k and v_{k+1} are three consequent samples of the signal.

Two notable features of Kaiser's algorithm are its fast tracking (only two multiplication and one subtraction are required) and robustness (as there is no singular point). With the aforementioned advantages, the TEO is used, in [84], to track the envelope of the voltage at the PCC utilizing the setup described in Section 5.2.2. Despite the superior advantages of the TEO, the tracked envelope displays severe spiking as high as 50% of the true value, as exhibited in Fig. 5.3. These spikes prevent the practical implementation of TEO.

5.3.2 Proposed Algorithm

Let v be the voltage signal, given by:

$$v \;=\; A\ sin(\omega t) \tag{5.4}$$

It is assumed that this signal is shifted, once, by a lead angle equal to ϕ, and at another time, by a lag angle equal to ϕ, also. The shifted signals are given by the following:

$$v^+ \;=\; A\ sin(\omega t + \phi) \tag{5.5}$$

$$v^- \;=\; A\ sin(\omega t - \phi) \tag{5.6}$$

Multiplying (5.5) and (5.6) gives:

$$v^-v^+ = \; A\ sin(\omega t - \phi)\ A\ sin(\omega t + \phi) \tag{5.7}$$

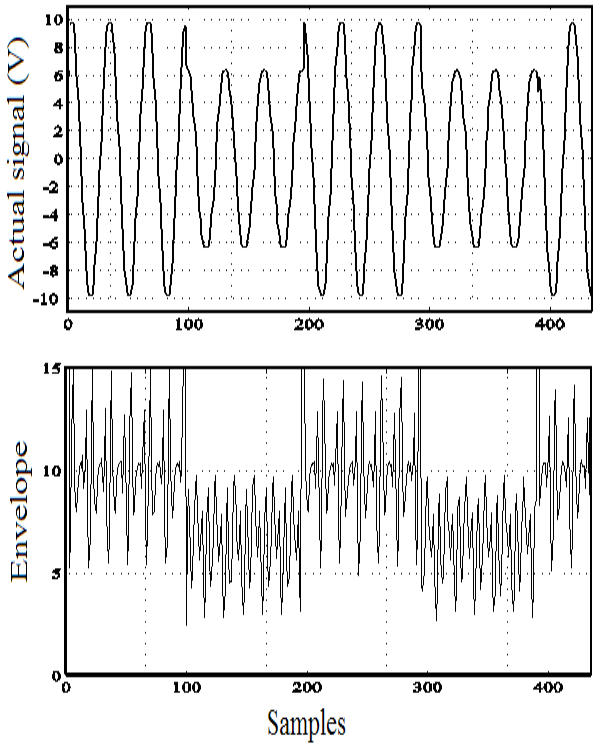

Figure 5.3: Voltage waveform with voltage fluctuation and tracked by TEO

using the trigonometric identity

$$sin(\omega t \pm \phi) = \ sin(\omega t)cos(\phi) \pm cos(\omega t)sin(\phi) \tag{5.8}$$

and substitute in (5.7) gives:

$$v^{-}v^{+} = \ A^2[\ sin^2(\omega t)cos^2(\phi) \ - \ cos^2(\omega t)sin^2(\phi)] \tag{5.9}$$

Now, consider the following equation:

$$\begin{aligned} v^2 - v^{-}v^{+} &= A^2 sin^2(\omega t) \\ &\quad - A^2[sin^2(\omega t)cos^2(\phi) - cos^2(\omega t)sin^2(\phi)] \end{aligned} \tag{5.10}$$

using the identity $cos^2(\phi) = 1 - \ sin^2(\phi)$ in (5.10) yields

$$v^2 - v^- v^+ = \ A^2[\ sin^2(\omega t) sin^2(\phi) \ + \ cos^2(\omega t) sin^2(\phi)] \tag{5.11}$$

which could be simplified to give the EO as:

$$EO = v^2 - v^- v^+ = \ A^2 sin^2(\phi) \tag{5.12}$$

Consequently, the the amplitude of the signal is given by:

$$A(t) = \sqrt{\frac{v^2 - v^- v^+}{sin^2(\phi)}} \tag{5.13}$$

Equation (5.12) is a continuous, not discrete, expression of the amplitude, or the envelope, of a sinusoidal signal. It is important to high light the fact that the TEO can be derived from the proposed algorithm by using a shift angle that is equal to one sample, *i.e.*, $\phi = 2\pi/T_S$ where T_s is the sampling time.

There are advantages of the new algorithm are: a) it is very simple algorithm, b) its continuous form is presented here, the discrete form can be obtained depending on the used shifting circuits, c) it performs fast tracking of the actual envelope, depending on the time constants of the shifting circuits, d) its hardware is inexpensive to implement, e) it is independent of the initial values of the signal, and f) its digital form is robust since it does not contain any division and thus, no singularity. The newly devised algorithm can perform fast tracking, in a fraction of the cycle, therefore it can help in manipulating the sag and the swell. Since, the tracked signal by the proposed algorithm should be harmonic free, it should be filtered before the new algorithm is applied.

5.4 Design of The Shift Circuit

The shifted signals, v^+ and v^- are obtained by using different shifting circuits. In this paper, these shifting circuits are explored with the emphasis on the design aspects and advantages of each circuit. To represent the worst case, the circuit is tested by initiating a sudden change in the amplitude occurs.

5.4.1 Shift Circuit Using the Inductive-Capacitive Circuit

For a branch of inductor L in series with resistance R_L, as illustrated in Fig. 5.4, the voltage across the resistance lags the original voltage by angle, ϕ_L, and is given by

$$\phi_L = tan^{-1}(\frac{\omega L}{R_L}) \tag{5.14}$$

Also, for a branch of capacitor C with resistor R_C, the voltage across the resistance leads the original signal by:

$$\phi_C = tan^{-1}(\frac{1}{\omega C R_C}) \tag{5.15}$$

Since the lead and lag angles need to be equal, the angles in (5.14) and (5.15) must be equal to yield

$$\omega = \frac{R_L}{R_C}\sqrt{\frac{1}{LC}} \tag{5.16}$$

The choice of the shift angle is important because it determines the time constant of each branch. The time delay of the shifting circuit is determined by the largest time constant of any branch in the circuit. To ensure a fast response, it is required to keep the time constant of both branches must be kept as small as possible.

The time constant of each branch is given in terms of the shift angle as:

$$\tau_L = \frac{L}{R_L} = \frac{tan(\phi)}{\omega} \tag{5.17}$$

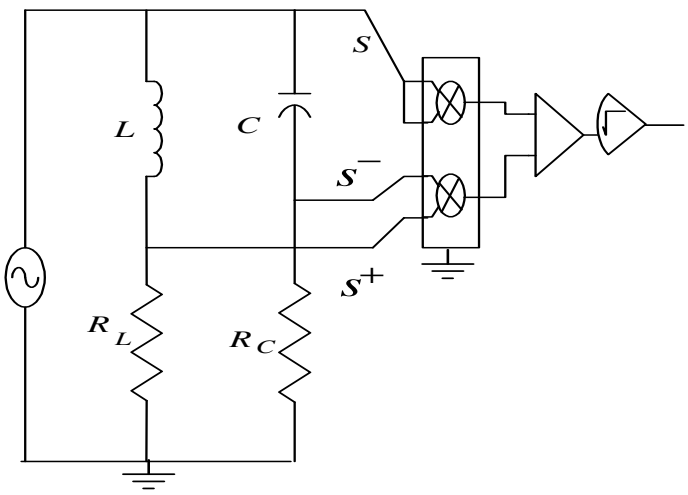

Figure 5.4: Envelope tracking using the inductive-capacitive circuit.

and

$$\tau_C = R_C C = \frac{1}{tan(\phi)\omega} \tag{5.18}$$

where $\phi_L = \phi_C = \phi$

Equations (5.17) and (5.18) indicate that there is a trade off between the two time constants. A small shift angle results in a large capacitive time constant and a small inductive time constants. To determine the best shifting angle, the time constant of the inductive branch, τ_L, and capacitive branch, τ_C, are plotted versus the shifting angle in Fig. 5.5. The best shifting angle is the one that gives minimum time constant for both branches. This angle is found to be at the intersection of both the time constant lines. It is evident that below the intersection point, the circuit will be slower due to the large time constant of the capacitive branch. While above the intersection point, the inductive time constant will be large. Therefore, the point of intersection gives the optimum time constant of the circuit. The optimum angle is found to be $\frac{\pi}{4}$ where both the time constants

are equal to $\frac{1}{\omega}$.

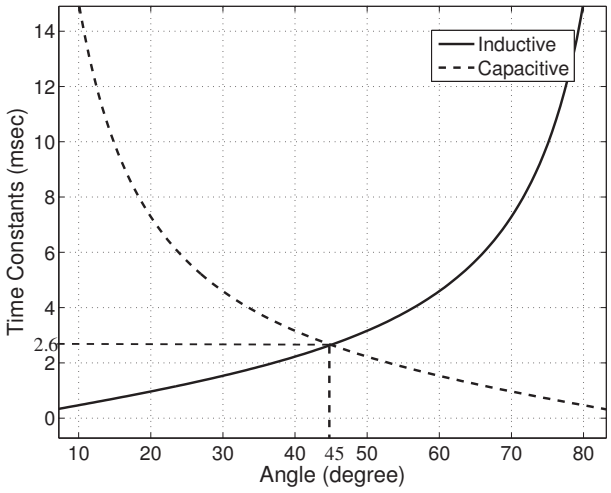

Figure 5.5: Time constant versus shift angle or inductive and capacitive branches

Although the results obtained by the inductive-capacitive circuit are satisfactory as displayed in Fig. 5.6, the values of the inductor and the capacitors are not available. For example, with resistance of $R_L = R_C = 100\ \Omega$, the values of the inductor and the capacitor used in the simulation are 265.4 mH and 26.5 μF, respectively. These values are not standard and need to be replaced by other components that might result in an inadequate response. However, this method is recommended when the algorithm is implemented in digital form.

Also, the results show that the algorithm gives satisfactory results, when the shift angle is varied between 45^o to 65^o with the best response at the angle of 45^o. However, for smaller angles, the time constant of the inductive circuit is smaller than that of the capacitive circuit and large spikes begin to appear.

5.4.2 Shift Circuit Using the Doubly Capacitive Circuit

The second passive circuit that can be utilized to produce the shifted signal is a circuit of the two capacitive branches with lead angles equal to ϕ_c and $2\phi_c$, resulting in signals v^+

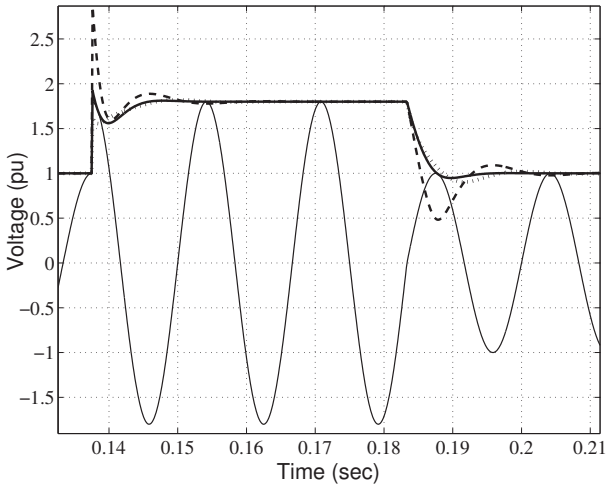

Figure 5.6: Tracking sharp changes using inductive-capacitive circuit with various shifting angles (- - - 35^o — 45^o ... 65^o)

and v^{++} respectively. Now, signal v^{+} leads the original signal by ϕ_c and lags v^{++} by the same angle. As a result, the proposed algorithm is written as,

$$A^2 sin^2(\phi) \;=\; (v^{+})^2 - v\; v^{++} \tag{5.19}$$

The circuit implements this configuration is shown in Fig. 5.7. Figure 5.5 signifies that the capacitive branch should work at large angle to produce small time constant; however, the maximum allowable shift angle is 45^o as its double is 90^o which is the maximum shift angle that can be achieved using this circuit. The time constant of the circuit should not be too small; otherwise the algorithm will mimic the TEO resulting in spikes discussed in Section 5.3.1.

The results of the circuit are exhibited in Fig. 5.8 with shift angles of 10^o, 22^o, and 44^o. At shift angle 10^o, the time constant is too large, longer than four cycles, and it takes a long time before reaching the steady state. On the other hand, at shift angle 44^o the time constant is very small, close to the sample time, and so the spikes start to appear. The best performance of this circuit is achieved at an angle of 22^o where a balance between the spikes and the large time constant is achieved.

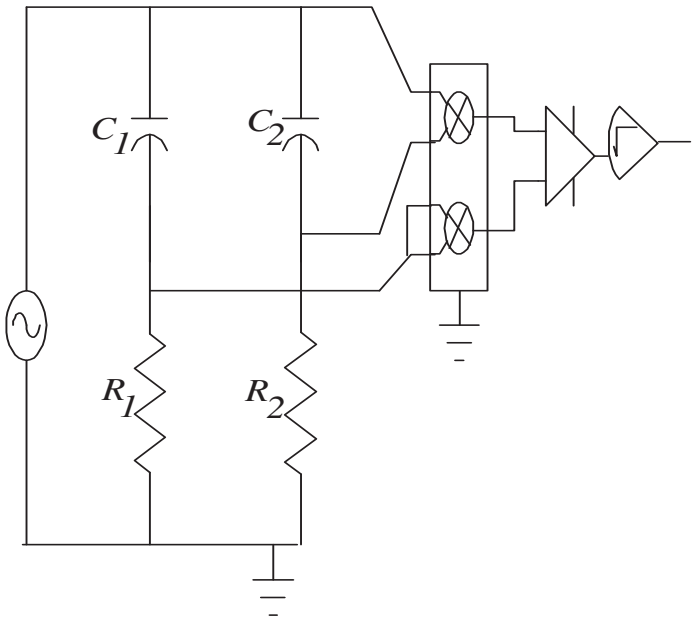

Figure 5.7: Envelope tracking using the doubly capacitive circuit

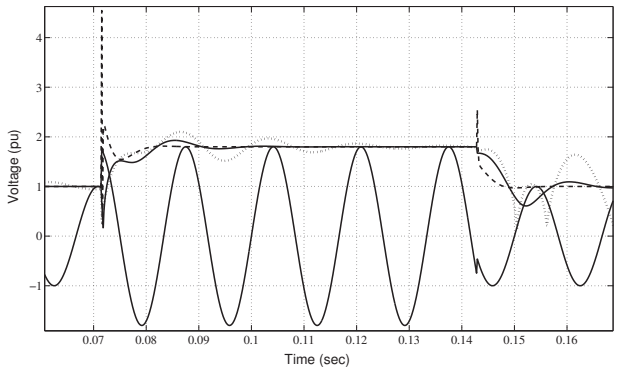

Figure 5.8: Tracking sharp changes using doubly capacitive circuit with various shifting angles (- - - 44^o — 22^o ... 10^o)

5.4.3 Shift Circuit Using Doubly Inductive Circuit

The third passive circuit is similar to the capacitive circuit, but with two inductive branches with lag angles equal to ϕ_L and $2\phi_L$ to give signals as v^- and v^{--} respectively. Now, the signal v^- lags the original signal by ϕ_L and leads v^{--} by the same angle. Consequently, the proposed algorithm is written as

$$A^2 sin^2(\phi) \;=\; (v^-)^2 - v\; v^{--} \tag{5.20}$$

The circuit that implements this configuration is similar to the one shown in Fig. 5.7 where the capacitors are replaced by inductors. The results are similar to those obtained by the capacitive circuit. It is evident that inductive circuit creates spikes at the lower angles, characterized by a small time constant, and is severely delayed at high angles. This is observed in Fig. 5.9 with the best results occurring at an angle of 22^o.

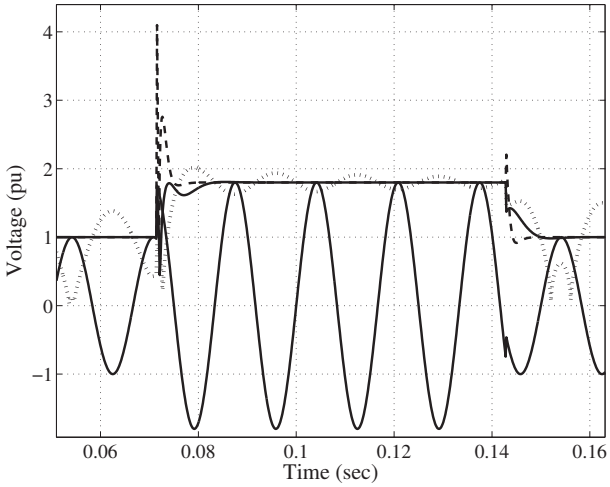

Figure 5.9: Tracking sharp changes using doubly inductive circuit with various shifting angles (- - - 10^o — 22^o ... 44^o)

5.4.4 Shift Circuit Using Transfer Function Circuit

Another circuit that should be considered is the well known lead-lag Transfer Function (TF),

$$TF = \frac{aTs + 1}{Ts + 1} \tag{5.21}$$

The TF in (5.21) can be a lead or a lag network according to the value of a [85]. The shifted signals could be realized by using two transfer functions, one to give the lead signal

in the form of

$$TF_{lead} = \frac{a_d T_d s + 1}{sT_d + 1} \tag{5.22}$$

and the other to give the lag signal in form of

$$TF_{lag} = \frac{a_g T_g s + 1}{sT_g + 1} \tag{5.23}$$

To ensure the best performance, the time constant of both TFs, lead and lag, should be as minimum as possible, but the minimum time constant is limited by the sampling time. The best response that can be obtained when the time constant equals the sampling time.

$$T_d \;=\; T_g \;=\; T_s \tag{5.24}$$

Since the lead and lag shift angles need to be equal, the following relation has to be valid [85]

$$a_d \;=\; \frac{1}{a_g} \;=\; a \tag{5.25}$$

Figure 5.10 illustrate the envelope tracked by the proposed algorithm with a lead-lag network with different values of a. It is obvious that at $a = 2$, the envelope converges to the actual envelope faster than when $a = 5$ and $a = 10$, however, the algorithm results in the appearance of spikes. Although these spikes do not attain severe values, such as those in inductive circuits or in the TEO, the rate of change of the spike can cause damage to any electronic components in the control circuit such as the Digital to Analog Converter (DAC). Moreover, at $a = 10$, the algorithm does not demonstrate a noticeable spike and it attains the actual value in less than one cycle.

Fig. 5.11 displays the percentage of error in the three cases. It is evident that when $a = 2$, the percentage of error falls to less than 5% in 0.2 of a cycle whereas percentage of error reaches the same percentage in 0.3 of a cycle when $a = 5$ and $a = 10$. However, the

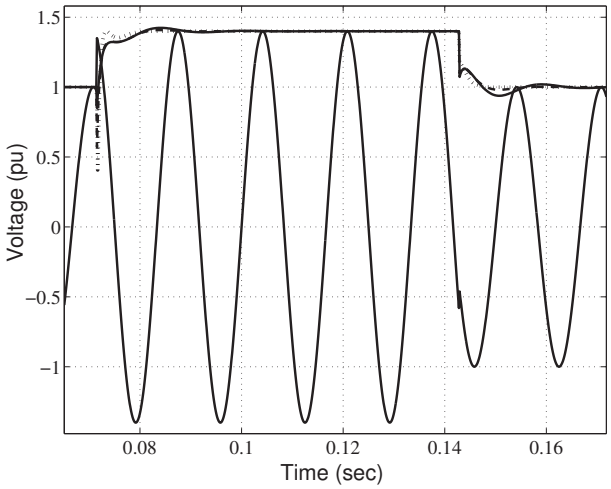

Figure 5.10: Tracking sharp changes using the TF circuit with various a (— 10 - - - 5 ... 2)

spike reaches as high as 90% when $a = 2$, but only 60% and 40% in the other two values.

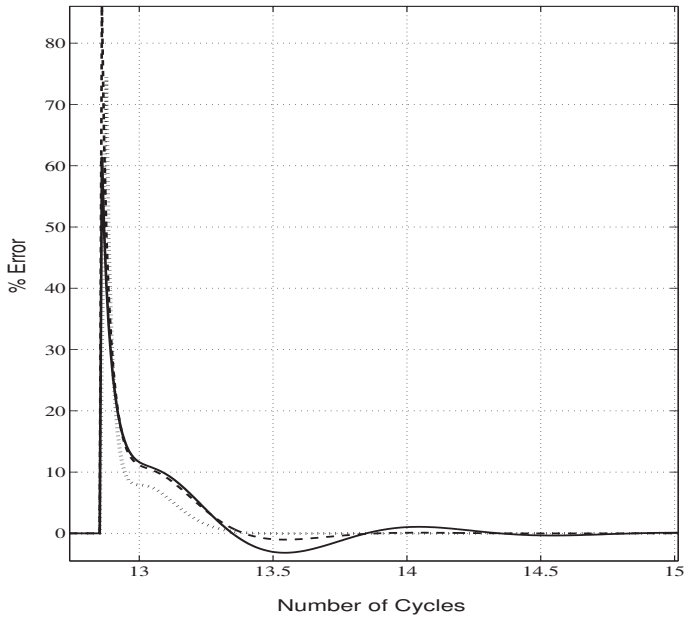

Figure 5.11: Error in tracking the envelope of sinusoidal waveform by TF with different values of a. (— 10 - - - 5 ... 2)

5.5 Simulation Results

In the previous section, the square wave envelope is used to design the lead-lag circuits. In this section, these circuits are tested with different envelope shapes to verify the designs. The circuits that will tested are:

- the inductive-capacitive circuit with $\phi = 45^o$
- the doubly capacitive with $\phi = 22^o$
- doubly inductive with $\phi = 22^o$
- the TF of lead-lag circuit with $a = 2$ and $T_s = 125\mu s$

Fig. 5.12 reflects a sinusoidal waveform, modulated by a sinusoidal waveform with frequency ($\frac{1}{10}$) of the fundamental frequency to simulate the periodical operation of rolling mills and pumps [86]. The results show that the error in the tracked envelope is less than 1.5% with all circuits.

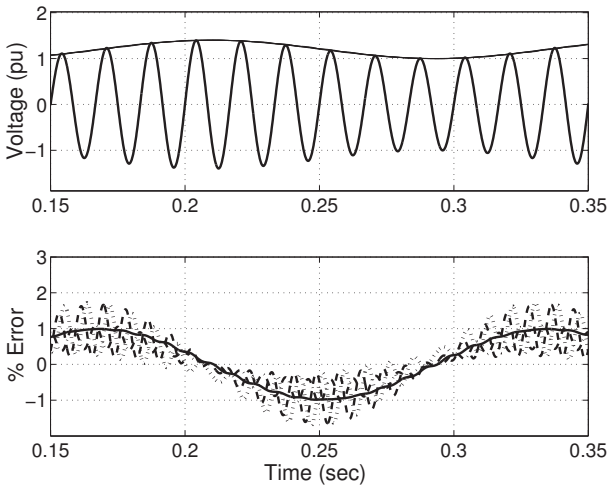

Figure 5.12: Tracking a voltage enveloped by sinusoidal wave of (1/10) of the fundamental frequency of utilizing different circuits. (... LL - - -CC -.-.-. LC — TF)

Consistently, the flicker caused by an arc furnace is always characterized by random changes in the amplitude [87]. Thus, it is necessary to test the novel algorithm to track

these random changes in the amplitude. To conduct the test, a sinusoidal waveform of unity amplitude with superimposed random changes in the amplitude of 0.1 variance and zero mean value will be tested. Fig. 5.13 presents the best three results for the tracked envelope. The mean square errors are found to be 6.3%, 5.8%, 14%, and 87.6% for the inductive-capacitive, TF, doubly capacitive and doubly inductive circuits, respectively.

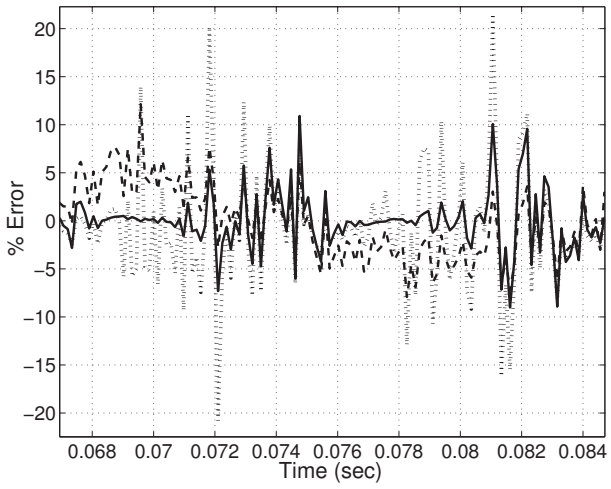

Figure 5.13: Tracking the envelope of a sinusoidal waveform by a lead lag network (— LC - - - TF ... CC)

5.6 Experimental Results

To evaluate the performance of the new algorithm, a simple PQ generator is built in the lab, as described in Section 5.2.2, and the voltage envelope is tracked by using a DSP that utilizes the discrete form of the proposed algorithm. The complete description of the laboratory setup is given in [84], and the discrete form of the proposed algorithm is described in the following section.

5.6.1 Discrete Form

The previous sections explore a number of circuits that can be implemented by using analogue circuits. It is more convenient to have the discrete form of (5.12) that can be used in digital calculation such as the DSP and virtual instruments. The sampling rate of the Analog to Digital Converter (ADC) of the digital system should be known in advance to choose the time constant of the circuit that will be implemented. There is no doubt that, the smaller the sample rate, the better the result.

The digital form can be realized with any numerical integration technique, such as Euler. The transfer function in (8.4) gives the shifted voltage signal,v^s, as:

$$v^s = \frac{aTs + 1}{Ts + 1}\, v \tag{5.26}$$

By applying Euler's backward method of integration to (8.5),

$$\begin{aligned} v_k^+ &= d_1 v_k + d_2 v_{k-1} + d_3 v_{k-1}^+ \\ v_k^- &= g_1 v_k + g_2 v_{k-1} + g_3 v_{k-1}^- \end{aligned} \tag{5.27}$$

The complete derivation of the constants is given in Appendix C. By substituting (6.8) in (5.12), the discrete form of the algorithm is provided.

5.6.2 Laboratory Results

A square envelope of the voltage signal is tracked by using the aforementioned setup in the lab; and the results are plotted in Fig. 5.14. The simulation shows that the best performance is obtained by the TF and the LC circuits, therefore, both circuits are implemented on a DSP (C2000LF2704 from Texas Instrument). Compared with the results obtained by the TEO, it is clear that the large spikes disappear except for small spikes due to the noise in the signal. This small percentage of high frequency noise is taken care of by a low-pass filter, as denoted in Fig. 5.15, where the envelope is filtered by a simple second

order low-pass filter. Since the amplitude of the signal changes at the peak point of the signal, the TEO exhibits large spikes that are more than twice the true value, whereas the proposed algorithm does not exhibits any spikes.

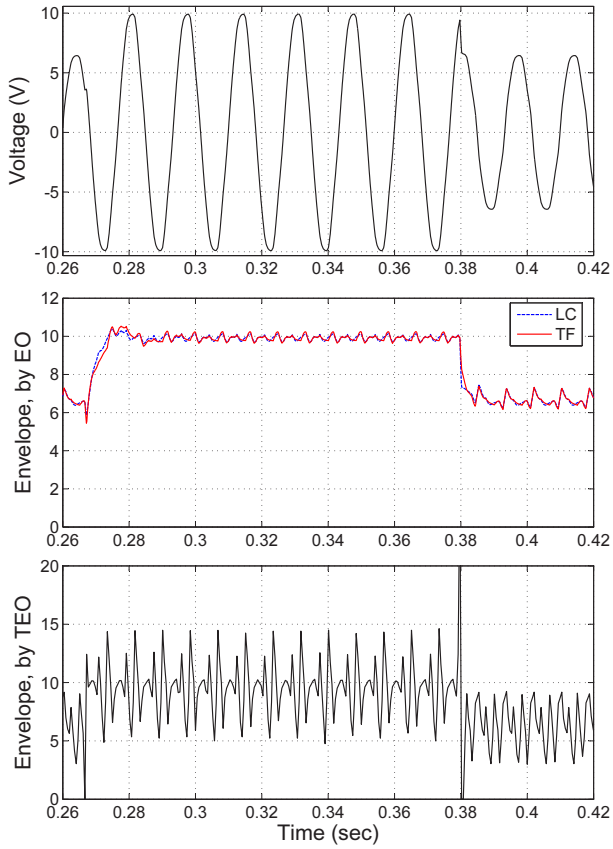

Figure 5.14: Envelope tracking by the proposed EO algorithm and TEO experimental results

5.7 Summary

In this chapter, a novel algorithm is proposed to calculate the energy of a periodic signal. This algorithm is used to compute the instantaneous changes in the amplitude, and thus,

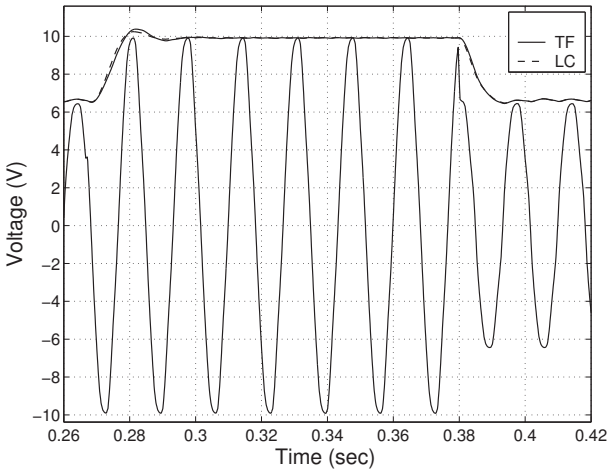

Figure 5.15: Filtered envelope by a second order filter

to track the envelope of the waveform. The algorithm is very robust as it is not sensitive to the input signal, sharp changes, and slow changes. In addition, the algorithm does not depend on the initial values and has no singularities.

The results demonstrate that the newly devised algorithm is capable of tracking the envelope of the voltage. Moreover, the algorithm does not show any spikes when the voltage level changes abruptly. However, there is a delay less than a cycle between the actual and the tracked envelope due to the utilization of shifting circuits. The tested shifting circuits confirm that the best results are achieved by using the transfer function networks or inductive-capacitive circuit.

To validate the proposed algorithm experimentally, a simple PQ generator is built in the laboratory and the envelope of the voltage signal is tracked by the proposed algorithm. The experimental results prove the ability of the proposed algorithm to track the envelope accurately.

Due to the robust and fast response of the proposed EO algorithm and its successful application for the ET, it can be used in the PLL and the SCE as well. Consequently, the PLL and the SCE processes can gain the same robustness as that of the EO. The upcoming chapter describes the implantation of the EO for the PLL circuit.

Chapter 6

Energy Operator Based PLL

The RCU is synchronized with the electric system through a PLL. The PLL algorithm should be as fast and robust as the measurement algorithm. Chapter 5 proposes a robust technique for the fast envelope tracking by using a novel algorithm to compute the EO. The PLL circuit can gain the same advantages if the the EO is utilized for the PLL. To accomplish this, another technique is developed.

6.1 Introduction

In electronics, a PLL is an electronic circuit that controls an oscillator to maintain a constant phase angle that is relative to a reference signal for synchronization purposes [88]. The desired PLL should possess generic properties, including rapid response that is robust and not affected by unbalanced conditions. In addition, the PLL should not be affected by system disturbances such as magnitude reduction (sag) or fluctuation (flicker). Moreover, the PLL must track the phase-jump efficiently and re-synchronize with the system as quickly as possible [89].

The simplest method to obtain the necessary phase information is to detect the zero crossing points of the utility voltages. However, since the zero crossing points can be detected only at each half-cycle of the utility frequency; *i.e.* 120 times per second for a 60

Hz power frequency, phase-jump tracking is impossible between the zero crossing points. As a result, fast tracking performance cannot be achieved. Another method is the technique of using the $dq0$ transform of the three-phase variables, but the operation of such techniques requires a balanced three-phase system which is not typical in distribution networks. The most common technique to implement a PLL is to use a Voltage Control Oscillator (VCO) with a PI circuit [88]. However, this method suffers from several drawbacks such as the long period of time to re-synchronize with the system [90], high demand of mathematical operations [91], and need for parameters tuning [92].

Previously, an enhanced PLL, based on estimating both the angle and the frequency has been reported in [93]. Although, the algorithm is accurate, it depends on estimation mathematics which are complex, and thus, costly.

Since the early work in power electronic control, Field Programmable Gate Array (FPGA) has attracted attention due to its flexibility, low cost, and concurrent operations [94]. Although, the FPGA has been used with DSPs or microcontrollers to form hybrid systems, it is adopted only in a minuscule parts of control circuits that do not require high mathematical burden such as Park's transform or the Pulse Width Modulation (PWM) in [95] and [96], respectively. Due to the complexity of the PLL algorithms, its implementation of FPGA is not affordable yet.

This chapter describes a new PLL algorithm that utilizes the EO introduced in chapter 5 and in [97]. The EO technique is fast, stable and accurate, so is the proposed PLL technique. The simple mathematical operations of the EO facilitate the development of a synthesizable PLL circuit to be implemented in an FPGA.

6.2 Conventional Phase Locked Loop

Figure 6.1 depicts the block diagram of a conventional PLL circuit. The Phase Detection multiplies its inputs to generate a signal which has a low-frequency component, proportional to the phase difference between the PD inputs, u_{vco} and u_{in}. The task of Low Pass

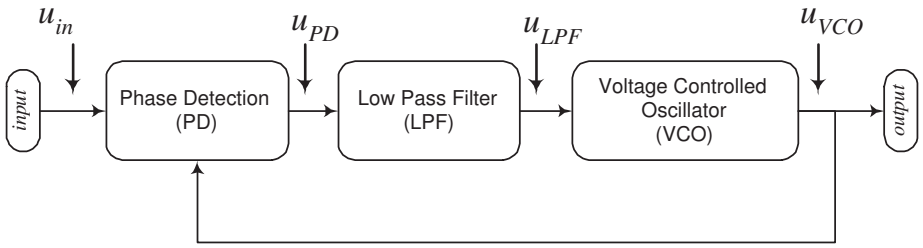

Figure 6.1: Conventional PLL Block Diagram

Filters (LPF) is to filter the high-frequency components and provide a proper error signal which controls the Voltage Controlled Oscillator (VCO). Any change in the phase angle (or frequency) of the input signal causes a deviation in the error signal from zero, which can be restrained by the control loop that introduces the proper variations to the frequency of the VCO.

If the change in the phase and/or frequency is small, the nonlinear function of the VCO is approximated by its linear term. In this case, it is possible to transform the PLL into a linear control system and perform the appropriate design and analysis. However, large and abrupt variations of phase and/or frequency of the input signal may not be properly tracked by a control loop. These kinds of variations can lock the PLL [88]. In addition, the parameters of the PLL circuit, especially the bandwidth, are sensitive to the application [98], [91]. Recently, PLL-parameters tuning is suggested in [92]. Its mathematical burden makes it hard to implement it on an FPGA. Moreover, this burden is increased when the tuning algorithm is included.

6.3 The Proposed PLL Algorithm

Since the early work in PQ, the ET algorithms have attracted the attention of researchers. In [99], the possibility of using the envelope of a sinusoidal waveform to detect the phase angle has been introduced. Recently, an accurate ET for a power signal has been developed and utilized to detect the angle [100]. Although the proposed algorithm is characterized

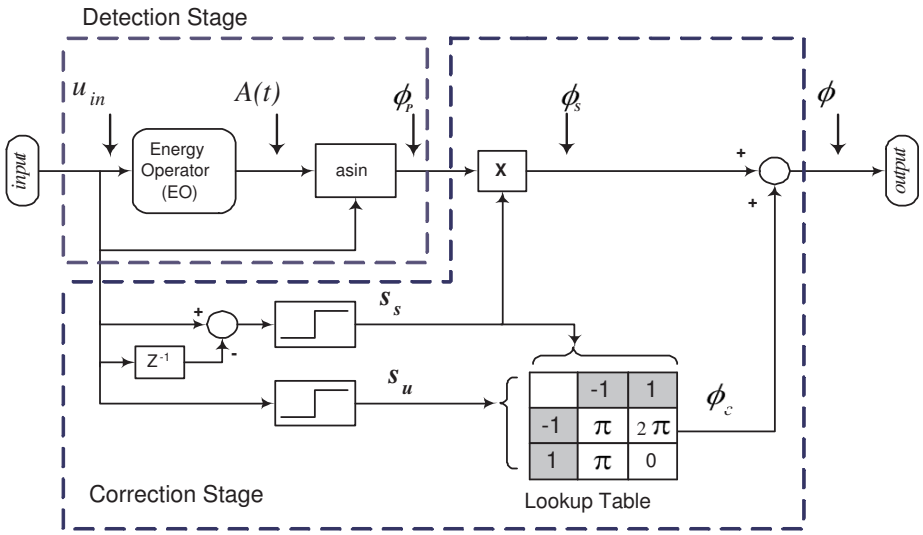

Figure 6.2: Proposed PLL block diagram for the FPGA application

by high accuracy, it is based on estimation techniques that are difficult to implement on an FPGA. The envelope tracking technique developed in this work and published in [97] encourages its use as a phase detector and consequently in PLL circuit. The newly PLL technique consists of two stages: the detection stage and the correction stage, as denoted in Fig. 6.2.

6.3.1 Detection Stage

In the detection stage, the angle of the sinusoidal wave is detected by the ET algorithm, where the input voltage signal is

$$u_{in} = A(t)sin(\phi) \tag{6.1}$$

The task of the envelope tracking is to detect the changes in the signal amplitude instantaneously, *i.e.* $A(t)$. Therefore, the amplitude of any sinusoidal signal is

$$A(t) = \sqrt{\frac{u_{in}^2 - u_{in}^- u_{in}^+}{sin^2(\phi)}} \tag{6.2}$$

where u_{in} is the input signal, u_{in}^{-} and u_{in}^{+} are the signals that lag and lead the actual signal by an angle equal to ϕ, respectively.

Once the amplitude is detected, the instantaneous value of the angle is given by

$$\phi_p = sin^{-1}(\frac{u_{in}}{A(t)}) \tag{6.3}$$

Figure 6.3 exhibits a sinusoidal waveform with the primary angle calculated according to (6.3). It is clear that the primary angle varies between $\frac{\pi}{2}$ and $\frac{-\pi}{2}$, but the expected output of the PLL is an angle that varies between 0 and 2π. Therefore, the primary angle needs to be corrected so that it varies between 0 and 2π, a task that is achieved in the correction stage.

6.3.2 Correction Stage

To correct the primary angle, ϕ_p, given by (6.3), it is mapped to another ϕ as follows:

$$\phi = \begin{cases} \phi_p & from\ 0\ to\ \frac{\pi}{2} \\ \pi - \phi_p & from\ \frac{\pi}{2}\ to\ \pi \\ \pi - \phi_p & from\ \pi\ to\ \frac{3\pi}{2} \\ 2\pi + \phi_p & from\ \frac{3\pi}{2}\ to\ 2\pi \end{cases} \tag{6.4}$$

According to (6.4), the angle tracking is divided into four quadrants. The signal sign, S_u, and the slope sign, Ss, are employed to determine the operating quadrant, where S_u and S_s have either +1 or -1 values. It is obvious that S_u is positive in the range of [0, π] and negative otherwise; S_s is negative in the range of [$\frac{\pi}{2}$, $\frac{3\pi}{2}$] and positive otherwise. The combination of S_u and S_s results in the four quadrants. To obtain S_s, the current sample is subtracted from the previous sample and then manipulated by a sign detector.

Another important note regarding (6.4) is that for the angle between $\frac{\pi}{2}$ and $\frac{3\pi}{2}$, the primary angle should be subtracted from π, if the slope of the signal is negative. Consequently, the primary angle, ϕ_p, needs to be multiplied by the slope sign to find a secondary

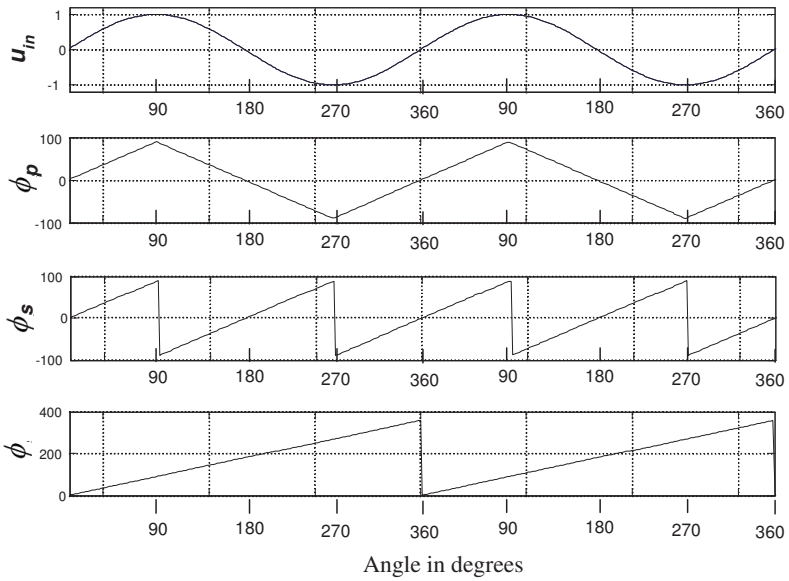

Figure 6.3: The tracked angle at different stages of the proposed technique

angle, ϕ_s, as follows:

$$\phi_s = S_s \phi_p \tag{6.5}$$

Finally, for ϕ_s to vary between 0 and 2π, a lookup table is constructed to add 0, π, or 2π according to S_u and S_s. This table is shown in Fig. 6.2 where the output of the lookup table is compensation angle ϕ_c. The actual angle is given by

$$\phi = \phi_s + \phi_c \tag{6.6}$$

6.4 Simulation Results

To examine the dynamic performance of the proposed algorithm, it is adopted to detect the angle of a power signal that suffers from different disturbances such as phase jump, sag and, flicker.

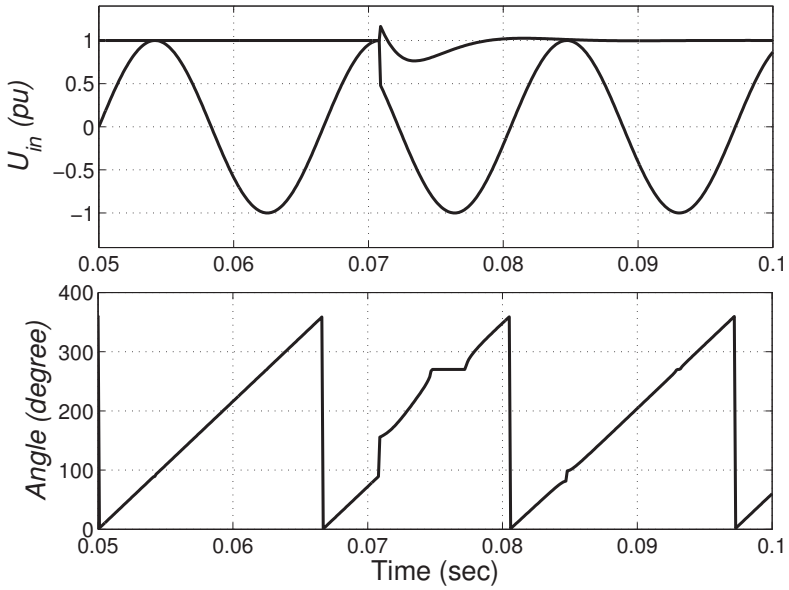

Figure 6.4: Response of the proposed algorithm to a phase shift 30^0 at the peak

6.4.1 Study Case 1: Phase Jump

A phase jump is defined as a sudden change in the angle of the voltage. A phase jump occurs for several reasons including a short-circuit fault which occurs frequently in the distribution systems and can not be predicted. Since the performance of power electronic equipment is affected dramatically by the phase jump, the PLL circuit must detect this phase jump quickly and re-synchronize itself with the system.

To test the capability of the proposed algorithm, a signal with a phase jump of 30^o is used. Also, the worst case, where the phase jump occurs at the peak point of the signal, is considered. The angle is tracked and the results are illustrated in Fig. 6.4. It is evident that the algorithm succeeds to re-synchronize with the system, and gives the true value in a quarter of a cycle.

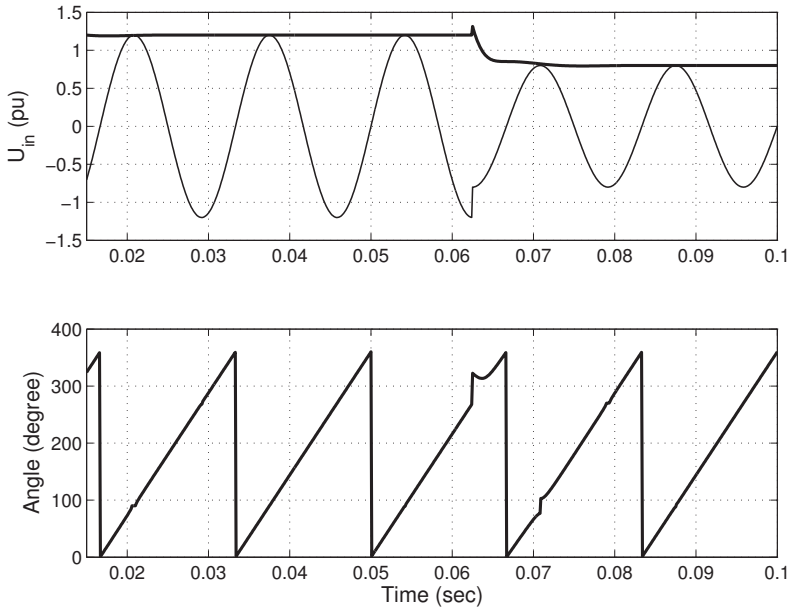

Figure 6.5: Response of the proposed algorithm to a voltage sag

6.4.2 Study Case 2: Voltage Sag

The second case study is to test the PLL when a sag occurs. The voltage sag is defined as a sudden change in the signal amplitude between 0.9 and 0.1 pu. The PLL should be able to detect the voltage sag and so that the circuit can re-synchronize with the system; otherwise, the equipment malfunction is expected. A signal of a voltage sag that occurs at the peak value, as signified in Fig. 6.5, is used in this case study. The result reflects the success of the proposed technique to extract the angle of the waveform within a quarter of a cycle.

6.4.3 Study Case 3: Voltage Flicker

Voltage flicker is defined as a slow change, caused by different non-linear loads such as arc furnace, in the *rms* value of the voltage signal. The voltage flicker is modeled as an amplitude modulation, where the modulating frequency is less than the fundamental frequency. A signal, modulated with a sinusoidal waveform with a frequency equal to $\frac{1}{10}$ of

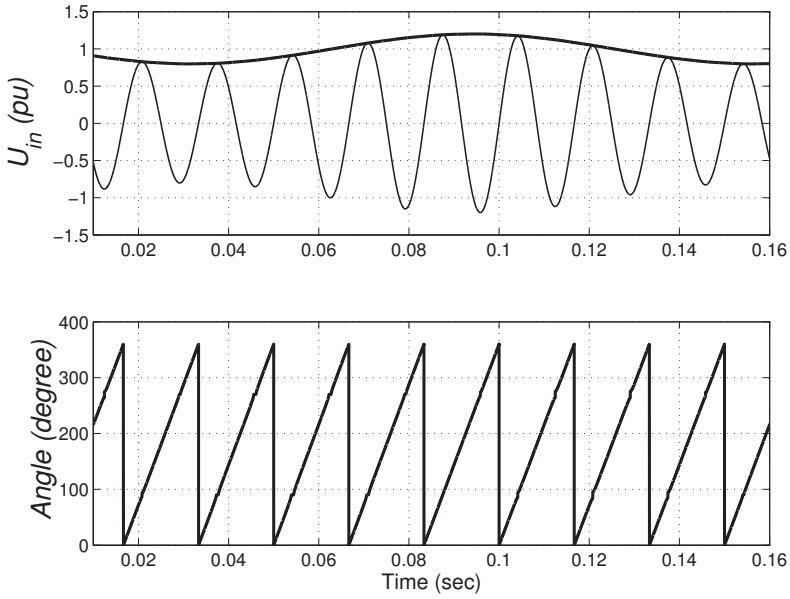

Figure 6.6: Response of the proposed algorithm to voltage flicker

the fundamental frequency, is selected to simulate the voltage flicker. Figure 6.6 indicates that the suggested PLL is not affected by the voltage flicker and can be synchronized with the system.

6.5 FPGA Design

In this section, an 8-bit FPGA is designed to implement the PLL circuit in Fig. 6.2. Although there are many designs to implement this circuit, the design should make use of the concurrency advantage of the FPGA with a minimum area. In the proposed design, there are three concurrent processes:

1. the EO process
2. an algorithm for the *arcsin* process
3. the correction process

The output of each process is fed to the next process, and the three processes are executed concurrently.

6.5.1 Energy Operator Process

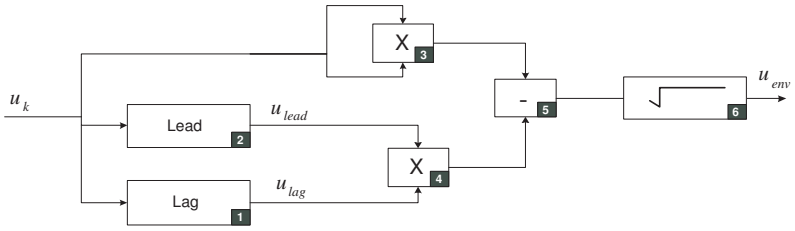

Figure 6.7: The EO process block diagram as implemented on the FPGA

The EO process, consisting of six blocks, is displayed in Fig. 6.7. The first and second blocks are needed to extract the lead and the lag signal, v^+ and v^-, respectively. The third and the fourth blocks are the multiplier circuits to calculate v^2 and v^+v^-. The fifth block is a subtractor to compute the EO. Finally, in the sixth block, the square root of the EO for the signal amplitude is calculated, as $A(t)$. Since the designs of the third to sixth blocks are very simple and found in many digital design texts [101], only the designs of the first and second blocks are described.

The first and second blocks are the lead and lag circuits which have the Transfer Function (TF) of

$$TF = \frac{as+1}{bs+1} \tag{6.7}$$

The TF can be a lead or a lag network according to the ratio of a/b. The application of Euler's backward method of integration yields

$$\begin{aligned} v_k^+ &= d_1 v_k + d_2 v_{k-1} + d_3 v_{k-1}^+ \\ v_k^- &= g_1 v_k + g_2 v_{k-1} + g_3 v_{k-1}^- \end{aligned} \tag{6.8}$$

Appendix C provides more details about these parameters. A sample rate of 8000

Samples Per Second (sps) is found to be adequate in the power applications. By using a sample rate of 8000 sps; *i.e.* $T_s = 125\mu s$, the values of (6.8) are found and shown in Table 6.1.

Table 6.1: Lead Network and the Lag Network Parameters

	1	2	3
d	0.412	-0.366	0.985
g	2.43	-2.40	0.891

Since the FPGA is built with integer numbers, the values in Table 6.1 are interpreted as zeros for the first row, and integers for the second row. Consequently, the lead and lag networks lose their accuracy. The easiest solution is to use floating point numbers in this process. However, this increases the area and the power consumption of the FPGA. To overcome these drawbacks without dealing with the floating point numbers, (6.8) is modified as follows:

$$\begin{aligned} v_k^+ &= [a_{d1}\ v_k + a_{d2}\ v_{k-1} + a_{d3}\ v_{k-1}^+] \ /\ b_d \\ v_k^- &= [a_{g1}\ v_k + a_{g2}\ v_{k-1} + a_{g3}\ v_{k-1}^-] \ /\ b_g \end{aligned} \tag{6.9}$$

This process converts all the values to integer numbers. A comparison of (6.9) and (6.8) reveals that $a_{d1}/b_d = d_1$, and so on, for all the parameters. Since the division by two operation is translated into a shifter, the superior choice of b_d and b_g should be a multiplier of two. Other values of b_d and b_g are acceptable too, but require a divider algorithm which occupies a large area of the FPGA and slows it down. The block diagram in Fig. (6.8) summarizes the process for the lead network. A similar block diagram for the lag network can be detected.

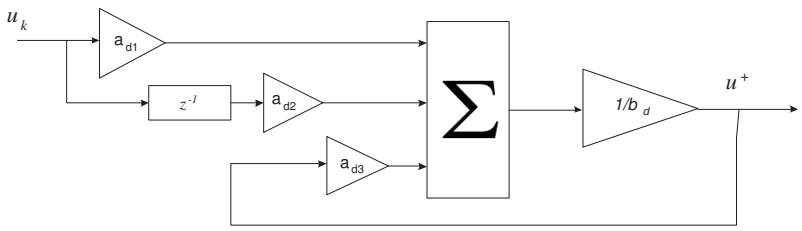

Figure 6.8: The lead network realization on an FPGA

6.5.2 *arcsin* Algorithm Process

The simplest method to compute the *arcsin* function is the use of Taylor's expansion, resulting in:

$$arcsin(x) = \sum \frac{(2n!)x^{2n+1}}{(2^n n!)^2(2n+1)} \qquad n = 0, 1, 2, 3... \tag{6.10}$$

The first three terms of (6.10) are

$$arcsin(x) = x + \frac{1}{6}x^3 + \frac{3}{40}x^5 \tag{6.11}$$

6.5.3 Correction Process

The correction unit receives two inputs: the voltage signal, u_{in} and the primary angle, ϕ_p. Since the EO and *arcsin* process require a clock cycles to perform their tasks, the primary angle is delayed beyond that of the actual voltage signal. Therefore, the voltage signal should be delayed by the number of clock cycles equal to the maximum number of clock cycles of either of the two previous processes. Since the FPGA operates at a very high clock frequency, a few nanoseconds, the delay can be neglected, compared to the sampling rate which is a few tens of micro seconds.

The VHDL code for the circuit is written and compiled by Xilinx tools. The code is synthesized and implemented on SPARTAN-2E from Xilinx. The floor plan of the FPGA in Fig. 6.9 demonstrates that the PLL circuit requires only a small area of the total area

of the FPGA, allowing more control algorithms on the chip.

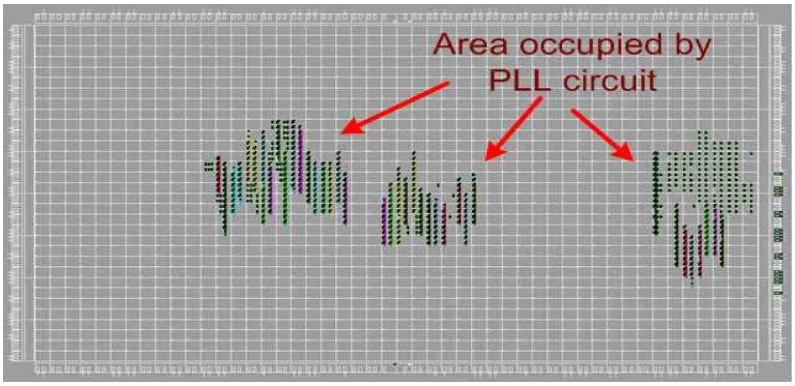

Figure 6.9: Area occupied by the PLL in the FPGA

6.6 FPGA Test Benchmark

The laboratory setup in Fig. 6.10 is used to test the dynamic performance of the proposed PLL circuit experimentally. The setup consists of a Power Signal Generator (PSG) that can generate power signals with different disturbances. The PSG is able to superimpose a voltage sag or a voltage flicker on the power signal. The signal, generated by the PSG, is digitalized by using the Data AcQuisition (DAQ) that feeds the captured data to the Real-Time Workshop. After the output of the FPGA is captured, the output is displayed again through the MatLab\Real-Time Workshop. Three different signals are tested: a pure power signal, a sag signal, and a flicker signal.

A pure power signal is generated by the PSG at a frequency of 60 Hz. Figure 6.11 proves that the FPGA can track the envelope successfully and extract the angle accurately. The idea behind this test is to evaluate the errors in the PLL output. Although the actual angle is not available, the actual voltage waveform is accessible. Therefore, to assess the accuracy of the PLL, the power signal is constructed again by using the angle from the PLL. Then, the actual signal is compared with the constructed signal consequently, the errors between

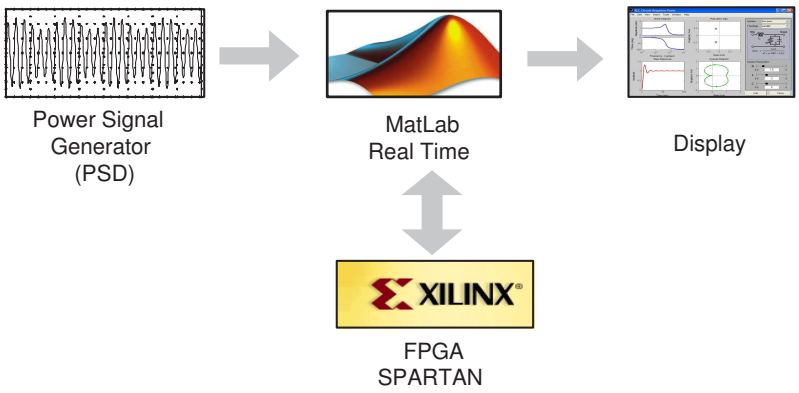

Figure 6.10: System used to test the FPGA

them are due to the PLL-error. The errors of the actual and of the constructed signal are shown in Fig. 6.11-c, where the maximum error deviation is approximately 2.5%.

The second case is a signal suffers from a voltage sag that occurs at the peak point of the signal. The envelope reaches the steady state in less than a quarter of a cycle, and the PLL is re-synchronized with the system as depicted in Fig. 6.12.

Finally, a voltage signal with a voltage flicker is employed. Again, it is confirmed that the circuit provides effective tracking for both the angle and the envelope, as reflected in Fig. 6.13.

6.7 Summary

This chapter introduces a new technique for the PLL circuit. The accuracy and simplicity of the proposed technique is gained from the EO technique. As a result, the technique can track the angle rapidly and with less computation effort.

The digital application of the proposed circuit, by using an 8-bits FPGA confirms its capability to be re-synchronized with the system under different conditions, including sag, swell, and flicker. Although the new circuit performs a fast synchronization with the system for voltage flicker, it needs a quarter of cycle to synchronize in the case of a voltage sag.

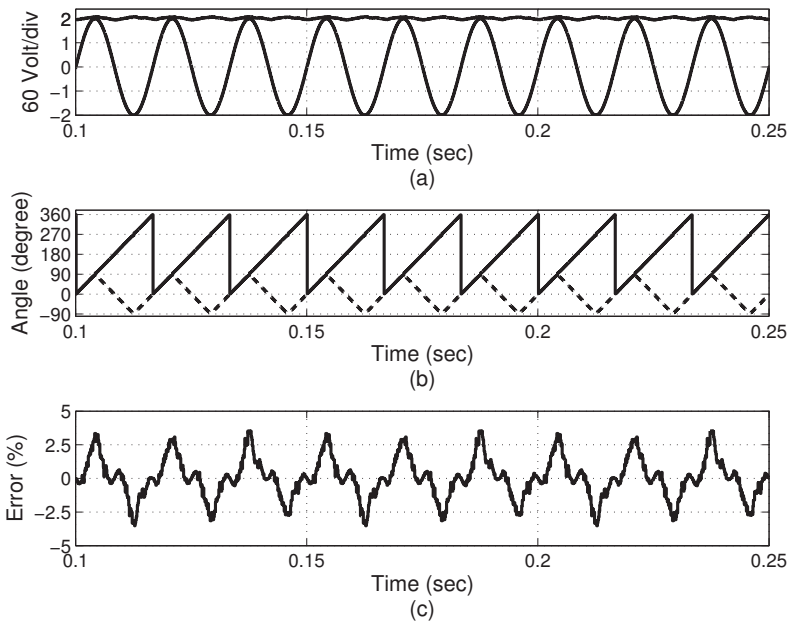

Figure 6.11: FPGA-PLL response of a pure sinusoidal waveform: a) the waveform envelope, b) the angle, and c) the error

The envelope tracking and the PLL are designed by using ET with great success. In the next chapter, the new EO and the PLL circuit, introduced in Chapters 5 and 6 respectively, is utilized for the symmetrical component extraction to gain the same advantages.

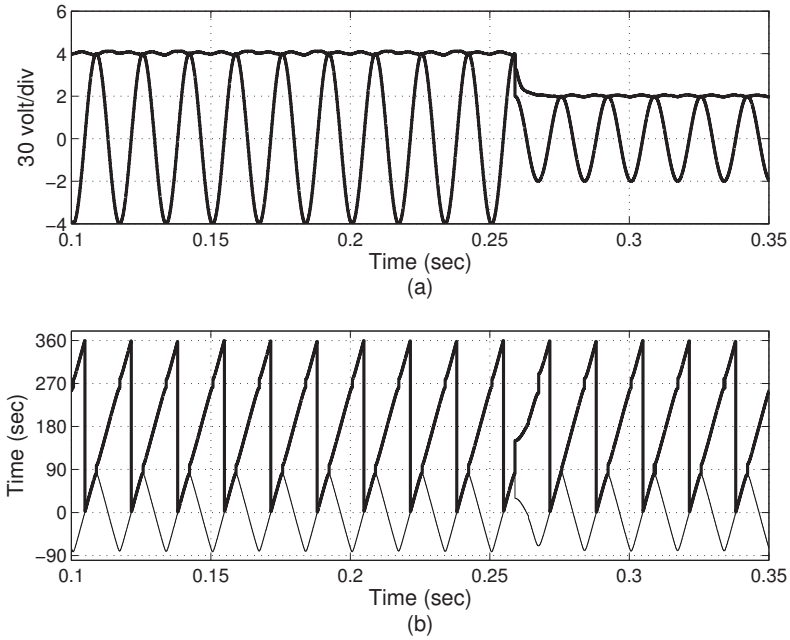

Figure 6.12: FPGA-PLL response of a sinusoidal waveform with sag: a) the waveform envelope and b) the angle

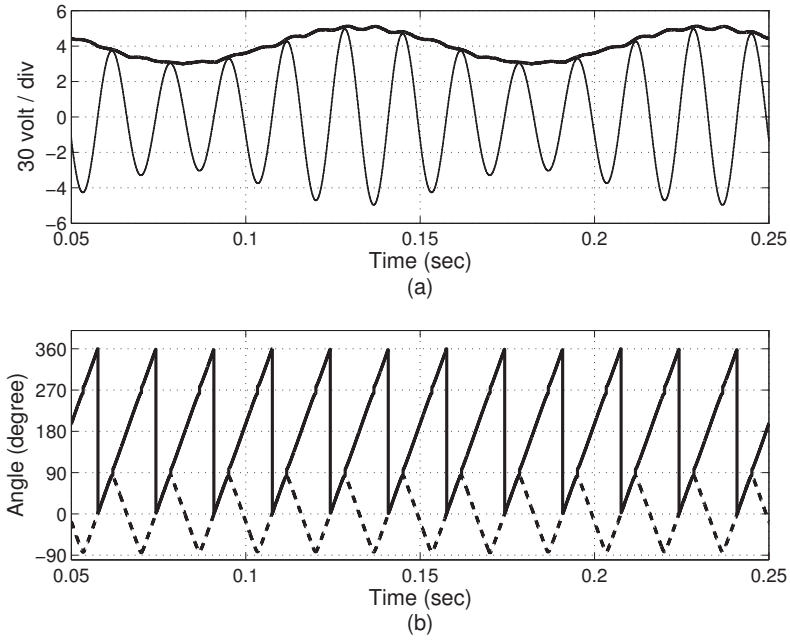

Figure 6.13: FPGA-PLL response of a sinusoidal waveform with flicker: a) the waveform and envelope b) the angle

Chapter 7

Symmetrical Component Extraction

Unbalanced voltage is a prevalent problem in distribution systems, affecting the operation of the rectifier, as well as the ASD. Therefore, it is essential to add the unbalance mitigation function to the power conditioning function of the rectifier.

7.1 Introduction

The idea behind the unbalance compensation is the extraction of the symmetrical component in the voltage at the PCC; therefore, a fast instantaneous algorithm for the on-line tracking of the required symmetrical component is needed [102], [103]. In an effort to achieve the on-line tracking, a number of digital signal processing algorithms are suggested. Fast Fourier Transform (FFT) and Walsh-Hadamard Transform (WHT) have been applied in [104] and [105] respectively. Since the FFT and WHT are using a window of samples, there is a delay between the actual and the tracked components equal to the window length. This delay limits its on-line application [100].

Recently, various estimation algorithms have been developed to estimate the symmetrical component. Recursive estimation methods, such as the Kalman Filter and Stat-Observer, are adopted to estimate the symmetrical components [106], [107]. Despite the superior advantages of the recursive estimation methods, they require powerful processing

units for the mathmatical complexity. Therefore, on-line usage is very limited [108]. A non-recursive method, requiring less computation, based on extending Newton-Type Algorithm (NTA), is introduced in [109]. Even though, the NTA needs fewer mathematical operations, it does not result in a fast convergence [110].

Consequently, in this chapter, a new technique to compute the symmetrical components utilizing the EO is proposed. As a result, the technique has the same benefits as the EO. Moreover, the proposed technique does not acquire any iteration. Another leading characteristic of the novel technique is the ease of digital implementation in the DSP, the micro controller or the FPGA.

This chapter introduces a novel control technique for unbalance mitigation. Due to the similarity between the DSTATCOM and rectifier circuit topology, the novel control technique is applied to the rectifier in this chapter before applying it to the rectifier in the next chapter. The newly devised control technique uses a fast instantaneous measurement of the symmetrical components.

7.2 Voltage Source Converter Equivalent Circuit

The VSC, in Fig. 9.2-a, is composed of a DC link capacitor, C_{DC}, connected at the DC-bus. The VSC is connected to the grid through a transformer which will act as a filter as well [111], [112]. By applying the GAM technique, the equivalent circuit is obtained, as shown in Fig. 9.2-b [103]. The voltage at the rectifier side after the filter, E_c, is a three-phase voltage which is controlled by the PWM signals [113].

Since the resistance of the filter, or the transformer, is very small compared to the inductance, the resistance is commonly neglected. Therefore, the angle difference between V_{pcc} and E_c is used to control the active power flow, whereas the reactive power flow is controlled by the magnitude of E_c [103].

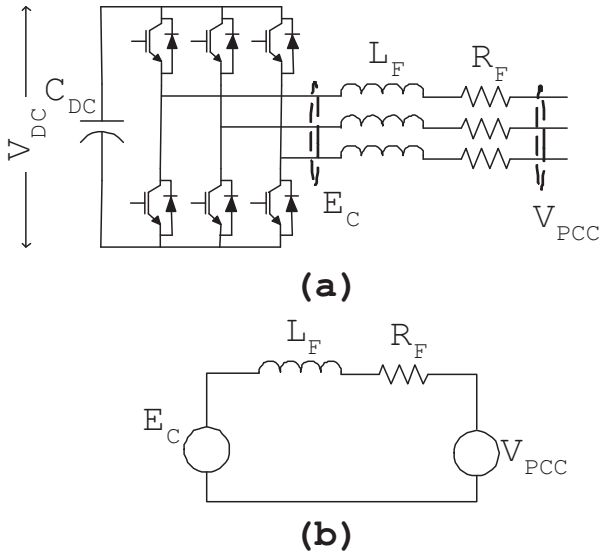

Figure 7.1: Voltage Source Rectifier (VSR): a) schematic diagram, b) equivalent circuit

7.3 Voltage Control Rectifier

The conventional control of the PWM Voltage Control Rectifier (VCR), depicted in Fig. 7.2-a, is explained briefly in Chapter 2 and this chapter will provide the details of the control. The VCR has two control signals, the first signal is the PWM modulation index, m, which controls the magnitude of the rectifier voltage and the second signal is the modulation angle of the PWM, ϕ, which controls the angle of the rectifier voltage [114].

By varying the modulation angle and index, the amount of power absorbed by the rectifier can be varied. Specifically, the active and reactive power are controlled by the modulation angle and index, respectively. This leads to two control loops.

The first control loop is employed to maintain a constant voltage at the DC-bus by drawing adequate active power from the grid. The PI or SMC controller, in Fig. 7.2-b, can be used for this purpose. The second control loop, shown in Fig. 7.2-c, is the voltage regulator that monitors the voltage at the PCC, and then manages the amount of the reactive power by controlling the modulation index. Any other controller can be used for this purpose.

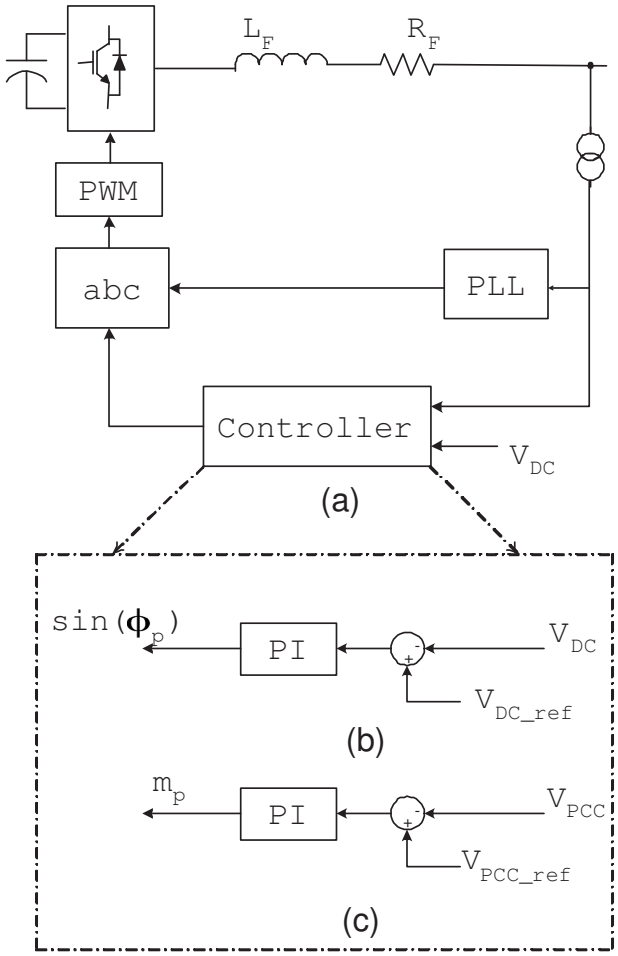

Figure 7.2: Control of the VCR under balanced conditions; a) block diagram, b) V_{DC} regulator, c) V_{PCC} regulator

The uncorrelation of the two control loops has been proven in different papers [112], [113], [115]. Therefore, the DC-bus voltage is usually seen by the V_{pcc}-regulator loop as a constant value. The modulation index and angle are then fed to a transformation circuit that converts them to the equivalent three phases signals, *abc*, which are used as a reference signal for the PWM.

Figure 7.2 indicates that the control system requires the measurements of the voltage at the PCC. Under balanced conditions, the three-phase voltages are identical, therefore, measuring one phase maps the other two phases. However, for the unbalanced three phase

voltages at the PCC, due to an unbalanced load or unbalanced supply, the measurements are quite complicated [104], [106]. Consequently, the voltage sensing should be modified.

7.4 Proposed Method for Unbalance Mitigation

The common technique for unbalanced voltage analysis is to analyze it into three sequences, namely positive, negative, and zero, which are known as symmetrical components [116]. A balanced three phase system has only a positive component, and no negative or zero sequence components.

Accordingly, the proposed technique has three functions. The first function is to regulate the voltage at the PCC, whereas the second and the third are to mitigate the voltage negative and zero sequence at the PCC, respectively. Consequently, three control loops are required. In addition, a fourth control loop is required to maintain the DC-bus voltage level. Typically, due to the existence of the second and third functions, the rectifier voltage, E_c is no longer balanced, but has positive, negative and zero components.

The newly developed technique, represented in Fig. 2.9, is composed of the following three blocks:

1.) *Symmetrical Components Extraction (SCE) Unit* ; which takes care of measuring the symmetrical components and feeds them to the control unit,

2.) *Controller Unit*; which defines the reference signals in the *pnz* sequence, and

3.) *Pattern Signal Generation (PSG) Unit*; which converts the control signals from the controller *abc*-pattern signals used by the PWM switching.

The following sections detail the three blocks of the proposed control.

7.5 Symmetrical Components Extraction Unit

The application of the symmetrical component concept is introduced as a decomposition of complex steady-state phasors in [116], where the unbalanced three phasors could be decomposed into another three balanced phasors, called the positive, negative, and zero components. Assume that the three phases voltages are given as

$$\begin{aligned} u_a &= U_a \ sin(\omega t + \phi_a) \\ u_b &= U_b \ sin(\omega t + \phi_b) \\ u_c &= U_c \ sin(\omega t + \phi_c) \end{aligned} \tag{7.1}$$

which can be written in phasor form as

$$\begin{aligned} \widehat{U}_a &= U_a \ \angle\phi_a \\ \widehat{U}_b &= U_b \ \angle\phi_b \\ \widehat{U}_c &= U_c \ \angle\phi_c \end{aligned} \tag{7.2}$$

The positive U_p, the negative U_n, and zero U_z, components are expressed in phasor form as

$$\begin{pmatrix} \widehat{U}_p \\ \widehat{U}_n \\ \widehat{U}_z \end{pmatrix} = \frac{1}{3} \begin{pmatrix} 1 & a & a^2 \\ 1 & a^2 & a \\ 1 & 1 & 1 \end{pmatrix} \begin{pmatrix} \widehat{U}_a \\ \widehat{U}_b \\ \widehat{U}_c \end{pmatrix} \tag{7.3}$$

where: $a = 1\angle 120$

By substitute (7.2) in (7.3) gives (7.4) which could be written in the time frame as in (7.5).

$$\begin{pmatrix} \widehat{U}_p \\ \widehat{U}_n \\ \widehat{U}_z \end{pmatrix} = \frac{1}{3} \begin{pmatrix} U_a \ \angle\underline{\phi_a + 0} + U_b \ \angle\underline{\phi_b + 120} + U_c \ \angle\underline{\phi_c + 240} \\ U_a \ \angle\underline{\phi_a - 0} + U_b \ \angle\underline{\phi_b - 120} + U_c \ \angle\underline{\phi_c - 240} \\ U_a \ \angle\phi_a + U_b \ \angle\phi_b + U_c \ \angle\phi_c \end{pmatrix} \tag{7.4}$$

$$\begin{pmatrix} u_p \\ u_n \\ u_z \end{pmatrix} = \frac{1}{3} \begin{pmatrix} U_a\ sin(\omega t + \phi_a + 0) + U_b\ sin(\omega t + \phi_b + 120) + U_c\ sin(\omega t + \phi_c + 240) \\ U_a\ sin(\omega t + \phi_a + 0) + U_b\ sin(\omega t + \phi_b - 120) + U_c\ sin(\omega t + \phi_c - 240) \\ U_a\ sin(\omega t + \phi_a) + U_b\ sin(\omega t + \phi_b) + U_c\ sin(\omega t + \phi_c) \end{pmatrix} \tag{7.5}$$

7.5.1 The Proposed Algorithm for Symmetrical Component Extraction

Equation (7.5) demonstrates that the positive component is the sum of three signals. The first signal is the phase voltage, u_a, without any shifting. The second signal is the phase voltage, u_b, but is shifted by an angle of 120^o which corresponds to the multiplication by the operator a. The third signal is the phase voltage, u_c, but is shifted by an angle of 240^o which corresponds to the multiplication by a^2. Since the signals, amplitudes, and angles vary with time, there should be a method to track those changes accurately. Therefore, the EO is adopted to track the changes in the amplitudes and the angles.

It has been shown in [81] that the energy of a sinusoidal signal is proportional to the square of the amplitude and the square of the frequency. As a result, the changes in the signal amplitude could be tracked by calculating the EO of the signal. To do this, Kaiser has proposed an algorithm using only two multiplications and one subtraction [83]. Despite its simplicity, its application shows that the algorithm results in severe spikes which limits its practical application [84]. An enhanced algorithm that overcomes the drawbacks of Kaiser's algorithm, has been proposed in [117], giving the amplitude as follows:

$$U_x(t) = \sqrt{u_x^2 - u_x^+ u_x^-}/sin(\theta) \tag{7.6}$$

where U_x is the amplitude of phase x, u_x is the actual signal, u_x^+ is a lead signal, u_x^- is a lag signal, θ is the lead /lag angle, and x is a subscript indicating the phase (a, b, c). The complete

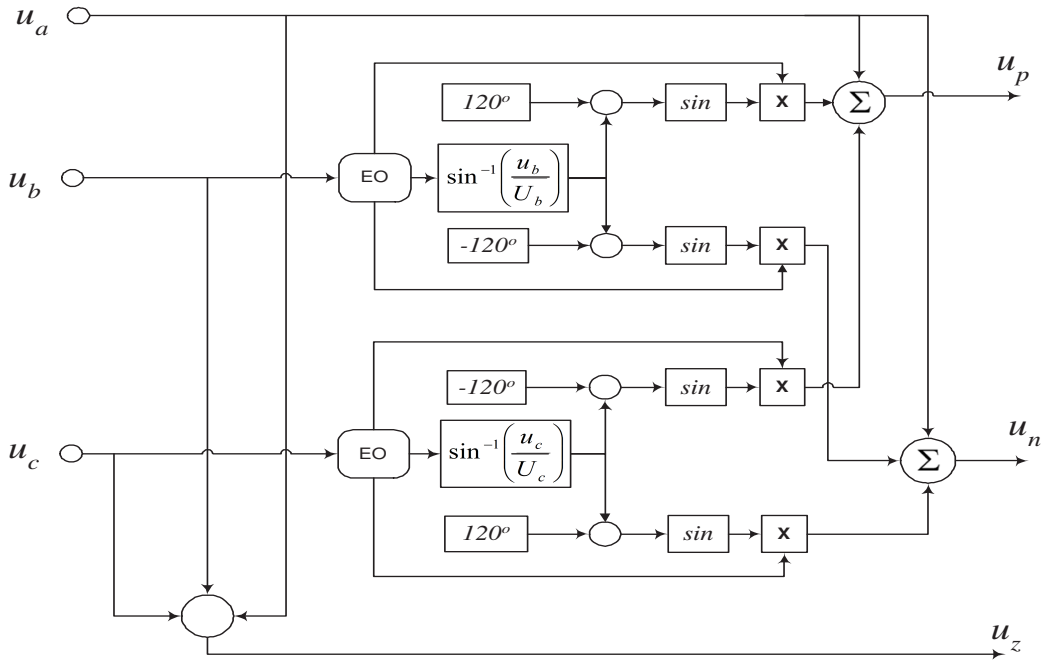

Figure 7.3: Block diagram of the proposed SEC algorithm

digital form of the EO is given in Appendix C.

If the amplitude of the signal is known, then the angle of the phase x, as a function of time, is given as:

$$\omega t + \phi_x = sin^{-1}\left(\frac{u_x}{U_x}\right) \tag{7.7}$$

The novel algorithm is applied twice to extract the magnitude and the angle of phases (*b and c*). By plugging the obtained values from (7.6) and (7.7) into (7.5), the positive, negative and zero components locked to phase a are attained. Figure 7.3 is a block diagram of the proposed algorithm to realize the symmetrical components.

Equations (7.5), (7.6) and (7.7) indicate that the novel algorithm does not need to iterate to compute the symmetrical components.

7.5.2 Applications

The simulation results that are presented in this section are simulated using the Fixed Point Toolbox from Matlab. The Fixed Point is used to simulate the real software application, such as DSP, or hardware application, such as the FPGA. In the all simulation cases, the sampling frequency is 8 KHz, and the nominal power frequency is set at 60 Hz for the three different applications hereafter.

1. Application I.

The first application is three phase voltages given as

$$\begin{aligned} u_a &= 1.0\ sin(\omega t + 0) \ = 1.0\ \angle 0 \\ u_b &= 1.2\ sin(\omega t - 150) \ = 1.2\ \angle -150 \\ u_c &= 0.8\ sin(\omega t + 90) \ = 0.8\ \angle 90 \end{aligned} \tag{7.8}$$

Equation (7.8) demonstrates that the three phases voltages are not balanced, according to (7.4) and (7.5), the positive and the negative components are

$$\begin{aligned} u_p &= 0.97\ sin(\omega t - 20.1) \ = 0.97\ \angle -20.1 \\ u_n &= 0.28\ sin(\omega t + 69.0) \ = 0.28\ \angle 69.0 \end{aligned} \tag{7.9}$$

The three-phase voltages, the positive and the negative components are illustrated in Fig. 7.4. It is evident that the positive and negative signals in the figure confirm those obtained from (7.8). The zero-sequence component has been omitted from the figure since its calculation is straight forward and can not be mistaken. In addition, the proposed technique does not affect the zero component calculation.

2. Application II.

Due to the continuous switching of loads, the actual electrical voltage usually suffers from continuous changes in its amplitude that cause voltage fluctuation. Since these changes in the voltage are slow (between 1 Hz and 20 Hz), they cause the light flicker, as well as equipment malfunction. Therefore, it is essential to validate the ability of the

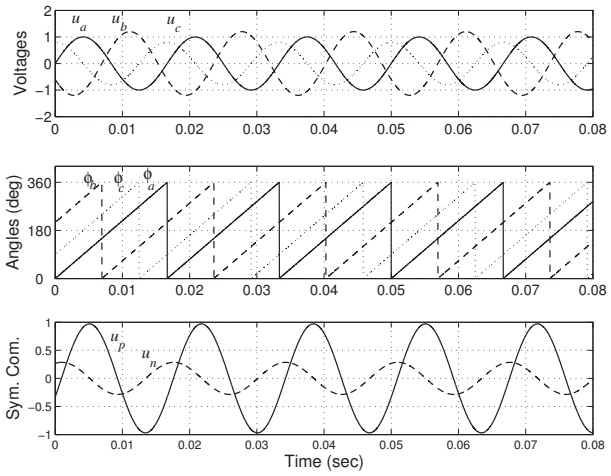

Figure 7.4: Symmetrical components of application I

proposed algorithm to track the symmetrical components with voltage fluctuations.

Typically, the voltage flicker is modeled as an amplitude modulation, where the fundamental frequency is the carrier and the flicker signal is the modulating signal. As a result, three voltage signals modulated by frequencies of 12, 10 and 16 Hz will be used to test the algorithm. Moreover, the three phases and the modulating signals are unbalanced. The three signals are given as

$$\begin{aligned} u_a &= [1 + 0.6\ sin(12\pi t + 0)]\ sin(\omega t + 0) \\ u_b &= [1 + 0.2\ sin(10\pi t + 60)]\ sin(\omega t - 150) \\ u_c &= [1 + 0.4\ sin(16\pi t - 30)]\ sin(\omega t + 90) \end{aligned} \tag{7.10}$$

Figure 7.5 shows both the three phases signals and the symmetrical components, where the proposed algorithm successfully to determines the positive and the negative components, even for voltage flicker.

3. Application III.

The third application is dedicated to the test of the dynamic performance of the algorithm. A voltage sag and a phase jump is used to examine the dynamical performance of the algorithm. Also, it is assumed that the sag and the phase jump occur at the peak of

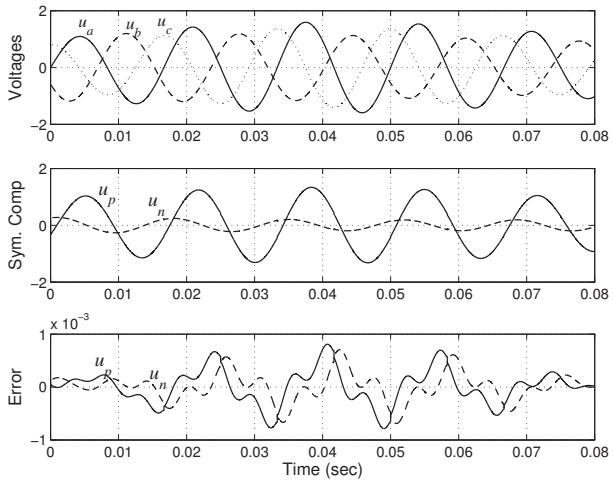

Figure 7.5: Symmetrical components of application II

the signal which of the most severe case.

The three phase voltages are considered to be balanced, until a disturbance occurs in the system at 0.05 second. The disturbance causes a voltage sag with different depthes for the three phases as well as for phase jumps in the three voltages, as plotted in Fig. 7.6. Before the disturbance, the system was balanced and ,therefore, the negative component vanishes. At 0.05 second, the sag and the phase jump are initiated and the proposed algorithm succeeds to determine the symmetrical components in less than half of a cycle.

7.6 Controller

The control unit receives the symmetrical components from the measurement unit and processes them to determine the symmetrical components, E_c^{pnz}. To achieve accurate E_c^{pnz}, the magnitude and the angle of each component, pnz, have to be determined. In fact, the modulation index of the PWM is proportional to the E_c^{pnz}, and the outputs of the control are m_{pnz} and ϕ_{pnz}.

The controller is responsible for three tasks, which are the compensation of the voltage for the positive, negative and the zero sequences. Not only are three control loops are

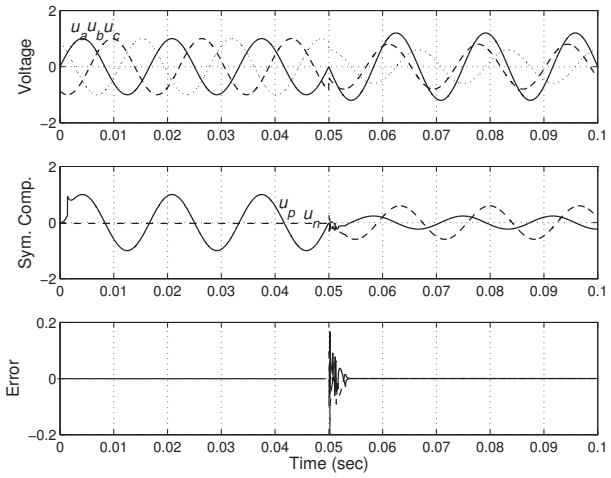

Figure 7.6: Symmetrical components of application III

needed for the three functions, but also a fourth control loop is required to maintain the DC-bus voltage at a constant level. The four control loops are shown in Fig. 7.7, and are discussed hereafter. It is proposed in this work to use the Sliding Mode Controller (SMC), which is explained in detail in Chapter 8.

7.6.0.1 DC-Bus Voltage Control Loop

To maintain a constant voltage at the DC-bus, an active power to counteract the power drawn by the inverter and the motor is necessary. The positive sequence angle is used to control the active power and, hence, maintain the DC-bus voltage as denoted in Fig. 7.7-a.

7.6.0.2 PCC-Voltage Regulation Control Loop

This control loop uses the balanced positive sequence components to measure the voltage at the PCC which is compared with a reference value to compute the error signal. The error signal is then handled by a controller, such as the SMC or PI in Fig. 7.7-b, to produce the magnitude of the positive sequence which controls the positive reactive power flow.

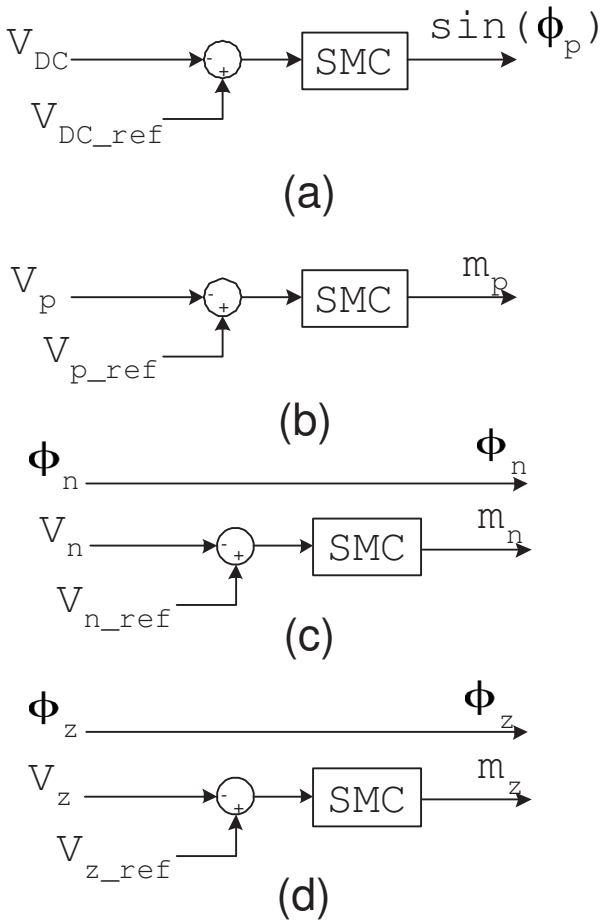

Figure 7.7: Proposed control unit: a) V_{DC}-regulator, b) V_{PCC}-positive component regulator, c) V_{PCC}-negative component regulator, d)V_{PCC}-zero component regulator

7.6.0.3 Negative Sequence Control Loop

The reason for using the rectifier to mitigate the unbalance is to use the reactive power for compensation. Therefore, the active power supplied in the negative sequence has to be zero. Shall the angle difference between the voltages; in the negative sequence, at the PCC and the VSR be zero, the active power will vanish in the negative sequence. Therefore, the E_C^n voltage angle will equal to the angle of the negative-sequence at the PCC as depicts in Fig. 7.7-c.

The reactive power is employed to compensate for the negative component at the PCC. Therefore, it is necessary to determine the adequate amount of reactive power in the negative sequence to cancel the negative component of the voltage at the PCC, *i.e.*, $V_{PCC}^n = 0$. Yet, the reactive power flow is controlled by the magnitude, and modulation index (m_n) of the negative component of E_C. The negative component of the voltage at PCC, V_{PCC}^n, is compared with the reference value, it should be zero, for controlling the negative modulation index of the PWM, as illustrated in Fig. 7.7-c.

7.6.0.4 Zero Sequence Control Loop

For the zero-sequence, the same control concept used in the negative sequence control loop is applied, as indicated in Fig. 7.7-d.

7.6.1 pnz to abc Transformation Unit

Since the PWM reference signals are required to be in the *abc* frame, and the output of the control unit consists of the symmetrical components, *pnz*, the output of the control unit is converted to the *abc* frame. This is achieved by inverting (7.3), producing the three following signals:

$$\begin{aligned} e_a &= E_p sin(\omega t + \phi_p) + E_n sin(\omega t + \phi_p) + E_z sin(\omega t + \phi_z) \\ e_b &= E_p sin(\omega t + \phi_p + \tfrac{2\pi}{3}) + E_n sin(\omega t + \phi_p + \tfrac{4\pi}{3}) + E_z sin(\omega t + \phi_z) \\ e_c &= E_p sin(\omega t + \phi_p + \tfrac{4\pi}{3}) + E_n sin(\omega t + \phi_p + \tfrac{2\pi}{3}) + E_z sin(\omega t + \phi_z) \end{aligned} \tag{7.11}$$

where, (ωt) is obtained from a PLL.

7.7 Rating of The Rectifier to Compensate for Unbalance

When the rectifier is operating under balanced conditions, the power rating is divided by three since the power is shared equally among the three phases and the ratings of the IGBTs and the transformer are determined based on this fact. Since, under unbalance condition, the currents in the three phases are not equal, the power is not equally shared.

Assume that the maximum expected voltage source unbalance in pnz is given as $V^{pnz}_{S,max}$, the maximum expected unbalanced load current is $I^{pnz}_{L,max}$ and the maximum unbalance allowed at the PCC is $V^{pnz}_{pcc,max}$. By neglecting the supply resistance,

$$V^{pnz}_{pcc} = V^{pnz}_{S,max} - jx_s[I^{pnz}_{L,max} - jI^{pnz}_{C,max}] \tag{7.12}$$

Consider the worst case scenario when the load is purely inductive, then

$$V^{pnz}_{pcc} = V^{pnz}_{S,max} - x_s[I^{pnz}_{C,max} - I^{pnz}_{L,max}] \tag{7.13}$$

and the compensation current is given by

$$I^{pnz}_{C,max} = -(I^{pnz}_{L,max} + [V^{pnz}_{pcc} - V^{pnz}_{S,max}]/x_s) \tag{7.14}$$

The voltage supplied by the rectifier is given as;

$$E^{pnz}_{C,max} = V^{pnz}_{pcc} \mp x_f I^{pnz}_{C,max} \tag{7.15}$$

Finally, the reactive power supplied by the rectifier in pnz will be given by;

$$Q^{pnz}_{C,max} = [(I^{pnz}_{C,max})^t]' E^{pnz}_{C,max} \tag{7.16}$$

Equation (7.16) presents the power rating of the rectifier as pnz components.

Another important parameter is the current rating of the power switches and the filter. The current rating is the maximum current expected in any phase which is given by converting $I^{pnz}_{C,max}$ to the abc sequence as

$$I^{abc}_{C,max} = aI^{pnz}_{C,max} \tag{7.17}$$

To demonstrate the effect of the unbalance on the rectifier rating, consider the system under study. Here, the maximum expected negative component of the load varies between zero and 1 pu, while the total load rating is kept constant. The maximum compensation current is computed by (7.14). For (7.14), the maximum unbalance allowed at the PCC, $V^{pnz}_{pcc,max}$, is needed to be known in advance. Ideally, the negative component at the PCC should be zero. However, in some systems, a smaller number of negative components can be allowed. So, three cases are studied, where the $V^{n}_{pcc,max}$ is 0%, 5% and 10%.

Figure 7.8 signifies the maximum expected difference in the current between phase a and b. It is obvious that the current difference between any two phases can be double than that of the actual rating. Consequently, in the design procedure, the maximum expected current is considered for re-rating both the IGBTs and transformer.

It is concluded that the power switches and the filter rating are higher in the case of the unbalance compensation. In addition, the rating increases with the increase of the negative and the zero components imposed by the load current or the source voltage.

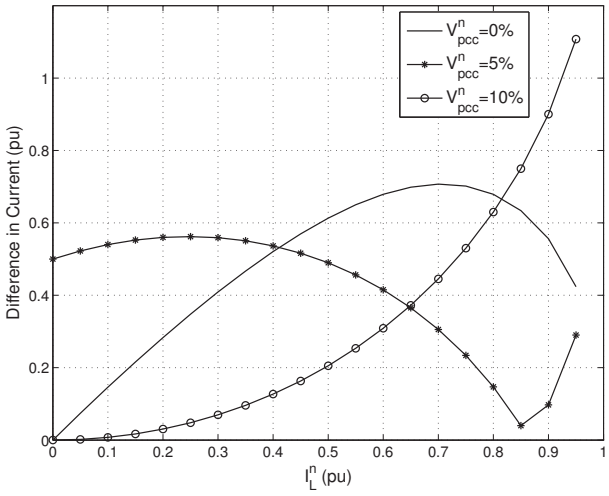

Figure 7.8: Maximum expected difference between two phases of the compensation current

7.8 Summary

The rectifier control unit requires a fast tracking of the symmetrical components; therefore, a new method for the SCE and its application is presented. The control technique is applied to two study cases proving the validity of the control technique.

The method is based on an EO that is fast, accurate and robust. As a result, the extraction gains the same advantages as the EO. The SCE method is tested when the voltage signals undergo sharp and sudden changes for the most severe case with accurate and fast results. The extracted symmetrical components are used by the controller to provide the reference signals to the PWM circuit. A novel control algorithm to mitigate the unbalance is presented in this chapter.

However, the PI-controller is used which is not robust due to the rectifier nonlinearities and system uncertainties. Therefore, the next chapter describes the use of the sliding mode controllers to permeate the rectifier nonlinearities and the system uncertainties, so that a robust controller is attained.

Chapter 8

Sliding Mode Controller

The performance of the rectifier, overshoot, and settling time, is significantly effected by the the chosen controller and the loads nearby the rectifier [59]. The nonlinearities and uncertainties of the system model definitely contribute to the system's dynamic response [118], [119]. A robust controller for the rectifier is required which is studied in this chapter.

8.1 Introduction

Traditionally, the control of the rectifier is implemented by using a Proportional-Integral (PI) controller which is fed by an error signal to determine the command signal. Consequently, the design of the PI-controller, which includes the determination of both the proportional and integral gains, is critical important. Various PI-controller design techniques have been explored for linear systems [65].

Since the rectifier is a nonlinear system, it is linearized around the operating point to optimize the PI-controller. However, the designed controller fails to give the optimum performance at different operating points [120]. Therefore, different adaptive control techniques have been suggested for the rectifier controller [66].

The design of the adaptive controller requires that an accurate model of the system be known in advance, which is not realistic assumption [58]. As a result, there is a need for a

controller whose performance does not depend on the exact system model, *i.e.*, a controller that is robust in terms of the system uncertainties [121].

Nonlinear system model imprecision might stem from the actual uncertainty about the plant; *i.e.* unknown plant parameters or models, or from the choice of a simplified representation of the systems dynamics [122]. In modeling, the two classification are: structured (or parametric) uncertainties and unstructured uncertainties (or unmodeled dynamics). The first type corresponds to inaccuracies in terms included in the model, whereas the second type corresponds to the inaccuracies in the system order [123].

Modeling inaccuracies have strong adverse effects on nonlinear control systems, especially fast acting systems such as static compensation [121]. One of the most important approaches to deal with model uncertainty is a robust control. The sliding mode control is a superior robust control approach. For the class of systems to which it applies, sliding mode controller design provides a systematic approach to the problem of maintaining stability and consistent performance in the face of modeling imprecisions [124].

SMC, as a robust control, has been applied to a number of power electronic-based systems with a great success. The performance is robust and dynamic response is enhanced [125], [126], [127]. Its application to the rectifier has been addressed in [121] for seeking the power system stability. This chapter proposes the SMC as a controller for the rectifier so that the system nonlinearities and uncertainties can be handled.

8.2 Sliding Mode Control

SMC is a special type of Variable Structure Control (VSC) systems. VSC systems are articulated by a set of feedback control laws and a decision rule. The decision rule, namely the switching function, selects a particular feedback control in accordance with the systems behavior. In sliding mode control, VSC systems are designed to drive the system states to a particular surface in the state space, named sliding surface. Once the sliding surface is attained, SMC keeps the states on the sliding surface. In general, SMC has two parts to

design. The first part involves the design of a switching function so that the sliding motion satisfies design specifications. The second is concerned with the selection of a control law that will make the switching surface attractive to the system state.

The main advantages of sliding mode control are:

- its dynamic behavior can be tailored by the particular choice of the sliding function, and
- the closed loop response becomes insensitive to system uncertainties

SMC due to its nature is discontinuous. This creates some problems in application such as chattering; an infinite frequency of the control effort is required at the sliding surface to keep the system states on the sliding surface [128]. Therefore, its implementation in mechanical systems is limited due to the slow responses of mechanical parts. Typically, the filtering and the continuous approximation of the SMC-control law is used to prevent such problems; however, its robustness property might be lost. Instead of filtering, smoothing the control with a bandwidth is conducted [122].

8.2.1 Sliding Manifold

VSC is a high-speed switched feedback control, where the gains in each feedback path switch between two values, according to a rule that depends on the value of the state at each instant. This switching action results in a sliding mode. The purpose of the switching control law is to force the plants state trajectory onto a pre-specified (pre-defined) surface, called a switching surface, in the state space and to maintain the plants state trajectory on this surface for subsequent time till a steady state is reached.

When the plant state trajectory is above the surface, the feedback path has a certain gain, and, if the trajectory drops below the surface, the path has a different gain. This surface defines the rule for proper switching. This surface is also called a sliding surface (sliding manifold). Ideally, once intercepted, the switched control maintains the plants

state trajectory on the surface for all subsequent time and the plants state trajectory slides along this surface to steady state. The most important task is to design a switched control that drives the plant state to the switching surface and maintain it on the surface upon interception. The Lyapunov approach is used to characterize this task.

8.2.2 Lyapunov Function

The Lyapunov method is usually used to determine the stability properties of an equilibrium point without solving the state equation. Let $V(x)$ be a continuously differentiable scalar function, defined in a domain D that contains the origin. Function $V(x)$ is said to be positive definite if $V(0) = 0$ and $V(x) > 0$ for x. The function is said to be negative definite, if $V(0) = 0$ and $V(x) < 0$ for x. The Lyapunov method is to assure that the function is positive definite, when it is negative, and the function is negative definite if it is positive. In that way, the stability is assured.

The Lyapunov function, which specifies the motion of the state trajectory to the sliding surface, is defined in terms of the surface. In addition, the gain is chosen such that the derivative of the Lyapunov function is negative definite, guaranteeing the motion of the state trajectory to the surface. After a proper design of the surface, a switched controller is constructed so that the tangent vectors of the state trajectory point towards the surface such that the state is driven to and kept on the sliding surface.

Let a single input nonlinear system be defined as

$$x = f(x) + b(x)u \tag{8.1}$$

where x is the state vector and u is the control input.

The function $f(x)$ is not precisely known, but the extent of the imprecision on $f(x)$ is upper bounded by a known, continuous function of x; similarly, the control gain, $b(x)$, is not exactly known, but has a known sign and is bounded by the known, continuous functions of x. The control problem is to force the state, x, to track a specific time-varying

state, x_d, in the presence of model imprecision on $f(x)$ and $b(x)$. A time varying surface, $s(t)$, is defined in the state space, $\mathbf{R}^n$, by equating the variable, $s(x,t)$, to zero, where

$$s(x,t) = (\frac{d}{dt}\Delta)^{n-1}e(t) \tag{8.2}$$

where Δ is a strict positive constant, taken to be the bandwidth of the system, and $e = x(t) - x_d$ is the error in the output state, where x_d is the desired state. The problem of tracking the n-dimensional vector, x_d, can be replaced by a first-order stabilization problem in s.

Now, the first order problem of keeping the scalar s at zero is achieved by choosing the control law, u, such that outside of $s(t)$

$$\frac{1}{2}\frac{d}{dt}s^2 \leq -\beta|s| \tag{8.3}$$

where β is a definite positive constant.

Equation (8.3) states that the squared distance to the surface, as measured by s^2, decreases along all the system trajectories. Thus, (8.3) constrains trajectories to point towards the surface, $s(t)$. Once on the surface, the system trajectories remain on the surface. In other words, satisfying the sliding condition makes the surface an invariant set (a set for which any trajectory starting from an initial condition within the set remains in the set for all future and past times). In addition, (8.3) implies that some disturbances or dynamic uncertainties can be tolerated, while the surface is kept as an invariant set.

Finally, (8.3) assures that if $x_{t=0}$ is actually shifted from x_d, the surface, $s(t)$, is reached in a finite time less than $|s_{t=0}|/\beta$. To prove that, let $s_{t=0} > 0$, and let t_f be the time required to hit the surface $s = 0$. Integrating (8.3) between $t = 0$ and t_f leads to

$$0 - s_{t=0} = s_{t=t_f} - s_{t=0} \leq -\beta(t_f - 0) \tag{8.4}$$

which means that

$$t_f \leq s(t=0)/\beta \tag{8.5}$$

implies that the trajectory reachs the manifold surface in less than $|s_{t=0}|/\beta$.

8.3 Controller Design

There are two steps to the SMC design. In the first step, the feedback control law, u, is selected to verify the achievement of the sliding condition. To account for the presence of modeling imprecision and of disturbances, the control law has to be discontinuous across s. Since the implementation of the associated control switching is imperfect, this leads to chattering problem. Practically, chattering is undesirable since it involves a high control activity and can excite high frequency dynamics that are neglected in the modeling. Thus, in the second step, discontinuous control law u is suitably smoothed to achieve an optimal trade-off between control bandwidth and the tracking precision. The first step achieves robustness for the parametric uncertainty, the second step achieves robustness for the high frequency un-modeled dynamics.

8.3.1 Feedback Control Law

In this section, the equations required for the SMC are derived. The task of the control is to keep the PCC voltage at a reference value; that is, choose the error signal so that it is equal to zero. The error signal is measured as the difference between the reference,V_{ref}, and the actual signals as

$$e = V_{pcc} - V_{ref} \tag{8.6}$$

For a three-phase system the voltage at the PCC is given in the PNZ as

$$V_{pcc} = \begin{pmatrix} v^p \\ v^n \\ vz \end{pmatrix} \tag{8.7}$$

As mentioned in Chapter 7, there is a need to regulate the pnz component. Therefore, the voltage magnitude at the PCC is regulated to a reference value and the error signal is

$$e = V_{pcc}^d - V_{ref} \tag{8.8}$$

where

$$V_{ref} = \begin{pmatrix} V_{ref}^p \\ V_{ref}^n = 0 \\ V_{ref}^z = 0 \end{pmatrix} \tag{8.9}$$

The system is stable if the error signal is damped after a definite time. To assure that condition; the following equation should be satisfied

$$\dot{e} = -Ae \tag{8.10}$$

where A is positive definite constant.

The sliding manifold is chosen as;

$$s = Ae + \dot{e} \tag{8.11}$$

Lyaponov's function for the sliding manifold is given as

$$V = \frac{1}{2}s^2 \tag{8.12}$$

which is differentiable, and its first differentiate is

$$\dot{V} = s\dot{s} \tag{8.13}$$

To ensure system stability, $\dot{V}$ should be a negative value. Substituting (8.11) into (8.13) gives

$$\dot{V} = s[A\dot{e} + \ddot{e}] \leq 0 \tag{8.14}$$

Appendix D gives the derivation of $\dot{e}$ and $\ddot{e}$. Substituting with $\ddot{e}$ into (8.14) yields

$$\dot{V} = s[A\dot{e} + F + G \times m] \leq 0 \tag{8.15}$$

To ensure the validity of (8.15), the following condition shall be met

$$[A\dot{e} + F + G \times m] \begin{cases} > 0 & \forall s < 0 \\ = 0 & \forall s = 0 \\ < 0 & \forall s > 0 \end{cases} \tag{8.16}$$

This is insured by using the control law

$$m = \frac{-F - A\dot{e}}{G} - k \times sgn(s) \tag{8.17}$$

where $k > 0$ and

$$sgn(s) = \begin{cases} +1 & \forall s > 0 \\ -1 & \forall s < 0 \end{cases} \tag{8.18}$$

Equation (8.17) indicates that the control signal contains the feedback signal and the switching signal that overcome the uncertainties in the system model.

8.3.2 Chattering Reduction

An ideal sliding mode exists only when the state trajectory of the controlled plant agrees with the desired trajectory at all times. This can require infinitely switching. In real systems, a switched controller has imperfections such as finite sampling time, and limiting the switching to a finite frequency. The representative point then oscillates within a

neighborhood of the switching surface. This oscillation is called chattering [129].

Control laws which satisfy the sliding condition (8.15) and lead to ideal tracking in the face of model uncertainty, are discontinuous across the surface, $s(t)$, causing control chattering [128]. The chattering is undesirable, since it involves extremely high control activity. Furthermore it can excite high-frequency dynamics, neglected in the course of the modeling. Chattering must be eliminated, or at least reduced, for the controller to perform appropriately. This can be achieved by smoothing out the control discontinuity in the thin boundary layer neighboring the switching surface [130].

$$B(t) = \{x, s(x,t) \mid \leq \gamma\} \qquad \gamma > 0 \tag{8.19}$$

where γ is the boundary layer thickness.

In other words, outside $B(t)$, the control law is chosen to guarantee that the boundary layer is attractive; hence all trajectories starting inside $B(t = 0)$ remain inside $B(t)$ for all $t \geq 0$; then u is interpolated inside $B(t)$. By choosing an appropriate value of γ, this approach guarantees an acceptable precision rather than perfect tracking.

8.4 Simulation Results

The integration of the SMC with the rectifier system, Fig. 8.1, is simulated by using MATLAB. The load, connected at the DC bus is implemented by a series resistance and inductor.

For the sake of comparison, the rectifier is controlled by a traditional PI-controller, and the rectifier performance is compared with the proposed SMC. The system supply and load is assumed to be balanced. The PI-controller parameters are optimized for the specific load and operating points. Appendix A gives the system and controllers parameters, where two PI-controllers are obtained. The first PI-controller is optimized when the load is an RL-load and is called PI_{RL}. Ziegler-Nichols' method is used to optimize the PI parameters which is illustrated in [131], [132].

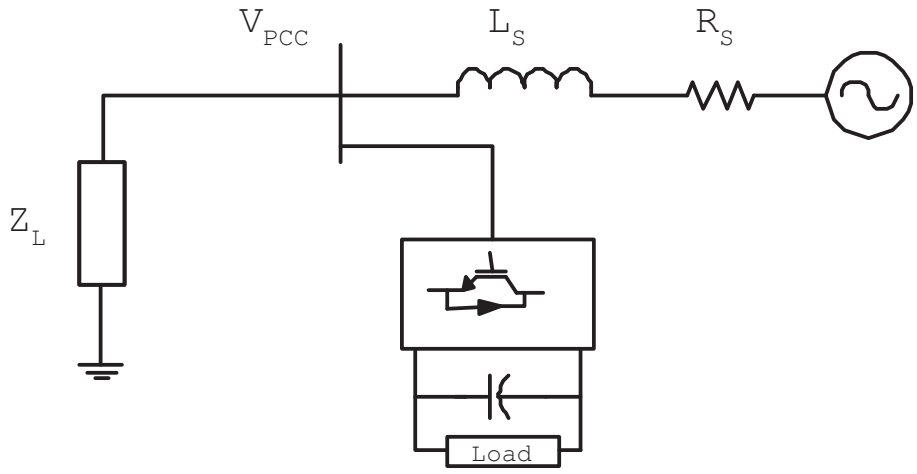

Figure 8.1: System used to evaluate the SMC

The optimized PI-controller is used to control the rectifier at different operating conditions, and its performance is compared with that of the proposed SMC. Three operating conditions are listed here, which are light load, normal load and almost full load.

For the light load condition, a load of 10% is connected to the PCC after 0.35sec. The PCC voltage oscillates where the rectifier is trying to compensate for the voltage drop initiated by the connected load. The V_{pcc} reaches the steady state before the PI-controller with less overshoot, as plotted in Fig. 8.2.

Since the PI-controller is optimized at 60% load, the SMC does not have an advantage over the PI-controller as both have almost the same settling time and overshoots. Figure 8.3 illustrates this study case.

For the heavy loading condition, an 90% load is connected at the PCC causing activation of the rectifier controller. The SMC provides a better response and less oscillation than the PI-controller, as conveyed in Fig. 8.4 shows. In figures 8.2, 8.3, and 8.4, the SMC settling time is hardly changed, which means that the SMC is barely affected by the operating conditions.

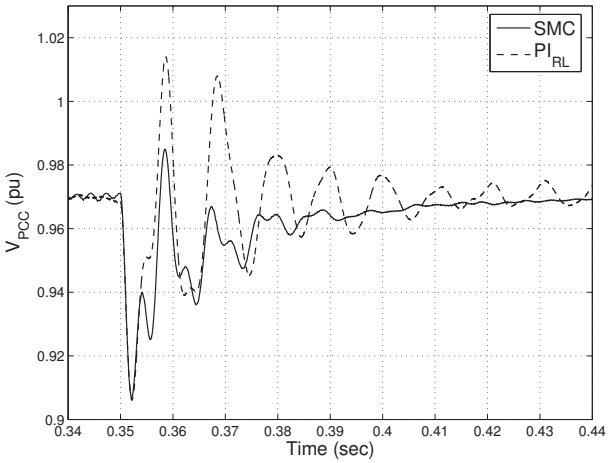

Figure 8.2: Performance of the SMC and PI at 10% load for the RL load

8.5 Summary

In this chapter, a unified approach for a sliding mode controller to control the rectifier is discussed. Such a controller is proposed to overcome the uncertainties in the loading conditions; therefore a robust control can be achieved. The design steps are laid out and exhibit the following advantages

- The design steps are easy and straightforward.
- The controller has good transient response at different loading conditions and different loads.
- The control scheme can be extended to other equipment's interface or any voltage source inventer-based equipment such as a distributed generator.

By designing a robust controller for the rectifier, the control of the VSR is composed of robust units: the ET, PLL, SCE, and controller. Therefore, the next step is to integrate these devised algorithms in a rectifier included in the ASD.

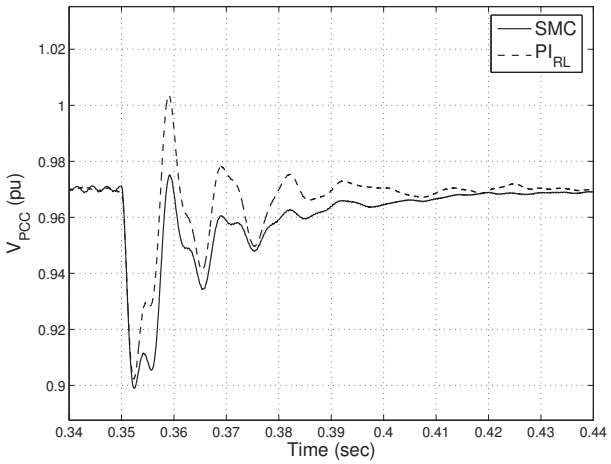

Figure 8.3: Performance of SMC and PI at 60% load for RL load

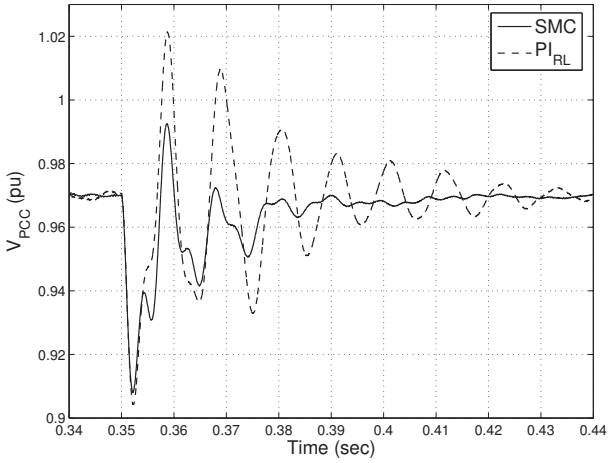

Figure 8.4: Performance of the SMC and PI at a 90% load for the RL load

Chapter 9

Self Immune Rectifier (SIR)

Previously, the RCU elements, including the ET, PLL, SCE, and controller, have been obtained by utilizing robust algorithms. These algorithms are used and tested individually. In this chapter, they are integrated into the rectifier control unit as part of the ASD which draws an active power to drive a motor.

9.1 Introduction

Three-phase VSR have a wide range of applications, such as electro-chemical process, traction equipment, controlled power supplies, and adjustable speed drives.

In this chapter, an extra function is added to the VSR to mitigate the PQ problems, caused by other loads at the PCC, *i.e.* the DSTATCOM function is integrated into the rectifier function. Such an implementation makes the rectifiers more friendly to the distribution system. A control technique is proposed for the additional function, based on controlling the rectifier in the voltage control mode. This type of rectifier is called Self Immune Rectifier (SIR).

9.2 Power Flow Control of the Rectifier

The VSR in Fig. 9.1 is by far, the most popular type of force-commutated rectifier which is selected as the base for the proposed technique; therefore, it is crucial to explain the rectifier in more detail.

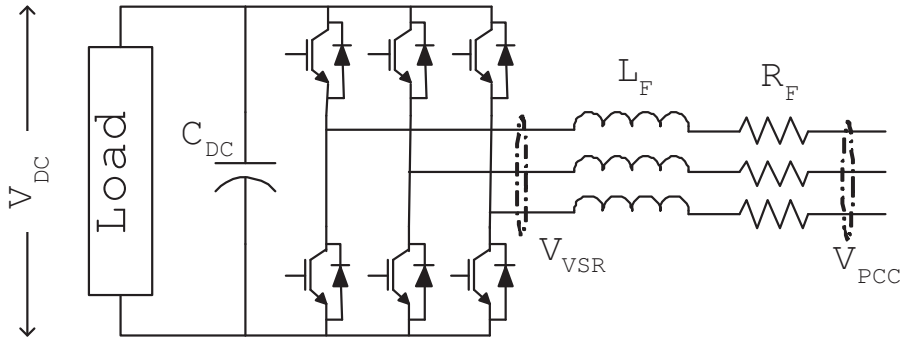

Figure 9.1: Voltage source rectifier using IGBTs for AC/DC conversion

The rectifier consists of six power switches along with six diodes. The PWM is used as a switching technique for the power switches so the current, drawn by the rectifier, is a harmonic-free sinusoidal waveform. The PWM technique needs two control signals, namely the modulation angle (ϕ) and modulation index (m) [133].

The equivalent circuit of the VSR in Fig. 9.1 is realized by applying the GAM and is shown in Fig. 9.2, where the AC-voltage at the front of the six switches bridge is known as the V_{VSR}. This voltage is a function of the PWM parameters, *i.e.*, modulation frequency ω_{PWM}, index m and angle ϕ and is given by

$$V_{VSR} = mV_{DC}sin(\omega_{PWM} + \phi) \tag{9.1}$$

Equation (9.1) relates that the voltage magnitude of the V_{VSR} can be controlled by the modulation index, m. So that the rectifier can operate properly, the PWM pattern must generate a fundamental voltage of V_{VSR} with the same frequency as that of the power source.

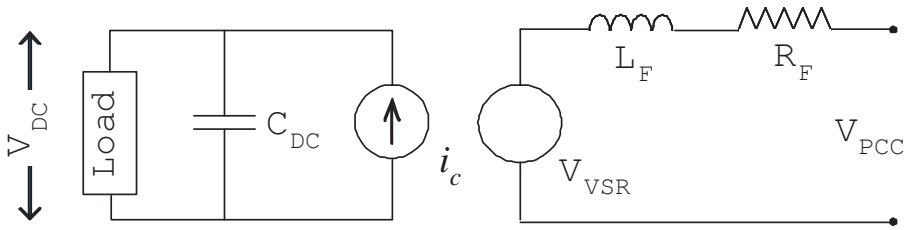

Figure 9.2: Equivalent circuit of Voltage Source Rectifiers using IGBTs for AC/DC conversion

Neglecting the filter resistance, R_F, the power flow between V_{PCC} and V_{VSC} is given as

$$\begin{aligned} P &= \tfrac{1}{x_f} V_{PCC} V_{VSR} sin\phi \\ Q &= \tfrac{1}{x_f} V_{VSR}^2 + \tfrac{1}{x_f} V_{PCC} V_{VSR} cos\phi \end{aligned} \tag{9.2}$$

Equation (9.2) signifies that the active power flow and reactive power flow can be controlled by the angle, ϕ, and the voltage magnitude of the voltage, respectively. As a result, by changing the amplitude of this fundamental by controlling m, and its angle ϕ with respect to the source voltage, the rectifier can supply or absorb both active and reactive power [34].

To obtain UPF, the reactive power that is drawn by the rectifier has to be zero, *i.e.* the current and the voltage have to be in-phase. Different control algorithms are proposed [134], [135], [29], [136]. These techniques can be classified as either current controlled or voltage controlled, where the voltage control is preferred due to its less switching than that of the current control [23].

The voltage control technique computes the modulation angle and index such that the UPF condition is attained. Two control loops are required to determine the PWM inputs as discussed in Chapter 2.

9.3 Self Immune Rectifier (SIR)

The idea behind the proposed system is to inject a reactive power from the rectifier into the system. This reactive power can be used to regulate the voltage at the PCC and mitigate PQ problems, such as sag, flicker, swell and harmonic. Such a configuration is called Self Immune Rectifiers (SIR) and increases the immunity of the ASD to PQ problems.

9.3.1 Proposed Configuration

As identified in Chapter 2, the components of the rectifier control unit are

1. The PLL takes care of synchronizing the PWM with the voltage at the PCC.
2. The controller regulates the voltages at the DC-bus and the AC-bus. The outputs of the control unit are the modulation index and modulation angle of the PWM.
3. The envelope tracking extracts the envelope of the sinusoidal voltage at the PCC and delivers it to the controller.
4. The SCE extracts the PNZ-component of the voltage at PCC.
5. The PSG unit converts the PWM indices to an equivalent three-phase signals according to

$$\begin{aligned} u_a &= m_p sin(\omega t + \phi_p) + m_n sin(\omega t + \phi_p) + m_z sin(\omega t + \phi_z) \\ u_b &= m_p sin(\omega t + \phi_p + \tfrac{2\pi}{3}) + m_n sin(\omega t + \phi_p + \tfrac{4\pi}{3}) + m_z sin(\omega t + \phi_z) \\ u_c &= m_p sin(\omega t + \phi_p + \tfrac{4\pi}{3}) + m_n sin(\omega t + \phi_p + \tfrac{2\pi}{3}) + m_z sin(\omega t + \phi_z) \end{aligned} \tag{9.3}$$

   where (ωt) is obtained from a PLL.

The robust techniques, developed in this thesis, are implemented in this chapter for the control unit of the SIR.

9.3.2 Proposed Control Technique

The tasks of the controller are to regulate the voltage at the PCC and at the DC-bus. Therefore, four control loops are required, as explained in Chapter 7 and illustrated in Fig. 9.3. Also, the controller requires that the voltage at the DC-bus and the symmetrical components of the voltage at the PCC be measured.

Equation (9.2) indicates that the active power flow can be controlled by the manipulation of the PWM modulation angle; thus, the angle, ϕ, is adopted to regulate the DC-voltage. The first control loop, DC-regulator, is a SMC-controller which monitors the voltage at the DC-bus and regulates it by varying the modulation angle.

The second to the fourth control loop are called AC-regulators which regulates the voltage at the PCC by pumping an adequate a mount of compensating reactive power into the distribution system. The error signal, the difference between the reference value and the actual voltage magnitude, is used by a controller such as the PI or SMC, to adjust the modulation index of the PWM, m, [136].

9.3.3 Harmonic Signal (u_H)

Figure 9.3 portrays a signal called u_H. It is reserved for harmonic mitigation, where the SIR operation is similar to APF operation. Various techniques have been proposed for the operation and control of the APF [137], [138]. The instantaneous power theory has the lead application of those techniques [139]. Therefore, it is selected in this thesis to determine the three-phase reference signals fed to the PWM switching technique.

9.4 Simulation Results

For the sake of evaluating the proposed control technique, the SIR system is simulated by using Matlab. In the simulation, the task of the SIR is to regulate the voltage at the PCC and at the DC-bus.

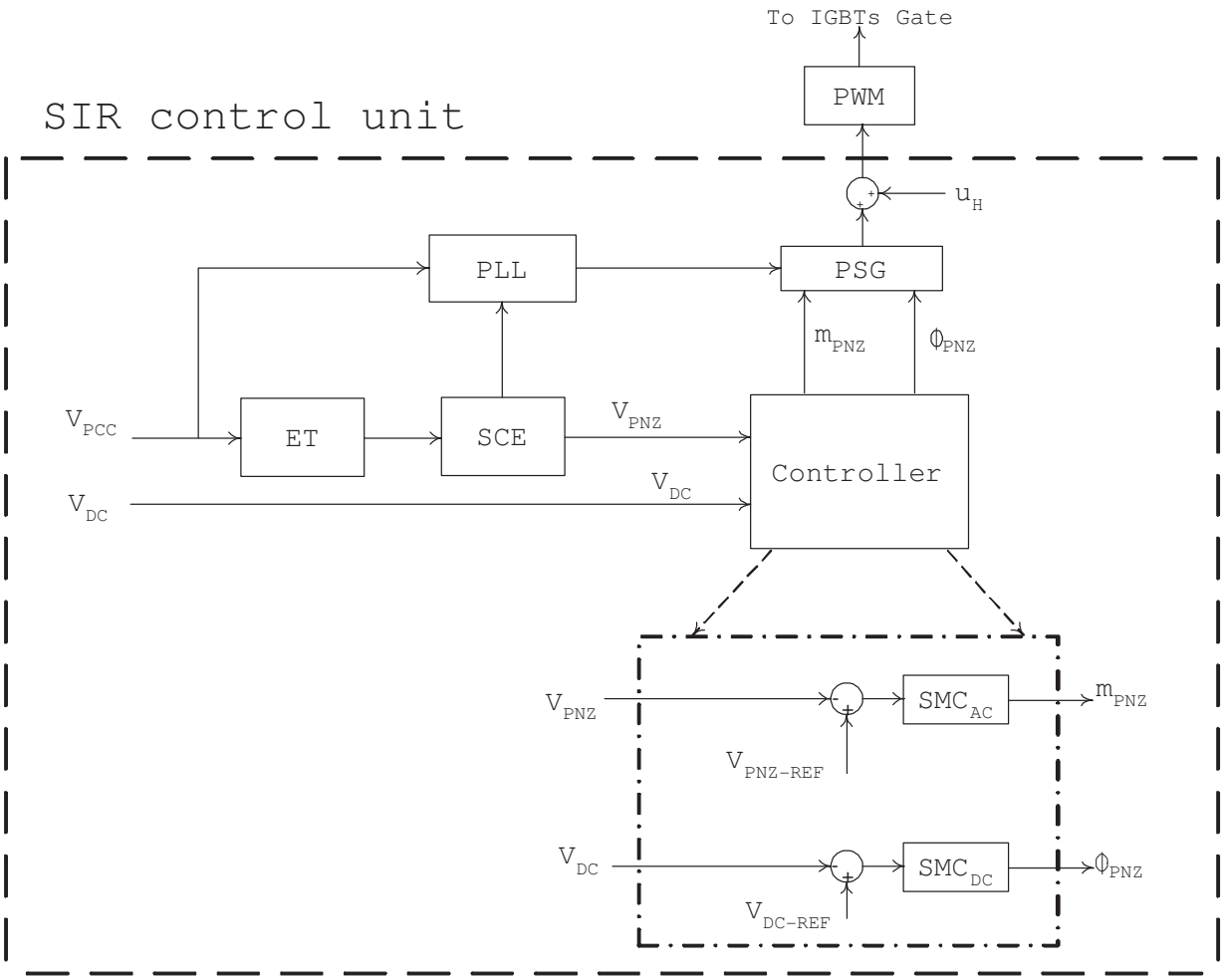

Figure 9.3: SIR control unit used as part of the ASD

The first case is a SIR connected to a resistive load, connected at the DC-bus, where the SIR is used as a static compensator. In the second case study, the SIR is a part of the ASD system and supplies a regulated DC-voltage to the inverter, and compensates for the voltage at the PCC.

9.4.1 Resistive Load at the DC-bus of The SIR

The *AC*/*DC* rectifier can supply a DC-power to different types of DC-loads such as welding machines or heaters. These loads are modeled as a resistance, connected at the DC-bus.

The system, Fig. 9.4, exhibits a 3-phase load, connected at the PCC, called an AC-load, and the SIR is connected at the same PCC. During normal operation, since both loads can vary, the voltage at the PCC fluctuates. This fluctuation is mitigated by injecting a reactive power by the SIR, so the voltage at the PCC is constant. In the following subsections, the effect of AC- and DC-load switching is explained.

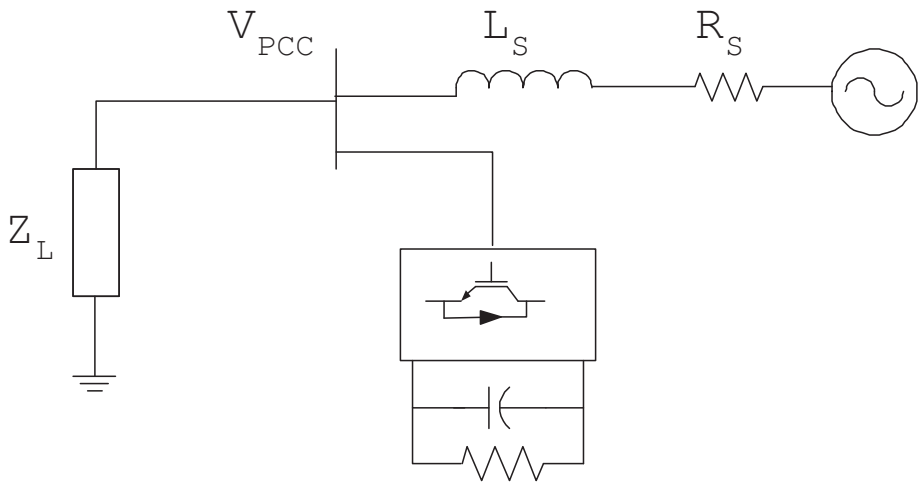

Figure 9.4: System of SIR supplying a resistive load

9.4.1.1 Step Change in the AC-load

The three-phase linear load, connected at the PCC, is increased by 50%, causing the V_{PCC} to drop. The AC-regulation control loop is activated and change the reactive power supplied by the SIR to compensate for this voltage drop.

Figure 9.5 traces the response of the system due to this event. It is evident that the voltage at the PCC oscillates and reaches the regulated value after 50ms. In addition, the reactive power supplied, by the SIR is increased, while the active power remains constant since there is no change in the DC-load.

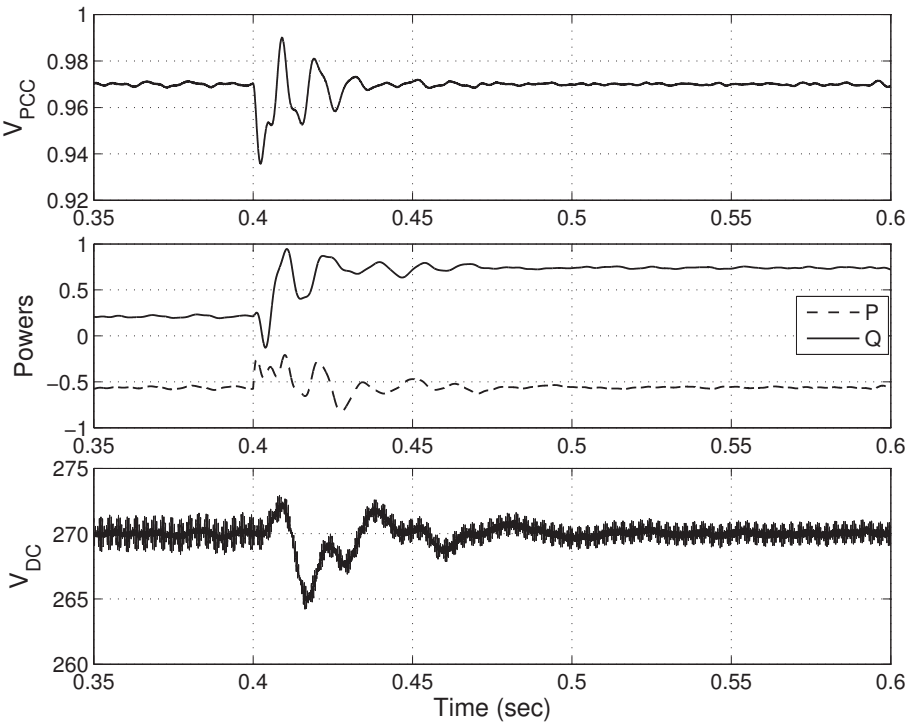

Figure 9.5: SIR response to a step change in the AC-load

9.4.1.2 Step Change in the DC-load

In this case, the DC-load increases from 0.5 pu to 1 pu producing a voltage drop at the the DC-bus. Consequently, the DC-regulator controller restrains the DC-bus voltage by absorbing more active power from the grid. This active power increase causes a voltage drop at the PCC. Again, the AC-regulator control loop is engaged and the reactive power will be increased to compensate for the voltage drop.

Figure 9.6 shows the response of the system due to this disturbance, where the voltage at the PCC and the DC-bus remain constant. In addition, both the active and reactive power are elevated.

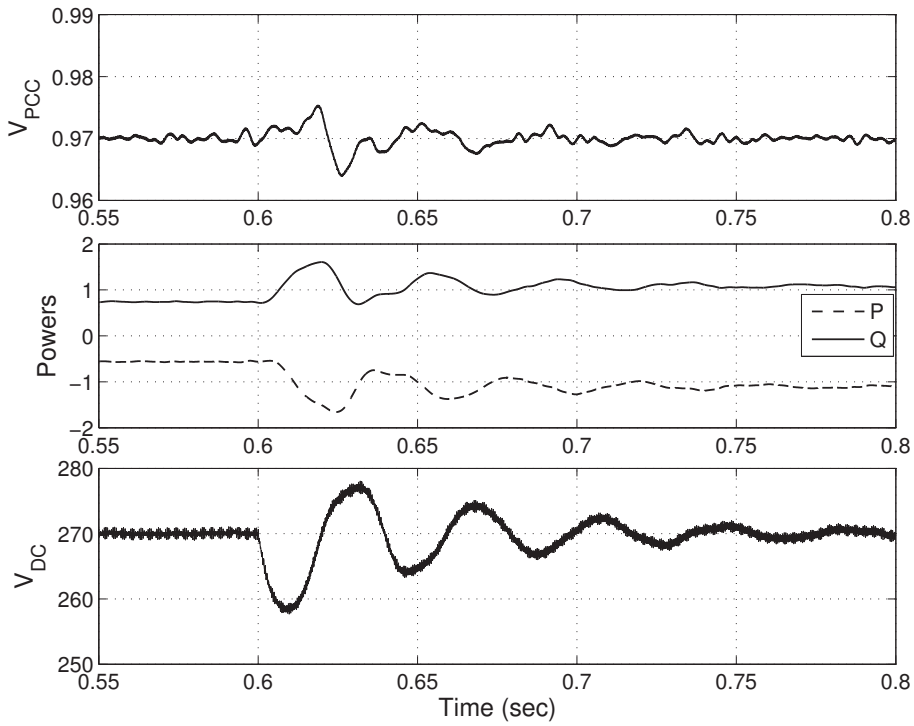

Figure 9.6: SIR response to a step change in the dc-load

9.4.2 SIR as a Part of Adjustable Speed Drive

The SIR can be a part of the ASD, as shown in Fig. 2.1, to deliver a DC-voltage to the inverter. The ASD with the SIR is denoted in Fig. 9.7 and the system data is presented in Appendix A.

9.4.2.1 Response to Different ASD Operating Points

The motor mechanical torque and mechanical speed will vary frequently and so does the active power drawn by the rectifier. Although the SIR can operate at UPF, the active power instigates a voltage drop at the PCC. Whether or not the voltage drop is initiated by the ASD or by any other load, the SIR can still supply a reactive power to compensate for these drops. Figure 9.8 reflects the power injected by the SIR at various operating points of the ASD where the active power has a negative sign because it is drawn by the

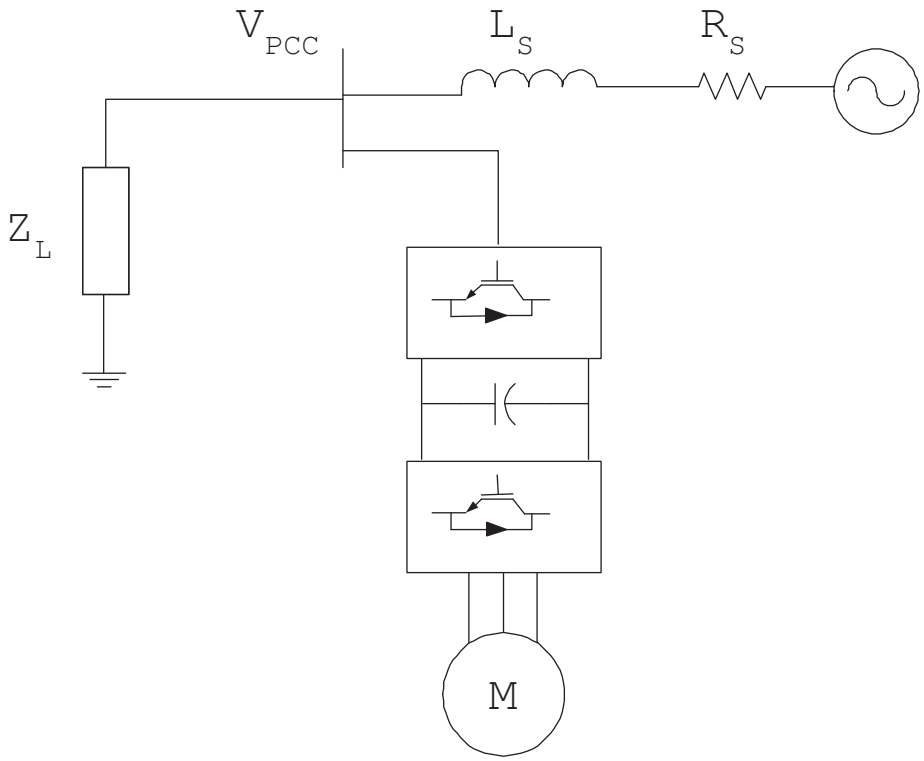

Figure 9.7: SIR is used as a part of ASD

ASD. It is evident that with the variation in the motor operating conditions, the voltage at the PCC remains constant as follow:

1. After 0.75s, the mechanical load, the torque, is increased to 75%, causing the active power drawn by the ASD to jump to a higher value. The increase in active power initiates a voltage drop at the PCC, which triggers the SIR controller to inject a compensating reactive power. Therefore, the voltage at the PCC and the DC voltage stay constant.

2. After 1.0s, the mechanical load jumps to 100% causing a further reactive power injection.

3. At 1.6s, the mechanical load is reduced to 60%. Therefore, the reactive power from the SIR is reduced to maintain the PCC at a constant value.

4. The speed is is reduced at 2s. Again, the SIR controller keeps the voltage at the PCC constant.

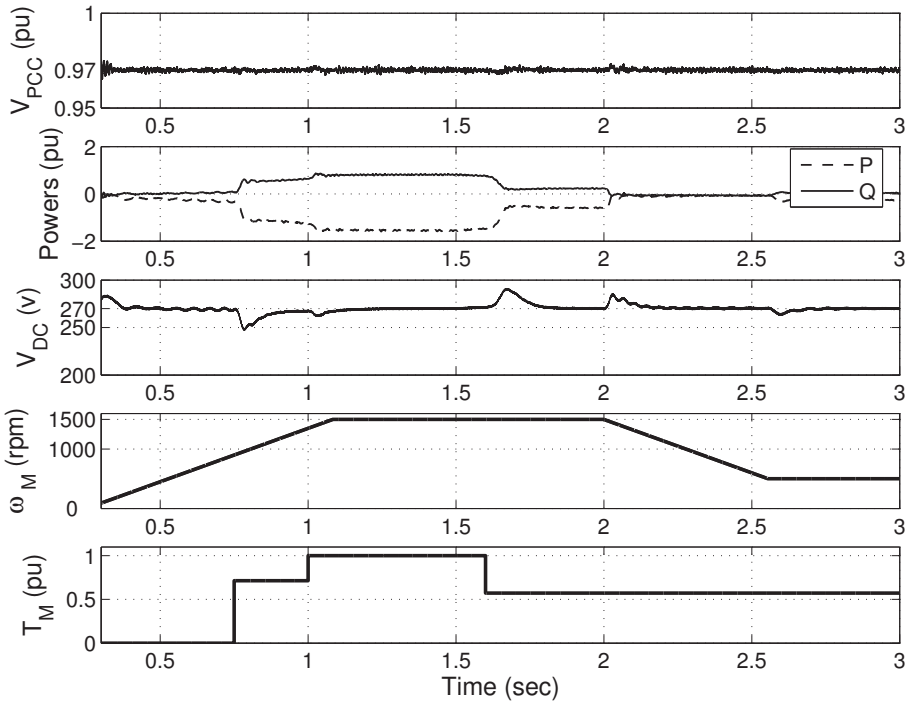

Figure 9.8: SIR response to variations in the motor load and speed

Figure 9.8 offers the voltage at the PCC and the DC bus remain constant during the different operating points of the ASD. Therefore, the speed of the ASD remains regulated which eliminates premature tripping of the ASD due to the PQ at the PCC.

9.4.2.2 Sag and Flicker Mitigation

The system is subjected to the same sag level and same flicker level at the PCC. Figure 9.9 and and Fig. 9.10 illustrate that the speed of the ASD is less affected by the voltage sag and flicker at the PCC, than the speed illustrated in Fig. 2.2 and Fig. 2.3.

By comparing Fig. 9.9 with Fig. 2.2, and Fig. 9.10 with Fig. 2.3, the following is noticed

1. The ASD speed remains within a 1% limits of the controller in Fig. 9.9 and 2.3, whereas it drops by almost 10% in Fig. 2.2 and fluctuates by 5% in Fig. 2.3.

2. Note 1 is also applicable for the DC-bus voltage.

3. The motor stator current stays within the limits, *i.e.* neither an overcurrent nor a current fluctutation is observed in Fig. 9.9 and Fig. 2.3.

4. The ASD, or the SIR current, increases during the sag and flicker periods. This increase is required to inject the compensation reactive power.

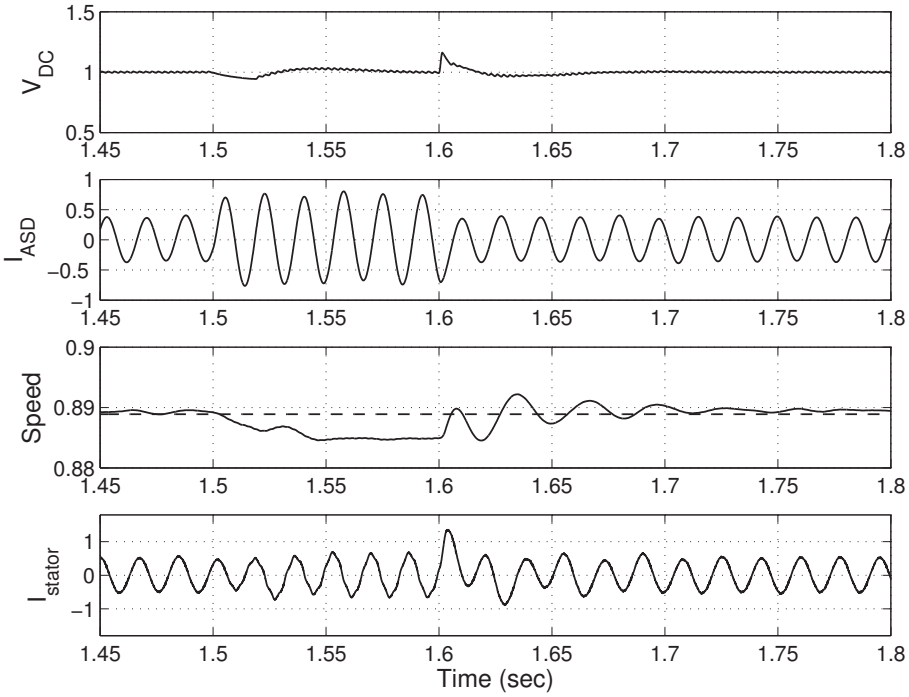

Figure 9.9: SIR response to sag

9.4.2.3 Unbalance Mitigation

In this study case, the unbalance mitigation is examined by using SIR. The system, described in Fig. 9.7, is studied. The unbalance voltage is caused by the unbalanced load

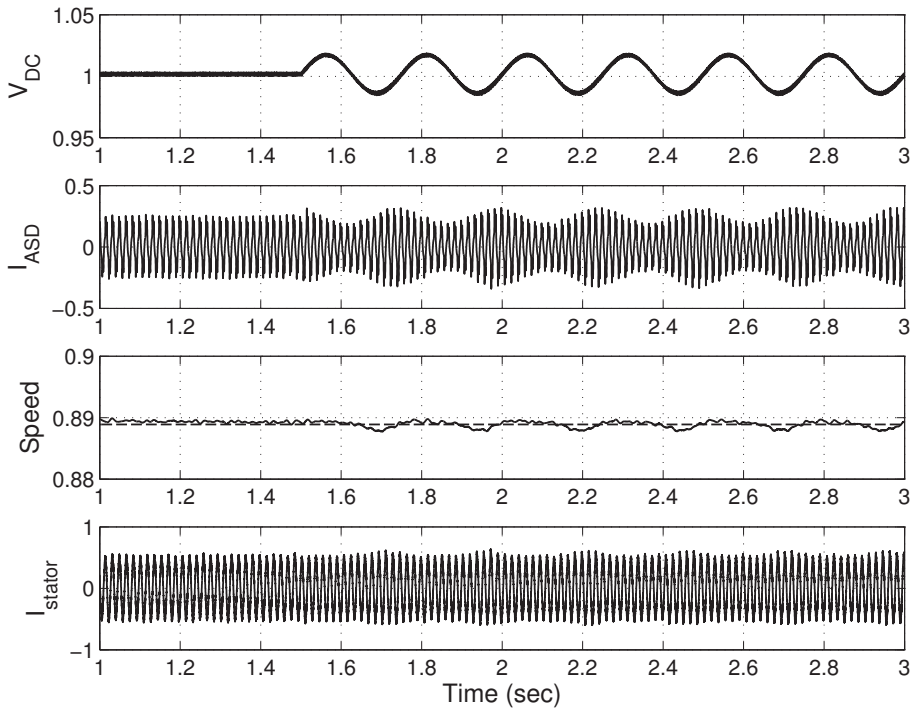

Figure 9.10: SIR response to flicker

connected at the PCC. The SMC and the PI-controller are used to define the command signals. Figure 9.11 portrays the system response when the unbalanced load is connected after 400msec with the SIR installed and without the SIR. It is clear that the SIR is able to cancel the negative and zero components of the voltage at the PCC when the SIR is controlled by the conventional PI and by the SMC with a better performance obtained by the SMC. Ziegler-Nichols' method is used to optimize the PI parameters which is illustrated in [131], [132].

9.4.2.4 Harmonic Mitigation

This study case is dedicated to describe the ability of the SIR to mitigate the harmonics, injected by a nonlinear load connected at the PCC. The linear load in Fig. 9.7 is replaced by a nonlinear load, namely a full-wave uncontrolled rectifier. The SIR is employed to regulate the voltage at PCC and to mitigate the harmonics injected by the nonlinear load.

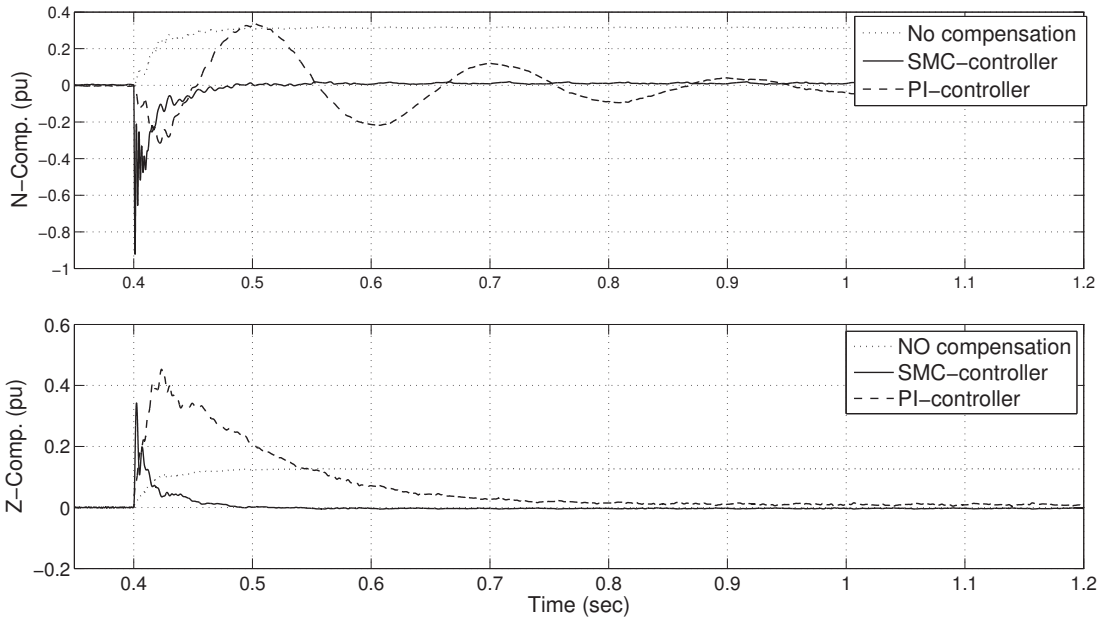

Figure 9.11: Symmetrical Components of the voltage at PCC

Initially, the "*other signals*" are disabled for 300ms, and then is enabled again to allow the harmonic mitigation. Figure 9.12 shows the voltage at the PCC, where the voltage signal is distorted. The harmonic content of the voltage signal is shown in Fig. 9.13, where the harmonic contents of the voltage has been reduced after 300ms. The reduction of the voltage harmonic content is due to the cleaned supply current in Fig. 9.14.

9.5 Discussion

The design of the rectifier involves the proper selection of the power switches, DC-capacitor, and transformer ratings. Definitely, there is an increase in the rectifier ratings due to the functions and the rectifier shall be re-rated. Since, these functions can be carried out by custom power devices, such as the DSTATCOM or APF, the cost of the re-rating versus the cost of the CP should be ascertained. If the rectifier is already in service, and the power switches are undergoing replacement, it is cost effective to re-rate the rectifier and

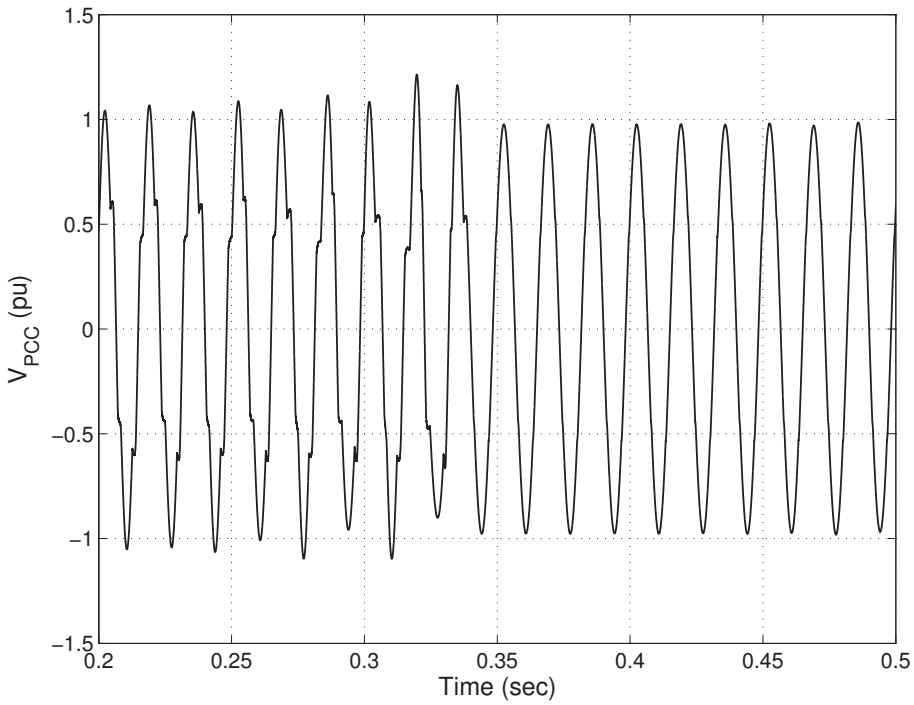

Figure 9.12: Voltage at PCC where harmonic mitigation starts after 0.3 seconds

add these functions to it.

A vital factor in the savings amount is the rating ratio of the SIR, compared with both the rating of the CP and that of rectifier. Assume that the active power rating of the rectifier is P_R, and the reactive power rating of the CP is Q_{CP}. The SIR rating is the summation of both powers and is

$$S_{SIR} = \sqrt{P_R^2 + Q_{CP}^2} \tag{9.4}$$

Let C_R be the cost of the rectifier and SIR ($\$/KVA$) and C_{CP} be the cost of the CP ($\$/KVA$); then, the total saving due to the SIR is

$$Saving(\$) = [C_{CP} * Q_{CP} + C_R * P_R] - C_R * S_{SIR} \tag{9.5}$$

Since the hardware requirements for the rectifiers and the CP are very similar, the cost

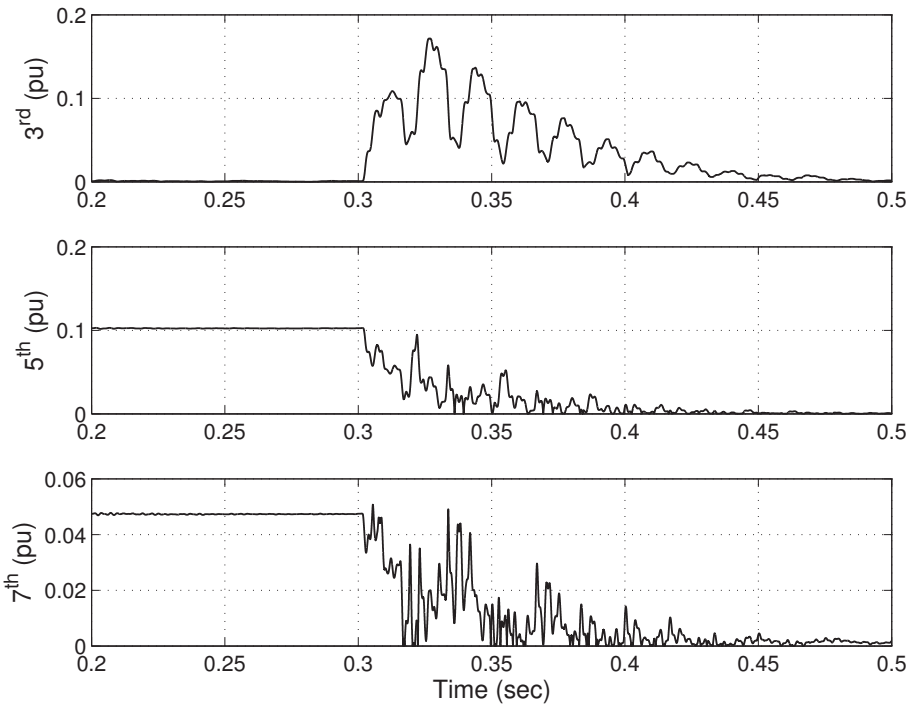

Figure 9.13: Harmonic contents in V_{PCC} where harmonic mitigation starts after 0.3 seconds

can be assumed to be equal or with small deviations. Accordingly, the savings percentage versus the rating ratio is plotted in Fig. 9.15 with the different costs. The figure relates that the saving percentage can as high as 35% of the actual cost, and as low as 5%, when $C_{CP} \leq C_R$. If $C_{CP} \geq C_R$, the savings percentage will be less than that of the other cases, as shown in Fig. 9.15. In addition, when the power rating of the rectifier is four times the CP rating, it is not economical to use the proposed technique, since as the cost is higher. Obviously, a comprehensive study should be conducted on the actual costs and ratings.

9.6 Summary

In this chapter, a novel function is integrated into the VSR to mitigate the PQ problems at the PCC by injecting a reactive power into the distribution network. In addition, the VSRs are more friendly to the distribution system in terms of the PQ. By adding this

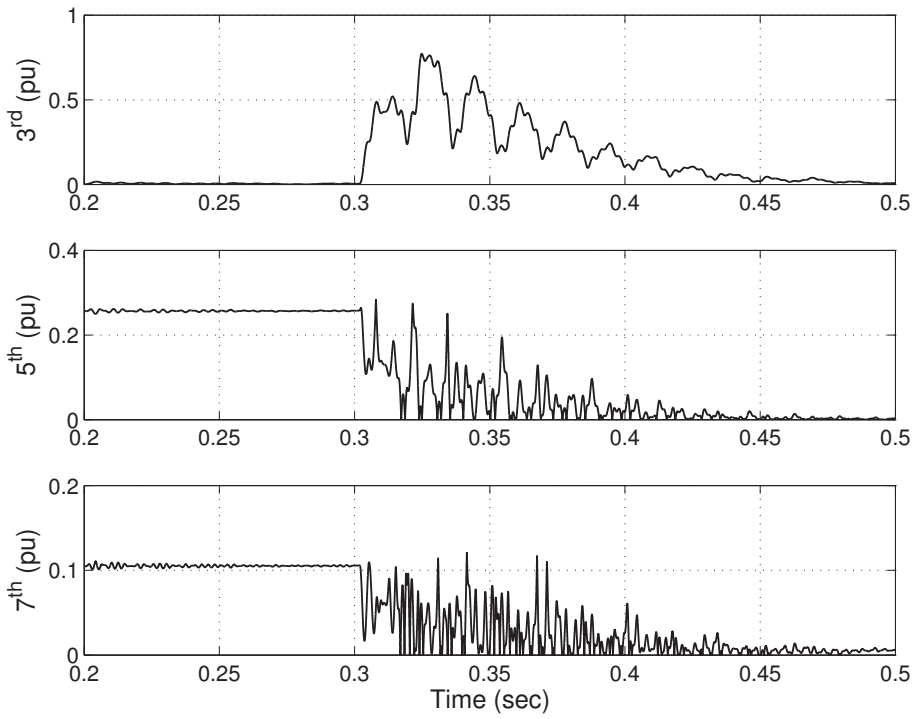

Figure 9.14: Harmonic contents in the supply current where the harmonic mitigation starts after 0.3 seconds

function, there is no need for the DSTATCOM; thus, the adherent interaction between them is avoided. This chapter proposes a control technique for the AC/DC rectifiers to carry out the newly added functions, based on the PWM switching technique.

Three study cases are presented where the rectifier is used to supply a DC-resistive load and as a part of the ASD. The study cases prove that the newly devised control technique can be used to add the extra function to the rectifier. The rectifier has supplied the adequate reactive power needed to compensate for the voltage drop, caused by the load on both the AC-side and DC-side of the rectifier. In addition, the harmonic mitigation capabilities hre confirmed.

Since the extra reactive power needed for the mitigation purposes is supplied from the DC capacitor, its capacity has to be re-rated to assure its capability for supplying adequate power. Therefore, an economic study should be conducted to compare the cost of re-rating

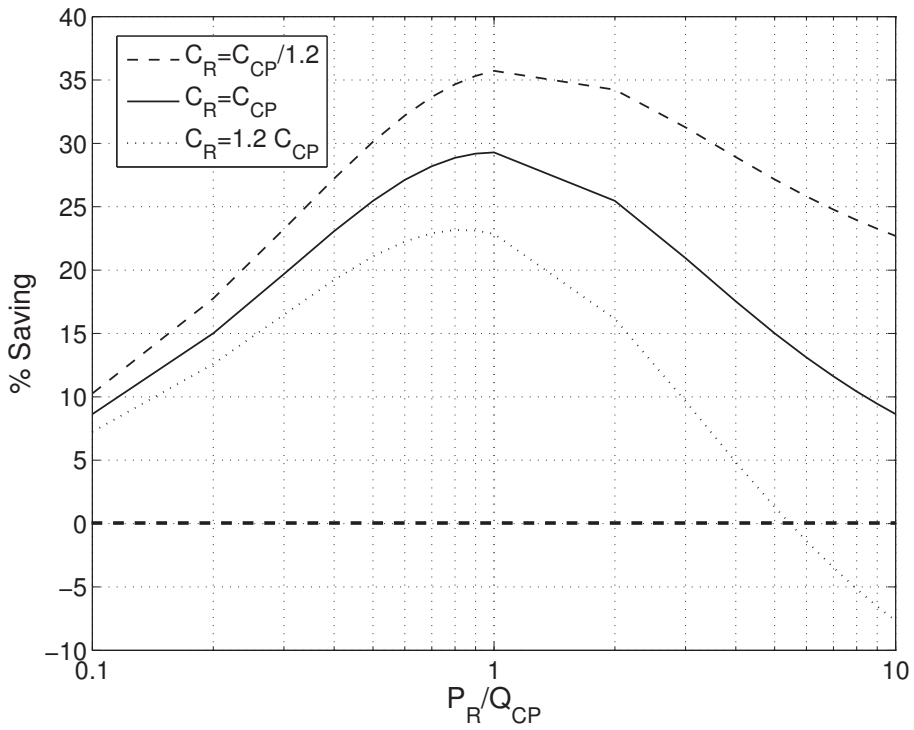

Figure 9.15: Savings percentage at different rating ratios

the rectifier and installing the DSTATCOM or APF to take care of the mitigation. The economic study reveals that the additional reactive power, required by the rectifier, plays an important role in determining the economical benefits of the SIR.

Chapter 10

Conclusion and Future Research

In this thesis, the effect of poor power quality on the ASD is investigated to avoid premature tripping of the ASD. An in-depth study indicates that the immunity of the ASD to poor power quality can be improved if the immunity of its rectifier is modified. Therefore, the rectifier control unit of the ASD is retrofitted with a power conditioning function to imrove the selfe immunity of the ASD. As a result, the ASD does not prematurely trip due to power quality problems. Various novel algorithms and techniques are presented to achieve self immunity for the ASD.

10.1 Conclusion

The conclusions derived from the comparison of the previous work in the literature and the new research in this thesis can now be summarized

1. A fast and robust control of the rectifier is achieved by using algorithms that are based on the energy operator which is inherently fast and robust. The drawbacks of Teager's energy operator can be overcome by utilizing a new algorithm.

2. The analogue and digital form of the new energy operator are realized by different circuit configuration. Four circuit configurations are investigated. The following can

be concluded:

- The lead-lag circuit gives the best performance, but it requires the use of active components. Therefore, it is suggested for the application which requires a high accuracy, regardless of the space, occupied by the circuit elements.
- The inductive-capacitive provides an acceptable performance, and needs only passive components, but a caution should be taken regarding the core saturation of the inductor.
- The doubly-capacitive also performs well, and it requires passive components only, which makes it more appropriate for the application that concerns the area of the circuit.
- The doubly-inductive circuit exhibits an acceptable performance, but its not recommended due to the inductor-core saturation.

3. A PLL can be achieved by using the energy operator and the application for envelope tracking with an accuracy of less than 2%.
4. The symmetrical components are extracted based, on a robust technique by using the energy operator.
5. The voltage control rectifier is adopted to mitigate the voltage unbalance caused by unbalanced loads or an unbalanced supply.
6. The higher the unbalanced voltage level is, the larger the rectifier capacity is.
7. The Sliding mode controller is tailored to fit the voltage control rectifier, and results in a robust response with respect to the system operating point and model uncertainties.
8. The ASD tripping due to power quality problems, can be eliminated, if the control of the rectifier is modified to mitigate the power quality problems.

9. The rating of the adjustable speed rectifier is increased by adding more functions. Therefore, there is a need for a study to compare the costs of installing a new DSTATCOM or integrating its function with the rectifier.

    - It is found that the rating of the DSTATCOM, with respect to the rating of the speed drive, is the most essential factor in the economic decision.
    - The maximum economic benefits are obtained when the rating of the DSTATCOM and the speed drive are equal.
    - The economic benefits of the integration is lost, when the rating of the DSTATCOM is larger than the rating of the speed drive .
    - The financial benefits might become losses, if the rating of the DSTATCOM is much higher than that of the speed drive rating.

10. The interaction between the DSTATCOM and the adjustable speed drive can not be neglected in any practical distribution system. These interactions can cause instability of the ASD, and consequently, unexpected tripping.

11. The characteristic equation of the current-control DSTATCOM indicates that its stability is highly effected by the mechanical load and speed of the motor, but the stability of the voltage-control DSTATCOM is not affected by either the load or the speed.

12. The distribution system can be monitored without installing monitors at all the buses by measuring certain state variables and computing the other variables. Therefore, the number of the monitors can be optimized.

13. The optimum allocation of the monitors can save up to 86% of the cost, depending on the system connectivity.

10.2 Contribution

The contribution of the work in this thesis can be summarized as follow

1. A novel method to monitor the entire distribution system at minimum cost is developed. The effect of data redundancy is considered and a new factor, called the redundancy data factor, is suggested to judge the allocation methods in terms of data redundancy.

2. The overlooked interactions between the adjustable speed drive and DSTATCOM are investigated as a major factor to be considered for the operation of the distribution system.

3. A novel method, which is stable and robust, for computing the energy operator to overcome the drawback of the existing method has been introduced. The method is used for the envelope tracking to extensively investigate sag, swell, flicker, and unbalance mitigation. Different circuits designs are discussed and thoroughly tested in the laboratory.

4. The new energy operator is adopted to build a fast and robust PLL circuit. The digital implementation of such a PLL in the laboratory by utilizing FPGA has been investigated.

5. A method for symmetrical components extraction is developed, based on the energy operator and the phase-locked loop. The method is as fast and robust as the energy operator. In addition, a new control method, used in the voltage-control rectifier for the unbalance compensation, caused by load and supply, is presented.

6. A robust controller based on the sliding mode control theory for the voltage-control rectifier is proposed. The adaptation of the sliding mode control for the rectifier is also provided.

7. A usage for the adjustable speed drive rectifier-circuit is devised to integrate the power conditioning functions so that there is no need for the DSTATCOM. Consequently, premature tripping of ASD due to power quality problems are mitigated. An appropriate control for this integration, along with an economics of such an integration is explained.

10.3 Future Work

The research work presented in this thesis discloses a number of issues that should be further investigated

1. Although the interaction between the DSTATCOM and adjustable speed drive is investigated in this work, the interaction between the adjustable speed drive and the distributed generation needs to be highlighted.

2. The coordination of the ASDs should be studied to enhance the power quality level throughout the entire system instead of the local bus. In addition, the coordination between the ASD and the distributed generation used in power quality problems mitigation should be studied.

3. Although a primary study of the financial benefits and limitation integrating the power conditioning to the ASD is initiated in this thesis, a detailed study is needed. A study of the economics should also consider its manifestation on the power quality contacts between the utilizes and the customers, since, the customer can save money by asking for a lower power quality level from the utility. This savings can be invested in retrofitting ASDs.

Appendix A

The System Data

The system studied has the following data

Table A.1: The Data of the system (all are in pu)

Param.	Value	Param.	Value
r_s	0.025	r'_r	0.020
x_s	2.075	x'_r	2.075
x_m	2.000	H	0.200
r_f	0.025	x_f	0.500
c_f	0.014		
r_t	0.110	x_r	0.180
C_{dc}	0.414	v_c	1.410

The ASD data are adapted from [140] with basis of 7.5hp and 115V. The data of the DSTATCOM are adapted from [112] based on 10KVA and 115V.

The PI-controller has a transfer function of form given in (A.1), where the subscript x denotes any subsystem.

$$PI_{ASD} = K_x^p + K_x^i \int \tag{A.1}$$

Appendix B

Induction Motor Matrices

$$x_{im} = \begin{pmatrix} x_s & 0 & 0 & 0 \\ 0 & x_s & 0 & 0 \\ 0 & 0 & x'_r & 0 \\ 0 & 0 & 0 & x'_r \end{pmatrix} \tag{B.1}$$

$$A_{im} = \begin{pmatrix} r_s & \frac{\omega}{\omega_b} x_s & 0 & \frac{\omega}{\omega_b} x_m \\ -\frac{\omega}{\omega_b} x_s & r_s & -\frac{\omega}{\omega_b} x_m & 0 \\ 0 & \frac{\omega-\omega_r}{\omega_b} x_s & r'_r & \frac{\omega-\omega_r}{\omega_b} x'_r \\ -\frac{\omega-\omega_r}{\omega_b} x_s & 0 & -\frac{\omega-\omega_r}{\omega_b} x'_r & r'_r \end{pmatrix} \tag{B.2}$$

$$x_s = x_{ls} + x_{ms} \tag{B.3}$$

$$x'_r = x'_{lr} + x'_{mr} \tag{B.4}$$

Where r_s and x_{ls} refer to the stator resistance and the leakage inductance, r'_r and x'_{lr} refer to the rotor resistance and the leakage inductance, respectively.

Appendix C

Digital Form Derivation Of The Energy Operator

The transfer function of the used lead and lag network is given by:

$$\frac{v^s}{v} = \frac{aTs + 1}{Ts + 1} \tag{C.1}$$

where v^s is the shifted signal and v is the original signal.

The lead and lag is determined based on the value of a. Equation (C.1) could be rewritten as:

$$(Ts + 1)v^s = (aTs + 1)v \tag{C.2}$$

Replacing the laplace differential operator s by its time domain operator yields:

$$T\frac{dv^s}{dt} + v^s = aT\frac{dv}{dt} + v \tag{C.3}$$

The numerical Euler backward integration method states that the differential parameters could be placed by:

$$\frac{dv}{dt} = \frac{v_k - v_{k-1}}{T_s} \tag{C.4}$$

where T_s is the sampling time. Applying (C.4) in (C.3) gives:

$$T\frac{v_k^s - v_{k-1}^s}{T_s} + v_k^s = aT\frac{v_k - v_{k-1}}{T_s} + v_k \tag{C.5}$$

Replacing $\frac{T}{T_S}$ by ϵ and rearranging for v_k^s gives:

$$v_k^s = \frac{v_k[1 + a\epsilon] - a\epsilon v_{k-1} + \epsilon v_{k-1}^s}{1 + \epsilon} \tag{C.6}$$

or simply as:

$$v_k^+ = d_1 v_k + d_2 v_{k-1} + d_3 v_{k-1}^+ \tag{C.7}$$

where:

$$d_1 = \frac{a_d\epsilon + 1}{\epsilon + 1}$$

$$d_2 = -\frac{a_d\epsilon}{\epsilon + 1} \tag{C.8}$$

$$d_3 = \frac{\epsilon}{\epsilon + 1}$$

and

$$v_k^- = g_1 v_k + g_2 v_{k-1} + g_3 v_{k-1}^- \tag{C.9}$$

where:

$$g_1 = \frac{a_g\epsilon + 1}{\epsilon + 1}$$

$$g_2 = -\frac{a_g\epsilon}{\epsilon + 1} \tag{C.10}$$

$$g_3 = \frac{\epsilon}{\epsilon + 1}$$

Appendix D

Derivation of $\ddot{e}$ for SMC

The rectifier circuit can be described in $dq0$-reference frame as

$$[\dot{i}] = z_1[i] + b_1 m + w_1 \tag{D.1}$$

where

$$z_1 = \begin{bmatrix} -R_f/x_f & 1 \\ -1 & -R_f/x_f \end{bmatrix} \tag{D.2}$$

$$b_1 = \frac{1}{x_f} \begin{bmatrix} kV_{dc}cos(\phi) \\ kV_{dc}sin(\phi) \end{bmatrix} \tag{D.3}$$

$$w_1 = \frac{1}{x_f} \begin{bmatrix} V_{pcc}^d \\ 0 \end{bmatrix} \tag{D.4}$$

$$[i] = \begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{D.5}$$

x_f and r_f are the filter inductance and resistance respectively,

i_d and i_q are the direct and quadrature components of the rectifier current.

Differentiating (D.1) yields

$$\dddot{[i]} = z_1\ddot{[i]} \tag{D.6}$$

Substituting with $\dot{i}$ from (D.1) gives

$$\ddot{[i]} = z_1(z_1[i] + b_1 m + w_1) \tag{D.7}$$

But;

$$\begin{aligned} \ddot{v}_{pcc}^{d} &= R_f \ddot{i_d} - x_f \ddot{i_q} \\ &= [R_f \quad -x_f]\ddot{[i]} \\ &= z_2\ddot{[i]} \end{aligned} \tag{D.8}$$

Combining (D.8) and (D.7) gives

$$\ddot{v}_{pcc}^{d} = z_2 z_1(z_1[i] + b_1 m + w_1) \tag{D.9}$$

or simply

$$\ddot{v}_{pcc}^{d} = F + Gm \tag{D.10}$$

where $F = z_2 z_1(z_1[i] + w_1)$ and $G = z_2 z_1 b_1$.

Since the reference value is a constant, it will disappear from the the first and second derivative of error signal. Therefore, the second derivative if the error signal is given as

$$\begin{aligned} \ddot{e} &= \ddot{v}_{pcc}^{d} \\ &= F + Gm \end{aligned} \tag{D.11}$$

Appendix E

Connectivity and Co-connectivity Matrices of case (1)

$$\mathbf{A} = \left(\begin{array}{c|cccccc} \frac{PQIN}{SV} & \#1 & \#2 & \#3 & \#4 & \#5 & \#6 \\ \hline v_1 & 1 & 1 & 0 & 0 & 0 & 1 \\ v_2 & 1 & 1 & 1 & 0 & 0 & 1 \\ v_3 & 0 & 1 & 1 & 1 & 1 & 0 \\ v_4 & 0 & 0 & 1 & 1 & 1 & 0 \\ v_5 & 0 & 0 & 1 & 1 & 1 & 1 \\ v_6 & 1 & 1 & 0 & 0 & 1 & 1 \\ i_{12} & 1 & 1 & 0 & 0 & 0 & 0 \\ i_{23} & 0 & 1 & 1 & 0 & 0 & 0 \\ i_{34} & 0 & 0 & 1 & 1 & 0 & 0 \\ i_{45} & 0 & 0 & 0 & 1 & 1 & 0 \\ i_{56} & 0 & 0 & 0 & 0 & 1 & 1 \\ i_{61} & 1 & 0 & 0 & 0 & 0 & 1 \\ i_{62} & 0 & 1 & 0 & 0 & 0 & 1 \\ i_{53} & 0 & 0 & 1 & 0 & 1 & 0 \end{array}\right) \tag{E.1}$$

$$\mathbf{B_j} = \left(\begin{array}{c|cccccc} \frac{PQIN}{SV} & \#1 & \#2 & \#3 & \#4 & \#5 & \#6 \\ \hline v_1 & 0 & 0 & 0 & 0 & 0 & 0 \\ v_2 & 0 & 0 & 0 & 0 & 0 & 0 \\ v_3 & 0 & 0 & 0 & 0 & 0 & 0 \\ v_4 & 0 & 0 & 0 & 0 & 0 & 0 \\ v_5 & 0 & 0 & 0 & 0 & 0 & 0 \\ v_6 & 0 & 0 & 0 & 0 & 0 & 0 \\ i_{12} & 1 & 1 & 0 & 0 & 0 & 1 \\ i_{23} & 1 & 1 & 1 & 0 & 0 & 1 \\ i_{34} & 0 & 1 & 1 & 1 & 1 & 0 \\ i_{45} & 0 & 0 & 1 & 1 & 1 & 0 \\ i_{56} & 0 & 0 & 1 & 1 & 1 & 1 \\ i_{61} & 1 & 1 & 0 & 0 & 1 & 1 \\ i_{62} & 1 & 1 & 0 & 0 & 1 & 1 \\ i_{53} & 0 & 0 & 1 & 1 & 1 & 1 \end{array}\right) \tag{E.2}$$

$$\mathbf{B_k} = \left(\begin{array}{c|cccccc} \frac{PQIN}{SV} & \#1 & \#2 & \#3 & \#4 & \#5 & \#6 \\ \hline v_1 & 0 & 0 & 0 & 0 & 0 & 0 \\ v_2 & 0 & 0 & 0 & 0 & 0 & 0 \\ v_3 & 0 & 0 & 0 & 0 & 0 & 0 \\ v_4 & 0 & 0 & 0 & 0 & 0 & 0 \\ v_5 & 0 & 0 & 0 & 0 & 0 & 0 \\ v_6 & 0 & 0 & 0 & 0 & 0 & 0 \\ i_{12} & 1 & 1 & 1 & 0 & 0 & 1 \\ i_{23} & 0 & 1 & 1 & 1 & 1 & 0 \\ i_{34} & 0 & 0 & 1 & 1 & 1 & 0 \\ i_{45} & 0 & 0 & 1 & 1 & 1 & 1 \\ i_{56} & 1 & 1 & 0 & 0 & 1 & 1 \\ i_{61} & 1 & 1 & 0 & 0 & 0 & 1 \\ i_{62} & 1 & 1 & 1 & 0 & 0 & 1 \\ i_{53} & 0 & 1 & 1 & 1 & 1 & 0 \end{array}\right) \tag{E.3}$$

$SV = State\ Variables$

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