Pixel Circuits and Driving Schemes for Active-Matrix Organic Light-Emitting Diode Displays

by

Shahin Jafarabadiashtiani

A thesis
presented to the University of Waterloo
in fulfilment of the
thesis requirement for the degree of
Doctor in Philosophy
in
Electrical and Computer Engineering

Waterloo, Ontario, Canada, 2007

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

Shahin Jafarabadiashtiani

I understand that my thesis may be made electronically available to the public.

Shahin Jafarabadiashtiani

Abstract

Rapid progress over the last decade on thin film transistor (TFT) active matrix organic light emitting (AMOLED) displays led to the emergence of high-performance, low-power, low-cost flat panel displays. Despite the shortcomings of the active matrix that are associated with the instability and low mobility of TFTs, the amorphous silicon TFT technology still remains the primary solution for the AMOLED backplane. To take advantage of this technology, it is crucial to develop driving schemes and circuit techniques to compensate for the limitations of the TFTs.

The driving schemes proposed in this thesis address these challenges, in which, the sensitivity of the OLED current to the transistor variations is reduced significantly. This is achieved by comparing the data signal with a feedback signal associated with the pixel current by means of an external driving circuit through a column feedback line. Depending on the nature of the feedback signal, (i.e. current or voltage) several pixel circuits and external drivers are proposed.

New AMOLED pixel circuits with voltage and current feedback are designed, simulated, fabricated, and tested. The performance of these circuits is analyzed in terms of their stability, settling time, power efficiency, noise, and temperature-dependence. For the pixel circuits with current feedback, an operational transresistance amplifier is designed and implemented in a high-voltage CMOS process. Measurement results for both voltage and current feedback driving schemes indicate less than a 2%/V sensitivity to shifts in the threshold voltage of the TFTs. By using current feedback and an accelerating pulse, programming times less than 50 s are achieved.

Acknowledgment

I would like to thank my supervisor, Professor Arokia Nathan for his valuable encouragements, guidance, support, and wonderful discussions during the course of my studies. Also, I want to express my gratitude to the members of my PhD committee: Prof. Gehan Amaratunga, Prof. Adel Sedra, Prof. James Martin, Prof. Manoj Sachdev, and Professor Sherman Shen for reading my thesis and for our discussions.

This work would not have been possible without the support of many other individuals at the Giga-to-Nano Lab. at the University of Waterloo. In particular, I would like to thank Dr. Denis Striakhilev for fabrication of the TFT circuits and Prof. Servati for providing me with a circuit-level model for simulation amorphous silicon TFTs. I am also thankful to my friend Reza Chaji for our insightful discussions. Many thanks to Dr. Sheng-Tao, Dr. Yuri Vigranenko, Dr. Mahdi Farrokh-Baroughi, Stephan Alexander, Majid gharghi, Mohammad Reza Esmaeili, Nader Safavian, Jeff Chang, and other members of Giga-to-Nano Lab for their support.

I want to acknowledge the support of the Natural Sciences and Engineering Research Council (NSERC) of Canada, Ontario Graduate Scholarship (OGS), University of Waterloo, and IGNIS Innovation Inc. for financial support.

I am particularly grateful to my wife, Pardis, for her patience, support, and love, during all happy and sad moments we share in our life. I am deeply grateful to my parents, Manour Jafarabadi Ashtiani and Mahindokht Delpasand Moghadam for their continuous love and support during my lifetime.

To my parents and my wife

Contents

List of Tables

List of Figures

Notation

A	amplifier gain
A_{OLED}	OLED area
A_{PD}	photodiode area
Ar	aperture ratio
A_{VT}	mismatch constant of threshold voltage
A_{β}	mismatch constant of transconductance
C_i	gate dielectric capacitance
C_{ov}	gate-drain overlap capacitance
C_{PD}	parasitic capacitance of data line
C_{PF}	parasitic capacitance of feedback line
E_a	activation energy
E_c, E_v	(conduction, valence) band edge
E_{dc}	slope of distribution of acceptor-like deep states
E_{dv}	slope of distribution of donor-like deep states
Er	settling error
E_{tc}	slope of distribution of acceptor-like tail states
E_{tv}	slope of distribution of donor-like tail states
f	frequency
g_{dc}	density of acceptor-like deep states at E_C
g_{dv}	density of donor-like deep states at E_V
g_m	small-signal transconductance
g_{tc}	density of acceptor-like tail states at E_C
g_{tv}	density of donor-like tail states at E_V
i_n	noise current
I_P	amplitude of accelerating pulse
I_{PROG}	programming current

k	Boltzman's constant (1.380662 x 10^{-23} J/K)
K	fitting coefficient of OLED
K	transconductance coefficient of TFTs
L	TFT length
$L(s)$	loop gain
L_{av}	average luminance of display
L_{ov}	gate-drain overlap
M	number of columns
N	number of rows
n_{free}	number of free electrons
N_i	number of interconnect lines in display
n_{ind}	number of induced electrons
n_{trap}	number of trapped electrons
q	elementary charge (1.6021892 x 10^{-19} C)
r_{ds}	small-signal drain-source resistance
R_F	feedback resistor
R_M	tansresistance
t	layer thickness
T	temperature
t_p	width of accelerating pulse
V_{DD}	supply voltage
V_{OLED}	OLED voltage
V_{sat}	saturation voltage of TFT
V_T	threshold voltage
W	TFT width
W_m	width of interconnections
W_p	spacing between interconnect lines
X_{pix}	length of OLED pixel
Y_{pix}	width of OLED pixel
ΔV_T	V_T shift
α	power factor of a-Si TFTs
β	charge injection factor
β	feedback gain

β	power factor of V_T shift
β_{th}	thermal noise coefficient (1 for triode, 2/3 for saturation)
η_{OLED}	efficiency of OLED
η_P	efficiency of OLED pixel circuit
η_{PD}	efficiency of photodiode
λ	channel length modulation parameter
μ_{FET}	field effect mobility
μ_n	electron mobility
ρ	resistivity
$\sigma(V_T)$	variance of mismatch in threshold voltage
$\sigma(V_T)$	variance of mismatch in transconductance
ω_p	dominant pole of amplifier

List of Abbreviations

AMLCD	active-matrix liquid crystal display
AMOLED	Active-matrix organic light emitting diode (display)
a-Si	amorphous silicon
BCE	back channel etch
CCII	second generation current conveyor
CPPC	current-programmed pixel circuit
DIP	dual inline package
ELM	electroluminescent layer
ETL	electron transport layer
HOMO	highest occupied molecular orbital
HTL	hole transport layer
ITO	Indium-Tin-Oxide
LCD	liquid crystal display
LUMO	lowest unoccupied molecular orbital
OLED	organic light emitting diode
OTA	operational transconductance amplifier
OTRA	operational transresistance amplifier
PCB	printed circuit board
PECVD	plasma-enhanced chemical vapor deposition
PLED	polymer light emitting diode
PMOLED	Passive-matrix organic light emitting diode (display)
QVGA	quarter video graphic array
SMU	source-meter unit
TFT	thin-film transistor
VPPC	voltage-programmed pixel circuit

Chapter 1
Introduction

Rapid advancements in the past decade in organic light-emitting diodes (OLEDs) have led to the emergence of a new generation of high-performance, low-power, low-cost flat panel displays. Compared with the ubiquitous liquid crystal displays (LCDs), the OLED display offers a larger viewing angle (>160^{o}), faster response time, higher contrast, lighter weight, lower power consumption, and lower cost [1]-[3]. Moreover, OLED displays can be fabricated on plastic substrates at low deposition temperatures for mechanical flexibility [4]. Since the invention of the small-molecule OLED in 1987 [5], and large-molecule OLED (PLED) in 1990 [6], researchers have focused on overcoming the technical challenges of OLED technology that involve encapsulation, lifetime, yield, colour efficiency, and drive electronics. OLEDs have already taken a share in the market for small displays, and are expected to grow into the large display market in the near future. Fig 1.1 depicts the present and expected OLED market for displays [7]. It is evident that a rapid

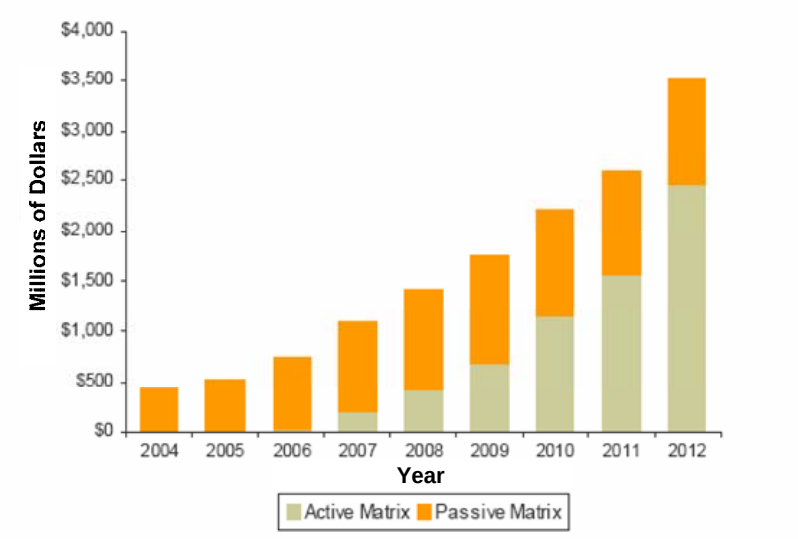


Figure 1.1: Present and expected OLED market. After [7]

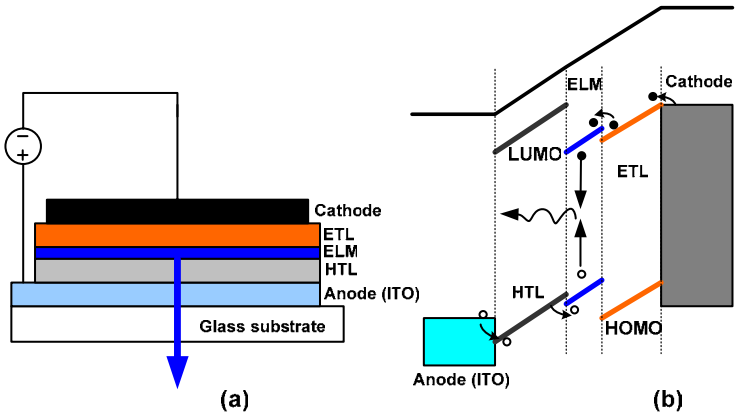


Figure 1.2: (a) Structure of an OLED, (b) Associated energy bands.

growth in excess of 300% is expected between 2007 and 2012. In addition to flat panel displays, OLED are becoming a serious competitor in the solid-state lighting market [8].

1.1 OLED Device

An OLED is a light-emitting device that consists of layers of organic materials, sandwiched between two electrodes. Fig. 1.2 (a) represents a typical OLED. It consists of an electron-injecting cathode, a transparent anode, an electron transporting layer (ETL), a hole transporting tayer (HTL), and a light-emitting organic layer (ELM). When the OLED is in forward bias, some of the injected electrons and holes recombine in the ELM and generate photons. The wavelength of the emitted light is determined by the bandgap of organic material, which is the difference in energy between the highest occupied molecular orbital (HOMO), and the lowest unoccupied molecular orbital (LUMO). Fig. 1.2 (b) shows the energy band diagram of an OLED. The anode terminal is composed of a transparent conductor with a high work function, such as indium-tin-oxide (ITO). The cathode terminal is fabricated from a metal that has a low work function, to facilitate the injection of electrons into the organic layer. The HTL and ETL increase the quantum efficiency of the OLED by reducing the potential barriers between the anode and cathode and EML for the holes and electrons, respectively.

Table 1.1 Lifetime of state-of-the-art OLEDs [14].

Colour	Lifetime (h)
Green	40000 at 500cd/m^2
Red	100000 at 500 cd/m^2
Blue	10000 at 500 cd/ m^2

Two types of electroluminescent materials are used in OLEDs: the small-molecule, and the large molecule. The electroluminescence performance of the two types is comparable. The principal difference is in the fabrication process. Small-molecule OLEDs are fabricated by vapor deposition and the patterning is achieved by using shadow masks [9]. On the other hand, large molecule OLEDs are solution-processed, and deposition and patterning are accomplished by different methods such as inkjet printing or screen printing [10][11]. The efficiency of OLED devices is described by its external quantum efficiency, current efficiency in cd/A, and power efficiency in lm/W. For the OLED pixel designs, the current efficiency in cd/A is normally used.

The key disadvantage of the OLED is its limited lifetime. The luminance of OLED devices degrades overtime. The degradation not only reduces the display luminance, but also shifts its emission colour whereby the degradation rates for red, green, and blue OLEDs are different. The degradation manifest itself in the formation of dark spots, stemming from destruction of the OLED materials by oxygen and humidity, and can be prevented by effectively encapsulating the device [12]. In addition, there is intrinsic degradation which is not well understood. However, it is believed to arise from charge trapping in the organic layers [13]. Table 1.1 lists the typical lifetimes of the state-of-the-art polymer OLEDs in 2006 [14]. It is evident that the lifetime of the blue OLEDs is much shorter than that of the green or red. The short lifetime of the blue OLED is posing a major challenge in the industry.

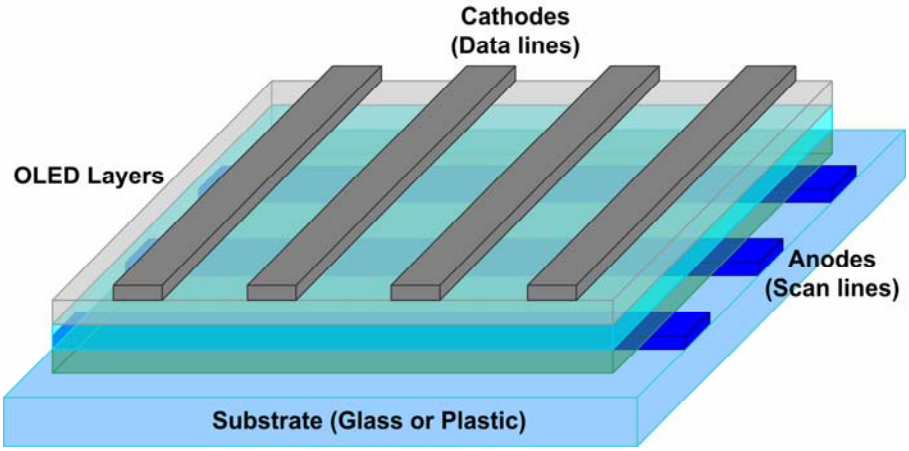


Figure 1.3: Simple sketch of a monochrome PMOLED display.

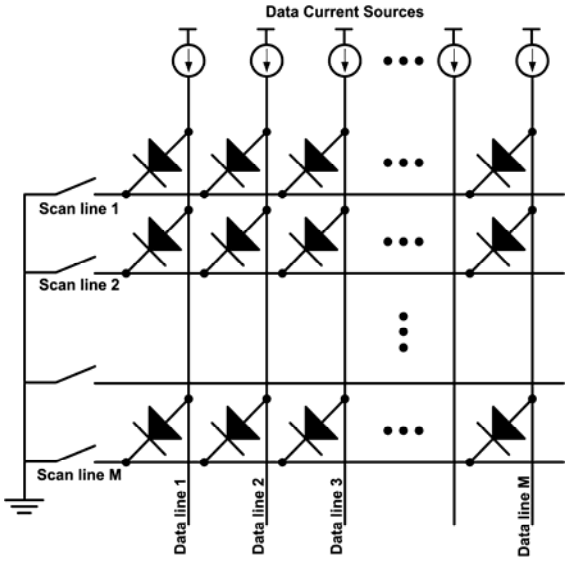


Figure 1.4: Equivalent circuit model of a PMOLED display.

1.2 Passive-Matrix OLED Display (PMOLED)

Passive-matrix OLED (PMOLED) displays consist of an array of OLEDs, whose cathode and anode terminals are connected to two sets of electrically-isolated orthogonal row and column lines. Fig. 1.3 illustrates a monochrome PMOLED display with the row and column lines. Fig. 1.4 provides an equivalent schematic of a PMOLED display and the control signals. The column lines, also called data lines, are connected to the off-panel data current sources. The row lines, also called select lines,

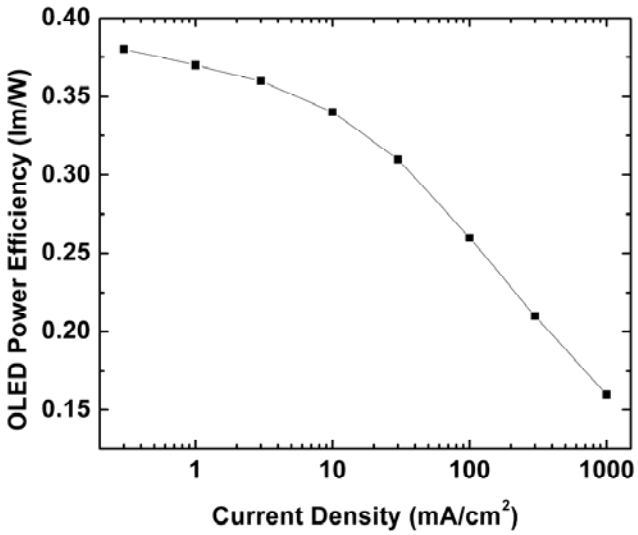


Figure 1.5: Typical OLED power efficiency versus current density. Adapted from [13]

are connected to the select switches. The array is addressed one row-at-a time. When a row line is selected, the associated select switch is ON. The OLEDs in the row are then driven by the current sources to the appropriate levels. Since there is no circuit to store the current, the OLEDs are turned off when the row is deselected. As a result, for an average luminance of L_{av}, the OLED needs to be driven to an instant illumination (L_{inst}) of

$$L_{inst} = \frac{ML_{av}}{Ar}, \tag{1.1}$$

where M is the number of rows, and Ar the aperture ratio of the pixel. Although the fabrication and drive scheme of PMOLED displays are easier than the active-matrix counterpart, PMOLED displays are not suitable for high-resolution large-size displays due to the lower efficiency.

For large PMOLED displays, the required instant luminance, and therefore, the programming current is high. However, the power efficiency of the OLEDs drops drastically for large current densities, as shown in Fig. 1.5 [15]. As a result, PMOLED displays cannot take advantage of the high OLED efficiency. Moreover, due to the high electrical stressing, PMOLED display degrades rapidly.

Another drawback of PMOLED displays is their low contrast ratio. When a row is selected, other reverse-biased OLEDs form branches that sink the current from the data current sources. The maximum leakage current (I_{Lmax}) should be smaller than the minimum OLED current (I_{Omin}). The maximum leakage current occurs when only one OLED in the selected row is ON. If the voltage drop of the ON OLED is much larger than the voltage drop of the reverse-biased OLEDs, then I_{Lmax} for a display with a resolution of M by N is given by [1]

$$I_{L\max} = (M-1)(N-1)I(V_{O\max} - 2V_{ON}). \tag{1.2}$$

Here, I(V_{Omax}-2V_{ON}) is the OLED current when the OLED voltage is ON, V_{ON} is the ON voltage of the OLED, and V_{Omax} is the OLED voltage for the largest gray scale. Obviously, I_{Lmax} is proportional to the number of rows and columns of the display. Based on the calculations presented in [1], for a typical OLED technology, the total number for pixels in a PMOLED should be smaller than 10,000, which is much less than the number of pixels required for a high information content display.

1.3 Active-Matrix OLED Display

In an AMOLED display, the pixels store the luminance data. Thus, the OLEDs are always ON. Therefore, the OLEDs are programmed with currents much smaller than those in PMOLED displays, resulting in higher efficiency operation and longer lifetime. Fig. 1.6 offers a simple block diagram of an AMOLED display. It consists of an array of pixels, a column driver, and a gate driver. When a pixel is selected by the gate driver, the data associated with the pixel luminance is stored and remains in the pixel until the next programming cycle. Since the OLED is a current-driven device, each AMOLED pixel requires a circuit to store the luminance data and to drive the OLED by current. This implies that the pixel circuit should have both switching and current-driving components.

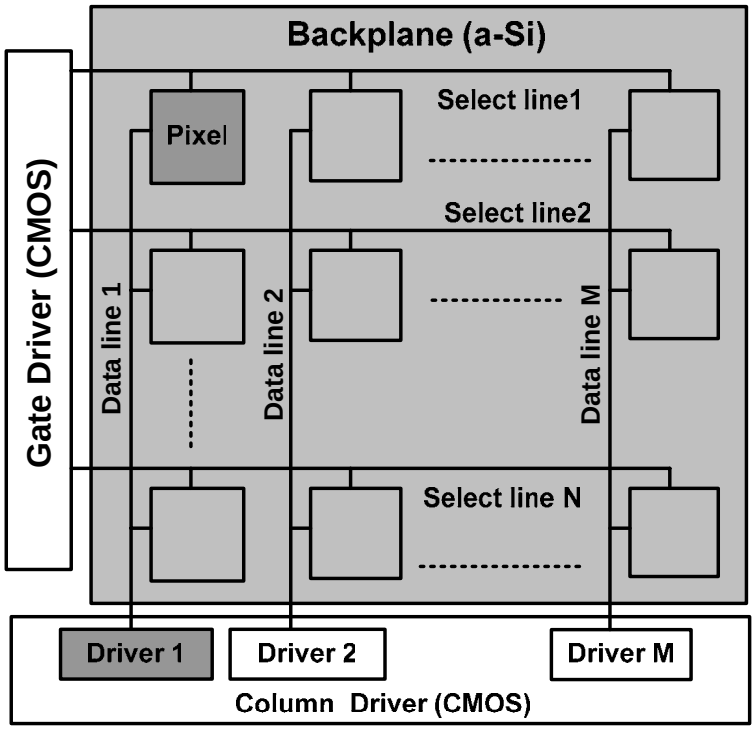


Figure 1.6: Block diagram of an AMOLED display.

Fig. 1.7 shows the simplest method of implementing an AMOLED pixel circuit. This circuit, referred as a 2-TFT pixel in the literature, consists of a driving TFT (T1), a switching TFT (T2), a storage capacitor (C_S), and an OLED. During the programming time, T2 is turned on by the select line and a voltage related to the luminance data is stored in C_S. During the hold (or frame) time, T2 is switched off, but T1 drives the OLED with a current until the next programming cycle.

In an AMOLED display, the pixel circuits are fabricated on glass or plastic substrates. The OLEDs can then be juxtaposed with the pixels in a coplanar bottom-emission structure or stacked above the circuits in a top-emission structure as shown in Fig. 1.8 and Fig 1.9, respectively.

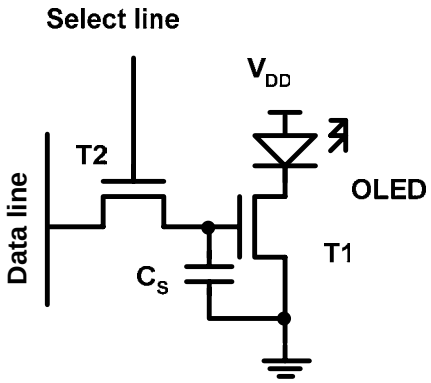


Figure 1.7: 2-TFT AMOLED pixel circuit.

The pixel circuits can be fabricated in different thin film transistor (TFT) technologies such as amorphous silicon (a-Si) or low-temperature poly silicon (LTPS). In the LTPS technology, silicon layers are deposited in the form of amorphous silicon at a low temperature, and then converted to polysilicon by laser annealing. LTPS TFTs have a field-effect mobility as high as 100 $cm^2V^{-1}s^{-1}$ which is ample for driving OLEDs. Moreover, their I-V characteristics are stable and do not change under gate bias stress. However, the LTPS technology has a high fabrication cost and low yield. Also, LTPS TFTs are prone to a high level of non-uniformity, particularly with the threshold voltage, due to uneven crystallization during laser annealing [16].

In the a-Si technology, the silicon active layer, the gate dielectric, and metal layers are deposited at temperatures below 350 ^{O}C to form the TFTs. Due to the relatively low process temperature, the deposited silicon and insulator layers are amorphous. Thus a-Si TFTs demonstrate a typical field-effect mobility, close to 1 $cm^2V^{-1}s^{-1}$ which is much smaller than that in LTPS TFTs. However, studies show that this level of mobility is enough to drive the currently-available OLEDs in most of the AMOLED display applications [17]. Amorphous silicon TFT technology is the dominant technology for AMLCD backplanes, and it has well-established infrastructure and low fabrication cost. Therefore, it is becoming the primary solution for fabrication of AMOLED backplanes [18].

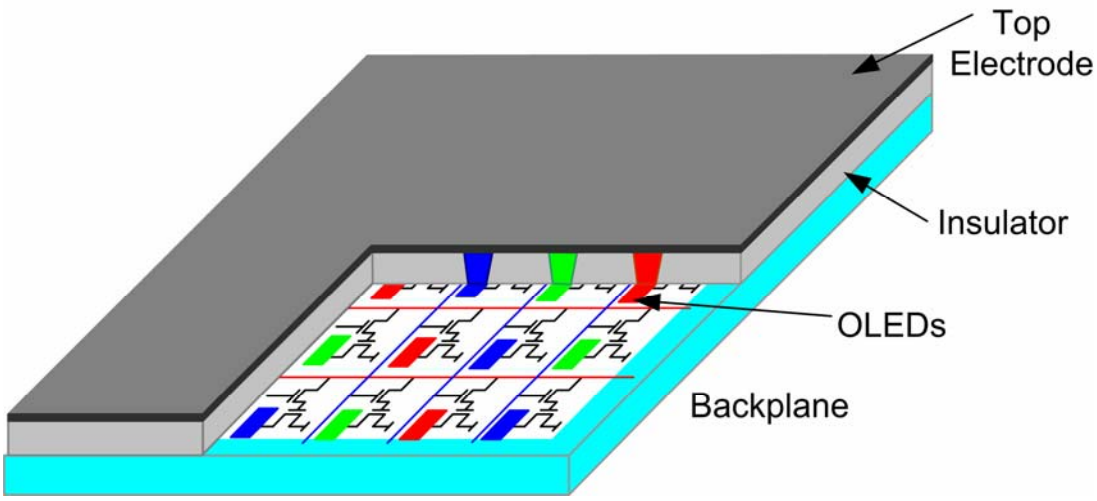


Figure 1.8: Typical implementation of a bottom-emitting AMOLED.

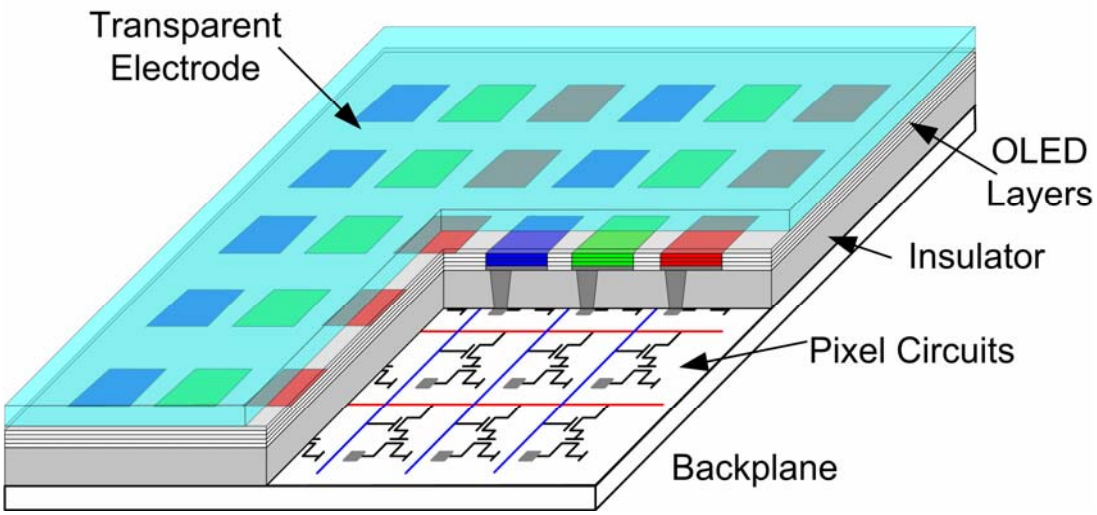


Figure 1.9: Typical implementation of a top-emitting AMOLED.

The main drawback of a-Si TFTs is the instability. When a voltage is applied to the gate-source terminals of an a-Si TFT, its threshold voltage (V_T) shifts [18]. The V_T shift in uncompensated pixel circuits such as the 2-TFT pixel, causes degradation in the OLED current over time. This not only degrades the display luminance, but also causes “image sticking” in monitors and cell phone displays that show static images.

1.4 Goal of the Thesis

Despite the maturity and low fabrication cost of a-Si TFT technology, the instability of a-Si TFTs is the primary barrier to their widespread use in AMOLED backplanes. The goal of the work, described in this thesis is to find reliable and low-cost driving schemes and AMOLED pixel circuits to compensate for the shortcomings of the existing a-Si TFTs, in particular instability, and to provide the OLED with a stable and predictable current. The thesis project includes both design of pixel circuits with a-Si TFTs and the external column drivers in a high-voltage CMOS technology. The integrated pixel-driving solution should reduce the sensitivity of the OLED current to the variations in TFT parameters, meet the programming time requirements of high-resolution displays, and result in simple pixel circuits and drivers.

Since the a-Si TFT is not a well-known device for circuit designers, an understanding of the device operation and its specific characteristics is essential. In Chapter 2, following introducing of the a-Si TFT device, different aspects of design of AMOLED pixel circuits with the a-Si TFTs are investigated along with design issues, concerning the OLED device and its integration with the structure of the pixel circuits.

Chapter 3 is a review of the state-of-the-art driving schemes, such as current and voltage driving, optical feedback, and time-based gray scaling for AMOLED displays. Because current driving is the first and most-discussed compensating scheme, it is investigated in more detail. Here, the stability and settling time of such a scheme are analyzed quantitatively for the first time.

A new driving scheme based on voltage feedback is presented in Chapter 4. The circuit performance, in terms of stability, settling time, temperature-dependence, and noise are closely examined together with measurement results from fabricated pixel circuits.

In Chapter 5, a new driving scheme based on current feedback is presented. The driving scheme utilizes a CMOS transresistance amplifier as an external column driver and an accelerating pulse at

low programming currents to achieve a fast current settling. After the analysis of the new driving scheme, measurement results of the fabricated CMOS transresistance amplifier and a-Si TFT pixels are discussed. Finally, Chapter 6 summarizes the contributions stemming from this research and provides suggestions for future research in this area.

Chapter 2
AMOLED Pixel Design Using a-Si TFTs

In this chapter different aspects of the design of AMOLED pixel circuits using a-Si TFTs are described. Unlike MOSFET, a-Si TFTs are not well-known to circuit designers. Therefore, the operation and modeling of a-Si TFTs are focused on. Subsequently, the specific issues of designing AMOLED pixel circuits with a-Si TFT are discussed. The conventional 2-TFT pixel circuit described in Chapter 1 is adopted as the standard AMOLED pixel circuit model to investigate how the limitations of a-Si TFTs affect AMOLED pixel circuit performance, including instability, settling time, temperature-dependence, power consumption, and noise.

The OLED characteristics are studied from the circuit-design perspective. The purpose of this part is mainly to study the limitations imposed by the OLED process and integration, to the selection of an appropriate AMOLED pixel circuit.

2.1 Amorphous Silicon TFT

a-Si TFTs can be fabricated by various techniques. There are four configurations for the fabrication of TFTs, based on the order of the different layers [19]. A simplified schematic of these four configurations is exhibited in Fig. 2.1. In the staggered configurations (Fig 2.1 (a) and (b)), the gate is not on the same side of the drain and source terminals, whereas in the coplanar configurations (Fig 2.1 (c) and (d)), the gate, source, and drain terminals are on the same side. In the inverted configurations, gate terminal is deposited before the gate dielectric and a-Si layers. In the top-gate configurations, the gate terminal is on the top of the a-Si layer. Most state-of-the-art a-Si TFTs are fabricated based on the inverted-staggered configuration in Fig. 2.1 (b). The main device layers of an a-Si TFT are the gate metal layer, gate dielectric layer, a-Si layer, n+ contact layer, and top-metal layer.

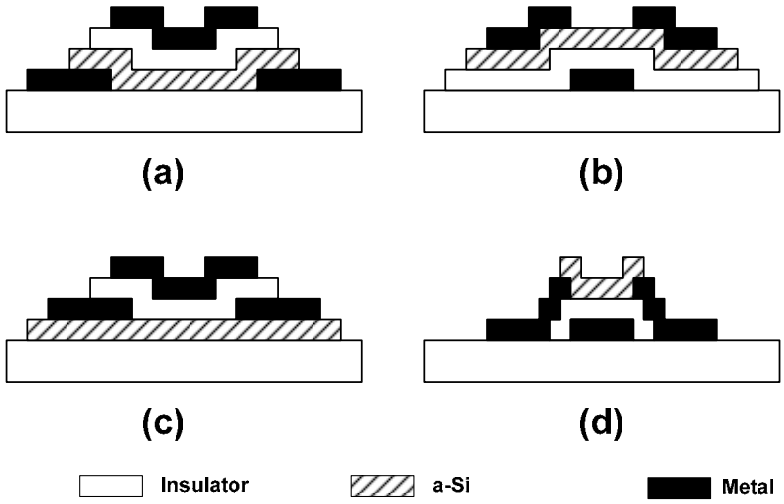


Figure 2.1: Four possible configurations of a-Si TFTs: (a) staggered, (b) inverted staggered, (c) coplanar, (d) inverted coplanar.

Typically, inverted staggered TFTs have two structures: the tri-layer and the back-channel etched (BCE). Fig. 2.2 reflects the schematics of these structures. The tri-layer TFT in Fig 2.2 (a) has three layers of amorphous silicon nitride. One of the layers is used as the gate dielectric, and the other two layers are employed to define the source and drain contacts, and to passivate the a-Si layer. In the BCE TFT in Fig 2.2 (b), the top surface of the a-Si layer is not passivated. A typical tri-layer TFT has 5 masks whereas a BCE TFT has 4 masks. Since a BCE TFT does not have a passivating layer on top of the a-Si, it has a higher reverse current and thus a smaller ON/OFF ratio due to the formation of a back channel [20] [21]. A tri-layer TFT has a lower reverse current and a better ON/OFF ratio due to the passivation. In the LCD industry, BCE TFTs are popular because of the fewer fabrication steps and lower device complexity. Since an in-house mature wet-etched tri-layer TFT process [22] with its device model is available, all of the designs and device parameters in this thesis are based on the tri-layer TFT devices.

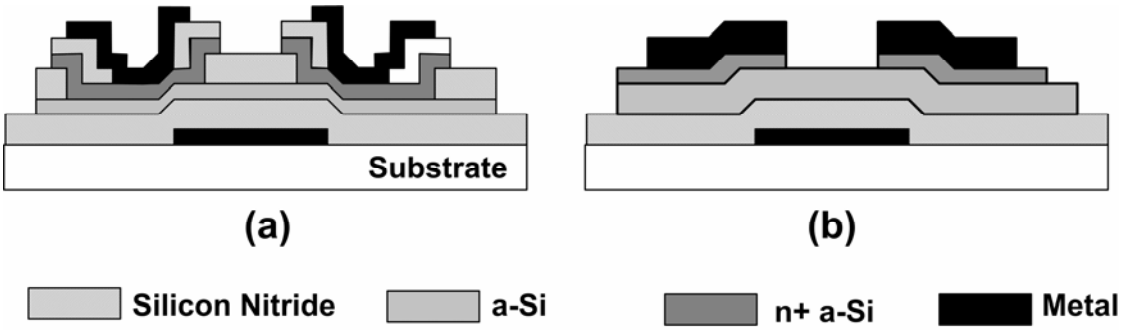


Figure 2.2: Inverted-staggered TFT structures: (a) tri-layer, (b) back-channel etched (BCE).

Table 2.1: Typical thickness of different layers in a tri-layer a-Si TFT.

Layer	Thickness (nm)
Gate metal	130
a-Si	50
a-SiN_X insulator	250
N+ microcrystalline silicon	30
Al drain/source	500

a-Si, silicon nitride, and n+ microcrystalline layers are deposited by plasma-enhanced chemical vapor deposition (PECVD). The gate, and drain/source metals are deposited by sputtering. The gate metal material is Cr. or Mo. The typical thicknesses of the layers are listed in Table 2.1 [23].

2.1.1 Operation of the a-Si TFT

a-Si TFT is an accumulation-mode field-effect transistor. The conduction of the electrons and holes in an a-Si TFT is primarily affected by the density of states. In contrast to crystalline silicon, a-Si is a disordered material. The short-range order in a-Si is similar to that in crystalline silicon and thus, it has a bandgap [24]. However, due to the lack of a long-range order, the conduction and valence bands in a-Si do not have abrupt band edges, but broadened tail states that continue into the forbidden band. Fig. 2.3 is a qualitative sketch of the density of states in intrinsic a-Si. As can be seen, the tail of the

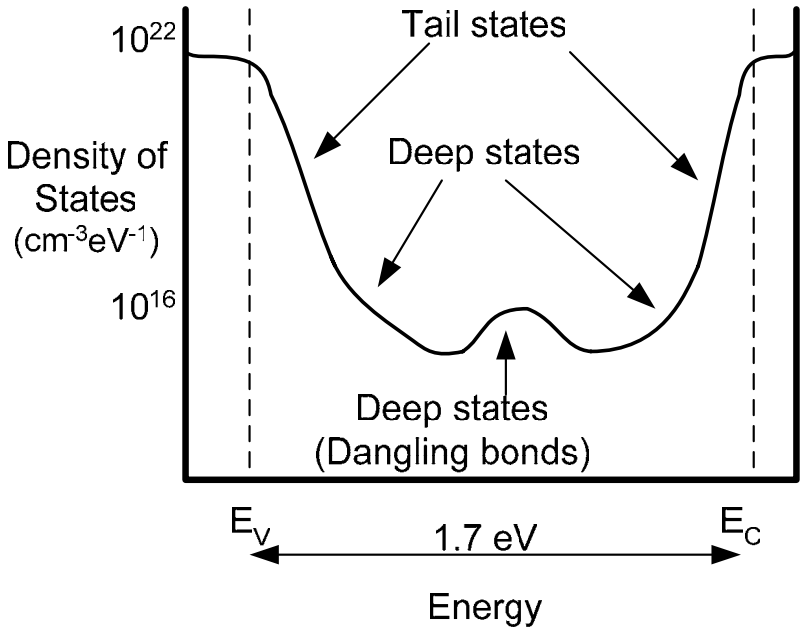


Figure 2.3: Density of states in amorphous silicon.

valence band is broader. The tail states close to the conduction band behave like acceptor states, and are called acceptor-like states. The tail states close to the valence band are also known as donor-like states. In addition to the tail states, a-Si has localized deep states that are placed between 0.6 eV to 1.4 eV above the valence band. It is believed that these states are principally created silicon dangling bonds. The density of the deep states depends on the deposition conditions and the concentration of hydrogen, and is in the order of 10^{15} to 10^{17} in electronic-grade a-Si [24].

The large number of tail states near the conduction band and the valence band is the primary reason for the low mobility of the electrons and holes in a-Si because of the frequent trapping of them. In a-Si, the number of trapped electrons in the tail states is much larger than the number of free electrons. Accordingly, the field effect mobility (μ_{FET}) of the electrons in a-Si TFTs is defined as

$$\mu_{FET} = \mu_n \frac{n_{free}}{n_{trap} + n_{free}}, \tag{2.1}$$

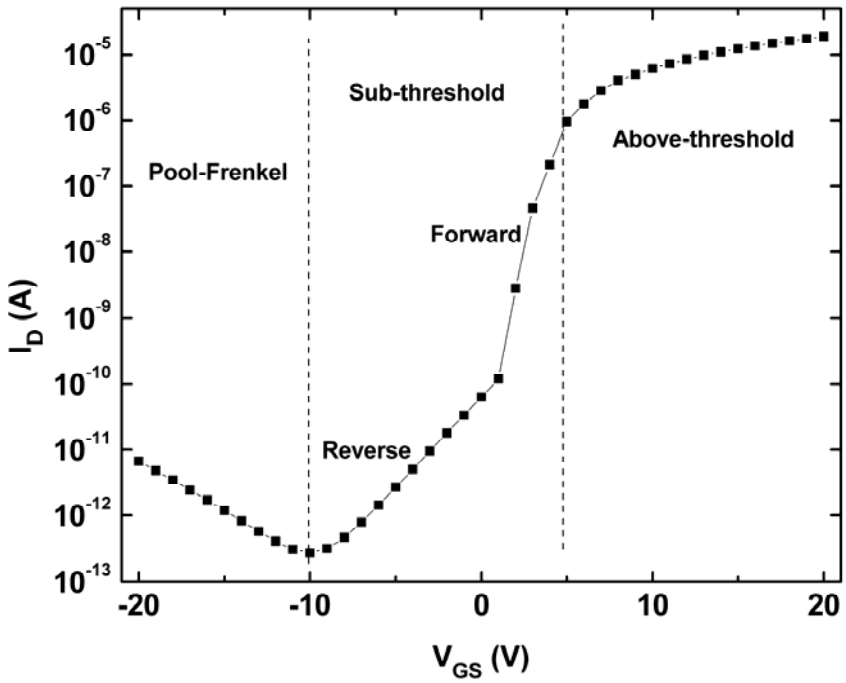


Figure 2.4: Typical I-V characteristic of an a-Si TFT.

where μ_n is the electron band mobility, n_{free} is the number of electrons, and n_{trap} is the number of trapped electrons in the band tail states [19]. Fig. 2.4 shows the drain-source current of an a-Si TFT as a function of the gate-source voltage (V_{GS}). Depending on the V_{GS}, three regions are defined: above threshold, sub-threshold, and Pool-Frenkel emission. For V_{GS}=0, the Fermi level is in the deep states. As the V_{GS} increases in the forward sub-threshold region, the Fermi level moves toward the conduction band and the deep states are filled by electrons. Simultaneously, a small number of electrons in the conduction band tail states participate in the conduction of a small sub-threshold current which is in the range of 10^{-9} to 10^{-12} A. As the V_{GS} increases, the density of the electrons increases and the sub-threshold current increases exponentially. When the V_{GS} rises above the threshold voltage, the number of electrons in the tail states exceeds the number of electrons in the deep states, and the Fermi level enters the conduction band tail. Due to the high density of the tail states, the Fermi level does not move into the conduction band by normal gate-source voltages. The current level in the above-threshold region is in the range of 10^{-7} A/□. For a small negative V_{GS}

(reverse sub-threshold), the Fermi level drops to lower deep states. The electrons in the tail states are depleted by the negative voltage; thus, the channel charge under the gate insulator is negligible. The low conduction in this region is caused by the formation of a back channel at the interface of the a-Si and the passivation layer. For large negative gate-source voltages (Pool-Frenkel emission), the drain current is small but increases exponentially. The conduction in this region is caused by the accumulation of holes in the interface between the a-Si and the gate insulator layers. The holes are generated by the Pool-Frenkel thermoionic emission at the drain-gate overlap region [25].

2.1.2 a-Si TFT Models

Several physical models for a-Si TFTs have been presented [26]-[30]. The focus of these models is the above-threshold and sub-threshold regions. In some newer models, the reverse characteristics of a-Si TFT are considered [25]. Most of the models are derived from similar fundamental assumptions: gradual channel approximation, and a two-part exponential distribution of the density of states in a-Si. The gradual channel approximation yields the following fundamental equations for the drain-source current:

$$I_D = -q\mu_{FET} n_{ind} W \frac{dV(x)}{dx} \tag{2.2}$$

$$n_{ind} = \frac{C_i}{q}\left(V_{gs} - V_{FB} - V(x)\right), \tag{2.3}$$

where n_{ind} is the total number of the induced electrons (both free and trapped electrons), W is the channel width, and V(x) is the channel potential. In the crystalline MOSFET, μ_{FET} is equal to the electron band mobility μ_n, and n_{ind} is equal to the free electrons, n_{free}. In a-Si TFT, a small number of electrons are free and participate in the conduction such that μ_{FET} is much smaller than μ_n. The relationship between μ_{FET} and μ_n is

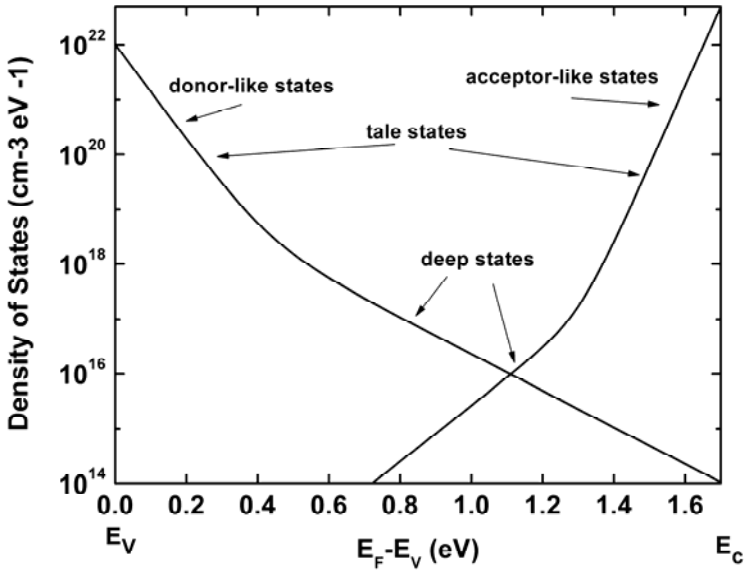


Figure 2.5: Exponential model of the density of states in a-Si. Adapted from [26]

$$\mu_{FET} = \mu_n \frac{n_{free}}{n_{ind}}. \tag{2.4}$$

To derive μ_{FET} from (2.4), the distribution of the density of states in a-Si must be calculated. Experimental results in [26] indicate that the distribution of both donor-like and acceptor like states can be modeled by two-part exponential equations as given by (2.5) and (2.6).

$$g_D(E) = g_{tv} \exp\left(\frac{E_V - E}{E_{tv}}\right) + g_{dv} \exp\left(\frac{E_V - E}{E_{dv}}\right) \tag{2.5}$$

$$g_A(E) = g_{tc} \exp\left(\frac{E - EC}{E_{tc}}\right) + g_{dc} \exp\left(\frac{E - E_C}{E_{dc}}\right) \tag{2.6}$$

Fig. 2.5 illustrates such a model for donor-like and acceptor like states [23].The differences between the a-Si TFT models stem from the way that μ_{FET} is derived from the density of states, and the simplifying assumptions.

Shur et al. have assumed that μ_{FET} is a function of n_{ind} and thus, the gate-source voltage [26]. A semi-analytical detailed model for a-Si TFT, based on numerically solving of the Poisson's equation

has been reported in [31]. Also, a more simplified, empirical model, based on the voltage-dependent mobility assumption has been presented [27] and implemented in AIM-SPICE. In the AIM-SPICE model, μ_{FET} is represented by

$$\mu_{FET} = \mu_n \left(\frac{V_{GS} - V_T}{V_{AA}} \right)^{\gamma}, \tag{2.7}$$

where V_{AA} and γ are process-dependent parameters. The current in the linear region is then given by the following MOSFET-like equations,

$$I_D = \mu_{FET} C_i \frac{W}{L} (V_{GS} - V_T) V_{dse} \tag{2.8}$$

$$V_{dse} = \frac{V_{DS}}{\left[1 + \left(\frac{V_{DS}}{V_{sat}} \right)^m \right]^{\frac{1}{m}}}. \tag{2.9}$$

Khakzar et al. [28] have suggested another analytical model, where the effect of temperature on the current and the density of the surface states are considered. To find an analytical solution for the relationship between the trapped electrons and the channel potential from the Poisson's equation, an exponential relationship is assumed. In the above-threshold region, the drain current in the linear region is given by

$$I_D = \mu_{FET} C_i \frac{W}{L} \left[(V_{GS} - V_T)^{\frac{2}{k_t}} - (V_{GS} - V_T - V_{DS})^{\frac{2}{k_t}} \right] \left(1 - \frac{V_{DS}}{\lambda} \right)^{-1} V_{DS}^{(2-2/k_t)} / 2, \tag{2.10}$$

where k_t is given by

$$k_t = -\frac{4}{15} \left(\frac{T}{T_{TS}} \right)^2 + \frac{T}{T_{TS}} + \frac{1}{15}, \tag{2.11}$$

where $T_{TS}=E_{tc}/k$. Servati et al. have developed a comprehensive model for both the reverse and the forward bias regions [25][30].This model is used in this thesis for all the circuit-level simulations. It

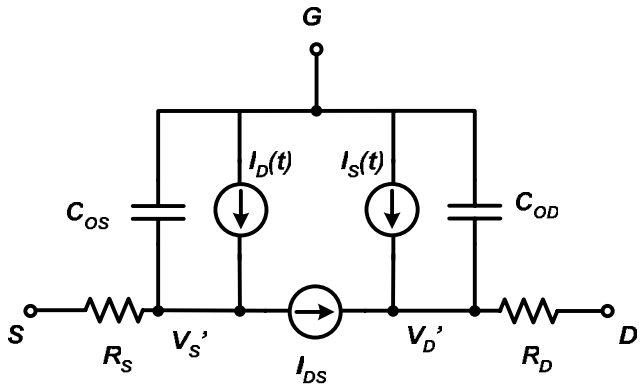


Figure 2.6: Equivalent circuit for the a-Si TFT model used in this thesis. Adapted from [30]

is assumed that μ_{FET} is smaller than μ_n by a constant factor. The drain current in the linear region is given by

$$I_D = \frac{\mu_{FET}}{\alpha}\zeta C_i^{\alpha-1}\frac{W}{L}\left[(V_{GS}' - V_T)^{\alpha} - (V_{GS}' - V_T - V_{DS}')^{\alpha}\right], \tag{2.12}$$

where ζ is a unit matching parameter, and α is equal to $2T/T_{TS}$ with a value close to 2. V_{GS}' and V_{DS}' are internal gate-source and drain-source voltages, after the drain and the source contact resistances are considered. Fig. 2.6 denotes an equivalent circuit of the TFT model. Here, R_D and R_S are the series contact resistance of the drain and source terminals. $I_D(t)$ and $I_S(t)$ model the dynamic behaviour of the channel charge, and C_{OD} and C_{OS} are the overlap capacitors between the gate and drain/source terminals.

2.1.3 Instability of a-Si TFTs

In contrast to crystalline silicon MOSFETs, a-Si TFTs demonstrate instability in the form of a shift in the threshold voltage under prolonged gate voltage bias stress. Fig. 2.7 shows the measured V_T shift in an a-Si TFT after it is exposed to different gate-source voltages for a period of 10 hours. After a fast initial increase in the V_T, it increases gradually. For a 20-V V_{GS}, V_T shift is in excess of 1.25 V within 10 hours.

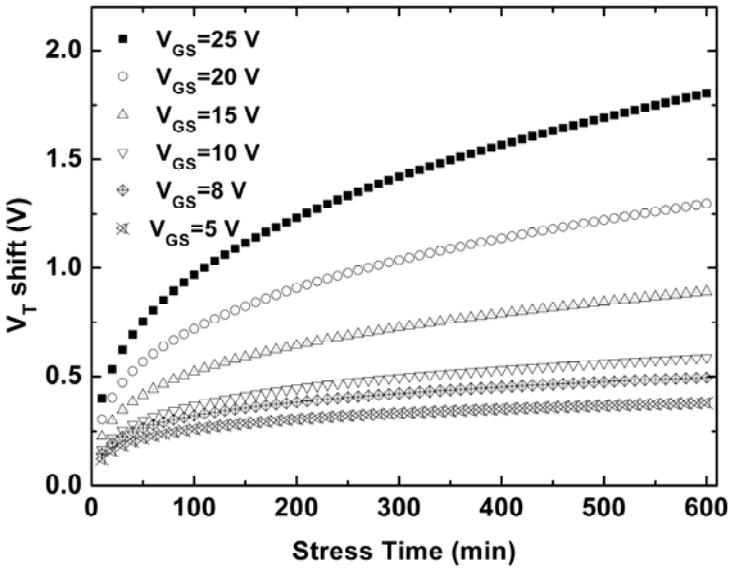


Figure 2.7 Shift in the threshold voltage of an a-Si TFT as a function of time. Adapted from [32]

For more than two decades, the mechanisms of the instability of a-Si TFTs have been studied extensively [33]-[40]. However, the models exhibit limited accuracy, in particular, for predicting the V_T shift under varying gate voltages. Research has indicated that two mechanisms are responsible for the V_T shift in a-Si TFTs: charge trapping in the a-Si/a-SiN interface and a-SiN gate dielectric, and defect creation in the a-Si layer. Powel has distinguished between these two mechanisms by stressing ambipolar TFTs with negative and positive gate voltages [33]. The results confirm that at high gate-source voltages, the shift in the V_T is primarily caused by the charge trapping. Since both a-Si and a-SiN gate dielectric layers are highly disordered, the defect density at the a-Si/a-SiN interface and the bulk of the a-SiN gate dielectric is high. As a result, the electrons in the TFT channel are easily trapped into the interface states and then trapped into the deep bulk states of the gate dielectric. The time constants associated with the interface states are relatively small (in the range of few to hundreds of milliseconds). Consequently, when the bias voltage is disconnected from the gate terminal, most of the trapped electrons in these shallow states are released, and the V_T returns rapidly to its initial point [34]. The time constants associated with the a-SiN states have a broader range and can be very long

(up to hundreds of hours) resulting in an almost permanent shift in V_T at the room temperature. The results in [33] reveal that the electron trapping in a-SiN occurs at gate voltages higher than 50 V. Furthermore, by increasing the ratio of the nitride in a-SiN, it is possible to considerably reduce the bulk charge trapping [41].

At lower gate voltages, the defect creation in the a-Si layer is assumed to be the dominant mechanism of the V_T shift, and occurs by braking weak Si-Si bonds. These weak bonds are the primary cause of the acceptor-like tail states in a-Si. The broken weak bonds form dangling bonds that are eventually stabilized by the dispersive diffusion of hydrogen atoms in the a-Si [35]. For a positive gate bias, these defect states are generated below the Fermi level, causing positive shift in V_T, and no significant change in the sub-threshold slope. The mechanism of defect creation is highly temperature-dependent such that the rate of the V_T shift increases considerably at higher temperatures.

Both the charge trapping and defect state creation mechanisms are reversible. However, at room temperature, the time constants can be in the range of a year [24]. Increasing the temperature considerably accelerates the reverse mechanisms. Annealing a TFT at a temperature range of 170 ^{O}C to 200 ^{O}C for near 2 hours is succeeded by a slow cooling cycle for more than 4 hours. This removes all the defect states and trapped electrons and returns the V_T to its original value. A positive V_T shift is also compensated for by applying a negative bias to the gate terminal [33][36]. The negative gate voltage accelerates the release of the trapped electrons. Moreover, the negative voltage generates deep defects above the Fermi level which compensate for the effect of the defects, generated by the positive bias. The Experimental results prove that for the same absolute value of the gate bias, the rate of the negative V_T shift is lower than the rate of the positive shift [36].

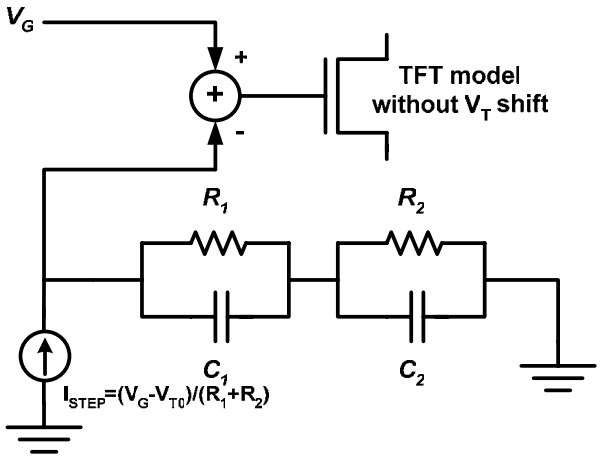


Figure 2.8: Circuit-level model for the V_T shift in a-Si TFTs. Adapted from [40].

2.1.4 V_T Shift Models

By assuming that defect creation is the major mechanism of V_T shift, Jackson and Powel have developed a power-law model for the V_T shift in the form of

$$\Delta V_T(t) = (V_{GS} - V_{T0})\left(\frac{t}{\tau}\right)^{\beta}, \tag{2.13}$$

where V_{T0} is the initial threshold voltage, t is the stress time, τ is a time constant, and β is a power factor constant [37]. In fact, the power-law model stems from a more accurate stretched exponential equation in the form of

$$\Delta V_T = (V_{GS} - V_{T0})\left(1 - \exp\left(-\frac{t}{\tau}\right)^{\beta}\right). \tag{2.14}$$

At room temperature, β has a value close to 0.5. Also, τ is temperature-dependent and is given by

$$\tau = \tau_0 \exp\left(\frac{E_a}{kT}\right), \tag{2.15}$$

where τ_0 is in the order of 10^{-10}s, and E_a=0.95eV is the activation energy. Kanicki has considered charge trapping as the dominant mechanism of the V_T shift [38]. The model is a stretched exponential

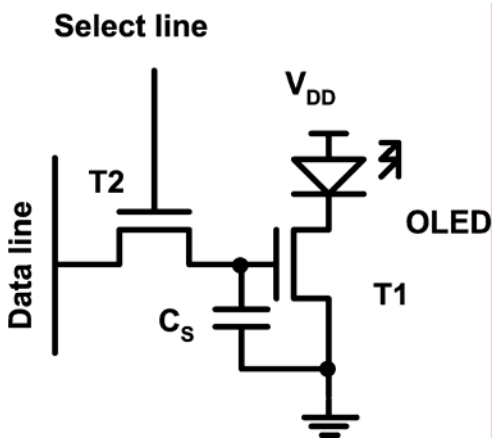


Figure 2.9: Conventional 2-TFT pixel circuit.

equation similar to (2.14) with β = 0.25, E_a=1.175eV, and τ_0 in the order of 10^{-12}. For a pulsed gate-source signal, Kanicki has introduced an empirical power-law model [39]

$$\Delta V_T(t) = A(V_{GS} - V_{T0})^{\alpha} t^{\beta} . \tag{2.16}$$

Here, τ is the effective ON time of the stressed TFT and A, α, and β are $1.5\text{x}10^{-4}$, 1.9, and 0.5, respectively. For all the models, it is assumed that V_{GS} is constant. In most cases however, the gate bias varies. Recently, Sambandan has presented an equivalent circuit description of the V_T shift based, on a stochastic model [40] where V_T shift is modelled by the two RC circuits in Fig. 2.8. The RC time-constants are associated with the shallow and deep states, and are extracted experimentally. Although the model has the advantage of compatibility with the circuit simulators, the model has not been fully proven since it is based on limited experimental results and relatively short stress times.

2.2 Pixel Design Considerations with a-Si TFT

In this section, different aspects of designing AMOLED pixel circuits with a-Si TFTs are discussed, particularly, those associated with the characteristics of a-Si TFTs. All the investigations are based on the conventional 2-TFT pixel circuit in Fig 2.9.

2.2.1 Instability in the OLED Current

As mentioned in Section 2.1.3, the threshold voltage of a-Si TFTs shifts under prolonged gate bias stress. For a positive gate bias, the shift is positive, and the V_T of the TFTs increases. In the 2-TFT circuit, the switching TFT (T2) is ON only during the programming cycle and OFF during the entire hold time thus has a negligible V_T shift. The driving TFT (T1) is ON continuously thus has a substantial positive V_T shift. If T1 is biased in the saturation region, the OLED current (I_{OLED}) is given by

$$I_{OLED} = K(V_{DATA} - V_T)^{\alpha}, \tag{2.17}$$

where V_{DATA} is the stored data voltage in C_S, and K is the transconductance factor of T1. Equation (2.17) indicates that the positive V_T shift in T1 results in a reduction in I_{OLED}. Fig. 2.10 shows the measured I_{OLED} and the associated relative error as a function of the V_T shift for a fabricated 2-TFT pixel circuit. The T1 and T2 sizes are equal to 600μm/23μm and 200μm/23μm and the nominal current is 2 μA. It is observed that, for 2.5-V V_T shift, I_{OLED} drops in excess of 95%, and eventually the pixel is turned off.

The degradation of the OLED current over time is shown in Fig 2.11 for an initial current of 15.5 μA. The 2-TFT pixel circuit has a limited life time due to the V_T shift in its drive TFT. Generally, depending on the fabrication process, and based on the models presented in Section 2.1.4, for a TFT with a W/L ratio of 5 and initial current of 1, a V_T shift between 3.5 V to 5 V is expected over 10,000 hours of stress. According to Fig 2.10, this V_T shift is sufficient to turn the pixel off. Even a 1-V V_T shift results in almost a 50% degradation in the OLED current and luminance. The high sensitivity of the 2-TFT circuit to V_T signifies the need for driving schemes that compensate for the V_T shift. One possible compensating method is to predict the V_T shift of the drive TFT in the 2-TFT and increase the pixel data accordingly. However, this scheme is not practical due to the lack of a model that can

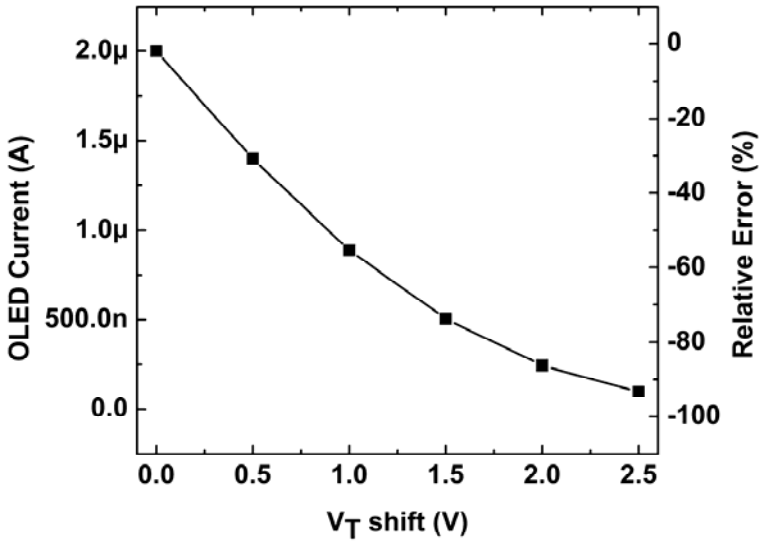


Figure 2.10: Measured OLED current and the associated relative change as a function of the V_T shift in a 2-TFT pixel circuit.

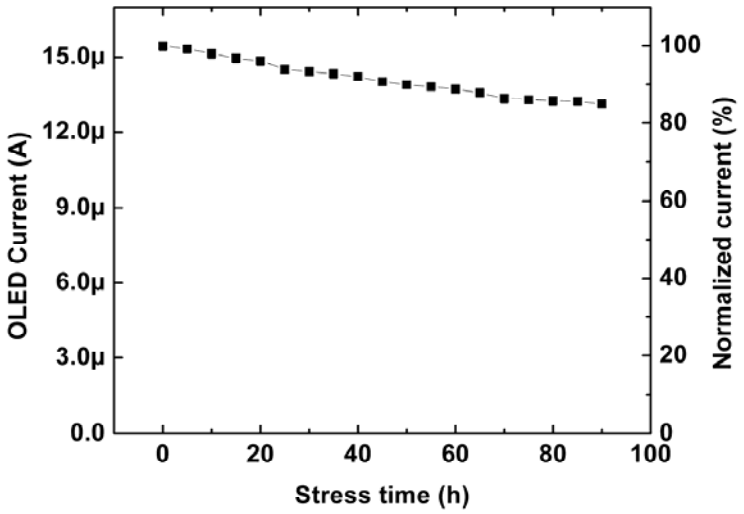


Figure 2.11: OLED current and the associated relative change as a function of stress time.

accurately predict the V_T shift for variable bias voltages at different temperatures and relaxation times, as well as the required processing capacity for each pixel.

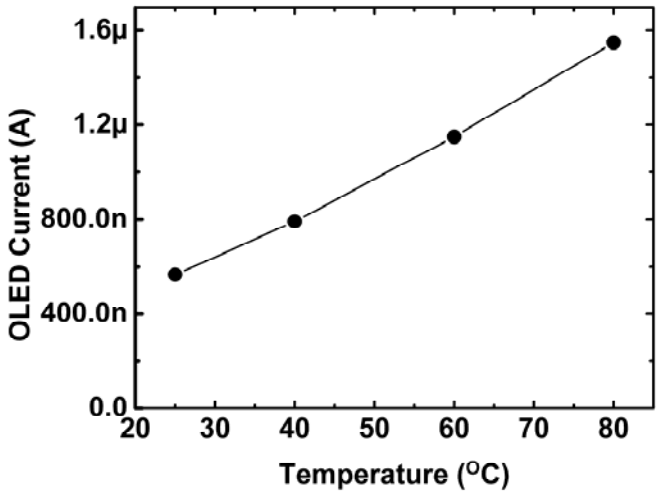


Figure 2.12: OLED current in a 2-TFT pixel circuit as a function of temperature.

2.2.2 Low Mobility

The low mobility of a-Si TFTs leads to high resistance of TFT switches and low transconductance of the driving TFTs. To obtain the required luminance in a display, the driving TFT should provide the OLED with sufficient current. Due to the low mobility of a-Si, the feasibility of a-Si TFT backplanes for AMOLED displays is a matter of debate. Owing to considerable improvements in the power efficiency of the OLEDs, the maximum pixel current in the state-of-the-art OLEDs can be easily provided by a-Si TFTs. An analytical model presented in [17] shows that the low mobility of a-Si TFTs is not a limiting factor and most of the pixel area is consumed by interconnections and signal lines. In some of the driving schemes such as current driving, the high resistance of TFT switches, and the low transconductance of the driving TFTs results in long programming times. This will be discussed in Chapter 3.

2.2.3 Effect of Temperature

The electrical characteristics of a-Si TFTs change with the temperature. As a result, without an external compensating scheme, the 2-TFT pixel circuit is very sensitive to temperature. Fig 2.12

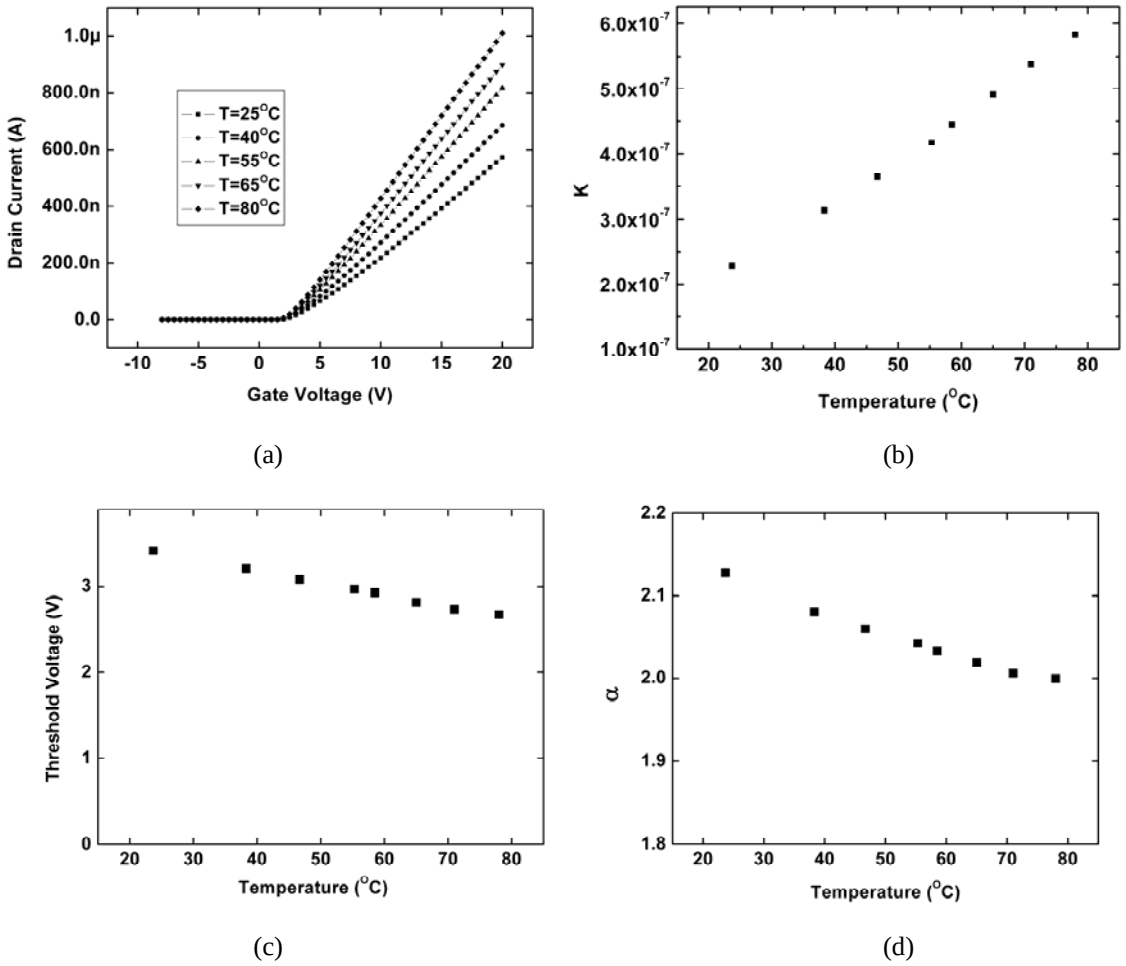


Figure 2.13: Effect of temperature on the characteristics of an a-Si TFT: (a) I-V characteristics for different temperatures, (b) transconductance coefficient (*K*) as a function of temperature, (c) threshold voltage as a function of temperature, (d) power factor of the TFT as a function of temperature.

shows the current in a 2-TFT pixel circuit as a function of temperature for an initial current of 500 nA.

It is evident that the current increases more than three times over a temperature range of 20 ^{O}C to 75 ^{O}C. Fig. 2.13 (a) denotes the measured I-V characteristics of an a-Si TFT in the triode region at different temperatures. The drain current increases with increasing the temperature. This occurs because of the increase in the transconductance of a TFT with temperature as shown in Fig. 2.13 (b). The increase in the transconductance is due to increase in the number of free electrons in the channel.

In addition, the threshold voltage of a TFT decreases as the temperature increases as shown in Fig. 2.14 (c). The power factor of a TFT, α, slightly decreases with the temperature, as shown in Fig. 2.16 (d).

For an a-Si TFT in the saturation region, an empirical temperature model has been reported in [42]. The TFT I-V characteristic is expressed by

$$I = K(T)(V_{DATA} - V_T(T))^{\alpha(T)}. \tag{2.18}$$

$K(T)$, $V_T(T)$, and $\alpha(T)$ are determined by the following equations:

$$V_T(T) = V_T(T_0) - \eta_1(T - T_0), \tag{2.19}$$

$$\alpha(T) = \frac{0.95q}{kT\beta} + \alpha_0, \tag{2.20}$$

$$K(T) = K_{T0} \exp\left[\eta_2\left(\frac{1}{T_0} - \frac{1}{T}\right)\right]. \tag{2.21}$$

Here, $\eta 1$, $\eta 2$, and β are process-dependent parameters and are obtained from measurement.

2.2.4 Power Efficiency

The power efficiency of an AMOLED pixel circuit (η_P) is defined as the ratio of the OLED power consumption to the overall power consumption of the pixel. For a given programming current, η_P is defined as

$$\eta_P(I) = \frac{P_{OLED}(I)}{P_{PIXEL}(I)} = \frac{V_{OLED}(I)}{V_{DD}(I)} = \frac{V_{OLED}(I)}{V_{OLED}(I) + V_{TFT}(I)}, \tag{2.22}$$

where V_{OLED} is the OLED voltage, and V_{TFT} is the total voltage drop on the TFTs in the driving path. To increase the efficiency, V_{DD}, and thus, V_{TFT} needs to be reduced. Therefore, a power efficient pixel circuit must have the minimum number of TFTs in the circuit's driving path. However, even in most of the pixel circuits with one TFT in the driving path, such as the conventional 2-TFT pixel, the

driving TFT is biased in the saturation region to reduce the sensitivity of the current to V_{DD} variation. This results in significant power consumption in the driving TFT.

2.2.5 Settling Time

The required programming time of a display depends on its resolution and the refresh rate. For example, in a quarter video graphic array (QVGA) display with a 60 Hz refresh rate, the available programming time is less than 70 μs. For high-definition applications, programming times smaller than 20 μs are required.

In the 2-TFT pixel, the settling time is mainly determined by the parasitic capacitance of the data line and the ON resistance of the switching TFT (T2). Fig. 2.14 shows a detailed model of the display column, when the Nth pixel is programmed. The line parasitic capacitance in each pixel (c_p) consists of the overlap capacitance between the column and row lines, and the gate-drain overlap capacitance in the switching TFTs. In contrast to polysilicon TFT and CMOS technologies, a-Si TFT process is not self-aligned. Due to the inverted staggered structure of the TFTs, certain amount of overlaps between gate and source and drain terminals are necessary to guarantee the formation of a reliable channel and low contact resistance. Depending on the technology, the overlap length is between 2 μm to 5 μm. The large overlap results in large gate-drain and gate-source parasitic capacitors. The total parasitic capacitance of the line (C_P) is given by

$$C_P = NC_i\left(W_S L_{OV} + A_{OV}\right) \tag{2.23}$$

where N is the number of columns, and A_{OV} is the total overlap area between the row and column lines for each pixel. W_S is the width of T2, and L_{OV} is the length of the gate-drain overlap. Depending on the size and resolution of the display, C_P range from a few pico-Farads to hundreds of pico-Farads [43].

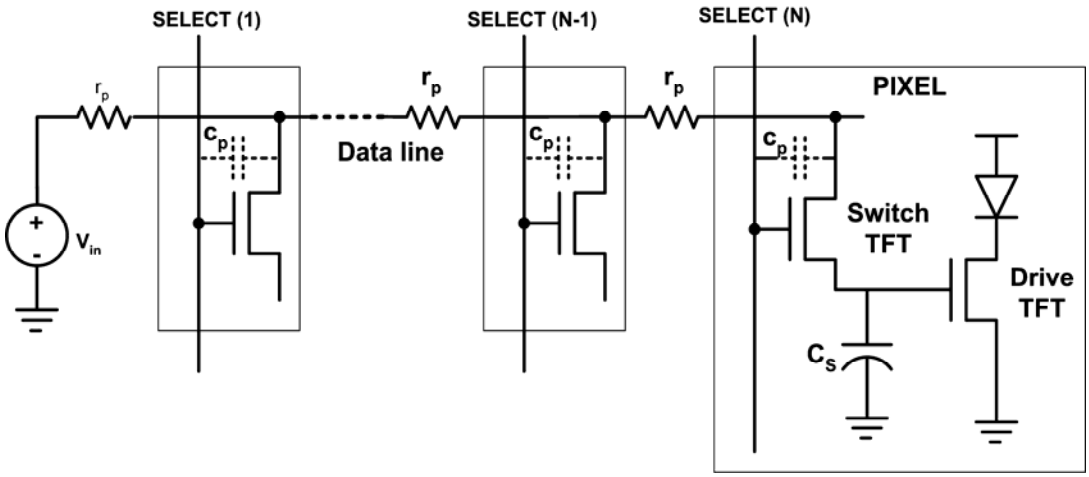


Figure 2.14: Model of a display column when a pixel is programmed.

The line series resistance per pixel (r_p) has a value in the range of 10 Ω [43]. Simulation and analytical data indicate that the total series resistance of the data line is much smaller than the ON resistance of the switch TFT; consequently, the effect of r_p on the settling time can be neglected. Based on this assumption, the 5%-settling-time of the data voltage in a 2-TFT is approximately equal to $3(C_P+C_{GS}+C_S)R_{ON}$, where R_{ON} is the ON resistance of the switching TFT, and C_{GS} is the gate-source capacitance of the drive TFT. For a TFT process with C_i=20nF/cm^2 and μ_{FET}=1 cm^2/Vs, and a pixel circuit with C_S=0.5 pF, T1=100/5 μm, T2=20/5 μm, A_{OV}=100 μm^2, and r_p =15 Ω, the simulated 5-% settling times for N=240 and N=640, are shorter than 2 μs. While in the 2-TFT pixel circuit the settling time is short, it will be shown that in some driving schemes such as current driving the settling time can be quite long.

2.2.6 Lack of p-channel Device

Due to the extremely low mobility of the holes in a-Si [23], fabrication of p-channel a-Si TFTs with a reasonable size is not possible. As a result, the pixel circuits must be designed only with n-channel devices. This limits the number of design alternatives. Moreover, as shown in Section 2.3.3, the lack of the p-channel TFT limits the possible alternatives in the integration of the conventional OLEDs into the display backplane.

2.2.7 Reverse Current

During the hold time, the stored voltage in C_S starts to decrease due to the reverse current of the switch TFT. As a result, the OLED current at the end of the hold cycle is smaller than the current at the beginning. The average reduction in the OLED current during the hold mode is approximated by

$$\Delta I_H \approx \frac{1}{2}\frac{t_{hold}}{C_S} I_{OFF}\, g_m \tag{2.24}$$

where t_{hold} is the hold time, I_{OFF} is the reverse current of the switching TFT, and g_m is the transconductance of the driving TFT for the nominal programming current (I_{PROG}). Due to the low reverse current of the a-Si TFTs, the resulting reduction in the hold current is small. For instance, for a display with a refreshing rate of 60 Hz, and a pixel circuit with C_S=0.5 pF, g_m=0.5 μA/V, and I_{OFF}=1 pA, ΔI_H is less than 4.2 nA which is negligible.

2.2.8 Charge Injection

Similar to any field-effect transistor, when a TFT switch is turned off, charge injection and clock feedthrough induce a negative error voltage to the sampled data voltage, reducing the hold current. As a result, the size of the drive TFT and the storage capacitor must be designed to maximize the hold current. In addition to the reduction in the hold current, the charge injection has considerable effect on the stability of many AMOLED pixel circuits. This will be studied in Chapter 3.

2.2.9 Limited Number of TFTs per Pixel

The number of TFTs per pixel circuit is limited due to the large size of the a-Si TFTs, the limited area of each pixel, and more importantly, the required high yield for a display. As a result, it is necessary that the AMOLED pixel circuits have as few numbers of TFTs as possible. In most of the reported pixel circuits, the number of TFTs per pixel is less than five or six. The limitation in the number of TFTs per-pixel prevents designers from realizing complex on-pixel compensation schemes. The external current drivers are implemented in CMOS technology and can accommodate

more complicated circuits. Therefore, a practical driving scheme must have a simple pixel circuit, and place most of the compensation circuits and processes to the off-panel external drivers.

2.2.10 TFT Noise

It is crucial to study the effect of noise in a-Si TFTs on the OLED current in AMOLED pixel circuits. The noise power spectra of a-Si TFTs consist of flicker and thermal noise components [44]. The equivalent thermal noise current is similar to that in crystalline MOSFETs as follows:

$$I_{th}^2(f) = \beta_{th} 4kT\mu_{FET} C_i \frac{W}{L}(V_{gs} - V_T) \tag{2.25}$$

where k is the Boltzman's constant, and T is the temperature. β_{th} is 1 when TFT is in the triode region and 2/3 when TFT is in the saturation region. Generally, the flicker noise model in the field-effect transistors can be described by the fluctuations in the number of carriers (ΔN, or Mc Worther theory) or fluctuations in the field effect mobility ($\Delta\mu$ or Hooge theory) [45]. According to the experimental results in the literature [44]-[47], it is known that the flicker noise in a-Si TFTs is described more accurately by the $\Delta\mu$ theory. The estimated flicker noise current in the triode and saturation regions is given by [44]:

$$I_f^2(f) = \frac{\alpha_{triode} q\mu_{FET}^2 C_i (W/L)^2}{WL}(V_{gs} - V_T)V_{ds}^2 \frac{1}{f}, \tag{2.26}$$

and

$$I_f^2(f) = \frac{\alpha_{sat} q\mu_{FET}^2 C_i (W/L)^2}{WL}(V_{gs} - V_T)^3 \frac{1}{f}. \tag{2.27}$$

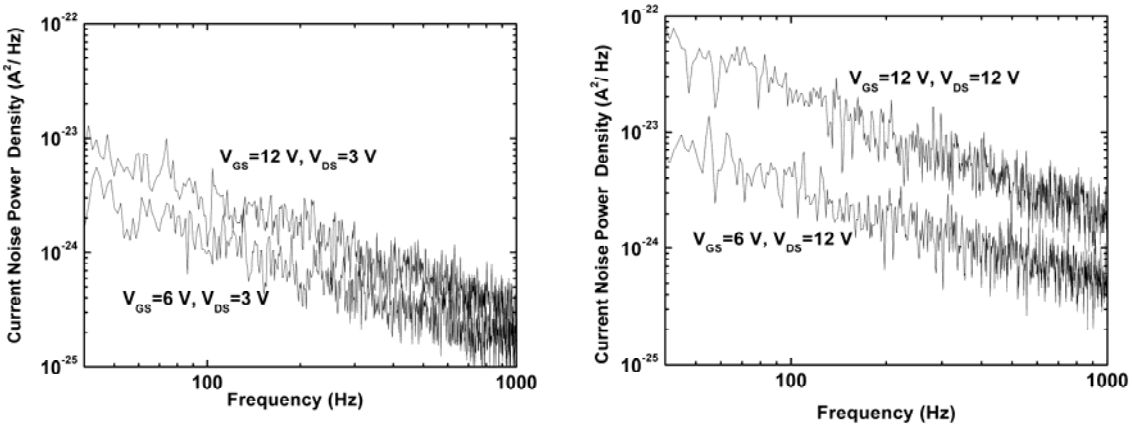


Figure 2.15: Measured noise spectra of an a-Si TFT in: (a) triode region, (b) saturation region.

Here, q is the charge of electron, f is the frequency, and α_{triode} and α_{sat} are the fitting constants, and depend on the fabrication characteristics of the TFTs. Fig. 2.15 shows the measured flicker noise spectra of an a-Si TFT with W=400 μm and L=23μm, fabricated at the University of Waterloo. For the fabricated devices, the approximated values of α_{triode} and α_{sat} are 0.02 and 0.008, respectively.

The RMS noise of the OLED current in a 2-TFT pixel circuit is calculated by the small-signal model in Fig. 2.16 for various currents. The OLED is modelled by a resistor (r_{OLED}), and a capacitor (C_{OLED}), derived from the empirical model described in Fig. 2.19. r_{ds} is the small-signal drain source resistance of T1. The V_{DS} of the switch TFT is zero in the steady sate thus its flicker noise is set to 0. To find the RMS noise current, the noise spectral density is integrated from the circuit sampling rate of 50 Hz to infinity. Fig. 2.17 shows the total RMS noise of the OLED current, including the effect of T1 and T2 as a function of the OLED current. Compared to the OLED current, the level of noise is almost negligible; that is, the maximum ratio of the noise to the OLED current is 2.3×10^{-4}. From this analysis, it is concluded that the TFT noise is not much of an issue in the design of a-Si TFT AMOLED pixel circuits.

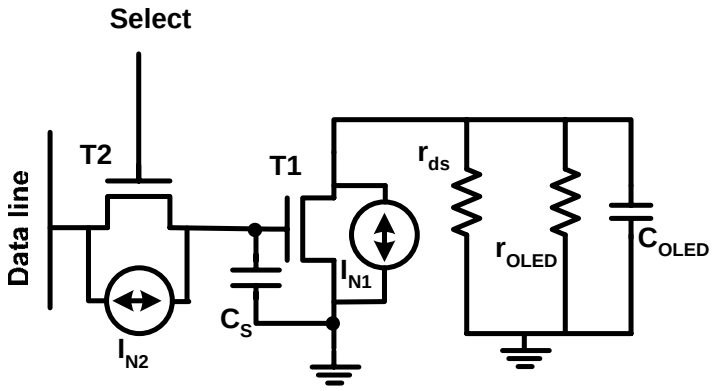


Figure 2.16: Circuit model for noise analysis of the 2-TFT pixel circuit.

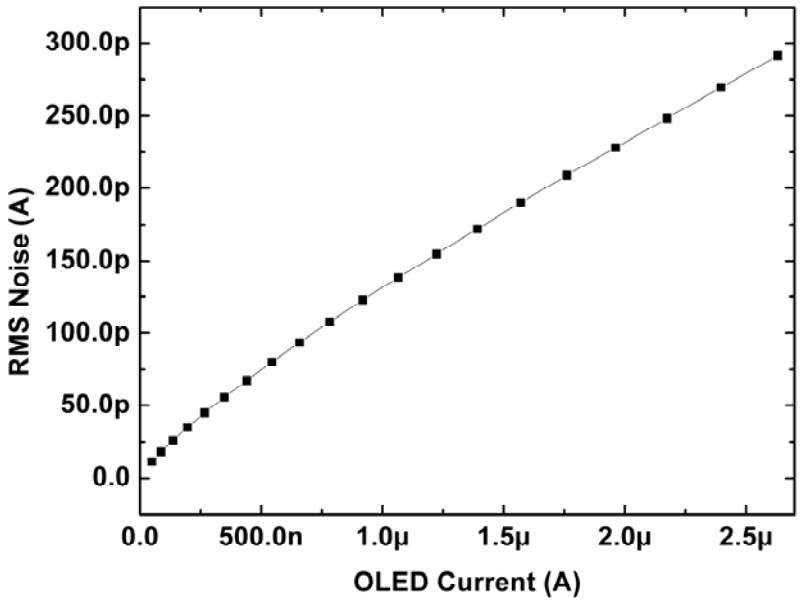


Figure 2.17: RMS noise of the 2-TFT circuit as a function of the programming current.

2.3 OLED in AMOLED Pixel Design

The physics and fabrication of OLED devices are subject to substantial research. The operation of the OLED, conduction, electroluminescent, and degradation mechanisms are debatable. In contrast to inorganic semiconductors, the properties of the organic semiconductors are much more dependent on the fabrication process and material type. This makes it difficult to find a general model for OLEDs.

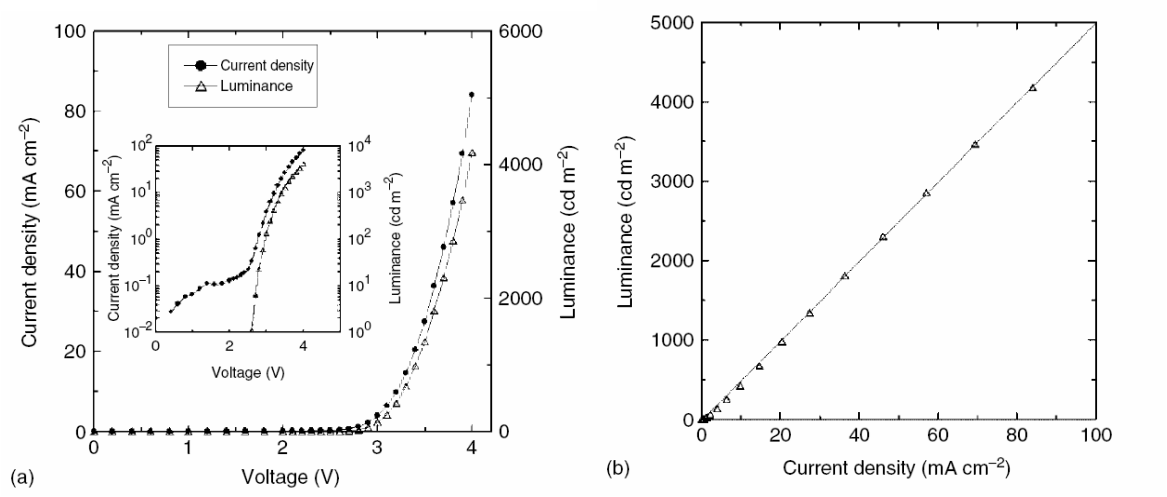


Figure. 2.18: Typical OLED characteristics: (a): I-V characteristics of an OLED, (b): Luminance versus current density. After [48].

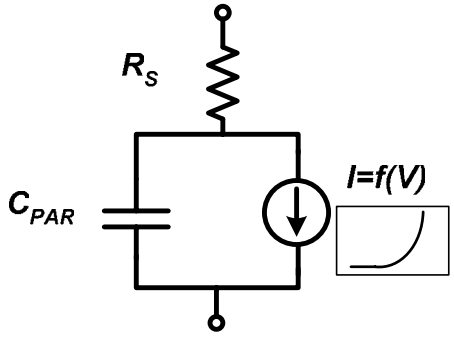


Figure 2.19: OLED equivalent circuit.

Moreover, due to the demands of the OLED market, the focus of the research on OLED is more about enhancing its lifetime and efficiency rather than comprehending the OLED operation and modelling.

Since there is no consensus circuit model for the OLED device, in the design of AMOLED circuits OLED is usually considered as a “black-box” circuit with empirically-derived circuit parameters. In the following sessions, some aspects of the OLED for the design of AMOLED pixels are discussed.

2.3.1 OLED Device Characteristics

Fig. 2.18 (a) and (b) depict a typical I-V characteristic and the luminance versus current density in a small-molecule OLED [48]. The I-V characteristic of the OLED is comparable to that in a diode.

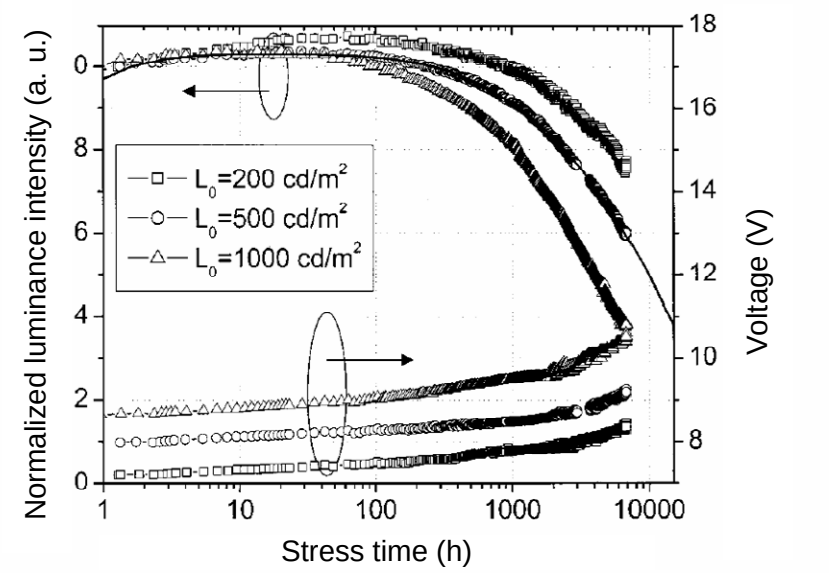


Figure 2.20: Typical luminance degradation of a small-molecule OLED and the associated shift in the OLED voltage. After [52]

However, it does not follow the exponential characteristic of the crystalline diodes and follows a power-law equation. The relationship between the luminance and current density is almost linear. Despite the OLED material and fabrication process, these characteristics are common in most of small-molecule and polymer OLEDs [1]. A generally-accepted model for the I-V characteristic of OLED is

$$I = KV^{m+1} / d^{2m+1} \tag{2.28}$$

where K is the fitting coefficient, m is an integer with a value in the range of 5 to 15, and d is the thickness of the OLED layer. The model is based on the assumption that the conduction of the electrons and the holes in OLED is trapped-charge limited [49]-[50]. For circuit simulations, the equivalent circuit in Fig. 2.19 is chosen. Here, I_{DC}=f(V) denotes the I-V characteristics of the OLED. The series ohmic resistance of the OLED is modelled by R_S, and C_{PAR} models the constant parallel capacitance of the OLED. Since the OLED layers are thin (usually in the range of 100 nm), C_{PAR} is large. A typical value for C_{PAR} is close to 25 F/cm2 [51].

2.3.2 OLED Degradation

As mentioned in Chapter 1, OLED luminance degrades over time. Studies of the OLED stability indicate that the luminance degradation is accompanied by a gradual increase in the OLED voltage [52] [13]. An example of such a shift in the OLED voltage is shown in Fig. 2.20. This shift in the OLED voltage (ΔV_{OLED}) is associated with the increase in the OLED resistance, caused by the same mechanisms that are responsible for the luminance degradation, that is, formation of dark spot defects [53], and injection of holes into the electroluminescent layer [13].

In an AMOLED pixel circuit, a shift in the OLED voltage changes the V_{DS} of the drive TFT, inducing the error in the OLED current due to the limited drain-source resistance of the TFT. If the OLED is placed in the source of the drive TFT, the resulting degradation is more severe due to the change in the V_{GS} of the drive TFT. Although ΔV_{OLED} is not desired in the OLED pixel circuits, it can be used as feedback of the degradation in luminance to compensate for the degradation of the OLED. An implementation of this idea is presented in Chapter 3.

2.3.3 Effect of OLED Integration on the AMOLED Pixel Circuits

Fig. 2.21 depicts the conventional integration of an OLED and a-Si TFT in a bottom-emission backplane. The OLED layers and the cathode metal are deposited on top of the transparent anode. The cathode layer is shared by all the OLEDs, and is connected to a ground terminal. In this configuration, the source of the drive TFT is connected to the OLED. Connecting the OLED to the drain terminal of the TFT is not possible because it requires patterning of the cathode metal and etching of the OLED layers, which drastically degrades the yield and OLED performance. Connecting the OLED to the source terminal of the drive TFT is not desired for several reasons: First, the pixel circuits need higher data and drive voltages. Secondly, in many pixel circuits, such as the conventional 2-TFT, the shift in the OLED voltage accelerates the degradation in the OLED current.

Another drawback of the conventional bottom-emission backplane is the small area available for the pixel circuit due to the coplanar structure of the integration.

In the conventional top-emission integration, light exits from the thin metal cathode layer, as shown in Fig 2.22 [12]. Since the TFT part of the circuit does not block the OLED, more area is available for the pixel circuits, and the display can have a higher aperture ratio. In this integration OLED is connected to the source terminal of the drive TFT. To connect the OLED to the drain terminal of the drive TFT, inverted OLED has been proposed. In an inverted OLED, the cathode terminal is deposited first, and the OLED layers and the common anode terminal are deposited later. Usually a thin metal layer such as Au is used for the anode instead of ITO since the sputtering of ITO damages to the organic layers. The integration of the OLED with backplanes with both top and bottom-emission configurations have been reported [53]-[54], and are illustrated in Fig. 2.23 and Fig. 2.24. The inverted OLED is not as mature as the conventional OLED, and usually exhibits a lower power efficiency. Due to the tradeoffs between different integration methods and OLED technologies, compatibility of a driving scheme with both of the conventional and inverted OLED technologies is highly advantageous.

2.4 Conclusion

Although a-Si TFTs have the advantage of a well-established infrastructure and low fabrication cost, they suffer from instability, low mobility, and sensitivity to temperature. To use a-Si TFTs for AMOLED pixel circuits, driving schemes are required to compensate for device shortcomings in circuit level. In particular, the driving schemes should compensate for the variations in the V_T and mobility of TFTs. Low pixel complexity, high power efficiency, and fast programming are also key design constraints. Integration of the TFT pixel circuits with OLED is also an important design factor that limits the circuit configurations.

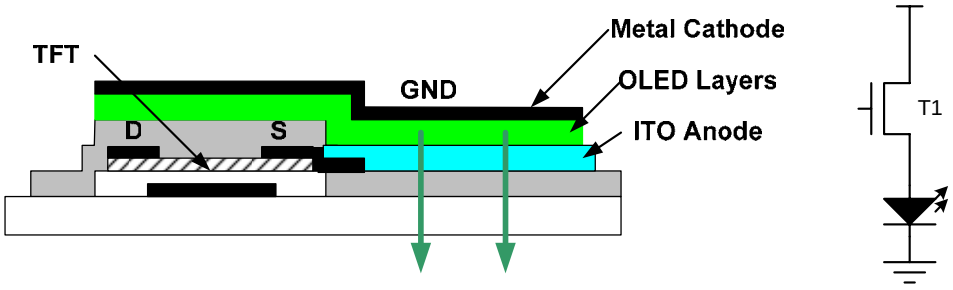


Figure 2.21: Integration of the bottom-emission backplane with a conventional OLED.

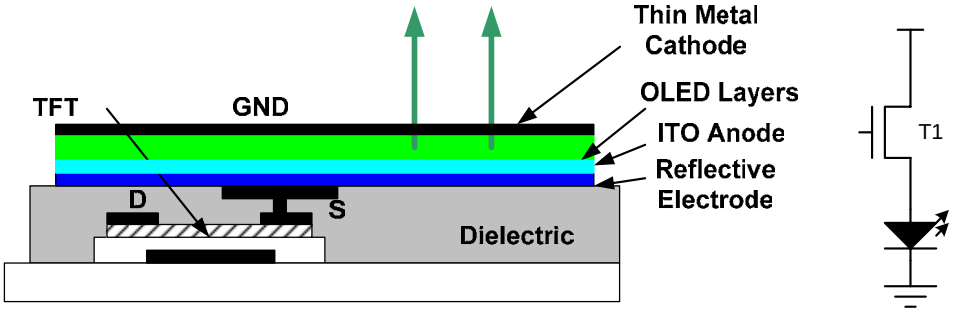


Figure 2.22: Integration of the top-emission backplane with a conventional OLED.

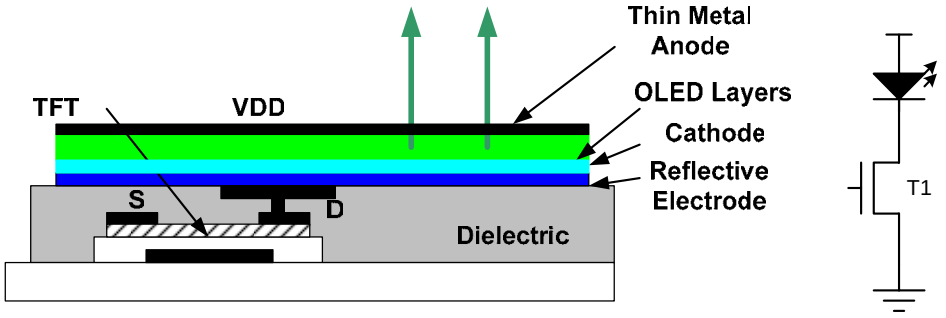


Figure 2.23: Integration of the top-emission backplane with an inverted OLED.

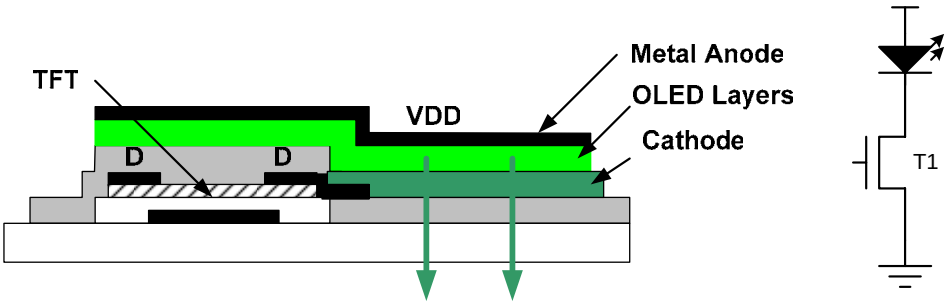


Figure 2.24: Integration of the bottom-emission backplane with an inverted OLED.

Chapter 3
Driving Schemes for a-Si TFT AMOLED Backplanes

As discussed in Section 2.2.1, in the conventional 2-TFT pixel circuit, the output current is sensitive to the threshold voltage shift of the driving TFT, leading to degradation of the luminance of the pixels over time. Several driving schemes have been introduced to reduce the sensitivity of the current to the V_T shift. In this chapter, some important AMOLED driving schemes including current and voltage programming are discussed in detail. In particular, the performance of the current programmed pixel circuits in terms of stability and settling time is investigated for the first time.

3.1 Current Programming

In the current programming driving scheme, the programming current flows through a diode-connected TFT during the programming time, and the gate-source voltage of the TFT is stored in a capacitor. The current is replicated by the pixel circuit for the OLED during the hold (frame) time. Such a driving scheme compensates for the V_T shift in the TFTs since the OLED current does not directly depend on the characteristics of the drive TFT. Generally, current-programmed pixel circuits (CPPCs) are categorized as mirrored and non-mirrored circuits [55]. As implied by the names, in a mirrored pixel, the sampling of the programming current and the driving of the OLED are performed by a current mirror. In a non-mirrored pixel circuit, the same TFT samples the programming current and drives the OLED.

Fig. 3.1 (a) shows the basic circuit diagram of a typical non-mirrored CPPC. It consists of an OLED, a storage capacitor (C_S), a drive TFT (T1), and some switch TFTs (S1 to S3). During the programming cycle, S1 and S2 are turned on and S3 is turned off. The programming current flows into the drive TFT through S1 and the gate-source voltage of T1 is stored in C_S through S2. After the

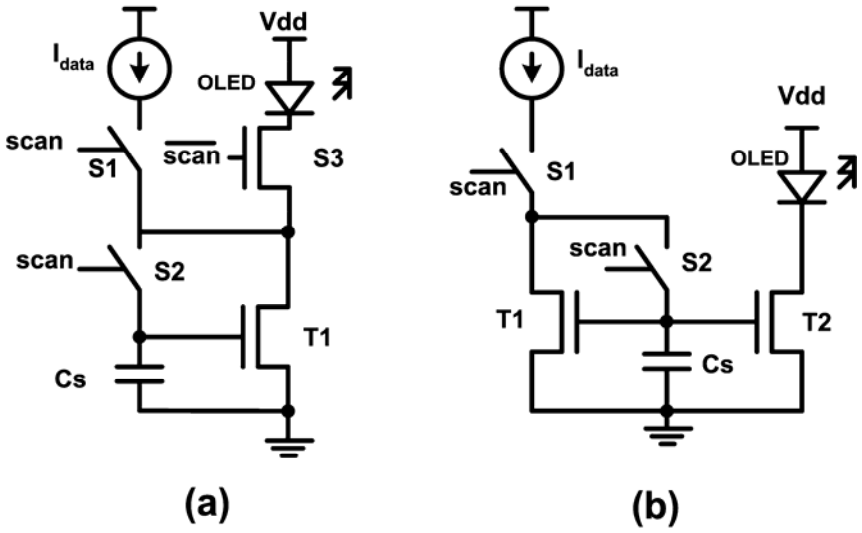


Figure 3.1: Conceptual circuits of current programmed pixels: (a) non-mirrored, (b) mirrored.

programming cycle, S1 and S2 are turned off and S3 is turned on. A copy of the programming current continues to flow into the OLED, since the gate-source voltage of T1 is stored in C_S.

Fig. 3.1 (b) shows the general implementation of a mirrored CPPC. Here, T1 and T2 form the current mirror, and S1 and S2 are the switches. When the pixel is programmed, S1 and S2 are turned on, allowing the current to flow into T1. If both T1 and T2 operate in the saturation region, the amount of current that passes through the OLED depends on the sizes of T1 and T2. After programming, S1 and S2 are turned off. Since the gate-source voltage of T2 is stored in C_S, the current through T2 does not change considerably. Assuming that T1 and T2 have identical characteristics, the current through T2 is a replica of the programming current.

The OLED current in the mirrored CPPCs depends on the ratio of the size of T1 to the size of T2. Consequently, in contrast to non-mirrored pixels that always have a unity gain, it is possible to design mirrored CPPCs with various gains. Another difference in the circuit topology between mirrored and non-mirrored CPPCs is that in most of the presented non-mirrored pixels, two TFTs are in the driving path. As a result, the non-mirrored pixels require higher supply voltages, and therefore consume more

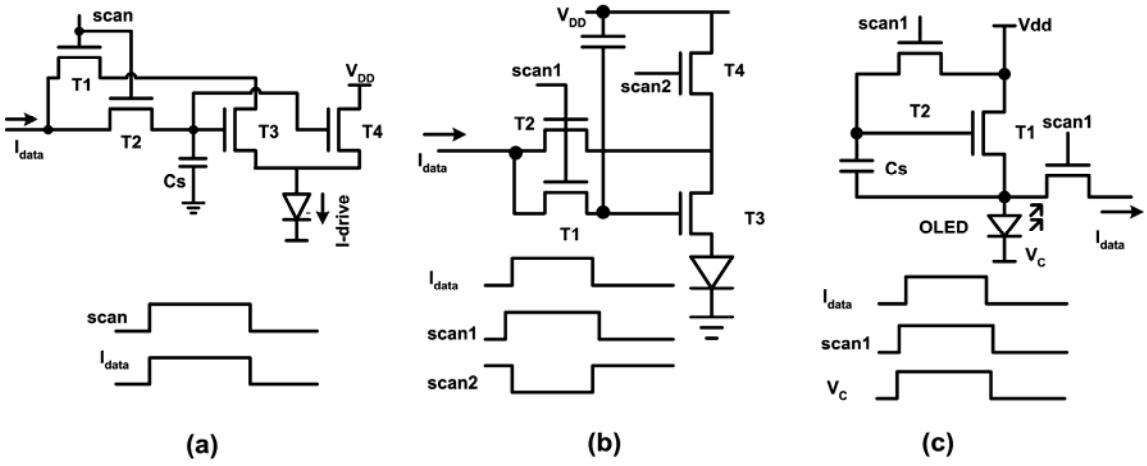


Figure 3.2: Three CPPCs: (a) 4-TFT mirrored pixel Sakaryia 2004 [64], (b) 4-TFT non-mirrored pixel Kanicki 2000 [57], (c) 3-TFT non-mirrored Ashtiani 2004 [58].

power. Mirrored CPPCs have only one TFT in the driving path. However, the matching of the current mirror TFTs must be high enough to achieve a high current uniformity over the display.

Several CPPCs have been introduced [56]-[68]. Fig. 3.2 depicts some selected mirrored and non-mirrored CPPCs. Although all of the pixel circuits operate according to the same principles highlighted in the general schematics of Fig. 3.1, the pixel circuits have their own design tradeoffs, depending on the technology and circuit topology. In the following sections, the stability, uniformity, and settling time of CPPCs are discussed.

3.1.1 Stability of CPPCs

Compared to the 2-TFT pixel circuit in Fig. 2.9, both mirrored and non-mirrored CPPCs significantly reduce the dependence of the current on the V_T of TFTs, thus reducing the effect of V_T shift on the pixel current. Moreover, CPPCs compensate for the variations in the characteristics of the TFTs, caused by temperature and mismatch. In practice however, some degree of dependence between the pixel current and the V_T remains due to the circuit and device non-idealities. The mechanisms underlying the dependence of the current on the V_T in the mirrored and non-mirrored

pixel circuits are different. In non-mirrored pixel circuits, the main source of the instability is the V_T-dependent charge injection of switches. In mirrored pixel circuits, though, different trends of the shift in the V_T of a-Si TFTs in the current mirror are principally responsible for the instability of the pixel current. Some previous experimental results presented by Sakaryia [64] have shown that the pixel current in a-Si mirrored CPPCs slightly increases over time. Although T1 and T2 have the same gate-source stress voltage, they operate in different regions. T2 has a higher drain voltage and always operates in the saturation region. However, except for the programming cycles, T1 is in the triode region. Based on experimental and analytical studies [69], in addition to the gate-source voltage, V_T shift in a-Si TFTs depends on the drain voltage, and for higher drain voltages the V_T shift is smaller. As a result, the rate of V_T shift in T1 is higher than that of T2, leading to a gradual increase in the pixel current over time.

3.1.1.1 Dynamic Instability in CPPCs

During the transition of the pixels from the programming to the hold cycles, the gate-source and drain-source voltages of the drive TFT vary, causing a dynamic error in the hold current [55]-[59]. The change in the gate-source voltage is primarily caused by the charge injection and capacitive couplings, associated with the gate-drain and gate-source overlap capacitors. Depending on the circuit structure, the drain-source voltage may change as the configuration of the pixel circuit changes from the programming to the hold cycles.

The amount of dynamic error depends on the V_T of the drive TFT, thus it causes instability in the pixel current. Although dynamic errors exist in both mirrored and non-mirrored CPPCs, it is more dominant in non-mirrored CPPCs. Assuming that the induced error in the gate-source voltage of the driving TFT is small compared to the absolute values, it is possible to analyze the effect of the V_T-dependent charge injection and changes in V_{DS} (ΔV_{DS}) by small-signal approximation. The error in the OLED current (I_{error}) is estimated by

$$I_{error} = g_m \Delta V_{GS} + g_{ds} \Delta V_{DS}, \tag{3.1}$$

where ΔV_{GS} is the error in the gate-source of the driving TFT from they charge injection. Here, g_m and g_{ds} are the small-signal transconductance and drain-source conductance of the drive TFT in the saturation region. Based on small-signal approximation, the dependence of the I_{error} on V_T variations (ΔV_T) can be estimated as

$$\Delta I_{error} = \frac{\partial I_{error}}{\partial V_T} \Delta V_T = g_m \frac{\partial \Delta V_{GS}}{\partial V_T} \Delta V_T + g_{ds} \frac{\partial \Delta V_{DS}}{\partial V_T} \Delta V_T . \tag{3.2}$$

The relationship between ΔV_{GS} and ΔV_{DS}, with V_T depends on the circuit configuration. The dynamic error in the general non-mirrored CPPC shown in Fig. 3.1 (a) is analyzed. The effect of the V_T-dependent charge injection is calculated by estimating the channel charge of S2, released into the gate-source capacitance of the driving TFT (T1) at the end of the programming cycle. The charge injection of the other switches (S1 and S3) is negligible. The following equation provides an approximation of the corresponding error in the gate-source voltage of T1

$$\Delta V_{GS1} = -\beta \frac{C_{GS2}(V_{selh} - V_{GS1} - V_{T2})}{C_{GS1} + C_{GS2} + C_S} \tag{3.3}$$

where V_{GS1} is the gate-source voltage of T1, C_{GS1} and C_{GS2} are the gate-source capacitors of T1 and S2, V_{T2} is the threshold voltage of S2, and V_{selh} is the select line voltage. Parameter β determines the portion of the charge released from the drain of S2. For high falling rates, β has a value close to 0.5. For a given programming current (I_{PROG}) V_{GS1} directly depends on the V_T such that

$$V_{GS1} = V_{T1} + \left(\frac{I_{PROG}}{K} \right)^{\frac{1}{\alpha}}, \tag{3.4}$$

assuming that the TFT I-V characteristic follows (2.17). From (3.3) and (3.4), $\frac{\partial \Delta V_{GS1}}{\partial V_T}$ is given by

$$\frac{\partial \Delta V_{GS1}}{\partial V_T} = \beta \frac{C_{GS2}}{C_{GS1} + C_{GS2} + C_S}. \tag{3.5}$$

From (3.5) it can be seen that the ratio of C_{GS2} to (C_S+C_{GS1}+C_{GS2}) has a significant effect on the dependence of the pixel current on the V_T shift. Thus, for smaller S2 sizes and for larger values of C_S, the pixel circuit is less sensitive to V_T of T1. For the pixel circuit of Fig. 3.1 (a), the change in V_{DS} from the programming to the hold cycles is found by

$$\Delta V_{DS} = V_{DD} - I_{PROG} R_{DSW3} - V_{OLED} - V_{GS1}, \tag{3.6}$$

where R_{DSW3} is the ON resistance of S3, and V_{OLED} is the voltage of the OLED. R_{DSW3} depends on V_T of S3 and is approximately given by

$$R_{DSW3} = \frac{1}{K\left(V_{selh} - V_{DD} - V_{T3}\right)^{\alpha-1}}. \tag{3.7}$$

From (3.6) it can be seen that $\partial \Delta V_{DS} / \partial V_T$ is equal to -1. Based on (3.2) to (3.6), the total dependence of the error in the current on V_T of T1 is approximated by

$$\Delta I_{error} = \left(g_m \beta \frac{C_{GS2}}{C_{GS1} + C_{GS2} + C_S} - g_{ds} \right) \Delta V_T. \tag{3.8}$$

For better understanding of the effect of the V_T shift of T1 on the pixel current, the pixel circuit of Fig. 3.1 (a) is simulated by CADENCE SPECTRE. The circuit parameters are listed in Table 3.1. Fig. 3.3 shows the relative error in the OLED current, caused by the V_T-dependent charge injection as a function of V_T-shift, for different sizes of S2. The nominal programming current is set to 1 μA. As predicted by (3.8), the error in the current increases as V_T increases and for larger sizes of S2, the sensitivity to V_T shift is higher.

Also, equations (3.6) and (3.7) reveal the dependence of ΔV_{DS} of T1 to the V_T of S3 (V_{T3}) and OLED voltage (V_{OLED}). Based on the same small-signal approach, the effect of ΔV_{T3} and ΔV_{OLED} on the pixel current is calculated by

Table 3.1: Circuit parameters used to simulate the circuit in Fig. 3.1 (a).

Design Parameter	Value
V_{sel} (V)	0-30
VDD (V)	20
C_S (pF)	2
T1 (W/L) (μm)	400/23
S1(W/L) (μm)	100/23
S2(W/L) (μm)	100-120/23
S2(W/L) (μm)	400/23

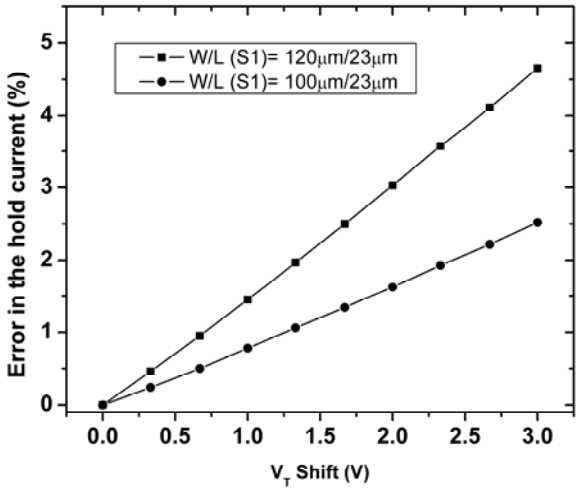


Figure 3.3: Error in the OLED current caused by the V_T-dependent charge injection as a function of the V_T shift.

$$\Delta I_{error} = \left(g_m \frac{C_{GS2}}{C_{GS1} + C_{GS2} + C_S} - g_{ds} \right) \Delta V_{T1} - g_{ds} \Delta V_{OLED} - IR_{DSW3} \frac{\Delta V_{T3}}{(V_{ON} - V_{T3})}. \quad (3.9)$$

Equation (3.9) provides several design constrains to reduce the dependence of the error in the pixel current on the V_T and V_{OLED}. To reduce the effect of V_{T1}, the size switch S2 must be selected small such that C_{GS2} becomes much smaller than the storage capacitor C_S. The effect of ΔV_{OLED} is

minimized by reducing g_{ds} by biasing T1 deeply in the saturation region. The effect of ΔV_{T3} can be reduced by reducing the value of R_{DSW3} by increasing V_{selh} or increasing the size of S3. Equation (3.9) also predicts the trend of the change in the current, as the threshold voltages increases. As can be seen, although the V_T-dependent charge injection of S2 increases the pixel current, the effect of S3 reduces the current. Moreover, the increment of the OLED voltage reduces the current. For the pixel circuit in Fig. 3.2 (b), (3.9) has to be modified to

$$\Delta I_{error} = \left(g_m \frac{C_{GS2}}{C_{GS1} + C_{GS2} + C_S} - g_{ds} \right) \Delta V_{T1} - \left(g_m \frac{C_{GS2}}{C_{GS1} + C_{GS2} + C_S} + g_{ds} \right) \Delta V_{OLED} - I R_{DSW3} \frac{\Delta V_{T3}}{(V_{ON} - V_{T3})}, \qquad (3.10)$$

since the OLED is in the source of the drive TFT in this circuit. For the circuit in Fig. 3.2 (c), the error in the current is given by

$$\Delta I_{error} = -\left(g_m \frac{C_{OV1} + C_{OV2}}{C_{GS1} + C_{GS2} + C_S} + g_{ds} \right) \Delta V_{T1} - g_{ds} \Delta V_{OLED} \qquad (3.11)$$

where C_{OV1} and C_{OV2} are the gate-drain overlap capacitors of T1 and T2,respectively.

3.1.2 Settling Time in CPPCs

Although current-programmed AMOLED pixel circuits have demonstrated a reasonable stability [56][59][64], their use in AMOLED displays are hindered by the long settling time of the programming current due to low mobility of the TFTs and the large parasitic capacitance of the data line. In particular, for small currents, the settling time can be far longer than the programming times required for high-resolution displays. This signifies the demand for a detailed study of the current settling in CPPCs and finding methods to improve the settling behaviour. To obtain an overview about the issue, a simplified analytical model is presented. Then, a detailed model is introduced and used to optimize the settling time.

3.1.2.1 Analytical Model

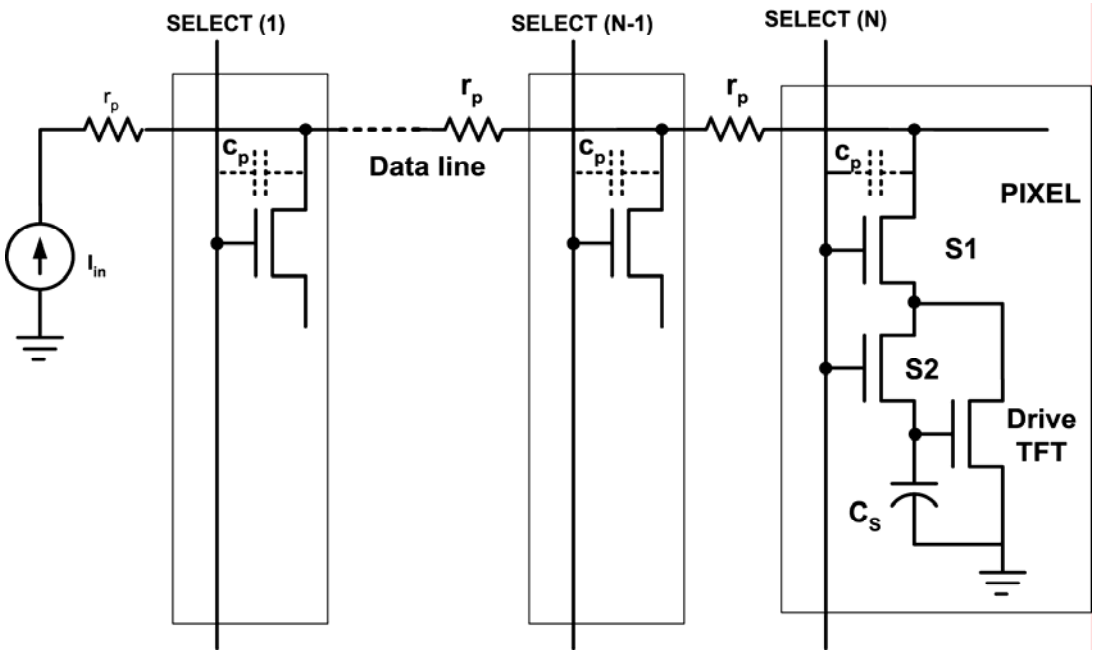


Figure 3.4: Detailed model of a CPPC during the programming cycle.

During the programming cycle, a CPPC is modelled as a diode-connected TFT and a storage capacitor (C_S) in series with a switching TFT as indicated in Fig. 3.4. All of the pixels in the same column add a parasitic capacitor (c_P) to the data line. This capacitor is associated with the gate-drain overlap capacitor of the switching TFTs in each pixel and the overlap between column and row lines. The overall effect of the series resistance of the data line associated with each pixel (r_p) is negligible compared to the high series resistance of the TFTs in the pixel circuit [43].

Even by neglecting the effect of r_p, the settling of the programming current in the circuit in Fig. 3.4 cannot be solved analytically. To achieve an analytical solution, the model in Fig. 3.4 is simplified to a circuit consisting of a diode-connected TFT (T1), an equivalent parasitic capacitance (C_P), and a current source, as shown in Fig. 3.5. The model neglects the effect of the series switch TFT which has a noticeable effect on the settling time. However, the model represents the current-dependent settling

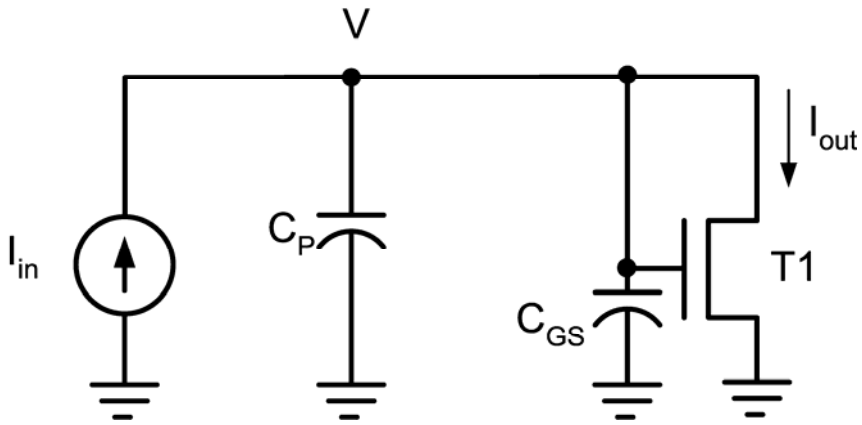


Figure 3.5: Simplified model of current programming used for the analysis.

behaviour of the CPPCs and provides an estimation of the settling time. The current of the pixel is described by the following equations:

$$I_{in}(t) = (C_P + C_{GS})\frac{dV}{dt} + K(V - V_T)^2, V > V_T, \tag{3.12}$$

$$I_{out} = \frac{1}{2}K(V - V_T)^2, V > V_T. \tag{3.13}$$

Here, C_P is the total parasitic capacitance of the data line. C_{GS} is the total capacitance of the pixel circuit and is the sum of the C_S and the gate-source capacitance of the TFT. By assuming that the data line is precharged to V_T at the beginning of programming cycle, the pixel current is expressed as

$$I_{out} = I_{in}\left(\frac{1 - \exp\left(-\frac{t}{\tau}\right)}{1 + \exp\left(-\frac{t}{\tau}\right)}\right)^2, \tag{3.14}$$

where τ is given by

$$\tau = \frac{C_P + C_{GS}}{\sqrt{2\mu.c_i\frac{W}{L}I_{in}}}. \tag{3.15}$$

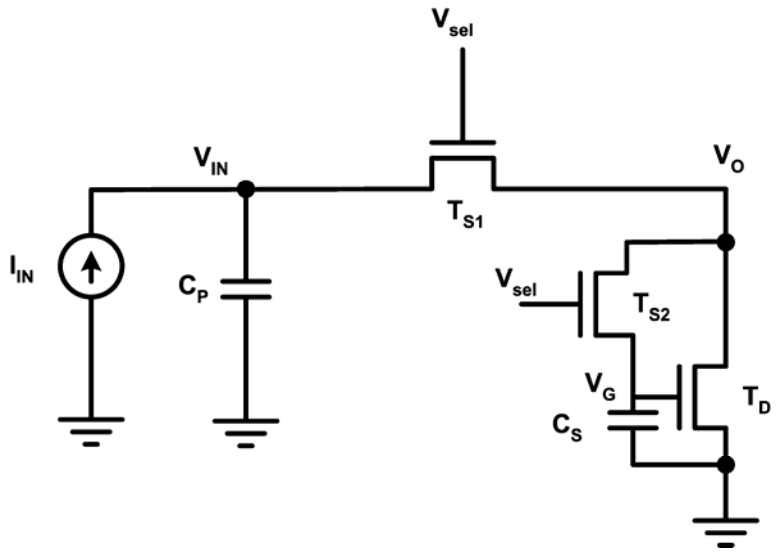


Figure 3.6: Detailed model used to estimate the settling time in CPPCs.

As can be seen, the time constant of the settling time is proportional to C_P and inversely proportional to the square root of the mobility and programming current. Thus, at small programming currents, CPPCs have long settling times.

3.1.2.2 Model for Numerical Simulation

To study the effect of the circuit parameters on the settling time and feasibility study of a-Si TFT CPPCs in different display applications, a circuit is derived from the detailed model in Fig. 3.4 and simulated numerically by MATLAB. Fig. 3.6 shows the equivalent circuit used for the simulations. T_D is the drive TFT. T_{S1} and T_{S2} are the switching TFTs. C_P is calculated by

$$C_P = NC_i\left(W_{S1}L_{OV} + A_{OV}\right) \tag{3.16}$$

where N is the number of rows, and A_{OV} is the total overlap area between the row and column lines for each pixel. W_{S1} is the width of T_{S1}, and L_{OV} is the length of the gate-drain overlap of T_{S1}. A simplified model for the settling of the current in T_D is given by solving the following:

Table 3.2: Circuit and device parameters used to simulate the circuit in Fig. 3.6.

Parameter	Description	Value
C_i	Insulator capacitance per unit area	20 nF /cm
μ	Field effect mobility	1 cm^2/Vs
L	Length of TFTs	5 μm
L_{OV}	Gate-drain overlap	3 μm
N	Number of rows	200
I_{IN}	Current range	50 nA to 500 nA
A_{OV}	Overlap area between the row and column	10 μm X 10 μm
C_S	Storage capacitor	250 fF
V_{SEL}	Select voltage	30 V
V_T	Threshold voltage	3 V
$V_{in}(0)$	Initial line voltage	3 V

$$C_P \frac{dV_{IN}}{dt} + K_1(V_{SEL} - V_O - V_{T1})(V_{IN} - V_O) - I_{IN} = 0 \tag{3.17}$$

$$C_G \frac{dV_G}{dt} - K_2(V_{SEL} - V_G - V_{T2})(V_O - V_G) = 0 \tag{3.18}$$

$$K_1(V_{SEL} - V_O - V_{T1})(V_{IN} - V_O) - K_2(V_{SEL} - V_G - V_{T2})(V_O - V_G) - \frac{1}{2}K_3(V_G - V_{T3})^2 . \tag{3.19}$$

Here, V_{T1}, V_{T2}, V_{T3}, K_1, K_2, and K_3 are the threshold voltages and the transconductance coefficients of T_{S1}, T_{S2}, and T_D, respectively. C_G is the sum of the storage capacitor (C_S) and the gate source capacitance of T_D. V_{SEL} is the voltage of the select line, and I_{IN} is the input current. V_O, V_{IN}, and V_G voltages are shown in the Fig. 3.6. Table 3.2 is a summary of the circuit parameters that are used for the simulations. The TFT parameters are based on a typical industrial a-Si TFT process. The display parameters are chosen based on a top-emission 2-3 inch display for mobile applications.

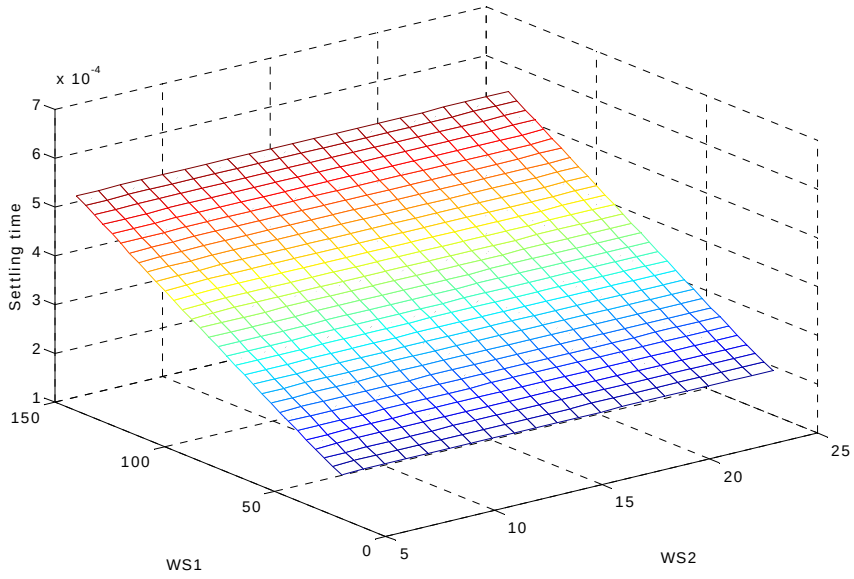


Figure 3.7: Settling time for different sizes of T_{S1} and T_{S2} switches.

3.1.2.3 Effects of T_{S1}, T_{S2}, and T_D

The effect of the size of T_{S1} and T_{S2} (W_{S1} and W_{S2}) on the settling time is investigated. Fig. 3.7 shows the settling time as a function of W_{S1} and W_{S2} for W_D=150 μm and I_{IN}=50 nA. Evidently, W_{S2} does not considerably affect the settling time. W_{S1} has a significant effect on the settling time, since it directly affects the size of C_P. Fig. 3.8 depicts the settling time as a function of the W_{S1} and W_D for a 50 nA programming current. As can be seen, reducing the size of T_{S1} reduces the settling time. The settling time is shorter for a larger size of T_D due to an increase in the transconductance seen by the current source. However, due to the limited area of a pixel, the maximum size of T_D is limited.

3.1.2.4 Optimizing the size of T_{S1}

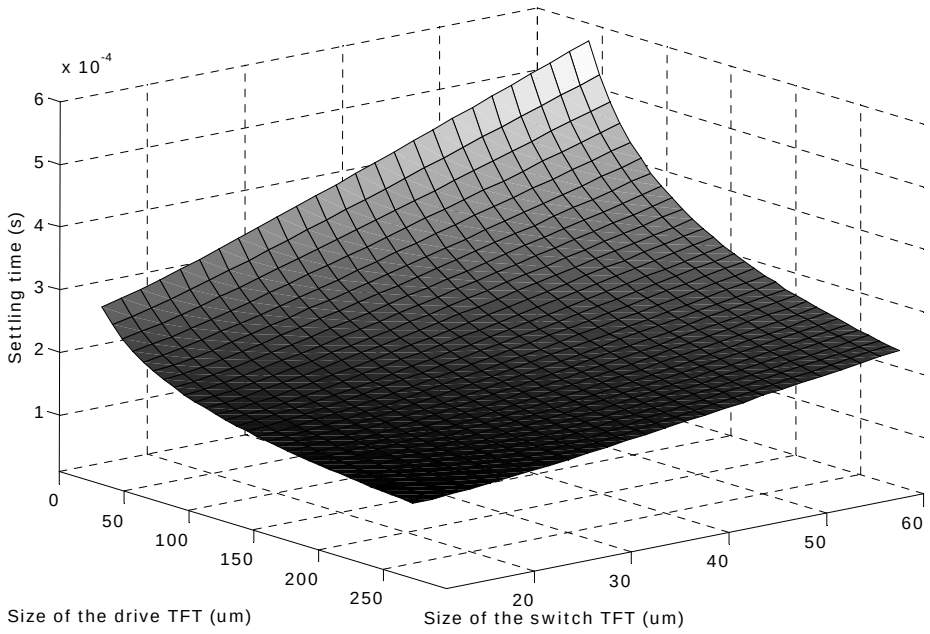


Figure 3.8: Settling time for different sizes of T_{S1} and T_D.

From the Fig. 3.7 and Fig 3.8 it can be seen that reducing W_{S1} reduces the settling time. However, W_{S1} should be large enough such that V_{IN} does not exceed the maximum tolerable voltage of the external current source (V_{S_MAX}). To satisfy this condition, the minimum size for T_{S1} (W_{S1_Min}) should be equal to

$$W_{S1\_Min} = \frac{LI_{IN\_MAX}}{\mu C_i (V_{SEL} - V_{T1} - V_{TD})(V_{S\_MAX} - V_{T3} - V_{TD})}. \tag{3.20}$$

Here, I_{IN_MAX} is the maximum current of a pixel, and V_{TD} is the effective gate-source voltage of T_D for I_{IN_MAX} and is given

$$V_{TD} = \sqrt{\frac{2I_{IN\_MAX}L}{\mu C_i W_D}}. \tag{3.21}$$

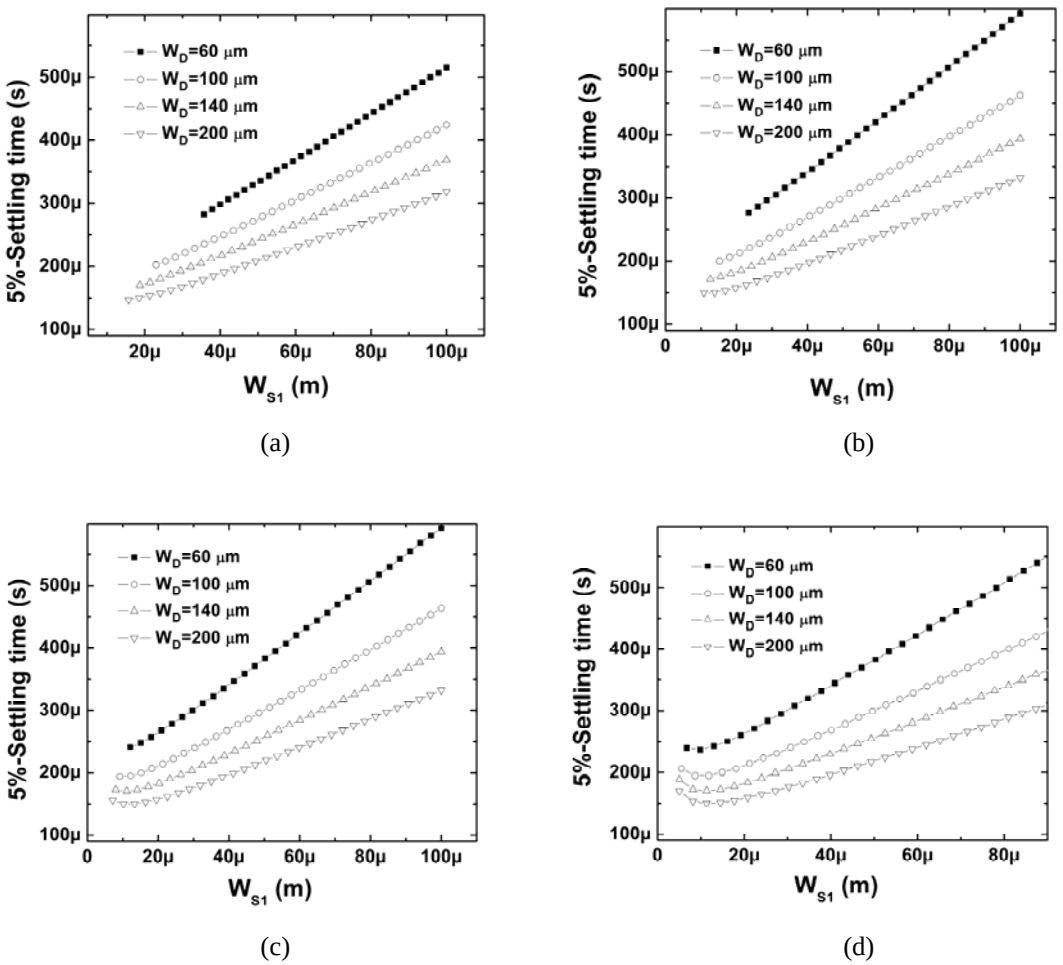


Figure 3.9: Settling time as a function of W_{S1} for different sizes of T_D and different values of V_{S_MAX}:

(a) V_{S_MAX}=10 V, (b) V_{S_MAX}=12 V, (c) V_{S_MAX}=15 V, (d) V_{S_MAX}=20 V.

Simulation results indicate that in some cases, the fastest settling time is not achieved by W_{S1_Min} because reducing the size of T_{S1} increases the resistance seen by C_P. Fig. 3.9 (a)-(d) show the settling time as a function of W_{S1} for a minimum current of 50 nA for different sizes of T_D and different values of V_{S_MAX}. The range of W_{S1} is between 100 μm to T_{S1_Min} for each size of T_D. As can be seen, for the larger values of V_{S_MAX}, and larger W_D, the optimum W_{S1} is slightly larger than W_{S1_Min}. Moreover, the minimum settling time is achieved for the higher values of V_{S_MAX}. However, V_{S_MAX} depends on the technology of the column driver and is not a design factor in some design cases.

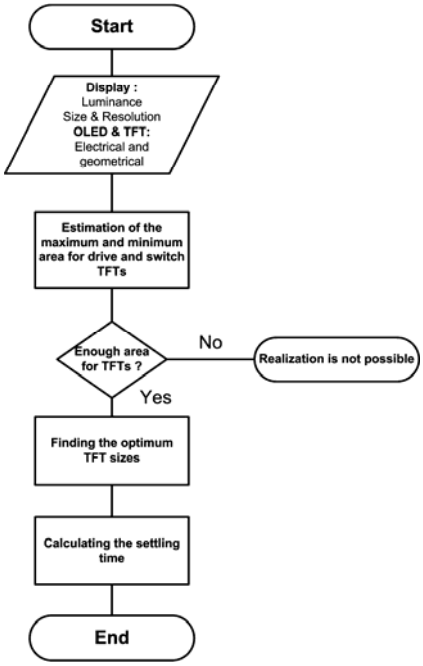


Figure 3.10: The flowchart of the method used to estimate the minimum possible settling time in different display applications.

3.1.2.5 Feasibility Study of the Settling Time in CPPC

From the analysis and the simulations, it can be concluded that the settling time principally depends on the size of the drive and switch TFTs, and the minimum pixel current. These parameters depend on the display parameters such as luminance, resolution, and the size. The minimum required current is determined by the display luminance, the number of the gray scales, and the pixel size. In addition, the size of the drive TFT is limited by the pixel area and the required aperture ratio. The minimum size for the switching TFTs is limited by the maximum operating voltage of the external column driver. In this section, the minimum settling times for different displays are estimated. The flow estimation is illustrated by Fig. 3.10.

At first, the display parameters such as size, resolution, luminance, and the required pixel aperture ratio are gathered for different display applications. After calculating the pixel size, the next step is to

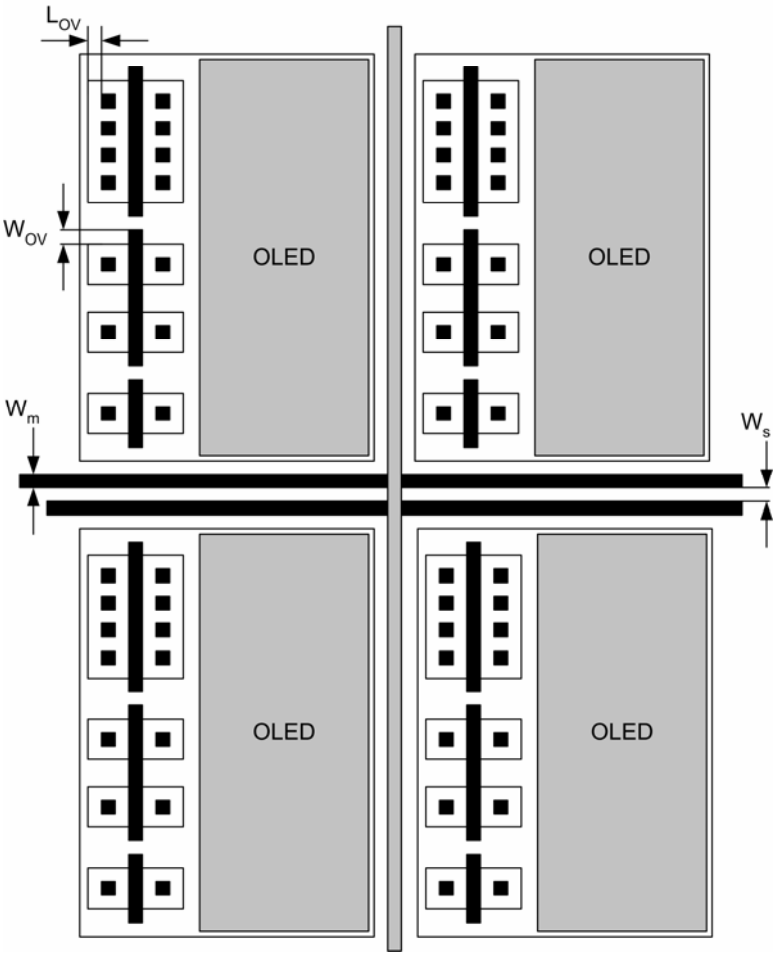


Figure 3.11: Conceptual AMOLED pixel layout for a 4-TFT CPPC.

estimate the available area for the switching and driving TFTs. Although the pixel area depends on the pixel circuit, OLED integration, and layout; the circuit area can be estimated based on the method presented in [17]. The calculations are based on the 4-TFT CPPC in Fig. 3.1 (a). Fig. 3.11 demonstrates a conceptual layout and the associated parameters. The circuit area, A_{CIR}, is then given by

$$\begin{aligned} A_{CIR} &= (W_D + W_{OV})(L + 2L_{OV}) + (W_{S1} + W_{OV})(L + 2L_{OV}) + (W_{S2} + W_{OV})(L + 2L_{OV}) \\ &+ (W_{S3} + W_{OV})(L + 2L_{OV}) + N_i(W_m + W_p)X_{pix} + MiY_{pix}(W_m + W_p) \end{aligned} \tag{3.22}$$

where all the parameters are listed in Table 3.3. From (3.22), the maximum size of the sum of W_D and W_{S1} is calculated. The next step is to find the optimum values for W_D and W_{S1} and determine the

Table 3.3: Definition and estimated values of parameters of the pixel layout of Fig. 3.11.

Parameter	Description	Value
W_D	Width of the drive TFT	Variable
W_{S1}	Width of the main switching TFT	Variable
W_{S2}	Width of the gate-source switching TFT	5 μm
W_{S3}	Width of the current-path switching TFT	5 μm
W_{OV}	Width overhead due to the gate contact region of the TFT	5 μm
L	Length of the TFTs	5 μm
L_{OV}	Length overhead due the source/drain contact region of the TFT	5 μm
W_m	Width of interconnect	5 μm
W_p	Spacing between interconnect lines	5 μm
X_{pix}	Length of pixel	Variable
Y_{pix}	Width of pixel	Variable
N_i	Number of row interconnect lines	2
M_i	Number of column interconnect lines	1

settling time. Table 3.4 summarizes the simulated settling times for some display applications. In addition, it exhibits some primary parameters of the display, and the available programming time.

For all of the displays, except QCIF, the settling time exceeds the maximum programming time allowed. This is more noticeable for high-resolution displays due to the existence of a larger parasitic capacitance. It is noteworthy that in the simulations, the effect of parasitic capacitances generated by the external column driver and the associated interconnections is neglected. Therefore, longer settling times are expected for a complete display system.

Table 3.4: Estimated settling times of current-programmed pixel circuits in different displays.

Display parameter	QCIF (Mobile)	QVGA (PDA)	XVGA (Monitor)
Luminance (cd/m^2)	100	200	1000
Resolution	144×176	240×320	768×1024
Display size (inch)	2	4	17
Aperture ratio	40%	40%	60%
Maximum pixel current (nA)	315	415	2200
Maximum settling time 5% (μs)	76	98	182
Required Programming time (μs)	110	70	20

3.1.3 Methods of Increasing the Programming Speed in CPPCs

From the results in Table 3.4, it is evident that conventional current programming fails to satisfy the settling time requirements of high-resolution AMOLED displays. As a result, despite a reasonable current stability, it is not considered as a practical solution for a-Si TFT technology. Due to the higher mobility of polysilicon TFTs, current programming is a more practical driving scheme to compensate for variations of the V_T. However, even in polysilicon TFT technology, current programming suffers from large settling times [67]. Several driving schemes have been presented to overcome the issue. These schemes are categorized as current scaling, current offset, and precharging.

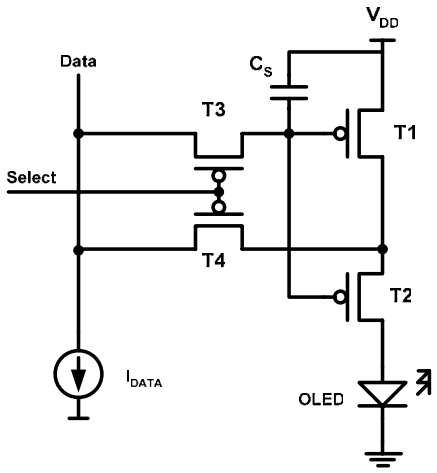


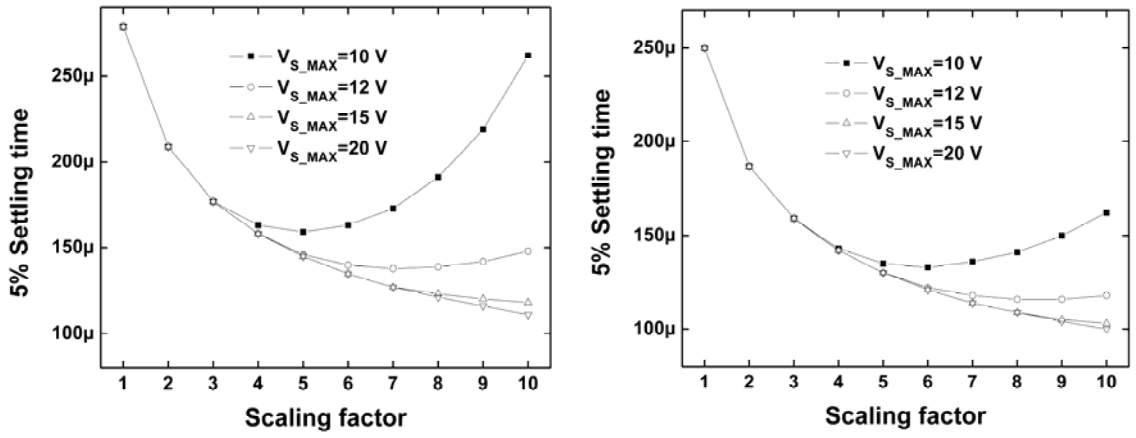
Figure 3.12: Current scaling in a non-mirrored CPPC [65].

3.1.3.1 Current Scaling

As shown by (3.15), the settling time in CPPCs decreases if the programming current increases. Therefore, by scaling down the current inside the pixel, it should be possible to increase the programming current and hence, reduce the settling time [65][66]. Scaling of the programming current is readily performed easily in a mirrored CPPC by using TFTs with different sizes in the current mirror. The scaling factor (*SF*) which is defined as the ratio of the programming current to the OLED current is given by the ratio of the reference TFT to the drive TFT. Fig 3.12 shows a non-mirrored pixel circuit with current scaling [65].The circuit is implemented with polysilicon TFTs but it can be easily modified for a-Si TFT technology. The scaling factor in this circuit is given by

$$SF = \frac{K_2}{K_1 + K_2} = \frac{W_2}{W_1 + W_2} \tag{3.23}$$

where K_1 and K_2 are the transconductance coefficients, and W_1 and W_2 are the channel width of T1 and T2, respectively. The effect of the current scaling on the settling time is simulated by the model in Fig. 3.6 for W_D=150 μm and 200 μm. For each V_{S_MAX} and scaling factor, the W_{S1_min} is calculated. If W_{S1} is larger than W_{S1_min}, the optimum value for W_{S1} is found, and the associated settling time for a programming current equal to I_{IN_MAX}/32 is calculated. Fig. 3.13 shows the settling time as a function



(a) (b)

Figure 3.13: Settling time as a function of the scaling factor in a current scaling CPPC: (a) W_D= 150 µm, (b) W_D= 200µm.

of the scaling factor for different values of V_{S_MAX}. As can be seen, the rate of improvement in the current settling decreases for larger scaling factors, in particular, for smaller values of V_{S_MAX}. By increasing the scaling factor (and thus increasing the programming current), a larger W_{S1} is required to ensure that V_{IN} does not exceed V_{S_MAX}. As a result, C_P also is increased, resulting in a larger settling time.

3.1.3.2 Current Offset

Another method for improving the settling is to add a constant current to the data current during the programming cycle, and then subtract the current inside the pixel. Fig. 3.14 shows a CPPC with on-pixel current subtraction [67]. Here, the subtraction is performed by applying a pulse through the acceleration control line to the storage capacitor (C_S) at the end of the programming cycle. The circuit shown here is implemented with p-channel TFTs in polysilicon technology; however, the n-channel dual of the circuit can be implemented by a-Si TFTs.

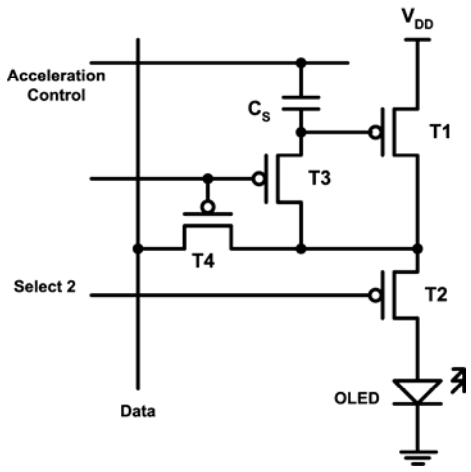


Figure 3.14: CPPC with current offset [67].

The current offset scheme is more efficient than current scaling, since it considerably increases the programming current at low gray scales. For example, if the maximum OLED current is 0.5 μA, then for a 32-level gray scale, the minimum programming current is 15.6 nA. By scaling the current by a factor of 2, the maximum current is 1.0 μA, and the minimum programming current increases to 31.2 nA. By using a 0.5 μA offset current, the maximum current is still 1.0 μA however, the minimum current is increased to 0.5156 μA, which is more than 16.5 times larger than that in the current scaling scheme. The current offset scheme is investigated by using the optimization method described in section 3.1.2.5 and the same circuit parameters. Fig. 3.15 shows the settling time as a function of the offset current for different values of V_{S_MAX}. As can be seen, there is an abrupt reduction in the settling time when the offset current is not zero. Settling times smaller than 50 μs (a reduction of more than 5 times) can be achieved by the current offset scheme. Similar to the current scaling, for smaller values of V_{S_MAX}, the settling time increases due to the large sizes required for W_{S1}. Despite the effectiveness of the current offset scheme in the reduction of the settling time, the OLED current in CPPCs with on-pixel current subtraction is sensitive to the mobility of the TFTs, and hence, to the temperature.

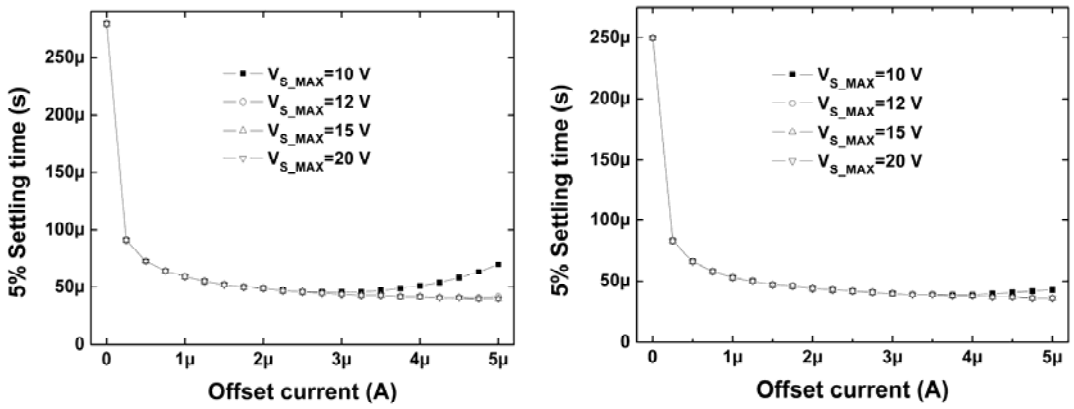


Figure 3.15: Settling time in s CPPC with current offset as a function of offset current for different values of V_{S_MAX}: (a) W_D=150 μm, (b) W_D=200 μm.

Moreover, the exact control on the OLED current is difficult. Calibration is also necessary, since the OLED current depends on the absolute values of the TFT parameters.

3.1.3.3 Precharging

Precharging the data line is another method for improving the settling time in CPPCs which is already used in PMOLED drivers. In this technique, a voltage close to the final line voltage associated with the programming current, is applied to the data line before the programming cycle to reduce the settling time.

Fig. 3.16 shows the settling time as a function of the precharge voltage and programming current for W_D=150 μm and W_{SI}=50 μm. For more clarity, the settling time as a function of the precharge voltage is shown in Fig. 3.17 for some specific programming currents. It is readily seen that if the line is precharged properly, the settling time is substantially reduced.

The key advantage of precharging is that no modification in the design of the CPPCs is required, and the process is performed by the external column driver. However, the design of the external column driver with the precharging capability is more complicated. For each programming current, the column driver needs to store the associated precharge voltage. In addition, as the V_T of the drive

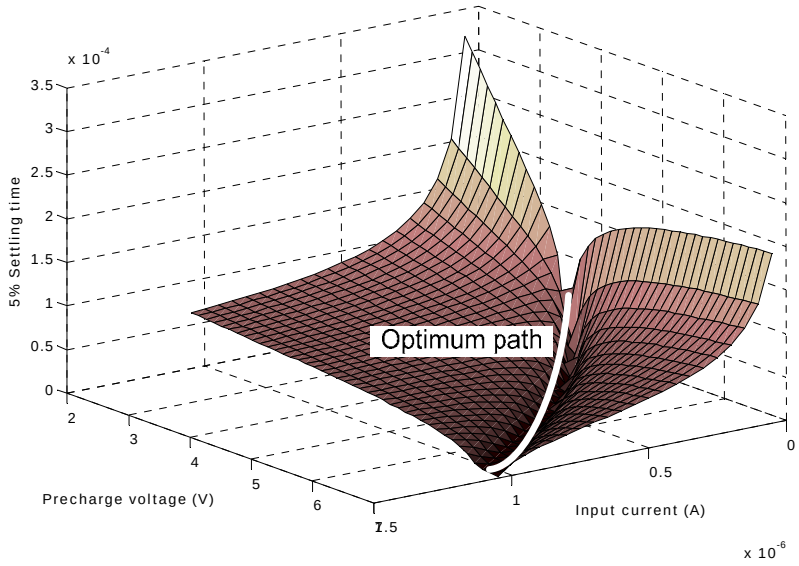


Figure 3.16: Settling time as a function of the precharge voltage and programming current.

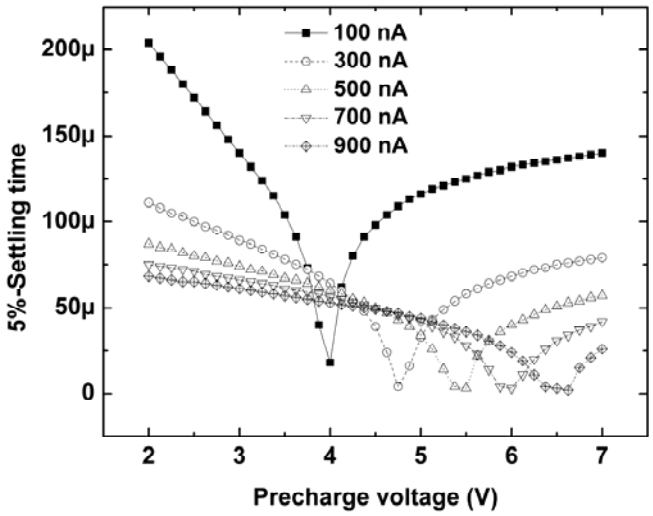


Figure 3.17: Settling time as a function of the precharge voltage for specific programming currents.

TFT shifts, the required precharge voltage increases. As a result, the performance of the precharging degrades over time, if the lines are precharged with constant voltages. One solution is to dynamically measure the V_T shift of each pixel during the programming time and correct the original precharge

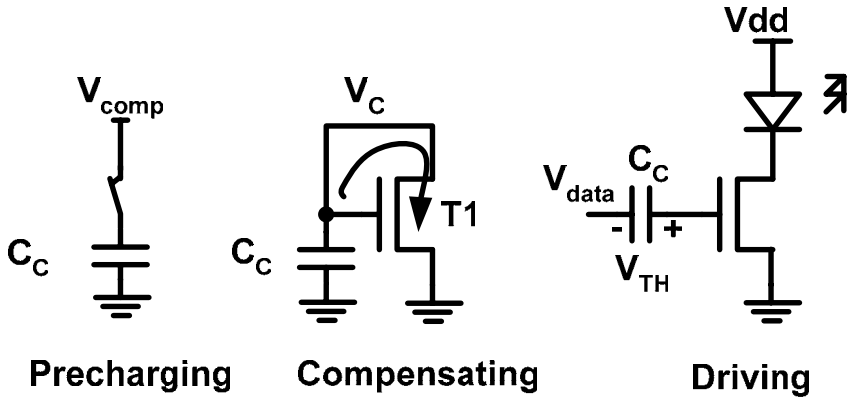


Figure 3.18: Operation of a voltage-programmed pixel circuit.

voltages [71]. However, this requires a complicated system with a complex processing and memory capabilities that are not cost effective.

3.2 Voltage Programming

In the voltage programming driving scheme, the luminance data is a voltage. The compensation for the V_T shift is performed by on-pixel measuring of the V_T, and adding it to the programming voltage. Fig. 3.18 illustrates the operation of this driving scheme.

The programming cycle starts by precharging a capacitor (C_C) to a voltage larger than V_T of the drive TFT (T1). During the compensating phase, C_C is connected to the gate of T1 while T1 is diode-connected. As a result, the capacitor discharges through T1, and the capacitor voltage (V_C) degrades until it is close to V_T. At the driving cycle, the programming voltage (V_{DATA}) is added to the voltage of the capacitor, thus, a gate-source voltage close to V_T+V_{DATA} is applied to T1. If T1 is in the saturation region, the current through T1 is independent of V_T and is given by

$$I_{out} = \frac{1}{2}K\left(V_{DATA} + V_T - V_T\right)^2 = \frac{1}{2}KV_{DATA}{}^2 . \tag{3.24}$$

Several circuit implementations of the voltage-programmed pixel circuits (VPPCs) in both a-Si and poly silicon TFTs have been reported [72]-[77]. Fig 3.19 illustrates two pixel circuits and the

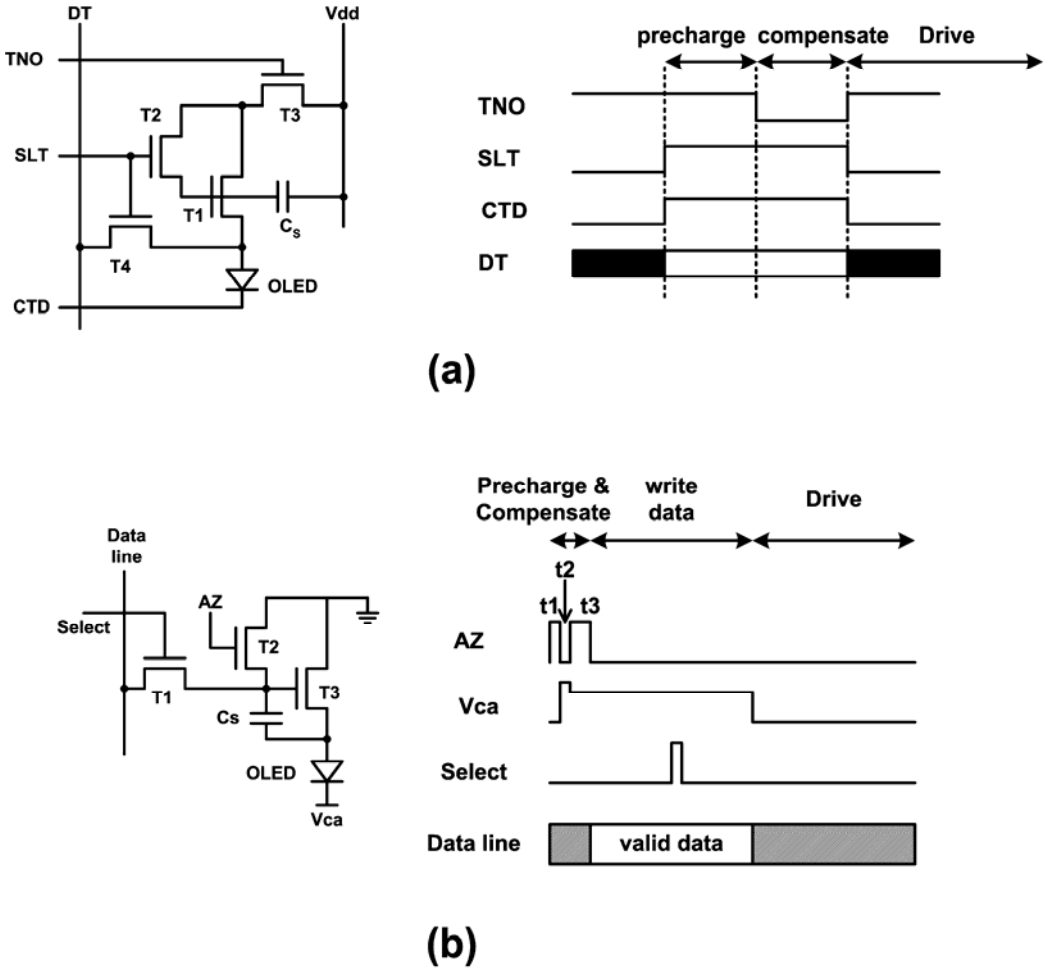


Figure 3.19: Samples of the voltage programmed pixel circuits: (a) 4-TFT [73] (b) 3-TFT [75].

associated controlling signals that represent two categories of the VPPCs. The operation of the 4-TFT VPPCs shown in Fig 3.19 (a) is similar to the operation illustrated in Fig. 3.18. Here, DT is the data signal, and TNO, SLT, and CDT are select signals. During the precharging phase, TNO, SLT, and CTD are high, turning T1 to T4 on and the OLED off. As a result, the gate of T1 is charged to a voltage higher than $V_{data}+V_{T1}$, where V_{data} is the data voltage on DT. During the compensating phase TNO is low turning T3 off. Consequently, C_S is discharged through T1 until the gate of T1 reaches to a voltage close to $V_{data}+V_{T1}$. During the drive cycle, TNO is high, and SLT and CTD are low. As a result, T1 current starts flowing into the OLED.

The pixel circuit in Fig. 3.19 (b) has only three TFTs and three select lines; however, the circuit operation is more complicated. At the beginning of the precharge phase, (t_1), AZ goes high and V_{CA} is a negative voltage. Consequently, a high current passes through T3 and a voltage higher than V_{T3} is stored in C_S. Then AZ goes low and V_{CA} is set to a high positive voltage. As a result, OLED is reversely biased. During the compensation phase (t_3), AZ rises and the voltage of V_{AC} is set to zero. Therefore, C_S is discharged through T3 until its potential reaches to V_{T3}. Since the OLED capacitance at the reverse bias (C_{OLED}) is much larger than C_S, the potential across the OLED changes very little. During the data writing phase, for a short time, the select line goes high, applying the data voltage on the gate of T3. A capacitive voltage divider is formed by the C_S and C_{OLED}. Since C_{OLED} is much larger than C_S, its final voltage does not change a lot, and remains close to $-V_{T3}$. C_S voltage however, becomes equal to $V_{T3}+V_{data}$. During the drive cycle, V_{CA} is set to a negative voltage. Consequently, the current through T3, begins to flow into the OLED. Since the gate-source voltage of T3 is $V_{T3}+V_{data}$, the pixel circuit compensates for the V_T shift in T3, as described by (3.24).

3.2.1 Tradeoff between Programming Time and Stability

Since the data signal is voltage, in the VPPCs, the large parasitic capacitance of the data line does not have a significant effect on the settling time. Similar to the conventional 2-TFT pixel circuit described in Chapter 2, the settling time of the data voltage (V_{data}) is primarily determined by the resistance of the pixel switch and the storage capacitor. For a nominal switch resistance of 1 MΩ and a storage capacitor of 1 pF, the time constant of the programming is less than 2 μs.

The programming time in the VPPCs is limited by the compensation phase, at which the storage capacitor is discharged by the diode-connected drive TFT. Due to the low transconductance of the TFT, discharging of the compensating capacitor is slow and at the end of the compensating phase the voltage of the compensating capacitor (V_C) does not reach to V_T. For the circuit shown in Fig. 3.18, V_C is calculated by the following equation:

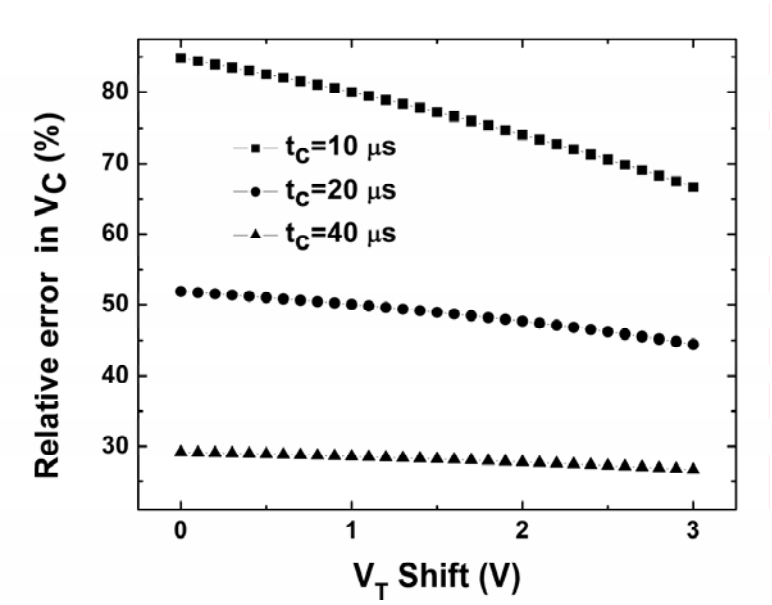


Figure 3.20: Relative error in V_C as a function of the V_T shift in T1 for different values of t_c.

$$C_C \frac{dV_C}{dt} + \frac{1}{2} K (V_C - V_T)^2 = 0 . \tag{3.25}$$

The solution of (3.25) for V_C is

$$V_C = V_T + \frac{V_{comp} - V_T}{(V_{comp} - V_T)\frac{K}{2C} t_c + 1}, \tag{3.26}$$

where t_c is the duration of the compensation cycle, and V_{comp} is the precharging voltage. The second term in (3.26) is the error of the compensation and depends on V_T. The dependence of V_C on the V_T causes error in the drive current of T1 as the V_T shifts. To reduce the error, t_c must be large; however, the maximum length of t_c is limited by the programming time of the display system. Fig. 3.20 shows the error at the end of the compensating phase as a function of the V_T shift in T1 for different values of t_c. Here, C_C is 1 pF, and V_{comp} is 10 V. The variations in the error for the 3-V V_T shift are 18%, 7.5%, and 2.5% for t_c values of 10 μs, 20 μs, and 40 μs, respectively. It is observed that, especially for smaller compensating times, the error in the compensating voltage depends considerably on the V_T.

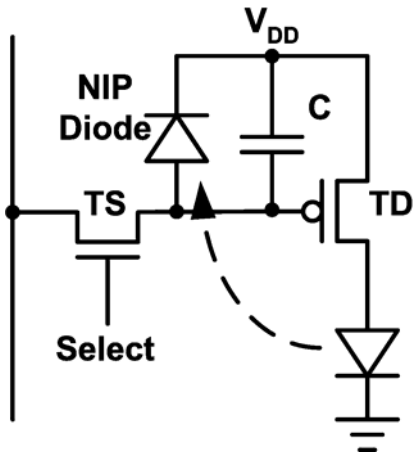


Figure 3.21: 2-TFT AMOLED pixel with optical feedback [78].

3.3 Optical Feedback

Most of the previous driving schemes compensate for the V_T shift in the TFTs, but cannot compensate for the degradation of the OLED luminance. Pixel circuits with in-pixel optical feedback are promising, since they can directly control the luminance of the OLED and compensate for the TFT and OLED degradation [78]-[80]. Fig 3.21 is a schematic of a simple AMOLED pixel circuit with optical feedback [78]. The circuit is a conventional 2-TFT pixel with an N-I-P photo diode in parallel with the storage capacitor. A portion of the OLED light is directed to the N-I-P diode. The N-I-P diode is in the reverse bias and has a small reverse current. When it is illuminated by the OLED, the reverse current significantly increases, resulting in the partial discharge of the storage capacitor, *C*. Discharge of *C* during the driving cycle, results in a lower average drive voltage on the driving TFT (TD), and thus, a lower OLED luminance. Degradation of the OLED luminance reduces the reverse current of the N-I-P diode, reducing the rate of the discharge of *C*. As a result, the average driving voltage of TD increases, resulting in a higher current for the OLED.

A circuit analysis provides more information about the circuit [80]. During the driving cycle, the currents at the gate of the TD are described by the following equation:

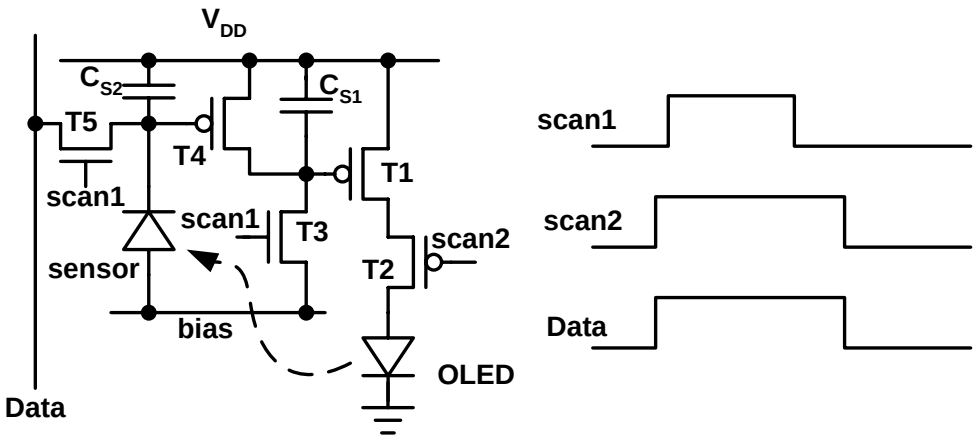


Figure 3.22: Modified AMOLED pixel circuit with optical feedback [79].

$$C\frac{dV}{dt} = -I_P = -\eta_{PD}A_{PD}\frac{\eta_{LED}}{A_{LED}}I(t) = -\eta_{PD}A_{PD}\frac{\eta_{LED}}{A_{LED}}\frac{1}{2}K\left(V(t)-V_T\right)^2, \tag{3.27}$$

where I_P is the photocurrent of the N-I-P diode, A_{PD} and η_{PD} are the area and the efficiency of the diode, respectively, A_{OLED} and η_{OLED} are the OLED area and efficiency. By integrating (3.27), $V(t)$ and $I(t)$ can be found. By integrating the OLED luminance over a frame time, the average luminance is found by the following:

$$L_{ave} = \frac{C}{\eta_{PD}A_{PD}T}\left[V(0)-V_T\right]\frac{T/\tau}{1+T/\tau} \tag{3.28}$$

where $V(0)$ is the initial programming voltage and τ is given by

$$\tau = \frac{2CA_{OLED}}{\eta_{OLED}\eta_{PD}A_{PD}K\left[V(0)-V_T\right]}. \tag{3.29}$$

Since the frame time is much larger than τ, (3.28) is simplified such that

$$L_{ave} = \frac{C}{\eta_{PD}A_{PD}T}\left[V(0)-V_T\right]. \tag{3.30}$$

From (3.30) it can be seen that the average luminance is independent of the OLED parameters and the mobility of TD. However, it has a linear relationship with V_T, which is not desirable. Another drawback of the circuit in Fig. 3.21 is that, compared to a 2-TFT pixel without optical feedback, the

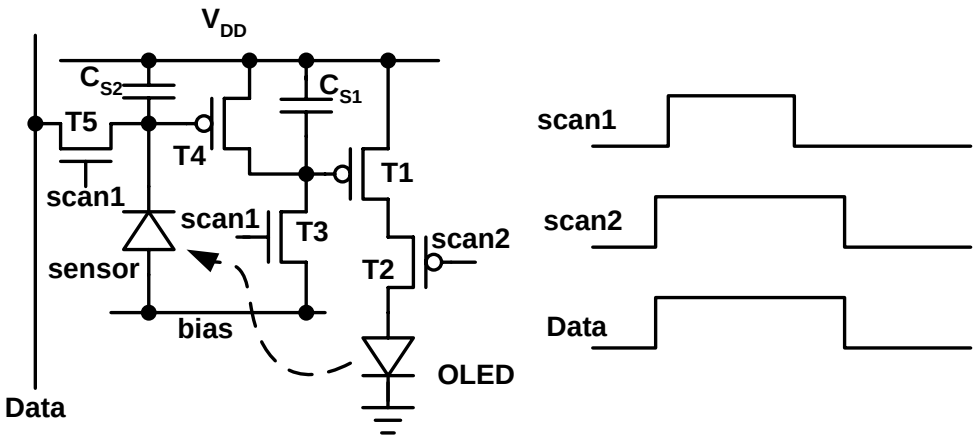


Figure 3.22: Modified AMOLED pixel circuit with optical feedback [79].

$$C\frac{dV}{dt} = -I_P = -\eta_{PD}A_{PD}\frac{\eta_{LED}}{A_{LED}}I(t) = -\eta_{PD}A_{PD}\frac{\eta_{LED}}{A_{LED}}\frac{1}{2}K\left(V(t)-V_T\right)^2, \tag{3.27}$$

where I_P is the photocurrent of the N-I-P diode, A_{PD} and η_{PD} are the area and the efficiency of the diode, respectively, A_{OLED} and η_{OLED} are the OLED area and efficiency. By integrating (3.27), $V(t)$ and $I(t)$ can be found. By integrating the OLED luminance over a frame time, the average luminance is found by the following:

$$L_{ave} = \frac{C}{\eta_{PD}A_{PD}T}\left[V(0)-V_T\right]\frac{T/\tau}{1+T/\tau} \tag{3.28}$$

where $V(0)$ is the initial programming voltage and τ is given by

$$\tau = \frac{2CA_{OLED}}{\eta_{OLED}\eta_{PD}A_{PD}K\left[V(0)-V_T\right]}. \tag{3.29}$$

Since the frame time is much larger than τ, (3.28) is simplified such that

$$L_{ave} = \frac{C}{\eta_{PD}A_{PD}T}\left[V(0)-V_T\right]. \tag{3.30}$$

From (3.30) it can be seen that the average luminance is independent of the OLED parameters and the mobility of TD. However, it has a linear relationship with V_T, which is not desirable. Another drawback of the circuit in Fig. 3.21 is that, compared to a 2-TFT pixel without optical feedback, the

The modified circuit does not require a high programming voltage due to the capability of the circuit to maintain the OLED luminance for as long as the entire frame time. L_{ave} is independent of the V_T of the drive TFT and is related to the V_T of T4. In a-Si TFT technology, the N-I-P photo sensor can be replaced by an a-Si TFT. Although pixel circuits with optical feedback have the advantage of compensating for the OLED degradation, some critical issues exist. First, the OLED luminance depends on the efficiency of the photo sensor. However, the efficiency of the a-Si photo sensors (TFT or N-I-P diodes) degrades over time due to the light-induced defects (Staebler-Wronski Effect) [81]. Moreover, none of the proposed pixels can completely cancel the effect of the V_T shift, therefore, under-compensation or over-compensation of the OLED luminance can occur.

3.3.1 Electrical Feedback for OLED Compensation

As mentioned in Section 2.3.2, when a constant current is applied to an OLED, its voltage increases as the luminance of the OLED decreases. As a result, the shift in the OLED voltage can be used as feedback of the degradation in luminance. Fig. 3.24 shows a pixel circuit that uses ΔV_{OLED} to compensate for the OLED degradation [82]. The circuit operates in three phases: precharging, compensating, and driving. In the precharging phase, SEL1 and SEL2 are high and SEL3 is low, so T1, T3, and T5 are ON, and T4 is OFF. As a result, the gate of T2 (node A) is charged to a potential close to V_{DD}. The voltage of the data line is set to $-V_P+V_{OLEDI}$ where V_P is the programming voltage, and V_{OLEDI} is a constant voltage equal to the initial ON voltage of the OLED.

In the compensating phase, SEL1 goes low, turning T1 off. Consequently, C_S starts discharging through T2 and the OLED until the voltage at node A becomes equal to $V_{T2}+V_{OLED}$. Here, V_{T2} is the threshold voltage of T2, and V_{OLED} is the ON voltage of the OLED. At the end of the compensation phase, the voltage of C_S (V_{CS}) is equal to

$$V_{CS} = V_{T2} + V_{OLED} - V_{OLEDI} + V_P . \tag{3.32}$$

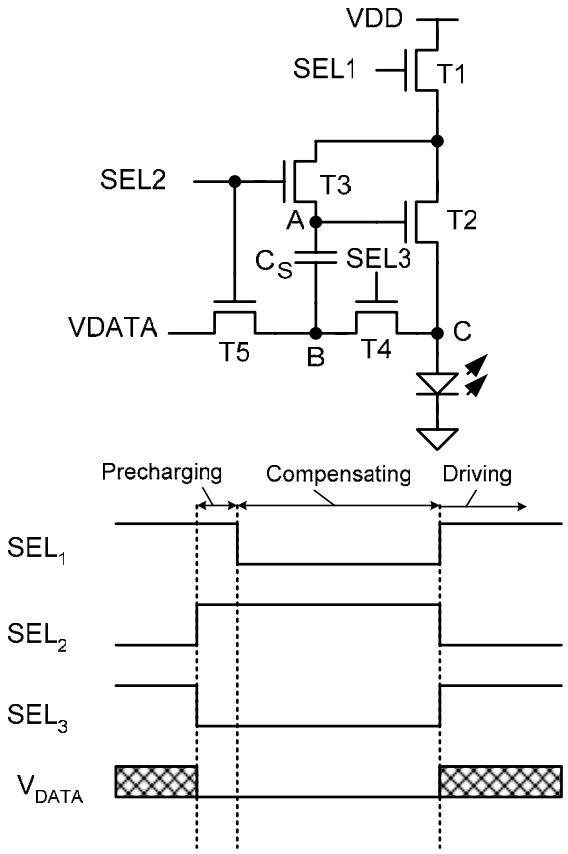


Figure 3.24: Pixel circuit that compensates for OLED degradation by measuring ΔV_{OLED}.

In the driving phase, SEL2 goes low and SEL1 and SEL3 go high, turning T1 and T4 on and T3 and T5 off. As a result, V_{CS} is applied to the gate-source of T2, and thus a current, equal to

$$I_{OUT} = \frac{K}{2}\left(V_P + \Delta V_{OLED}\right)^2 \tag{3.33}$$

flows into the OLED. Here, ΔV_{OLED} is the shift in the voltage of the OLED, and is equal to V_{OLED}-V_{OLEDI}. From (3.33), it can be seen that the OLED driving current increases as ΔV_{OLED} increases over time. Moreover, the current is not dependent on V_{T2}. The pixel circuit is simulated using CADENCE SPECTRE with an a-Si:H TFT model. Fig. 3.25 illustrates the transient waveforms of the OLED current and the voltage at node A, for a programming voltage of 1.3 V for different shifts in the

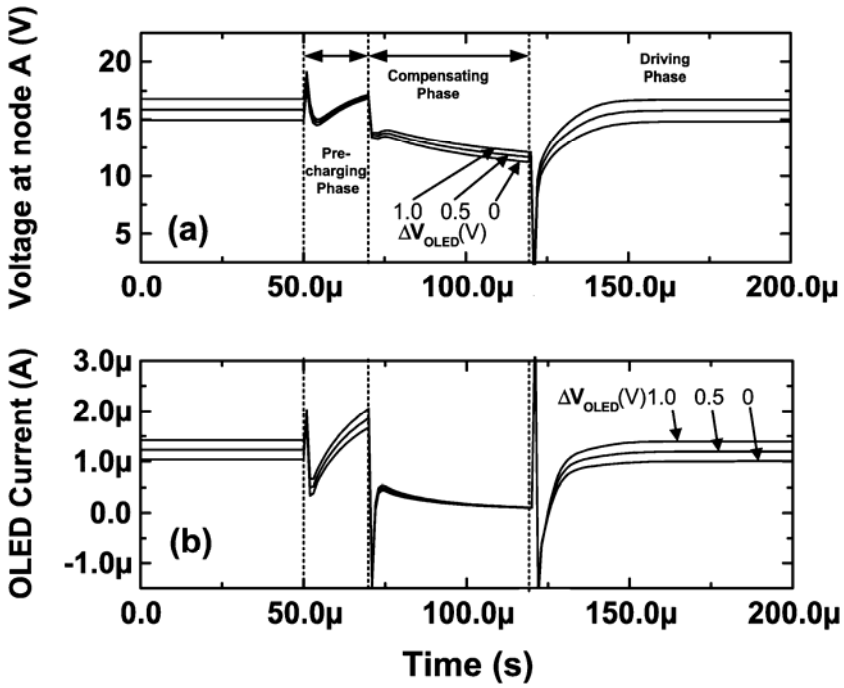


Figure 3.25: Transient waveforms from circuit-level simulations when V_P=1.3 V, ΔV_{OLED} =0, 0.5, and 1.0 V: (a) voltage at node A, (b) OLED current.

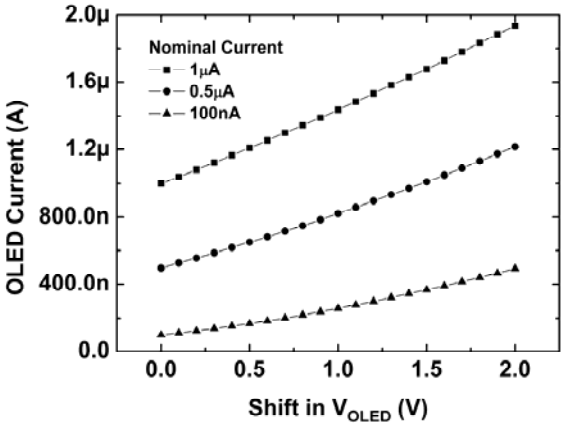


Figure 3.26: OLED current as a function of shift in OLED voltage for different initial OLED currents.

OLED voltage (ΔV_{OLED} =0, 0.5, and 1.0V). As can be seen in Fig. 3.25 (a), at the end of the compensating phase, the voltage at node A is larger for larger ΔV_{OLED} values. Since the increase in the OLED voltage is stored in C_S, the OLED current is higher for a larger ΔV_{OLED}, as indicated in Fig. 3.25 (b). The current impulse at the beginning of the driving phase is due to a rapid change in the

voltage at node C as T4 is turning off. Fig. 3.26 shows the OLED current as a function of ΔV_{OLED}. As can be seen, the circuit effectively increases the OLED current as ΔV_{OLED} increases. For ΔV_{OLED} equal to 2 V, the OLED current increases in excess of 0.9 μA, 0.7 μA, and 300 nA, for initial OLED currents of 1 μA, 0.5 μA, and 100 nA.

3.4 Time-Based Driving Scheme

In a category of AMOLED pixels, time-based gray scaling is used to reduce the average OLED current to the TFT parameters [83][84]. In these circuits, the driving TFT operates like a switch, and the OLED luminance is regulated by controlling its ON to OFF ratio during the frame cycle. Figure 3.27 demonstrates an AMOLED pixel with time-based gray scaling and the controlling signals [83]. The circuit consists of an inverter, three switches, a storage capacitor, and an OLED. The inverter is implemented by two TFTs (T1 and T2) as shown in Fig. 3.27. During the writing cycle, S1 and S2 are ON and S3 is OFF. Since the input and output terminals of the inverter are connected, the voltage at node A, (V_{IN}), is in the transition region of the inverter. When V_{IN}=V_O, both T1 and T2 are in the saturation region. If T1 is large enough to keep V_O less than the ON voltage of the OLED, and the threshold voltages of T1 and T2 are equal, the following equation is satisfied:

$$K_2\left(V_{DD}-V_O-V_T\right)^2 = K_1\left(V_O-V_T\right)^2. \tag{3.34}$$

V_O is then calculated by

$$V_O = V_T + \frac{\sqrt{K_1}}{\sqrt{K_1}-\sqrt{K_2}}V_{DD}, \tag{3.35}$$

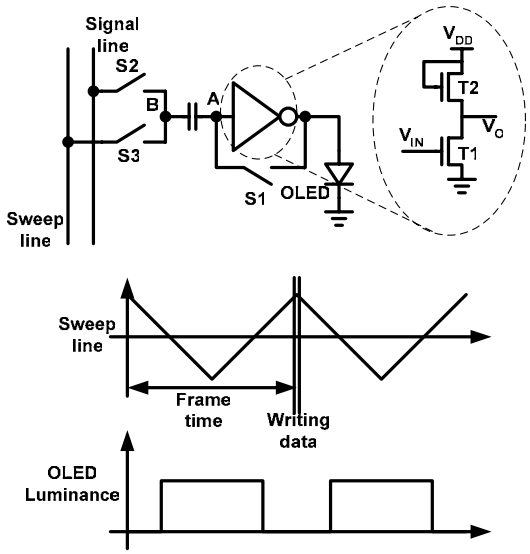


Figure 3.27 AMOLED pixel with time-ratio gray scaling and the associated controlling signals [83].

where K_1 and K_2 are the transconductances of T1 and T2, respectively. The transition voltage is directly proportional to the V_T of T1 and T2. During the writing cycle, the node B is connected to the data voltage (V_{DATA}) thus, a voltage equal to V_{DATA}-V_O is stored in C_S. During the frame cycle, S1 and S2 are turned off and S3 is turned on, connecting node B to the sweep line. A sweep voltage with a triangular shape is applied to node B. The output of the inverter is OFF, until the voltage at node A becomes smaller than the transition voltage. At this point, the state of the inverter output changes to high, turning the OLED on. The OLED remains ON, until the sweep voltage exceeds the transition voltage during the rise time. As implied by (3.35), the pixel circuit can partially compensate for the V_T shift in T1 and T2, since the transition of the inverter, and thus, the luminescent time of the OLED is independent of V_T. However, the OLED current during the ON times is a function of the OLED characteristics and V_T of T2. As a result, the average OLED luminance degrades over time. One possible solution is to replace T2 with an n+ amorphous silicon resistor. However, even in the proposed modified circuit, the OLED current, and therefore, the luminance, depends on the V_{DD} and the ON voltage of the OLED. As a result, a shift in the ON voltage of the OLED causes the OLED

current, and thus the OLED luminance to degrade. Moreover, due to the dependence of the OLED current on V_{DD}, the display luminance is not uniform due to the I-R drop in the V_{DD} line.

3.5 Conclusion

Based on the feasibility study presented in this chapter, current-programmed pixel circuits are not fast enough for high-resolution AMOLED displays. Three methods of improving the settling time in current-programmed pixel circuits are discussed. These methods are current-scaling, current offset and precharging the data line. Among these methods, current offset provides the fastest settling. However, pixel circuits with current offset cannot compensate for mobility variations, and thus, are sensitive to temperature. Voltage driving scheme with on-pixel estimation of V_T shift demonstrates faster programming. However voltage programmed pixel circuits are more sensitive to V_T shift and temperature versions. Pixel circuits with optical feedback have the advantage of compensating for both V_T shift and OLED degradation. However, these pixels suffer from instability of the amorphous silicon photo sensors and inaccurate compensation for V_T shift. Some new driving schemes such as using shift in the OLED voltage as a measure of its luminance degradation are promising but are not still proven by measurement results.

Chapter 4
Driving AMOLED Pixel Circuits with Voltage Feedback

As discussed in the previous chapters, the principal challenges in design of AMOLED pixel circuits in a-Si technology are the instability and low carrier mobility of the TFTs. Therefore, it is crucial to find driving schemes that can provide the OLED with a stable current, and satisfy the programming time requirements of the displays. In the design of analog circuits, negative feedback is extensively used to desensitize the desired circuit parameters, such as gain, to the variations in the values of the circuit components [85]. Negative feedback is also used to reduce the non-linear distortion and to control the transient response of the circuit. These features indicate that feedback can be a promising solution for design of reliable pixel circuits for AMOLED displays. In this chapter, a driving scheme based on feedback that can effectively compensate for the instability of the a-Si TFTs and offers a faster programming, is proposed.

At first, the novel driving scheme and the associated pixel circuits are introduced. Then the performance of the new driving scheme is investigated based on the same AMOLED design considerations, presented in Chapter 2. Measurement results of the fabricated circuits are presented at the end of this chapter.

4.1 Driving AMOLED Pixel Circuits with Feedback

A general diagram of an AMOLED pixel circuit with feedback is shown in Fig. 4.1. It comprises an OLED, a driver circuit, a storage capacitor, a feedback circuit, and some switching components. In addition to the select and data lines, the pixel circuit has a feedback line that transmits a signal associated with the OLED current to the external column driver. This signal is generated by the feedback circuit during the programming cycle. The external (column) driver compares the input data with the feedback signal and generates the proper signal for the OLED driver. The feedback and data

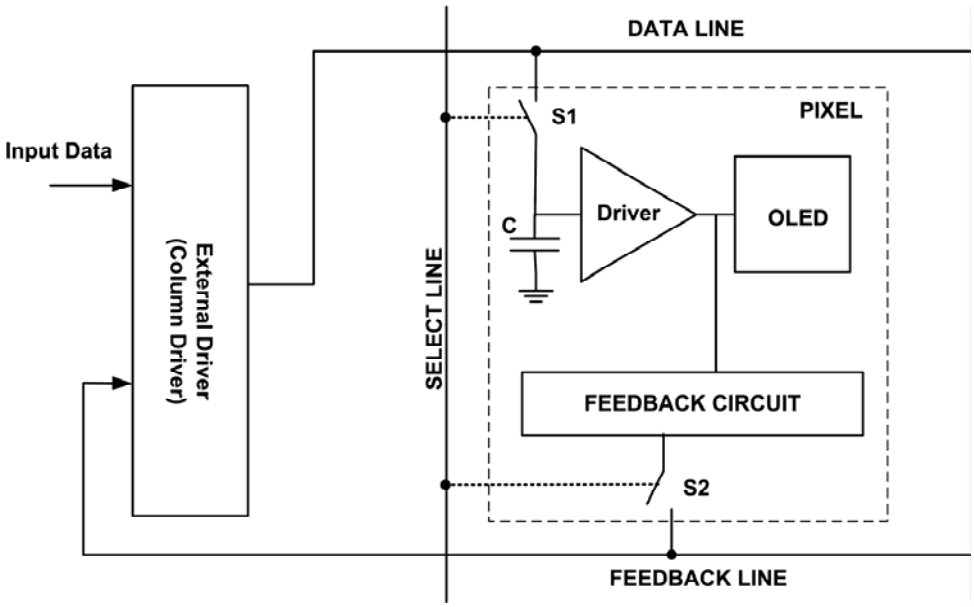


Figure 4.1: General AMOLED pixel circuit with feedback.

lines are shared by all pixels in the same column, as illustrated in Fig 4.2 [86]. In relation to the nature of the feedback signal, the feedback driving schemes are categorized into voltage feedback and current feedback. In this chapter, circuits with voltage feedback are studied.

In an AMOLED pixel circuit with voltage feedback, the OLED current is converted into voltage by a feedback circuit in the pixel. Although the negative feedback reduces the sensitivity of the OLED current to the parameters of TFTs such as V_T, the current-to-voltage converter element in the feedback circuit must be stable, since its absolute value directly affects the OLED current. In addition, the realization of the feedback circuit should be compatible with the TFT process, and should not require extra processing steps or masks. Such a current-to-voltage conversion can be achieved by using a resistor in the current path of the OLED. The resistor can be fabricated by the same n+ a-Si or n+ microcrystalline silicon layer used for contacts of the TFTs. Implementation and characteristics of the n+ resistors is discussed in more detail in Sections 4.3.1.1 and 4.4.

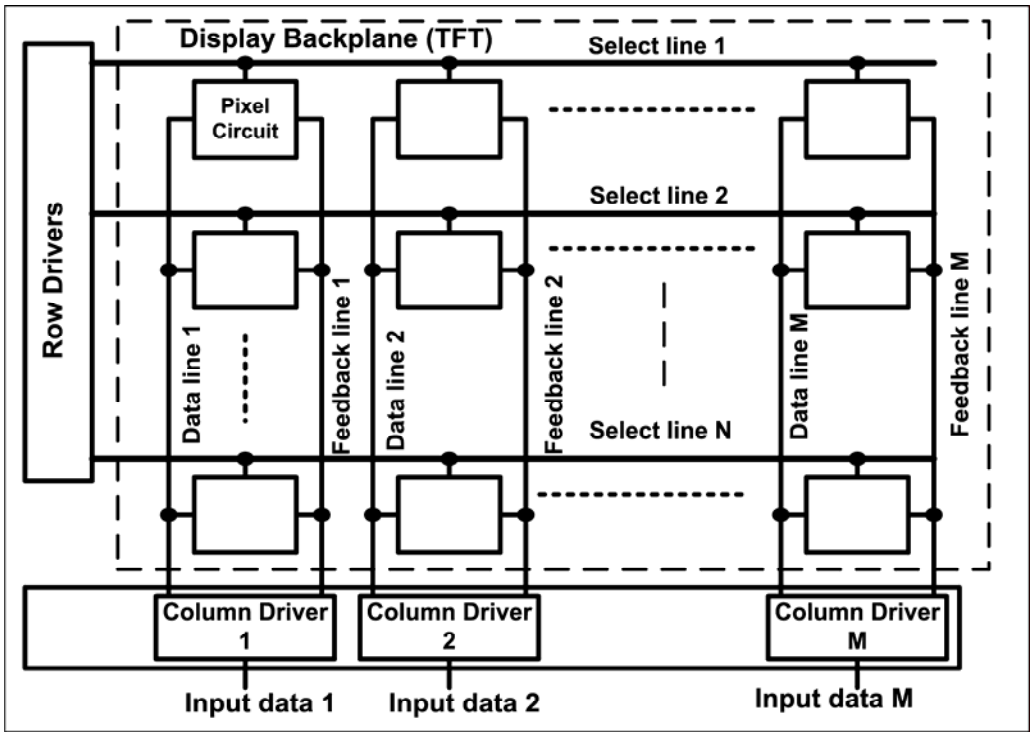


Figure 4.2: Array of AMOLED pixel circuits with feedback.

4.2 Proposed Pixel Circuits

Fig. 4.3 shows a schematic of a pixel circuit and the external column driver with voltage feedback [87]. The pixel circuit consists of a drive TFT (T1), two switch TFTs (T2 and T3), a storage capacitor (C_S), a feedback resistor (R_F), and an OLED. The anode terminal of the OLED is connected to V_{DD}. The external column driver, in its simplest form, is a differential amplifier.

The pixel circuit has two modes of operation: programming and hold. In the programming mode, the voltage of the select line goes high, turning T2 and T3 on. The current through T1 is converted to a voltage (V_F) by R_F. This voltage is conveyed to the inverting input of the differential amplifier by the feedback line. Due to the inherent negative feedback in the circuit, the output voltage of the differential amplifier adjusts the current of T1 to minimize the difference between the input data voltage (V_{IN}) and V_F. Assuming that the voltage gain of the differential amplifier is very high and its

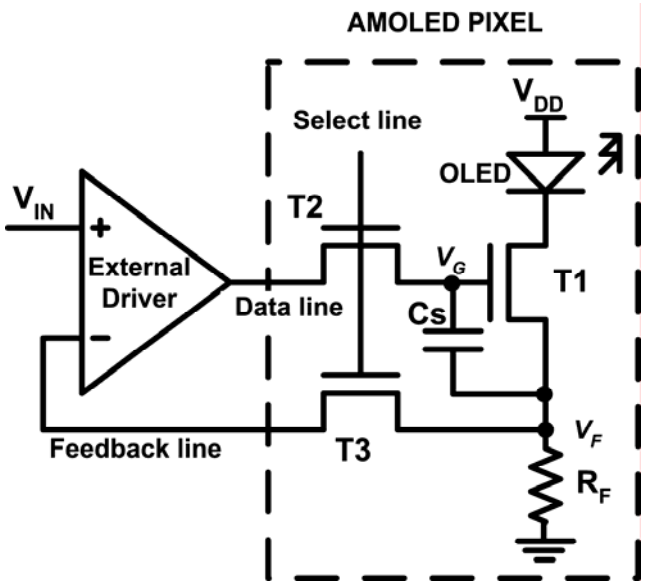


Figure 4.3: AMOLED pixel circuit with voltage feedback.

input bias current is much smaller than the programming current, the current through T1 (I_{PROG}) eventually becomes approximately equal to

$$I_{PROG} \approx \frac{V_{IN}}{R_F}. \tag{4.1}$$

It is evident that I_{PROG} is determined by V_{IN} and R_F and not by the parameters of T1. Considering the high stability of the n+ a-Si resistors, an equally high stability of I_{PROG} is expected. The effect of T2 and T3 on the programming current is negligible, because no current passes through these switches in the steady state.

In the hold mode, the select line goes low, disconnecting T1 from the differential amplifier by turning T2 and T3 off. However, the OLED current does not change considerably during the hold mode since C_S stores the gate-source voltage of T1. The pixel circuit compensates for the V_T shift in T1, as long as the voltage at the gate of T1 (V_G) does not exceed the maximum output range of the differential amplifier (V_{OMAX}), and the voltage at the select line is high enough to turn T2 on. If V_{DD} is

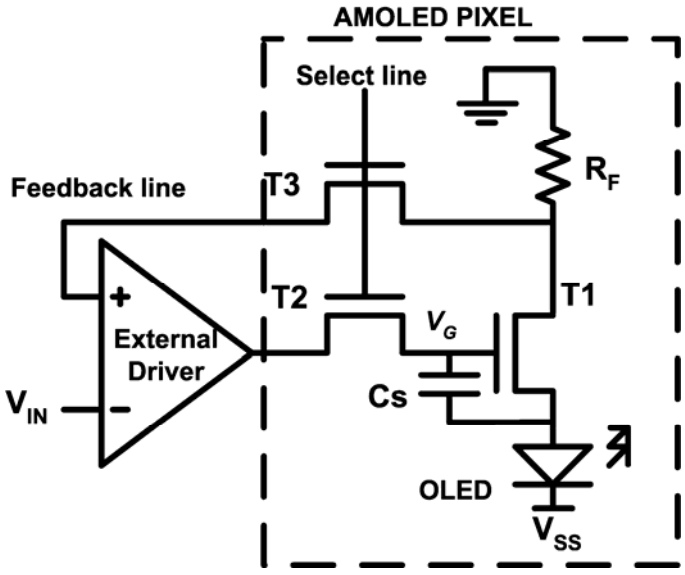


Figure 4.4: AMOLED pixel circuit with resistive feedback with common-cathode OLED.

high enough to keep T1 in the saturation region, then the maximum ΔV_T that can be compensated by the circuit (ΔV_{TM}) is given by

$$\Delta V_{TM} = Min\left(V_{OMAX} - V_{T1o} - \left(\frac{I_{MAX}}{K}\right)^{\frac{1}{\alpha}} - I_{MAX} R_F , V_{SELH} - V_{T1o} - V_{T2o} - \left(\frac{I_{MAX}}{K}\right)^{\frac{1}{\alpha}} - I_{MAX} R_F \right). \qquad (4.2)$$

Here, I_{MAX} is the maximum programming current, V_{SELH} is the voltage of the select line at the programming mode, K is the transconductance coefficient of T1, and V_{T1o} and V_{T2o} the initial V_T of T1 and T2, respectively. The first and second terms in (4.2) are associated with the limited operating voltage of the differential amplifier and the maximum voltage of select line, respectively.

Fig. 4.4 shows another configuration of the pixel circuit, where the anode terminal of the OLED is connected to the source of the driving TFT (T1). It is very similar to the circuit in Fig. 4.3. However, the cathode of the OLED is not patterned and is common for all the OLEDs. Such a configuration is more compatible with conventional OLEDs, as explained in Section 2.3.3. The main drawback of this circuit is the larger voltage swing required for the differential amplifier and the select line.

4.3 Analysis of the Performance

In the following sections, a comprehensive study of the performance of the proposed driving scheme is conducted. The performance of the driving scheme is evaluated according to the design considerations for the AMOLED pixel circuits, presented in Chapter 2.

4.3.1 Stability Analysis

Due to the inherent negative feedback of the circuit, ideally, there is no error in the OLED current due to variations in the static characteristics of T1, in particular, those associated with the threshold voltage shift. However, static and dynamic effects such as the limited gain of the external differential amplifier and the charge injection cause error in the final value of the OLED current. These effects are not only responsible for the gain and offset error in the pixel circuits, but also result in the dependence of the OLED current on the V_T shift. In the following sections, mechanisms of instability in the OLED current are studied.

4.3.1.1 Stability of Feedback Resistor

According to (4.1), the OLED current is inversely proportional to R_F; thus, instability in R_F instigates instability in the OLED current. As a result, it is crucial to investigate the stability of R_F at the first step of the design of the pixels. Stability of several fabricated n+ microcrystalline silicon resistors, used in the implementation of R_F, are measured. To accelerate the aging process, the resistors are stressed by a 1.0 mA current which is three orders of magnitude larger than normal currents in an AMOLED pixel. All of the measurements are conducted at the fixed temperature of 30 ^{o}C. Fig. 4.5 shows the measured resistance of three resistors as a function of the stress time. As can be seen, the resistors are highly stable. The measured deviations of the resistors are smaller than the inaccuracy of the measurement setup, and are caused by small fluctuations in the temperature.

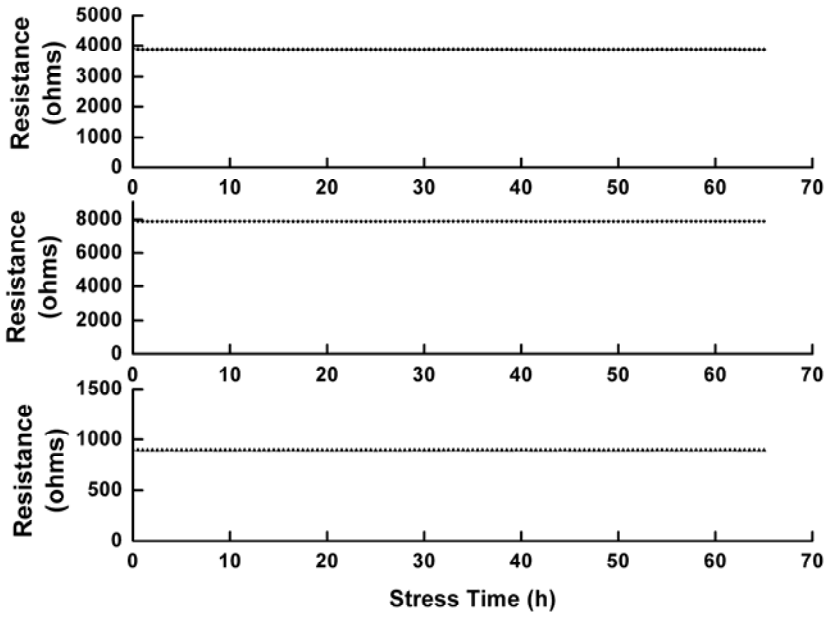


Figure 4.5: Measured resistance of three n+ microcrystalline silicon resistors as a function of the stress time.

4.3.1.2 Static Stability

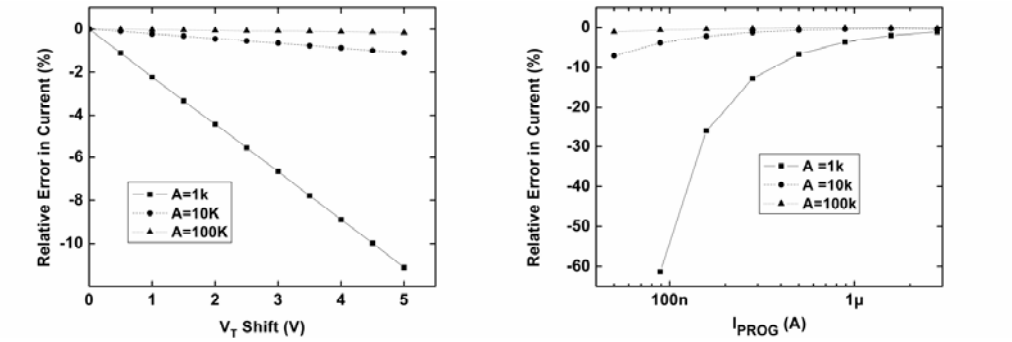
Although the negative feedback reduces the effect of the V_T shift of T1 on the OLED current, the V_T shift still affects the OLED current due to the finite gain of the feedback loop. For a differential amplifier with a gain of *A*, I_{PROG} for the circuit in Fig. 4.3 is almost equal to the following:

$$I_{PROG} \approx \frac{2KA^2V_{IN}R_F - 2KAV_{T1}R_F + 2KAV_{IN}R_F + \sqrt{1+4KA^2V_{IN}R_F}}{2KA^2R_F^2} \tag{4.3}$$

where V_{T1} is the threshold voltage of T1. For a large *A*, (4.3) is reduced to

$$I_{PROG} \approx \frac{V_{IN}}{R_F} - \frac{V_{T1}}{AR_F}. \tag{4.4}$$

If V_{T1}/A is much smaller than V_{IN}, then the effect of V_{T1} on I_{PROG} can be neglected and (4.4) is reduced to (4.1). The relative error in I_{PROG} ($\Delta I_{PROG}/I_{PROG}$) is also given by



(a) (b)

Figure 4.6: Simulation results from a pixel circuit with voltage feedback: (a) relative error in the programming current as a function of the V_T shift for different gains of the differential amplifier, (b) relative error in the programming current as a function of the programming current.

Table 4.1 Circuit parameters of Figure 4.3 used for the circuit-level simulations.

Design Parameter	Value
V_{sel} (V)	0-25
V_{DD} (V)	20
C_S (pF)	2
W1/L1 (μm)	600/23
W2/L2 (μm)	100/23
W3/L3 (μm)	200/23
R_F (kΩ)	100
I_{data} (μA)	0-5

$$\frac{\Delta I_{PROG}}{I_{PROG}} = -\frac{\Delta V_{T1}}{AV_{IN}}. \tag{4.5}$$

For smaller currents, the sensitivity to the V_T shift is higher. Therefore, in the design of the external driver, the minimum gain of the differential amplifier should be selected for the lowest programming current. For further investigation, pixel circuit in Fig. 4.3 is simulated with the circuit parameters

listed in Table 4.1. Fig. 4.6 (a) shows the relative error in I_{PROG} as a function of ΔV_{T1} for different values of A for I_{PROG}=500 nA. As predicted by (4.5), the sensitivity of the current to V_T shift is negative, and is smaller for larger gains. Fig. 4.6 (b) shows the relative error in I_{PROG} as a function of I_{PROG} for different values of A for ΔV_{T1} =3 V. As can be seen, for smaller currents the relative error increases. Therefore, A should be large enough to limit the maximum error in the entire range of I_{PROG}.

4.3.1.3 Dynamic Stability

During the transition of the circuit from the programming to the hold mode, the effects of charge injection and clock feed-through of T2 on the gate-source voltage of T1 (V_{GS1}) cause error in the hold current. The amount of error caused by the charge injection depends on V_{GS1}, and thus, V_{T1}. Therefore, as V_{T1} shifts over time, the hold current also changes. Simulations show that the induced error is small compared to the absolute value of V_{GS1}. Therefore, the error in the OLED current (I_{error}) can be estimated by a small-signal analysis as follows:

$$I_{error} = g_{m1}(I_{PROG}).\Delta V_{GS1}. \tag{4.6}$$

Here, ΔV_{GS1} is the error in V_{GS1} induced by the charge injection and clock feed-through of T2, and $g_{m1}(I_{PROG})$ is the transconductance of T1 for the programming current of I_{PROG} and is given by

$$g_m \approx k\alpha\left(\frac{I_{PROG}}{k}\right)^{\frac{1}{\alpha}}. \tag{4.7}$$

The shift in I_{error} (ΔI_{error}) is approximated by

$$\Delta I_{error} = \frac{\partial I_{error}}{\partial V_{T1}}\Delta V_{T1} = g_{m1}(I_{PROG})\frac{\partial \Delta V_{GS1}}{\partial V_{T1}}\Delta V_{T1}. \tag{4.8}$$

The next step is to find the dependence of ΔV_{GS1} on V_{T1}. ΔV_{GS1} can be approximated by

$$\Delta V_{GS1} = -\beta \frac{C_{GS2}(V_{selh} - V_{G1} - V_{T2})}{C_{GS1} + C_S} + \frac{C_{ov2}(V_{selh} - V_{sell})}{C_{GS1} + C_S}. \quad (4.9)$$

The first and the second terms are associated with the charge injection and clock feed-through, respectively. V_{G1} is the gate voltage of T1, C_{GS1} and C_{GS2} are the gate-source capacitors of T1 and T2, V_{T2} is the threshold voltage of T2, C_{ov2} is the gate-drain overlap capacitance of T2, and β determines the portion of the charge of T2, released from drain terminal. If the falling rate of the select line voltage is fast, β is close to 0.5 [70]. V_{selh} and V_{sell} are the voltage of the select line in programming and hold modes. V_{G1} is given by:

$$V_{G1} = V_{GS1} + R_F I_{PROG} = V_{T1} + \left(\frac{I_{PROG}}{K}\right)^{\frac{1}{\alpha}} + R_F I_{PROG}. \quad (4.10)$$

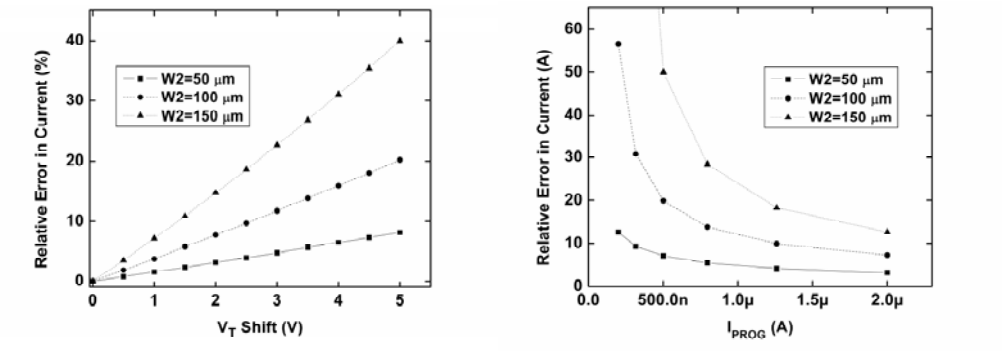
For a specific I_{PROG}, the charge injection term is a function of V_{GS1} therefore it changes as V_{T1} shifts. By substituting (4.10) and (4.9) into (4.8) ΔI_{error} is given by

$$\Delta I_{error} = g_m \beta \frac{C_{GS2}}{C_{GS1} + C_S} \Delta V_{T1}. \quad (4.11)$$

Equation (4.11) reveals the dependence of ΔI_{error} on the V_T shift of T1. It can be seen that ΔI_{error} is proportional to the ratio of C_{GS2} to C_S+C_{GS1}. Thus, for smaller T2 sizes and larger values of C_S, the pixel circuit is less sensitive to the V_T shift. Moreover, from (4.11) it is evident that, in contrast to the effect of the limited gain, V_T-dependent charge injection tends to increase the OLED current. The relative error is calculated by combining (4.11) and (4.7) such that

$$\frac{\Delta I_{PROG}}{I_{PROG}} = -\frac{\alpha k^{1-\frac{1}{\alpha}}}{I_{PROG}^{1-\frac{1}{\alpha}}} \beta \frac{C_{GS2}}{C_{GS1} + C_S} \Delta V_{T1}. \quad (4.12)$$

To investigate the effect of the V_T-dependent charge injection, the pixel circuit in Fig. 4.3 is simulated with the circuit parameters in Table 4.1. Fig. 4.7 (a) shows the relative error in the hold current as a function of ΔV_{T1} for different sizes of T2 for I_{PROG}=1 μA. As predicted by (4.11), the error



(a) (b)

Figure 4.7: Simulated stability of a pixel circuit with voltage feedback: (a) relative error in the hold current as a function of the V_T shift for different sizes of T2 switch, (b) relative error in the hold current as a function of the programming current for different sizes of T2 switch.

in the current increases as ΔV_{T1} increases, and for larger sizes of T2, sensitivity to V_T shift is higher. Fig. 4.7 (b) shows the relative error in the hold current as a function of I_{PROG} for ΔV_{T1}=3 V for different sizes of T2. As predicted by (4.12), the error increases for smaller currents.

For nominal circuit values, the effect of the V_T-dependent charge injection is much larger than the effect of the limited gain. As a result, the OLED current slightly increases over time as V_T of T1 increases. Such behaviour can be useful for colour AMOLED displays, since pixel circuits can be designed to compensate for the OLED aging, and the rate of the current increment for different OLED colours can be designed by changing the size of T2 switch.

4.3.1.4 Instability Due to Shift in OLED Voltage

In the voltage and current-programmed pixel circuits, variations in the I-V characteristics of the OLED change the drain-source voltage (V_{DS}) of the drive TFT. This induces error in the OLED current due to the imperfect saturation characteristic of a-Si TFTs. In the proposed pixel circuits, the feedback considerably increases the output resistance seen by the drain terminal of the drive TFT. As

a result, the hold current is not influenced by variations in the I-V characteristics of the OLED. For the circuit in Fig. 4.3, the output resistance seen from the drain terminal (r_{out}) of T1 is equal to

$$r_{out} = R_F + r_{ds} + (A+1)g_m R_F r_{ds}\,, \tag{4.13}$$

where r_{ds} is the small-signal drain-source resistance of T1. Compared to that of a conventional 2-TFT pixel circuit, the output resistance is increased by a factor of $A.g_m.R_F$. For example, for typical values of g_m=1 μA/V, R_F=100 kΩ, and A=1000, the output resistance is 100 times larger than the original r_{ds}. For the circuit in Fig. 4.4, the impedance, seen by the OLED is equal to

$$r_{out} = \frac{R_F + r_{ds} + Ag_m R_F r_{ds}}{1 + g_m r_{ds}}\,. \tag{4.14}$$

For typical r_{ds} and g_m values, $g_m.r_{ds}$ is much smaller than 1, resulting in similar values for (4.13) and (4.14).

4.3.2 Effect of the Reverse Current of TFTs

When a pixel is selected, the other pixels in the same column are deselected and their switch TFTs are OFF. However, each OFF TFT has a small reverse current, as shown in Fig. 4.8. Due to the large number of switch TFTs connected to the feedback line, the total parasitic current of the feedback line can be considerable. The current of the feedback line affects the programming current of the selected pixel. If the reverse current of a TFT switch is I_{OFF}, then the programming current of the selected pixel is approximated by

$$I_{PROG} = \frac{V_{IN}}{R_F} + \left(1 + \frac{R_{S3}}{R_F}\right)(N-1)I_{OFF}\,. \tag{4.15}$$

For simplicity, it is assumed that the gain and the input resistance of the external differential amplifier are infinite. N is the number of rows, and R_{S3} is the ON resistance of T3. The second term in (4.15) is the error associated with the reverse current and should be smaller than the minimum pixel current. The value of I_{OFF} principally depends on the fabrication process, TFT size, and the biasing

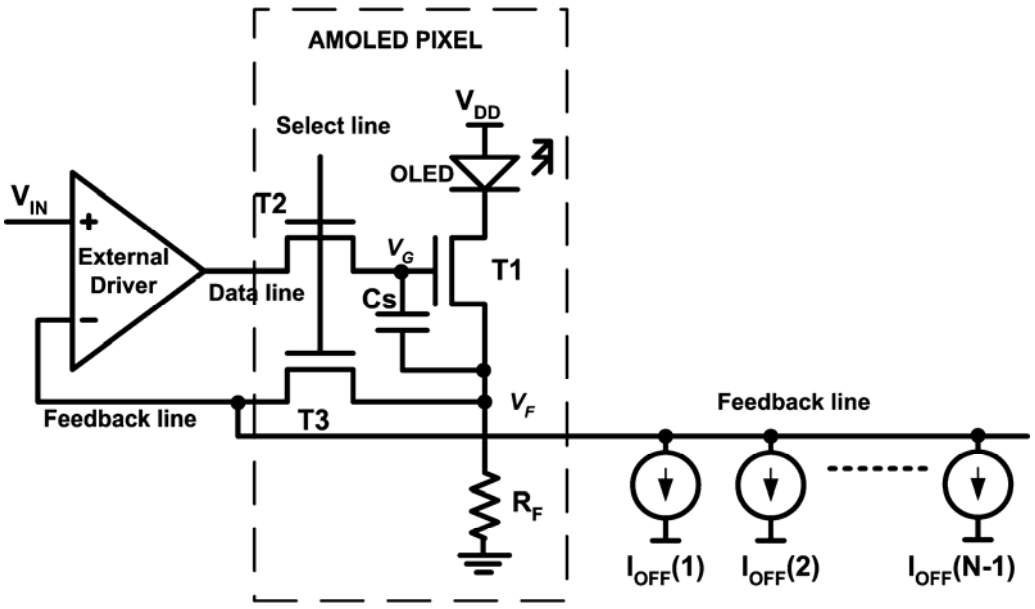


Figure 4.8: Circuit model to illustrate the effect of the reverse current of TFTs on the programming current.

voltage of the switch TFTs, and can be in the range of 0.1 pA to 10 pA [18]. Usually, R_{S3} is larger than R_F so that the term $(1+R_{S3}/R_F)$ in (4.15) is larger than 10. For a QVGA display with N=240, I_{OFF}=1 pA, and R_{S3}/R_F=10, the estimated error in I_{PROG} is close to 2.65 nA. Although in most of applications, the error level is tolerable, for a very low-power display with very high-efficiency OLEDs, the error level can be close to the minimum pixel current. To minimize the error, it is crucial to minimize I_{OFF} by properly biasing the TFT switches in the reverse mode.

4.3.3 Mismatch of the Feedback Resistors

Since the pixel current is determined by the feedback resistor, the uniformity of the pixel current depends on the matching properties of the feedback resistors. R_F is given by $R_F = \rho \frac{l}{tw}$ where l, w, and t are the length, width, and thickness of the resistor, respectively, and ρ is the resistively of the material. For n+ amorphous silicon and n+ microcrystalline resistors, ρ is uniform since the short-

range order of the material is much smaller than the dimensions of the resistors. As a result, mismatch of the resistor is determined only by the geometrical parameters, as given by

$$\frac{\Delta R_f}{R_f} = \left|\frac{\Delta l}{l}\right| + \left|\frac{\Delta w}{w}\right| + \left|\frac{\Delta t}{t}\right|. \tag{4.16}$$

The relative variations in the length and width of the resistor, $\Delta l/l$ and $\Delta w/w$, are defined by the accuracy of photolithography, and $\Delta t/t$ is determined by the uniformity of the film thickness, which depends on the deposition conditions. The matching requirements of the resistors depend on the desired quality of the display and its application. So far, no matching data for n+ resistors are available from an industry source. However, a uniformity close to that of a-Si TFTs is expected.

4.3.4 Effect of Temperature

As discussed in Section 2.2.3, threshold voltage and mobility of a-Si TFTs change with temperature. In the proposed driving scheme, the negative feedback significantly reduces the sensitivity of the OLED current to the variations in TFT parameters, and thus, temperature variations. However, temperature variations affect the OLED current by several mechanisms. Some of these mechanisms are the temperature-dependence of R_F, change in the charge injection of T2, and change in the reverse current of the switch TFTs.

4.3.4.1 Variations of R_F

Since I_{PROG} directly depends on the value of R_F, any change in R_F by temperature, changes I_{PROG}. Measurement results indicate that temperature coefficient of the fabricated n+ microcrystalline resistors is close to +0.003/^{o}C. For the pixel circuit of Table 4.1, such a temperature coefficient results in 17.5% increase in the OLED current over a range of 50 ^{o}C for a nominal current of 500 nA. Although the estimated change is much smaller than that in a conventional 2-TFT or a voltage-programmed pixel circuit, it remains unacceptable for many applications. The sensitivity of the pixel circuit to temperature can be improved by using a reference resistor in each column as shown in Fig.

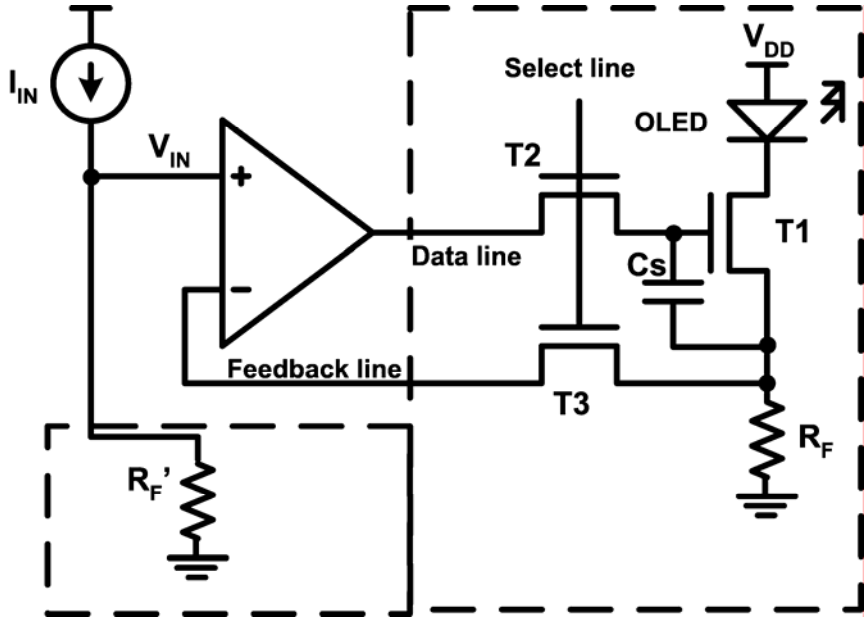


Figure 4.9: Temperature-independent driving method for pixel circuits with voltage feedback.

4.9. Here, V_{IN} is generated by passing the data current (I_{IN}) through a reference n+ microcrystalline resistor (R'_F). The programming current of the pixel circuit is expressed as

$$I_{PROG} = I_{IN} \frac{R_F'}{R_F}. \tag{4.17}$$

Since R_F and R'_F have identical temperature coefficients, sensitivity of the OLED current to the temperature is significantly reduced.

4.3.4.2 Change in the Reverse Current of T2

As discussed in Section 2.2.7, the reverse current of an a-Si TFT switch is small and does not significantly affect the hold current. However, the reverse current increases at higher temperatures. Fig. 4.10 shows the measured reverse current of a TFT as a function of the temperature for V_{GS}=-8 V. As can be seen, the increase in the reverse current is in excess of 4.6 times for a temperature range of 50 ^{o}C. The increase in the reverse current results in a faster discharge of C_S during the hold mode, leading to degradation of the average hold current. The dependence of the average hold current on the temperature due to change in the leakage current can be approximated by

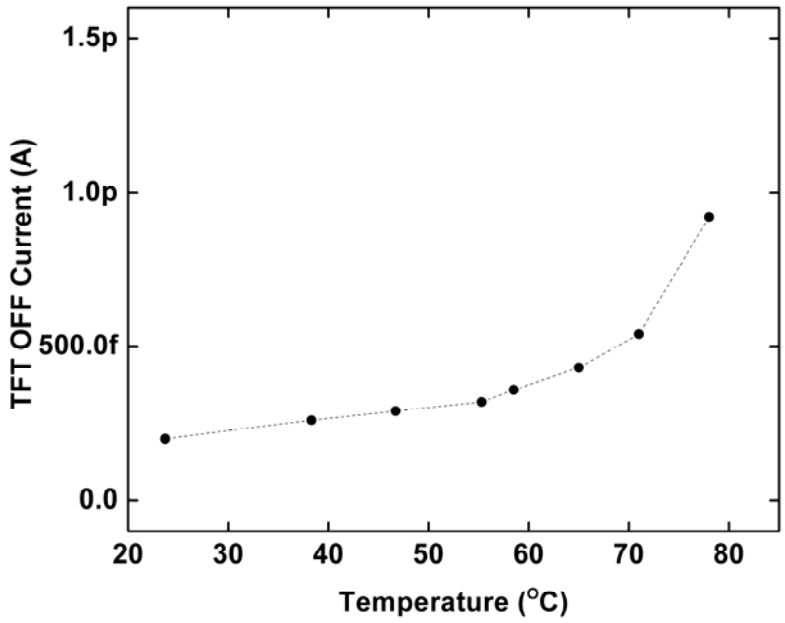


Figure 4.10: TFT reverse current as a function of temperature.

$$\Delta I_{HLR} \approx \frac{1}{2}\frac{t_{hold}}{C_S} g_m(I_{PROG})\frac{\partial I_{OFF}}{\partial T}\Delta T \ . \tag{4.18}$$

Here, t_{hold} is the hold time, and $\frac{\partial I_{OFF}}{\partial T}$ determines the sensitivity of the reverse current of TFT to temperature. According to the data in Fig. 4.10, for a 50 ^{o}C change in temperature, less than 1% error in the hold current is estimated for I_{PROG}=500 nA, t_{hold}=16.67 ms, and C_S=2 pF. This error is much smaller than the current variations caused by other mechanisms.

4.3.4.3 Change in Charge Injection of T2

By using the scheme shown in Fig. 4.9, variations of the programming current can be eliminated. However, the temperature-dependent charge injection has a noticeable effect on the hold current during the circuit transition from the programming to the hold mode. The mechanism of temperature-dependent charge injection is similar to the V_T-dependent charge injection. The error induced in the hold current by the charge injection depends on the V_T of T1 and T2. By increasing the temperature, V_{T1} and V_{T2} decreases. A decrease in V_{T2} directly increases channel charge of T2, and thus, increasing

the charge injection. A decrease in V_{T1} increases the channel charge of T2 by reducing V_{GS1}, and thus, increasing the gate-source voltage of T2. In addition to the change in the threshold voltage, the change in the mobility of T1 reduces the hold current by increasing the transconductance of T1. A simplified small-signal analysis similar to that presented in Section 4.3.1.3 summarizes the above discussion as follows:

$$\frac{\partial \Delta V_{GS1}}{\partial T} = \beta \frac{C_{GS2}}{C_{GS1} + C_S} \left(\frac{\partial V_{T1}}{\partial T} + \frac{\partial V_{T2}}{\partial T} + \frac{\partial}{\partial T} \left(\frac{I_{PROG}}{K} \right)^{\frac{1}{\alpha}} \right). \tag{4.19}$$

The expansion of the third term in (4.19) is complicated, since both α and K are functions of the temperature. However, equation (4.19) predicts that by increasing the temperature, the hold current decreases.

4.3.5 Power Consumption

The efficiency of the pixel circuits with voltage feedback are less than that of a conventional 2-TFT circuit due to the power consumption in the feedback resistor. For the pixel circuits of Fig 4.3 and Fig. 4.4, the power efficiency is mathematically expressed as

$$\eta_P(I) = \frac{V_{OLED}}{V_{DD}} = \frac{V_{OLED}(I_{PROG})}{V_{DS}(I_{PROG}) + V_{OLED}(I_{PROG}) + R_F I_{PROG}}. \tag{4.20}$$

To increase the efficiency, R_F should be minimized. However, a low value for R_F results in a low gain for the feedback loop, leading to inaccuracy in the OLED current. Simulation results show that for R_F values smaller than 100 kΩ, the power consumption in R_F is much smaller than that in the driving TFT.

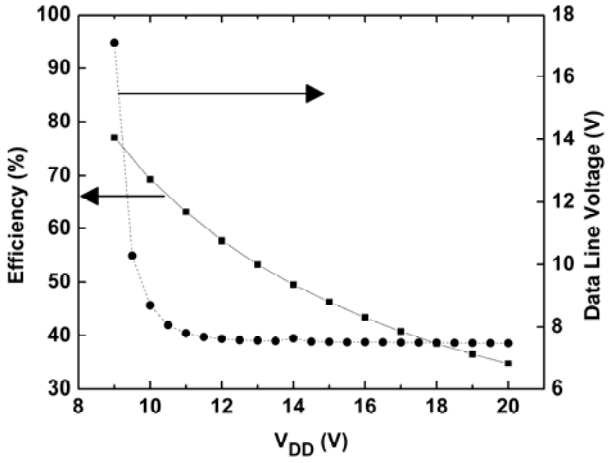


Figure 4.11: Simulated pixel efficiency and the maximum voltage of the data line as a function of supply voltage in the pixel circuit in Fig. 4.3.

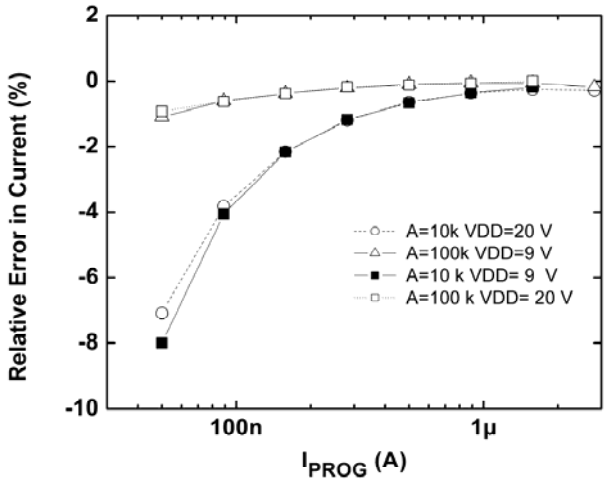


Figure 4.12: Comparison of the relative error when T1 is biased in the triode and saturation regions.

An effective method of increasing the efficiency is to reduce V_{DS}. Due to the feedback in the system, T1 can be biased in the triode region instead of the saturation region, thus increasing η_P substantially. However, biasing T1 in the triode region causes some problems. First, due to the lower transconductance of T1 in the triode region, higher driving voltages are required for the external drivers. Secondly, a reduction in the transconductance of T1 results in a reduction in the DC loop gain, leading to a higher sensitivity to the V_T shift.

To study the effect of biasing T1 in the triode region, the circuit in Fig. 4.3 with the circuit parameters listed in Table 4.1 is simulated with different V_{DD} values. Fig. 4.11 shows η_P and the maximum voltage of the data line as a function of V_{DD} for I_{PROG}=500 nA and I_{PROG}=2 μA, respectively. The efficiency of the pixel increases from 34.5% to 77% as V_{DD} decreases from 20 V to 9 V. For the same V_{DD} range, the maximum voltage of the data line for I_{PROG}=2 μA increases from 7.4 V to 17.1 V. Sensitivity of I_{PROG} to 3 V shift in V_{T1} is compared in Fig. 4.12 for V_{DD}=20 V and V_{DD} =9 V. As predicted, the sensitivity to the V_T shift is higher for the smaller V_{DD}. However, for a high loop gain, the reduction in sensitivity is small. For instance, for A=10 k, the maximum difference in the relative error is less than 1%.

4.3.6 Settling Time

To evaluate the settling time, the transient response of the circuit in Fig. 4.3 is simulated by CADENCE SPECTRE. The parameters of the pixel circuit are the same as those listed in Table 4.1. A behavioural model, with a unity-gain bandwidth of 1 MHz is used as the differential amplifier. The total parasitic capacitance of the lines (C_P) is approximated by

$$C_P = NC_i(\Delta LW_S + A_{INT}), \tag{4.21}$$

where N is the number of rows, ΔL is the gate-drain overlap length in the switching TFTs, W_S is the width of the switch TFT, and A_{INT} is the total overlap area between the column and the row lines. For example, in a typical 2-inch QVGA display with N=200, C_i=20nF/cm^2, ΔL=4μm, W_S=50μm, and A_{INT}=100 μm^2, an 8-pF parasitic capacitance is expected. However, considering the wider current range and the larger size of the prototype pixels, the parasitic capacitance of the data and feedback lines are set to 40 pF to avoid an optimistic estimation of the settling time.

Fig. 4.13 shows the 5%-settling time of I_{PROG} as a function of the programming current for different values of A. It is observed that the settling time increases for both low and high programming

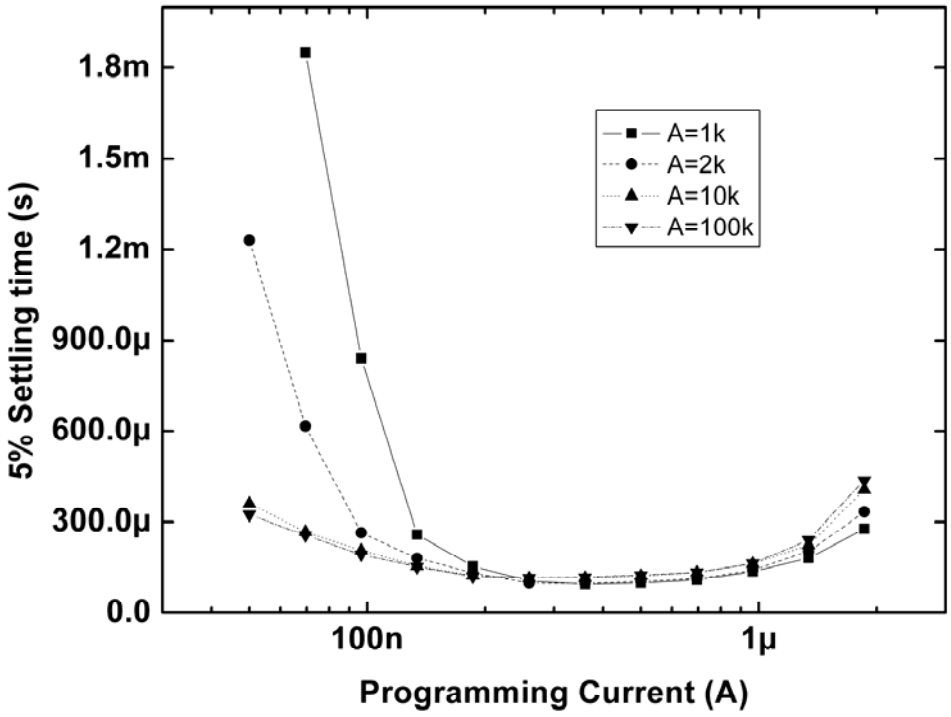


Figure 4.13: Simulated 5% settling time in the pixel circuit of Fig. 4.3 as a function of the programming current for different gains of the differential amplifier.

currents. Moreover, at lower programming currents, a larger A results in a shorter settling time, while at higher currents a larger A leads to a longer settling time.

4.3.6.1 Small-Signal Analysis

To investigate the effect of circuit parameters on the settling time, the circuit in Fig. 4.3 is analyzed. Fig. 4.14 shows the small-signal model of the circuit in Fig. 4.3. T1 is modelled by a gate-source capacitor (c_{gs}) and a transconductance (g_m). T2 and T3 are modelled by R_{S2} and R_{S3} resistors, respectively. The parasitic capacitance of the feedback line is modeled by C_{PF}. The effect of the parasitic capacitance of the data line is taken into account by the transfer function of the differential amplifier, (A_{op}(s)). A_{op}(s) is estimated by a single-pole transfer function, expressed as

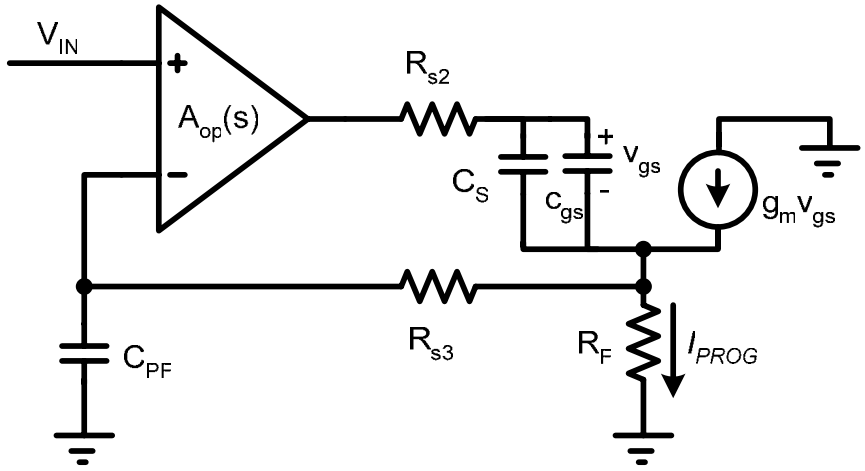


Figure 4.14: Small-signal model of the pixel in Fig. 4.3 in the programming mode.

$$A_{op}(s) = \frac{A_0}{1 + \frac{s}{\omega_p}}, \tag{4.22}$$

where ω_p is the -3 dB bandwidth of the differential amplifier. Table 4.2 lists a set of small-signal values which are derived from the circuit parameters in Table 4.1, based on the TFT model presented in the literature [18].

Considering the current of T1 as the output and V_{IN} as the input signals, a series-series feedback configuration can be distinguished. The loop gain of the feedback network is the product of the open-loop, (A_L) and the feedback (β) transfer functions. β is defined and calculated as follows:

$$\beta(s) = \frac{V_F}{I_{PROG}} = \frac{R_F}{1 + (R_F + R_{s3})C_{PF}s} \tag{4.23}$$

and A_L is calculated by

(4.24)

$$A_L(s) = A_{op}(s)\frac{(g_m + (C_S + c_{gs})s)[1 + (R_F + R_{s3})C_{PF}s]}{1 + g_m R_F + [(R_{s2} + R_F)(C_S + c_{gs}) + (R_F + R_{s3})C_{FP} + R_F R_{s3} g_m C_{PF}]s + [R_{s2}(R_F + R_{s3})(C_S + c_{gs})C_{FP} + R_F R_{s3} C_{PF}(C_S + c_{gs})]s^2}$$

The overall loop gain, (L(s)) is then given by:

(4.25)

$$L(s)=\frac{A_0 R_F g_m}{1+\frac{s}{\omega_p}}\frac{\left(1+\frac{g_m}{(C_S+c_{gs})}s\right)}{1+g_m R_F+[(R_{s2}+R_F)(C_S+c_{gs})+(R_F+R_{s3})C_{PF}+R_F R_{s3} g_m C_{PF}]s+[R_{s2}(R_F+R_{s3})(C_S+c_{gs})C_{FP}+R_F R_{s3} C_{PF}(C_S+c_{gs})]s^2}$$

where L(s) has a zero at

$$z_{p_1}=-\frac{g_m}{(C_S+c_{gs})}, \tag{4.26}$$

a real pole at ω_p, and two real poles associated with the second-order polynomial. Based on the extracted small-signal values in Table 4.2, It is assumed that $R_F<<R_{s2}$, R_{s3}, $(c_{gs}+C_S)<<C_{FP}$, and $g_m R_F<<1$. Therefore, the roots of the polynomial are approximated as follows:

$$\omega_{p1}=-\frac{1}{R_{s3}C_{PF}} \tag{4.27}$$

$$\omega_{p2}=-\frac{1}{R_{s2}(c_{gs}+C_S)}. \tag{4.28}$$

The loop gain at DC (L_{DC}) is approximately equal to

$$L_{DC}=R_F A_0 g_m. \tag{4.29}$$

Fig. 4.15 illustrates the Root-Locus of the circuit in Fig. 4.14. As can be seen, the transient response of the circuit is mainly affected by the dominant poles (ω_p, ω_{p1}), and L_{DC}.

From the analysis, the long settling times of the low and high currents can be explained. At low currents, g_m is small, leading to a small L_0. As a result, the feedback system is over-damped, and the settling of I_{PROG} is slow. In the same way, at high programming currents, L_0 is large, and the system is under-damped. Therefore, high overshoot in I_{PROG} increases the settling time.

Table 4.2: Small-signal parameters for the circuit of Fig. 4.3.

Design Parameter	Value
ω_p	100 rad/s
g_m	0.5 μA/V
C_{GS}	2 pF
C_{FP}	40pF
R_{s2}	1.1 MΩ
R_{s3}	1.1 MΩ
R_F	100 kΩ

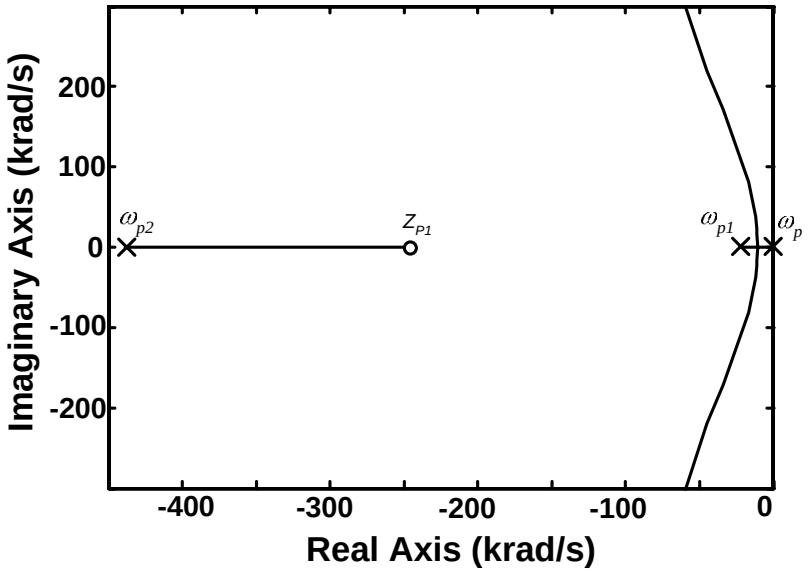


Figure 4.15: Root-Locus of the circuit shown in Fig. 4.14.

Since ω_{p1} is a dominant pole, it is preferred to be pushed to the highest possible frequency. For this purpose, C_{PF} and R_{S3} need to be minimized. However, to reduce C_{PF}, the width of T3 must to be reduced, which directly increases R_{S3}, accordingly. If A_{INT} in (4.21) is large, then by increasing the width of T3 it is possible to reduce ω_{p1}. However, the maximum size of T3 is limited by the area and aperture ratio of the pixel.

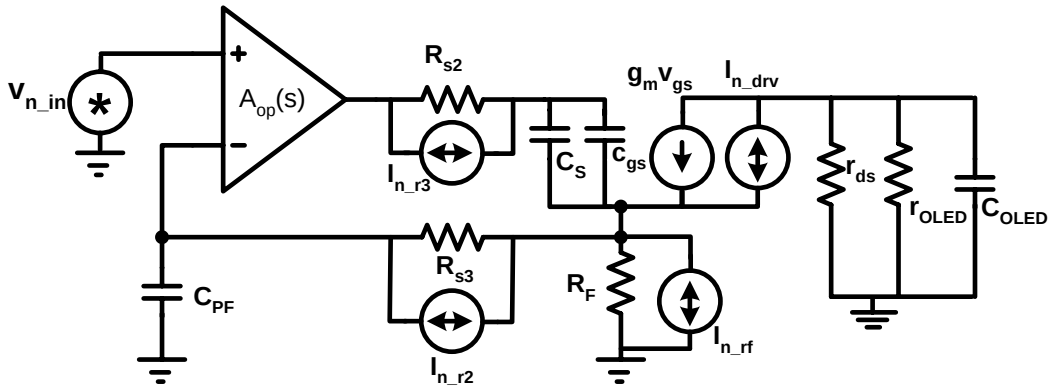


Figure 4.16: Small-signal model for noise analysis of the pixel circuit in Fig. 4.3.

Simulation results show that increasing ω_p up to 100 krad/s cause large overshoots in the OLED current or even instability. For higher ω_p values, the system becomes stable and the programming time considerably decreases from the order of hundreds of microseconds to the order of few tens of microseconds. However, the power consumption in such a high-bandwidth amplifier exceeds the power consumption specifications of display systems.

4.3.7 Noise Analysis

As mentioned in Section 2.2.10, flicker and thermal noise is not a considerable issue in many a-Si TFT AMOLED pixel circuits, such as the 2-TFT pixel. In the presented voltage feedback driving scheme, however, it is important to investigate the noise performance of the system due to the number of circuit components, and the extended bandwidth of the system. The noise in the circuit is analyzed as described in Section 2.2.10. Based on the small-signal noise model in Fig. 4.16, the transfer functions of the noise sources, and thus, the frequency response of the noise of the OLED are calculated. The small-signal values listed in Table 4.2 are used for the numerical calculations. Then, after the noise sources are replaced by their estimated measured physical models, the total noise power is calculated. Although the results might not be in a perfect match with the real measurements, they provide an estimate of the noise which is essential to evaluate the performance of the proposed driving scheme.

The transfer functions for the noise sources are as follows:

$$H_{N1} = \frac{i_{nOLED}}{v_{n\_in}} = \frac{\omega_p A_0 \left[1 + sC_{PF}\left(r_{s3} + R_F\right)\right]}{DEN(s)} g_m H_O(s) \tag{4.31}$$

$$H_{N2} = \frac{i_{nOLED}}{i_{n\_rf}} = \frac{R_F\left[\omega_p A_0 + \left(1 + \omega_p r_{s3} C_{PF}\right)s + r_{s3} C_{PF} s^2\right]}{DEN(s)} g_m H_O(s) \tag{4.32}$$

$$H_{N3} = \frac{i_{nOLED}}{i_{n\_r3}} = \frac{r_{s3}\left[\omega_p A_0 + R_F C_{PF} w_p s + R_F C_{PF} s^2\right]}{DEN(s)} g_m H_O(s) \tag{4.33}$$

$$H_{N4} = \frac{i_{nOLED}}{i_{n\_r2}} = \frac{r_{s2}\left(s + \omega_p\right)\left(1 + \left(r_{s3} + r_{s2}\right)C_{PF} s\right)}{DEN(s)} g_m H_O(s) \tag{4.34}$$

$$H_{N5} = \frac{i_{nOLED}}{i_{n\_drv}} = \frac{\left(s + \omega_p\right)\left(1 + \left(r_{s3} + r_{s2}\right)C_{PF} s\right)}{DEN(s)} H_O(s) \tag{4.35}$$

where DEN(s) and H_O(s) are defined as:

$$H_O = \frac{i_{nOLED}}{i_{T!}} = \frac{r_{ds}}{r_{ds} + r_{OLED}} \frac{1}{1 + (c_{gs} + C_{OLED})(r_{ds} \,||\, r_{OLED})s}. \tag{4.36}$$

(4.25)

$$DEN(s) = \omega_p\left(1 + g_m R_F + A_0 g_m R_F\right) + \left[1 + g_m R_F + \omega_p C_{PF}\left(R_F + r_{s3} + g_m R_F r_{s3}\right) + \omega_p c_{gs}\left(R_F + r_{s2} + R_F A_0\right)\right]s$$
$$+ \left[C_{PF}\left(R_F + r_{s3} + R_F r_{s3} g_m\right) + c_{gs}\left(R_F + r_{s2}\right) + \omega_p C_{PF} c_{gs}\left(R_F r_{s3} + R_F r_{s2} + r_{s2} r_{s3}\right)\right]s^2 + C_{PF} c_{gs}\left(R_F r_{s3} + R_F r_{s2} + r_{s2} r_{s3}\right)s^3.$$

Here, v_{n_in} is the input-referred noise of the opamp, I_{n_rf} is the current noise of the feedback resistor, I_{n_drv} is the current noise of T1, and i_{n_r2} and i_{n_r3} are the noise currents associated with T2 and T3 switches respectively. lastly, i_{n_r2} and i_{n_r3} are the noise currents of T2 and T3 switches. The flicker noise component of the switches is negligible because in the steady-state condition, their drain-source voltages are zero. i_{n_rf} is $4kT/R_F$. i_{n_drv} has both flicker and thermal components as presented in Section 2.2.10. v_{n_in} strongly depends on the op-amp design and fabrication technology. To estimate v_{n_in}, a two-stage OTA is designed in a 20-V 0.8mm double-extended CMOS technology. Its input-referred noise voltage spectra is obtained by the SPECTRE noise simulation. The input stage of the OTA has

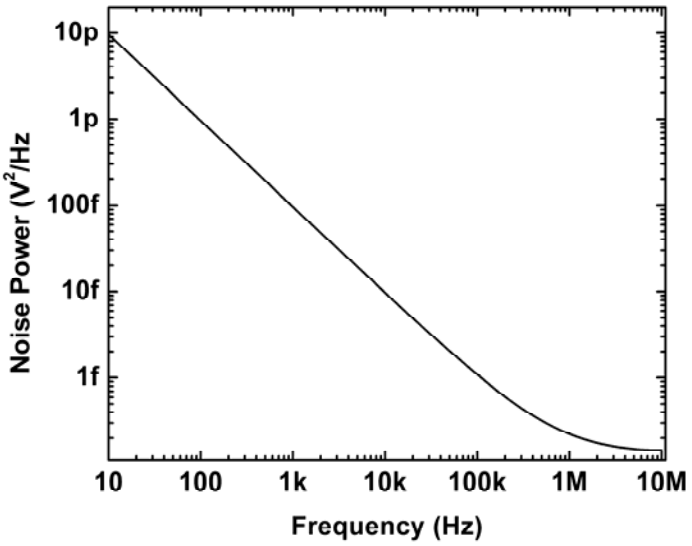


Figure 4.17: Simulated input-referred noise power in a typical op-amp implemented in a 20-V CMOS technology

pmos transistors with *W*/*L* of 160μm/4μm and a bias current of 100 μA. The detail of the OTA design is found in Appendix A. Fig. 4.17 shows the simulated v_{n_in}. The noise power of the OLED current is simulated for different programming currents based on the described noise model. Fig. 4.18 shows the RMS noise current of the OLED for different programming currents. The peak in the noise current between 1 μA and 2 μA is due to an associated peak in the noise transfer functions at this current range. Fig. 4.19 illustrates the contribution of the noise sources to the OLED current for OLED currents of 0.5 μA and 2 μA. As can be seen, the contribution of v_{n_in} is the highest. i_{n_r3} and I_{n_rf} have the second and the third highest contributions, respectively, whereas the effects of I_{n_drv} and i_{n_r2} are negligible. From the simulations, it can be seen that the total contribution of the op-amp and TFT noise is not considerable. The maximum ratio of the RMS noise to the OLED current level is less than 0.5%, which is also negligible.

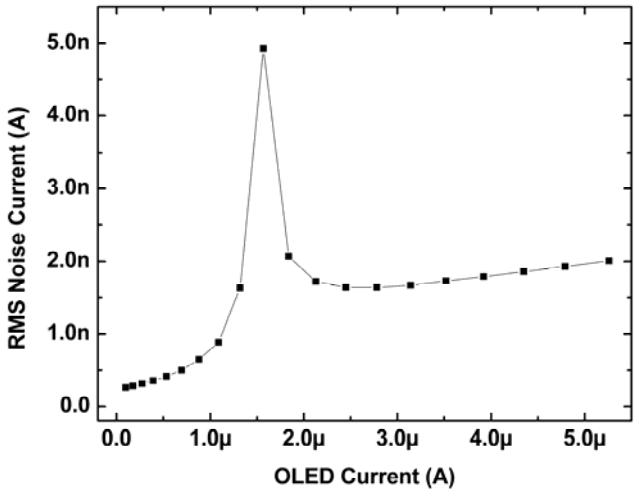
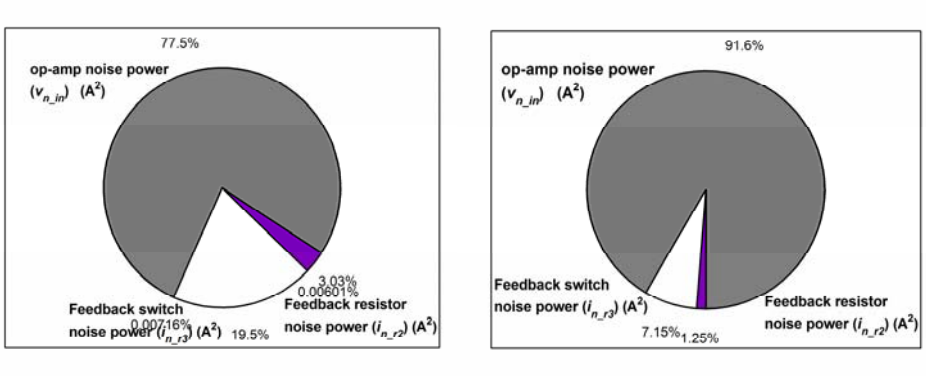


Figure 4.18: Calculated RMS noise current of the OLED for different programming currents.



(a) (b)

Figure 4.19: Contribution of the noise sources (a) I_{PROG}= 0.5 µA, (b) I_{PROG}= 2 µA.

4.4 Measurement Results

Prototypes of the pixel circuits are fabricated in a tri-layer in-house TFT process. The TFT process steps are described in [18]. The typical values of the device mobility, threshold voltage, and ON/OFF ratio were ~0.9-1.0 cm^2/Vs, 2-3 V, and 10^8-10^9, respectively. TFT contact layer is microcrystalline n+ and the resistors are fabricated with the same layer, thus, no additional mask or process steps are

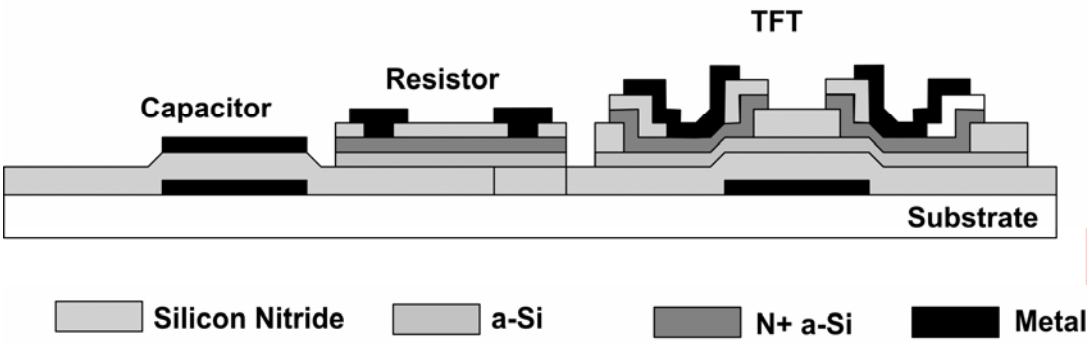


Figure 4 .20: Sketch of the cross-section of a TFT, n+ resistor, and a capacitor in the tri-layer wet-etched process provided by the G2N lab at the University of Waterloo.

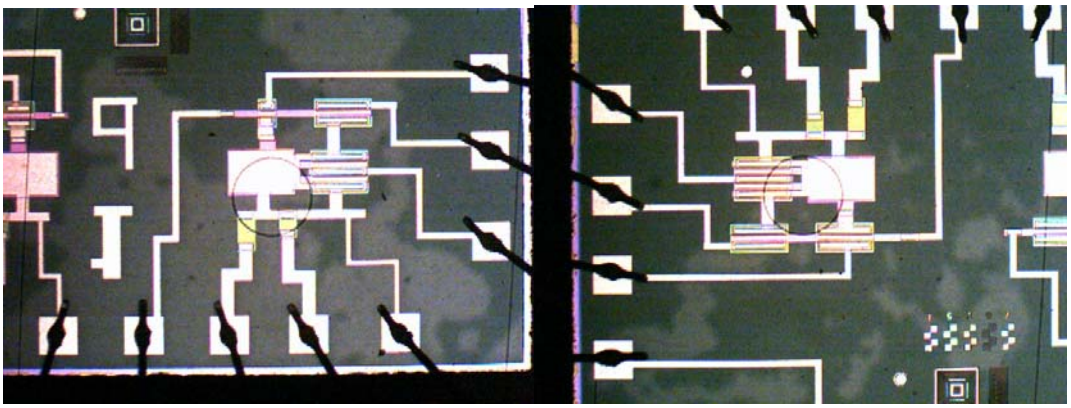


Figure 4.21: Micrograph of two fabricated pixel circuits.

required. The storage capacitors are fabricated by the gate and contact metals. The schematic cross sections of a TFT, a resistor, and a capacitor are shown in Fig. 4.20.

Generally, the pixel parameters such as the size of the TFTs are determined by the display parameters such as luminance, size, resolution, and the process characteristics such as the efficiency of the OLED, and the mobility of the TFTs. However, to achieve a sufficient yield, the fabricated prototype has larger TFT sizes than those in an industrial process. The circuit parameters for two different fabrication runs are listed in Tables 4.3 and 4.4.

Table 4.3: Design parameters for the fabricated AMOLED pixels, set I.

Design Parameter	Value
V_{sel} (V)	0-25
Vdd (V)	20
C_S (pF)	10
W1/L1 (μm)	800/23
W2/L2 (μm)	200/23
W3/L3 (μm)	600/23
R_F (kΩ)	50
I_{data} (μA)	0-15

Table 4.4: Design parameters for the fabricated AMOLED pixels, set II.

Design Parameter	Value
V_{sel} (V)	0-25
Vdd (V)	15
C_S (pF)	2
W1/L1 (μm)	400/23
W2/L2 (μm)	50, 100, 200, 300/23
W3/L3 (μm)	200/23
R_F kΩ	100
I_{data} (μA)	0-5

Fig. 4.21 is a photo micrograph of two fabricated pixel circuits. The pixel circuits are diced and packaged in 24-pin DIP ceramic packages. To provide the pixel circuits with the required signals, a general-purpose PCB board is used. For dynamic and settling time tests, discrete capacitors are used to emulate the effect of the data and feedback parasitic capacitors. A commercial monolithic FET-

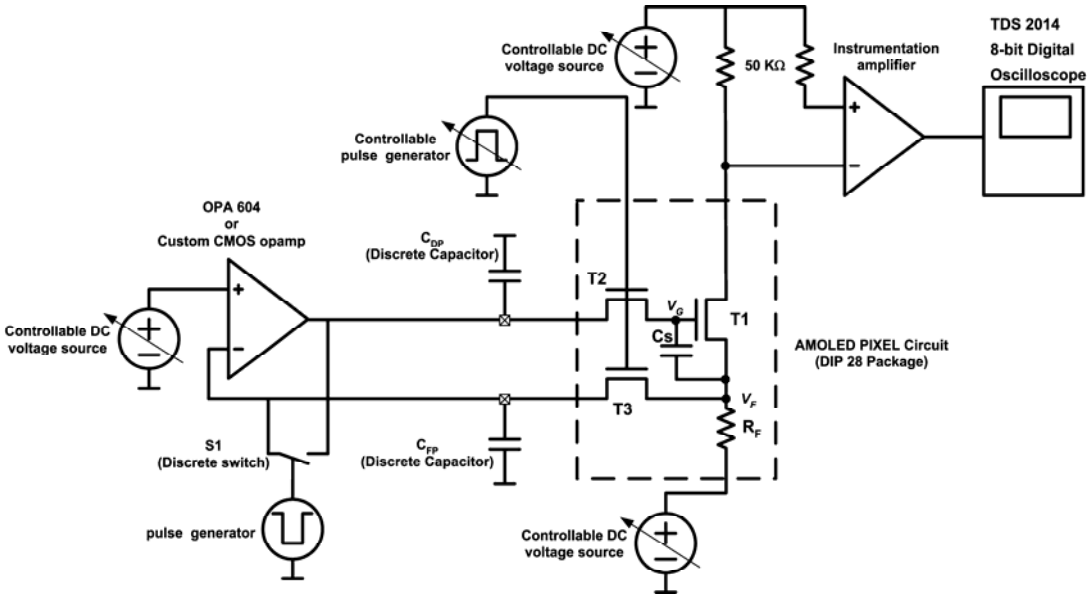


Figure 4.22: Simplified diagram of the test setup used for the transient measurements.

input Op-Amp (AN604) is used as the external driver due to its low input bias current. A 100 kΩ external resistor is used to measure the programming and hold currents. The voltage across the resistor is captured by a digital oscilloscope with 8-bit resolution. Fig. 4.22 shows a simplified diagram of the test setup.

4.4.1 General Operation

Fig. 4.23 shows the measured programming current as a function of V_{IN}, for a supply voltage of 20 V for the pixel circuit of Table 4.3. In this test, the select line remains high, and the current is measured by a Kiethley 236 source-meter unit (SMU), due to its high accuracy. As predicted by (4.1), the I_{PROG} - V_{IN} curve is highly linear, and has a slope of 1/51.4kΩ, which is very close to the measured conductance of R_F. Fig. 4.24 shows the measured transient waveforms of the current of T1 and the select line for various pixel circuits and programming currents. The hold current is smaller than the programming current due to the effect of charge injection and clock feedthrough of T2.

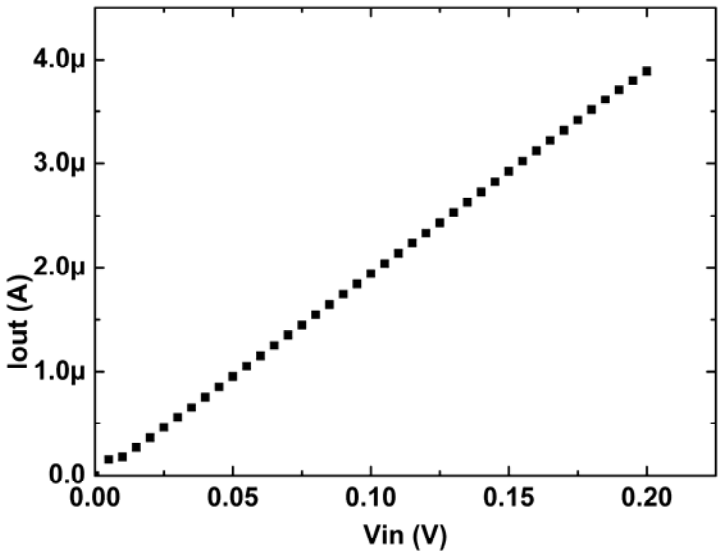


Figure 4.23: Measured I/O characteristics of a fabricated the pixel circuit with resistive feedback.

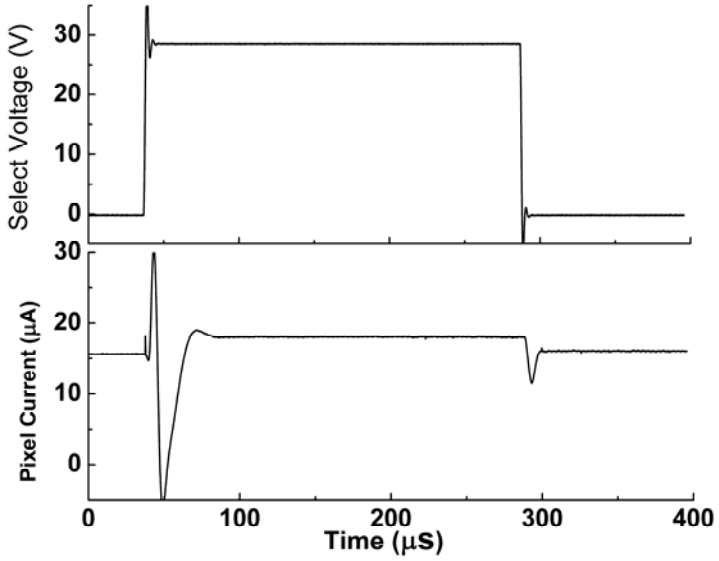


Figure 4.24: Measured transient response of the resistive-feedback pixel circuit.

4.4.2 Stability

To investigate the stability of the proposed driving scheme, lifetime tests for different pixel circuits are conducted. A set of lifetime tests are done for a pixel circuit with parameters listed in Table 4.3.

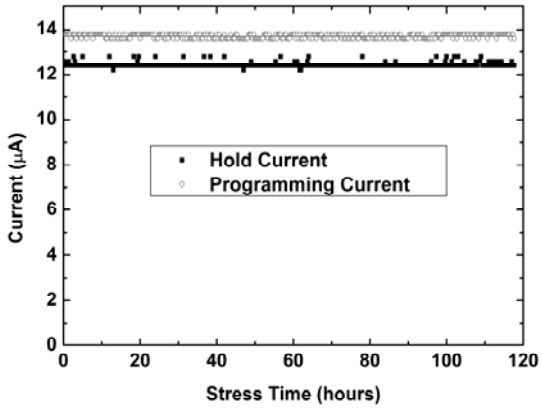


Figure 4.25: Programming and hold mode current as a function of stress time at room temperature.

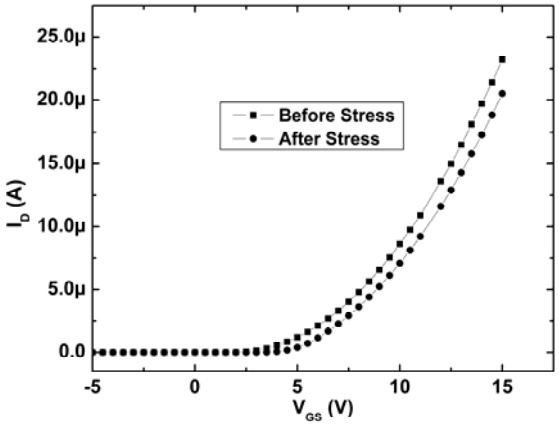


Figure 4.26: I-V characteristic of T1 before and after stress.

The pixel circuit is driven by a 14.5μA current pulse with a programming time of 250μs and a hold time of 2 ms for 120 hours at room temperature. Fig. 4.25 shows the programming and the hold currents as a function of the stress time. As can be seen, variations in the currents are not significant. The small fluctuations in the current are caused by the limited accuracy of the measurement equipment and the noise of the system. The I-V characteristic of the driving TFT (T1) is measured before and after the stress as shown in Fig. 4.26. Measurement results show that although the threshold voltage of T1 is shifted more than 1.3 V, the pixel current is stable. The measurement of R_F before and after stress shows no change in the value of this resistor.

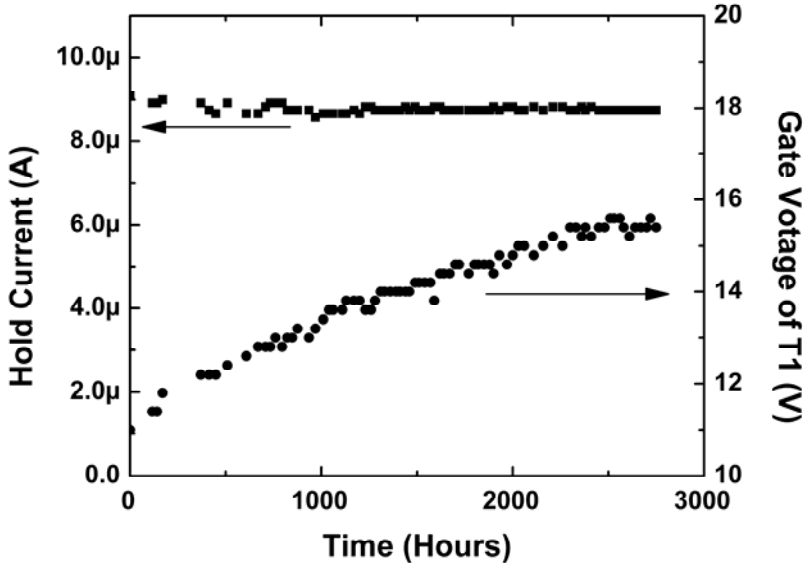
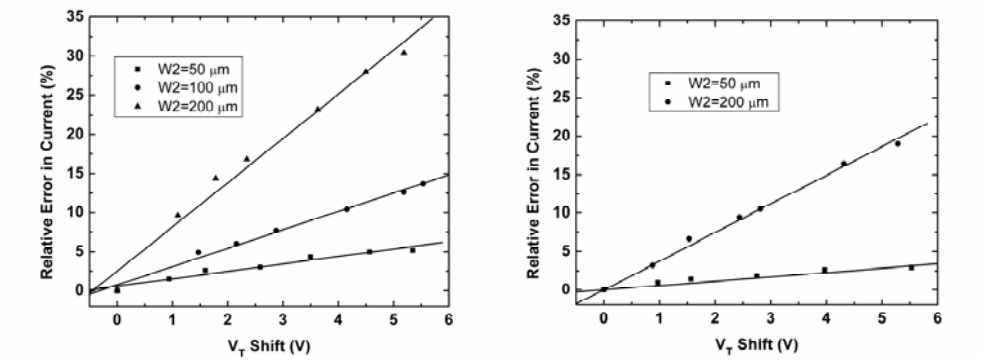


Figure 4.27: Measured hold current of a pixel circuit as a function of the stress time.

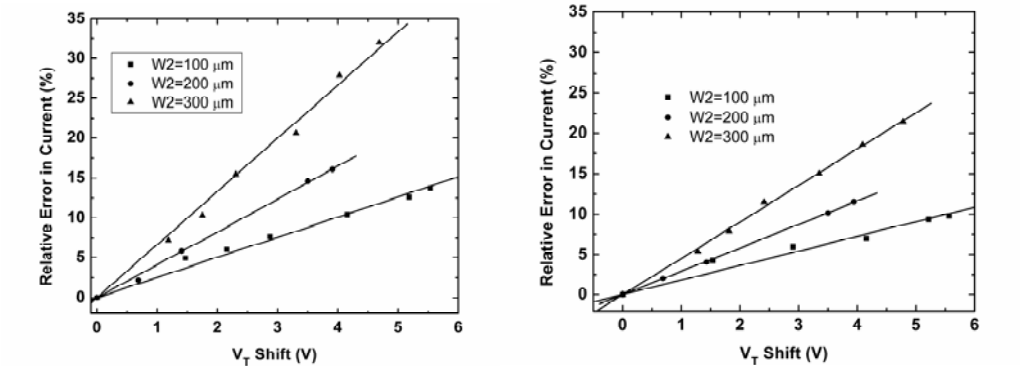
An extended lifetime test for the same pixel circuit is performed for a stress time of 2700 hours at room temperature. Fig. 4.27 shows the measured pixel current and gate voltage of the drive TFT as a function of the stress time. The current at the hold mode is close to 9 μA. The measurement results reveal that the pixel current is nearly independent of the V_T shift of the TFTs; the variations of the pixel current are less than 3.5% over 2700 hours and primarily are caused by variations of the temperature. The threshold voltage of T1 has a shift in excess of 4.5V.

To investigate the dynamic stability, pixel circuits with different sizes of T2 are fabricated and the change in their hold current as a function of V_T shift in T1 is measured. To reduce the measurement times, V_T shift is accelerated by stressing T1 with a 30-V voltage gate-source. Between the stress cycles, the hold current of the pixel circuits are measured. The circuit parameters of the pixel circuits are listed in Table 4.4. Compared with the circuit parameters listed in Table 4.3, these circuits are smaller, and thus, closer to the circuit sizes of real pixels. In particular, the size of C_S is much smaller. As a result, based on (4.11), a higher sensitivity to the V_T shift is expected.



(a) (b)

Figure 4.28: Measured relative error in hold current as a function of V_T shift in T1 for different sizes of T2 for: (a) I_{PROG}= 2 μA, (b), I_{PROG}= 4 μA in fabricated pixel circuit A.



(a) (b)

Figure 4.29: Measured relative error in hold current as a function of V_T shift in T1 for different sizes of T2 for: (a) I_{PROG}= 2 μA, (b), I_{PROG}= 4 μA in fabricated pixel circuit B.

Fig. 4.28 and Fig 4.29 shows the relative error in the hold current as a function of the V_T shift for the programming currents of 2 μA and 4 μA for two pixel circuits (A and B) with different sizes of T2. As predicted by the analysis, the hold current increases as V_T shifts. For larger sizes of T2, the increase in the hold current is more. Furthermore, the relative error is larger for smaller programming currents, as predicted by (4.13). Table 4.5 summarizes the error rates of the current per V_T shift for different switch sizes for both data sets.

Table 4.5: Summary of the error rates of the hold current versus V_T shift for different switch sizes for the tested pixel circuits.

	Sensitivity of Relative Error to V_T Shift of T1			
	Pixel A I_{PROG}=2 μA	Pixel A I_{PROG}=4 μA	Pixel B I_{PROG}=2 μA	Pixel B I_{PROG}=4 μA
W/L=50/23 μm	1.1 %/V	0.6 %/V	-	-
W/L=100/23 μm	3.1 %	1.8 %/V	2.5 %/V	1.8 %/V
W/L=200/23 μm	6.2 %/V	3.2 %/V	4.1 %/V	2.9 %/V
W/L=300/23 μm	-	-	6.7 %/V	4.5 %/V

Sensitivity of the hold current to the V_T shift is much smaller in the pixel circuits with feedback than that is a 2-TFT circuit. For instant, for 2.5-V V_T shift in a feedback circuit with T2=100/23 and a programming current of 2 μA, the relative error is less than 7% while for a 2-TFT pixel circuit, the relative error is in excess of 95 %.

4.4.3 Effect of Temperature

Sensitivity of programming and hold currents to temperature is measured. To discover the effect of temperature on the programming current, the temperature-sensitivity of the pixel current is measured for two cases: In the first test, V_{IN} is a constant voltage. In the second test, the temperature-independent circuit in Fig 4.9 is used. Fig 4.30 shows the measured relative current as a function of the temperature for a nominal current of 5.2μA. In the first experiment, the change in current is close to 14% for a range of 60 ^oC. By using the temperature-independent circuit, the error in the current is reduced to less than the sensitivity of the measured setup.

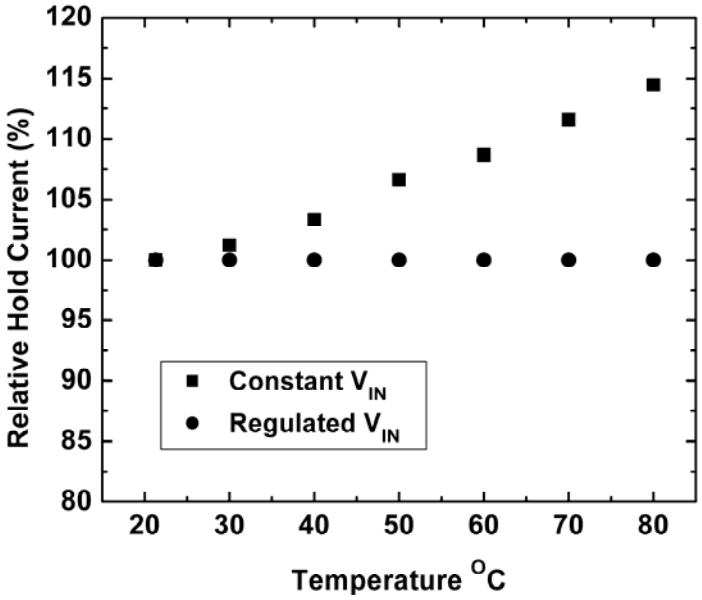
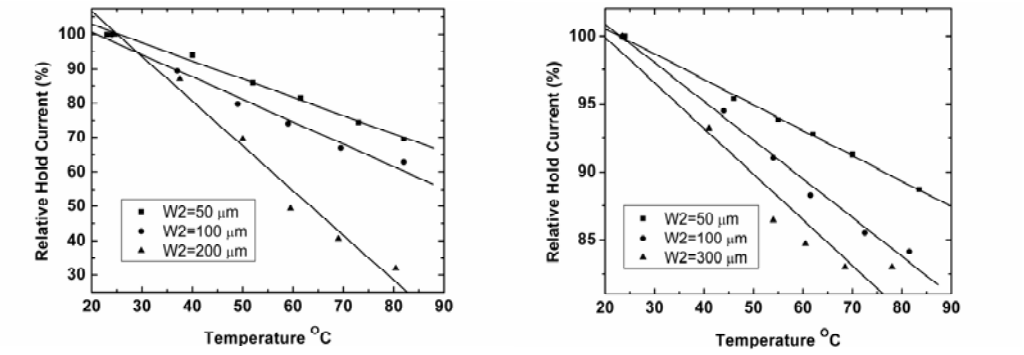


Figure 4.30: Relative error in the programming current as a function of temperature for constant and regulated V_{IN}.

The sensitivity of the hold current to the temperature is measured for different sizes of T2. The pixel circuit in Table 4.4 is used for the tests. Fig 4.31 (a) and (b) show the relative current as a function of the temperature for the programming currents of 1 μA and 2 μA. As predicted in Section 4.3.4, by increasing the temperature, the hold current decreases, and the error rate is higher for the larger sizes of T2. The relative change in the hold current is larger for smaller currents. For the 1-μA current, the changes in the hold current over a temperature range between 25 ^{o}C to 75 ^{o}C are 25%, 33%, and 60% for W/L sizes of T2 equal to 50μm/23μm, 100μm/23μm, and 300μm/23μm, respectively. For the 2-μA current, the changes are 9%, 15%, and 20% for the same W/L sizes and temperature ranges. From the measurement results, it can be seen that the sensitivity of the hold current to the temperature is considerable, particularity for the large sizes of T2 and smaller currents. Therefore, the size of T2 must be as small as possible. A lookup-table-based temperature compensation system is required for some applications.



(a) (b)

Figure 4.31: Measured relative error in the hold current as a function of temperature for:

(a) I_{PROG}=1 μA, (b) I_{PROG}=2 μA.

4.4.4 Settling Time

Fig 4.32 shows the measured 5%-settling time of the pixel circuit whose parameters are listed Table 4.5 as a function of the programming current for 50 pF, and 100 pF parasitic capacitances. For currents smaller than 4 μA, no overshoot was observed. For C_{PF} smaller than 1 nF, the programming current was stable whereas for larger C_{PF}, instability in the programming current is observed. The tendency of the circuits to operate in the over-damped mode is more than the tendency predicted by the simulation results. This can be explained by the considerable difference between the TFT device model used for the simulations and the parameters of the fabricated TFT. The effective mobility of the fabricated TFTs is three times large than that in the model. Moreover, the conductance of the n+ microcrystalline contacts is improved by a factor of ten in the fabricated TFTs. As a result, the poles associated to T2 and T3 are shifted toward higher values, increasing the stability.

It is important to note that although the settling time in the proposed AMOLED pixel circuits with voltage feedback are much faster than the CPPCs with similar TFT and capacitor sizes, the programming times are still large and might not fulfill the requirements for high-resolution displays.

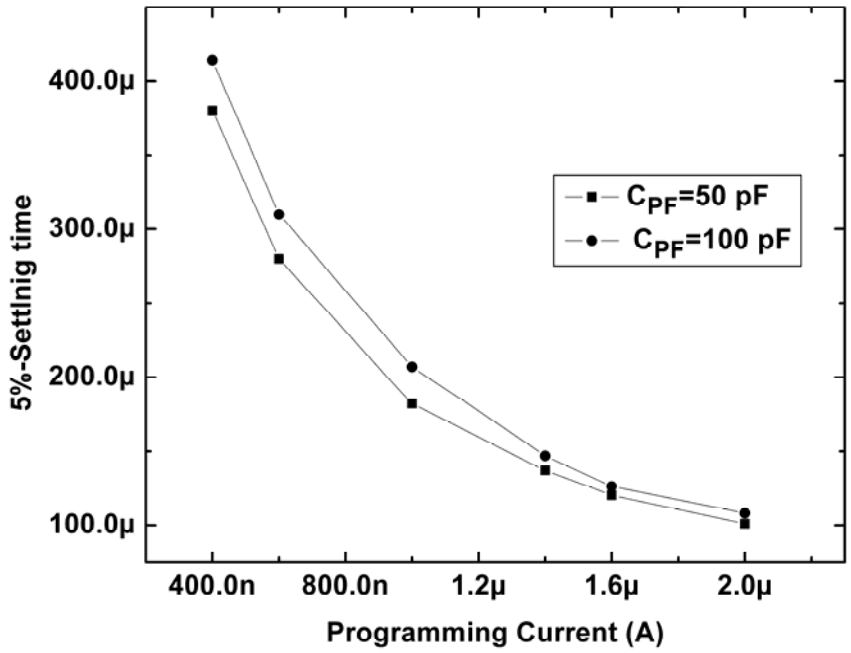


Figure 4.32: Measured settling time of a pixel circuit with voltage feedback as a function of the programming current for different line capacitances.

4.5 Conclusion

A new scheme of driving AMOLED displays with a-Si TFTs is presented based on feedback. By sending a feedback voltage from each pixel to a column driver during the programming cycle, the driving scheme can compensate for V_T shift and other variations of a-Si TFTs. Measurement results demonstrate that the OLED current is highly stable. The only noticeable source of instability is V_T-dependent charge injection of the TFT switched which results in a rise in the hold current. This effect can be reduced by choosing TFT switches with small sizes. Both analysis and measurements results demonstrate a current-dependent settling behavior. For small programming currents, the settling times are larger due to lower loopgain of the system. The settling time is also affected by a time constant associated with the resistance of the feedback switch and the parasitic capacitance of the feedback line. Due to sensitivity of the settling time to parasitic capacitance of the feedback line, voltage driving is not fast enough for high-resolution, large-area displays.

Chapter 5
Driving AMOLED Pixel Circuits with Current Feedback

As discussed in Chapter 4, negative feedback can be used to effectively reduce the sensitivity of the OLED current to the V_T shift of TFTs, the shift in the OLED voltage, and temperature variations. However, AMOLED pixels with voltage feedback require a current-to-voltage converter element in the current path of the OLED. In the circuits presented in Chapter 4, the n+ resistor acts as the current-to-voltage converter. Although the n+ resistors demonstrate high stability, the uniformity of the current is limited by their matching properties. Another disadvantage of the proposed circuits is the slow settling times at low programming currents. The slow settling mainly stems from the delay in the feedback line associated with its large parasitic capacitance and the large resistance of the feedback switch.

In this chapter, a driving scheme based on current feedback is introduced. Since the feedback signal is current, there is no need for a current-to-voltage converter; thus, better uniformity is expected. Moreover, by using a transresistance amplifier as the external column driver with an accelerating pulse at low programming currents, a fast current settling is achieved.

5.1 AMOLED Pixel Circuits with Current Feedback

Fig. 5.1 shows a schematic of the implementation of a pixel circuit with current feedback and the external column driver [88]. It comprises a pixel circuit, a column driver, and the associated controlling signals. The pixel circuit consists of a drive TFT (T1), three switch TFTs (T2-T4), a storage capacitor (C_S), and an OLED. The external column driver is a single-ended operational transresistance amplifier (OTRA). Luminance data is provided by a current source (I_{DATA}). I_{DATA} can be a current-steering digital to analog converter, or a voltage-to-current converter circuit.

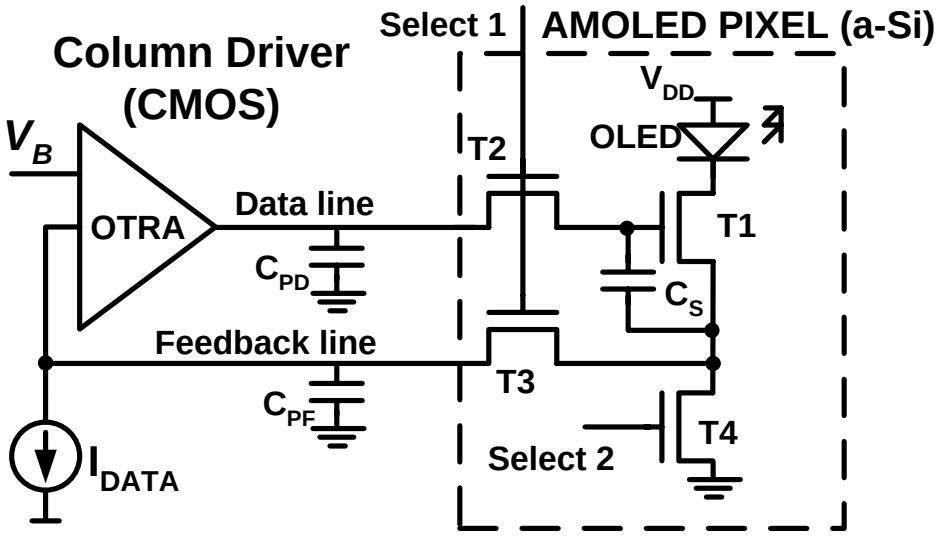


Figure 5.1: AMOLED pixel circuit with current feedback and the external column driver.

The pixel circuit has two modes of operation: programming and hold. During the programming mode, select 1 is high and select 2 is low, turning T2 and T3 on and T4 off. Consequently, the gate and the source terminals of T1 are connected to the output and input terminals of the OTRA through the data and feedback lines. Due to the inherent negative feedback in the circuit, the OTRA adjusts the gate voltage of T1 to minimize the difference between the current through T1 with the data current. If the transresistance of the OTRA is high, the current through T1 becomes approximately equal to I_{DATA}. In the hold mode, select 1 is low and select 2 is high, disconnecting T1 from the OTRA. Consequently, a current close to I_{DATA} starts flowing into the OLED since the gate-source voltage of T1 is stored in C_S. V_{DD} must be high enough to keep T1 in the saturation region in both the programming and hold modes. The pixel circuit compensates for the V_T shift in T1 as long as the gate voltage of T1 does not exceed the swing of the OTRA, and T2 can be turned on properly by select 1.

Fig. 5.2 and Fig. 5.3 show two possible alternatives with common-cathode OLED [89]. The pixel circuit in Fig. 5.2 has only three TFTs, and one select line. In this circuit, the voltage of the feedback

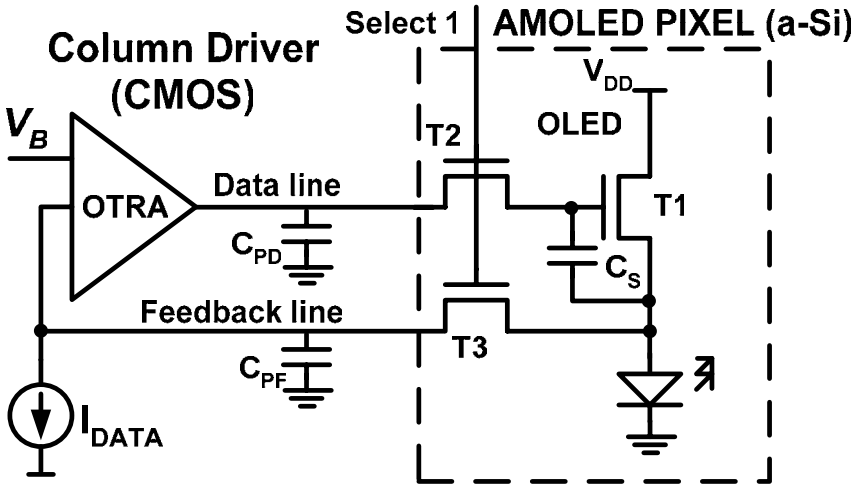


Figure 5.2: 3-TFT pixel circuit with current feedback.

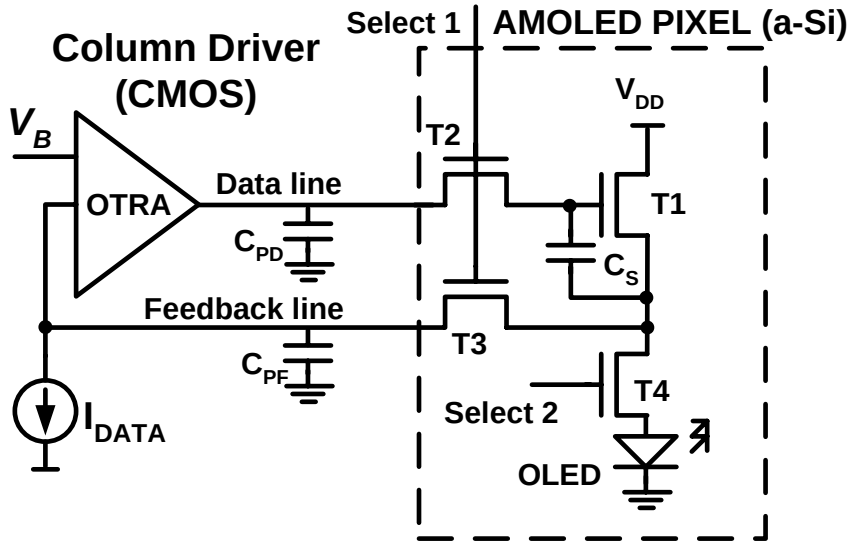


Figure 5.3: 4-TFT pixel circuit with current feedback with common-cathode OLED.

line (V_B) is selected low enough to retain the OLED in the reverse bias during the programming mode. To satisfy this condition, the upper limit of V_B must be

$$V_B < V_{OLED} - R_{DS3} I_{DMAX} \tag{5.1}$$

where I_{DMAX} is the maximum programming current, R_{DS3} is the ON resistance of T3, and V_{OLED} on is the ON voltage of the OLED.

Table 5.1: Circuit parameters used for circuit-level simulations.

Design Parameter	Value
C_S (pF)	4
W1/*L1* (μm)	600/23
W2/*L2* (μm)	50/23, 100/23, 200/23
W3/*L3* (μm)	600/23
W4/*L4* (μm)	600/23
I_{DATA} (μA)	0-2
Select 1,2 voltage (V)	0 -20

Although the circuit in Fig. 5.2 has fewer TFTs and a lower power consumption, it has a slower settling, which is discussed in more details in Section 5.2.5.

5.2 Analysis of the Performance

In the following sections, a comprehensive study of the performance of the driving scheme is conducted. The arrangement of the analysis is similar to the study of the voltage feedback driving, presented in Section 4.3.

5.2.1 Analysis of the Stability

The primary causes of instability in the pixel circuits with current feedback are similar to those in the circuits with voltage feedback, including the limited feedback loop gain, the V_T-dependent charge injection, and the change in the I-V of the OLED.

5.2.1.1 Static Stability

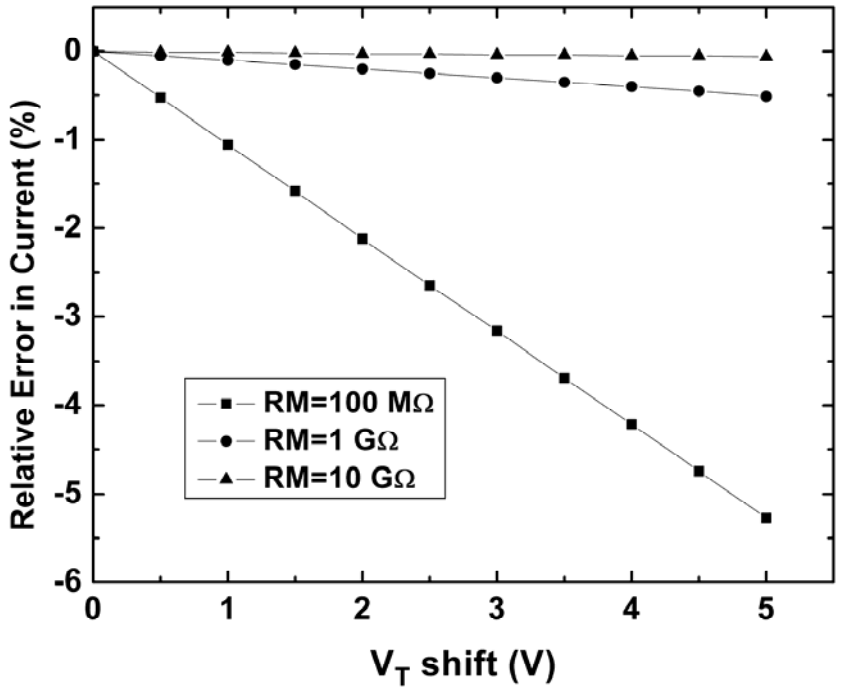


Figure 5.4: Error in the programming current as a function of V_T shift in T1 for the 4-TFT pixel circuit shown in Fig. 5.1.

For an ideal OTRA with an infinite transresistance, the current through T1 during the programming mode (I_{PROG}) is equal to I_{DATA}. However, due to the limited transresistance of the OTRA, I_{PROG} depends slightly on the threshold voltage of T1 (V_{T1}). Assuming that the input resistance of the OTRA is zero, I_{PROG} is calculated by

$$I_{PROG} = \frac{KR_M^2 I_{DATA} - KR_M V_{T1} + 1 - \sqrt{1 - 2KV_{T1}R_M + 2KR_M^2 I_{DATA}}}{KR_M^2}, \tag{5.2}$$

where R_M is the transresistance of the OTRA. For a high R_M, I_{PROG} is approximately equal to

$$I_{PROG} \approx I_{DATA} - \frac{V_{T1}}{R_M}. \tag{5.3}$$

If R_M is very large, V_{T1}/R_M is much smaller than I_{DATA} and the effect of V_{T1} can be neglected. For instance, for a minimum programming current of 100 nA and a V_T shift of 5 V, R_M should be larger than 5 GΩ to achieve less than 1% error in I_{PROG}. For further investigation, the 4-TFT pixel circuit in

Fig. 5.1 is simulated with the design values listed in Table 5.1. Fig. 5.4 shows the relative error in I_{PROG} as a function of ΔV_{T1} for different values of R_M for I_{PROG}=1 μA. For R_M=10 GΩ, the error in I_{PROG} is less than 0.1% which is negligible.

5.2.1.2 Dynamic Stability

The effect of the V_T-dependent charge injection of T2 on the OLED current is similar to that in the voltage feedback circuits. Based on the same approach, the change in the current induced by the shift in the threshold voltage in the drive TFT (ΔV_{T1}) is estimated by

$$\Delta I_{error} = g_m \beta \frac{C_{GS2}}{C_{GS1} + C_S} \Delta V_{T1}. \tag{5.4}$$

Since ΔI_{error} is positive, an increase in the hold current is expected as V_{T1} shifts over time. In the 3-TFT pixel circuit, in addition to the error induced by the V_T shift, the shift in the OLED voltage induces an error to the V_{GS} of T1 (V_{GS1}) through its gate-drain overlap capacitor. The associated change in V_{GS1} (ΔV_{GS1}) is approximated by the following:

$$\Delta V_{GS1} = -\frac{C_{ov1}(V_{OLED} - V_B - I_{OLED} R_{DS3})}{C_{GS1} + C_S}. \tag{5.5}$$

C_{ov1} is the overlap capacitor between the gate and drain of T1. The associated error in the hold current is given by

$$\Delta I_{error} = -g_m \frac{C_{ov1}}{C_{GS1} + C_S} \Delta V_{OLED}. \tag{5.6}$$

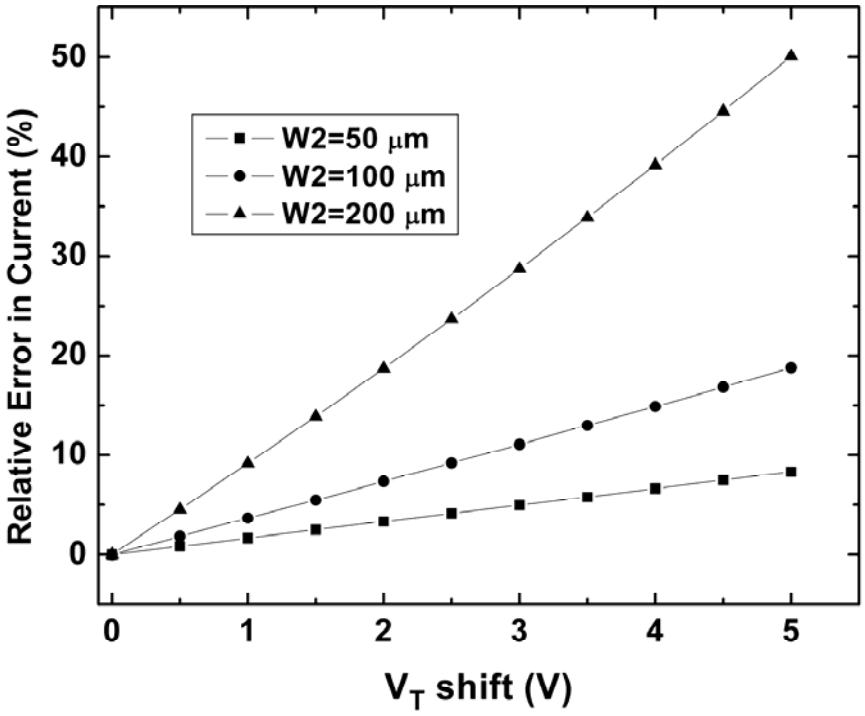


Figure 5.5: Relative error in the hold current in the circuit of Fig. 5.1 as a function of ΔV_{T1} for different sizes of T2.

Equation (5.6) predicts that in contrast to the effect of the V_T shift, the shift in the OLED voltage reduces the hold current. To investigate the effect of the V_T-dependent charge injection, the 4-TFT and 3-TFT circuits shown in Fig. 5.1 and 5.2 are simulated with the circuit parameters listed in Table 5.1.

Fig. 5.5 shows the relative error in the hold current in the 4-TFT circuit as a function of ΔV_{T1} for different sizes of T2 for I_{PROG}=1 μA. As predicted by (5.4), the error increases as ΔV_{T1} increases, and for the larger sizes of T2, the sensitivity to the V_T shift is higher. Simulation of the 3-TFT circuit shows similar results. The effect of shift in the OLED voltage on the hold current is also simulated for the 3-TFT circuit. The relative error in the hold current as a function of ΔV_{OLED} is shown in Fig 5.6 for different overlap sizes of T1. As predicted by (5.6), the larger overlap sizes result in a higher sensitivity of the hold current to $\Delta V_{OLED.}$

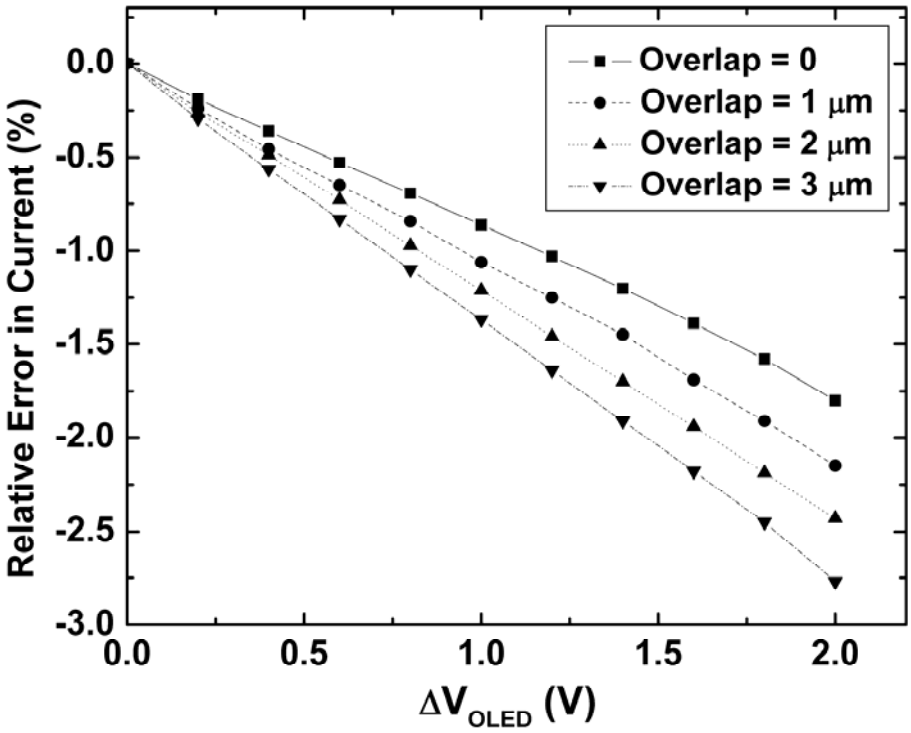


Figure 5.6: Relative error in the hold current as a function of ΔV_{OLED} for different TFT overlap sizes.

5.2.1.3 Instability Due to Change in V_{DS} of T1

In the presented pixel circuits, the drain-source voltage of T1 changes during the transition from the programming to the hold mode. Due to the imperfect saturation characteristics of T1, the change in V_{DS1} (ΔV_{DS1}) causes error in the hold current. ΔV_{DS1} depends on the OLED voltage in the 3-TFT and the OLED voltage and the ON resistance of T4 in the 4-TFT circuits. Therefore, as the voltage OLED and the V_T of T4 shifts over time, ΔV_{DS1}, and thus, the hold current decreases. The error induced in the OLED current by the change in ΔV_{DS1} depends on the circuit, and can be estimated by a small-signal analysis similar to that presented in Chapter 4. For the 4-TFT circuit, ΔV_{DS1} during the transition from the programming to mode the hold mode is given by

$$\Delta V_{DS1} = V_{DS}(hold) - V_{DS}(porgram) = V_B + I_{OLED}\left(R_{DS3} - R_{DS4}\right) - V_{OLED} \tag{5.7}$$

where R_{DS3} and R_{DS4} are the ON resistance of T3 and T4, respectively. Assuming that R_{DS4} is approximately equal to $1/[K_4(V_{GS4}-V_{T4})]$, the error induced by the variations of V_{T4} (ΔV_{T4}) in the hold current is expressed as:

$$\Delta I_{error} = \frac{1}{r_{ds1}} \frac{\partial \Delta V_{DS1}}{\partial V_{T4}} \Delta V_{VT4} = -\frac{I_{OLED}}{r_{ds1}} \frac{1}{K_4 (V_{G4} - V_{T4})^2} \Delta V_{T4} \tag{5.8}$$

where r_{ds1} is the small-signal drain-source resistance of T1. To reduce the sensitivity of the hold current to ΔV_{T4} the overdrive voltage of T4, (V_{GS4}-V_{T4}) should be large. Simulation results show that for V_{G4}-V_{T4} equal to 25, the relative error is less than 0.1% for I_{PROG}=100nA, and is negligible. In the 3-TFT circuit, the shift in the OLED voltage (ΔV_{OLED}) changes ΔV_{DS1} since the OLED is out of the circuit during the programming mode. In this circuit, ΔI_{error} is given by:

$$\Delta I_{error} = \frac{1}{r_{ds1}} \frac{\partial \Delta V_{DS1}}{\partial V_{OLED}} \Delta V_{OLED} = -\frac{\Delta V_{OLED}}{r_{ds1}}. \tag{5.9}$$

Due to the large size of r_{ds1} the associated ΔI_{error} is much smaller than the errors that were studied in Section 5.2.1.2.

5.2.2 Effect of Reverse Current of TFTs

Similar to the pixels with voltage feedback, the reverse currents of the feedback switches in the pixel circuits in the same column cause an error in the programming current of the selected pixel. If the reverse current of each feedback switch is I_{OFF}, then the programming current of the selected pixel is approximated by

$$I_{PROG} = I_{DATA} + (N-1) I_{OFF} \tag{5.10}$$

where N is the number of display rows. Compared to the pixel circuits with voltage feedback, it is observed that the error in the current feedback driving scheme is ($1+R_{S3}/R_F$) times smaller.

5.2.3 Effect of Temperature

Due to the negative feedback of the system, the programming current in the presented pixel circuits are almost independent of the temperature. However, the temperature-dependent charge injection of T2 causes temperature-dependent variations in the hold current. Similar to the circuits with voltage feedback, any increase in the temperature decreases the V_T of T1 and T2, increasing the channel charge of T2. As a result, the charge injected by T2 at the end of the programming mode increases, therefore, the hold current decreases.

In the 3-TFT pixel circuit, the OLED voltage also decreases, when the temperature increases. A reduction in the OLED voltage results in an increase in the hold current through T1 overlap capacitor as described in Section 5.2.1.2. Therefore, in this circuits change in V_{T1} and V_{T2} and change in V_{OLED} with temperature has opposite effects on the current and the overall change in the OLED current is determined by the temperature-dependent characteristics of the OLED and TFTs.

5.2.4 Power Consumption

The power efficiencies in the 4-TFT and 3-TFT pixel circuits are given by (5.11) and (5.12) respectively:

$$\eta_P(I) = \frac{V_{OLED}}{V_{DD}} = \frac{V_{OLED}(I_{PROG})}{V_{DS1}(I_{PROG}) + V_{OLED}(I_{PROG}) + R_{DS4} I_{PROG}}, \tag{5.11}$$

$$\eta_P(I) = \frac{V_{OLED}}{V_{DD}} = \frac{V_{OLED}(I_{PROG})}{V_{DS1}(I_{PROG}) + V_{OLED}(I_{PROG})}. \tag{5.12}$$

Due to the series resistance of T4, the 4-TFT pixel circuit requires a higher supply voltage, lowering the power efficiency. Unlike the pixel circuits with voltage feedback, it is not possible to decrease the power consumption by biasing T1 in the triode region. The reason is that the terminal voltages of T1 change from the programming to the hold mode in the current feedback circuits. Therefore, V_{DS} of T1 is different in the programming and the hold modes. As a result, if T1 is biased

in the triode region, the hold current of the pixel circuit cannot be predicted accurately since it highly depends on V_{DD}, V_{OLED}, and the ON resistance of T4.

5.2.5 Settling Time

The effect of parasitic capacitance of the data and feedback lines (C_{PD} and C_{PF}) on the settling time is suppressed by using an OTRA as the external column driver. Due to the low input and output impedance of the OTRA, the time constants, associated with C_{PD} and C_{PF} are small. However, the limited bandwidth of the OTRA, the high ON resistance of the TFT switches, and the size of C_S, affects the settling time. More importantly, the wide range of the loop gain for the entire range of the OLED current results in a varied settling behaviour. In the 3-TFT pixel circuit, large parasitic capacitance of the OLED (C_{OLED}) also has a negative role in the settling time.

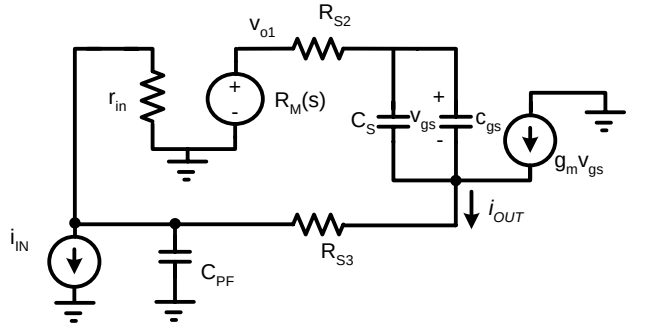
5.2.5.1 Small-Signal Analysis

To investigate the effect of the parasitic capacitances and the circuit parameters on the settling time, a small-signal analysis of the circuit is performed. The simple small-signal equivalent circuits of the pixel circuits in Fig. 5.1 and 5.2 in the programming mode are shown in Fig. 5.7 (a) and Fig 5.7 (b), respectively.

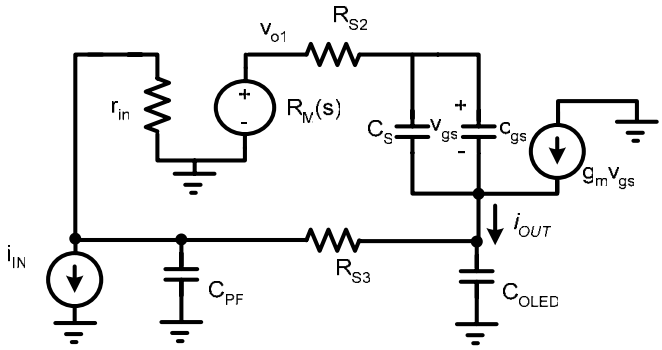
T1 is modelled by c_{gs} and g_m. R_{S2} and R_{S3} are the ON resistances of T2 and T3, respectively. OTRA is modelled by an input resistance (r_{in}) and a current-controlled voltage source with a transresistance equal to

$$R_M(s) = \frac{R_{M0}}{1 + \frac{s}{\omega_p}}. \tag{5.13}$$

Here, R_{M0} is the DC transresistance and ω_p is the dominant pole of the OTRA. Simulations show that the effect of the second pole of the OTRA associated with C_{PD} is small compared with the effect of the other poles, and is neglected in the analysis. For the 3-TFT pixel circuit, the OLED in the



(a)



(b)

Figure 5.7: Small-signal equivalent circuits for: (a) circuit in Fig. 5.1, (b) circuit in Fig. 5.2.

reversed bias is modeled by C_{OLED}. Both of the circuits have a shunt-series feedback. The open-loop transfer function of the circuit, A_L(s), for the 4-TFT circuit is:

$$A_L(s) = \frac{1}{1 + r_{in} C_{PF} s} \cdot \frac{R_{M0}}{1 + \dfrac{s}{\omega_p}} \cdot \frac{g_m + (c_{gs} + C_S)s}{1 + R_{S3} g_m + (R_{S2} + R_{S3})(c_{gs} + C_S)s}. \tag{5.14}$$

A_L(s) has three poles and a zero equal to

$$z_1 = -\frac{g_m}{(c_{gs} + C_S)}, \tag{5.15}$$

$$p_1 = -\omega_p, \tag{5.16}$$

$$p_2 = -\frac{1}{r_{in}C_{PF}}, \tag{5.17}$$

$$p_3 = -\frac{1+R_{S3}g_m}{\left(R_{S2}+R_{S3}\right)\left(c_{gs}+C_S\right)}. \tag{5.18}$$

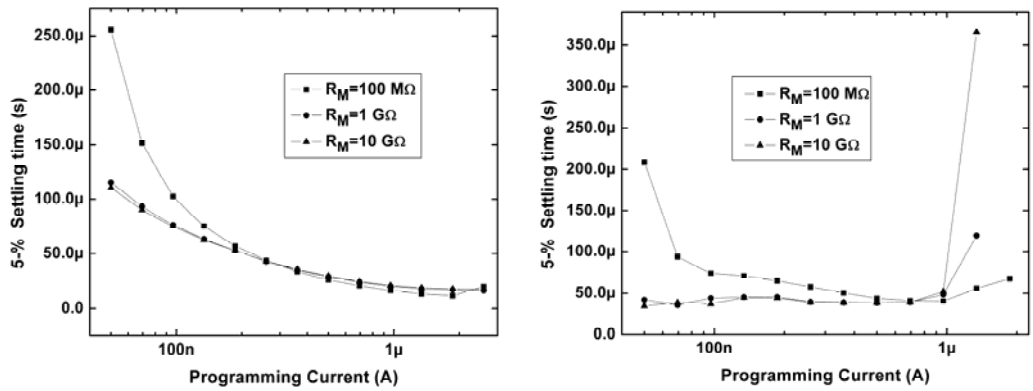
Despite the large size of C_{PF}, p_2 is much larger than other poles thanks to the small value of r_{in}. As a result, the closed-loop settling behaviour of the circuit is mainly affected by ω_p, p_3, and z_1. Generally, ω_p is the dominant pole of the system. The effect of p_3 on settling can be suppressed by reducing the size of C_S, and decreasing R_{S2}, and R_{S3} by increasing the size of T2 and T3. However, based on (5.4), reducing C_S increases the sensitivity of the current to the V_T shift. In addition, the maximum sizes of T2 and T3 are limited by the available pixel area. The DC loop gain of the circuit (A_{DC}) is equal to

$$A_{DC} = \frac{R_{M0}g_m}{1+R_{S3}g_m}. \tag{5.19}$$

Due to the large current range of the programming current, the variations of g_m are large. Therefore, the range of the A_{DC} is large, resulting in different settling behaviours in the OLED current range. In particular, for low programming currents, the circuit might be over-damped, resulting in a slow settling.

The 3-TFT pixel circuit has a more complicated open-loop transfer function that is expressed as

$$A_L(s) = \frac{1+R_{S3}C_{OLED}s}{1+\left(R_{S3}C_{OLED}+r_{in}C_{PF}+r_{in}C_{OLED}\right)s+r_{in}R_{S3}C_{PF}C_{OLED}s^2}\cdot \frac{R_{M0}}{1+\frac{s}{\omega_p}}\cdot\frac{g_m+s\left(c_{gs}+C_S\right)}{1+g_mR_{S3}+\left(\left(R_{S2}+R_{S3}\right)\left(c_{gs}+C_S\right)+R_{S3}C_{OLED}\right)s+R_{S2}R_{S3}C_{OLED}\left(c_{gs}+C_S\right)s^2}. \tag{5.20}$$



(a) (b)

Figure 5.8: 5-% settling time as a function of the programming current for different values of R_M for: (a) 4-TFT circuit, (b) 3-TFT circuit.

Assuming that C_{OLED} is much larger than (C_S+c_{gs}) and r_{in} is very small, the first term in (5.20) has a doublet close to -1/$R_{S3}C_{OLED}$ and another pole close to -1/$r_{in}C_{PF}$. The third term in (5.20) has a zero at -g_m/(C_S+c_{gs}), and two poles close to -1/$R_{S3}C_{OLED}$ and -1/R_{S2}(C_S+c_{gs}). Compared to the 4-TFT, the 3-TFT circuit has an extra pole and a doublet close to -1/$R_{S3}C_{OLED}$. Due to the large size of C_{OLED} and R_{S3}, these poles and zeros are large and result in a slower settling.

5.2.5.2 Evaluation and Enhancement of the Settling

The transient responses of the 4-TFT and 3-TFT circuits are simulated by CADENCE SPECTRE. The parameters of the pixel circuit are the same as those listed in Table 5.1. A behavioural model with ω_p=100 rad/s and r_{in}=0 is used for the OTRA. Fig 5.8 (a) and (b) show the simulated settling time as a function of the programming current for different values of R_M. It can be seen that the settling time in the 3-TFT circuit is considerably larger at higher currents. For a specific value of R_M, the minimum settling time is also longer in the 3-TFT pixel circuit. Compared to the pixels with voltage feedback, the settling time of the pixels with current feedback is smaller than that in the pixel circuits with voltage feedback.

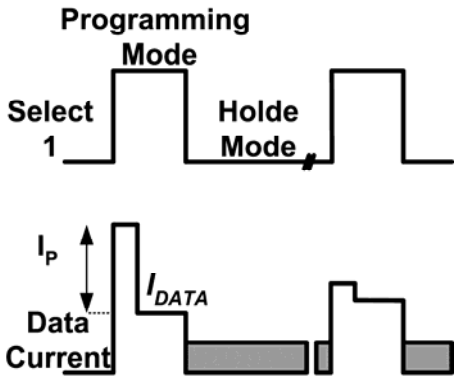


Figure 5.9: The accelerating current pulse in current feedback driving.

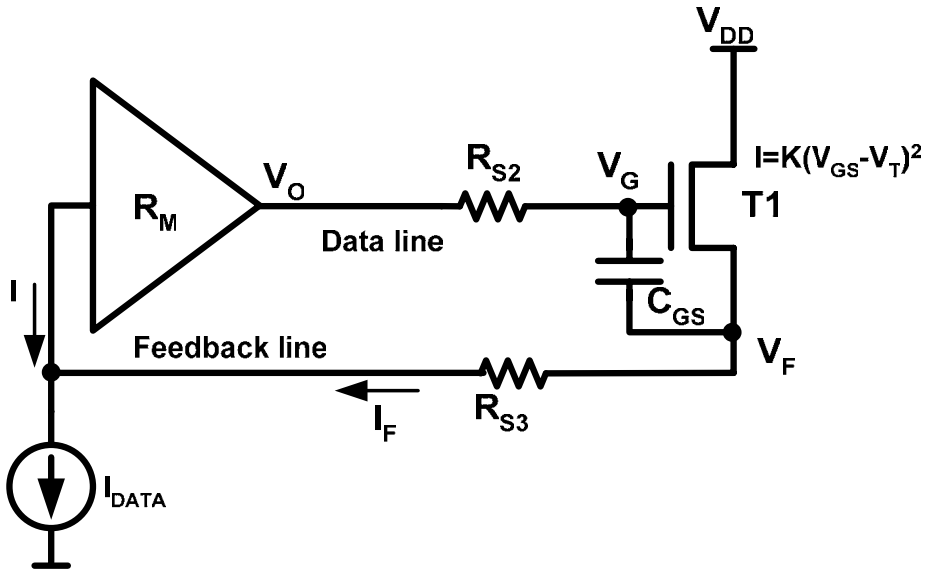


Figure 5.10: Simplified non-linear model used to calculate the optimum amplitude of the accelerating

To improve the programming speed at low currents, in particular in the 4-TFT pixel circuit, an accelerating current pulse is added to the beginning of the programming current, as illustrated in Fig 5.9 [90]. The accelerating current pulse precharges C_S and increases the transconductance of T1 at the beginning of the programming mode thus reducing the settling time.

For a specific programming current, there is an optimum current pulse that yields the fastest settling time. The simple model in Fig. 5.10 is used to analyze the settling time when the accelerating pulse is applied. V_{GS1} is determined by the following differential equation:

$$\left(\left(C_S + c_{gs1}\right) + \frac{R_{S2}\left(C_S + c_{gs1}\right)}{R_{S3} + R_M}\right)\frac{dV_{GS1}}{dt} = -K\left(V_{GS1} - V_T\right)^2 - \frac{V_{GS1}}{R_{S3} + R_M} + \frac{R_M}{R_{S3} + R_M} I_{DATA}. \quad (5.21)$$

Since R_M is much larger than R_{S2} and R_{S3}, (5.21) can be reduced into the simpler equation:

$$\left(C_S + c_{gs1}\right)\frac{dV_{GS1}}{dt} = -K\left(V_{GS1} - V_T\right)^2 + I_{DATA}. \quad (5.22)$$

By solving (5.22), V_{GS1} is calculated and thus, I_{PROG} is given by

$$I_{PROG}(t) = I_{IN}\left(\frac{e^{\frac{t}{\tau_{IN}}} - C_{IN}e^{-\frac{t}{\tau_{IN}}}}{e^{\frac{t}{\tau_{IN}}} + C_{IN}e^{-\frac{t}{\tau_{IN}}}}\right)^2. \quad (5.23)$$

Here, τ_{IN} is equal to $\frac{C_S + c_{gs1}}{\sqrt{KI_{DATA}}}$, and C_{IN} corresponds to the initial condition of V_{GS1} and is given by

$$C_{IN} = \frac{\sqrt{\frac{I_{DATA}}{K}} - V_0}{\sqrt{\frac{I_{DATA}}{K}} + V_0} \quad (5.24)$$

where V_0 is the initial voltage of V_{GS1}. The general solution of the settling time is then given by

$$t = \tau_{IN} \ln\left(\sqrt{C_{IN}}\sqrt{\frac{1+\sqrt{1-Er}}{1-\sqrt{1-Er}}}\right). \quad (5.25)$$

Here, Er is the settling error and is equal to $(I_{DATA}\text{-}I_{PROG}(t_{end}))/I_{DATA}$, where $I_{PROG}(t_{end})$ is the current of T1 at the end of the programming cycle. To find the optimum settling time, when the accelerating pulse is applied, V_{GS1} at the end of t_p (V_{OP}) is calculated from (5.22) for I_{DATA}=I_P by the following:

$$V_{OP} = \sqrt{\frac{I_P}{K}}\tanh\left(\frac{t_p}{\tau_p}\right), \quad (5.26)$$

and the result is substituted into (5.24) as V_0 to calculate the settling time for $t>t_p$. From (5.25), it can be seen that for $t>t_p$ the settling time is zero if the following condition is satisfied:

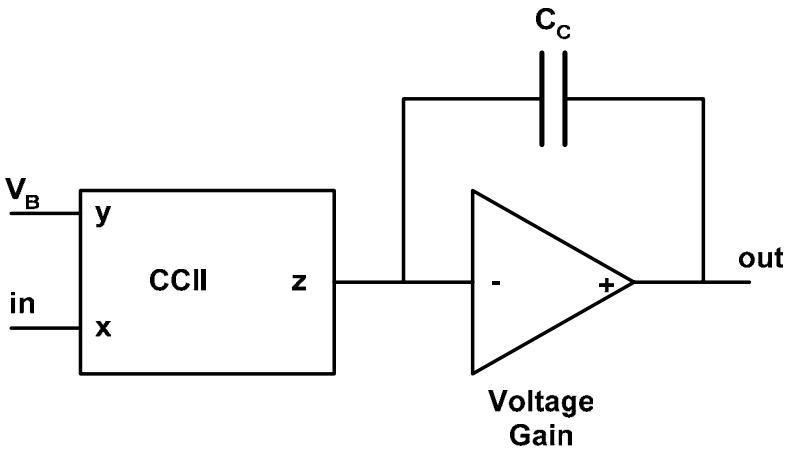


Figure 5.11: General implementation of an OTRA.

$$C_{IN}\frac{1+\sqrt{1-Er}}{1-\sqrt{1-Er}}=1. \tag{5.27}$$

By substituting (5.26) into (5.27),

$$\sqrt{\frac{I_P}{K}}\tanh\left(\frac{t_p}{\tau_p}\right)=\sqrt{1-Er}\sqrt{\frac{I_{DATA}}{K}}\ . \tag{5.28}$$

Since $t_p << \tau_p$, (5.28) is simplified to

$$I_P t_p=\sqrt{1-Er}\left(C_S+c_{gs1}\right)\sqrt{\frac{I_{DATA}}{K1}}\ . \tag{5.29}$$

Equation (5.29) indicates that for a specific programming current, the product of I_P and t_p is constant. In other words, the charge delivered by the accelerating pulse for a specific programming current is constant and proportional to C_S and square root of the programming current.

5.3 Design of the OTRA

Ideally, an OTRA has a zero input resistance and an infinite transresistance. A common method for the implementation of an OTRA is cascading a second generation current conveyor (CCII) with a voltage gain stage, as shown in Fig. 5.11 [91]. In a CCII [92], the x terminal has low input impedance and follows the voltage at the high-impedance y terminal. The high-impedance z terminal copies the

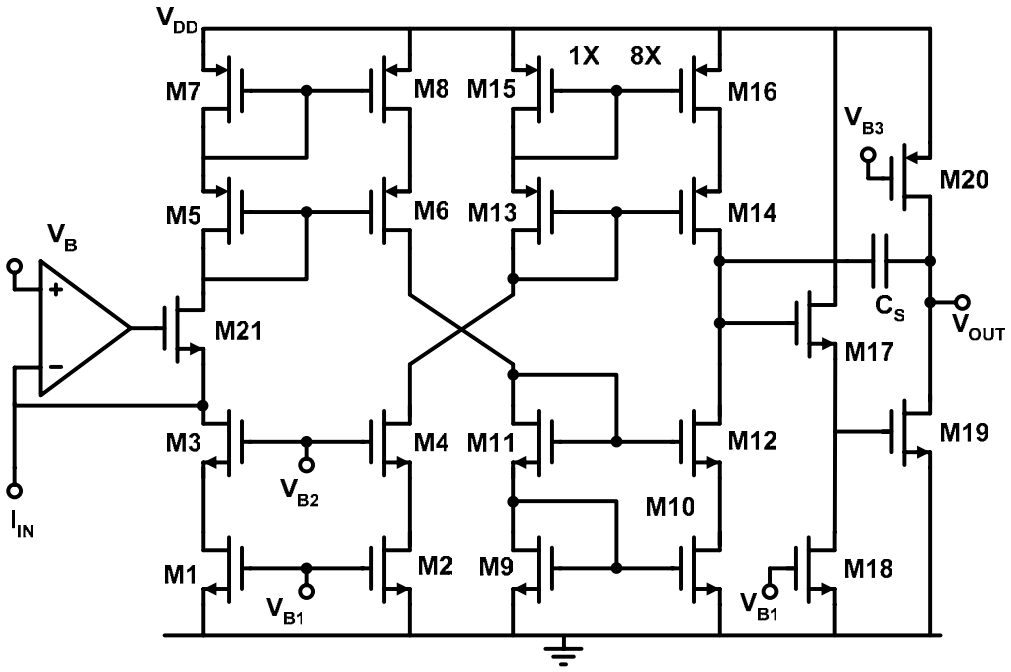


Figure 5.12: Schematic of the implemented CMOS OTRA.

current of x. To achieve a high transresistance in excess of 1 GΩ, the voltage gain stage is used. C_C is the compensating feedback capacitor.

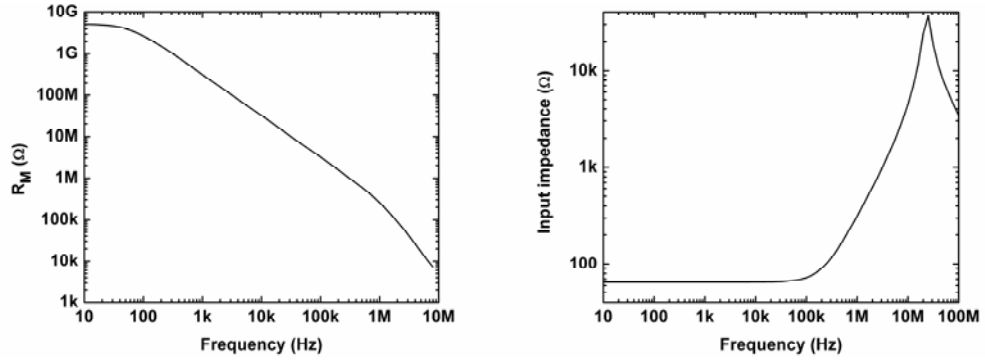
A CMOS implementation of a single-input, single-output OTRA is shown in Fig. 5.12. The OTRA consists of a class-A current conveyor as the input stage, a current amplifier, and an output voltage amplifier. The input stage of the current conveyor is realized by a low-impedance input stage composed of M21 and a feedback amplifier. The feedback amplifier is used as the input stage to reduce r_{in} and fix the voltage of the input terminal. The feedback amplifier is a differential amplifier with PMOS input transistors. Based on small-signal analysis, r_{in} is approximated by

$$r_{in} \approx \frac{1}{(A_{IN}+1)g_{m21}} \tag{5.30}$$

where A_{IN} is the voltage gain of the feedback amplifier. The casocde current mirror composed of M5 to M8 conveys the input current to the current amplifier. The bias current of the current is mirror is provided by two cascade current sources relized by M1, M2, M3, and M4. The bias current of the

Table 5.2: Circuit parameters used for the circuit-level simulations (all sizes in micrometre).

Transistor	Size	Transistor	Size
M1-M4	20/6	M21	40/6
M9,M11	20/6	M5-M8	20/4
M10, M12	160/6	M13, M15	20/4
M17, M18	40/6	M14, M16	160/4
M19	80/6	M20	80/4



(a) (b)

Figure 5.13: Frequency responses of the OTRA: (a) R_M, (b) r_{in}.

input stage is 50 μA. The second stage which consists of a PMOS and a NMOS current mirror amplifies the input current by a factor of 8 to improve the slew rate. The input current is converted to voltage by the high output resistance of the cascode stage. The output stage consists of a source-follower (M17-M18) and a class-A gain stage (M20-M21). The source follower is used as a voltage level shifter to bias M12 and M10 deep in the saturation region to achieve a higher transresistance. The open loop transresistance of the circuit at DC is approximated by

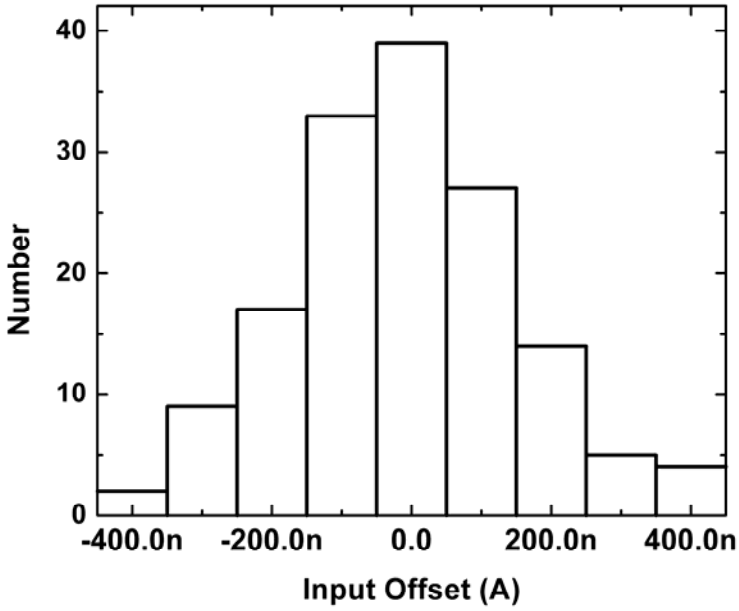


Figure 5.14: Distribution of the input offset of the OTRA from 150 Monte-Carlo simulation runs.

$$R_M = 8\left[\left(g_{m12}r_{o12}r_{o10}\right) \| \left(g_{m14}r_{o14}r_{o16}\right)\right]\frac{g_{m17}g_{m19}\left(r_{o20} \| r_{o19}\right)}{g_{m17}+g_{mb17}}. \tag{5.31}$$

The OTRA is implemented in a 0.8 μm 5/20 V quadruple well, double-metal, double-poly CMOS technology with extended drain and gate terminals. The minimum channel length of the 20V NMOS and PMOS transistors are 6 μm and 4 μm, respectively. The sizes of the transistors are listed in Table 5.2. Fig 5.13 (a) and (b) show the simulated input resistance and the transresistance as a function of the frequency. Below 100 kHz, r_{in} is close to 75Ω; above 100 kHz, r_{in} increases due to a zero, associated with the dominant pole of the feedback amplifier.

5.3.1 Offset of the OTRA

Since the current offset of the OTRA is added directly to the programming current, it should be smaller than the minimum pixel current. To reduce the offset, the selected sizes of the transistors in the current mirror are large. Due to the lack of the statistical matching data of the transistors, the

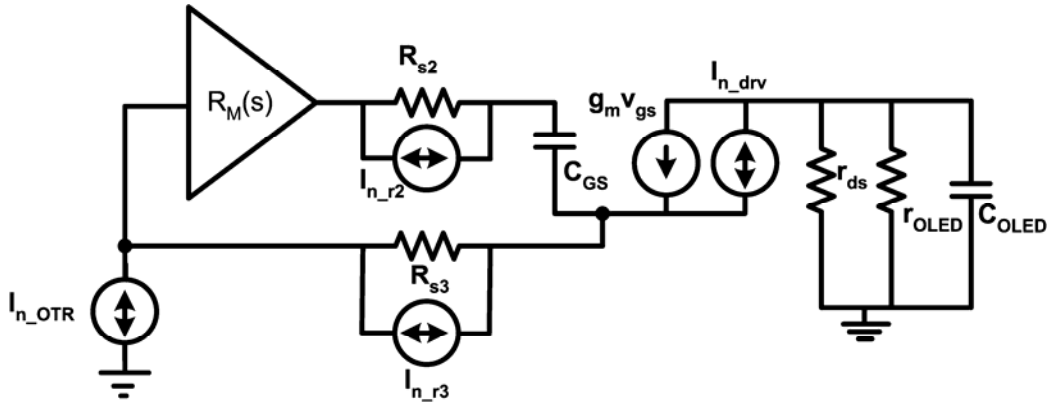


Figure 5.15: Small-signal equivalent circuit of the 4-TFT pixel circuit for noise analysis.

standard matching model of Pelgrom [93] is used. In this model, the variance of the mismatch in the threshold voltage and transconductance (β) of CMOS transistors are calculated by

$$\sigma(V_T) = \frac{A_{VT}}{\sqrt{WL}} \tag{5.32}$$

$$\frac{\sigma(\beta)}{\beta} = \frac{A_{\beta}}{\sqrt{WL}} \tag{5.33}$$

where A_{VT} and A_{β} are the mismatch constants. For the simulations, A_{VT} is set to 10 mV.μm. A_{β} is set to 2.3 %.μm and 3.2 %.μm for the n-channel and p-channel transistors, respectively. Fig. 5.14 shows the result of the circuit-level Monte-Carlo simulations for the OTRA for 150 runs. 87% of the offset values are within the range of 200 nA. While the current offset is acceptable for the current levels used in the implemented pixel circuits, it is large for some applications such as mobile applications. The current offset can be reduced by reducing the bias current and increasing the size of the mirror transistors. Another method to reduce the offset is the dynamic offset cancellation [95].

5.4 Noise Analysis

The analysis of the noise presented here is similar to the analysis of the noise in the pixels with voltage feedback. Here, the analysis for the 4-TFT pixel circuit in Fig. 5.1 is presented. Fig. 5.15

shows the equivalent small-signal of the pixel in the programming mode with the TFT and OTRA noise sources. The noise transfer functions are listed as follows:

$$\frac{i_{nOLED}}{i_{n\_r3}} = \frac{r_{s3}(\omega_p + s)}{\omega_p(1 + g_m R_{M0} + g_m r_{s3}) + \left[c_{gs}\omega_p(R_{M0} + r_{s3} + r_{s2}) + g_m r_{s3} + 1\right]s + c_{gs}(r_{s3} + r_{s2})s^2} g_m H_O(s) \quad (5.34)$$

$$\frac{i_{nOLED}}{i_{n\_r2}} = \frac{r_{s2}(\omega_p + s)}{\omega_p(1 + g_m R_{M0} + g_m r_{s3}) + \left[c_{gs}\omega_p(R_{M0} + r_{s3} + r_{s2}) + g_m r_{s3} + 1\right]s + c_{gs}(r_{s3} + r_{s2})s^2} g_m H_O(s) \quad (5.35)$$

$$\frac{i_{nOLED}}{i_{n\_drv}} = \frac{(\omega_p + s)}{\omega_p(1 + g_m R_{M0} + g_m r_{s3}) + \left[c_{gs}\omega_p(R_{M0} + r_{s3} + r_{s2}) + g_m r_{s3} + 1\right]s + c_{gs}(r_{s3} + r_{s2})s^2} H_O(s) \quad (5.36)$$

$$\frac{i_{nOLED}}{i_{n\_OTR}} = \frac{\omega_p R_{M0}}{\omega_p(1 + g_m R_{M0} + g_m r_{s3}) + \left[c_{gs}\omega_p(R_{M0} + r_{s3} + r_{s2}) + g_m r_{s3} + 1\right]s + c_{gs}(r_{s3} + r_{s2})s^2} g_m H_O(s) \cdot \quad (5.37)$$

H_O(s) is defined by (4.35), I_{n_drv} is the current noise of T1, and i_{n_r2} and i_{n_r3} are the noise currents associated with T2 and T3 switches respectively. i_{n_OTR} is the input-referred noise of the OTRA. From the circuit-level simulation of the circuit of Fig. 5.12, the power density of i_{n_OTR} is estimated as depicted in Fig. 5.16.

The noise power of the OLED current is simulated for different programming currents, and demonstrated in Fig. 5.17. The dominant term in the noise power is the noise of the OTRA, and the noise of TFTs is negligible.

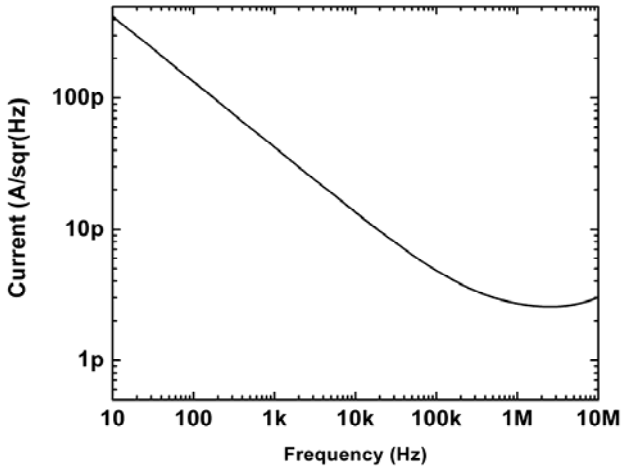


Figure 5.16: Simulated input-referred noise of the OTRA.

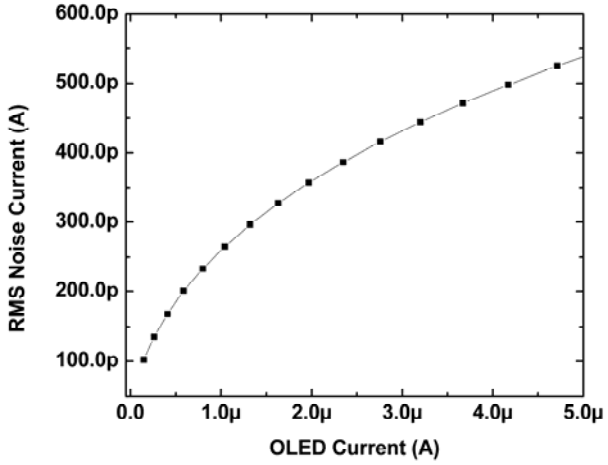
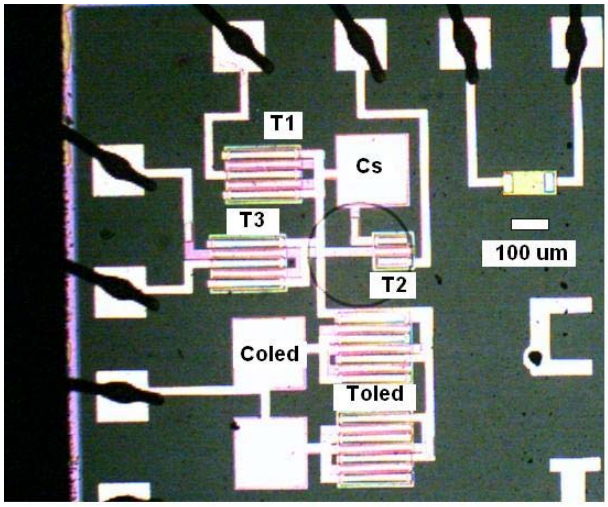
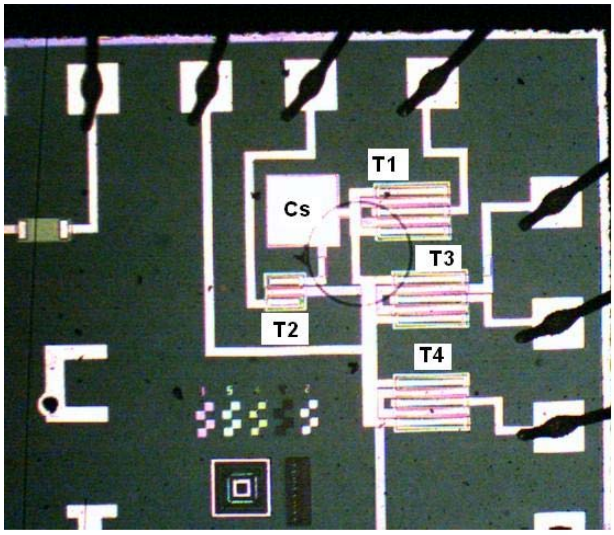


Figure 5.17: Calculated RMS noise current of the OLED for different programming currents.



(a)



(b)

Figure 5.18: Micrographs of the fabricated pixel circuits (a) 3-TFT, (b) 4-TFT.

5.5 Measurement Results

The pixel circuits are fabricated by the same TFT process as that for the fabrication of the pixels with voltage feedback. The parameters of the pixel circuits are listed in Table 5.1. Due to the possible

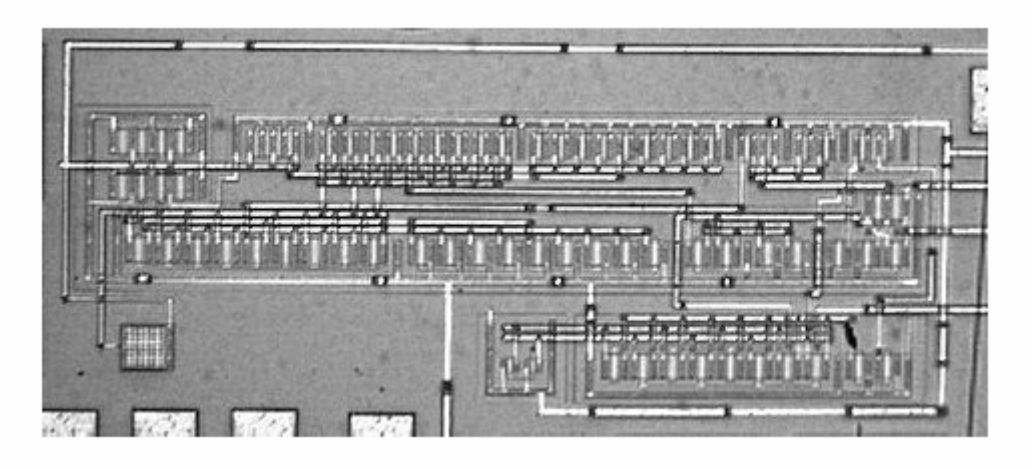


Figure 5.19: Micrograph of a fabricated OTRA in CMOS technology.

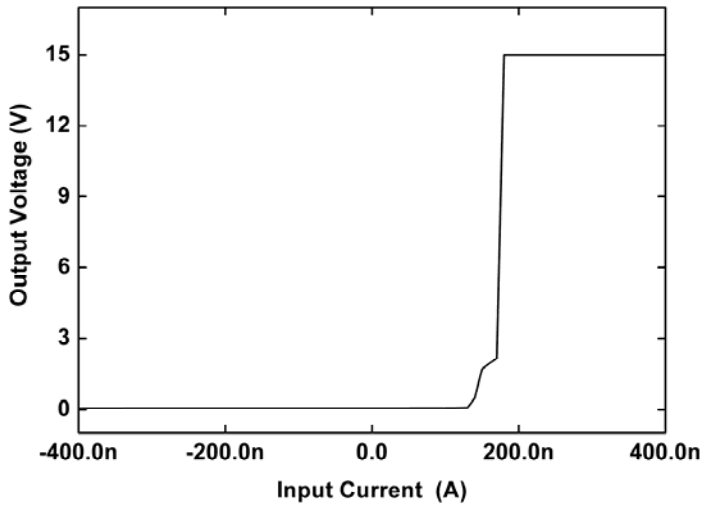


Figure 5.20: Measured DC I/O characteristics of a fabricated OTRA.

yield issues, the sizes of the TFTs and C_S are larger than those in a standard industrial TFT process. Therefore, longer settling times are expected. Fig. 5.18 (a) and (b) show the micrographs of the fabricated 3-TFT and 4-TFT pixel circuits.

The OTRA is fabricated in a 0.8-μm 5/20-V quadruple-well, double-metal, double-poly CMOS technology [94]. A micrograph of the chip is shown in Fig. 5.19. The die area is 700 μm by 240 μm, and the power consumption is less than 17.5 mW for a 17-V supply voltage. Fig. 5.20 shows a sample of the measured DC I/O characteristics of the fabricated OTRA for a supply voltage of 20V.

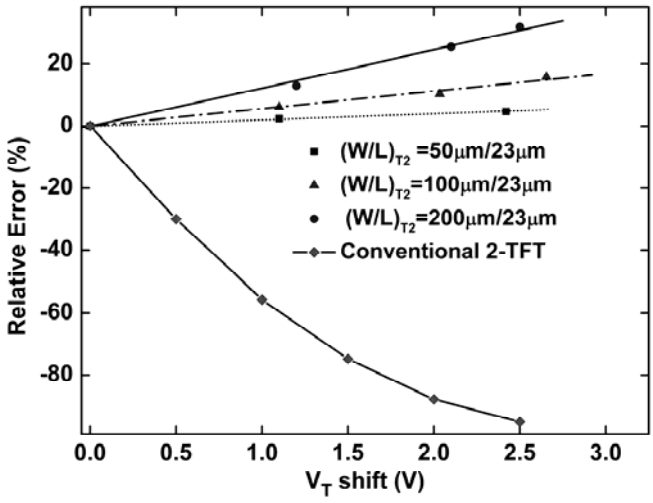


Figure 5.21: Measured relative error in the hold current as a function of V_T shift in T1 for different sizes of T2 for I_{PROG}= 2 μA in comparison with error in an uncompensated 2-TFT pixel circuit.

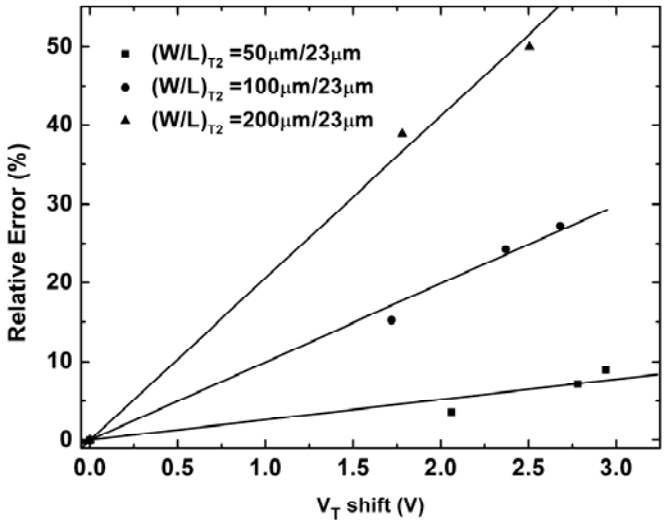


Figure 5.22: Measured relative error in the hold current as a function of V_T shift in T1 for different sizes of T2 for I_{PROG}= 1 μA.

5.5.1 Measurement of the Stability

The change in the hold current as a function of the V_T shift in T1 is measured for the pixel circuits with different sizes of T2. To reduce the measurement time, the V_T shift is accelerated by stressing T1 with a 30-V voltage gate-source voltage. Between the stress cycles, the hold current of the pixel

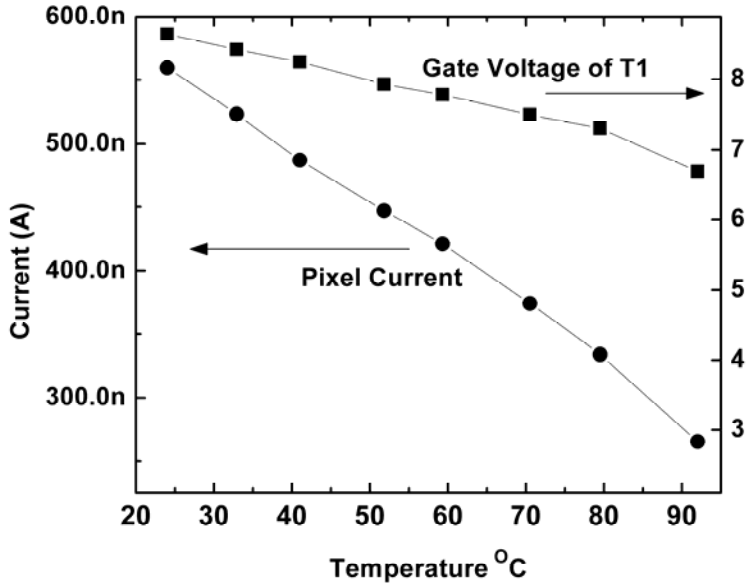


Figure 5.23: Measured hold current as a function of the temperature and the associated change in the gate voltage of T1.

circuits is measured. Fig. 5.21 shows the relative error in the hold current in the 4-TFT pixel circuit as a function of V_T shift for a programming current of 2 μA. For comparison, the error in a conventional 2-TFT pixel with the same T1 size is added. As predicted by (5.4), the hold current slightly increases as V_T shifts, and the rise of the current is higher for the larger sizes of T2. For 2.5 V shift in V_{T1}, the relative changes in the currents are less than 5%, 14%, and 31% for T2 sizes of $(W/L)_{T2}$= 50 μm/23 μm, 100 μm/23 μm, and 200 μm/23 μm, respectively. The degradation in the current of the 2-TFT pixel for the same V_T shift is in excess of -95%.

Fig. 5.22 shows the relative error for a programming current of 1 μA. The errors in the current for the same sizes of T2 are 7%, 23%, and 48%.

5.5.2 Effect of Temperature

The sensitivity of the hold current to the temperature is measured for the 4-TFT pixel circuit. Due to the lack of an OLED, the temperature test for the 3-TFT circuit is not accurate. Fig 5.23 shows the

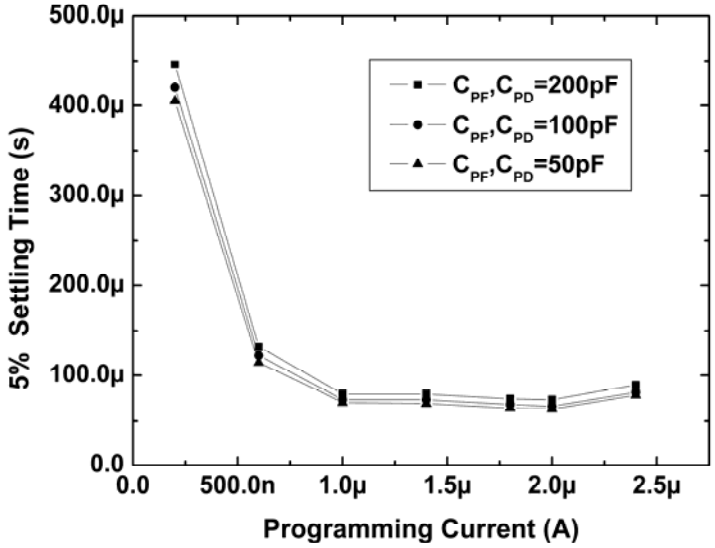


Figure 5.24: Measured settling time in the 4-TFT pixel circuit as a function of the programming current for different line capacitances with no accelerating pulse.

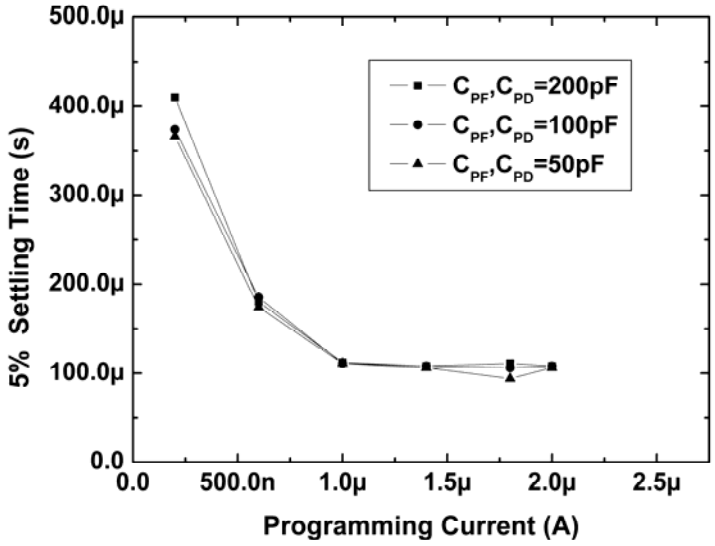


Figure 5.25: Measured settling time in the 3-TFT pixel circuit as a function of the programming current for different line capacitances with no accelerating pulse.

measured relative current as a function of the temperature and the associated change in the gate voltage of T1 for $(W/L)_{T2}$ =100 µm/23 µm. As predicted in Section 5.2.3, the hold current decreases as the temperature increases. The decrease in the gate voltage of T1 with an increase in temperature also

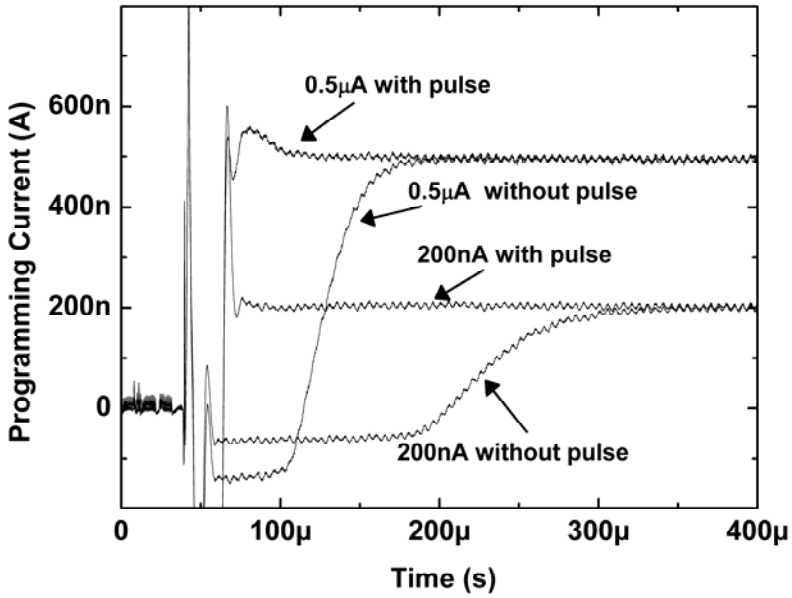


Figure 5.26: Measured transient response of the programming current with and without accelerating pulse.

supports the idea that the change in the hold current is due to the temperature-dependent charge injection of T2.

5.5.3 Settling Time

Fig. 5.24 shows the measured 5-% settling time of the 4-TFT pixel circuit as a function of the programming current for 50 pF, 100pF, and 200 pF parasitic capacitances without the accelerating pulse. The maximum relative difference between the settling times is less than 14%, indicating the reduced effect of the parasitic capacitances on the settling time. The result of the same measurement for the 3-TFT pixel circuit is shown in Fig. 5.25. As can be seen, the Settling time in the 3-TFT pixel circuit is larger than that in the 4-TFT pixel circuit. For both circuits, the variations in the settling time for currents larger than 1 μA is small. In this range, the settling time in the 3-TFT circuit is less than 110 μs and in the 4-TFT circuit is less than 80 μs. Below 1 μA, the settling time rises rapidly in both of the pixel circuits.

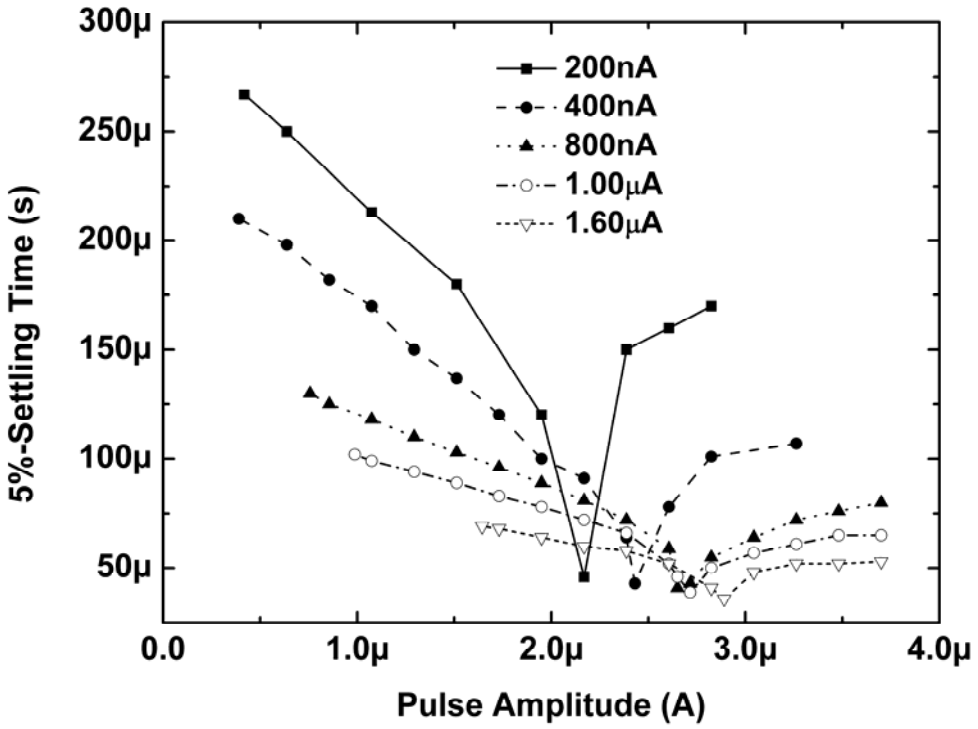


Figure 5.27: Settling time as a function of the accelerating pulse for different programming currents.

Due to the limited swing of the OTRA, it is not possible to test the circuits with programming currents larger than 2 µA. Despite the simulation results, large overshoots in the programming currents are not observed in the 3-TFT pixel circuit. One possible explanation is that the transresistance of the OTRA decreases at high currents due to the limited output swing, limiting the loop gain of the feedback.

The effect of the accelerating pulse on the settling time is investigated for C_{PF} and C_{FD} equal to 100 pF in the 4-TFT pixel circuit. Fig. 5.26 shows the measured programming currents of 0.5 µA and 200 nA with and without applying a 30-µs accelerating pulse to I_{DATA}. By applying the accelerating pulses, the settling times are reduced from 150 µs and 320 µs to 45 µs and 48 µs, respectively.

Fig. 5.27 shows the 5% settling time of the pixel circuit as a function of I_P for different programming currents. t_P is 30 µs, and C_{PF} and C_{PD} are set to 100 pF. For currents as low as 200 nA,

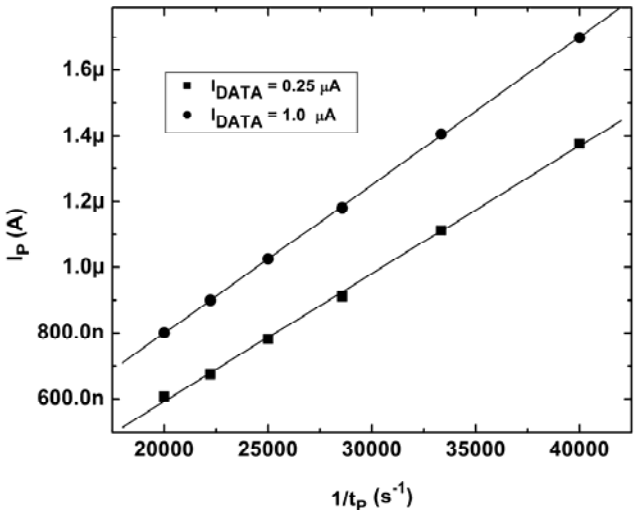


Figure 5.28: Optimum amplitude for the accelerating pulse as a function of $1/t_p$ for different programming currents.

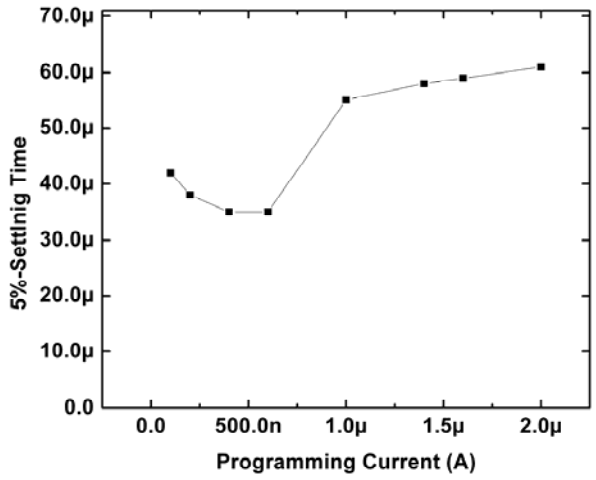


Figure 5.29: Settling time as a function of the programming current when a single-level accelerating pulse is used.

the settling time is less than 50 µs. Fig 5.28 shows the optimum amplitude for I_P as a function of $1/t_p$ for different programming currents. The relationship between I_P and $1/t_p$ is almost linear, as predicted by (5.29).

If the settling requirements are not very high, then instead of using an optimum pulse for each programming current, it is possible to use only one accelerating pulse for the low currents. Fig 5.29

shows the results of this approach. Here, no pulse is applied for currents smaller or equal to 1 μA and a 2-μA pulse for smaller currents. For the entire current range, settling time is smaller than 65 μs.

5.6 Conclusion

Circuit analysis and the measurement results show that the current feedback driving scheme is similar to the voltage feedback scheme in terms of stability and sensitivity to temperature. By employing a transresistance amplifier as the external driver, the negative effect of the parasitic capacitance of the feedback line on the settling time is reduced. As a result, current feedback pixel circuits demonstrate faster settling times. Measurement results show that using an accelerating pulse improves the settling times of small currents by prechaging the gate-source capacitance of the drive TFT.

Chapter 6
Summary and Future Work

Despite shortcomings of the OLED and the TFT, in particular, the instability and low mobility of the latter, amorphous silicon TFT technology remains the primary low-cost solution for driving AMOLED displays. To take advantage of this technology, it is crucial to develop driving schemes to compensate for these shortcomings by exploiting circuit techniques. The solutions must be compatible with both a-Si and OLED technologies, simple to implement in large AMOLED arrays, and capable of providing OLEDs with stable and predictable current. The new driving schemes proposed in this work address such challenges. Here, the sensitivity of the OLED current to spatial and temporal variations in TFT parameters is mitigated significantly by deploying a feedback signal associated with the pixel current to an external column driver circuit through a column feedback line. Depending on the nature of the feedback signal (i.e. current, or voltage), different external drivers are proposed accordingly.

To evaluate the new schemes, different aspects of the AMOLED pixel circuit design with a-Si TFTs are discussed. Also, some important measures of the performance such as stability, programming speed, sensitivity to temperature, and power efficiency are considered. The performance of state-of-the-art AMOLED driving schemes is examined in terms of stability and programming time. Amongst the conventional drive schemes, current programming is investigated in depth. The results confirm that despite the proven stability and low temperature-dependence, the family of the current programmed pixel circuits is prone to slow programming. This is due to the low mobility of a-Si TFTs and the large parasitic capacitance of the data lines. On the other hand, voltage-programmed pixels with on-pixel compensation of the V_T shift, demonstrate much faster programming. However, the inherent tradeoff between the accuracy of the estimating the V_T shift and the programming speed in these pixels results in a limited stability, and thus, shorter lifetimes.

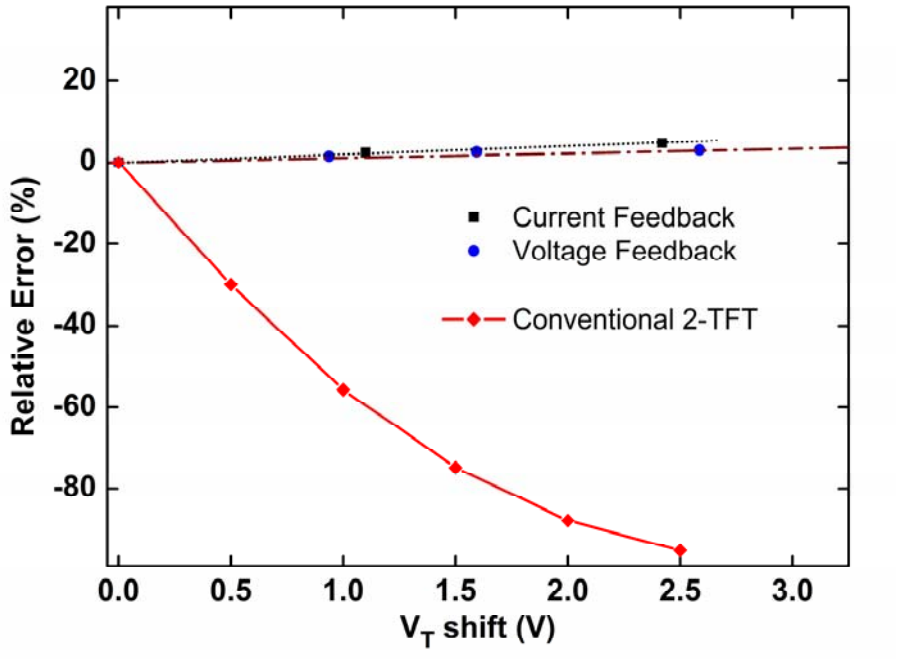


Figure 6.1: Comparison of the stability of a 2-TFT, pixel circuits based on voltage feedback, and current feedback.

6.1 Comparison of the Proposed Schemes

The driving schemes and the associated pixel circuits that are presented in this thesis are analyzed, simulated, fabricated, and successfully tested. Measurement results indicate that both voltage feedback and current feedback driving schemes are highly stable. A comparison of the measured sensitivity of the pixel current to V_T shift contrasted between a conventional 2-TFT, a voltage feedback, and a current feedback pixel circuit with similar drive and switching TFT sizes, is demonstrated in Fig. 6.1. Both the voltage and the current feedback circuits exhibit similar stability performance and are both superior to that of the uncompensated 2-TFT pixel circuit. The V_T-dependent charge injection phenomenon in compensated AMOLED pixel circuits is introduced for the first time and proven to be the principal cause of the slight increase in the pixel current.

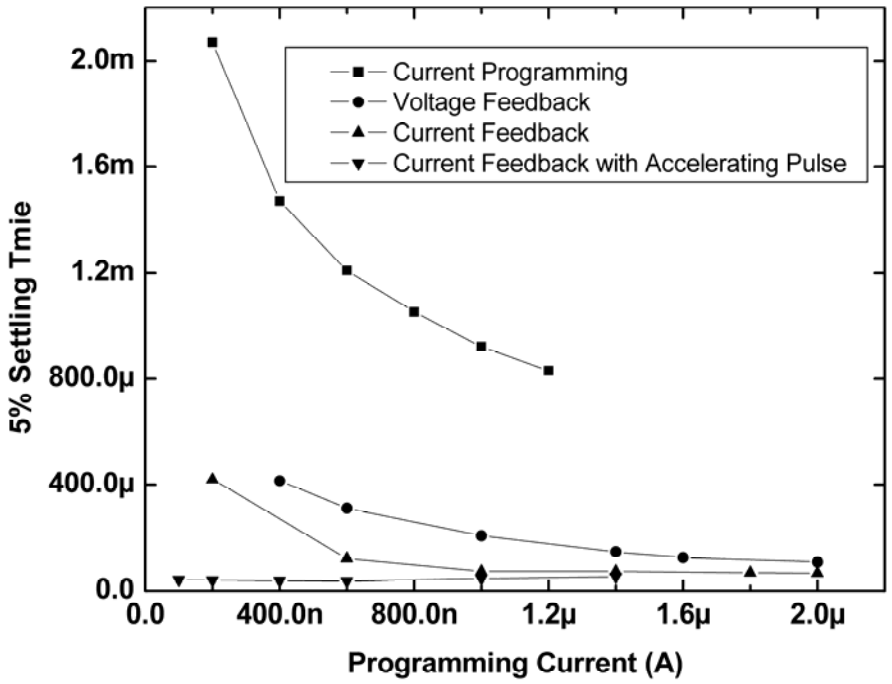


Figure 6.2: Comparison of the settling time of a current-programmed pixel, a voltage feedback pixel, a current feedback pixel, and a current feedback pixel circuit with accelerating pulse.

Both the proposed voltage and current feedback driving schemes indicate faster settling than current programming, but slower settling compared to that of the 2-TFT pixel circuit. Fig. 6.2 compares the measured settling time for a current programmed, a voltage feedback, a current feedback, and a current feedback circuit with accelerating pulse with the same drive and switching TFT sizes and a 100 pF line capacitor. The comparison shows that feedback driving schemes are much faster than current programming. However, the voltage feedback circuit is slower due to the relatively large time constant associated with the parasitic capacitance of the feedback line and the ON resistance of the feedback switch. The current feedback scheme has a faster settling, since the effect of the parasitic capacitance of the feedback line is suppressed thanks to the use of the external OTRA. In addition, measurement results demonstrate that applying an accelerating pulse at the beginning of the programming cycle can effectively reduce the settling time at low programming currents.

Table 6.1: Qualitative comparison of the AMOLED diving schemes.

Driving Scheme	Stability	Settling	Temperature dependence	Power efficiency	Driver Complexity	Uniformity
2-TFT	Low	Very fast	Poor	High	Simple	Medium
Current	High	Slow	Good	Low/High*	Medium	High
Voltage	Medium	Fast	Poor	Low/High*	Medium	Medium
Voltage Feedback	High	Medium	Good	Very High**	Medium	Medium
Current feedback	High	Fast***	Good	Low/High*	Medium/ Complex	High

* pixel circuit configuration dependent

** drive TFT biased in the triode region

*** with accelerating pulse

A qualitative comparison between the different driving schemes is summarized in Table 6.1. In all schemes presented, current feedback and current programming has the highest uniformity, since the pixels are directly programmed with current. On the other hand, voltage feedback has the highest power efficiency, since the drive TFTs can be biased in the triode region, thus lowering the supply voltages of the AMOLED panel.

6.2 Future Work

As demonstrated by this thesis, compensating techniques at the circuit level can compensate for some of the shortcomings of a-Si TFTs, thus facilitating the use of this low-cost technology. However, the limited lifetime of OLED devices, in particular the blue OLED, is still a major barrier, constraining

the rapid growth of AMOLED technology. AMOLED pixel circuits with optical feedback are possible candidates to compensate for the OLED degradation. However, the circuits are complex and potentially undermining the aperture ratio. Moreover, they require extra processing steps to integrate the optical sensors in the pixels. As mentioned in Chapter 2, recent studies demonstrate a correlation between the luminance degradation in an OLED device and its voltage. As a result, the OLED voltage can be employed as an electrical feedback signal to estimate the OLED degradation. Accordingly, a feedback driving scheme should be developed to measure and compensate for both the V_T shift in the drive TFT and the luminance degradation of the OLED.

Appendix A
Implementation of a High-Voltage OTA

A two-stage operational transconductance amplifier (OTA) is implemented and fabricated in a 20-V 0.8-μm CMOS technology. The size of the OTA is 530 μm by 300 μm, thus, can be accommodated without any problem on an external AMOLED driver integrated system. Fig. A.1 shows the schematic of the OTA. To improve the gain, the first stage is cascode. To bias the cascade transistors properly in the saturation region, a source follower stage is employed as a DC level shifter to connect the input stage to the output stage. Table A.1 lists the sizes of the transistors. Fig A.2 shows the microphotograph of the fabricated OTA. The OTA is used as the external column driver for pixel circuits with voltage feedback. Compared to OPA604 Op-amps, no noticeable change in pixel waveforms and performance is observed.

Table A.1: Circuit parameters of the OTA (all sizes in micrometre).

Transistor	Size	Transistor	Size
M1-M4	160/4	M11	120/6
M5-M8	80/6	M12	320/6
M9	160/4	M13	320/4
M10	80/6		

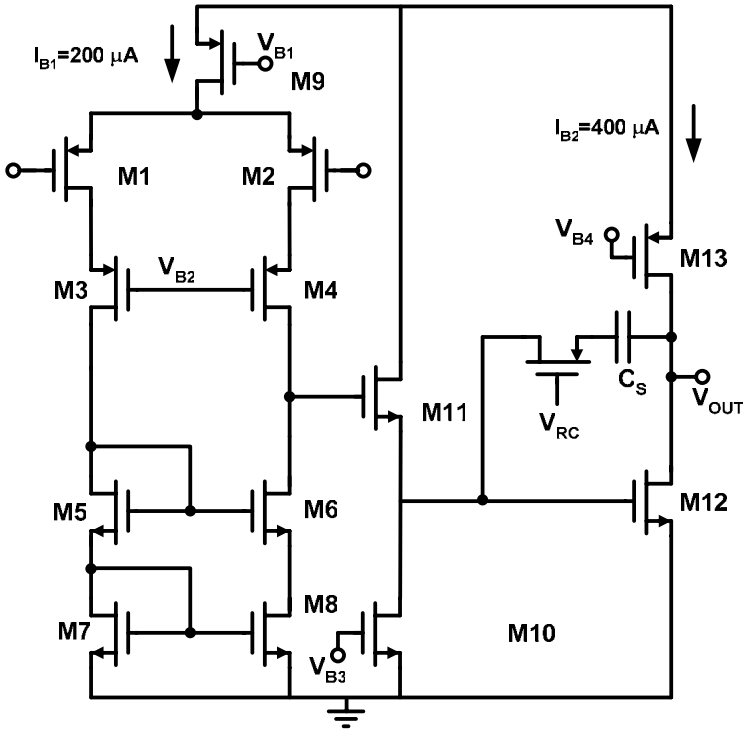


Figure A.1: Schematic of the implemented OTA.

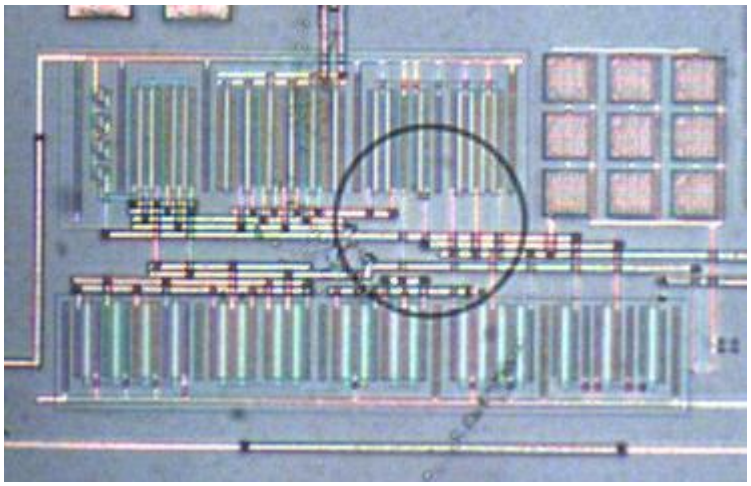


Figure A.2: Micrograph of the fabricated OTA.

Bibliography

[1] G. Gu and S. R. Forrest, "Design of flat-panel displays based on organic light- emitting devices," *IEEE J. Sel. Topics in Quantum Electronics*, vol. 4, no. 1, pp. 83-99, 1998.

[2] J. N. Bardsley, "International OLED technology roadmap," *IEEE J. Sel. Topics in Quantum Electronics*, vol. 10, no. 1, pp. 3-9, 2004.

[3] J. R. Sheats, H. Antoniadis, M. Hueschen, W. Leonard, J. Miller, R. Moon, D. Roitman, and A. Stocking, "Organic electroluminescent devices," *Science*, vol. 273, pp. 884-8, 1996.

[4] A. Sugimoto, H. Ochi, S. Fujimura, A. Yoshida, T. Miyadera and M. Tsuchida, "Flexible OLED displays using plastic substrates," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 10, pp. 107-14, 2004.

[5] C. W. Tang, and S. A. VanSlyke, "Organic electroluminescent diodes," *Appl. Phys. Lett.*, vol. 51, pp. 913-15, 1987.

[6] J. H. Burroughes, D. D. C. Bradley, A. R. Brown, R. N. Marks, K. Mackay, R. H. Friend, P. L. Burns, and A. B. Holmes, "Light-emitting diodes based on conjugated polymers," *Nature*, vol. 347, pp. 539-41, 1990.

[7] OLED Market tracker H1 2006, isupply, http://www.isuppli.com.

[8] Universal Display Company, http://www.universaldisplay.com

[9] P. F. Tian, V. Bulovic, P. E. Burrows, G. Gu, S. R. Forrest, and T. X. Zhou, "Precise, scalable shadow mask patterning of vacuum-deposited organic light emitting devices," *Journal of Vacuum Science & Technology A* (*Vacuum, Surfaces, and Films*), vol. 17, pp. 2975-81, 1999.

[10] J. Bharathan and Y. Yang, "Polymer electroluminescent devices processed by inkjet printing: I. Polymer light-emitting logo," Appl. Phys. Lett., vol. 72, pp. 2660-2, 1998.

[11] D. A. Pardo, G. E. Jabbour, and N. Peyghambarian, “Application of screen printing in the fabrication of organic light-emitting devices,” *Adv Mater*, vol. 12, pp. 1249-52, 2000.

[12] P. E. Burrows, V. Bulovic, S. R. Forrest, L. S. Sapochak, D. M. McCarty and M. E. Thompson, “Reliability and degradation of organic light emitting devices,” *Appl. Phys. Lett*., vol. 65, pp. 2922-2924, 1994.

[13] H. Aziz, Z. D. Popovic, N. X. Hu, A.M. Hor, and G. Xu, “Degradation mechanism of small molecule-based organic light-emitting devices,” *Science*, vol. 283, pp. 1900-1902, 1999.

[14] Novaled Inc. http://www.novaled.com/

[15] R. S. Deshpande, V. Bulovic, and S. R. Forrest, “White-light-emitting organic electroluminescent devices based on interlayer sequential energy transfer,” *Appl. Phys. Lett*., vol. 75, pp. 888-890, 1999.

[16] M. Stwart, R. S. Howell, L. Dires, and K. Hatalis, “Polysilicon TFT technology for active matrix OLED displays,” *IEEE Trans. Electron Devices*, vol. 48, pp. 845-851, 2001.

[17] A. Kumar, A. Nathan, and G. E. Jabbour, “Does TFT mobility impact pixel size in AMOLED backplanes?” *IEEE Trans. Electron Devices*, vol. 52, no. 11, pp 2386-2394, Nov. 2005.

[18] A. Nathan, P. Servati, A. Sazonov, D. Stryahilev, K.S. Karim, *a-Si:H TFTs on glass and plastic in a-Si:H Thin Film Transistors*, Ed: Y. Kuo, Kluwer Academic Publishers, 79-181, 2003.

[19] M. J. Powell, “The Physics of Amorphous-Silicon Thin-Film Transistors,” *IEEE Trans. Electron Devices*, vol. 36, no. 12, pp. 2753-2763, Dec. 1989.

[20] S. M. GadelRab and S. G. Chamberlain, "Thick-layered etched-contact amorphous silicon transistors," IEEE Trans. Electron Devices, vol. 45, pp. 465-471, 1998.

[21] S. GadelRab, A. Miri and S. Chamberlain, "A comparison of the performance and reliability of wet-etched and dry-etched a-Si: H TFTs," *Electron Devices, IEEE Transactions on,* vol. 45, pp. 560-563, 1998.

[22] A. M. Miri and S. G. Chamberlain, "A totally wet etch fabrication technology for amorphous silicon thin film transistors," in *Amorphous Silicon Technology - 1995. Symposium,* , pp. 737-742, 1995.

[23] A. Nathan, P. Servati, A. Sazonov, D. Stryahilev, and K.S. Karim, *a-Si:H TFTs on glass and plastic in a-Si:H Thin Film Transistors,* Ed: Y. Kuo, Kluwer Academic Publishers (2003) 79-181.

[24] R. A. Street, *Hydrogenated Amorphous Silicon*, London, Cambridge University Press, 1991.

[25] P. Servati and A. Nathan, “Modeling of the reverse characteristics of a-Si:H TFTs,” *IEEE Trans. Electron Devices*, vol. 49, no. 5, pp. 812-819, 2002.

[26] M. Hack, M. S. Shur, and J. G. Shaw, “Physical models for amorphous silicon thin-film transistors and their implementation in a circuit simulation program,” *IEEE Trans. Electron Devices*, vol. 36, no. 12, pp. 2764-2769, 1989.

[27] M. S. Shur, H. C. Slade, M. D. Jacunski, A. A. Owusu, and T. Ytterdal, “SPICE models for amorphous silicon and polysilicon thin film transistors,” *J. Electrochem.Soc.*, vol. 144, no. 8, pp. 2833-2839, 1997.

[28] K. Khakzar and E. H. Lueder, “Modeling of amorphous-silicon thin film transistors for circuit simulations with SPICE,” *IEEE Trans. Electron Devices*, vol. 39, no. 6, pp. 1428-1434, 1992.

[29] T. Leroux, “Static and dynamic analysis of amorphous-silicon field-effect transistors,” *Solid-State Electron.*, vol. 29, no. 1, pp. 47-58, 1986.

[30] P. Servati, D. Striakhilev, and A. Nathan, “Above-threshold parameter extraction and modeling for amorphous silicon thin-film transistors,” *IEEE Trans. Electron Devices*, vol. 50, no. 11, pp. 2227-2235, 2003.

[31] M. Shur, M. Hack, and J. G. Shaw, “A new analytical model for amorphous silicon thin-film transistors,” *J. Appl. Phys*., vol. 66, no.7, pp. 3371-3380, 1989.

[32] N. Mohan, K. S. Karim, and A. Nathan, “Design of Multiplexer in Amorphous Silicon Technology,” *Journal of Vacuum Science and Technology* A, vol. 20, no. 3, pp. 1043-1047, 2002.

[33] C. van Berkel, and M. J. Powell, “Resolution of amorphous silicon thin-film transistor instability mechanisms using ambipolar transistors,” *App. Phys. Lett*., vol. 51, no. 14, pp. 1094-1096, 1987.

[34] A. Akavan Fooman, *Threshold Voltage Instability and Relaxation in Hydrogenated Amorphous Silicon Thin Film Transistors*, Master thesis, University of Waterloo, 2005.

[35] W. B. Jackson, M. Marshall, and M. D. Moyer, “Role of hydrogen in the formation of metastable defects in hydrogenated amorphous silicon,” *Phys. Rev. B*, vol. 39, no. 2, pp. 1164-1179, 1989.

[36] Ya-Hsiang Tai, Jun-Wei Tsai, Huang-Chung Cheng and Feng-Cheng Su, "Instability mechanisms for the hydrogenated amorphous silicon thin-film transistors with negative and positive bias stresses on the gate electrodes," *Appl. Phys. Lett.*, vol. 67, pp. 76-78, 1995.

[37] M. J. Powell, C. van Berkel, and J. R. Hughes, “Time and temperature dependence of instability mechanisms in amorphous silicon thin-film transistors,” *App. Phys. Lett*., vol. 54, no. 14, pp. 1323-1325, April 1989.

[38] F. R. Libsch and J. Kanicki, “Bias-stress-induced stretch-exponential time dependence of charge injection and trapping in amorphous silicon thin-flm transistors,” *Appl. Phys. Lett.*, vol. 62, no. 11, pp. 1286-1288, 1993.

[39] C.-S. Chiang, J. Kanicki, and K. Takechi, “Electrical instability of hydrogenated amorphous silicon thin-film transistors for active-matrix liquid-crystal displays,” *Jpn. J.Appl. Phys.*, Part 1, vol. 37, no.11, pp. 4704-4710, 1998.

[40] S. Sambandan and A. Nathan, "Equivalent circuit description of threshold voltage shift in a-Si:H TFTs from a probabilistic analysis of carrier population dynamics," *IEEE Trans. Electron Devices*, vol. 53, pp. 2306-11, 2006.

[41] M. J. Powell, C. van Berkel, I. D. French and D. H. Nicholls, "Bias dependence of instability mechanisms in amorphous silicon thin-film transistors," *Appl. Phys. Lett.*, vol. 51, pp. 1242-4, 10/19. 1987.

[42] W. Lee, G. W. Neudeck, J. Choi, and S. Luan, “ A model for the temperature-dependent saturated I_D-V_D characteristics of an a-Si:H thin-film transistor,” *IEEE Trans. Electron Devices*, vol. 38, no. 9, pp. 2070-2074, 1991.

[43] A. Nathan, A. Kumar, K. Sakariya, P. Servati, S. Sambandan, and D. Striakhilev, “Amorphous silicon thin film transistor circuit integration for organic LED displays on glass and plastic,” *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 215-222, 2003.

[44] J. B. Boudry, and I. E, Antonuk, “Current-noise-power spectra of amorphous silicon thin-film transistors,” *J. Appl. Phys.*, vol.74, no.4, pp. 2529-2534, 1994.

[45] M, Valenza, C. Barros, M. Dumas, D. Riguad, T. Ducourant, N. Szydlo, and H. Lebrun, “Conduction and 1/f noise analysis in amorphous silicon thin-film transistors,” *J. Appl. Phys.*, vol. 79, no. 2, pp. 923-928, 1996.

[46] J. Rhayem, D. Riguad,, M. Valenza, N. Szydlo, and H. Lebrun, “1/f noise modeling in long channel amorphous silicon thin film transistors,” *J. Appl. Phys*., vol.87, no.4, pp. 1983-1989, 2000.

[47] J. Rhayem, D. Riguad,, M. Valenza, N. Szydlo, and H. Lebrun, “1/f noise modeling in small channel amorphous silicon thin film transistors,” *J. Appl. Phys*., vol. 83, no. 7, pp. 3660-3667, 1998.

[48] B. Geffroy, P. Le Roy, and C. Prat, “Organic light-emitting diode (OLED) technology: materials, devices, and display technologies,” *Polymer International*, vol. 55, pp. 572-582, 2006.

[49] A. J. Campbell, D. D. C. Bradley, and D.G. Lidzey, “Space-charge limited conduction with traps in poly(phenylene vinylene) light emitting diodes,” *J. Appl. Phys*., vol. 82, no. 12, pp. 6326-6342, 1997.

[50] P. E. Burrows, Z. Shen, V. Bulovic, D. M. McCarty, S. R Forrest, J. A. Corbin, and M. E. Thompson, “Relationship between electroluminescence and current transport in organic heterojunction light-emitting devices,” *J. Appl. Phys*., vol. 79, no. 10, pp. 7991-8006, 1996.

[51] R. M. A Dawson et-al, “The impact of the transient response of organic light emitting diodes on the design of active matrix OLED displays,” in *IEDM Tech. Dig.*, pp. 875-878, 1998.

[52] R.C. Kwong *et al*., “High operational stability of electrophosphorescent devices,” *Appl. Phys. Lett*., vol. 81, no. 1, pp. 162-164, July 2002.

[53] V. Bulovic, P. Tian, P. E. Burrows, M. R. Gokhale, S. R. Forrest and M. E. Thompson, “A surface-emitting vacuum-deposited organic light emitting device,” *Appl. Phys. Lett.*, vol. 70, pp. 2954-6, 1997.

[54] T. Chu, J. Chen, S. Chen, C .J. Chen, C. H. Chen,"Highly efficient and stable inverted bottom-emission organic light emitting devices," *Appl. Phys. Lett*., vol. 89, no. 23, pp. 2922-2924, 1994.

[55] A. Nathan, G.R. Chaji, and S.J. Ashtiani, "Driving schemes for a-Si and LTPS AMOLED displays," *IEEE J. of Display Technology*, vol. 1, no.2, pp. 267-277, Dec. 2005.

[56] Y. He, R. Hattori, and J. Kanicki, "Current-source a-Si:H thin-film transistor circuit for active-matrix organic light-emitting displays," *IEEE Electron Device Lett.*, vol. 21, pp.590-592, Nov. 2000.

[57] Y. He, R. Hattori, and J. Kanicki, "Improved a-Si:H TFT circuits for active-matrix organic light emitting displays," *IEEE Trans. Electron Devices*, vol. 48, no.7 pp. 1322-1325, July 2001.

[58] R. Hattori, T. Tsukamizu, R. Tsuchiya, K. Miyake, Yi He, and J. Kanicki, "Current-writing active-matrix circuit for organic light emitting diode display using a-Si:H thin-film-transistors," *IEICE Trans. Electron*., vol. E83-C, pp. 779-782, 2000.

[59] S. J. Ashtiani, P. Servati, D. Striakhilev, and A. Nathan, "A 3-TFT current-programmed pixel circuit for active-matrix organic light-emitting diode displays," *IEEE Trans. Electron Devices*, vol. 52, no. 7, pp. 1514-1518, 2005.

[60] W. F. Aerts, S. Verlaak and P. Heremans, "Design of an organic pixel addressing circuit for an active-matrix OLED display," IEEE Trans. Electron Devices, vol. 49, pp. 2124-30, 2002.

[61] Y. Lin and H-P. D. Shieh, "A novel current memory circuit for AMOLEDs," *IEEE Trans. Electron Devices*, vol. 51, no. 6, pp. 1037-1040, 2004.

[62] M. Ohta, H. Tsutsu, H. Takahara, I. Kobayashi, T. Uemura, and Y. Takubo, "A novel current programmed pixel for active matrix OLED displays," *Dig. of Tech. Papers, SID Int. Symp.*, San Jose, pp. 108-111, 2003.

[63] T. Sasaoka, M. Sekiya, A. Yumoto, J. Yamada, T. Hirano, Y. Iwase, T. Yamada, T. Ishibashi, T. Mori, M. Asano, S. Tamura, and T. Urabe, "A 13-inch AM-OLED display with top emitting structure and adaptive current mode programmed pixel circuit (TAC)," in *Dig. of Tech. Papers, SID Int. Symp.*, pp. 384-386, 2001.

[64] K. Sakariya, P. Servati, and A. Nathan, "Stability analysis of current programmed a-Si:H AMOLED pixel circuits," *IEEE J. of Solid-State Circuits*, vol. 51, no. 12, pp. 1477-1486, 2004.

[65] J. Lee, W. Nam, S. Jung, and M. Han, "A new current-scaling pixel circuit for AMOLED," *IEEE Electron Device. Letts.*, vol. 25, no. 5, pp. 280-282, 2003.

[66] Yen-Chung Lin, H. -. D. Shieh and J. Kanicki, "A novel current-scaling a-Si:H TFTs pixel electrode circuit for AM-OLEDs," IEEE Trans. Electron Devices, vol. 52, pp. 1123-31, 2005.

[67] S. Ono and Y. Kobayashi, "An accelerative current-programming method for AM-OLED," *IEICE Trans. Electronics*, vol. E88-C, pp. 264-269, Feb. 2005.

[68] P. Servati and A. Nathan, "Functional pixel circuits for elastic AMOLED displays," *Proc. IEEE*, vol. 93, pp. 1257-64, 2005.

[69] K. S. Karim, A. Nathan, M. Hack, and W. I. Milne, "Drain-bias dependence of threshold voltage stability of amorphous silicon TFTs," *IEEE Electron Device Letts.*, vol. 25, pp. 188–190, 2004.

[70] G. Wegmann, E. A. Vittoz, and F. Rahali, "Charge injection in analog MOS switches," *IEEE J. of Solid-State Circuits*, vol. SC-22, no. 6, pp. 1091-1097, 1987.

[71] G.R. Chaji, S. Ashtiani, S. Alexander, R. Huang, D. Striakhilev, P. Servati, K. Sakariya, A. Kumar, and A. Nathan, "Pixel circuits and drive schemes for large-area a-Si AMOLED, " in *IDMC 2005*, Taiwan, 2005.

[72] J. Goh, H-J. Chung, and J. Jang, “A new pixel circuit for active matrix organic light emitting diodes,” *IEEE Electron Device. Lett.*, vol. 23, no. 9, pp. 544-546, 2002.

[73] J. Goh, J. Jang, K. Cho, and C. Kim “A new a-Si:H thin-film transistor pixel circuits for active matrix organic light-emitting diodes,” *IEEE Electron Device. Lett.*, vol. 24, no. 9, pp. 583-585, 2003.

[74] S. H. Jung, W. J. Nam, and M. K Han, “A new voltage-modulated AMOLED pixel design compensating for threshold voltage variation in poly-si TFTs,” *IEEE Electron Device Letts.*, vol. 25, pp. 690-692, 2004.

[75] J. L. Sanford and F. R. Libsch, “TFT AMOLED pixel circuits and driving methods,” *Dig. of Tech. Papers, SID Int. Symp.*, Baltimore, pp. 10-13, 2003.

[76] S. W. Tam, Y. Matsueda, M. Kimura, H. Maeda, T. Shimoda, and P. Migliorato, “Poly-Si driving circuits for organic EL displays,” in *Proc. of SPIE*, vol. 4295, pp. 125-133, 2001.

[77] G. Chaji, P. Servati, and A. Nathan, “Driving scheme for stable operation of 2-TFT a-Si AMOLED pixel,” Electron. Lett., vol. 41, pp. 499-500, 2005.

[78] A. Giraldo *et al*., “Optical feedback in active matrix polymer OLED displays,” *LEOS* 2003, vol. 2, pp. 529-530, Oct. 2003.

[79] D. Fish, M. Childs, S. Deane, J. Shannon, W. Steer, N. Young, A. Giraldo, H. Lifka and W. Oepts, “Improved optical feedback for OLED differential ageing correction,” *Journal of the Society for Information Display*, vol. 13, pp. 131-132, 2005.

[80] A. Nichols, T. N. Jackson, M. H. Lu, and M. Hack, “Bi-stable a-si:H TFT phosphorescent OLED active matrix pixel,” *61st Device Research Conference*, 23-25 June 2003, pp. 189-90, 2003.

[81] D. L. Staebler and C. R. Wronski, “Optically induced conductivity changes in discharge-produced hydrogenated amorphous silicon,” J. Appl. Phys., vol. 51, pp. 3262-8, 1980.

[82] S. J. Ashtiani, G. R. Chaji, and A. Nathan, "AMOLED pixel circuit with OLED luminance degradation compensation," *IEEE J. of Display Technology*, vol. 3, no. 1, pp. 36-39, 2007.

[83] H. Akimoto, H. Kageyama, M. Miyamoto, Y. Shimizu, N. Kasai, H. Awakura, A. Shingai, N. Tokuda, K. Kajiyama, and S. Nishitani, "Clamped-inverter circuit architecture for luminescent-period-control driving of active-matrix OLED displays," *Journal of the Society for Information Display*, vol. 13, pp. 429-432, 2005.

[84] Jong-Wook Seo, Hanbyul Kim, Bongok Kim and Youngkwan Kim, "A charge-pump active-matrix pixel driving method for organic light-emitting diode display applications," *Japanese Journal of Applied Physics*, Part 1, vol. 41, pp. 7391-7395, 2002.

[85] A. Sedra, and K. Smith, *Microelectronic Circuits*, Fifth edition, Oxford University Press, 2004.

[86] S. J. Ashtiani and A. Nathan, "A driving scheme for active-matrix organic light-emitting diode displays based on feedback," *IEEE/OSA Journal of Display Technology*, vol. 2, pp. 258-264, 2006.

[87] S. Jafarabadiashtiani et al, "A new driving method for a-Si AMOLED displays based on voltage feedback," *Dig. of Tech. Papers, SID Int. Symp.*, Boston, pp. 316-317, May 25-27, 2005.

[88] S.J Ashtiani and A. Nathan, "A driving scheme for AMOLED display based on current feedback," Proceeding of *IEEE Custom Integrated Circuits Conference* (CICC) 2006, pp.289-292, Sept. 2006.

[89] S. Jafarabadi ashtiani, P. Servati, and A. Nathan, "A high-speed driver for current-programmed-active-matrix OLED displays**,"** *The 3rd International IEEE-NEWCAS Con.*, pp. 400-403, 19-22 Jun, 2005.

[90] S. J. Ashtiani and A. Nathan, “A fast driving scheme for a-Si:H AMOLED displays based on voltage feedback,” in *Proc. Annu. Meeting LEOS* 2005, pp. 925-926, October 2005.

[91] H. Elwan, A. M. Soliman, and M. Ismail, “A CMOS norton amplifier-based digitally controlled VGA for low-power wireless applications,” *IEEE J. Solid-State Circuits*, vol. 48, no. 3, pp. 245-254, Sept. 2004.

[92] A.S. Sedra, G.W. Roberts, and F. Gohh, “The current conveyor: history, progress and new results,” *IEE Proc. G., Electron. Circuits Syst.*, vol. 137, (2), pp. 78-87, 1990.

[93] M. Pelgrom, A. Duinmaijer, and A. Welbers, “Matching properties of MOS transistors,” *IEEE J Solid State Circuits,* vol. 24, no. 5, pp. 1433-1439, 1989.

[94] Dalas Semiconductor, http://www.dalsasemi.com.

[95] G. Palmisano and G. Palumbo, “High performance CMOS current comparator design,” *IEEE Transactions on Circuits and Sysytems-II: Analog and Digital Signal Processing,* vol. 43, no. 12, 1996.