Threshold Voltage Instability and Relaxation in Hydrogenated Amorphous Silicon Thin Film Transistors

by

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AUTHOR'S DECLARATION FOR ELECTRONIC SUBMISSION OF A THESIS

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Abstract

This thesis presents a study of the bias-induced threshold voltage metastability phenomenon of the hydrogenated amorphous silicon (a-Si:H) thin film transistors (TFTs). An application of gate bias stress shifts the threshold voltage of a TFT. After the bias stress is removed, the threshold voltage eventually returns to its original value. The underlying physical mechanisms for the shift in threshold voltage during the application of the bias and after the removal of the bias stress are investigated.

The creation of extra defect states in the band gap of a-Si:H close to the gate dielectric interface, and the charge trapping in the silicon nitride (SiN) gate dielectric are the most commonly considered instability mechanisms of threshold voltage. In the first part of this work, the defect state creation mechanism is reviewed and the kinetics of the charge trapping in the SiN is modelled assuming a simplified mono-energetic and a more realistic Gaussian distribution of the SiN traps. The charge trapping in the mono-energetic SiN traps was approximated by a logarithmic function of time. However, the charge trapping with a Gaussian distribution of SiN traps results in a more complex behavior.

The change in the threshold voltage of a TFT after the gate bias has been removed is referred to threshold voltage relaxation, and it is investigated in the second part of this work. A study of the threshold voltage relaxation sheds more light on the metastability mechanisms of a-Si:H TFTs. Possible mechanisms considered for the relaxation of threshold voltage are the annealing of the extra defect states and the charge de-trapping from the SiN gate dielectric. The kinetics of the charge de-trapping from a mono-energetic and a Gaussian distribution of the SiN traps are analytically modelled. It is shown that the defect state annealing mechanisms cannot explain the observed threshold voltage relaxation, but a study of the kinetics of charge de-trapping helps to bring about a very good agreement with the experimentally obtained results. Using the experimentally measured threshold voltage relaxation results, a Gaussian distribution of gap states is extracted for the SiN. This explains the threshold voltage relaxation of TFT after the bias stress with voltages as high as 50V is removed.

Finally, the results obtained from the threshold voltage relaxation make it possible to calculate the total charge trapped in the SiN and to quantitatively distinguish between the charge trapping mechanism and the defect state creation mechanisms. In conclusion, for the TFTs used in this thesis, the charge trapping in the SiN gate dielectric is shown to be the dominant threshold voltage metastability mechanism caused in short bias stress times.

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And last, but most importantly, I dedicate this thesis to the love of my life, Maryam, who has stood behind me during this time. She has helped me even with my research and tried so hard to ease the pressure of the work. I would never be able to compensate all the things she did for me.

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Chapter 1

Introduction

Good electronic properties of hydrogenated amorphous silicon (a-Si:H) such as the fairly high carrier mobility (≈1 cm^2/Vs) and a high photoconductivity [1-3], and the ability to achieve low cost deposition of the a-Si:H films at low temperatures over large surfaces were strong motivating factors for the employment of this material in large area electronics. Typical applications of a-Si:H include displays, digital scanners, fax machines, video cameras, medical x-ray imagers, and solar cells. In most of these applications, a-Si:H thin film transistors (TFTs) [4] function either as simple switching elements in, for example, passive matrix imagers or, as active elements in electronic devices such as active matrix organic light emitting diode (AMOLED) displays and active matrix flat panel imagers (AMFPIs). For most of these applications, a high resolution, long lifetime, low power consumption and acceptable performance in adverse conditions are crucial. At present,

research is focussed on a-Si:H material and devices to improve the quality and reliability of these electronics systems.

Although a-Si:H TFTs are economical, these devices have the disadvantages of metastable changes of threshold voltage after a prolonged application of gate bias stress called threshold voltage shift. It adversely affects the operation of a-Si:H TFT circuits, most importantly, when the TFT is an active element in such as AMOLED displays. For example, the output current of OLEDs, and as a result, the pixel brightness decreases over time, since the threshold voltage of the driving TFT increases [5]. This is further explained in Chapter 2. Although the threshold voltage shift mechanisms have been extensively studied to predict the long-term behaviour of a-Si:H TFT circuits, the present available models in the literature do not completely account for the experimental results. Due to ever-growing application of the TFTs in large area electronics, more accurate model for threshold voltage shift of the a-Si:H TFTs is needed. In this thesis, I review and discuss the different mechanisms of threshold voltage shift. Furthermore, the change in the threshold voltage of the TFTs after removing bias stress, called relaxation, is investigated. This provides another means to study the mechanisms that are responsible for the threshold voltage shift in a-Si:H TFTs.

1.1 A Brief Historical Account of Hydrogenated Amorphous Silicon

Un-hydrogenated a-Si, which is prepared by thermal evaporation or the sputtering of Silicon (Si), has a very high defect density. This high defect density prevents realizing of many desirable electrical properties such as doping and photoconductivity. The electronic transport in un-hydrogenated a-Si is almost done through defect states.

In 1969, Chittick, Alexander, and Sterling reported the deposition of a-Si:H material using a plasma dissociation of Silane (SiH_4) gas [1]. After three decades, the a-Si:H is still deposited using SiH_4 plasma, although the design of deposition systems has changed. In the first reactor, plasma was excited by a radio-frequency coil placed outside the quartz chamber (inductive reactors). At present, most reactors are capacitive due to their structures which are simpler than those of their inductive counterparts. Typically, capacitive reactors consist of two parallel electrodes within a stainless steel chamber. The deposition mechanism is the

same for both kinds of reactors. The deposited material exhibited an increased conduction due to impurities and a low defect density. Further research has demonstrated that the a-Si:H exhibits good electrical transport properties and strong photoconductivity [2][3]. A few years later, in 1974, Lewis et al. succeeded in dramatically reducing the defects in sputtered amorphous silicon (a-Si) by introducing hydrogen (H) gas into the deposition system. The material has similar properties to those of glow discharge a-Si:H, and contains about 10 atomic percents of H. In 1975, the substitutional n-type or p-type doping of a-Si:H was reported by Spear and LeComber. The doping was done simply by the addition of diborane (B_2H_6) or phosphine (PH_3) to the deposition gas. Since then, although the glow discharge and the sputtered a-Si:H have been studied, the glow discharge material has been favoured over the sputtered material because of the slightly better quality achieved.

The early research on a-Si:H devices was initiated at RCA laboratories by Carlson and Wronski (1976). They realized a-Si:H solar cells with conversion efficiencies of 2-3%. In that year, a-Si:H p-n junctions were also realized by Spear et al. [6]. Finally, LeComber et al., in 1979, were the first to report a a-Si:H thin film transistor (TFT) [4]. The application of the a-Si:H TFT in large area electronics was demonstrated two years later by Snell et al. in 1981 [7]. Since then, a-Si:H TFTs have been employed in many applications, most attractive being active matrix displays and active matrix flat panel imagers (AMFPIs).

1.2 Density of States in a-Si:H

A band gap, separating the occupied valance band from the empty conduction band, is one of the fundamental properties of semiconductors. Although the band gap is a consequence of the periodicity of the lattice, it is also equivalently described by splitting of the bonding and anti-bonding states. Based on the second theory, the bands are mostly influenced by the short-range order, which is similar in both a-Si and crystalline Silicon (c-Si). However, the presence of disorder in a-Si affects the electronic state of the material in the following ways [8]: 1) The density of states (DOS) distribution is broadened forming the band tails; 2) The band tail states are localized; that is, at zero temperature, electrons occupy the tail state below the mobility edge are not fully mobile and do not contribute to the conduction; 3) The

scattering length is reduced to atomic distances; 4) The conservation of the momentum in the electronic transitions is lost. The last phenomenon necessitates that the energy-momentum band structure of c-Si should be replaced by the energy dependent DOS distribution, $N(E)$. $N(E)$ is divided into three parts: conduction and valence bands, band tail regions close to the band edges, and defect states in the forbidden gap as seen in Fig. 1.1 [8].

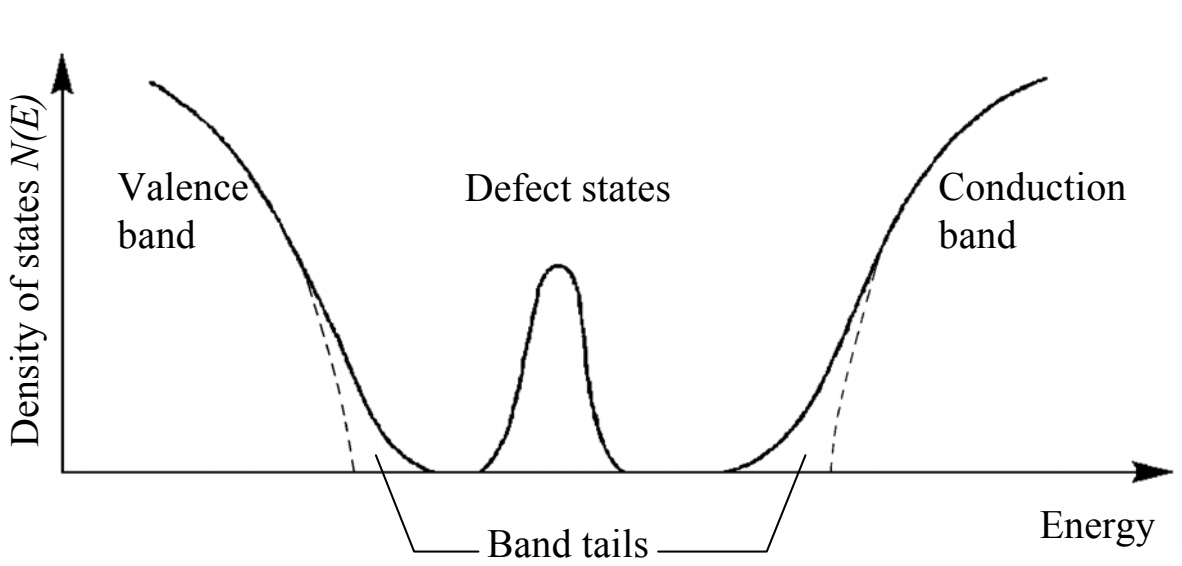

Fig. 1.1 Schematic density of states (DOS) for a-Si (solid line) and crystalline silicon (dashed lines) showing conduction and valence bands, band tails, and defect states [8].

The valence and conduction bands are formed by splitting of the sp^3 hybrid orbitals of tetrahedral silicon bonding. Therefore, the valence and conduction bands are largely influenced by the short-range order of the Si atoms rather than the periodicity of the structure. This implies that, although the detailed features of the conduction band and valence band are different for a-Si:H and c-Si, they possess the same overall shape. In addition, the existence of Si-H bonds adds more features to the DOS.

The essential difference between the crystal phase and the amorphous phase of semiconductors is observed at their band edges. In contrast to c-Si which possesses sharp band edges, a-Si:H has a tail of localized states extending into the gap. The term, localized, indicates that electrons in these states are essentially immobile and do not contribute to the conduction [9]. The localized tail states are separated from the extended bands states (valence or conduction bands) by the mobility edge as depicted in Fig. 1.2.

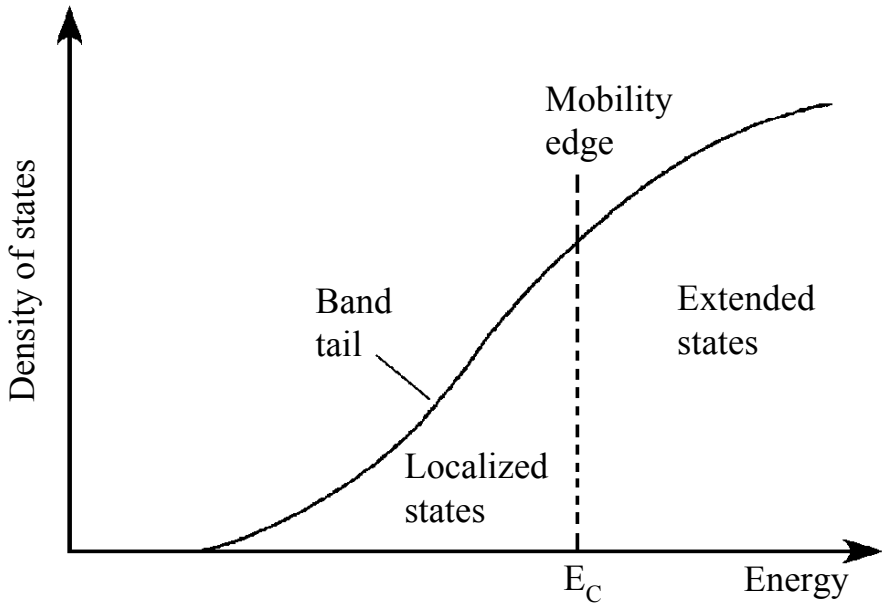

Fig. 1.2 Density of states (DOS) distribution near the conduction band edge of a-Si:H, showing the localized states and extended states separated by the mobility edge [8].

Information about the *N(E)* in the valence band tail can be derived from the photoemission experiments [10]. The experimental data demonstrates that *N(E)* in the valence band tail has an approximate linear energy dependence from 0.5 eV above the band edge down to the densities of 3×10^{21} $cm^{-3}eV^{-1}$ at the band edge. Near and below the band edge, the tail takes an exponential form over several orders of magnitude of the *N(E)*. The minimum of *N(E)* depends on the quality and the deposition conditions of a-Si:H and is not more than 10^{15} - 10^{16} $cm^{-3}eV^{-1}$ for a good quality a-Si:H. The characteristic energy of the valence exponential tail kT_V is approximately 45 meV and is often described by the characteristic temperature T_V (T_C for the conduction band tail) by

$$N(E) = N_0 \exp(-E / kT_V) . \tag{1.1}$$

The DOS in the conduction tail states is obtained from the rate of the thermal excitation of the trapped carriers during electronic transport. Since the conduction of the electrons and holes occurs by frequent trapping in the tail states, followed by excitation to the higher energy states, the effective or drift mobility is lower than the free mobility in the conducting states. Therefore, the measurement of the drift mobility provides an accurate way to find the DOS in the band tails. The drift mobility is measured by using the time-of-flight experiment

[11]. The time-of-flight data, with the assumption that there is an exponential density of tail states for the electrons and holes, yields a characteristic temperature T_C of 250-300K for the electrons and T_V of 400-450K for the holes [12]. The mobility gap of a-Si:H, which is defined as the difference between the conduction (E_C) and valence (E_V) band edge energies, is also estimated to be 1.85-1.9 eV by the time-of-flight and photoemission data.

The defects significantly influence the performance of a-Si:H devices. They reduce the photosensitivity, suppress the doping efficiency and degrade the performance of a device. Those defects whose their electronic states are placed within the band gap are more important, since they act as recombination and trap centers. Material defects are defined as the departure from the ideal amorphous network which is a continuous random network with the bonds satisfied [8]. This leads to the definition of coordination defects such as Si dangling bonds, four-fold donor states, or acceptor states. Typically, coordination defects create states in the forbidden energy gap of a semiconductor. Structural information about the defects and the DOS come from electron spin resonance (ESR) [13] and deep level transient spectroscopy (DLTS) [14][15] experiments. These experiments give information about *N(E)* for upper half of the band gap and there is no experiment to give a detailed DOS for the lower half of the band gap. The overall shape of the defect band is assumed to be Gaussian for theoretical simulation and is confirmed by the photocapacitance data [16].

1.3 Electronic Properties of a-Si:H

a-Si is not a completely disordered material. Study of the atom pair distribution function demonstrates that amorphous materials possess the same short-range order as crystals but lack the long-range order [8]. Si atoms in a-Si:H have the same average bond length and bond angles with the same number of neighbours as those in c-Si.

In a-Si, the abrupt band edges of c-Si are replaced by the broadened tail of states extending into the forbidden gap. These additional states originate from the deviation of the bond length and angle. The band tail states are very important despite their relatively small concentration, since the electronic transport occurs at the band edge. Departure from an ideal network such as coordination defects creates electronic states deep within the band gap. These types of

defects affect many electronic properties of a material by controlling the trapping and the recombination. In the next section, two important electrical characteristics of a-Si:H; namely, DC conductivity and carrier mobility, are briefly discussed.

1.3.1 DC Conductivity

The conductivity of a-Si:H is thermally activated and is expressed by

$$\sigma(T) = \sigma_0 \exp(-E_\sigma / kT) . \tag{1.2}$$

The activation energy E_σ is defined as the average energy of the conducting carriers with respect to the Fermi energy, and prefactor σ_0 is the conductivity prefactor. The E_σ and σ_0 strongly depend on the processing conditions such as the deposition conditions, doping concentrations, and the thermal history of the material [17]. The measured values of σ_0 versus the activation energy are reflected in Fig. 1.3.

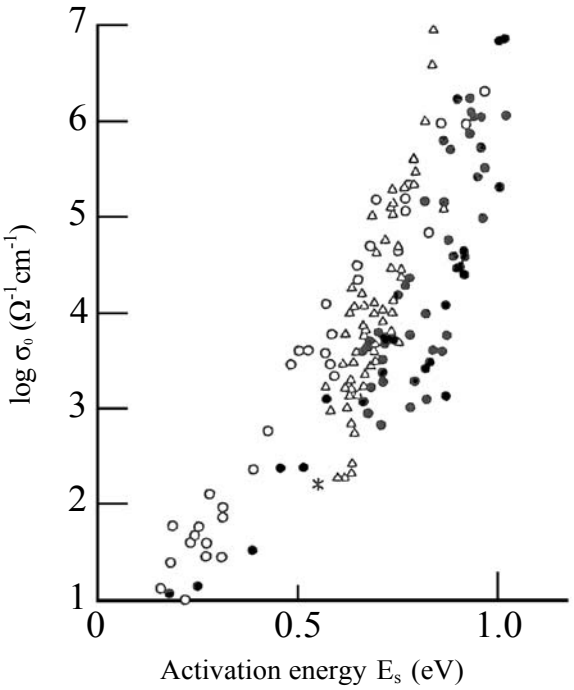

Fig. 1.3 Conductivity prefactor versus the conductivity activation energy [17].

1.3.2 Carrier Mobility

Carrier mobility is defined as the ratio of the electron or hole drift velocity to the applied electric field. The mobility in a-Si:H is usually measured by the time-of-flight technique [11]. In this technique, the measured mobility is drift mobility rather than free carrier mobility, which is the mobility of electron in conduction band. This is due to the fact that the average motion of carriers is measured over a period of time longer than the time needed for the carriers to be trapped in the band tail states. The drift mobility depends on the DOS and free carrier mobility [8], expressed by

$$\mu_D = \mu_0 /(1 + f_{trap}) , \tag{1.3}$$

where f_{trap} is the ratio of the time that the carrier spends in localized traps to the time that is spent in the mobile states, and μ_0 is the free carrier mobility.

Assuming a multiple trapping model of transport in an exponential band tail with the slope of 312°C and 500°C yields the free carrier mobilities of 11 and 0.67 $cm^2V^{-1}s^{-1}$ for the electrons and holes, respectively (Fig. 1.4) [12].

The drift mobility is approximately 1 $cm^2V^{-1}s^{-1}$ for electrons at room temperature, and is almost two orders of magnitude smaller for holes. The reason for the low drift mobility of holes is explained by the larger DOS in the valence band tail.

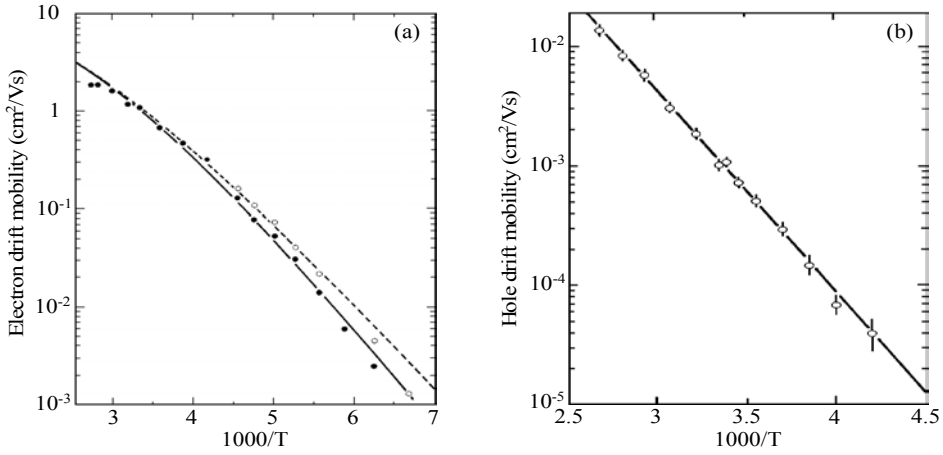

Fig. 1.4 (a) Electron drift mobility data for an electric field of 10^4 V/cm (closed circles) and 2×10^4 V/cm (open circles) and (b) hole drift mobility data for an electric field of 5.8×10^4 V/cm fitted (lines) to the multiple trapping transport mechanism, assuming exponential band tails [12].

1.3.3 Metastability

a-Si:H exhibits metastable phenomena, in which an external electronic excitation such as illumination causes a reversible change in the density of states of the material. In other words, defects are created in the a-Si:H whenever the quasi-Fermi level is shifted from the equilibrium point. The shift in the quasi-Fermi level can be caused by light [18][19] such as in Staebler-Wronski effect, doping [20] or electric field [21]. The created defects reduce the carrier lifetimes and affect the device electrical characteristics. For example, the creation of extra defects within the bandgap of a-Si:H, move the quasi-Fermi level towards the valence band and shift the threshold voltage of a TFT to higher values. In the following chapters, the carrier induced creation of defects in the active layer of a a-Si:H TFT and the resulting threshold voltage shift of the TFT due to the application of gate bias stress will be discussed.

1.4 Thesis Organization

This thesis focuses on the threshold voltage shift of a-Si:H TFT due to a prolonged application of a positive gate voltage stress and the subsequent relaxation of the threshold voltage after the termination of gate bias stress. In Chapter 1 an introduction to a-Si:H material and its properties is given. The electronic DOS of a-Si:H and carrier mobility in a-Si:H, which will be frequently referred to throughout the thesis, are also briefly discussed.
Chapter 2 is a review of the fabrication technology, applications, and modelling of a-Si:H TFTs. There are two roles of TFTs in electronic circuits: a switching function in applications such as active matrix liquid crystal displays (AMLCDs) and passive pixel sensor (PPS) imagers, or an active element function in electronic devices such as active pixel sensors (APSs) and AMOLED displays. For a wide variety of applications, the performance requirements of a TFT in terms of the threshold voltage shift, ON/OFF current ratio, subthreshold slope, and leakage current are outlined. The extracted threshold voltage, and as a result, the quantitative study of the threshold voltage shift, substantially depends on the model used for the I-V characteristics of the TFT. The physics of a-Si:H and the threshold voltage extraction method are discussed in the last two sections of Chapter 2.

Threshold voltage shift mechanisms, due to the application of bias stress, are investigated in Chapter 3. First, the experimental setup used for the application of bias voltage and measurement of the I-V characteristics of a TFT is explained, and then the experimental results of the bias stress test are presented. Then, defect state creation and charge trapping in the silicon nitride (SiN) gate dielectric of TFTs are introduced as the underlying mechanism for the threshold voltage shift of the transistor.

Defect state creation is extensively studied and the supporting evidence for the creation of the extra defect states in the a-Si:H layer close to gate dielectric interface are reviewed. The defect pool model, the role of H atoms and the band tail electrons, and finally, the kinetics of defect state creation are also discussed. Charge trapping in SiN is an alternative mechanism for the threshold voltage shift of TFTs. The kinetics of charge trapping in the mono-energy level and the Gaussian distribution of the SiN traps are analytically modeled at the end of Chapter 3.

In Chapter 4, the threshold voltage relaxation phenomena and its underlying mechanisms are studied. After the gate bias is removed, the threshold voltage of the transistor eventually returns to its original value. This phenomenon is referred to the relaxation of threshold voltage. Threshold voltage relaxation results are presented at the beginning of Chapter 4. Defect state annealing and charge de-trapping from SiN are considered as possible threshold voltage relaxation mechanisms. It is argued that the defect state annealing model cannot explain the threshold voltage relaxation results observed in this work. On the contrary, the analytical models, derived for the kinetics of charge de-trapping from the SiN for the two cases, mono-energetic traps and the Gaussian distribution of SiN traps, are both in good agreement with the experimental results. Then, the distribution of SiN traps is approximated by fitting our model to the experimentally obtained threshold voltage relaxation results. Lastly, by using the threshold voltage relaxation results, the total threshold voltage shift, due to the charge trapping in the SiN can be calculated. This provides a means to quantitatively distinguish between the charge trapping mechanism and the defect state creation mechanism.

Finally, in Chapter 5, the main contributions of this work in understanding the metastability phenomena of a-Si:H TFTs are summarized. Limitation of the present work and suggestion for future work are also briefly discussed.

Chapter 2

Amorphous Silicon Thin Film Transistors

a-Si:H TFT was first proposed by LeComber et al. in 1979 [4]. Two years later, the application of this device in large area electronics was demonstrated by Snell and his coworkers [7]. Since then, there has been an intense effort to improve the performance and characteristics of TFTs [22-25]. a-Si:H TFTs are employed in many applications today such as liquid crystal displays (LCDs) [26], active matrix organic light emitting diode (AMOLED) displays [5] and image sensors [27]. To reduce the design cost of these applications, the modelling of the current-voltage characteristics and the long-term behavior of a TFT, especially their threshold voltage, is important. In this chapter, issues including the fabrication technology, applications, modelling, and parameter extraction of TFTs are briefly looked at.

2.1 a-Si:H TFT Technology

a-Si:H TFTs are fabricated by using a variety of structural topologies and materials. For TFT topologies, there are four types of planar topologies: staggered, inverted staggered, coplanar and inverted coplanar structures [28]. In the coplanar structure, the source, drain and gate electrodes are placed on the same side of the a-Si:H active layer, whereas in the staggered TFTs, the source and drain are placed on one side and the gate on the opposite side of the a-Si:H layer. The difference between the inverted and non-inverted structures is in the sequence of the deposition of the a-Si:H and gate electrode layers. In an inverted structure, the gate electrode is placed at the bottom of the structure, but in a non-inverted structure, the gate metal is on top.

The most popular structure of a TFT which is responsible for the state-of-the-art performance is the inverted staggered structure in Fig. 2.1. Usually hydrogenated amorphous silicon nitride (a-SiN_x:H) is used as the gate insulator of a TFT because of the relatively low interface defect density between the a-Si:H active layer and the a-SiN_x:H insulator layer. Other insulators such as silicon oxide are also employed as the gate insulator [29]. The gate, source, and drain electrodes are made of Cr, Mo or Al metals. Highly n-doped a-Si (n^+ a-Si:H) or n^+ microcrystalline Si is used to reduce the contact resistance between the metal and the a-Si:H layer.

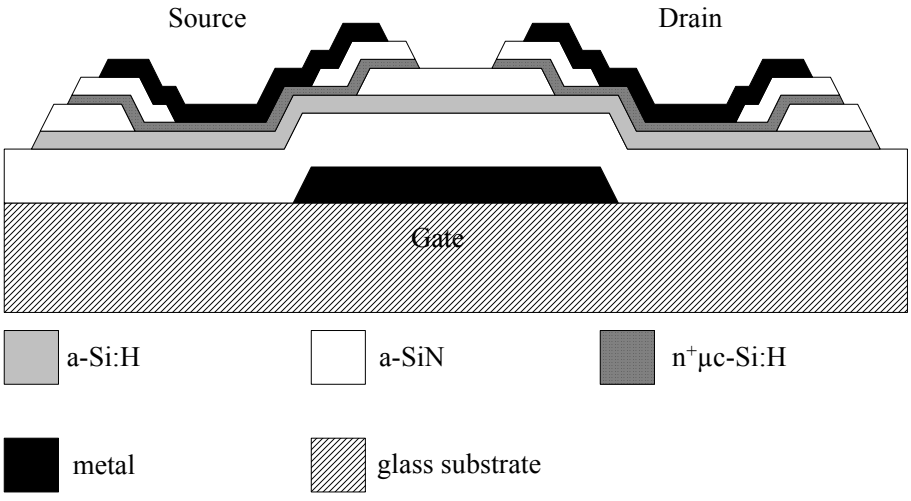

Fig. 2.1 Schematic cross section of an inverted staggered TFT showing different layers.

In this work, TFTs with inverted staggered structure have been used for bias stress experiment. The fabrication process of these TFTs is not a self-aligned process [28] and requires five masks [30]. After the deposition and patterning of the gate metal, a-SiN_x:H/a-Si:H/a-SiN_x:H stacked layers are consecutively deposited by using the plasma enhanced chemical vapor deposition (PECVD) technique. This ensures that the gate insulator and the active layer are not exposed to the environment, and as a result, have a low surface state trap density. In the next step, the source and drain windows are opened, followed by a deposition of n^+a-Si:H and a-SiN_x:H layers. Then, the n^+a-Si:H contact layer is removed between the drain and source regions, and the contact vias are opened in the last a-SiN layer. Lastly, the fabrication is completed by a metal deposition and patterning to form the source, drain, and gate electrodes of the TFT.

2.2 Applications of a-Si:H TFTs

For many years, a-Si:H TFT has been used as a simple switching element in liquid crystal displays (LCD) [31] and passive pixel sensors (PPS) [32]. Recently, TFT is also employed as a linear integrated circuit element in active matrix flat panel imagers (AMFPI) [33] and active matrix organic light emitting diode (AMOLED) displays [34]. Despite the differences of the functionality of TFTs, the architecture of all active matrix arrays is similar as illustrated in Fig. 2.2. Each pixel in the array consists of a sensor or light emitting device and one or more TFTs. The address and data lines run horizontally and vertically between the pixels and connect each pixel to the external circuitry.

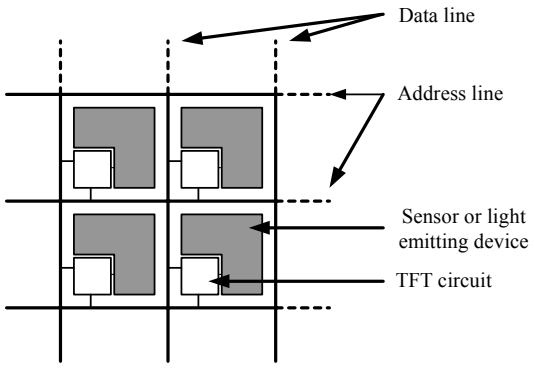

Fig. 2.2 General schematic of an active matrix array.

Depending on the function of the TFT in a circuit, the requirements for the performance of the device changes. This, in turn, dictates the complexity and the cost of the fabrication process. The role of TFTs in imager and display drivers is divided into two categories: (1) for applications such as AMLCD, where TFT acts as switches and (2) for applications such as AMOLED displays, where TFTs are used as linear integrated circuit elements. In the following sections, the required TFT characteristic and the circuit structure for several applications are explained.

2.2.1 AMLCD and PPS Imagers

Typical pixel architectures for an AMLCD and a PPS imager are portrayed in Fig. 2.3. In an AMLCD, each pixel consists of a TFT, a liquid crystal (LC) cell capacitance (C_L), and an additional storage capacitance (C_S) to improve the dynamic characteristics of the pixel [31]. During operation, one address line is turned HIGH. Then, the C_L and C_S capacitances are charged to a certain voltage by the data line. This voltage across the C_L changes the amount of rotation in the polarization plane of the light which passes through the LC material. The rotation angle varies from 90° for unbiased material to almost zero for the material with a peak voltage (20-30V). Therefore, placing two polarizers on both sides of the LC material allows the adjustment of the intensity of the passing light, by changing the applied voltage across the cell. Usually, polarizers are positioned with perpendicular polarization planes in order to provide the maximum intensity, when the applied voltage is zero. The application of a full drive voltage results in light transmission through the LC material with less than 1% of the intensity of its maximum value.

The quality of the performance of TFT is not critical for AMLCDs. The TFT acts only as a switch which connects the C_L and C_S capacitors to the data line. Since the TFT has a low leakage current (in the order of fA), it does not discharge the accumulated charge in C_L and C_S. As a result, the voltage across the LC material, and thus, the light intensity of the pixel remains constant while the other rows of the display are addressed. The demands of the forward characteristics of a TFT are also not very great compared to other applications. For example, a TFT does not need to drive a high current such as that in OLED. Moreover, since

the gate terminal of the transistor is not subjected to a high constant positive voltage for a long period of time, the shift in the threshold voltage of the TFT due to the bias stress is also quite small.

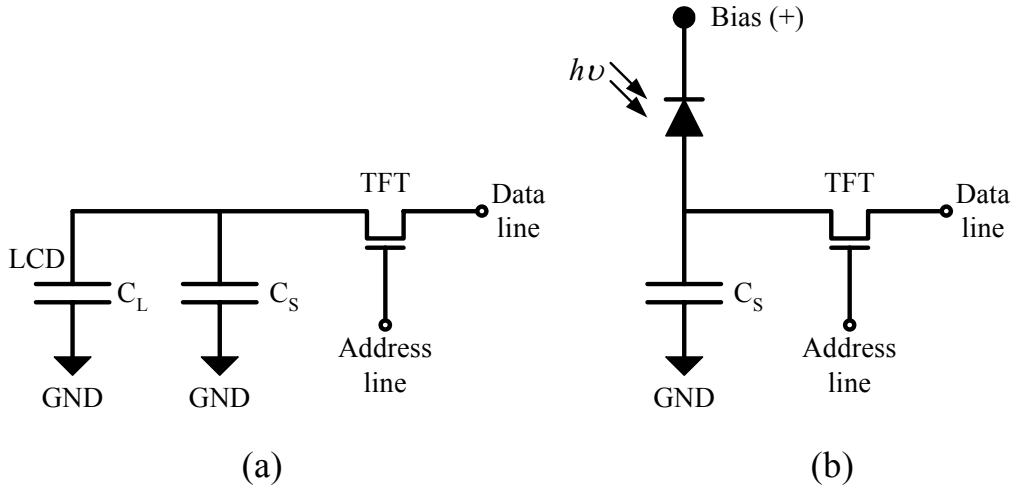

Fig. 2.3 Pixel architecture for (a) an AMLCD and (b) a PPS imager.

The PPS in Fig. 2.3 [32] consists of a sensing element, a storage capacitor, and a TFT acting as a switching device. Some of the common light-sensing devices employed are amorphous selenium (a-Se) photoconductors, reverse biased p-i-n, and Schottky barrier diodes [8]. The operation of the PPS consists of three modes: integration, readout, and reset. During the integration mode, the address line is LOW and the generated charge by the sensor is accumulated in C_{pix} (the sum of the sensor, parasitic, and storage capacitances). This charge is proportional to the amount of radiation and the time of integration (the total time that the TFT is OFF). In the readout mode, the accumulated charge in C_{pix} is transferred to the data line by addressing the TFT. After the readout, the pixel capacitance C_{pix} is charged to some steady state value during the reset mode of the operation. In both the readout and reset modes, the TFT is biased in the linear region of its output characteristics to provide a low ON resistance for a quick charge and discharge of the pixel capacitance.

In general, for a PPS application, the reverse characteristics of a TFT are critical, since the leakage current decreases the stored charge in C_{pix} during the integration time, where a TFT is in the OFF state. Besides, for the high performance of PPS imagers, the TFT must have a

high ON/OFF current ratio, a low subthreshold slope, and a low resistance in the linear region of operation [32].

2.2.2 Active Pixel Sensors and OLED Displays

Fig. 2.4 (a) shows a schematic of a voltage mediated active pixel sensor (APS) imager [33]. Each pixel includes a radiation sensor device, a storage capacitance C_S, and three TFTs. The operation of the APS is similar to the PPS. During the integration mode, an amount of charge is accumulated in C_S. The transistors denoted as AMP and READ in Fig. 2.4(a) form a source follower circuit, which produces an output current in a resistive load. The value of the current is a function of the voltage on the gate of the transistor AMP, and it is proportional to the charge accumulated in C_S.

An APS is one of the most demanding applications of a TFT. The leakage current of the transistor RESET has an adverse effect on the performance, and on the signal-to-noise ratio of the imager by reducing the charge of the storage capacitor. Moreover, the output current is sensitive to the bias induced threshold voltage shift of the transistor AMP. The high ON current, low ON/OFF current ratio, and low subthreshold slope are also required to achieve high performance of the imager.

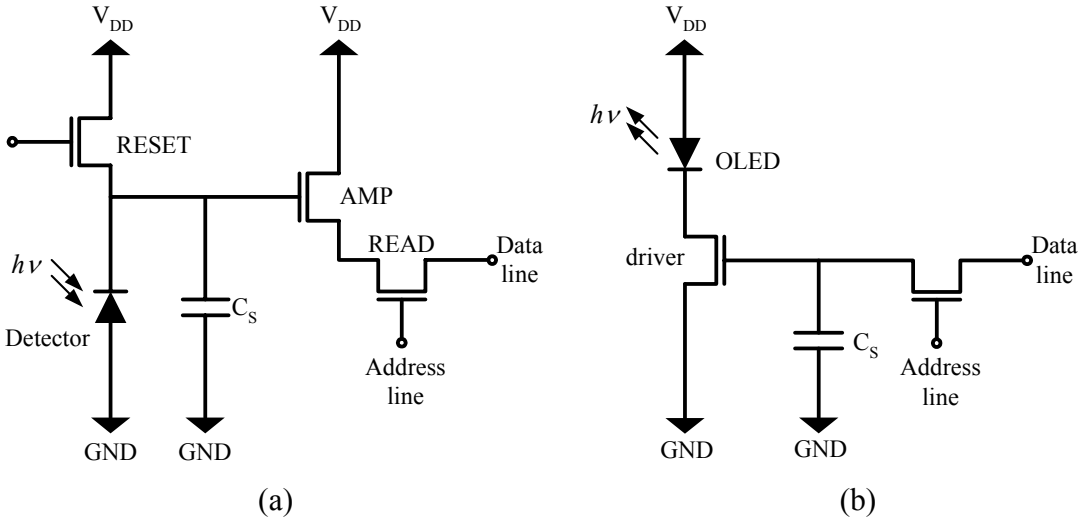

Fig. 2.4 Pixel architecture for (a) an APS and (b) an AMOLED display.

An OLED consists of a stack of organic materials sandwiched between two appropriate electrodes [34]. Electrons and holes are injected from the electrodes into the organic layer. The recombination of the injected electrons and holes into the organic material generates excitons which decay radiatively and produce visible photons.

Some of the advantages of OLED displays over LCDs are faster response time, a lower power consumption, an ability to be fabricated on flexible substrates, a higher contrast, and wider viewing angles [35]. Despite these superiorities, there are still many challenging issues specifically related to the drive electronics [5].

The high-resolution applications require the use of active matrix addressed displays [34]. The simplest OLED driver which consists of two transistors (2-T circuit) is illustrated in Fig. 2.4 [5]. During the addressing period, the storage capacitance is charged to a certain voltage by the switching transistor. Then, the address line becomes LOW and the voltage of C_S stays almost constant throughout the frame time which depends on the number of addressing lines and frame rates. This voltage specifies the current passing through the drive transistor, and consequently, the intensity of the light coming from the pixel.

Since an OLED requires a high drive current, the forward static characteristics of the TFTs are important. In the 2-T driver circuit, the gate of the drive TFT usually has a constant positive voltage during a frame time. This causes the threshold voltage of the transistor to shift inevitably to a higher value and consequently the output current of the transistor, and hence, the light intensity of the OLED decreases over time. Several circuits have been conceived and employed to compensate for the threshold voltage shift and maintain the output current. Most circuits, using current programming method in which the TFT is programmed with an input current instead of an input voltage controlling the drive current [5][36]. However, voltage programmed circuits are also employed [37][38]. In addition to the threshold voltage shift, the TFT must also have a low subthreshold slope, a high ON/OFF current ratio, and a low leakage current. These requirements make AMOLED display drivers one of the most demanding applications in terms of the expected TFT performance.

2.3 Physics of the a-Si:H TFTs

By increasing the applications of a-Si:H TFTs in which a TFT serves as an active circuit element, precise modelling of the current-voltage characteristics of transistor becomes more and more a necessity. Up to the present time, numerous models have been presented in the literature. For example, Demassa et al. [39] have proposed an approach based on an exponential distribution of band tails, when a-Si:H active layer is very thin. Leroux [40] has presented an analytical model for the static and dynamic characteristics of the a-Si:H TFT considering the effect of the a-Si:H film thickness, but neglecting the contribution of the deep states. Shur et al. [41] have presented a model describing different operating regimes by using the following definition for the field effect mobility:

$$\mu_{FET} = \mu_0 \left(\frac{n_{free}}{n_{induced}} \right). \tag{2.1}$$

With (2.1) as the basic definition for the field effect mobility, the above-threshold drain-source current equations for linear and saturation regions are expressed by

$$I_{DS} = \begin{cases} \mu_{FET} C_i \dfrac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \dfrac{V_{DS}^2}{2\alpha_{Sat}} \right] & \text{for } V_{DS} < \alpha_{sat} (V_{GS} - V_T) \\ \mu_{FET} C_i \dfrac{W}{L} \dfrac{(V_{GS} - V_T)^2 \alpha_{sat}}{2} & \text{for } V_{DS} \geq \alpha_{sat} (V_{GS} - V_T). \end{cases} \tag{2.2}$$

Here C_i, W, L, and V_T are the gate capacitance per unit area, channel width, channel length, and threshold voltage, respectively. The parameter α_{sat} accounts for the variation of the depletion charge across the channel. The DOS in the mobility gap of the a-Si:H for both acceptor-like and donor-like states can be accurately modelled by the sum of the two exponential functions [42]. Since the characteristic temperature of the tail states is lower or in the order of the thermal temperature, the quasi-Fermi level moves slowly toward the conduction band as the gate voltage is increased. Therefore, μ_{FET} is a weak function of the gate bias, and is described by a power law [41],

$$\mu_{FET} = \mu_0 \left(\frac{V_{GS} - V_T}{V_{AA}} \right)^{\gamma}. \tag{2.3}$$

Here, γ is the power parameter and V_{AA} is the characteristic voltage which is geometry dependent.

In another model, presented by Servati et al., a different approach has been used to derive the drain-source current in the above-threshold region of operation [43]. In this model, the conductivity is written as

$$\sigma_n = q\mu_{band} n_{free}, \tag{2.4}$$

where n_{free} is the density of electrons excited to the extended states whose energies are higher than the mobility edge E_C, μ_{band} is the electron mobility in the extended states, and q is the elementary charge. In (2.4), the contribution of the hopping conduction of the localized states to the conductivity σ_n has been neglected. The density of the free electrons is given by

$$n_{free} = N_C \exp\left[\frac{E_F - E_C}{kT}\right] = N_{fi} \exp\left(\frac{\psi}{V_{th}}\right). \tag{2.5}$$

E_F, N_C, k, T and V_{th} are the Fermi level, the concentration of free electrons when $E_F = E_C$, the Boltzmanns constant, temperature, and thermal voltage (kT/q), respectively. Also, ψ and N_{fi} are defined by $(E_F - E_i)/q$ and $N_C \exp[(E_i - E_C)/kT]$, where E_i is the intrinsic Fermi level of a-Si:H.

An increase in the gate-source voltage moves the quasi-Fermi level towards the mobility edge. In the above-threshold region of the operation ($V_{GS} > V_T$), the quasi-Fermi level resides in the conduction band tail. As a result, the number of trapped ($n_{trapped}$) electrons in the localized tail states is much larger than the number of free electrons; $n_{trapped}$ is approximately equal to the total number of induced electrons $n \sim n_{trapped}$. Integration over the exponential DOS, weighted by the Fermi-Dirac probability function, yields the density of the trapped electrons in the conduction band tail as follows:

$$n_{trapped} = N_{ti} \exp\left(\frac{\psi}{V_{nt}}\right), \tag{2.6}$$

where V_{nt} is the slope of the conduction band tail, and N_{ti} is the density of the trapped electrons when $E_F = E_i$. By adopting (2.5) and (2.6), the number of free electrons can be related to the number of trapped electrons by

$$n_{free} = \frac{N_{fi}}{N_{ti}^{\frac{\alpha}{2}}} n_{trapped}^{\frac{\alpha}{2}}, \tag{2.7}$$

where $\alpha = 2V_{nt} / V_{th}$. By substituting (2.7) into (2.4), the conductivity in the above-threshold region of operation ($n \sim n_{trapped}$) is expressed as

$$\sigma_n = q\mu_{band}\frac{N_{fi}^{\frac{\alpha}{2}}}{N_{ti}^{\frac{\alpha}{2}}}n^{\frac{\alpha}{2}}. \tag{2.8}$$

With (2.8), Servati has derived the following expressions for the drain-source current in the linear and saturation regions of operation [43]:

$$I_{DS} = \begin{cases} \mu_{eff}\zeta C_i^{\alpha-1}\frac{W}{L_{eff}}(V_{GS}-V_T-0.5V_{DS})^{\alpha-1}(V_{DS}-(R_S+R_D)I_{DS}) & V'_{DS} < \alpha_{sat}(V'_{GS}-V_T) \\ \mu_{eff}\zeta C_i^{\alpha-1}\frac{W}{L_{eff}}\gamma_{sat}(V_{GS}-R_sI_{DS}-V_T)^{\alpha}(1+\frac{\lambda}{L_{eff}}V_{DS}) & V'_{DS} > \alpha_{sat}(V'_{GS}-V_T). \end{cases} \tag{2.9}$$

Here, μ_{eff}, ζ, α_{sat}, R_S, R_D, L_{eff}, and W are the effective mobility, unity matching parameter, saturation parameter, source contact resistance, drain contact resistance, effective channel length, and channel width, respectively. V'_{DS} and V'_{GS} are also defined by

$$V'_{GS} = V_{GS} - I_{DS}R_S \quad \text{and} \quad V'_{DS} = V_{DS} - (R_s + R_D)I_{DS}. \tag{2.10}$$

Although all the models predict the true I-V characteristics of a TFT, the last model enjoys the simplicity, and includes the effect of the source and drain contact resistances. Furthermore, the different parameters such as the field effect mobility are geometry and bias independent. In the remainder of this thesis, Servatis's model is used for extracting the threshold voltage of a TFT. The procedure for the threshold voltage extraction is explained in the next section.

2.4 Parameter Extraction

To study the threshold voltage shift due to bias stress, a simple but accurate method of threshold voltage (V_T) extraction must be used. In contrast to the c-Si MOSFETs, the power parameter of the drain-source current is not exactly 2. Moreover, the presence of a high source and drain contact resistance adds even more complexity to the parameter extraction procedure.

Both the linear and saturation regions of operation are used to extract V_T. By using (2.9) and defining the parameters g_{mlin} and g_{msat} as

$$g_{mlin} \cong \frac{\partial I_{DS,lin}}{\partial V_{GS}} \quad \text{and} \quad g_{msat} \cong \frac{\partial I_{DS,sat}}{\partial V_{GS}}, \tag{2.10}$$

the following equations can be easily derived [43]:

$$\frac{I_{DS,lin}}{g_{mlin}} = \frac{V_{GS} - V_T - 0.5V_{DS}}{\alpha - 1} \frac{V_{DS}}{V_{DS} - R_{DS} I_{DS,lin}} \tag{2.11}$$

and

$$\frac{I_{DS,sat}}{g_{msat}} = \frac{V_{GS} - V_T + R_{DS} I_{DS,sat} (\frac{\alpha - 1}{2})}{\alpha}, \tag{2.12}$$

where $I_{DS,lin}$ and $I_{DS,sat}$ are the drain-source current in the linear and saturation regions of operation and R_{DS} is the sum of the drain and source contact resistances.

The plots of the right hand sides of (2.11) and (2.12) versus V_{GS}, when $R_{DS} I_{DS,lin} << V_{DS}$ and $R_{DS} I_{DS,sat} << V_{GS}$, give straight lines. From the slope and the x-intercept of this line, α and V_T can be determined. The same result is also achieved by the method developed by Cerdeira et al. [44]. Based on this method, an integration of I_{DS} over V_{GS}, divided by I_{DS} (V_{GS}) yields the following equations for the saturation and linear regions:

$$\frac{\int_0^{V_{GS}} I_{DS,lin}(v_{gs}) dv_{gs}}{I_{DS,lin}(V_{GS})} = \frac{V_{GS} - V_T - 0.5V_{DS}}{\alpha - 1} \tag{2.13}$$

and

$$\frac{\int_0^{V_{GS}} I_{DS,sat}(v_{gs}) dv_{gs}}{I_{DS,sat}(V_{GS})} = \frac{V_{GS} - V_T}{\alpha}, \tag{2.14}$$

if it is assumed that $R_{DS} I_{DS,lin} << V_{DS}$ and $R_{DS} I_{DS,sat} << V_{GS}$.

Although the two methods result in the same values for V_T and α, the first method uses the derivative of I_{DS}, which is derived easier. For this reason, throughout this thesis, the parameters are extracted by using (2.12).

2.5 Summary

In this chapter, a-Si:H TFTs and their fabrication processes were briefly reviewed. The role of TFTs in AMLCDs, PPSs, APSs and OLED displays were also discussed. The performance requirements of the TFT in terms of the threshold voltage shift, ON/OFF current ratio, subthreshold slope, and leakage current for each of these applications were outlined. In Sections 2.3 and 2.4, the TFT model, which is used for the fitting the I-V characteristics of the TFTs, and the parameter extraction procedure were explained.

Chapter 3

Bias-Induced Threshold Voltage Shift in a-Si:H TFTs

Well-established industrial fabrication process of a-Si:H TFT produces transistors with quite uniform characteristics across the substrate and from run to run [46]. However, TFT characteristics are seriously shifted due to bias stress. The most important characteristic shift of a-Si:H TFTs is the shift in the threshold voltage of the device due to the prolonged application of gate bias. The threshold voltage shift severely impacts the operation of a-Si:H TFT circuits, especially where the transistor acts as an active element such as in AMOLED displays. For instance, the output current of OLEDs drastically decreases over time with the threshold voltage shift of the driving TFT; therefore, without a circuit compensation scheme, the application of two TFT pixel circuits [5] is not suitable for AMOLEDs.

There have been many efforts to study the threshold voltage shift mechanisms and to estimate the long-term behaviour of the threshold voltage of a transistor by its dependence on the stress period and voltage [47-50]. These investigations commonly concern applying DC or AC voltages to the gate electrode of the TFT, and the joint effect of relaxation and stress of the TFT has been neglected. In addition, the present models [48][50] for threshold voltage shift do not completely explain the experimental results. The increasing use of TFTs in large

area electronics necessitates a more precise model of the threshold voltage shift of a-Si:H TFT. This chapter traces the underling mechanisms for the threshold voltage shift, and the threshold voltage shift models presented in literature for the positive gate bias stress. Later in this Chapter, I present an analytic model for the kinetics of charge trapping in SiN, which is developed for the cases of the charge trapping in the mono-energetic and the Gaussian distribution of SiN traps.

3.1 Shift in the Threshold Voltage Caused by a Positive Gate Bias

The effect of bias voltage and stress time on threshold voltage shift (ΔV_T) has been investigated on two sets of a-Si:H TFTs, each set includes 9 TFTs with different aspect ratios W/L. Samples are of the inverted-staggered, bottom gate structure fabricated using a standard trilayer process [45] with process conditions given in appendix A. The experimental set up measuring the bias and time dependence of threshold voltage is denoted in Fig. 3.1. First, the sample was annealed at 180°C for one hour and cooled to room temperature at a rate of 1°C/min. The transfer characteristics (I_D -V_G) of the TFT were measured by the Keithley SMU 236 parameter analyzer at V_D=15V for the gate voltages of -5V ≤ V_G ≤ 15V with 0.25V step. This was followed by the application of a gate stress voltages with the Keitley SMU while V_{DS} = 0 V. Gate bias stress voltages of 10, 15, 20, 25, 35 and 50V were used in this work, similar to the range of values employed in Ref. [48] and [50]. At certain times, which are shown in Fig. 3.4, the bias stress was removed, and the transfer characteristics were measured. All the experiments were performed at room temperature (T = 298 K).

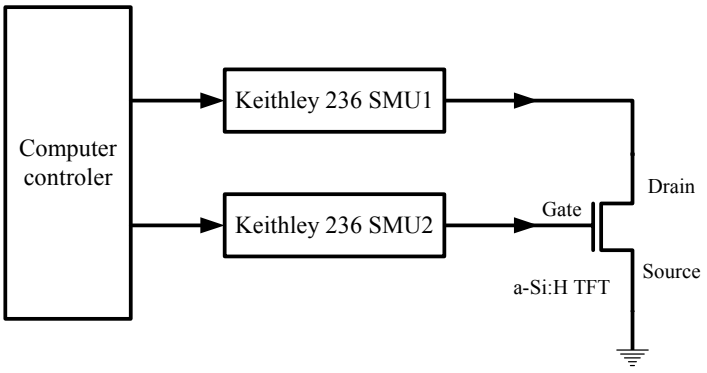

Fig. 3.1 Experimental setup for the ΔV_T measurement.

The transfer characteristics of a TFT with W/L = 500/100 μm after t = 0, 9×10^2 and 1.26×10^4 seconds of a 20V gate bias stress are shown in Fig. 3.2. The TFT were fabricated using MP6 process explained in appendix A and has an initial threshold voltage V_{T0} of 1V. It can be seen that the transfer characteristics are shifted to more positive gate-source voltages by increasing the stress time.

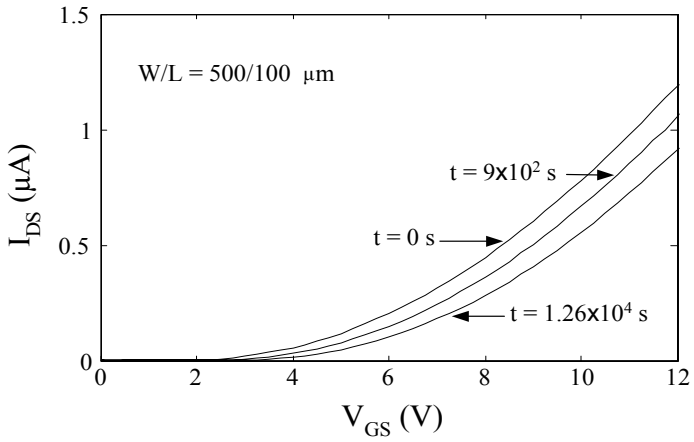

Fig. 3.2 Transfer characteristics of a TFT at different times after the application of a 20V gate bias stress (V_{DS} = 0 V during the stress).

To study the effect of bias stress on the subthreshold region of operation, the transfer characteristics of Fig. 3.2 are plotted on the semi-logarithmic scale in Fig. 3.3.

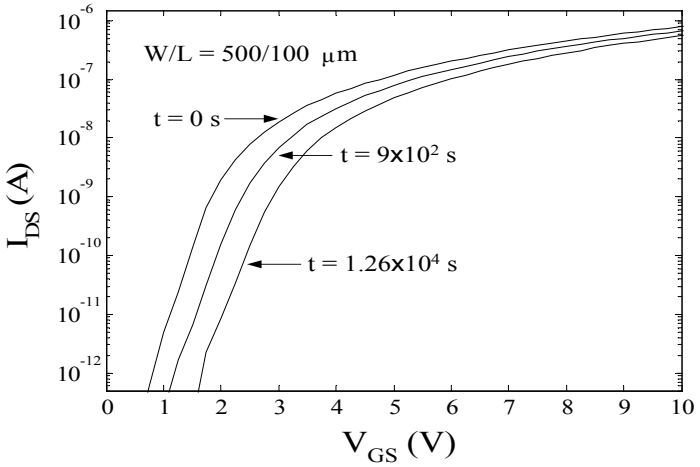

Fig. 3.3 I-V characteristics of a TFT plotted on a semi-logarithmic scale after t = 0, 9×10^2, and 1.26×10^4 s of the application of a 20V gate bias stress (V_{DS} = 0 V during the stress)

Fig. 3.3 reveals that, although the transfer characteristics are moved to higher gate voltage values by increasing the stress time, the subthreshold slope ($dV_{GS}/d\ \log_{10} I_{DS}$) does not change significantly in this experiment. The effects of higher stress voltages and longer stress times on the subthreshold slope are also studied. For the application of stress voltages as high as 35V and for stress times longer than 10 hours, the subthreshold slope does not increase more than 5% of its original value.

The threshold voltage is extracted from the measured transfer characteristics by employing the method described in Section 2.4. The time dependence of threshold voltage shift (ΔV_T) is plotted in Fig. 3.4 for the stress voltages of 10, 15, 20, 25, 35, and 50 V, applied to the gate with $V_{DS} = 0$ during the bias stress. In Fig. 3.5, the threshold voltage shift versus $V_{ST} - V_{T0}$, after 3.5 hours of bias stress, is shown. V_{T0} and V_{ST} are the initial threshold voltage of the TFT and gate bias stress voltage, respectively.

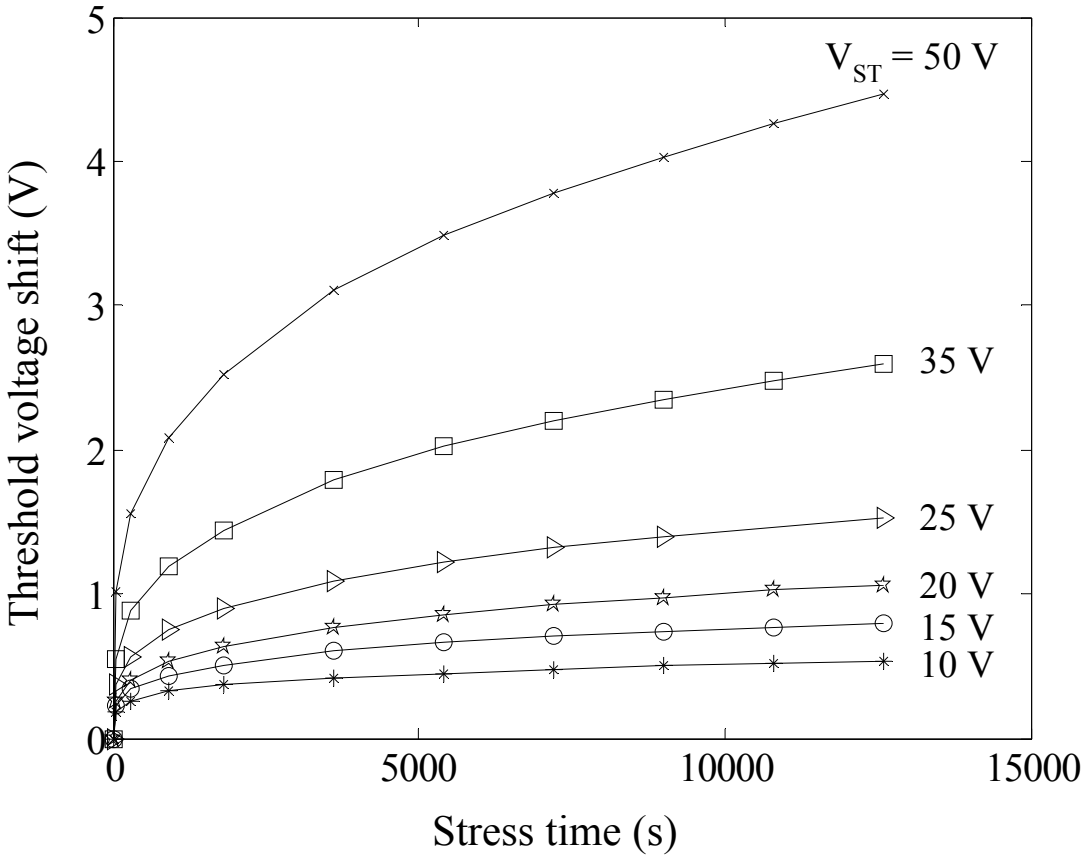

Fig 3.4 Threshold voltage shift versus time for different stress voltages (V_{DS} = 0 V during the stress, and the TFT aspect ratio is W/L = 500/100 μm).

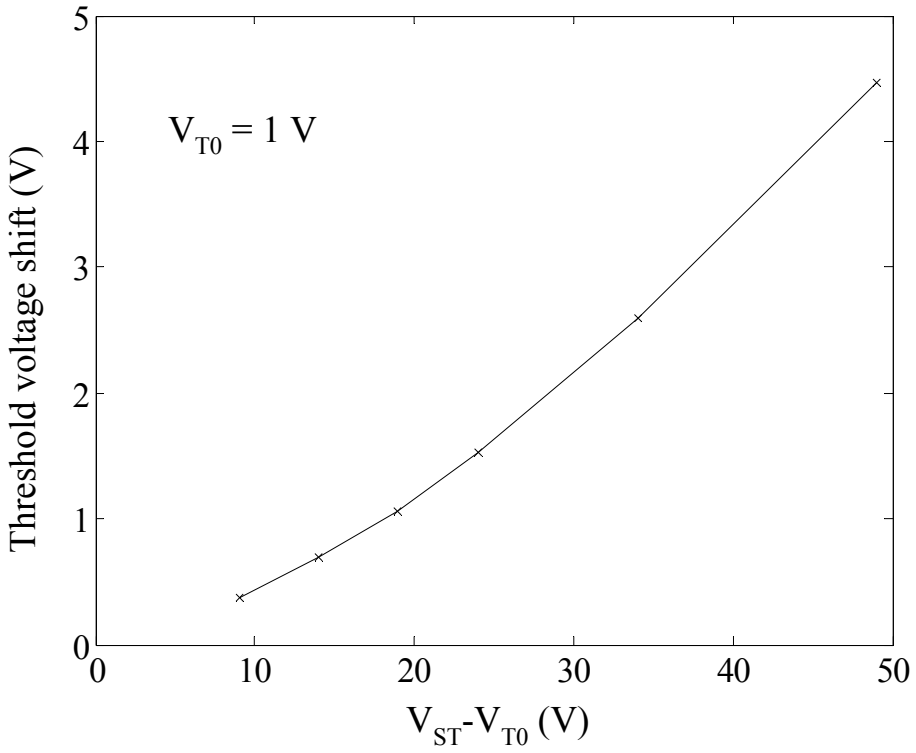

Fig. 3.5 Threshold voltage shift vs. $V_{ST} - V_{T0}$ after 3.5 hours of bias stress (during the application of the gate stress V_{DS} = 0 V).

The initial threshold voltages for the samples used for the bias stress tests in Fig. 3.4 and Fig. 3.5 are 1.0V. After each test, the samples were annealed at 180°C for 1 hour and then cooled down to room temperature at a rate of approximately 1 °C/min. The annealing process retrieved the threshold voltage of the TFT within 50mV of its original value.

The experimental data in Fig. 3.4 and Fig. 3.5 demonstrate that the threshold voltage shift increases almost linearly with the effective stress voltage, $V_{ST} - V_{T0}$.

In the next few sections of this chapter, the various models discussed in the literature and the underlying mechanisms for threshold voltage shift are reviewed. The main focus of this thesis is on the effect of the positive DC bias stress, when the drain is connected to the source.

3.2 Mechanisms Responsible for Threshold Voltage Shift of a-Si:H TFTs

The threshold voltage shift in SiN gate insulator TFTs was originally attributed to charge trapping in the slow states located in SiN [47] (Powel, 1983). In 1987, Powel et al. proposed an alternative model involving the slow creation of defect states in a-Si:H [48]. It is believed that these defect states are Si dangling bonds similar to those arising in photo-induced degradation phenomenon [49]. In 1993, the threshold voltage shift was again interpreted as a result of charge injection from the channel into the traps located at the a-Si:H/a-SiN_x:H interface or inside the gate insulator as reported by Libsch et al. [50].

The principal difference between the charge trapping and defect state creation models is that in Ref. [47] and [50], the charge is assumed to be slowly trapped into already existing states in the bulk or interface of the gate dielectric which are in poor communication with the a-Si:H conduction band. Contrarily, the defect state creation model proposes that there is a slow process of the creation of the extra states, which are in good communication with the a-Si:H conduction band. The term communication between two different states implies how fast carriers can move from one state to another. For example, good communication between defect states and conduction band of a-Si:H means that electrons of the conduction band trap into defect states in much shorter times than the duration of bias stress experiment.

Although the underlying mechanism for the threshold voltage shift is still controversial, it is widely accepted that both mechanisms perhaps operate simultaneously [51-53]. At high gate biases such as 100V, the charge trapping in the SiN is responsible for the threshold voltage shift of the TFT [48]. However, at low gate stress voltages as low as 25V, the V_T shift of a-Si TFTs is mostly due to the defect state creation in the a-Si:H active layer near the interface [48]. In the following sections, I review the charge trapping and defect state creation models and discuss the kinetics of charge trapping due to a positive gate voltage for the mono-energetic level, and a realistic Gaussian distribution of the SiN trap states.

3.2.1 Defect State Creation Mechanism

In this section, I present the supporting evidence for the increase in the density of the dangling bond defect states within a-Si:H. Then, I review the defect pool model [54] to describe the creation and removal of the states at different energies inside the band gap of the a-Si [54] due to the application of bias stress. The roles of H atoms [55] and band tail carriers [56] in the metastable defect formation are also discussed. Finally, the kinetics of defect state creation and the stretched exponential behaviour of the threshold voltage shift is explained by the dispersive diffusion of the H atoms in the a-Si:H network [51][55].

3.2.1.1 Creation of Extra Defect States in a-Si:H due to Bias Stress

Evidence of the creation of extra defect states in a-Si:H came from the photo-induced charge emission of TFTs biased into depletion after a period of positive bias stress [49]. The experimental procedure is as follows. First, a gate field is applied to a source-drain connected transistor for a period of time, t_g. During this time, the source and drain contacts inject electrons through the a-Si:H layer toward the SiN interface. After a delay time t_d from the termination of the gate field, the sample is briefly illuminated, yielding a discharge current flow through the source and drain contacts. The total emitted charge over time is not in a simple exponential form of an RC discharge and exhibits dispersion. Possibly, this is due to a range of trapped-carrier-release time constant arising from a variation in the trap depth. The charge emission is described by the following equation:

$$Q(t) = Q_0 \int \frac{N(E)}{N_t} \exp\left(\frac{-t}{\tau(E,T)}\right) dE \,, \tag{3.1}$$

where $\tau(E,T) = \upsilon^{-1} \exp(E/kT)$, $N(E)$ is the distribution of traps per unit volume per unit energy, and $N_t = \int N(E) dE$.

In (3.1), it is assumed that the illumination is sufficient to completely discharge the trap states. Hepburn et al. [49] have found that a Gaussian distribution of the trap states with a centre depth of E_0 = 0.85 eV, a standard deviation of ΔE = 0.08 eV, and an attempt-to-escape frequency of $\nu = 10^{12}$ Hz gives a good fit to their experimental data. The magnitude of the

emitted charge also increases as t_g increases. Since the emitted charge can also come from the tunnelling of the electrons into the dielectric during the application of the gate voltage, another supporting experiment is needed to reach a more definite conclusion.

The photo-induced discharge (photo-discharge) of the electrons after the application of the gate voltage can be further used to distinguish between trapped electrons inside the SiN and the trapped electrons inside the extra defect states in the band gap of a-Si:H. In the [49], the gate voltage was applied for a considerably long time (t_g = 24 hours), followed by the discharge of all trapped charges by a sufficiently lengthy pulse of illumination. Then, the transistor was annealed at a certain temperature for a period of time, t_{ann}. This is followed by the application of a very short pulse voltage to the gate (t_g = 1s), and second illumination to discharge the trapped electrons. The secondary discharge pulse has a considerable greater amplitude than those observed when a fresh or annealed sample is subjected to a single charge-discharge cycle with t_g = 1s. The annealing of the samples at 450K for 30 minutes recovers the original response of the transistor to the applied gate field.

Fig. 3.6 depicts the secondary photo-discharge response as a function of t_{ann}. The decay of the charge is very slow at room temperature but increases at higher temperatures with an activation energy of 1.5 eV.

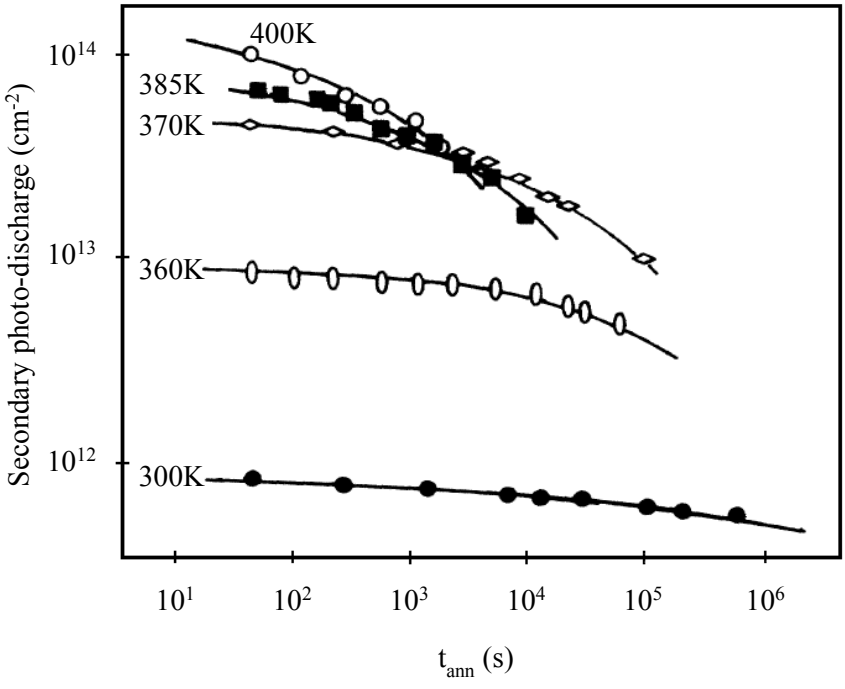

Fig. 3.6 Secondary photo-discharge response versus annealing time [49].

Observation of the enhanced secondary discharge pulse, and the fact that release and annealing processes have two different activation energies, 0.85 eV and 1.5 eV, respectively, suggest that the trapping and detrapping of electrons to and from the dielectric cannot be the only mechanism involved in the observed photo-discharge phenomenon. The creation of metastable dangling-bond states within the a-Si:H close to the dielectric interface is consistent with the experimental data. Moreover, the annealing rate of the dangling-bond states responsible for the Staebler-Wronski effect [18], exhibits activation energies of approximately 1.5 eV, similar to those of the annealing activation energy of the defect states observed in the photo-discharge experiment. This also supports the idea of the creation of the extra defect states due to the application of the gate bias stress.

3.2.1.2 Defect Pool Model

There are two distinct mechanisms responsible for the threshold voltage shift of a-Si:H TFTs: charge trapping in the SiN dielectric and the creation of extra defect states in the a-Si:H layer close to the SiN gate dielectric interface. The defect pool model [54] proposed in 1992, presents a unifying description for the creation and removal of the states at different energies in the band gap. Based on this model, the creation of the states in the upper part of the band gap (above the zero-bias position of the Fermi energy level) leads to a positive shift of the electron threshold voltage, an increase of the electron subthreshold slope, and a negative shift of the hole threshold voltage, but it does not affect the hole subthreshold slope. On the other hand, creation of the states in the lower part of the band gap causes the electron threshold voltage to move to a higher positive voltages, and the hole threshold voltage to more negative values. It also increases the hole subthreshold slope, but does not affect the electron subthreshold slope. The electron and hole threshold voltages or subthreshold slopes refer to the corresponding parameters, when the TFT operates as an n-channel or p-channel device, respectively. Figs 3.2 and 3.3 clearly show a positive threshold voltage shift and no change in the subthreshold slope for the n-channel operation of TFTs, supporting the idea of the creation of the states in the lower part of the band gap.

Using the field effect method, Powel et al. [57] have calculated the energy-dependent DOS of a-Si:H throughout the band gap from the transfer characteristics for oxide gate transistors. Since the number of trap states is much smaller in silicon oxide (~10^{14} cm^{-3}) than in SiN (~10^{18} - 10^{19} cm^{-3}), to get rid of the effect of the charge trapping into the gate dielectric, transistors with silicon oxide as the gate dielectric have been used for bias stress tests in [54]. The calculated DOS for oxide transistors is depicted in Fig. 3.7. The results indicate that for low positive biases, the state creation in the lower part of the band gap is the dominant mechanism, whereas at low negative biases states are created in the upper part of the band gap. For SiN gate TFTs, the removal of the states from the lower part of the band gap due to low negative gate voltages has been also proposed [54], complicating the presumed instability mechanisms of SiN gate TFTs even more. For a SiN gate transistor as presented in the next chapter, even at low positive bias stresses, the charge trapping is not negligible.

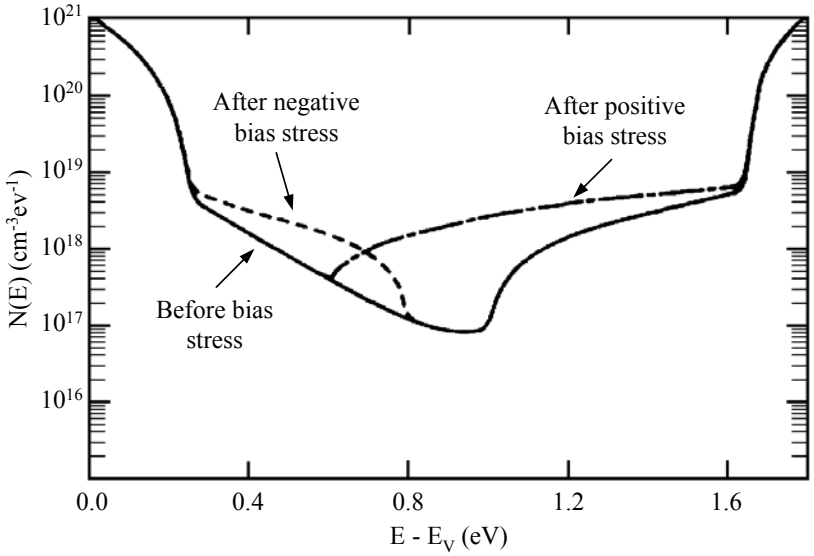

Fig. 3.7 Calculated density of states (DOS) before (solid line), after positive (chain line), and after negative (dashed line) bias stress for an oxide gate transistor [54].

The physics of state creation and removal processes, proposed by Street et al. [58], are based on breaking the weak Si-Si bonds to form a Si dangling bond. The weak bond state can be converted to a dangling bond by the following reactions:

$$Si_4^0 + e \rightarrow Si_3^- \tag{3.2}$$

$$Si_4^0 + h \rightarrow Si_3^+ . \tag{3.3}$$

The first reaction (3.2) happens under electron accumulation and the resulting dangling bond is negatively charged, called a D^- defect. Under hole accumulation, the second reaction (3.3) takes place in which the created dangling bond is positively charged and labeled as D^+. A defect state can also be formed as a neutral defect D_0, which is the result of breaking a weak Si-Si bond without interacting with an electron or a hole. The energy of the defect state depends on the charge state of the defect, its formation energy, and the position of the Fermi level. When a D^- state is formed, its formation energy is reduced by the energy released from falling of a quasi-Fermi level electron to the defect state. Similarly, the fall an electron from a D^+ defect energy level to the quasi-Fermi level, reduces the formation energy of that defect state. The difference in the formation energy of a defect formed as a D^- or D^+ state at energy E^* for a certain quasi-Fermi energy level E_F is given by

$$E_{form}(D^+) - E_{form}(D^-) = 2(E_F - E^*) - U\,, \tag{3.4}$$

where U is the correlation energy, and E^* is the defect energy when it is singly occupied, i.e., the +/0 transition energy.

In [58], the formation energy of a neutral defect is defined as the one-electron energy difference between the valence band state and dangling bond,

$$E_{form}(D^0) = (E^* - E_{VB})\,, \tag{3.5}$$

where $E_{form}(D^0)$ is the formation energy of the neutral defect at E^*, and E_{VB} is the valence band energy.

By using (3.5), the formation energies of the charged defects are expressed as [54]

$$E_{form}(D^+) = E_F - E_{VB} \tag{3.6}$$

$$E_{form}(D^-) = 2E^* - E_F + U - E_{VB}\,. \tag{3.7}$$

If a pool of potential defects $P(E)$ is assumed, which is the distribution of energies at which a defect can be formed, the density of created defects $D(E)$ at the equilibration temperature T^* is given by the product of $P(E)$ and the probability of the defect formation at energy E. Therefore,

$$D(E) = P(E)\exp(-E_{form}/kT^*)\,. \tag{3.8}$$

There are separate contributions to $D(E)$ from the D^- and D^+ states. If a Gaussian distribution is assumed for $P(E)$, since the formation energy of the D^- states depends on the

energy of the defect, $D(E)$ for the D^- states becomes another Gaussian with the same width σ as $P(E)$ but the peak is shifted by

$$\Delta E = 2\sigma^2 / kT^* - U \tag{3.9}$$

from the peak in $P(E)$.

The $D(E)$ for D^+ is also Gaussian with the same width and peak as that of $P(E)$. This is due to the fact that the formation energy of the D^+ states does not depend on the defect energy.

If the weak-bond energy is attributed to the exponentially distributed valence band tail states, (3.8) is replaced by an integral over the tail states and the Boltzmann factor, $\exp(-E_{form} / kT^*)$, is replaced by the Fermi-Dirac-like distribution function. In the case of $E_0 > kT^*$, where E_0 is the characteristic energy of the valence band tail states, expressions similar to (3.8) and (3.9) result with kT^* replaced by E_0.

Fig. 3.8 represents the calculated DOS for intrinsic a-Si:H [54]. D_e, D_h, and D_0 represent the states initially formed as D^-, D^+, and D^0, respectively. Each D_e, D_h, and D_0 state has +/0 and 0/- transition energies, which is the position of the single and double- occupancy levels, separated by U. For example, D_e^-, D_e^0, and D_e^+ are different charge states of D_e defects. The D_e^0 and D_e^+ defects are initially formed as D_e^-, but lose one or two electrons, depending on the position of the Fermi level.

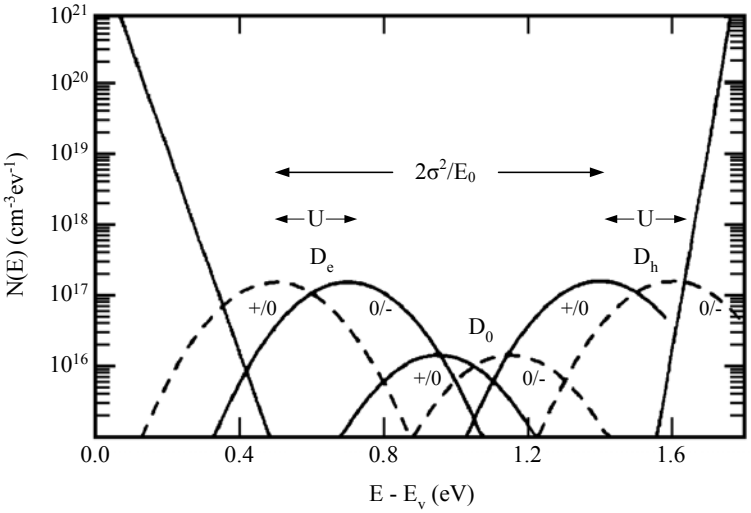

Fig. 3.8 Calculated density of states (DOS) in a-Si:H. D_e, D_h, and D_0 states and their corresponding +/0 and 0/- transitions are shown; the valence and conduction band tails are also indicated [54].

Based on (3.6) and (3.7), lowering E_F decreases the formation energy of the D_h states and increases the corresponding value for the D_e states. This leads to an exponential increase in the density of the D_h states and an exponential decrease in the density of the D_e states. Raising E_F does not affect the energy position of the D_e and the D_h states, but the majority of the defect states change from D_h to D_e.

In summary, this model gives the energy position of the dangling bonds created by positive and negative bias stresses. A positive bias stress increases the Fermi energy that leads to the formation of defect states in the lower part of the band-gap, whereas a negative bias stress results in the formation of defects in the upper part of the band-gap.

3.2.1.3 Role of Hydrogen Atoms and Band-tail Carriers in the Formation of Metastable Defects

The breaking of weak Si-Si bonds is the most accepted model that has been developed to explain the defect creation process due to the shift in the Fermi level of a-Si:H [58][59]. After a weak Si-Si bond is broken, the new Si dangling bonds must be stabilized; otherwise, two adjacent Si dangling bonds form another Si-Si bond. It has been proposed that some H motion is involved in the kinetics and stabilization of the metastable defects [55][60]. The basic model suggests that H, which is bonded to Si, is either released interstitially with subsequent trapping or changes position from one Si atom to another to create and anneal the dangling bonds. The idea behind this model, called the diffusion-mediated metastable changes [56], is that there are certain configurations in the Si network which can produce defects, when an H atom diffuses to that particular position. Consequently, the time dependence of the defect creation process is determined by the diffusion of the H atoms towards these defect formation sites. For this happens, the H atom must leave the Si-H bond to occupy a transport state before bonding to another Si-H bond. This H transport state can be an unbonded H-interstitial state, a state in which two H atoms are paired or a state in which the H atom is partially attached to the Si atom before bonding to another Si atom.

The supporting evidence for the involvement of H in the metastable changes of a-Si:H comes from a number of observations [60-65]. First, all the metastable changes anneal at temperatures between 150º and 230ºC. It is known that at these temperatures, H diffuses quite rapidly through the network [61][62]. Secondly, an annealing temperature, grater than 420ºC, is required to reduce the large spin densities found in the unhydrogenated material. Also, only crystallization temperatures higher than 600ºC reduce the defect density to a level found in a-Si:H [63]. Thirdly, the motion of an H atom provides a mechanism for stabilizing the metastable defects against recombination, since the H is mobile and not constrained by more than one bond. Furthermore, H diffusion has been found to be dispersive; that is, it exhibits a time-dependent diffusion coefficient similar to the carrier transport in a-Si [62]. This dispersive H motion accounts for the stretched exponential decay of the excess carriers in doped a-Si [60], the annealing of light induced defects [64], and the carrier-induced creation of defects [65].

The role of the band tail carriers in the process of the creation of dangling bonds is also significant. Experimental results reveal that increasing the carrier density increases the rate at which H atoms hop; in other words, increases the diffusion rate of H atoms [62]. It means that the carriers enhance the rate at which H atoms excite from the bond state to the transport state. As it was discussed before, the formation energies of charged defects are given by (3.6) and (3.7). Based on these equations, the position of the Fermi level can affect the H hopping rate. When the carrier density is high (E_F is either close to the conduction band edge or the valence band edge), the energy needed to excite the H atoms into transport states, the hopping energy barrier, is lowered by the energy released from the falling of an electron into or from the dangling bond as the Si-H bond breaks.

The number of band-tail electrons per unit volume n_{BT} is related to the Fermi level by the following equation:

$$n_{BT} = N_c \exp(-(E_C - E_F)/kT), \tag{3.10}$$

where E_C is the conduction band edge, and N_C is the number of states per unit volume within kT of E_C. Since the hopping rate exponentially increases with lowering the energy barrier, this lowering of the energy barrier for hopping is equivalent to a hopping rate proportional to n_{BT} [56].

Finally, the non-exponential (the stretched-exponential which is discussed in the next section) behaviour of the defect creation and annealing has important consequences. The stretched-exponential suggests that there is an approximately exponential energy barrier for the creation and annealing processes. This exponential distribution of energy barriers is not surprising and seems to be the general effect of disorder on the energy level in a-Si (for example, the exponential distribution of band tails). In the next section, the kinetics of defect state creation is discussed by using the aforementioned model.

3.2.1.4 Kinetics of Defect State Creation

The kinetics of defect creation can be explained by the hydrogen-diffusion-mediated equilibration of the Si weak bonds with the defects and band-tail carriers. For a weak Si-Si bond to break and become stabilized, the weak bond must be occupied by an electron, and a H atom must diffuse to the site. The rate of creation is proportional to the density of the weak bonds N_{WB} which is a subset of the tail states, the occupancy of weak bond site by band tail carriers, and the diffusion coefficient of H [51].

In the theory of multiple trapping for trap-limited band transport with the exponential distribution of trap energies, the dispersive diffusion coefficient is given by [66]

$$D(t) = D_{00}(\omega t)^{-\alpha}, \tag{3.11}$$

where D_{00} is the microscopic diffusion, ω is the H attempt frequency, and α is the temperature-dependent dispersion parameter which is given by $\alpha = 1 - \beta = 1 - T/T_0$. The characteristic energy of the exponential distribution of the trapping sites is assumed to be kT_0. Therefore, the rate of change in the density of the dangling bonds $\frac{d\Delta N_{db}}{dt}$ due to positive bias stress can be expressed as

$$\frac{d\Delta N_{db}}{dt} = AN_{WB}\frac{n_{BT}}{N_{BT}}D_{00}(\omega t)^{\beta-1}. \tag{3.12}$$

In equation (3.12) the term $\frac{n_{BT}}{N_{BT}}$ represents the occupancy of weak bond sites by band tail electrons, where N_{BT} is the density of the band tail states, and n_{BT} is the density of the band tail electrons.

The density of the band tail electrons can be expressed in terms of the threshold voltage and gate-source bias stress of the transistor as follows:

$$n_{BT} = C_i(V_{GS} - V_T)/l_D, \tag{3.13}$$

where C_i is the dielectric gate capacitance of the transistor per unit area and l_D is the thickness of accumulation region, assumed to be approximately 2nm [67].

Assuming C_i is constant, the change in the density of the dangling bond defect states is related to the threshold voltage shift of the TFT by the following equation:

$$C_i \Delta V_T = q \Delta N_{db}. \tag{3.14}$$

Substituting (3.13) and (3.14) into (3.12) and solving the subsequent equation, results in the stretched-exponential behaviour for threshold voltage shift of transistor;

$$\Delta V_T(t) = (V_{GS} - V_{T0})\left\{1 - \exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right]\right\}, \tag{3.15}$$

where V_{T0} is the initial threshold voltage of the TFT.

In (3.15), it is essential to note that the time origin of the threshold voltage shift is the moment when the carrier concentration is shifted from its equilibrium value and not from the deposition time or another time reference point. The term τ capsulates the effects of the density of weak bonds, the density of the band tail states, and the diffusion coefficient of H.

$$\tau = \tau_0 \exp(E_\tau / kT), \tag{3.16}$$

where $\tau_0 = 1/\omega$ and

$$E_\tau = kT_0 \ln\left[\frac{\beta N_{BT}}{A \tau_0 N_{WB} D_{00}}\right]. \tag{3.17}$$

For short periods of time and small threshold voltage shifts, (3.15) can be approximated by

$$\Delta V_T(t) = (V_{GS} - V_{T0})\left[\frac{t}{\tau}\right]^{\beta}. \tag{3.18}$$

The published values for β, T_0, τ_0, and E_τ by different researchers for a-Si:H TFTs are summarized in Table (3.1); the variation of reported values may arise from different processes conditions used to fabricate the TFT by different groups.

Table 3.1 Published values in the literature for β, T_0, τ_0, and E_τ

	β	T_0 (K)	τ_0 (s)	E_τ (eV)
Kakalios et al. [60]	.45±.05 at room temp.	600	2×10^{-10}	.95
Powell et al. [51]	.45 (313K) - .65 (373K)	-	-	.9
Jackson et al. [55]	.56 (320K) - .67 (380K)	-	6×10^{-10}	.95
Libsch et al. [50]	.254±0.006 (295K)	$T_0^* = 229K$, $\beta_0 = 1.04$ (T<80ºC)	3.19×10^{-12}	1.17

In the reported values for β and T_0 by Libsch et al., β is related to the temperature by $\beta = T/T_0^* - \beta_0$ rather than $\beta = T/T_0$. In that model, which will be discussed later, the threshold voltage shift is caused by charge trapping in the SiN gate dielectric, not because of the defect state creation in the a-Si:H active layer.

If the charge trapping in the SiN is negligible, the experimental result in Fig. 3.4 can be used to extract the β and τ values at different voltages. The TFT used for bias stress test has an initial threshold voltage of V_{T0} = 1V and an aspect ration (W/L) of 500/100µm. After each bias stress test, the transistor is annealed at 180°C for 1 hour and cooled down to room temperature (293K) at a rate of approximately 1 °C/min. The annealing process retrieves the threshold voltage of TFT within 50mV of its original value. A bias stress test has also been conducted on another sample fabricated using MP5 process (appendix A) with an aspect ratio of 200/200µm and V_{T0} = 4V, resulting in similar value for β and τ. The β value for the TFT with the initial threshold voltage of 1V increases with the applied bias stress voltage from 0.20 to 0.29 which may be due to the effect of charge trapping in the gate dielectric. On the contrary, τ decreases when we increase the stress voltage. For a 10V stress voltage, τ takes the value of 2.1×10^{10} s which decreases to 7.3×10^{7} s for a 50V stress voltage. The decrease in the value of τ, by increasing the stress voltage may be due to the effect of the band tail electrons and lowering the hopping barrier for the H atoms [56] or to the increase in the

charge trapping rate in the SiN gate dielectric. Table (3.2) summarizes the extracted values for β and τ at different bias stress voltages for a TFT with W/L = 500/100μm and $V_{DS} = 0V$ during the application of stress gate voltage.

Table 3.2 Extracted β and τ for a TFT with an initial threshold voltage of V_{T0} = 1V and an aspect ration (W/L) of 500/100μm

V_{ST} (V)	10	15	20	25	35	50
β	0.2	0.23	0.26	0.27	0.29	0.28
τ (s)	2.1×10^{10}	2.5×10^{9}	6.8×10^{8}	3.6×10^{8}	9.3×10^{7}	7.3×10^{7}

The values of β and τ are impacted by the details of the fabrication process and the deposition conditions of the different layers in the a-Si:H TFT. For example, the extracted values for a fabricated TFT with a different fabrication process, W/L = 1000/23μm, gate stress voltage of 20V and V_{T0} = 0 V, are β = 0.38, and $\tau = 5.9\times10^{6}$ s, respectively.

The main difference between the results presented in Tables (3.2) and (3.1) is the kinetics of the instability of TFT. For instance, a bias stress test of 20V for 1.2×10^{4} s, performed in [55] caused, approximately, 4V shift in the threshold voltage, but the total threshold voltage shift of the TFTs used in this work are less than 1V for the same stress time. This can be due to the difference in the fabrication process of TFT and material quality of various layers. Hence, for these small threshold voltage shifts, the effect of charge trapping in SiN may not be negligible, and significantly affects the threshold voltage shift behaviour of TFTs examined in this work.

3.2.2 Charge Trapping in the SiN Gate Dielectric

Charge trapping in the gate dielectric is an alternative mechanism for threshold voltage shift, particularly for a-Si:H TFTs with SiN as the gate dielectric due to prolonged application of bias stress. When a positive voltage is applied to the gate terminal, the electrons located at the a-Si:H/SiN interface inject into trap states, which are usually Si dangling bonds, in the bandgap of the SiN. The trapping of carriers into the gate dielectric does not affect the

subthreshold slope of the TFT. This is also supported by Fig. 3.3. Powel et al. [48] has proposed that charge trapping is the mechanism responsible for the threshold voltage shift of a transistor at high stress voltages. In Fig. 3.9, the threshold voltage shift over time for different bias stress voltages is plotted on linear and logarithmic scales [51].

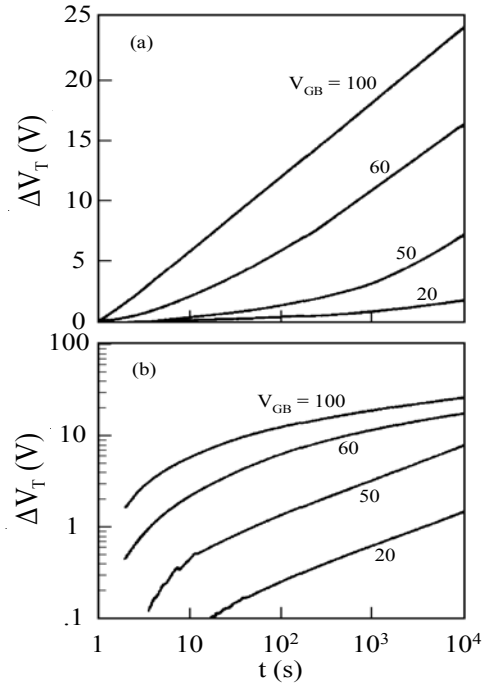

Fig. 3.9 Threshold voltage shift versus time for different stress voltages plotted on (a) a linear scale and (b) a logarithmic scale [51].

It is evident in Fig. 3.9 that for high stress voltages such as 100V, the threshold voltage shift has a logarithmic time dependence (see Fig. 3.9 (a)). Since the charge trapping in the gate dielectric is logarithmic in time [47], $\Delta V_T \propto r_d \log(1+t/t_0)$, it can be concluded that the principal instability mechanism must be charge trapping in the SiN gate dielectric. At low stress voltages and short time periods, the threshold voltage shift is given by a line in the log-log scale in Fig. 3.9 (b), and therefore has a power law time dependence (3.18). Thus, at low bias stresses, state creation is the dominant mechanism for the threshold voltage shift of a TFT.

In addition, the threshold voltage shift of a TFT depends on the SiN composition [48]. Powel et al. report that ΔV_T increases slowly at low bias voltages, but above some critical value V_{GC}

of the bias, ΔV_T increases more rapidly. This critical voltage value depends on the composition of the SiN and increases with the band gap of the SiN gate dielectric. For silicon-rich SiN which has a small bandgap, V_{GC} can be as small as 15-20V, and charge trapping may be the main instability mechanism at low bias voltages.

Libsch et al. [50] has devised a model that is based on charge trapping in SiN. Here, the stretched exponential behaviour of ΔV_T is explained by a multiple trapping model. The injected carriers from the channel first thermalize in the localized band tail states of the a-Si:H/a-SiN_x:H interface and in the a-SiN_x:H layer close to the interface, and then move to the deeper energies in the a-SiN_x:H at longer stress times, larger stress voltages, or higher temperatures. The power parameter of the stretched exponential is modelled by $\beta = T / T_0^* - \beta_0$ for stress temperatures lower than 80ºC, and is temperature independent for temperatures higher than 80ºC. Although this model explains the time dependent behaviour of ΔV_T, it is not consistent with the results of the bias stress test conducted on ambipolar transistors [52][53].

In the following sections, the kinetics of charge trapping in the mono-energetic level and the Gaussian distribution of traps in SiN are modelled. The threshold voltage shift of the TFT, due to charge trapping in both mono-energetic level and Gaussian distribution of SiN traps, is approximated by the suitable logarithmic functions of time.

3.2.2.1 Kinetics of Charge Trapping with Mono-Energetic Level of Traps in SiN Gate Dielectric

The energy-band diagram of the a-Si:H TFT near the interface of the a-Si:H/a-SiN_X:H far away from the source and drain terminals for zero and positive applied gate voltages, are shown in Fig. 3.10. It is assumed that the bulk of the a-Si:H has a potential of zero, and there is no band bending at the interface of the a-Si:H and SiN, when the gate voltage is zero.

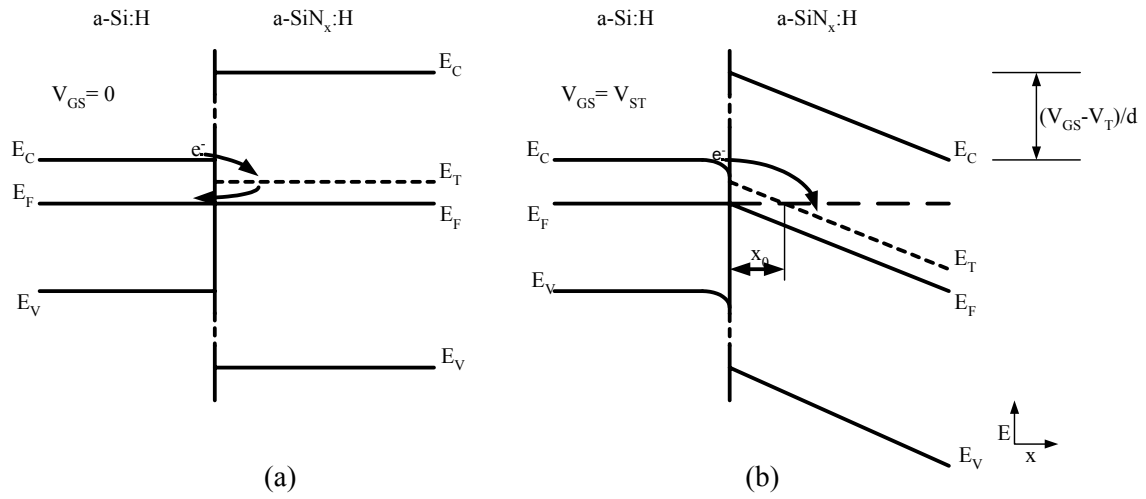

Fig. 3.10 Energy-band diagram of the a-Si:H TFT near the gate dielectric interface for (a) $V_{GS} = 0$ and (b) $V_{GS} = V_{ST}$.

In Fig. 3.10, a simplified mono-energetic level of traps, which is not a function of the position *x*, is assumed inside the SiN gate dielectric. It is believed that these trap states are Si dangling bonds which are formed during the deposition of the SiN layer [68].

When the gate voltage is zero, as in Fig. 3.10 (a), it is obvious that if an electron were to tunnels into a trap state inside the SiN, due to the presence of an empty state above the Fermi level (conduction tail states) the electron will tunnel back to the a-Si:H. When the gate voltage is not zero, the trap level is bent throughout the gate dielectric. In this situation, if an electron tunnels into a SiN trap state distant x_0 (the position, where E_T crosses the Fermi level in the a-Si:H) from the interface, the probability for that electron to return to the a-Si:H is very small due to the small number of empty states with energies lower than the Fermi level of a-Si:H.

A number of charge trapping mechanisms is possible in the presence of a positive gate voltage [47]; namely the Fowler-Nordheim injection, direct tunnelling from the valence band, trap assisted injection, direct or phonon-assisted tunneling from the conduction band, and tunnelling from the filled states in a-Si:H [69]. The first three mechanisms can be ignored, since they usually take place in relatively high electric fields. The last two mechanisms result in a similar equation for the kinetics of charge trapping in SiN and are discussed in this chapter.

To model the time dependence of charge trapping in SiN, the same methodology that is employed by Koelmans et al. is used here [69].

(1) The assumed mono-energetic trap level has a total density of N_{tr} which is position independent and placed E_C - E_T below conduction band of SiN.

(2) The kinetics of charge trapping and de-trapping into and from the states located inside the SiN is given by a Shockley-Read-Hall-like recombination equation.

(3) The trapped electrons in the conduction band tail of the a-Si:H are injected into the SiN gate dielectric.

(4) The tunneling mechanism is accounted for by assuming a capture cross-section $S(x)$ which exponentially decreases with the increased distance from the interface, so that

$$S(x) = S_0 \exp(-ax). \tag{3.19}$$

The decay parameter a is given by [70],

$$a = \frac{2}{\hbar}\sqrt{2m^* E_t\left(1-\frac{Fx}{2E_t}\right)}, \tag{3.20}$$

where m^* , E_t, F, and $\hbar$ are the effective tunnelling mass of the electron, barrier height, electric field inside the insulator, and reduced Plank's constant $\hbar = \frac{h}{2\pi}$, respectively. For the calculation of a in this thesis, it is assumed that $m^* = 0.6m_e$ [71], where m_e is the rest mass of an electron.

(5) The threshold voltage shift is also assumed to be negligible, compared to the applied gate voltage; and the band bending inside the SiN is not affected by the injected electrons.

(6) At room temperature, the redistribution of the trapped electrons inside the SiN after the injection from the a-Si:H is ignored; that is after an electron tunnels into a trap inside SiN, the electron will not tunnel into the adjacent empty traps during the experiment.

According to such assumptions, the kinetics of charge trapping inside the SiN are described by

$$\frac{dn_{tr}(x,t)}{dt} = S(x)\bar{v}[n_t(N_{tr} - n_{tr}(x,t)) - n_{empty}(x)n_{tr}(x,t)], \tag{3.21}$$

where n_t is the density of trapped electrons in the conduction band-tail of a-Si:H at the interface, $n_{tr}(x,t)$ is the concentration of the filled SiN traps, $\bar{v}$ is the thermal velocity of the electrons, and $n_{empty}(x)$ is the concentration of empty states that correspond to the trapped states located at distant x from the interface.

In (3.21), the first and second terms inside the bracket are, respectively, proportional to the rate at which the traps are being filled and emptied.

The position of the quasi-Fermi level of a-Si:H at the interface is written as

$$\psi = \frac{E_F - E_i}{q} = V_{nt} \ln(\frac{n_t}{N_{ti}}), \tag{3.22}$$

where q is the elementary charge, V_{nt} is the characteristic slope of the conduction band-tail, E_i is the intrinsic Fermi level of the a-Si:H, N_{ti} is the density of the trapped electrons when $E_F = E_i$, and n_t is the density of the trapped electrons at the interface [43]. n_t can be alternatively calculated from the applied gate voltage, and for the case of zero source and drain voltages, is given by [43]

$$n_t = \frac{C_i^2 V_i^2}{q\varepsilon\alpha V_{th}}. \tag{3.23}$$

Here, C_i is the gate capacitance per unit area, ε is the a-Si:H dielectric constant, V_{th} is the thermal voltage, α is defined by (2.8), and V_i is the potential drop across the gate dielectric which is given by the difference between the gate voltage and threshold voltage of the TFT, $V_G - V_T$.

The number of empty states depends on the position of the quasi-Fermi level and is written as

$$n_{empty}(x) = n_t \exp\left[\frac{E_T(x) - E_F}{V_{nt}}\right]. \tag{3.24}$$

Here, E_F is the quasi-Fermi level of the a-Si:H, and $E_T(x)$ represents the energy of the traps located at position x from the interface.

$E_T(x)$ can be expressed in terms of the quasi-Fermi level of a-Si:H, the zero bias energy level of the traps E_T, the applied gate voltage, the threshold voltage of the TFT, and the gate dielectric thickness d.

$$E_T(x) = (E_T - E_F) \cdot (\frac{x_0 - x}{x_0}) + E_F, \tag{3.25}$$

where

$$x_0 = d\frac{E_T - E_F}{qV_i} = d\frac{E_T - E_F}{q(V_G - V_T)}. \tag{3.26}$$

By using (3.21)-(3.26), an analytical solution is found for the density of the trapped electrons inside the SiN.

The rearrangement of (3.21) yields

$$\frac{dn_{tr}(x,t)}{dt} + S(x)\bar{v}(n_t + n_{empty}(x))n_{tr}(x,t) = S(x)\bar{v}n_t N_{tr}. \tag{3.27}$$

Since the elements of (3.27) are time independent, except for n_{tr}, the density of the trapped electrons at time t and distance x from the interface is given by

$$n_{tr}(x,t) = \frac{n_t N_{tr}}{n_t + n_{empty}(x)}\left\{1 - \exp\left[-tS_0\bar{v}(n_t + n_{empty}(x))\exp(-ax)\right]\right\}. \tag{3.28}$$

The integration of $n_{tr}(x,t)$ at time t, with respect to x over the dielectric thickness, gives the total number of trapped electrons inside the SiN. As a result, the threshold voltage shift of the TFT, caused by the injected electrons inside the SiN at time t, $\Delta V_T(t)_{trap}$, are expressed in terms of the total trapped electrons and the gate capacitance of the TFT.

$$\Delta V_T(t)_{trap} = \frac{q}{C_i}\int_{x=0}^{d} n_{tr}(x,t)dx \tag{3.29}$$

The integration of (3.29) can be simplified in order to find an approximate closed form equation for the threshold voltage shift of the TFT. By substituting (3.24) and (3.25) into (3.28),

$$\begin{aligned} n_{tr}(x,t) &= \frac{n_t N_{tr}}{n_t + n_{empty}(x)}\left\{1 - \exp\left[-\exp(-a(x - x_{\max}(t))\right]\right\} \\ &= \frac{N_{tr}}{1 + \exp(\frac{(E_T - E_F)}{V_{nt}} \cdot (\frac{x_0 - x}{x_0}))}\left\{1 - \exp\left[-\exp(-a(x - x_{\max}(t))\right]\right\} \end{aligned} \tag{3.30}$$

with

$$x_{\max}(t) = \frac{1}{a}\ln[S_0\bar{v}(n_t + n_{empty}(x))t]$$
$$= \frac{1}{a}\ln\left[S_0\bar{v}n_t(1+\exp\left(\frac{(E_T - E_F)}{V_{nt}}\cdot(\frac{x_0 - x_{\max}(t)}{x_0})\right))t\right]. \quad (3.31)$$

For a long t, the $x_{max}(t)$ increases and the exponential term inside the logarithm can be ignored so that

$$x_{\max}(t) = \frac{1}{a}\ln[S_0\bar{v}n_t t]. \quad (3.32)$$

From (3.30), it is evident that for x, smaller than x_0 and larger than $x_{max}(t)$, the density of the trapped electrons inside the SiN decreases exponentially.

Fig. (3.11) exhibits the concentration of the trapped electrons in the SiN as a function of the distance from the interface after 3.5 hours of a 35V bias stress. N_{tr} and the energy position of the trap levels are revealed by using the threshold voltage relaxation results which are discussed in Chapter 4. The capture cross-section of the traps S_0 is assumed to be 1×10^{-17} cm^2 which is in the range of the values employed in the literature [69][70][72].

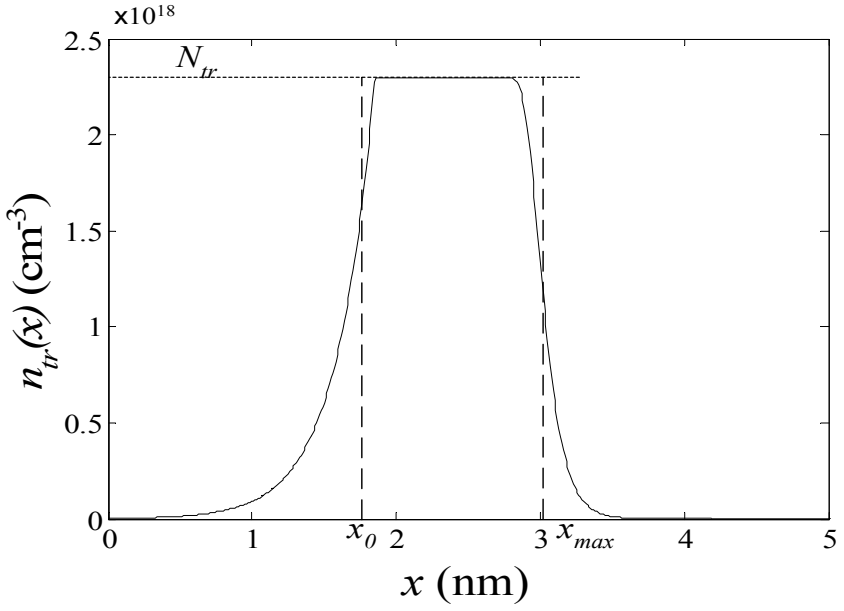

Fig. 3.11 Calculated trapped electron concentration in SiN as a function of the distance from the a-Si:H/a-SiN$_x$:H interface after 3.5 hours of a 35V bias stress using the threshold voltage relaxation results of Chapter 4.

For lengthy stress times when $x_{max}(t)$ is larger than x_0, the trapped charge inside the traps, closer than x_0 and farther than $x_{max}(t)$ from the interface, can be ignored, but not that of trapped between these positions. Consequently, the integration of (3.29) is approximated with

$$\int_{x=0}^{d} n_{tr}(x,t)dx \approx N_{tr}(x_{maz}(t) - x_0) . \tag{3.33}$$

By defining the parameter t_0 as

$$t_0 = \frac{1}{S_0 \bar{v} n_t} \exp(a x_0) \tag{3.34}$$

and by substituting (3.32), (3.33), and (3.34) into (3.29), the threshold voltage shift of the TFT due to charge trapping in SiN is expressed as

$$\Delta V_T(t)_{trap} \approx \frac{q N_{tr}}{a C_i} \ln(\frac{t}{t_0}) \tag{3.35}$$

Based on (3.35), threshold voltage shift of a transistor, caused by the charge injection in the gate dielectric, demonstrates a logarithmic time-dependence. Since the charge trapping and defect state creation occur simultaneously during the bias stress, the experimental results for the threshold voltage shift cannot be used to extract N_{tr} and t_0. The threshold voltage relaxation experiment (discussed in Chapter 4) is employed to extract the different parameters. For example, t_0 for a 35V bias stress is calculated to be approximately 28 ms. N_{tr} and E_t, for the equivalent mono-energetic trap level of SiN (the mono-energetic trap level which gives a result close to the threshold voltage relaxation result (Chapter 4, Fig. 4.13) achieved by using the realistic distribution of traps inside the dielectric) for $V_{GS} = V_{ST} = 35$V are 2.3×10^{18} cm^{-3} and 0.21 eV, respectively. Furthermore, this supports the assumption of the localization of the injected electrons inside trap level of SiN during the application of bias stress. The value of $x_{max}(t)$ after 3.5 hours of a 35V bias stress (Fig. 3.11) is calculated to be 30.5 Å, and the average distance between two traps in SiN is calculated to be 75.7 Å using N_{tr}. From a simple calculation, the time needed for the trap to trap tunnelling is in the order of 10^{25} s which is much longer than the period of the bias stress test experiment.

In the above discussion, the injection of free electrons (conduction band electrons) into the trap states in SiN has been ignored. It is also possible for the free electrons to be trapped inside the dielectric. In fact, the tunnelling parameter a (decay parameter) is smaller for the free electrons, since the barrier height is slightly shorter than that of the trapped electrons

located at the Fermi level of a-Si:H. This reduction in the barrier height is due to the higher energy of the free electrons by approximately 0.2-0.3eV, depending on the applied gate bias. The tunnelling rate can also be higher for free electrons which can be modelled by a larger capture cross-section. This may occur due to the localization of the electrons at the band tail of the a-Si:H which reduces the tunnelling probability of the trapped electrons, compared to that of free electrons.

The effect of the band tail carriers is included in (3.21) by adding an additional term which represents the carrier injection of the free electrons inside the gate dielectric, as follows:

$$\frac{dn_{tr}(x,t)}{dt} = S(x)\bar{v}[(n_t + \eta n_{free})(N_{tr} - n_{tr}(x,t)) - n_{empty}(x)n_{tr}(x,t)], \tag{3.36}$$

where n_{free} is the number of free electrons and η is a dimensionless parameter taking into account the effect of the higher tunnelling rate of the free electrons. Also, it is noteworthy for (3.36), the decay parameter has been assumed to be equal for both the free and trapped electrons. This is a reasonable assumption, since the barrier height in equation (3.20) is roughly 2eV, and a 0.2-0.3eV decrease in the barrier height does not significantly affect *a*.

By using (3.22) and (3.23), the position of the quasi-Fermi level, and as a result, the density of the free electrons is calculated as [43]

$$n_{free} = N_C \exp\left[\frac{(E_F - E_C)}{kT}\right], \tag{3.37}$$

where N_C is the concentration of electrons when $E_F = E_C$, k is the Boltzmanns constant, and T is the temperature. Substituting the typical values of 10^{19} cm^{-3} and 6×10^{13} cm^{-3} for N_C and N_{ti}, respectively [43], and the extracted value of 30 meV for V_{nt} into (3.27) and (3.23) yields 5.2×10^{19} cm^{-3} of trapped electrons and 2.6×10^{15} cm^{-3} of free electrons at V_{GS} = 35V for the TFT with the dielectric thickness of 300nm. Since the density of the free electrons is four to five orders of magnitudes smaller than n_t, the effect of the free electrons can be neglected in (3.36). However, it is possible to find N_{tr} and the corresponding E_t to achieve the same charge trapping result from either the trapped electrons or free electrons. This is due to the fact that neglecting the effect of either n_{free} or n_t does not affect the nature of (3.36), but only changes the extracted values for the density and energy level of the SiN traps. Although, the tunnelling phenomenon most likely occur from both free and trapped electrons; the effect of the trapped electrons may be more pronounced because of the larger density of the trapped

electrons. The next Sections discuss the effect of the Gaussian distribution of the traps inside the SiN for charge trapping, and the resulting threshold voltage shift of the transistor.

3.2.2.2 Kinetics of Charge Trapping with Gaussian Distribution of Traps in SiN Gate Dielectric

The density of gap states in a-SiN_x:H has been calculated by Robertson et al. [68]. A schematic energy distribution of the SiN gap states is depicted in Fig. 3.12 based on calculated energy level of the principal traps: Si (≡Si) and N (=N) dangling bonds, ≡SiH, =NH, and ≡Si-Si≡ defects [68]. The following conclusion is summarized in [68]. ≡SiH and =NH give states which lie outside the gap. The bonding states of ≡Si-Si≡ defects lie 0.1 eV above the valence band, and its antibonding state is in the conduction band. Neutral Si dangling bonds produce gap states with the DOS peak near the midgap. The neutral N dangling bonds produce gap states which peak at the valence band maximum. Since the Si dangling bonds outnumber =N centres, the latter are doubly occupied and negatively charged, some of the ≡Si centres are empty and positive, and others are singly occupied and neutral. Therefore, the position of the Fermi level lies within the ≡Si centres. The density of the dangling bonds depends on the deposition conditions and changes from approximately 10^{17} to 10^{19} cm^{-3} for plasma and chemical vapor deposited films, respectively.

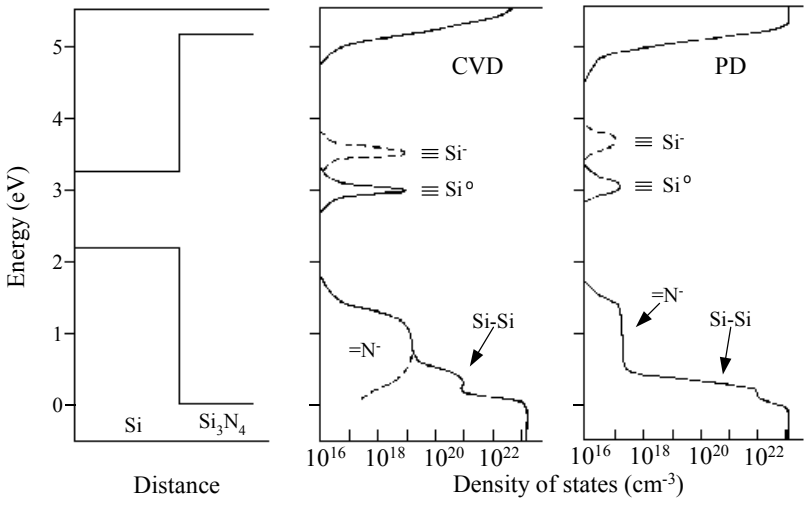

Fig. 3.12 Proposed density of the gap state for CVD and PD deposited a-SiN_x:H [68].

The charge trapping in the gate dielectric at different stress voltages can be explained by using a position independent Gaussian distribution of the SiN traps throughout the gate dielectric with a peak of N_{trm} at the mean value of E_{tm} above the Fermi level and a standard deviation of σ,

$$N'_{tr}(E) = N_{trm} e^{-\left(\frac{E-E_{tm}}{\sigma}\right)^2}. \tag{3.38}$$

$N'_{tr}(E)$ gives the density of the traps per unit energy at an energy level E above the Fermi level of SiN. The kinetics of charge trapping is given by the following rate equation.

$$\frac{dn'_{tr}(x,E,t)}{dt} = S(x)\bar{v}[n_t(N'_{tr}(E) - n'_{tr}(x,E,t)) - n_{empty}(x,E)n'_{tr}(x,E,t)], \tag{3.39}$$

where $n'_{tr}(x,E,t)$ is the concentration of the filled traps per unit energy at time t located at x and the energy level E above the quasi-Fermi level of SiN. $n_{empty}(x,E)$ is the concentration of the empty states in the a-Si:H corresponding to the traps at an energy E and a distance x, $S(x)$ is the position dependent capture cross-section of the trap states, and $\bar{v}$ is the thermal velocity of the electrons. In writing (3.39), the effect of the free electrons, due to their small concentration compared to the band tail trapped electrons n_t has been ignored.

The solution of (3.39) is

$$n'_{tr}(x,E,t) = \frac{n_t N'_{tr}(E)}{n_t + n_{empty}(x,E)}\left\{1 - \exp\left[-tS_0\bar{v}(n_t + n_{empty}(x,E))\exp(-ax)\right]\right\}, \tag{3.40}$$

where

$$n_{empty}(x,E) = n_t \exp\left[\frac{E_T(x,E) - E_F}{V_{nt}}\right] \tag{3.41}$$

with

$$E_T(x,E) = (E - E_F)\cdot\left(\frac{x_0(E) - x}{x_0(E)}\right) + E_F \tag{3.42}$$

and

$$x_0(E) = d\frac{E - E_F}{qV_i} = d\frac{E - E_F}{q(V_G - V_T)}. \tag{3.43}$$

In the above equations, d is the dielectric thickness, E_F is the quasi-Fermi level of the a-Si:H, V_G is the gate bias, and V_T is the threshold voltage of the TFT.

The threshold voltage shift of a TFT at time t, $\Delta V_T(t)_{trap,}$ can be calculated by integrating the density of the trapped electrons over the dielectric thickness and trap energy levels as follows:

$$\Delta V_T(t)_{trap} = \frac{q}{C_i} \int_{E=E_F}^{E_c} \int_{x=0}^{d} n'_{tr}(x,E,t)\,dEdx\,. \tag{3.44}$$

Here, C_i represents the gate dielectric capacitance per unit area, E_F is the Fermi level of SiN and E_C is the SiN conduction band edge.

The profile of the trapped electrons in the SiN, as a function of the distance from the interface after 100, and 10^4 seconds of 15V and 35V bias stresses are exhibited in Fig. 3.13. N_{trm}, E_{tm}, and σ are discovered to be 1.0×10^{19} $eV^{-1}cm^{-3}$, 0.25 eV, and 0.21 eV, respectively, by using the threshold voltage relaxation results of Chapter 4.

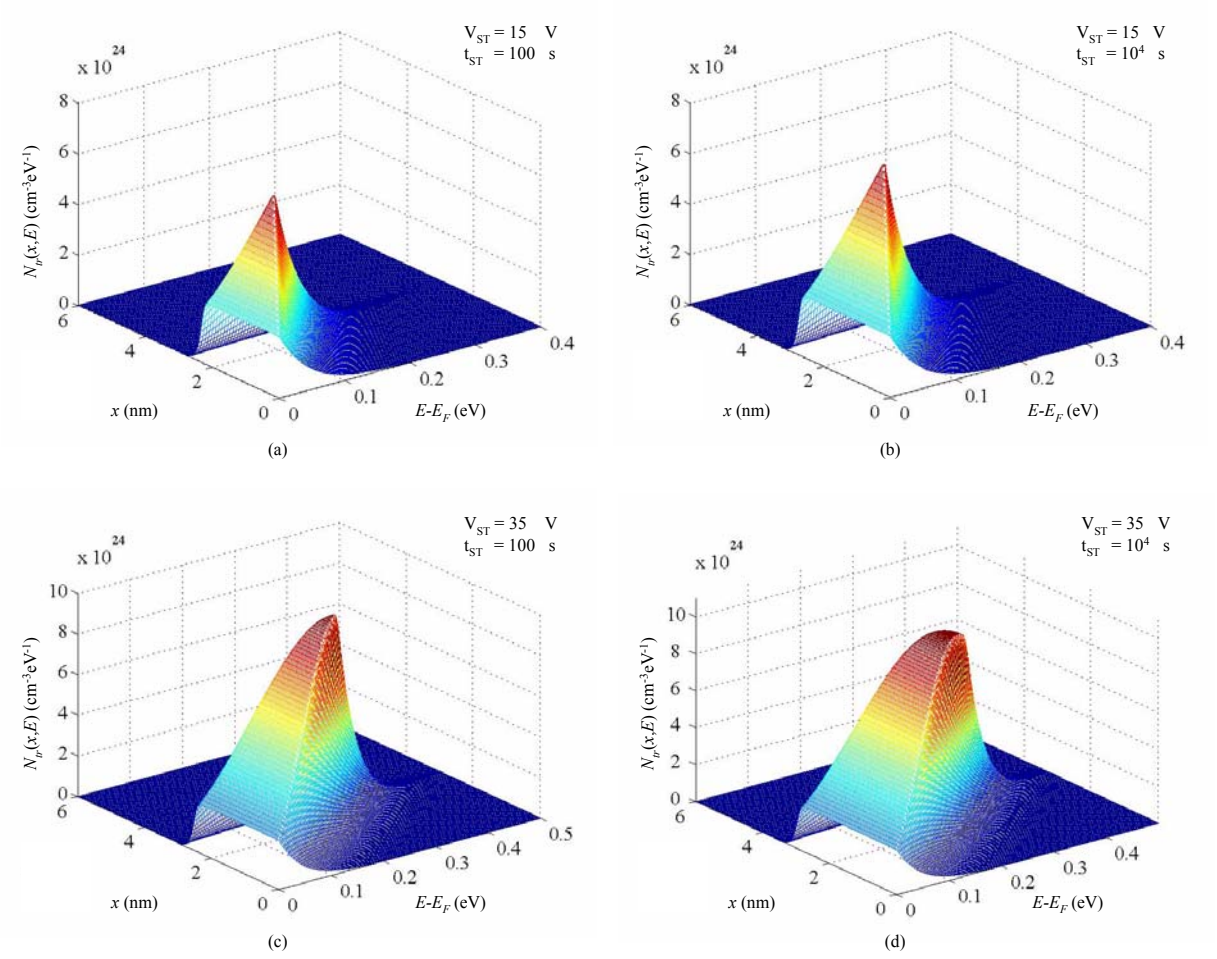

Fig. 3.13 Concentration of trapped electrons in SiN as a function of the distance from a-Si:H interface and energy level of trap states after 100 and 10^4 s of 15 and 35V stresses.

Fig. (3.13) confirms that by increasing the stress voltage, the carriers can trap in higher energy-level SiN traps. The effect of the longer stress times is the trapping of the electrons in farther states from interface and is the increasing of $x_{max}(t)$. From (3.32), it is easy to find out that for long stress times, $x_{max}(t)$ becomes virtually independent of the energy level of the traps and is mostly affected by the bias stress time (compare Fig. 3.13 (a) with (c), and (b) with (d)).

Equation (3.29) is simplified by the method described in the last section. The total charge per unit energy, trapped at any energy level of the SiN, can be approximated by

$$\begin{aligned} Q'(E,t)_{trap} &= q\int_{x=0}^{d} n'_{tr}(x,E,t)dx \\ &\approx \frac{qN'_{tr}(E)}{a}\ln(\frac{t}{t_0(E)}) \end{aligned} \tag{3.45}$$

where

$$t_0(E) = \frac{1}{S_0\bar{v}n_t}\exp[ax_0(E)] = \frac{1}{S_0\bar{v}n_t}\exp[\frac{ad}{q(V_G - V_T)}(E - E_F)]. \tag{3.46}$$

Here, V_G, V_T, d, S_0, $\bar{v}$, n_t, E_F, a, and $N'_{tr}(E)$ are the gate stress voltage, threshold voltage of a TFT, dielectric thickness, capture cross-section at the interface, thermal velocity of electrons, concentration of trapped band tail electrons at the interface, quasi Fermi level of a-Si:H, tunnelling parameter, and concentration of the trap states per unit energy at the energy level E above the SiN Fermi level, respectively.

For (3.45), it is assumed that the tunnelling parameter a is not affected significantly by distance. This is a reasonable assumption, if the barrier height is high and the applied field is small. Based on (3.20), a(x) shows only a 10% change over a 60Å distance from the interface. Furthermore, the applied gate voltage is much larger than the threshold voltage of a TFT; therefore, a change in the threshold voltage does not affect the value of V_G - V_T significantly. The integration of (3.45) over the SiN energy levels gives the threshold voltage shift of the TFT as follows:

$$\begin{aligned} \Delta V_T(t)_{trap} &= \frac{1}{C_i}\int_{E=E_F}^{E_{up}(t)} Q'(E,t)_{trap}\,dE \\ &\approx \frac{q}{aC_i}\int_{E=E_F}^{E_{up}(t)} N'_{tr}(E)\ln(\frac{t}{t_0(E)})dE \end{aligned} \tag{3.47}$$

However, care must be taken in choosing the upper limit of the integral $E_{up}(t)$. Since (3.45) is valid only when t is larger than $t_0(E)$, it can be assumed that there is no significant trapped charge in the states whose $t_0(E) > t$. Thus, the upper limit of the integral becomes

$$E_{up}(t) = E_F + \frac{q(V_G - V_T)}{ad} \ln(S_0 \bar{v} n_t t) . \tag{3.48}$$

Substituting (3.48) and (3.37) into (3.47) and setting $E_F = 0$ yield

$$\Delta V_T(t)_{trap} = A(t)\ln(t) + B(t) , \tag{3.49}$$

where

$$A(t) = \frac{qN_{trm}}{aC_i} \int_0^{E_{up}(t)} e^{-\left(\frac{E-E_{tm}}{\sigma}\right)^2} dE \, ^* \tag{3.50}$$

and

$$\begin{aligned} B(t) = -\{ & \frac{qdN_{trm}}{C_i(V_G - V_t)} \left[\frac{\sigma^2}{2} \left(e^{-\left(\frac{E_{tm}(t)}{\sigma}\right)^2} - e^{-\left(\frac{E_{up}(t)-E_{tm}}{\sigma}\right)^2} \right) + E_{tm} \int_0^{E_{up}(t)} e^{-\left(\frac{E-E_{tm}}{\sigma}\right)^2} dE \right] \\ & + \frac{qN_{trm}}{aC_i} \ln\left(\frac{1}{s_0 \bar{v} n_t}\right) \int_0^{E_{up}(t)} e^{-\left(\frac{E-E_{tm}}{\sigma}\right)^2} dE \} \end{aligned} \tag{3.51}$$

$A(t)$ and $B(t)$ are presented in Fig. (3.14) for a 15V bias stress and with trap density parameters used for the calculation of Fig. (3.13).

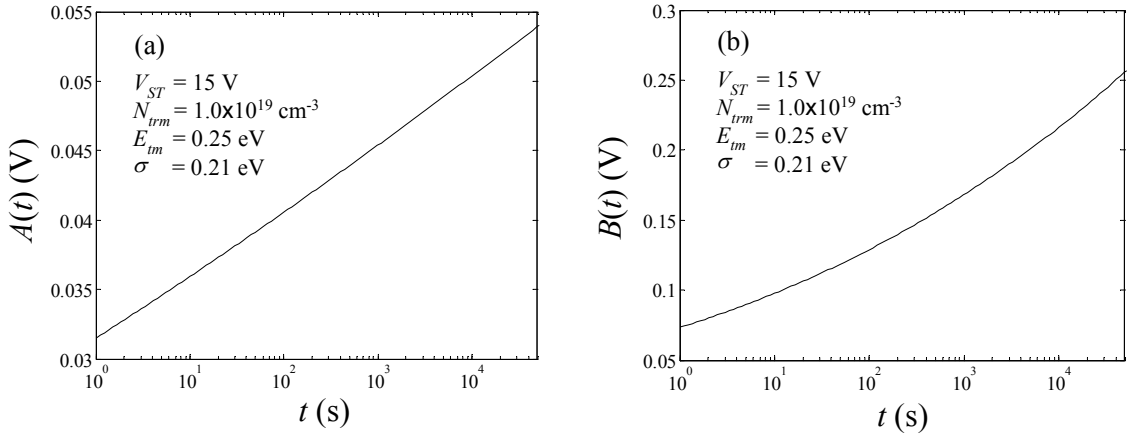

Fig. 3.14 Calculated (a) $A(t)$ and (b) $B(t)$ using (3.50) and (3.51), respectively, for a 15V bias stress.

* Note that N_{trm} is the peak concentration of the Gaussian distribution of traps in SiN per unit volume per eV.

In Fig. 3.15 plots of the threshold voltage shift of a TFT due to the charge trapping in the SiN by using (3.49) (dashed line), the numerical integration of (3.44) (solid line), and the experimental results for the total threshold voltage shift of the TFT under a 15V gate bias stress (open circles) are shown.

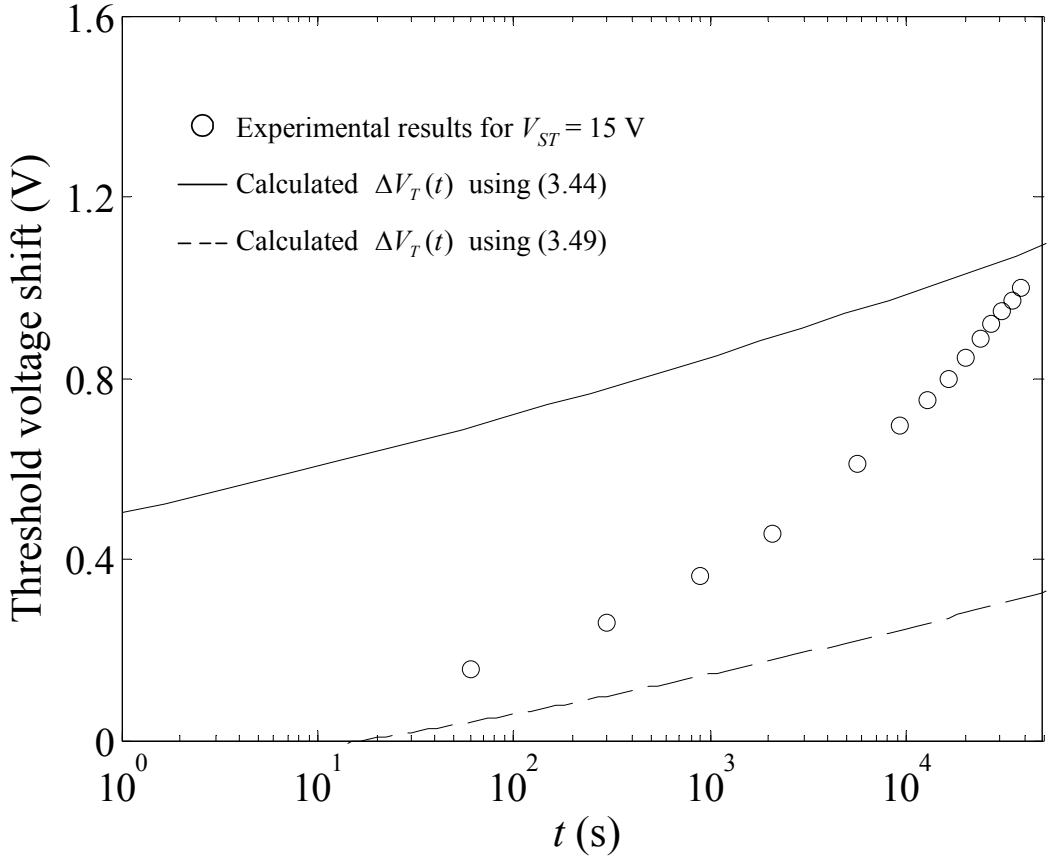

Fig. 3.15 Calculated threshold voltage shift using (3.49) (dashed line) and (3.44) (solid line); the experimental results of $\Delta V_T(t)$ due to a 15 V bias stress are also shown (open circles).

From Fig. 3.15, it can be seen that the estimated threshold voltage shift due to the charge trapping in short periods of time exceeds the total threshold voltage shift which has been experimentally measured. This occurs because of the effect of measuring the transfer characteristics of the TFT in order to extract the threshold voltage shift of the transistor. During the $I_D - V_{GS}$ sweep, a portion of the trapped charge is released which decreases the amount of the threshold voltage shift of the TFT. In Chapter 4, it is demonstrated that the

amount of released charge after the termination of the bias stress depends on the Fermi level of the a-Si:H, and is affected by the kinetics of the defect state creation. Since the effect of the defect state creation and charge trapping cannot be found separately by using bias stress experiment, the position of the quasi Fermi level is not known during the bias stress; therefore, the amount of released charge is difficult to calculate during the $I_D - V_{GS}$ sweep. Furthermore, the threshold voltage shift, which has been calculated by (3.49), is considerably smaller than the numerical integration of (3.44). This results from neglecting the effect of the trapped carriers closer than $x_0(E)$ or farther than $x_{max}(t)$ to/from the interface in (3.47). However, it is obvious that the numerical results have a logarithmic time dependence which can be modelled by an equation like (3.49).

3.3 Summary

In this chapter, the threshold voltage shift of transistors due to bias stress has been reviewed. The mechanisms responsible for this shift are the defect state creation and the charge trapping in the SiN. To explain the energy level of the created extra defect states in the band gap of a-Si:H, the defect pool model has been described. Based on this model, application of a positive gate voltage produces extra defect states in the lower half of the band gap. The H atoms and band tail carriers play important roles in the kinetics of the defect state creation. The kinetics of defect state creation has been explained by hydrogen-diffusion-mediated equilibration of the Si weak bonds with defect and band tail carriers. Finally, the charge trapping of carriers inside the SiN has been reviewed, and the kinetics of charge trapping in both the mono-energetic and Gaussian distribution of traps in the SiN has been modeled by a Shockley-Read-Hall-like recombination equation.

Chapter 4

Relaxation of Threshold Voltage after Removing the Bias Stress

Following the termination of the gate bias stress of a a-Si:H TFT, its threshold voltage eventually returns to its original value. This phenomenon is called the relaxation of the threshold voltage. Although, the threshold voltage shift of a TFT under prolonged bias stress has been extensively investigated by numerous researchers, the relaxation of the threshold voltage has been studied only by a few authors [55][56]. An in depth study of the relaxation phenomenon provides additional information about the kinetics of the charge injection from the a-Si:H to the SiN, and the trap density of the SiN near the interface with a-Si:H. Moreover, this study facilitates quantitatively distinguishing between the different instability mechanisms of a-Si:H TFTs. In this chapter, the underlying mechanisms for the relaxation of

a-Si:H threshold voltage is reviewed, and the time dependence of the threshold voltage relaxation is modelled.

4.1 Relaxation of Threshold Voltage after Removing the Positive Bias Stress

To measure the threshold voltage relaxation of a TFT, after the removal of the bias stress, the experimental setup in Fig. (3.1) is employed. Following the positive bias stress test and by using Keitley SMUs, V_{GS} and V_{DS} were set to zero at room temperature. At certain times, which are shown in Fig. 4.3, the transfer characteristics (I_D -V_G) of the TFT were measured by using the Keithley SMU 236 parameter analyzer at V_D = 15V for -5V ≤ V_G ≤ 15V with 0.25V step. The TFTs were fabricated using MP5 and MP6 processes explained in appendix A and the bias stress test was explained in Section 3.1.

The transfer characteristics of a TFT after $t = 0$, 6×10^2 and 1.26×10^4 seconds of removing the bias stress for a sample which was under a 20V bias stress for 3.5 hours are shown in Fig 4.1. The TFT were fabricated using MP6 process and has an aspect ratio of W/L = 500/100 μm. It is obvious that the transfer characteristics shift to lower positive gate-source voltages by increasing the relaxation time.

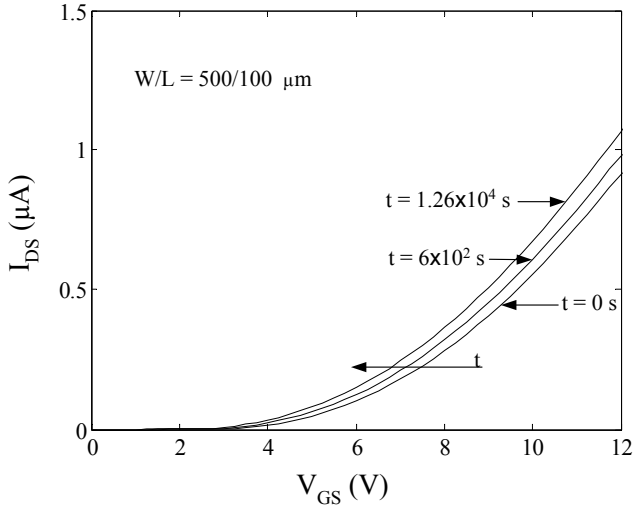

Fig. 4.1 Transfer characteristics of a TFT at different times after removing the 20V bias stress (the aspect ratio of TFT is W/L = 500/100 μm).

In order to study the effect of relaxation on the subthreshold region of operation, the transfer characteristics of Fig. (4.1) are plotted on a semi-logarithmic scale in Fig. 4.2.

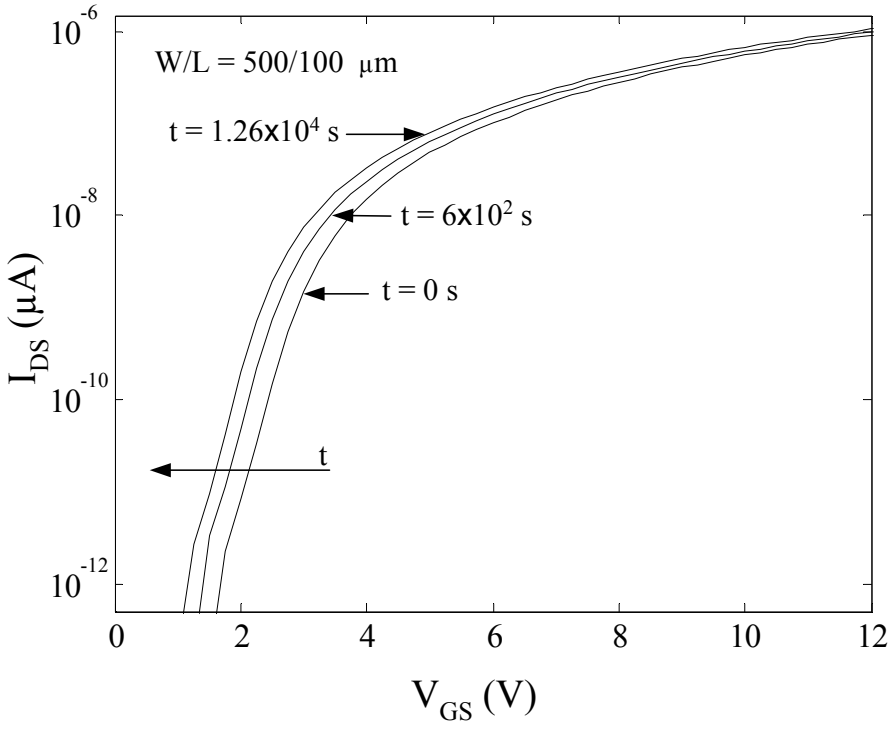

Fig. 4.2 I-V characteristics of a TFT plotted on a semi-logarithmic scale after t = 0, 6×10^2, and 1.26×10^4 seconds of removing the 20V gate bias stress.

In Fig. 4.2, it can be easily seen that, although the transfer characteristics are moved to lower gate voltages over time, the subthreshold slope (dV_{GS} /d $\log_{10}$ I_{DS}) does not change significantly, when the relaxation time is increased. The subthreshold slope is also studied after the removal of bias stresses with higher stress voltages and longer stress times. The subthreshold slope does not change significantly during the relaxation of the threshold voltage, after the bias stresses as high as 35V and the stress times more than 50 hours are withdrawn.

By the extraction method described in Chapter 2.4, the threshold voltage of the TFT was extracted from the measured transfer characteristics. This is plotted in Fig. 4.3(a) as a function of time. In Fig. 4.3(b), the time dependence of the threshold voltage relaxation (ΔV_T = $V_T(t_{ST})$-$V_T(t_{relax})$) is plotted after the removal of bias stresses such as 10, 15, 20, 25, 35, and 50 V applied to the gate with V_{DS} = 0 and t_{ST} = 3.5 hours (t_{ST} =1.26×10^4 seconds). The tested

transistor has a W/L = 500/100 μm and an initial threshold voltage (V_{T0}) of 1.0 ± 0.05 V for each bias stress-relaxation experiment.

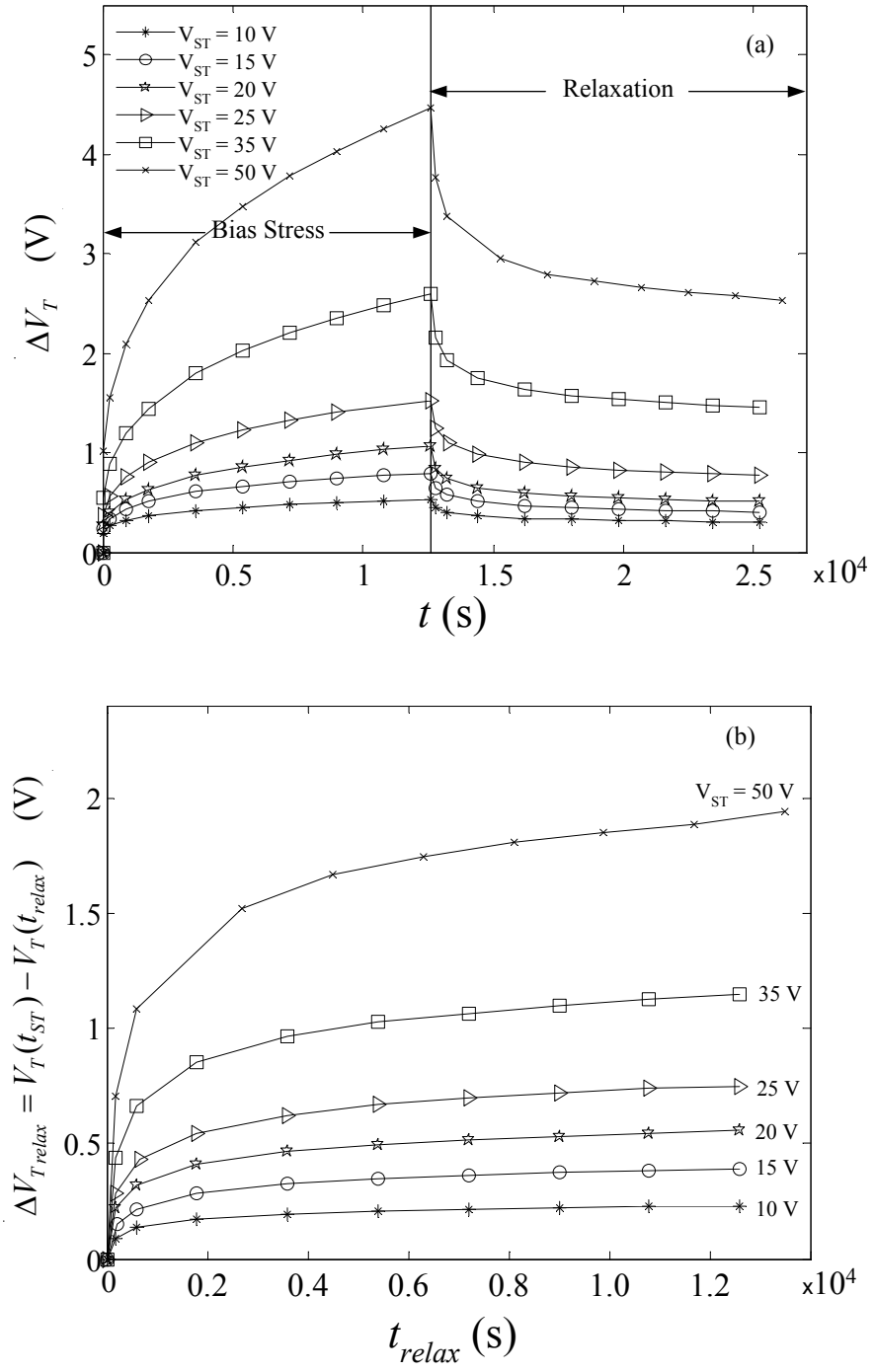

Fig. 4.3 (a) Threshold voltage shift as a function of time for different bias stresses and (b) relaxation of threshold voltage after 3.5 hours of bias stress at different gate voltages.

The relaxation of the threshold voltage (ΔV_T) of a TFT, as a function of the effective stress voltage (V_{ST} - V_{T0}) after $t_{relax} = 1.26\times10^4$ seconds of the termination of bias stress is portrayed in Fig. 4.4. The stress time for the bias stress experiment is $t_{ST} = 1.26\times10^4$ s. V_{T0} and V_{ST} are the initial threshold voltages of the TFT (~ 1.0V) and the gate stress voltage, respectively. It is evident in Fig. 4.4 that ΔV_T almost increases with V_{ST} - V_{T0}, somewhat linearly except at the highest stress voltage.

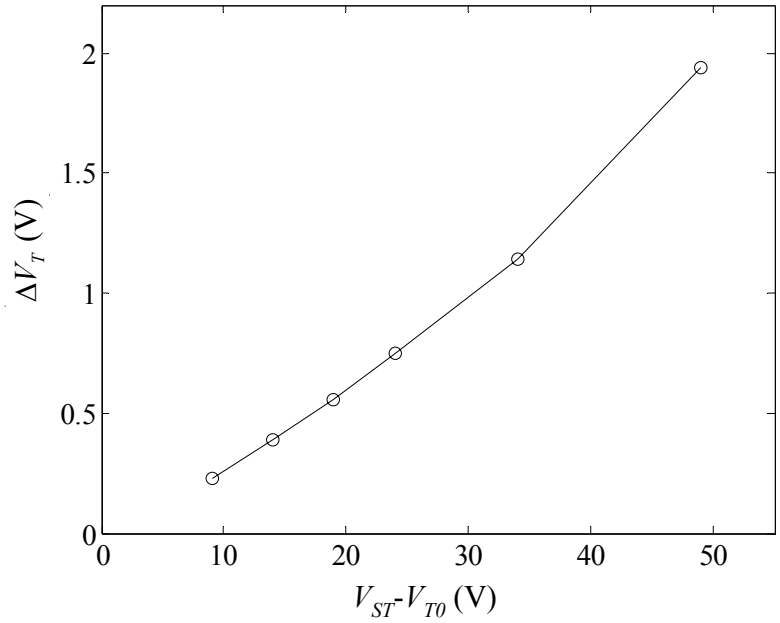

Fig. 4.4 Threshold voltage relaxation as a function of V_{ST} - V_{T0} after $t_{relax} = 1.26\times10^4$ seconds of removing the bias stress ($t_{ST} = t_{relax}$).

4.2 Mechanisms Responsible for the Relaxation of Threshold Voltage after Removing the Gate Bias Stress

The relaxation of threshold voltage, discussed in the literature [50][56], has been attributed to two mechanisms: the annealing of the extra defect states in the a-Si:H layer close to the interface created during the application of bias stress prior to relaxation, and the de-trapping of the injected carriers into SiN gate dielectric. Since it is widely accepted that defect state creation and charge trapping in SiN occur simultaneously during the application of the gate

bias stress [51][52][53], the reverse phenomena must also occur concurrently after the bias stress is removed. A study of these phenomena indicates that the mechanisms have different kinetics which can be used to quantitatively distinguish between them.

In the following sections, the kinetics of defect state annealing are reviewed and compared with my experimental results shown in Fig. 4.3. The time behaviour of charge de-trapping from filled states in the SiN is also modelled for two cases of de-trapping from the mono-energetic level and the Gaussian distribution of traps in SiN.

4.2.1 Defect State Annealing

The defect annealing process and its kinetics can be explained by a dispersive diffusion of H [56]. According to the diffusion-mediated metastable changes model, when an H atom diffuses towards a defect, the defect can be annealed. The possible mechanisms for this are (1) the reverse of the reaction happens during the defect creation explained in Chapter 3; however, the paths of diffusion may not be the same, or (2) involvment of another H atom. The energy barrier or hopping rate for defect annealing is not necessarily equal to the corresponding value for the defect creation. This may occur because (1) the network may relax after defect creation; therefore, the energy barrier changes; (2) the defect annealing can happen by involving a different H atom with a different energy barrier; and (3) defect annealing and creation may occur through different diffusion paths.

In the annealing experiments, when the bias is removed, the negatively charged defects in the lower half of the band-gap lose their electrons quickly, like in a fraction of a second [73]. The band tail carrier density drops to even smaller values than the intrinsic a-Si:H due to the lowering of the Fermi level by the extra defects created during the bias stress. Since n_{BT} is small, the H diffusion becomes equal to the H diffusion in undoped a-Si:H. Furthermore, the kinetics of defect annealing is almost independent of the number of band tail electrons. This is because of the existence of higher density of the defect states than the number of band tail electrons. The time dependence of the annealing process is found by solving the following equation:

$$\frac{d\Delta N_{db}(t)}{dt} = -D_{\min}(\omega t)^{-\alpha}(B\Delta N_{db}(t)), \tag{4.1}$$

where D_{min} is the H diffusion coefficient in undoped a-Si:H, ΔN_{db} is the density of the extra defect states, ω is the H attempt frequency, B is the proportionality constant, α is the temperature-dependent dispersion parameter which is given by $\alpha = 1 - \beta = 1 - T/T_0$, and T_0 is the characteristic temperature of the exponential distribution of the trapping sites.

The number of extra defect states is given by

$$\Delta N_{db}(t) = N_{db}(t) - N_{db0}. \tag{4.2}$$

Here, N_{db0} is the equilibrium density of the defect states.

The threshold voltage shift can be found from the change in the density of the defect states ΔN_{db}, the gate capacitance of the TFT per unit area C_i, and the elementary charge q,

$$C_i \Delta V_T = q\Delta N_{db}. \tag{4.3}$$

Substituting (4.3) into (4.1) and solving the resultant first order differential equation yields the relaxation of the threshold voltage as a function of time. This is expressed as

$$\Delta V_{T\,relax}(t) = (V_T(t_{stress}) - V_{T0})\left\{1 - \exp\left[-\left(\frac{t}{\tau_a}\right)^{\beta}\right]\right\} \tag{4.4}$$

with

$$\tau_a = \tau_0 \exp(E_\tau / kT) \tag{4.5}$$

and

$$E_\tau = kT_0 \ln\left[\frac{\beta}{B\tau_0 D_{\min}}\right]. \tag{4.6}$$

Here $\tau_0 = 1/\omega$ and $\Delta V_{T\,relax}(t) = V_T(t) - V_T(t_{ST})$.

It is expected that the defect annealing rate will be slower than the defect creation rate, since the number of band tail carriers are very small, and the H diffusion in a-Si:H is very slow. Besides, the time constant is slightly defect density dependent due to the lower annealing barrier in a higher-defect-density material [56].

The activation energy E_τ for the annealing of the defect states (the defect removal process), and an attempt to escape frequency τ_0^{-1} have been reported to be 1.5 eV [74] (1.27 eV [56]), and in the order of 10^{13} Hz [74], respectively.

The time constants τ for the annealing and the creation (generation) mechanisms, which have been extracted from a least-square fit of (4.4) to the experimental data, are shown in Fig. 4.5 [56].

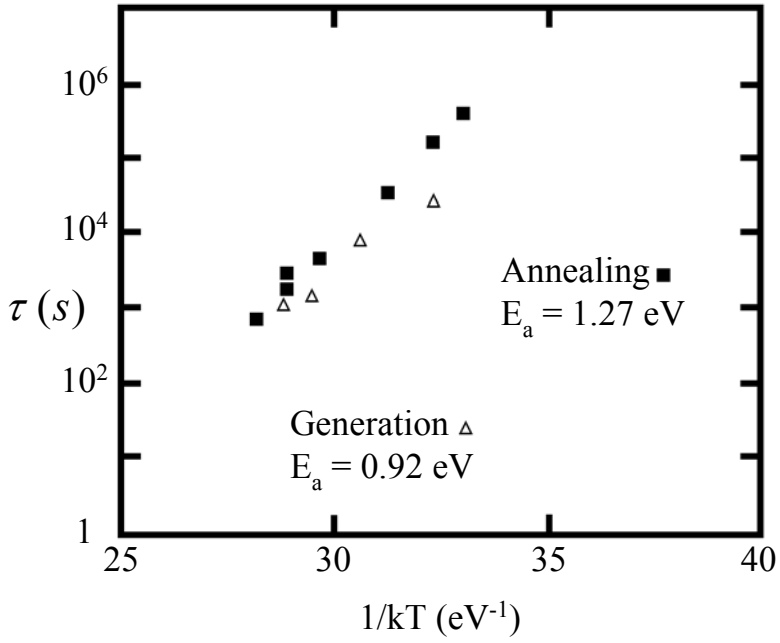

Fig. 4.5 τ for the annealing and creation mechanisms as a function of $1/kT$ [56].

In Fig. 4.5, the expected τ for the annealing at room temperature is in the order of 10^8 s. The extracted parameter for β and τ for the experimental results of Fig. 4.3(b) is given in Table 4.1.

Table 4.1 Extracted β and τ for a TFT with W/L = 500/100μm which had been under t_{ST} = 3.5 hours of bias stress at different stress voltages V_{ST}; $\Delta V_T(t_{ST})$ is the total threshold voltage shift at the end of the bias stress period.

V_{ST} (V)	10	15	20	25	35	50
β	0.25	0.27	0.26	0.26	0.24	0.25
τ (s)	4.1×10^4	3.1×10^4	3.5×10^4	4.8×10^4	1.0×10^5	1.2×10^5
$\Delta V_T(t_{ST})$ (V)	0.44	0.74	1.06	1.52	2.60	4.47

Table 4.1 conveys that, τ increases with the density of defect states in the material (increasing $\Delta V_T(t_{ST})$). Furthermore, the value of τ for the defect removal is approximately six orders of

magnitude smaller than the corresponding parameter for defect creation. This is not supported by the aforementioned model, since the H diffusion increases with the concentration of band tail electrons. Consequently, τ must be larger for the defect annealing than for the defect creation process.

Even if the same parameters for the defect annealing as in Table 3.2 are adopted, which are extracted by neglecting the effect of charge trapping on the threshold voltage shift of the TFT, the amount of threshold voltage relaxation cannot exceed 0.02, 0.04, 0.06, 0.1, 0.2 and 0.4 V after 3.5 hours of relaxation following the 10, 15, 20, 25, 35, and 50V bias stress experiments of Fig. 4.3(a), respectively. Therefore, it is concluded that the relaxation in the threshold voltage of a TFT, plotted in Fig 4.3(b), is not related to the defect annealing mechanism but mostly comes from the de-trapping the injected electrons into the SiN gate dielectric. This may be the result of higher stability of the a-Si:H active layer of the TFTs employed in this work.

4.2.2 Charge De-trapping of the Injected Carriers into SiN

The charge de-trapping or the charge back tunnelling had been proposed as a source of error in the experimental results of threshold voltage shift, when the bias was removed to measure the TFTs I-V characteristics [50]. This mechanism may also be responsible for the relaxation of threshold voltage shift after the bias stress is removed. Although the kinetics of the charge trapping in the gate dielectric has been investigated in the literature, the time dependence of the charge de-trapping has not been studied for the relaxation of the threshold voltage at room temperature.

The relaxation results, in Fig. 4.3(b), are not consistent with the defect state creation mechanism (Section 4.2.1), possibly due to the charge de-trapping of the injected carriers into the SiN. In the next few sections, kinetics of the charge de-trapping from the mono-energetic level and the Gaussian distributed SiN traps are modelled. The simulation results in both cases are in good agreement with the experimental results. Furthermore by using the threshold voltage relaxation results of Fig. 4.3 (b), the density of SiN traps as a function of the energy can be determined.

4.2.2.1 Charge De-trapping from the Mono-Energetic Level of Traps in SiN

After the removal of the gate bias, the energy level of traps in the SiN which had been bent during the bias stress straightens, if the threshold voltage shift is small. In this situation, the trapped electrons, which have been energetically below the quasi-Fermi level of the a-Si during the bias stress, are now placed above the a-Si:H Fermi level. Since the states above the Fermi level of a-Si:H are empty, the injected electrons tunnel back to the a-Si:H over time. Fig. 4.6 illustrates the energy-band diagram of a a-Si:H TFT near the interface of a-Si:H/a-SiN_X:H away from the source and drain terminals, when the gate voltage is removed. It is assumed that the bulk of the a-Si:H has a potential of zero, and the band bending at the interface of the a-Si:H and SiN is negligible for a zero gate voltage. In Section 3.2.2.1, it was shown that the distribution of trapped electrons at time t after the application of bias stress can be approximated to be zero for $x < x_0$ and $x > x_{max}(t)$ from the interface, and will be completely full between x_0 and $x_{max}(t)$.

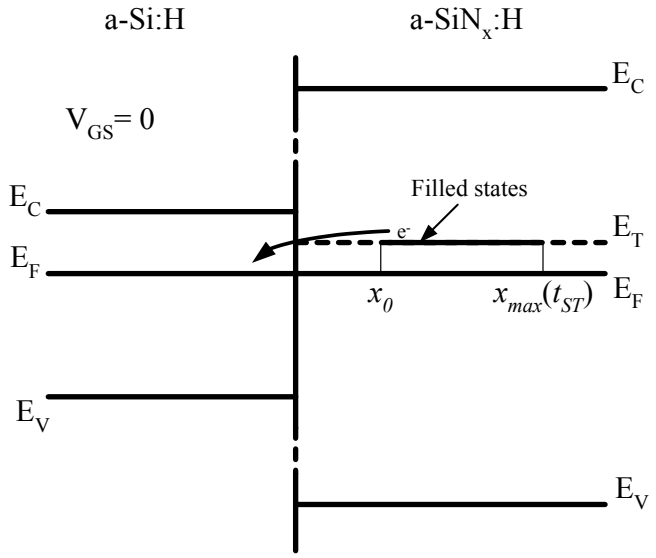

Fig. 4.6 Energy-band diagram of the a-Si:H TFT near the gate dielectric interface after the removal of the bias stress for $t = t_{ST}$.

The quantities x_0 and $x_{max}(t)$ are given by (3.26) and (3.31), respectively. The parameter x_0 depends on the applied gate voltage V_G, threshold voltage V_T, energy level of the traps E_T, and the dielectric thickness d. The parameter $x_{max}(t)$ is related to the density of the trapped

electrons in the band tail of the a-Si:H n_t, thermal velocity of the electrons $\bar{v}$, capture cross-section of the SiN traps S_0, tunnelling parameter a, and bias stress time t_{ST}.

The kinetics of charge de-trapping can be explained by a Shockley-Read-Hall-like recombination equation. Similar to the method in Section 3.2.2.1 for the charge trapping of electrons inside the SiN, the tunnelling mechanism is taken into account by assuming an electron capture cross-section $S(x)$ for the states in the conduction band tail of the a-Si:H. $S(x)$ exponentially decreases for the trapped electrons inside the SiN with the increasing distance from the interface. It is

$$S(x) = S_0 \exp(-ax). \tag{4.7}$$

Since the electric field in the gate dielectric is negligible after the bias stress is withdrawn, the tunnelling parameter is reduced to

$$a = \frac{2}{\hbar}\sqrt{2m^*(E_C - E_T)}, \tag{4.8}$$

where m^*, E_C, and $\hbar$ are the effective mass of the electrons, energy level of the conduction band above the Fermi level, and reduced Plank's constant, $\hbar = \frac{h}{2\pi}$, respectively. From Fig. 4.5 it is evident that $E_C - E_T$ is the energy barrier of electrons tunnelling from the SiN into the a-Si:H layer.

Because the concentration of electrons above the Fermi level of a-Si:H is very small in the absence of a gate bias, the injection of electrons into the SiN can be neglected. This simplifies (3.21) to

$$\frac{dn_{tr}(x,t_r)}{dt} = -S(x)\bar{v}n_{empty}n_{tr}(x,t_r), \tag{4.9}$$

where t_r is the relaxation time after the removal of the bias stress, $n_{tr}(x,t_r)$ is the concentration of the filled SiN traps at time t_r and at a distance x from the interface, $\bar{v}$ is the thermal velocity of the electrons, and n_{empty} is the concentration of the empty states at the energy level E_T above the a-Si:H Fermi level.

The number of empty states is represented by

$$n_{empty} = N_{ti}\exp\left[\frac{E_T - E_F}{V_{nt}}\right], \tag{4.10}$$

where N_{ti} is the density of the trapped electrons when $E_F = E_i$.

The solution of (4.9) gives the number of trapped electrons as a function of the relaxation time t_r and position x such that

$$n_{tr}(x,t_r) = n_{tr}(x,t_{ST}) \exp\{-S_0 \bar{v} n_{empty} t_r \exp(-ax)\} . \quad (4.11)$$

$n_{tr}(x,t_{ST})$ is the initial concentration of the trapped electrons inside the SiN at the end of the bias stress. By substituting

$$x_{relax}(t_r) = \frac{1}{a} \ln[S_0 \bar{v} n_{empty} t_r] \quad (4.12)$$

into (4.11), the density of the trapped electrons as a function of the distance from the interface is written as

$$n_{tr}(x,t_r) = n_{tr}(x,t_{ST}) \exp\{-\exp[-a(x - x_{relax}(t_r))]\}. \quad (4.13)$$

Thus, the number of electrons which has tunnelled back into the a-Si:H by the time t_r is expressed by

$$n_{relax}(x,t_r) = n_{tr}(x,t_{ST})(1 - \exp\{-\exp[-a(x - x_{relax}(t_r))]\}). \quad (4.14)$$

The integration of (4.14) over the dielectric thickness gives the total relaxed charge at t_r, $Q_{relax}(t_r)$, and is proportional to the threshold voltage relaxation, expressed by

$$\Delta V_{T\,relax}(t_r) = \frac{Q_{relax}(t_r)}{C_i} = \frac{q}{C_i} \int_{x=0}^{d} n_{relax}(x,t_r) dx . \quad (4.15)$$

By using the parameters in Table 4.2 for charge trapping and de-trapping, the simulation results are in good agreement with the experimental results of the threshold voltage relaxation as presented in Fig. 4.7. The electron capture cross-section of the band tail states of a-Si:H, S_0, is assumed to be 10^{-15} cm^2 [8]. It is very important to note that sensitivity analyses are needed to find out the sensitivity of (4.13)-(4.15) to the parameters such as a and S_0 which will be done in the future.

Table 4.2 Concentration N_{tr} and energy level E_T of the mono-energetic SiN traps which are used for the charge trapping and de-trapping simulations; N_{ti} is the assumed DOS at the Fermi level of a-Si:H after 3.5 hours of bias stress with V_{ST}.

V_{ST} (V)	10	15	20	25	35	50
N_{tr} (cm^{-3})	4.3×10^{17}	8×10^{17}	1.15×10^{18}	1.6×10^{18}	2.3×10^{18}	3.7×10^{18}
E_T (eV)	0.05	0.08	0.12	0.16	0.21	0.3
N_{ti} (cm^{-3}eV^{-1})	5×10^{13}	4×10^{13}	2×10^{13}	8×10^{12}	5×10^{11}	5×10^{10}

By increasing the bias stress, the total threshold voltage shift, and as a result, the number of defect states in the lower half of the band gap, increases which shifts the quasi Fermi level towards the midgap. Hence, the DOS at the quasi Fermi level is decreased by increasing the bias stress voltage. Also, for the calculation of the threshold voltage relaxation, the effect of the electrons which are relaxed for 10s after the termination of the bias stress must be neglected. This is due to the 30s time needed to measure the I-V characteristics to extract the V_T of the TFT. For charge de-trapping simulations, it is assumed that the annealing of the defect states is negligible and the position of the quasi Fermi level does not change during the experiment.

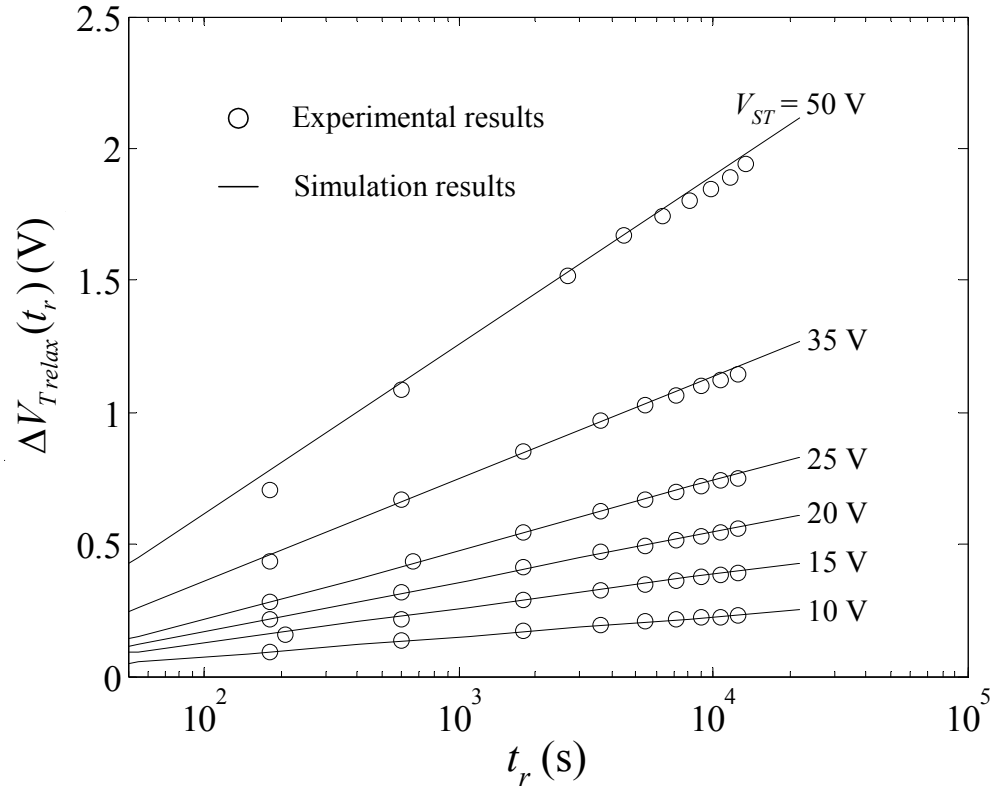

Fig. 4.7 Charge de-trapping simulation results using the parameters of Table 4.2 after 3.5 hours of bias stress with V_{ST}; the experimental results are also shown (open circles).

The numerical integration of (4.15) can also be approximated by a logarithmic function in time for the threshold voltage relaxation of the TFT. With the simplified profile or a

distribution of the trapped electrons inside the SiN, Fig. 4.6, the total charge trapped in the SiN after the bias stress is written as

$$Q_0 = qN_{tr}(x(t_{ST}) - x_0). \tag{4.16}$$

At time t_r after the bias stress is removed, the density of the trapped electrons is given by (4.13). The distribution of the trapped electrons, immediately after the bias stress of 35V for 3.5 hours and after t_r = 1000s of relaxation, are plotted in Fig. (4.8). The parameters of Table 4.2 are used for the SiN trap levels, and $x_{relax}(t_r)$ is calculated to be 22.0Å.

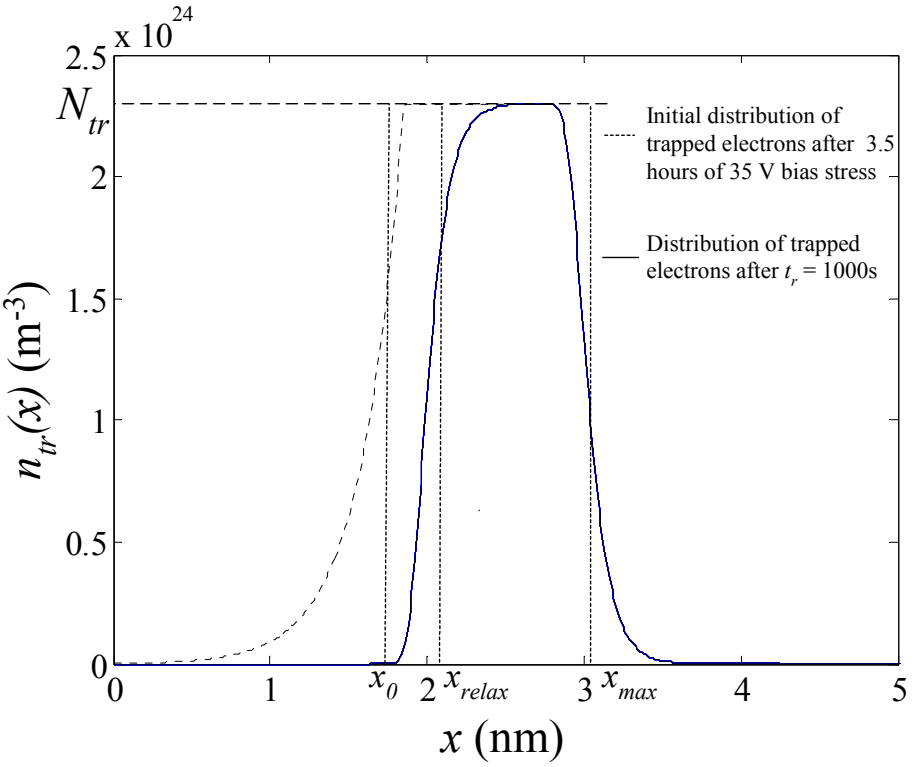

Fig. 4.8 Distributions of the trapped electrons immediately after a bias stress with 35V for 3.5 hours (dashed lines) and after 100s of relaxation (solid lines); the position of x_0, x_{max}, and x_{relax} are also shown.

The number of trapped electrons inside the SiN at time t_r is approximated by

$$Q(t_r) = qN_{tr}\left[x(t_{ST}) - x_{relax}(t_r)\right]. \tag{4.17}$$

Therefore, the number of electrons which have tunnelled back to the a-Si:H is calculated as follows:

$$Q_{relax}(t_r) = Q_0 - Q(t_r) = qN_{tr}\left[x_{relax}(t_r) - x_0\right]. \tag{4.18}$$

Substituting (4.18) and (4.12) into (4.15) yields

$$\Delta V_{T\,relax}(t_r) = \frac{qN_{tr}}{aC_i}\ln(t/t_0') \tag{4.19}$$

with

$$t_0' = \frac{1}{S_0 \bar{v} n_{empty}} \exp(ax_0)\,. \tag{4.20}$$

Equation (4.19) is valid only when $x_{relax}(t_r)$ is larger than x_0 and smaller than $x_{max}(t_{ST})$ which means that $t_0' < t_r < \frac{1}{S_0 \bar{v} n_{empty}} \exp\left(ax_{\max}(t_{ST})\right)$.

Fig. 4.9 demonstrates the lines obtained by the least square fits of equation (4.19) to threshold voltage relaxation of the TFT (Fig. 4.3 (b)) after 3.5 hours of bias stress with different gate voltages. It is obvious that the results achieved by using (4.19), displayed in Fig. 4.9 and the numerical calculation of (4.15), presented in Fig. 4.7, are very similar.

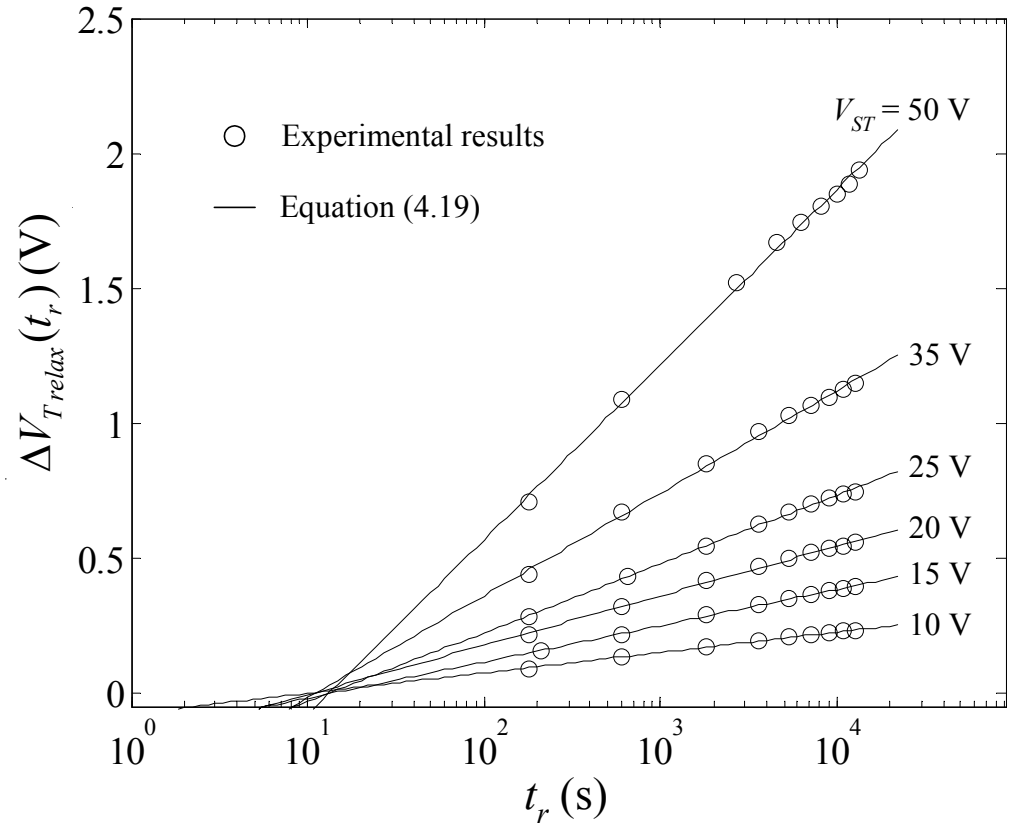

Fig. 4.9 Solid lines are the result of the least-square fitting of (4.19) to the experimental threshold voltage relaxation after different bias stress tests for 3.5 hours (open circles).

The slopes and x-intercepts of the lines in Fig. 4.9 can be used to extract the parameters of Table 4.2. The value of N_{tr} for the relaxation after the bias stress with a certain voltage is calculated by using (4.19), and the slope of the line fitted to the experimental results. In the calculation of N_{tr}, it is assumed that the energy of E_C is much greater than that of E_T, and the dependence of a on E_T can be ignored. By adopting the value of N_{tr} and the following recursive method, E_T and N_{ti} are calculated.

(1) It is assumed that the total threshold voltage shift of the TFT occurs because of charge trapping in the SiN $\Delta V_{T\,trap} = \Delta V_{T\,total}$.

(2) By substituting $\Delta V_{T\,trap}$ and N_{tr} into (3.35), the value of E_T is given.

(3) By substituting E_T and the x-intercept of the line fitted to the experimental results into (4.20) n_{empty} and N_{ti} are found.

(4) N_{ti} can be used to calculate the number of created defects in the lower half of the band gap ΔN_{db} and $\Delta V_{T\,defect} = qC_i \Delta N_{db}$.

(5) By using $\Delta V_{T\,defect}$, the charge trapping component of the threshold voltage shift is given by $\Delta V_{T\,trap} = \Delta V_{T\,total} - \Delta V_{T\,defect}$.

(6) The repetition of steps (2) to (5) yields a consistent set of volumes for N_{ti}, E_T, and $\Delta V_{T\,relax}$.

The values obtained for N_{tr}, E_t, and N_{ti} by this method are very close to the parameters in Table 4.2 that are used for the charge trapping and de-trapping calculations. For example, the relaxation after a bias stress of 10V, results in $N_{tr} = 4.3\times10^{17}$ cm^{-3}eV^{-1}, $E_T = .052$ eV, $N_{ti} = 5.2\times10^{13}$ cm^{-3}eV^{-1}, and $\Delta V_{T\ relax} = 0.39$ V. This is consistent with the lowering the quasi Fermi level of the a-Si:H by 4 meV with respect to the conduction band as a result of the creation of 7.7×10^{7} cm^{-3} defect states at 1eV below E_C.

The results of this section for the energy levels and the concentrations of traps in the SiN can be interpreted as the average energy and the number of states into which electrons get trapped during the bias stress experiment. In the next section, I try to explain the threshold voltage relaxation result by using a realistic Gaussian distribution of the SiN traps.

4.2.2.2 Charge De-trapping from the Gaussian Distribution of SiN Traps

So far, it is confirmed that the charge trapping and de-trapping mechanisms can be modelled by using a mono-energetic level of the traps inside the SiN. Fig. 4.10 shows the extracted values of N_{tr} and E_T from the threshold voltage relaxation experiments as a function of the gate voltage during the bias stress.

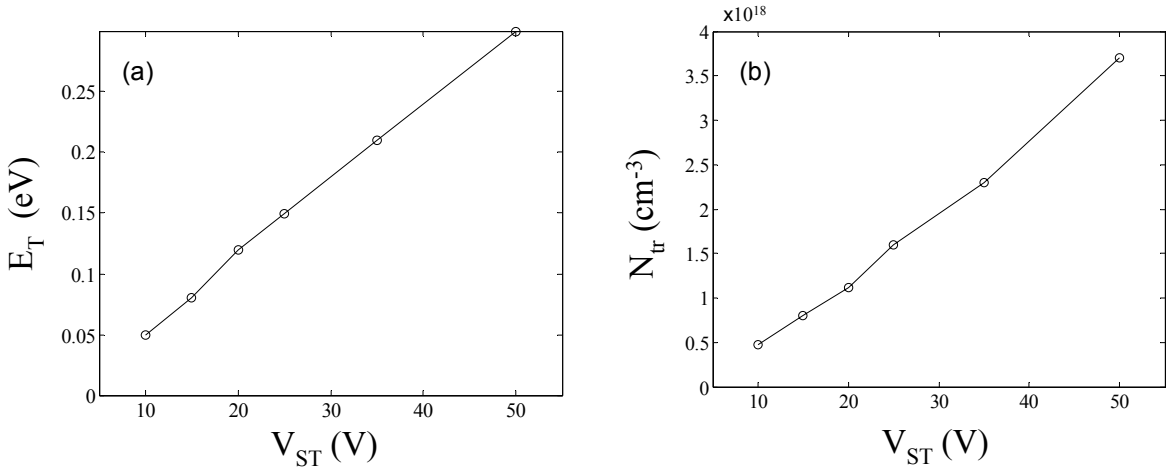

Fig. 4.10 (a) E_T and (b) N_{tr} are extracted from the threshold voltage relaxation results after removing 3.5 hours of bias stress with different stress voltages.

From Fig. 4.10, it is obvious that E_T and N_{tr} increase with the stress voltage. This can be explained by assuming that there is a Gaussian distribution of the traps inside the SiN with a mean energy value above the quasi Fermi level [68]. By increasing the bias stress, band bending inside the SiN increases, and the electrons can tunnel into the higher energy-level SiN traps. Therefore, the number of traps into which the carriers can trap and the average energy of these states both increase.

The kinetics of the charge de-trapping from Gaussian distribution of traps is similar to the charge release from the mono-energetic SiN traps. After time t_r of removing the gate bias, the number of trapped electrons inside the SiN per unit energy at position x from the interface and the energy level E above the quasi Fermi level of the SiN is given by

$$n'_{tr}(x,E,t_r) = n'_{tr}(x,E,t_{ST}) \exp\{-S_0 \bar{v} n_{empty}(E) t_r \exp(-a(E)x)\}, \quad (4.21)$$

where $n'_{tr}(x,E,t_{ST})$ is the density of the trapped electrons per unit energy at position x and energy level E after t_{ST} of bias stress, S_0 is the electron capture cross-section of a-Si:H

conduction band tail states, $\bar{v}$ is the thermal velocity of electrons, $n_{empty}(E)$ is the number of empty states at energy E above the quasi Fermi level of a-Si:H, and $a(E)$ is the tunnelling parameter.

$n_{empty}(E)$ is related to N_{ti}, E_F of a-Si:H, and the characteristics energy of the conduction band tail V_{nt} by the following equation

$$n_{empty}(E) = N_{ti} \exp\left[\frac{E - E_F}{V_{nt}}\right]. \tag{4.22}$$

The tunneling parameter $a(E)$ for electrons trapped at energy E above the SiN quasi Fermi level is given by

$$a(E) = \frac{2}{\hbar}\sqrt{2m^*(E_C - E)}, \tag{4.23}$$

where m^* is the effective mass of electrons, E_C is the conduction band edge, and $\hbar$ is the reduced Plank's constant, $\hbar = \frac{h}{2\pi}$, respectively.

To calculate the relaxation of the threshold voltage after a time t_r of removing the bias stress, the total number of electrons which have been de-trapped from the SiN states during the relaxation period must be found out. The number of released electrons per unit volume unit energy from the SiN traps $n'_{relax}(x,E,t_{ST})$ by time t_r is calculated by subtracting $n'_{tr}(x,E,t_r)$ from $n'_{tr}(x,E,t_{ST})$. The integration of $n'_{relax}(x,E,t_{ST})$ over the dielectric thickness and the trap energy levels of the SiN yields the total number of electrons that tunnel back to the a-Si:H. Therefore, the relaxation of the threshold voltage after time t_r of removal of the bias stress is written as

$$\Delta V_T(t)_{relax} = \frac{q}{C_i}\int_{E=E_F}^{E_c}\int_{x=0}^{d} n'_{tr}(x,E,t_r)\,dE\,dx, \tag{4.24}$$

where C_i represents the gate capacitance, and q is the elementary charge.

By using the trap distribution of (3.38) inside the SiN and choosing N_{trm}, E_{tm}, and σ to be 1.0×10^{19} $eV^{-1}cm^{-3}$, 0.25 eV, and 0.21 eV, respectively, the charge trapping and the subsequent de-trapping calculations are in good agreement with the experimentally obtained threshold voltage relaxation results. For the charge de-trapping calculations, the electron capture cross-section of the a-Si:H conduction band tail states is assumed to be 10^{-15} cm^2, and the values of Table 4.2 are employed for N_{ti}.

The profile of trapped electrons inside the SiN as a function of the distance from the interface and the energy of the trap states after t_r = 100, and 10^4 seconds of removing 15V and 35V bias stresses are exhibited in Fig. 4.11.

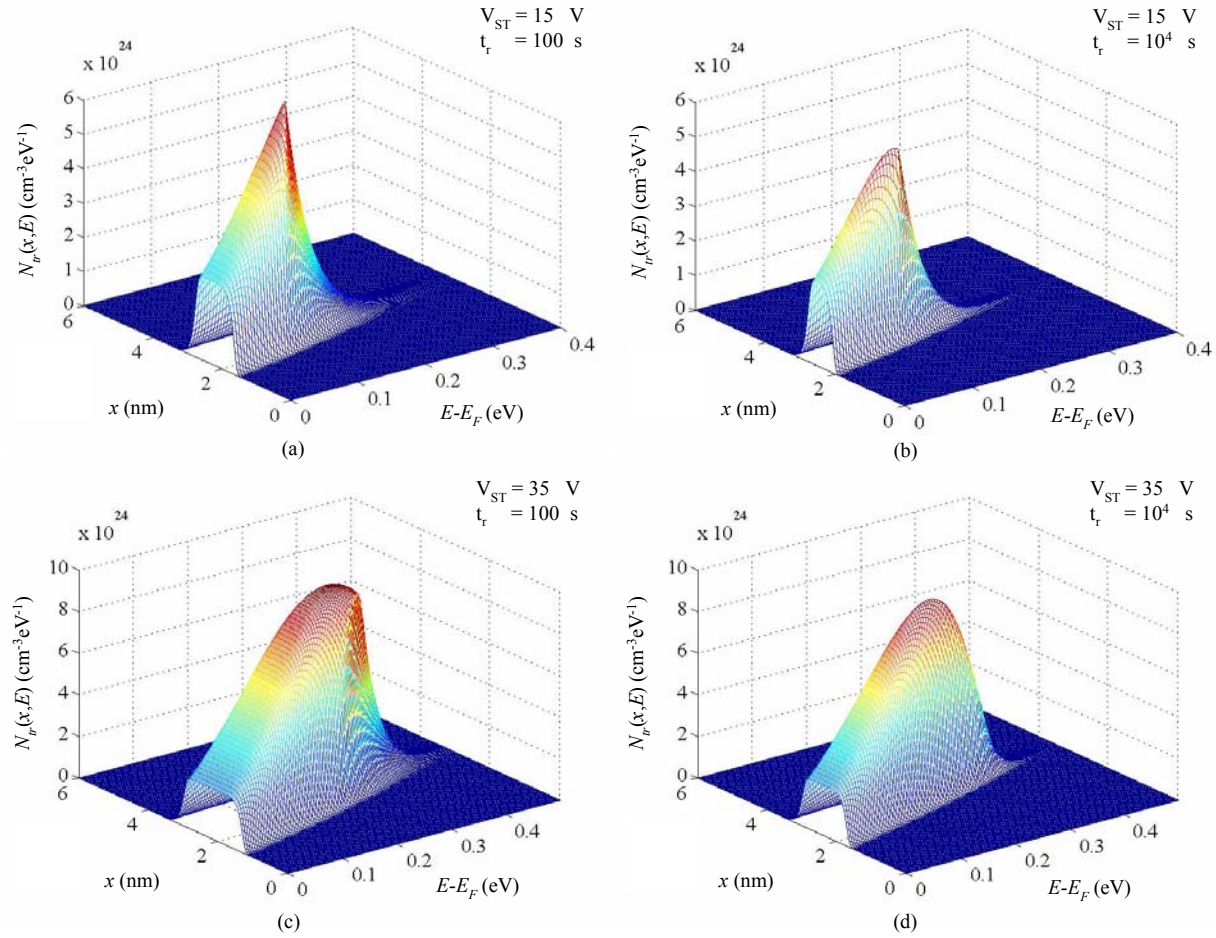

Fig. 4.11 Concentration of filled traps as a function of the distance and energy after 100 and 10^4 seconds of removing (a), (b) a 15V bias stress and (c), (d) a 35V bias stress for 3.5 hours.

Equation (4.21) suggests that the rate of releasing the electrons from the traps is faster for the states located closer to the interface. Thus, at first the states close to the interface become empty; then, by increasing the relaxation time the states farther are depleted. This can be seen by the comparison of (a) with (b), and (c) with (d) in Fig. 4.11. Furthermore, the rate of release of the states which are located in the higher energy traps is faster. This is due to the

fact that the electrons trapped in the higher energy states encounter a lower energy barrier for tunnelling back to the a-Si:H layer.

The predicted relaxations of the threshold voltage shift using (4.24) are shown in Fig 4.12 along with the experimental results. For the calculation of $\Delta V_{T\,relax}$, the effect of the charge which is released 10s after the removal of the bias stress is neglected. This is due to the charge de-trapping during the measurement of the I-V characteristics of the TFT.

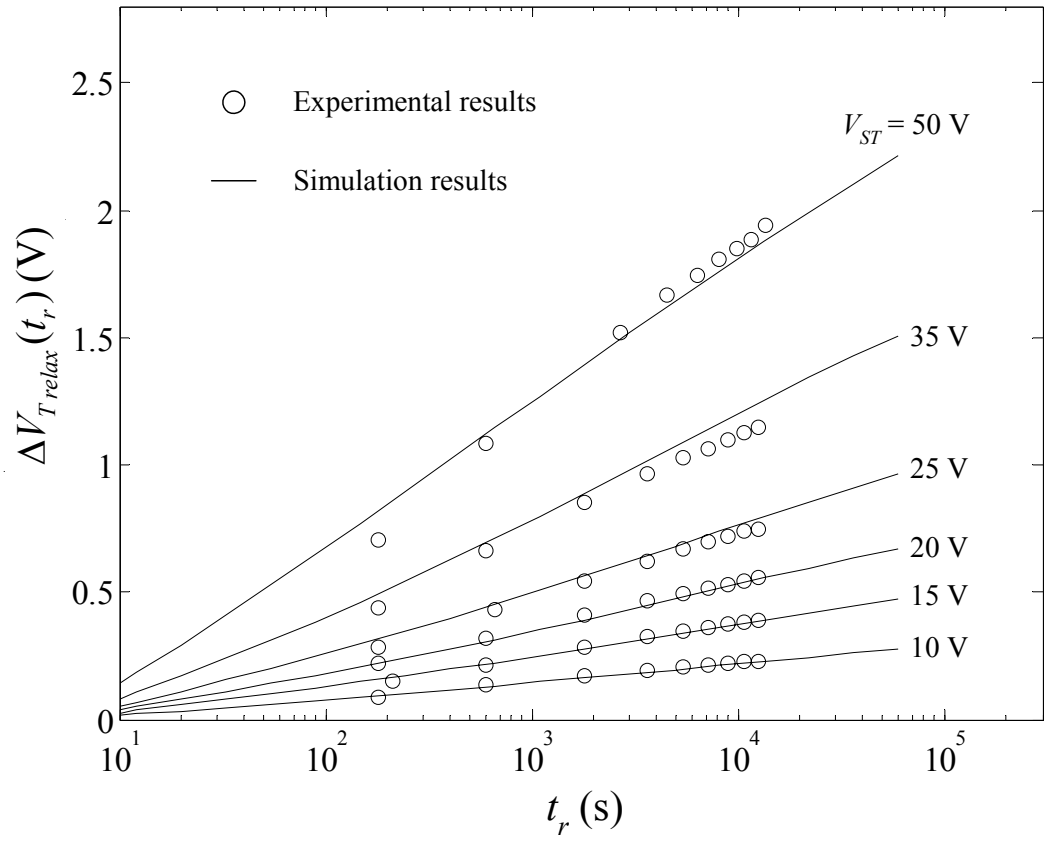

Fig. 4.12 Calculated threshold voltage relaxation using (4.24) (solid lines) and the experimental results (open circles) after 3.5 hours of bias stress with V_{ST}.

Fig. 4.12 confirms that the simulations are in good agreement with the experimental results. However, at higher stress voltages, the simulation results deviate slightly from the experimentally obtained threshold voltage relaxation. This may be the result of neglecting the charge trapping of the a-Si:H conduction band electrons, or relaxation during the measurement of the I-V characteristics.

The investigations of the effect of higher stress biases and longer relaxation times will complete this section. The threshold voltage relaxation after 10.5 hours of 15V bias stress is denoted in Fig. 4.13. The calculated threshold voltage relaxation, based on (4.24) is also presented. It is obvious that the simulation results are very close to the experimental results, in Fig 4.13. N_{ti}, used for the charge de-trapping calculations, decreases over time due to the creation of extra defect states in the lower half of the band-gap. N_{ti} is estimated to be 1.5×10^{13} $cm^{-3}eV$ using the method described in Chapter 3.

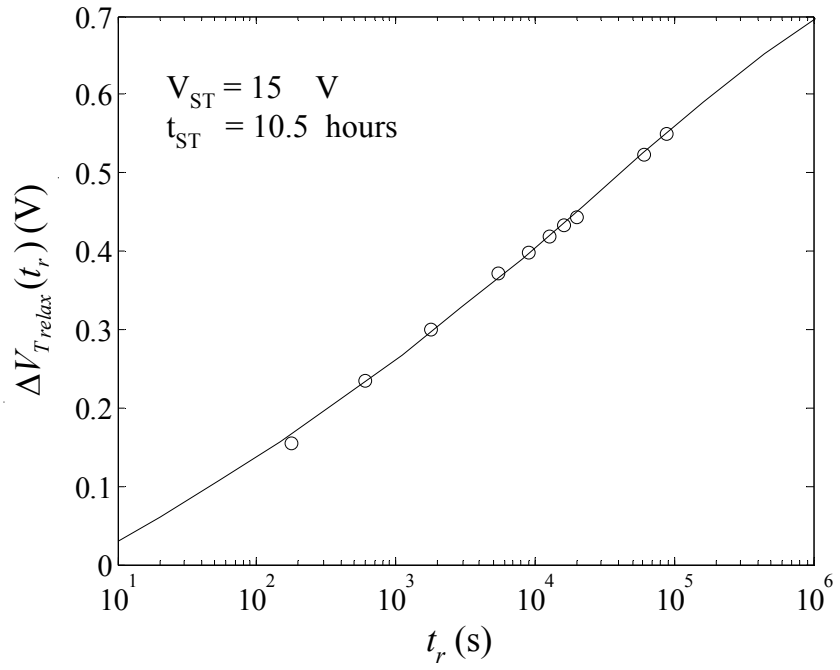

Fig. 4.13 Threshold voltage relaxation calculated using (4.24) (solid line), and the experimental results (open circles) after 10.5 hours of bias stress with 15V.

4.3 Quantitative Distinction between the Charge Trapping and the Defect State Creation

In chapter 3, the defect state creation and the charge trapping in the SiN were discussed as the mechanisms responsible for the threshold voltage shift of a a-Si:H TFTs. Although the effect of charge trapping is assumed to be negligible for stress voltages as low as 10 or 15V

[48], the present study of the threshold voltage relaxation clearly demonstrates that $\Delta V_{T\,relax}$ cannot be explained by the defect state annealing process; however the phenomenon is consistent with the charge de-trapping or back tunnelling of the injected electrons into the SiN traps. Therefore, if the effect of the charge trapping in the SiN is neglected for low bias stresses, the observed relaxation of the threshold voltage, which is more than 50% of the total threshold voltage shift after the bias stresses as low as 10V cannot be explained.

With the results obtained in this Chapter, the total number of electrons trapped in the SiN can be calculated. Therefore, the total threshold voltage shift of the TFT due to charge trapping in the SiN $\Delta V_{T\,trap}$ can be determined. In addition, it is also possible to approximate $\Delta V_{T\,trap}$ by adopting the recursive method presented in Section 4.2.2.1. Consequently, the portion of the threshold voltage shift which is related to the defect state creation is given by $\Delta V_{T\,defect} = \Delta V_{T\,total} - \Delta V_{T\,trap}$.

Fig. 4.14 shows calculated $\Delta V_{T\,defect}$ as a function of the effective bias voltage, V_{ST} - V_T, after 3.5 hours of the application of the bias stress.

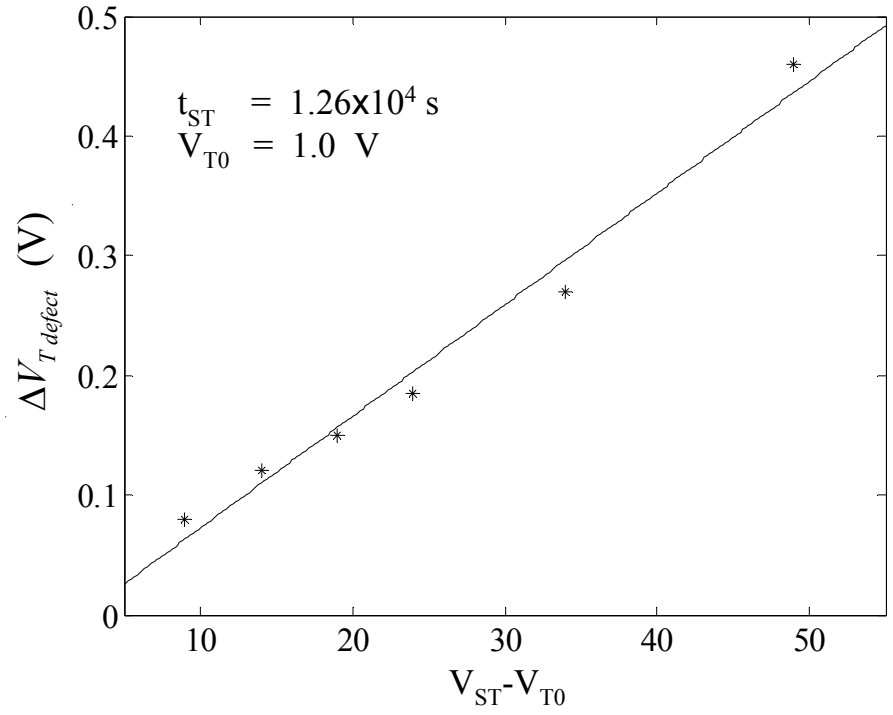

Fig. 4.14 Calculated $\Delta V_{T\,defect}$ as a function of $V_{ST} - V_{T0}$ after 3.5 hours of bias stress.

Fig. 4.14 reveals that $\Delta V_{T\,defect}$ increases linearly with the applied voltage. This is expected for the defect state creation mechanism, since, based on (3.15), the kinetics of the creation of extra defects is proportional to effective gate voltage. In addition, comparison of Fig. 4.14 and Fig. 3.5 shows that only a small portion of the total threshold voltage shift is due to the defect state creation; thus, charge trapping is the dominant mechanism for the threshold voltage shift in the range of stress times used in this thesis. However, for longer stress times, the defect state component of ΔV_T increases proportionally to t^{β}, but the charge trapping component increases with ln(t). Therefore, for longer stress times, the defect state creation may become more dominant mechanism for the threshold voltage shift of TFT. For example, by using the SiN trap states calculated in this Chapter, the bias stress tests at 10V for 3500 hours results in a $\Delta V_{T\,trap}$ of 0.64. On the other hand by assuming $\beta \approx 0.5$ the defect state creation component increases by a factor of 30 which yields $\Delta V_{T\,defect}$ more than 2.5V. Consequently, for this stress time, $\Delta V_{T\,defect}$ is almost four times larger than $\Delta V_{T\,trap}$ and the defect state creation is expected to be the dominant mechanism for the metastable changes in the threshold voltage of TFTs used in this work. However, a more general conclusion cannot be drawn since the kinetics of charge trapping and defect state creation depend on the details of processing steps used for fabrication of TFT.

4.4 Summary

The underlying mechanisms for the threshold voltage relaxation of a TFT, after the termination of the bias stress, have been investigated in this chapter. The relaxation of the threshold voltage after removing the gate bias is attributed to the annealing of defect states and the charge de-trapping of the electrons from the SiN states. The model based on annealing the created extra defects has been ruled out, and the kinetics of $\Delta V_{T\,relax}$ have been explained by the charge release of the injected electrons into the SiN during the application of the gate bias. The simulation results, presented in the Section 4.2, support the threshold voltage relaxation model based on charge de-trapping from the SiN states. The simulation

results agree with the experimentally obtained threshold voltage relaxation, after the bias stress with different stress voltages and stress times are withdrawn. An energy dependent Gaussian distribution of SiN gap states (traps) with a maximum value of 1.0×10^{19} $eV^{-1}cm^{-3}$, a mean energy of 0.25 eV above the SiN Fermi level, and a standard deviation of 0.21 eV explains the kinetics of the threshold voltage relaxation observed in this work. Finally, a quantitative distinction between charge trapping and defect state creation mechanisms is done.

Chapter 5

Conclusions and Future Work

The threshold voltage shift of a-Si:H TFTs due to the prolonged application of a positive bias stress to the gate of transistor and the subsequent threshold voltage relaxation after the gate bias is removed, were investigated. Defect state creation and charge trapping in the gate dielectric are believed to be the mechanisms responsible for the threshold voltage shift of a a-Si:H TFT.

A comprehensive study of the defect state creation and charge trapping mechanisms was carried out in this thesis. Different aspects of the defect state creation mechanism such as the defect pool model, the role of H atoms and band tail carriers, and the kinetics of defect state creation mechanism were also studied. Then, the kinetics of charge trapping into the SiN gate dielectric was modelled for two cases: the simplified mono-energetic SiN traps above the Fermi level, and the realistic Gaussian distribution of SiN traps. The charge trapping in mono-energetic SiN traps is approximated by a logarithmic function of time, where its slope

and x-intercept in a semi-logarithmic scale are shown to be proportional to the number of the traps and their energy level, respectively. The charge trapping in the Gaussian distribution of traps also reveals a logarithmic time dependence. However, its slope and x-intercept increases over time due to the injection of carriers into higher energy-level traps. During the application of gate bias, the charge trapping and the defect state creation occur simultaneously; therefore, the experimental results of ΔV_T do not provide any particular information about the quantitative effect of each of these mechanisms on the threshold voltage shift of a TFT.

In addition in this thesis I have investigated the relaxation of the threshold voltage, following the termination of bias stress. The possible mechanisms for this relaxation such as the annealing of the defect states and the charge back tunnelling of trapped electrons inside the SiN were proposed. The experimentally obtained results for the relaxation of threshold voltage do not support the defect state annealing mechanism. The kinetics of charge de-trapping from the mono-energetic and Gaussian distribution of SiN traps were analytically modelled assuming a Shockley-Read-Hall-like recombination process. The calculations of charge trapping and de-trapping in and from a Gaussian distribution of SiN traps were performed which show a good agreement with the kinetics of threshold voltage relaxation.

Moreover, the total trapped charge in the SiN, and as a result, the charge trapping component of the threshold voltage shift were calculated using the developed charge trapping and de-trapping models. This provides a quantitative distinction between the defect state creation and the charge trapping mechanisms. Based on the calculated results for the charge trapping and the defect state creation components of threshold voltage shift, it was concluded that for the TFTs employed in this work, the charge trapping is the dominant threshold voltage shift mechanism. For longer stress times, the defect state creation may become the principal instability mechanism. However, a general conclusion cannot be drawn since the kinetics of both mentioned mechanisms strongly depends on the fabrication process of TFT.

More importantly, the qualities of the a-Si:H active layer and a-Si_xN:H gate dielectric layer strongly influence the kinetics of threshold voltage shift and relaxation of TFT. For example, a-Si_xN:H dielectric layers deposited at different temperatures and with different SiH_4/NH_3 gas ratios have different concentration of gap states. This changes the kinetics of charge trapping mechanism into the gate dielectric. The deposition condition of a-Si:H layer also

affects the rate of the creation and annealing of the extra defect states in the active layer by changing the number of weak bonds inside the layer.

Furthermore, it must be mentioned that the experimental results reported in this thesis and the charge trapping/de-trapping calculations have been achieved using one of the TFTs in a sample fabricated by MP6 process. However, the individual bias stress tests performed on the other TFTs on the same die are within ±10% of the results reported here. The initial threshold voltages of the TFTs fabricated by MP6 process show only ±0.2V deviation from the typical 1.0V threshold voltage. The bias stress tests also were performed on TFTs fabricated using MP5 process and the results are in good agreement with the results obtained from MP6 TFTs. The initial threshold voltages of MP5 transistors are 4.0V ±10%.

The main contributions of this thesis for the study of the threshold voltage shift mechanisms are as follows:

- Developed a model for studying the kinetics of the charge trapping into mono-energetic and a Gaussian distribution of the SiN gap states.
- Studied experimentally the relaxation of the threshold voltage shift, after the removal of the bias stress.
- Developed an analytical model for studying the kinetics of charge de-trapping from the mono-energetic and Gaussian distribution of SiN traps during the relaxation of the stress.
- Using the experimental results of the threshold voltage relaxation data, a Gaussian distribution for the SiN traps was determined.
- A quantitative distinction between the charge trapping and the defect state creation mechanisms was made for a wide range of stresses.

There are several issues regarding the proposed model in this thesis, which should be considered in the future work. The sensitivity of the presented models for the kinetics of charge trapping and de-trapping to various parameters such as the energy barrier of the tunnelling, the effective mass of the electron, the parameters of the Gaussian distribution of the SiN traps, and the capture cross section of the SiN traps and a-Si:H defects must be studied. Performing the bias stress and relaxation experiments at different temperatures also helps to distinguish between the defect state creation and charge trapping mechanisms due to their different temperature behaviour. Moreover, the kinetics of the defect state creation and

charge trapping mechanisms are greatly influenced by the processing conditions of the TFT. This necessitates an in-depth study of the effects of processing conditions especially the quality of SiN gate dielectric and a-Si:H active layer on threshold voltage shift and relaxation of TFT.

Appendix A - Processing Conditions of a-Si:H TFTs

TFTs employed in this work are of the inverted staggered structure, which their fabrication steps were explained in Section 2.1. Two types of TFTs fabricated using MP5 and MP6 processes were used for bias stress and relaxation tests. The only difference between MP5 and MP6 is the type of the contact layer for drain and source. MP5 employs heavily n-doped a-Si:H (n^+ a-Si:H) as the contact layer, while MP6 uses heavily n-doped micro-crystalline silicon (n^+ μc-Si:H) contact layer. Molybdenum (Mo) and aluminum (Al) have been used for the first metal (gate metal) and the second metal (contact metal) layers, respectively. The deposition conditions of different layers are shown in Table A.1.

Table A.1. Thin film deposition parameters for MP5 and MP6 fabrication processes.

	i a-Si:H	a-SiN_x:H	n^+ a-Si:H	n^+ μ-Si:H	Mo	Al
Fabrication process	MP5/MP6	MP5/MP6	MP5	MP6	MP5/MP6	MP5/MP6
Deposition system	MVS Cluster (PECVD)	MVS Cluster (PECVD)	MVS Cluster (PECVD)	MVS Cluster (PECVD)	Edwards (Sputtering)	Edwards (Sputtering)
Substrate temperature (°C)	300	300	300	300	Room Temp.	Room Temp.
Power (W RF)	2	2	2	10	400	400
Process pressure (m Torr)	400	400	400	1900	5	5
Base Pressure (m Torr)	$\sim 10^{-6}$	$\sim 10^{-6}$	$\sim 10^{-6}$	$\sim 10^{-6}$	$\sim 2\times 10^{-6}$	$\sim 2\times 10^{-6}$
Flow rates (sccm)	SiH_4: 20	NH_3: 100 SiH_4: 5	SiH_4: 20 PH_3: 2 H_2: 1	PH_3: 0.5 H_2: 250 SiH_4: 1	Ar: 30	Ar: 30
Deposition rate (Å/s)	2	1.3	1.3	1.3	2.5	1.8
Thickness (nm)	300	50	50	50	120	1000

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