Analysis of the Deep Sub-Micron a-Si:H Thin Film Transistors

by

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I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

The recent developments of high resolution flat panel imagers have prompted interests in fabricating smaller on-pixel transistors to obtain higher fill factor and faster speed. This thesis presents fabrication and modeling of short channel amorphous silicon (a-Si:H) vertical thin film transistors (VTFT).

A variety of a-Si:H VTFTs with different channel lengths, from 100 nm to 1 μm, are successfully fabricated using the discussed processing steps. Different structural and electrical characteristics of the fabricated device are measured. The results of I-V and C-V characteristics are comprehensively discussed. The 100 nm channel length transistor performance is diverged from regular long channel TFT characteristics, as the short channel effects become dominant in the device, giving rise to necessity of having a physical model to explain such effects.

An above threshold model for a-Si:H VTFT current characteristics is extracted. The transport mechanisms are explained and simulated for amorphous silicon material to be used in the device model. The final model shows good agreement with experimental results. However, we used numerical simulation, run in Medici, to further verify the model validity. Simulation allows us to vary different device and material parameters in order to optimize fabrication process for VTFT. The capacitance behavior of the device is extensively studied alongside with a TFT breakdown discussion.

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Chapter 1: Introduction

When first deposited in early 60s, nobody could predict that, in a few decades, amorphous silicon would play a major role in display and imaging electronic industries[1]. Today, presence of large area displays owes to maturity of hydrogenated amorphous silicon (a-Si:H) thin film transistors (TFT), which not only have enabled large area active matrix pixel addressing, but also have reduced final price of products due to low fabrication cost.

Physics of amorphous materials was developed with studies on chalcogenide glasses, while silicon based amorphous alloys were introduced later [2]. Yet early sputter deposited amorphous silicon had poor electrical properties, such as high defect density. Later in 1969, Chittick *et al.* used glow discharge for deposition of silicon films with lower defect density [3]. Today amorphous silicon material is deposited by plasma enhanced chemical vapor deposition (PECVD), which is based on Chittick's work. Having high quality material in hand, electronics people started to think about making devices using amorphous phase silicon; the first hydrogenated amorphous silicon device was a solar cell [4], and then Spear *et al.* proposed a-Si:H based thin film transistors (TFT) for device application in 1979 [5].

Nowadays, a-Si:H TFT is a well developed technology with ON/OFF current ratio of 10^8, threshold voltages as low as 1.5 V, subthreshold slope of 0.3 V/Dec, and field effect mobility of 1 cm^2/VSec. All of these improvements owe to applicability of TFTs in the back planes of different large area electronic applications such as active matrix flat panel displays and image sensors.

1.1 Active Matrix Flat Panel Electronics

Although cathode-ray tube (CRT) has been the dominant electronic display for about 75 years, flat-panel displays (FPDs) have recently edged the CRT for many applications. The active-matrix liquid-crystal display (AMLCD), the most successful FPD to date, has conquered virtually all modern portable display applications, including notebook computers, personal digital assistants, hand-held telephones, and camera viewfinders. Liquid-crystal displays (LCDs), when first used in computers, were fabricated as passive-matrix-addressed displays with diagonal sizes less than 10 inches. Yet, they are currently available with about 17 inches sizes in computers and with about 23 inches sizes in desktop monitors [7], and are still developing very fast. Recently (March 2005) Samsung Corporation has successfully demonstrated an 82-inch LCD high definition (HD) TV with 12.44 million TFT used to achieve full HD image of 6.22 million pixels [8]. It wasn't long ago when Sharp Corporation introduced 65V-inch AQUOS LCD color TV in October 2004, the world's largest at the time [9] with the totally 6,220,800 dots [1,920 (H) x 1,080 (V) x RGB]. While Samsung has announced shipment of its 57-inch 1080p LCD-TV in June 2005 for $16K, LG Electronics seems not to be far behind with a 55-inch 1080p model coming in fall 2005 [10]. Figure 1.1 shows a surplus of flat panel technology from CRT during these years. As it is clear from this figure, by the end of 2006, the market of FPD will be around 70 billion Dollars which is around 61% of the total electronic display market [11]. AMLCD constitutes 75% of the FPD market which is totally 55% of the display market, a number yet to increase by introduction of larger and better quality displays [12].

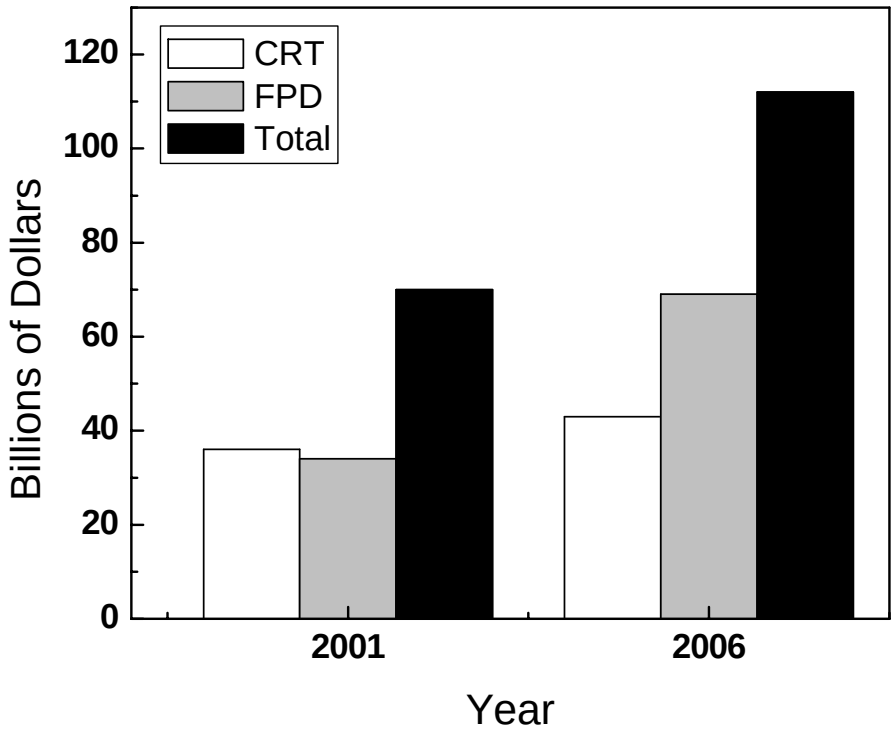


Figure 1. 1: Share of flat panel displays from the total electronic display market as in 2001 and anticipated in 2006, adopted from [11].

Generally, active matrix TFT backplane, which is used in AMLCDs and recently in AMOLEDs (Active Matrix Organic Light Emitting Diode), is an array of pixels with vertical and horizontal programming lines. Rows are connected to gates of switching TFT of the pixels, columns drive TFT sources, and drains are connected to the liquid crystal (LC). Gates and sources are scanned and programmed periodically by external CMOS driver for every pixel in a-Si:H AMLCD. Low temperature poly-silicon AMLCDs, due to better stability of poly-Si electrical characteristics, can have built-in drivers which reduces fabrication costs. Also there are some circuit requirements for AMLCDs that have to be addressed based on signal timings. For example, for 60 Hz operation the line time is 34.7 μsec, so the charging time of each pixel must be less than this number to maintain the

contrast of pictures. This number for a 852×480 wide VGA (WVGA) display with a pixel pitch of 0.974 mm is about 16.9 μsec [7]. Table 1.1 summarizes some requirements for active matrix pixel design.

Table 1. 1: Technology and Display parameters for double layer metallization AMLCD (adopted from [7]).

AMLCD Technology Parameter	**Value**
Row (Gate) Bus Resistance (Width 30 μm)	***18.8*** *Ω/mm*
Row Bus Capacitance (Width 30 μm)	***226*** *fF/mm*
Column (Source) Bus Resistance (Width 10 μm)	***45*** *Ω/mm*
Column Bus Capacitance (Width 10 μm)	***82.4*** *fF/mm*
Row to Column Bus Overlap Capacitance	***15.3*** *fF*
Sub-Pixel LC Capacitance	***8.24*** *pF/mm^2*
Sub-Pixel Storage Capacitance	***204*** *pF/mm^2*
TFT Channel On-Resistance (W/L=100/4.5)	***0.0634*** *MΩ.mm*
TFT Channel Off-Resistance (W/L=100/4.5)	***0.607*** *TΩ.mm*
TFT Gate to Source Capacitance	***689*** *fF/mm*
TFT Gate to Drain Capacitance	***919*** *fF/mm*
Row Driver Resistance	***1*** *kΩ*
Row Driver Capacitance	***1*** *pF*
Column Driver Resistance	***1.4*** *kΩ*
Column Driver Capacitance	***1.4*** *pF*
AMLCD Display Parameter for *m×n = 1280×720* FDP Format	
Aspect Ratio	***16 ×9***
Horizontal Pixel Pitch	***0.974*** *mm*
Vertical Pixel Pitch	***0.974*** *mm*
Pixel Array Width	***1246*** *mm*
Pixel Array Height	***701*** *mm*
Display Size	***56.3*** *Inch*
Worst case Sub-Pixel Charging Time	***26.8*** *μsec*

Another generation of FPD which is growing very fast is AMOLED displays (Figure 1.2a). Figure 1.2b shows the rate of market growth for AMOLEDs, which owes to specific characteristics of organic LEDs. Fast response time (< 10 μsec), large viewing angle

(~170^{o}), high contrast and brightness, light weight, lower power consumption, and high efficiency have given AMOLED displays very promising future [13]. OLED displays can potentially be used in different fields such as automotive, consumer electronics, digital video technologies, industrial, scientific medical applications, and telecommunications. Recently, Samsung electronics, the leader in TFT-LCD technology announced manufacture of the largest single-panel AMOLED display with 40-inch screen and the highest resolution at 1280 pixels by 800 pixels, implemented by amorphous silicon technology [14].

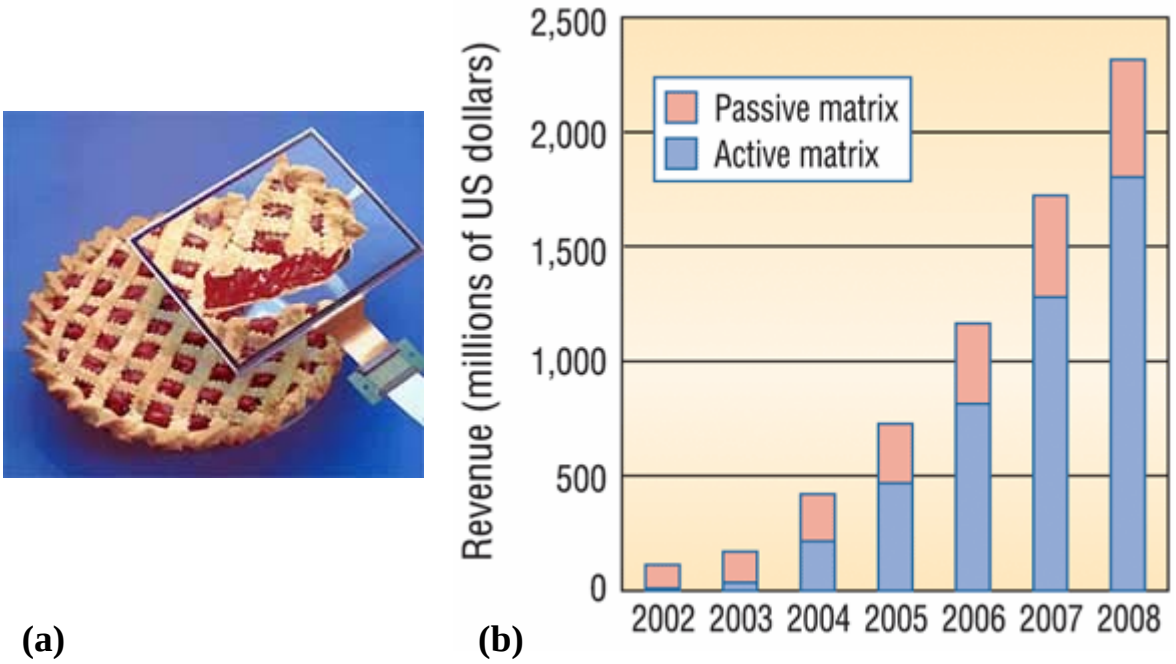


Figure 1. 2: a) Vivid picture from AMOLED b) OLED displays, particularly those using active-matrix technologies, will become more popular during the next five years and will generate an increasing revenue [13].

1.2 Motivation for Short Channel TFT

Generally it is of interest to have more driving current for both AMLCDs and AMOLEDs. LCD driver circuits switch the display by applying the pulse shape voltage to the liquid crystal. Thus, according to Equation 1.1, we can get faster switching by having more current or less capacitance [14].

$$i_o = C_{LC} \frac{dV_o}{dt} \tag{1.1}$$

Now, based on field effect transistor current equation [15], we may conclude that either the field effect mobility (μ_{FE}) or the *W/L* ratio has to be increased in order to get shorter switching time.

Table 1. 2: The characteristics of LTPS and a-Si:H TFTs [16].

	LTPS TFT	**a-Si:H TFT**
Mobility	50~200	0.5~1
Type of TFT	PMOS and NMOS	NMOS
TFT Uniformity	Worse	Better
Numbers of Mask	9~10	4~5
Cost (Array only)	High	Low
Cost (Module)	Low (Built-in driver)	High (External driver)
Equipment Investment	High	Low
Yield	Low	High
Overall Cost	Cheaper in smaller size panels	Cheaper in large size panels
Output Current	High	Low
Degradation	Not Sensitive	Sensitive

One way to enhance driver characteristics is fabricating the flat panel backplanes based on poly-Si which is a high mobility material with large area deposition properties. Although this material shows higher mobility and stability compared to a-Si:H, more fabrication steps are involved in making poly-Si based chips due to re-crystallization, which makes the

fabrication process more complicated. Also, grain boundaries create some non-uniformity in the different spots of the panels that causes non-uniform brightness across the display panel [16]. Table 1.2 provides a comparison between poly-Si and a-Si:H TFTs.

Another solution for increasing the output current is to increase *W/L*, by either increasing *W* or decreasing *L*. Increasing channel width translates to wasting pixel size and reducing fill factor (FF), so we have to reduce the channel length to get more current. Moreover, smaller channel length results in shorter electron transit time from source to drain,

$$t_D \propto \frac{L^2}{\mu_{FE}(V_G - V_T)} \tag{1.2}$$

and less capacitances [17] for conventional TFT structures, all of which give rise to faster performance. However, in a lateral TFT technology, making devices with smaller channel length requires expensive lithography. On the other hand, assuming 5-10 μm channel length, which is suitable for affordable lithography [18], for a reasonable *W/L* ratio the TFT area would be at least 15×20 μm^2 resulting in poor FF.

Therefore, fabricating vertical transistors, in which the channel length is defined by the insulating material thickness between source and drain, seems to offer an economical solution. This way, even deep sub-micron channel lengths can be defined by 5-10 micron lithography. So the TFT size would be independent of channel length and around 5×5 μm^2, compared to 15×20 μm^2 for conventional TFT structures. Figure 1.3 shows a comparison between lateral and vertical TFT structures [19].

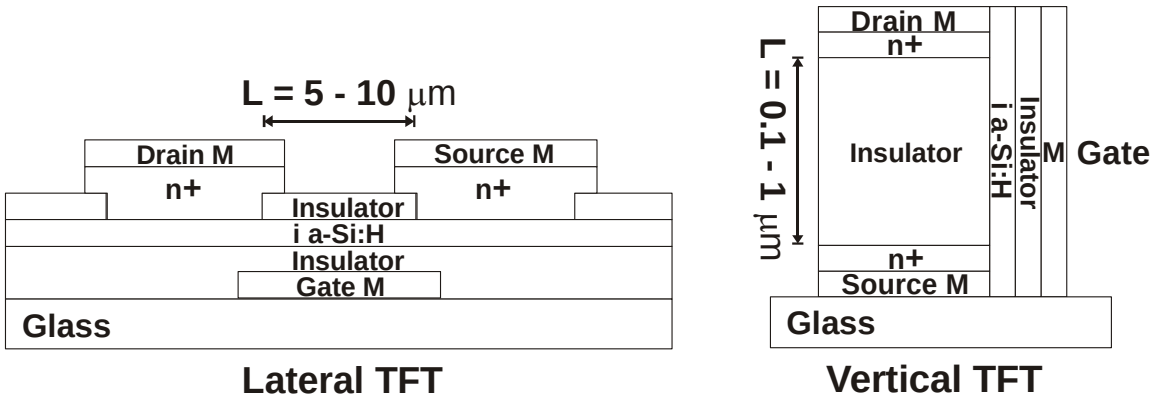


Figure 1. 3: Structures of lateral and vertical TFT (dimensions not to scale) [19].

Therefore, by applying Vertical TFT (VTFT) to active matrix driver circuits, we can increase display aperture ratio or the fill factor (FF) of the image sensors, and at the same time, obtain short response times and enhanced driving currents. FF is the ratio of active area over total pixel area, which can be calculated for square pixels as

$$FF = \frac{L_P^{\,2} - (L_{TFT} \times W_{TFT})}{L_P^{\,2}} \tag{1.3}$$

where L_P is the pixel pitch. It is obvious that FF decreases as pitch size shrinks.

Looking at the trend of display panel development, we will find out that for high resolution pictures, pixel size (L_P) becomes smaller (Figure 1.4) [20], which degrades the aperture ratio. The case is even worse in flat panel imagers, where the pixel size may shrink down to 100 μm for x-ray sensors [21] and 50 μm for mammography [22]. Therefore smaller transistors would be a solution for high resolution panels.

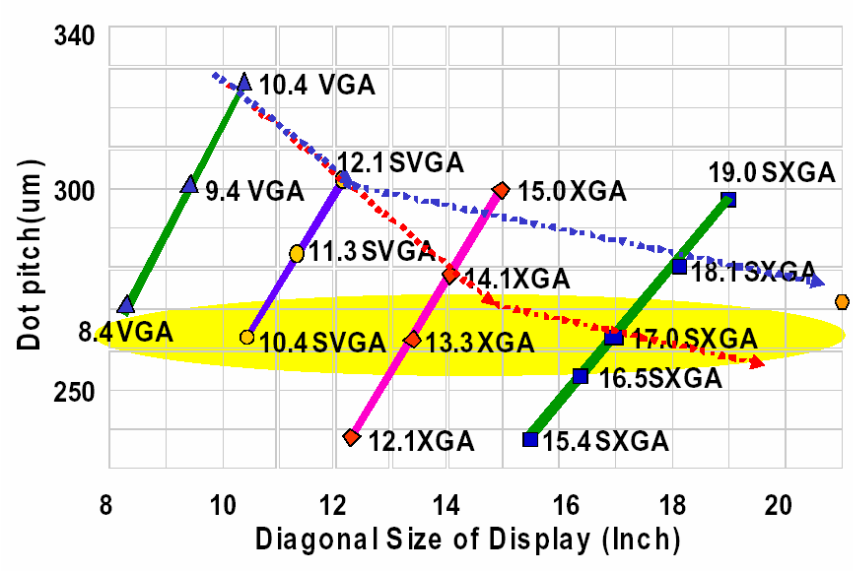


Figure 1. 4: Trend of TFT pixel size change in TFT LCD panels [20].

1.3 Thesis Objectives

The main objective of this work is to study electrical characteristics of recently developed VTFT technology in the a-SiDIC group, University of Waterloo, and finding optimized structure design for active matrix flat panel applications. To achieve this goal, the thesis is divided into following categories:

I) VTFT fabrication
   - *a)* Fabricating various device dimensions.
   - *b)* Testing different materials for different parts of VTFT.

II) Device characterization
   - *a)* I-V characterization.
   - *b)* Capacitance-voltage measurement.

III) Device modeling
   - *a)* Simulating electrical field and potential in the device, especially in the a-Si:H active region.
   - *b)* Physic-based extraction of forward above-threshold current characteristics of VTFT.
   - *c)* Evaluating device capacitances.

IV) VTFT optimization
   - *a)* Comparing physical model predictions with the fabricated device characteristics.
   - *b)* Using obtained data to improve VTFT operation.

1.4 Thesis Organization

In this thesis, two different topics about short channel hydrogenated amorphous silicon (a-Si:H) TFTs are discussed; first, the structure and fabrication of Vertical a-Si:H TFTs (VTFT), and second, device modeling which incorporates physical properties of a-Si:H material, field effect in a-Si:H, and short channel effects in TFTs with submicron channel.

In chapter 2, we review physics of the amorphous semiconductors especially a-Si:H. After a brief introduction to the amorphous material electronic structure, the density of states and mobility edges are described. The definition of field effect mobility for the disordered material with exponential band tail is also presented. Moreover, various carrier transport mechanisms such as space charge limited and drift-diffusion currents in the a-Si:H film are discussed.

In chapter 3, we describe the structure, process and characteristics of conventional long channel TFTs, alongside with a discussion about a-Si:H TFT electrical breakdown. Later on, vertical TFTs (VTFT) are introduced and the fabrication steps are described. The I-V and C-V characteristics for fabricated VTFT structures are also discussed. Finally, the characteristic of a VTFT-based inverter is reviewed.

In chapter 4, we start with long channel a-Si:H TFT model and then incorporate short channel effects including drain induced barrier lowering (DIBL), gate leakage, and back gate effect. The final model shows good agreement with the experimental results. However, numerical simulations are run to verify the model on the device characteristics. Eventually, capacitance characteristics are evaluated in the end of this chapter.

Finally, chapter 5 concludes the thesis.

Chapter 2: Carrier Transport in Amorphous Silicon

From electrical point of view, materials are classified into three major groups: metals, semiconductors, and insulators. According to Mott's N-8 rule, atoms, whether they are in a crystalline or an amorphous network, bond to their neighbors. But in amorphous materials long range periodicity of structure is absent, and only short range order exists. This means that electron's wave function is determined in very small range of space. Therefore, Heisenberg Uncertainty Principle implies that the uncertainty in wave-vector k increases ($\Delta k/k \sim 1$). In this case, k is not a good quantum number for describing the eigen-states, and the concept of Fermi surface is no longer valid. In other words, no well-defined E-K diagram exists [1], [2].

Conduction observation of disordered materials shows that the relation of conductivity follows the Arrhenius form versus temperature. This can help to extract the density of states in the material. Nevertheless, Starting with Anderson localization theory [23], it was found out that density of states can be defined as combination of localized and non-localized states. Localized states appear as energy levels in the material band gap and form

trap states, tailing the band edges. For crystalline-like material, electron density of states consists of only non-localized states that form valance and conduction bands.

This chapter generally introduces some key concepts of amorphous semiconductor physics used in the following chapters. First we start from definition of mobility gap and then discuss density of free and trapped carriers, based on density of states (DOS). Later, a definition for mobility used in device level analysis will be introduced. Finally, we will investigate different regimes of carrier transport in bands and band tails, including space charge limited (SCL) and drift-diffusion currents.

2.1 Electronic Structure

As mentioned, amorphous silicon, unlike crystalline counterpart, doesn't have periodicity in material structure. Although band structure is easily defined for crystalline material, electronic structure of amorphous material acquires comprehensive solid state study to obtain a good model. Due to the fact that there is strong interaction between neighboring atoms in amorphous material, which is absent in crystalline materials, the wave function, Ψ_E, becomes localized. This means that each wave function Ψ_E is confined to a small region in space. This was first proposed by Anderson (1958) in his classical paper on "Absence of diffusion in certain random lattices"; the above phenomenon is known as Anderson localization [23]. He modeled potential well network by random distributed values of potential, instead of identical potential distribution in crystalline materials. Assuming potential difference between deepest and shallowest well as V_0 he calculated that for

$$\frac{V_0}{B} > 5 \qquad (2.1)$$

The energy bands become localized. In this relation $B = 2ZI$ is a band width where Z is a coordination number and I, the transfer integral, which depends on the shape of the potential wells and their spacing. V_0 is larger in materials with more disorder where more localization exists [2].

Mean free path (L) can be defined based on phonon scattering; in well defined extended band structures $kL>>1$, where k is the electrons wave vector, a quantum quantity. This implies high mean free path for electrons in crystalline structures. In disordered semiconductors, because of heavy scattering, mean free path would decrease until $kL\sim1$. This is the case where wave vector definition is no longer valid and localization occurs [2]. Ioffe and Regel (1960) proposed that values of L which $kL<1$ is impossible [24]. This leads us to think about a new structure for disordered materials. Gobanuv in his book assumed that near the edges of conduction or valence bands, the states in non-crystalline materials are localized and in the valence and conduction bands, like crystalline material, we have extended states [25].

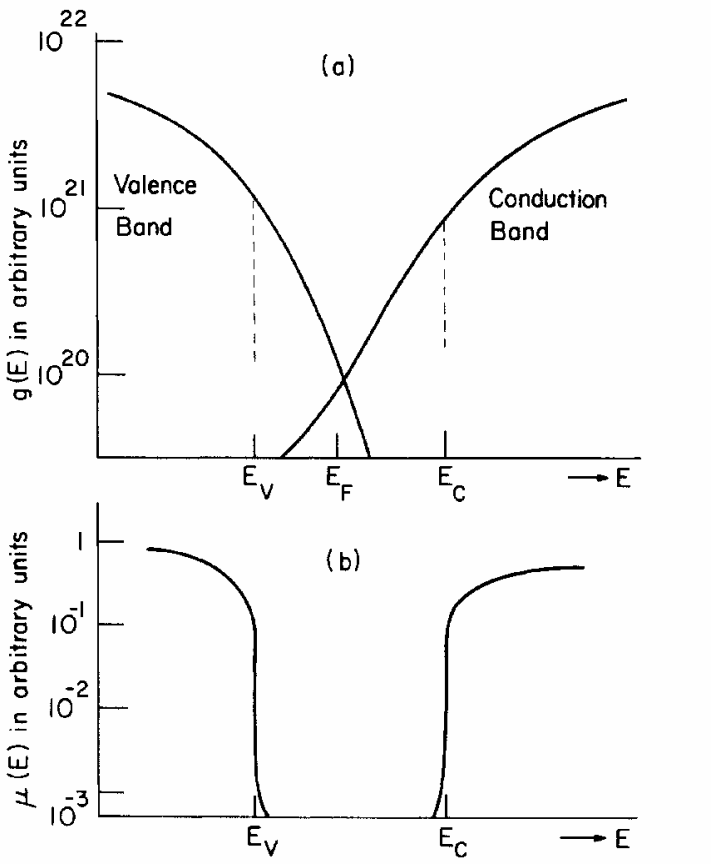


Figure 2. 1: Sketch of a) density of states of the valence and conduction bands b) electron mobility near conduction band and hole mobility near valence band, in arbitrary units [27] .

The edge separating the localized and extended states is referred as the mobility edge and can be defined as energy in which $V_0 \sim 5B$. We expect crystalline like conduction beyond these edges and no transport in the localized states unless by means of hopping due to trap like characteristics of these states [2], [26]. Cohen *et al*. [27] proposed a band model and described mobility edges based on their model. Figure 2.1 shows the density of states (DOS) and mobility versus energy respectively. This model assumes that in an alloy, most of the atoms are in sites satisfying their valence requirements (Mott's N-8 rule). Also in this model the valence and conduction band tails overlap, this means that an electron in a valence band in some regions of material may have a higher energy than an extra electron in a nonbonding (non-valence) states in another part of the material. Such electrons drop from the top of the valence band tail into spatially distinct states in the lower conduction band tail. The Fermi level E_F thus falls near the center of the gap [27]. Conduction band states are neutral when unoccupied, but valence band states are neutral when occupied by an electron. And all of these charged states above and below E_F act as efficient trapping centers for electrons and holes respectively. As it is also clear from Figure 2.1b the mobility in the localized states drops three orders of magnitude for both electrons and holes. This is the reason why in experiments one can see well defined activation energy for conductivity [27]. Later on, it was found out that because of the broken bond in the amorphous material, some deep levels of density of states exists exactly at the middle of the band gap; based on the charge of these states, they can shift a little bit toward either conduction or valence band [2], [28]. Figure 2.2 shows the random network and dangling bond in the amorphous silicon network.

Electronic transport in amorphous solids may occur in three ways [2]:

i) Electrons in the extended states can easily move in the conduction band with finite mobility. But these are excited electrons from below Fermi level into conduction band and thus this kind of conduction vanishes at lower temperatures.

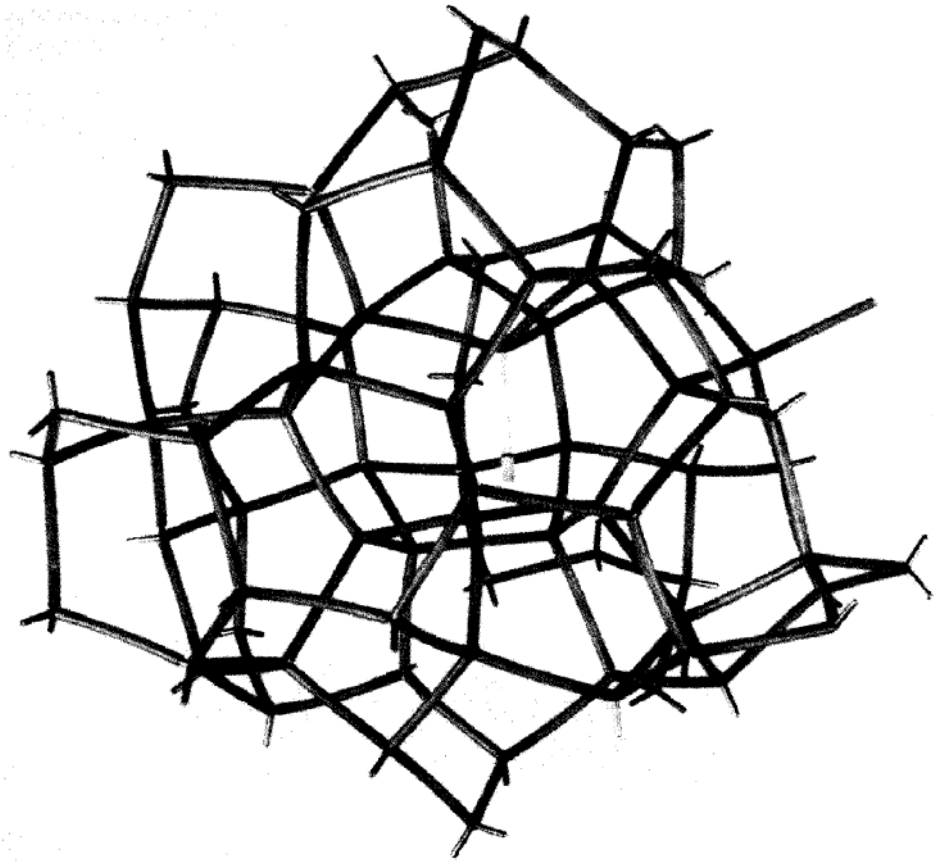


Figure 2. 2: Dangling bonds in the random network, simulating random structure of amorphous Silicon [28].

$$\sigma = \sigma_{\min} \exp\left(-\frac{E_C - E_F}{kT}\right) \tag{2.2}$$

where k is the Boltzmann's constant, T is temperature and σ_{min} is defined for $V_0 = 2B$ as

$$\sigma_{\min} = \frac{0.026e^2}{\hbar a} \tag{2.3}$$

a is the average distance between neighboring atoms in Å [3].

ii) Transport by carriers excited into localized states at the band edges and hopping at energies close to E_A and E_B where conduction and valence band tails vanish respectively in Mott DOS model. By assuming the conduction only by electrons we can write:

$$\sigma = \sigma_1 \exp\left(-\frac{E_A - E_F + w_1}{kT}\right) \tag{2.4}$$

where w_1 is the activation energy for hopping, which decreases with decreasing temperature. σ_1 is also a parameter which is much smaller than σ_{min}.

iii) If the density of states at E_F is finite, then carriers located near the Fermi energy level can hop between deep localized states by a process analogous to impurity conduction in heavily doped crystalline semiconductors. The conductivity is then obtained as below:

$$\sigma = \sigma_2 \exp\left(-\frac{w_2}{kT}\right) \tag{2.5}$$

where w_2 is the hopping energy for deep states and $\sigma_2 << \sigma_1$. This transport mechanism is the dominant mechanism at very low temperatures.

2.2 Density of States (DOS)

As discussed above, density of states remains a valid concept for non-crystalline materials and its distribution over band gap can be determined by various methods. Generally the shape of DOS is almost as in Figure 2.1, except for the deep states. Beyond E_C and E_V states are extended and in the mobility gap there are localized states including tail and deep states. For the DOS in the band gap we can use the exponential distribution as in crystalline materials and get the free carrier distribution in the bands. Yet obtaining the density of trap states in the mobility gap of amorphous silicon is a major issue.

There are several proposed approaches to measure the density of tail and deep defect states in the mobility gap. One widely used method for determining gap states is based on the field effect measurements [29], [30], [31]. Authors in ref [31] also prove that at room temperature, conduction is dominated by extended electron states. Certain research groups also have reported DOS measurement using junction capacitance measurement by different techniques. Capacitance-voltage measurement [32], deep level transient spectroscopy (DLTS) [33], thermally stimulated capacitance [33], and the drive level capacitance profiling [34] are different methods for obtaining DOS by capacitance measurement.

Another technique for determination of the DOS is measurement of space charge limited current (SCLC) [35] specifically near the mid gap. In addition, there are also some other method such as: measurement of frequency dependence of conduction and capacitance in α-Si Schottky diode [36] and transient and steady state photoconductivity (TPC and SPC) [37]. Figure 2.3 shows a comparison between results of different methods as discussed in [38].

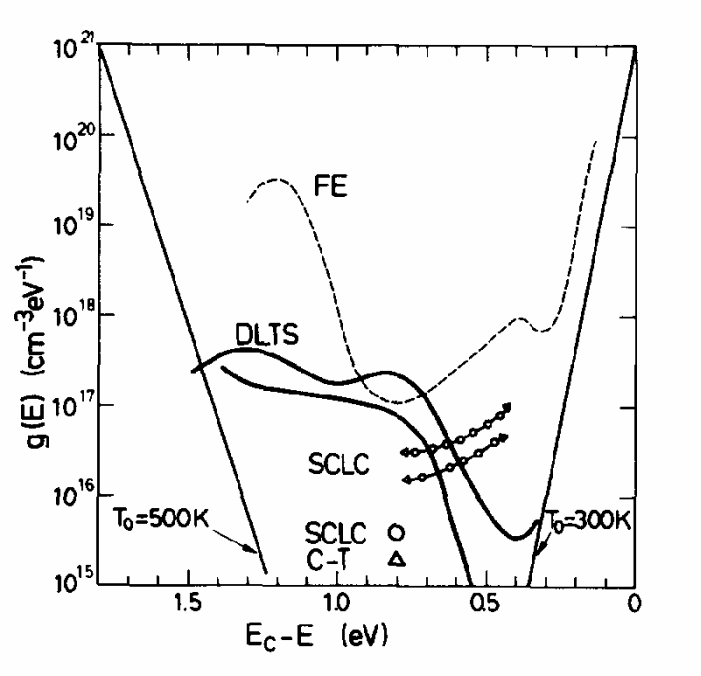


Figure 2. 3: Sketch of density of states measured by different techniques. T_0 is the parameter of tail states [38].

As is clear in the figure above, DOS measured with any field effect methods is larger than the other techniques, due to impact of interface state charges on field effect measurement [32]. But generally, density of states near the band gap changes between 2×10^{15} for intrinsic and 10^{18} cm^{-3} for highly doped amorphous silicon, and near the band edges, it varies between 2×10^{20} and 5×10^{22} cm^{-3}. Tiedje and Rose in [39], assuming power law for the distribution function of hopping time, proved that density of states in amorphous silicon mobility gap has exponential dependence on Fermi energy level position. Later on,

analytical expressions were derived to extract carrier concentration for device modeling purposes [40], [41], [42].

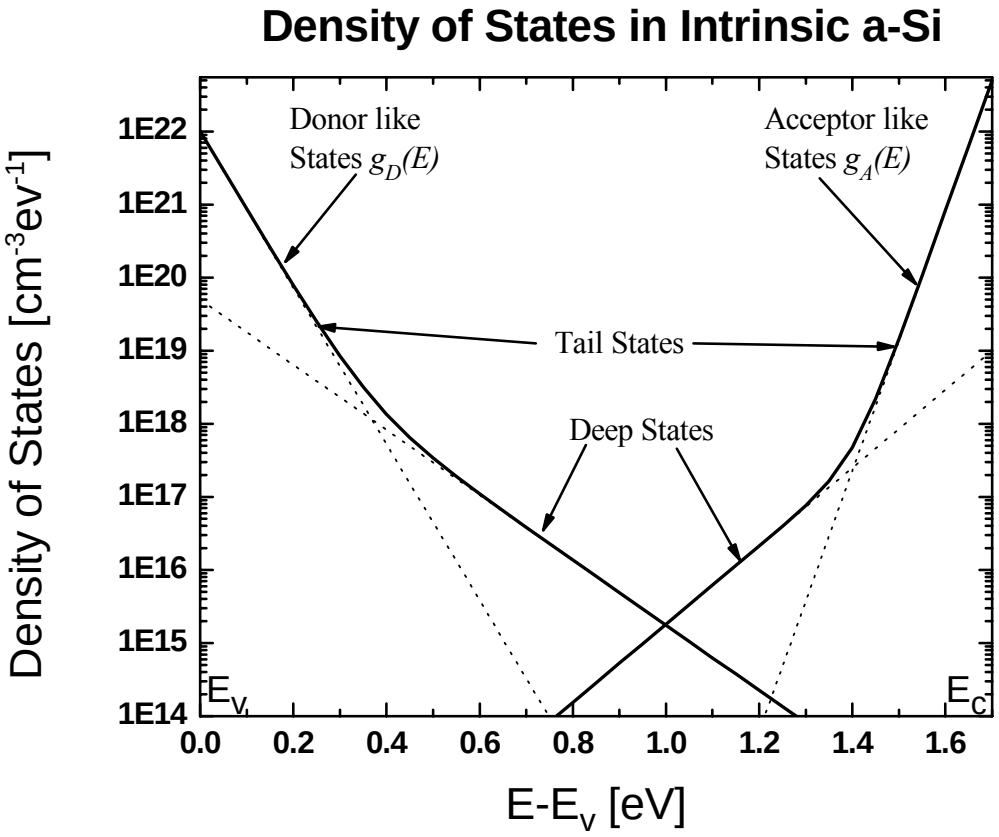


Figure 2. 4: Density of states (DOS) in the mobility gap of device-quality amorphous silicon. Note the asymmetry of the distribution toward conduction band, Adopted from [41].

Distribution of localized states in mobility gap can be presented as the exponential distribution of the both tail and deep states as in Figure 2.4. The tail and deep states near the conduction band above Fermi energy level are called acceptor like states, because they are neutral when empty and negatively charged when filled with an electron. Analogous to this, localized states near the valence band are donor like states which are neutral when

filled and positively charged while empty. Assuming energy of valence band located at zero, we can write the acceptor like DOS $g_A(E)$ as a function of energy as

$$g_A(E) = g_{tc} \exp\left(\frac{E - E_V}{kT_{tc}}\right) + g_{dc} \exp\left(\frac{E - E_V}{kT_{dc}}\right) \tag{2.6}$$

where E is the energy of each states from conduction band edge E_C, E_V is the valence band edge and k is Boltzmann constant. g_{tc} and g_{dc} present amount of density of states at the conduction band edge for tail and deep acceptor like states, respectively. Also T_{tc} and T_{dc} determine the slope of density of states for acceptor like states. Relation for donor like density of states $g_D(E)$ can be written in analogous to acceptor like density of states as in equation 2.7.

$$g_D(E) = g_{tv} \exp\left(-\frac{E}{kT_{tv}}\right) + g_{dv} \exp\left(-\frac{E}{kT_{dv}}\right) \tag{2.7}$$

here g_{tv} and g_{dv} are the tail and deep states level at valence band edge and T_{tv} and T_{dv} are their distribution slope, respectively. There are various amount of these parameters fitted in different works. We adopt our distribution of DOS with the data in [41], as sketched in Figure 2.4. Table 2.1 shows the amount of parameters we use in this thesis. As mentioned before, the density of states in the mobility gap is asymmetrical and total amount of donor like states are more than amount of acceptor like states, which lead the Fermi energy level shifted slightly toward conduction band for intrinsic material. Intrinsic material would thus behave like a lightly n-doped semiconductor [1].

Table 2. 1: Approximated values for exponential density of states formula, compiled from [37] and [41].

Tail States		Deep States	
DOS @E_C [$cm^{-3}eV^{-1}$]	Characteristics T [^oK]	DOS @E_V [$cm^{-3}eV^{-1}$]	Characteristics T [^oK]
$g_{tc} \sim 5\times10^{22}$	$T_{tc} \sim 300$	$g_{tv} \sim 1\times10^{22}$	$T_{tv} \sim 500$
$g_{dc} \sim 1\times10^{19}$	$T_{dc} \sim 1000$	$g_{dv} \sim 5\times10^{19}$	$T_{dv} \sim 1200$

Next step is to calculate amount of trapped and free charge carriers, based on obtained density of states in the bands and mobility edge. To calculate trapped electrons n_t and holes p_t, we multiply the proper density of states with probability of occupation for each states, or in another word, Fermi-Dirac function *f(E)*. So we can write

$$n_t = \int_{E_V}^{E_C} g_A(E) f(E) dE \tag{2.8}$$

and similarly for holes

$$p_t = \int_{E_V}^{E_C} g_D(E)\left(1 - f(E)\right) dE \tag{2.9}$$

The Fermi-Dirac function in equilibrium condition is defined as

$$f(E) = \frac{1}{1 + \exp\left(\frac{E - E_F}{kT}\right)} \tag{2.10}$$

Shaw *et al.* in [41] numerically calculated equations 2.8 and 2.9 and fitted two polynomials to the result, which is too complicated to reach a simple device model. Tsai *et al.* also approximate the Fermi-Dirac function to solve two integrals analytically for donor and acceptor like states, but still the result for charge carrier distribution seems very complex [42]. Shur *et al.* in their work in [40] solved these equations and obtained an approximate exponential distribution for trapped charge carriers, depending on whether they have characteristics temperature more or less than $T \sim 300$ ^{o}K. This distribution is valid as long as E_F is more than a few kT far from mobility edge, which is the case for amorphous silicon. Due to importance of electrons in the amorphous silicon devices we only investigate negatively charged carrier distribution. So we can write the trapped electrons in localized states as

$$n_t(E_F) = N_{tc} \exp\left(\frac{E_F - E_C}{kT_{tc}}\right) + N_{dc} \exp\left(\frac{E_F - E_C}{kT_{dc}}\right) \tag{2.11}$$

where T_{tc} and T_{dc} are the same amount as in acceptor like DOS distribution and N_{tc} and N_{dc} are the amount of tail and deep state electrons near the conduction band edge. Some expressions for these two parameters are obtained in [40]. So based on Shaw's approximation, parameters for Equation 2.11 can be found in Table 2.2. Obtained carrier distribution is plotted in Figure 2.5.

Table 2. 2: Approximated values for trapped electron exponential model for T=300 ^{o}K, compiled from [41].

Type	DOS @E_V [$cm^{-3}eV^{-1}$]	Characteristics T [^{o}K]
Tail States	$N_{tv} \sim 1\times10^{21}$	$T_{tc} \sim 300$
Deep States	$N_{dv} \sim 5\times10^{18}$	$T_{dc} \sim 1000$

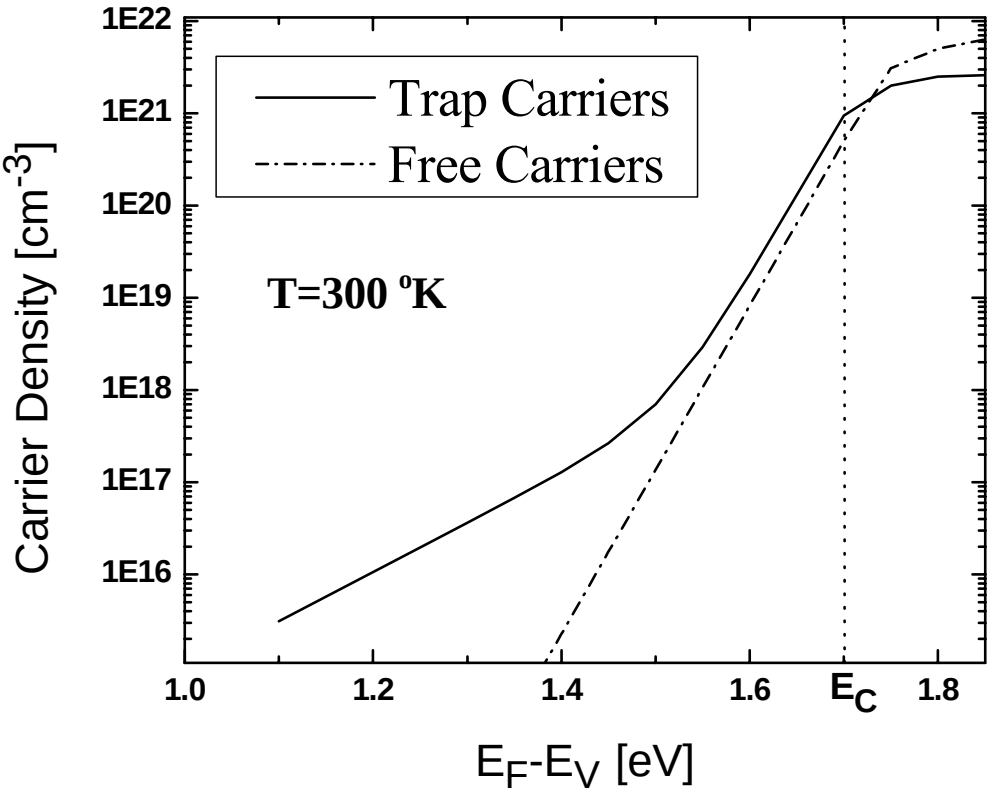


Figure 2. 5: Free and trapped charges versus Fermi level position for DOS distribution in Figure 2.4 as adopted from[41].

So far we discussed the density of states in the mobility gap but as it is shown in Figure 2.5, slopes of both extended and localized states decreased and do not follow the exponential forms any more. In crystalline semiconductors density of states which starts from conduction band edge is proportional to square root of energy ($E^{0.5}$). Mott [2] assumed for the distribution of DOS in the band to have a form like,

$$N_t(E) \propto E^n \tag{2.12}$$

where n is an empirical parameter. Figure 2.5 shows these two power relations in the conduction band beyond E_C.

Assume characteristics temperature for certain mobility gap states as T_o, and T is the lattice temperature. Then if the dispersion parameter, T_o/T, becomes greater than unity, density of states distribution would be less than Fermi-Dirac distribution function and most of the carriers would locate close to the Fermi level E_F. The characteristic temperature in the acceptor like tail states is very close to thermal energy at room temperature and consequently, when the Fermi level is in tail states, most of the charge is actually located above the Fermi level. So the ratio of the mobile to localized charge carriers is less sensitive to the shift of Fermi level as the charge distribution in the localized states is less dependant on Fermi level position [40]. Thus due to the amount of characteristic temperature for the case of obtained deep (T_{dc}=1000 ^{o}K) and tail (T_{tc}=300 ^{o}K) states we can neglect amount of deep electrons and only take the first term in the right hand side of Equation 2.11 into account. So finally, the density of trapped electrons can be approximated as

$$n_t(E_F) = N_{tc} \exp\left(\frac{E_F - E_C}{kT_{tc}}\right) \tag{2.13}$$

Figure 2.5 also shows the distribution of free carriers in the band. This can be calculated from

$$n(E_F) = N_C \exp\left(\frac{E_F - E_C}{kT}\right) \tag{2.14}$$

where N_C is the effective density of band states and is approximately around 10^{21}[$cm^{-3}eV^{-1}$] [39].

2.3 Field Effect Mobility

After calculating charge concentrations in the semiconductor, one of the important parameters to derive is field effect mobility. In amorphous silicon due to presence of localized states in which the carriers can transport only by hopping, mobility is very different from band mobility. Mott [2] assumed that there is absolutely zero mobility in

localized states and calculated the total mobility by obtaining the fraction of carriers in the band. These band carriers can move easily in the band and their transport is described by field-effect mobility. The electron mobility in acceptor like states can be written as

$$\mu_D = \mu_0 \left(\frac{n_0}{n_t + n_0} \right) \tag{2.15}$$

here μ_0 is the mobility at the band , and n_0 is the amount of free carriers in the band. Field effect mobility then can be obtained by substituting n_0 and n_t from (2.11) and (2.14). Figure 2.6 shows calculated field-effect mobility of different temperatures as a function of Fermi level. As temperature increases, field effect mobility also increases due to more excitation of electrons from below Fermi level to conduction band. Characteristic temperature of conduction band tail for simulated sample is T_c=300 ^{o}K. For temperatures above this temperature, conduction would become non-dispersive as observed in experiments [39]. So we just calculate the mobility up to this critical temperature. This is the basis of voltage dependency of mobility in amorphous silicon devices.

Approximately, drift mobility can be extracted and written as an Arrhenius like behaving parameter [2], as observed in experiments.

$$\mu_{eff} = \mu_0 \frac{N_c}{N_t} \exp\left(-\frac{E_F}{kT} \right) \tag{2.16}$$

For simplicity we use Equation (2.12) instead of (2.11) to substitute into (2.15). First we obtain a relation for density of band carriers in terms of trapped carriers as in [43]

$$n_0 = \frac{N_c}{N_t^{\alpha}} n_t^{\alpha/2} \tag{2.17}$$

where α is the dispersion parameter and can be defined as following

$$\alpha = \frac{2T_t}{T} \tag{2.18}$$

and T_t is the characteristic temperature in (2.13). This parameter (α) will later appear in TFT characteristics. Now for certain amount of carrier concentration (N_0), the field effect mobility is defined as [43]:

$$\mu_{eff} = \mu_0 \frac{N_c}{N_0}\left(\frac{N_0}{N_t}\right)^{\alpha/2} \tag{2.19}$$

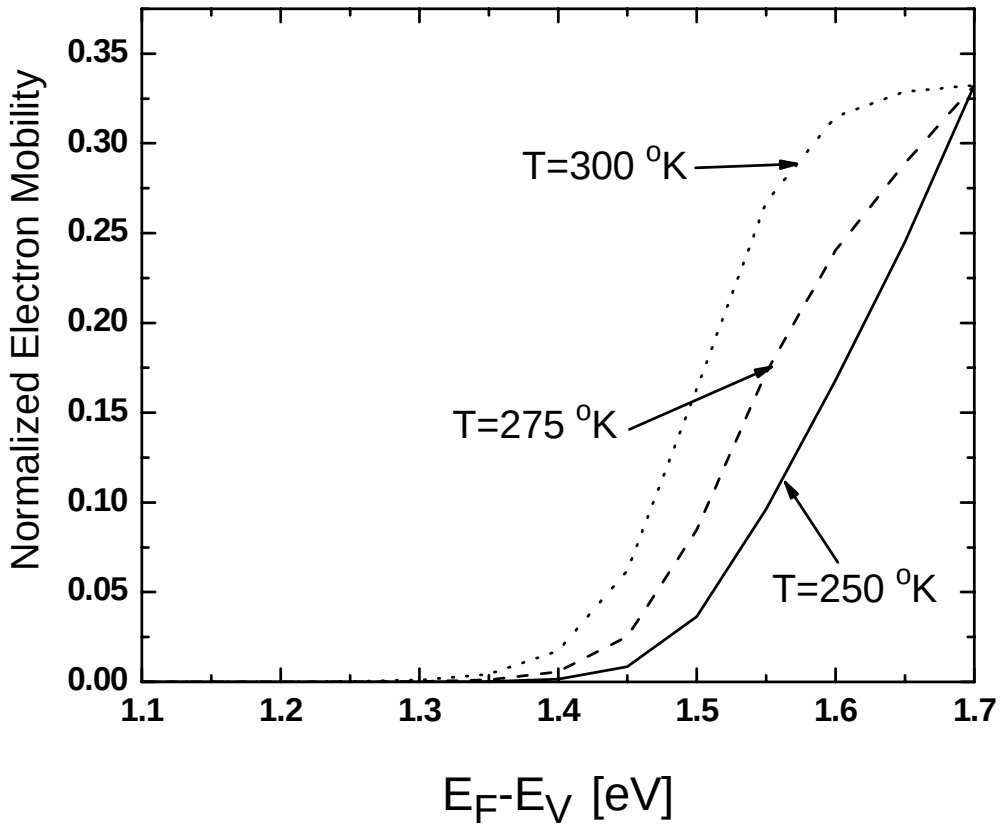


Figure 2. 6: Ratio of Field effect mobility to band mobility as a function of Fermi level for different temperatures.

The band mobility is typically around 10-20 cm^2/Vs at 300 ^oK, and will be reduced by increasing the temperature due to electron scattering in the band [41], as of Mott's work in [2] that extracts a *1/T* dependence of band mobility.

2.4 Transport in Amorphous Silicon

2.4.1 Space Charge Limited Current (SCLC)

Current can exists in the thin insulating materials, far away from Ohmic current. Thermal carriers in low conductivity materials are generally negligible and carriers injected from the contacts play major role in conduction. This kind of current, which is called space charge limited current (SCLC), follows voltage super-linearly and flows only if one of two contacts act as Ohmic contact. The theory of SCLC was developed for vacuum diodes at the beginning of 20th century. Here, we study the SCLC in parallel plate capacitor with semi-insulating materials such as dielectric. Presence of traps makes actual SCL current much less than what in the crystals, due to accumulation of some portion of charges in trapped states and hence, separation of mobile and non-mobile charges. These traps not only decrease amount of current, but also change the shape of I-V characteristics. This forms the basis for extracting trap density from I-V measurement [35].

There are three fundamental equations that govern SCL regime

$$J = \rho\mu(F)F \tag{2.20}$$

$$\frac{dF}{dx} = \frac{\rho}{\varepsilon} \tag{2.21}$$

$$\frac{dV}{dx} = F \tag{2.22}$$

where ρ is the amount of the space charge density, ε is electric permittivity, and F is the electric field. Note that, here the diffusion current has been neglected in (2.20). Solving Eq 2.20-2.22 we can obtain,

$$J_{SCL} = P\varepsilon\mu(F)\frac{V^2}{L^3} \tag{2.23}$$

where P is the correction factor for the SCLC and is a weak function of applied voltage [44] but is usually assumed constant and equal to 9/8 [46]. This equation does not take trapped charges into account. Here mobility is a function of electric field and may increase with electric field.

As it is clear from (2.23) even in semiconductors without trap states, SCLC increases as a quadratic function of voltage. Moreover, for shorter electrode spacing, current increases super-linearly which determines one of the most important characteristics of SCLC. Also because of presence of space charges between two electrodes, capacitance would increase from its original parallel plat capacitance (C_0) [44] as

$$C = C_0\left(1+\frac{1}{p}\right) \tag{2.24}$$

where p is

$$p = \frac{d\ln J}{d\ln V} \tag{2.25}$$

Now, assume we have electron trapping sites in the semiconductor and the distribution of trapped charge follows (2.13). Then by solving Equations 2.20 – 2.22 for this material, the SCL current is obtained as

$$J_{SCL} = P\varepsilon^{\alpha/2}\mu(F)\frac{V^{\alpha/2+1}}{L^{\alpha+1}} \tag{2.26}$$

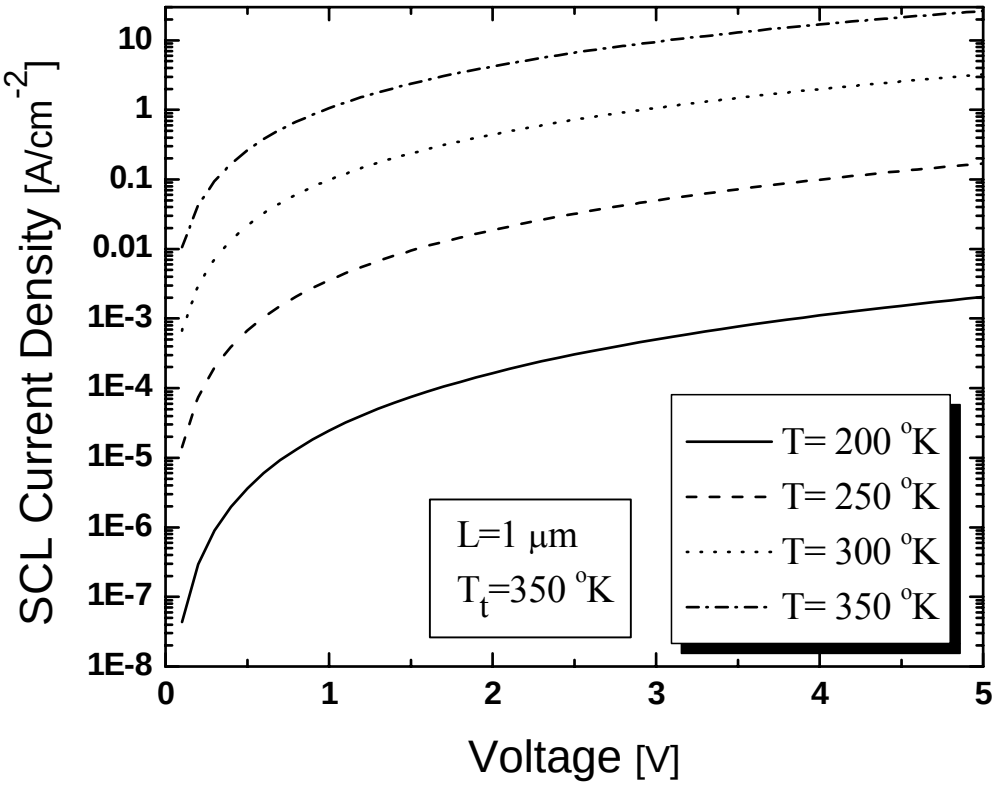


Figure 2. 7: Space charge limited current (SCLC) density for 1 μm thick amorphous silicon with charge distribution presented in section 2.2 in various temperatures.

where P is again a correction factor that will now depend on both electric field and temperature. Also the material dispersion parameter is α. This equation is valid only for samples in which $T_t \geq T$ or $\alpha \geq 2$. Otherwise, the relation for the material without trap, Eq (2.23), governs with the mobility of disordered semiconductor substituted [45]. We see that for $\alpha = 2$ and the same correction factor, this formula reduces to (2.23) for semiconductor without trap. It can be seen that for lower temperature the power law increases, but the coefficient of current density rises too. Thus, for very low temperatures the current starts to show Ohmic current characteristics [47]. So, temperature reduction can be used to suppress the SCLC. Figure 2.7 shows calculated SCLC for 1 μm thick a-Si:H capacitor at various

temperatures. It is observed that, in spite of less current level, the characteristics of lower temperature have higher power law and more rapid increase of SCL current with applied voltage.

On the other hand, it is good to note that by increasing the voltage and consequently the Fermi level position mobility raises helping amount of SCLC increase. But as of in Equation 2.26 and Figure 2.6 this dependence is found to be too weak to consider.

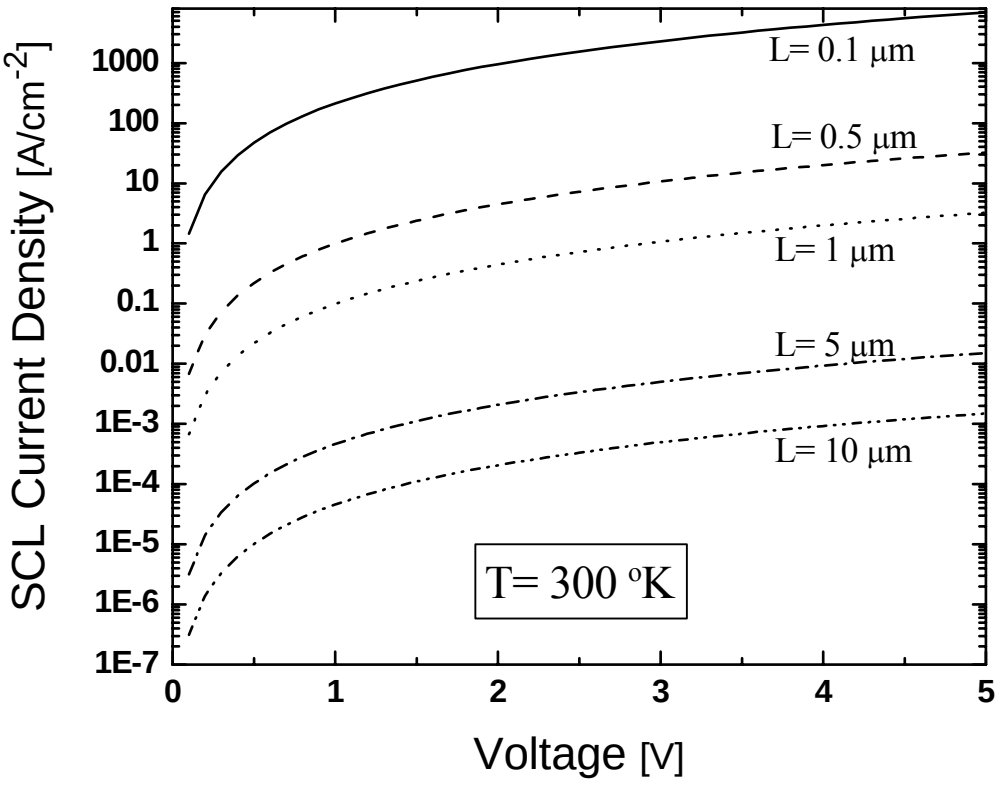


Figure 2. 8: Space charge limited current (SCLC) density for different thickness amorphous silicon samples at 300 °K.

Another aspect of (2.26) is the dependency of SCLC to length of the sample. Current has the strong dependency on length which may become even stronger in shorter lengths.

Figure 2.8 depicts the SCL current for different capacitor spacings. It is interesting to note that the current drops more than three orders of magnitude if the length shortened only by one order of magnitude. For example at V = 4 V, the current density for 0.1 μm inter-electrode spacing is 4.2 kA/cm^{-2} while it is just 1.9 A/cm^{-2} for 1 μm spacing.

Similar to the case of trap-free sample, here we have even more capacitance due to space charge density. This increase is mostly because more charges are stored in the investigated material with high trap density. Equation (2.27) presents amount of capacitance [44] in comparison to trap-free sample (2.24)

$$C = C_0\left(1+\frac{\alpha}{2p}\right) \tag{2.27}$$

where p is the same as in (2.25).

Finally, it is worthy to note that, this mechanism is applicable to extract field-dependant mobility in organic semiconductors like conjugated polymers, molecularly doped polymers, organic glasses, and molecular organic materials [44], [48].

2.4.2 Drift-Diffusion regime

Up to here, we have assumed that either the applied voltage is so strong or the spacing is very large that the injected carriers from Ohmic contacts do not meet each other, increasing minimum amount of carriers in the conduction band. So, injected space charges can flow in the band, building SCLC. In the case of low applied field and short spacing (as small as carriers diffusion length in the band) although smaller amount of injected carriers lowers the free carriers, short distance between contacts let the carrier's exponential distribution tail reach the other contact. This phenomenon increases net amount of free carriers in the band. In this regime of transport, carriers both drift and diffuse. The current associated with the above mechanism is called "drift-diffusion" current. In other words, drift-diffusion current is the drift current of carriers diffused from contacts.

Solving Poisson's and current continuity equations for the case of short n^+-n^--n^+ structure Nishizawa *et al.* [49] showed that the current can be solved as:

$$J = \frac{16\varepsilon kT\mu}{q}\frac{V}{L^3} \tag{2.28}$$

This current shows a linear dependence on voltage, which is pretty similar to Ohmic current. But drift-diffusion current changes drastically with length, which is attributed to the diffusion of carriers from contact to semiconductor.

We have numerically solved both continuity equation and Poisson's equation together for an amorphous silicon material using MEDICI software. Amorphous material properties are defined for the software the same as the properties explained in Section 2.2. Figure 2.9 shows the simulated structure. The simulation was run for a film with thickness of 50 nm and different intrinsic layer length from 100 nm to 1mm. Also length of each n^+ region set to 0.1 of the intrinsic film length. Electric field was varied over five orders of magnitudes for each length to investigate different transport regimes.

Figure 2. 9: Schematic of the simulated structure.

Two n^+ regions are included to have good amount of injections or in other words to have Ohmic contacts. Figure 2.10 shows the current versus electric field for different intrinsic layer thicknesses. Three different transport regimes are observable in this plot. It can be seen that Ohmic regime has the electrical filed- and length-independent conductivity, which means that current flow is only due to thermal carriers in the band and not any injected ones. As the length is reduced, two other regimes (SCLC and drift-diffusion) start competing. For the lower electrical fields drift-diffusion can represent more carriers in the band, while for higher electrical fields injected carriers increase until the SCLC becomes dominant at very high electrical fields.

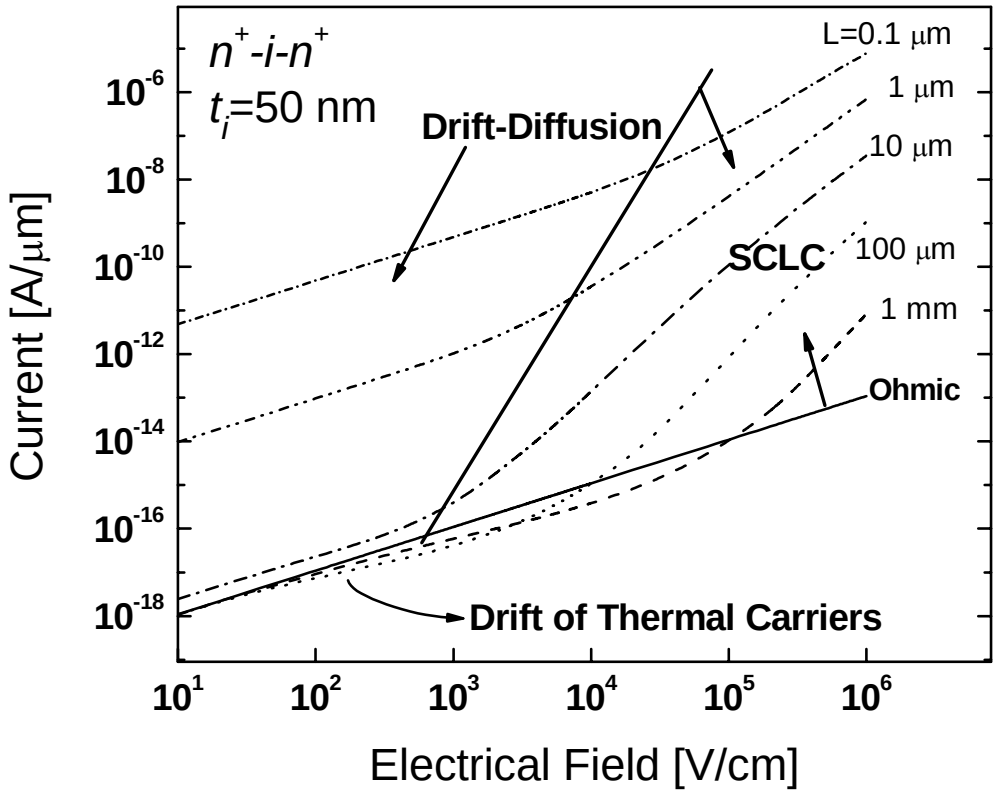


Figure 2. 10: Simulated current versus electrical field for different intrinsic layer lengths.

Table 2. 3: Current density versus electrical field relations for different transport regimes, highlighting dependence of each on length.

Transport Regime	*Ohmic*	*Drift-Diffusion*	*SCLC*
Current Density (J)	$q\mu NE$	$\frac{16\varepsilon kT\mu}{q}\frac{E}{L^2}$	$\frac{9}{8}\varepsilon\mu\frac{E^2}{L}$

Dependence on length is also extractable from Figure 2.10, as in the same electrical field, the difference from each step of length to another in SCLC region is close to one order of current magnitude while for drift-diffusion region this difference is close to two ordres. This confirms the J-E relations brought in Table 2.3. Mackenzie *et al.* in their work [50] measured I-V of the same structure with intrinsic a-Si:H length of 650 nm at different temperatures. They got the result close to ours, as their sample at 300 ^{o}K switched from drift-diffusion regime to SCLC regime at 4×10^{3} V/cm which is close to our simulation result ($<10^{4}$ v/cm).

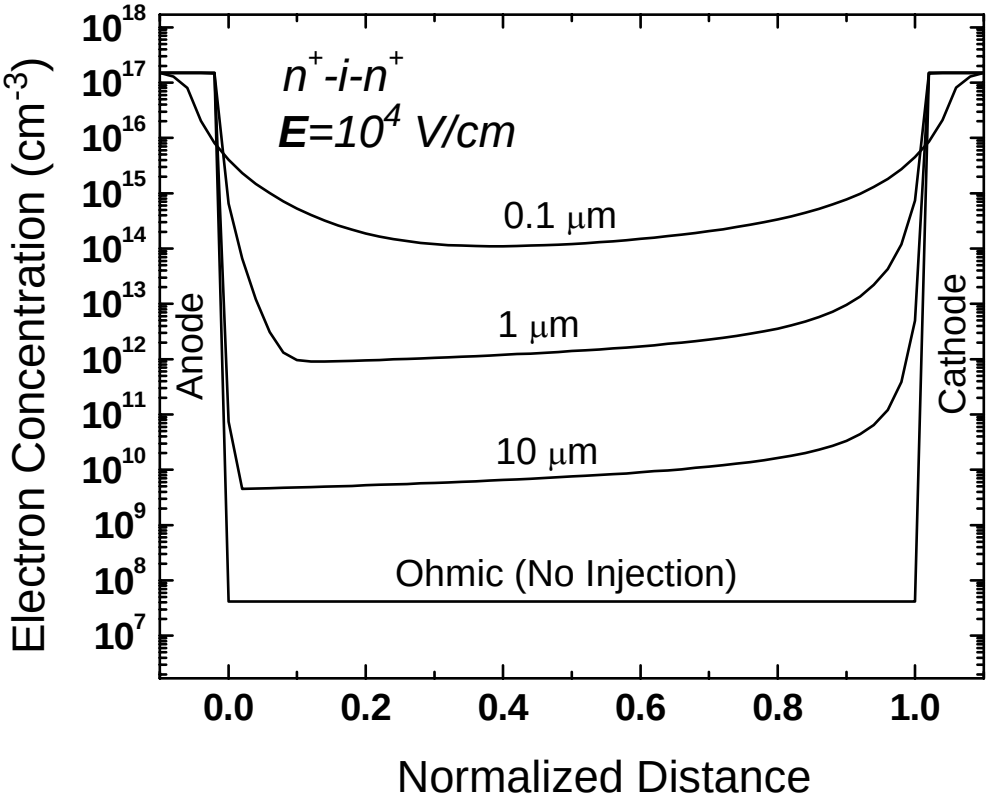


Figure 2. 11: Electrons band concentration along the intrinsic material at electrical field of 10^{4} V/cm.

Figure 2.11 shows electron band concentration along the intrinsic material at electrical field of10^4 V/cm. Positive voltage is applied to anode electrode and so the electrons are injected from cathode. This curve gives good insight to different regimes and carrier distribution in each one. Comparing Figures 2.10 at the E = 10^4 V/cm and 2.11 implies that the 10 μm sample is completely in SCLC regime whereas the 100 nm sample is completely in drift-diffusion regime. The 1 μm sample is located in the transition region between two regimes. We can see that in SCLC regime carrier concentration is more than thermal carriers but still these carriers do not interact with carriers from the other. So they decay before reaching the other contact. But in drift diffusion regime as the length of sample is compared to carrier diffusion length, injected carriers meet at the middle of the device and increase minimum amount of carriers in the band.

Chapter 3: Thin Film Transistors

Amorphous silicon based thin film transistor (TFT) has been developing over the past twenty five years since its invention in 1979 [5]. Nowadays, it is widely used in various flat panel electronic circuits and is fabricated on the backplane of displays and imagers. This chapter first discusses conventional lateral TFT structure and its fabrication process. Then different electrical characteristics of conventional TFT will be reviewed. Finally structure, fabrication, and electrical characteristics of vertical TFT (VTFT) will be presented and investigated.

3.1 Lateral Thin Film Transistors

Concept of thin film transistors is very similar to crystalline MOS devices. The conductivity between drain and source terminals is modulated by an applied gate voltage. Gate voltage controls band bending and Fermi level at the semiconductor-insulator interface (increases amount of Fermi energy level). Positive voltage at the gate causes accumulation of electrons at front interface and formation of the high conductivity channel [51]. In this section, we first describe different TFT structures and then introduce fabrication process for them. Later, electrical characteristics such as I-V and C-V

characteristics will be presented. Finally, we will review device breakdown in amorphous silicon based structures.

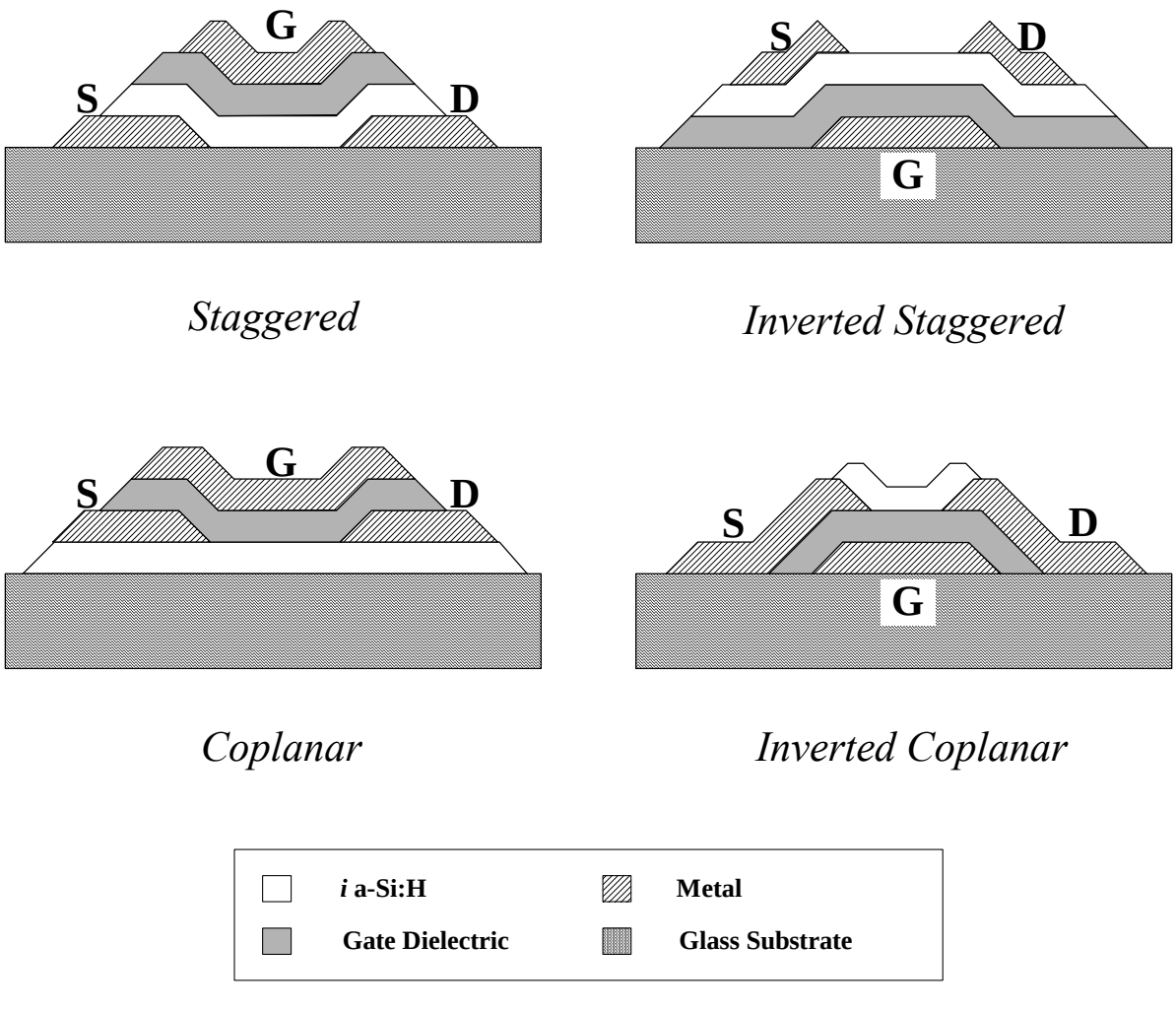


Figure 3. 1: Different configurations for lateral TFTs [52].

3.1.1 Structure

Generally, there are four different types of lateral thin film transistors (Figure 3.1). The major difference between these structures is defined by the order of deposition for semiconductor, gate insulator, drain-source contact, and gate electrode layers. As is clear from Figure 3.1, for the staggered structures, the intrinsic layer is located between source/drain contacts and gate metal, while for coplanar structure all of these three electrodes are located in the same side of the amorphous silicon film, similar to crystalline MOSFET structures. In the inverted structures the gate electrode is located at the bottom of the transistor structure. This means that the active amorphous silicon layer and source and drain contacts are deposited on top of the gate insulator which is typical silicon nitride. Interface defects reduce quality of a-Si:H during growth degrading the active part of the device in non-inverted TFT. Practically, best amorphous silicon based TFTs are fabricated with inverted-staggered structure [52]. This fact has been confirmed in ref [53], which shows that the field effect mobility in inverted staggered structure is about 30% higher than in staggered TFT. Another benefit of inverted structures is that they can shield the back light of LCD penetrating into transistor and hence eliminate photo-generated leakage current in the LCD backplane electronics.

In this thesis we just study the characteristics of inverted staggered a-Si:H TFTs. These transistors are fabricated in a five mask process (Figure 3.2) [54]. In this process, after metal (Mo or Cr) sputtering for gate, first mask is applied to pattern it. Then, a-SiN_x/ a-Si:H / a-SiN_x layers are deposited by PECVD respectively. Mask 2 patterns a top nitride and then drain and source n^+ a-Si and passivation nitride films are deposited afterward. Mask 3 separates the drain and source following mask 4 opening the contact via. Finally the Aluminum is deposited for contacts and patterned with the mask 5. The fabricated device also needs to be annealed to reduce defects and sinter contact resistance. Figure 3.2 shows briefly different masking processes for TFT.

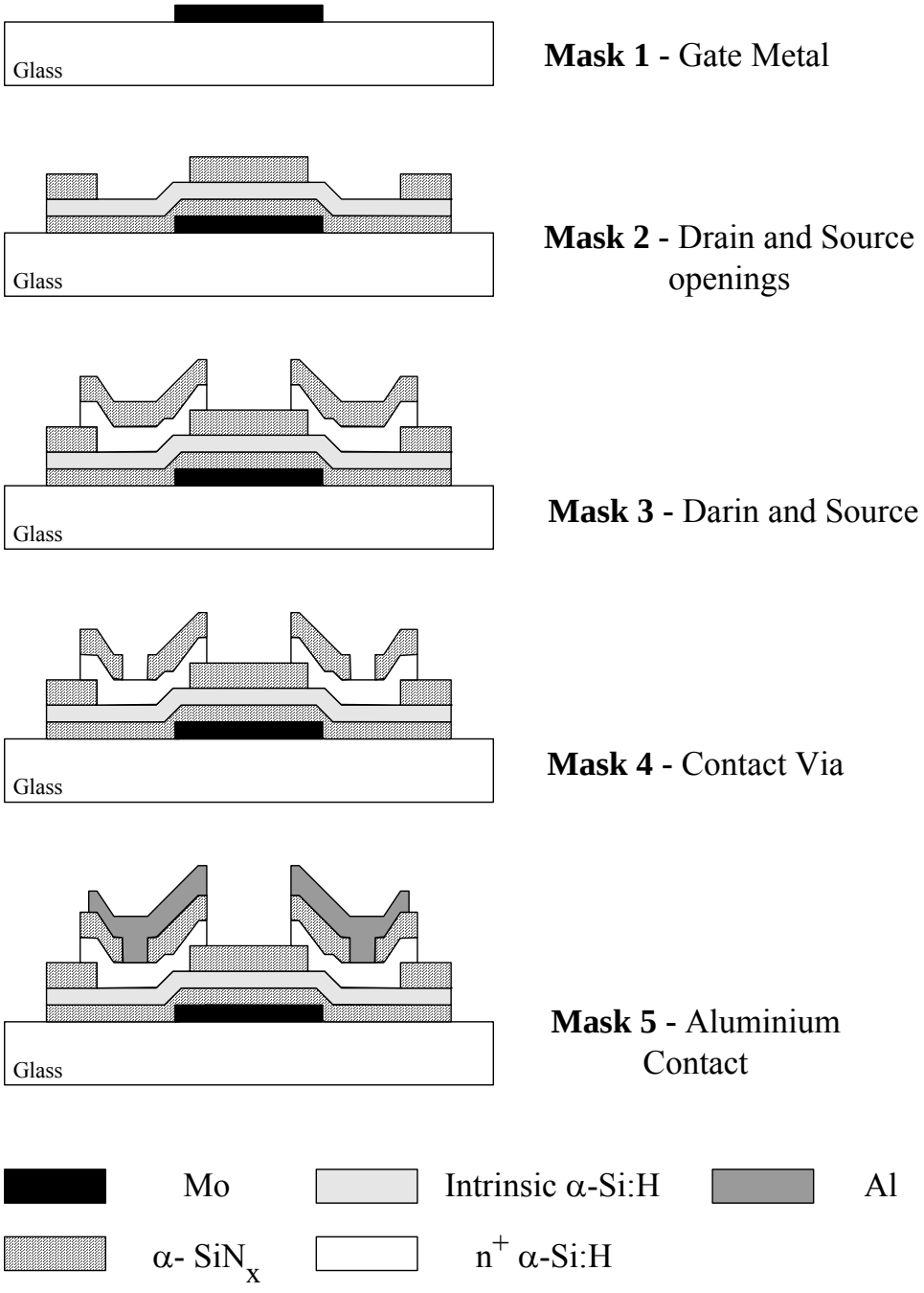


Figure 3. 2: Fabrication Process for Inverted-Staggered a-Si:H TFT [54].

3.1.2 Characteristic

As we discussed in chapter 2, amorphous silicon films suffer from low mobility. For electrons, field effect mobility is about 0.5-1 cm^2/V.Sec in TFT. Also because of higher amount of donor-like defects, the mobility of holes is two orders of magnitude less than that of electrons; therefore only NMOS devices are parctically feasible. Figures 3.3 and 3.4 show the transfer and output characteristics of an N-type a-Si:H inverted staggered TFT fabricated in aSiDIC group, University of Waterloo [55]. The fabricated TFT (W/L = 50/20 μm) has a dynamic range of about 8 ($I_{ON}/I_{OFF} = 10^8$) and a leakage current of 10 fA at the drain source voltage of 5 V. No current crowding effect is observed on output characteristics, which indicates good quality of source and drain contacts.

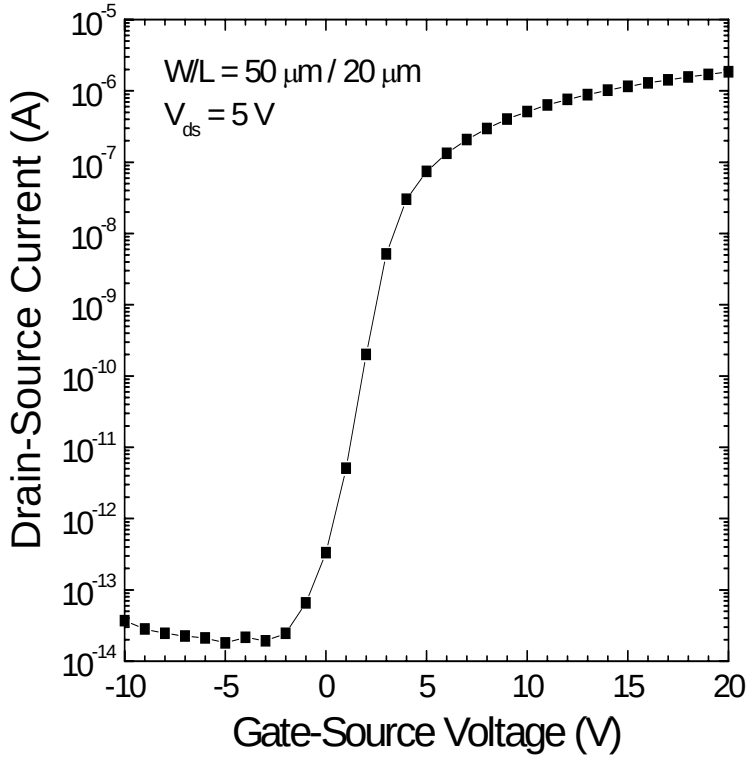


Figure 3. 3: Transfer characteristics of a-Si:H TFT fabricated in a-SiDIC group, University of waterloo [55].

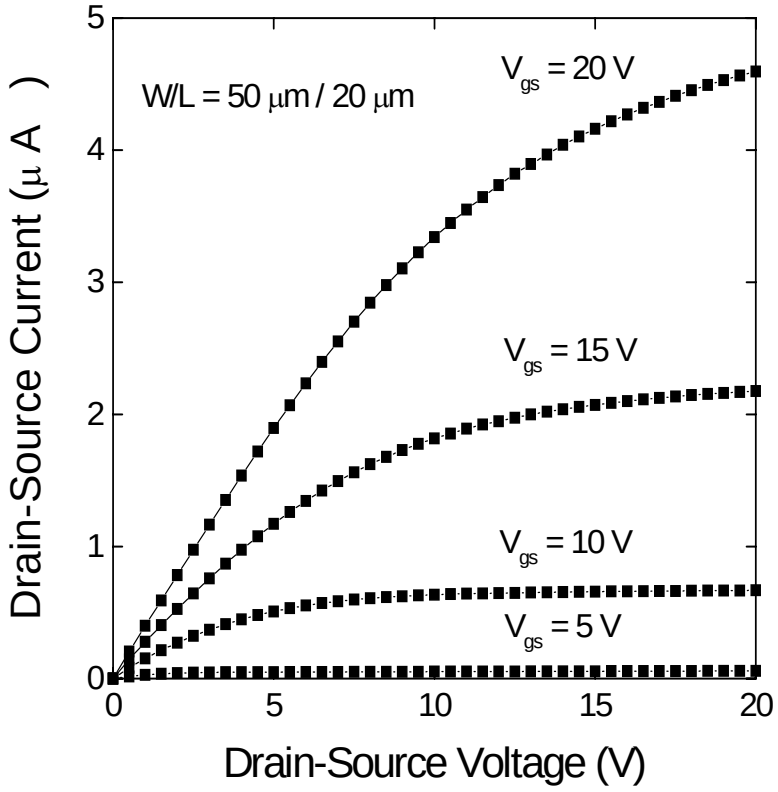
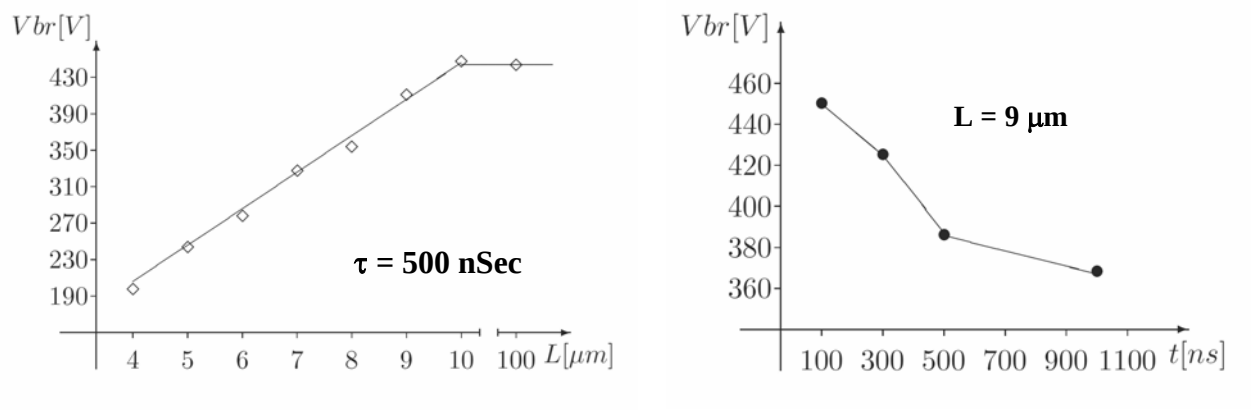


Figure 3. 4: Output characteristics of a-Si:H TFT fabricated in a-SiDIC group, University of waterloo [55].

3.1.3 Breakdown

Since TFTs are used in AMLCD and AMOLED backplane drivers, they have to be capable of tolerating high voltage and high current. This high level of voltage and current can cause failure in TFTs. Therefore, it is very important to study TFT breakdown mechanisms. Basically, there are two major mechanisms of breakdown known for TFTs. One is caused by high gate voltage and the other is due to high drain voltage. The former is the material breakdown and the later is a thermal phenomenon. In this section these two effects are briefly discussed.

In crystalline silicon based MOS transistors, increasing drain voltage extends depletion region at the drain side until joining the source side depletion region, which is called punch through. Under this condition, drain current increases until the device reaches the thermal breakdown. This breakdown voltage can be defined as the voltage at which the drain current increases sharply accompanied by a decrease in the drain voltage. The interval between punch through and breakdown is called snap back. In this regime if the applied voltage is removed, transistor survives and will not damage. In a-Si:H TFTs because of the traps in the conducting materials, transistor does not show any snap back behavior during breakdown. On the other hand, high contact resistances, creates a large voltage drop across contacts and lowers level of the drain current. Therefore, TFT can thermally break down especially from the drain side, where it experiences higher electrical field. Thus, it can be concluded that the main mechanism of breakdown is impact ionization. As shown in Fig 3.5, the breakdown voltage strongly depends on the channel length and stress time, which confirms presence of a weak punch through effect in the device [56], [57].



(a) **(b)**

Figure 3. 5: The average value of the breakdown voltage versus a) different channel lengths b) different stress times [57].

Golo *et al.* [57] show that for long channel TFTs, there is almost no effect of punch through; the breakdown voltage remains constant with the channel length. But as the channel length starts to shrink below 10 μm, breakdown voltage follows a linear drop with the channel length by rate of ~ 40 V/μm. So for the 1μm channel length, it should be less than 70V. However compared to longer transistors, TFTs with the channel lengths L< 1μm are affected much more by drain induced barrier lowering (DIBL). On the other hand, dependence of breakdown voltage on stress time is due to the dominance of the breakdown due to thermal process, which is called impact ionization [56].

Prior to breakdown, different TFT parameters, such as sub-threshold slope and threshold voltage, start to degrade. These can be attributed to the trapping of charges in the dielectric, interface and film traps during stress and also to trap state generation in the energy gap; a part of these stress induced traps can be recovered by thermal annealing. From the fact that the concentration of the dangling bonds has an Arhenius type temperature dependence, the transistor breaks down faster in higher temperature. On the other hand, as stress current is applied, TFT warms up and this causes breakdown to take place earlier than expected. This phenomenon is called self heating [56].

The other breakdown mechanism deals with the breakdown of the gate dielectric due to high applied gate voltage. Due to the very thin dielectric of TFTs, in the range of hundred nanometers, small voltages may cause very high electric field in the dielectric. This can cause material breakdown at gate. Typically, the breakdown viltage for silicon nitride gate dielectric is a few MV per cm of the thickness. For example a TFT with 250 nm dielectric thickness can tolerate up to 150 V of gate bias, while for 50 nm thick dielectric, maximum gate bias can be as low as 30 V.

3.2 Vertical Thin Film Transistors (VTFT)

3.2.1 History of Vertical Channel TFTs

Since first amorphous silicon TFT fabrication [5], people have been thinking about shrinking the channel length. Vertical structure is one choice for implementing very short channel devices. Uchida *et al.* proposed the first vertical amorphous silicon TFT in1984 [58], [59], Figure 3.6a. This structure is very similar to vertical MOS, and stacked n^+-n^--n^+ layers act as source, channel and drain, which are gated by metal (M). This structure suffers from high off-current due to high space charge limited current, which flows from inner parts of the n^- a-Si:H film and can not be controlled by gate [59]. Figure 3.6b has added a p-type material to suppress the SCLC in the off mode. Although this structure reduces effective channel length, p-type amorphous material can barely be inverted to make channel due to high defect density. The solution is to eliminate the p-type amorphous material close to channel. Figure 3.6c depicts this modification, where a thin intrinsic amorphous material is deposited at the sidewall of the p type a-Si:H. Now by thinning the intrinsic material, SCLC can be decreased to obtain higher ON/OFF current ratio. But still n-p-n structure between drain and source may cause small amount of leakage current in the transistor off state. So by replacing p-type layer with an intrinsic layer, this leakage current can be reduced to intrinsic material leakage, which is negligible. Figure 3.6d shows improved structure with M/I/i a-Si:H layers for gate metal to channel, and M/n^+/I/n^+/M layers for drain metal to source metal. Later, the VTFT structure was enhanced again and different major changes were applied to the structure, such as using μc-Si:H to improve contact resistance [60], [61] and using p-type layer in between insulator to reduce high field effects [62]. Therefore, various characteristics have been reported in literature. Some authors also used poly-silicon as semiconductor for the channel to obtain higher mobility [63].

There are also two major types of reported TFT structures; top gate and bottom gate TFT [63], [64], [65]. Moreover, different materials have been applied for gate dielectric, such as

silicon nitride, silicon oxide etc, and for the channel such as SiC [66] excimer-laser a-Si [64] and organic semiconductors [67], [68].

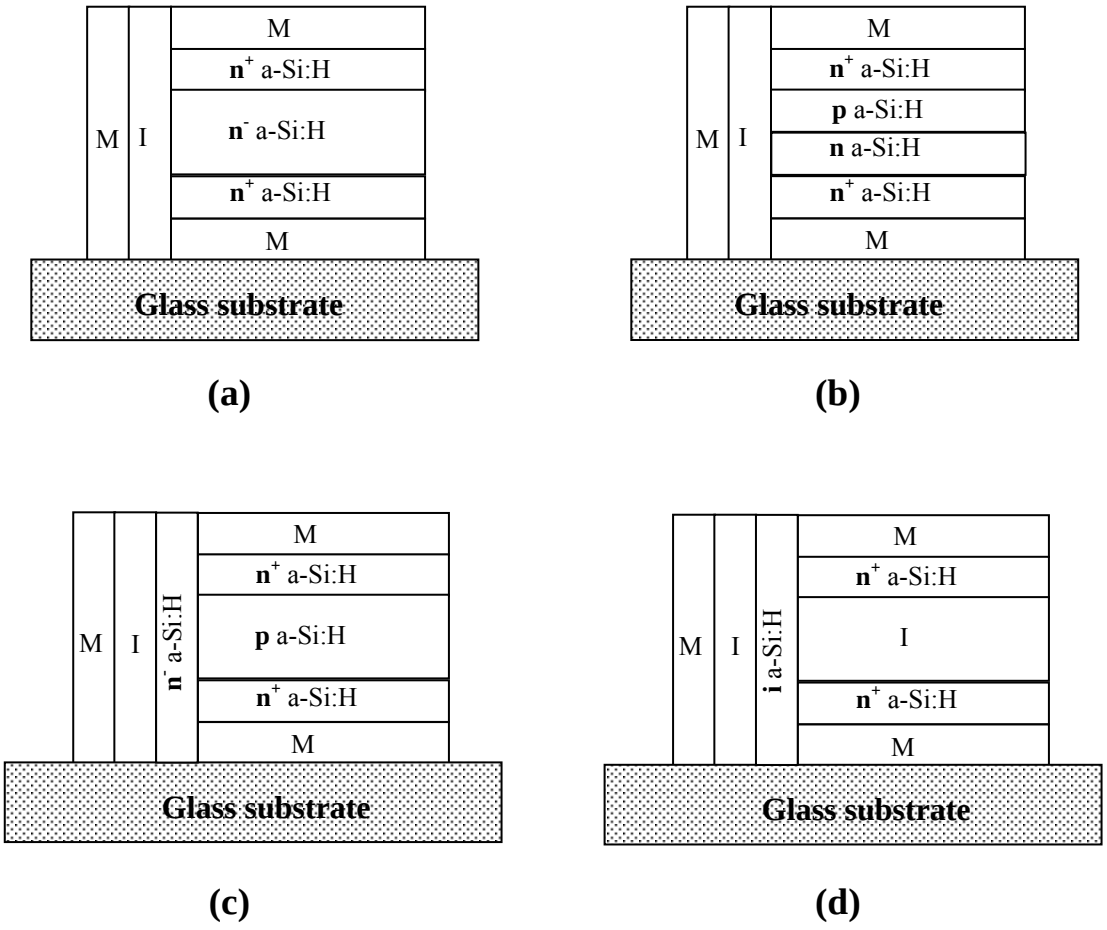


Figure 3. 6: Cross section of various vertical TFT structures [58], "M" and "I" denote metal and insulator, respectively.

3.2.2 Structure under Study

3.2.2.1 VTFT Device Structure

The structure in Figure 3.6d has the best characteristics among different available structures. We have started with the concepts of this structure and come up with the device structure shown in the Figure 3.7.

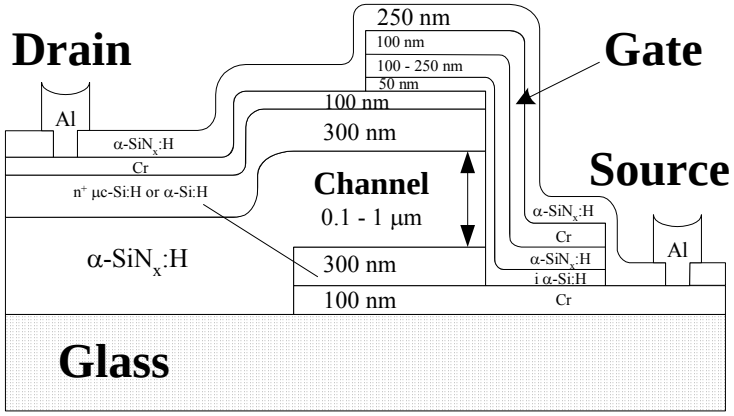


Figure 3. 7: Fabricated and investigated a-Si:H VTFT device structure [19].

This structure basically is very similar to staggered TFT structure in terms of sequence of deposition of source/drain, channel, gate dielectric, and gate. Thicknesses of the different layers can vary regarding physical properties and fabrication limitations. For example channel thickness can vary from 20 nm to 100 nm, and channel length can change between 100 nm and 1 μm. Gate insulator and passivation layer were chosen to be silicon nitride, as the available amorphous silicon nitride quality was much better than amorphous silicon oxide. The thickness of gate insulator varies from 20 nm to 250 nm, depending on the channel length and scaling rules. Cr layers are used for metallization and deposited 100 nm for each electrode. Drain and source n^+ regions, which can be amorphous or microcrystalline for various on contact resistances, have 300 nm thickness. For final passivation material, we use 250nm amorphous silicon-nitride, and for contact metals Al has been used.

3.2.2.2 VTFT Fabrication Process

The fabrication process for the designed structure in [54] is the CMOS compatible process which means that no specific machine is required for VTFT fabrication. This is a five mask process based on conventional TFT process [69]. First three masks are for gate source and drain patterning, mask four is for contact via opening and mask five is for contact metallization patterning. Figure 3.8 shows different mask process sequences and proportional deposition for each step. Following is the fabrication details for each step.

Mask 1 Source Patterning

At the beginning 100 nm Cr is sputtered as a source electrode on the three inches Corning 1737 glass substrate. The glass substrate was cleaned before Cr deposition by standard RCA1 and RCA2 cleanings [70]. Then 300 nm n^+ μc-Si:H or a-Si:H is deposited by PECVD to make source Ohmic contact. In the next step photo resist (PR) is applied and patterned by the first mask to act as a mask for etching. The n^+ film outside the mask is removed by CF_4 plasma, and the underneath Cr can be etched by wet etching ($Ce(NH_4)_2(NO_3)_6$:1 + CH_3COOH:1 + H_2O:5). At the end, PR is stripped by plasma ashing followed by applying PR stripper.

Mask 2 Drain Patterning

In this step, in the one chamber pump down a-SiN_x:H film and n^+ μc-Si:H or a-Si:H are deposited over the wafer using PECVD. The a-SiN_x:H defines the channel wall and its length, which varies from 100 nm to 1 μm, and 300 nm n^+ region is for forming drain electrode Ohmic contact to 100 nm Cr film on top. This layer is deposited using sputtering Cr source. Again PR is applied and patterned with mask two. Top Cr layer is etched by the same wet etchant as previous step. Now is the time for dry etching the n^+ / nitride / n^+ layers to define the channel. This step is very critical, because the etching has to be completely anisotropic to get prefect trench. Any inclined configuration in this step brings difficulties in future film depositions. We use CF_4 / H_2 plasma to do reactive ion etching (RIE). As this gas doesn't react with Cr, we can use drain Cr layer as a mask and source Cr layer as etch stop layer. After etch, thin layer of a polymer is resided on the vertical wall

that can prevent good contact from channel to drain and source. So, we use EKC265^{TM} post-etch residue remover followed by a dip in buffered Hydrofluoric acid (BHF) (HF:1 + NH_4F:80 + H_2O:120) solution removing polymer and native oxide on the n^+ sections of the wall, respectively. Theses guarantee good electrical conduction between channel and n^+ layers.

Mask 3 Gate Patterning

After wall refinement, sample is immediately loaded into PECVD chamber to deposit 50 nm intrinsic a-Si:H, and 250 nm a-SiN_x:H for vertical channel and gate dielectric, respectively. Subsequently, 100 nm Cr layer again is sputtered to form gate electrode. Mask three is used to pattern PR coated substrate. Etchings starts with Cr wet etching and then a-SiN_x:H and i a-Si:H films are removes by CF_4 plasma etching.

Mask 4 Via Openings

After mask three the device structure is almost completed. Therefore, a 250 nm a-SiN_x:H film is deposited by PECVD for passivation layer and protecting active layers against test ambient. This layer is also used in next step as etch-stop layer for contact Aluminum etching. Mask four lithography step is to define vias for contacts to reach different VTFT electrode's metallization. CF_4 plasma is used at room temperature to etch the nitride and open vias.

Mask 5 Final Metallization

Eventually, 1 μm Aluminum is deposited using DC sputtering for final metallization. Mask five patterns wiring and the additional Aluminums are removed by PAN solution (H_2PO_3:25 + CH_3COOH:2 + HNO_3:1 + H_2O:5) at 45 ^oC. The last step before testing the device is the annealing, which is performed for three hours in 175 ^oC. If it is required to package the chip, wire can be bonded to Al contacts, elsewhere for direct probing the devices probes can directly measure connecting to Al contacts.

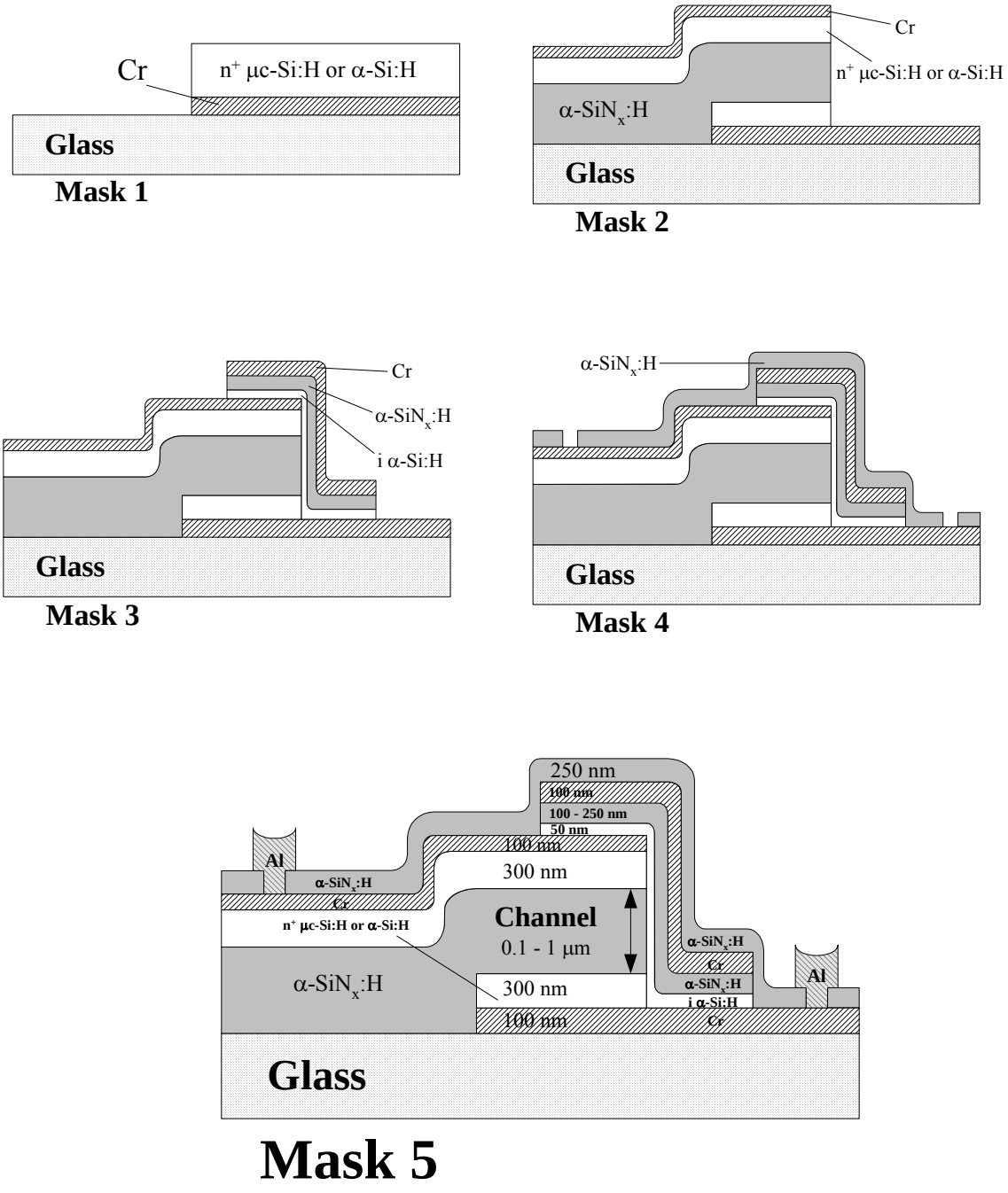


Figure 3. 8: Fabrication sequence of a-Si:H VTFT during different lithographical steps. Each material is shaded in unique color and dimensions are not to scale.

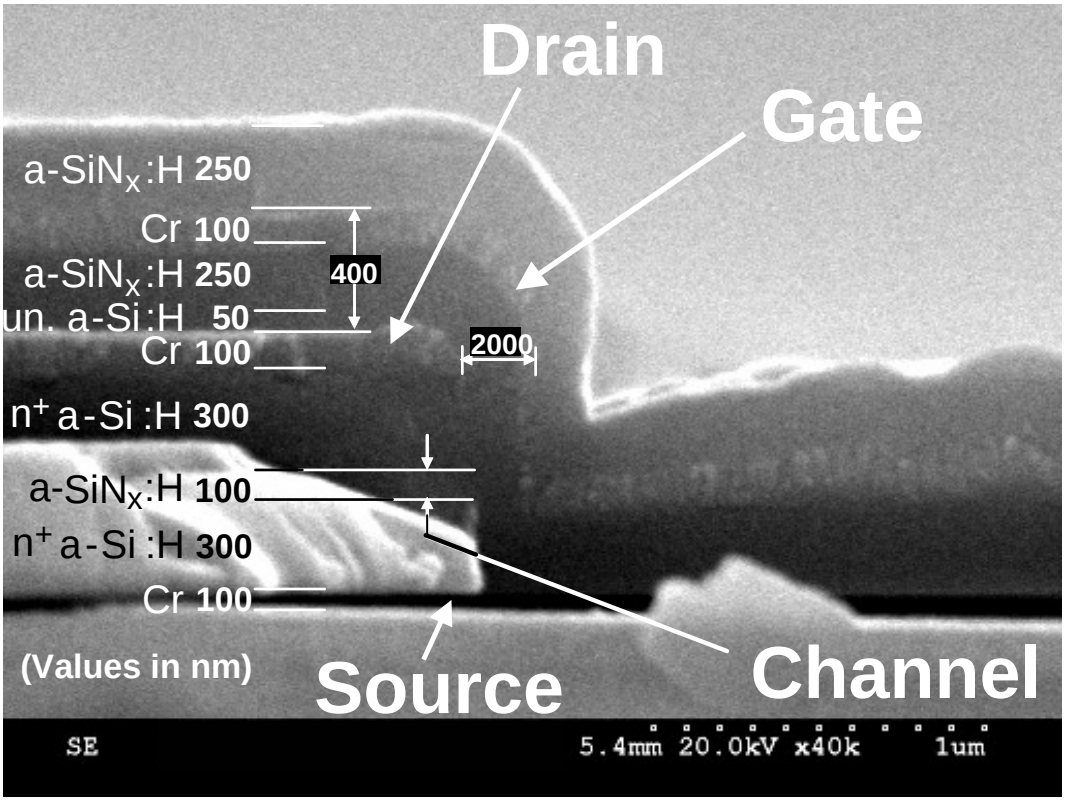


Figure 3. 9: Cross section of 100 nm channel length a-Si:H VTFT [54].

The SEM picture in Figure 3.9 displays a fabricated a-Si:H VTFT device structure with 100 nm channel length and n^+ a-Si:H Ohmic contact. In spite of the fact that the colors of a-SiN_x:H and n^+ a-Si:H are identical, the 100 nm channel and thickness of other layers can be determined from the picture, as shown. Moreover, it depicts perfect alignment of the drain and source along the 100 nm vertical channel, which owes to anisotropic dry etching performed in the second mask process step. Another important issue appeared in this graph is the perfect step coverage of the films along the vertical wall. In case of having poor step coverage, device may suffer from lack of electrical conduction between drain and source. Furthermore, the film's covered thickness in the vertical direction is almost half of which in horizontal surfaces. This means that depositing 50 nm i-layer on the substrate makes a

25 nm channel layer at the vertical surface [54], [71]. This has to be considered in the device design and analysis process.

3.2.2.3 VTFT I-V Characteristics

Various samples with different channel lengths and layer thicknesses have been fabricated. A summary of parameters of fabricated VTFTs is listed in Table 3.1. In this section we present the results for three different samples: #1- Long channel VTFT (1 μm), #2- Short channel device (100 nm) which shows saturation, and #3- Short channel sample (100 nm) without saturating characteristics. Figures 3.10 to 3.15 display various transfer and output characteristics for these samples. It is worth mentioning that among all fabricated devices, sample #3 with 100 nm channel length and 125 nm gate dielectric thickness is the only VTFT that shows no saturation in out put characteristics (Figure 3.11).

Table 3. 1: Summary of device parameters for different samples. Intrinsic a-Si:H thickness for all of the samples is 25 nm.

Sample	W (μm)	L (μm)	t_{SiN} (nm)	I_{off} (A) @ V_D=1.5 V	I_{on}/I_{off} @ V_D=1.5 V	S (V/Dec)
#1	11	0.1	125	10^{-14}	$> 10^6$	1.4
#2	100	0.1	50	$< 10^{-10}$	$> 10^5$	1.5
#3	100	1	125	$< 10^{-13}$	$> 10^6$	1.6

Generally, fabricated transistors have off-current in range of pico-ampere and ON/OFF current ratio of more than 10^6 for low drain voltages (V_D=1.5 V). Behavior of VTFT in sub-threshold region is not as good as longer channel TFTs, as the devices show sub-threshold slope around 1.5 V/Dec. Because, Figures 3.12 and 3.14 are extracted from the output characteristic data, these graphs do not carry the information for negative gate voltages. Amount of off current and ON/OFF current ratio are reported as their availability in these graphs. Moreover, we will talk about threshold voltage later.

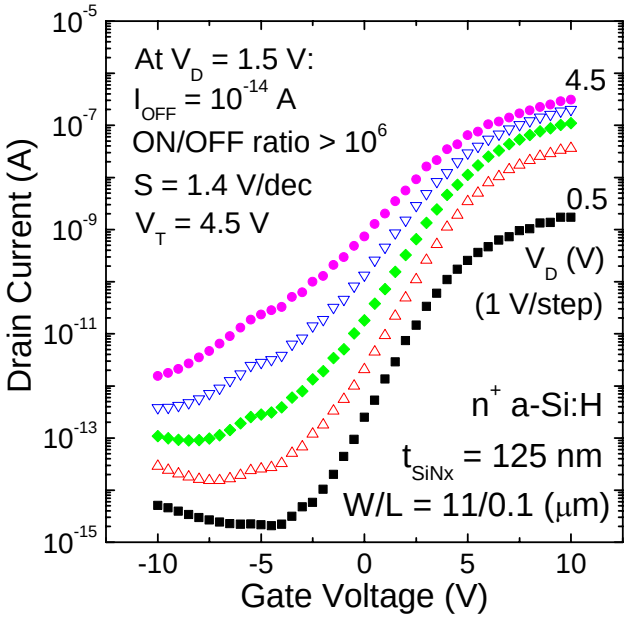


Figure 3. 10: Transfer characteristics of VTFT sample # 1.

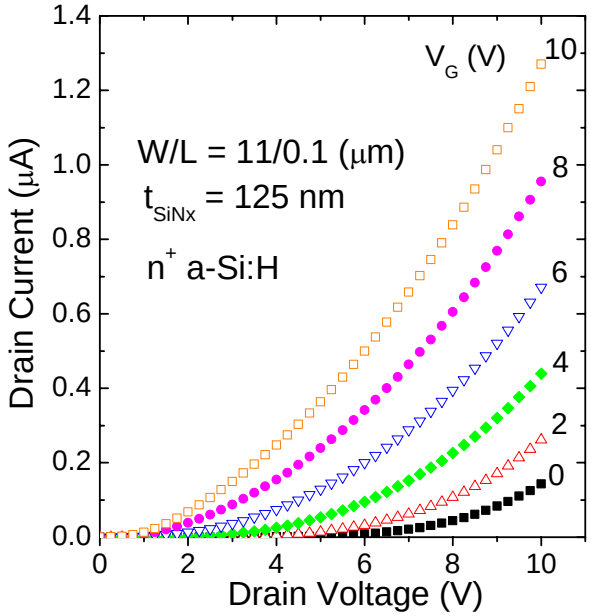


Figure 3. 11: Output characteristics of VTFT sample # 1.

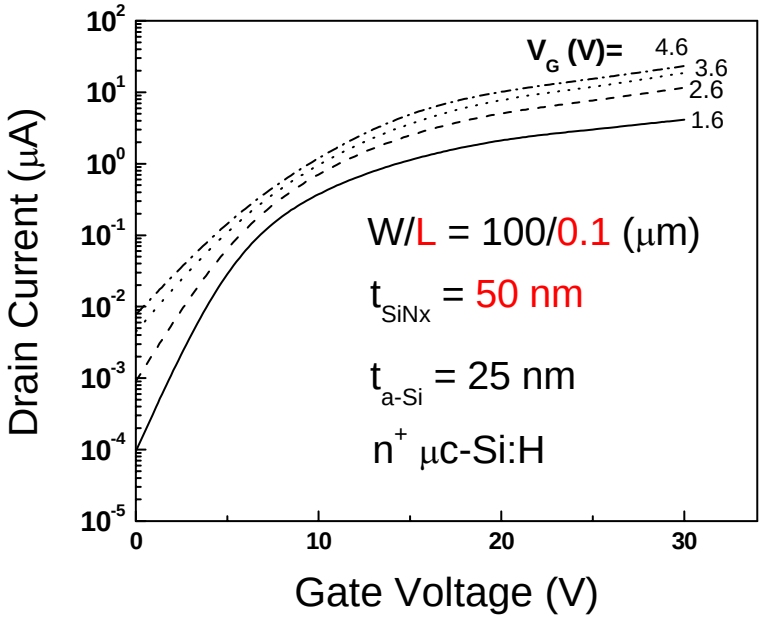


Figure 3. 12: Extracted transfer characteristics of VTFT sample # 2.

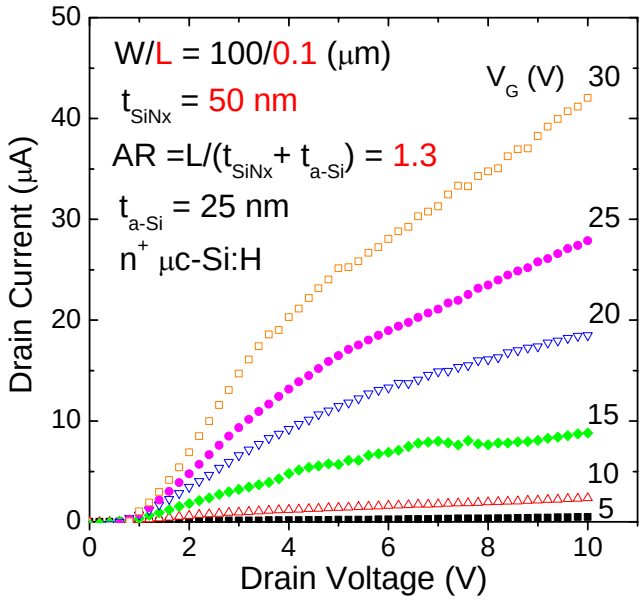


Figure 3. 13: Output characteristics of VTFT sample # 2.

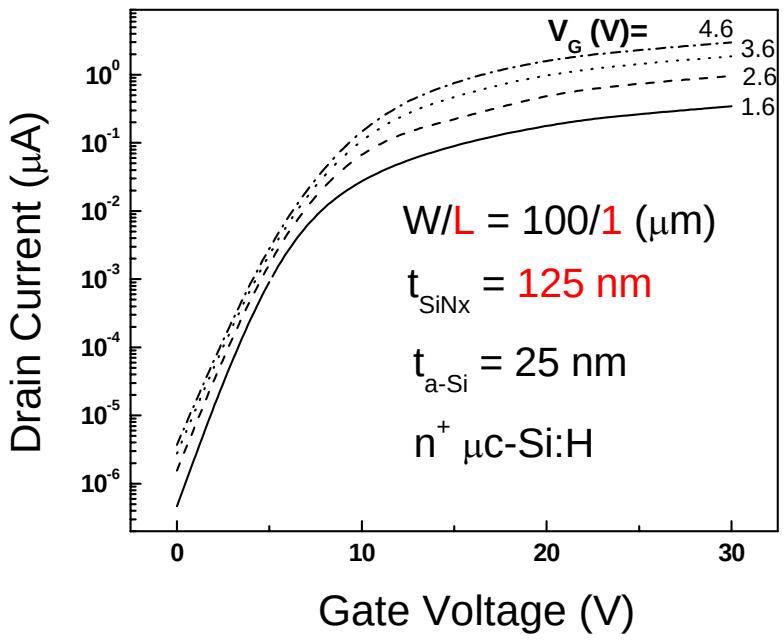


Figure 3. 14: Extracted transfer characteristics of VTFT sample # 3.

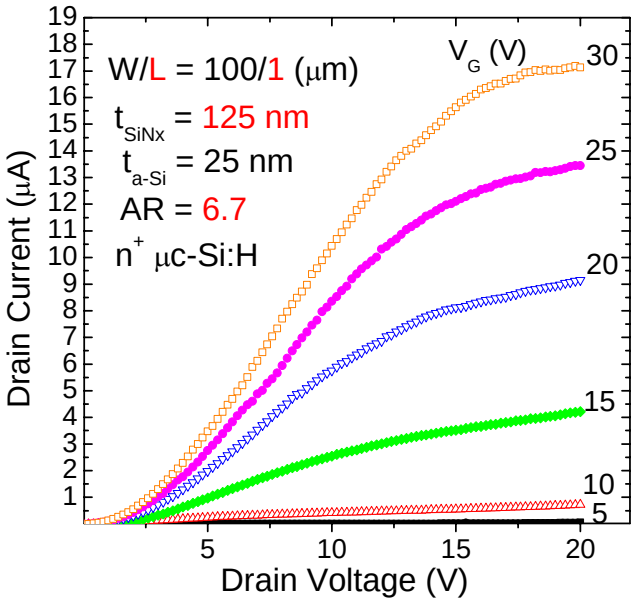


Figure 3. 15: Output characteristics of VTFT sample # 3.

3.2.2.4 VTFT C-V Characteristics

Since VTFTs are mostly applicable in the active matrix backplanes, they are operating as electronic switch. Especially, according to Equation 1.2 and considering VTFT's very short channel, the response time is limited by overlap capacitances. Generally, these capacitances are determining the RC time constant of the circuit's switching transient. To measure the capacitances associated with both gate-drain and gate-source overlaps, we shorted drain to source and measured the C-V between gate and drain-source contact for different frequencies. Figure 3.16 shows C-V characteristics for sample #1 with channel width of 100 μm. The value of capacitance at negative voltages reflects only the amount of overlap capacitances. The average of this capacitance is measured to be around 185 fF.

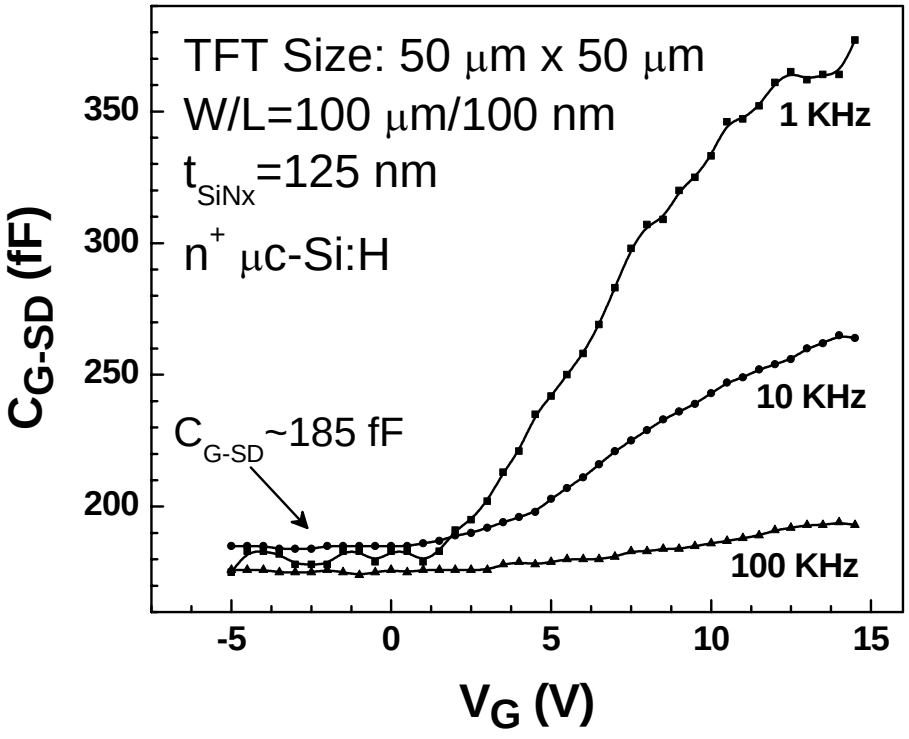


Figure 3. 16: Total a-Si:H VTFT gate input capacitance versus gate voltage for different AC voltage frequencies.

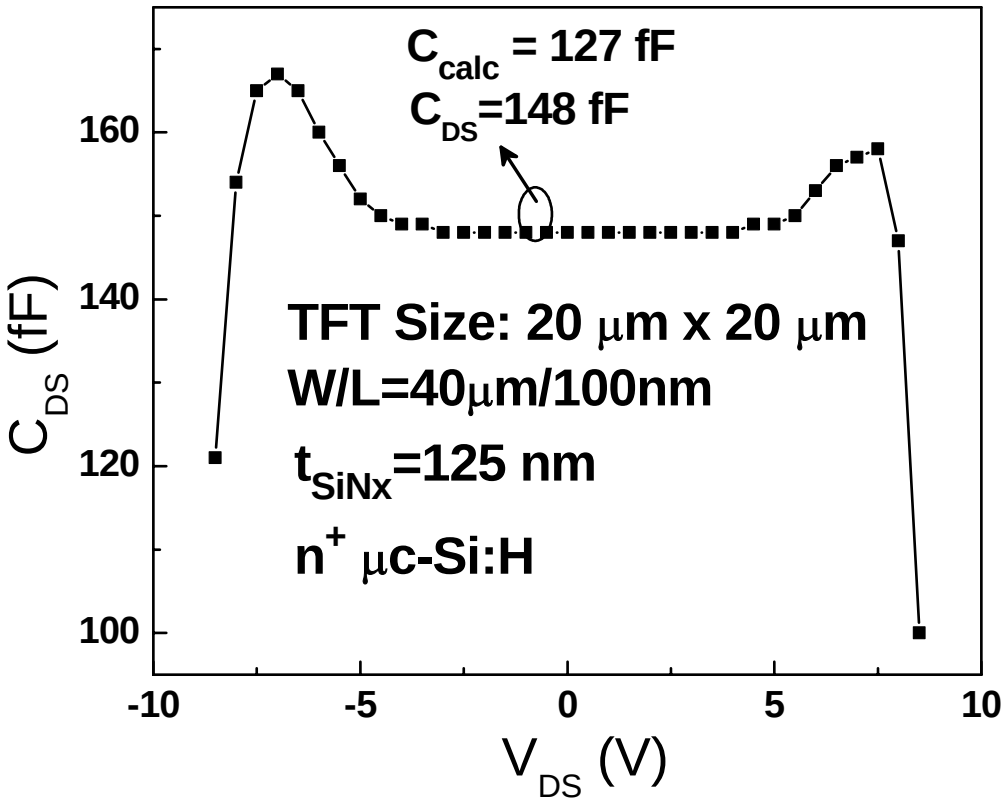


Figure 3. 17: a-Si:H VTFT drain-source capacitance versus drain voltage.

As it is clear from graph, there is no-maximum peak of the C-V graph and by reducing the measurement frequency the curve maximum value increases. This effect is mostly due to electron's long life time in the traps, which requires long time to respond to applied voltage. So very low frequency signal, as low 10 Hz, has to be used to obtain correct C-V characteristics [32]. But, applying very low frequency increases the measurement noise associated with the LCR-meter system range. We observed that the 1 KHz graph in Figure 3.16 has already views some noises. Another important capacitance in the device is drain to source capacitance. This is due to the fact that the electrical field of this capacitance may accumulate some parts of the semiconducting material at the back interface. Figure 3.17

shows the C-V test result for C_{DS}. Although, there is two n^+ μc-Si:H layers in this capacitance, the result show no voltage dependence. The only change in the capacitance is at the switching on and off the test voltage that brings transient effects in the measurement [72]. The steady state capacitance is 148 fF as the calculated capacitance based on overlaps is 127 fF (the calculation will be discussed on chapter four). Finally, it is worthy to note that all these small capacitances owe to VTFT device small dimensions, which is promising for high speed switching.

3.2.3 VTFT Inverter

The NMOS inverter schematic shown in Figure 3.18 is fabricated with two VTFTs. T1 operates as active load and T2 is the main drive transistor. Figure 3.19 shows the transfer characteristics (V_{out} versus V_{in}) for the VTFT sets with 100 nm channel length and 125 nm gate dielectric thickness. The inverter shows very low switching slope as they have very high contact resistance. This high contact resistance and effect of drain and gate leakage currents also drop the output voltage level very lower than V_{DD}, although negative input voltage can minimize leakage current and raise the output voltage to the supply voltage (V_{DD}).

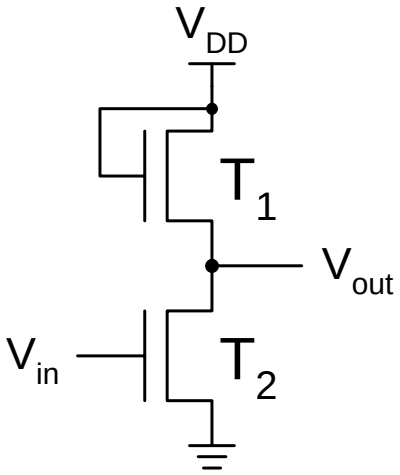


Figure 3. 18: Schematic circuit of VTFT inverter.

Figure 3.20 shows the effect of contact resistance in the switching slope and output voltage level. It compares output characteristics of two different NMOS inverters, one with n^+ μc-Si:H and another with n^+ a-Si:H Ohmic contacts. As the former shows the less contact resistance, correspondent output characteristics becomes sharper.

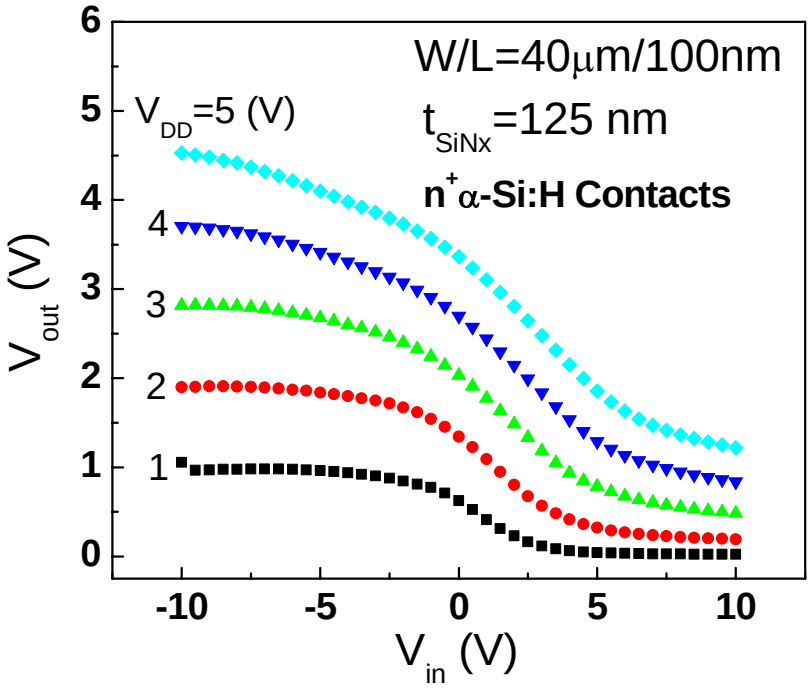


Figure 3. 19: Transfer characteristics of the VTFT NMOS inverter.

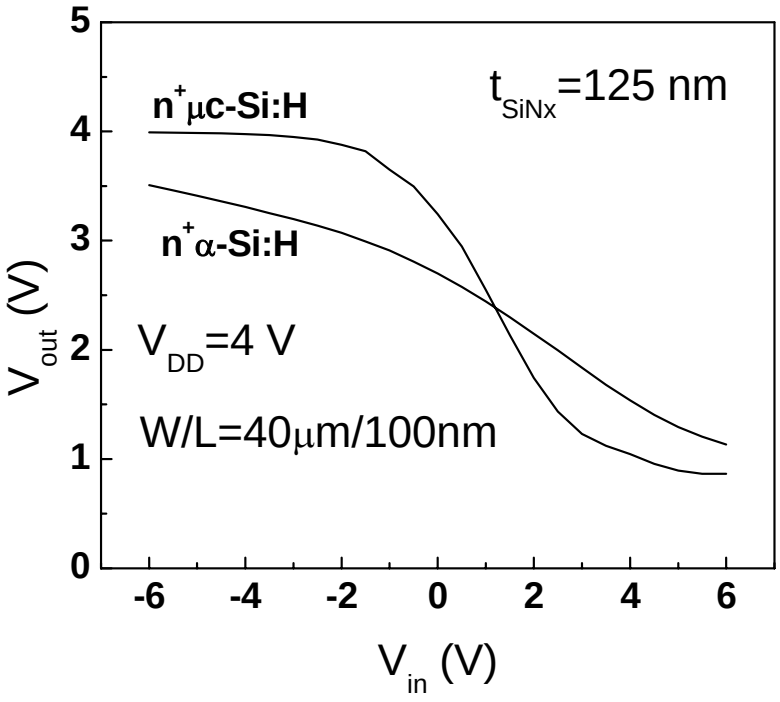


Figure 3. 20: Comparison between transfer characteristic of VTFT inverters with n^+ μc-Si:H and a-Si:H contacts.

Chapter 4: Modeling and Device Physics of The VTFTs

A physical model for characteristics of a-Si:H VTFT is crucial for design and simulation of active matrix backplane pixel circuits. The effect of short channel sizes and presence of amorphous silicon material with carrier trap sites for active region contribute to the complexity of VTFT. In practice, neither using conventional TFT models nor employing any CMOS short channel model would be capable of interpreting VTFT device characteristics. On the other hand, solving physical equation to obtain a compact model seems too complicated, and in need of oversimplifications that make it impractical. Therefore, we start from conventional TFT model and, based on short channel device physics, introduce new parameters that affect the device behavior. Numerical simulations, which solve exact physical equations, also provide device characteristics for available device parameters. This can help to understand the effect of varying different parameters on the device output and transfer characteristics. This chapter presents a study on above threshold behavior of VTFT followed by the equivalent circuit model for described VTFT. Moreover, device capacitance characteristics presented in Chapter 3 are discussed. Finally, VTFT breakdown is studied.

4.1 Long Channel TFT Models

Shur *et al.* [73], [74], Leroux [75], Khakzar *et al.* [76], Servati *et al.* [77] and other authors have reported several analytical model for different operational regions of a-Si:H TFTs. The basic physics of all of these models are similar. Shur *et al*'s model [73], [74] is used in AIM-SPICE model and Leuroux model [75] is used in Silvaco-Atlas TFT module. Servati *et al.* consider electrical field at the back interface zero while other authors assume electrical potential zero at this point. As the zero E-field assumption is closer to reality, we built our transistor model on the Servati's model. This model is based on the physics of a-Si:H material and considers both free and trapped carriers as in Equation 2.11. The effect of non-idealities such as contact resistance is also included, which let us to more easily fit short-channel non-ideal properties to this model. In this section after introducing TFT model, we will compare and verify the numerically obtained TFT characteristics with the simulation run in MEDICI software.

When no gate voltage is applied, Fermi level is slightly above mid gap. This effect is mainly because of the distribution of traps and dangling bonds in the amorphous material and causes the a-Si:H to be weakly n-type [1]. In this case negligible amount of electrons participate in the conduction and hence there is almost no conduction between drain and source. By increasing gate voltage and before threshold, Fermi energy level starts moving upward and conduction band electrons start to pile up. But because of the high temperature characteristics of the deep traps and interface states, most of the electrons get trapped in these states. However, in this range of gate voltage, there is still a small population of conducting electrons in the channel, leading to small currents in the range of 10^{-12} to 10^{-8}A. This regime is called sub-threshold regime, which the small number of electrons flow along front interface (a-Si:H / a-SiN_x:H interface closer to gate). Raising gate voltage increases concentration of electrons and consequently the current rises exponentially. By further increasing the gate voltage, Fermi level reaches the conduction band tail states with lower characteristics temperature, which is the transition to above threshold region ($V_{GS} > V_T$). Fast exponential increase of band tail states lowers Fermi level shift rate in

comparison with sub-threshold region. In this regime conducting carriers reaches to an amount which can make high drain current in range of μA [43].

In the negative applied gate voltages, accumulated electrons are repelled from front interface to the back interface (a-Si:H / a-SiN_x:H interface closer to drain and source). This repulsion of carriers leads to decrease of sub-threshold current until a channel forms close to the back interface called back channel. The current associated with this conduction path is known as reverse sub-threshold current. Further decrease in negative voltage leads some carriers to be emitted in the back channel at very high negative filed. This region is called Pool-Frenkel [43].

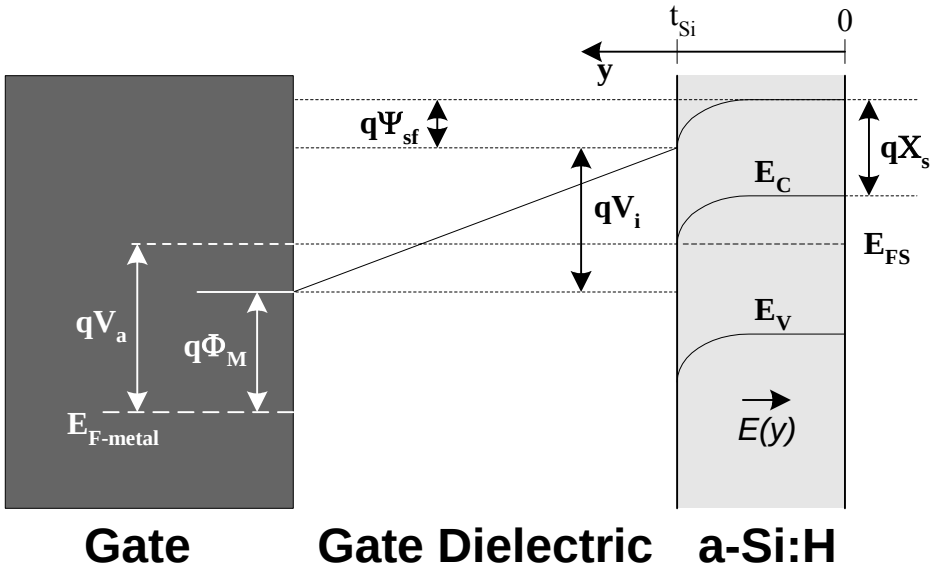


Figure 4. 1: Band diagram for arbitrary TFT cross-section with applied gate voltage (V_a).

Figure 4.1 shows the band diagram of the TFT channel in an arbitrary cross section. This shows the band bending at the front interface as a voltage is applied to gate. This voltage divides between three parts: flat band voltage, across dielectric, and across semiconductor. In the band bending equations also all charges should be considered. There are some charges trapped in the nitride, front interface, semiconductor, and in back interface. Threshold voltage equation has to take all these parts into account [43]. To obtain electrical field and potential, Poisson's equation has to be solved for the trapped and free carriers in

the Equations 2.11 and 2.14 (Figure 2.5), respectively. Equation 4.1 shows the Poison's equation for amorphous silicon based TFT.

$$\nabla^2\psi = -\frac{q(n_t + n)}{\varepsilon_{Si}} \tag{4.1-a}$$

$$\nabla^2\psi = \frac{\partial^2\psi}{\partial x^2} + \frac{\partial^2\psi}{\partial y^2} \tag{4.1-b}$$

where n_t is trapped carriers, n is free carriers, and ε is amorphous silicon permittivity. For long channel device, E_x and E_y are independent and therefore the equation can be written in two separate equations. But for the case of short channel device, Equation 4.1 must be solved simultaneously for both x and y. At the zero drain voltage even in short channel TFT one dimensional equation can be solved to obtain potential across the channel and band bending.

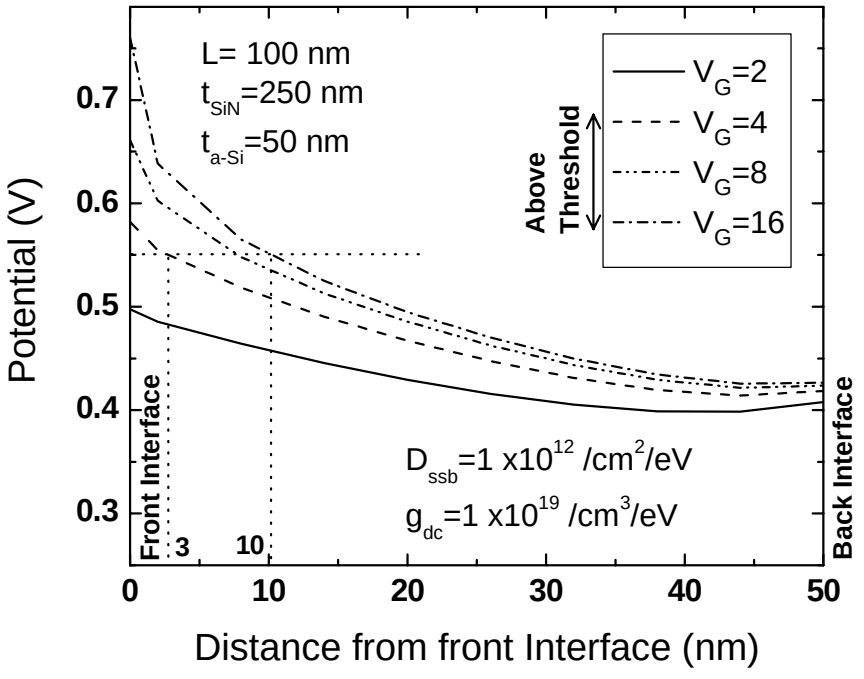


Figure 4. 2: Potential in the a-Si:H layer for regular defect density.

Figure 4.2 shows the numerically solved result for the channel potential in the short channel TFT with MEDICI. This graph is for the 250 nm gate dielectric thickness and 50 nm i-layer thickness, which is similar to long channel device settings. The interface states in the amorphous silicon and amorphous nitride (D_{ssb} and D_{ssf}) is assumed to be 1×10^{12} and 1×10^{11} $cm^{-2}eV^{-1}$ respectively. Moreover, the density of states in the Figure 2.4 is used for trapping charge density and the staggered structure has simulated. This result shows good agreement with the result reported in [43], which shows validity of our potential and E-field model used in simulation. Another interesting point in this graph is the thickness of the channel in the device. As it is shown in the figure the channel thickness is around 5 nm for gate voltages around 10 V and can increase up to 10 nm for higher gate voltages. Thus, for as thin as 25 nm i-layer channel takes maximum 40% of it.

For long channel TFTs, Equation 4.1 can be analytically solved by the assumption of gradual channel approximation, as the potential vary gradually in the channel from drain to source. Servati *et al.* model has the ability of modeling channel length modulation, contact resistance, and therefore channel enlargement that make this model to add other non-ideal effects in it [43]. This section is mostly focus on the above threshold characteristics of TFT. Equations 4.2 and 4.3 are the model for above threshold linear and saturation regions, respectively. The condition for linear region is that $V_{DS} < \alpha_{sat}(V_{GS}-V_T)$, where α_{sat} is the saturation parameter and as mobile carriers reduce to zero before the ideal pinch-off, the value of this parameter is less than 1.

$$I_{DS} = \mu_{eff}\zeta C_i^{\alpha-1}\frac{W}{L_{eff}}(V_{GS}-V_T-0.5V_{DS})^{\alpha-1}(V_{DS}-R_{DS}I_{DS}) \tag{4.2}$$

$$I_{DS} = \frac{\mu_{eff}}{\alpha}\zeta C_i^{\alpha-1}\frac{W}{L_{eff}}\gamma_{sat}(V_{GS}-0.5R_{DS}I_{DS}-V_T)^{\alpha}(1+\frac{\lambda}{L_{eff}}V_{DS}) \tag{4.3}$$

where, a is as defined in Equation 2.18, μ_{eff} is the effective mobility, ζ the unit matching parameter, L_{eff} the effective channel length, λ channel length modulation parameter, and

R_{DS} is the sum of drain and source contact resistances. γ_{sat} scales down the current to make it continuous with linear region current at the saturation point, as in Equation 4.4.

$$\gamma_{sat} = 1 - (1 - \alpha_{sat})^{\alpha} \tag{4.4}$$

We have also simulated the current characteristics of a staggered structure TFT by MEDICI simulator. Investigated device has 23 μm channel length with the two 1 μm n^+ regions. The thickness of gate dielectric, n^+ regions, and i-layer is 250 nm, 100 nm, and 50 nm respectively. The simulator separately defines the grids for each region of the structure. We have defined the 50 nm channel with meshes with 5 nm spacing to have maximum precision in this area. n^+ regions have 10^{19} cm^{-3} impurity concentration (~ 1% PH_3 gas portion), which less than 1% of that is efficient because of the trap states in the amorphous material [1], Figure 5.17. Therefore, free electron's concentration would be around 10^{16} cm^{-3} in the flat band state. Furthermore, for front interface we have defined interface states as $D_{SSf} = 1 \times 10^{11}$ $cm^{-2}eV^{-1}$ and for back interface it is defined as $D_{SSb} = 1 \times 10^{12}$ $cm^{-2}eV^{-1}$, while the fix charges in the nitride is set to $Q_F = 3 \times 10^{10}$ cm^{-2}. The band gap of 1.7 eV and trap states as Equations 2.6 and 2.7 are also defined for the software for semiconducting regions. As it is set, simulator uses Shockley-Read-Hall recombination model with fixed lifetime and Boltzmann carrier statistics. Basically, it starts from boundary conditions and find the potential in the neighboring meshes for couple of times by Newton method to minimize the error. Moreover, we have inactivated the tunneling and impact ionization to observe their effect separately. The parameters up to here suffice for the simulator to solve the potential and E-field in the device, as it is in the Figure 4.2, [78].

To model transistor's current, it is required to define the mobility model for simulator. We have found Aurora mobility model the closest to our application, although it is not the exact match for the mobility model explained in the section 2.3 [78]. This model takes temperature and doping density into account. However, the effect of Fermi level shift is indirectly included as the amount of free electrons increase by shifting Fermi level up. Also for modeling the contact resistance we have used lumped resistance in the drain and

source contacts, following the model in ref [77]. It is worthy to note that due to the fact that we have deactivated the tunneling especially in the nitride, we did not introduce any gate leakage current. Running the simulation for TFT output characteristics, we have swept drain voltage while the gate voltage is set in different steps. For transfer characteristics the process is visa versa. Appendix 1 shows the code written for 23 μm TFT Medici simulation.

Figure 4.3 shows the simulation result, for the channel width of 100 μm. By comparing this graph with the one in Figure 3.4, we find out that the Medici simulation has good agreement with both experiment and the model. The fact is that, by giving steps of 5 V in gate, the simulation couldn't converge, so we have run it for 2 V gate voltage steps and picked closest gate voltage to what in Figure 3.4 is.

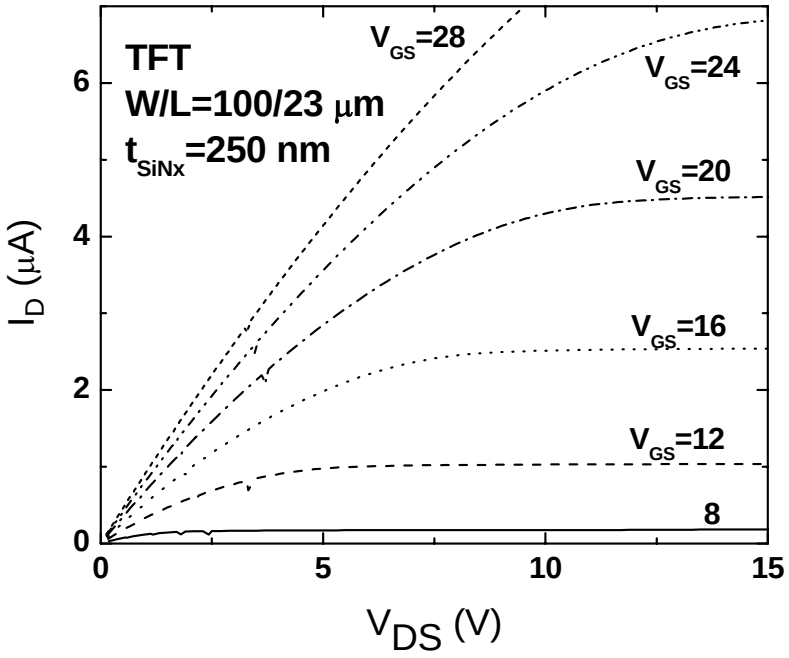
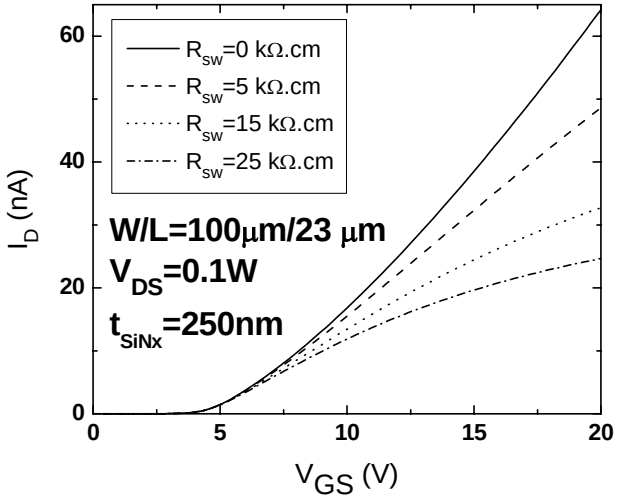
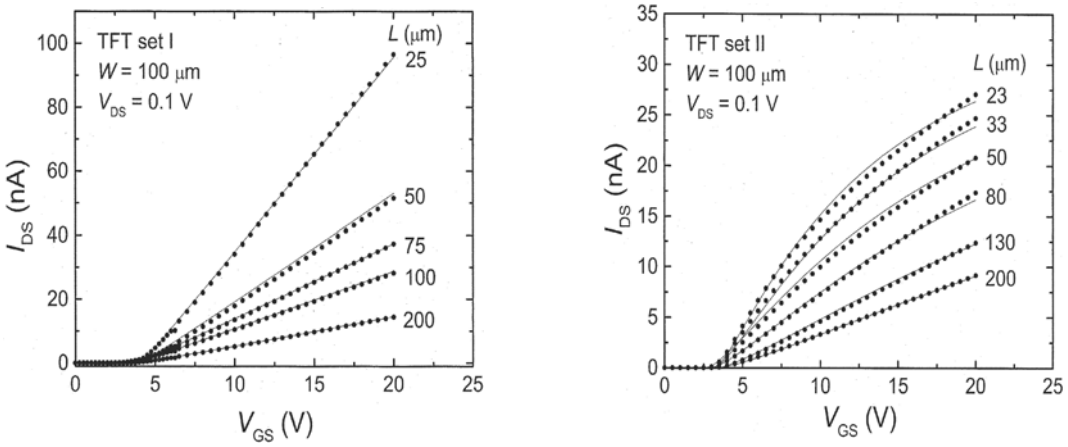


Figure 4. 3: MEDICI result for the TFT output characteristics.



a)



b) **c)**

Figure 4. 4: Effect of contact resistances on transfer characteristics, a) MEDICI simulation, L=23 μm b) the model in [77], R_{DS}W=0.229 kΩ.cm c) the model in [77], R_{DS}W=25 kΩ.cm.

Figure 4.4a is the simulation result for transfer characteristics at very low drain voltage. This curve is used for measuring the contact resistance and threshold voltage in conventional CMOS and TFT. The simulation is run for different contact resistances. It is obvious that as the contact resistance increases relative to channel resistance, the current

drops. Moreover, as the gate voltage increases channel resistance decreases and resistance of the contact becomes more dominant. Therefore, the current curve bends. Figures 2.4b and c show the experiment and model result for the same case, but for different channel lengths. The curve for L=25 μm and $R_{DS}W$=0.229 kΩ.cm is close to Figure 4.4a solid curve. As the curve for L=23 μm and $R_{DS}W$=25 kΩ.cm matches with the Figure 4.4a last curve. These results also verify the validity of Medici simulation.

4.2 Short Channel TFT Considerations

By decreasing the channel length, especially lower than 1 μm, the electrical field in the device is increased enormously. The high electrical field brings many second order effects into device and makes its characteristics different from standard transistor behavior. The solution for this problem is to scale other device dimensions (rather than channel length) to keep the shape of electrical field similar to what it is in conventional devices [80]. But this may become very difficult in the TFT technology in sort of thinning the layer thicknesses. For example for constant E-field scaling in TFTs, assume we have characteristics for the device with 23 μm channel length. If we want to shrink it down to 1 μm, then the i-layer thickness has to become 2 nm, while the case for 100 nm channel length is even worst (2 Å!). But, as we discussed in Figure 4.2 the channel thickness is around 5 nm, and thin layer makes interface effects dominant. So the i-layer can not be thinner than 15 nm and do not tolerate this type of scaling. The same argument is also valid for gate dielectric. Thus, in short channel TFT considering MOS scaling rules are not feasible.

The mobility model for the a-Si:H TFT discussed in 2-3, is still valid in short channel device, because the carriers in the band do not reach the thermal velocity and don't saturate. High density of carrier traps and dangling bonds lead to very low electron's mean free path in amorphous materials. Just for estimation of electron's maximum velocity we can start their mean free path as around 10nm. Assuming voltage of 20 volts across 100nm channel, electron's maximum velocity is calculated to be 8.3×10^5 cm/sec, which is more

than one order of magnitude lower than electron's thermal velocity. Thus, for short channel TFT the mobility model same as longer channel TFT's can be applied.

The effect of drain induced barrier lowering (DIBL) is also present in short channel a-Si:H TFTs. This arises from sharing of accumulated charges under gate control with the drain and source regions. Therefore, the voltage on drain and source can accumulate charges in some parts of channel, and reduce the gate control on channel formation. So, we expect to have lower threshold voltage by increasing drain voltage or shortening channel length [79]. Moreover, sub-threshold slope and above threshold saturation point is affected by DIBL.

In the short channel staggered structures another important effect is the dominance of the SCLC, discussed in the 2-4. This super linear current determines the shape of output characteristics at high drain voltages in short channel TFTs. In CMOS counterpart this effect translated to punch-through current when at high drain voltages depletion region expands until touching source. Actually, both of these currents are from the same physics: carrier transport in the charge depleted region (n^+-i-n^+ layers) [80]. It is worthy to mention that for poly-silicon short channel TFTs the Kink effect is observed as the impact ionization occurs in the high drain voltages. The increasing shape of this current is steeper than SCLC [81]. In a-Si:H TFT's Kink effect doesn't exist since the device thermally breaks down due to high SCLC.

Another short channel effect in a-Si:H TFTs is that the channel resistance decreases and contact resistances exceed it. Therefore, channel enlarges in the i-layer to decrease the contact resistance by having maximum flow area. This effect causes reduction of current level and presence of current crowding like shape in output characteristics. while, the channel length modulation still exists in TFT.

4.3 Vertical TFT Modeling

4.3.1 Above Threshold Region

Figure 4.5 shows the simplified structure for VTFT which looks like the structure of the staggered TFTs but rotated 90 degree. Assuming very thin channel in comparison with i-layer thickness, electrons can flow from source to drain using three major paths as shown in this figure. The first and the most important mechanism to conduct current is the channel current. Electrons can easily travel the short distance between the source contact and the channel by space charge limited (SCL) transport mechanism as they do the same for traveling between channel and drain contact. Because of very thin i-layer the resistance of this part is negligible in comparison with channel resistance. In the accumulated channel electrons are drifted toward drain in the electrical field effect of the drain. This mechanism has been modeled comprehensively for long channel inverted-staggered TFT, as discussed in section 4-1. However, some authors have also investigated short channel size effects (down to 1μm). Model extracted by Servati *et al.* [77] is used with some changes for short channel behavior to model VTFT channel current in this section.

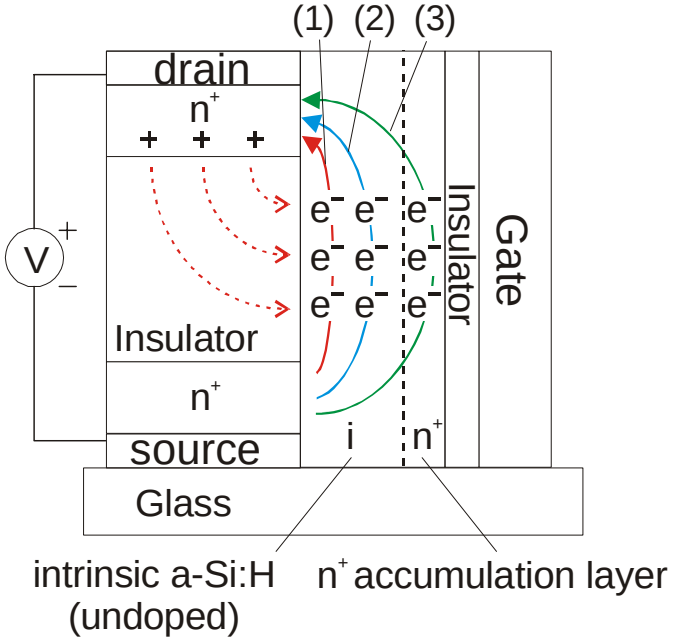


Figure 4. 5: Schematic of VTFT and various current paths from drain to source.

Second current in our model, shown in Figure 4.5, is the a-Si:H bulk current, which is mainly controlled by drain voltage rather than gate voltage. This current, parallel to channel current, passes trough amorphous material by SCL mechanism and increases severely as the channel length shrinks down. Therefore, for VTFT, SCL current (SCLC) is comparable with channel controlled counterpart. The third and least important current in above threshold regime is called back interface current, which is due to interface states between a-Si:H and a-SiN_x:H boundary locating between drain and source. An off-current characteristic of the TFT is strongly affected by back interface current but, in above threshold this term is almost negligible. For above threshold study, first two parts will be separately discussed.

Total above threshold drain current, based on above model, can be written as below,

$$I_{DS} = I_{ch} + I_{bulk} + I_{back} \tag{4.5}$$

4.3.1.1 Channel Current

Drain Induced Barrier Lowering

To get channel current, as we have discussed above, mobility model remains unchanged, but effect of drain voltage on the short channel has to be added. In the conventional c-Si short channel MOS structures DIBL is modeled by subtracting a ΔV_t from threshold voltage, which has the linear relationship with drain voltage [80]. This relation is super-linear for poly-silicon short channel TFTs, due to lateral field affected grain barrier height lowering [79]. But in the case of amorphous silicon staggered structure transistors, the drain is located as far as a-Si:H thickness from the channel and the density of the trap states are holding some charges in the semiconductor material, the exponent of V_{ds} alters to lower values. Based on previous models of the V_t shift, we have modeled short channel threshold voltage, V_{tsc}, to fit VTFT characteristics as,

$$V_{tsc} = V_t - \Delta V_t \tag{4.6}$$

where,

$$\Delta V_t = \alpha_1 V_{DS}{}^{\alpha_2} \exp\left(-\frac{\alpha_3 L}{(t_{a-si} + 2t_{SiN})} \right) \tag{4.7}$$

where α_1, α_2 and α_3 are the fitting parameters. These three parameters depend on amorphous material density of states and thickness of a-Si:H and a-Si:N_x:H layers. For the case of non-staggered structures, because the drain and source are attached to channel, α_2 will be bigger than the case of staggered structures, which is the case for VTFT. Therefore, we expect an exponent less than one for VTFTs. The exponential term in Equation 4.7 controls range of threshold voltage shift for various film thicknesses. We can see that, for very long channels or very thin nitride thicknesses effect of DIBL does not appear. Figure 3.14 shows the transfer characteristics for 1 μm channel length having no shift in threshold voltage with different drain voltages.

Jacunski *et al.* [79] has proposed an empirical model for short channel poly-silicon TFT's down to 1μm in Equation 4.8, showing temperature and channel length dependence. In this model drain voltage has quadratic dependence in threshold voltage shift. In the poly-silicon short channel TFT, higher drain voltage lowers energy barriers of grain boundaries at the channel area and helps it to be accumulated earlier.

$$\Delta V_t = \frac{A_t V_{DS}{}^2 + B_t}{L} + \Delta V_{t0}(T - 25^\circ C) \tag{4.8}$$

where, A_t, B_t, and ΔV_t are all fitting parameters and B_t is always zero in fittings (!). In room temperature (T = 25 ^oC) and for longer than 1 μm channels ($L >> t_{a\text{-}Si} + 3t_{SiNx}$) these two models are matched with following relation,

$$A_t = \frac{\alpha 1}{\alpha 3}(t_{a-Si} + 2t_{SiN}) \tag{4.9}$$

Another important parameter which affects α_2 indirectly is the contact resistance. As the contact resistance increases the channel length enlarges to let the current face bigger area.

Channel enlargement leads the channel to have more overlap with drain and getting more impact from it. Consequently, increasing the contact resistance (especially from the drain side) causes more DIBL effect which means more α_2. Figure 3.10 presents the results for transfer characteristics of a VTFT with n^+ α-Si:H drain-source contact, while Figure 4.6 depicts the graph for VTFT with n^+ μc-Si contact. It is obvious that for the transistor with higher contact resistance, Figure 3.10, threshold voltage is affected more than the second one. Briefly, as the channel shrinks, specially without proper scaling in a-Si:H and a-SiN_x:H, ΔV_t grows until starts being comparable with original threshold voltage. It is good to note that, this shift (decrease) in TFT threshold voltage is totally and originally different from the threshold voltage shift (increase) in a-Si:H TFT under long term stress. The model in this paper is only for short term above threshold characteristics, and the shift discussed above is reversible, which is totally different from the stress shift.

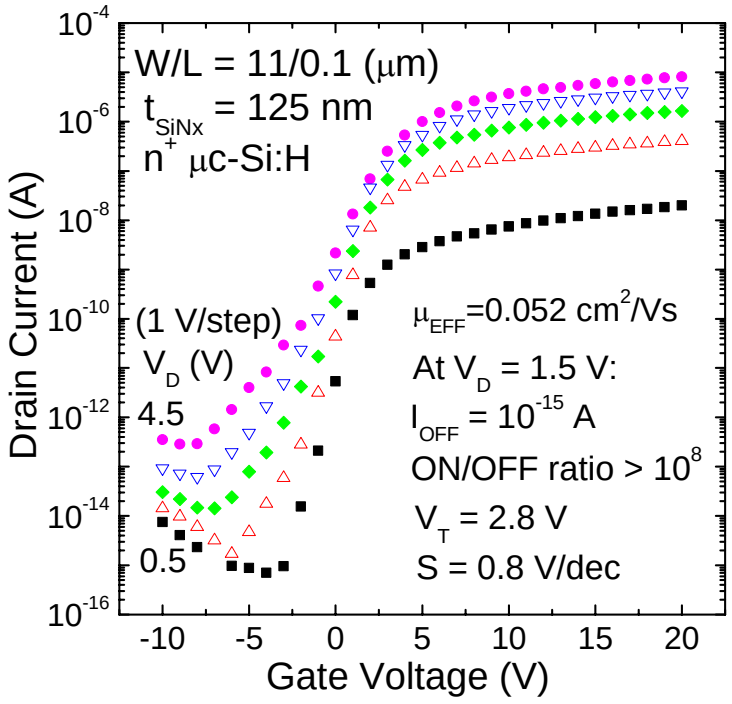


Figure 4. 6: Transfer characteristics for 100 nm channel length VTFT (n^+ μc-Si:H).

Gate Leakage

Although obeying the constant E-field scaling rules is not feasible in the thin film, we have tried to make the thicknesses as thin as possible. For example the gate dielectric thickness has been thinned down to 50 nm. This thin dielectric layer increases amount of gate leakage due to carrier tunneling, which is ideally zero. Therefore, gate has an effective current and resistance that make a voltage drop across it. Voltage divider lowers actual potential on the front interface, thus higher voltage has to be applied to gate terminal to obtain the result without gate leakage. Figure 4.7 shows the gate leakage versus gate current for the 125 nm gate dielectric thickness. At low gate voltages there are an exponential dependence, while this dependence becomes power dependant in higher gate voltages. This fact is because at low gate voltages dielectric leakage mechanism is dominant [82], while by increasing this voltage the diode in series with gate and source takes the control of current. The resistance measured with this curve is actually in series with the gate and the diode series resistances.

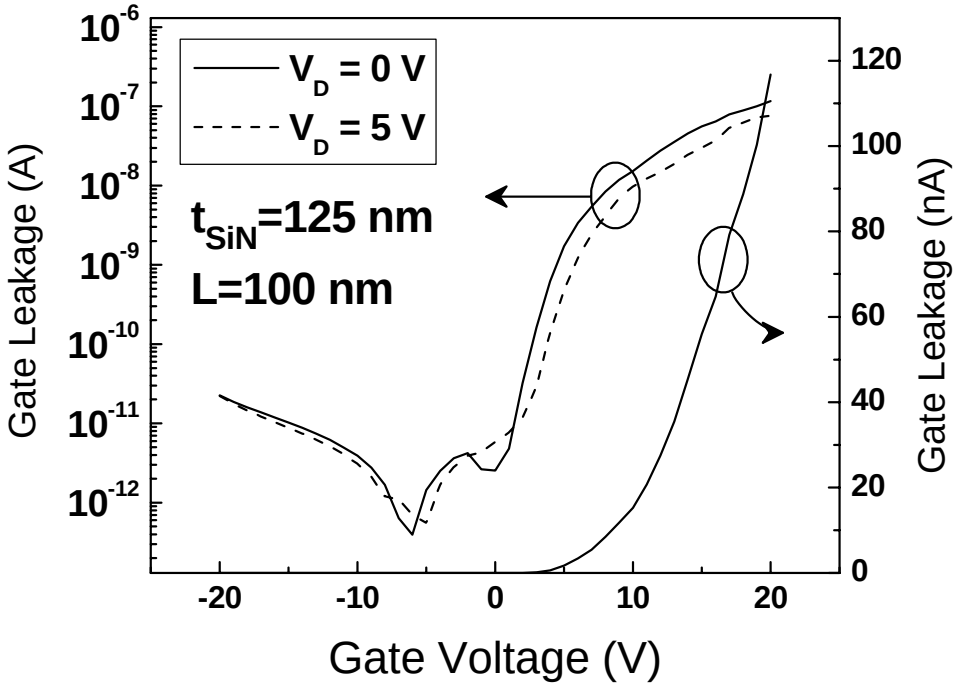


Figure 4. 7: Gate leakage current for different drain biases in linear and logarithmic scales.

Figure 4.8 shows the relation between gate leakage current and drain-source current. At the zero drain voltage leakage current is six times as the drain current and source current is almost equals to the leakage current. On the other hand, at higher drain voltages, where amount of drain current increases, drain and source currents converge to each other and leakage current becomes negligible. This fact says that gate and drain currents are added to make source current as in Equation 4.10,

$$I_S = I_D + I_{leakage} \tag{4.10}$$

So when no drain voltage is applied the drain current is almost zero and leakage current builds the source current. By increasing the drain voltage drain current raises and becomes dominant, while leakage current remains constant with drain voltage, Figure 4.7. The story for gate voltage increment is also the same, while by increasing gate voltage gate leakage also increases, but the rate and amount is too small to consider.

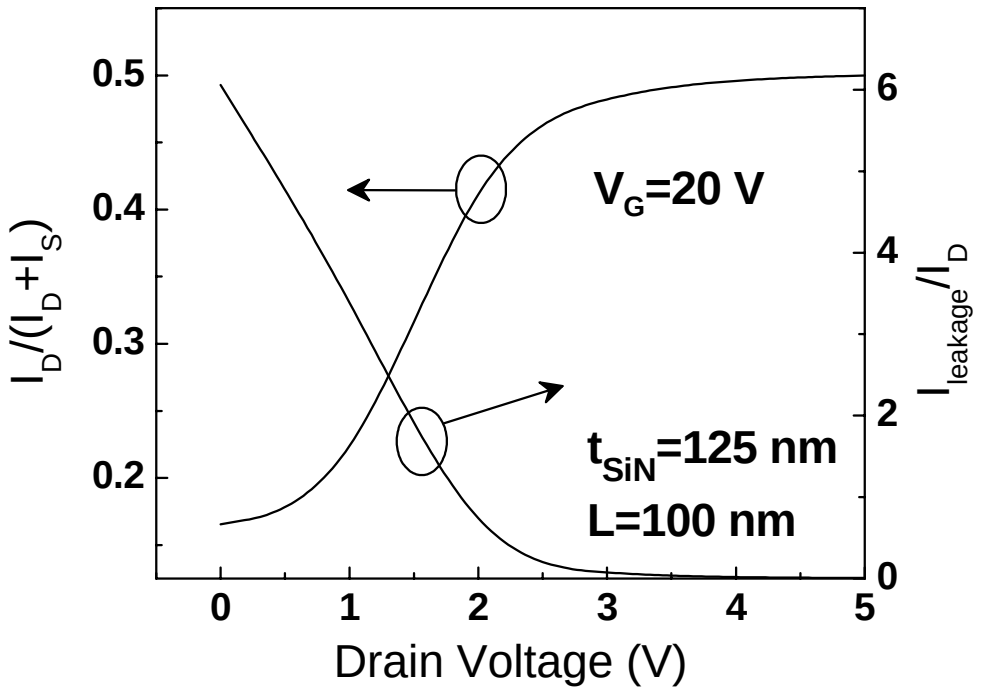


Figure 4. 8: Gate leakage comparison with drain and source currents at high gate voltage as the drain voltage increases.

We have modeled this current with a gate series resistance, which is drain voltage independent. So, for each specific gate voltage we can assume that the constant percentage of the gate terminal voltage is dropped across the real gate. But if we increase the gate voltage, based on linear curve in Figure 4.7, the gate resistance decreases. Therefore, the real voltage for each gate voltage can be modeled as,

$$V_G' = \frac{R_s(A_s V_G + B_s)}{1 + R_s(A_s V_G + B_s)} V_G = f(V_G) V_G \tag{4.11}$$

where, V_G` is the gate voltage to put in the current equation, $A_s$ and $B_s$ are gate dielectric resistance parameters, and $R_s$ is the drain-source contact resistance. It can be observed that for high gate voltages of $V_G$` approach to terminal voltage. Also, due to lower series resistance in VTFT with n^+ μc-Si:H Ohmic contact the effect of gate leakage is more critical.

4.3.1.2 Bulk Current

The second term of current shown in Figure 4.5 is the a-Si:H bulk current or SCLC. Layers of Cr, n^+ a-Si:H and i-layer at the source side of the channel make an Ohmic contact from which the electrons in the conduction band can easily diffuse through the contact to the i-layer material. Concentration of these diffused electrons decreases exponentially from the contact to the drain side. For very long channels this concentration decays very fast close to source. As the channel length shrinks amount of conduction band electrons at the drain side increase. This leads to have more electrons drifted by the drain voltage and so increase in the drift current. Using the equation introduced in Section 2.4 we know that this current has the following super linear functionality,

$$I_{SCLC} = P \mu_{eff} W t_{aSi:H} \frac{V_{DS}^{\alpha/2+1}}{L^{\alpha+1}} \tag{4.12}$$

where *P* is the model parameter for the SCLC which is the weak function of applied voltage as in [44] but can be usually assumed constant and as 9/8 [45]. Here mobility is a function of gate voltage. By increasing applied gate voltage the mobility increases,

particularly at the areas closer to gate, due to band bending. This initiates SCLC between drain and source.

As it was mentioned above, the back channel current is almost negligible in the above-threshold region, and becomes dominant in the negative gate voltage regime [83].

The output characteristics model for above threshold region is extracted and compared with the experiments. Table 4.1 shows the model parameters fitted with to the experimental data.

Table 4. 1: Extracted Parameters for sample VTFT Model (L=100 nm, n^+ μc-Si:H contact).

Physical Parameters	Amount	Unit
μ_{eff} – effective mobility	0.7	cm^2/Vs
V_T – Long Channel Threshold Voltage	2.5	V
α – Power Parameter	2	-
Dependant or Fitting Parameters		
α_{sat} – Saturation Parameter	0.2	-
γ_{sat} – Saturation Current Parameter	0.36	-
λ – Channel Length Modulation Parameter	0.08	μm/V
α_1 – Threshold Voltage Shift Parameter 1	0.1	-
α_2 – Threshold Voltage Shift Parameter 2	0.4	-
α_3 – Threshold Voltage Shift Parameter 3	0.2	-
$f(V_G)$ – Gate leakage Parameter	0.7	-
P – SCLC Parameter	8.57×10^8	Vcm/s

The model also follows any changes in the thickness of the layers. Figure 4.9 shows how the data and model follow each other. Model of gate leakage and DIBL perfectly matches with the reality. Note that in this specific VTFT thicknesses setting, for drain voltages up

to 15 V SCLC has not become comparable with channel current, while for t_{SiNx} = 125 nm it controls the most behaviors of the device, as it is in Figure 3.11.

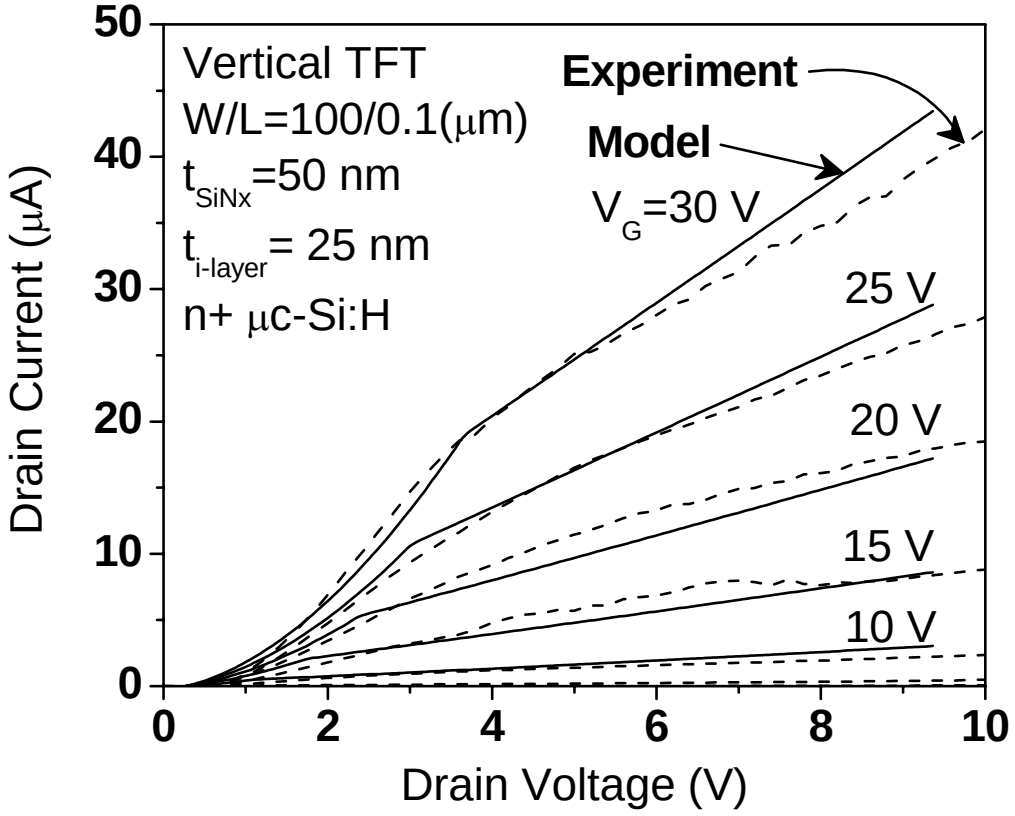


Figure 4. 9: Comparison between model simulation results (solid lines) and measurement date (dashed lines) for the output characteristics of the VTFT with L = 100 nm and t_{SiNx} = 125 nm.

4.3.2 Simulation Results

In this section we use Medici software to simulate the device characteristics and especially, the effect of short channel length. Figure 4.10 shows the 3-D plot of potential in the 100 nm VTFT with 250 nm gate dielectric and 50 nm i-layer thickness for drain voltage of 5 volts and various gate voltages changing from off to on condition.

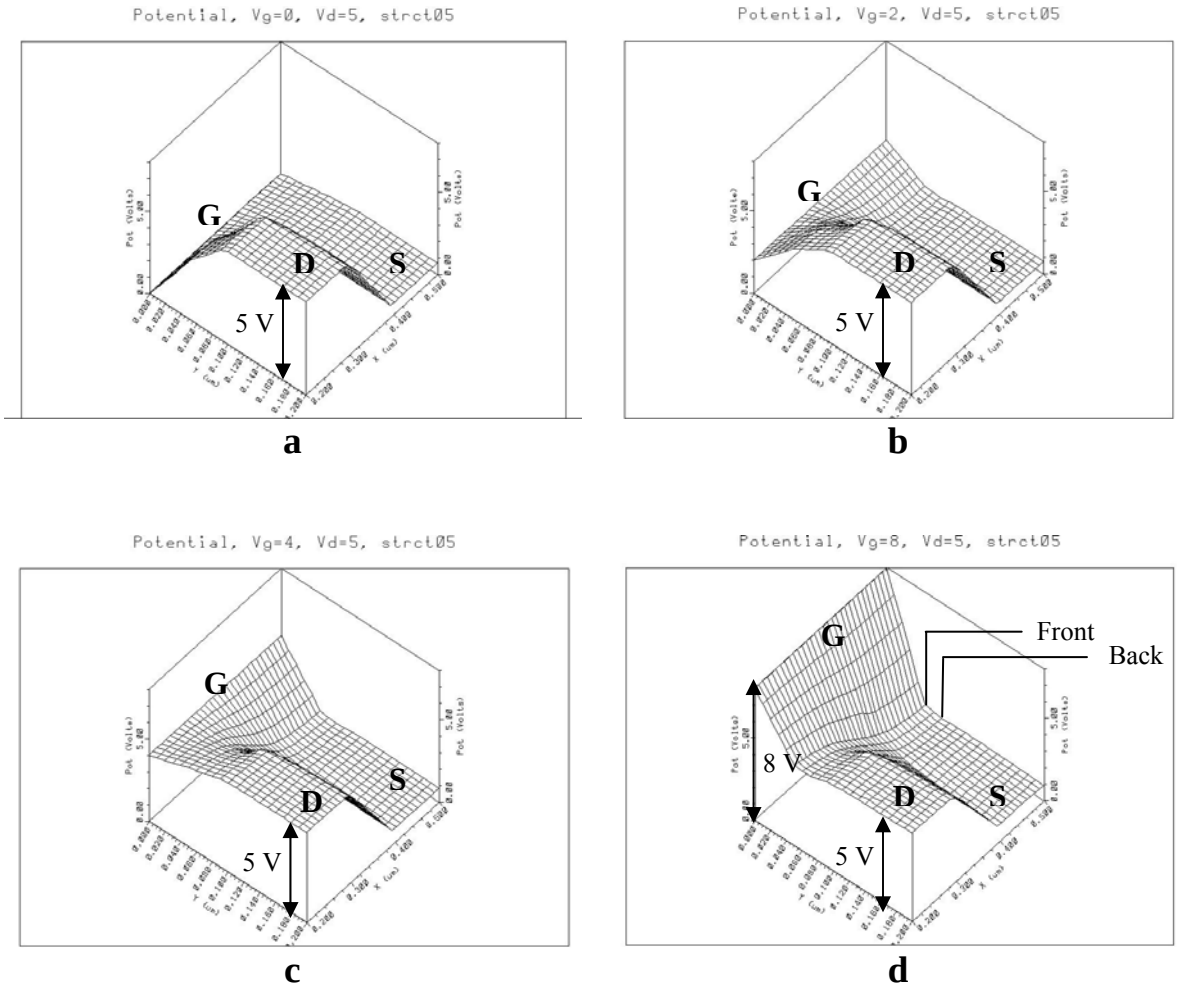


Figure 4. 10: Three dimensional plots of VTFT potential with 100 nm channel length and 250 nm gate dielectric thickness for V_D = 5 V and a) V_G = 0 V, b) V_G = 1 V, c) V_G = 4 V, and c) V_G = 8 V.

We can see that for the applied drain voltage, potential in the i-layer close to drain is raised in comparison with Figure 4.2 that have zero drain voltage. This change initiates due to DIBL effect. Figure 4.11 illustrates more comprehensive explanation of voltage changes across the i-layer. We can see that more half of the drain voltage is dropped in the middle of back interface, showing non-linear effect of drain voltage on the back interface and back gate effect.

Figure 4.12 depicts the simulation result for output characteristics of 100 nm channel length VTFT with 50 nm gate dielectric and 25 nm i-layer thickness. The simulation has run without series resistance to study only effect of channel resistance on the I-V characteristics. We see that effect of current crowding at very small drain voltages has been eliminated with zero contact resistance. This effect in higher drain voltages appears in the level of current, as the level of current in the simulation is one order of magnitude higher than experiment model. We have also observed that although for high drain voltages device lies in saturation, no saturating behavior is shown in output characteristics, because of short channel effects. Figure 4.13 confirms this idea as by enlarging the channel length, and showing more saturating behaviors in the devoice characteristics. This graph is simulated in 16 V gate voltage. Moreover, to have good zoom of current each curve is multiplied by the channel length. 1 μm channel length device saturates earlier 500 nm sample. This means that DIBL effect is minimal and also α_{sat} is very close to long channel amounts. 100 nm channel length device has no saturating performance due to high gate dielectric thickness and therefore low gate control on the channel and dominance of SCLC. Figure 4.14 shows the trend of saturation as we are thinning the gate dielectric. This is a trade-off between channel current and SCLC discussed earlier. Even with high gate voltages SCLC is dominant in comparison with channel current. It is also good to note that all of these results are for zero contact resistance, while the contact resistance also aggravates the short channel effects.

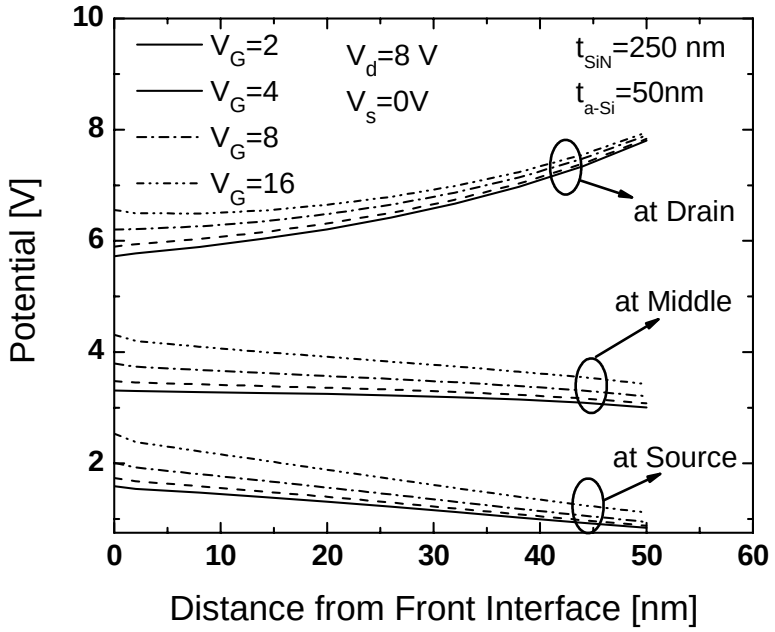


Figure 4. 11: Potential across i-layer for different gate voltages.

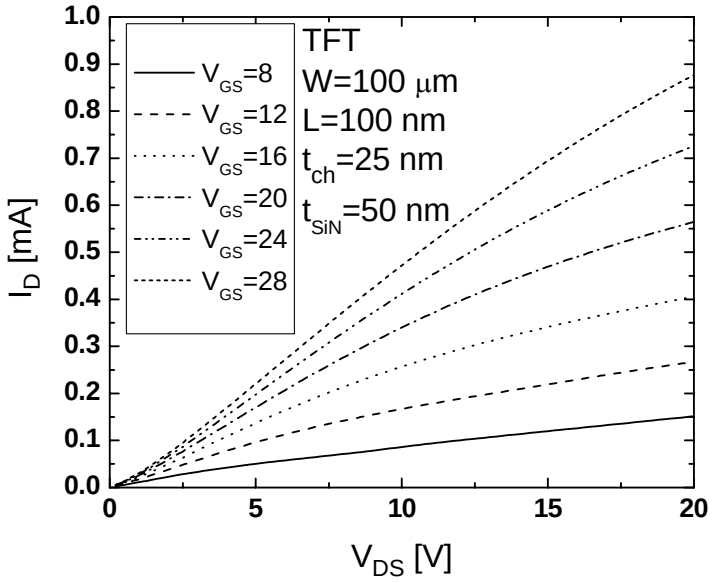


Figure 4. 12: MEDICI results for output characteristics of a simulated device structure.

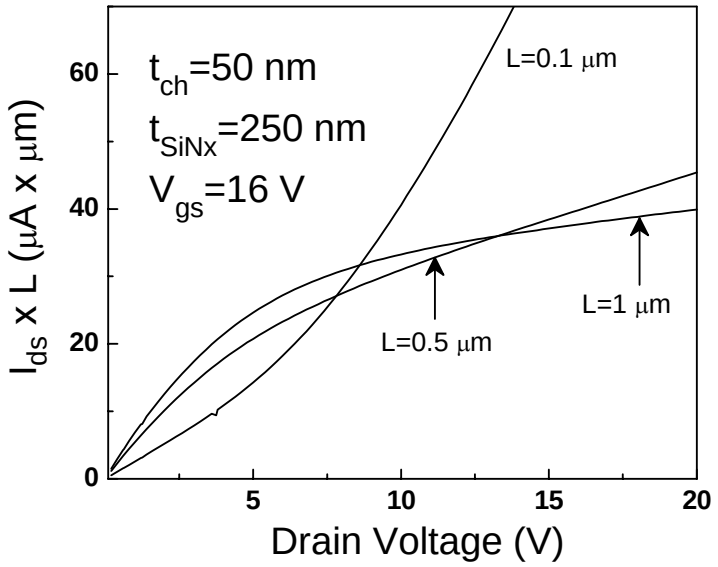


Figure 4. 13: Effect of channel length on the output characteristics of a-Si:H VTFT, (V_{GS} = 16 V).

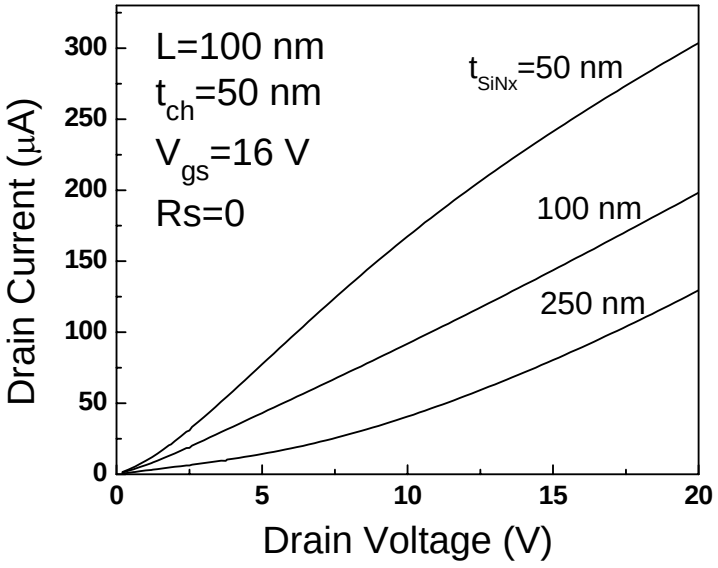


Figure 4. 14: The effect of gate dielectric thickness on the output characteristics of a-Si:H VTFT, (V_{GS} = 16 V).

4.3.3 Equivalent Circuit

To apply VTFT in any higher level design processes an equivalent circuit is required for device to describe its behavior at static and dynamic regimes. Figure 4.15 shows the VTFT structure drawn with the various circuit elements in each section. The drain current consists of three parts in the Equation 4.5, explaining various VTFT operating region characteristics. Leakage current model is also shown from gate to channel for drain and source contacts, separately. Gate resistance models the voltage drop die to leakage mechanism. Moreover, the source-drain contacts to the i-layer are implemented with two resistances at each terminal, R_{S1}, R_{S2}, R_{D1}, and R_{D2}, in parallel with two non-ideal Schottky diodes. These resistances finally models as a single series resistance in circuit model called contact resistance. The important fact is that, this bunch of resistors and diodes are the drain current path, and hence device I-V characteristics affects from them, especially when channel length scales down.

Figure 4.16 illustrates the simplified electrical operation of this equivalent circuit. A major modification to the model is the elimination of diodes, because the source side's diode is usually reverse biased and the drain counterpart has very high contact resistance that the current can be neglected, although the area of the diodes are bigger than n^+ / i-layer contact area. I_{Dl} and I_{Sl} are the leakage current model for TFT, which is discussed in section 4-3-1-1. It is good to note that in the samples investigated before, I_{Dl} is very small due to smaller contact resistance at the source side. But, this current may become dominant over I_{Sl}. For static simulations, all of the capacitances can be opened, but they play major role in dynamic characteristics, especially the capacitance in between gate and drain is very important. The voltage in one side of C_{GD} is A_V times of the other side's voltage and therefore, amount of capacitance in output is multiplied by gain (A_V) based on Miller's theorem [15]. The second important capacitance is C_{DS}, as this capacitance determines the switching time-constant. Each of R_D and R_S also represents the n^+ / i-layer contact resistance in parallel with the non-ideal Schottky diode with high series resistance, which is negligible.

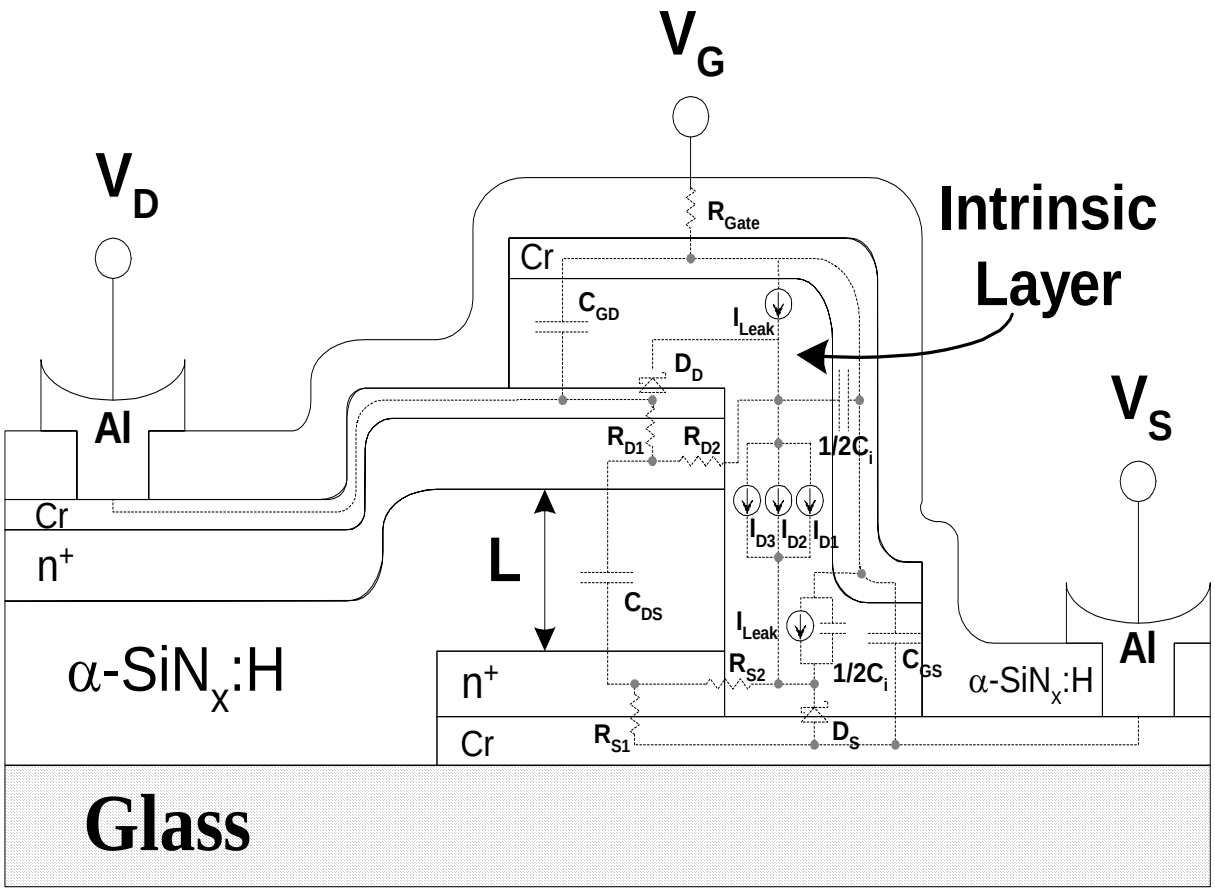


Figure 4. 15: VTFT structure with built-in circuit elements.

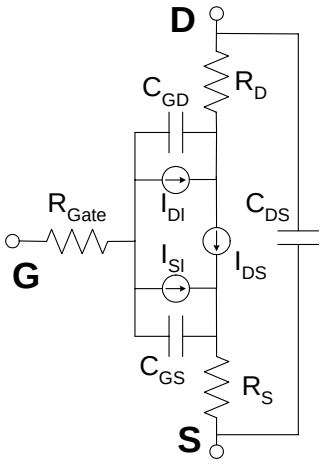


Figure 4. 16: Equivalent circuit for VTFT structure on Fig 4.15.

4.4 VTFT Capacitances

When we use transistors as a switch in the back plane of the flat panel electronics, the capacitance of the device affects the RC time constant and consequently the speed of switching. Figure 4.17 views a 3-Dimensional picture of the VTFT, showing the overlap of the different deposited layers. Intrinsic a-Si:H contributes in two C_{GD} and C_{GS} capacitances in parallel with their overlap capacitances. Due to very tiny volume of semiconductor, the overlaps capacitors are playing major role in determining final capacitance amount. Therefore, the overlap capacitances have to be minimized for increasing the speed of transistor. Fortunately, the VTFT size is very small so these overlap capacitances becomes very small. C_{DS} is another capacitance which is not important in lateral TFT, but in VTFT has the amount in the same range as other capacitances and aggravates back gate effect because of drain-source overlap.

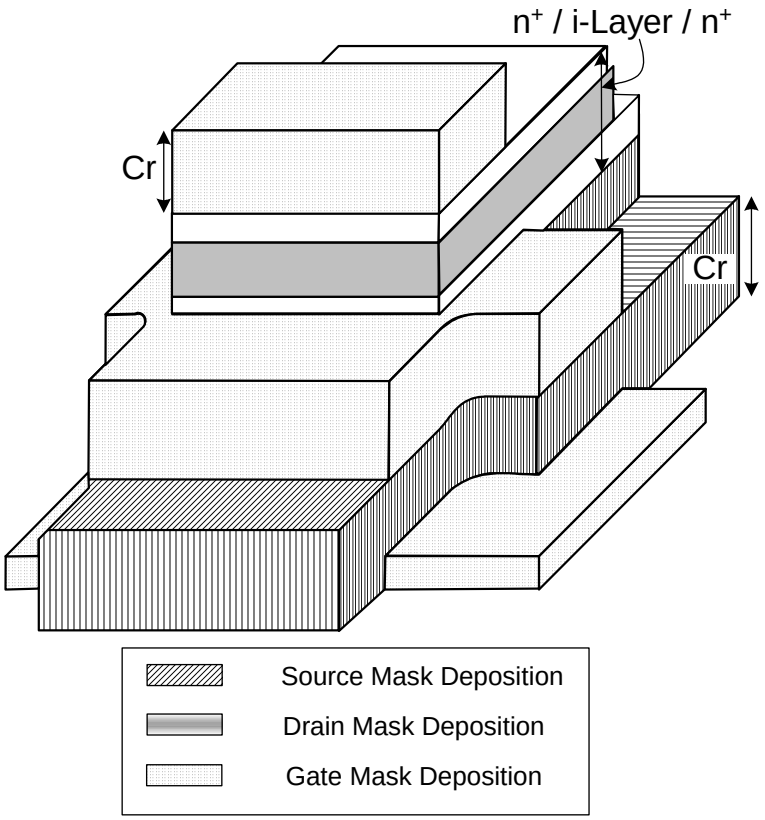
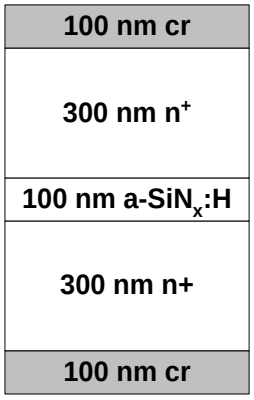
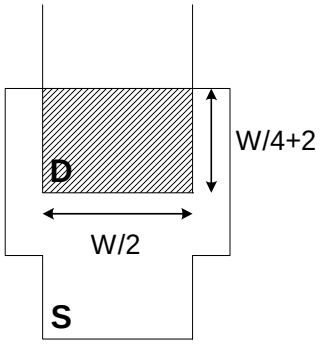


Figure 4. 17: Three dimensional schematic view of VTFT showing different thicknesses.

Drain - Source

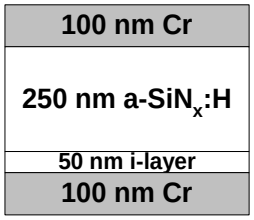
$$A = \frac{W}{2}\left(\frac{W}{4} + 2\right)$$

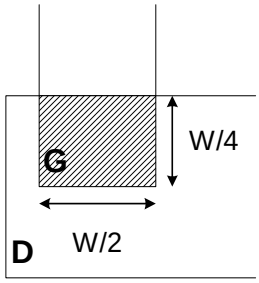




Gate - Drain

$$A = \frac{W^2}{8}$$

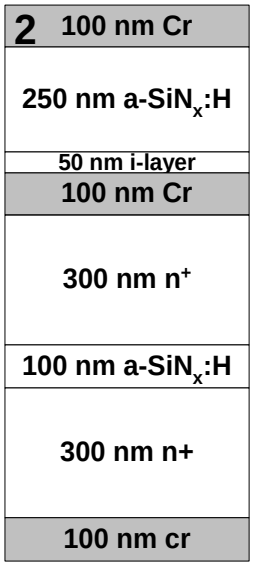


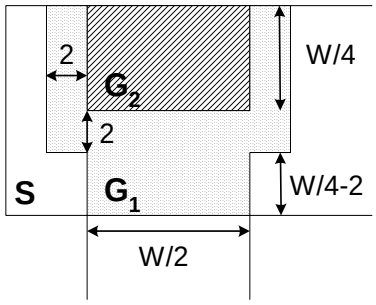


Gate - Source

$$A_1 = \frac{W^2}{8}$$

$$A_2 = \frac{W^2}{8} + W + 8$$





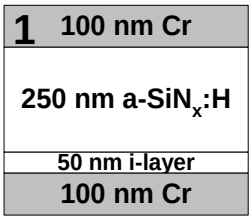


Figure 4. 18: various capacitances overlap area and the proportional thickness sandwiched between their electrodes. Amount of area for different overlaps also is calculated.

Rectangles in the Figure 4.18 actually define the channel width (W/2 + W/4 + W/4). Three vertices of all of these rectangles overlaps forming channel area. Therefore, the perimeter of them is supposed to be constant. For minimizing the capacitance we can design aspect ratio of these areas as high as possible by getting less area.

Chapter 5: Conclusions

In this thesis, the physics and modeling of the hydrogenated amorphous silicon (a-Si:H) vertical thin film transistors (VTFT) was studied. Due to the fact that investigated device includes material with trap states and at the same time consists of very short channel length, the device physics had to be reviewed completely. Therefore, a comprehensive study on amorphous material electronic structure and density of states in the band structure was carried out. Based on electronic material properties, the mobility model is defined for carriers. Defining carrier's mobility, we have completely investigated their transport mechanisms in various electric field regimes for the a-Si:H material.

Several a-Si:H VTFTs of 100 nm channel length and different parameters were fabricated and a various characterization techniques were implemented to identify structural and electrical properties. Static characteristic of the device shows ON/OFF current ratio as high as 10^8 and overlap capacitances as low as 185 fF for W=100 μm. On the other hand, short channel behavior appears in the characteristics, especially for samples with thicker gate dielectric. Moreover, lower breakdown voltage in comparison with conventional TFTs was measured. Thus, more analysis on the device was required, while no model is available for short channel a-Si:H TFTs.

Because of the difficulties of solving device equations in short channel regime, we chose the most comprehensive a-Si:H TFT model and added various short channel effects observed in the fabricated device characteristics to model above threshold characteristics of a-Si:H VTFT. Final model is in good agreement with experimental results. However, the model needed to be further verified by means of numerical simulation. We employed Medici software to develop a code, to numerically simulate the device. Various sets of device parameters were simulated to provide an understanding of the physics and effect of each parameter, and eventually, the optimum a-Si:H VTFT settings. It was found that by thinning the gate dielectric and intrinsic a-Si:H layer, gate voltage takes more control over the channel area and the channel current becomes dominant in short channel a-Si:H TFTs. This fact was also explained by comparing constant E-field scaling rules with the scaling parameters in the device under study. At the same time, both modeling and numerical simulation show that thinner intrinsic layer reduces the bulk current (SCLC).

Appendix A: Medici Code for TFT Simulation

```
COMMENT TFT Simulation
COMMENT CHANNEL THICKNESS=50nm NITRIDE THICKNESS=250nm Channel length=23 um
COMMENT Defining Structure
MESH OUT.FILE=TFT.MSH
X.MESH WIDTH=10 H1=1 SUMMARY
X.MESH WIDTH=23 H1=0.9 SUMMARY
X.MESH WIDTH=10 H1=1 SUMMARY
Y.MESH WIDTH=.24 N.SPACES=5
Y.MESH WIDTH=.06 N.SPACES=10
Y.MESH WIDTH=.1 N.SPACES=5
ELIMINATE COLUMNS Y.MAX=0.24
ELIMINATE COLUMNS Y.MIN=0.31
REGION NAME=GATE-NITRIDE NITRIDE
REGION NAME=CHANNEL Y.MIN=0.25 Y.MAX=0.3 SILICON
REGION NAME=DRAIN X.MIN=0 X.MAX=10 Y.MIN=0.3 SILICON
REGION NAME=SPACER X.MIN=10 X.MAX=33 Y.MIN=0.3 NITRIDE
REGION NAME=SOURCE X.MIN=33 X.MAX=43 Y.MIN=0.3 SILICON
ELECT NAME=GATE X.MIN=8 X.MAX=35 TOP
ELECT NAME=DRAIN X.MIN=0 X.MAX=10 BOTTOM
ELECT NAME=SOURCE X.MIN=33 X.MAX=43 BOTTOM
COMMENT Specify doping
COMMENT PROFILE UNIFORM CONC=1E16 P.TYPE
PROFILE CONC=3E17 X.MIN=0 X.MAX=10 Y.CHAR=.001 Y.MIN=.310 Y.MAX=0.4 N.TYPE
PROFILE CONC=3E17 X.MIN=33 X.MAX=43 Y.CHAR=.001 Y.MIN=0.310 Y.MAX=0.4 N.TYPE
INTERFACE REGION=(CHANNEL,GATE-NITRIDE) QF=3.1E11 P.ACCEPT=3E11 N.ACCEPT=3E11
INTERFACE REGION=(CHANNEL,SPACER) P.ACCEPT=3E12 N.ACCEPT=3E12
PLOT.2D GRID FILL
+ TITLE="TFT Transistor Structure tch=50, tsin=250 L=23um"
```

```
COMMENT Material and Simulation Settings
MODELS SRH ARORA SRFMOB
MATERIAL SILICON EG300=1.7
+ NC300=2.5E20 NC.F=1.58
+ NV300=2.5E20 NV.F=1.85
MOBILITY SILICON MUN1.ARO=10 MUN2.ARO=100 MUP1.ARO=2 MUP2.ARO=40
MOBILITY REGION=DRAIN MUN1.ARO=0.25 MUN2.ARO=2.5 MUP1.ARO=0.05 MUP2.ARO=1
MOBILITY REGION=SOURCE MUN1.ARO=0.25 MUN2.ARO=2.5 MUP1.ARO=0.05 MUP2.ARO=1

SYMB GUMM CARR=0
SOLVE V(GATE)=.1 OUT.FILE=TFT.INI
COMMENT Simulation with traps
LOAD IN.FILE=TFT.INI
ASSIGN NAME=EV N.VAL=-1.7/2
ASSIGN NAME=EC N.VAL=1.7/2
COMMENT Calculate characteristic length for hole states
ASSIGN NAME=PCHRT N.VAL=0.043 PRINT
ASSIGN NAME=PCHRD N.VAL=0.103 PRINT
COMMENT Gererate hole traps
TRAP DISTR N.TOT="-(5E19*EXP(-(@FENER-@EV)/@PCHRD)+1E22*EXP(-(@FENER-@EV)/@PCHRT))"
+ TAUN="1E-5" TAUP="1E-6"
+ MIDGAP COND="(@FENER<0)"
COMMENT Calculate characteristic length for electron states
ASSIGN NAME=NCHRT N.VAL=0.03 PRINT
ASSIGN NAME=NCHRD N.VAL=0.069 PRINT
COMMENT Generate electron traps
TRAP N.TOT="(1E19*EXP((@FENER-@EC)/@NCHRD)+5E22*EXP((@FENER-@EC)/@NCHRT))"
+ TAUN="1E-5" TAUP="1E-6"
+ MIDGAP COND="(@FENER>0)"


COMMENT Simulate with traps
SYMB GUMM CARR=0
SOLVE V(GATE)=0 V(SOURCE)=0
SYMB NEWT CARR=2
METHOD N.DAMP
SOLVE V(GATE)=0 V(SOURCE)=0

COMMENT ******************************************************************************
COMMENT ******************************************************************************

COMMENT Plot channel potential
SOLVE V(GATE)=0 V(SOURCE)=0 V(DRAIN)=0
PLOT.1D POTENTIA X.START=33 X.END=33 Y.START=0.25 Y.END=0.3
+ POINTS TOP=1 BOTTOM=-1 COLOR=2 SYMB=1
+ TITLE="Potential across the channel TFT" OUT.FILE="TFT/chanpotvg0.xls"

SOLVE V(GATE)=2 V(SOURCE)=0 V(DRAIN)=0
PLOT.1D POTENTIA X.START=33 X.END=33 Y.START=0.25 Y.END=0.3
+ POINTS COLOR=2 SYMB=2 UNCH
+  OUT.FILE="TFT/chanpotvg2.xls"

SOLVE V(GATE)=4 V(SOURCE)=0 V(DRAIN)=0
PLOT.1D POTENTIA X.START=33 X.END=33 Y.START=0.25 Y.END=0.3
+ POINTS COLOR=2 SYMB=2 UNCH
+  OUT.FILE="TFT/chanpotvg4.xls"

SOLVE V(GATE)=6 V(SOURCE)=0 V(DRAIN)=0
```

```
PLOT.1D POTENTIA X.START=33 X.END=33 Y.START=0.25 Y.END=0.3
+ POINTS COLOR=2 SYMB=4 UNCH
+  OUT.FILE="TFT/chanpotvg6.xls"

SOLVE V(GATE)=8 V(SOURCE)=0 V(DRAIN)=0
PLOT.1D POTENTIA X.START=33 X.END=33 Y.START=0.25 Y.END=0.3
+ POINTS COLOR=2 SYMB=5 UNCH
+  OUT.FILE="TFT/chanpotvg8.xls"

SOLVE V(GATE)=12 V(SOURCE)=0 V(DRAIN)=0
PLOT.1D POTENTIA X.START=33 X.END=33 Y.START=0.25 Y.END=0.3
+ POINTS COLOR=2 SYMB=6 UNCH
+  OUT.FILE="TFT/chanpotvg12.xls"

SOLVE V(GATE)=16 V(SOURCE)=0 V(DRAIN)=0
PLOT.1D POTENTIA X.START=33 X.END=33 Y.START=0.25 Y.END=0.3
+ POINTS COLOR=2 SYMB=7 UNCH
+  OUT.FILE="TFT/chanpotvg16.xls"


LABEL LABEL="Vgs=0" SYMB=1
LABEL LABEL="Vgs=2" SYMB=2
LABEL LABEL="Vgs=4" SYMB=3
LABEL LABEL="Vgs=6" SYMB=4
LABEL LABEL="Vgs=8" SYMB=5
LABEL LABEL="Vgs=12" SYMB=6
LABEL LABEL="Vgs=16" SYMB=7


COMMENT ********************************************************************************
COMMENT ********************************************************************************

CONTACT NAME=DRAIN RESIST=2.5E7
CONTACT NAME=SOURCE RESIST=15E7
COMMENT CONTACT NAME=DRAIN CON.RESI=5
COMMENT SOLVE

COMMENT Id-Vgs Vd=4
LOG OUT.FILE=TFT/TFTVD4.IVL
SOLVE V(GATE)=-5 V(SOURCE)=0 V(DRAIN)=4 ELEC=GATE VSTEP=.2 NSTEP=100
LOG CLOSE
PLOT.1D Y.AX=I(DRAIN) X.AX=V(GATE) IN.FILE=TFT/TFTVD4.IVL SYMB=1 LOG OUT.FILE="TFT/TFTid-
vgsvd4.xls"
+ Title="Id - Vgs for 23um TFT"
+ LEFT=-10 BOTTOM=1E-18

COMMENT Id-Vgs Vd=8
LOG OUT.FILE=TFT/TFTVD8.IVL
SOLVE V(GATE)=-5 V(SOURCE)=0 V(DRAIN)=8 ELEC=GATE VSTEP=.2 NSTEP=100
LOG CLOSE
PLOT.1D Y.AX=I(DRAIN) X.AX=V(GATE) IN.FILE=TFT/TFTVD8.IVL SYMB=2 UNCH LOG
OUT.FILE="TFT/TFTid-vgsvd8.xls"

COMMENT Id-Vgs Vd=12
LOG OUT.FILE=TFT/TFTVD12.IVL
SOLVE V(GATE)=-5 V(SOURCE)=0 V(DRAIN)=12 ELEC=GATE VSTEP=.2 NSTEP=100
LOG CLOSE
PLOT.1D Y.AX=I(DRAIN) X.AX=V(GATE) IN.FILE=TFT/TFTVD12.IVL SYMB=3 UNCH LOG
OUT.FILE="TFT/TFTid-vgsvd12.xls"
```

```
LABEL LABEL="Vds=4" SYMB=1
LABEL LABEL="Vds=8" SYMB=2
LABEL LABEL="Vds=12" SYMB=3


COMMENT ******************************************************************************
COMMENT ******************************************************************************

COMMENT ID-VDS Graphs
COMMENT (VG=8)
LOG OUT.FILE=TFT/TFTVG8.IVL
SOLVE V(GATE)=8 V(SOURCE)=0 V(DRAIN)=0 ELEC=DRAIN VSTEP=.2 NSTEP=100
LOG CLOSE
PLOT.2D FILL Title="Vg=8 for TFT L=23um"
CONTOUR FLOWLINES
PLOT.2D Title="Vg=8 for TFT L=23 um"
CONTOUR POTENTIA
PLOT.1D POTENTIA X.START=8 X.END=8 Y.START=0.25 Y.END=0.4
PLOT.1D POTENTIA X.START=0 X.END=43 Y.START=0.25 Y.END=0.25
+ Title="Potential Along the front inteface"
PLOT.1D ELECTRON X.START=5 X.END=38 Y.START=0.25 Y.END=0.25
+ BOT=1E5 Y.LOGARI COLOR=2 OUT.FILE="profileVg08.xls"
+ Title="Electron Concentration Along the front inteface"
PLOT.1D J.TOTAL X.START=0 X.END=10 Y.START=0.3 Y.END=0.3
+ POINTS COLOR=2   Title="Current Density across drain"
+ OUT.FILE="TFT/TFTJDVg08.xls"
PLOT.1D J.TOTAL X.START=33 X.END=43 Y.START=0.3 Y.END=0.3
+ POINTS COLOR=2  Title="Current Density across Source"
+ OUT.FILE="TFT/TFTJSVg08.xls"


COMMENT (VG=12)
LOG OUT.FILE=TFT/TFTVG12.IVL
SOLVE V(GATE)=12 V(SOURCE)=0 V(DRAIN)=0 ELEC=DRAIN VSTEP=.2 NSTEP=100
LOG CLOSE
PLOT.2D FILL Title="Vg=12 for TFT L=23um"
CONTOUR FLOWLINES
PLOT.2D Title="Vg=12 for TFT L=23 um"
CONTOUR POTENTIA
PLOT.1D POTENTIA X.START=8 X.END=8 Y.START=0.25 Y.END=0.4
PLOT.1D POTENTIA X.START=0 X.END=43 Y.START=0.25 Y.END=0.25
+ Title="Potential Along the front inteface"
PLOT.1D ELECTRON X.START=5 X.END=38 Y.START=0.25 Y.END=0.25
+ BOT=1E5 Y.LOGARI COLOR=2 OUT.FILE="profileVg12.xls"
+ Title="Electron Concentration Along the front inteface"
PLOT.1D J.TOTAL X.START=0 X.END=10 Y.START=0.3 Y.END=0.3
+ POINTS COLOR=2   Title="Current Density across drain"
+ OUT.FILE="TFT/TFTJDVg12.xls"
PLOT.1D J.TOTAL X.START=33 X.END=43 Y.START=0.3 Y.END=0.3
+ POINTS COLOR=2   Title="Current Density across Source"
+ OUT.FILE="TFT/TFTJSVg12.xls"



COMMENT (VG=16)
LOG OUT.FILE=TFT/TFTVG16.IVL
SOLVE V(GATE)=16 V(SOURCE)=0 V(DRAIN)=0 ELEC=DRAIN VSTEP=.2 NSTEP=100
LOG CLOSE
```

```
PLOT.2D FILL Title="Vg=16 for TFT L=23um"
CONTOUR FLOWLINES
PLOT.2D Title="Vg=16 for TFT L=23 um"
CONTOUR POTENTIA
PLOT.1D POTENTIA X.START=8 X.END=8 Y.START=0.25 Y.END=0.4
PLOT.1D POTENTIA X.START=0 X.END=43 Y.START=0.25 Y.END=0.25
+ Title="Potential Along the front inteface"
PLOT.1D ELECTRON X.START=5 X.END=38 Y.START=0.25 Y.END=0.25
+ BOT=1E5 Y.LOGARI COLOR=2 OUT.FILE="profileVg16.xls"
+ Title="Electron Concentration Along the front inteface"
PLOT.1D J.TOTAL X.START=0 X.END=10 Y.START=0.3 Y.END=0.3
+ POINTS COLOR=2   Title="Current Density across drain"
+ OUT.FILE="TFT/TFTJDVg16.xls"
PLOT.1D J.TOTAL X.START=33 X.END=43 Y.START=0.3 Y.END=0.3
+ POINTS COLOR=2  Title="Current Density across Source"
+ OUT.FILE="TFT/TFTJSVg16.xls"

COMMENT (VG=20)
LOG OUT.FILE=TFT/TFTVG20.IVL
SOLVE V(GATE)=20 V(SOURCE)=0 V(DRAIN)=0 ELEC=DRAIN VSTEP=.2 NSTEP=100
LOG CLOSE
PLOT.2D FILL Title="Vg=20 for TFT L=23um"
CONTOUR FLOWLINES
PLOT.2D Title="Vg=20 for TFT L=23 um"
CONTOUR POTENTIA
PLOT.1D POTENTIA X.START=8 X.END=8 Y.START=0.25 Y.END=0.4
PLOT.1D POTENTIA X.START=0 X.END=43 Y.START=0.25 Y.END=0.25
+ Title="Potential Along the front inteface"
PLOT.1D ELECTRON X.START=5 X.END=38 Y.START=0.25 Y.END=0.25
+ BOT=1E5 Y.LOGARI COLOR=2 OUT.FILE="profileVg20.xls"
+ Title="Electron Concentration Along the front inteface"
PLOT.1D J.TOTAL X.START=0 X.END=10 Y.START=0.3 Y.END=0.3
+ POINTS COLOR=2   Title="Current Density across drain"
+ OUT.FILE="TFT/TFTJDVg20.xls"
PLOT.1D J.TOTAL X.START=33 X.END=43 Y.START=0.3 Y.END=0.3
+ POINTS COLOR=2   Title="Current Density across Source"
+ OUT.FILE="TFT/TFTJSVg20.xls"

COMMENT (VG=24)
LOG OUT.FILE=TFT/TFTVG24.IVL
SOLVE V(GATE)=24 V(SOURCE)=0 V(DRAIN)=0 ELEC=DRAIN VSTEP=.2 NSTEP=100
LOG CLOSE
PLOT.2D FILL Title="Vg=24 for TFT L=23um"
CONTOUR FLOWLINES
PLOT.2D Title="Vg=24 for TFT L=23 um"
CONTOUR POTENTIA
PLOT.1D POTENTIA X.START=8 X.END=8 Y.START=0.25 Y.END=0.4
PLOT.1D POTENTIA X.START=0 X.END=43 Y.START=0.25 Y.END=0.25
+ Title="Potential Along the front inteface"
PLOT.1D ELECTRON X.START=5 X.END=38 Y.START=0.25 Y.END=0.25
+ BOT=1E5 Y.LOGARI COLOR=2 OUT.FILE="profileVg24.xls"
+ Title="Electron Concentration Along the front inteface"
PLOT.1D J.TOTAL X.START=0 X.END=10 Y.START=0.3 Y.END=0.3
+ POINTS COLOR=2   Title="Current Density across drain"
+ OUT.FILE="TFT/TFTJDVg24.xls"
PLOT.1D J.TOTAL X.START=33 X.END=43 Y.START=0.3 Y.END=0.3
+ POINTS COLOR=2   Title="Current Density across Source"
+ OUT.FILE="TFT/TFTJSVg24.xls"
```

```
 COMMENT Plot Results
 PLOT.1D Y.AX=I(DRAIN) X.AX=V(DRAIN) IN.FILE=TFT/TFTVG0.IVL SYMB=1
OUT.FILE="TFT/TFTid-vdsvgs0.xls"
+ Title="Id - Vds for TFT L=23um" LEFT=0 BOTTOM=0 TOP=2e-7
PLOT.1D Y.AX=I(DRAIN) X.AX=V(DRAIN) IN.FILE=TFT/TFTVG8.IVL SYMB=2 UNCH
OUT.FILE="TFT/TFTid-vdsvgs8.xls"
PLOT.1D Y.AX=I(DRAIN) X.AX=V(DRAIN) IN.FILE=TFT/TFTVG12.IVL SYMB=3 UNCH
OUT.FILE="TFT/TFTid-vdsvgs12.xls"
PLOT.1D Y.AX=I(DRAIN) X.AX=V(DRAIN) IN.FILE=TFT/TFTVG16.IVL SYMB=4 UNCH
OUT.FILE="TFT/TFTid-vdsvgs16.xls"
PLOT.1D Y.AX=I(DRAIN) X.AX=V(DRAIN) IN.FILE=TFT/TFTVG20.IVL SYMB=5 UNCH
OUT.FILE="TFT/TFTid-vdsvgs20.xls"
PLOT.1D Y.AX=I(DRAIN) X.AX=V(DRAIN) IN.FILE=TFT/TFTVG24.IVL SYMB=6 UNCH
OUT.FILE="TFT/TFTid-vdsvgs24.xls"

 LABEL LABEL="Vgs=0" SYMB=1
 LABEL LABEL="Vgs=8" SYMB=2
 LABEL LABEL="Vgs=12" SYMB=3
 LABEL LABEL="Vgs=16" SYMB=4
 LABEL LABEL="Vgs=20" SYMB=5
 LABEL LABEL="Vgs=24" SYMB=6
```

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