Design of Sampling Mixer and A/D Converter for High IF Digitization

by

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Abstract

The thesis discusses the issues and solutions in the design of an A/D converters for high IF signals in wireless communication systems. The first part of the thesis examines the problem of harmonic and intermodulation distortion in high frequency MOS sampling mixer circuits. It departs from traditional analysis for such circuits by using the method of Volterra series. Three different distortion mechanisms are identified and analyzed separately for the top-plate sampling mixer: the time-invariant distortion valid for 0 fall time of the gate LO signal, time-varying distortion due to finite fall time and non-uniform sampling distortion due to abrupt cutoff. The thesis adapts and applies the method of Volterra series to all the three mechanisms and derives expressions for distortion for them. It then analyzes the practically important case of bottom-plate sampling. The second part of the thesis discusses issues in the design of a passive sigma-delta modulator operating at the high clock-speeds necessary for adequate SNR and bandwidth. In particular, it discusses the design issues of a BiCMOS comparator consisting of a preamplifier and regenerative-latch with low input-referred noise and high clock-speed. Finally, the design issues and implementation details of an experimental, proof of concept, IF digitizer using a passive loop-filter based sigma-delta A/D converter in a 0.8 μ m BiCMOS technology are discussed. The prototype achieves an SNR of 72 dB, HD2 of -72 dB,IM_3 of -65 dB for a -3 dBm 100MHz IF input signal at a power level of 12.5 mW.

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Chapter 1

Introduction

1.1 Background and Motivation

The signal processing requirements imposed by conditions in a wireless communication channel (in contrast to other kinds of information channels) is one of the most challenging in a scientific and technical sense. This challenge comes about because of the fact that, though the physics of electromagnetic propagation, through say a transmission line, is well understood, a good deal of confusion still exists among the scientific community around issues related to mathematic modeling, circuit representation,device operation, figures of merit and measurement techniques at RF (radio frequencies). Added to this are technical difficulties relating to the harshness of the wireless channel: the extremes of received power level of the desired signal(possibly varying rapidly with time) together with extremes of power levels of the interfering channels, and the great diversity in the type and number of interfering signals.

Traditionally, a divide and conquer approach has been used to overcome the effect of strong interfering signals occupying nearby channels and masking a weak desired signal : mixing the received signals down to a lower intermediate frequency(at which it would be easier to amplify as well as filter out undesired signals) band-

pass filtering the lower intermediate frequency, amplifying it and repeating the same strategy for a lower intermediate frequency. This approach is shown in Fig. 1.1 and is known as heterodyning. The last mixing stage is usually a part of a detector and consists of a pair of mixers with their local oscillators (LO) in quadrature(90 degrees phase shifted from each other). This is done in order to preserve the phase information of the signal. The variation in the desired signal strength is compensated with an automatic-gain-control circuit(AGC). This approach, though the mainstay of almost all conventional wireless receiver designs, has many drawbacks. The first is the complexity and cost of the approach when implemented in IC form: each IF filtering stage requiring external LC/crystal/ceramic filter, each mixer stage requiring a separate local oscillator(LO). Another drawback is the excessive power dissipation in this architecture due to multiple mixers, amplifiers, and off-chip driver stages and portability issues due to the size and weight of batteries.

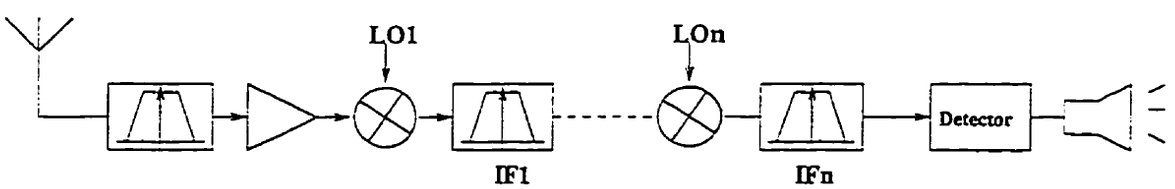


Figure 1.1: Principle of radio detection using multiple IF stages

Another approach to the complexity of the wireless signal processing problem has been the conversion of the wireless signal at any stage of the signal processing chain into digital form. Digital representation of the signal allows channel selection(filtering),gain control and demodulation with an accuracy and repeatability that is difficult to achieve using internal or external analog components. This also has important manufacturing advantages for high-volume wireless based consumer products such as cellular phones since trimming procedures can be eliminated. Even though A/D conversion has been used for baseband or low IF signal processing in wireless transceivers, its use in IF processing has been limited so far. One of the reasons for the slow evolution of IF A/D conversion is that sampling has been tra-

ditionally understood as an ideal mathematical operation of taking uniform instantaneous snapshots of a signal and is therefore quite removed from the complexity of the real world circuits in which a host of circuit imperfections cause deviation (and therefore distortion and noise) from the mathematical ideal. This thesis examines the issues involved in the A/D conversion of high IF signals (lying in the 100-150 MHz frequency) and clarifies the prospects for conversion of higher IF or even RF frequencies lying at or beyond 900 MHz.

1.1.1 Comparison with State of the Art

A first step in the direction of IF A/D conversion is a 13 bit sigma-delta A/D converter with built-in mixer for 10 MHz IF input frequency using CMOS technology by Feng Chen [1] . However, there are two limitations to this work. First of all, this work is limited to a relatively low IF of about 10 MHz. Secondly, the modulator clock frequency, which decides the oversampling ratio and therefore the SNR, is limited also to 10 MHz. One of the reasons for this is that the gain-boosting circuit upon which this work relies to improve SNR, degrades the distortion distortion performance at high IF input and clock frequencies.

A second approach using a bandpass sigma-delta modulator uses a clock that is four times the IF frequency. Simply as a consequence of this fact, the achievable SNR may be poor and the power dissipation may be excessive. Additional dissipation may be due to the active(opamp based) loop-filters used though opamp sharing architectures do help to reduce the power somewhat. The main advantage of this approach is that I-Q separation may be done very easily(by selecting alternate bits). Since I-Q separation is done in the digital domain, I-Q path mismatch does not occur. A design that combines IF AGC stage, subsampling gain stage and bandpass sigma-delta modulator has been reported in [2]. However, measurement results show a peak SNR of about 60 dB for an IF of 80 MHz. This work also does not report 2

tone measurement results at 80 MHz IF.

This thesis overcomes the limitation of the prior state of art in the most important areas. First, the sample-and-hold circuit, that is essentially a mixer, is analyzed using the method of Volterra Series. This analysis is further extended to the time-varying case when the clock waveform has finite fall-time. Using this analysis the distortion behaviour of the mixer can be predicted upto a few hundred MHz or even higher and has been experimentally verified upto 100 MHz. Secondly, the modulator SNR has been improved by using BiCMOS technology
(a) by making use of the high g_m of the bipolar transistor in the comparator to reduce its equivalent input noise
(b) by increasing the modulator clock frequency and hence the oversampling ratio by a faster BiCMOS circuit design.

In this chapter, direct sampling and A/D conversion of an IF signal is discussed and considered as an alternative to the conventional approach: mixing down the IF signal, performing low-pass filtering on it and following it by a baseband A/D converter. The concepts of image rejection, intermodulation distortion(IM_3) related to mixers and demodulators are introduced. Finally, the bandpass sampling mixer is introduced and compared with conventional MOS Gilbert mixer for low frequencies.

1.2 Bandpass Sampling

The Nyquist criterion specifies that the minimum sampling rate for a band-limited signal is twice the maximum frequency component in the signal. For a bandpass signal of bandwidth 2B and centered around a frequency f_c the sampling rate specified by this criterion is $2f_c + 2B$. However, a simple extension of the sampling theorem shows that such a rate may not be the minimum necessary for perfect reconstruction of the signal. The *Bandpass Sampling Criterion* specifies that the minimum rate at which the A/D converter has to sample in order to preserve the information

content of the signal(i.e. no spectrum overlap of the frequency shifted versions of the input signal spectrum) lies between 4B and 8B [3]. This is illustrated in Fig. 1.2. This criterion, therefore, relaxes the sampling rate requirements on the A/D converter. A critical requirement for bandpass sampling A/D converters is that the sample-and-hold circuit be able to instantaneously sample the bandpass signal with sufficient accuracy. A second critical requirement is that the signal be sufficiently band-limited using bandpass filters to prevent the aliasing of components outside the signal bandwidth.

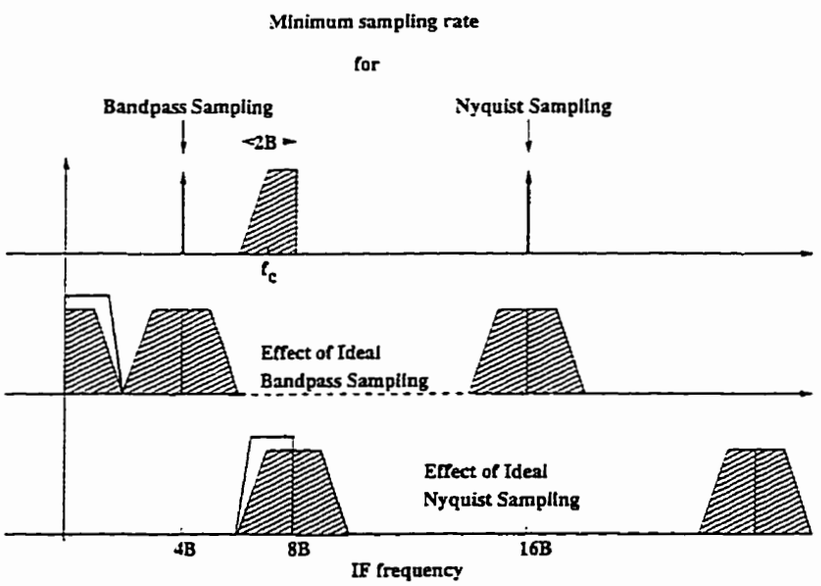


Figure 1.2: Effect of Nyquist and bandpass sampling of an IF signal

It is clear that ideal bandpass sampling, apart from continuous to discrete time conversion, also achieves frequency down-conversion or *mixing* by shifting the center frequency of the bandpass signal by a multiple of the sampling rate so that in the discrete-time-frequency domain it lies between 0 and half the sampling rate. In this sense the sample-and-hold (sometimes known as track-and-hold) circuit component of the A/D converter can and will be referred to as the *sampling mixer*. For the case of narrow-band signals ($f_c >> 2B$), if a sampling rate that is a sub-multiple of

the the maximum frequency ($f_c + B \approx f_c$) is chosen, the sampling mixer is referred to as *sub-sampling mixer*. The overall scheme of IF down-conversion(mixing) and A/D conversion is shown in Fig. 1.3. The baseband A/D converter is clocked at a sampling rate that is large enough to accommodate the signal band. The baseband switched-capacitor network may provide some channel selectivity and/or signal gain. This architecture essentially isolates the problem of IF A/D conversion into a problem of bandpass sampling with a well-designed sampling mixer and the problem of processing discrete-time signals with relatively small bandwidth as compared to the IF signal center frequency f_c using a baseband switched-capacitor network and finally the A/D conversion of the discrete-time samples.

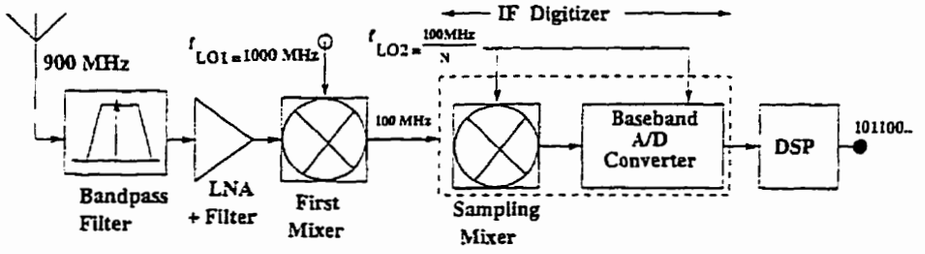
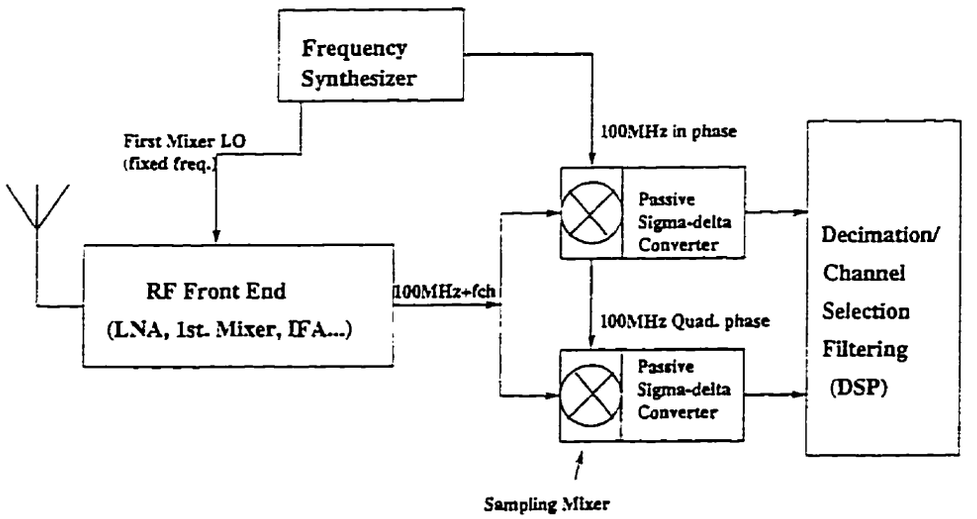


Figure 1.3: Overall scheme of IF digitization using bandpass sampling

1.3 A Radio Architecture using IF Digitization

A radio system that uses bandpass sampling of IF signals is shown in Fig. 1.4. Signals from the antenna are processed through an RF front-end consisting of RF pre-selection filters,LNA, first Mixer, IF amplifier, IF filter and AGC. The output of this front-end is the desired channel as well as undesired channels in the same band. The first mixer LO is of fixed frequency. Channel selection is done by tuning the frequency of the second mixer LO. Since this is at the first IF frequency and not near the frequency of the RF signal, the phase noise specifications are easier to meet. The choice of the first IF frequency comes from image rejection requirements that

constrain the first IF to be about one-tenth of the frequency of the RF signal. This leads to a first IF frequency of about 100 MHz for a 900 MHz RF signal. The output of the RF front-end is now processed through two separate A/D converters that sample and mix down to baseband or to a low second IF using two separate sampling mixers with their sampling (LO) clocks in quadrature phase. This method of mixing and detection is known as *quadrature mixing* and *quadrature detection*. Each of these A/D converters (including their associated sampling mixer) are referred to hereafter as an *IF digitizer*.



Radio Architecture for 100 MHz IF Digitization

Figure 1.4: A radio architecture using 100 MHz IF A/D conversion

1.4 Thesis Organization

This thesis is concerned mainly with the design of the IF digitizer. Two of the essential blocks of the digitizer are the sampling mixer and the baseband A/D converter. Chapter 2 summarizes the physical mechanisms in the MOS device that degrade

the resolution of the sampling mixer by adding distortion and noise. Chapter 3 contains a mathematical analysis of the distortion mechanism in the sampling mixer using Volterra series. Chapter 4 discusses the the issues related to the design of the baseband A/D converter specifically concentrating on passive sigma-delta modulator implementation for low power. Chapter 5 discusses the design of a prototype proof-of-concept IF digitizer, measurement results,chip layout and PCB layout issues.

1.5 Specifications of IF Mixers

Mixers are difficult to characterize from the viewpoint of gain, distortion and noise. Additional difficulties lie in measurement techniques for important figures of merit. For example, a figure of merit for noise may be specified in terms of equivalent input-referred noise voltages and currents as is frequently done for low-frequency analysis. However, at high frequencies such measurements are difficult to carry out and even lose meaning when transmission lines are involved since voltages and currents change along a transmission line that is not matched at both ends. Instead, signals are characterized in terms of power and the mixer characterized in terms of scattering ('s') parameters. Nevertheless, important features of circuit behavior do not change if the terminal voltage point of view is retained for both analysis and measurements.

1.5.1 Dynamic Range Specifications

The dynamic range requirement on the mixer specifies two extreme input signal levels over which the mixer is able to detect weak desired channel signals:

- Distortion Limit: Strong adjacent channel interferers with the weak desired channel signal(Fig. 1.5-a)

- Noise Limit: Extremely weak desired channel signal barely resolvable above the noise floor.(Fig. 1.5-b)

Distortion in the mixer produces harmonic and intermodulation components in the desired band due to the presence of strong interference signals. The dynamic range requirements on the mixer are dependent upon the filtering and gain distributions in the receiver as well as the AGC design. For example, the dynamic range of an IF digitizer with a resolution of $DR\ dB$ can be improved to $(DR + A_{agc})\ dB$ if the digitizer is preceded by an AGC with a maximum gain of A_{agc}.

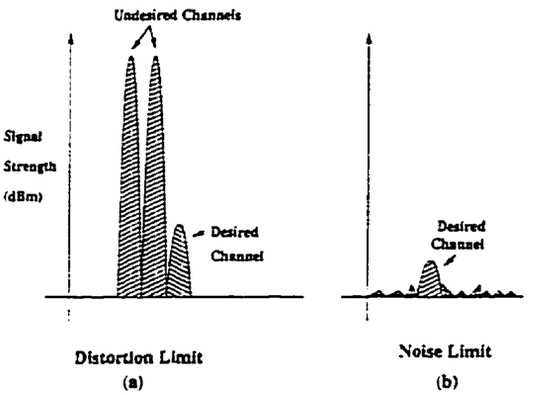


Figure 1.5: Dynamic range requirements

Distortion specifications

Distortion in an amplifier circuit may be specified to be of harmonic or intermodulation type. For example, if a sinusoid $A \cdot sin(2\pi f_{RF} t)$ is applied to a circuit input, the harmonic distortion of n'th order, HD_n may be defined to be the ratio of the magnitude of the frequency component at nf_{RF} appearing at the output to that at f_{RF}. If two tones at f_1 and f_2 are applied at the input, the output consists of tones which in general are at $mf_1 \pm nf_2$. The IM_2^+ is defined to be the ratio of the magnitude of the distortion component at $f_1 + f_2$ at the output to the component at f_1 applied at the input. IM_2^- may be analogously defined by considering the magnitude of the output distortion component at $f_1 - f_2$. The

IM_3 is defined to be the ratio of the magnitude of the distortion component at $2f_1 - f_2$ at the output to the component at f_1. In the case of mixers, the distortion components and the signal component of interest will be shifted by the local-oscillator frequency f_{LO} and its harmonics. This will be discussed further in chapter 3.

Image rejection specifications

One of the problems inherent in a mixer is that when it down-converts a signal at frequency f_{RF} to an intermediate frequency f_{IF} with a local oscillator clock at f_s, the mixer will down-convert the desired signal at $f_{RF} = f_s - f_{IF}$ as well as an image signal at $f_{RF-image} = f_s + f_{IF}$. Thus the mixer may become sensitive to strong interfering signals located at $2f_{IF}$ above the desired signal. This problem may be alleviated by using bandpass filters and tuned amplifiers preceding the mixer which filter out the image band as illustrated in Fig. 1.6. It may also be overcome by a specially designed *image reject mixer* which converts the desired RF signal an into analytic form (which is a complex representation that has a one-sided spectrum), and performing ideal frequency shifts in the complex domain. The image suppression using this technique is limited by the accuracy of complex multiplications.

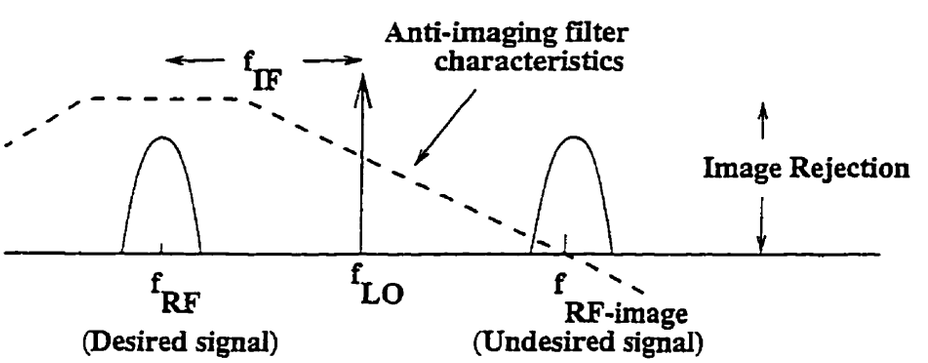


Figure 1.6: Image rejection using a bandpass filter

The image rejection of a mixer is defined as the ratio of the sensitivity in the image band of the mixer to its sensitivity in the signal band. This specification depends upon the spectrum allocations in bands adjacent to the desired band.

Noise specifications

The noise specification of the mixer may be expressed in terms of an equivalent noise voltage referred to the input. This specification may be expressed in terms of the Noise Figure by referring the equivalent input noise power to the power developed in a 50 ohm resistor. The equivalent input noise voltage takes into account the thermal, shot and 1/f components of noise in the sampling mixer and the A/D converter. Chapter 4 discusses the analysis of noise for the sampling mixer and the passive loop-filter based sigma-delta modulator.

1.6 A Comparison of Mixer Architectures

In this section, the MOS Gilbert mixer and the NMOS switch mixer are introduced and compared from the viewpoint of distortion. The objective is to show that for relatively low frequencies NMOS switches with capacitive load offer better distortion than MOS Gilbert mixers.

1.6.1 The MOS Gilbert Mixer

The MOS Gilbert mixer is an adaptation of a mixer based upon the 'Gilbert multiplier' [4]. A possible implementation of a MOS Gilbert mixer is shown in Fig. 1.7. For suitably small sinusoidal input signals at $f_{RF}$and f_{LO}, the circuit functions as a multiplier so that the output voltage consists of sinusoids at frequencies $(f_{RF} \pm f_{LO})$. The sinusoidal frequency component at $(f_{RF} + f_{LO})$ will be filtered by the low-pass filter$(R1 - C1)$ formed at the output nodes so that the

mixed down component at $(f_{RF} - f_{LO})$ appears at the output. In a general non-ideal multiplier, the output will consist of sinusoids at $(mf_{RF} \pm nf_{LO})$ for integers m and n, some of which will form distortion components close to and at multiples of the desired downconverted signal at $(f_{RF} - f_{LO})$.

In practice, the mixer is operated with large LO signals and small RF signals. The transistors M3,M4,M5,M6 behave as commutating switches which are either in the triode region when the LO signal is 'HIGH' and in cutoff when LO is 'LOW'. Their function is to steer the differential drain current in the emitter-coupled pair M1-M2 into one output node or the other depending upon the polarity of the LO signal. It may be easily shown that in this mode of operation, the differential output current flowing into the output nodes is equal to the differential drain current of the source-coupled pair multiplied by a periodic square wave waveform, S(t), that has an alternating pattern($\div$1,-1,+1 ..) with 50 % duty cycle, with a DC value of 0 and with a period of $T_s = 1/f_{LO}$. This square-wave function can be expanded into a Fourier series:

$$S(t) = \sum_{i=1}^{\infty} b_i cos(\omega_{LO} t)$$

where the switching coefficients are obtained as

$$b_i = \frac{sin(n\pi/2)}{n\pi/2} \tag{1.1}$$

We therefore obtain $b_1 = \frac{2}{\pi}, b_2 = 0, \quad b_3 = \frac{2}{3\pi}$.

Under these ideal switching conditions, the distortion of the mixer is primarily governed by the distortion in the source-coupled pair M1,M2. The distortion in the mixer may be obtained by expanding the differential output current of the source-coupled pair($i_o = i_{d1} - i_{d2}$) as a power series expansion of the differential input voltage v_{in}:

$$i_o = a_1 v_{in} + a_2 v_{in}^2 + a_3 v_{in}^3 \ldots$$

where $a_1 = \sqrt{I_{EE} K'} \quad a_2 = 0 \quad a_3 = -\frac{1}{16} \frac{K'^{3/2}}{\sqrt{I_{EE}}}$

The voltage developed at the output without the low-pass filter is therefore:

$$v_o = (a_1 v_{in} + a_3 v_{in}^3 + \ldots) \left(\sum_{n=1}^{\infty} b_n cos(n\omega_{LO} t) \right)$$

With a low-pass filter formed at the output nodes by shunting them with capacitances to ground, the output of the mixer may be given by:

$$v_{o-lpf} \approx a_1 b_1 A cos(\omega_{RF} - \omega_{LO})t + a_3 b_3 A^3 cos3(\omega_{RF} - \omega_{LO})t$$

From the coefficients a_i and b_i above we may now determine the harmonic distortion in the output voltage as:

$$HD_2 = 0 \tag{1.2}$$

$$HD_3 = \frac{A^2}{48(V_{GS} - V_t)} \tag{1.3}$$

$$IM_3 = \frac{A^2}{48(V_{GS} - V_t)} \tag{1.4}$$

For a 100 MHz IF mixer design, with a $(V_{GS} - V_t)$ of 0.53V [5] the calculated value of IM_3 is -42.6 dB.

1.6.2 The NMOS switch mixer

An NMOS switch mixer is shown in Fig. 1.8-a. Its basic operation is as a switch that chops the input voltage with a pulse pattern as shown in Fig. 1.8. When the

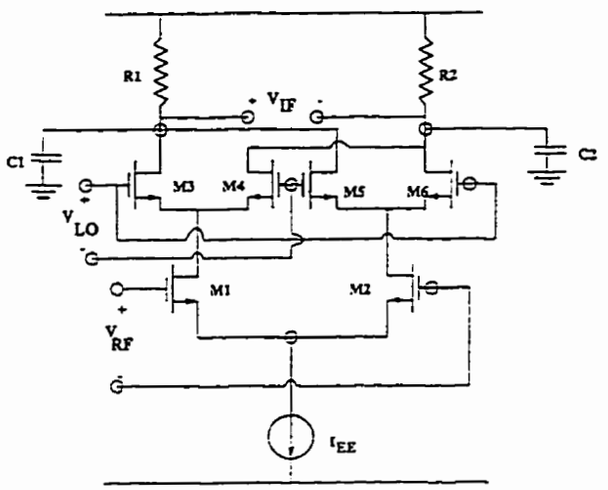


Figure 1.7: Conventional "Gilbert" mixer using MOS transistors

gate voltage is 'HIGH'(VDD), the output approximately follows the input with a deviation that depends upon the switch drain current characteristics. When the gate voltage is 'LOW', the output collapses to the ground voltage. This type of mixer has been extensively studied in [6]

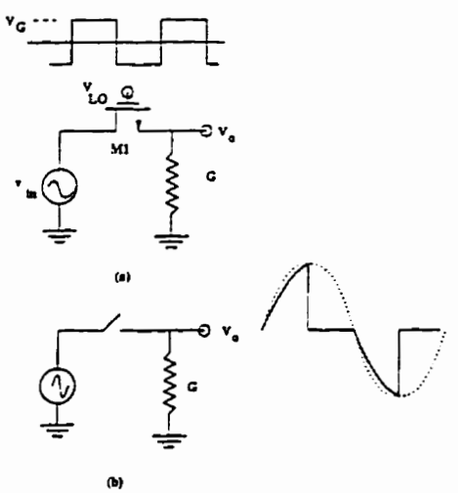


Figure 1.8: MOS switch mixer with a resistive load(a) and its equivalent circuit(b)

The expressions for distortion in the NMOS switch mixer may be derived by assuming a load of conductance G and assuming that the MOS transistor is on so

that it is in the triode region i.e. there is no switching and therefore no mixing operation taking place. The circuit is now said to be operating in the 'amplifier' mode. The output voltage can now be expressed as a power series (or Taylor series) expansion of the input voltage.

$$v_o = H_1 v_i + H_2 v_i^2 + H_3 v_i^3 \ldots$$

The distortion components for the 'amplifier' mode are then obtained directly from the coefficients of the power series expansion of the output voltage. The distortion coefficients in the switching or mixing mode are determined simply by multiplying the coefficients in the 'amplifier' mode by the switching coefficients given by equation (1.1).

If the NMOS transistor has a finite device constant K' and therefore finite conductance, the small-signal non-linear drain current equation can be written as: [1]

$$i_d = K' \left((V_{GS} - V_t)(v_d - v_s) - \frac{1}{2}(v_d^2 - v_s^2) \right)$$

Therefore, replacing v_d by v_o, v_s by v_{in} and g by $K'(V_{GS} - V_t)$ we have:

$$g v_o + G = g v_{in} - \frac{K'}{2}(v_{in}^2 - v_o^2) \tag{1.5}$$

Expressing $v_o = v_{o1} + v_{o2} + \ldots$ where v_{on} is the $n'th$ order distortion component and equating the terms of the same order on both sides, we obtain for small G,

$$H_1 = 1 \tag{1.6}$$

[1] The ac non-linear drain current equation is obtained by re-writing the general MOS equation $I_d = K'((V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2)$ so that the signal dependent term V_S is separated from the $(V_{GS} - V_t)$ term.

$$H_2 = -\frac{K'}{(V_{GS}-V_t)^2} \tag{1.7}$$

$$H_3 = \frac{G}{K'(V_{GS}-V_t)^3} \tag{1.8}$$

The expressions for conversion gain and harmonic distortion terms may be obtained from the power series coefficients, H_n, from the definitions given in 1.5.1. Assuming that the circuit input is a sinusoid $A \cdot cos(\omega_{RF}t)$

$$HD_n = \frac{|H_n \cdot A^n cos^n(\omega_{RF}t)|_n}{|H_1 \cdot A cos(\omega_{RF}t)|_1} \tag{1.9}$$

$$= \frac{H_n \cdot A^{n-1}}{H_1} \tag{1.10}$$

where the operator $|\ |_n$ gives the amplitude of the n'th harmonic.

Assuming that the input consists of a sum of two sinusoids, $(A \cdot cos\omega_{RF1}t + A \cdot cos\omega_{RF2}t)$, the third order intermodulation distortion may be derived as,

$$IM_3 = \frac{3H_3 \cdot A^2}{H_1} \tag{1.11}$$

From the above definitions, the conversion gain(H_1), harmonic and intermodulation distortion in an NMOS switch mixer with resistive load and operating in the 'amplifier' mode may be obtained as,

$$H1 = 1 \tag{1.12}$$

$$HD_2 = \frac{AG}{2K'(V_{GS}-V_t)^2} \tag{1.13}$$

$$HD_3 = \frac{A^2G}{4K'(V_{GS}-V_t)^3} \tag{1.14}$$

$$IM_3 = \frac{3A^2G}{4K'(V_{GS}-V_t)^3} \tag{1.15}$$

where A is the amplitude of the input signal, K' is the device constant equal to $\mu C_{ox}\frac{W}{L}$, V_{GS} is the gate-source bias and V_t is the effective threshold voltage.

It may be observed that as $G \to 0$, the distortion components tend vanish since the non-linear drain current becomes vanishingly small. This leads to the expectation that if the load of conductance G is replaced by a capacitive load with susceptance ωC the distortion in the mixer may be small for sufficiently small ω and C. This circuit now becomes a sampling mixer.

The exact calculation of harmonic and intermodulation distortion in a sampling mixer cannot be done by using a power series. This is because power series analysis assumes that the circuit consists of memoryless(purely resistive) non-linearities. Although in some cases a simple substitution of G by $j\omega C$ gives correct results, this substitution fails in general. For a precise and complete analysis, which gives correct predictions for distortion, it is necessary to use Volterra Series. This issue will be revisited in chapter 3 where Volterra Series is introduced.

In addition to the distortion due to a non-linear drain current, the sampling mixer suffers from a number of impairments that degrade the noise and distortion performance of the circuit. The next chapter will summarize the physical mechanisms of the NMOS device that limit the accuracy of the sampling mixer circuit.

Chapter 2

Accuracy Limitations in MOS sampling mixers

In the previous chapter it was shown that an NMOS switch mixer with capacitive load is superior in terms of its distortion performance compared to the MOS Gilbert mixer. The mixer is now known as the simple or the top-plate sampling mixer and is shown in Fig. 2.1. The top-plate sampling mixer operates as follows. When the sampling clock voltage applied at the gate is 'HIGH' the transistor is on and the output tracks the input. When the clock voltage goes 'LOW' the transistor is in cutoff, the output is frozen and a sampled voltage is stored on the top-plate of the sampling capacitance, C. Another variation of the sampling mixer is the bottom-plate sampling mixer which will be introduced in chapter 3.

In this chapter, the physical mechanisms of noise and distortion that limit the accuracy of A/D conversion in a MOS sampling mixer will be summarised. These mechanisms set limits to the signal-to-distortion ratio, SDR, and the signal-to-noise ration,SNR that can be achieved by the circuit. They also serve to illustrate the basic tradeoffs between the signal-to-noise and signal-to-distortion ratio in the MOS sampling mixer. Since the MOS sampling mixer is the most

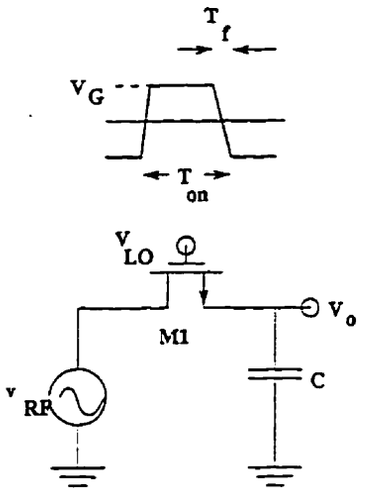


Figure 2.1: The top-plate sampling mixer

important circuit block that limits the performance of an A/D converter for IF digitization, it will set the performance limits for the overall A/D converter as well.

2.1 Distortion Limits in a MOS Sampling Mixer

The distortion in a MOS sampling mixer occurs mainly due to:

1. drain current as a non-linear function of the source and drain voltages with the gate voltage assumed fixed
2. modulation of threshold voltage due to body effect
3. non-linear source and drain capacitances
4. "aperture effects" due to finite fall time of the gate voltage
5. channel charge as a non-linear function of the source and drain voltages

A complete and accurate calculation of distortion for the sampling mixer due to items (1)-(3) can only be done by formulating a non-linear time invariant

system and using the Volterra Series method to solve for distortion. This will be done in chapter 3. An accurate calculation of aperture effects on distortion is more difficult and will be done using the time-varying formulation of a Volterra Series in the same chapter. In this section a simple estimation of distortion due to drain current non-linearity and the non-linear channel-charge will be calculated using power series analysis.

2.1.1 Distortion due to MOS Drain Current Non-linearity

In the previous chapter the expressions for distortion for NMOS switch mixers with a resistive load were calculated assuming an 'amplifier' mode of operation. If the output of the circuit is observed in the discrete-time domain (i.e. taking snapshots of the mixer output at sampling intervals) and assuming that the bandpass sampling criterion holds, the the discrete-time frequency spectrum is a periodic non-overlapping replication of the spectrum in the continuous-time domain at intervals of the sampling frequency. Thus, under a set of ideal switching conditions (such as 0 fall-time and no charge injection), it may be sufficient to obtain an estimate of harmonic distortion by determining the distortion of the mixer in the 'amplifier' mode. For a sampling mixer a first order estimate of the distortion may be obtained by replacing G in the NMOS switch mixer by $j\omega C$ where C is the total sampling capacitance. This leads to the following formulae for distortion,

$$HD_2 = \frac{A\omega C}{2K^{'}(V_{GS} - V_t)^2} \tag{2.1}$$

$$HD_3 = \frac{A^2\omega C}{4K^{'}(V_{GS} - V_t)^3} \tag{2.2}$$

where A is the amplitude of the input signal, $K^{'}$ is the device constant equal to $\mu C_{ox}\frac{W}{L}$, V_{GS} is the gate-source bias and V_t is the effective threshold voltage.

The minimum distortion will occur when there is no explicit load capacitance at the output and the total capacitance consists of the source/drain to substrate capacitance of the device only. These junction capacitances are a function of the geometry of the transistor and the technology used. If the load capacitance is expressed as $C = cWLC_{ox}$ where WLC_{ox} is the total gate capacitance, where c is the scale factor between the source/drain capacitance and the gate capacitance, and L is the minimum effective length of the transistor, we may write the expressions for harmonic distortion as follows:

$$HD_2 = \frac{AcL^2\omega}{2\mu(V_{GS} - V_t)^2} \tag{2.3}$$

$$HD_3 = \frac{A^2cL^2\omega}{4\mu(V_{GS} - V_t)^3} \tag{2.4}$$

Note that the quantity $\frac{L^2}{\mu(V_{GS} - V_t)}$ is proportional to the f_T of the process. Thus, the lower bound on the harmonic distortion of the sampling mixer is independent of the device size and is limited by the process f_T and the IF input frequency. [1] Table 2.1.1 shows the parameters for a 5 V 0.8μ BiCMOS process. Assuming a gate-source bias of 2.5 V, $c = 1$, an effective gate length equal to the minimum effective length, $L = 0.8\mu m$, a $V_t = 0.8147$, an input amplitude $A = 0.316V$ (corresponding to a 0 dBm signal) and an input signal frequency of 100 MHz, an $HD_2 = -66.5dB$ and $HD_3 = -87.1dB$ are obtained.

2.1.2 Distortion due to Charge-injection

In a MOS switched-capacitor circuit the channel charge stored in the MOS switching transistor when it is on, is a non-linear function of the source/drain

[1] A BiCMOS process is assumed because an NMOS based sampling mixer and loop-filter can be used for achieving low distortion and a low noise high-speed bipolar transistor for designing the comparator(1-bit quantizer) of the sigma-delta modulator.

t_{ox}	175 A^o
V_{t0-n}	0.8147 V
μ_n	475 $cm^2/V.s$
N_{sub}	$3.62e+16/m^3$
ϕ_f	$0.393V$
γ	$0.561\sqrt{V}$
$\frac{\Delta C_j}{\Delta W}$	$1.5fF/\mu m$

Table 2.1: Typical BiCMOS process parameters

terminal voltages.

$$Q_{channel} = C_{ox}WL\left((V_{GS} - V_t) - \gamma(\sqrt{v_s - v_B + 2\phi_f} - \sqrt{2\phi_f})\right) \qquad (2.5)$$

where v_s is the small-signal source voltage, v_B is the bulk bias and $2\phi_f$ is the surface potential of a transistor in strong inversion. When the transistor turns off, this stored charge is redistributed between the source and drain terminals and will therefore contribute to distortion. The charge partitioning depends upon a switching parameter $B = (V_{GS} - V_t)\sqrt{\frac{K'}{aC}}$ and the ratio of the capacitances at the source and drain terminals, where a is the fall slew-rate of the voltage applied at the gate and C is the load capacitance [7]. Here the worst case distortion due to charge injection in a simple representative passive switched-capacitor circuit will be analyzed. This circuit is shown in Fig. 2.2. M1 and C_s form a sampling mixer. C_s is assumed to be much smaller than the dump capacitance, C_L. The gain of this circuit is unity for sufficiently small input frequencies near DC so that low frequency distortion components at the output can be referred to the input directly. The distortion due to charge-injection occurs when M1 and M2 turn off at the end of clock-phase $\phi 1$ and $\phi 2$, respectively.

M1 turning off: If the turnoff of M1 is slow due to a large fall time in the clock phase $\phi 1$, the channel charge flows mostly to the input terminal since the

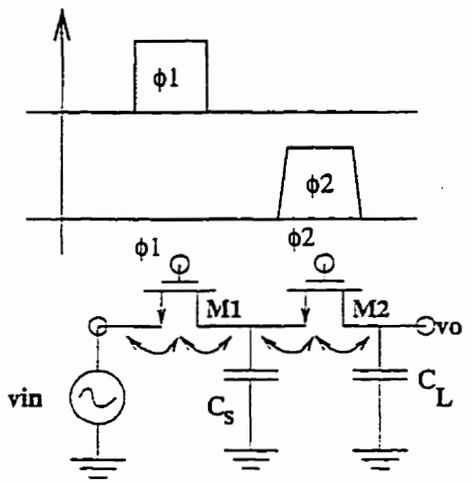


Figure 2.2: Charge-injection in a passive SC circuit

terminal, impedance looking into that node is 0. The worst case distortion occurs when the gate voltage falls instantaneously, so that the MOS transistor cuts off abruptly. Under this condition, the channel charge is partitioned equally between the two terminals. Assuming small-signal conditions, the signal dependent components in equation (2.5) can be expanded as

$$Q_{sig-channel} = C_{ox}WL\gamma\sqrt{V_X}\left(\frac{1}{2}(\frac{v_s}{V_X}) - \frac{1}{8}(\frac{v_s}{V_X})^2 + \frac{1}{16}(\frac{v_s}{V_X})^3 \ldots\right) \tag{2.6}$$

where $V_X = (-V_B + 2\phi_f)$.

This expression leads to a power series expansion of v_o, the sampled voltage as follows:

$$v_o = v_s + \frac{C_{ox}WL\gamma\sqrt{V_X}}{C_s}\left(\frac{1}{2}(\frac{v_s}{V_X}) - \frac{1}{8}(\frac{v_s}{V_X})^2 + \frac{1}{16}(\frac{v_s}{V_X})^3 \ldots\right) \tag{2.7}$$

From this equation the power series coefficients may be derived as:

$$H_1 = 1.0 \tag{2.8}$$

$$H_2 = -\frac{C_{ox}WL\gamma}{16C_sV_X^{\frac{3}{2}}} \tag{2.9}$$

$$H_3 = \frac{C_{ox}WL\gamma}{32C_sV_X^{\frac{5}{2}}} \tag{2.10}$$

Assuming an input sinusoid of amplitude A, the expressions for harmonic distortion may now be derived as :

$$HD_2 = \frac{AC_{ox}WL\gamma}{32C_sV_X^{\frac{3}{2}}} \tag{2.11}$$

$$HD_3 = \frac{A^2C_{ox}WL\gamma}{128C_sV_X^{\frac{5}{2}}} \tag{2.12}$$

Upon substitution of a reasonably small sampling capacitance of $C_s = 0.2pF$, $W/L = 100\ \mu m/0.8\mu m$ (based upon an optimal design given in chapter 5) and the relevant parameters from Table 2.1.1 we obtain an $HD_2 = -62.6dB$ and $HD_3 = -94.9dB$ for $A = 0.316V$.

M2 turning off: In this case, only the channel charge of M2 injected into C_L matters, since the charge injected into C_s will be discharged during the next ϕ_1 phase of the clock anyway, when C_s samples the input. Under the worst case condition that the gate voltage fall-time is sufficiently large and $C_s \ll C_L$, almost all the channel charge will flow into C_L, However, since C_L is much larger than C_s, the distortion voltage components will be much smaller than for the case when M1 turns off.

2.2 Noise in a MOS Sampling Mixer

The sources of noise that limit the SNR in MOS sampling mixers are :

- Thermal Noise due to MOS switching transistors
- Phase-noise in the sampling clock

- Wide-band noise at the input

The effect of thermal noise of the transistors constituting the sampling mixer has already been discussed in [8]. The essential result is that the equivalent input noise variance is given by $v_n^2 = kT/C_s$ and that the noise power-spectral-density (PSD) is given by,

$$S(f) = \frac{2kT}{f_s C} \tag{2.13}$$

Phase Noise in the sampling(LO) clock:

Assuming that the sampling clock of period T is jittered by a random process $\zeta(t)$, with power spectral density $S_\zeta(f)$, the PSD of the oscillator output can be shown to be [9]:

$$S_C(f) = \frac{B^2}{4}\left(\delta(f) + (2\pi f_s)^2 S_\zeta(f)\right) * (\delta(f+f_s) + \delta(f-f_s)) \tag{2.14}$$

This equation says that the effect of the jitter process is to modulate the jitter spectrum around the LO center frequency, f_s, with a scale factor of $\frac{B^2}{4}(2\pi f_s)^2$. When an RF signal is sampled with such a jittered clock, PSD of the sampled error is given by is given by:

$$S_\epsilon(f) = \frac{A^2}{4}\left((2\pi f_{RF})^2 S_\zeta(f - f_{RF} + kf_s)\right) \tag{2.15}$$

where the the IF frequency is given by $kf_s - f_{RF}$. The noise variance may be calculated by assuming that the jitter process has a uniform spectral density $S_\zeta(f)$, and with variance $R_\zeta(0) = \Delta_{\tau_j}^2$:

$$v_{n-jitter}^2 = R_\epsilon[0] = \frac{A^2}{2}[(2\pi f_{in})^2 R_\zeta(0)] \tag{2.16}$$

$$= \frac{A^2}{2}\left(2\pi f_{in}\Delta_{\tau_j}\right)^2 \tag{2.17}$$

The noise spectral density due to jitter at the output for a given sampling clock frequency may now be written as :

$$\frac{v_{n-jitter}^2}{\Delta f} = \frac{A^2}{f_s}\left(2\pi f_{in}\Delta_{\tau_j}\right)^2 \tag{2.18}$$

We may therefore observe that for a given rms noise jitter in the sampling clock period, the total rms output noise voltage originating from jitter is proportional to the amplitude and frequency of the IF input. This has important system design implications since the phase noise of the sampling clock produced by a synthesizer may have to be designed for an adequately small jitter. From the above formula, in order to obtain an SNR of 80 dB for a 0 dBm, 100 MHz IF input, a 10 MHz sampling clock and a 20 kHz signal bandwidth, the maximum rms jitter allowed is 1.78 picoseconds.

Wide-band Noise at the input: A simple estimate of the output power spectral density in a sampling mixer due to wide-band noise from the IF input may be had by first observing that the finite sampling bandwidth of the sampling mixer when the NMOS transistor is on will filter out wide-band input noise. This low-pass filtered noise is sampled in the ideal sense as illustrated in Fig. 2.3. The undersampling of wide-band noise from the input results in aliasing of noise spectral components lying beyond $\frac{f_s}{2}$, as illustrated in Fig. 2.3. Assuming a wide-band input noise source of uniform(white) spectral density N_i, the noise spectral density at the output of the sampling mixer may be calculated simply by summing up the areas of bands around multiples of $f_s/2$ and is found to be:

$$\frac{v_{n-wb}^2}{\Delta f} = \frac{K^{'}(V_{GS}-V_t)N_i}{2C_s f_s} \tag{2.19}$$

$$\frac{v_{n-wb}^2}{\Delta f} = \frac{N_i}{2\tau f_s} \tag{2.20}$$

$$\tag{2.21}$$

where τ is the time-constant of the sampling circuit. For a sampling rate $f_s = 10MHz$, MOS $W/L = 100\mu/0.8\mu$,a sampling capacitance $C_s = 0.2pF$, and

assuming parameters given in Table 2.1.1, the output noise spectral density of the simple sampling mixer degrades from its value at the input N_i by a factor of 5003 or 37 dB due to aliasing effects. It may be observed that the output noise spectral density due to wide-band noise at the IF input in a simple sampling mixer:

- degrades in direct proportion to the bandwidth of the circuit and therefore in inverse proportion to the sampling capacitance.
- degrades with decreasing sampling frequency or with subsampling

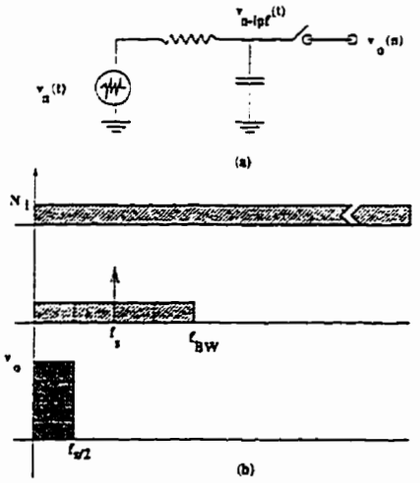


Figure 2.3: Model for wide-band noise from IF input

The above discussion shows that there is a tradeoff between signal-to-distortion and signal-to-noise ratio in the choice of the sampling capacitance. Increasing the sampling capacitance reduces the signal-to-distortion ratio arising from the MOS drain current non-linearity as seen from equation (2.4) whereas signal-to-noise ratio due to a MOS switch thermal noise, as well as wide-band IF input noise increases. The output noise spectral density due to all the noise sources considered increases(and therefore SNR decreases) directly with a decrease in sampling rate. This sets a lower limit to the subsampling rate. The problem of aliased wide-band thermal noise and jitter in the sampling clock are serious. However, a rigorous

mathematical treatment of noise is difficult since it involves the theory of stochastic differential equations and has been addressed elsewhere [10] . A more immediate problem is the analysis of distortion in a sampling mixer which will be discussed in chapter 3.

Chapter 3

Distortion Analysis in MOS Sampling Mixers using Volterra Series

In the previous chapters, distortion in MOS circuits has been analyzed using a power series. If the circuit has frequency dependent elements power series fails to correctly predict distortion. Although in a few cases (such as HD_2 and HD_3 in the sampling mixer) a simple substitution into formula derived using a power series may give correct results, but in general (as for IM_2,IM_3) this method may fail. The generalization of a power series to include frequency dependent circuit elements (capacitors and inductors) is known as a Volterra series. The application of Volterra series to a non-linear circuit assumes that the circuit is time-invariant i.e. it is operating as an 'amplifier' in which the output frequencies are harmonically related to the frequency of the sinusoid applied at the input. In contrast, a sampling mixer is a time-varying circuit in which the conductance of the NMOS switch is modulated by the applied gate voltage waveform. Therefore the output consists of sinusoids at the sum and difference of the sampling clock

frequency and the IF input frequency and their multiples. Nevertheless, essential distortion behaviour of the sampling mixer may be obtained by a time-invariant distortion analysis of the circuit using a Volterra series. Furthermore, in these applications Volterra series can be generalized to include time-varying behaviour under a set of conditions that are easily met by the sampling mixer. This chapter will introduce Volterra series and apply it directly to the sampling mixer by first assuming some ideal sampling conditions. It will then incorporate effects of finite fall-time of the applied gate signal by generalizing Volterra series to include time-varying circuits. This part has essentially been a contribution of Wei Yu([11], [12]) but has been included here for completeness. The overall goal is to arrive at formulae useful in the design of actual sampling mixer circuits.

3.1 Analysis of Harmonic Distortion Using Volterra series

Harmonic and intermodulation distortion can be analyzed using the theory of Volterra series [13]. The theory says that a time-invariant system that is mildly non-linear [1] may be expanded into a linear term, plus a second order term, plus a third order term, etc. Mathematically, if the input is $x(t)$, the output $y(t)$ is represented by a series of the type ,

$$\begin{aligned} y(t) &= \int_{-\infty}^{\infty} h_1(t-\tau_1)x(\tau_1)d\tau_1 \\ &\quad + \int\int_{-\infty}^{+\infty} h_2(t-\tau_1, t-\tau_2)x(\tau_1)x(\tau_2)d\tau_1 d\tau_2 \\ &\quad + \int\int\int_{-\infty}^{+\infty} h_3(t-\tau_1, t-\tau_2, t-\tau_3)x(\tau_1)x(\tau_2)x(\tau_3)d\tau_1 d\tau_2 d\tau_3 \\ &\quad + \cdots, \end{aligned} \tag{3.1}$$

[1] A mildly non-linear system can be roughly described as a system in which the amplitudes of the linear components are much larger than the distortion(non-linear) components.

where $h_n(\tau_1, \tau_2 \cdots \tau_n)$ is the $n'th$ order Volterra kernel. More succinctly, $y(t)$ can be written as

$$y(t) = \mathbf{H_1}[x(t)] + \mathbf{H_2}[x(t)] + \mathbf{H_3}[x(t)] + \cdots, \tag{3.2}$$

where $\mathbf{H_n}$ represents the $n'th$ order operator with kernel h_n. This series is called the Volterra series. Volterra kernels form a basis for sufficiently well behaved systems. Therefore, a mildly non-linear system can be expanded in Volterra series in one and only one way.

3.1.1 Frequency Response: Volterra Series Kernel Transform

The Volterra kernels defined above also have their corresponding n-dimensional transforms defined as follows:

$$H_n(\omega_1, \omega_2, \cdots \omega_n) = \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} \ldots h(\tau_1, \cdots, \tau_n) e^{-j(\omega_1\tau_1 + \omega_2\tau_2 + \ldots \omega_n\tau_n)} d\tau_1 \cdots d\tau_n \tag{3.3}$$

Expanding a system in a Volterra series enables the determination of its sinusoidal frequency response. Therefore the Volterra series is directly related to harmonic distortion [14]. For example, the response to a sinusoidal input for a second order system contains terms that is twice the input frequency plus a DC term. More specifically, for an input of $A \cdot cos(\omega_0 t)$, the output is,

$$\begin{aligned} y(t) &= \left(\frac{A}{2}\right)^2 H_2(j\omega_0, j\omega_0) e^{2j\omega_0 t} + \left(\frac{A}{2}\right)^2 H_2(-j\omega_0, -j\omega_0) e^{-2j\omega_0 t} \\ &\quad + \left(\frac{A}{2}\right)^2 H_2(j\omega_0, -j\omega_0) + \left(\frac{A}{2}\right)^2 H_2(-j\omega_0, j\omega_0). \end{aligned}$$

Since the first two (and the last two) terms are conjugates of each other, $y(t)$ may be re-written as

$$y(t) = 2\left(\frac{A}{2}\right)^2 Re\{H_2(j\omega_0, j\omega_0) e^{2j\omega_0 t}\} + 2\left(\frac{A}{2}\right)^2 Re\{H_2(j\omega_0, -j\omega_0)\}$$

Thus, the response of a second order system to a sinusoid of frequency ω_0 is also a sinusoid of frequency $2\omega_0$ and with amplitude $\frac{A^2}{2}|H_2(j\omega_0, j\omega_0)|$ and phase

$arctan(H_2(j\omega_0, j\omega_0))$. The determination of the Volterra series kernel transforms $H_n(\omega_1 \cdots \omega_n)$, can be done by inspection of the (non-linear) governing differential equation. This is done by first writing the output in its Volterra series expansion:

$$v_o = v_{o1} + v_{o2} + v_{o3} + \cdots \tag{3.4}$$

$$\tag{3.5}$$

The differential equation is re-written with v_o expanded as above. Since the Volterra expansion is unique, terms of the same order can be separated. For example, the second order equation will contain terms such as $v_{in}^2, v_{in}v_{o1}, v_{o1}^2 \cdots$. Since, $n'th$ order equation can consist only of terms involving $v_{o(n-1)}$ or lower order, the first order kernel transform H_1, which is the same as the linearized transfer function, can be determined first and higher order transforms H_n determined successively. The end result is that using the Volterra series expansion output voltage or current of a node may be written as a Volterra series expansion of the applied input voltage or current consisting of a sum of sinusoids as follows:

$$v_o(t) = H_1(\omega_1)v_{in}(\omega_1) + H_2(\omega_1, \omega_2)v_{in}^2 + H_3(\omega_1, \omega_2, \omega_3)v_{in}^3 \cdots \tag{3.6}$$

After determining the kernel transforms H_n, the following formulae are obtained:

$$HD_2 = \frac{A}{2} \cdot \frac{|H_2(\omega, \omega)|}{|H_1(\omega)|} \tag{3.7}$$

$$HD_3 = \frac{A^2}{4} \cdot \frac{|H_3(\omega, \omega, \omega)|}{|H_1(\omega)|}. \tag{3.8}$$

Intermodulation can be quantified in a similar way:

$$IM_2 = A \cdot \frac{|H_2(\omega, -\omega)|}{|H_1(\omega)|} \tag{3.9}$$

$$IM_3 = \frac{3A^2}{4} \cdot \frac{|H_3(\omega, \omega, -\omega)|}{|H_1(\omega)|}. \tag{3.10}$$

Therefore, obtaining the Volterra series coefficients is the key to calculating the harmonic and intermodulation distortion.

3.1.2 Application of Volterra Series to a MOS Gilbert Mixer

A MOS Gilbert mixer is a popular candidate for the implementation of RF mixers[[15]]. In chapter 1, the distortion in the MOS Gilbert mixer shown in Fig. 1.7 was derived using a power series method assuming low RF and LO frequencies. The main source of distortion in this mixer comes from the non-linearity in the transconductance amplifier formed by M1-M2 due to the square-law relationship between the drain current and gate-source voltage. Thus the differential drain current of the source-coupled pair M1-M2 is a non-linear function of the input voltage. The harmonic distortion in the differential current at $2\omega_{RF}, 3\omega_{RF}\ldots$ will be mixed down by multiplication with the harmonics in the LO input by the 2 source-coupled pairs M3-M4,M5-M6 to generate mixed-down components at $2\omega_{IF}(=2(\omega_{RF}-\omega_{LO}))$, $3\omega_{IF}\ldots$, where ω_{IF} is the desired IF frequency.

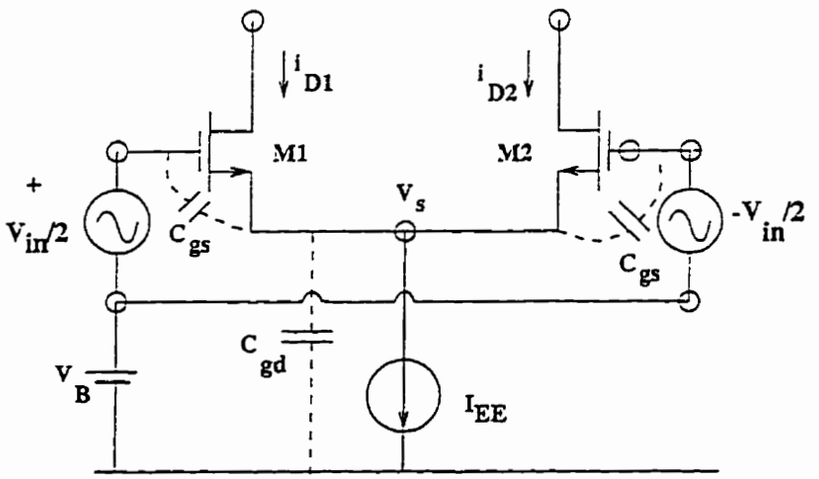


Figure 3.1: Source-coupled pair

In order to analyze the distortion due to the source-coupled pair M1-M2, the latter is redrawn in Fig. 3.1. It is desired to find out the drain current in M1, i_{D1}, as a Volterra series expansion of the applied input v_{in} i.e.

$$i_{d1} = G_1 v_{in} + G_2 v_{in}^2 + G_3 v_{in}^3 \cdots$$

In order to determine the G_n's, the Volterra series expansion of the common-source node v_s should be derived:

$$v_s = H_1 v_{in} + H_2 v_{in}^2 + H_3 v_{in}^3 \cdots$$

This is done by writing the KCL at the common-emitter node:

$$(2C_{gs} + C_d)\frac{dv_s}{dt} + I_{EE} - \frac{K'}{2}\left((v_{G_1S} - V_t)^2 + (v_{G_2S} - V_t)^2\right) = 0$$

Here, the v_{G_1S} and v_{G_2S} are the total gate-source voltages(including the sum of DC and small-signal components) and v_s is the small-signal voltage of the common source node.

Upon removing the DC terms and using the substitution $v_{G_1S} - v_{G_2S} = v_{in}$, the above equation may be re-written as follows:

$$(2C_{gs} + C_d)\frac{dv_s}{dt} - \frac{K'}{2}\left(\frac{v_{in}^2}{2} + 2v_s^2 - 4v_s(V_{GS} - V_t)\right) = 0 \qquad (3.11)$$

Expressing v_s in its Volterra series expansion,

$$v_s(t) = v_{s1}(t) + v_{s2}(t) + v_{s3}(t) \cdots$$

the differential equation (3.11) may be separated into equations involving first, second and third order terms,

$$(2C_{gs} + C_d)\frac{dv_{s1}}{dt} - \frac{K'}{2}(-4v_{s1}(V_{GS} - V_t)) = 0 \qquad (3.12)$$

$$(2C_{gs} + C_d)\frac{dv_{s2}}{dt} - \frac{K'}{2}\left(\frac{v_{in}^2}{2} + 2v_{s1}^2\right) = 0 \qquad (3.13)$$

$$(2C_{gs} + C_d)\frac{dv_{s3}}{dt} - \frac{K'}{2}(4v_{s1}v_{s2} - 4v_{s3}(V_{GS} - V_t)) = 0 \qquad (3.14)$$

These equations lead to Volterra kernel transform(frequency domain) expressions,

$$v_{sn} \rightarrow H_n(\omega_1, \omega_2, \cdots \omega_n) v_{in}^n$$

$$\frac{dv_{sn}}{dt} \rightarrow j(\omega_1 + \omega_2 + \cdots + \omega_n) H_n(\omega_1, \omega_2, \cdots \omega_n) v_{in}^n$$

Equations (3.12 - 3.14) can be transformed so that they are a function of the Volterra kernel transforms H_n and solved successively for $n = 1, 2, 3$. However, when doing multiplications, care has to be taken to write the frequency domain expressions symmetrically with respect to $\omega_1 + \omega_2 + \cdots$. This is known as *symmetrization* of the kernel [14]. For example, the determination of $H_3(\omega_1, \omega_2, \omega_3)$ would involve a term $H_1(\omega_1)H_2(\omega_2, \omega_3)$. This term has to be re-written so as to make it symmetric with respect to $\omega_1, \omega_2, \omega_3$ so that the Volterra kernel transform H_3 itself is symmetrical with respect to $\omega_1, \omega_2, \omega_3$.

$$\overline{H_1(\omega_1)H_2(\omega_2, \omega_3)} = \frac{1}{3}\left(H_1(\omega_1)H_2(\omega_2, \omega_3) + H_1(\omega_2)H_2(\omega_1, \omega_3) + H_1(\omega_3)H_2(\omega_1, \omega_2)\right)$$

Following, these procedures, the Volterra kernel transforms may be obtained,

$$H_1(\omega_1) = 0 \tag{3.15}$$

$$H_2(\omega_1, \omega_2) = \frac{K'}{4\left(j(\omega_1 + \omega_2)(C_d + 2C_{gs}) + 2K'(V_{GS} - V_t)\right)} \tag{3.16}$$

$$H_3(\omega_1, \omega_2, \omega_3) = 0 \tag{3.17}$$

$$\tag{3.18}$$

The Volterra series coefficients for drain current ,G_n, may be easily obtained from the coefficients H_n for relatively low frequencies $\left(\omega_1, \omega_2, \omega_3 \ll \frac{K'(V_{GS} - V_t)}{C_d + 2C_{gs}}\right)$,

$$G_1(\omega_1) = \frac{1}{2}\sqrt{K' I_{EE}} \tag{3.19}$$

$$G_2(\omega_1,\omega_2) = 0 \tag{3.20}$$

$$G_3(\omega_1,\omega_2,\omega_3) = -\frac{K^{'}}{16(V_{GS}-V_t)}\left(1-\frac{j(\omega_1+\omega_2+\omega_3)(C_d+2C_{gs})}{3K^{'}(V_{GS}-V_t)}\right) \tag{3.21}$$

Note that the gain G_1 is half of the transconductance of the each transistor M1/M2($\sqrt{K^{'}I_{EE}}$) as expected from small signal linear analysis.

The harmonic and intermodulation distortion are obtained as,

$$HD_3 = \frac{A^2}{4}\frac{|G_3(\omega_1,\omega_1,\omega_1)|}{|G_1(\omega_1)|} \tag{3.22}$$

$$= \frac{A^2}{32(V_{GS}-V_t)^2}\sqrt{1+\left(\frac{\omega_1(C_d+2C_{gs})}{K^{'}(V_{GS}-V_t)^2}\right)^2} \tag{3.23}$$

$$IM_3 = \frac{3A^2}{4}\frac{|G_3(\omega_1,\omega_1,-\omega_2)|}{|G_1(\omega_1)|} \tag{3.24}$$

$$\approx \frac{3A^2}{32(V_{GS}-V_t)^2}\sqrt{1+\left(\frac{\omega_1(C_d+2C_{gs})}{3K^{'}(V_{GS}-V_t)^2}\right)^2} \tag{3.25}$$

$$\tag{3.26}$$

3.2 Mixing using "Ideal" Sampling: Time-Invariant Distortion

The top-plate sampling mixer is shown in Fig. 3.2. To visualize the mixing behavior of the circuit, it may be modeled as a time-invariant non-linear system(operating as an 'amplifier') followed by an ideal sampling circuit as shown in Fig. 3.3. It is assumed that a constant voltage is applied at the gate and an RF signal, $V_{RF}(t)$ of sufficiently small amplitude is applied at the input so that the NMOS transistor is in the triode region. The frequency spectrum at the output of the amplifier formed by R_{M1}, C will have harmonic components at nf_{RF} where $n = 2, 3...$ as shown in Fig. 3.4-(b). The fundamental as well as the harmonic components of the amplifier can be analyzed using the time-invariant Volterra series theory.

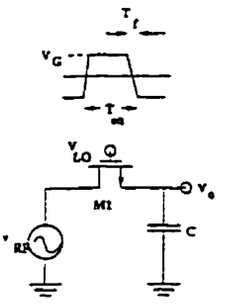


Figure 3.2: Top-plate MOS sampling mixer

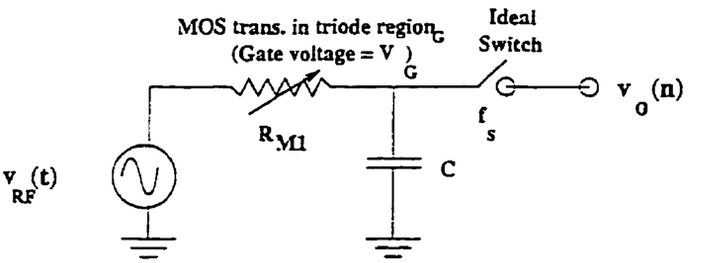


Figure 3.3: The time-invariant model for MOS sampling mixer

In order to mix the signal at f_{RF} down to near DC, it is sampled with a periodic impulse train shown in Fig. 3.4-c. This is followed by an ideal low-pass filter with a cutoff frequency at $f_s/2$ to extract the baseband component of the sampled output. The effect of this ideal sampling operation is to replicate the output spectrum by shifting it by nf_s where $n = 1, 2, ..$ so that a shifted component of output is mixed down to near DC. This is shown in Fig. 3.4-(d). The harmonic components at nf_{RF} will now reappear near DC at $nf_{RF} - nf_s$ and close to $f_{IF} = f_{RF} - f_s$ in the baseband. It may also be noted that it is possible to mix down the output to the same positions in the baseband by using a sampling clock with a frequency that is a sub-harmonic of f_s (subsampling).

The mixing operation just described may now be used to approximate the behaviour of a sampling mixer under some ideal conditions. The voltage applied at the gate is an ideal square-wave with 0 rise and fall-time that switches the MOS transistor on and off periodically. Charge-injection and non-quasi-static effects of

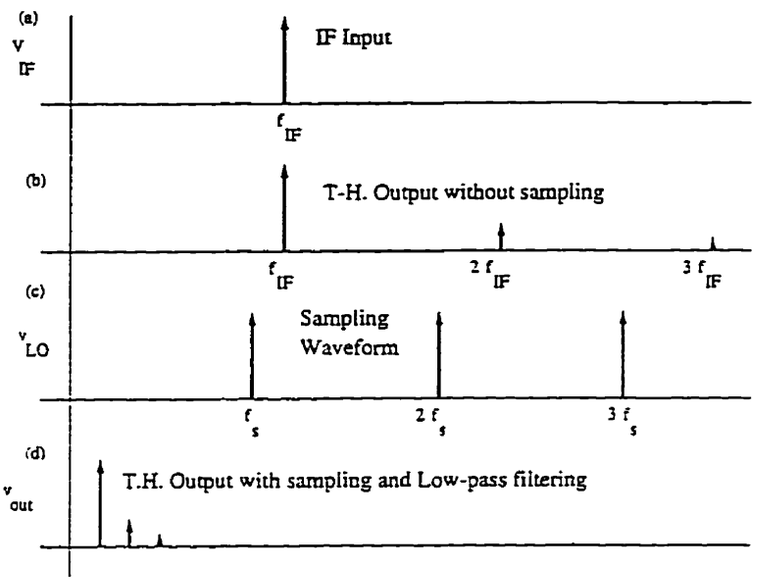


Figure 3.4: Mixing as ideal sampling

the MOS transistor are ignored. When the gate voltage is at V_G, the MOS transistor is in the triode region and the output transistor tracks the input voltage. When the MOS transistor turns off the tracked output voltage is held onto the capacitor. When the sampling mixer operates as a mixer in this manner it is said to be in the *time-invariant* mode. Assuming that the time constant of the circuit is much smaller than the gate on period, the output voltage reaches steady state within several time constants after the MOS transistor turns on. Under this condition, assuming that the input signal has a sufficiently narrow bandwidth to guarantee that the bandpass sampling criterion is met , the distortion components seen in the discrete-time frequency domain(Fig. 3.4-d) are the same as those for the case when the circuit is working in the 'amplifier' mode(Fig. 3.4-a) except for shifts by integer multiples of the sampling frequency. Therefore, to calculate distortion components when the sampling mixer behavior can be approximated by time-invariant it is only needed to analyze distortion in the 'amplifier' mode, which can be done using the time-invariant Volterra series theory.

Some distortion terminologies are introduced and illustrated. Suppose that a single pure sinusoidal input $sin(\omega t)$ is applied to a non-linear system, the harmonic distortion of nth order is defined to be the magnitude of the $sin(n\omega t)$ term at the output. If two tones are applied at the input, frequencies at the sum and difference of input frequencies are present at the output. Therefore, two different kinds of 2nd order intermodulation (IM_2) are possible. For an input of $sin(\omega_1 t) + sin(\omega_2 t)$, IM_2^+ is defined as the magnitude of the $sin((\omega_1 + \omega_2)t)$ term at the output, and IM_2^- that of the $sin((\omega_1 - \omega_2)t)$ term. Intermodulation of 3rd order (or IM_3) is defined as the magnitude of the $sin((2\omega_1 - \omega_2)t)$ term for an input of $sin(\omega_1 t) + sin(\omega_2 t)$. It is to be noted that the physical origin of HD_2 and IM_2^+ is the same, and HD_2 is related to IM_2^+ by a factor of 2. In the following analysis, unless explicitly specified IM_2 refers to IM_2^-.

For example, in the case that the RF input has 2 tones at frequency f_{RF1} (say at 100.3MHz) and f_{RF2} (say at 100.4MHz), respectively, with a sampling clock frequency f_s at 100MHz. The components visible in the baseband are shown in Fig. 3.5. The 100kHz component is the IM_2^- component at $f_{RF1} - f_{RF2}$. The 200kHz component is due to IM_3 at $2f_{RF2} - f_{RF2}$ (200.2MHz) mixed down to the baseband. The component at 700kHz is the IM_2^+ component at $f_{RF1} + f_{RF2}$ (200.7MHz) mixed down. HD_2 components at 600 and 800kHz, as well as HD_3 component at 900kHz, may also be observed. By using a differential architecture, even order distortion (e.g. HD_2, IM_2) may be made considerably smaller (by the mismatch factor) than in a single-ended architecture.

3.2.1 Time-Invariant Distortion in a Sampling Mixer

The harmonic distortion of a sampling mixer is now analyzed under time-invariant assumptions. The distortion in the output is determined by calculating its Volterra coefficients (Volterra kernel transforms). As discussed in chapter 2, distortion in a

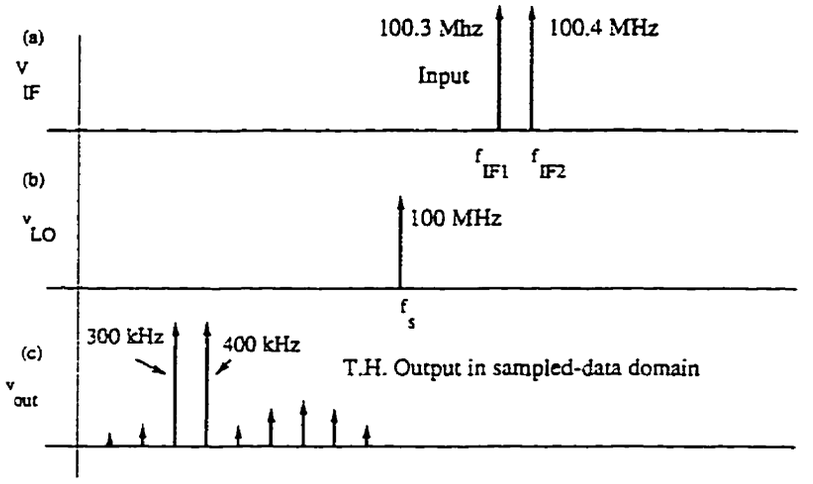


Figure 3.5: Mixing distortion using 2 tones

MOS sampling mixer circuit configuration when it is operating in the 'amplifier' mode is due to the non-linear drain current source voltage relationship, non-linear source/drain junction capacitances and modulation of the threshold voltage due to the body effect.

Distortion in a Sampling Mixer due to Drain Current Non-linearity

The basic MOS drain-current equation is given as:

$$I_d = K'((V_{GS} - V_t)V_{DS} - \tfrac{1}{2}V_{DS}^2)$$

where $K' = \mu C_{ox} W/L$, and V_t is the threshold voltage. Either the input or the output side may be regarded as the source. [2] Assuming that the output and input are considered to be the drain and source, respectively, the system differential equation becomes:

$$g v_o + C\frac{dv_o}{dt} = g v_{in} - \frac{K'}{2}(v_{in}^2 - v_o^2), \tag{3.27}$$

[2] It may be shown that the difference between the estimates of distortion is negligibly small in the two cases

where $g = K'((V_{GS} - V_t))$. Expressing $v_o(t)$ in its Volterra series expansion,

$$v_o(t) = v_1(t) + v_2(t) + v_3(t) + ...,$$

where $v_n(t) = \mathbf{H_n}[v_{in}(t)]$, the expansion is substituted into (3.27). Keeping only first three orders, the following equation is obtained:

$$g(v_1 + v_2 + v_3) + C\frac{v_1 + v_2 + v_3}{dt} = gv_{in} - \frac{K'}{2}(v_{in}^2 - v_1^2 - 2v_1v_2).$$

Note, v_{in} is first order since the input is a pure sinusoidal; the term v_1^2 is second order; and v_1v_2 is third order. Equating the coefficients:

$$\begin{cases} gv_1 + C\frac{dv_1}{dt} &= gv_{in} \\ gv_2 + C\frac{dv_2}{dt} &= \frac{K'}{2}(v_1^2 - v_{in}^2) \\ gv_3 + C\frac{dv_3}{dt} &= -K'v_1v_2 \end{cases} \tag{3.28}$$

The solutions to this set of differential equations are the Volterra coefficients H_1, H_2 and H_3. Since a constant gate voltage hence a constant g is assumed, it can be shown that:

$$H_1(\omega_1) = \frac{g}{g + j\omega_1 C} \tag{3.29}$$

$$= 1 \tag{3.30}$$

$$H_2(\omega_1, \omega_2) = \frac{\frac{K'}{2}(H_1(\omega_1)H_1(\omega_2) - 1)}{g + j(\omega_1 + \omega_2)C} \tag{3.31}$$

$$= -\frac{j(\omega_1 + \omega_2)C}{2K'(V_{GS} - V_t)^2} \tag{3.32}$$

$$H_3(\omega_1, \omega_2, \omega_3) = \frac{-K' \cdot H_1(\omega_1) \cdot H_2(\omega_2, \omega_3)}{g + j(\omega_1 + \omega_2 + \omega_3)C} \tag{3.33}$$

$$= \frac{j(\omega_1 + \omega_2 + \omega_3)C}{3K'(V_{GS} - V_t)^3} \tag{3.34}$$

where the assumption of a small time-constant ($g \gg j\omega C$) is used, and expressions are symmetrized. Substituting (3.30)-(3.34) into (3.7)-(3.10) yields the harmonic distortion and intermodulation. In particular,

$$HD_2 = \frac{A}{2} \cdot \frac{\omega C}{K'(V_{GS} - V_t)^2} \tag{3.35}$$

$$HD_3 = \frac{A^2}{4} \cdot \frac{\omega C}{K^{'}(V_{GS} - V_t)^3} \tag{3.36}$$

$$IM_2 = 0 \tag{3.37}$$

$$IM_3 = \frac{A^2}{4} \cdot \frac{\omega C}{K^{'}(V_{GS} - V_t)^3}. \tag{3.38}$$

Distortion in a Sampling Mixer due to Junction-capacitance Non-linearity

The load capacitance of the sampling mixer which includes the non-linear junction capacitances can be written as,

$$C = C_0 + C_1 v + c_2 v^2 \cdots \tag{3.39}$$

where C_0 includes the junction capacitances.

The system differential equation may now be written as:

$$g v_o + C_0 \frac{dv_o}{dt} + C_1 v_o \frac{dv_o}{dt} + C_2 v_o^2 \frac{dv_o}{dt} + \cdots = g v_{in} \tag{3.40}$$

where $g = K^{'}((V_{GS} - V_t))$. Expressing $v_o(t)$ in its Volterra series as before,

$$v_o(t) = v_1(t) + v_2(t) + v_3(t) + ...,$$

where $v_n(t) = \mathbf{H_n}[v_{in}(t)]$, substituting the expansion into equation (3.40) and simplifying for low frequencies,

$$H_2(\omega_1, \omega_2) = \frac{j(\omega_1 + \omega_2 + \omega_3)C_1}{2K^{'}(V_{GS} - V_t)} \tag{3.41}$$

$$H_3(\omega_1, \omega_2, \omega_3) = \frac{j(\omega_1 + \omega_2 + \omega_3)C_2}{3K^{'}(V_{GS} - V_t)} \tag{3.42}$$

$$\tag{3.43}$$

Taking the ratio of distortion due to junction capacitance non-linearity to that due to MOS drain current non-linearity leads to the the following,

$$\frac{H_{2-cap}}{H_{2-MOS}} = \frac{1}{2}(V_{GS} - V_t)\frac{C_1}{C_0} \tag{3.44}$$

$$\frac{H_{3-cap}}{H_{3-MOS}} = \frac{1}{3}(V_{GS} - V_t)^2\frac{C_2}{C_0} \tag{3.45}$$

$$\tag{3.46}$$

The non-linear capacitance coefficients in equation (3.39) may be obtained by power series expansion of the following equation for area junction capacitance,

$$C_j = \frac{C_{j0}}{\left(1 + \frac{v_s + V_B}{\phi}\right)^{PHA}} \tag{3.47}$$

where C_{j0} is the zero-bias junction capacitance,V_B is the substrate-source bias, PHA is the junction exponent parameter and ϕ is the built-in potential of the junction diodes as given in spice (level 3) diode models. Upon substitution of parameters given in Table 2.1.1 of chapter 2, with $\phi = 0.9236V$, with a source-substrate bias $V_B = 2.5V$, $C_0 = 0.352pF$, $\frac{C_1}{C_0} = 0.033, \frac{C_2}{C_0} = 0.007$, the following results are obtained:

$$\frac{H_{2-cap}}{H_{2-MOS}} = 0.013, \quad \frac{H_{3-cap}}{H_{3-MOS}} = 0.0015.$$

These show that distortion due to capacitive non-linearity may be neglected in our analysis.

Distortion in a Sampling Mixer due to the Body Effect

Distortion due to body effect may be calculated by expressing the threshold voltage as a non-linear function of the the source-substrate voltage in the MOS drain current equation. This equation may now be written as,

$$i_D = K'\left[V_{GS} - V_{t0} - \gamma\left((2\phi_f - V_B)^{\frac{1}{2}} - (2\phi_f)^{\frac{1}{2}}\right)\right]V_{DS} - \frac{K'}{2}V_{DS}^2$$

The small-signal drain current i_d may now be expressed as a power series expansion of the source and drain voltages, v_s, v_d,

$$i_d = g^{'}(v_d - v_s) - c_1 v_d v_s + c_1 v_s^2 + c_2 v_d v_s^2 - c_2 v_s^3$$

where

$$g^{'} = K^{'}(v_{GS} - V_{t0}^{'}) \tag{3.48}$$

$$V_{t0}^{'} = V_{t0} + \gamma\left(\sqrt{(2\phi_f - V_B)} - \sqrt{2\phi_f}\right) \tag{3.49}$$

$$c_1 = K^{'}(1 + \theta_1) \tag{3.50}$$

$$c_2 = \frac{K^{'}\gamma}{8(2\phi_f - V_B)^{\frac{3}{2}}} \tag{3.51}$$

$$\theta_1 = \frac{\gamma}{2\sqrt{(2\phi_f - V_B)}} \tag{3.52}$$

Upon re-writing the differential equation and deriving the Volterra coefficients in a manner similar to previous cases, the expressions for harmonic and intermodulation distortion, when the body effect is included, may be derived as [6],

$$HD_2 = HD_{2-0}(1 + \theta_1) \tag{3.53}$$

$$HD_3 = HD_{3-0}(1 + \theta_1)^2 \tag{3.54}$$

$$IM_3 = IM_{3-0}(1 + \theta_1)^2 \tag{3.55}$$

where $HD_{2-0}, HD_{3-0}, IM_{3-0}$ are the expressions for distortion without body effect as derived in equations 3.35 - 3.38. Therefore, the effect of body bias on distortion is to add a body bias dependent factor to the distortion. For the typical process parameters given in Table 2.1.1 and for $VB = -2.5V$, this factor is 1.25 dB for HD_2 and 2.5 dB for HD_3 and IM_3.

3.3 Mixing with Finite Fall-time LO Waveform in a Sampling Mixer

Distortion analysis for the case of time-invariant analyzed in the previous section assumes that a perfect square wave sampling clock(LO) with 0 fall-time has been applied at the gate so that the sampling mixer alternates between a tracking phase when the clock is 'HIGH' and a cutoff phase when the output voltage is held constant when the clock goes 'LOW'. However, if the sampling-clock voltage deviates from the ideal square wave, two effects start to emerge which will invalidate the time-invariant distortion expressions derived using the Volterra series method. If the gate voltage fall-time is finite, the approximate time-constant of the circuit as given by:

$$\tau = \frac{C}{g} = \frac{C}{K^{'}(V_{GS} - V_t)},$$

gradually increases since the MOS transistor on resistance increases as the MOS leaves the triode region. In the extreme case, for a very slow rate of fall of the gate voltage, distortion may tend to infinity at the instant of cutoff as predicted by time-invariant formulae (3.35 - 3.38) when $(V_{GS} - V_t) = 0$. This mechanism of distortion will be referred to as *time-varying* distortion. In addition, the precise instant of sampling depends not only on the gate fall slew-rate waveform but also on the input amplitude and frequency resulting in *non-uniform-sampling* distortion.

3.3.1 Distortion due to Non-uniform Sampling

In the analysis of the distortion in a sampling mixer using the model in Fig. 3.3 the output voltage is assumed to be sampled at equally spaced instants. This assumption is not exactly true if the gate voltage has non-zero fall-time. The instance of true sampling is when $(V_{GS} - V_t) = 0$, so the time at which sampling

occurs depends both on gate voltage but also on the input voltage. This introduces distortion. A simple explanation of the origin of the distortion due to non-uniform-sampling is shown in Fig. 3.6. Assume that a sinusoid of amplitude A is intended to be sampled at time t_0. If the fall-time of the gate voltage is 0, then the voltage sampled at t_0 depends only on the amplitude of the signal at that instant. For example, the sampled value of a signal of amplitude $A/2$ is exactly the same. However, if the gate voltage falls off with a finite slope and if it samples the sinusoid of amplitude A exactly at t_0 with a value A, the value sampled for the sinusoid of amplitude $A/2$ is no longer the same but is smaller by an error ϵ depending upon the slope of the input sinusoid at $t = t_0$ and the slope of the gate voltage.

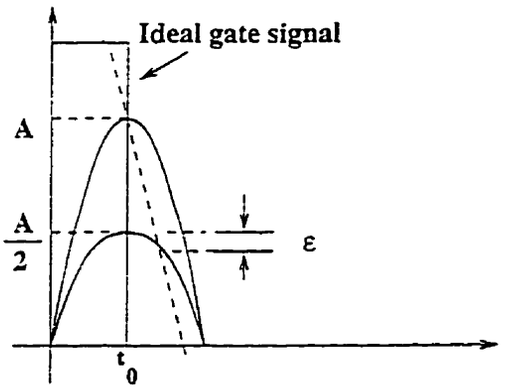


Figure 3.6: Distortion due to sampling error

A formal method of analyzing distortion due to sampling error is to expand the input signal $f(t)$, assumed to be smooth, around an intended sampling instant at time 0, using power series and determining t, the cutoff instant, as a function of $f(t)$ and the slope of the falling edge. Assume that the gate voltage has a falling edge of finite-slope α, where $\alpha = 2V_G/T_f$ as shown in Fig. 3.7.

The falling edge has the form $e(t) = V_G - \alpha t$. Since the MOS transistor enters cut-off at $V_{gate} - V_{source} = V_t$, and the input is applied at the source side, sampling occurs at the instant when $e(t) - V_t = f(t)$. Using the approximation

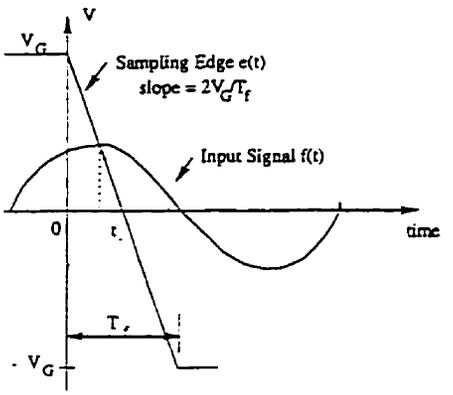


Figure 3.7: Derivation of cutoff instant t

$f(t) \approx f(0) + f'(0)t$, and solving for the cut-off time,

$$t = \frac{V_G - V_t - f(0)}{\alpha + f'(0)} \approx \frac{V_G - V_t - f(0)}{\alpha}\left(1 - \frac{f'(0)}{\alpha} + \frac{f'(0)^2}{\alpha^2}\right), \tag{3.56}$$

where it is assumed that α is large. Substituting the above expression for t into the Taylor expansion for $f(t)$ around 0, and collect the first three order terms,

$$f(t) = f(0) - \frac{f'(0)f(0)}{\alpha} + \left(\frac{f''(0)f^2(0)}{2\alpha^2} + \frac{f'(0)^2 f(0)}{\alpha^2}\right), \tag{3.57}$$

where again large α is assumed. Therefore, because of the finite fall-time, the sampled value $f(t)$ differs from the desired value $f(0)$ by additional signal dependent terms, which produces distortion. Since the sampling time is arbitrary, equation (3.57) is valid if time 0 is replaced by an arbitrary sampling time.

The signal dependence can be analyzed by Volterra series. The linear term in equation (3.57) is $f(0)$, so $H_1 = 1$. The second order term is the product of the derivative with the function itself. Using the composition from linear terms and using symmetrization, the Volterra series coefficients are found to be:

$$H_2(\omega_1, \omega_2) = -\frac{j(\omega_1 + \omega_2)}{2\alpha}, \tag{3.58}$$

$$H_3(\omega_1, \omega_2, \omega_3) = -\frac{(\omega_1 + \omega_2 + \omega_3)^2}{6\alpha^2}. \tag{3.59}$$

Using these results in (3.7)-(3.10), harmonic and intermodulation distortion can be calculated exactly:

$$HD_2 = \frac{A}{4}\left(\frac{j\omega T_f}{V_G}\right) \tag{3.60}$$

$$HD_3 = \frac{3A^2}{32}\left(\frac{\omega T_f}{V_G}\right)^2 \tag{3.61}$$

$$IM_2 = 0 \tag{3.62}$$

$$IM_3 = \frac{A^2}{32}\left(\frac{\omega T_f}{V_G}\right)^2 \tag{3.63}$$

Comparing the non-uniform-sampling distortion as given by equation (3.63) with the time-invariant distortion as given by equation (3.38),

$$\frac{IM3_{n.u.s}}{IM3_{i.s.}} = \frac{1}{4}\left(\frac{T_F^2}{\tau T}\right)\frac{(V_{GS}-V_t)^2}{V_G^2} \tag{3.64}$$

The above equation shows that the non-uniform-sampling distortion becomes comparable to the time-invariant distortion when the fall-time is in the order of $\sqrt{\tau T}$, where τ is the RC time constant formed by the MOS resistor and the load capacitor, and T is the period of the input signal. Therefore, the sampling error is a bigger problem at high frequency. Thus, an important requirement in the design of a high IF digitizer is the design of an LO buffer that can meet the fall-time requirements imposed by non-uniform-sampling distortion.

3.3.2 Time-Varying Distortion in a Sampling Mixer

As mentioned in the previous section, it is necessary to generalize the Volterra series to time-varying systems in order to analyze a sampling mixer with an arbitrary LO waveform. In this section, a time-varying Volterra series is developed, and its frequency response explored. This section of the thesis has been contributed by Wei Yu.

Time-Varying Systems

The notion of impulse response can be easily generalized to linear time-varying systems by the addition of another time variable [16]. The impulse response of a linear time-varying system , $h_1(t,\tau)$, consists of two variables, and is defined as the response of the system for an input of $\delta(t-\tau)$. In this case, the system response for an arbitrary input becomes:

$$y_1(t) = \int_{-\infty}^{\infty} h_1(t,\tau)x(\tau)d\tau. \tag{3.65}$$

The time variable t is called the observation time and τ the launch time because $h_1(t,\tau)$ represents the output observed at time t for an impulse input launched at time τ. Under general continuity conditions, a linear time-varying system can be completely characterized by its two dimensional impulse response. The extension of the Volterra series to time-varying systems has been originally developed by Wei Yu ([12], [11]). This work shows how to construct higher order time-varying kernels from lower order kernels in both the time and frequency domains.

Higher order kernels are generalized in a way similar to first order kernels. For example, a second order kernel has two launch time variables plus an observation time variable. $h_2(t,\tau_1,\tau_2)$ is the system response to two impulses launched at time instants τ_1 and τ_2. In general, a mildly non-linear time-varying system has the following Volterra series expansion:

$$\begin{aligned} y(t) &= \int_{-\infty}^{\infty} h_1(t,\tau_1)x(\tau_1)d\tau_1 \\ &\quad + \int\int_{-\infty}^{\infty} h_2(t,\tau_1,\tau_2)x(\tau_1)x(\tau_2)d\tau_1 d\tau_2 \\ &\quad + \int\int\int_{-\infty}^{\infty} h_3(t,\tau_1,\tau_2,\tau_3)x(\tau_1)x(\tau_2)x(\tau_3)d\tau_1 d\tau_2 d\tau_3 + \cdots, \end{aligned} \tag{3.66}$$

In the linear time-invariant case, the impulse response may be found in either the time domain or the frequency domain. In fact, the frequency domain solution is often much easier to obtain than the time domain impulse response.

However, for time-varying systems, the frequency response is no longer well defined, and hence, it is necessary to directly apply impulses at the system input and find the output expression in the time domain. This amounts to solving the differential equation directly, which is not trivial in general. But, for first order differential equations, such as the sampling mixer equation, this method is feasible.

Suppose that in the mixer equation (3.28), g varies with time. In particular, g goes to 0 when the transistor turns off. The zero state response of the first order equation

$$gv_1 + C\frac{dv_1}{dt} = gv_{in},$$

is obtained using the integrating factor:

$$v_1(t) = \int_0^t e^{-\int_\mu^t \frac{g(\xi)}{C}d\xi} \frac{g(\mu)}{C} v_{in}(\mu)d\mu. \tag{3.67}$$

Setting $v_{in}(\mu) = \delta(\mu - \tau)$ gives the impulse response of the first order system:

$$h_1(t,\tau) = \begin{cases} e^{-\int_\tau^t \frac{g(\xi)}{C}d\xi} \frac{g(\tau)}{C} & if \quad t \geq \tau \\ 0 & if \quad t < \tau. \end{cases} \tag{3.68}$$

Next, the second order kernel is calculated. In general, a second order system can be thought of as the composition of linear systems as shown in Fig. 3.8. In

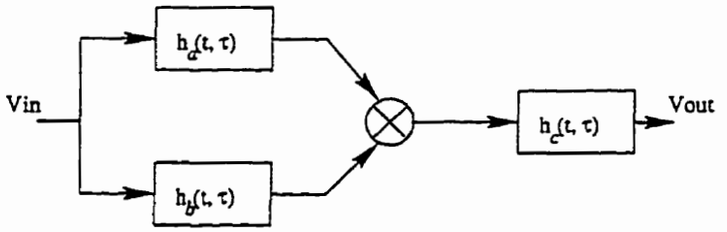


Figure 3.8: Composition of second order system from first order systems

particular, if the impulse responses of the linear systems are $h_a(t,\tau)$, $h_b(t,\tau)$, and $h_c(t,\tau)$ respectively, the second order kernel can be computed as follows:

$$h_2(t,\tau_1,\tau_2) = \int_{-\infty}^{\infty} h_c(t,\tau)h_a(\tau,\tau_1)h_b(\tau,\tau_2)d\tau. \tag{3.69}$$

The expression for third order systems is similar. If in Fig. 3.8 h_a is second order, and therefore the overall system is third order, then the overall system kernel is:

$$h_3(t,\tau_1,\tau_2,\tau_3) = \int_{-\infty}^{\infty} h_c(t,\tau)h_a(\tau,\tau_1,\tau_2)h_b(\tau,\tau_3)d\tau. \tag{3.70}$$

Therefore, as was done with the time-invariant case, h_2 and h_3 can be solved consecutively. For example, the second order kernel is found by substituting $v_1(\tau)$ from (3.67) and setting the input as an impulse in the solution to the second order equation in (3.28):

$$v_2(t) = \int_0^t e^{-\int_\tau^t \frac{g(\xi)}{C}d\xi} \frac{g(\tau)}{C} \left(\frac{K'}{2}\right) (v_1^2(\tau) - v_{in}^2(\tau))d\tau. \tag{3.71}$$

Since the differential equations are linear and first order, there is no theoretical difficulty in obtaining the solution. Following this method, the complete time domain solution to the system can be obtained.

In a sampling mixer where the output points of interest are at the sampled points, it is needed to sample v_2 and apply Fourier analysis to the sampled points to obtain the second order distortion. This procedure, although straightforward in theory, is tedious even for a simple system such as the sampling mixer. However, as will be shown in the next section, by exploring the frequency domain interpretation and by taking advantage of the fact that output is in the sample data domain, the problem can be simplified significantly.

Time-varying Volterra series in Sampled Systems

Suppose that sampling occurs at time 0. Let $h_1(t,\tau)$ be the time-varying kernel of the system with a non-zero fall-time LO waveform. The linear term in the sampled output voltage is,

$$y(0) = \int_{-T}^{0} h_1(0,\tau)x(\tau)d\tau + ZIR, \tag{3.72}$$

where T is the sampling period, and ZIR is the zero input response due to the initial condition. Since it is assumed that the RC time constant for the sampling

mixer is much smaller than the sampling period, the ZIR is negligible. Also, because of the small time constant, the lower limit of integration may be replaced by $-\infty$:

$$y(0) = \int_{-\infty}^{0} h_1(0,\tau)x(\tau)d\tau. \tag{3.73}$$

Further, since the output voltage of interest is at the sampling instant, the time-varying characteristic of importance occurs during the time within a few time constants before the sampling instant. This means that the same Volterra kernel applies to every sampling instant except the kernels are shifted by nT, integer multiples of the sampling period. To simplify computation, the Volterra kernel is kept identical for each sampling period. Therefore, instead of shifting the kernel, the input signal is shifted backward in time by nT keeping the sampling instant at time 0. This effectively keeps the functional form of the kernel identical for all samples. Further, there is nothing special about sampling points nT. So, if sampling occurs at an arbitrary time t, the sampled voltage can be represented as,

$$y(t) = \int_{-\infty}^{0} h_1(0,\tau)x(\tau+t)d\tau. \tag{3.74}$$

This $y(t)$ is a fictitious signal, whose value at t represents the sampled value of the output if sampling is to occur at t. If sampling occurs at instants nT, the output voltage samples are just $y(T), y(2T), ..., y(nT)$. Hence the non-ideal sampling of the output signal is reduced to the ideal sampling of $y(t)$, where $y(t)$ is related to the input $x(t)$ by equation (3.74). This is convenient because harmonic distortion of the ideal sampled $y(nT)$ is same as the harmonic distortion of the continuous signal $y(t)$. So the problem of calculating distortion in a non-ideal sampled output is reduced to the problem of calculating the distortion in the continuous signal $y(t)$.

The transformation from equation (3.72) to (3.74) also reduces a time-varying system to a time-invariant system, as the relation between x and y in equation (3.74) is time-invariant. This situation is analogous to the analysis of discrete control systems where although a zero-order-hold is not a time-invariant

operation in the continuous time domain, the input-output relation is nevertheless time-invariant in the sampled data domain.

It remains to find the impulse response of the linear time-invariant system equation (3.74). Denote its impulse response in the time and frequency domain by $\hat{h}_1(t)$ and $\hat{H}_1(\omega)$, respectively. To find $\hat{h}_1$, set $x(t) = \delta(t)$ in equation (3.74), it follows that,

$$\hat{h}_1(t) = \begin{cases} h_1(0,-t) & if \quad t \geq 0 \\ 0 & if \quad t < 0. \end{cases} \tag{3.75}$$

The frequency response is its Fourier transform:

$$\hat{H}_1(\omega) = \int_{-\infty}^{0} h_1(0,\tau) e^{j\omega\tau} d\tau, \tag{3.76}$$

where again, $h_1(t,\tau)$ is the time-varying kernel.

The same technique applies to higher order systems. For a second order system, the sampled data domain response is:

$$y(t) = \int_{-\infty}^{0}\int_{-\infty}^{0} h_2(0,\tau_1,\tau_2) x(\tau_1 + t) x(\tau_2 + t) d\tau_1 d\tau_2, \tag{3.77}$$

and the frequency response is:

$$\hat{H}_2(\omega_1,\omega_2) = \int_{-\infty}^{0}\int_{-\infty}^{0} h_2(0,\tau_1,\tau_2) e^{j\omega_1\tau_1} e^{j\omega_2\tau_2} d\tau_1 d\tau_2. \tag{3.78}$$

Again, the second order kernel may be obtained from its composition from first order systems as in equation (3.69).

The frequency domain expression is of most interest. It is in fact possible to bypass the time domain expression and obtain the frequency domain result directly. Assuming a composition form as in Fig. 3.8, substituting equation (3.69) into (3.78), then:

$$\hat{H}_2(\omega_1,\omega_2) = \int_{-\infty}^{0}\int_{-\infty}^{0}\int_{-\infty}^{0} h_c(0,\tau_3) h_a(\tau_3,\tau_1) h_b(\tau_3,\tau_2) e^{j\omega_1\tau_1} e^{j\omega_2\tau_2} d\tau_3 d\tau_1 d\tau_2.$$

More succinctly and for convenience only, define,

$$\hat{H}_1(\omega,t) = \int_{-\infty}^{t} h_1(t,\tau) e^{j\omega\tau} d\tau, \tag{3.79}$$

and

$$\hat{H}_2(\omega_1, \omega_2, t) = \int_{-\infty}^{t} \int_{-\infty}^{t} h_2(t, \tau_1, \tau_2) e^{j\omega_1 \tau_1} e^{j\omega_2 \tau_2} d\tau_1 d\tau_2. \tag{3.80}$$

Then, the following formula is obtained:

$$\hat{H}_2(\omega_1, \omega_2, t) = \int_{-\infty}^{t} h_c(t, \tau) H_a(\omega_1, \tau) H_b(\omega_2, \tau) d\tau. \tag{3.81}$$

In particular, setting $t = 0$ gives the sampled frequency domain kernel for the system of Fig. 3.8,

$$\hat{H}_2(\omega_1, \omega_2) = \int_{-\infty}^{0} h_c(0, \tau) H_a(\omega_1, \tau) H_b(\omega_2, \tau) d\tau. \tag{3.82}$$

The Third order frequency domain representation is similar. If h_a in Fig. 3.8 is second order, then,

$$\hat{H}_3(\omega_1, \omega_2, \omega_3, t) = \int_{-\infty}^{t} h_c(t, \tau) H_a(\omega_1, \omega_2, \tau) H_b(\omega_3, \tau) d\tau, \tag{3.83}$$

and the overall frequency domain kernel is,

$$\hat{H}_3(\omega_1, \omega_2, \omega_3) = \int_{-\infty}^{0} h_c(0, \tau) H_a(\omega_1, \omega_2, \tau) H_b(\omega_3, \tau) d\tau. \tag{3.84}$$

Time-Varying Distortion in a Sampling Mixer

The sampling mixer of Fig. 3.2 is analyzed in the sampled data domain. Assume the input side is the source, the output is then the drain, from the basic MOS equation : [3]

$$\hat{g}(v_D - v_S) - \frac{K'}{2}(v_D - v_S)^2 + C\frac{dv_D}{dt} = 0.$$

The MOS transistor conductance is defined as $\hat{g} = K'(v_{GS} - V_t)$. The MOS transistor enters the cut-off region at $v_{GS} - V_t = 0$, so the value of $\hat{g}$ goes to zero at each sampling point. Since the RC time constant is assumed to be small, the region of most importance is the time right before the sampling instant. Therefore,

[3] Assuming the output side being source will give a slightly different differential equation, but the form of the answer is the same.

$\hat{g}$ may be approximated by a linear function prior to each sampling point. This assumption is most valid if the system time constant is smaller than the fall-time of the gate voltage. In practical cases where this is not true, the analysis yields a limiting case and provide a useful bound. The slope of the linearly varying g is just the slope of the cutting edge v_G minus the slope of the input signal v_S to a first order approximation. If $\beta = (2K'V_G)/T_f$, where V_G and T_f are as indicated in Fig. 3.2, and define $g = -\beta t$, the MOS equation becomes:

$$(g - K'\frac{dv_s}{dt} \cdot t)(v_d - v_s) - \frac{K'}{2}(v_d - v_s)^2 + C\frac{dv_d}{dt} = 0.$$

Letting $v_s = v_{in}$, $v_d = v_o$, expanding v_o into its Volterra series as before, and collecting the first three order terms,

$$\begin{cases} gv_1 + C\dfrac{dv_1}{dt} &= gv_{in} \\ gv_2 + C\dfrac{dv_2}{dt} &= K'\dfrac{dv_{in}}{dt}t(v_1 - v_{in}) + \dfrac{K'}{2}(v_1 - v_{in})^2 \\ gv_3 + C\dfrac{dv_3}{dt} &= K'\dfrac{dv_{in}}{dt}tv_2 + K'(v_1 - v_{in})v_2. \end{cases} \tag{3.85}$$

To calculate H_1, equation (3.79) is used where the time domain $h_1(t,\tau)$ is already solved in equation (3.68).

$$\begin{aligned} \hat{H}_1(\omega,t) &= \int_{-\infty}^{t} h_1(t,\tau)e^{j\omega\tau}d\tau \\ &= \int_{-\infty}^{t} e^{-\int_{\tau}^{t}\frac{g(\xi)}{C}d\xi}\frac{g(\tau)}{C}e^{j\omega\tau}d\tau \\ &= \int_{-\infty}^{t} e^{-k^2(\tau^2-t^2)}(-2k^2\tau)e^{j\omega\tau}d\tau, \end{aligned}$$

where the substitution of $g = -\beta t$ and $k^2 = \beta/2C$ are made. This integral cannot be evaluated analytically. However, the value of the integral when t is close to 0 is of interest, so the upper limit of the integral is close to zero. The integrand is a rapidly increasing function of τ as τ approaches 0, so effectively, the only relevant portion of the integration is when τ is close to 0. Therefore, it can be assumed

that $e^{j\omega\tau} \approx 1 + j\omega\tau$. In this case, the integral becomes: [4]

$$\hat{H}_1(\omega, t) = 1 + j\omega t - j\omega\sqrt{\frac{\pi}{4}} \cdot \frac{1}{k} \cdot e^{k^2t^2}(erf(kt) + 1). \tag{3.86}$$

So,

$$\hat{H}_1(\omega) = 1 - j\omega\sqrt{\frac{\pi}{4}} \cdot \frac{1}{k} \tag{3.87}$$

The second order term is evaluated using (3.81), where the time-varying kernel is obtained from its composition from first order terms:

$$\begin{aligned}\hat{H}_2(\omega_1, \omega_2, t) &= \int_{-\infty}^{t} \frac{e^{-\int_\tau^t \frac{g(\xi)}{C} d\xi}}{C} K' \cdot j\omega_1 \cdot e^{j\omega_1\tau} \cdot \tau \cdot (\hat{H}_1(\omega_2, \tau) - e^{j\omega_2\tau}) + \\ &\int_{-\infty}^{t} \frac{e^{-\int_\tau^t \frac{g(\xi)}{C} d\xi}}{C} \left(\frac{K'}{2}\right) (\hat{H}_1(\omega_1, \tau) - e^{j\omega_1\tau})(\hat{H}_1(\omega_2, \tau) - e^{j\omega_2\tau}) d\tau.\end{aligned} \tag{3.88}$$

Again, approximate $e^{j\omega t}$ by its Taylor expansion, substitute (3.86) to (3.88):

$$\begin{aligned}\hat{H}_2(\omega_1, \omega_2, t) &= \frac{\omega_1\omega_2}{C} \cdot K' \cdot \sqrt{\frac{\pi}{4}} \cdot \frac{1}{k} \cdot e^{k^2t^2} \int_{-\infty}^{t} \tau(erf(k\tau) + 1)^2 d\tau + \\ &\frac{\omega_1\omega_2}{C} \cdot \frac{K'}{2} \cdot \left(\frac{\pi}{4}\right) \frac{1}{k^2} \cdot e^{k^2t^2} \int_{-\infty}^{t} e^{k^2\tau^2}(erf(k\tau) + 1)^2 d\tau.\end{aligned} \tag{3.89}$$

Fortunately, at $t = 0$, the last two integrals may be evaluated numerically,

$$\hat{H}_2(\omega_1, \omega_2) = -\omega_1\omega_2 \left(\frac{K'}{C}\right) \cdot \frac{b}{k^3}. \tag{3.90}$$

where $b = 0.234$ comes from the evaluation of the definite integrals. (The relative contributions from the two integrals are actually comparable.) Finally, $\hat{H}_3$ is obtained in the same way:

$$\begin{aligned}\hat{H}_3(\omega_1, \omega_2, \omega_3, t) &= \int_{-\infty}^{t} \frac{e^{-\int_\tau^t \frac{g(\xi)}{C} d\xi}}{C} K' \cdot j\omega_1 \cdot e^{j\omega_1\tau} \cdot \tau \cdot \hat{H}_2(\omega_1, \omega_2, \tau) d\tau + \\ &\int_{-\infty}^{t} \frac{e^{-\int_\tau^t \frac{g(\xi)}{C} d\xi}}{C} K' (\hat{H}_1(\omega_3, \tau) - e^{j\omega_3\tau}) \hat{H}_2(\omega_1, \omega_2, \tau) d\tau.\end{aligned} \tag{3.91}$$

The above expression needs to be evaluated for $t = 0$. Because the $\hat{H}_2$ terms contain two integrals, there are in total four definite integrals. This is tedious but

[4] The error function is defined as: $erf(t) = \frac{2}{\sqrt{\pi}} \int_0^t e^{-x^2} dx$.

doable. Numerically, the answer turns out to be:

$$\hat{H}_3(\omega_1,\omega_2,\omega_3) = j\omega_1\omega_2\omega_3 \cdot \left(\frac{K'}{C}\right)^2 \cdot \frac{c}{k^5}, \tag{3.92}$$

where $c = 0.0913$ numerically. Equations (3.87), (3.90) and (3.92) are the final solution to the sampled time-varying Volterra series. To summarize the results in terms of circuit parameters:

$$\hat{H}_1(\omega) = 1 - j\omega \cdot \sqrt{\frac{C}{K'}}\left(\frac{T_f}{V_G}\right)^{1/2} \cdot a \tag{3.93}$$

$$\hat{H}_2(\omega_1,\omega_2) = -\omega_1\omega_2 \cdot \sqrt{\frac{C}{K'}}\left(\frac{T_f}{V_G}\right)^{3/2} \cdot b \tag{3.94}$$

$$\hat{H}_3(\omega_1,\omega_2,\omega_3) = j\omega_1\omega_2\omega_3 \cdot \sqrt{\frac{C}{K'}}\left(\frac{T_f}{V_G}\right)^{5/2} \cdot c, \tag{3.95}$$

where again $a = 0.886, b = 0.234, c = 0.0913$ numerically. It may be recalled that this result is obtained by assuming a linearly decreasing g. In reality, g is nearly constant for a large part of the sampling period. Therefore, this solution is an asymptotic case.

If the Volterra coefficients for the non-ideal sampling MOS sampling mixer are compared with the time-invariant case, it will be found that the non-linearity due to the time-varying nature is much smaller than the time-invariant case. Notice that the time-varying distortion varies with the cube of the frequency, so theoretically, at high frequency the time-varying distortion may overtake the time-invariant distortion. However this does not happen even at around the 1 GHz RF frequency range. The fact that the time-varying distortion is small can be intuitively explained. There are two sources of non-linearity from the MOS drain current equation:

$$I_d = K'((V_{GS} - V_t)V_{DS} - \tfrac{1}{2}V_{DS}^2)$$

An obvious source of non-linearity is the square term V_{DS}^2, but this effect is secondary for the time-invariant case, where the major contributing factor is the

input signal dependent conductance $K'(V_{GS} - V_t)$. However, in a non-ideal sampling mixer, the first order signal dependence in g is eliminated because the sampling always occurs when $V_{GS} - V_t = 0$, hence the local behavior of g prior to cut-off is approximately the same for each sampling point. Therefore, the only non-linear factors left are the signal dependence in the derivative of the conductance and the V_{DS}^2 term, which are significantly smaller. However, we are not really getting something for free here. Although in the case of a non-ideal mixer, the $K'(V_{GS} - V_t)$ term causes much less input dependence in g, the V_{GS} term manifests as an altogether different source of distortion. Because cut-off occurs when $V_{GS} - V_t = 0$, the cut-off time is now input signal dependent. In other words, the distortion in the amplitude domain is translated into non-uniform-sampling distortion.

3.4 Simulation Results and Comparison with Theory

Hspice simulations are performed to verify the theoretical results derived in the previous sections for the cases of time-invariant, time-varying and non-uniform-sampling distortion. The sampling mixer is fed with either single tone or two tones near 100MHz at its IF input. For example, to estimate intermodulation distortion, a 100.3 and 100.4 MHz signal are applied at the IF input, and a 100MHz square-wave sampling clock at the gate. Consistent with our standing assumptions, the RC time constant during the on period has been chosen to be approximately 20ps and therefore much smaller than the 5 ns, the on period of the sampling clock. The NMOS device data for this simulation are given in Table 2.1.1. A V_{GS} of 2.5 V has been assumed.

3.4.1 Simulation Accuracy and Speedup

A number of precautions have to be taken to ensure numerical accuracy, convergence and charge conservation in the simulations. The simulation accuracy has to be calibrated with ideal sine tones and simple linear models. The maximum time-step value and time algorithm also have to be chosen consistent with the dynamic range to be expected from simulations. The time-step parameter (DELMAX) is crucial in determining simulation accuracy. Experience has shown that a DELMAX as low as 0.1 ps is necessary to achieve reasonably accurate results. Charge conservation is particularly difficult to achieve. It depends on the level of the MOS model chosen, the MOS device capacitance (CAPOP) model and the integration method. Our experience has also been that the charge conservation models (CAPOP=4 and CAPOP=9 in Hspice) either have poor convergence properties or produce numerical inaccuracy. Charge-injection and charge-conservation problems have been by-passed by calculating the device capacitances separately and inserting linear capacitances into the circuit and using a no-capacitance (CAPOP=5) model. Without these precautions, the simulation results can be rendered totally useless.

Hspice simulation for very small values of DELMAX can make the simulation time impractically long. A major factor in speeding up the simulation time has been the insight that the RC time-constant during the on period of the MOS transistor is much smaller than the on period itself. Thus, since the circuit reaches steady state within only a tiny fraction of the on period, it is only necessary to simulate around the sampling edge. This has been accomplished by repeated simulations at uniform phase intervals of the input sine-wave for a total phase interval of 360 degrees, which corresponds to exactly 1 period of the mixed down frequency.

3.4.2 Harmonic Distortion

Figure 3.9 plots the 2nd and 3rd order harmonic distortion of a sampling mixer with a MOS switch W/L of 102 $\mu m/0.8\ \mu m$. The sampling capacitance is 0.2pF. An additional capacitance of 0.152 pF is added to account for source/drain capacitance. A square-wave with fall-time varying between 10ps and 1.28ns is applied at the gate. In this simulation the Spice model parameter gamma has been set to 0 to exclude substrate bias modulation of the threshold voltage (in order to make the simulation consistent with the model of non-linearity used for the MOS transistor in the theoretical analysis). The distortion picture of the mixer may be clarified by dividing the distortion curves in the graph into 3 regions:

1. A relatively flat portion corresponding to small fall-times up to a few tens of picoseconds.

2. A region with distortion decreasing with fall-time and having a distinct minima.

3. A region with distortion increasing with fall-time occurring for large fall-times and with a distinct slope of 20 dB/decade for HD_2 and 40 dB/decade for HD_3.

Region 1 shows an asymptotic behavior towards 0 fall-time. This asymptotic distortion value is very close to that predicted from time-invariant(time-invariant) harmonic distortion model formulae (3.35)-(3.38). This is to be expected since it has been shown in section 3.2 that for a fall-time of 0, the harmonic distortion of the MOS sampling mixer approaches the time-invariant harmonic distortion.

Region 3 displays asymptotic behavior towards a log-linear relation that increases at 20 dB/decade for HD_2 and 40 dB/decade for HD_3. This line corresponds to the distortion predicted by non-uniform-sampling distortion

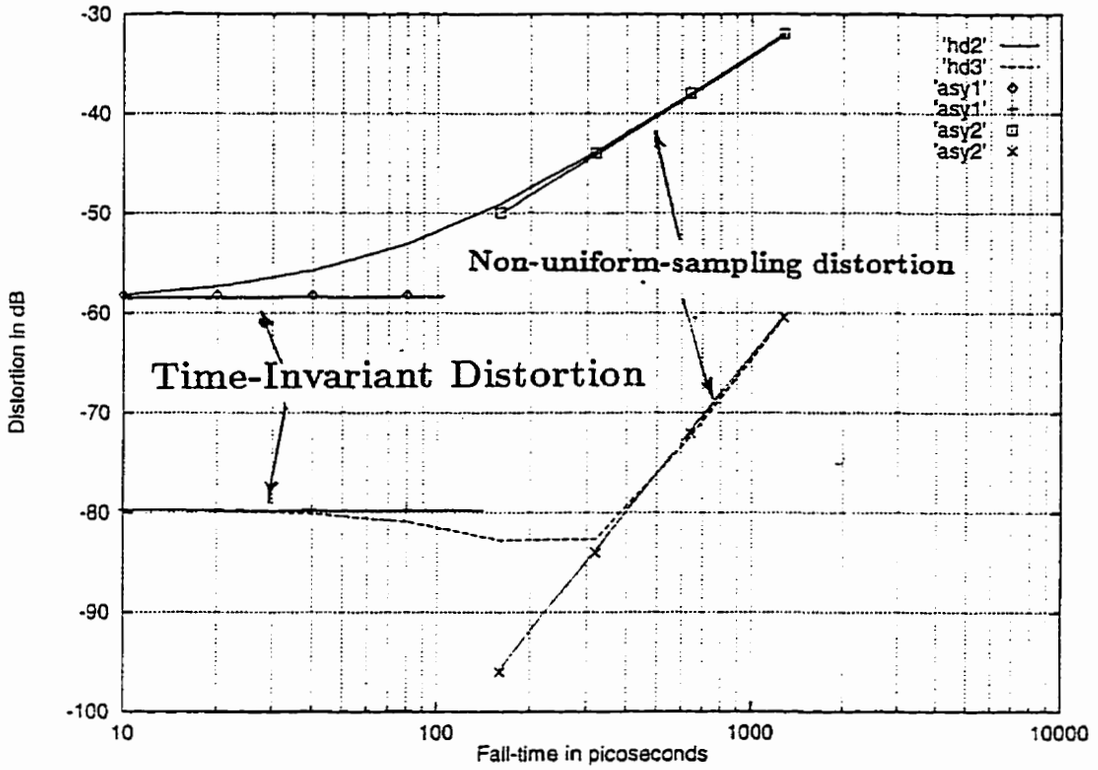


Figure 3.9: HD_2(top trace) and HD_3(bottom trace) in a top-plate sampling mixer vs. fall-time

equations (3.60)-(3.63). Hence, for large fall-times, harmonic distortion is limited by non-uniform-sampling distortion.

Region 2 can be explained by time-varying distortion of a MOS sampling mixer at whose gate a non-zero fall-time sampling signal is applied. In section 3.3.2 it was pointed out that for the case of non-ideal sampling if sampling error is neglected, harmonic distortion, now attributed to time-varying distortion, becomes very small. Thus it is possible for the fall-time to lie in an intermediate region where the fall-time is large enough so that the contribution due to the time-invariant operation is small, while at the same time the fall-time is small enough that non-uniform-sampling distortion does not manifest itself.

In order to highlight the role of time-varying distortion it may be first noted that the third order non-uniform-sampling distortion is proportional to the square of the input frequency, ω. Thus, for large fall-times, by reducing the input frequency non-uniform-sampling distortion may be reduced sufficiently enough for time-varying distortion to manifest itself over a wider window (i.e. region 2) of the sweep of fall-time. Conversely, by increasing the input frequency, non-uniform-sampling distortion may increase to the point that it completely swamps the time-varying distortion. This trend is confirmed in Fig. 3.10 which plots HD_3 vs. fall-time for 25, 100 and 500 MHz.

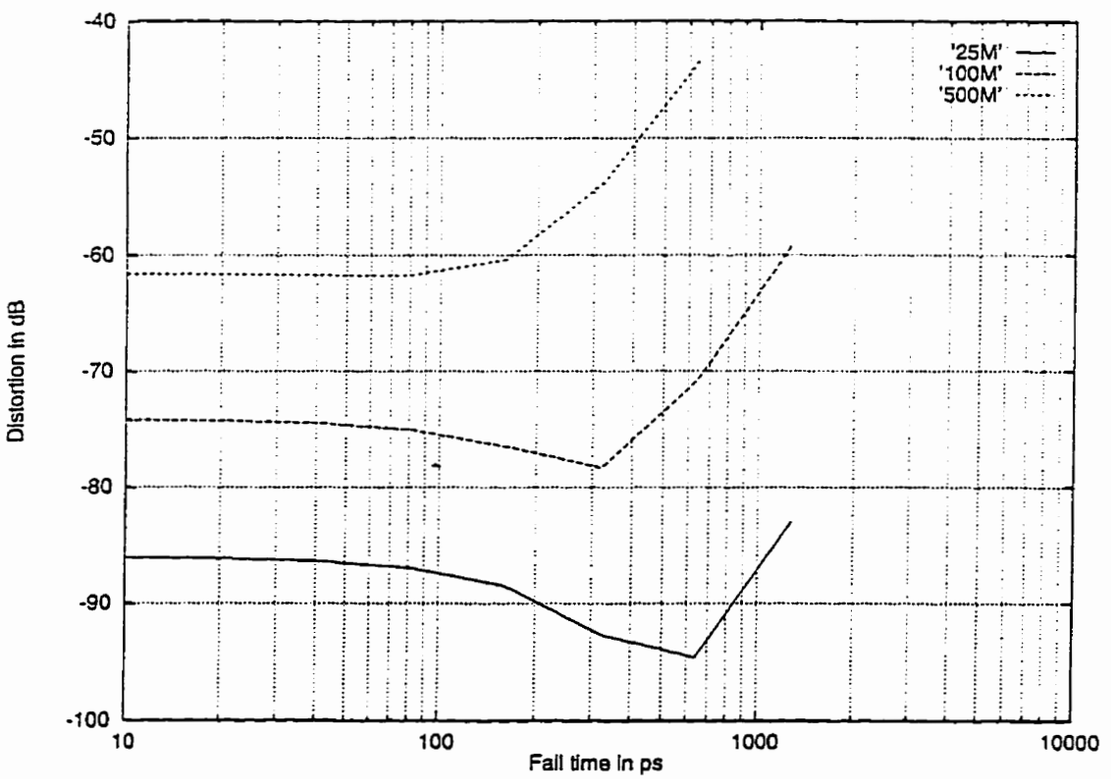


Figure 3.10: IM_3 vs T_f for 500 (top), 100 (middle) and 25 MHz (bottom) IF frequency

Thus, it has been shown both by simulation and by time-varying analysis, that a region with a distortion smaller than the 0 fall-time asymptotic value

predicted by time-invariant distortion exists which explains the decreasing distortion and minima observed in this region. The practical significance of this result is that the distortion of a MOS sampling mixer can actually be better than what would be predicted by time-invariant Volterra series theory by a proper choice of fall-time. It may be noted that this does not occur for HD_2 and IM_2 in this particular case because non-uniform-sampling distortion is bigger than the time-invariant distortion, even for small fall-times.

3.4.3 Intermodulation Distortion

Figure 3.11 shows the intermodulation distortion of the MOS sampling mixer obtained by applying two tones at 100.3 and 100.4 MHz at the IF input and a 100MHz sampling clock at the gate. IM_2^- resulting from the difference of the two input frequencies is very small. IM_2^+, which behaves the same as HD_3, is shown. The distortion characteristics again match very well with the theoretical prediction both for the time-invariant formulae developed in section 3.2 and for the non-uniform-sampling distortion developed in section 3.3.1. Again, the initial decrease in the IM_3 curve as the fall-time increases may be explained by the system time-varying nature. In general, intermodulation distortion is slightly worse than harmonic distortion, but they exhibit similar behavior with respect to fall-time.

3.5 Bottom-Plate Sampling

In this section bottom-plate sampling is analyzed as a practical application of the theoretical results developed earlier. The basic configuration is shown in Fig. 3.12. The input is at v_{IF}, and the output is taken as the differential voltage between X and Y. During sampling the bottom switch opens first which effective fixes the amount of charge on the capacitor C_s, then the top switch opens, which fixes the

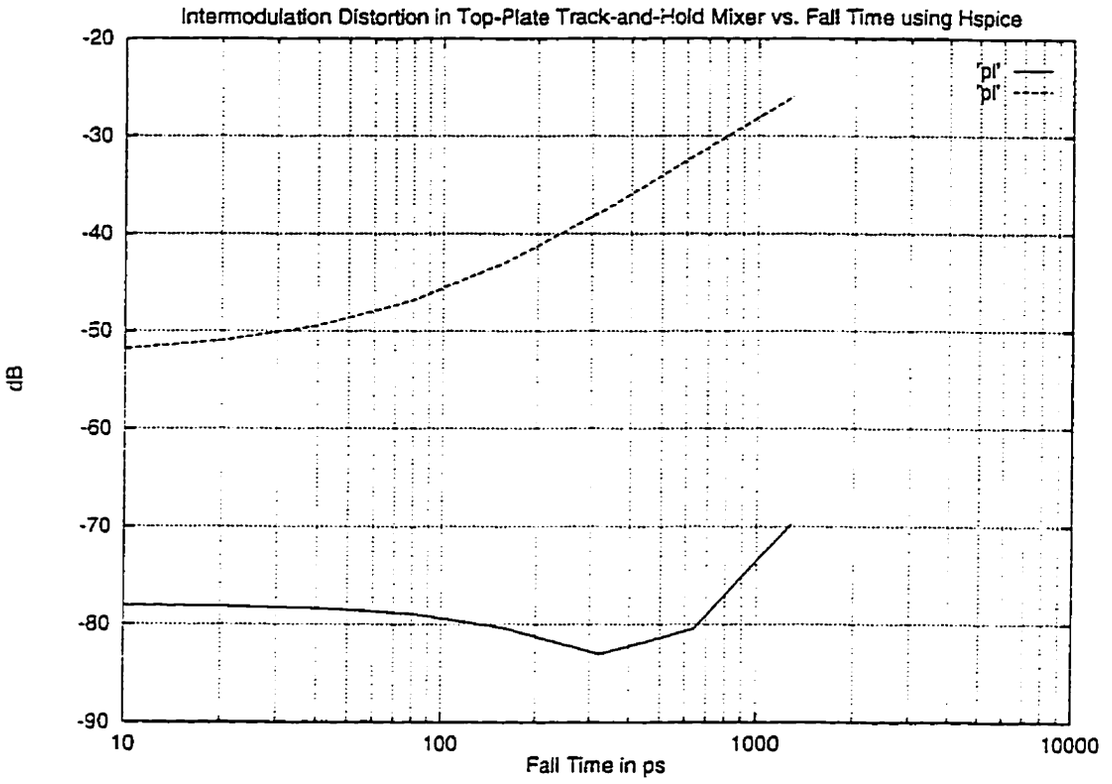


Figure 3.11: IM_{2+}(top-trace) and IM_3(bottom-trace) of a sampling mixer vs. fall-time

voltage level of X and Y. In the figure, C_j is included as the junction capacitor of the top switch, which can be fairly large, and C_p is included as the junction capacitor of the bottom switch, which is typically much smaller.

The main advantage of bottom-plate sampling is that it eliminates the charge injection problem. As explained in chapter 2, when a MOS transistor turns *off*, the charges that comprise the inversion layer are injected to either the source or the drain side depending on the relative impedance seen on each side. In the normal case of a sample-and-hold (Fig. 3.2), the impedance on the output side ($1/j\omega C_s$) can be very small, so it attracts the extra charges, which disturb the output signal level and contribute to distortion. This does not happen in bottom-plate sampling. At the opening of the bottom switch, charges are injected to the ground, while at

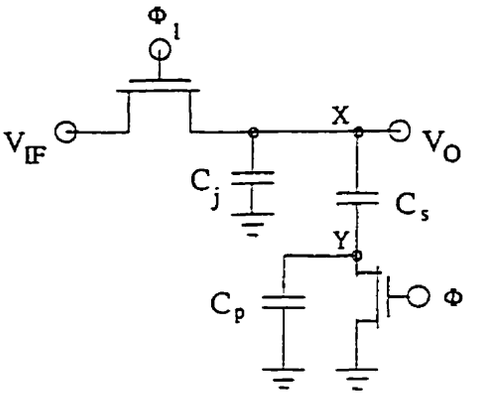


Figure 3.12: Bottom-plate Sampling

the opening of the top switch, the charges are injected to the input. In either case, very little extra charges are dumped to the sampling capacitor.

To analyze this circuit, the transistors are first modelled as simple switches. It can be shown that the output voltage has two components:

$$V_{out} = V_{bottom} + V_{top} \tag{3.96}$$

where V_{bottom} and V_{top} are the voltages across the sampling capacitor when the bottom switch and top switch open respectively.

Distortion due to the two parts are now analyzed separately. As discussed before, three components in each part need to be considered: the time-invariant distortion, the time-varying distortion, and the non-uniform-sampling distortion.

3.5.1 Distortion due to Opening of Bottom Switch

It is noticed that the non-uniform sampling error is small when the bottom switch is opened. This is because the source and the drain of the bottom switch are kept almost constant at the ground level, which eliminates signal dependent sampling.

Next, the continuous time distortion can be calculated from the coupled differential equations. Assume that both transistors are working in the triode

region with device constants K_1', K_2', respectively. Define $g_1 = K_1'(V_{GS_1} - V_t)$ and $g_2 = K_2'(V_{GS_2} - V_t)$, the governing equations are:

$$\begin{cases} g_1(v_{in} - X) - \dfrac{K_1'}{2}v_{in}^2 + \dfrac{K_1'}{2}X^2 = C_s\dfrac{dX}{dt} - C_s\dfrac{dY}{dt} \\ g_2 Y - \dfrac{K_2'}{2}Y^2 = C_s\dfrac{dX}{dt} - (C_s + C_p)\dfrac{dY}{dt}, \end{cases} \tag{3.97}$$

where X and Y are the voltage on the 2 terminals of the capacitor, i.e. nodes X and Y, for which the following Volterra series expansions can be assumed:

$$\begin{aligned} X(t) &= \mathbf{H_1}[v_{in}(t)] + \mathbf{H_2}[v_{in}(t)] + \mathbf{H_3}[v_{in}(t)] + \cdots, \\ Y(t) &= \mathbf{G_1}[v_{in}(t)] + \mathbf{G_2}[v_{in}(t)] + \mathbf{G_3}[v_{in}(t)] + \cdots. \\ V_{bottom}(t) &= X(t) - Y(t) = \mathbf{J_1}[v_{in}(t)] + \mathbf{J_2}[v_{in}(t)] + \mathbf{J_3}[v_{in}(t)] + \cdots, \end{aligned} \tag{3.98}$$

where $\mathbf{J_n} = \mathbf{H_n} - \mathbf{G_n}\ Y(t)$ may be first solved in terms of $X(t)$ using the second equation in (3.97) to obtain

$$Y(t) = \mathbf{I_1}[X(t)] + \mathbf{I_2}[X(t)] + \mathbf{I_3}[X(t)] + \cdots, \tag{3.99}$$

Thus from 3.97, we can obtain both $Y(t), X(t)$ in terms of v_{in}.

The circuit for evaluation of the coefficients $\mathbf{I_n}$ is shown in Fig. 3.13. The system equations can be written as,

$$\begin{cases} g_2 v_1 + (C_p + C_s)\dfrac{dv_1}{dt} = C_s\dfrac{d}{dt}v_{in} \\ g_2 v_2 + (C_p + C_s)\dfrac{dv_2}{dt} = \dfrac{K_2'}{2}v_1^2 \\ g_2 v_3 + (C_p + C_s)\dfrac{dv_3}{dt} = K_2' v_1 v_2, \end{cases} \tag{3.100}$$

The Volterra coefficients may now be solved as ,

$$I_1(\omega_1) = \frac{j\omega_1 C_s}{g_2 + j\omega_1 C_s'} = 0 \tag{3.101}$$

$$I_2(\omega_1, \omega_2) = \frac{(j\omega_1 C_s)(j\omega_2 C_s)}{2K_2'^2(V_{GS} - V_t)^3} \tag{3.102}$$

$$I_3(\omega_1, \omega_2, \omega_3) = \frac{(j\omega_1 C_s)(j\omega_2 C_s)(j\omega_3 C_s)}{2K_2'^3(V_{GS} - V_t)^5} \tag{3.103}$$

where $C_s' = C_s + C_p$

Expressions for HD_2, HD_3, IM_3 may be derived in a manner similar to previous cases. A substitution of $C_s = 0.2pF$, $\omega_1 = 2\pi 100MHz$, $K_2' = 1.87e-03A/V^2$ for a $W/L = 15\ \mu/0.8\ \mu$, $(V_{GS} - V_t) = 1.487V$, gives second harmonic distortion $HD_{2-bot} = -114\ dB$.

The ratio of distortion produced by the bottom switch to that of the top switch may now be computed as,

$$\frac{HD_{2-bot}}{HD_{2-top}} = \frac{K_1'\omega_2 C_s}{2K_2'^2(V_{GS} - V_t)} \tag{3.104}$$

From the above formula the distortion due to the top switch with $W/L = 15\ \mu m/0.8\ \mu m$ as compared to that due to the bottom switch of the same size is higher by 33 dB. Therefore distortion due to the bottom switch can be made negligibly small.

If the assumption is made that $g_1 \gg j\omega C_s$, $I_n = G_n$. Since I_n has been shown to be small, the time-invariant distortion in a bottom-plate sampling mixer can be considered to be approximately the same as that of the top-switch sampling mixer. Therefore,

$$HD_3 = \frac{A^2}{4} \cdot \frac{j\omega(C_s + C_j)}{K_1'(V_G - V_t)^3} \tag{3.105}$$

$$IM_3 = \frac{A^2}{4} \cdot \frac{j\omega(C_s + C_j)}{K_1'(V_G - V_t)^3}. \tag{3.106}$$

Note that the continuous time distortion is determined by the (W/L) ratio of the top switch.

Finally, time-varying distortion needs to be taken into account. This is difficult because the differential equation is second order with non-constant coefficients for which solutions are not easily found. However, it is possible to simplify the situation. When the bottom switch opens, the resistance between the

source and the drain increases with time and eventually reaches infinity; but the top switch stays closed, hence its resistance is relatively small. Therefore, the top switch can be neglected altogether and the problem may be simplified to that shown in Fig. 3.13, which has only one capacitive node, which produces a first order equation that can be solved. However, as in the case of the simple sampling mixer of Fig. 3.2, the time-varying distortion can be expected to be much smaller than the time-invariant distortion. More importantly, the amplitude of the signal at the bottom plate $Y(t)$ is expected to be much smaller than the amplitude of the input/output in any case. Thus, for all practical purposes the time-varying distortion due to the opening of the bottom switch is negligibly small.

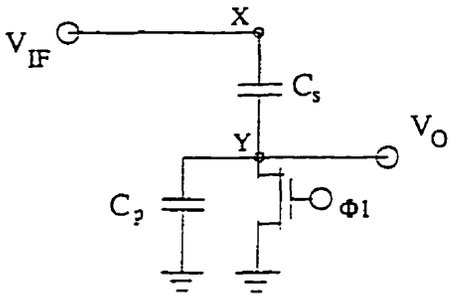


Figure 3.13: Simplified circuit for bottom-plate sampling

Therefore, as the bottom switch opens, the distortion accumulated is mainly due to the time-invariant operation as expressed in equations (3.105) and (3.106), because both the time-varying and the non-uniform-sampling distortions are small.

3.5.2 Distortion in Opening Top Switch

The distortion analysis for the top switch is considerably simpler. This is when the bottom switch is open, so the situation is identical to the case in Fig. 3.2 except that the capacitor is primarily due to parasitics. The distortion again consists of three parts: time-invariant, time-varying, and non-uniform-sampling distortion.

The time-invariant distortion is given by equations (3.35)-(3.38):

$$HD_3 = \frac{A^2}{4} \cdot \frac{j\omega C}{K_1'(V_G - V_t)^3} \tag{3.107}$$

$$IM_3 = \frac{A^2}{4} \cdot \frac{j\omega C}{K_1'(V_G - V_t)^3}, \tag{3.108}$$

where the capacitor C here is,

$$C = \frac{C_s C_p}{C_s + C_p} + C_j. \tag{3.109}$$

Since the capacitor in this case is primarily due to the parasitic, which is much smaller than in the single switch case, the time-invariant distortion is small. The non-uniform-sampling distortion is the same as before as given by (3.60)-(3.63):

$$HD_3 = \frac{3A^2}{32}\left(\frac{\omega T_f}{V_G}\right)^2 \tag{3.110}$$

$$IM_3 = \frac{A^2}{32}\left(\frac{\omega T_f}{V_G}\right)^2 \tag{3.111}$$

Again, the time-varying distortion is very small.

Therefore, as the top switch opens, because both time-invariant and time-varying distortion are small, the total distortion is mainly due to the non-uniform-sampling distortion due the top switch alone in a top-plate non-uniform-sampling configuration.

3.5.3 Total Distortion

It can be seen that the distortion due to the opening of the bottom switch comes from the time-invariant operation, and that due to the opening of the top switch comes from non-uniform sampling, so the total distortion is just a linear combination of the two as in (3.96).

$$HD_3 = \frac{A^2}{4} \cdot \frac{j\omega(C_s + C_j)}{K_1'(V_G - V_t)^3} + \left(\frac{C_p}{C_s + C_p}\right) \cdot \frac{3A^2}{32}\left(\frac{\omega T_f}{V_G}\right)^2 \tag{3.112}$$

$$IM_3 = \frac{A^2}{4} \cdot \frac{j\omega(C_s + C_j)}{K_1'(V_G - V_t)^3} + \left(\frac{C_p}{C_s + C_p}\right) \cdot \frac{A^2}{32}\left(\frac{\omega T_f}{V_G}\right)^2 \tag{3.113}$$

This is similar to the case of a simple sample-and-hold mixer. However, the major difference is that the distortion due to sampling (when the top switch opens) is less by a factor of $\frac{C_p}{C_s+C_p}$, which is significant. Therefore, distortion due to a non-zero fall-time is less a problem in bottom plate sampling than in the simple case of Fig. 3.2. This is another advantage of bottom-plate sampling.

3.5.4 Simulation of Bottom-plate sampling mixer

Fig. 3.14 shows the plot of HD_2 and HD_3 for a bottom-plate sampling mixer without body effect (gamma has been set to 0). The distortion trend is similar to the trend for top-plate sampling mixer shown in Fig. 3.9. However, as expected, the non-uniform-sampling distorion is smaller in the former because of the attenuation due to the attenuation by the series network consisting of C_s and C_p in Fig. 3.13. It is also noticed that the dip in HD3 that occurs in a top-plate sampling mixer due to time-varying distortion, does not occur in the bottom-plate case. A convincing explanation for this behavior has not been found.

3.6 Design of LO Buffer

Distortion in a sampling mixer has been shown to be dependent upon the fall-time of the LO signal driving the gates of the mixing transistors. Therefore it is necessary to design buffers that can shape the LO signal so that its fall-time is minimized in order to ensure that time-invariant distortion mechanism dominates for both the top and bottom switches. [5]. The LO buffer circuit required for bottom-plate sampling mixer is essentially a chain of CMOS inverters as shown in Fig. 3.15. The size of the NMOS transistor of the buffers, MN1 and MN3 are relatively large to provide a pull-down current current large enough for a desired

[5]Note that if a top-plate sampling mixer is used minimum distortion is achieved at a finite fall-time where time-varying distortion mechanism is active

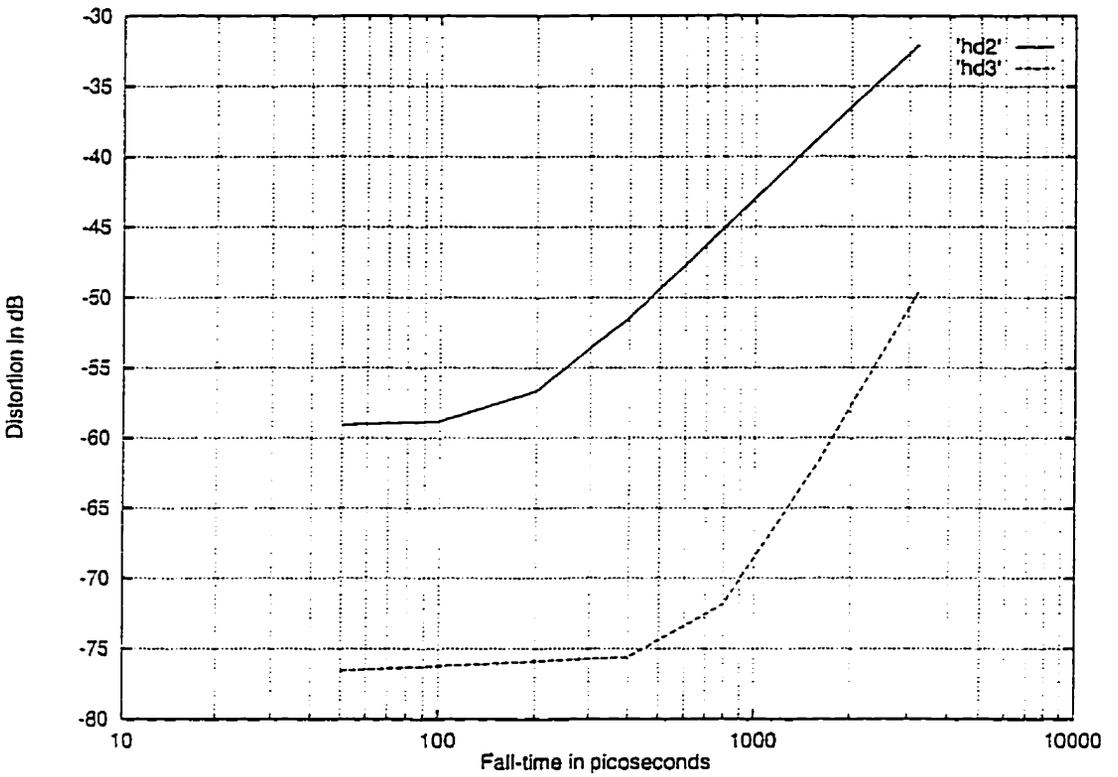


Figure 3.14: HD_2(top trace) and HD_3(bottom trace) in a bottom-plate sampling mixer vs. fall-time

small fall slewing time. The fall-time achievable is dependent upon the drain-substrate junction capacitances of the LO buffer outputs, the capacitance looking into the gate of the mixer transistors and the logic swing. It may be noted that there is a transistor size beyond which the junction capacitances prevent any further decrease in fall-time. The derivation of exact analytical solution is complicated by the fact that drain-current expressions for the saturation region have to incorporate effects such as mobility degradation due to velocity saturation. As a result, the familiar long-channel square-law relationship between drain current and gate-source overdrive ($(V_{GS} - V_t)$) is no longer valid. A second complication is that the pinch-off point is no longer at ($(V_{GS} - V_t)$). One empirical approach reported [17], uses an "α-Power Law" in which the $I_d \propto (V_{GS} - V_t)^{\alpha}$, where α is

dependent upon device channel length and varies between 2 and 1(for a completely velocity saturated device). The analytical solution for fall-time is:

$$T_f = \frac{t_{0.9} - t_{0.1}}{0.8} \tag{3.114}$$

$$= \frac{C_L V_{DD}}{I_{D0}} \left(\frac{0.9}{0.8} + \frac{V_{D0}}{0.8 V_{DD}} ln \left(\frac{10 V_{D0}}{e V_{DD}} \right) \right) \tag{3.115}$$

where $C_L = C_{gate} + C_{dp} + C_{dn}$ is the total load capacitance,

I_{D0} is the maximum saturation current with gate and drain tied to V_DD

$V_{D0} = V_{DD} - V_{th}$.

For a mixer transistor $W/L = 100\mu\ m/0.8\mu m$ that has a total gate capacitance of 160 fF, $V_{DD} = 5V$, $V_{D0} = 4.417V$, a buffer NMOS transistor $(W/L)_n = 60\mu\ m/0.8\mu m$, $C_{dp} + C_{dn} = 167\ fF$, the calculated value of T_f is 177 ps. The value obtained from Hspice simulation is 160 ps. Therefore, even though this model is empirical, it gives a reasonable estimate of the fall-time of the LO signal driving the transistors of the sampling mixer.

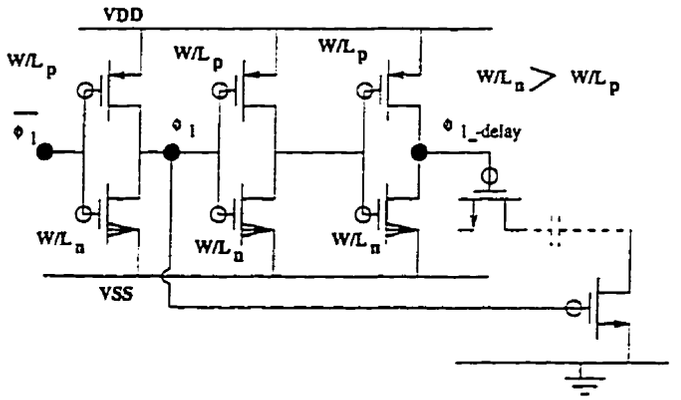


Figure 3.15: LO Buffer driving a bottom-plate sampling mixer

3.7 Design Example

Assume that it is required to design a bottom-plate sampling mixer with minimum length($0.8\mu m$) devices in 0.8 μm BiCMOS technology and with the following requirements:

Signal amplitude =$0.316V$(0dBm corresponding to 50 Ω)

$SNR_{kT/C} = 70\ dB$

$IM_3 = -70\ dB$

$f_{BW} = 8\ MHz$

$f_s = 20\ MHz$

$f_{IF} = 200\ MHz$

The process related parameters assumed are given below:

$V_t = 1.013\ V$ (including body effect)

$(V_{GS} - V_t) = 1.487\ V$

Junction cap. per unit width = $Cj_W = 1.52\ fF/\mu m$

Device constant K' per unit width= $K'_W = 1.39e-04\ A/V^2\mu m$

Using the formula for noise power due to kT/C noise of the sampling transistor given in equation (2.13), the value of the sampling capacitance C_s is calculated to be 0.662 pF. The total capacitance seen in the distortion calculation includes the junction capacitance which is dependent upon the size of the top switch. The top switch size is determined by expressing the total capacitance as a function of K' and by solving the IM_3 equation for time-invariant distortion as a function of K'.

$$IM_3 = \frac{A^2\omega\left(C_s + (\frac{Cj_W}{K'_W})K'\right)}{4(V_{GS} - V_t)^3K'}$$

From the above equation the device constant of the top switch $K'_{top} = 0.0298A/V^2$ and the $(W/L)_{top} = 214\ \mu m/0.8\ \mu m$ are obtained. The size of the bottom switch

may be obtained from equation (3.104) $(W/L)_{bottom} = 20.5\mu m/0.8\ \mu m$. The time-constant of the circuit including the junction capacitance is about $\tau = 23ps$. The requirement on the fall-time of the gate signal so that non-uniform-sampling distortion is negligible can be obtained from equation (3.64) to be $T_f \ll 340\ ps$. The sampling mixer LO buffer therefore needs to be designed for a fall-time much less than this value. For the MOS Gilbert mixer, using the same data for A and $(V_{GS} - V_t)$ and using the expression for IM_3 derived using Volterra series given in equation (3.24), we obtain an IM_3 of at least -47.5 dB (higher if junction capacitances are included) which is considerably larger than the IM_3 of the designed sampling mixer.

3.8 Discrete-time vs. Continuous-time Distortion in a Sampling Mixer

The sampling mixer of Fig. 3.2 can be operated both for discrete-time as well as continuous-time observation. So far, distortion has been calculated in the discrete-time domain, i.e. by assuming that the sampling mixer is observed by taking snapshots of the voltage held in the capacitance when the MOS switch has turned off. The question naturally arises how the distortion observed in the sampled mode of operation differs from the distortion observed in the continuous-time mode. This question may be answered under the condition that the time-constant of the circuit is small as assumed in the analysis for discrete-time observation and that the initial conditions of the circuit when the switch turns on have a negligible effect on the output i.e. the output reaches steady state as soon as the switch turns on. The model for the calculation of distortion is shown in Fig. 3.16.

The output of the circuit in the continuous-time domain for an ideal square wave applied at the gate of the switch can be shown to be:

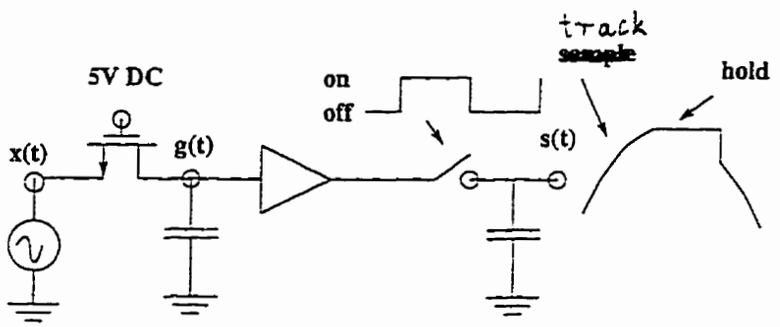


Figure 3.16: Continuous-time mixer distortion model

$$S(\omega) = \frac{1}{2}\sum_{-\infty}^{\infty} G(\omega - n\omega_s)\left(e^{-j\frac{\omega T_s}{4}} sinc(\frac{\omega T_s}{4}) + e^{-j\frac{n\pi}{2}} sinc(\frac{n\pi}{2}) e^{-j\frac{\omega T_s}{2}}\right)$$

where $G(\omega)$ is the fourier transform of the input signal and T_s is the sampling clock period. It is clear that the effect of the sample-and-hold is to perform the mixing(frequency translation) function but with a conversion gain factor. The gains obtained for the different harmonic components of the input signal are:

$$Low - frequency : (n = 0) \qquad S(\omega) = G(\omega) \tag{3.116}$$

$$Fundamental : (n = -1) \qquad S(\omega) = \frac{1}{2}[1 + j\frac{2}{\pi}]G(\omega + \omega_s) \tag{3.117}$$

$$2nd\ Harmonic : (n = -2) \qquad S(\omega) = \frac{1}{2}G(\omega + 2\omega_s) \tag{3.118}$$

$$3rd\ Harmonic : (n = -3) \qquad S(\omega) = \frac{1}{2}[1 + j\frac{2}{3\pi}]G(\omega + 3\omega_s) \tag{3.119}$$

From the above equations the conversion gains for mixing with different harmonics are obtained as:

$$C.G._{(\omega = 0)} = 0dB \tag{3.120}$$

$$C.G._{(\omega = \omega_s)} = -3.1dB \tag{3.121}$$

$$C.G._{(\omega = 2\omega_s)} = -6.0dB \tag{3.122}$$

$$C.G._{(\omega = 3\omega_s)} = -5.83dB \tag{3.123}$$

$$\tag{3.124}$$

The harmonic and intermodulation distortion for the output of the sampling mixer but observed in continuous-time domain may now be related to the distortion observed in discrete-time as follows:

$$\frac{HD_{2-cont}}{HD_{2-discr}} = \frac{1}{\sqrt{1+4/\pi^2}} = -2.9dB \tag{3.125}$$

$$\frac{HD_{3-cont}}{HD_{3-discr}} = \sqrt{\frac{1+4/(9\pi^2)}{1+4/\pi^2}} = -2.73dB \tag{3.126}$$

$$\frac{IM_{3-cont}}{IM_{3-discr}} = 1.0 = 0dB \tag{3.127}$$

Therefore, it may be concluded that for a very small RC time constant and for ideal clock waveforms, distortion of the sampling mixer circuit when the output is observed as discrete samples is related to the distortion when the output is observed continuously.

Chapter 4

Design of Passive Sigma-delta Modulators for IF Digitizers

4.1 Introduction

In chapter 1 it was shown that the problem of IF digitization can be reduced to a problem of the design of a sampling mixer and the problem of the design of a low-noise base-band A/D converter. This chapter addresses the second part. Base-band A/D converters can be designed using a number of available architectures: successive-approximation, pipelined, algorithmic, flash or sigma-delta depending upon considerations such as the bandwidth of the signal that is to be converted, power dissipation, chip-area etc. In this chapter, the design of the base-band A/D converter using sigma-delta is discussed. The motivation for this architecture comes mainly from low bandwidth applications such as wireless pagers, cellular phones, videophone and low bit-rate data applications which have channel bandwidths restricted to a few tens of kilohertz and for which oversampling is suitable. Furthermore, increasingly aggressive power budgets are making it necessary to use passive architectures for the A/D converter as in the

case of the sampling mixer. This chapter therefore discusses issues and solutions in the design of passive sigma-delta A/D converters upto resolutions of 13 bits and clocked at frequencies upto a few tens of megahertz.

Passive sigma-delta A/D converters (that do not use opamps in their loop-filters) have been shown in a previous work [1], [18] to be capable of achieving extremely low power and upto 13 bit resolution for IF digitizers operating with upto 10 MHz IF input as well as 10 MHz sampling clock frequency. For higher IF frequencies, a higher clock frequency is desirable for two reasons:

(a) For a given signal bandwidth, the signal mixed down to base-band by the sampling mixer is converted with a larger oversampling ratio and therefore can be converted with higher quantization SNR. Alternatively, for a given SNR a wider signal bandwidth can be converted.

(b) As shown in chapter 2 aliasing effects cause wide-band RF noise to be folded over into the Nyquist band. The aliasing factor reduces at a higher clock frequency leading to a better SNR.

The previous work also discusses a gain-boosting method that was measured to provide about 6 dB additional loop-gain and therefore a corresponding improvement in SNR. However, the passive gain-boosting network requires a network of CMOS switches in series which not only slow down the maximum clock frequency of the modulator but also load the nodes of the loop-filter with non-linear junction capacitances that give rise to distortion at high clock frequencies.

In the present work a different approach has been taken to improve the sigma-delta modulator resolution without compromising clock speed. In this approach the modulator SNR is improved by reducing the equivalent input noise of the comparator by using the bipolar transistor available in BiCMOS processes. The clock-speed of the modulator has also been improved substantially in the

present design over previous work by using a BiCMOS preamplifier and latch. It should be noted that the design of such comparators is far more critical than the comparators used in quantizers of active loop-filter based sigma-delta modulators because the signal levels in the former case are very small and comparable to the equivalent input noise of the comparator.

This chapter will begin by reviewing the theory and principle of operation of a passive sigma-delta A/D converter. It will then analyze the effect of quantization noise, thermal noise due to the switches and the thermal noise contributed by the comparator to the total SNR of the converter. Design considerations for low-noise, high-speed comparators and a loop-filter are discussed next, followed by a roadmap for the sigma-delta modulator design. Finally, the chapter will compare comparators using BJT input stages with those using MOS input stages and show why BJT input comparators are not suitable because of their equivalent input noise current due to base current shot noise.

4.2 SNR in a Passive Sigma-delta Modulator

Passive sigma-delta modulators consist of a sample-and-hold and a summing network, a switched-capacitor based loop-filter and a 1-bit quantizer consisting of a clocked comparator. The switched-capacitor based loop-filter consists only of switches and capacitors and implements a low-pass noise-shaping transfer function in the discrete-time domain. Since the loop-filter does not have any gain and may even have attenuation in the signal band, the quantizer provides the requisite loop gain necessary for the modulator to suppress the quantization noise in the signal band. The analysis of SNR due to quantization noise and the noise due to the comparator have been done in [1] and is reviewed here.

4.2.1 SNR due to Quantization Noise

A simple model for visualization of the operation of a second-order passive sigma-delta modulator is shown in Fig. 4.1. R-C sections R1,C1 and R2,C2 implement a second-order low-pass transfer function which provide noise-shaping, by filtering out the quantization noise at low frequencies near the signal band. The comparator functions both as a quantizer and crucially provides the necessary loop-gain required for proper noise-shaping. The resistor Rz and capacitor C2 provide a high frequency zero in the transfer function to improve stability by increasing the phase margin of the system at unity gain in open loop.

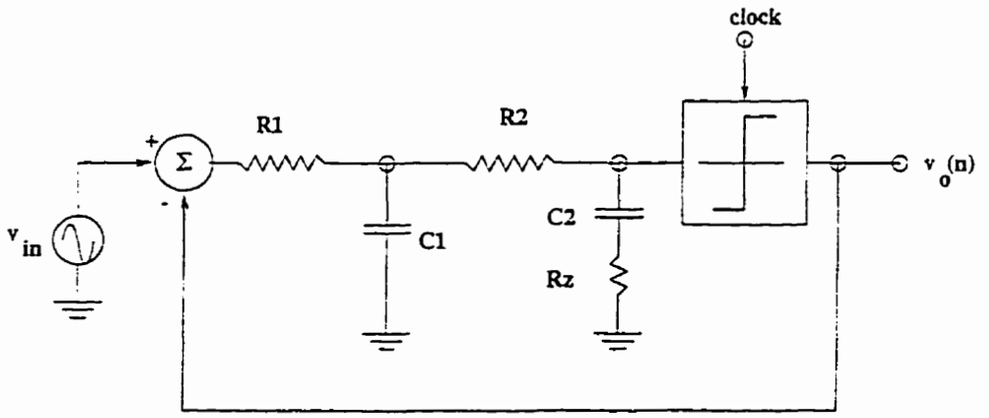


Figure 4.1: Model for passive loop-filter based sigma-delta modulator

The maximum SNR that can be achieved in a second-order modulator can be shown, under white-noise assumption for the quantization noise, to be,

$$SNR_dB = 15log_2OSR + 6(k-1) - 11.1 \qquad (4.1)$$

where OSR is the oversampling ratio and k is the number of bits of resolution in the quantizer. For a 1 bit (2 level) quantizer this formula gives an SNR limit of 108 dB for an OSR of 256(corresponding to say for a clock frequency f_s of 10 MHz and a signal bandwidth of 20 kHz).

In a passive sigma-delta modulator, the analysis of SNR is different from the

case of active loop-filter based sigma-delta modulators. In the former, the only source of loop-gain is the gain of the quantizer that needs to be calculated. The gain of the quantizer may be shown to be approximated by the reciprocal of the gain of the loop-filter at an input frequency of half the sampling rate f_s. The comparator gain may be considered to be uniform from 0 to π in the discrete-time frequency domain. For a second order system consisting of a cascade of first order non-interacting loop-filter stages (in which the second stage does not load the first) the gain of the quantizer can be shown to be,

$$G = \frac{1}{H(e^{j\pi})} \tag{4.2}$$

$$\approx \frac{\omega_s^2}{\pi^2 \omega_{p1} \omega_{p2}} \tag{4.3}$$

where $\omega_{p1}(= \frac{f_s C_{R1}}{C1})$ and ω_{p2} are the equivalent pole frequencies formed by the two stages and $\omega_s = 2\pi f_s$, where f_s is the sampling frequency.

Based upon the model presented in Fig. 4.1, for relatively low input frequencies ω comparated to the clock frequency, the loop-gain may be written as,

$$GH = \frac{\omega_s^2}{\pi^2 \omega_{p1} \omega_{p2} \left(1 + \frac{j\omega}{\omega_{p1}}\right)\left(1 + \frac{j\omega}{\omega_{p2}}\right)} \tag{4.4}$$

The quantization noise power spectral density expressed in $Volts/\sqrt{Hz}$ can now be shown to be,

$$\sqrt{N_{quant}} \approx \frac{\Delta}{|GH|\sqrt{f_s/2}} \tag{4.5}$$

$$= F \frac{\omega_{p1}\omega_{p2}\ \Delta}{\omega_s^{5/2}(1 + \frac{j\omega}{\omega_{p1}})(1 + \frac{j\omega}{\omega_{p2}})} \tag{4.6}$$

where F is a constant factor equal to 35.0 .

From equation (4.5), it is clear that for two non-interacting cascaded stages with identical pole frequencies and for relatively low signal bandwidths, the SNR is inversely proportional to the square of the ratio of the pole frequency to the sampling frequency. This trend is shown in Fig. 4.2. Though the equation for loop-gain is derived for non-interacting stages, simulation results show that this result is valid in general. The equation also shows a sensitivity of -20 dB per decade of pole frequency of each stage (-40 dB per decade for both poles moving together). As will be shown later in this chapter, this has important design constraints on the sizing of capacitors and the switches.

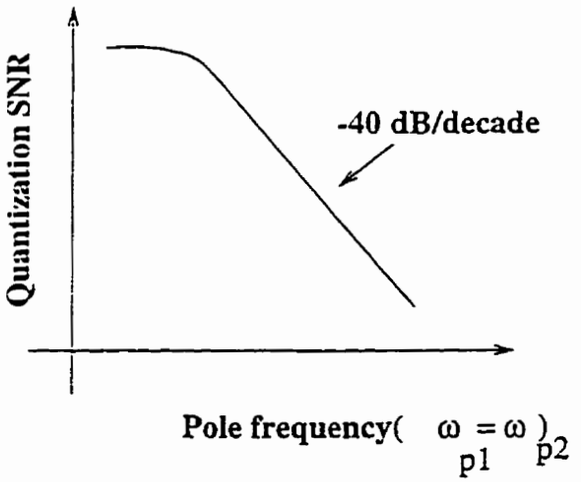


Figure 4.2: SNR vs. pole frequency for passive sigma-delta modulators

4.2.2 Effect of Comparator(Quantizer) Thermal Noise on SNR

The comparator thermal noise may be accounted for by assuming that the noise may be modeled as white noise of uniform spectral density and determining the equivalent input rms noise voltage v_{n-comp}. Assuming a 2 pole loop-filter as before, the noise power density referred back to the input of the modulator, can

now be shown to be,

$$\sqrt{N_{comp}} = \frac{v_{n-comp}|G|}{|1+GH|\sqrt{f_s/2}} \tag{4.7}$$

$$\approx \frac{v_{n-comp}}{\sqrt{f_s/2}}\left(1+j(\frac{\omega}{\omega_{p1}}+\frac{\omega}{\omega_{p2}})\right) \tag{4.8}$$

The above equation shows that when the effect of comparator thermal noise the SNR is inversely proportional to the sum of the pole frequencies. This trend is shown in Fig. 4.3. This is to be expected since for lower pole frequencies, the attenuation due to the loop-filter will be higher and therefore the noise due to the comparator when referred back to the input of the modulator will be higher.

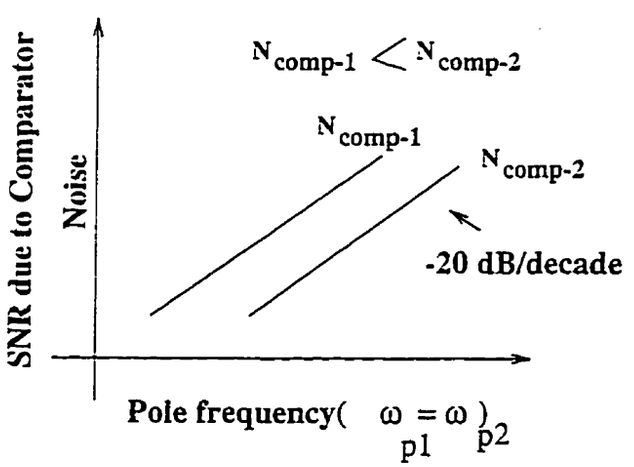


Figure 4.3: Effect of comparator noise on SNR in passive sigma-delta modulators

The total input referred noise PSD is given by,

$$N_{total} = N_{comp} + N_{quant}$$

Thus the SNR due to quantization noise and comparator noise may now be plotted as a function of the pole frequencies of the loop-filter as shown in Fig. 4.4. From this figure it is clear that for a given comparator rms equivalent thermal noise v_{n-comp} there is an optimal pole location at which $N_{comp} = N_{quant}$.

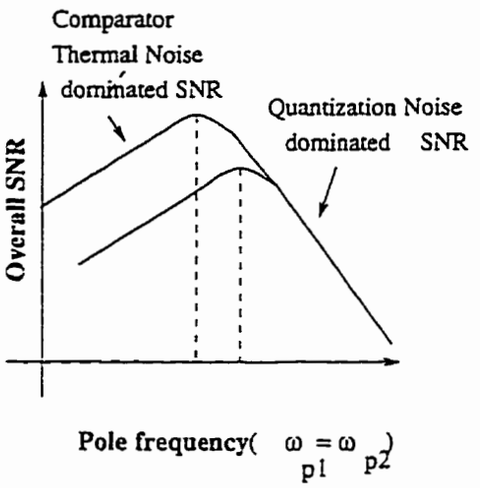


Figure 4.4: SNR in passive vs. pole frequency sigma-delta modulators

4.3 Design Considerations for High-speed Low-noise Comparators

The comparator of a passive sigma-delta modulator not only serves as a quantizer but also amplifies weak signals that result from the attenuation by the passive loop-filter. [1] Apart from quantization noise, two factors tend to introduce additional degradation of the weak signal. The first is due to noise generators in the devices of the comparator. The second source of degradation is the inability of the comparator to react to small changes in input signal especially at high speeds. These sources are not only tedious to analyze at the circuit level but additional difficulties arise in incorporating their effects at the sigma-delta modulator system level. This section will discuss important comparator design parameters that affect SNR degradations due to these factors and use a behavioral model that incorporates these parameters. The behavioral model will then be incorporated

[1] As will be shown in a later section, in this respect the comparator resembles the function of a low-noise amplifier of an RF front-end except that the input frequencies are about one-tenth of what are encountered in typical RF stages.

into a C program that can simulate important effects without taking recourse to circuit(Spice) simulations.

The noise generators in devices may be due to shot noise as in the case of base-emitter/base-collector junctions in BJT, thermal noise due to physical resistors within the devices or 1/f noise. They are dependent upon bias conditions such as bias current and are limited by the bandwidth of the signal path in the comparator. These noise sources are cumbersome to deal with analytically if the circuit consists of more than a few devices. A great deal of simplification may result if only the input stage is considered. Furthermore, as shown in [4], it is possible to model the effect of all noise sources with an equivalent voltage and current noise sources at the inputs of the comparator. This approach is adopted and for system level simulations of the modulator an equivalent input noise that is assumed white from 0 to $f_s/2$ is extracted from circuit simulation(Hspice) using .NOISE and .AC analysis.

4.3.1 Overdrive Recovery

A second important source of SNR degradation is the fact that the rms value of the signal at its input is very small, typically a few hundred microvolts. Therefore, the comparator may not be able to toggle from one cycle to the next with a change in the polarity of the input signal if the input signal is weak. This is due to the fact that the comparator internal nodes may have memory that may need to be reset and overdriven at every clock cycle. More often overdrive recovery problems are due to regenerative latch stages that are required for power efficient regenerative amplication of the weak signals. This problem is aggravated at higher clock frequencies at which the latch or its driving circuitry may be unable to respond. In order to overcome the previous state stored in the latch, it may be desirable to amplify the input signal first and then drive the latch. This is

accomplished by a preamplifier stage.

The effect of poor overdrive recovery on the modulator SNR is illustrated in Fig. 4.5. In the first half of every clock cycle, the latch output recovers to near midway between its latched voltages(+/- VLATCH) With a sufficiently large input signal, the latch is able to recover to its midway position soon enough to be able to toggle from its previously latched value as in cycles I and II. However, if the input level is small or the available settling time is not sufficient, as in cycle III and IV, the preamplifier output voltage may not be sufficient to overdrive the previous state of the latch. This results in a wrong code output that results in a tracking error and therefore SNR degradation.

The SNR degradation due to overdrive recovery depends primarily upon preamplifier gain, bandwidth, latch gain and the latch state voltage. Higher gain and bandwidth in the preamplifier help in the overdrive recovery because both help to overturn the state of the latch as its output decays from its (large) initial state. However, a higher preamp bandwidth may not necessarily be desirable because it may result in excessive noise being admitted through the preamplifier stage. Thus a critical part of the design is to be able to optimally design preamplifier gain, bandwidth and a latch stage volt. ge that results in the maximization of the SNR. However, in order to be able to do this, a behavioral model of the modulator that incorporates comparator noise and overdrive recovery error needs to be built and simulated.

4.3.2 Noise in BiCMOS Preamplifiers

In high-speed, low-noise applications, because of the problem of overdrive recovery in a latch, it may be necessary to preamplify the weak input signal with sufficient gain to drive the latch. Thus a low-noise preamplifier stage is critical. BiCMOS technology helps in the design of preamplifiers for these applications mainly

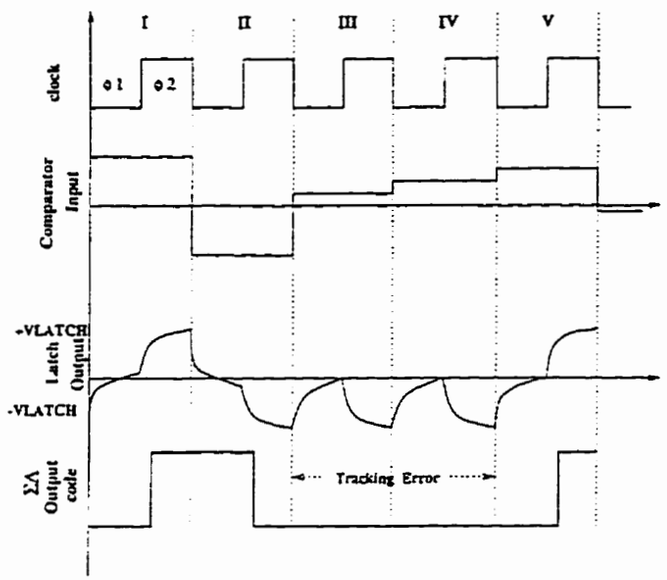


Figure 4.5: Effect of poor overdrive recovery in passive sigma-delta modulators

because of the use of a scaled BJT as a low-parasitic, low-noise and high-transconductance stage for small signals. The transconductance of a BJT is linearly proportional to current (I_c/V_T) whereas for a MOSFET it is proportional to the square root($\sqrt{2I_dK'}$). This may result in the available transconductance of an NMOS stage being an order of magnitude poorer for a given drain current than that for a BJT with the same collector current. However, as will be shown later the shot noise of a BJT causes the equivalent input noise of the BJT input comparator to exceed that of an NMOS input comparator. A secondary complication is that at low clock frequencies, the base current may leak off charge provided by the capacitors connected to the output node of the loop-filter and therefore reduce loop-gain. For these reasons a BJT cannot be used directly at the input of a comparator. Instead an NMOS/PMOS source follower is used as a buffer stage to drive a BJT emitter-coupled pair that provides the bulk of the gain required for the preamplifer.

A BiCMOS preamplifier using NMOS input is shown in Fig. 4.6. The source

follower M1-Ibias (M2-Ibias) provides the buffering necessary for a capacitively driven input. Its gain is less than unity because of the finite input impedance looking into the base of Q1/Q2 causes source-degeneration. However, by increasing the transconductance of M1 the gain may be brought to a reasonable value close to unity without incurring area or input capacitance penalty. The gain of the emitter-coupled stage is $g_{m-Q1}R_1$ and depends on the overdrive recovery requirements set by the latch stage following the preamplifier stage. It is set typically in a range from 30 - 100. A shorting switch connected to the output nodes serves to reset the node at the end of the preamplification phase (i.e. during phase ϕ_2) and helps in improving the SNR due to overdrive recovery errors.

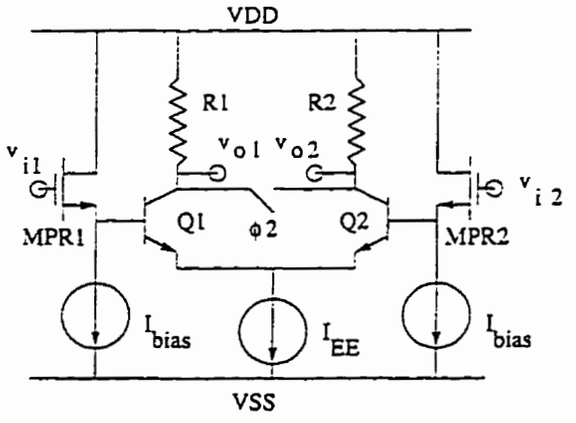


Figure 4.6: An NMOS input preamplifier

Noise Analysis of the Preamplifier

The dominant sources of noise in the preamplifer are the thermal, shot and 1/f noise of M1/M2, the thermal noise of the base-spreading resistance of Q1/Q2 and the collector shot noise of Q1/Q2. The equivalent input noise of the stage may be found by drawing the small-signal equivalent circuit shown in Fig. 4.7. R_{sw} is the on resistance of switches M7 and M8 of the loop-filter in Fig. 4.11. If flicker noise of the M1/M2 are ignored, the equivalent input noise power density and equivalent

input noise voltage are determined as,

$$N_{comp} = 8kT\left(\frac{2}{3}\left(\frac{1}{g_{m-M1}}+\frac{1}{g_{m-Mbias}}\left(\frac{g_{m-Mbias}}{g_{m-M1}}\right)^2\right)\right) + 8kT\left(r_{bb-Q1}\left(\frac{\left(1+g_{m-M1}r_{\pi-M1}\right)}{g_{m-M1}r_{\pi-M1}}\right)^2+R_{sw}\right) \quad (4.9)$$

$$v_{n-comp}^2 = N_{comp}f_{NBW} \quad (4.10)$$

The the equivalent input noise bandwidth, f_{NBW}, is

$$f_{NBW} = \frac{1}{4\pi R1 C_{pr}}$$

for a 1 pole model approximation where C_{pr} is the sum total of all capacitances looking into the output node. From equation (4.9) it is clear that the comparator equivalent input noise may be most effectively reduced by

- Increasing g_{m-M1} which results in increased power dissipation
- Reducing $g_{m-Mbias}$ by decreasing its size
- Reducing r_{bb-Q1} by choosing Q1 with large emitter area
- Reducing the equivalent bandwidth, f_{NBW} by increasing C_{pr}

4.3.3 Behavioral Model

A simple behavioural model of the sigma-delta modulator that can simultaneously model the effects of poor overdrive recovery and noise in single-stage comparators is shown in Fig. 4.8. The model takes into account the finite bandwith in the signal path upto the point of decision making of the latch during the preamplification phase(ϕ_1 (shown in Fig. 4.5) by a single time constant τ_{pr}. Since

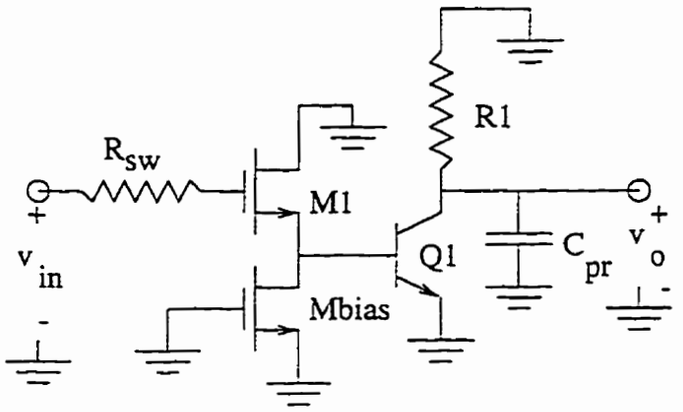


Figure 4.7: Equivalent circuit of an NMOS input preamplifier

the circuit is linear, the two effects add up to result in a net positive or negative voltage which decides the state of the latch. The gain of the comparator upto the decision point(output node of the latch) is modeled by the DC gain of the circuit upto the decision making point. During the preamplification phase, the input signal is amplified with a time constant τ_{pr} while the latch decays to its midway point also with time constant τ_{pr}. During the latching phase any small positive(negative) voltage that may develop at the decision point causes the output to latch to $+VLATCH(-VLATCH)$.

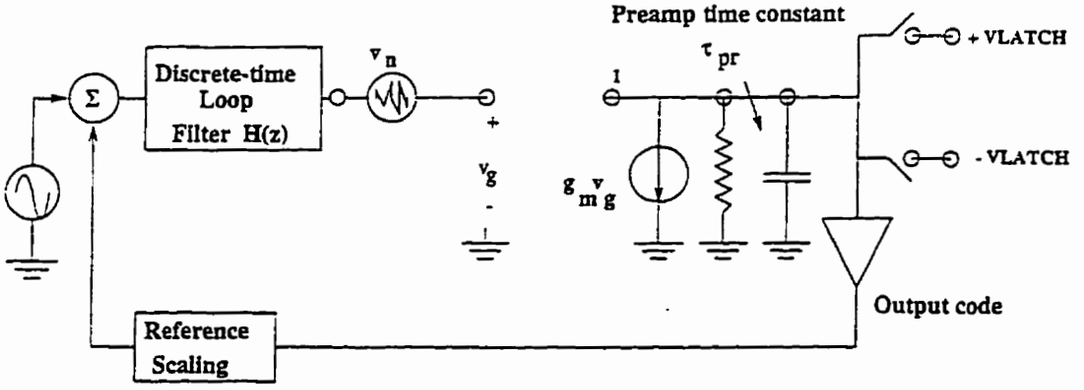


Figure 4.8: Behavioral model of sigma-delta modulator with o.d. recovery model

The model described above has been incorporated into a C program that

simulates the behaviour of a passive sigma-delta modulator. The effect of finite bandwidth has been included by an explicit evaluation of the transient waveform at the decision node(latch output) with the initial condition being the state of the latch in the previous clock cycle. The effect of bandwidth limiting seen by the equivalent input noise of the comparator has also been incorporated. It may be seen that the effect of available preamplifier settling time(T_{pr}) and finite bandwidth due to time constant τ_{pr} can be incorporated by a single normalized parameter equal to their ratio(T_{pr}/τ_{pr}). Some options such as comparator input reset, finite input capacitance and input offset have also been included. For the cases in which latching occurs in a stage separate stage following the preamp stage, it is easy to extend the model described above by proper scaling of the preamplification and overdrive recovery effects.

Simulation Results

As expected, both finite gain and bandwidth have a significant effect on the modulator SNR. The variation of SNR with finite gain is shown in the plot of Fig. 4.9 for the cases of moderate bandwidths. The SNR of the comparator increases with gain because the SNR is overdrive recovery error limited. Thus a larger gain results in larger preamplification and therefore the latch is able to recover from its previous state with smaller input levels. For very low gains the modulator becomes unstable and therefore the SNR degrades rapidly. At very large bandwidths, the SNR is almost independent of gain. Here the SNR is limited by comparator noise and/or quantization noise. Overdrive recovery errors are small because the comparator is able to recover from its state in the previous cycle almost instantaneously. A larger gain does not help since both signal and noise are amplified by the same amount.

The plot in Fig. 4.10 shows the variation of the SNR with bandwidth for two

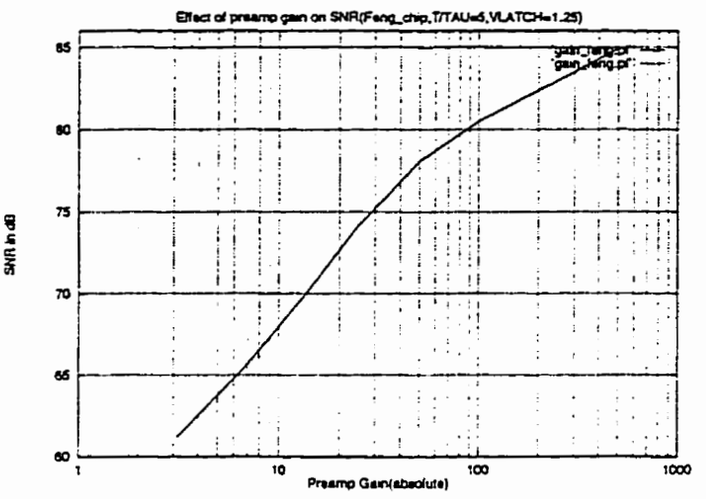


Figure 4.9: SNR variation with gain for moderate and high bandwidth

values of comparator equivalent input noise power density for a given loop-filter topology. The -3 dB/octave SNR degradation with preamplifier bandwidth. (as shown by the -3 dB/octave trend curve) is expected since a doubling in the bandwidth results in a doubling of noise power admitted and therefore SNR degradation of 3 dB. The rapid fall-off in the SNR for low bandwidths is due to the comparator being unable to recover from its previous latched state owing to the slow decay of the initial condition at the latched voltage during the preamplification phase. Thus an optimal bandwidth exists for which both the overdrive recovery error and total noise power admitted are small.

4.4 Design Considerations for the Passive Loop-filter

4.4.1 Second-order Loop-filter Capacitor Ratio Design

The design of loop-filters of arbitrary order for a passive sigma-delta modulator is complicated. The formulae developed for the SNR in section 4.2.1 and 4.2.2 may no longer be valid and input range and stability issues may become serious. For

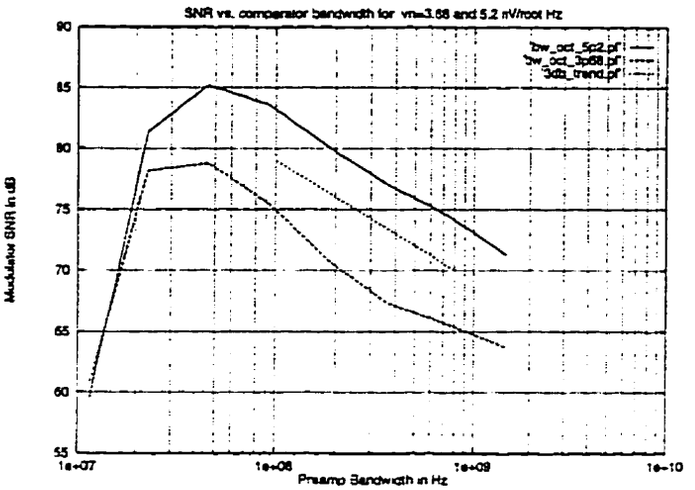


Figure 4.10: SNR variation with bandwidth

the second-order modulator , filter synthesis programs may be used to compute capacitor ratios required based on criteria such as the SNR for a given OSR, comparator equivalent input noise (v_{n-comp}), maximum capacitor area, capacitor ratio spread etc. The design of the loop-filter would then follow an iterative procedure illustrated in Fig. 4.21.

Fig. 4.11 shows a single-ended switched-capacitor loop-filter implementation of the passive sigma-delta modulator. Capacitors C_{R1} and C_{R2} which are switched capacitors and analogous to resistors R1,R2, respectively in Fig. 4.1. Capacitor C_{R0} and C_2 form the high-frequency zero that helps to improve loop stability analogous to the role of Rz and C2 in Fig. 4.1. The clock and data output waveforms are shown in Fig. 4.12. The complete loop-delay from the loop-filter feedback path to the comparator output is one sample period. Switches M1 and M5 may be a conventional bottom-plate sample-and-hold circuit if the input is a baseband signal. If the input is an IF signal they may form a part of the bottom-plate sampling mixer. If so, their design will proceed according to criteria developed in chapter 4.

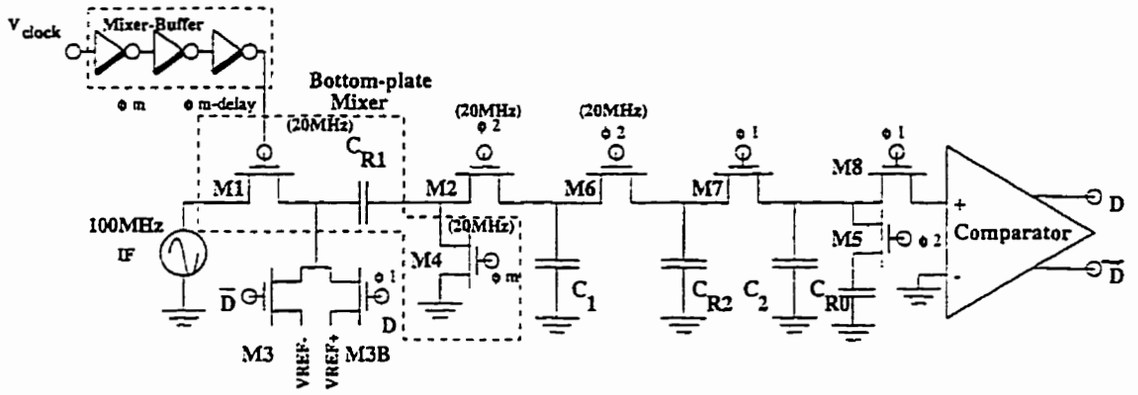


Figure 4.11: Passive sigma-delta modulator(single-ended)

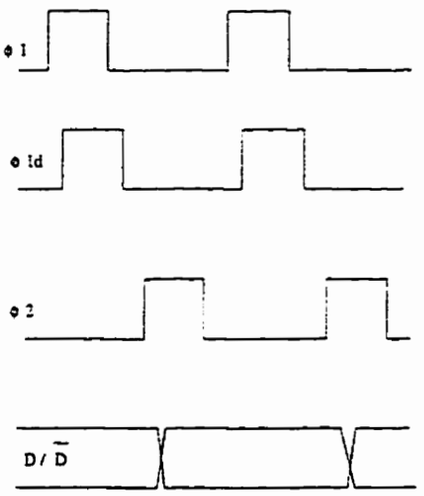


Figure 4.12: Clock timing for a passive sigma-delta modulator

4.4.2 Estimation of Thermal Noise due to Loop-filter Switches

The thermal noise due to the switches of the loop-filter network constrain the minimum values of the loop-filter capacitors. This noise may be calculated by the following procedure,

- Identify each circuit path for which noise may be sampled onto a capacitance.
- Calculate the total capacitance seen in such a path Cp_i.

- Simplify the discrete-time circuit and its transfer function
- Determine the discrete-time frequency transfer function $Hs_i(e^{j\theta})$ for the noise voltage in each path to the output of the loop-filter

The noise variance at the output of the loop-filter can be shown to be the sum of contributions of the noise variance due to P paths, each of which may be calculated using the discrete-time equivalent of the Paley-Wiener criterion [19]:

$$v_{n-switch}^2 = \sum_{i=1}^{P} \frac{kT}{Cp_i} \int_{-\pi}^{\pi} \left| H_{s_i}(e^{j\theta}) \right|^2 d\theta \tag{4.11}$$

For the loop-filter topology chosen, five noise circuit paths are identified. These are enumerated below.

1. H_{s_1} : M1- C_{R1} - M4 during ϕ_1 with $Cp_1 = C_{R1}$
2. H_{s_2} : M3/M3B- C_{R1} - M2 - $C1$ during ϕ_2 with $Cp_2 = \frac{C_{R1}C_1}{C_{R1}+C1}$
3. H_{s_3} : $C1$ - M6 - C_{R2} during ϕ_2 with $Cp_3 = \frac{C_{R2}C_1}{C_{R2}+C1}$
4. H_{s_4} : C_{R2} - M7 - C_{R0} during ϕ_1 with $Cp_4 = \frac{C_{R2}CR0}{C_{R2}+CR0}$
5. H_{s_5} : C_{R0} - M7 - $C2$ during ϕ_2 with $Cp_5 = \frac{C_{R0}C_2}{C_{R0}+C2}$

M1-M4 during ϕ_1: For this path the transfer function is the same as the open-loop transfer-function of the loop-filter. It is determined to be,

$$H_{s_1}(z) = \frac{z^{-1}bC_{R1}(d - C_{R0}z^{-1})}{ed - (dC_1 + eC_{R0} + bdC_{R2} + aeC_{R0})z^{-1} + (C_1C_{R0} + bC_{CR2}C_{R0} + aC_{R0}C_1)} \tag{4.12}$$

where $z = e^{j\theta}$ and

$$a = \frac{C_{R0}}{C_{R0} + C_{R2}} \tag{4.13}$$

$$b = \frac{C_{R2}}{C_{R2} + C_{R0}} \tag{4.14}$$

$$e = C_{R1} + C_{R2} + C_1 \tag{4.15}$$

$$d = C_2 + C_{R0} \tag{4.16}$$

$$f = C_{R0} + C_{R2} + C_1 \tag{4.17}$$

The transfer function for path 2 is the same as the path 1 except for a slight change in C_{p_2} from C_{p_1}. The output noise variance contributions due to all the other paths are similarly calculated after determining their corresponding transfer functions and using the integral equation (4.11). It may be noted that noise due to M7 is contributed both directly in the continuous-time sense as well as in the sample-and-held sense as charge stored in $C_{R2}/C2$. The continuous-time component of the noise may be taken into account by lumping it with the comparator equivalent input noise.

4.5 Effect of Junction Parasitics: Switch Sizing

From a settling viewpoint, it may be desirable to increase the size of the switches of the switched-capacitor loop-filter network so that the gain error resulting from a finite voltage drop across the switch may be minimized. In section 4.2.1, it was shown that the quantization SNR has a sensitivity of 6 dB to an octave change in pole frequency. Apart from charge injection considerations, this sensitivity has an important constraint on the maximum switch size since the junction capacitances of the source/drain to substrate junctions may shift the pole locations significantly, especially if the capacitors of the switched-capacitor network are small.

Fig. 4.13 shows a switched-capacitor implementation of the first-order RC

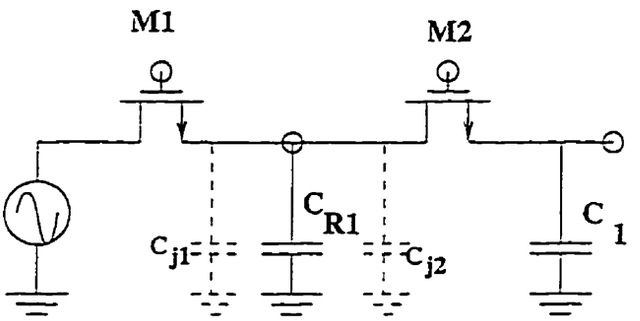


Figure 4.13: Junction parasitics of a first-order switched-capacitor section

section R1-C1 of Fig. 4.1. To compute the maximum switch size, we first note that in the low-frequency approximation model,

$$\omega_{p1} = \frac{1}{R1C1} = f_s \frac{C_{R1}}{C1}$$

Since the pole frequency ω_{p1} is small as compared to the clock frequency, C_{R1} becomes much smaller than $C1$. The actual size of C_{R1} may be determined from distortion consideration to be very small. Since, as shown in equation (4.5), the quantization SNR is inversely proportional to ω_{p1}, the junction parasitics due to transistors M1, M2, C_{j1}, C_{j2} become important. Therefore,

$$\frac{\delta SNR}{SNR} = -\frac{\delta C_{R1}}{C_{R1}} \tag{4.18}$$

From the above equation, for a 2 dB SNR degradation, it may be shown that the maximum allowable fractional change in C_{R1} is $\frac{\delta C_{R1}}{C_{R1}} = 0.25$.

4.6 Comparison of PMOS, NMOS and BJT Input Stages

A comparison of preamplifier stages with NMOS,PMOS and BJT input transistors with respect to the equivalent input noise voltage is useful. NMOS input stages

have an advantage over PMOS input stages in that they offer a larger transconductance for the same bias current. However, 1/f noise in the former is poorer. So the total equivalent input noise (v_{n-comp})depends upon the noise bandwidth over which these noise components are integrated. Typical equivalent input noise is plotted in Fig. 4.14 for a PMOS and an NMOS input stage with the same device size and bias current. The PMOS stage has a thermal noise floor of 4.97 $nV/\sqrt{Hz}$ whereas the NMOS stage has a thermal noise floor of 4.32 $nV/\sqrt{Hz}$ It is clear that over a sufficiently large noise bandwidth the thermal noise component may ultimately dominate over the 1/f component.

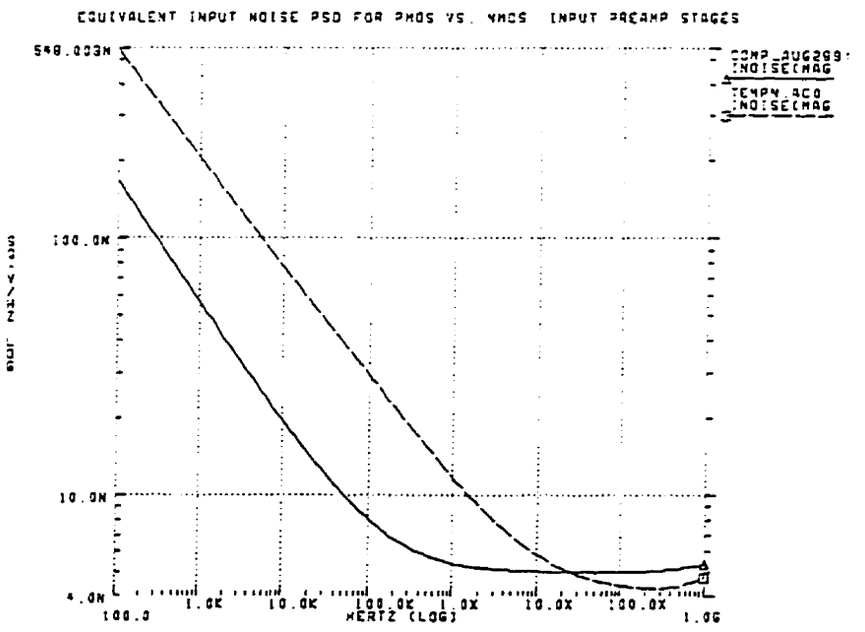


Figure 4.14: Equivalent input noise for PMOS and NMOS input preamplifers

Effect of base current shot noise

A more relevant comparison for a BiCMOS technology is between NMOS and BJT input stages. The finite base current may pose the problem of discharging the capacitors connected to the output node of the loop-filter. This problem however may not be serious and in any case may not be an issue at high enough clock frequencies when the charge from the loop-filter is refreshed more frequently. A more fundamental limitation comes because the noise model for a BJT differs from that of an NMOS in that the former has a significant equivalent input current noise [4]. This noise component, which is due to base current shot noise, causes a voltage drop at the base when the impedance looking into the source is large. This is the situation when the input BJT transistor is connected to the output of the loop-filter of the modulator. The effect of the equivalent input current noise will be calculated by determining the total input voltage variance developed at the base v^2_{shot}. This will be compared with the variance of the equivalent input voltage noise due to collector current shot noise .

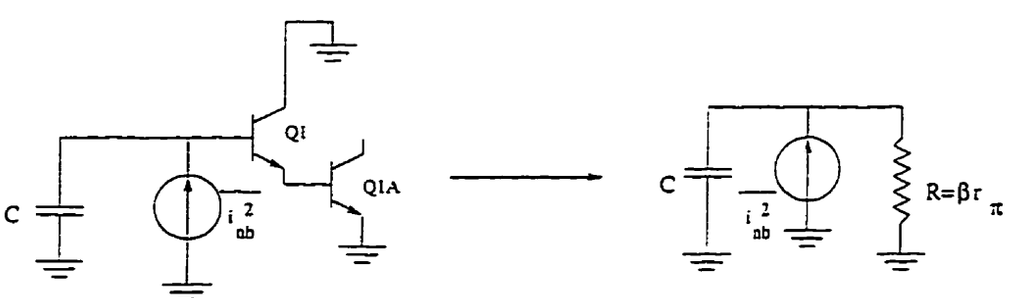


Figure 4.15: Shot noise model for a BJT input preamplifer

Fig. 4.15 shows the input stage of a Darlington-pair type input for a preamplifier and the shot noise component of its equivalent input noise current.

$$N_{i-shot-base} = \frac{\overline{i_{n-b}}^2}{\Delta f} = 2qI_b \tag{4.19}$$

$$N_{v-shot-base} = \frac{\overline{v_{n-b}}^2}{\Delta f} = 2qI_bR^2 \tag{4.20}$$

Assuming that the series base resistance r_b is negligible, the ratio of the equivalent input noise due to base shot noise to that due to collector shot noise can now be shown to be,

$$\frac{N_{v-shot-base}}{N_{v-shot-coll}} = \frac{3}{4}\left(\frac{I_b R}{V_T}\right) g_m R \tag{4.21}$$

where $V_T = \frac{kT}{q}$

From equation (4.21) it is clear that the component of equivalent input noise voltage PSD developed at the base due to base current shot noise may be very significant for large R as would be the case for a Darlington pair input. The factor inside the bracket will be approximately 10 for an $I_b = 1\ \mu A$ and $R = \beta r_\pi = 250\ k\Omega$ for $\beta = 100$ and $r_\pi = 2.5k\Omega$ where r_π is the small-signal input impedance of the common-emitter transistor Q1A and β is the current gain of Q1. However, the total noise voltage developed due to the shot noise component will be band-limited by the low-pass filter formed by resistor R and capacitor C looking into the output node of the loop-filter, This is shown in Fig. 4.16. The noise due to other sources such as collector shot noise and series base resistance is also shown at a PSD level (N_{BJT}). The total integrated noise at the base for a noise bandwidth of $f_{NBW} = \frac{1}{4RC}$ is calculated to be,

$$v_{shot}^2 = \frac{qI_b R}{2C} \tag{4.22}$$

Equation (4.22) shows that for a relatively large input impedance, R and for relatively small noise bandwidths, the shot noise component of the total comparator noise may dominate over other sources of noise and may be larger than that of an NMOS preamplifier biased with the same drain current.

A Darlington-pair (D.P.) based preamplifier stage shown in Fig. 4.17 was simulated for noise analysis. The inductance L serves as an AC open-circuit, but biases the

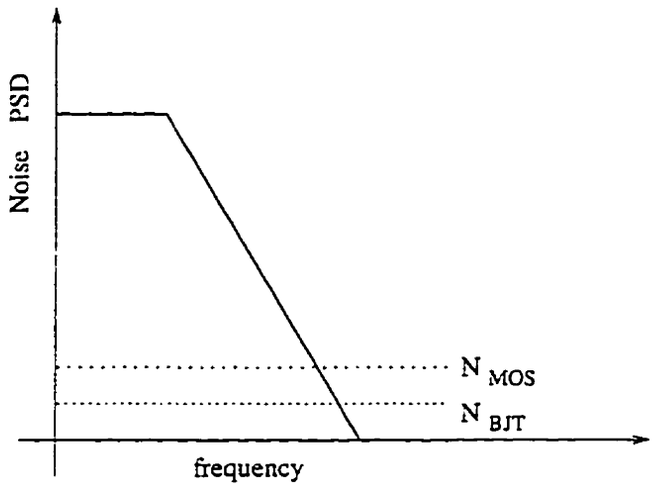


Figure 4.16: Equivalent input noise PSD of a BJT input preamplifer

base input to a desired DC voltage V_B so that Q1 is biased for 100 μA DC collector current. The capacitor C serves as an AC short. The BJT have sufficiently large area so that the collector and base shot noise components dominate over the thermal noise component due to series base resistance. The noise referred back to v_{in} is plotted and compared with a similar stage with Q1 replaced with an NMOS transistor as shown in Fig. 4.18. This NMOS transistor is biased with a smaller transconductance than the input BJT of the Darlington pair. Note at sufficiently high frequencies at which thermal noise dominates, the input referred noise is determined by the transconductance of the respective devices. Then the equivalent input noise PSD for the NMOS preamplifier is larger than the D.P. preamplifier.

For relatively low frequencies upto about 1 MHz, the equivalent input noise voltage for the D.P. preamplifier is dominated by the base current shot noise which slopes off at -20 dB/decade with frequency as expected from the R-C low-pass filter formed at the input. For the NMOS preamplifer, noise is dominated by the 1/f noise which has a smaller PSD and different PSD slope than the former case.

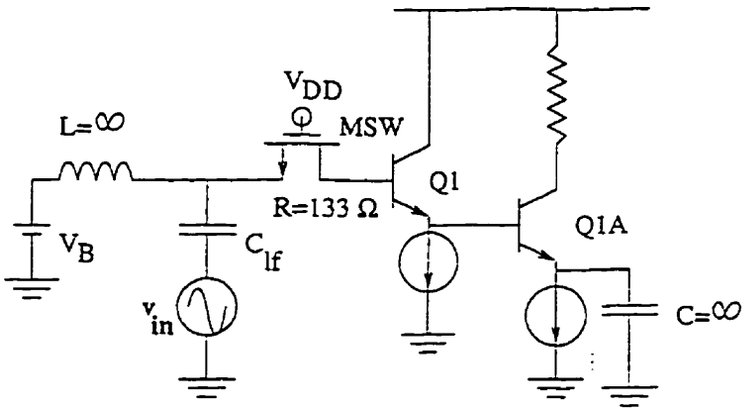


Figure 4.17: A Darlington-pair input preamplifer

At higher frequencies, the collector current shot noise component is expected to dominate over the base shot noise component for the D.P. preamplifier which results in the flattening out of the PSD curve. In the case of the NMOS preamplifier, the thermal noise should dominate over 1/f noise and as expected, the noise PSD exceeds that for the D.P. case. If the equivalent input noise is integrated from 10 KHz to 100 MHz, it is found to be 74 μV for the NMOS and 1.07 mV for the D.P. preamplifiers. Thus these simulations clearly show that having a BJT input preamplifier is not desirable when the input source is capacitive and the noise bandwidth is small.

Some interesting qualitative comparisons may be made between the signal processing in comparator for passive $\Sigma - \Delta$ modulator and the RF processing circuits such as LNA especially as it relates to noise. Both circuits process weak signals that are susceptible to circuit noise. RF circuits require sources with source impedances that should be optimum for minimum Noise Figure. As shown in section 4.6, a BJT input preamplifier cannot be driven by a capacitive source as is the case when loop-filters are based upon passive switched-capacitor circuits. This is analogous to the case when LNA's with small input impedance are driven with sources with large source impedance(which may be resistive or reactive type) in

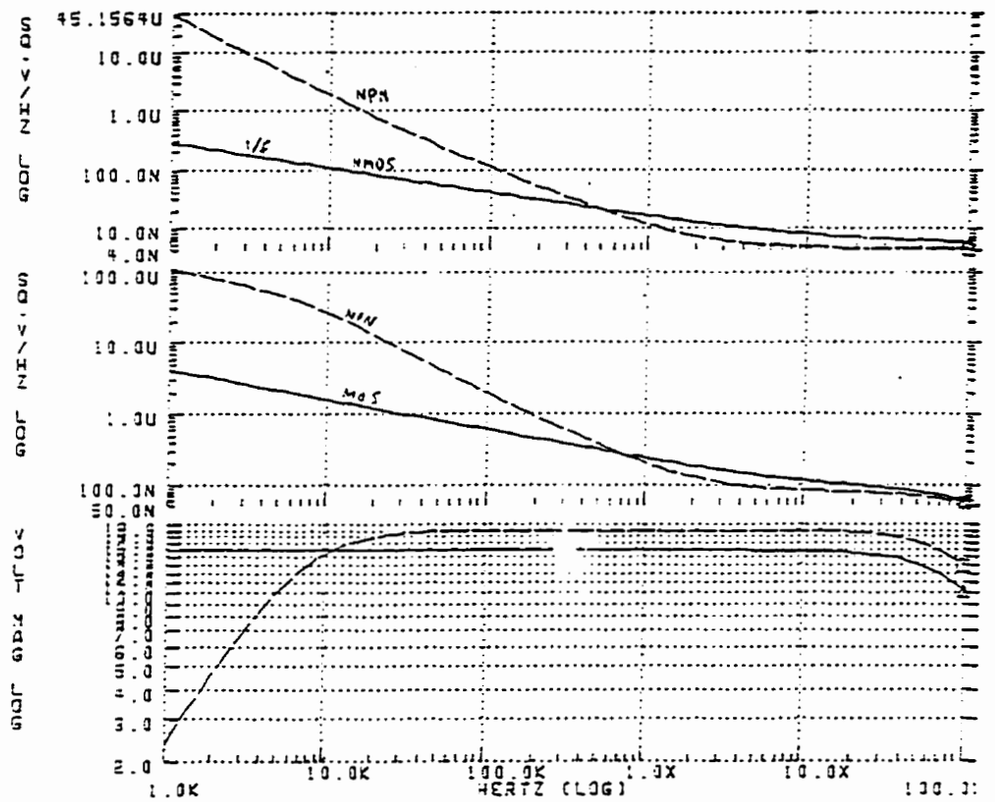


Figure 4.18: Comparison of eq. input noise PSD in NMOS/BJT input preamp.

which case the noise performance is likely to be poor.

One of the differences between the two circuits is in the method of processing of wide-band circuit noise. In the comparator circuit, the preamplifier amplifies the input signal and also introduces wide-band noise that can be represented by an equivalent input noise with PSD N^2_{comp}. This noise is filtered by the pole(s) of the preamplifier circuit. Fig. 4.19 shows the model of comparator for noise analysis. The preamplifier gain is modeled by a gain block. The band-limiting of wide-band noise is represented by an ideal low-pass filter with cutoff frequency at f_{cutoff}. The sampling switch models the latch decision node. If the cutoff frequency of the low-pass filter formed by the preamplifier is less than half the sampling frequency, the comparator equivalent input noise PSD is N^2_{comp}, the noise PSD of the

preamplifier. On the other hand, as shown in Fig. 4.20, if the cutoff frequency of the low-pass filter exceeds this frequency, the noise spectrum above half the sampling rate will fold over into the Nyquist bandwidth, resulting in the equivalent input noise to exceed N^2_{comp}. This phenomenon is analogous to aliasing of wide-band noise for the sampling mixer discussed in chapter 2. It may also be noted that though the aliasing effect of wide-band does occur in active loop-filter based sigma-delta modulators, its effect is not important since the signal power at the comparator(quantizer) input is much larger than in the active case.

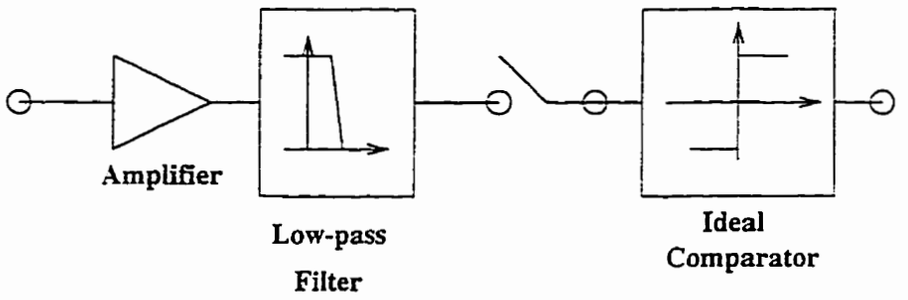


Figure 4.19: Comparator model for passive sigma-delta modulator

4.7 A Design Roadmap

A design roadmap shown in Fig. 4.21 assists in the design of the loop-filter and a BiCMOS preamplifier given the SNR,bandwidth, power dissipation, power supply voltage and technology criterion. The roadmap assumes that the oversampling ratio is determined mainly from the quantization SNR requirements. The design starts from the minimum OSR requirement from equation (4.1) and a relaxed budget for comparator power. The two iterative loops shown optimize for $v_{n-quant}$ and v_{n-comp} until the two are equal and the power budget constraints are met. Equations (4.9) and (4.10) govern the optimization for v_{n-comp}.

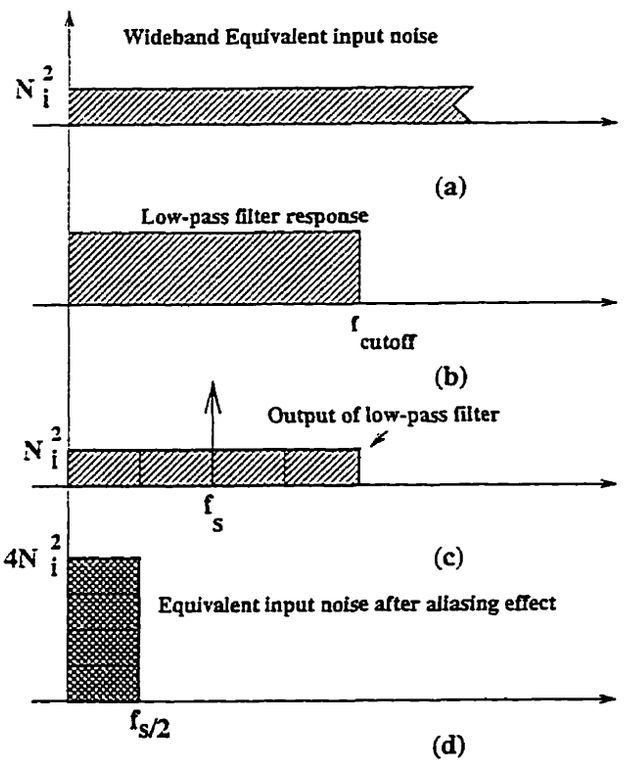


Figure 4.20: Aliasing effect of preamplifier noise at latch decision node

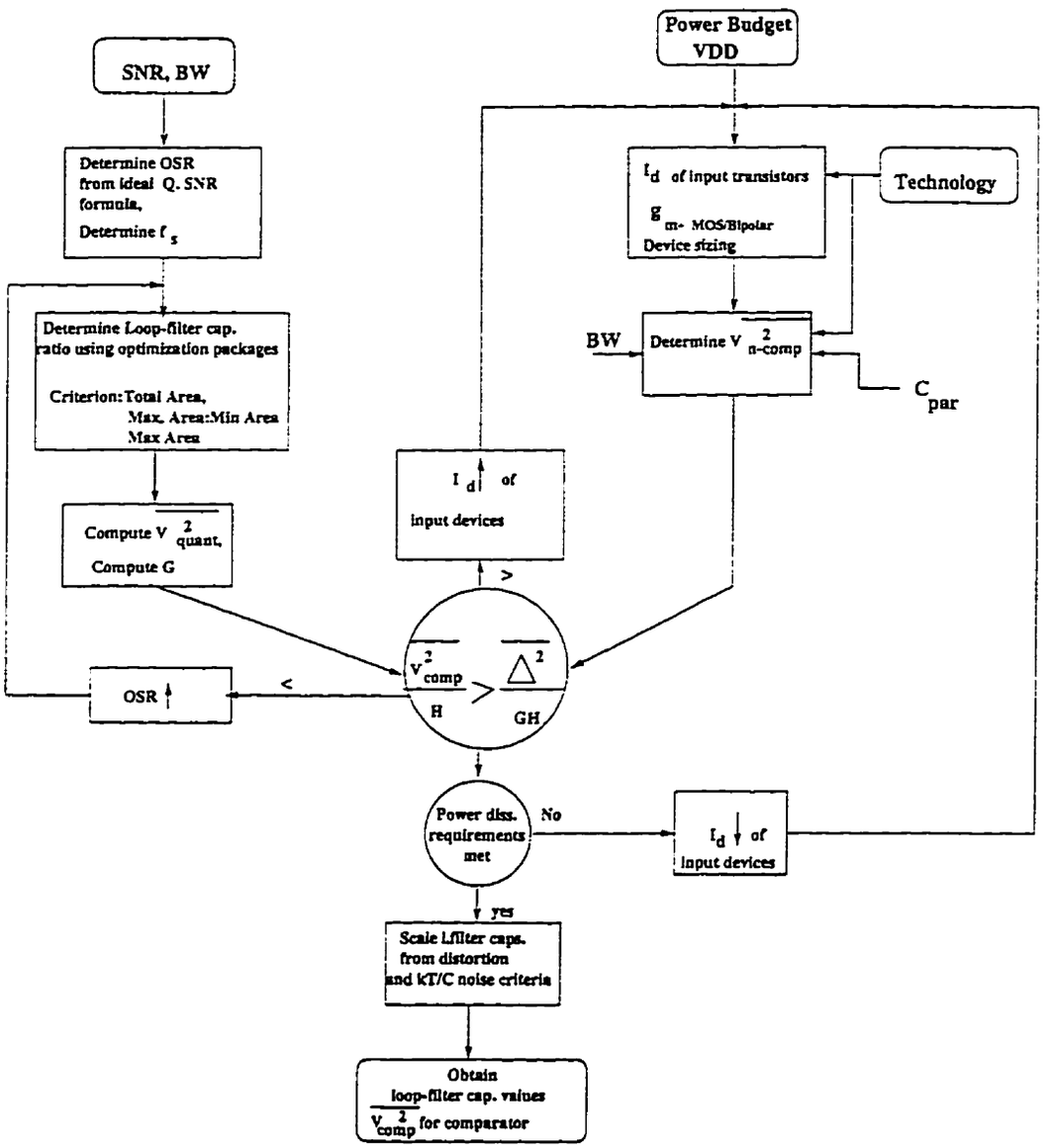


Figure 4.21: Roadmap for design of passive sigma-delta modulator

Chapter 5

Prototype Design and Measurement Results

In chapter 3 the distortion in a sampling mixer was analyzed and formulae for distortion in a bottom-plate sampling mixer were derived. Chapter 4 discussed the effect of noise due to devices in the comparator and loop-filter on the SNR of the passive sigma-delta modulator. The effect of overdrive recovery errors due to finite preamplifier gain and bandwidth were also discussed through behavioural level simulations. In this chapter the design and measurement results of a prototype digitizer for 100 MHz IF input implemented in a 0.8 μm BiCMOS technology is presented.

5.1 Prototype Design

The complete block level architecture of the prototype designed is shown in Fig. 5.1. The blocks that lie in the signal paths architecture, including the sampling mixer, the loop-filter and the comparator are completely differential from the input to the output. This symmetry is carried over to layout. This reduces all second

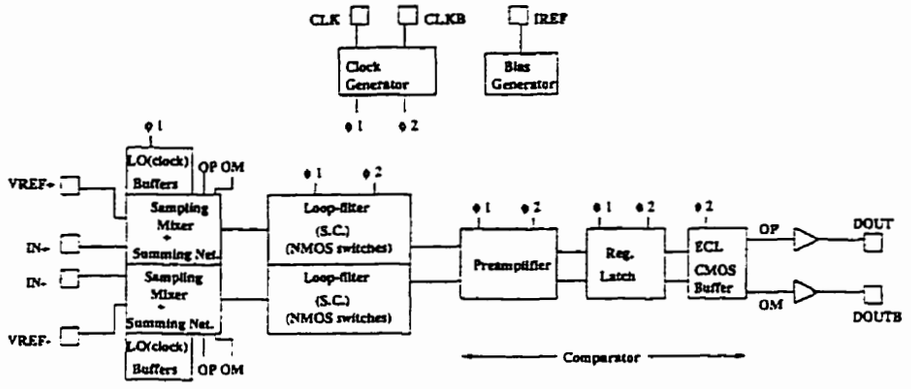


Figure 5.1: Block level architecture of the prototype IF digitizer

order distortion in the sampling mixer and the sigma-delta modulator by factors which are related to parameter mismatch. For example, a mismatch in K' of 1 % is expected to reduce the second harmonic distortion by 40 dB from its single-ended value.

The starting specifications of the optimal design are an SDNR of 78 dB for a bandwidth of 40 kHz. The optimal design of the loop-filter and comparator preamplifier follow the iteration procedures outlined in Fig. 4.21. This leads to a $v_{n-comp} = v_{n-quant} = 93\ \mu V$.

5.1.1 Sampling Mixer

Sampling Mixer top-switch size: $W/L = 102\ \mu m/0.8\ \mu m$, $K' = 0.0138\ A/V^2$.
Bottom-switch size: $W/L = 17\ \mu m/0.8 \mu m$, Sampling capacitance ($C_{r1}$): 0.2 pF

A $V_{GS} = 3\ V$, $V_B = -2\ V$ has been assumed.

Assuming that the sampling mixer is operating in the time-invariant distortion dominated region, the distortion may be calculated from equations (3.35,3.36, 3.38) and 3.55(to include body effect) to be,

$$HD_2 = -62.3\ dB,\ HD_3 = -84.1\ dB,\ IM_3 = -84.1\ dB$$

5.1.2 Loop-filter

The single-ended architecture of the loop-filter is shown in Fig. 4.11. The loop-filter has been implemented using NMOS switches. This helps to improve the speed of the basic sigma-delta modulator over a CMOS switch based design by reducing the junction parasitics at the various nodes of the loop-filter. It also greatly simplifies layout by eliminating the placement and routing of PMOS transistors and their clock signals. The loss of dynamic range is not important since the signal levels at the various nodes of the loop-filter are less or equal to the rms level of the input signal which is 0 dBm or 0.316 V.

Loop-filter Capacitor Ratios

The optimal capacitor ratios are shown in Table 5.1.

C_{R1}	2	0.2 pF
C_1	300	30 pF
C_{R2}	1	0.1 pF
C_{R0}	66.6	6.66 pF
C_2	37.5	3.75 pF

Table 5.1: Capacitor ratios for prototype design

Loop-filter Switch Size

The size of loop-filter switch sizes M6-M7 are obtained from equation (4.18). Assuming a worst case SNR degradation of 2 dB, $\frac{\delta C_{R2}}{C_{R1}} = 0.25$. For a nominal $C_{R1} = 0.1\ pF$, $C_{j6} = C_{j7} = 12.5\ fF$. From the junction capacitor sensitivity data given in Table 2.1.1 $\frac{\Delta C_j}{\Delta W} = 1.5 fF/\mu m$. The widths of transistors M6 and M7 are calculated to be,

$$W_{M6} = W_{M7} = \frac{25fF}{2 \times 1.5\ fF/\mu m} = 8.5\ \mu m$$

Switch Thermal Noise

The noise contributions for each noise path described in section 4.4.2 is determined by numerical integration and shown in Table 5.1.2. The total rms noise due to thermal noise in switches is determined to be $39.2\mu V$ for the set of capacitor data shown in Table 5.1.

Path	Integral	$v^2_{ni-switch}$ in V^2
1	0.01	2.07 e - 10
2	0.01	2.08 e - 10
3	0.00114	0.474 e - 10
4	0.01719	7.310 e - 10
5	0.1998	3.45 e - 10
Total		15.4 e - 10

Table 5.2: kT/C Noise summary

5.1.3 Comparator Design

The complete schematic of the BiCMOS comparator is shown in Fig. 5.2. It consists of a preamplifier, regenerative latch, ECL-CMOS converters, bias circuit and buffers/pad drivers. The device sizes are given in Table 5.3 and the bias currents of the preamp and latch are given in Table 5.1.3.

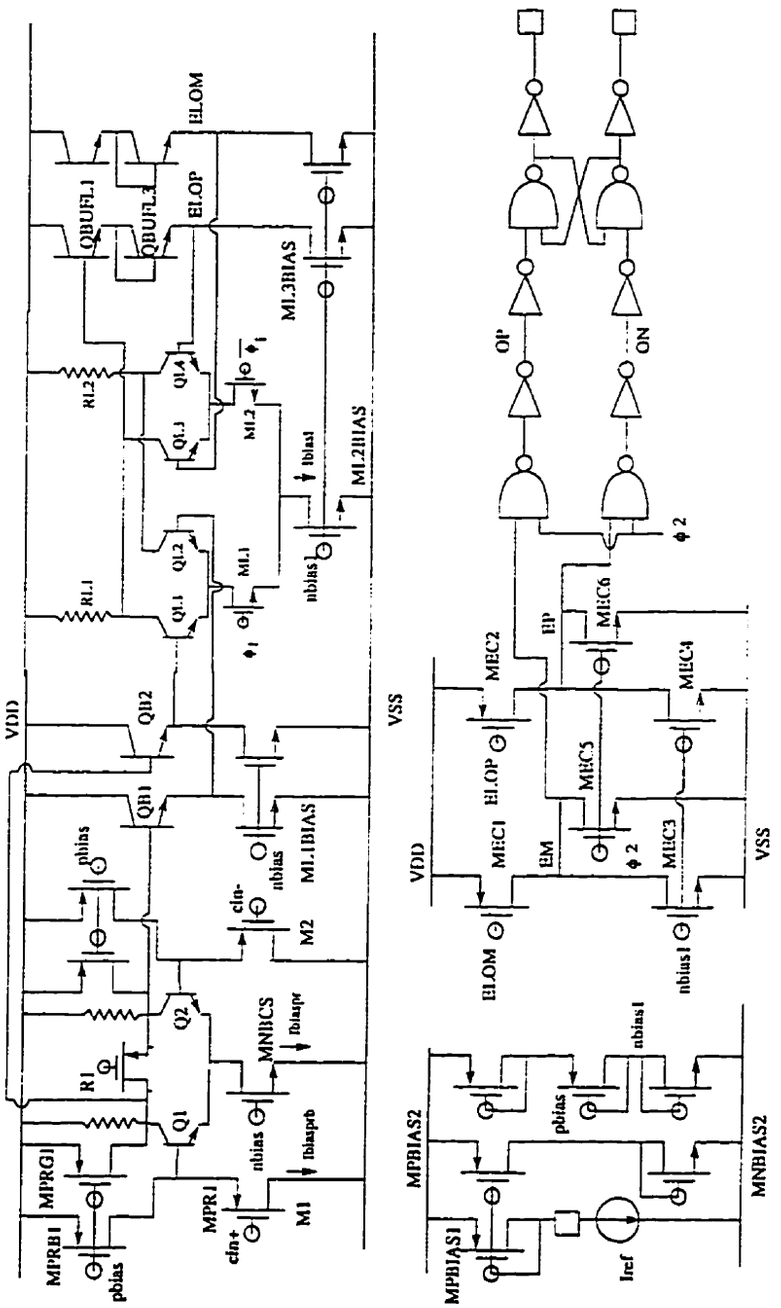


Figure 5.2: Complete BiCMOS comparator schematic

Preamplifier

For the designed operating point of the preamplifier, $g_{m-MPR1} = 1.884\ mA/V$, $g_{m-MPRB1} = 0.464\ mA/V$, $r_{bb-Q1} = 83.2\ \Omega$, $r_{\pi-Q1} = 23.9\ k\Omega$, $g_{m-Q1} = 3.78\ mA/V$, $R_{sw} = 0$. From equation (4.9) an equivalent input noise PSD of $\sqrt{N_{comp}} = 4.8\ nV/\sqrt{Hz}$ is obtained. The value obtained from Hspice is 5.4 $nV/\sqrt{Hz}$. The preamplifier bandwidth is obtained from Hspice simulations and found to be 154.3 MHz. Thus the total equivalent noise of the comparator is obtained from equation (4.10) to be $v_{n-comp} = 84.3\ \mu V$. From section 5.1.2, the switch thermal noise is calculated to be 40.9 μV. The total noise referred to the input of the comparator due to the comparator and the kT/C noise of the loop-filter switches is therfore, $\sqrt{84.3^2 + 40.9^2}\ \mu V = 93.7\ \mu V$. The behavioural level simulator discussed in chapter 4 is now programmed with a thermal noise equivalent to this value and gives a SNR of 74.8 dB for an oversampling ratio of 128. This corresponds to a 40 kHz signal bandwidth for an clock frequency of 20 MHz.

The resistors RL1 and RL2 are poly resistors. The collector currents through Q1-Q2 is partly shunted by PMOS current sources MPBIAS1 and MPBIAS2. These serve to adjust the common-mode swing required at the input of the latch stage.

Regenerative Latch

The BiCMOS regenerative latch consists of a pair of emitter-followers followed by two emitter-coupled pairs QL1-QL2, QL3-QL4 and two level-shifters formed by diode drops available from QBUFL1 and QBUFL3. The emitter-follower buffers required at the inputs of the latch are implemented with transistors QB1,QB2. During the preamplification phase ϕ_1, the signals are first buffered by the emitter-follower pairs. Because ML1 is switched on the current source I_{bias} is

steered into the common emitters of QL1-QL2 which amplify the signal further at their collectors. During phase $\overline{\phi_1}$, the amplified signal at the collectors of QL1-QL2 are regeneratively amplified(amplified with positive feedback) by QL3-QL4 as follows. A small positive signal at the collector of QL3 is fed back via the level shifter to the base of QL4. A negative signal at the collector of QL4 similarly reduces the voltage at the base of QL3. This causes the signal at the collector of QL3 to rise further and that at the collector of QL4 to fall until a latched state is reached when QL3 is turned off and QL4 carries all of the sourced current I_{biasl}. The collector of QL3 is now at V_{DD}, the positive supply rail and that of QL4 is at $V_{DD} - I_{biasl}RL2$. The emitter-follower buffer pairs provide a low-impedance source for driving the bases of QL1-QL2. This is necessary because the large latch output voltage swings may couple substantial kick-back transient noise through the collector-base junction capacitances of QL1-QL2 if their bases are driven by a high impedance source. This would be the case when the preamplifier outputs are directly connected to the bases of QL1-QL2. The kick-back noise voltage at the bases of QL1-QL2 with the emitter-follower buffer in place depends upon the output impedance and therefore the transconductances of the emitter-follower transistors. Therefore the emitter-follower stages need to be biased with sufficient current to provide adequate low impedance at their outputs. The level translators QBUFL1,QBUFL3 are required to prevent saturation of Q3L-Q4L when the latch voltage swings are large. They further serve to buffer the latch outputs for driving the following level translator stage.

The overdrive recovery error due to the latch may be controlled by the latch swing $VLATCH = I_{biasl}RL2$ and by minimizing the parastics at the collectors of Q3L-Q4L. The latter can be achieved by using minimum emitter-area devices for QL1,QL2,QL3,QL4 and by using poly resistances for RL1,RL2. It may be noted that the equivalent input noise of the latch is substantially attenuated by the preamplifier gain and may be relatively unimportant as compared with noise due

to the preamplifier.

The signal swing of the regenerative latch(VLATCH) is typically about two diode drops. For achieving rail-to-rail CMOS swings an ECL-CMOS translator is required. Transistors MEC1 and MEC3 implement this function. The output of this stage is gated with a ϕ_2 clock signal to make it compatible with the VREF summing circuit at the input of the modulator. The rest of the circuit beyond the ECL-CMOS converter implement another stage of latching and buffering to drive the output pad driver circuits.

Name	Size
MPR1	144 μm/0.8 μm
MPRB1	12 μm/0.8 μm
MSW	5 μm/0.8 μm
Q1	4x
R1	5 μmx260 μm
MNBCS	28 μm/0.8 μm
QB1	2x
ML1BIAS	7.8 μm/0.8 μm
QL1	2x
ML1	50 μm/0.8 μm
ML2BIAS	24 μm/0.8 μm
QBUFL1	2x
QBUFL3	1x
ML3BIAS	8.8 μm/0.8 μm

Table 5.3: Device sizes in prototype design

Source	Current
Ibiasprb	160 μA
Ibiaspr	444 μA
Ibiasl	483 μA

Table 5.4: Bias currents in prototype design

5.2 Chip Layout

Fig. 5.3 shows a microphotograph of the complete chip. The main block consisting of the sampling mixer and the sigma-delta modulator is the square-shaped region that lies to the left of the logo(WTADX). The clock generator block lies below the logo. Some large capacitors that decouple the power, ground and bias lines are also visible as square or rectangular blocks. The IF inputs pads are the top and middle pads of the left column of pads and are connected to the main block by lines that are shielded by a cage structure possible with the three metal layers available in the $0.8\mu m$ BICMOS process. The bias lines and reference voltage(VREF) are similarly shielded. An enlargement of the main block is shown in in Fig. 5.4. The sampling mixer and loop-filter occupies approximately the left half of the chip with the large capacitors of loop-filter occupying the areas near the top and bottom edge of the photograph. The comparator occupies the right half of the chip. A zoom of sampling mixer and loop-filter are shown in Fig. 5.5. The bottom-plate sampling mixer roughly occupies the rectangular area in the left-center of the photograph. Buffers that drive the top and bottom switches and generate the delay required for bottom-plate sampling are at the top and bottom of the sampling mixer block.

A very important part of the prototype design and testing is attention to guidelines for guard-rings, grounding and shielding. The effectiveness of guard-rings depends upon the nature of the substrate. For high resistivity

substrates, guard-rings help to reduce the impedance of the underlying substrate to ground. Guard-rings have been used to isolate the different sections of the chip: the clock-generator(digital) , the sampling mixer, loop-filter switches and capacitors , the preamplifier, latch and ECL-CMOS converters and buffers. Apart from using guard-rings, the back-plane contact has been connected to ground to reduce substrate coupled noise. However, at high frequencies bond-wire inductances may increase impedances to ground and reduce the effectiveness of this technique. To overcome this multiple ground pads are used. The chip uses separate power and ground supplies to isolate the low noise loop-filter and comparator sections from noise coupled through the digital supply and ground lines. The bias,VREF and power lines are decoupled inside the chip through on chip capacitors varying between 10 pF to about 50 pF.

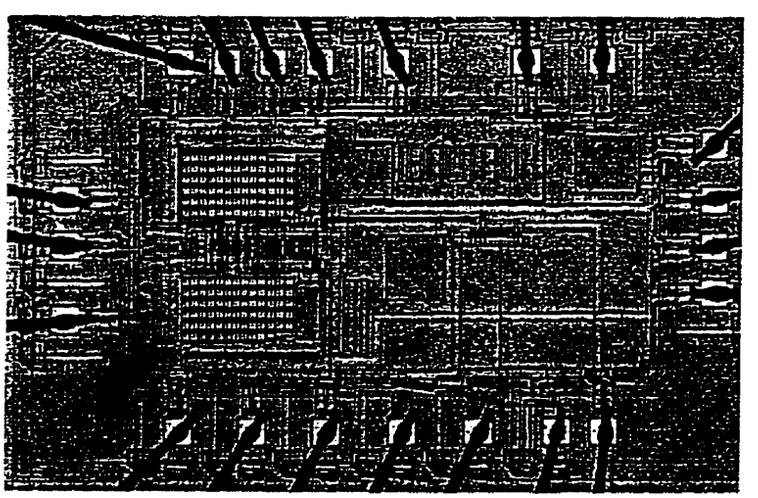


Figure 5.3: Microphotograph of prototype IF digitizer chip

5.3 Test Setup for Prototype Measurements

The test setup for the prototype measurements is shown in Fig. 5.6. The 100 MHz input signal is obtained from an HP-8648A signal generator and fed into a 5 %

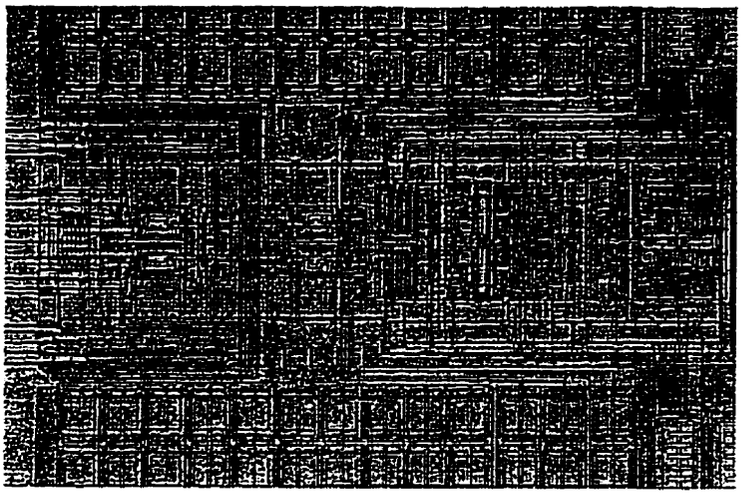


Figure 5.4: Enlargement of main IF digitizer block

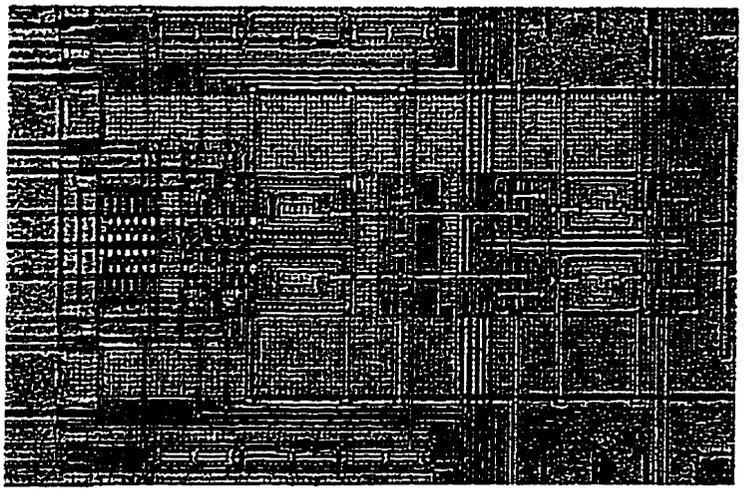


Figure 5.5: Enlargement of sampling mixer and loop-filter section

passband 100 MHz center frequency bandpass filter from TTE. The output of this filter is then fed into a 0-180 degree phase splitter whose two outputs are connected to the IF+ and IF- inputs of the prototype board. The two IF inputs are then connected to the IF inputs of the chip through microstrip traces designed for a 50 ohm characteristic impedance. These traces terminate at the input pins of the chip in 50 ohms to ensure that reflections are minimized. For good second

harmonic measurements, it is important to make sure that the two input paths from the signal input to the chip input pins are matched to sufficient accuracy so that second order(e.g. HD_2, IM_{2+}) distortion is dominated by mismatches due to the differential circuit(sampling mixer) inside the chip. The clock inputs and data outputs of the board are connected via microstrip traces to the control and pattern ports of a VXI Analog tester which captures data at 20 MHz clock speed and stores it in a memory of 64K depth. The connecting cables and connectors for the IF input, clock and data are of BNC type.

The spurious and phase noise characterization of the IF signal source (HP-8648A) and the clock source (HP VXI analog tester) are critical for SNR measurements. The FFT spectrum of the data output at or near the tone frequencies is shaped not only by the windowing function chosen but also the phase noise skirts and spurious tones of these sources.

5.3.1 Board Design Guidelines

A set of recommendations regarding grounding and shielding that helped to improve the SNR are:

- Potential ground loops in the main IF digitizer board should be identified and removed
- Logic interface chips such as data buffers and level translators on the main(digitizer) board can cause serious SNR degradation through ground induced noise coupling
- Low impedance ground connections between a noisy logic board and the main(digitizer) are to be avoided to prevent creation of ground loops
- Clock and data signal connections between boards should be differential so as to avoid return currents flowing through ground nodes.

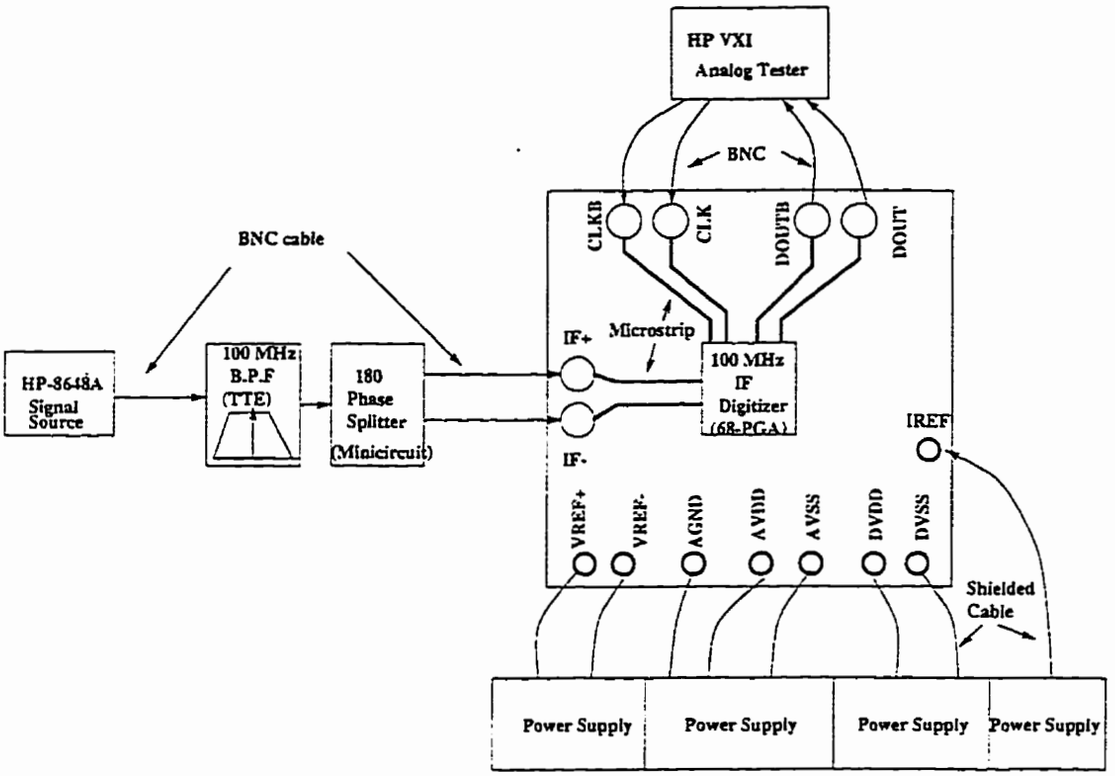


Figure 5.6: Prototype test setup

- The test set-up should be enclosed in a mu-metal box which should have a top cover

5.4 Measurements Results

The output of the IF digitizer is a digital bitstream. Distortion and SNR measurements are done by performing a 64k FFT on this bitstream. A reference level calibration is done at the system level. The SNR is calculated by calibrating the signal power and noise power for a given bandwidth and a given windowing function by integration of the FFT output data. From system level simulations, for $V_{REF} = 0.8\ V$, a 0 dBm (amplitude of 0.316 V for 50 ohms terminations) gives a

signal peak of 76.2 dB for a Hanning window. The test-setup shown in Fig. 5.6 is then calibrated to account for losses in the cables, insertion losses in the bandpass filter and splitter. When testing, the input signal is adjusted appropriately to account for the losses in the input path.

5.4.1 Idle Channel Noise

A representative plot of the measured idle channel (IF inputs shorted to ground) 64k FFT spectrum of the output code for a 10 MHz clock is shown in Fig. 5.7. The SNR obtained by taking the ratio of a hypothetical 0 dBm signal and the integrated noise power from DC to 20 kHz is found to be 76.8 dB. For a 20 MHz clock, the measured SNR is determined to be 73 dB.

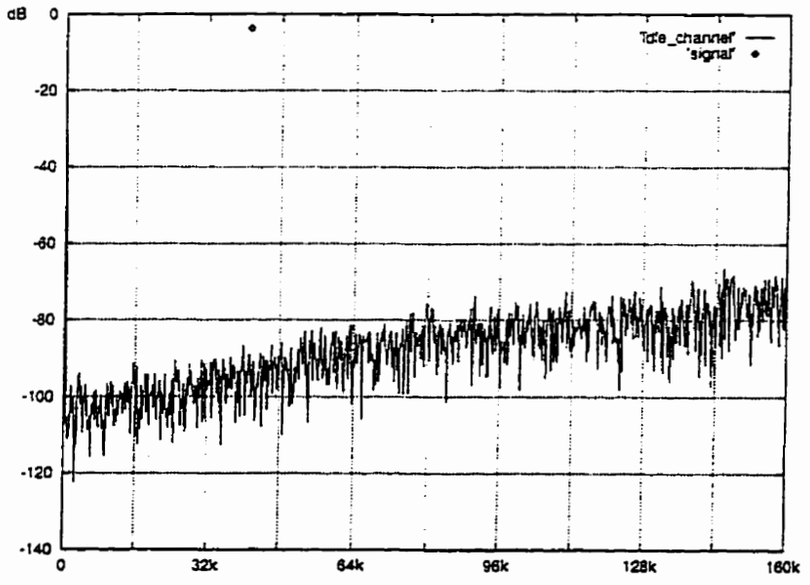


Figure 5.7: 64k FFT plot of an idle channel test

5.4.2 Single Tone Test

A representative FFT plot of single tone test output code in which a 100 MHz IF input is subsampled with a sampling clock of 10 MHz is shown in Fig. 5.8. For 0 dBm input signal an HD_2 of -76 dB and HD_3 of less than -80 dB are measured. The measured SNR for this test is 71.4 dB.

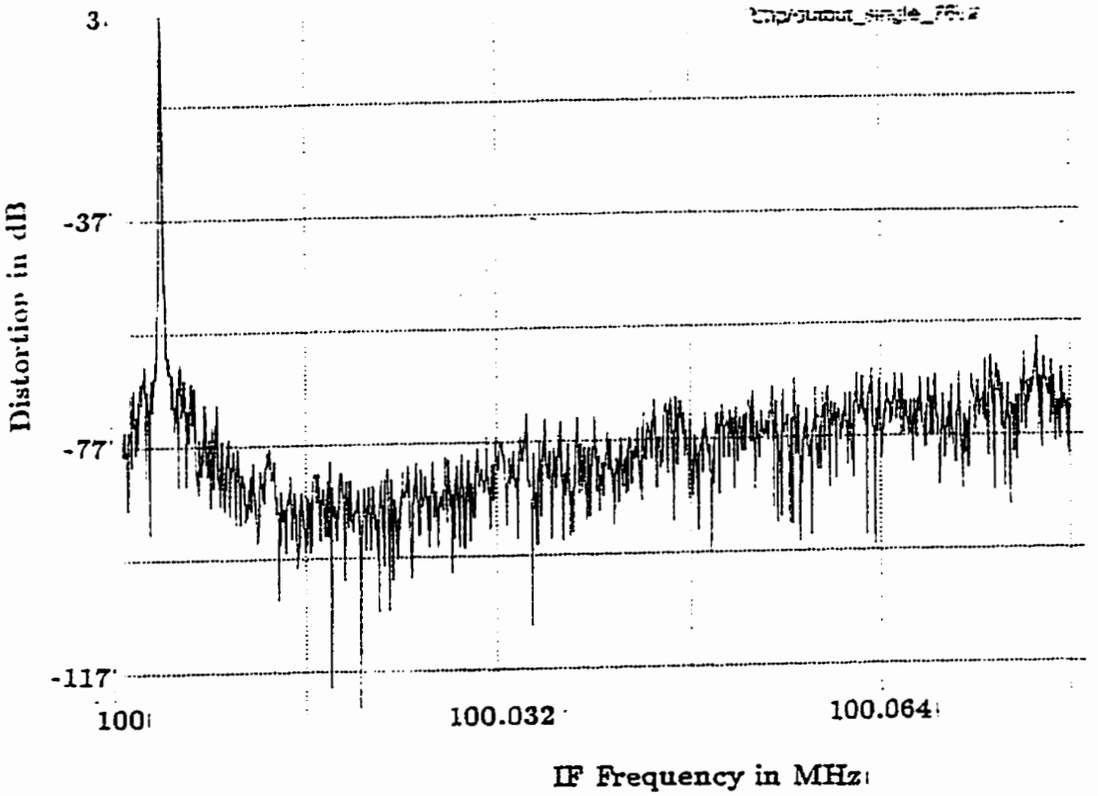


Figure 5.8: 64k FFT plot of a single tone test for 100 MHz IF input

A FFT plot of a single tone test at 150 MHz IF input with a 10 MHz sampling clock is shown in Fig. 5.9. The measured SNR for a 0 dBm input is -70.1 dB. The HD_2 measured is -71.4 dB. The third harmonic distortion component is buried in the noise floor.

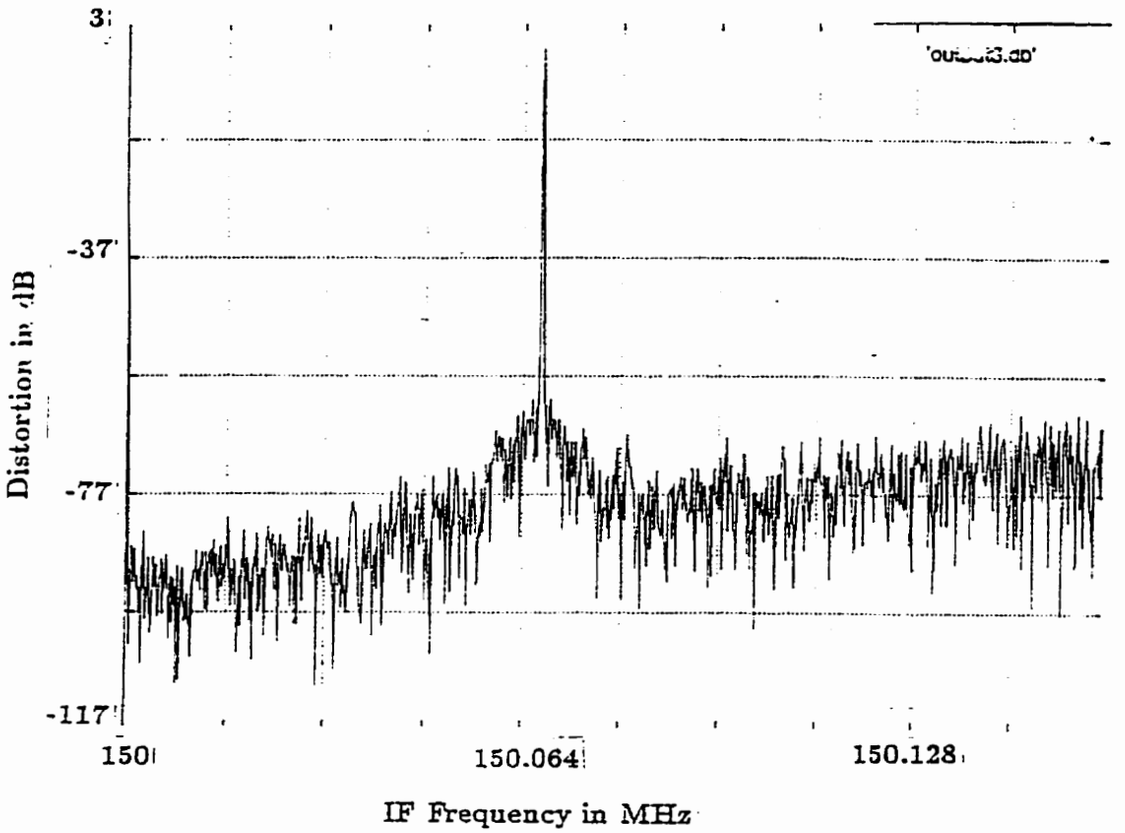


Figure 5.9: 64k FFT plot of a single tone test for 150 MHz IF input

5.4.3 Two Tone Test

A two tone intermodulation test is performed by taking tones at 100.01 and 100.03 MHz, and measuring the IM_3 distortion at 100.04 MHz. Fig.5.10 shows the plot of the FFT for this 2 tones test. An IM_3 of -65 dBm is measured for a -3 dBm input.

5.4.4 Tests at 40 MHz and Higher Clock Frequencies:

Tests at clock frequencies higher than 20 MHz are hampered by the poor phase noise and spurious performance as well as limited memory depth of the 100MHz IMS-XL100 tester. This has restricted tests upto 40 MHz clock frequency that is possible (with a designed serial-parallel adaptor board) with the HP-VXI tester.

Another serious limitation comes from the EMI/RFI as well as noise coupled through ground paths in the board, power supplies, tester system. PLL-based frequency multiplier solutions were also attempted. These have the problem that for the very small closed loop bandwidth that is required to filter out the spurious, the PLL may be unable to lock because of an extremely narrow lock range.

Idle channel and single tone tests were performed at 40 MHz and higher. For tests at 40 MHz clock frequency, a 1-bit serial to 2-bit parallel adaptor board was designed using FAST TTL logic. The ground loop coupling and shielding issues related to boards seriously impacted upon the measured SNR. For example, it was found that direct ground connections through low-impedance paths (through say a coaxial cable ground) between the main IF digitizer board and the noisy adaptor board degrade the SNR by an order of 30 dB or more. Using the guidelines given in section 5.3.1 the idle channel noise of the IF digitizer was reduced to 70 dB for the 40 MHz clock.

5.4.5 Summary of Test Results

A summary of test results is shown in Table 5.4.5. Idle channel measurements show agreement with behavioural simulation results based upon a calculation of the equivalent input noise of the loop-filter and the comparator referred to the comparator input. Third harmonic distortion measurement is masked by the noise floor and is less than -80 dB indicating that it is within reasonable error than the distortion predicted in section 5.1.1. The second harmonic distortion measurement shows that the path mismatch (due to gain and phase errors) from the splitter to the sampling mixer outputs is about 1.9 dB. This suggests that mixer gain and phase mismatch is substantial and further layout matching techniques such as 'quad' structures are necessary. The IM_3 measured from two tone tests is larger than the predicted value and different from the measured HD_3 suggesting that

distortion mechanisms other than non-linear MOS switch resistance may be important. The measured SNR for single and two tone tests also is poorer from the idle channel SNR. This is mostly due clock jitter as explained in chapter 2. A precise quantification of this noise is difficult because it is practically difficult to measure the variance of clock jitter τ_j.

Characteristic	Test condition	Value
SNR	Idle channel at 10 MHz	76.8 dB
SNR	Idle channel at 20 MHz	73.0 dB
SNR	Idle channel at 40 MHz	70.0 dB
HD_2	100 MHz, 0 dBm IF ,10 MHz	-76.0 dB
HD_3	100 MHz, 0 dBm IF ,10 MHz	< -80.0 dB
IM_3	100 MHz, -3 dBm IF ,10 MHz	-65.0 dB
HD_2	150 MHz, 0 dBm IF ,10 MHz	-71.4 dB
SNR	150 MHz, 0 dBm IF ,10 MHz	70.1 dB

Table 5.5: A summary of measurement results

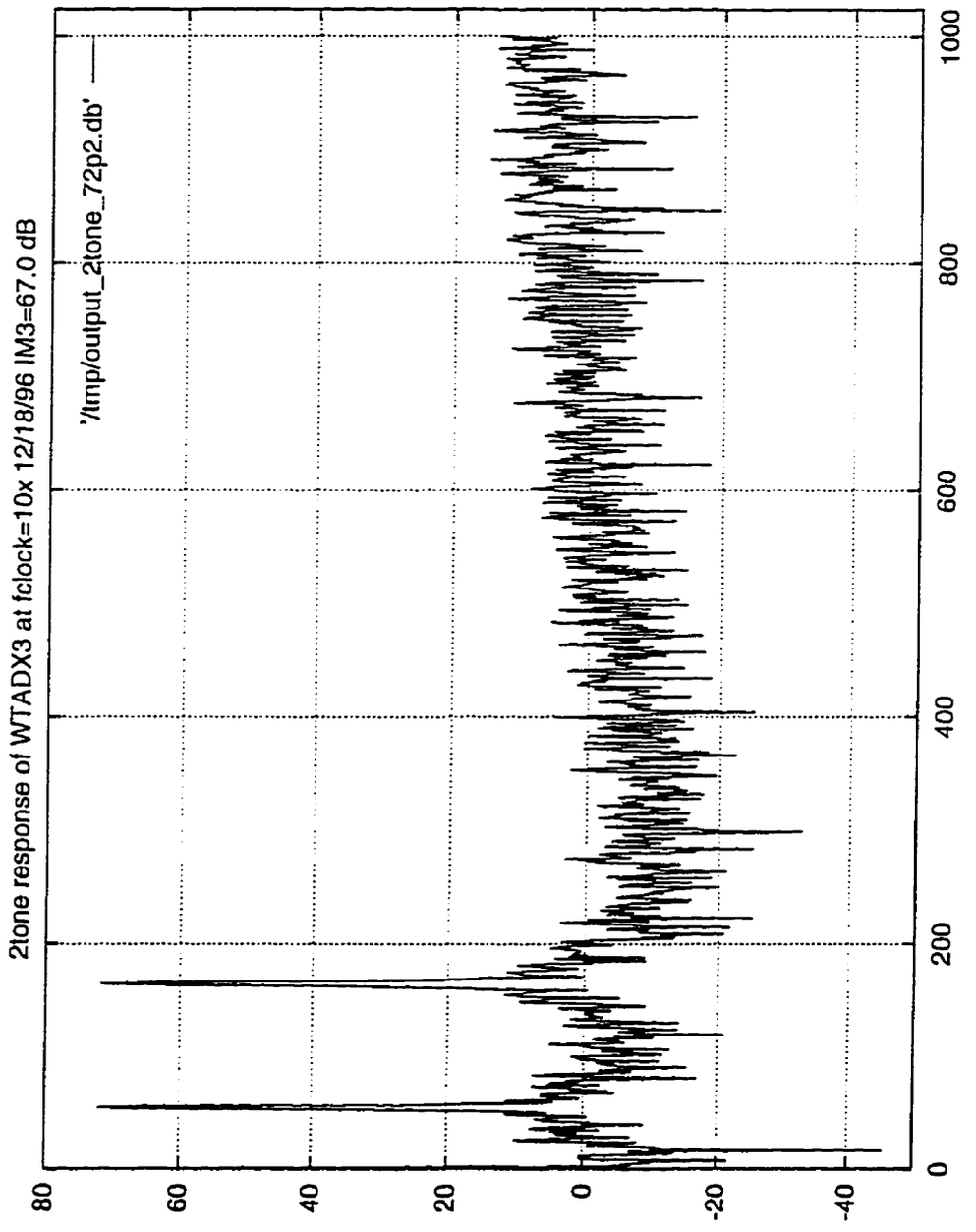


Figure 5.10: 64k FFT plot of a two tone test with 100.01 and 100.03 MHz IF input

Chapter 6

Conclusions

This thesis demonstrates that the advantages that result from digital signal processing of low IF signals in a radio receiver as demonstrated in [1] can be extended to high IF (100 MHz and beyond) processing as well. Traditionally analog functions such as IF channel filtering, AGC and demodulation can be pushed into the digital domain. This can be done by an IF digitizer design with a sufficiently low distortion and with sufficiently low inband noise to meet most high IF processing requirements. The key components in such an IF digitizer design have been identified as the design of the sampling mixer and the design of a high-resolution sigma-delta modulator. Contributions have been made in both areas.

Distortion mechanisms in the sampling mixer have been studied. The powerful and accurate method of Volterra Series has been applied to distortion analysis and a complete picture of distortion in a sampling mixer has emerged. This analysis suggests that for high IF digitization, the most important parameters that can essentially characterize distortion are the K' of the MOS switch, the gate overdrive $(V_{GS} - V_t)$ and the fall-time T_f of the sampling-clock waveform applied at the gate, the frequency of the input signal and the total sampling capacitance.

Furthermore, T_f essentially decides the distortion mechanism. For small T_f, distortion approaches the time-invariant regime for which HD2,HD3 and IM3 are derived using a time-invariant Volterra Series analysis. For large T_f, both non-uniform-sampling distortion and time-varying distortion mechanisms are active. Distortion formulae are derived for both mechanisms. It is shown that for high IF time-varying distortion is small. The distortion in a bottom-plate sampling mixer is analyzed and it is shown that distortion due to the bottom switch is relatively small compared to the top switch distortion for all the three mechanisms of distortion.

The design of a high-resolution baseband sigma-delta modulator using a passive loop-filter is critically dependent upon an accurate analysis of the thermal noise due to the switches of the loop-filter, the devices in the comparator and degradations due to overdrive recovery. The noise due to loop-filter switches and the comparator was analyzed. The dependence of a sigma-delta modulator SNR on preamplifer gain, bandwidth, latch voltage and comparator noise is also shown. A comparison of the comparator equivalent input noise for NMOS,PMOS and bipolar inputs was done and it was shown that a bipolar input preamplifier stage is not suitable for a comparator design.

Measurements on prototype designs show reasonable agreement with the theoretical results for HD3. The degradation in IM3 observed in measurement results and the fact that it is different from the measured HD3 gives rise to the conjecture that it is due to a source of non-linearity different from that of the MOS switch. One potential source is the bond-wire inductance. Preliminary simulations show that there is noticeable degradation in distortion if a series inductance is added at the input of the sampling mixer. The measured idle channel SNR agrees with the theoretical calculations reasonably well.

Future Work

While it was shown that it is possible to analyze distortion in a sampling mixer reasonably accurately, the effect of gate noise/spurious and wideband RF noise have not been analyzed rigorously and correlated with measurement results. As in the case of distortion, this analysis is complicated by the requirement of a time-varying analysis and is therefore a useful avenue of research. The issue of gain and phase mismatch in the I and Q paths of the radio architecture that uses direct IF conversion (as in Fig. 1.4) is an important issue. Preliminary work shows that the gain and phase mismatch in the sampling mixer is small for 100 MHz IF but degrades with increasing frequency. The gain and phase mismatch in the closed-loop transfer function of the sigma-delta modulator due to mismatches in the capacitors of the loop-filter can also be shown to be small because the feedback loop suppresses errors due to mismatches in the elements of the loop. Another important avenue of research is the effect of bond-wires in the applications where the IF digitizer inputs are taken from outside the chip. Preliminary simulations show that the bondwires in a typical PGA package cause significant degradation in distortion even for 100 MHz IF.

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Glossary

LO	Local Oscillator
RF	Radio Frequency
IF	Intermediate Frequency
SNR	Signal-to-noise ratio
PSD	Power Spectral Density
μ	Effective mobility of silicon
C_{ox}	Gate capacitance per unit area of a MOS transistor
K'	MOS Device Constant equal to $\mu C_{ox}\frac{W}{L}$
W/L	Ratio of effective width to effective length of a MOS transistor
V_t	Threshold Voltage of the MOS transistor
	(including non-ideal effects)
BJT	Bipolar Junction Transistor
$(V_{GS} - V_t)$	gate overdrive in a MOS transistor