Hardware-in-the-loop Tests on Distance Protection Considering VSC Fault-ride-through Control Strategies

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Abstract: The short-circuit response of a voltage source converter (VSC) can vary from each other significantly with different control strategies. This study investigates the performance of distance protection under unbalanced faults considering two control strategies during fault-ride-through using hardware-in-the-loop tests. Variations on fault type, converter current limit, fault resistance and pre-fault power flow conditions are also examined. The tests reveal that the error in measured impedance caused by fault resistance will be enlarged in a converter-dominated power system. The first control strategy tends to cause overreach problem while the second can raise both overreach and underreach problems. The indeterminacy associated with the second strategy is jointly affected by control parameters, converter current limit, fault resistance and pre-fault power flow conditions. The findings of this study can help to stipulate grid requirements under unbalanced faults.

1 Introduction

Voltage source converters (VSCs) are widely used in renewable energy sources and high-voltage direct current (HVDC) connections. With conventional power plants gradually phased out, the power system will be evolving into a converter-dominated one in the future. According to Danish Ministry of Climate and Energy, Denmark aims to achieve 100% renewable energy supply by 2050, being completely independent of fossil fuels [1]. The short-circuit response of a VSC is mainly governed by its control system and it can be significantly different from that of a synchronous generator (SG). Modern grid codes have imposed fault-ride-through (FRT) requirements on converter-based generation in terms of a lower limit of a voltage-against-time profile. With limited converter overload capability, the priority of power injection during FRT period can be either given to active power or reactive power [2]. However, the current grid codes generally lack statements regarding unbalanced faults and therefore it is a common practice nowadays for VSC to provide only positive-sequence short-circuit current under grid unbalanced faults. Recently, attentions have been given to the possibility of injecting negative-sequence reactive current to mitigate negative-sequence voltage under unbalanced faults, which has already been suggested in a German standard [3]. According to [4], transmission system operators may also specify a requirement for negative-sequence current injection from HVDC. Given different control strategies, the short-circuit response of VSC can vary from each other and may pose threats to the reliability of distance protection.

In the past years, numerous studies have been conducted regarding the potential impact of VSC on distance protection. However, most of them only focus on balanced faults. Among the few works investigating the performance of distance protection under unbalanced faults [5–8], VSC is controlled to only inject positive-sequence current and none of them has considered negative-sequence current injection or different levels of converter current limit. In this paper, the performance of distance protection under unbalanced faults is evaluated considering different FRT control strategies. The first strategy (FRT1) only injects positive-sequence active power under fault conditions. In contrast, the second strategy (FRT2) gives priority to reactive power injection and deploys flexible positive- and negative-sequence power control strategy introduced by Teodorescu *et al.* [9], where the amount of positive- and negative-sequence reactive power can be flexibly adjusted. Considering the limited converter overload capability, both strategies restrict current within a pre-specified limit for each phase during unbalanced faults. In addition, variations on converter current limit, fault resistance and pre-fault power flow conditions are all examined through hardware-in-the-loop (HIL) tests using a commercial distance relay.

2 FRT strategies

Considering a three-phase current-controlled VSC, the short-circuit response under unbalanced faults mainly depends on how the current references are formulated. If $\boldsymbol{v} = [v_a\ v_b\ v_c]^{\mathrm{T}}$ and $\boldsymbol{i} = [i_a\ i_b\ i_c]^{\mathrm{T}}$ are the voltage and current vectors at the point of common coupling (PCC), the instantaneous power p and q can be expressed as [10]

$$p = \underbrace{\overbrace{\boldsymbol{v}^+ \cdot \boldsymbol{i}^+}^{p^+} + \overbrace{\boldsymbol{v}^- \cdot \boldsymbol{i}^-}^{p^-}}_{\bar{p}} + \underbrace{\boldsymbol{v}^+ \cdot \boldsymbol{i}^- + \boldsymbol{v}^- \cdot \boldsymbol{i}^-}_{\tilde{p}} \tag{1}$$

$$q = \underbrace{\overbrace{\boldsymbol{v}_\perp^+ \cdot \boldsymbol{i}^+}^{q^+} + \overbrace{\boldsymbol{v}_\perp^- \cdot \boldsymbol{i}^-}^{q^-}}_{\bar{q}} + \underbrace{\boldsymbol{v}_\perp^+ \cdot \boldsymbol{i}^- + \boldsymbol{v}_\perp^- \cdot \boldsymbol{i}^+}_{\tilde{q}} \tag{2}$$

where the operator '⊥' refers to the vector that lags the associated one by 90°; the superscripts '+' and '−' represent positive- and negative-sequence components; $\bar{p}$ and $\bar{q}$ are the constant active and reactive power terms that contain positive-sequence power p^+, q^+ and negative-sequence power p^-, q^-; while $\tilde{p}$ and $\tilde{q}$ are the oscillating active and reactive power terms whose average values are zero. According to [9], the active and reactive current references can be formulated as

$$\boldsymbol{i}_P^{\mathrm{ref}} = k_p \frac{P^{\mathrm{ref}}}{|\boldsymbol{v}^+|^2}\boldsymbol{v}^+ + (1-k_p)\frac{P^{\mathrm{ref}}}{|\boldsymbol{v}^-|^2}\boldsymbol{v}^- \tag{3}$$

$$\boldsymbol{i}_Q^{\mathrm{ref}} = k_q \frac{Q^{\mathrm{ref}}}{|\boldsymbol{v}^+|^2}\boldsymbol{v}_\perp^+ + (1-k_p)\frac{Q^{\mathrm{ref}}}{|\boldsymbol{v}^-|^2}\boldsymbol{v}_\perp^- \tag{4}$$

where k_p and k_q are two flexible scalars. By substituting (3) and (4) into (1) and (2), there are

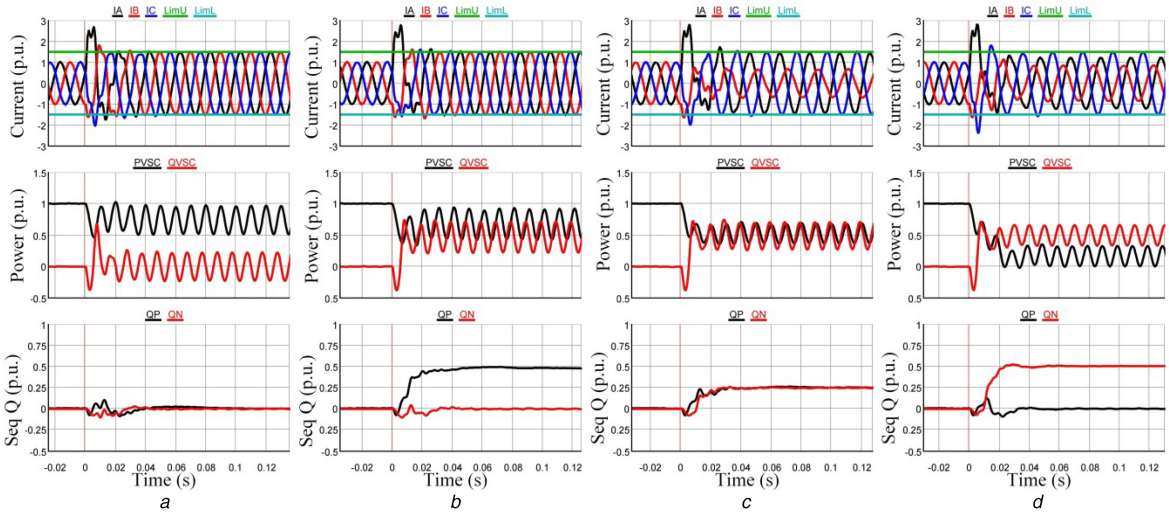

Fig. 1 *Short-circuit response of VSC subject to AB fault at the PCC*
(a) FRT1, ***(b)*** FRT2 ($Q^{\text{ref}} = 0.5$ p . u ., $k_q = 1$), ***(c)*** FRT2 ($Q^{\text{ref}} = 0.5$ p . u ., $k_q = 0.5$), ***(d)*** FRT2 ($Q^{\text{ref}} = 0.5$ p . u ., $k_q = 0$)

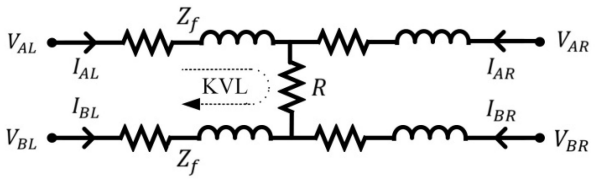

Fig. 2 *Circuit diagram for AB fault*

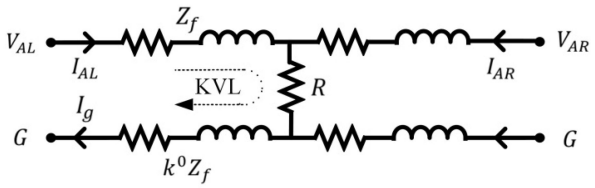

Fig. 3 *Circuit diagram for AG fault*

$$\frac{p^+}{p^-} = \frac{k_p P^{\text{ref}}}{(1-k_p)P^{\text{ref}}} \quad \frac{q^+}{q^-} = \frac{k_q Q^{\text{ref}}}{(1-k_q)Q^{\text{ref}}} \tag{5}$$

Therefore, the relative relationship between positive- and negative-sequence power can be flexibly controlled through k_p and k_q, which enables various FRT strategies to be deployed. In this paper, two different FRT strategies under unbalanced faults are examined:

- *FRT1:* only positive-sequence active power is injected ($Q^{\text{ref}} = 0$, $k_p = 1$);
- *FRT2:* reactive power injection is prioritised with different values of k_q ($Q^{\text{ref}} \neq 0$, $k_q = 1$, 0.8, 0.6, 0.4, 0.2 or 0);

In order to restrict the current flowing through converters within the limit $I_{\max}$ for each phase, the maximum allowed active power $P_{\max}$ should be properly calculated. Based on [9], $P_{\max}$ can be expressed as a function of $I_{\max}$, Q^{ref}, k_p, k_q and grid conditions. In this paper, the active power reference is restrained using the methods presented in [9]. The detailed equations are not repeated here for brevity. As an example, with a 1.5 p.u. current limit in each phase, Fig. 1 illustrates the short-circuit response of a VSC subject to a solid AB fault at the PCC. The short-circuit response is significantly different from each other with various FRT strategies.

3 Distance protection for unbalanced faults

The circuit diagrams in Figs. 2 and 3 demonstrate AB fault and AG fault, where Z^f is the positive-sequence apparent impedance from the relay to the fault location; R is the fault resistance; k^0 is the zero-sequence compensation factor; L and R denote quantities related to local and remote terminal, respectively.

With Kirchhoff's voltage law applied in Figs. 2 and 3, there are

$$\begin{aligned} V_{AL} - V_{BL} &= Z_f I_{AL} - Z_f I_{BL} \\ &\quad + R(I_{AL} + I_{AR} - I_{BL} - I_{BR}) \end{aligned} \tag{6}$$

$$V_{AL} = I_{AL} Z_f + R(I_{AL} + I_{AR}) + I_g k^0 Z_f \tag{7}$$

By rearranging (6) and (7), the typical expressions used by distance relays to calculate the apparent impedance for phase-phase and phase-ground elements are

$$Z_{AB} = \frac{V_{AL} - V_{BL}}{I_{AL} - I_{BL}} = Z_f + R\left(1 + \frac{I_{AR} - I_{BR}}{I_{AL} - I_{BL}}\right) \tag{8}$$

$$Z_{AG} = \frac{V_{AL}}{I_{AL} + k^0 I_g} = Z_f + R\left(1 + \frac{I_{AR} - k^0 I_g}{I_{AL} + k^0 I_g}\right) \tag{9}$$

Since both $((I_{AR} - I_{BR})/(I_{AL} - I_{BL}))$ and $((I_{AR} - k^0 I_g)/(I_{AL} + k^0 I_g))$ are complex quantities, the existence of fault resistance R will introduce an additional impedance to be added to Z_f, which cause a measuring error in the measured impedance Z_{AB} and Z_{AG}. For a conventional power system, this error is usually insignificant and thus can be mitigated by tilting the reactance element clockwise or counter-clockwise [11]. However, for a converter-dominated power system, the error might be enlarged and unpredictable, posing threat to the reliability of distance protection as the short-circuit response of VSC is significantly different from that of SGs.

4 Test system

The single-line diagram of the studied 400 kV power system is presented in Fig. 4. A SG is connected at bus 1, which is the slack bus of the system. Two VSCs (VSC1 and VSC2) rated at 500 MVA each are interfaced with the grid on bus 5 and bus 6, respectively. Two adjustable loads (L1 and L2) are connected at bus 2 and bus 6. A distance relay is equipped to protect the transmission line between bus 6 and bus 2 (line 6–2), whose total length is 30 km.

In this paper, the performance of distance relay is evaluated through HIL tests as illustrated in Fig. 5. The power system is modelled by RSCAD and simulated in RTDS (Real Time Digital Simulator). The three-phase voltage and current needed by the distance relay are extracted from the Analog Output Card and amplified by the V & I Amplifier. The control signal from the relay is sent back to RTDS through the Digital Input Card, forming a closed loop.

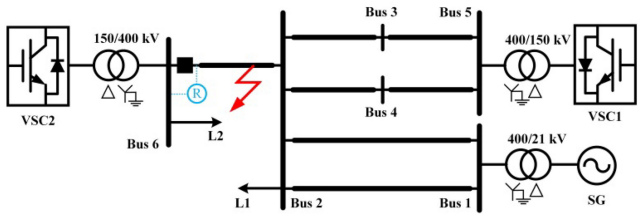

Fig. 4 *Single-line diagram of the studied power system*

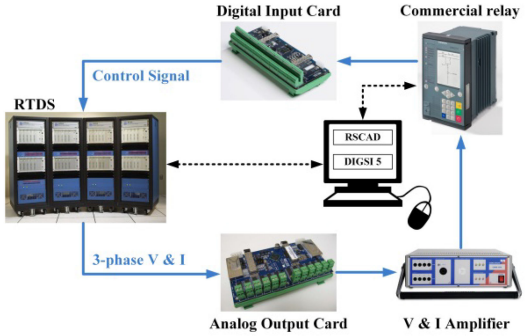

Fig. 5 *HIL test platform*

Table 1 Test scenarios

Scenarios (VSC2)	Current limit (VSC2), p.u.	AG fault resistance, Ω	AB fault resistance, Ω
Sx.1	1.00	0	0
Sx.2	1.00	5	1
Sx.3	1.25	5	1
Sx.4	1.50	5	1
Sx.5	1.25	10	2

$x = 1$: FRT1, $x = 2$: FRT2.

When $x = 2$, $k_q = 1$, 0.8, 0.6, 0.4, 0.2 or 0.

5 Case studies

For the following case studies, two types of unbalanced faults (AG and AB faults) are considered. The fault is initiated at 75% (22.5 km) of line 6–2 while the zone-1 protection of the distance relay is set to protect 80% (24 km) of the line using classic method with a quadrilateral characteristic curve. For VSC1, FRT2 with $k_q = 1$ is always deployed and the current limit is fixed at 1 p.u. (2.7217 kA). For VSC2, its FRT strategy and current limit can be changed. The variations are summarised in Table 1 with different fault resistance. Prior to the fault, each VSC is delivering 500 MW active power at unity power factor. Three different pre-fault power flow conditions are examined by changing the amount of the loads according to Table 2, where power flow 1 imports 500 MW active power from bus 2 to bus 6 while power flow 3 exports 500 MW active power from bus 6 to bus 2. It is assumed that the reactive power reference for both VSCs under fault conditions are generated using $Q^{\text{ref}} = |\boldsymbol{v}^+| \cdot I_Q$. The value of I_Q is obtained using the Danish grid code in [12], which can be mathematically expressed by $I_Q = -2.5|\boldsymbol{v}^+| + 2.25$ $(0 \le I_Q \le 1)$. For each test scenario and pre-fault power flow condition, the HIL test is repeated ten times.

5.1 FRT1

Figs. 6 and 7 summarise the measured fault distance for AG and AB faults, respectively, for different scenarios when FRT1 is applied for VSC2. As is shown in Figs. 6 and 7, the measured fault distance is still accurate when there is no fault resistance (S1.1). However, due to the measuring error, overreach problem (under-estimating fault distance) occurs for both AG and AB faults when fault resistance is present (S1.2–S1.5) regardless of pre-fault power flow conditions.

Table 2 Load level for different power flow conditions

Load	Power flow 1 (load import), MW	Power flow 2, MW	Power flow 3 (load export), MW
L1	0	500	1000
L2	1000	500	0

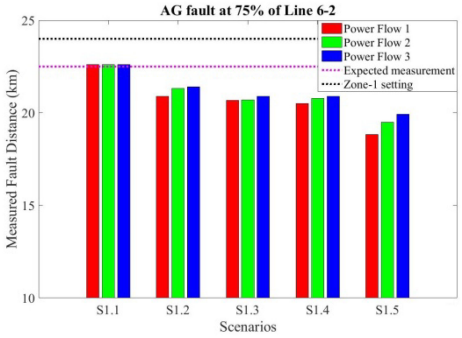

Fig. 6 *Measured fault distance with FRT1 (AG fault)*

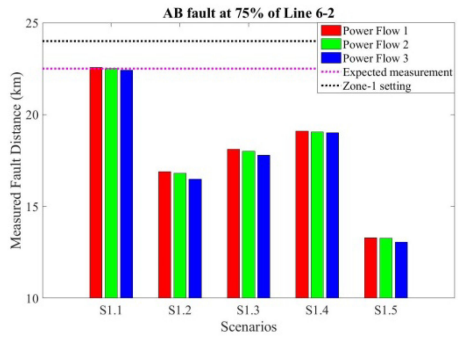

Fig. 7 *Measured fault distance with FRT1 (AB fault)*

For AG fault, the different levels of VSC2 current limit have less effect on the reach (by comparing S1.2–S1.4 in Fig. 6). Nevertheless, the overreach gets aggravated with lower current limit (by comparing S1.2–S1.4 in Fig. 7) for AB fault. In addition, faults with higher fault resistance exhibit larger measuring error, aggravating the overreach problem for both AG and AB faults (by comparing S1.3 and S1.5 in Fig. 6 or Fig. 7).

Corresponding to the five scenarios with power flow 1 in Fig. 7, Figs. 8*a–e* present the measured impedance locus under AB fault for S1.1–S1.5, where Figs. 8*b–e* illustrate overreach when there is fault resistance. For the sake of comparison, VSC2 is then replaced by a conventional SG and the same HIL tests are repeated. Fig. 8*f* shows the corresponding measured impedance locus for AB fault with 2 Ω fault resistance and power flow 1. Given the same fault conditions, Fig. 8*f* gives relatively accurate result while Fig. 8*e* exhibits significant error. This indicates that the measuring error caused by fault resistance will be enlarged in a converter-dominated power system, degrading the reliability of distance protection.

5.2 FRT2

With the FRT strategy of VSC2 changed to FRT2, the same HIL tests are repeated according to Tables 1 and 2. Figs. 9 and 10 summarise the corresponding measured fault distance for AG and AB faults, respectively, with different values of k_q.

According to Figs. 9 and 10, the measured fault distance is relatively accurate when there is no fault resistance involved (S2.1). However, as long as fault resistance is present (S2.2–S2.5), the measured fault distance exhibits error and both underreach (over-estimating fault distance) and overreach problem (under-estimating fault distance) can arise, depending on the value of k_q, VSC2 current limit and the values of fault resistance.

Taking Fig. 9*b* as an example, the measured fault distance for S2.2–S2.5 is gradually increasing with k_q changing from 1 to 0.

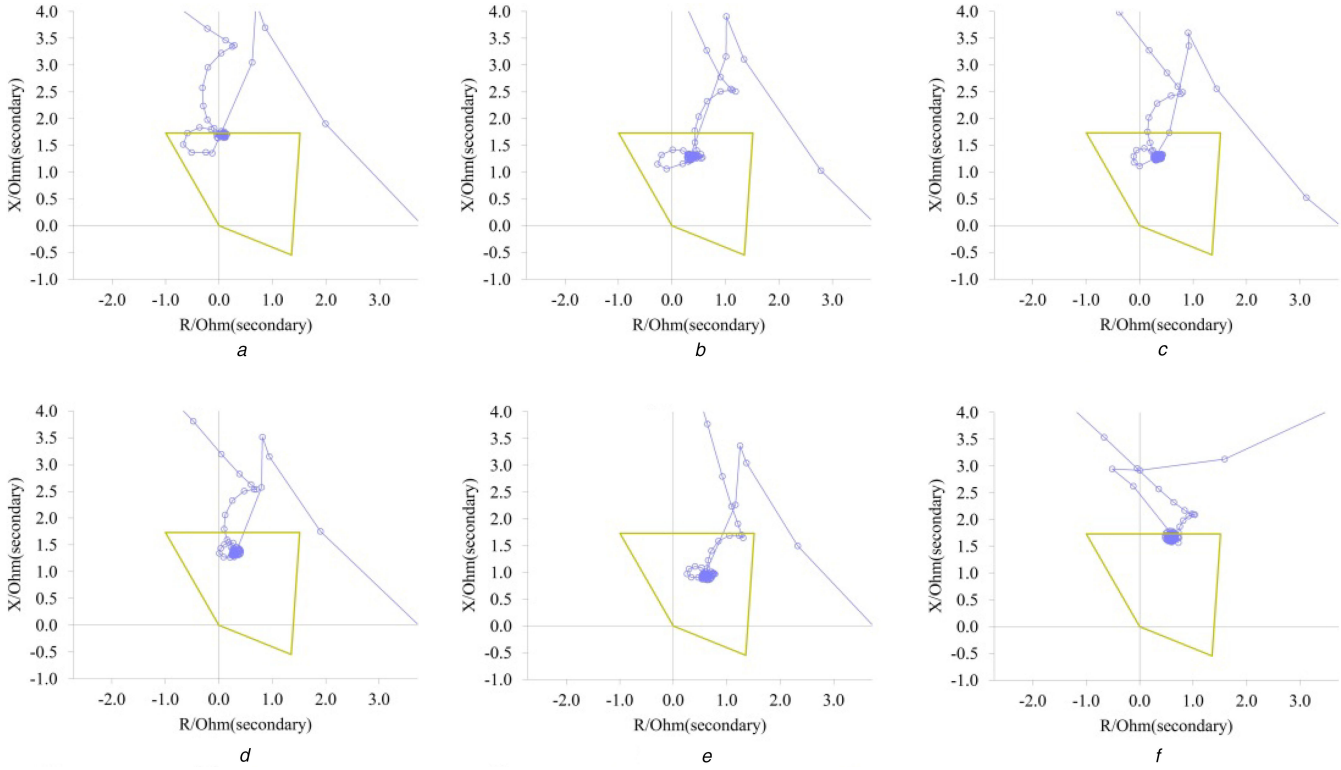

Fig. 8 *Measured impedance locus for AB fault (power flow 1)*
(a) S1.1, ***(b)*** S1.2, ***(c)*** S1.3, ***(d)*** S1.4, ***(e)*** S1.5, ***(f)*** VSC2 is replaced by SG

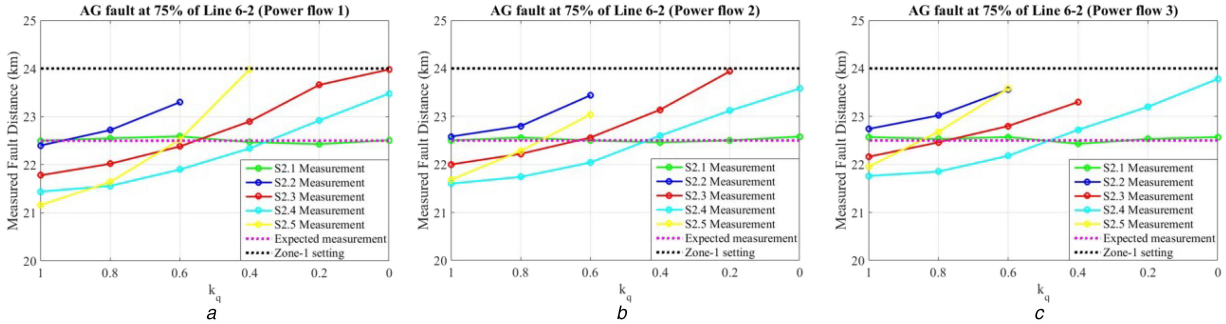

Fig. 9 *Measured fault distance with FRT2 (AG fault)*
(a) Power flow 1, ***(b)*** Power flow 2, ***(c)*** Power flow 3

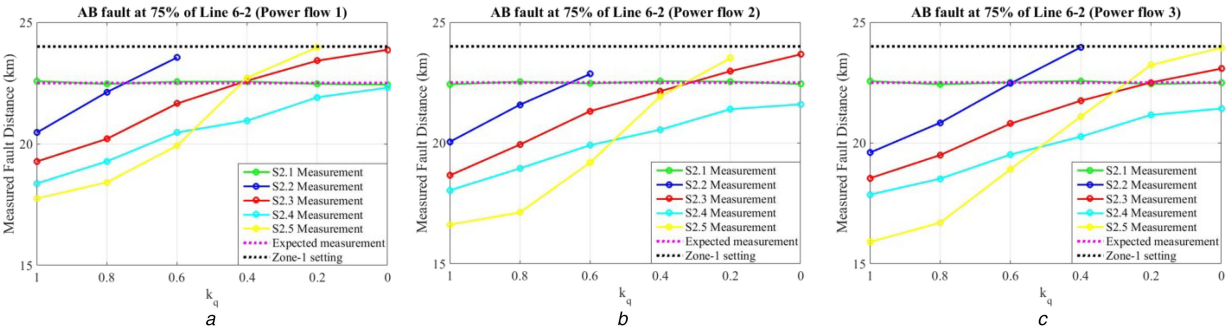

Fig. 10 *Measured fault distance with FRT2 (AB fault)*
(a) Power flow 1, ***(b)*** Power flow 2, ***(c)*** Power flow 3

Regarding S2.3 in Fig. 9*b*, the measuring error caused by the fault resistance is reflected as overreach when $k_q = 1$ or 0.8. Nevertheless, the measuring error is reflected as underreach when k_q is below 0.6. In the worst case, the distance relay does not operate with $k_q = 0$ because the calculated impedance between the relay and fault location is larger than the zone-1 setting.

With the current limit of VSC 2 increased from 1.25 p.u. (S2.3) to 1.5 p.u. (S2.4), the entire line of S2.3 in Fig. 9*b* moves downwards, which on the one hand mitigates underreach problem for below 0.4 but on the other hand aggravate the overreach problem for above 0.6. Similarly, the entire line of S2.3 in Fig. 9*b* moves upwards when the current limit of VSC2 decreases from 1.25 to 1 p.u. (S2.2), resulting in the entire line of S2.2 above the correct value.

Given the same VSC2 current limit, the impact of k_q becomes more significant with higher fault resistance. In Fig. 9*b*, the slope of the entire line of S2.3 increases when the fault resistance is increased (by comparing S2.3 to S2.5), which aggravates the

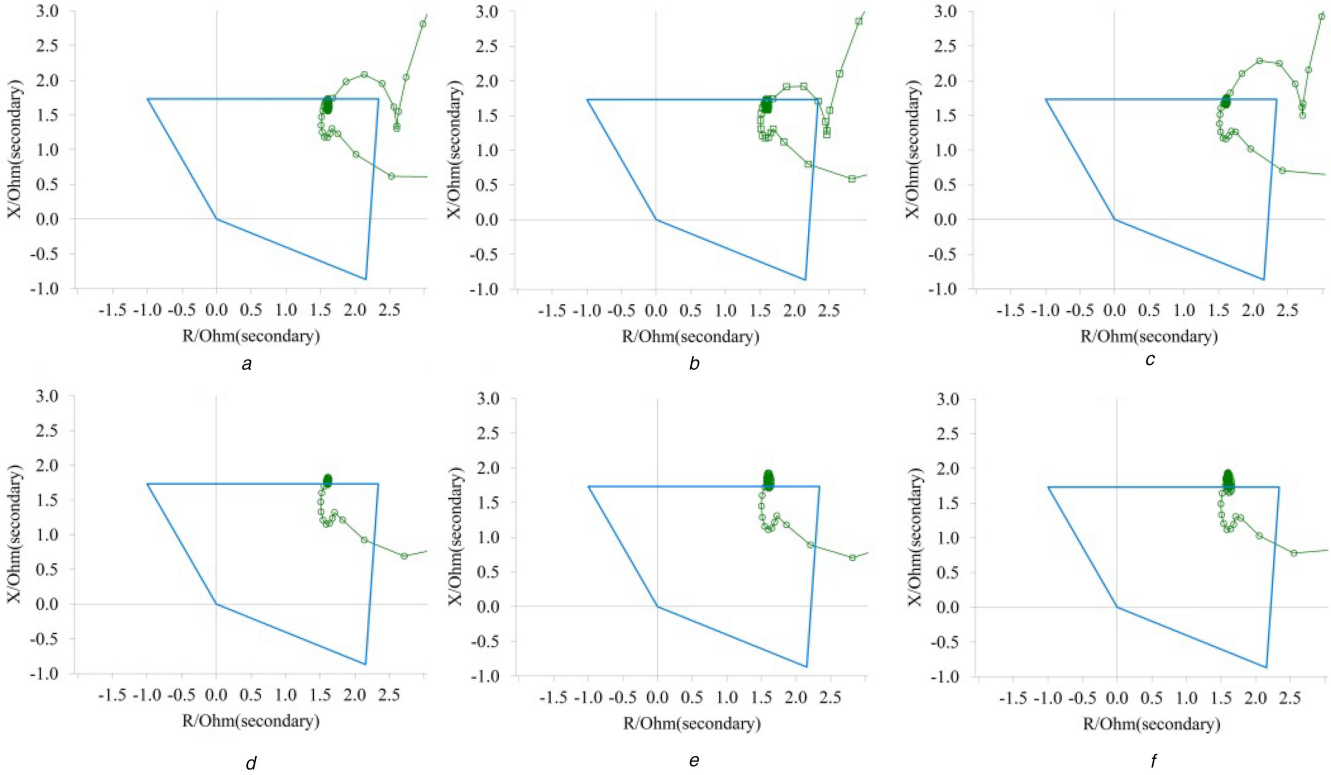

Fig. 11 *Measured impedance locus for AG fault (S2.5, power flow 3)*
(a) $k_q = 1.0$, ***(b)*** $k_q = 0.8$, ***(c)*** $k_q = 0.6$, ***(d)*** $k_q = 0.4$, ***(e)*** $k_q = 0.2$, ***(f)*** $k_q = 0.0$

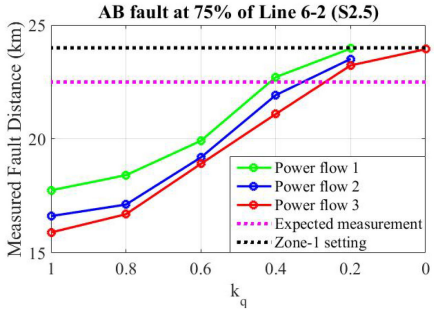

Fig. 12 *Measured fault distance for AB fault (S2.5)*

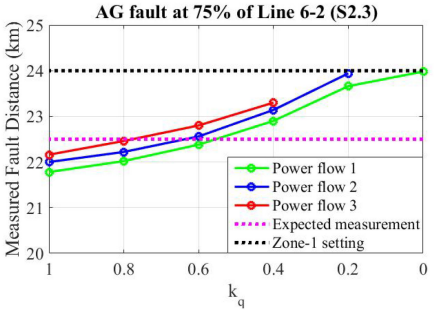

Fig. 13 *Measured fault distance for AG fault (S2.3)*

overreach problem for higher k_q and the underreach problem for lower k_q. The effect of k_q, converter current limit and fault resistance described above can also be observed in other subfigures of Figs. 9 and 10.

Corresponding to S2.5 in Fig. 9*c*, Fig. 11 presents the measured impedance locus under AG fault with different values of k_q. For $k_q = 1$, 0.8 or 0.6, the relay operates and clears the fault. However, as presented in Figs. 9*d–e*, the measured impedance stabilises outside zone 1 and the relay fails to trip when $k_q = 0.4$, 0.2 or 0.

According to [13] for a distance relay using classic method, the measuring error depends on pre-fault power flow conditions in a way that load import tends to cause underreach while load export tends to cause overreach. This means the measured fault distance under load import condition is slightly larger than that of load export condition. However, this might not be valid anymore with the presence of VSC. Figs. 12 and 13 compare the measured fault distance under different pre-fault power flow conditions for AB fault (S2.5) and AG fault (S2.3), respectively. In Fig. 12, the entire line of power flow 1 (load import) is above the entire line of power flow 3 (load export), which complies with the statements in [13]. However, an opposite trend can be observed in Fig. 13, where the entire line of power flow 1 is below the entire line of power flow 3. Together with the impact from converter current limit and fault resistance, this inconformity makes it even harder to predict whether overreach or underreach could occur, which may invalidate conventional countermeasures.

6 Conclusions

This paper has evaluated the performance of distance protection under unbalanced faults through HIL tests considering two different VSC FRT control strategies in various scenarios. The test results reveal that the measuring error caused by fault resistance can be enlarged and unpredictable with the presence of VSC. The first examined strategy tends to cause overreach problem while the second examined strategy can cause both underreach and overreach problems. For both FRT control strategies, the measuring error is also affected by the converter current limit. Regarding the second strategy with the capability of injecting negative-sequence reactive power during unbalanced faults, the associated indeterminacy aggravates as the relative relationship between positive- and negative-sequence reactive power and pre-fault power flow conditions also impact the measuring errors. This uncertainty makes it difficult to decide the amount of negative-sequence current injection under unbalanced faults and to design the relay settings. Therefore, non-pilot distance protection using classic method might not be appropriate serving as a primary protection of transmission lines for converter-dominated power systems. FRT control strategies and converter current limit under grid unbalanced faults are of great importance for evaluating the performance of

distance protection, which should not be ignored in the relevant studies. A potential solution to the problem revealed in this paper could be the deployment of distance protection using reactance method instead of classic method, which will be tested in future work.

7 Acknowledgment

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