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w Power 135mW Pipeline ADC With Speed 80 MSPS 8-bit

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***Abstract*- This paper describes a pipeline analog-to-digital converter is implemented for high speed camera. In the pipeline ADC design, prime factor is designing operational amplifier with high gain so ADC have been high speed. The other advantage of pipeline is simple on concept, easy to implement in layout and have flexibility to increase speed. We made design and simulation using Mentor Graphics Software with 0.35µm CMOS technology with a total power dissipation of 135 mW. Circuit techniques used include a precise comparator with latch, operational amplifier and Non-Overlapping clock. A switched capacitor is used to sample, multiplying and hold at each stage. Simulation a worst case DNL and INL of 0,6 LSB. The design operates at 3,3 V dc. The speed camera cmos at 10.000 frames/s.**

I. INTRODUCTION

CMOS image sensors have evolved in the past years as a promising alternative to the conventional Charge Coupled device (CCD) technology. CMOS offer lower power consumption, more functionality and the possibility to integrate a complete camera system on one CHIP.

The high speed camera used matrices photodiode to capture objects and each photodiode send an analog pixel to matrices column. Output analog pixel is converted to digital pixel by ADC then output from ADC is processed by digital processor element. ADC is used to converter is pipeline. Diagram block high speed camera is shown in figure 1.

In the real time images processing, sensors function is important because it has function as transducer, so images can be processed to application for examples, face tracking and face recognition, medical imaging, industrial, sports and so on[4,5].

Figure 1. Describes 64x64 active pixel sensors (APS) is used capture object. We used the row decoder is charged to send to each line of pixels the control signals. The prosess scan of parallel 64 column APS in one time, where one pixel ≤ 100ns and speed camera 10.000 frames/s same as 100us/frames[5,6].

Number of ADC is used in the system are 64 on parallel condition. Function of ADC in the process is important to convert from analog pixels to digital pixels where speed camera 10.000 frames/s same as 100us/frames, 100us/64row/128cycle same as 12,2ns. so wherever we must design pipeline ADC which have transfer rate 80 Msamples/s.

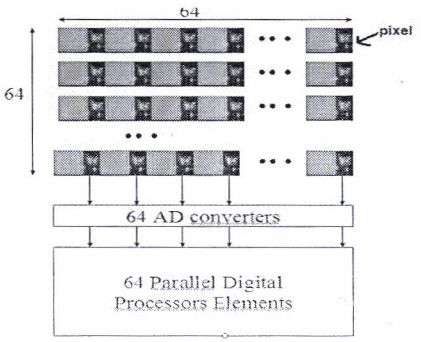


Figure 1. Diagram Block high speed camera

II. ONE-BIT PER STAGE PIPELINE ARCHITECTURE

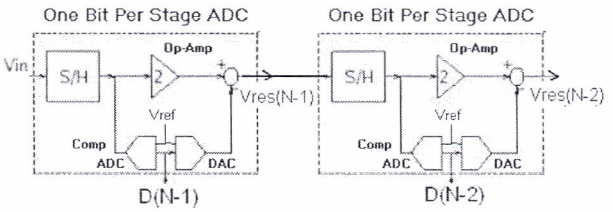
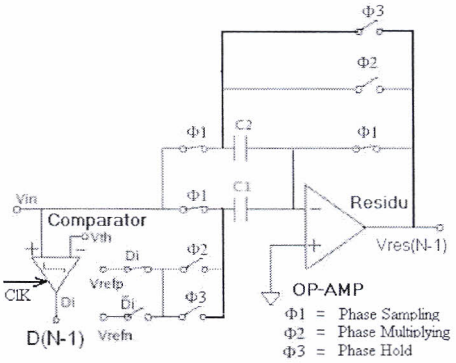


Figure 2. One bit/ stage architecture

Figure 2 shows block diagram of an ideal N-stage, 1-bit per stage pipelined A/D converter. Each stage contributes a single bit to digital output. The most significant bits are resolved by first stage in the pipeline. The result of stage is passed on the next stage where the cycle is repeated. A pipeline stage is implemented by the conventional switched capacitor (SC), it is shown at figure 3[1].



Fiure. 3. Scheme of switched capacitor pipelined A/D converter

Vrefp is the positive reference voltage and *Vrefn* is a negative reference voltage. Each stage consists of capacitor C1, C2, an operational amplifier and a comparator. Value of *C1* and *C2* are equal in my design. Each stage operates in a sampling phase, a multiplying phase and hold phase.

During the sampling phase Φ1 , the comparator produces a digital output *Di*. *Di* is 1 if *Vin* > *Vth* and *Di* is 0 if *Vin* < *Vth*, where *Vth* is the threshold voltage defined midway between *Vrefp* and *Vrefn*. During multiplying phase Φ2, C2 is connected to the output of the operational amplifier and C1 is connected to either the reference voltage *Vrefp* or *Vrefn*, depending on the bit value *Di*. If *Di* = 1, C1 is connected to *Vrefp*, resulting in the resedu (Vout) is :

$$Vout(i) = 2 \times Vin(i) - Di.Vrefp \quad (1)$$

Otherwise, C1 is connected to *Vrefn*, giving an output voltage

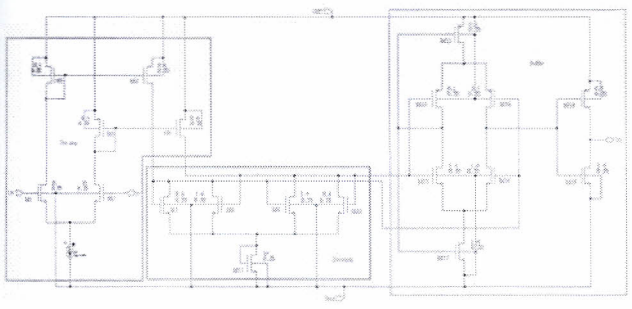
$$Vout(i) = 2 \times Vin(i) - \check{D}.Vrefn \quad (2)$$

And hold phase Φ3, at same multipliying phase with hold value residu voltage for next stage.

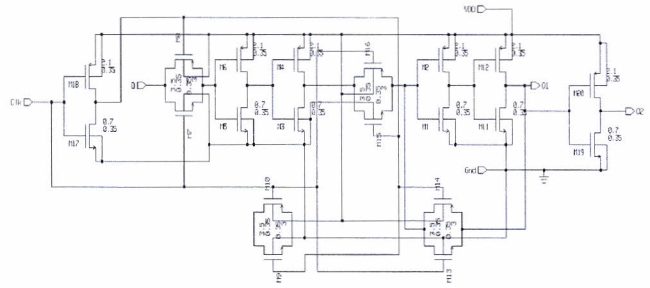
III. PRECISION COMPARATOR WITH LATCH

Precision comparator is implemented to each stage of the ADC. We prefer to use precision comparator then digital correction to minimize offset error of comparator and better output of ADC.

This comparator consists of three blocks: preamplifier, decision circuit and output buffer. First block is the input preamplifier which the circuit is a differential amplifier with active loads. The size of transistors M1 and M2 are set by considering the diff-amp transconductance and the input capacitance. Second block is a positive feedback or decision circuit, it is the heart of the comparator. The circuit uses positive feedback from the cross gate connection of M8 and M9 to increase the gain of the decision element. Third stage is output buffer; it is to convert the output of the decision circuit into a logic signal. The inverter (M18 and M19) is added to isolate any load capacitance from the self biasing differential amplifier. The complete circuit of comparator is shown in figure 4.



(a) Presicion comparator



(b) Latch

Figure 4. The Precision comparator with latch circuit

IV. OPERATIONAL AMPLIFIER

In this pipeline ADCs, operational amplifier is very important to get accurately result. We used an operational transconductance amplifier which has a gain of approximately 62,6dB for a bias current of 20 μA with Vdd = 3,3 V and Vss = -3,3 V. A value of loading capacitor is 0.275 Pf. The complete circuit is shown in figure 5. Transistors M9 and M10 functions as a constant current source, and transistors M8, M5 and M7 functions as two current mirror 'pairs'. The transistors M1,M2,M3,M4 are the differential amplifier.

Transistor M6 is an output amplifier stage. In the simulation, we got the resultat for phase margin (PM) was -140 degre, A gain was 62,2dB and Gain bandwidth product was 800 MHz as fig.6. A power dissipation mesured of 1,6mW.

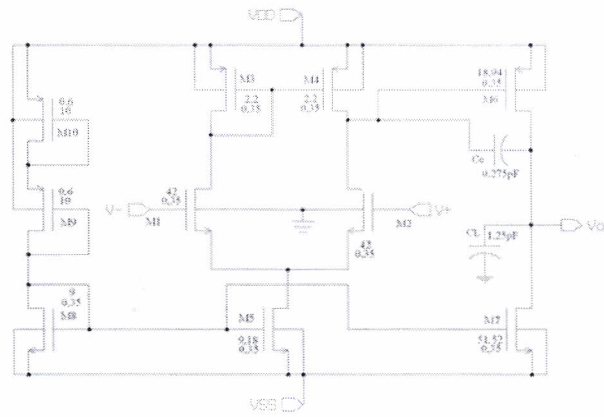


Figure 5 : Operational Tranconductance Amplifier

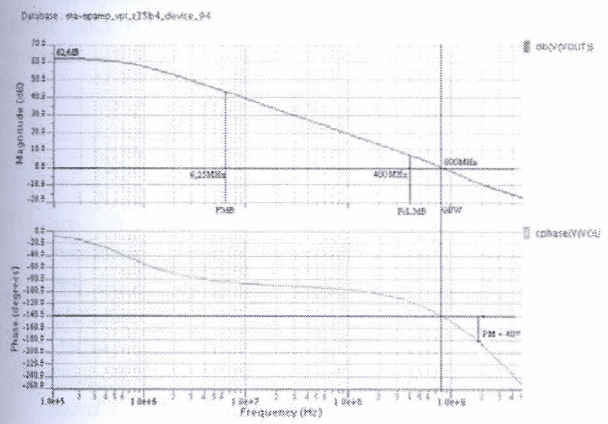


Figure 6: Opamp simulation

V. NON OVERLAPPING CLOCK

In the design pipeline A/D converter use non-overlapping clock is used to proces sampling , multiplying and hold. Each periode phase at 4,16ns, with used gate not and nand for delay frequency input 80MHz or 12,5ns. So clock used for delay latch circuit output comparator, the purpose keep output parallel. Complete circuit non-overlapping clock at figure 7.

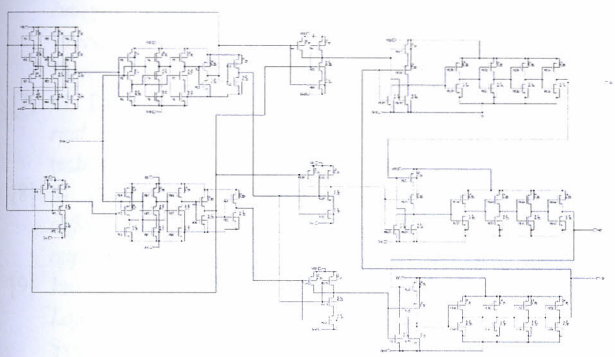


Figure 7. Non-Overlapping Clock Circuit

VI. RESULT

One stage A/D converter layout was estimated to occupy about 200 µm x 98 µm, it is seen at figure 8.

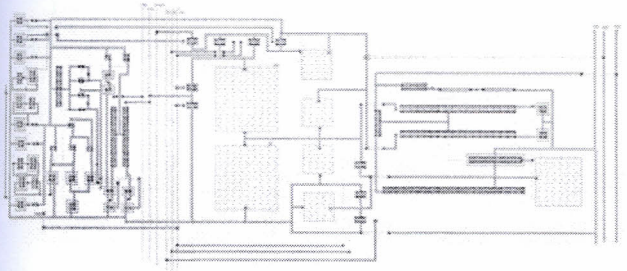
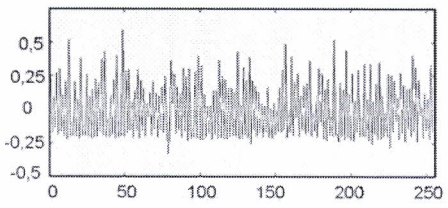


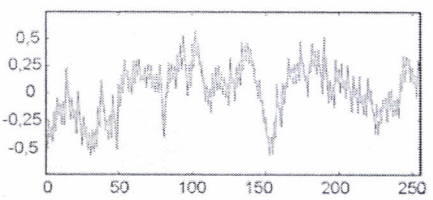
Figure 8. Lay-Out ADC Pipeline 1-bit/stage

Figure 9 shows the dc linearity of the ADC at conversion rate of 80 Msamples/s. In the figure 8(a), the code is plotted versus integral nonlinearity (INL) value and figure 8(b), the code is plotted versus differential nonlinearity (DNL). Note that since each simulation lasted 120 minutes, only 250 codes were tested. As shown, the worst INL is less than 0.6 LSB; the DNL is less then 0.6 LSB.

Figure 10 shows the result simulation output digital 8-bit ADC with vin = 0V for 2V, threshold voltage comparator = 1V and reference voltage 2V. the frequency clock at 80 MHz, periode simulation 3,2us as same voltage input 2 volt.



(a) DNL 0,6LSB



(b) INL 0,6 LSB

Figure 9. Curve of code DNL and INL

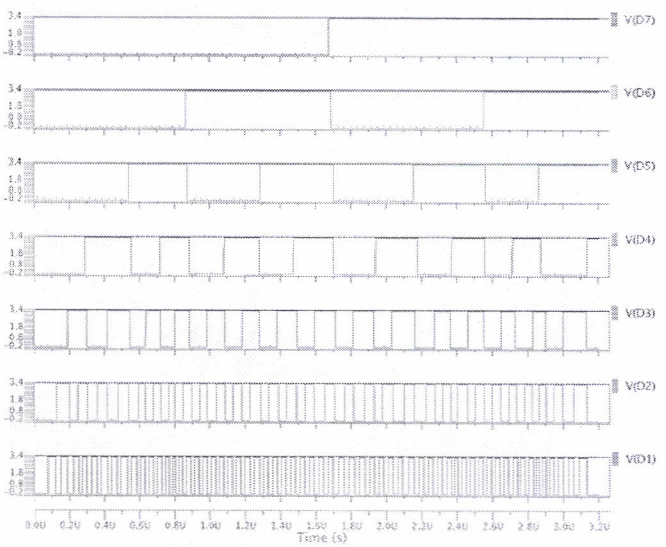


Figure 10. Result Complate 8-bit ADC Pipeline.

VII. CONCLUSION

The pipeline ADC 8-bits, 80 Msamples/s were implemented in 0.35µm technology CMOS Proces with total power dissipation 130 mW. Refer to result of experiment; the ADC can be implemented for high speed camera.

The system use topology one bit per stage with three phase clock with purpose good residu voltage and digital output.

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