Role of Contacts in Capacitance Measurements of Solar Cells Justin Davis, James Harger, Addison Wisthoff and Jennifer Heath Department of Physics, Linfield College, McMinnville, OR.

Abstract

The electronic properties of low cost, thin-film solar cells are complicated by the non-ideal nature of the semiconductor layers. Typically, the fundamental electronic properties of such materials are evaluated using current-voltage and capacitance-voltage measurements. However, in these devices, it is common for the back contact to be non-ohmic. We are exploring the impact of such a back contact on the outcome of standard capacitance-based characterization techniques. We compare computer models of capacitance response with measurements of simple model electronic circuits, and of solar cell devices.

Introduction

A Solar Cell is a photo-active diode which converts light into electrical energy. With multi-crystalline cells, ideal characteristics are no longer observed, complicating the solar cell model.



Figure 1: Solar Cells on TJ Day Hall of Linfield College, McMinnville Campus



Figure 3: SEM cross-section of a single crystalline silicon solar cell, showing secondary electron contrast (note that the surface is textured to enhance light absorption.)



Figure 2: layers in a typical solar cell.



Figure 4: Cross-section of a thin film *Cu*(*In*,*Ga*)Se₂ solar cell. Reproduced from [2].

PN Junction



Figure 5: Schematic of the p-n junction at the heart of the solar cell. Diffusion of free carriers across the p-n junction forms a charged region near the junction, resulting in an electric field and counteracting drift current. In equilibrium, these effects balance, creating a fixed region depleted of free carriers, the 'depletion region', of width W.







Numerical Models

After seeing the theoretical capacitance with an ohmic contact, it is interesting to analyze the effect a bad back contact has upon solar cells. A bad back contact resists the flow of current from the cell.



Figure 7: (a) An example of a band diagram for the semiconductor material with a back contact barrier. In order to model this, a voltage difference from the cell and contact was used. Model created with SCAPS [1]; (b) Numerical modeling for CV data using the model shown in (a).

(1)



Figure 8: (a) Results for a circuit model of a bad back contact; two back-to-back diodes. Inset: circuit diagram. (b) Recorded data for CIGS solar cell at 120K and room temperature. A bad back contact likely explains the low temperature results.



Figure 9: Analysis of data from Fig. 8, using the standard C-V analysis illustrated in Figure 6. (a) Results for each individual diode, and the back-to-back diodes show that the individual diode results can be recovered from back-to-back diode data at appropriate values of bias. (b) Results from the solar cell at 120K may illuminate differences between the top and back of the absorber layer.



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Circuit Results

Future Work

 More sophisticated modeling of current transport in a device. • Explore the nature of the back contact including the height, the dependence of temperature, and sample fabrication details.

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References

[1] M. Burgelman, et al., *Thin Solid Films*, **361**, 527 (2000). [2] Rockett, et al., Thin Solid Films **372**, 212 (2000). [3] T. Eisenbarth, et al., J. Appl. Phys. **107**, 034509 (2010).