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# Capacitance Measurements of Defects in Solar Cells: Checking the Model Assumptions

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**Capacitance Measurements of Defects in Solar Cells: Checking the Model Assumptions**


**Justin Davis**


A Thesis

Presented to the Department of Physics

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In partial fulfillment of the requirements

For the Degree of

BACHELOR OF SCIENCE

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## Thesis Acceptance

## Linfield College

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Date Submitted: May 2015

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# Abstract

Capacitance measurements of solar cells are sensitive to minute changes in charge in the material. For that reason, capacitance is used in several methods to electrically characterize defects in the solar cell. Standard interpretations of capacitance rely on many assumptions, which, if wrong can skew the results. We explore possible alternative explanations for capacitance transitions, such as a non-ideal back contact and series resistance. Using Drive Level Capacitance Profiling measurements, a capacitance step is linked to a defect between the energy bands of a solar cell.

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# 1. Introduction

## 1.1 Thin Film Solar Cells

Solar energy provides a viable option for future mass energy production. In 2013, around 0.3% of energy consumed came from solar conversion while the amount of solar energy hitting Earth was over 10,000 times the total energy consumed [1]. More efficient ways of harnessing and storing that energy would result in a viable energy alternative to oil and coal. Currently, researchers are trying to better understand thin film cells because they require less energy and cheaper materials to manufacture than other solar cells. Overall, the goal is a more cost effective means of creating electrical energy.

Most thin film cells are composed of polycrystalline material. Currently, the most efficient thin film solar cells are around 21% efficient [2]; meaning 21% of the total optical energy hitting the cell is converted into electricity. While this is amongst the higher conversion efficiencies for polycrystalline solar cells, there is still a lot of room for improvement. Theoretically, thin film cells can be up to around 30% efficient [3]. To reach this maximum, the movement of charge carriers inside the cell needs to be better understood.

To picture the movement of charged particles, the differential capacitance of cells is measured because it responds to minute changes in the charge of the material. The capacitance

measurements can then be interpreted to distinguish between different electronic properties of the cell.

Specifically, the source of a signal response in thin film cells will be analyzed. Currently, there is a description for the response which depicts a charge trap inside the material itself. This means that charge carriers are stuck inside the material and are constraining the flow of current. Other possibilities for the signal response are a bad back contact, where an energy difference between the cell and the outside circuit exists, and a thermally activated circuit response. These two suggestions could cause the analysis of defects in the material to be skewed, ultimately inhibiting the understanding of thin film cells.

# 2. Theory

## 2.1 Background

The simplest model of a solar cell is based on a pn junction between two semiconductor layers. Semiconductors have a band gap, difference in potential difference from its valence to conduction band, of around 1 eV. Additionally, cells have a conductive transparent contact on top which allows sunlight through and a grid on the top, as well as a back contact allowing charge carriers to flow from the cell, as displayed in figure 1.
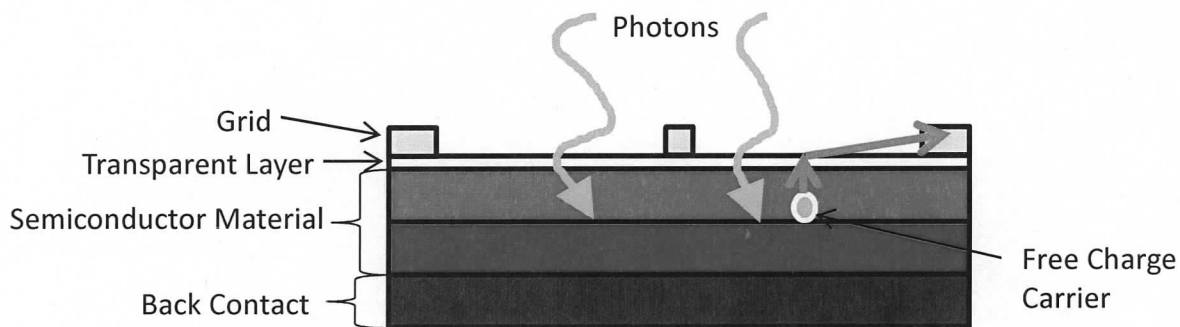


Figure 1. A basic set up for a solar cell and the different layers. The semiconductor material comprises the bulk of the solar cell. Sun light produces free charge carriers, which are then swept through the material from the electric field in the depletion region.

The semiconductor material is comprised of a junction between p and n type material. The p type is doped to have free holes. A hole is the lack of an electron in the atomic lattice, and being free refers to that it can move about the material. Conversely, the n type material is

doped so there are free electrons. It is important to note that these sides by themselves are

neutral.

When the p and n type materials are placed next to each other, they exchange charges.

The free holes migrate from the p to the n material, and the free electrons migrate from the n

to the p type material. This flow of charge is known as the diffusion current. The buildup of

charge creates an electric field and a current in the opposite direction, known as drift current,

which opposed the diffusion current. Once the solar cell reaches equilibrium, all of the free

charge carriers near the interface are swept out of the area, leading to an area with no free

charge carriers, called the 'depletion region' as shown in figure 2a. This region will be charged

because there will be missing electrons on the n side and extra electrons on the p side, causing

a difference in potential energy between the p and n sides. The difference in energy will cause

the p side to have a higher energy than the n side, as displayed in figure 2b.
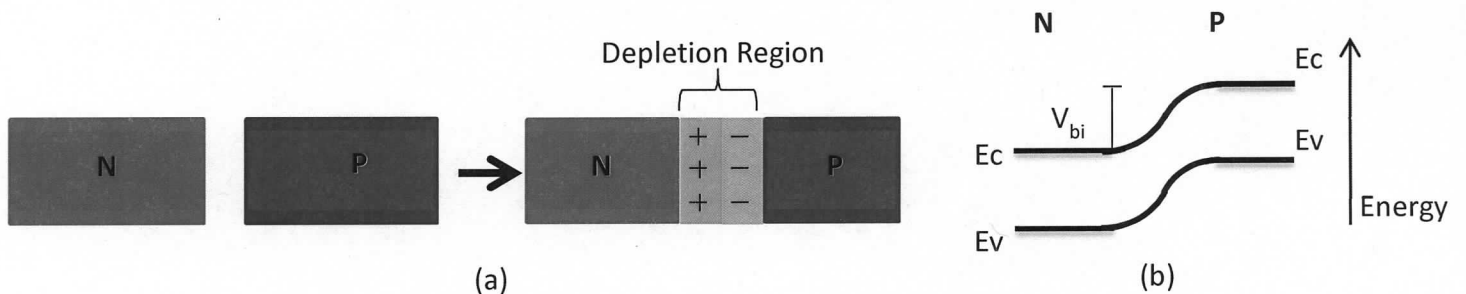


*Figure 2. Schematic for a PN Junction. (a) p and n material by themselves (b) When the P and N type materials come together, there is a built in electric field which sweeps free carriers away from the interface. This area without any free charge carriers is called the depletion region. The band diagrams for the p and n sides, along with the built in potential ($V_{bi}$) are displayed.*

The bending of the bands potential in the material occurs in the depletion region, and

the degree of bending is determined on the amount of doping in the material. Since the

number of charge carriers exchanged in each direction is the same, if the n side doped more

heavily than the p side, most of the bending will occur in the p region. This doping is typically

the case in solar cells.

The band bending in the depletion region indicates the presences of an electric field.

This electric field will push negative charge carriers towards the n side. This electric field then

makes the solar cell act similar to a diode, only allowing current to flow easily in one direction.

Differential capacitance is used in many methods to examine electrical properties of

solar cells. Differential capacitance is the change in charge over the change in potential, or can

be related to a solar cell by

$$C = \frac{dq}{dV} = \frac{\varepsilon A}{w} \tag{1}$$

where $\varepsilon$ is the dielectric constant, $A$ is the area, and $w$ is the depletion width.

Four experimental methods can be used to measure the charge response of the solar

cells, based on applying a DC bias, an AC bias, and changing the applied AC frequency. Each

method used will be described in detail below.

## 2.2 CV Analysis (Capacitance-DC Voltage)

One way to characterize the cell is through applying a DC bias. The bands respond based

on the density of free carriers in the p and n type material as displayed in figure 3. For these

bands, the n side is heavily doped compared to the p side. The n side being heavily doped

means that for a given area on the n side, there are a couple of orders of magnitude higher

more free electrons than free holes on the p side. Most of the depletion region will now reside

in the p side because more area in the p side will correspond to the same number of charge

carriers. Here, it will be assumed the entire depletion region is in the p side.

When no bias is applied, the solar cell will be in its normal equilibrium state as pictured in figure 3 b. Applying a reverse bias as in figure 3c, which corresponds to applying a positive potential to the n side, will further cause the exchange in charge carriers; increasing the potential between the p and n side, and creating a larger depletion width. A forward bias, as displayed in figure 3a, will do the opposite. Applying a negative potential to the p side decreases the depletion width. Based on the number of carriers in the material, a measurement of the capacitance can be derived where [4]

$$C = \sqrt{\frac{q\varepsilon_s N_B}{2(V_{bi}-V)}} \tag{2}$$

Looking at equation 2, it is apparent that if you plot $1/c^2$ vs the applied voltage, you should get a linear plot. This is referred to as a Mott Schottky Plot. Then, from the slope of the line, you can find the doping density of the material ($N_B$), the built in potential ($V_{bi}$), and the depletion width knowing the constants $q$, as the elementary charge and $\varepsilon_s$, the permittivity of the material. This analysis of an expected CV relationship is shown in figure 4.
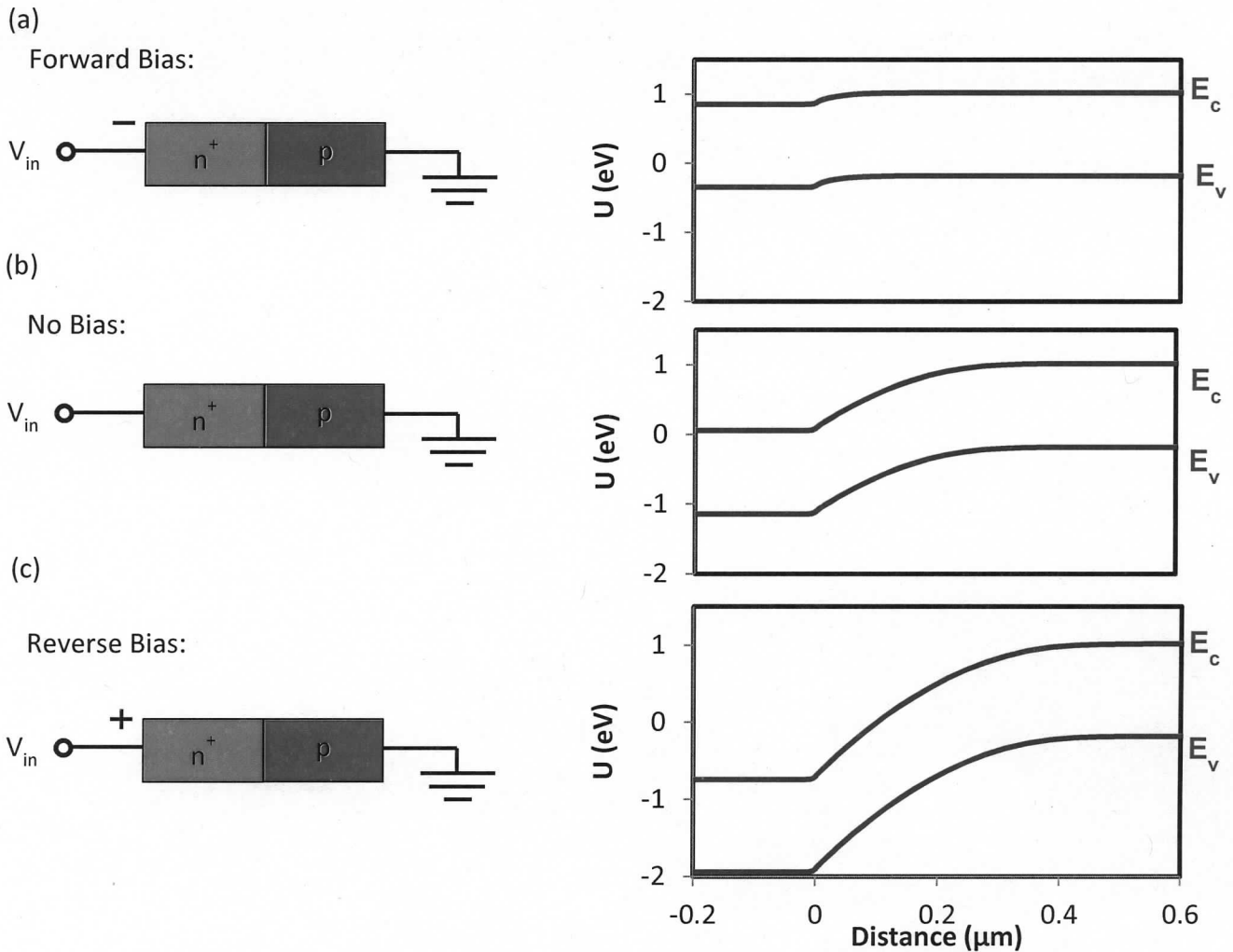
*Figure 3. The band diagrams and the applied bias for CV analysis. (a) For forward bias, a negative potential is placed on the n side, decreasing the potential difference between the p and n sides. (b) For no bias, the p and n sides are separated by a certain energy, known as the built in potential ($V_{bi}$). (c) For reverse bias, a positive potential is placed on the n side, increasing the potential difference between the p and n sides. These band diagrams were modeled using SCAPS [9].*

*Figure 4. (a) Ideal CV results. The capacitance rises rapidly in forward bias. (b) Mott Schottky Plot which gives a linear relationship and characterizes the cell using equation 2. Modeled using SCAPS [9].*

## 2.3 Admittance Spectroscopy (Capacitance-frequency)
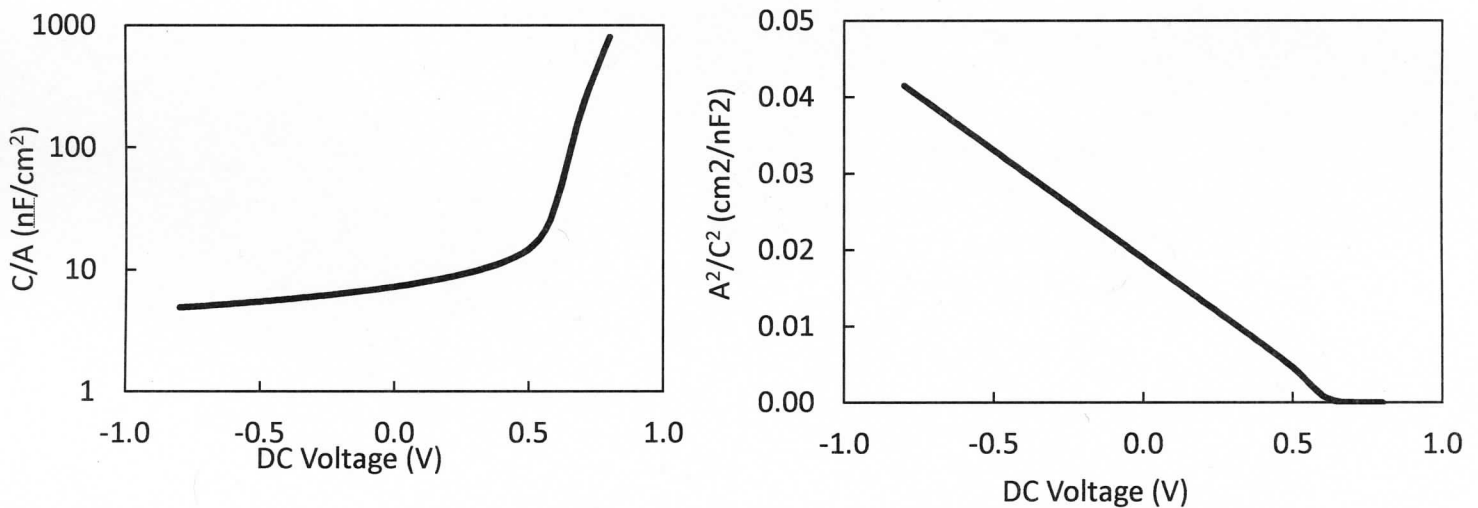
Admittance spectroscopy is used to measure the energy level of a charge trap inside of the band gap of the material. These traps allow free charge carriers to move inside them, and while filled, the trap inhibits the flow of charges in the cell. Charge carriers are able to escape the trap based on thermal and statistical probabilities. Charges escaping can be related to a characteristic time corresponding to the energy level of the defect. The time it takes for charge carriers to escape the trap is examined by applying an AC bias and varying the frequency while measuring the capacitance. At low frequencies, the AC bias does not inhibit the flow of charge carriers from the traps; they are able to move in and out of the trap at a normal rate.

However, as the frequency is increased, the charge carriers have smaller and smaller amounts of time to escape the trap. Once a critical frequency is reached, charges

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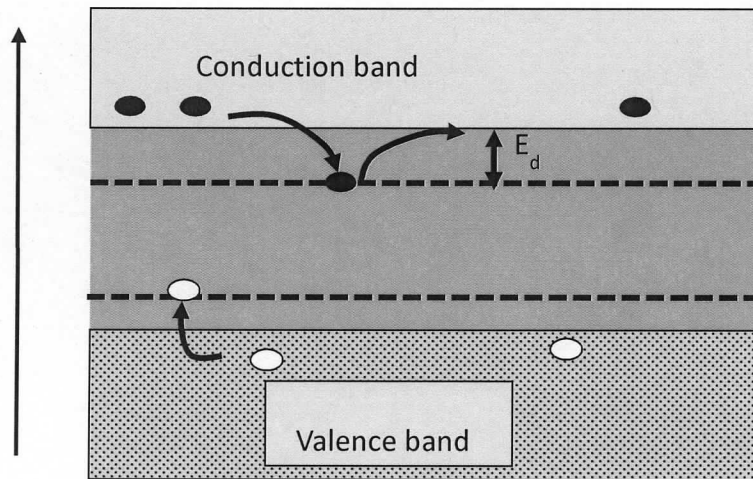
electron energy

*Figure 5  Schematic of a defect energy level inside the bands of a solar cell. Charge carriers may move in and out of these traps. The time it takes for charges to move in and out of the cell can be used to characterize the energy level of the defect.*

are stuck in the trap and no longer add to the capacitance measurement of the cell. Charges

being trapped lead to a drop in capacitance as shown in figure 6.



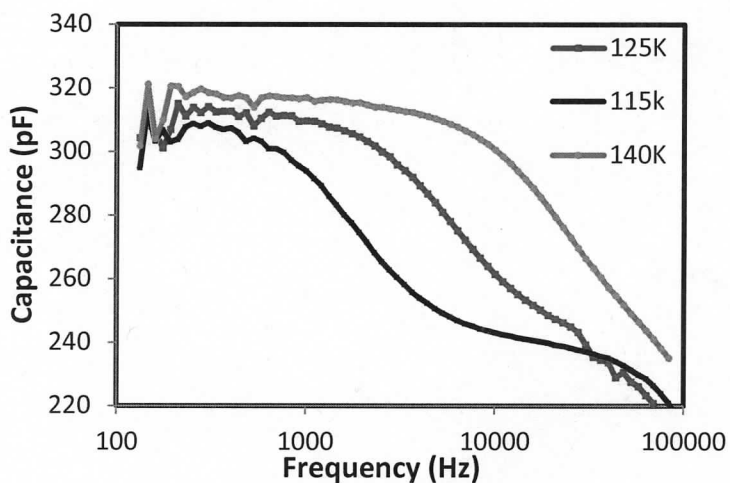*Figure 6.  A typical capacitance step seen for a defect as the AC frequency is increased. This data was taken on a thin film CIGS solar cell at different temperatures.*

By analyzing the step in figure 6 the energy level of the defect can be found. This can be

done using a relationship modeling the emission rate of charge carriers, $e_n$ from the defect [5]:

$$e_n = \gamma \sigma_{na} T^2 exp[-\frac{E_{na}}{kT}]$$

(3)

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where $\sigma_{na}$ is the capture cross section for electrons, $\gamma$ is a thermal prefactor, $T$ is temperature, $E_{na}$ is the energy level of the defect, and k is Boltzmann's constant. The emission rate can then be related to the applied frequency of the AC bias. Capture or emission of charge at the trap can only be observed for values of the frequency when the emission rate is greater than the angular frequency. Equation 2 can then be rewritten to model the different energy levels still able to respond, $E_e$ for a certain applied frequency [5]

$$E_e = kTln\left(\frac{\gamma\sigma_{na}T^2}{\omega}\right) \qquad (4)$$

To model the energy level of defects, the frequency corresponding to the largest change in capacitance needs to be found. This frequency can then be used with equation 3 to model the energy level of the trap.

## 2.4 Thermally Activated RC Circuit

One possible explanation for the response in figure 6, other than a defect in the material, is a thermally activated RC filter [7]. In order to show this is not the case for our samples, we measured the current as a function of voltage from the cell at different temperatures. From the current voltage relationship, the resistance of the cell could be found using Ohm's law. Once the resistance of the cell is found, the measured capacitance from the CV analysis can be used to find the capacitance. Once the resistance and capacitance are known, the RC time constant can be calculated and the capacitance step can be analyzed to see if it really is acting similar to a low pass RC filter. Our data showed this is not the case.

## 2.5 Drive Level Capacitance Profiling (DLCP)

To determine the origin of the signal response shown in figure 6, DLCP was used. Specifically, the effect of the back contact on admittance spectroscopy came into question

DLCP is a strictly AC measurement which yields the density of carriers in the material and the location of the first charge response. Since it is an AC bias, the frequency can explicitly be chosen.

Determining what frequency to use for DLCP measurements is crucial. In order to test the effect a charge trap has on the material, analyzing Cf data similar to figure 6 is useful. Two frequencies, one lower than the admittance step and one higher the admittance step, are chosen. The higher frequency should result in a lower density of carriers because charges will be stuck inside the trap, unable to respond. Additionally, the position of the charge response should remain the same. This is because the defect inside the main junction should stay in the same position relative to the back contact.

DLCP uses a number of AC amplitudes, while shifting the waves to keep the maximum applied bias ($V_{ac}$) the same as illustrated in figure 7a. This ensures that the same location inside the depletion region of the cell is being measured. Because a small signal approximation is no longer accurate, the capacitance measurement needs to be fit with a higher order relationship as a function of $V_{ac}$ as follows

$$dQ = C_0 dV + C_1(dV)^2 + C_2(dV)^3 + \cdots \tag{5}$$

which is similar to equation 1. However it no longer has the linear relationship, as shown in figure 7b. $C_0$ can be used to approximate the capacitance of the cell. Furthermore, the values of $C_0$ and $C_1$ can be used to find the density of carriers [8] where:

$$N_{DL} \equiv -\frac{C_0^3}{2q\varepsilon A^2 C_1} = p + \int_{E_F}^{E_V+E_e} g(E,x)dx \tag{6}$$

Along with the density of carriers, the first moment of charge response, <x>, can be estimated with the capacitance [5] where

$$<x> = \frac{\varepsilon A}{C} \tag{7}$$

If this value stays constant, it can be assumed the location inside the material being measured is not moving.
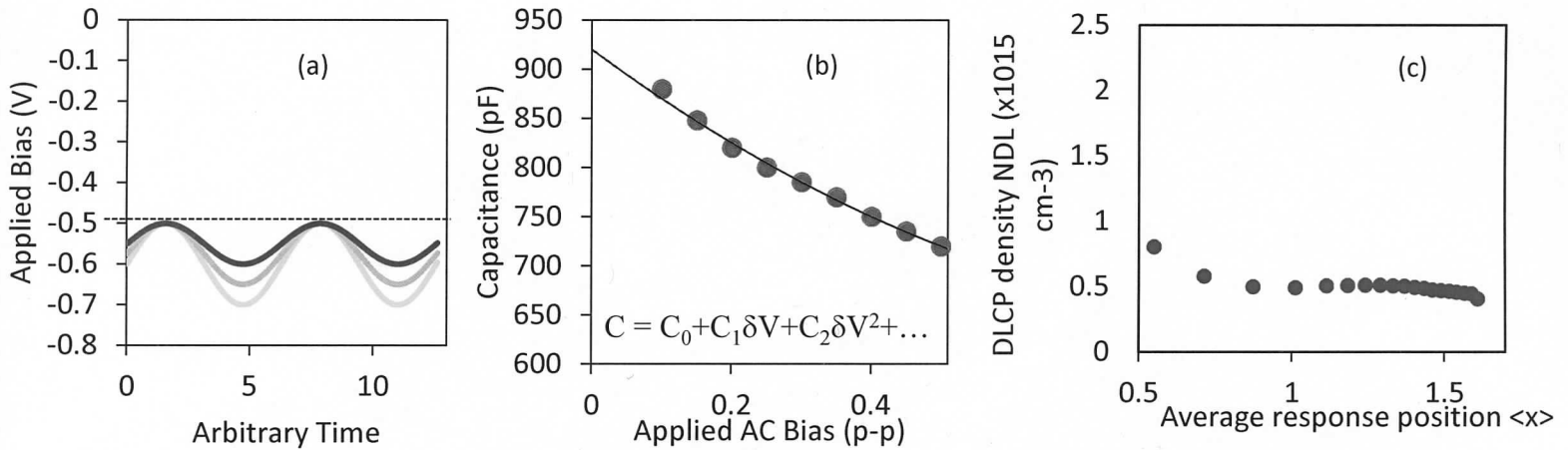


Figure 7 (a) Method of varying $V_{ac}$ during the DLCP measurement so the measurement location remains constant. (b) Capacitance dependence on $|V_{ac}|$. $C_0$ and $C_1$ are used to find the density of carriers ($N_{DL}$). (c) Variation of $N_{DL}$ with average measurement location <x>.

# 3. Experimental Methods

## 3.1 Experiments/Methods

The solar cell samples studied were thin film $Cu(In_{x-1}G_x)S_2$ cells grown on a molybdenum back contact at the University of Delaware. To take measurements, the solar cells had to be prepped. Starting out, a small square of the CIGS material was scratched out to ensure the capacitance measurements were in the range our equipment could measure.

To measure the area of this square, which is important to know for capacitance measurements, the cell was placed next to a meter stick and a picture was taken. ImageJ software was used to find the area [6]. Using imageJ, you can calibrate the distance of a number of pixels of a picture. The meter stick allowed us to calibrate a known distance, and then area of the square was found.

The square we etched out was then connected to a copper wire to create the front contact. Since the cell was grown on the back contact made of molybdenum, another piece of the cell was etched off so it could be accessed. Then a small copper wire was soldered on to connect the solar cell with the electrical circuit.

Next the solar cell sample was mounted on a rod and placed inside the cryostat. The

cryostat connected to various electrical devices to take measurements on the solar cell. The

experimental set up with the various electrical devices is shown in figure 8.
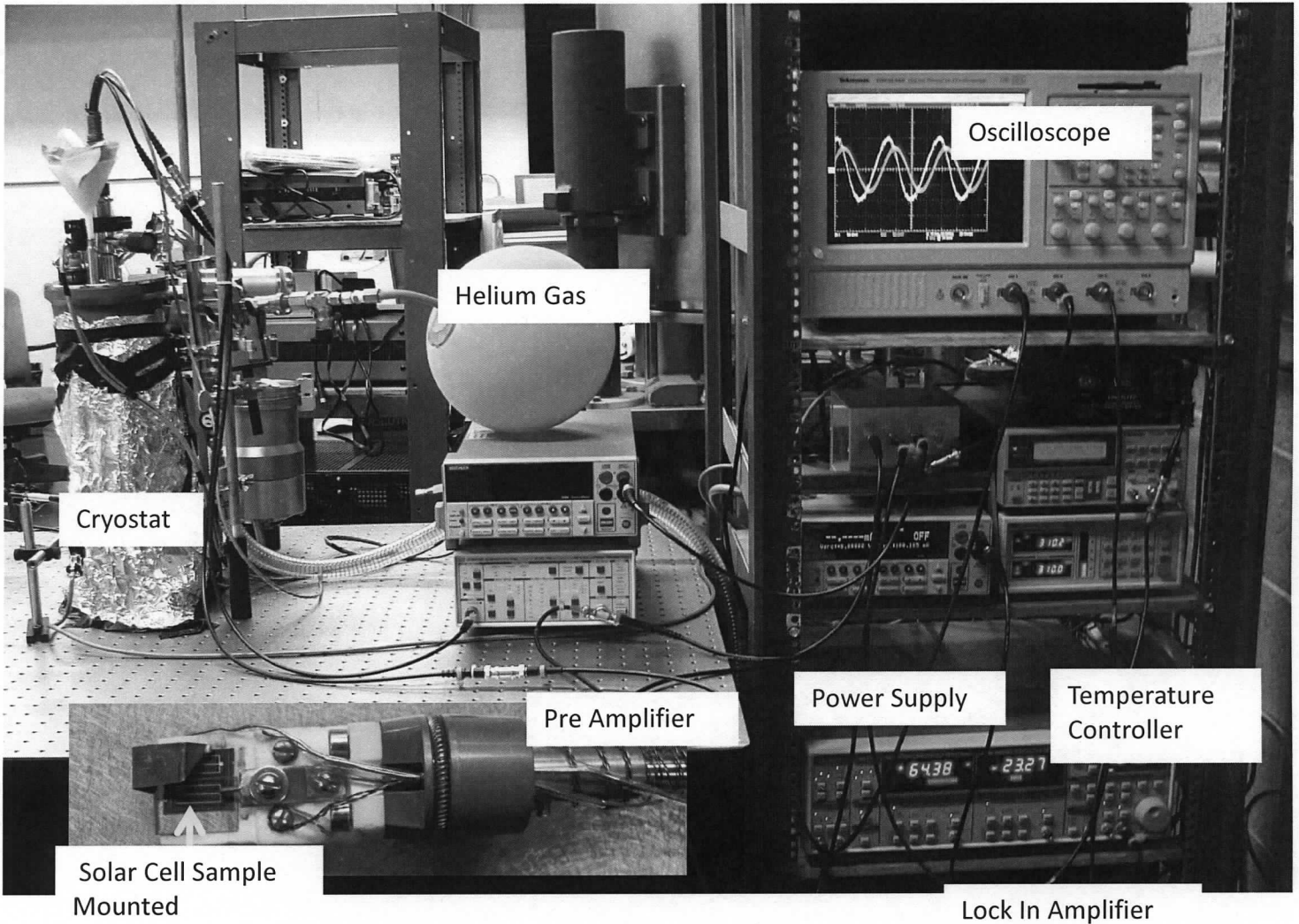


*Figure 8. Experimental set up with different apparatuses labeled. A solar cell sample is mounted on a rod and placed inside the cryostat. The cryostat and sample are then cooled down between 80 and 150 Kelvin using liquid nitrogen. The cryostat is connected to the various electrical equipment so the solar cell can be measured.*

Once the sample was secure inside the cryostat, the inner chamber of the cryostat that held

the sample was filled with helium. Helium is a good thermal conductor and helped ensure the

sample was at a desired temperature. This meant the normal air had to be removed first. This

was done using a rotary vane pump to rough out the chamber and then a balloon filled with helium was used to backfill the chamber. The vacuum and balloon were connected to the cryostat through different gauges.

After purging the inner chamber, the solar cell was then cooled down using liquid nitrogen. Liquid nitrogen's boiling point is 77 Kelvin, which allowed the sample to be cooled to between 80 and 150 Kelvin for different trials. The sample was cooled down for a number of reasons. One reason was in order to see the defect response in AS. At higher temperatures, a much higher frequency than we were capable of applying is needed to see the signal response. Additionally at lower temperatures, less charge carriers are moving throughout the solar cell, leading to larger reactions with small applied biases. In order to avoid metastable changes, the sample was left at 310 Kelvin overnight between taking measurements.

Liquid nitrogen was poured into the top of the cryostat through the funnel pictured in figure 8. Then an internal heater reheated the liquid nitrogen gas to adjust the temperature of the sample. The temperature controller followed a PID algorithm which kept the actual temperature of the sample close to the desired temperature. For each measurement, twenty minutes after the heater reached a desired temperature was given to ensure the sample reached the chosen temperature. Finally measurements could be taken of the sample.

For many of the experiments, the current was measured yielding the capacitance of the sample. From equation 1, the capacitance is change in charge over the change in potential. Taking the derivative with respect to time of both the charge and potential gives a relationship including current ($\frac{dq}{dt}$). The change in potential with respect to time then was found by applying a small AC bias with the lock in amplifier. An AC bias with an amplitude of 20 mV was applied

and from there the capacitance of the system could be calculated. This process is shown in equation 8.

$$C = \frac{dQ}{dV} \rightarrow C\frac{dV_{ac}}{dt} = I_{ac}$$ (8)

Thin film cells can be modeled as a resistor and capacitor in parallel meaning the response for each are around 90 degrees out of phase. Using a lock in amplifier, the resistance and conductance phases can be distinguished.

## 3.2 Current Voltage (IV) Measurements

Current Voltage measurements required a power supply and a computer program that swept through a range of voltages and measured the capacitance. A voltage was placed across the sample, and the output current was measured. Normally, we swept from -1.0V to 1.0V in increments around 10 mV. A maximum current output was controlled from the power supply so the solar cell was not overloaded. These measurements were very quick. The IV data were then directly saved onto the computer and could be opened into an excel file. Sometimes we swept further into forward bias to see if a bad back contact was significantly affecting the behavior of the cell.

## 3.3 Capacitance Voltage (CV) Measurements

Capacitance Voltage measurements were used to find properties of the material from the capacitance relationship in equation 2. Additionally, they were used to examine the effect of a bad back contact present in the CIGS sample. For CV measurements, a power supply, lock in amplifier, preamplifier, and oscilloscope were used. Since the differential capacitance is the

change in current over the change in voltage, an AC bias of 20 mV was applied. Then for each DC bias, the capacitance of the cell was measured.

## 3.4 Admittance Spectroscopy- Capacitance frequency (Cf) Measurements

Capacitance frequency measurements are used to describe a trap charge between the bands of semiconductor material. In order to take Cf measurements, a power supply, lock in amplifier and a preamplifier were used. The power supply was used to ground the system for these measurements to ensure no stray DC bias affected the measurements. The lock in amplifier then swept through a range of frequencies, usually from 100 Hz to 10 kHz that were applied to the sample. Similar to the CV measurements, the current out of the cell was then used to determine the capacitance with the preamplifier. A computer program was used for these measurements to sweep through the frequencies and measure the capacitance.

## 3.5 Capacitance Voltage frequency (CVf) Measurements

Capacitance Voltage frequency measurements were used to see if a DC bias changed the charge trap energy level from normal admittance spectroscopy. From equation 3, the energy level of the defect should not change with a DC bias. For the CVf measurements, a DC bias ranging from -1.0V to 1.5V in by 0.2V increments was applied while taking Cf measurements. This required a circuit element to combine AC and DC biases to apply to the sample. Moving into forward bias, the capacitance step would disappear. The disappearance was possibly due to applying a higher DC bias than the built in potential of the solar cell, causing the

measurements to stray from ideal behavior. Once the capacitance step disappeared, no more measurements were taken.

## 3.6 Drive Level Capacitance Profiling (DLCP) Measurements

Drive Level Capacitance Profiling measurements were used to decipher between a bad back contact and a charge trap between the bands for the CIGS samples. For these measurements, two power supplies, a preamplifier, lock in amplifier, oscilloscope, and a computer program were used. The computer program was initially written to only apply a reverse bias to the sample. This is why both power supplies needed to be used. A constant DC bias was applied by one of the power supplies which was not connected to the program. Then, the other power supply was controlled and ran from some reverse bias to 0V. When it got to 0V, the other power supply would then be applying a forward bias, so we reached as far as positive 1.5V. Since DLCP allows the user to pick a certain frequency to record measurements at for an applied AC bias, both a low and a high frequency were used. The high frequency corresponded to the position when charge carriers should be trapped inside the defect of the material. A significant difference between charge carriers between a low and a high frequency points to a trap inside the cell, rather than a bad back contact.

# 4. Results and Analysis

## 4.1 Numerical Modeling

A number of thin film devices were characterized. These thin film cells, made of Copper, Indium, Gallium, and Selenide (CIGS), were analyzed using the before mentioned methods. The first non-ideal attribute examined was a bad back contact. To understand bad back contact behavior, numerical modeling was used through a program called SCAPS [9]. A heavily doped pn junction was used to model a solar cell. Additionally, a back contact of 0.5 eV was assigned to the pn$^+$ junction, and the CV relationship shown in figure 9 was found.
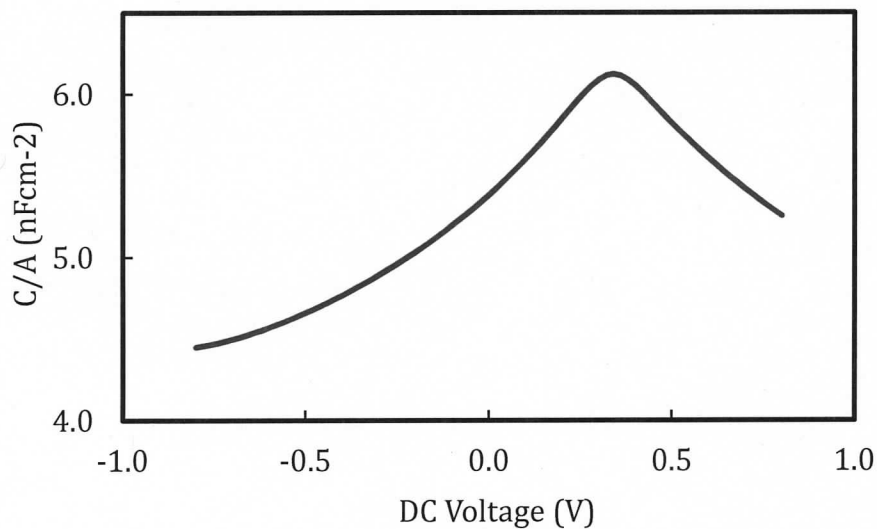


*Figure 9. Numerical CV relationship for a cell with a bad back contact of height 0.5 eV [9]. The back contact controls the capacitance measurement in forward bias [10].*

## 4.2 CIGS Cell Displaying a Bad Back Contact

       The CV relationship in figure 9 shows a rollover effect on the capacitance measurement of the pn$^+$ junction. Since the only difference from this numerical model and the CV characterization shown in figure 4a is a bad back contact, it was hypothesized the back contact was taking over the capacitance measurement of the cell. The next step was to match our numerical results with measurements taken on an actual thin film cell. A CIGS cell was measured that was thought to display back contact behavior. Figure 10a shows the CV measurements.
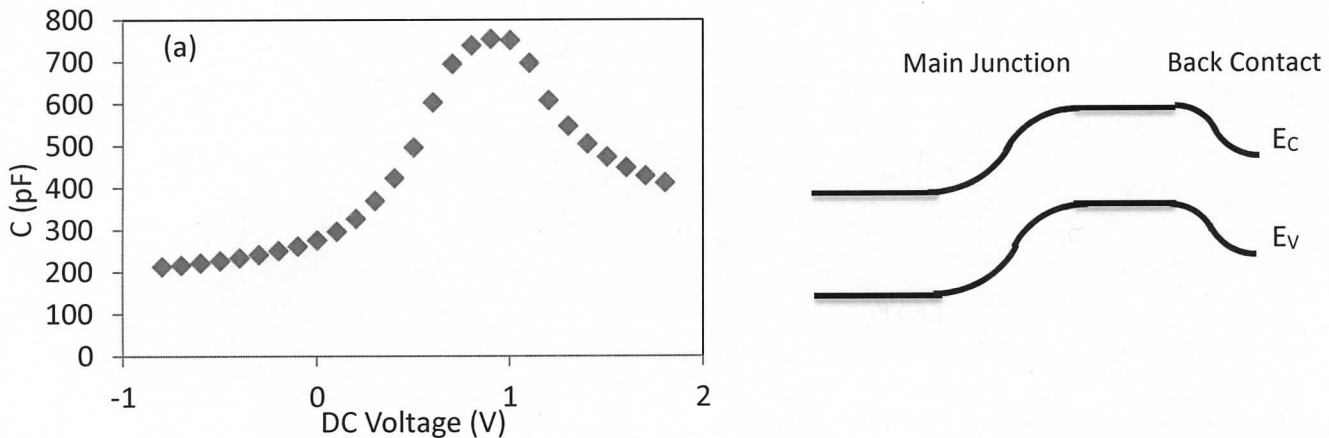


*Figure 10. (a) CV profiling for CIGS sample D934#1. Normal CV profiling to 0.5 V forward bias, and then there is a roll over effect where the Capacitance drops back down. (b) Band diagram for a bad back contact. The back contact has its own depletion region with opposite orientation of the main junction. As the cell is put into forward bias, the back contact is subjected to reverse bias and eventually takes over the capacitance measurement of the cell for CV measurements.*

       The rollover effect of the thin film's capacitance displayed in figure 9 is very similar to the numerical results in figure 10a. This led us to believe the sample did have an energy barrier at the back contact restricting the flow of current. Figure 10b shows this energy barrier in a

similar relationship as the main junction of the cell. The back contact has its own depletion region that is aligned in the opposite direction of the main junction. This means when the entire cell is under a forward bias, the back contact is put under a reverse bias, causing the back contact's depletion width to increase. Since capacitance is proportional to the inverse of depletion width from equation 1, it causes the capacitance measurement to decline and therefore takes over the capacitance measurement of the cell [10].

## 4.3 Admittance Spectroscopy with Bad Back Contact

The back contact behavior's influence on admittance spectroscopy then came into question. The admittance response was always thought to come from charge traps between the bands of the thin film cells, but a model with a bad back contact could change the admittance spectroscopy relationship entirely.

The same sample was tested to see if the admittance step displayed a non-ideal relationship. The results are shown in figure 11.
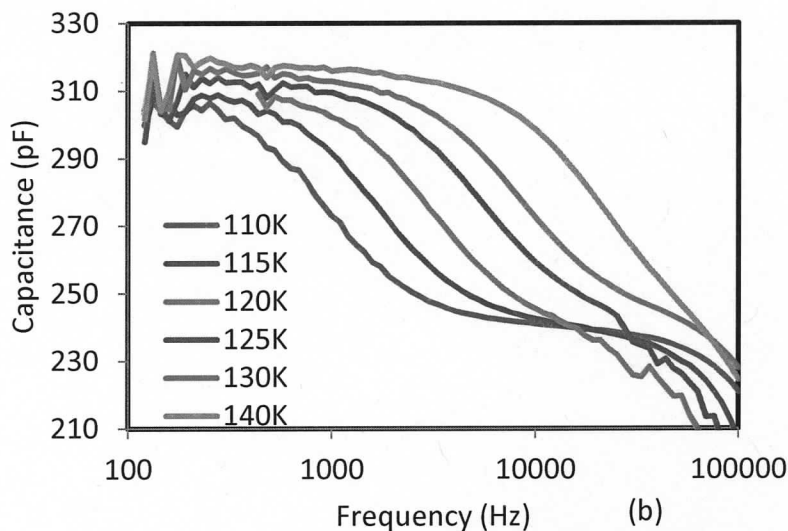


*Figure 81. Cf data for cell D934# showing the capacitance step thought to come from a defect in the material for a range of temperatures.*

The shape of the admittance spectroscopy appears similar to figure 6 and it clearly shows a drop in capacitance. Next, the energy level of the trap charge was found to see if it resembled the energy height of defects commonly found in CIGS samples.

In order to find the energy level of the defect in the material, the moment where the capacitance changed the greatest in the Cf data was found. This is the frequency where the capacitance reading in the admittance spectroscopy is changing the most. This frequency stands for the point where charge carriers are no longer able to escape the charge trap inside the bands of the material. This frequency can then be correlated to the energy level of the defect using Equation 3. This process is shown in figure 12.
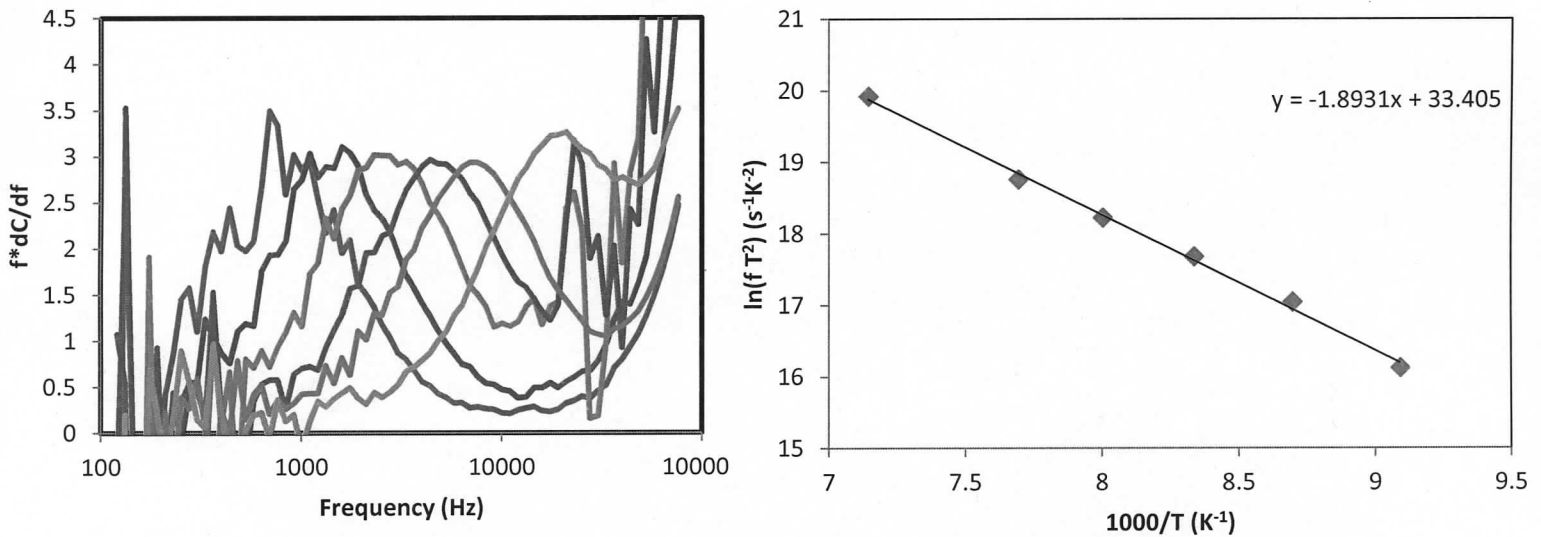


Figure 92. (a) Analyzing the signal response from figure 11. The peaks correspond to the critical frequency, where the charges are trapped inside the defect in the material and no longer contribute to the capacitance signal.(b) Arrhenius plot of the peaks yielding the energy barrier of the defect to be 120 eV.

For this sample, the trap state was measured to be 120 meV from the y-intercept in figure 12b. This is an expected value, since the trap in CIGS devises is normally around 100 meV [10].

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The admittance spectroscopy for a cell with a bad back contact exhibited the same capacitance response as a cell without a measured bad back contact. This led to questioning if the response could instead come from a charge interaction with the back contact.

## 4.4 Capacitance Voltage Frequency Results

One idea to rule out the back contact's influence on the admittance spectroscopy was to apply a DC bias and see if the energy level of the charge trap was altered. Since a DC bias changes the width of the depletion region at the back contact, if it was the reason for the response step then there should be a shift in freeze out frequency as the back contact energy barrier increases. If the back contact played no role, then the applied DC bias should have no effect on the frequencies of the step in the admittance spectroscopy measurements. This is due to equation 3 where the emission rate of electrons from a trap has no dependence on DC bias. The results of applying a DC bias at 130K for the sample are shown in figure 13.
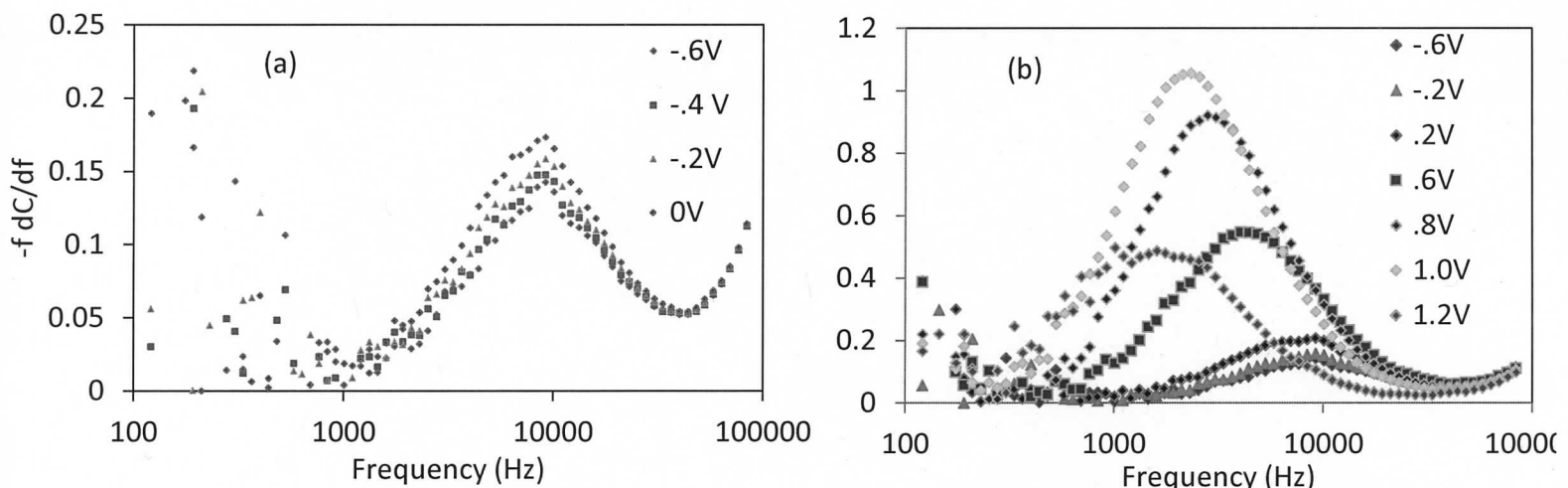


Figure 103.  Analyzing Cf data with different applied DC bias'. (a) Zoomed in of the reverse bias. It is apparent there is no shift in the critical frequency, or emission rate, for charge carriers. (b) There appears to be a shift in emission rate in forward DC bias.

The data in figure 13a shows no shift in emission rate for reverse bias. This is expected because the main junction of the cell is dominating the capacitance measurement, and the back contact should be so small it does not affect the cell overall. However, the data also shows an apparent shift in the emission rate of electrons for the sample in forward bias in figure 13b. Since the back contact depletion region increases as we move into forward bias, it should dominate these measurements. The energy barrier at the back contact is increasing, which would correspond to a lower frequency needed to freeze out the carriers and lead to the capacitance step.

## 4.5 Drive Level Capacitance Profiling Results

In order to decipher between the bad back contact and the defect in the material, DLCP was used. DLCP allows us to measure capacitance as a purely AC measurement. This means the frequency is held constant. In order to pick what frequency to run the measurements at, the Cf response in figure 11 was used. Looking at the response for 130K, a frequency below the step of 1 kHz and a frequency above the step of 30 kHz were chosen. It was expected that if the charge trap inside the bands was responsible for the admittance step, then there should be a significant difference in the density of carriers. This is due to the charges being trapped and not able to respond at the higher frequency. The results are shown in figure 14.
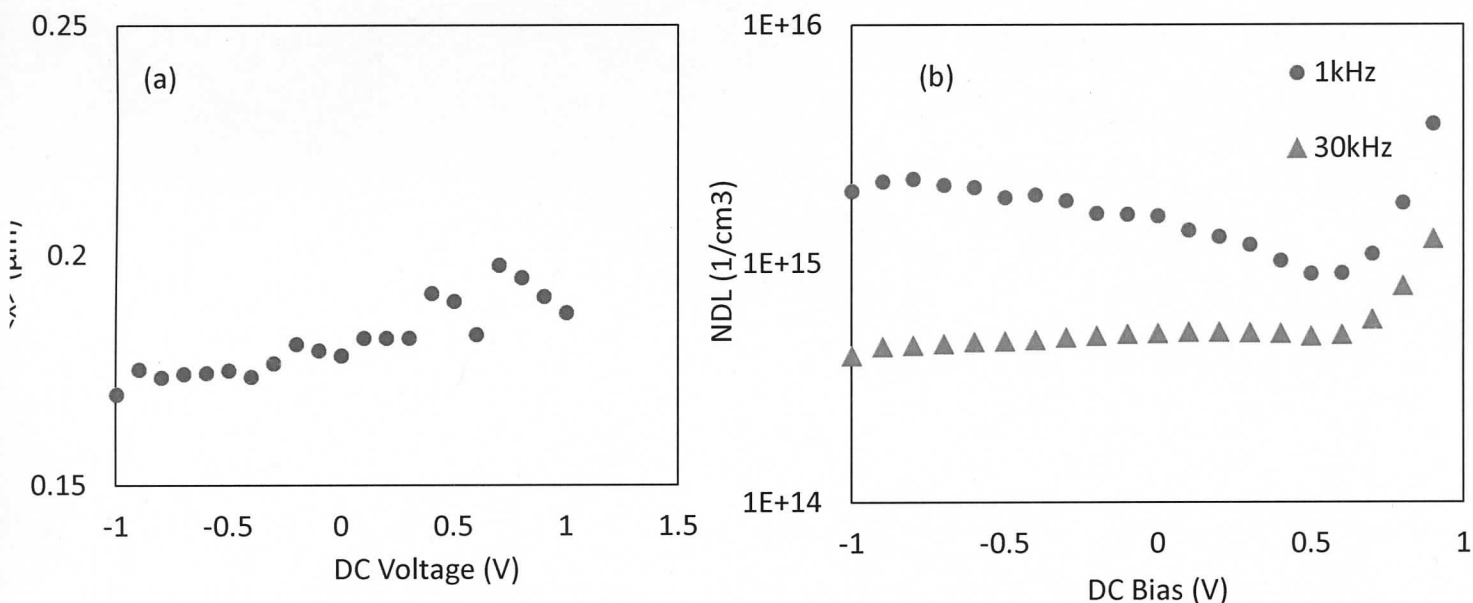
*Figure 114. (a) The distance inside the cell where the response is seen, <x> , remains roughly the same for a given applied DC bias. (b) The density of carriers at different frequencies. One above the capacitance step, one in the middle and one above. There is a significant decrease at the higher frequency, resembling the presence of a defect.*

Both the distance of the first charge response in the cell, <x>, and the density of carriers were significant. The first charge response does not shift for the entire trial. This means the location of charge response is inside the material, and not coming from the bad back contact. Additionally, between the low and the high frequencies, there is a significant difference of charge carriers responding in the material as shown in figure 14b. Since the higher frequency displays a lower density of carriers, it reveals charges are stuck inside a defect in the material. This defect is the trap that lies between the bands. Ultimately, it is apparent this defect is the reason for the admittance step seen in figure 11.

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# 5. Conclusions

A thin film solar cell with a bad back contact was measured and analyzed using standard capacitance profiling. The role this bad back contact in admittance spectroscopy measurements came into question and the possibility that the back contact causes the admittance step was investigated. The back contact's role in admittance spectroscopy was shown to be small compared to other factors. Instead, like previously thought, a charge trap in between the bands of the material is responsible for the admittance step. This conclusion resulted from the DLCP measurements where a large difference in the density of carriers for different frequencies was evident. However, from the energy shift in figure 13, there is a possibility the back contact does contribute to the response.

Other samples that display a bad back contact need to be characterized to see if these results can be replicated. Additionally, comparing admittance spectroscopy results between two solar cells, one that displays a bad back contact and one that does not, could be very useful in figuring out the role the bad back contact plays. This could be done through numerical modeling as well.

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