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**DEVELOPMENT OF A PROCESS FOR FABRICATING HIGH ASPECT RATIO
PARYLENE MICROSTRUCTURES**

By

**Asma Waqar,
B.Tech. Jawaharlal Nehru Technological University, 2000**

**A Thesis
Submitted to the faculty of the
Graduate School of the University of Louisville
in partial fulfillment of the requirements
for the Degree of**

Master of Science

**Department of Electrical and Computer Engineering
University of Louisville
Louisville, Kentucky**

May 2006

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PARYLENE MICROSTRUCTURES**

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Thesis Approved on

January 27th, 2006

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ACKNOWLEDGEMENTS

I would like to acknowledge and appreciate the continuous support from the professors and the research assistants during the progress of this thesis. Firstly, I would like to acknowledge Dr. Kevin Walsh, my thesis director, who has been a constant source of knowledge and inspiration. I am grateful to the members of my thesis committee for their encouragement and guidance. Special thanks to Mark Crain, Michael Martin, Usha Gowrishetty, Glenna Haberzette, Alex Isham, Thomas J. Roussel, Mehdi Yazdanpanah, Radhika Mani and Gopi Bhimarasetti for their contribution and advice.

ABSTRACT

PARYLENE (poly-para-xylylene) is mostly used as a conformal protective polymer pin-hole free coating material to uniformly protect any component configuration on diverse substrates. This thesis describes in detail how the unique properties of parylene can be conveniently combined with MEMS technology to meet biocompatibility requirements of biological and chemical applications and develop unique microstructure shapes. Since etching of parylene is not readily possible, the best way to mold it into any shape would be to etch hollow molds in silicon and deposit parylene in them. It is easy to etch away the silicon mold for releasing these parylene structures. Parylene is non-reactive in wet etchants (like TMAH or KOH) that are used to etch silicon. These microstructures can be helpful in implants and other biomedical applications.

This technique allows for the production of unique microstructures, many of which are not realizable by other fabrication technique. Any other material that conforms easily in silicon molds and is non-reactive with silicon and silicon etchants, can be molded in the shape of the fabricated molds. A material that is tested for these properties can be deposited because most of the fabrication processes (like etching, lithography, oxidation and wafer bonding) are performed only on silicon for preparing the molds. Materials deposited by CVD (chemical vapor deposition) or less viscous liquids that solidify on cooling, can be investigated for deposition in molds. Many useful applications

can be derived by combining this method with various materials.

CAD tools were used to simulate the mask features for designing this microstructure and to layout the photomask pattern. A fabrication procedure is devised from these simulation results and the process is implemented in a Class 100/1000 Cleanroom facility at the Lutz Micro/Nanotechnology Cleanroom core facility, University of Louisville. A complete guide to fabricate this MEMS-based parylene structure is provided in this thesis project. Important observations, complete experimental procedure and results are discussed in detail.

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CHAPTER 1

INTRODUCTION

This thesis describes in detail how the unique properties of parylene can be conveniently combined with MEMS (Micro Electro Mechanical Systems) technology to meet biocompatibility requirements of biological and chemical applications and to develop unique microstructure shapes. High aspect ratio molds are fabricated in silicon or similar substrate, followed by deposition of PARYLENE (poly-para-xylene). Parylene conforms to virtually any shape, including sharp edges, crevices, points or flat and exposed internal surfaces. The surface is then etched away in order to release the parylene structures, which now take the shape of the original molds (Fig. 1). Due to the biocompatible nature and barrier properties of parylene, these microstructures can be used for implants and similar biomedical applications, such as parylene micro-tacks for the attachment of implanted micro-device to a tissue.

1.1 Biocompatibility

During the last two decades significant advances have been made in the development of *biocompatible* and *biodegradable materials* for biomedical applications. In the biomedical field, the goal is to develop and characterize artificial materials or, in other words, "spare parts"[1] for use in the human body to measure, restore, and improve physiologic function and enhance survival and quality of life. The European Society for

Biomaterials (ESB) defined "biocompatibility" in 1986 as “the ability of a biomaterial to perform with an appropriate host response on a specific application” [2]

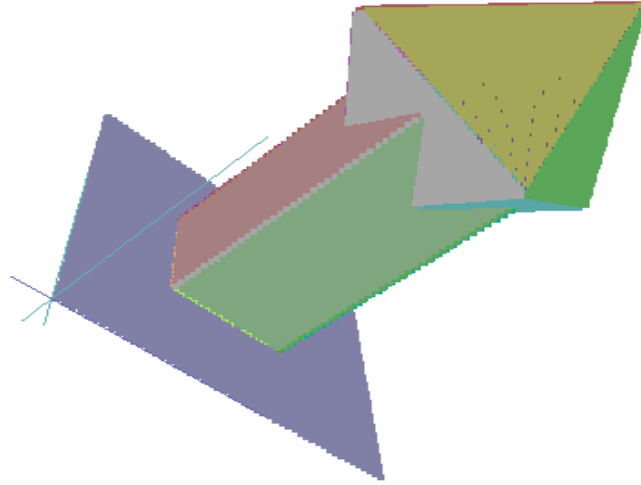


Fig. 1: Computer simulation of the proposed unique microstructure not possible with conventional microfabrication

The notion of biocompatibility has evolved in conjunction with the continuing development of materials used in medical devices and the operative principle was that of inertness—as reflected, for example, in the definition of *biocompatibility* as "the quality of not having toxic or injurious effects on biological systems." [3].

1.2 Applications

Materials that are able to function in intimate contact with living tissue with minimal adverse or rejection by the body are called biomaterials (*ex: 316L stainless steel, Titanium, Alumina, Hydroxyapatite*). Devices engineered from biomaterials and designed to perform specific functions in the body are generally referred to as biomaterials devices or implants [4]. The biocompatibility of a medical implant will be influenced by a number of factors, like the toxicity of the materials, the form and design of the implant,

the surgeon skills in inserting the device, the dynamics or movement of the device *in situ*, biostability, and the nature of the reactions that occur at the biological interface [5].

Among the prominent applications for biomaterials are:

- Orthopedics - joint replacements (hip, knee – Figs. 2 and 3), bone cements, bone defect fillers, fracture fixation plates, and artificial tendons and ligaments [6].



Fig. 2: Hip Joint consisting of a ball (made of metal or ceramic) and socket (made of UHMWPE that's ultra high molecular weight polyethylene) [7]



Fig. 3: Knee replacement consisting of a metallic femoral component (left) and UHMWPE tibial component (right) [7]

- Cardiovascular—vascular grafts (Fig. 4), heart valves, pacemakers, artificial heart (Fig. 5) and ventricular assist device components, stents, balloons, and blood substitutes [8].



Fig. 4: Vascular Grafts [9]



Fig. 5: Artificial heart [10]

- Ophthalmics—contact lenses (Fig. 6), intraocular lenses (Fig. 7), corneal implants and artificial corneas [11].

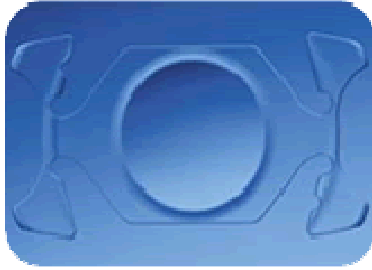


Fig. 6: Lens made from hydrophilic acrylic material [12]



Fig. 7: ARRAY® multifocal intraocular lens [13]

- Other applications—dental implants, cochlear implants, tissue screws and tacks, burn and wound dressings, artificial skin (Fig. 8), tissue adhesives and sealants, drug-delivery systems, surgical tape (Fig. 9) matrices for cell encapsulation and tissue engineering, and sutures [14].



Fig. 8: Artificial skin composed of a layer of silicone rubber and a layer of modified collagen [15]



Fig. 9: Surgical tape [16]

1.3 Role of polymers in medicine

Typically inorganic (metals, ceramics, and glasses) and polymeric (synthetic and natural) materials have been used for such items as artificial heart-valves (polymeric or

carbon-based), synthetic blood-vessels, artificial hips (metallic or ceramic), medical adhesives, sutures, dental composites, and polymers for controlled slow drug delivery [17]. The development of new biocompatible materials includes considerations that go beyond nontoxicity to bioactivity as it relates to interacting with and, in time, being integrated into the biological environment as well as other tailored properties depending on the specific *in vivo* application [18]

Polymers have a long history in medicine and they play an important role in biomedical applications (*ex: poly(vinyl alcohol), poly(methacrylic acid), poly(lactic acid) (PLLA), UHMW polyethylene, Polyurethane*). These polymers include polymeric hydrogels (Fig.11), biodegradable polymers (Fig.10), tissue friendly functional polymers, and biocompatible but nonbiodegradable polymers [19]. Their usage extends from traditional applications such as catheters, syringes, blood contacting extra corporeal devices, to matrices for drug delivery, cell encapsulation and modification, tissue regeneration, artificial organ making, and other such intelligent functions [20].

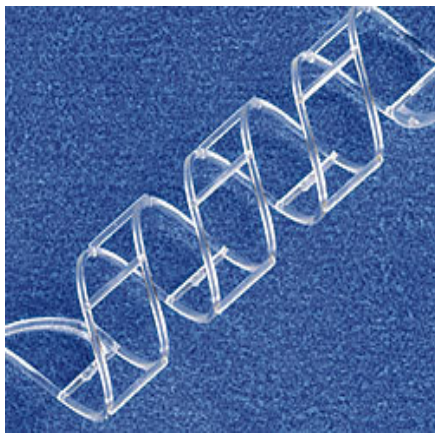


Fig.10: A biodegradable intravascular stent prototype is molded from a blend of polylactide and trimethylene carbonate [21]

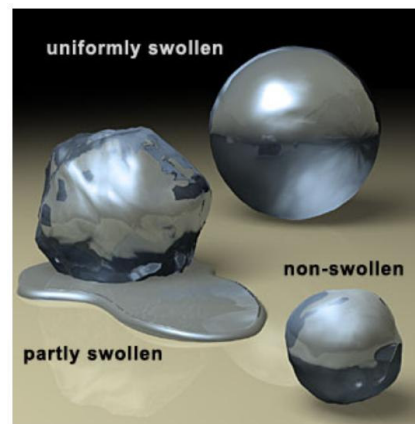


Fig. 11: Swollen polymer gel [22]

PARYLENE (name for a unique product family: poly-para-xylylene), is mostly used as a conformal protective polymer pin-hole free coating material to uniformly protect any component configuration on diverse substrates such as metal, glass, paper, resin, plastic, ceramic, ferrite and silicon (see Fig. 12). Its medical applications include, providing a non-reactive, inert, pinhole-free barrier for biomedical instrumentation and permitting a compatible functional utilization with body implant devices. Due to its biocompatible nature, barrier properties and compatibility with microfabrication techniques it is now being investigated for further applications in the biomedical field. Because of its unique properties, parylene conforms to different shapes, including sharp edges, crevices, points, or flat and exposed internal surfaces. This characteristic enables parylene to be conveniently combined with MEMS technology, to meet biocompatibility requirements of biological and chemical applications.

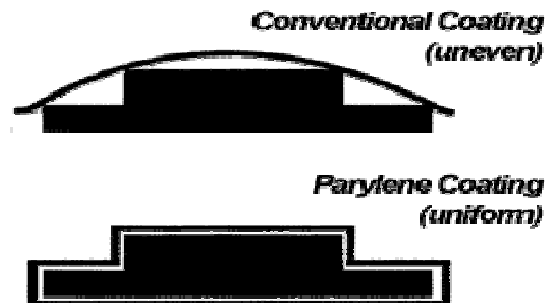


Fig. 12: Comparison of conventional and parylene coating [23]

PARYLENE is inert to acids and bases, as well as organic solvents. Parylene dimer (raw material) is produced in three variations (Fig. 13), each suited to the requirements of a category of applications [23].

Parylene C: The most widely used dimer, providing a useful combination of properties, plus a very low permeability to moisture, chemicals, and other corrosive gases.

Parylene N: The chemical name of parylene N is [2,2]-paracyclophane and the formula is $C_{16}H_{16}$ [24]. It provides high dielectric strength and a low dielectric constant which is independent of frequency, and a low dissipation factor, making it ideal for high frequency applications [25]. Best selection is where greater coating protection is required. It has the greatest penetrating power with respect to deep recesses and ‘blind’ holes.

Parylene D: Maintains its physical strength and electrical properties at higher temperatures.

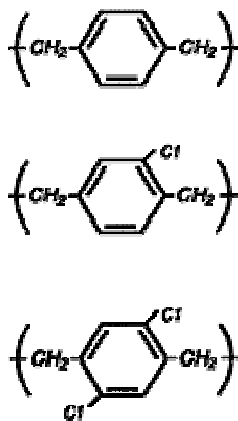


Fig. 13: Parylene N, C, D [23]

Xylenes are a family of isomeric, colorless aromatic hydrocarbon liquids, that contain the general formula $C_6H_4(CH_3)_2$. They are produced by the destructive distillation of coal or by the catalytic reforming of petroleum naphthenic fractions [26]. The term xylene refers to a group of three benzene derivatives which encompasses *ortho*-, *meta*-, and *para*- isomers of dimethyl benzene. The *o*-, *m*- and *p*- isomers (Fig. 14) specify to which carbon atoms (of the main benzene ring) the two methyl groups are attached. Counting the carbon atoms from one of the ring carbons bonded to a methyl group, and counting towards the second ring carbon bonded to a methyl group, the *o*- isomer has the IUPAC (International Union of Pure and Applied Chemistry) name of 1,2-

dimethylbenzene. The *m*- isomer has the IUPAC name of 1,3-dimethylbenzene. And *p*- isomer has the IUPAC name of 1,4-dimethylbenzene [27].

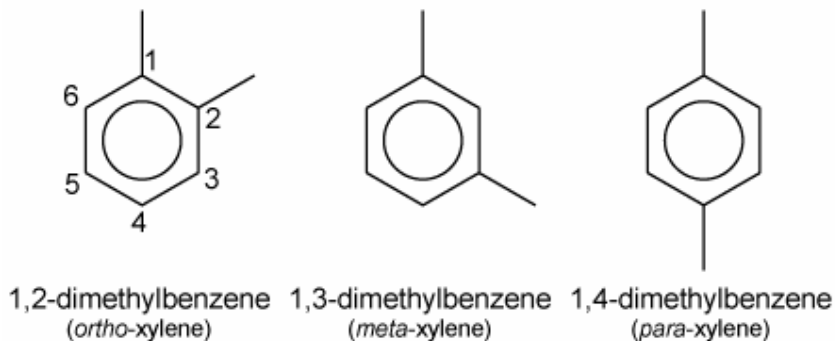


Fig. 14 *ortho*-, *meta*-, and *para*- isomers [27]

[2,2]Paracyclophane is the parent compound in the family of cyclophanes. This molecule consists of two benzene rings on top of each other in parallel planes and connected by ethano bridges at the *para* positions [28]. In Parylene C (Polychloro-*p*-xylylene), a chlorine atom is substituted for one of the hydrogen atoms on the benzene ring of each *para*-xylylene moiety [29]. Parylene D, the third version, has two chlorine atoms in the ring and possesses superior physical and electrical properties at higher temperatures than the N and C grades. It also has the highest degree of thermal stability of the three variants [30].

Historically, proposed mechanisms of plasma polymerization have been based on conventional chain growth polymerization, such as free radical or ionic polymerization. In conventional chain growth polymerization, an initiating species reacts with monomer, and this process continues with the subsequent addition of monomer, proceeding until the reaction is terminated by processes such as disproportionation, combination, or transfer of reactive agents to some species separate from the polymer chain [31].

Chain growth polymerization is a molecular process that can proceed at low (atmospheric) pressure with catalysts, or spontaneously at high pressures without catalysts, or in the liquid phase under a variety of conditions. The resultant polymer has a regular, repeating structure based on the monomer. As will be shown later, vacuum deposition polymerization is an "atomic" process which yields a highly crosslinked product with a random structure, and vacuum conditions make gas phase chain growth a highly improbable growth mechanism due to thermodynamic constraints [31].

Vacuum deposition processes, such as Parylene polymerization, UWD and plasma polymerization, occurs due to the dissociation of covalent bonds in gas phase molecules, and subsequent reactions between gas phase species and surfaces result in the deposition of polymeric materials. Dissociation results from interactions between monomer and energetic species, such as ions, electrons, photons, and excited neutrals. In parylene polymerization, bond dissociation is due to thermolysis of monomer. The term monomer is not used in the same sense as in conventional polymerization. In vacuum deposition, the term monomer refers to any compound which can be used to deposit a film of polymeric material. Such compounds include but are not limited to those used in conventional polymerization. For example, plasma polymers can be obtained from methane, benzene, and saturated fluorocarbons [31].

The deposition (Fig.14) takes place in three steps: vaporization, pyrolysis and polymerization. The Dimer changes from a solid to a vapor and the molecules move down the tube by virtue of the reduced pressure at the opposite end. The Dimer moves into the pyrolysis zone which is at 680 degrees C and the high temperature cleaves the Dimer into two divalent radical monomers. The monomer molecules enter the deposition

chamber and re-form as a long chain polymer on all surfaces within the chamber [32]. In the deposition stage, parylene polymerizes spontaneously onto the surface of objects being coated, with no cure-related hydraulic or liquid surface-tension forces, either initially or subsequently. The coating grows as a conformal film (polypara-xylylene) on all exposed substrate surfaces, edges, and in crevices, at a predictable rate. There is no liquid phase, and substrate temperature remains near ambient [33].

Parylene's chemical structure—particularly its high molecular weight, crystallinity, and all-carbon backbone is of significance to medical applications. The absence of polar entities in the essential makeup of all three of the parylenes makes them hydrophobic, stable, and resistant to chemical attack [33].

Studies show each molecule makes an average of 10,000 collisions and because of the short mean free path of the molecule vapor (less than 1 M.M.), the coating forms slowly and uniformly over surfaces with both sharp edges and deep crevices with no pin holes [32].

The source substances are chemically widely stable Dimer molecules (di para Xylylene, see Fig. 15). If the steam is escorted by a high temperature zone, a chemically highly reactive monomer (Fig. 16) forms from the Dimer. On a cold surface the substance immediately polymerizes (Fig. 17) forming a polymer coating [34].

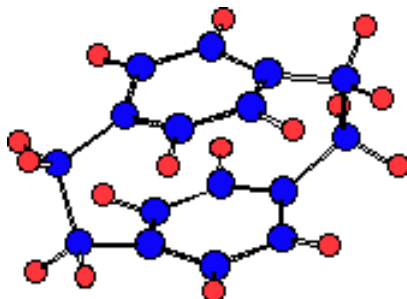


Fig. 15 Dimer [34]

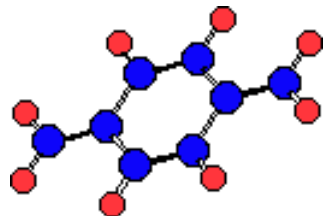


Fig. 16 Monomer [34]

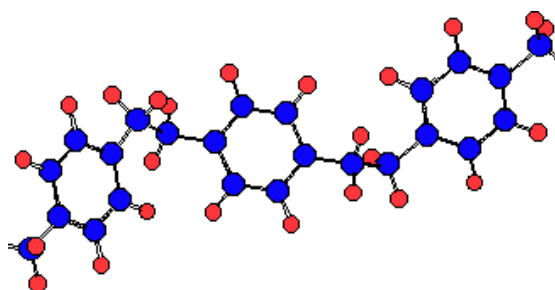


Fig. 17 Polymer [34]

The deposition process is depicted in Fig 18.

1. Sublimation under vacuum at approx. 140°C of the stable crystalline dimer di-p-xylylene to produce vapors of this material.
2. Pyrolysis of the vapors at approx. 650°C to form gaseous reactive monomer para-xylylene.
3. Depositions and simultaneous polymerization to form poly-p-xylylene or Parylene.

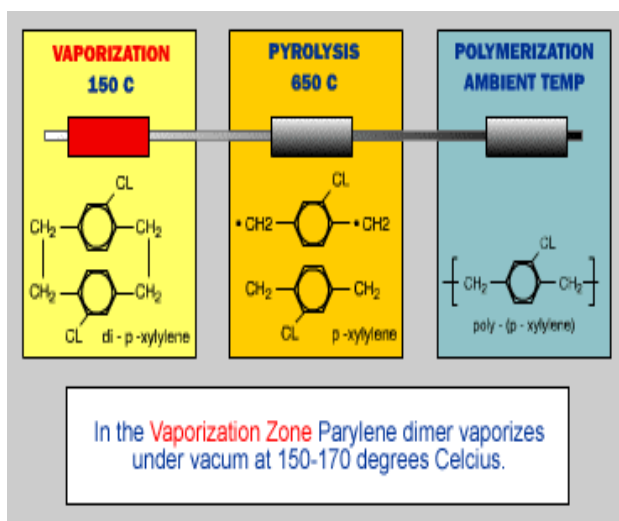


Fig. 18: Parylene deposition process [46]

CHAPTER 2

DESIGN AND FABRICATION

An attempt is made towards combining microfabrication techniques with parylene properties, to fabricate microstructures that can find wide applications in the biomedical field, like the polymers mentioned in Chapter 1. High aspect ratio trenches are etched in silicon followed by parylene deposition in these trenches. This technique allows for the production of unique microstructures, many of which are not realizable by any other fabrication technique. The first step in the process is the design of the photomask.

2.1 Photomask

A photomask is a transparent plate with a design of opaque patterns, which is used to withhold light during its use. It is a square glass plate with a patterned emulsion of metal film on one side. It masks out selected areas of light during the patterning of other substrates. Photomasks can be made on glass or film substrates. The opaque patterns can be made of silver, chrome, chrome oxide, iron oxide, copper, aluminum, silicon oxide and other materials.

2.1.1 ACES

Anisotropic Crystalline Etch Simulation (ACES) is the first PC-based 3-D etch simulator. It is developed by the Micro Actuators, Sensors and Systems Group (MASS) <http://galaxy.micro.uiuc.edu> MEMS designers, and fabricators can submit a geometric description of an input mask and process information (etch rates, etch times etc.).

This mask will be processed by the simulation software to yield an etched output shape (Fig. 19).

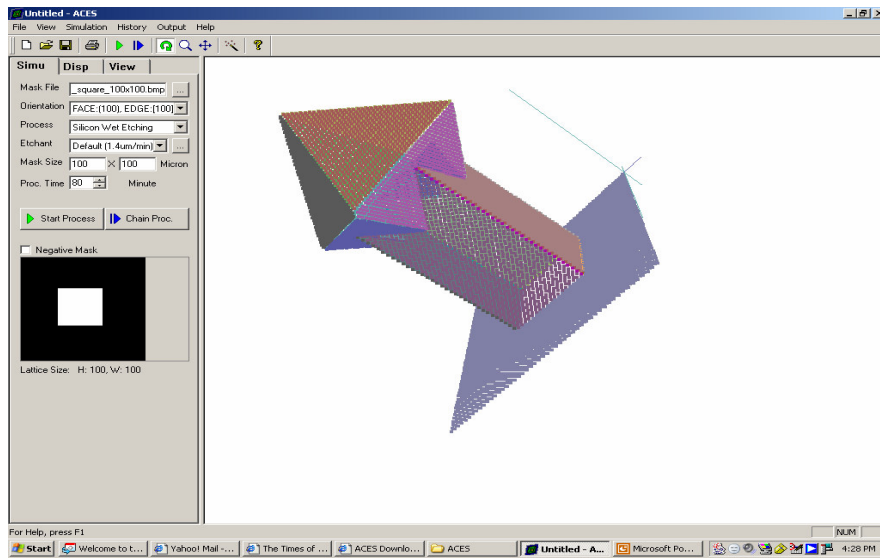
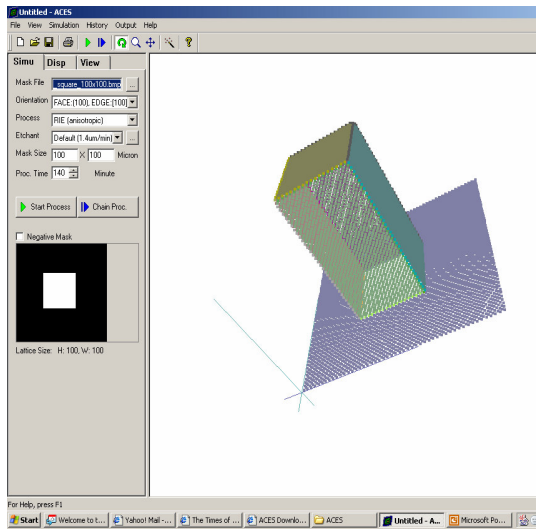


Fig. 19: ACES simulation

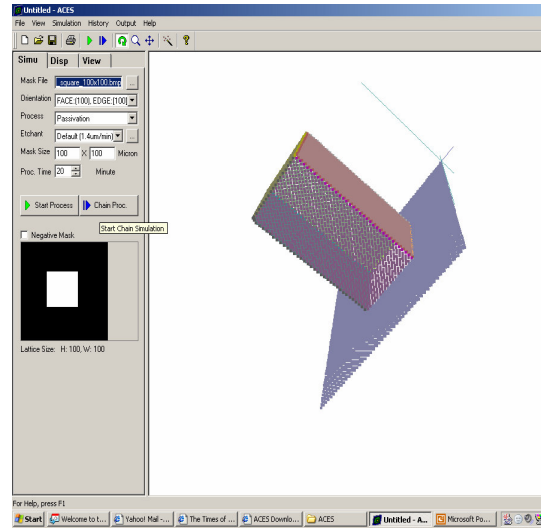
Simulation results can be obtained by selecting a mask from the mask file of the ACES directory and performing etching and passivation processes for wafers of given orientations. The tool enables the user to design the mask features and establish a fabrication process. The CAD simulation result for a square mask is as shown in Fig. 20. The first step is performing a reactive ion etch (RIE) on a Si <100> wafer for a process time of 140 minutes (Fig. 20a), followed by passivation of the side walls using the same mask (Fig. 20b). The wafer is again subjected to RIE for 20 minutes, this time to reopen only the bottom surface of the etched structures (Fig. 20c). The final step is to run Si anisotropic etching for 80 minutes (Fig. 20d). However, during the actual fabrication process, a new wafer is bonded to the first wafer and wet etching (RIE) is actually done on the second wafer. This process will be discussed in detail in the subsequent chapters. This CAD tool is mainly used to experiment with various masks and wafer orientations and select the appropriate masking features. But the fabrication steps are determined by

taking into consideration other factors as well. For example in this case if the exact sequence is replicated in the lab, that is, when the passivation of sidewalls is followed by performing an RIE, there would be no effect on the wafer because the passivation blocks the etchant and it is not practically possible to remove this material just at the bottom of the wafer. That is why holes are etched in the first wafer and after passivating this wafer, it is bonded to a new wafer. The second wafer, which now acts as a base for the first wafer, is exposed to the etchant. So there are variations in the steps but this tool definitely helps in determining the mask features and the processes, which ultimately lead to the desired results.

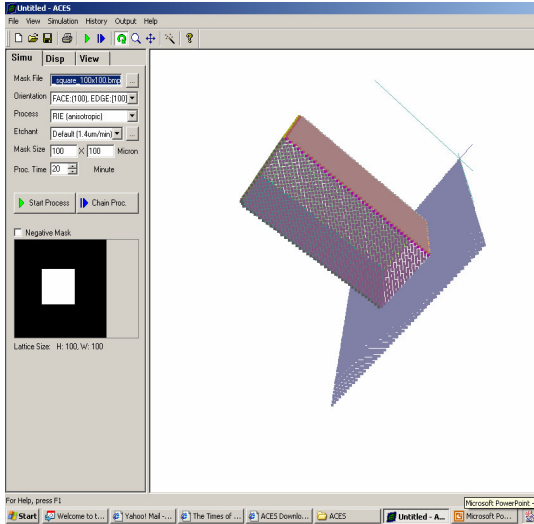
Different mask features (see Fig. 21) that give similar results can be tested using the ACES tool and the final layout of the mask can be designed in the layout editor (L-EDIT).



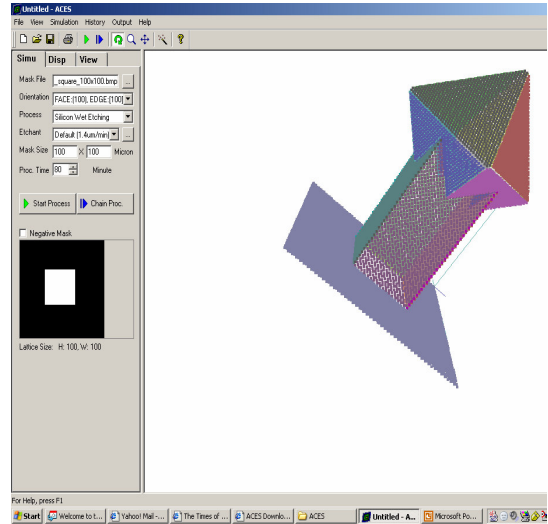
(a) RIE



(b) Passivation



(c) RIE



(d) Si wet etching

Fig. 20: CAD simulation result for a square mask

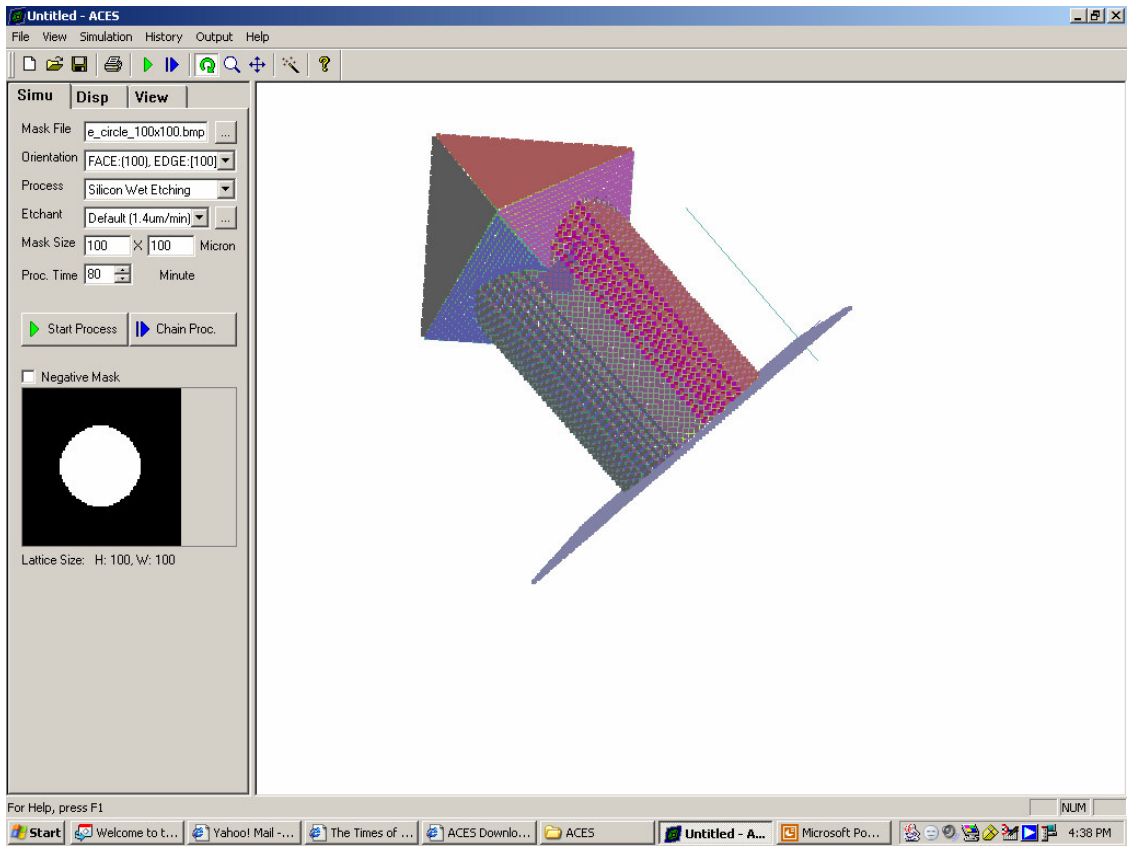


Fig. 21: Simulation results for a mask with a circular hole

2.1.2 L-Edit

LAYOUT EDITOR [47] provides complete and easy control over all the layout operations. The easy-to-use interface allows one to design immediately, without a steep learning curve or extended setup phase. Complex Boolean and derived layer operations can be performed with arbitrary polygonal curves and shapes. Coordinate and distance values can be displayed in any technology unit, and design dimensions can be scaled swiftly and accurately using the rescale Wizard [47]. Since a negative photoresist will be used in this process, a light field mask (Fig. 22) is designed (clear background with opaque images).

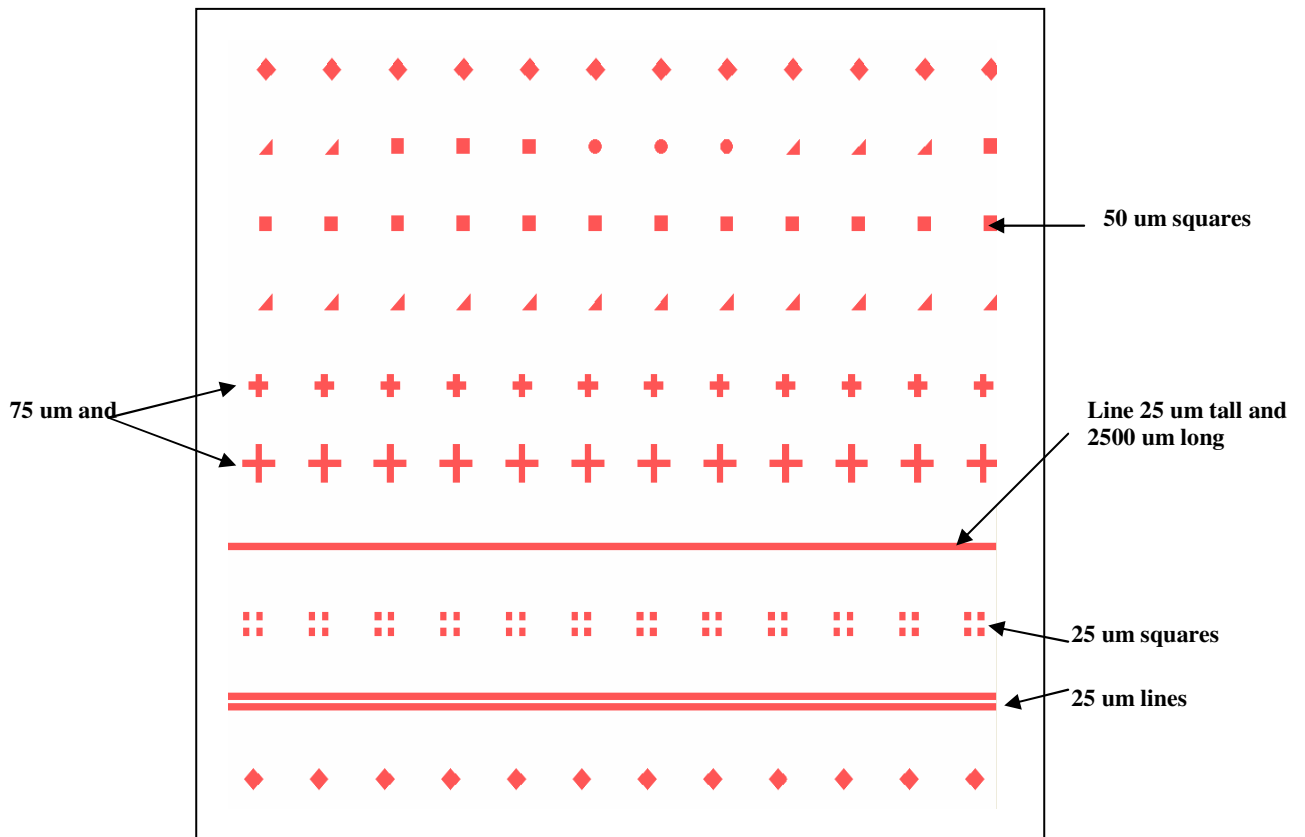
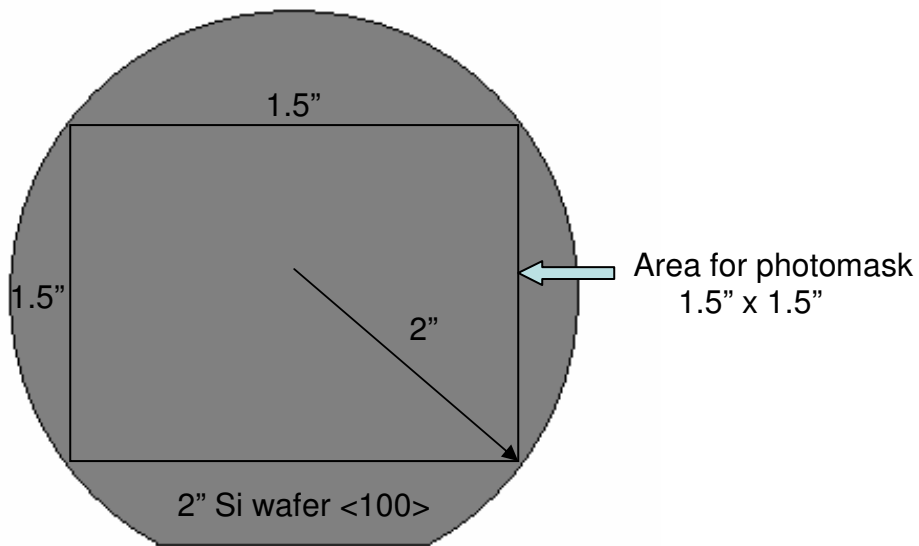


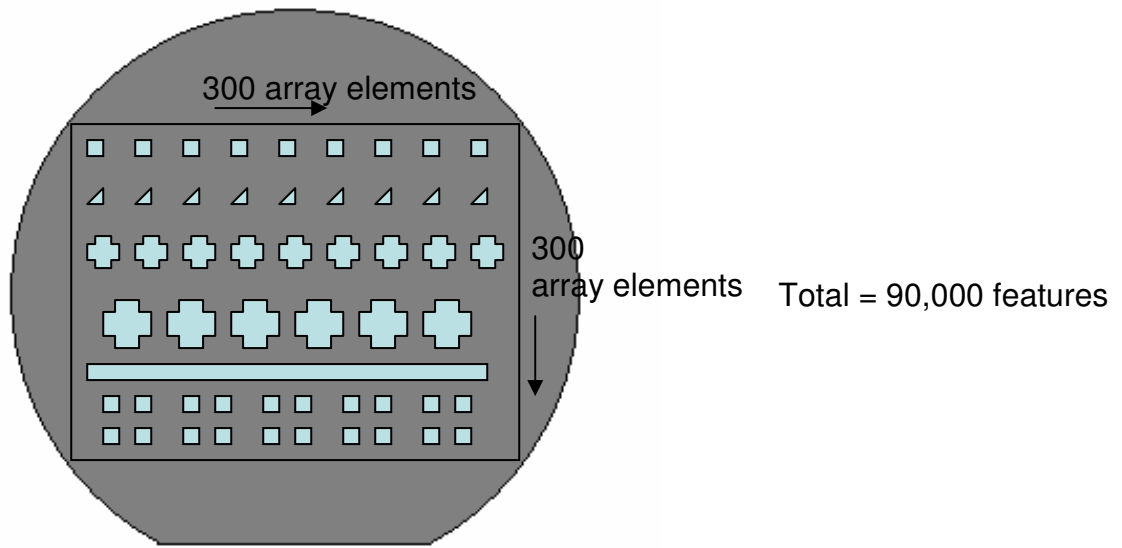
Fig. 22: Light field Photomask

An array is defined as the area on the photomask that has repeating patterns. The number of arrays repeated is calculated from the size of the wafer and the features on the mask. For maximum yield, the array pattern should cover maximum area on the substrate on which the mask is printed.

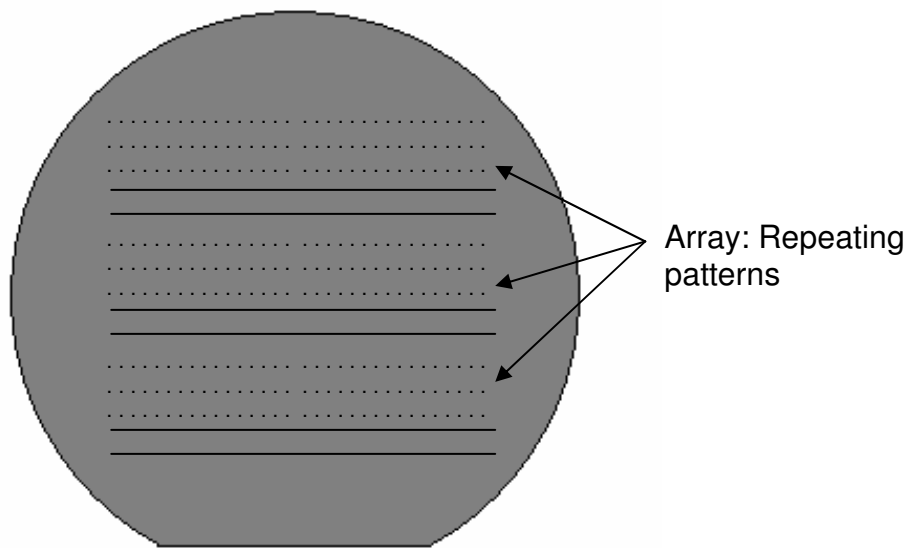
As shown in Fig.23, multiple arrays are required on a photomask to cover a 2" wafer. The spacing between each feature is 200 μm . The pattern is designed to fit in a 1.5" x 1.5" area on the substrate.



(a)



(b)



(c)

Fig. 23: (a) Area for the mask (b) Number of features (c) Final mask: Making of the light field photomask

CAD system is used to describe the circuit patterns electrically. Digital data produced by CAD system drives a pattern generator that transfers the patterns directly to electron-sensitized mask. Mask consists of a fused silica substrate covered with chromium. Circuit pattern is first transferred to the electron-sensitized layer (electron resist), which is transferred into the underlying chromium layer for the finished mask.

2.2 Fabrication Steps

After the photomask is designed and printed, a complete fabrication process is developed (Fig. 24). The starting wafer is an n-type Si <100> wafer of diameter 2 inch (3 inch wafers can also be used). The following is the sequence of steps:

1. RCA (Radio Corporation of America) wafer clean
2. Thermal oxidation
3. Photolithography
4. Plasma etching (DRIE – Deep Reactive Ion Etching)
5. Oxide removal
6. RCA clean and oxidation (passivation)
7. Silicon fusion bonding
8. Anisotropic wet etching (TMAH – Tetra Methyl Ammonium Hydroxide)
9. Contamination removal and BOE (Buffered Oxide Etch)
10. Parylene deposition
11. Substrate etch
12. Releasing of parylene

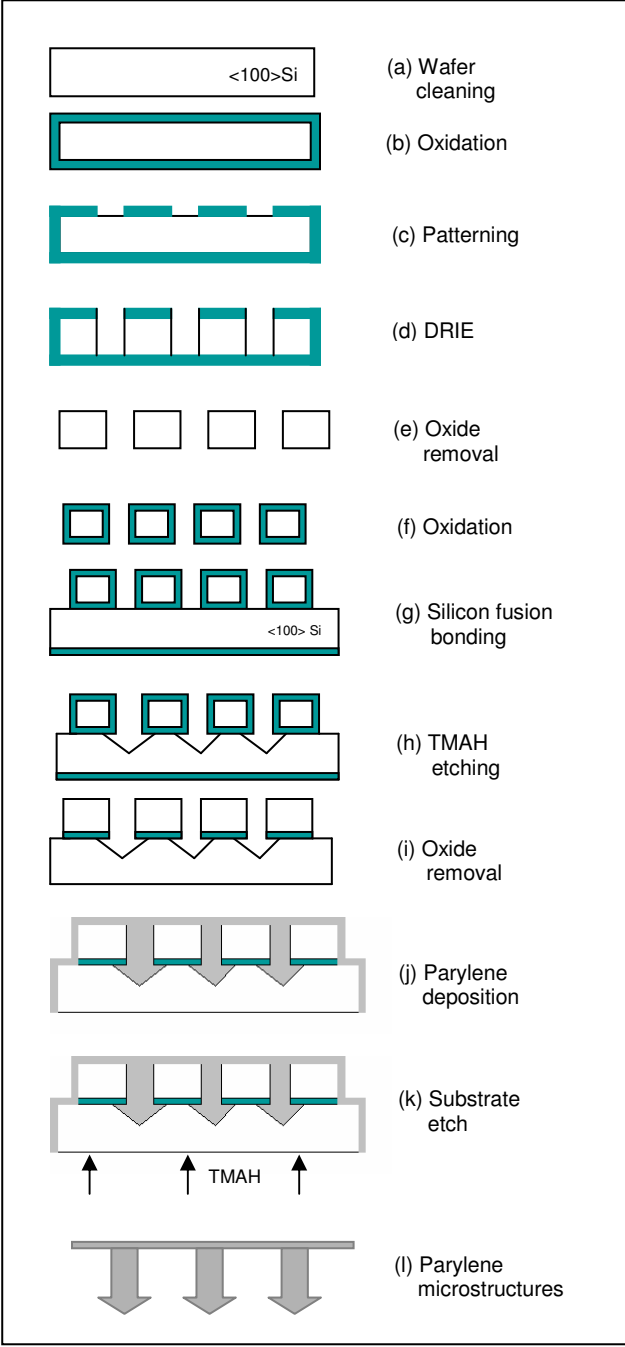


Fig. 24: Fabrication sequence

2.2.1 Initial wafer clean

The purpose of the RCA clean is to remove organic contaminants (such as dust particles, grease or silica gel) from the wafer surface; then remove any oxide layer that may have built up; and finally remove any ionic or heavy metal contaminants [48]. The RCA clean procedure should be performed immediately prior to any crucial step, especially those involving high temperatures. The starting wafer for the process is a 3 inch, <100> Si n-type wafer (Fig. 24 a). Initial wafer clean involves two steps: base clean and acid clean.

Base clean is performed to remove residual organic contamination left over from the solvent cleaning or any other previous processing. Acid clean removes ionic and metallic contamination. The proportion of chemicals recommended for each cleaning process depends on the wafer size. A table of proportions for initial wafer clean is provided below:

		2" Wafer Processing					3" Wafer Processing	4" Wafer Processing
Base Clean	NH ₄ OH (1 part)	50mL	60mL	65mL	70mL	75mL	100 mL	200 mL
	DI (5 parts)	250	300	325	350	375	500	1000
	H ₂ O ₂ (1 part)	50	60	65	70	75	100	200
	TOTAL (mL)	350	420	455	490	525	700	1400
Acid Clean	HCl (1 part)	50	60	65	70	75	125	230
	DI (4 parts)	200	240	260	280	300	500	920
	H ₂ O ₂ (1 part)	50	60	65	70	75	125	230
	TOTAL (mL)	300	360	390	420	450	750	1380

Table 1: Table of proportions for initial wafer clean [49]

2.2.2 Oxidation

Under exposure to oxygen, a silicon surface oxidizes to form silicon dioxide (SiO_2). Native silicon dioxide is a high-quality electrical insulator and can be used as a barrier material during impurity implants or diffusion and for electrical isolation of semiconductor devices (Fig. 24b). The ability to form a native oxide was one of the primary processing considerations, which led to silicon becoming the dominant semiconductor material used in integrated circuits today.

Thermal oxidation of silicon is easily achieved by heating the substrate to temperatures typically in the range of 900-1200 degrees C (Pressure: 0.2 - 1.0 atm, SiO_2 thickness: 0.03 - 2 mm). The atmosphere in the furnace where oxidation takes place can either contain pure oxygen or water vapor. Both of these molecules diffuse easily through the growing SiO_2 layer at these high temperatures. Oxygen arriving at the silicon surface can then combine with silicon to form silicon dioxide. The chemical reactions that take place are either



for so-called "dry oxidation" or



for "wet oxidation". Due to the stoichiometric relationships in these reactions and the difference between the densities of Si and SiO_2 , about 46% of the silicon surface is "consumed" during oxidation [50]. That is, for every 1 um of SiO_2 grown, about 0.46 um of silicon is consumed (as shown in the Fig. 25).

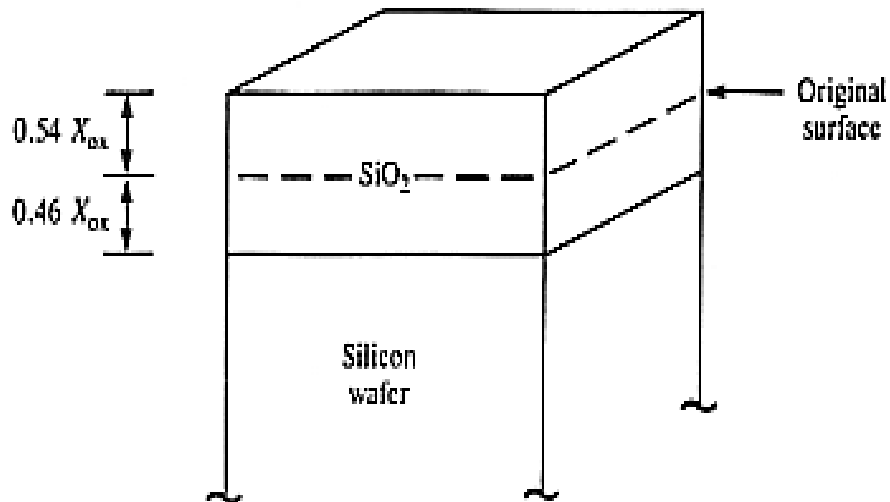


Fig. 25: SiO₂ growth [51]

The Lindberg furnaces (Fig. 26) are used for very high temperature laboratory processes such as oxidation and doping. Three-zone furnaces have three independent heating zones controlled by independent thermocouples, which produce a uniform temperature curve throughout all three zones. The controllers use data from the center zone thermocouple to control the endzone thermocouples.

A comparison of oxide thickness versus oxidation time at different temperatures for wet and dry oxidation is shown Fig. 27. Wet oxidation is done on the RCA cleaned silicon wafer at 1000⁰ C. A layer of 0.45μm thick silicon dioxide is sufficient to proceed with the patterning. The thickness of oxide can also be determined by observing the color. In this case the color was violet red.



Fig. 26: Lindberg furnaces

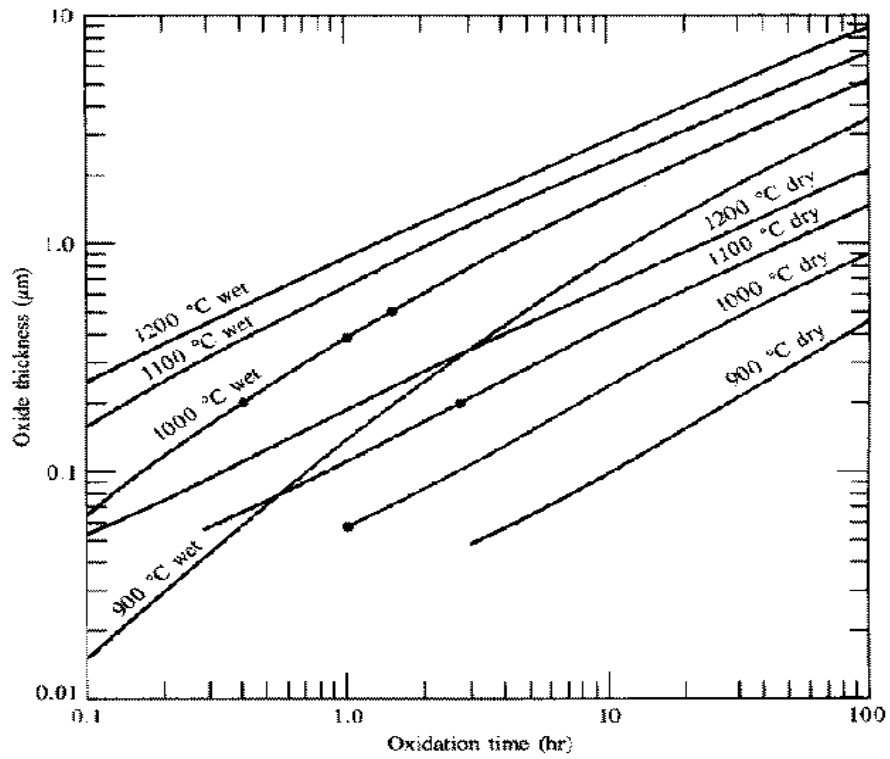


Fig. 27 Oxide thickness vs. oxidation time [51]

2.2.3 Photolithography

Photolithography is the process of transferring geometric shapes from a mask to the substrate. Photolithography involves the following steps: wafer cleaning, barrier layer formation, photoresist application, soft baking, mask alignment, exposure and development, and hard-baking.

After the formation of the SiO₂ layer, the wafer surface is thoroughly cleaned for the application of photoresist. High-speed centrifugal whirling of silicon wafers is the standard method for applying photoresist coatings in IC (Integrated Circuits) manufacturing. This technique, known as "Spin Coating," produces a thin uniform layer of photoresist on the wafer surface [52].

An appropriate photoresist and developer is needed for the photolithography process. There are two types of photoresists: positive and negative. By exposing resist to UV rays in specific areas, the material underneath the resist can be removed. In case of positive resists, exposure to the UV light changes the chemical structure of the resist so that it becomes more soluble in the developer. The exposed resist is then washed away by the developer solution, leaving windows of the bare underlying material. In other words, "whatever shows, goes." The mask, therefore, contains an exact copy of the pattern, which has to remain on the wafer [53]. See Fig. 24(c)

Negative resists behave in just the opposite manner. Exposure to the UV light causes the negative resist to become polymerized, and more difficult to dissolve. Therefore, the negative resist remains on the surface wherever it is exposed, and the developer solution removes only the unexposed portions. Masks used for negative photoresists, therefore, contain the inverse (or photographic "negative") of the pattern to

be transferred. The figure below shows the pattern differences generated from the use of positive and negative resist (Fig. 28).

OCG HNR 80 Resist and OCG HNR 120 Resist (OCG Microelectronic Materials, Inc.) are negative photoresists that are designed to provide improved resolution and process latitude in both contact and non-contact exposure systems. They are formulated to virtually eliminate post-development scumming related to ambient conditions and minimize poor development phenomena associated with process delays. These resists also have lower mask to wafer sticking tendencies during contact exposures and reduce defects caused by this effect. One of the main criteria for selecting a photoresist was to test the strong adhesion property of the resist to the substrate during the plasma etch. Since holes had to be etched through the substrate, it was essential to use a strong resist that could survive the plasma etch. Various resists (positive and negative) were put to task and based on the end result, the OCG thick resist was selected for lithography. A light field photomask had to be used for the transfer of pattern.

The developer used for OCG thick resist is the Waycoat negative resist developer (WNRD). The developed film has to be rinsed with Iso propanol. According to the specifications of OCG resist, water should not be used anytime during the development.

By soft-baking the substrate, almost all the solvents are removed from the photoresist coating. Soft-baking plays a very critical role in photo-imaging. The photoresist coatings become photosensitive, or imageable, only after softbaking. Over soft-baking will degrade the photosensitivity of resists by either reducing the developer solubility or actually destroying a portion of the sensitizer. Undersoft-baking will prevent light from reaching the sensitizer. Positive resists are incompletely exposed if

considerable solvent remains in the coating. This undersoft-baked positive resist is then readily attacked by the developer in both exposed and unexposed areas, causing less etching resistance.

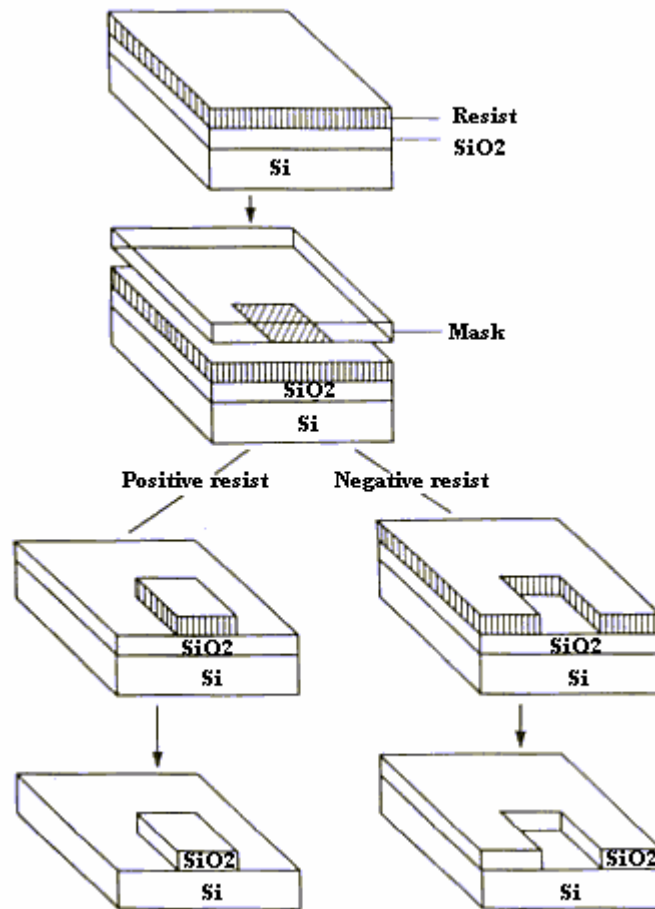


Fig. 28: The pattern differences generated from the use of positive and negative resist [54]

One of the most important steps in the photolithography process is mask alignment. The mask has to be aligned with the wafer, so that the pattern can be transferred onto the wafer surface accurately. Each mask after the first one must be aligned to the previous pattern.

Once the mask has been accurately aligned with the pattern on the wafer's surface, the photoresist is exposed through the pattern on the mask with a high intensity ultraviolet light [55]. There are three primary exposure methods: contact, proximity, and projection. Contact printing is used in this case.

The exposed film is now ready for development. At low-exposure energies, the negative resist remains completely soluble in the developer solution. As the exposure is increased above threshold energy, more of the resist film remains after development. At exposures two or three times the threshold energy, very little of the resist film is dissolved.

Hard-baking, which is the final step in the photolithography process, is necessary to harden the photoresist and improve adhesion of the photoresist to the wafer surface.

The parameters used for photolithography for this fabrication process are as follows:

RAMP = 100

SPREAD SPEED = 500 RPM for 5 seconds

SPIN SPEED = 5000 RPM for 30 seconds

SOFT BAKE = 5 minutes

HARD BAKE = 10 minutes

EXPOSURE TIME = 3.2 seconds

DEVELOPING TIME = 4 minutes

AB-M Intensity-Controlling Power Supply systems (Fig. 29) are designed to produce significantly improved printing performance due to their ability to operate and precisely control the exposing source over a wide range of intensities. The capability allows the process engineer to develop an exposure matrix, and then select the optimum

time/intensity relationship needed to produce the desired printing quality. The user inputs the desired intensity/time function and the controller then delivers the selected parameters to an accuracy of better than $\pm 2\%$. This accuracy is maintained throughout the life of the lamp.

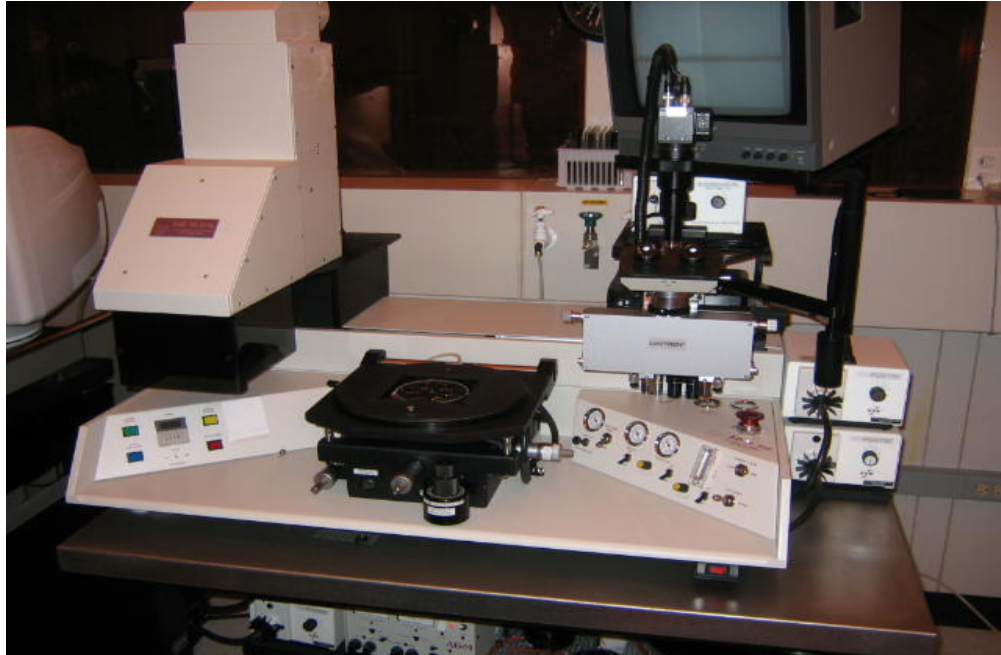


Fig. 29: ABM IR Mask Aligner

2.2.4 Deep Reactive Ion Etching:

Fig. 30 shows the classification of different etching processes. Anisotropic and isotropic etching fall under the category of wet etching, whereas plasma etching is categorized as a dry etch process. Both wet and dry etchants are used in this thesis.

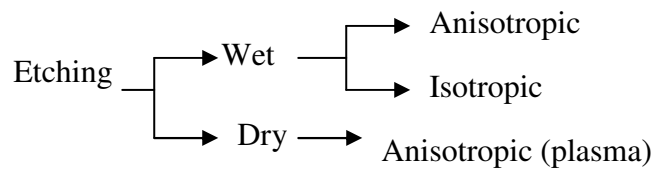


Fig. 30 Classification of Etching process

Fig. 31 shows the etch profiles from anisotropic and isotropic etching. Plasma is an ionized gas composed of equal numbers of positive and negative charges and a different number of unionized molecules and is produced when electric field is applied to a gas. This causes the gas to break down and become ionized. It is initiated by free electrons that gain kinetic energy from electric field, collide with gas molecules, and loose energy. Energy transferred causes the gas molecules to be ionized (i.e., to free electrons). Free electrons gain kinetic energy from the field, and the process continues. Plasma etching is a chemical reaction combined with physical ion bombardment.

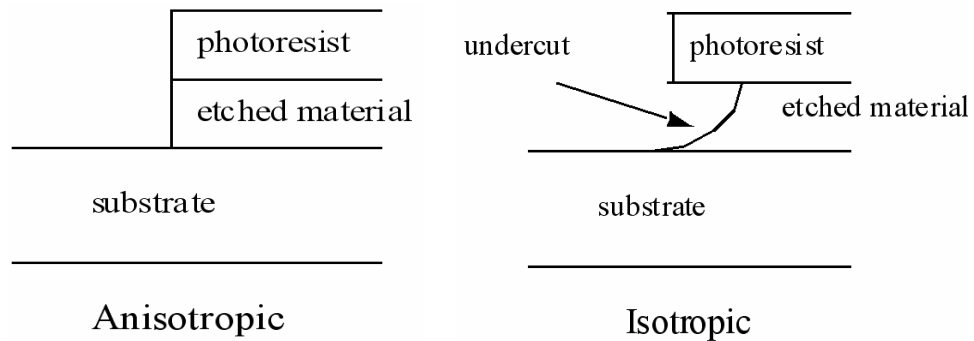


Fig. 31: Etch profiles from anisotropic and isotropic etching

The STS Multiplex ICP (inductively coupled plasma) system, which is a DRIE system (Fig. 32), is used in this experiment to etch holes in the substrate. It allows for the copying of a specific pattern onto silicon wafers. This is achieved through etching using specific gases. This machine is also capable of holding multiple wafers at a single time so the same procedure need be repeated for each sample.

DRIE is a high aspect ratio, deep trench silicon etching process. The principle of the deep trench silicon etching process is an alternating fluorine based etching and passivation of the structures. SF_6 (Sulphur Hexaflouride) etches the silicon substrate in

the etch cycle and the sidewall is coated by C_4F_8 (Octafluorocyclobutane) in the passivation cycle to prevent undercutting [45]

This results in sidewall profiles of $90^\circ \pm 1^\circ$ with aspect ratios of up to 40:1 (an example is shown in Fig. 33). Masking layers can be made of photo resist or silicon oxide. The features of DRIE are:

- etch rate of up to 6 $\mu\text{m}/\text{min}$
- aspect ratio up to 40:1
- selectivity to positive resist > 75:1
- selectivity to silicon oxide >150:1
- etch depth capability 10 to 550 μm (through wafer etching)
- sidewall profile $90^\circ \pm 1^\circ$
- feature size 1 to >500 μm

Fig. 34 shows the schematic of STS ICP etching system. The system consists of ICP electronics, loadlock and wafer loader unit and a process chamber. The plasma is inductively coupled at 13.56 MHz via the matching unit and coil assembly into an alumina chamber.



Fig. 32: STS Multiplex ICP

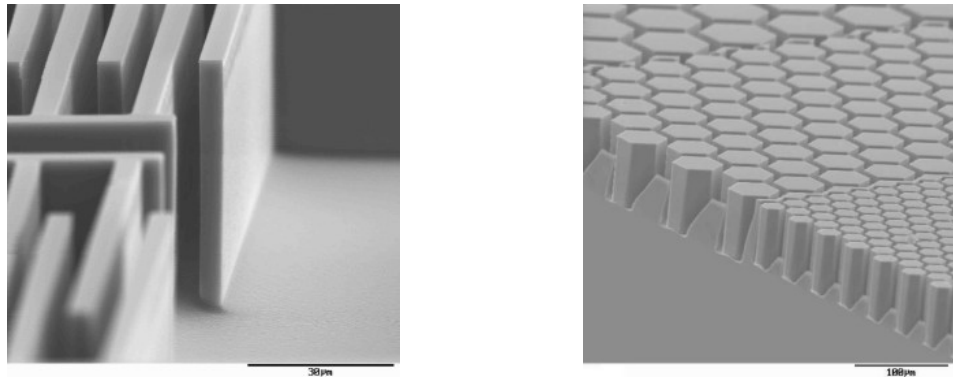


Fig. 33: Comb drive manufactured with DRIE [46]

Independent energy control is provided by 13.56 MHz RF biasing of the electrode via automatic power control and impedance matching. Process gas is introduced to the chamber through the upper over assembly. The wafers are placed on the electrode assembly which is powered at 13.56 MHz. Temperature control of the wafer platen is required for certain processes and is achieved using a recirculating deionized water system. The Al load-lock has a transparent hinged lid that allows easy access for loading/unloading of wafer carrier. After loading of the wafer into the loadlock, the

system automatically carries out pump down, leak check and transfer of the wafer into the process chamber via the carriage assembly after which the process is started. In this ICP system, the coil power and platen power voltage were controlled by independent RF power generators and the processing gases were switchable. By switching the gases periodically, the system can process the silicon wafer by etching and passivation, respectively. This means that the high aspect ratio silicon etching is completed by the accumulation of many shallow trench etchings by SF_6 and polymer depositions by C_4F_8 .

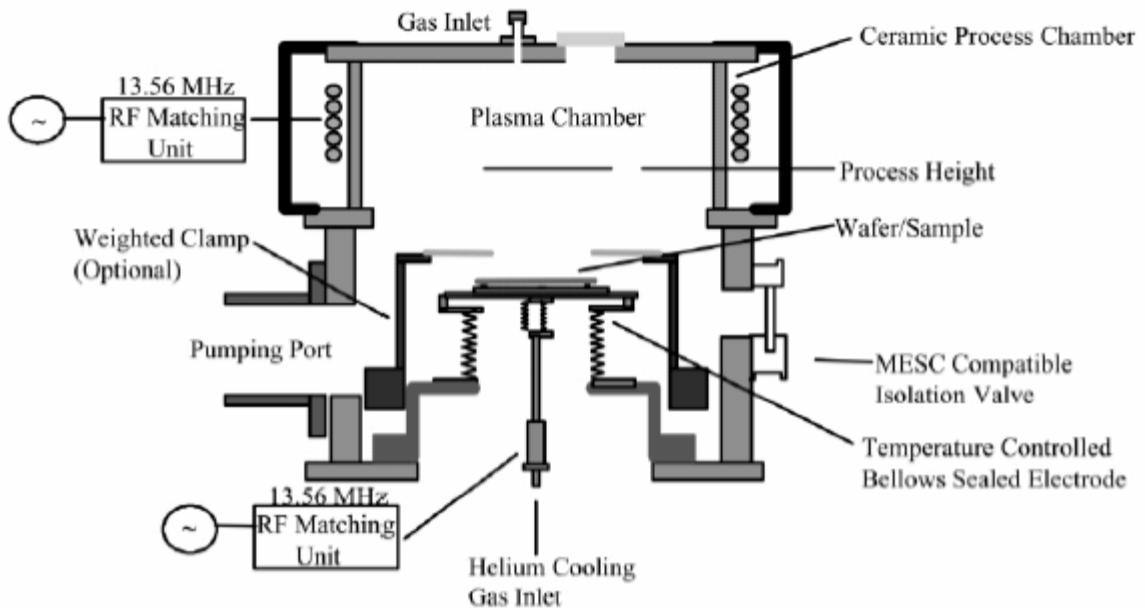


Fig. 34 Schematic diagram of ICP (STS Multiplex ASE) etcher system [47]

Results from STS DRIE ($150\mu\text{m}$ etched trenches) are shown in Fig. 35. The substrate is subjected to through-wafer DRIE to etch holes (Fig. 24d). The wafer is cleaned thoroughly after stripping (nanostrip) the photoresist and removing the oxide mask. The plasma etch leaves many contaminants and polymers on the wafer and it is

suggested to perform a rigorous RCA clean on the wafer. This is discussed in the next step.

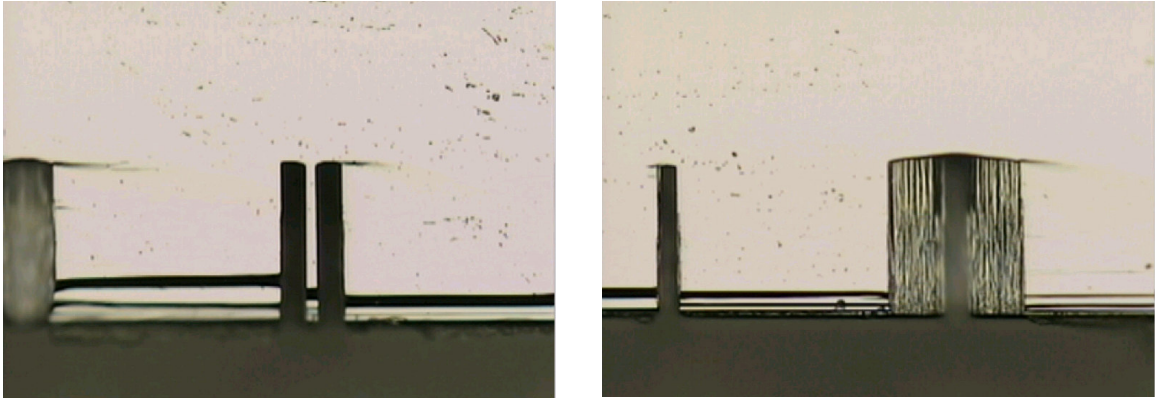


Fig. 35 Results from STS DRIE: 150 μ m etched trenches

2.2.5 Contamination removal and oxidation

Buffered Oxide Etch (BOE) solution (6 parts 40% NH_4F and 1 part 49% HF) etches away silicon dioxide (Fig. 24e) at an etch rate of 1200 $\text{\AA}/\text{min}$ at 22° C. Acid and base cleaning procedure is repeated to ensure complete removal of contaminants.

A fresh layer of silicon dioxide is grown on the cleaned wafer. The thickness of oxide is very crucial in this step as it later serves as a protective barrier for the sidewalls during TMAH (Tetra Methyl Ammonium Hydroxide) etching. At least 1 μm of thick wet oxide (Fig. 24f) is required to resist the etchant. The oxide thickness on the sidewalls is usually less than the thickness on the surface because the opening of the trench is very small and it takes time for the passage of oxygen inside the trench during thermal oxidation. However, caution should be taken not to grow a very thick oxide as it might lead to blocking of the trench. The wafer can now be prepared for silicon fusion bonding. Silicon fusion bonding requires the processed wafer to be bonded to a 3inch/4inch wafer. Later the bonded pair is subjected to anisotropic etching in TMAH. The first wafer is

protected by the presence of oxide mask on its surface and sidewalls. Only the bottom wafer is exposed to the etchant. Thus, the oxide layer serves as a protective mask for the first wafer and also helps in the bonding process by forming a strong adhesion layer between both the wafers.

2.2.6 Silicon Fusion Bonding

If two solids with clean and flat surfaces are brought into close proximity at room temperature, attractive forces pull the two bodies together into intimate contact so that bonds can form across the interface (Fig. 24g). There are many factors governing the bonding behavior of two surfaces. First of all, the surfaces must be flat and smooth. The second parameter governing the 'bondability' is surface chemical state and surface termination. The basic procedure in semiconductor wafer bonding starts with 'mirror polished' surfaces that are cleaned, 'activated' and given their final surface termination using a combination of chemical treatments. The wafers are then brought together at room temperature. If proper surface conditions apply, the wafers will bond spontaneously. After room temperature bonding a heat treatment at elevated temperature is performed to strengthen the interface bonding [48].

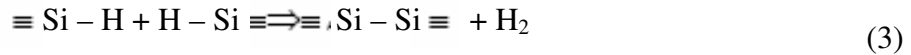
The forces involved in room temperature wafer bonding are mainly short-range intermolecular and interatomic forces, such as Van der Waals, capillary and electrostatic forces (Fig. 36). Therefore, wafer bonding puts high demands on surface microroughness, cleaning and chemistry. Surface pre-treatments in wafer bonding are classified in hydrophobic or hydrophilic treatments. Usually hydrophilic semiconductor surfaces are covered with native or thermal oxides. The surface oxide is terminated by polar hydroxyl groups, OH, and therefore attracts polar water molecules. The water molecules present

on the surface assist in spreading the 'bonding wave' and to form bridging between the mating surfaces during room temperature bonding. Upon the subsequent heat treatment the interface water either reacts with the surrounding oxide or diffuses away from the interface, so that covalent bonding is formed between the surfaces. At room temperature the linkage between surfaces in hydrophilic wafer bonding is achieved by two to three monolayers of water. Hydrophilic wafer bonding is therefore less sensitive to microroughness as compared to hydrophobic bonding. When the wafers have been bonded together at room temperature usually the interaction, or bonding energy, is relatively weak. Therefore, a heat treatment is performed to increase the bond-strength. The annealing enhances out-diffusion of interface trapped molecules and desorption of chemisorbed surface atoms, such as hydrogen. At the same time the annealing activates formation of covalent bonds between the bonded surface, like crystal-to-crystal bonding in the case of hydrophobic bonding.

A problem that sometimes occurs in wafer bonding is the presence of interface bubbles or voids. Macroscopic voids appear at the bonded interface due to i) trapped particles or dust contamination, ii) surface protrusion and iii) trapped gas. To avoid contamination of particles and dust on the surface before bonding, wafer bonding is preferably performed in a clean-room environment, or in a micro clean-room set-up [49]. Particles inhibit interaction between the opposing surfaces, and as a consequence a 1 μm dust particle trapped at the interface commonly results in an unbonded area (void) of 1 cm in diameter.

Gas bubbles occur either by air trapping during room temperature bonding or more commonly during the subsequent heat treatment. The reason for formation of interface

bubbles and voids upon storing or annealing is generally accepted as being nucleated by adsorbed hydrocarbons and increased in size by hydrogen entrapment [50]. Hydrogen is present both in hydrophobic and hydrophilic bonded interfaces (in hydrophilic bonding the hydrogen mainly originates from interface molecular water). In hydrophobic bonding, hydrogen is generated from surface hydrides during annealing:



In case of hydrophilic bonding, hydrogen is created from reaction with interface water molecules:



Hydrogen diffuses along the interface until they nucleate at locations of hydrocarbons or other interface cavities. When the pressure from trapped hydrogen gas exceeds the energy of adhesion a macroscopic void is formed. In silicon wafer bonding voids typically appear when annealing in the temperature range 200-800°C. Annealing above 800 °C usually makes the gas-filled voids disappear completely. Special care has to be taken in choosing proper surface treatment in order to avoid void formation. Other techniques to avoid formation of voids includes: bonding the wafers under vacuum condition, pre-etching wafers to make arrays of channels at the interface for the escape of trapped gases, pre-heating the wafers at 600-800 °C in argon or oxygen ambient, to oxidize and desorb hydrocarbons before bonding [51].

For hydrophilic bonds, normal surface preparation is achieved with a standard RCA clean immediately prior to the bond. The presence of hydroxyl radicals on the mirror polished silicon surface permits a good initial contact bond. The bond is initiated

by pressing in the middle of one of the wafers to create a preliminary point of contact. A single bonding wave propagates from the center of the wafers. The viscosity and pressure of the ambient gas as well as the wafer contact energy influences its speed.

Subsequent heating dehydrates the surface and promotes a number of processes. The hydroxyl groups form water molecules that cause the oxidation of the bonding surfaces resulting in a Si-O-Si bond as the hydrogen diffuses away. At higher temperatures oxygen will also diffuse into the crystal lattice creating a bond interface indistinguishable from the remainder of the silicon crystalline structure. As annealing temperatures are increased beyond 1000°C the strength of the bond approaches that of silicon itself.

RCA clean is repeated on the wafers followed by surface activation. This is done by exposing the wafers to oxygen plasma and the equipment used for this purpose is the March RIE. Ensure that the wafer pair is super-clean prior to plasma exposure.

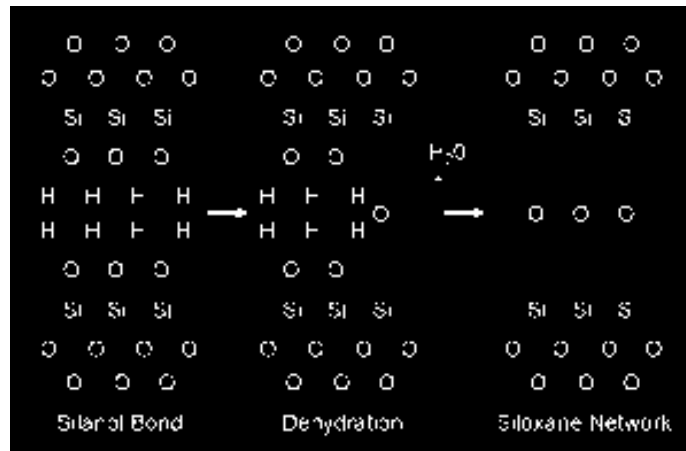


Fig. 36: Schematic of Si/Si bonding mechanism [52]

March RIE is a Reactive Ion Etching device (Fig. 37), primarily used to strip resist or etch patterns in wafers after the photolithography process. In this case it is used for surface activation of the wafers. High energy ions are accelerated toward the wafer in a

vacuum chamber, causing particles to be released from the substrate. This RIE is equipped with a process controller and solid state RF power generator.

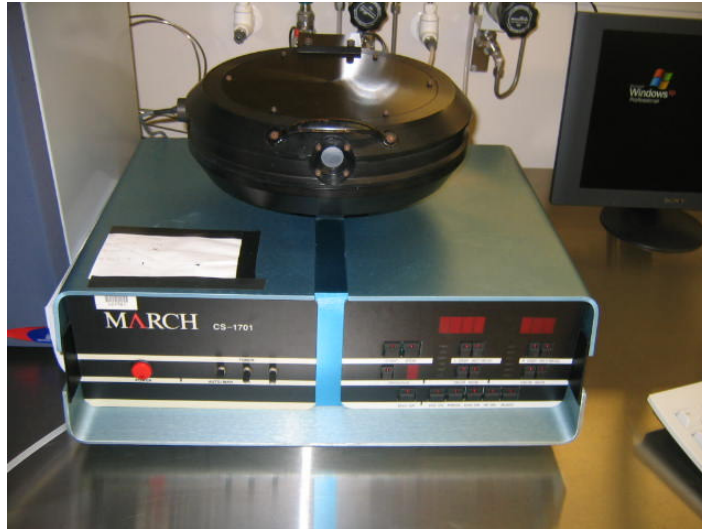


Fig. 37: MARCH Reactive Ion Etching device

The pair is exposed to the following conditions in the RIE system:

O₂ plasma, 150 W power, 400 mTorr pressure, 90 sccm (36%) O₂ flow, 5 min. Following plasma activation, the wafers are immediately dipped in DI water for a minute and then the surfaces are dried using nitrogen. They are now brought into proximity (at 45°) and the bond is initiated by pressing the center of the wafer for initiating a point of contact. The angle of contact between the two wafers is 45° so that when the etching is done in the next step, a three-dimensional etch profile is created. The wafer pair is annealed in nitrogen atmosphere at 1000°C in the Lindberg furnace.

2.2.7 Anisotropic etching

The anisotropic etching of silicon is a ubiquitous process in micromachining. Complex microsystems can be generated using the anisotropic properties of single-crystal silicon in an orientation dependent dissolution reaction. V-groove structures are easily fabricated using an anisotropic etchant like KOH or tetramethylammonium hydroxide

(TMAH). TMAH aqueous solutions (Fig. 38) are very favorable due to their excellent etch selectivity between Si and SiO₂. Bulk micromachining (Fig. 39) solution of 25%wt TMAH [CH₃]₄NOH] and 17% vol of IPA (Iso propanol) has an etch rate of 10 μm/hr @ 70C.

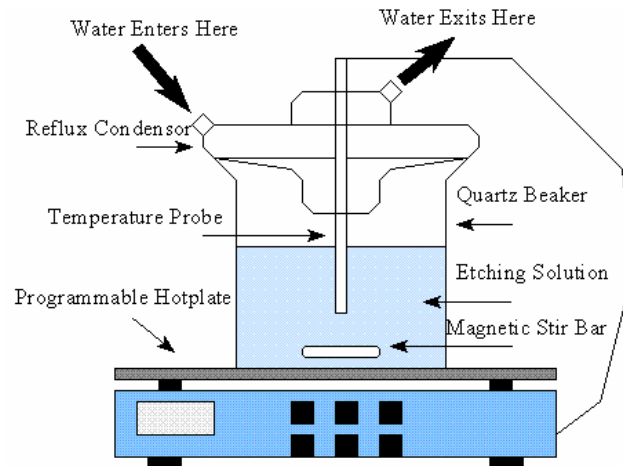


Fig. 38: Setup for bulk micromachining of Si wafer using TMAH

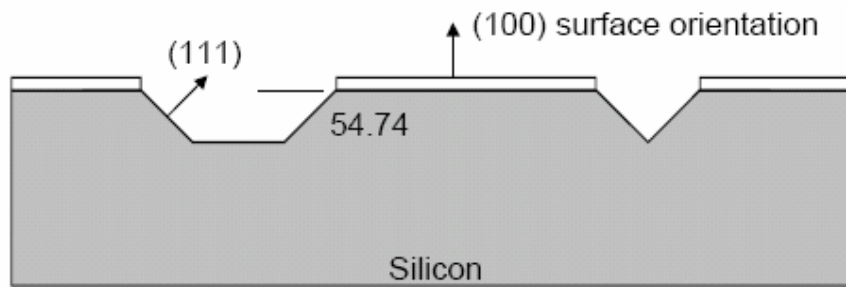


Fig. 39: Etch profile of Si using TMAH [53]

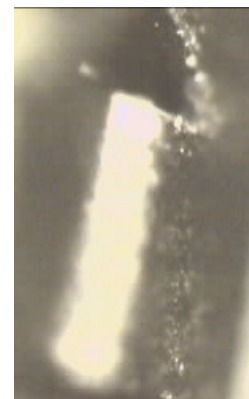
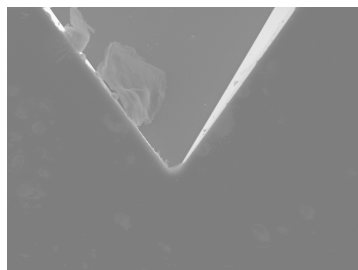
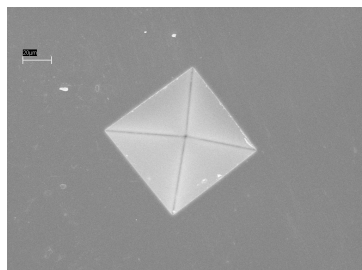


Fig. 40: Results of TMAH etching

In this experiment the feature size was also one of the main factors influencing the depth of the trenches etched. Fig. 40 shows the results of TMAH etch (30 to 50 μm deep trenches). In this case it usually takes more than the calculated etch time because the solution has to flow through the narrow holes and attack the surface beneath (Fig. 24h). Just before leaving the wafer pair in etching solution, it is advised to dip it in dilute HF or BOE for few seconds. This would ensure that the native oxide on the second wafer is completely removed. A thick layer of oxide (1 μm or more) on the top wafer helps in this step because while the native oxide of second wafer is being etched, some silicon dioxide on the top wafer will be etched as well.

2.2.8 BOE

After the wet etching is completed the pair of bonded wafers is left in BOE until all the exposed oxide is etched away. RCA1 and 2 cleaning procedures are repeated to remove any contamination inside the hollow molds (Fig. 24i). The mold is now ready for parylene deposition.

2.2.9 Parylene Deposition

The deposition process requires a special machine and consists of three steps.

1. Sublimation under vacuum at approx. 140°C of the stable crystalline dimer di-p-xylylene to produce vapors of this material.
2. Pyrolysis of the vapors at approx. 650°C to form gaseous reactive monomer para-xylylene.
3. Depositions and simultaneous polymerization to form poly-p-xylylene or Parylene.

The vapor deposition process (Fig. 41) begins when a measured amount of raw material (dimer) is heated in a vacuum system until the material sublimes to form a gaseous monomer. The gas then flows into a deposition chamber containing the substrate to be coated. Upon encountering the substrate, the gas converts into a solid polymer state, which takes the form of a completely conformal transparent polymer film. The thickness of the coating can be controlled by regulating the amount of gaseous monomer entering the chamber [54]. Parylene is deposited in thickness ranging from a few angstroms to 50 microns or more depending on the function of the parylene film. The equipment used to deposit parylene is the *Specialty Coating Systems PDS 2010* (Fig. 42).

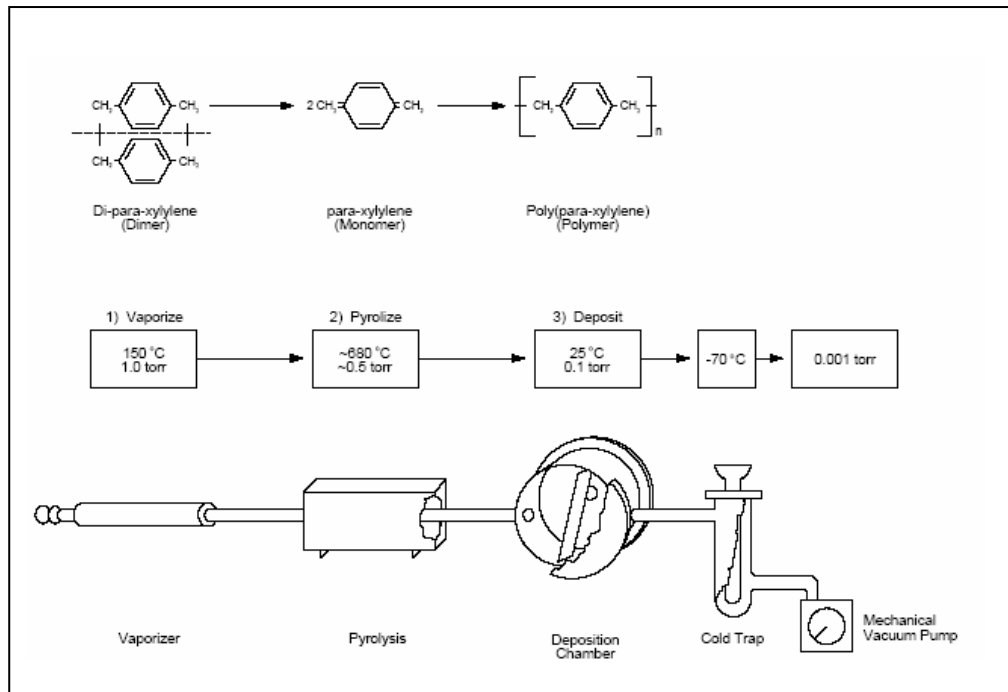


Fig. 41: Parylene deposition process [55]



Fig. 42: SCS Parylene Deposition System

This machine deposits a sublimated conformal layer of a polymer on the surface of objects under vacuum at nearly ambient temperature (Fig. 24j). This has the benefit of allowing bio-compatibility for implantation, thermal, vapor, chemical, mechanical and electrical barriers to substrates and devices with layers of micron and sub-micron thicknesses.

2.2.10 Releasing of the parylene

Parylene is released by etching away the entire substrate in TMAH solution. Parylene is inert to TMAH etching so there will be no effect on the polymer. Depending upon the thickness of wafers used, it takes couple of hours before silicon of the bonded wafers is etched completely. Even if the sample is left overnight, parylene will not get etched in TMAH. Conductivity of parylene can be improved by sputtering a thin layer of gold. This helps in capturing images under SEM (Fig. 24h, Fig. 24i).

CHAPTER 3

RESULTS AND DISCUSSION

Images of a diced sample deposited with parylene are shown in Fig. 43. This is prior to the releasing process. Parylene can be viewed under the SEM, even though it is non-conductive because it is still embedded in silicon, which is conductive. However, after etching away silicon, a layer of conductive material, like gold, has to be sputtered for viewing parylene under SEM. As indicated in the images, parylene conforms to sharp corners and crevices. The top left image is taken under an optical microscope and the other ones under an SEM. SEM gives a far better resolution than the optical microscope and is very accurate in taking measurements.

Dicing the sample helps in measuring the dimensions of the parylene, tightly embedded in silicon. This gives a comparison of microstructures before and after the releasing process. Changes in dimensions, if any, can be noted. Also, it helps in determining if parylene is deposited all the way till the end. The sample has to be diced accurately at the center. An array (or row) of features has to be selected for dicing. The blade position and the thickness of dicing blade can be calculated from the feature size. The dicing blade has to be accurately aligned at the center of the feature.

The final results of parylene microstructures, taken at different angles and magnifications are shown in Fig. 44. The dimensions are as indicated in Fig. 45. The length of the trunk is same as the thickness of the top wafer. It is usually between 250-

350 μm in length and the base formed by TMAH etching is 57 μm deep and 100 μm wide. These dimensions depend on factors like feature size and etch time.

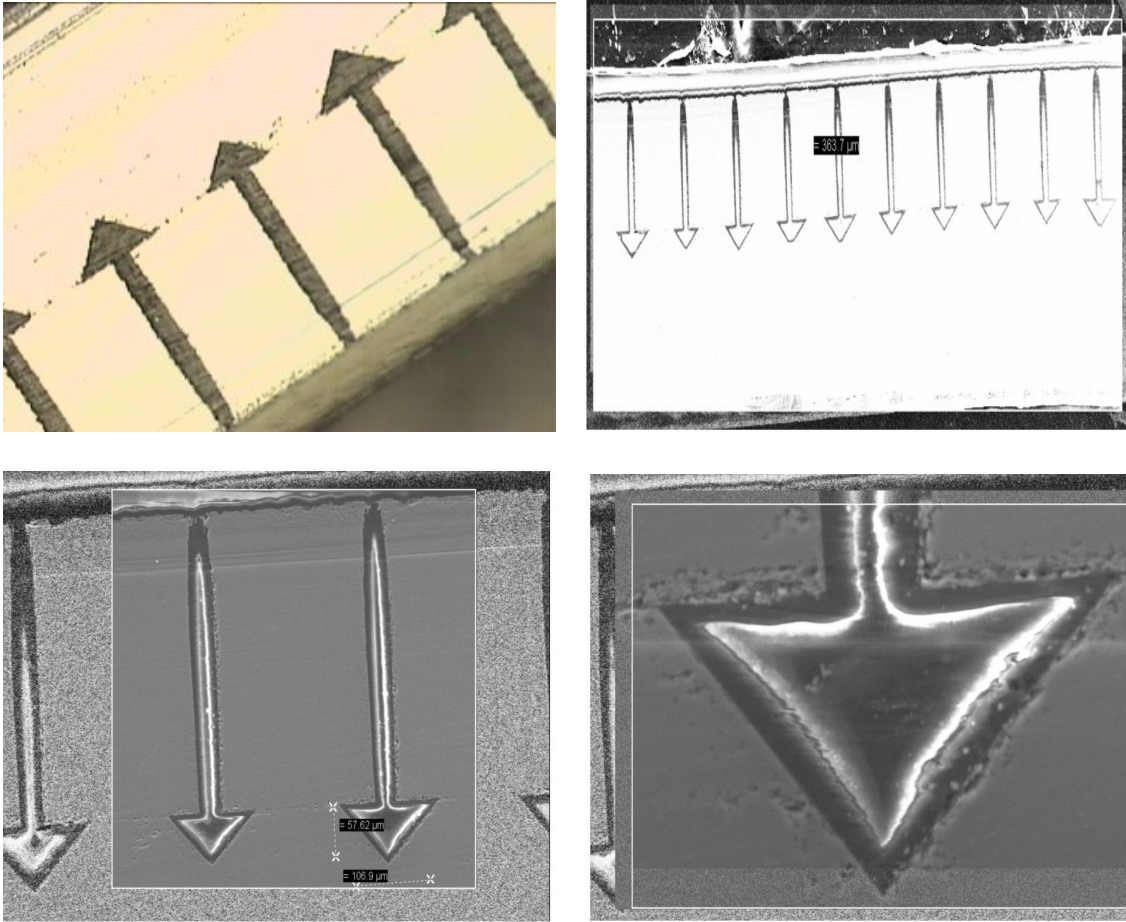


Fig. 43: Optical and SEM images of parylene deposited diced samples

Results of TMAH etching vary with the feature size. Each sample has features of different sizes, which are exposed to TMAH etching for the same amount of time. The results vary with the feature size, even though they are exposed for the same length of time. This is because of the narrow passage for small feature sizes. As indicated, the smaller features have smaller pyramids or caps and likewise.

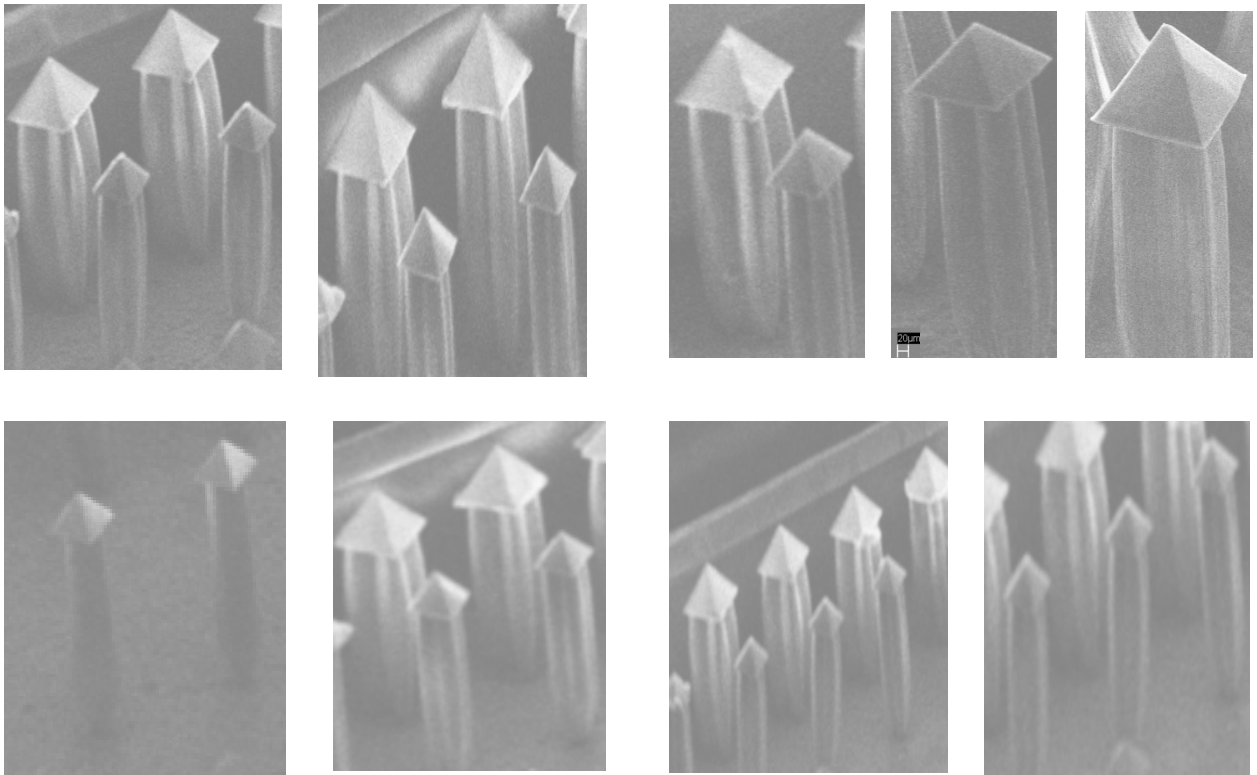
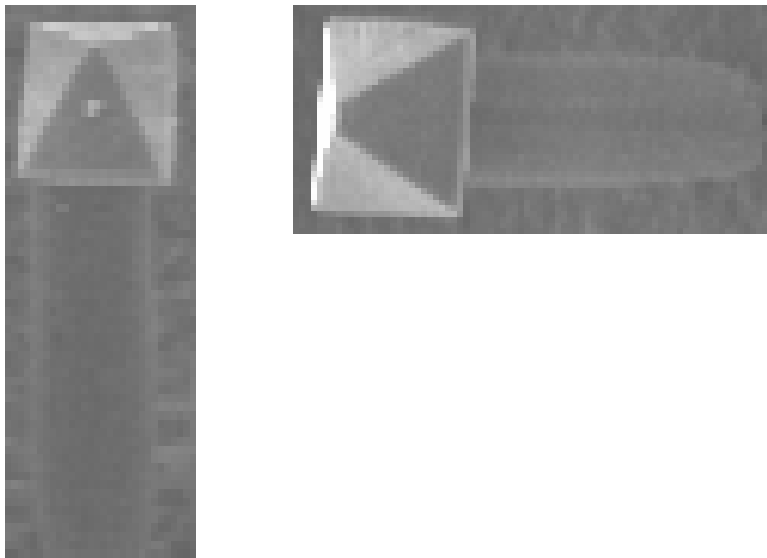


Fig. 44 SEM images of released parylene at different angles and magnifications



200µm
|-----|

MAG = 37 X
EHT = 20.00 kV

WD = 7 mm

Signal A = SE1
Photo No. = 3873

Date :20 Feb 2004
Time :16:58:38

Fig. 45 SEM images of parylene at different angles and magnifications

The wafers used (only the top wafer, in which DRIE holes are etched) for this experiment can be single or double side polished. It is recommended that double side polished wafers be used only after the experiment parameters are well established. They are more expensive than their single side polished counterparts. During silicon fusion bonding, the polished surfaces of both the wafers are bonded. The unpolished surface of the first wafer forms the base for these microstructures. The roughness of the unpolished side will be reflected in the final results, as parylene takes up the shape of the

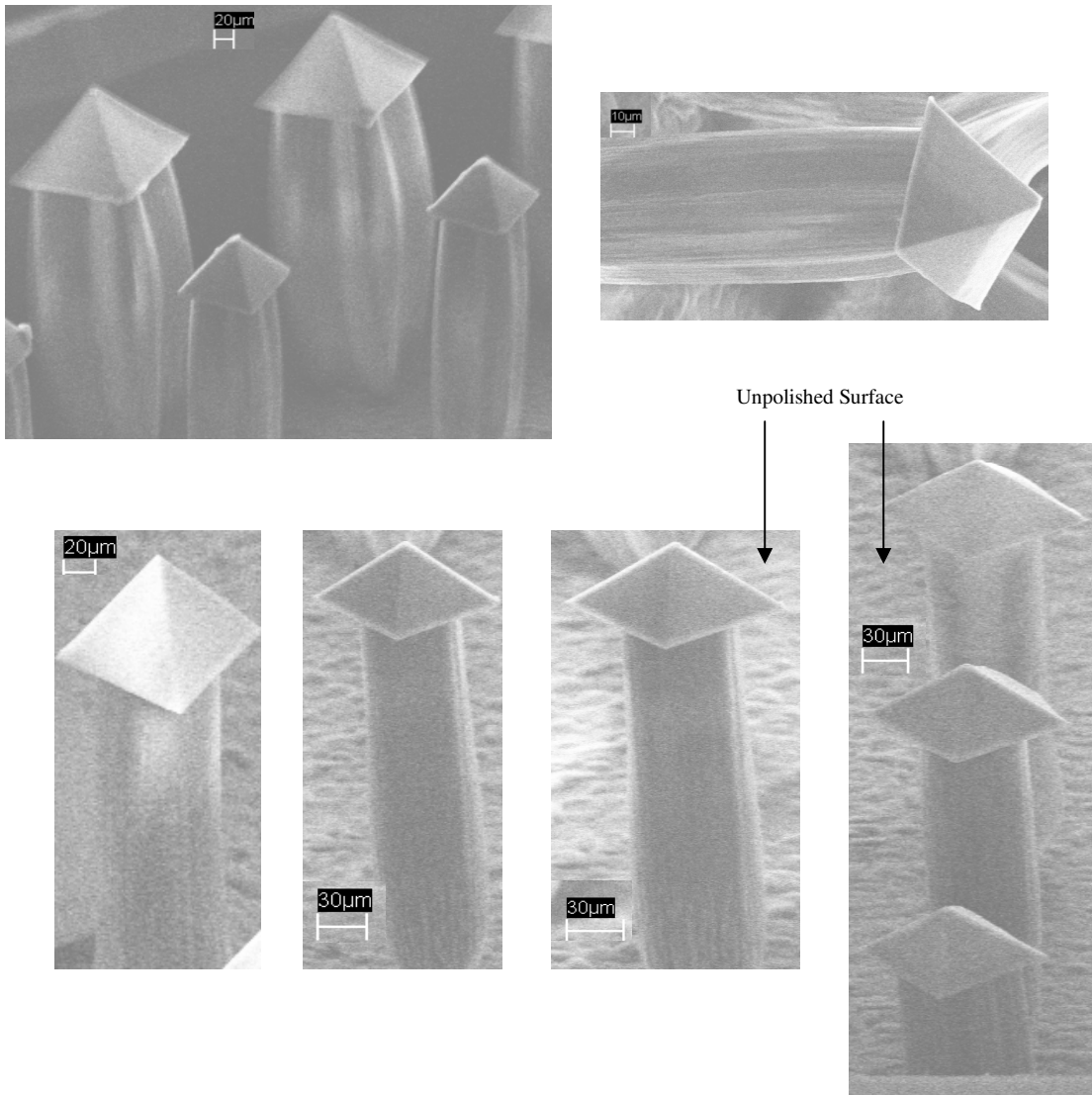


Fig. 46 SEM images of parylene at different angles and magnifications

rough surface. This is shown in Fig. 46. The surface looks much smoother if a double side polished wafer (first wafer) is used. It is not necessary to use a double-side polished wafer for the second wafer as the roughness of the base depends only on the first wafer.

Fig. 47 shows the optical images of the same microstructures. These were taken before the samples were imaged under SEM. They were later helpful in determining the cause of “ballooning effect” (Fig. 48) which will be discussed next.



Fig. 47: Optical images of the released parylene microstructures

While imaging the samples under the SEM, a ballooning effect (Fig. 48) was observed which could be accounted for the pressure differences and not any fabrication defects. This is validated by the fact that when the sample was imaged under the optical microscope prior to using it under the SEM, there was clearly no indication of any swelling at the roots (refer Fig. 47). Though the optical image is not clear enough (due to reflectivity of parylene), it definitely helps in confirming that the ballooning was not a fabrication defect, but the effect resulting from exposure to vacuum under the SEM. While filling up the molds with parylene, it is unlikely that the trunk of the structure is completely filled. This is because it takes time for parylene to get through the narrow passage (trunk) and deposit at the bottom. Meanwhile, the opening tends to get blocked,

leaving some areas in the trunk unfilled. While imaging the samples under SEM, they can be left in the vacuum for a long time (more than an hour) so that they can come back to their original shape.

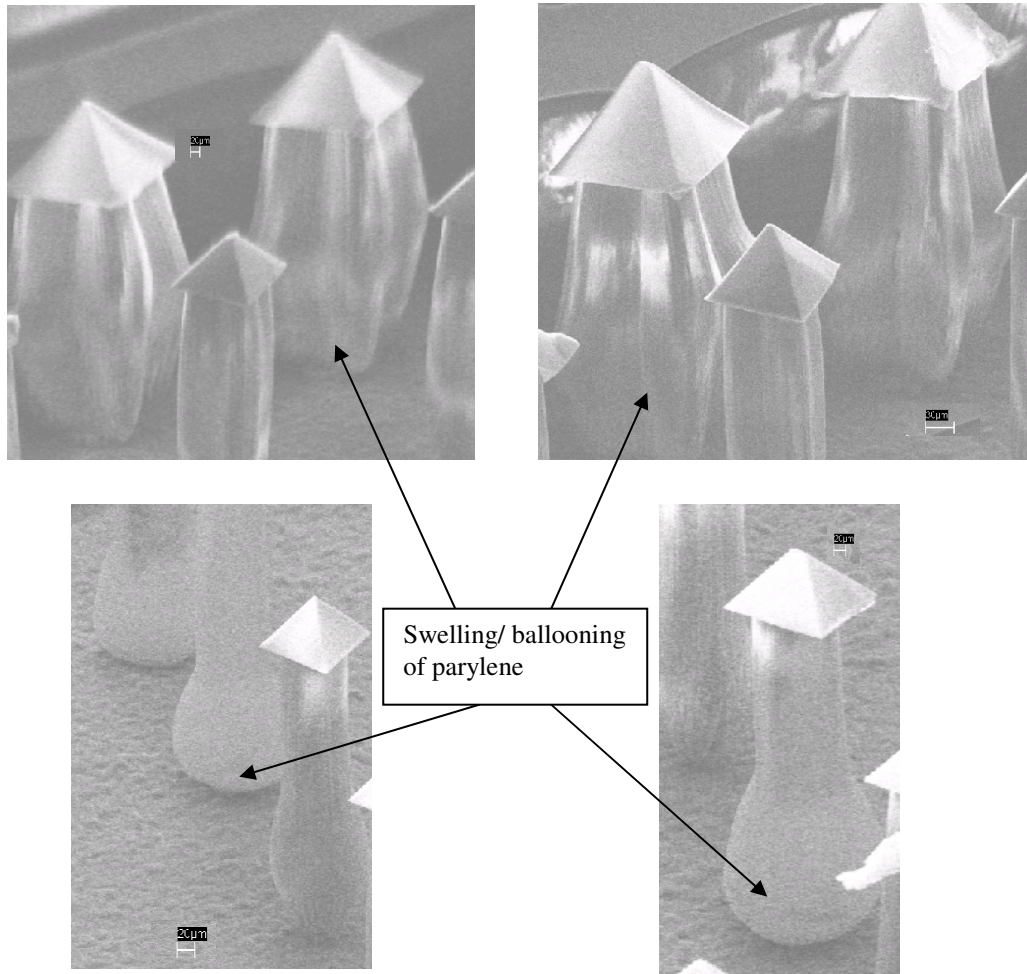


Fig. 48: Swelling of parylene due to pressure difference (vacuum in SEM)

The fabrication sequence shown in Fig 24 has to be followed strictly. However, the parameters for each step were selected after testing the sample for the following steps. For instance, various photoresists were tested under dry etch to observe which one survives best in plasma etch. Based on the results of DRIE, OCG thick was chosen for patterning in the previous step (Refer Fig. 24c and 24d). Since OCG is a negative resist, a light field photomask had to be processed. Similarly, as discussed in section 2.2.5, 1 μm

of wet oxide was grown on the plasma etched wafer (Fig. 24f) because after silicon fusion bonding the wafer pair had to be dipped in oxide etchant for removing native oxide on second wafer. The oxide layer had to be very thick because it was obvious that the oxide on the top wafer would be attacked as well. The main purpose of growing oxide on the first wafer was to protect the sidewalls from being etched in TMAH. A very thick layer cannot be grown because it would end up sealing the passage completely. 1 μm of oxide was thick enough to protect the sidewalls and survive the dilute BOE dip.

Instead of working with one wafer at a time, a batch of wafers can be processed and stored at different stages of fabrication. This should be done only after the specifications for that step have been well determined. This way if a wafer gets spoiled in subsequent steps, the process does not have to be repeated from step1. A new wafer can be selected from the batch and processed from that step forward. For example, after confirming that OCG is the resist most suitable for DRIE, a batch of wafers can be patterned using that resist. After this stage, one or two wafers from the batch can be processed further. If these wafers go bad while determining the parameters for latter stages (say, silicon fusion bonding), a fresh patterned wafer can be used from the batch and processed from the DRIE step onwards. Accordingly, when silicon fusion bonding is successful for the first sample, other wafer pairs can be bonded and stored aside for future use. If a bonded pair goes bad during parylene deposition, other pairs can come handy. It takes only two steps (TMAH etch and oxide removal - Fig. 24h and i) to prepare them for deposition. The process need not be started from the very beginning because this batch of wafers has already been processed until the 'silicon fusion bonding' step. This method saves time, is cost-effective and increases productivity.

Silicon fusion bonding is a crucial part of the experiment. As discussed in section 2.2.6, a strong silicon fusion bond can be initiated only when the task is carried out in a very clean environment. Especially because it is the activated molecules on the surfaces of the wafers that interlink together, forming a bond. There can be no bonding between unclean or rough surfaces. Also, it is much easier to bond the wafers that are oxidized. In this case bonding is between an oxidized and unoxidized wafer. No adhesives or epoxy can be used between the wafers because they are inappropriate for TMAH solution and parylene deposition system. The bonding has to initiate at a molecular level and even one speck of dust makes a huge difference. It would be better if this task is carried out in a class 100 facility. While processing the wafers for bonding, care should be taken to maintain smooth and clean wafer surfaces. If scratches or dust are left behind in previous processing steps, there will be poor or no bonding. Obtaining a successful bond highly depends on these two factors. As described earlier, silicon fusion bonding is a four step process: cleaning, activation, bonding and annealing. The time gap between these steps should be minimal. The complete bonding process takes roughly six to eight hours. Caution should be taken to avoid situations that enhance impurities. It's advised to perform the bonding when there are minimum lab users around. Also, new pair of gloves should be used when initiating the bond by pressing the wafer at the center. This should be the only time when the wafer comes into direct contact with the hand. Apart from this step, always use sterilized tweezers to handle wafers in all the steps. Be careful not to mishandle them and cause scratches. This would adversely affect the bonding. Only DI (de-ionized) water should be used. If this procedure is followed accurately, chances of successful bonding are very high. After the DRIE and prior to oxidation, it is advisable to

process the wafer in acetone, chlorobenzene, xylene, nanostrip and DI water. This ensures the removal of stubborn contaminants and residues from the etching process.

It is essential that the bonding between the two wafers is good, because parylene conforms to virtually any shape, including sharp edges, crevices, points and if there is weak bonding at some points, parylene will deposit in the crevices between the wafers as well (Fig. 49). For every structure to be isolated, a strong fusion bond should be ensured. The places where the bonding is weak can be easily recognized after the final step when the substrate is etched away after parylene deposition.

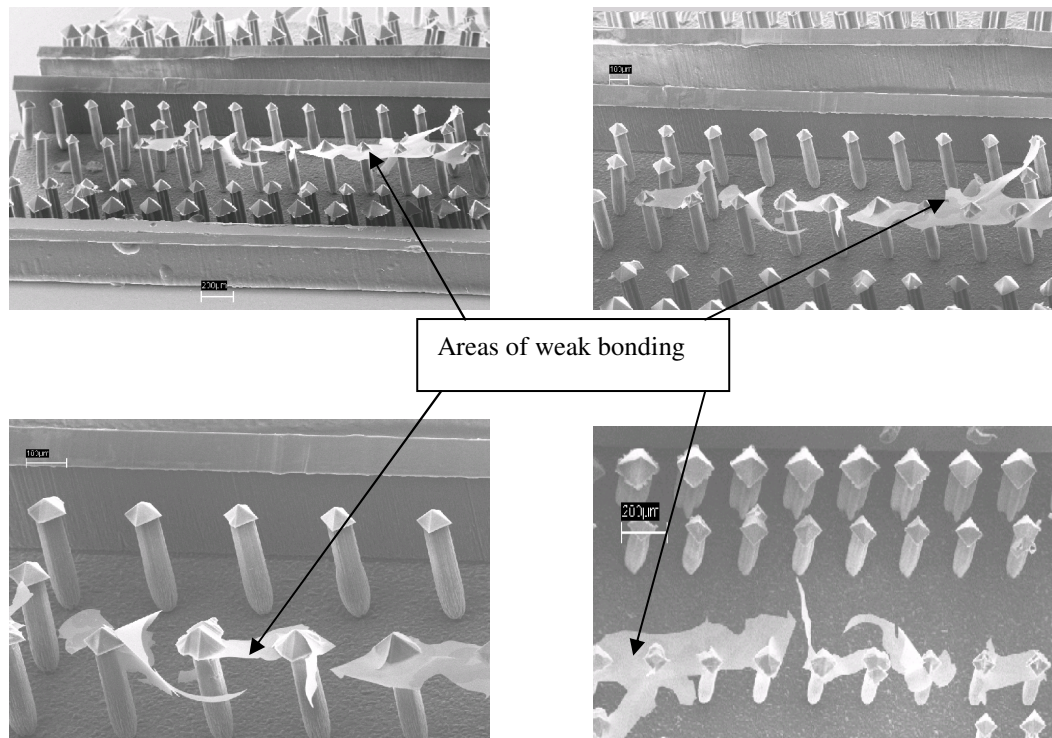


Fig.49: Deposition of parylene in areas of weak bonding

CHAPTER 4

CONCLUSIONS AND RECOMMENDATIONS

The unique properties of parylene have been conveniently combined with MEMS technology, to meet biocompatibility requirements of biological and chemical applications. High aspect ratio molds in silicon have been successfully fabricated and parylene has been deposited in these molds. The released parylene structures, which are now in the shape of the molds, can be tested for implants and similar biomedical applications.

Similar techniques can be combined to design parylene into a desired shape. Since etching of parylene is not readily possible, the best way to mold it into any shape would be to fabricate molds and deposit parylene in them. Until now parylene was mostly utilized for its barrier properties and has been used as a protective material for circuit boards and similar applications. By investigating its biocompatible properties, its adaptability in medical field has been established. Since most of the procedure is carried out in a class 1000/100 cleanroom facility, contamination is reduced to a minimum.

This thesis proves that it is possible to mold parylene and similar materials by etching the desired shape in silicon and depositing the material. Many applications can be derived from this method, depending on the type of mold and the kind of material deposited in them. While selecting the material to be filled, it is essential to test the reactivity of this material with silicon and also, the ability to easily flow through the

narrow passage. The obvious choice would be a gas or a less viscous liquid that transforms into a solid on cooling. Chemical vapor deposition of diamond in the trenches can be tried and used as atomic force microscope tip. Exposing the sample in oxygen can result in conversion of silicon to silicon dioxide and completely filling up the trenches. Similarly, silicon nitride can be experimented for same application. Another factor that influences the choice of these materials is their reactivity with TMAH, which is used to release the microstructures.

The CAD (ACES) simulation gives the designer an opportunity to generate creative designs by combining the masks with different wafer orientations ($\langle 100 \rangle$, $\langle 110 \rangle$, $\langle 111 \rangle$). This tool comes in handy at the beginning of a project and gives an idea about the fabrication steps. L-Edit is another software, which is very efficient in designing the mask features accurately. It reproduces the mask layout for in a file that can be used in printing the mask.

While designing the procedure, it is essential to check if all the facilities are available in the laboratory. Some procedures are standard and are applicable to any wafer, whereas, most of the time, special parameters have to be established for that particular process. And these parameters can be exclusive to this process only. Also, they can vary with the size and orientation of wafers.

In any experimental procedure it is crucial that the wafer surface is maintained clean. Any impurities will be reflected in the final results and can result in failure of the next steps. Even if the wafer is stored inside the cleanroom, there is a possibility of contamination or reaction with atmospheric oxygen. If the samples are used after a while (like after a day or so), performing RCA cleaning, prior to the processing, ensures

removal of any impurities. A RCA clean should be performed whenever a wafer comes into contact with chemicals (like BOE, TMAH), prior to thermal oxidation, after dicing, after storing for a longtime, after etching processes (dry or wet) and whenever the sample is taken outside the cleanroom.

The defects in the results should be studied in detail and the cause has to be investigated and rectified before proceeding to the next step. This can resolve some important fabrication issues and can also lead to some important discoveries. Every observation has to be well documented for future reference by other lab users.

The samples have to be continuously monitored during the processing because practical implementation may not follow the theoretical calculations. There are other factors as well, which may influence the process. Under ideal situations like a given atmospheric pressure, temperature and so on, the experiment results will be as expected. These conditions will be maintained at all the times in the lab. However, there are certain factors that have to be taken into account like, number of lab users, which will have an effect on the results of an experiment (example, silicon fusion bonding). Additionally, the presence of other samples under the same fumehood, like a wafer left in nanostrip generates vapors in the fumehood, which react with the sample. Sometimes the success of a process depends on these factors too. The goal should be to avoid contamination in every step. The next step in the experiment would be to test the structures inside a human body for characterizing the efficiency of these devices. Since each structure is bound by a layer of parylene at the base, they can be isolated by simply peeling or cutting off each device. Also, the sputtered gold can be dissolved in a gold solvent. Care should be taken to cleanse human

and chemical contaminants prior to testing. The deposited parylene can be characterized by testing for different properties listed in Fig. 50, 51, 52.

Properties	Parylene N	Parylene C	Parylene D
Melting Point (°C)	420	290	380
T5 Point (°C) (modulus = (10 ⁵ psi))	160	125	125
T4 Point (°C) (modulus = (10 ⁴ psi))	>300	240	240
Linear Coef. of Expan. at 25 °C (x10 ⁵ , (°C) ⁻¹)	6.9	3.5	3-8
Thermal Conductivity at 25 °C (10 ⁻⁴ cal/(cm·s· °C))	3.0	2.0	-
Specific Heat at 20 °C (cal/g· °C)	0.20	0.17	-

Fig. 50 Thermal Properties of Parylene [56]

Properties (1)	Parylene N	Parylene C	Parylene D
Dielectric Strength, dc volts/mil short time, 1 mil films ^a	7,000	5,600	5,500
corrected to 1/8 in	630	500	490
Volume Resistivity, ohm-cm, 23 °C, 50% RH ^b	1.4X10 ¹⁷	8.8X10 ¹⁶	1.2X10 ¹⁷
Surface Resistivity, ohms, 23 °C, 50% RH ^b	10 ¹³	10 ¹⁴	10 ¹⁶
Dielectric Constant ^c 60 Hz 1 KHz 1 MHz	2.65 2.65 2.65	3.15 3.10 2.95	2.84 2.82 2.80
Dissipation Factor ^c 60 Hz 1 KHz 1 MHz	0.0002 0.0002 0.0006	0.020 0.019 0.013	0.004 0.003 0.002

Fig. 51 Electrical properties of parylene [56]

Properties (1)	Parylene N	Parylene C	Parylene D
- Secant (Young's) Modulus (psi)	350,000	400,000	380,000
- Tensile Strength (psi)	6,000-11,000	10,000	11,000
- Yield Strength (psi)	6,100	8,000	9,000
- Elongation to Break (%)	20-250	200	10
- Yield Elongation (%)	2.5	2.9	3.0
- Density (g/cm ³)	1.10-1.12	1.289	1.418
- Index of Refraction (n ₀ ²³)	1.661	1.639	1.669
- Water Absorption (% after 24 hrs)	----- Less than 0.1 -----		
- Rockwell Hardness	R85	R80	R80
- Coefficient of Friction			
Static	0.25	0.29	0.33
Dynamic	0.25	0.29	0.31

Fig. 52 Physical and Mechanical properties of parylene [56]

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Qualifications:

Proven expertise in team-based environment, ability to implement creativity, strong problem solving skills, multi-tasking, technical presentation and effective communication and collaboration skills. Highly motivated, inquisitive, creative and resourceful with a strong desire to share knowledge and pursue engineering and management skills.

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M.S in Electrical and Computer Engineering (Pursuing)
University of Louisville, <http://www.louisville.edu/>, Louisville, KY
GPA (3.40/4.00)

B.Tech Degree in Electronics and Communications Engineering
JNTU, Hyderabad, India
Graduated in June 2000. GPA (3.80/4.00)

System Knowledge:

DOS, UNIX, Windows, C, C++, HTML, VB6.0, VBScript, Toolbox ST, Mercury Test Director, Quick Test Professional, .NET, Cadence, Access, L-EDIT, Lab View VI, Matlab, Magic, Simulink, IRSIM, ACES, PSpice, Microsoft Office

Work Experience:

Associate Controls Engineer, General Industries, TMEIC-GE, Salem, VA, January 2005- till date

- Specifications for drives and controls used in Mining, Navigation, Coal Industry, Paper Industry
- Test Automation
- AutoCAD layouts for assembling the drives

STEP Intern, Product/Process Reliability Department, GE Energy, Salem, VA, January 2005 – December 2005

- I/O Distribution Firmware Validation for Turbine Control Systems (MarkVIe)
- Firmware Test Automation
- Execution of Testplans and Interpretation of results

Graduate Student Assistant, Electrical and Computer Engineering Department, University of Louisville, Louisville, KY, 2001 – 2004

- Instructor for Control Systems Lab

- Responsible for lab maintenance, scheduling tasks, calibration and upgrading of the equipment on a regular basis
- Supervision of lab users

Assistant Engineer, Electronics Corporation of India Limited (ECIL), Department of Atomic Energy, Hyderabad, India, 1999- 2001

Signal Processing and Control Electronics for Temperature Compensation and Modulation of Fiber Optic Gyroscope (FOG)

- Design, development, fabrication and testing of electronics to provide temperature compensation for variation in NULL and SCALE FACTOR over a temperature range of -30°C to $+70^{\circ}\text{C}$. The FOG output, NULL voltage and SCALE FACTOR are highly susceptible to temperature variations. Fiber optic gyroscope sensors have applications in robotics, defense, automobile industries and especially aerospace for stabilization and sub-inertial navigation.
- Implementation of test software and hardware for test setups, recording performance characteristics and sources of errors and analysis of results. Circuitry consists of temperature sensor, A/D and D/A converters, EPROM, CMOS switches, counter, decoder and op-amps.
- Programming the EPROM: Loading the data through keyboard and loading the data through software. While the EPROM is in circuit, it can be used for reading data or for programming data into it. The read operation is performed more often than the programming operation, which is performed only once, generally after the chip has been erased. Programming is done by a special device 'EPROM programmer'

Technical Projects:

Development of a model for capacitive microphone using LEDIT software

- Optimization of the resolution involves the resonance frequency defined by the membrane area, the thickness and stress, to be placed slightly above the upper frequency limit of the measured signal. In practice, stress and thickness are defined by the fabrication process, and most of the membrane materials used show very high stress, that microphones with a small membrane area (in the order of 1 mm^2) cannot be optimally designed. A stress-releasing technique is to form corrugations in the diaphragm.

Designing and building of a pressure transducer using piezo-resistive elements

- Microfabricated pressure sensors comprise a small but useful subset of integrated circuits. Integrated sensors of high quality can be very sensitive to pressure changes, making them ideal for applications in which bulky machined sensors are not able to perform, or are too large, or consume too much power. Typical applications of integrated pressure sensors include microphones, biomedical instrumentation (*e.g.*, blood and fluid pressure), vacuum sensing, wind-tunnel model instrumentation, automobile power and acceleration measurement, and even household electronics

Integrated circuit layout of a Serial-in parallel-out and parallel-in parallel-out register using MAGIC software for VLSI design. Chip manufactured by MOSIS Company, CA

- Shift registers are a type of sequential logic circuit; a group of flip-flops connected in a chain so that the output from one flip-flop becomes the input of the next flip-flop.

Design and fabrication of biomedical VELCRO (Master's Thesis)

- The unique properties of PARYLENE (poly-para-xylylene) can be conveniently combined with MEMS technology, to meet biocompatibility requirements of biological and chemical applications. Due to the biocompatible nature and barrier properties of parylene, these microstructures can be used for implants and other biomedical applications.

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Available upon request