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Antonio Dell'Aquila, Agostino Lecci

A Current Control for Three-Phase Four-Wire Shunt Active Filters

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Professional paper

An active filter has been proposed to compensate for harmonic distortion, line neutral current and reactive power in three-phase four-wire systems.

The focus is concentrated on current control in order to achieve optimum current tracking by means of fixed frequency driving signals. The effectiveness of proposed control was proved in simulations where the harmonic pollution and imbalance caused by a highly distorting load have been drastically reduced.

Key words: active filters, fuzzy logic, harmonics, power quality

1 INTRODUCTION

Shunt active filters are designed to compensate for harmonic currents, reactive power and neutral current by injecting filtering currents into the electric grid. These can be considered as a controlled current source and prove to be particularly effective when their control system provides a good reference tracking [1–17]. The simplest control technique for current controlled PWM inverters, used as an APF, is hysteresis control. However, at critical points, where changes of reference waveform slope are unpredictable, hysteresis control causes a dangerous increase in switching frequency which cannot be justified, even if it has the advantage of not exceeding the designed error band.

The proposed current control, on the other hand, aims to reduce tracking error, by means of a fixed frequency driving signal. During the switching period in each inverter leg, the control allows the proper state for a longer interval resulting in the quickest possible error reduction. Furthermore, the frequency of the driving signal remains fixed. Active filter regulation is achieved by means of a fuzzy controller which corrects the amplitude of mains fundamental current reference in order to move the power balance. In transients and at start up the supply is asked to feed an amount of power different from that absorbed by the load, in order to compensate d.c. side voltage error.

The effectiveness of the proposed active filter control was proved in a simulation, where the compensation of the harmonic pollution caused by a hard distorting and unbalanced load is carried out, and is evaluated by means of a performance index. Harmonic compensation as well as reactive power reduction and line neutral current reduction are achieved by using 10 kHz inverter switching signals.

2 ACTIVE FILTER TOPOLOGY AND REFERENCE COMPUTING

The proposed three-phase four-wire shunt active filter is shown in Figure 1.

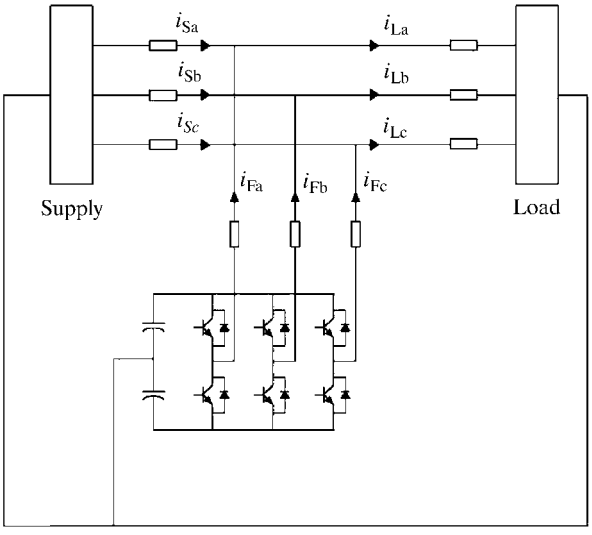

Fig. 1 Proposed three-phase four wire active power filter

The active power filter (APF) is made up of a three-phase inverter which is connected to the mains by passive output filters. The output filter consists of a link reactor, which limits the amplitude and frequency of the switching ripple.

Reference computation is achieved aiming at three different compensating tasks. Line neutral current reduction remains the main goal, but by means of a proper reference waveform, reactive power and harmonics compensation can also be achieved.

The aim is to make mains provide a set of three balanced sinusoidal currents in phase with the mains voltage, so that full active power absorbed by the load is fed by the mains. The amplitude of the mains currents which satisfies these ties is as follows:

$$\hat{I}_{Smean} = k\frac{\hat{I}_{La1}\cos\varphi_{La1} + \hat{I}_{Lb1}\cos\varphi_{Lb1} + \hat{I}_{Lc1}\cos\varphi_{Lc1}}{3}. \quad (1)$$

The term k allows d.c. bus voltage regulation: in fact d.c. bus voltage regulation acts on the amplitude of mains fundamental reference currents with a gain k, in order to let a part of the fundamental frequency current to be fed or drained by the active filter. The value of k is quite near to unity.

In order to charge the d.c. bus capacitors, the power fed by the source must be higher than that absorbed by the load ($k > 1$). Power in excess is drawn by the active filter which lets the d.c. capacitors charge.

In order to discharge the d.c. bus capacitors, the power of the source must be lower than that absorbed by the load ($k < 1$). The dearth power is given by the active filter which lets the d.c. bus capacitors discharge.

A fuzzy controller has been used to compute the factor k, in order to manage the energy balance among the grid, the load and the active filter.

3 DC BUS VOLTAGE CONTROL

The d.c. bus voltage control, is described in Figure 2.

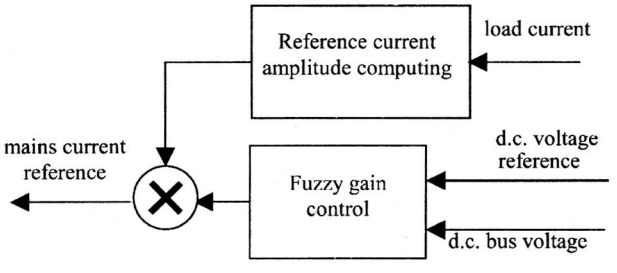

Fig. 2 Mains fundamental reference generator block

This consists of a block implementing equation (1) and the amplitude of the output current is modulated by the gain k. The value of k is quite near to unity; when k is above unity, more power is required from the mains than that required by the load. Power in excess is drawn by the active filter which lets the d.c. capacitor charge. When k is below unity, the d.c. bus voltage decreases.

The optimum value for the k gain is calculated by a fuzzy inference system, which receives as inputs the slope of d.c. average bus voltage and d.c. voltage error. Both quantities are normalised by suitable values. Thus, each range is between –1 and 1 normalised unity.

The whole range is covered by the membership functions shown in Figures 3 and 4. The values inferred for k gain are not too far from unity as Figure 5 displays. The numbers placed above the membership functions are fuzzy set labels. Each label represents its membership function and it is the mean value of the range of the same fuzzy set.

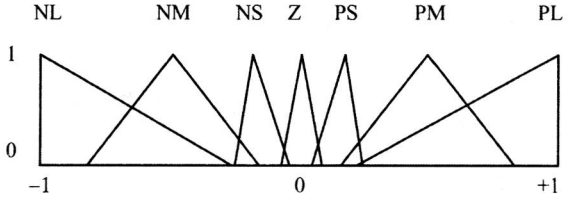

Fig. 3 d.c. voltage error normalised membership functions

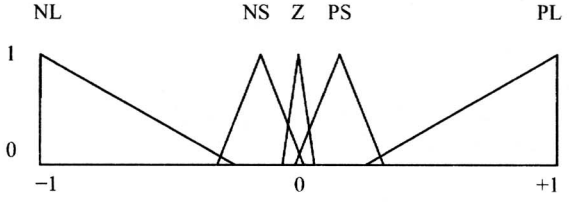

Fig. 4 d.c. voltage slope normalised membership functions

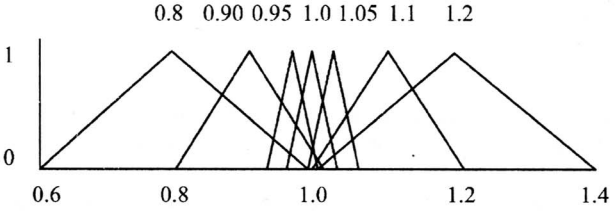

Fig. 5 Output weight membership functions for k value

In Table 1 a breakdown of the inference rules for fuzzy control is shown, where: NL = Negative Large; NM = Negative Medium; NS = Negative Small; Z = = Zero; PS = Positive Small; PM = Positive Medium; PL = Positive Large.

Table 1 **Fuzzy rules for d.c. bus voltage control**

		voltage error						
		NL	NM	NS	Z	PS	PM	PL
d.c. voltage slope	NL	0.80	0.90	0.95	1.0	1.05	1.1	1.2
	NS				1.0			
	Z				1.0			
	PS				1.05			
	PL				1.05			

Therefore if the time reference frame is synchronised with mains voltage in phase »a«, reference currents for the APF are:

$$\begin{aligned} i_{Fa}^{*} &= i_{La} - i_{Sa}^{*} = i_{La} - \hat{I}_{Smean} \sin \omega t, \\ i_{Fb}^{*} &= i_{Lb} - i_{Sb}^{*} = i_{Lb} - \hat{I}_{Smean} \sin\left(\omega t - \frac{2}{3}\pi\right), \\ i_{Fc}^{*} &= i_{Lc} - i_{Sc}^{*} = i_{Lc} - \hat{I}_{Smean} \sin\left(\omega t - \frac{4}{3}\pi\right). \end{aligned} \quad (2)$$

4 CURRENT CONTROL

The proposed current control computes the duty cycle for each leg in order to ensure zero tracking error by the end of the switching period. In Figure 6, the bold line represents the reference current while the other is the filtering current, in the hypothesis of zero final tracking error.

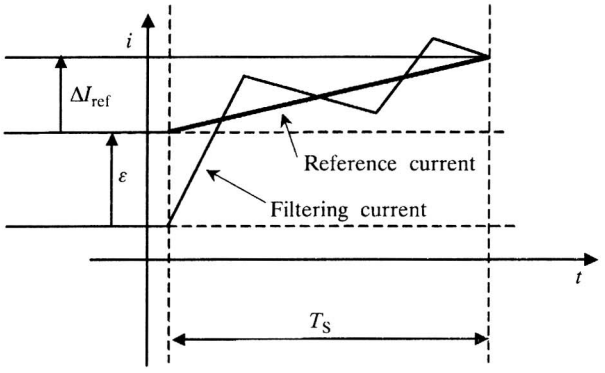

Fig. 6 Reference and filtering currents during a switching period T_S

The slope of filtering current depends on the state of the converter, the switching pattern and the voltage across coupling inductances.

In the Appendix, a full development of a design equation is carried out which allows for the computation of a proper duty cycle for each leg, thus ensuring the achievement of zero current error by the end of the sampling period.

The proposed design equation is as follows:

$$D_i = \frac{1}{2} + \frac{1}{v_{dc}}\left[v_{in} + L_F\left(s_i^{*} + \frac{\varepsilon_i}{T_S}\right)\right] \quad (3)$$

where $i = a, b, c$ is the index of the phase, D is the duty cycle, v_{dc} is the d.c. bus voltage, v_{in} is the line-to-neutral current on the i^{th} phase, L_F is the coupling inductance, s^{*} is the reference current slope, ε is the current tracking error and T_S is the sampling period. This equation can be applied in closed loop control if line voltages, filtering currents and capacitor voltages are fed back to the controller and if coupling inductance L_F and sampling period T_S are known. The duty cycle in each phase is computed by means of (3) and is supplied to a proper PWM modulator.

5 SIMULATION RESULTS

Simulations were performed to prove the effectiveness of the proposed active filter current control. In the simulated model, distorted currents were characterised by a very high harmonic content as they are due to PC power suppliers and they have a THD greater than 100 %. Moreover, an unrealistic fault current was forced to flow in the second phase of polluting load in order to determine a large load neutral current. Non-linear load was fed by sinusoidal and symmetrical mains phase voltages, 50 Hz frequency, 400 V_{rms} line-to-line voltages. Coupling inductances L_F are 5 mH. Without active filtering, this non-linear load drastically reduced the quality of mains currents as well as of phase voltages, due to line impedances. The introduction of a performance index, THD reduction, defined in the following, allows us to evaluate the effectiveness of proposed APF harmonic filtering.

$$\mathrm{THDR} = \left(1 - \frac{\mathrm{THD_S}}{\mathrm{THD_L}}\right) \quad (4)$$

where $\mathrm{THD_S}$ is THD of mains current while $\mathrm{THD_L}$ is THD of load current.

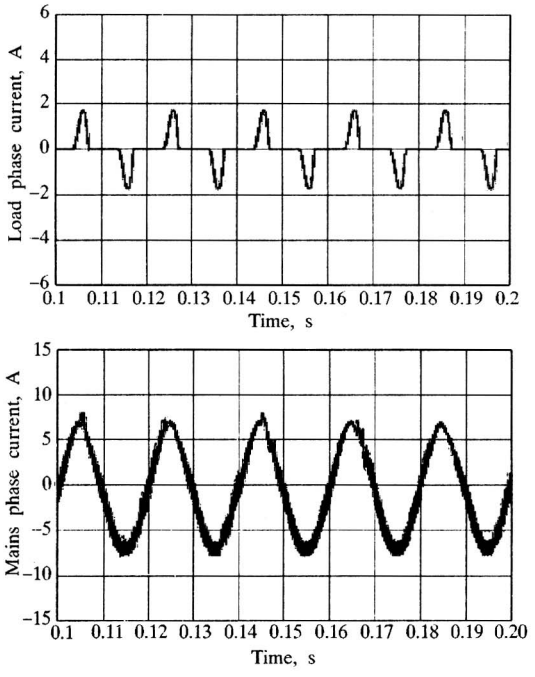

Fig. 7 Harmonic compensating action: load and mains »a« phase currents

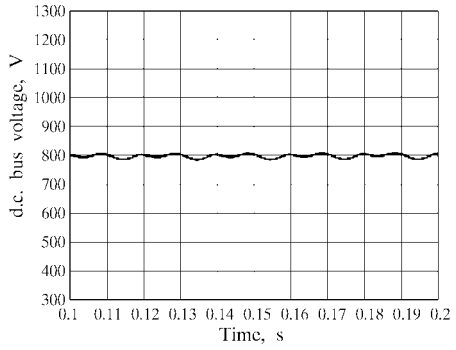

Fig. 8 Fuzzy regulation on active filter d.c. side: d.c. bus voltage

As shown in Figures 7 and 8, the proposed algorithm proved to be effective in reducing mains harmonic content as well as neutral current. It is important to point out that the polluting load was designed in order to drain a large current on phase »b« and therefore create a notable imbalance between the three phases. Reference waveform generation distributes active power among the phases, thus causing a line current on »a« and »c« phases which has a larger fundamental component compared to »a« and »c« uncompensated line currents, as shown in Figure 7. In phase »b« the opposite happens.

A switching frequency of 10 kHz gives the following results: THDR index exceeded 90 % and, above all, the peak neutral current was reduced from 15 A to less than 3 A.

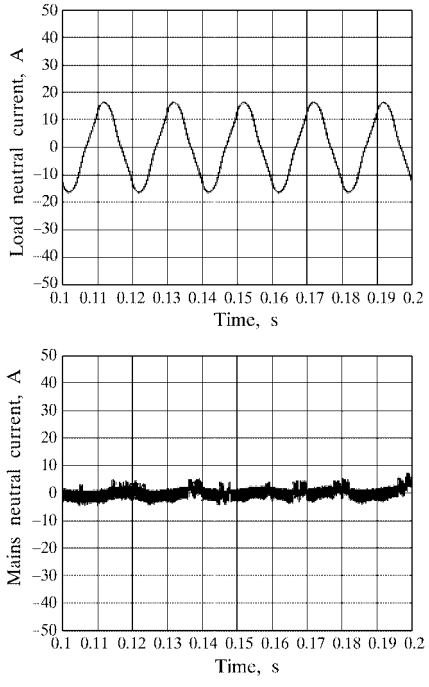

Fig. 9 Neutral current reduction: load and mains neutral currents

This compensation result was made possible by an optimum regulation of d.c. bus voltage, which maintained its reference of 800 V by means of a fuzzy controller. Figure 9 shows this result.

6 CONCLUSIONS

A shunt active filter was proposed. Its control strategy is the result of an analytical development which supplies a design equation for switching signal generation and effective current tracking. Simulations were carried out to show active filter performance under highly polluting load operation; the effectiveness of proposed filter is shown by numerical results.

7 APPENDIX

A complete development of control design equation (3) is given in this section. The analysis of current waveforms is carried out for one phase only, since the same considerations are valid in every phase.

Figure 10 shows reference and filtering currents in one phase during the switching period. In the same diagram, four time subintervals are shown, determined by the switching instants, and the changes of filtering current during each subinterval are labelled.

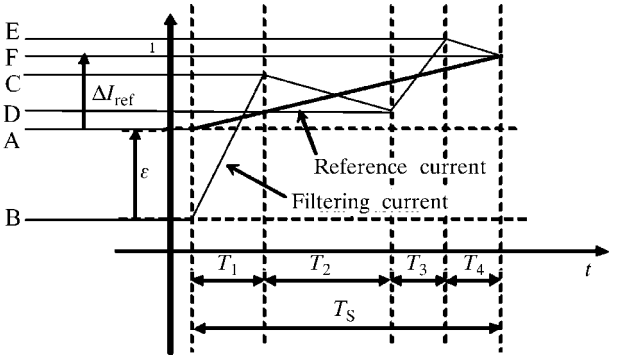

Fig. 10 Reference and filtering current during switching period T_S

In order to achieve a error by the end of the switching period, the sum of changes in filtering currents, diminished by initial tracking error ε, should be equal to reference current change.

Thus the following calculation is used:

$$AF = AB + BC + CD + DE + EF \tag{5}$$

that is:

$$s^* T_S = -\varepsilon + s_1 T_1 + s_2 T_2 + s_3 T_3 + s_4 T_4 \tag{6}$$

where s^* is the reference current derivative in T_S, (s_1, s_2, s_3, s_4) are the derivatives of compensating current in the four intervals T_1, T_2, T_3, T_4, and

$$T_1 + T_2 + T_3 + T_4 = T_S \tag{7}$$

while ε is the tracking error at the beginning of the switching period:

$$\varepsilon = i_{F\_\mathrm{ref}} - i_F. \tag{8}$$

Equation (6) is valid for all the inverter legs:

$$\begin{aligned} s_a^* T_S &= -\varepsilon_a + s_{a1}T_1 + s_{a2}T_2 + s_{a3}T_3 + s_{a4}T_4 \\ s_b^* T_S &= -\varepsilon_b + s_{b1}T_1 + s_{b2}T_2 + s_{b3}T_3 + s_{b4}T_4 \\ s_c^* T_S &= -\varepsilon_c + s_{c1}T_1 + s_{c2}T_2 + s_{c3}T_3 + s_{c4}T_4. \end{aligned} \tag{9}$$

The dependency of the intervals T_i on the values of the duty cycle D can be seen as follows. If $D_{\min}$ is the duty cycle on the inverter leg which switches first, D_{mean} is the duty cycle on the inverter leg which is the next to change and $D_{\max}$ is the larger duty cycle which is the last to change on the inverter leg, the following calculations can be made:

$$\begin{aligned} T_1 &= D_{\min} T_S \\ T_2 &= (D_{\mathrm{mean}} - D_{\min}) T_S \\ T_3 &= (D_{\max} - D_{\mathrm{mean}}) T_S \\ T_4 &= (1 - D_{\max}) T_S. \end{aligned} \tag{10}$$

By substituting (10) for (9) the result is:

$$\begin{aligned} & s_a^* + \frac{\varepsilon_a}{T_S} - s_{a4} = \\ & = D_{\min}(s_{a1} - s_{a2}) + D_{\mathrm{mean}}(s_{a2} - s_{a3}) + D_{\max}(s_{a3} - s_{a4}), \\ & s_b^* + \frac{\varepsilon_b}{T_S} - s_{b4} = \\ & = D_{\min}(s_{b1} - s_{b2}) + D_{\mathrm{mean}}(s_{b2} - s_{b3}) + D_{\max}(s_{b3} - s_{b4}), \\ & s_c^* + \frac{\varepsilon_c}{T_S} - s_{c4} = \\ & = D_{\min}(s_{c1} - s_{c2}) + D_{\mathrm{mean}}(s_{c2} - s_{c3}) + D_{\max}(s_{c3} - s_{c4}). \end{aligned} \tag{11}$$

It is possible to point out the dependence of s_i on voltage drop across coupling inductances L_{Fi}.

The following equation can be used:

$$s_i = \frac{v_{Lfi}}{L_{Fi}}. \tag{12}$$

The voltage drop across coupling inductances may be computed by following the path shown in Figure 11.

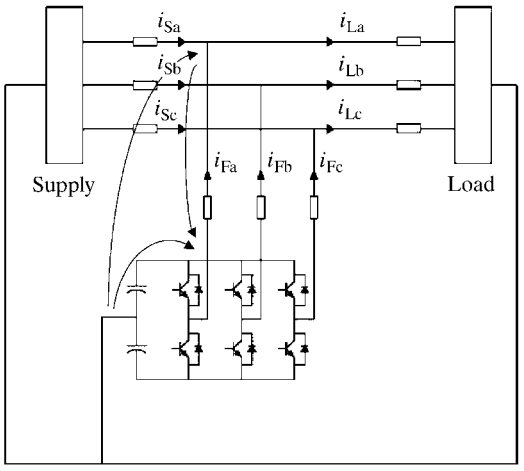

Fig. 11 Close path for inductance voltage drop computing

By following the path in Figure 11 the result is:

$$v_{LFa} + v_{an} - v_{C1} = 0 \tag{13}$$

and in the hypothesis that a complete d.c. voltage regulation is achieved:

$$v_{C1} = v_{C2} = \frac{v_{dc}}{2} \tag{14}$$

resulting in:

$$v_{LFi} = -v_{in} + g_i \frac{v_{dc}}{2} \tag{15}$$

where $i = a, b, c$, and $g_i = +1$ if upper switch is closes and $g_i = -1$ if lower switch is closed in i^{th} inverter leg.

Considering the term:

$$(s_{i1} - s_{i2}), \tag{16}$$

by substituting (12) and (15) for (16), we obtain the following results:

$$(s_{i1} - s_{i2}) = \frac{v_{dc}}{2L_F}(g_{i1} - g_{i2}) \tag{17}$$

where the first index is $i = a, b, c$ while the second one refers to the time interval T_1, T_2, T_3, T_4, where g is computed.

Generally each leg changes its status only once during the switching period. The three switching instants are different. The switching order of the three inverter legs may be: (a, b, c) or (a, c, b), (b, a, c), (b, c, a), (c, a, b), or the last case (c, b, a).

The following table may be useful in finding switching variable g values in the different cases:

Table 2. **Switching function g during T_S in the six different cases**

	Switching sequence (a, b, c)			
g_a	1	–1	–1	–1
g_b	1	1	–1	–1
g_c	1	1	1	–1
	T_1	T_2	T_3	T_4

	Switching sequence (a, c, b)			
g_a	1	–1	–1	–1
g_b	1	1	1	–1
g_c	1	1	–1	–1
	T_1	T_2	T_3	T_4

	Switching sequence (b, c, a)			
g_a	1	1	1	–1
g_b	1	–1	–1	–1
g_c	1	1	–1	–1
	T_1	T_2	T_3	T_4

	Switching sequence (b, a, c)			
g_a	1	1	–1	–1
g_b	1	–1	–1	–1
g_c	1	1	1	–1
	T_1	T_2	T_3	T_4

	Switching sequence (c, b, a)			
g_a	1	1	1	–1
g_b	1	1	–1	–1
g_c	1	–1	–1	–1
	T_1	T_2	T_3	T_4

	Switching sequence (c, a, b)			
g_a	1	1	–1	–1
g_b	1	1	1	–1
g_c	1	–1	–1	–1
	T_1	T_2	T_3	T_4

If switching sequence is (a,b,c) the following calculation are used:

$$\begin{aligned} D_{\min} &= D_a \\ D_{\text{mean}} &= D_b \\ D_{\max} &= D_c \end{aligned} \tag{18}$$

and by substituting (18) and (17) for (11) the following results are obtained:

$$\begin{aligned} s_a^* + \frac{\varepsilon_a}{T_S} - s_{a4} &= D_{\min}\frac{v_{dc}}{L_F}, \\ s_b^* + \frac{\varepsilon_b}{T_S} - s_{b4} &= D_{\text{mean}}\frac{v_{dc}}{L_F}, \\ s_c^* + \frac{\varepsilon_c}{T_S} - s_{c4} &= D_{\max}\frac{v_{dc}}{L_F}. \end{aligned} \tag{19}$$

If switching sequence is a,c,b the following calculation are used:

$$\begin{aligned} D_{\min} &= D_a \\ D_{\text{mean}} &= D_b \\ D_{\max} &= D_c \end{aligned} \tag{20}$$

Therefore it is possible to obtain the following three equations which relate D values to other electrical parameters:

$$\begin{aligned} s_a^* + \frac{\varepsilon_a}{T_S} - s_{a4} &= D_{\min}\frac{v_{dc}}{L_F}, \\ s_b^* + \frac{\varepsilon_b}{T_S} - s_{b4} &= D_{\max}\frac{v_{dc}}{L_F}, \\ s_c^* + \frac{\varepsilon_c}{T_S} - s_{c4} &= D_{\text{mean}}\frac{v_{dc}}{L_F}. \end{aligned} \tag{21}$$

It is possible to analyse the other four situations in the same way. By solving equations with respect to D, the result is a design equation which may be applied to each inverter leg:

$$D_i = \frac{1}{2} + \frac{1}{v_{dc}}\left[v_{in} + L_F\left(s_i^* + \frac{\varepsilon_i}{T_S}\right)\right]. \tag{22}$$

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Upravljanje strujom trofaznih paralelno spojenih aktivnih filtara s četiri vodiča. Opisan je aktivni filtar za kompenzaciju harmonijskog izobličenja, struje nultog sustava i jalove snage u trofaznim sustavima s četiri vodiča.

Pozornost je usmjerena na upravljanje strujom da se postigne optimalno slijeđenje struje s pomoću konstantne frekvencije pobudnog signala. Djelotvornost predloženog upravljanja ispitana je simulacijom, gdje su harmonijsko zagađenje i neravnoteža, uzrokovani jakom distorzijom tereta, drastično reducirani.

Ključne riječi: aktivni filtri, neizrazita logika, harmonici, kvaliteta snage

AUTHORS' ADDRESSES:

Antonio Dell'Aquila, Professor
Agostino Lecci, PhD student
Dipartimento di Elettrotecnica ed Elettronica
Politecnico di Bari
Via E. Orabona 4, 70125 Bari, Italy

Phone: +39-080-5963.366/433
Fax: +39-080-5963.410
dellaqui@poliba.it
lecci@ieee.org
http://dee.poliba.it

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