ISSN 0005–1144
ATKAAF 42(1–2), 53–61 (2001)

Miro Milanovic, Alenka Hren, Franc Mihalic

Input Displacement Factor Correction for Three-Phase Three-Level AC to DC PWM-based Boost Rectifier

UDK 621.314.6
IFAC IA 5.5.4;4.7.1

Original scientific paper

Pulse width modulation (PWM) strategy for a matrix structured three-phase three-level AC to DC boost rectifier is developed. Such approach has been used on purpose to control the input displacement power factor close to unity. The connection between matrix switching function and PWM requirement very well describes all restrictions that occur in the modulation algorithm. This modulation algorithm enables the input displacement factor correction without an input current sensor. The only necessary control variable is the measured displacement angle between input voltage and input current.

Key words: matrix converter, ac-dc converter, switching function, pulse width modulation, input displacement factor

1. INTRODUCTION

A switching matrix analysis in power converter circuits was first investigated in [1] and then more recently, using the generalized high frequency switching strategy, in [2]. Such analyzes offer a pleasant method for understanding the power conversion between sources and sinks through the switching converter circuit. The AC-AC conversion function has been discussed in [2] and [3], where the emphases were done in the modulation strategies and improving the range of three-phase output voltage. In [4] the authors introduced a space vector modulation strategy in the AC to AC converter. In [5] and [6] it is shown that for the hysteresis control of the input phase current and resistive fundamental mains behavior the central point potential can be controlled by an offset of the phase current reference values. This paper deals with the development of the PWM algorithm for the three-phase three-level AC to DC converter based on the switching matrix approach.

2. DESCRIPTION OF CONVERTER BY SWITCHING FUNCTIONS

In approaching a design of the switching power converter shown in Figure 1(a) for any application, two related sets of parameters are of paramount

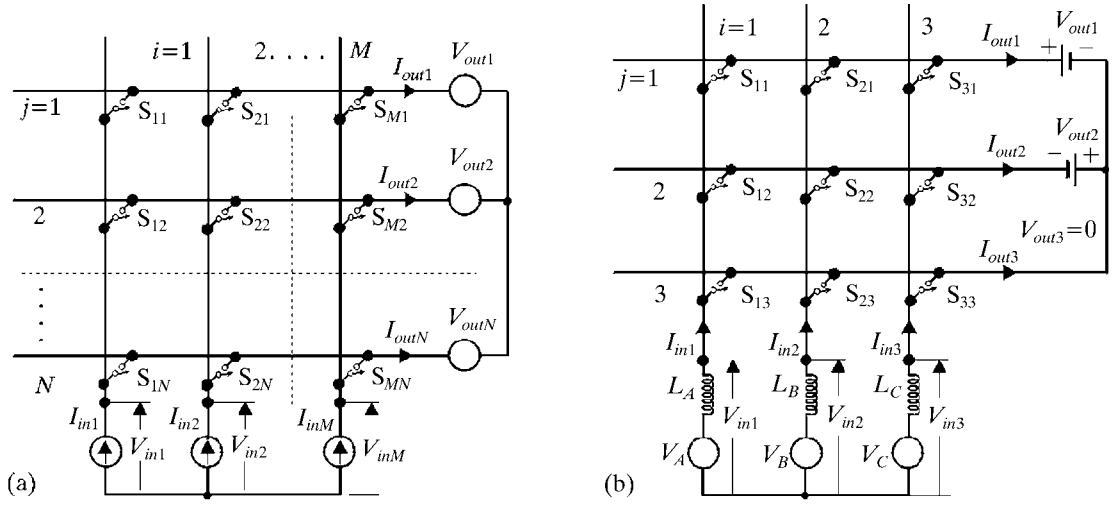

Fig. 1 (a) General switching matrix with current inputs. (b) The rectifier circuit with M = N = 3

interest. The internal currents and voltages of the converter switching loops will determine the selection of active switching device to be used and also auxiliary passive components needed to enable the devices to operate properly. The switching algorithm used to connect the M input lines with the N output lines is based on Figure 1(a). In order to obtain a precise, quantitative means for describing the converter internal structure and external terminal properties, the switching pattern is needed. This can be conveniently done by defining a function, so called a Switching function which has been defined in [1](1):

$$H_{ij} = \begin{cases} 1 & \text{for} \quad S_{ij} = \text{ON} \\ 0 & \text{for} \quad S_{ij} = \text{OFF} \end{cases}. \tag{1}$$

The circuit shown in Figure 1(a) will not operate when the voltage sources are short-connected and when the currents have no path to flow. Because of this the switching function must satisfy next condition:

$$\sum_{j=1}^{N} H_{ij} = 1, \quad i = 1 \ldots M. \tag{2}$$

The switch in the switching matrix connects the I_{in_i} current sources from the set of M input variables with V_{in_j} voltage sources from the set of the N output variables. Whenever the switch is OFF, the blocking voltage appears across it. The voltage impressed on the input line i can be written as:

$$V_{in_i} = \sum_{j=1}^{N} H_{ij} V_{out_j} = 1, \quad i = 1 \ldots M. \tag{3}$$

The voltage across the switches can be obtained as a difference between the voltage on i and line j like:

$$V_{sw_{ij}} = V_{in_i} - V_{out_j}. \tag{4}$$

Substitution of (3) into (4) gives:

$$V_{sw_{ij}} = \sum_{m=1}^{N} H_{im} V_{out_m} - V_{out_j} \quad i = 1 \ldots M, \; j = 1 \ldots N. \tag{5}$$

The next step to be defined is the current through the switches. In general the Kirchoff's current low valid for output matrix converter current could be expressed as:

$$I_{out_N} = -\sum_{j=1}^{N-1} I_{out_j}. \tag{6}$$

The input current could be represented as a linear combination of output currents as follows:

$$I_{in_{ij}} = \sum_{j=1}^{N-1} H_{ij} I_{out_j} - H_{iN} I_{out_N}, \quad i = 1 \ldots M. \tag{7}$$

Equation (6) should be substituted into (7) and finally:

$$I_{in_{ij}} = \sum_{j=1}^{N-1} H_{ij} I_{out_j} - H_{iN} \sum_{j=1}^{N-1} I_{out_j}, \quad i = 1 \ldots M. \tag{8}$$

The main aim followed in this section was to find the expression for estimating the switches currents. The current through switch can be expression by:

$$I_{sw_{ij}} = H_{ij} I_{in_i}, \quad i = 1 \ldots M, \quad j = 1 \ldots N. \tag{9}$$

It is evident that the current through the switches can be estimated only when the output current is known. From (5) and (9) the internal structure of switching matrix converter was defined.

2.1. Power converter circuits analyzed by switching Function

In previous section the general approach has been introduced and presented. The circuit shown in Figure 1(b) is appropriate for further analysis. Anyway, the next presumptions will make the analysis easier. The number of input and output lines are equal:

$$M = N = 3. \tag{10}$$

The quantitative assessment of switching converter performance and characteristics for AC to DC converter have been analyzed here are:

- The current sources (voltage sources with inductors) are presented on the input lines.
- The voltage sources/sinks (capacitors) are presented on the output lines.
- The power flow has to be bi-directional.

For output voltage definition it is necessary to presume the next requirements:

- To establish the »output voltage« (V_{in_i}, see Figure 1(b)) the three output voltage sources (V_{out_j}) are available.
- The blocking voltage on semiconductor switches has to be half of the entire output voltage.

2.1.1. Voltage properties

For three-level converter output the voltages will appear on the output capacitors. Because of DC requirements the output voltages could be defined as follows:

$$\begin{aligned} V_{out_1} &= +V_{o1} \\ V_{out_2} &= -V_{o2} \\ V_{out_3} &= 0. \end{aligned} \tag{11}$$

After defining the voltage external terminal properties, the internal properties will be further considered. The base of this analysis is given in (5) and (9). Let us define the voltages impressed on switches on the first vertical line. First, consider the switch S_{11}. After expanding (9) the blocking voltage on the switch is:

$$V_{sw_{11}} = \left(H_{11}V_{out_1} + H_{12}V_{out_2} + H_{13}V_{out_3}\right) - V_{out_1}. \quad (12)$$

The blocking voltage on the switch S_{11} has finally two values because of (2):

– When $H_{12} = 1$ and $H_{13} = 0$, the blocking voltage will be:

$$V_{sw_{11}} = V_{out_2} - V_{out_1} = -V_{o1} - V_{o2}. \quad (13)$$

– When $H_{12} = 0$ and $H_{13} = 1$, the blocking voltage will be:

$$V_{sw_{11}} = V_{out_3} - V_{out_1} = -V_{o1}. \quad (14)$$

From (13) and (14) the next conclusion could be done: When the switch S_{11} is OFF it must block the negative voltage in both case.

For the switch S_{12} the voltage property can be evaluated by:

$$V_{sw_{12}} = \left(H_{11}V_{out_1} + H_{13}V_{out_3}\right) - V_{out_2}. \quad (15)$$

The blocking voltage on the switch S_{12} has also two values because of (2):

– When $H_{11} = 1$ and $H_{13} = 0$, the blocking voltage will be:

$$V_{sw_{12}} = V_{out_1} - V_{out_2} = V_{o1} - \left(-V_{o2}\right). \quad (16)$$

– When $H_{11} = 0$ and $H_{13} = 1$, the blocking voltage will be:

$$V_{sw_{12}} = V_{out_3} - V_{out_2} = -\left(-V_{o2}\right). \quad (17)$$

From (16) and (17) the next conclusion could be done: When the switch S_{12} is OFF it must block the positive voltage in both case.

For the switch S_{13} the voltage property can be evaluated by:

$$V_{sw_{13}} = \left(H_{11}V_{out_1} + H_{12}V_{out_2}\right) - V_{out_3}. \quad (18)$$

The blocking voltage on the switch S_{13} has also two values because of (2):

– When $H_{11} = 1$ and $H_{12} = 0$, the blocking voltage will be:

$$V_{sw_{13}} = V_{out_1} - V_{out_3} = V_{o1}. \quad (19)$$

– When $H_{11} = 0$ and $H_{12} = 1$, the blocking voltage will be:

$$V_{sw_{13}} = V_{out_2} - V_{out_3} = -V_{o2}. \quad (20)$$

From (19) and (20) the next conclusion could be done: When the switch S_{13} is OFF it must block the positive and negative voltage in both case.

2.1.2. Current properties

The current can be evaluated from (8) and (9). For the switch in the first vertical line (8) could be expanded as follows:

$$I_{in_1} = H_{11}I_{out_1} + H_{12}I_{out_2} - H_{13}\left(I_{out_1} + I_{out_2}\right). \quad (21)$$

Because of (2) it follows:

$$I_{in_1} = H_{11}I_{out_1} = I_{sw_{11}}. \quad (22)$$

or

$$I_{in_1} = H_{12}I_{out_2} = I_{sw_{12}}. \quad (23)$$

or

$$I_{in_1} = H_{13}\left(I_{out_1} + I_{out_2}\right) = I_{sw_{13}}. \quad (24)$$

From (22) appears the current property of switch S_{11}. According to the DC converter output the output current into voltage source V_{out1} must have positive direction. For the voltage and current properties of the switch S_{11} can be supposed: When the switch S_{11} is OFF it should block the negative voltage, and when it is ON it should conduct the positive current. Such properties are normal for the diode.

From (23) appears the current property of switch S_{12}. According to the DC converter output the output current into voltage source V_{out2} must have negative direction. For the voltage and current properties of the switch S_{12} can be supposed: When the switch S_{12} is OFF it should block the positive voltage, and when it is ON it should conduct the negative current. Such properties are normal for the reverse connected diode.

To define the properties of the switch S_{13} the next consideration from (24) should be done: Because of condition (2) the switching function $H_{11} = H_{12} = 0$, but the current must have the way to flow. Because of this the switching function in the second vertical line must satisfy next conditions: $H_{22} = 1$ and $H_{21} = 0$ or $H_{22} = 0$ and $H_{21} = 1$ and similar for the third vertical line. From this description the next conclusion could be done: When $H_{22} = 1$ the switch S_{13} conducts the positive current which has the same direction as current I_{out2}. When the switching function $H_{21} = 1$ the switch S_{13} conducts current which has the same direction as current I_{out1}. The current trough switch S_{13} could has both directions. According to this for the voltage and

current properties of the switch S_{13} could be done: When the switch S_{13} is OFF it should block the positive and negative voltage and when it is ON it should conduct the positive and negative current. Such properties are normal for a bi-directional switch. The results of above analysis are summarized in Table 1, where voltage and current characteristics of all switches in first vertical line are defined.

Table 1. **The switching device current and voltage properties**

	S_{11}	S_{12}	S_{13}
Current is:	Positive	Negative	Both
Blocking voltage is:	Negative	Positive	Both
Switching device is:	Diode	Diode	Bi-dir. switch

Bi-directional switches S_{13}, S_{23} and S_{33} can be constructed in five different combinations of diodes and transistors. After it's substitution in the scheme in Figure 1(a) the five different structures, of the three-phase three-level boost rectifier can be established. The varieties of AC to DC converter types have been depicted in Figure 2(a), (b), (c), (d) and (e) respectively.

3. SWITCHING PATTERN

For establishing the switching pattern the switching matrix approach is very powerful tool. The power supply voltage and input currents are:

$$\begin{aligned} V_A &= \hat{V}\cos(\omega t) \\ V_B &= \hat{V}\cos\left(\omega t - \frac{2\pi}{3}\right) \\ V_C &= \hat{V}\cos\left(\omega t - \frac{4\pi}{3}\right), \end{aligned} \tag{25}$$

$$\begin{aligned} I_{in1} &= \hat{I}\cos(\omega t + \varphi) \\ I_{in2} &= \hat{I}\cos\left(\omega t - \frac{2\pi}{3} + \varphi\right) \\ I_{in3} &= \hat{I}\cos\left(\omega t - \frac{4\pi}{3} + \varphi\right). \end{aligned} \tag{26}$$

From Figure 1(b) it can be seen that the switching matrix input voltages V_{in_i} can be formed as a combination of output voltages V_{out_j}, as follows:

$$\begin{aligned} V_{in_1} &= H_{11}V_{out_1} + H_{12}V_{out_2} + H_{13}V_{out_3} \\ V_{in_2} &= H_{21}V_{out_1} + H_{22}V_{out_2} + H_{33}V_{out_3} \\ V_{in_3} &= H_{31}V_{out_1} + H_{32}V_{out_2} + H_{33}V_{out_3}. \end{aligned} \tag{27}$$

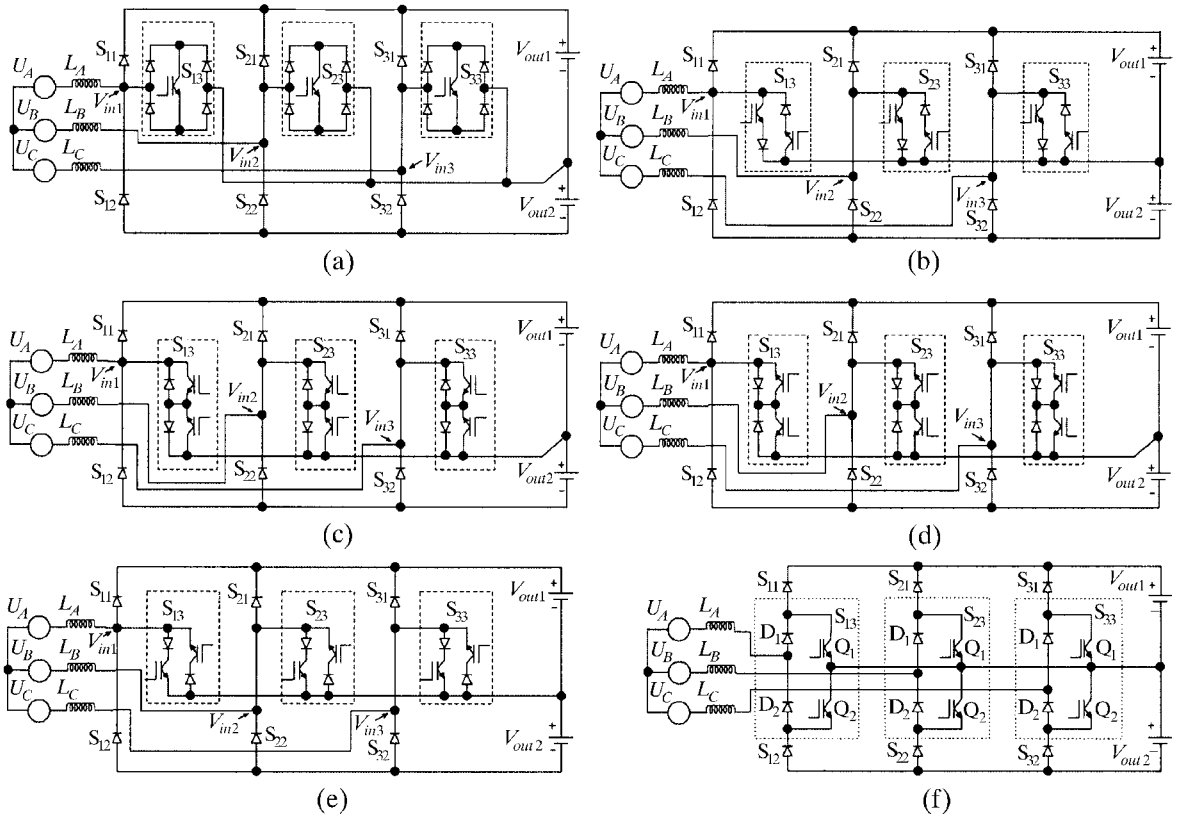

Fig. 2 Six circuit topologies

On the other hand the voltages V_{in_i} can be constructed when the output voltages are connected by the switching matrix with the terminals u, v and w (Figure 2(f)) during the time intervals t_1, t_2 and t_3. The input voltages can be defined as:

$$\begin{aligned} V_{in_1} &= \frac{1}{T_S}\left(t_1 V_{out_1} + t_2 V_{out_2} + t_3 V_{out_3}\right) \\ V_{in_2} &= \frac{1}{T_S}\left(t_1 V_{out_2} + t_2 V_{out_3} + t_3 V_{out_1}\right) \\ V_{in_3} &= \frac{1}{T_S}\left(t_1 V_{out_3} + t_2 V_{out_1} + t_3 V_{out_2}\right) \end{aligned} \tag{28}$$

where V_{out1}, V_{out2} and V_{out3} are the output voltages defined in (11) and $T_S = t_1 + t_2 + t_3$. In (28) it is assumed that the voltage on terminals u, v and w is, in effect, the average value of the three switching events weighted by the time of »dwell« on each of the voltages connected to the output of the rectifier. Because of the input current wave-shape requirement the inductance voltage drop must have the sinusoidal wave-shape as well. Based on this the input voltages first harmonics V_{in_i} must have sinusoidal wave-shape and can be expressed by:

$$\begin{aligned} V_{in_1} &= \hat{V}_{in}\cos(\omega t + \beta) \\ V_{in_2} &= \hat{V}_{in}\cos\left(\omega t - \frac{2\pi}{3} + \beta\right) \\ V_{in_3} &= \hat{V}_{in}\cos\left(\omega t - \frac{2\pi}{3} + \beta\right) \end{aligned} \tag{29}$$

where β is the phase shift between V_{in1} and V_A. From (26) and (28) it follows:

$$\frac{t_1}{T_S} = H_{11} = H_{22} = H_{33} \tag{30}$$

$$\frac{t_2}{T_S} = H_{12} = H_{23} = H_{31} \tag{31}$$

$$\frac{t_3}{T_S} = H_{13} = H_{21} = H_{32}\,. \tag{32}$$

With appropriate β the current through the inductance L_A, L_B and L_C will have no phase shift versus $V_{A,B,C}$. Therefore the switching pattern algorithm must be sensitive on β in order to get the rectifier unity power factor operation. In (30) the switching function H_{33} represents the state of the bi-directional switch S_{33} in the third vertical line of the rectifier (Figure 1(b)). This switch is controllable. Other two switches S_{11} and S_{22} are diodes and they are turned on or off depending on the direction of the current through the switch S_{33}. The same conclusion is follows from (8) and (9). There are two other controllable switches S_{23} and S_{13} as well. From (2) follow the conditions when the diodes switching function H_{I1} and H_{I2} will be unity. They can be expressed:

$$\begin{aligned} H_{11} + H_{12} &= 1 - H_{13} \\ H_{21} + H_{22} &= 1 - H_{23} \\ H_{31} + H_{32} &= 1 - H_{33}\,. \end{aligned} \tag{33}$$

From (33) follows that the diodes switches S_{11} and S_{12} in the first vertical line could be active when the bi-directional switch S_{13} is non-active ($H_{13} = 0$). In this case the new active switch in this vertical line will be defined by the input current direction as:

$$\begin{aligned} H_{13} &= 0 \\ H_{11} &= 1 \Rightarrow I_{in1} > 0 \\ H_{12} &= 1 \Rightarrow I_{in1} < 0\,. \end{aligned} \tag{34}$$

Let us define the function whose will describe the sign of the input current:

$$H_{in_k} = \begin{cases} 1 \text{ for } I_{in_k} \geq 0 \\ 0 \text{ for } I_{in_k} < 0 \end{cases} \tag{35}$$

where $k = 1...3$. From (33), (34) and (35) it follows:

$$\begin{aligned} H_{i1} &= (1 - H_{i3}) \cdot H_{in_i} \\ H_{i1} &= (1 - H_{i3}) \cdot \left(1 - H_{in_i}\right) \end{aligned} \tag{36}$$

where $i = 1...3$. Substituting (36) into (27) yields:

$$\begin{aligned} V_{in_1} &= H_{in1}(1 - H_{13}) \cdot V_{o1} + \\ &\quad + (1 - H_{in1})(1 - H_{13}) \cdot V_{o2} + H_{13} V_{o3} \\ V_{in_2} &= H_{in2}(1 - H_{23}) \cdot V_{o1} + \\ &\quad + (1 - H_{in2})(1 - H_{23}) \cdot V_{o2} + H_{23} V_{o3} \\ V_{in_3} &= H_{in3}(1 - H_{33}) \cdot V_{o1} + \\ &\quad + (1 - H_{in3})(1 - H_{33}) \cdot V_{o2} + H_{33} V_{o3} \end{aligned} \tag{37}$$

and comparing with (37) with (27) for t_1/T_s, t_2/T_s and t_3/T_s yields:

$$\frac{t_1}{T_s} = H_{33} = 1 - \frac{q\cos\left(\omega_i t + \frac{2\pi}{3} + \beta\right)}{2H_{in3} - 1} \tag{38}$$

$$\frac{t_2}{T_s} = H_{23} = 1 - \frac{q\cos\left(\omega_i t - \frac{2\pi}{3} + \beta\right)}{2H_{in3} - 1} \tag{39}$$

$$\frac{t_3}{T_s} = H_{13} = 1 - \frac{q\cos(\omega_i t + \beta)}{2H_{in3} - 1} \tag{40}$$

where $q = \hat{V}_{in} / \hat{V}_{o1}$. From (29), it is evident that the switching function sum in vertical lines is always a unity (Figure 1(a)).

4. VOLTAGE VECTORS

To define the available voltage vectors the scheme in Figure 2(f) is appropriate to define the states of the switches on the next way. For one of the vertical line (vertical legs of the converter) states of the switches are:

$$1 = \begin{cases} Q_{A1} = 0 \\ Q_{A2} = 1 \quad \text{for} \quad I_{in1} > 0 \end{cases} \tag{41}$$

$$-1 = \begin{cases} Q_{B1} = 1 \\ Q_{B2} = 0 \quad \text{for} \quad I_{in1} < 0 \end{cases} \tag{42}$$

$$0 = \begin{cases} Q_{C1} = 0 \\ Q_{C2} = 0. \end{cases} \tag{43}$$

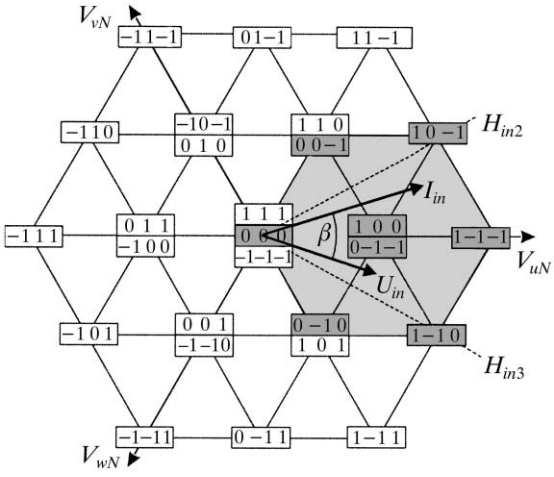

Fig. 3 The voltage vectors hexagon

Table 2. **The voltage vectors**

V_i	Q_{A1}, Q_{A2}	Q_{B1}, Q_{B2}	Q_{C1}, Q_{C2}	U_{uv}	U_{vw}	U_{wu}	U_{uN}	U_{vN}	U_{wN}
V_0	0	0	0	0	0	0	0	0	0
V_1	0	0	1	0	$-V_D/2$	$V_D/2$	0	0	$V_D/2$
V_2	0	0	–1	0	$V_D/2$	$-V_D/2$	0	0	$-V_D/2$
V_3	0	1	0	$-V_D/2$	$V_D/2$	0	0	$V_D/2$	0
V_4	0	1	1	$-V_D/2$	0	$V_D/2$	0	$V_D/2$	$V_D/2$
V_5	0	1	–1	$-V_D/2$	V_D	$-V_D/2$	0	$V_D/2$	$-V_D/2$
V_6	0	–1	0	$V_D/2$	$-V_D/2$	0	0	$-V_D/2$	0
V_7	0	–1	1	$V_D/2$	V_D	$V_D/2$	0	$-V_D/2$	$V_D/2$
V_8	0	–1	–1	$V_D/2$	0	$-V_D/2$	0	$-V_D/2$	$-V_D/2$
V_9	1	0	0	$V_D/2$	0	$-V_D/2$	$V_D/2$	0	0
V_{10}	1	0	1	$V_D/2$	$-V_D/2$	0	$V_D/2$	0	$V_D/2$
V_{11}	1	0	–1	$V_D/2$	$V_D/2$	$-V_D$	$V_D/2$	0	$-V_D/2$
V_{12}	1	1	0	0	$V_D/2$	$-V_D/2$	$V_D/2$	$V_D/2$	0
V_{13}	1	1	1	0	0	0	$V_D/2$	$V_D/2$	$V_D/2$
V_{14}	1	1	–1	0	V_D	$-V_D$	$V_D/2$	$V_D/2$	$-V_D/2$
V_{15}	1	–1	0	V_D	$-V_D/2$	$-V_D/2$	$V_D/2$	$-V_D/2$	0
V_{16}	1	–1	1	V_D	$-V_D$	0	$V_D/2$	$-V_D/2$	$V_D/2$
V_{17}	1	–1	–1	V_D	0	$-V_D$	$V_D/2$	$-V_D/2$	$-V_D/2$
V_{18}	–1	0	0	$-V_D/2$	0	$V_D/2$	$-V_D/2$	0	0
V_{19}	–1	0	1	$-V_D/2$	$-V_D/2$	V_D	$-V_D/2$	0	$V_D/2$
V_{20}	–1	0	–1	$-V_D/2$	$V_D/2$	0	$-V_D/2$	0	$-V_D/2$
V_{21}	–1	1	0	V_D	$V_D/2$	$V_D/2$	$-V_D/2$	$V_D/2$	0
V_{22}	–1	1	1	$-V_D$	0	V_D	$-V_D/2$	$V_D/2$	$V_D/2$
V_{23}	–1	1	–1	$-V_D$	V_D	0	$-V_D/2$	$V_D/2$	$-V_D/2$
V_{24}	–1	–1	0	0	$-V_D/2$	$V_D/2$	$-V_D/2$	$-V_D/2$	0
V_{25}	–1	–1	1	0	$-V_D$	V_D	$-V_D/2$	$-V_D/2$	$V_D/2$
V_{26}	–1	–1	–1	0	0	0	$-V_D/2$	$-V_D/2$	$-V_D/2$

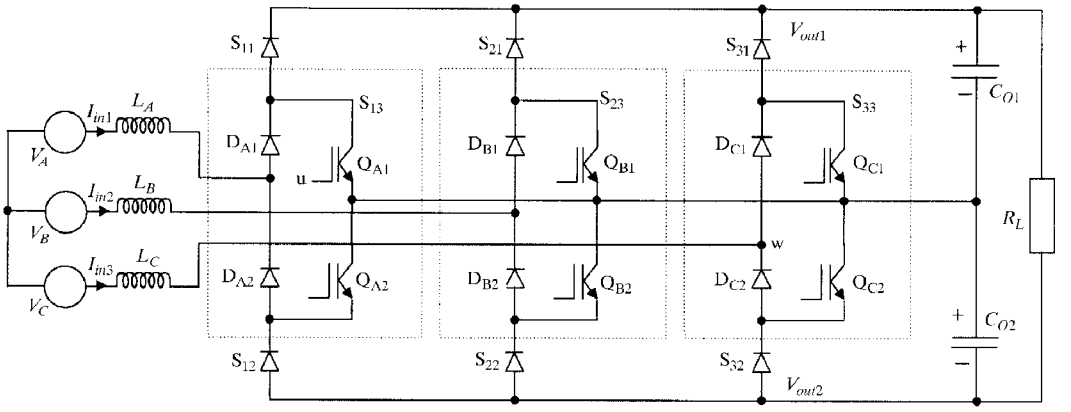

Fig. 4 The experimental circuit

As can be seen there are 27 states or there are 27 available voltage vectors. This voltage vectors are summarized in Table 2. The voltage vectors which will be established between the converter terminals u, v and w can be expressed with next formula:

$$V_k = \frac{2}{3}\left(V_{uN} + V_{vN}e^{-\frac{2\pi}{3}} + V_{wN}e^{\frac{2\pi}{3}}\right) \qquad (44)$$

where $k = 1, 2...27$. When we apply the values from Table 2 in (44) the voltage vectors are defined:

$$V_1 = \frac{2}{3}\left(0 + 0\cdot e^{-\frac{2\pi}{3}} + 0\cdot e^{\frac{2\pi}{3}}\right)$$

$$V_{15} = \frac{2}{3}\left(\frac{V_D}{2} + \frac{V_D}{2}\cdot e^{-\frac{2\pi}{3}} - \frac{V_D}{2}\cdot e^{\frac{2\pi}{3}}\right) \qquad (45)$$

$$V_{26} = \frac{2}{3}\left(-\frac{V_D}{2} - \frac{V_D}{2}\cdot e^{-\frac{2\pi}{3}} - \frac{V_D}{2}\cdot e^{\frac{2\pi}{3}}\right).$$

From the voltage vector hexagon in Figure 3 follows that a few of different switching combination give the same switching vector. For example, the vectors V_8 and V_9 define the same voltage vector. For vectors choosing there are two main constraints:

1. The vectors which define the same inner hexagon point charge the different capacitor. It can be summarized that with the using of the both switching states the balance of the output voltages can be reached.
2. Regarding the position of the current vectors I_{in} it is not possible to reach all of available vectors. For example, from vectors which describe the hexagon origin only the vector V_1 can be reached because the vectors V_{13} and V_{26} require that all input currents I_{ini} should have the same sign. In the case that the vectors V_{in} and I_{in} have the position as is shown in Figure 3, vector V_{in} can be established from the vectors which are placed in the $-V_{vN}$ and V_{uN} direction. Because I_{in3} has negative sign the voltage vector V_{11} can not be realized. Vector V_{in} can be established only from the voltage vectors which limited the local shaded hexagon (Figure 3). When current vector pass the line H_{in2} the next hexagon should be used.

5. EXPERIMENTAL RESULTS

In Figure 4 the experimental circuit is shown. The measurement has been done with converter where the input inductances have values: $L_A = L_B = L_C = 5$ mH, the output capacitances have values $C_{O1} = C_{O2} = 100$ μF.

Based on the above description the pulse width modulation algorithm has been implemented on the micro-controller unit. The Hitachi SH7032 micro-controller has been used. By using solutions from (38), (39) and (40) the input phase angle φ in (26), can be adjust by computing appropriate β in (29). The input values of the PWM algorithm are the desired output voltage V_{o1} and input angle β which can be provided to the PWM algorithm on different ways. In this experiment the control of the input phase angle φ has been used as shown in Figure 5.

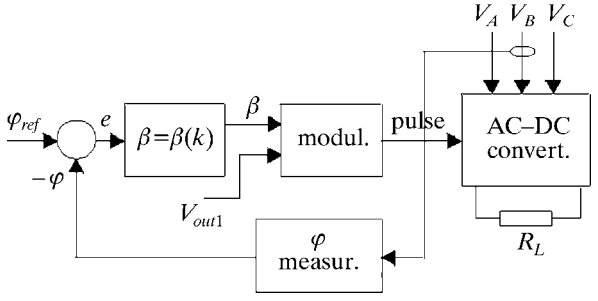

Fig. 5 The input phase angle control scheme

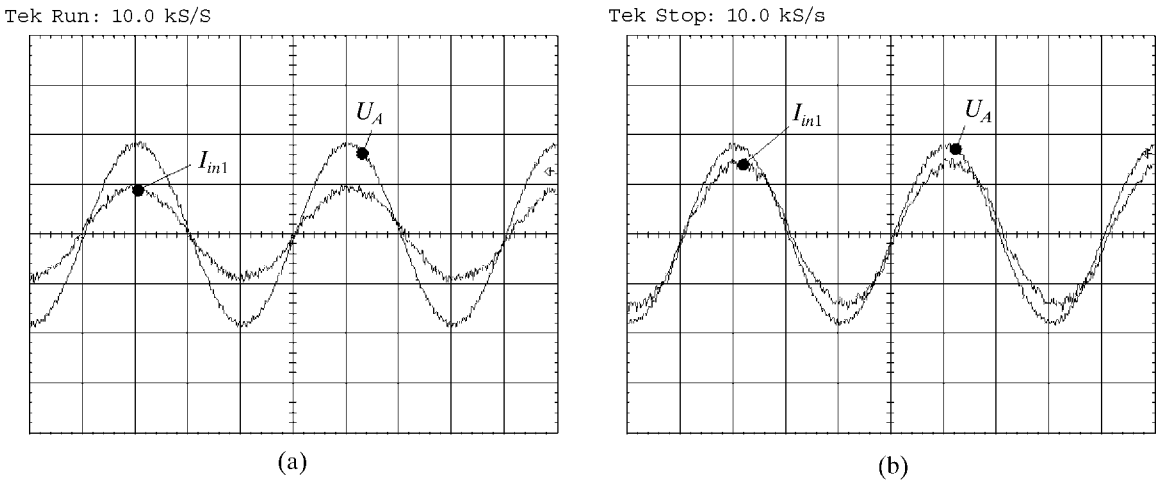

Fig. 6 The input voltage V_A and input current I_{in1}, y-axis 100 V/div, x-axis 1 A/div (The laboratory voltage source has been used.) (a) Resistance load 100 Ω, (b) Resistance load 66 Ω.

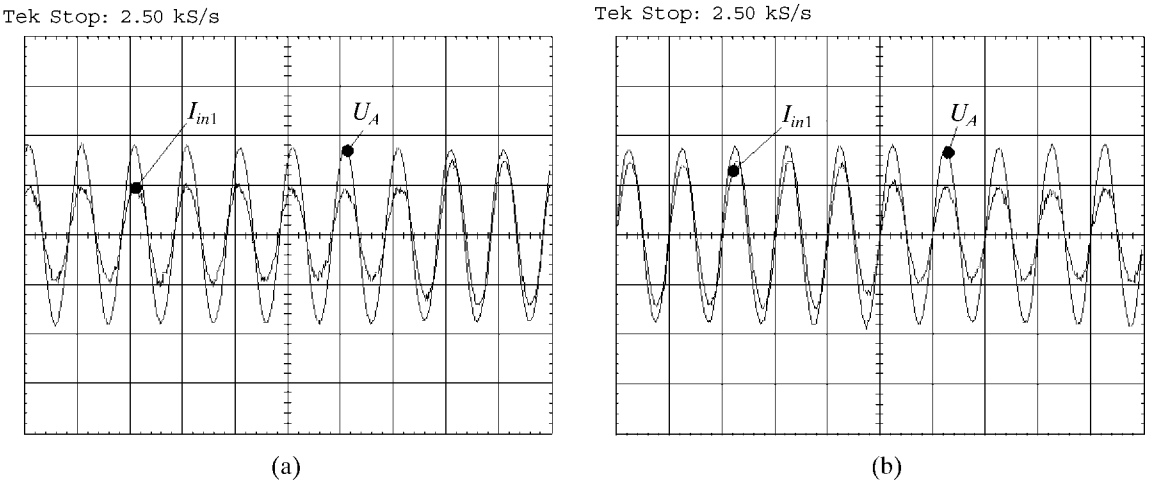

Fig. 7 The input voltage V_A and input current I_{in1}, y-axis 100 V/div, x-axis 1 A/div (The laboratory voltage source has been used.) (a) Resistance load changes from 100 Ω to 66 Ω, (b) Resistance load changes from 66 Ω to 100 Ω.

In Figures 6(a) and (b) an operation of rectifier in different operating points is shown. Figures 7(a) and (b) show the unity power factor operation of the converter by step load change when RL has been changed from 100 Ω to 60 Ω and vice versa.

6. CONCLUSION

Based on the switching matrix converter theory, the topologies of a three-phase three-level AC to DC converter (rectifier) have been developed. This analytical approach enables that from the external terminal requirements it is possible to define the converter internal structure. The switching matrix approach enable the best overview into the modulations algorithm. By switching matrix approach the appropriate switching sequences have been chosen. It has been also shown that the rectifier unity input displacement factor operation can be achieved with the control of the input displacement angle φ, without measurement of the input current.

REFERENCES

[1] P. Wood, **Switching Power Converters.** New York: Van Nostrand, 1981.

[2] A. Alesina, M. G. B. Venturini, **Solid-state Power Conversion: a Fourier Analysis Approach to Generalised Transformer Synthesis.** IEEE Transactions on Circuits and Systems, vol. CAS-28, pp. 319–330, April 1981.

[3] A. Alesina, M. G. B. Venturini, **Analysis and Design of Optimum-Amplitudenine-Switch Direct ac/ac Converter.** IEEE Transactions on Power Electronics, vol. 4, No. 1, pp. 101–112, January 1989.

[4] L. Huber, D. Borojevic, **Switching Frequency Optimal PWM Control of a Three-Level Inverter.** Proceedings of the 3rd European Conference on Power Electronics and Applications, Aachen, vol. III, pp. 1267–1272, October 1989.

[5] J. W. Kolar, U. Drofenik, F. C. Zach, **DC Link Voltage Balancing of a Three-Phase/Switch/Level PWM (Vienna) Rectifier by Modified Hysteresis Input Current Control,** Proceedings PCIM'95, vol. II, Nurnberg – Germany, June 1995.

[6] Y. Zhao, Y. Li, T. A. Lipo, **Forced Commutated Three-Level Boost Type Rectifier.** Conference Record of the 28th IEEE IAS Annual meeting, Toronto, pp. 771–777, October 1993.

[7] M. Milanovic, B. Sedmak, F. Mihalic, A. Hren, **PWM Algorithm for Three-Phase Three Level AC to DC Boost Converter.** Conference Record of the IEEE ISIE'99 Annual meeting, Bled–Slovenia, pp. 21–28, July 1999.

Korekcija faktora faznog pomaka trofaznog trorazinskog uzlaznog ispravljača zasnovanog na PWM-u. U radu je razvijen PWM algoritam za upravljanje matrično-strukturiranim trofaznim trorazinskim ispravljačem. Takav način upravljanja uzet je radi mogućnosti korekcije faktora pomaka ($\cos\varphi$) na jediničnu vrijednost. Veza između prekidačkih funkcija i zahtjeva na impulsno-širinski modulator jasno opisuje sva ograničenja modulacijskog algoritma. Razvijeni modulacijski algoritam omogućuje korekciju faktora pomaka bez mjerenja ulazne struje pretvarača. Za potrebe te korekcije dovoljno je samo mjerenje faznog kuta između napona i struje na ulazu ispravljača.

Ključne riječi: matrični pretvarač, ispravljač, prekidačka funkcija, impulsno-širinska modulacija, faktor pomaka – $\cos\varphi$

AUTHORS' ADDRESSES:

Miro Milanovic
Alenka Hren
Franc Mihalic
University of Maribor
Faculty of Electrical Engineering and Computer Science
Smetanova 17, SI-2000 Maribor, Slovenia
milanovic@uni-mb.si

Received: 2001–10–05