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Mobile Phone Power Amplifier Linearity and Efficiency Enhancement Using Digital Predistortion

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Abstract — The new generation mobile communication systems using spectrum efficient linear modulation schemes (QPSK, 8PSK, QAM) need linear power amplifiers in the transmission path to have good ACPR and EVM values. Linearization methods can be used to increase the linearity of the power amplifiers (PA). However, it is not reasonable to use complicated, power consuming and high cost systems. This paper presents a digital predistortion implementation for WCDMA signals using an FPGA (Field Programmable Gate Array) as DSP and investigates the application of this system in handsets. The method applied requires minimum change in the conventional transmitter path configuration but considerable PAE improvement can be achieved.

I. Introduction

The power amplifier (PA) is one of the most power consuming components in a mobile communication system. If the system linearity requirements are stringent, then the power efficiency is worse because the PA must be operated with more back-off. PA linearization can be applied to improve the linearity, decrease the required amount of back-off and hence increase the efficiency. Digital predistortion (DP) is an accurate and robust linearization method and can be applied in the new generation mobile handsets as seen in Fig.1. Components which need to be adjusted will be discussed. No feedback path is used in contrast to implementations typical for base station PAs, in order to make it compatible with available handset configurations.

The additional efforts for the processor benefit in long term from a fast and continuous improvement in the digital integrated circuit technology as its performance benefits from device scaling. The power consumption decreases and the clock frequencies increase. In future more and more tasks will be done in digital domain, because the digital ICs are more reliable and flexible compared to the analog ones. Therefore the DP is a promising linearization technique. It can also be easily implemented together with a DC-DC converter to achieve higher efficiencies [1].

II. Digital Predistortion

Digital predistortion is implemented in digital baseband as shown in Fig.1. It is composed of the address calculation, the look up table (LUT) and the complex multiplier. Each sample of the complex baseband signal is modified according to a LUT containing the inverse of the PA characteristics [2,3]. For this purpose AM-AM and AM-PM nonlinearities of the PA are characterized first. Using this information a LUT composed of two data arrays (real and imaginary or magnitude and phase) containing the complex predistortion coefficients is generated. The predistorter transfer characteristics changes the incoming signal in such a way that the cascade connection of the predistorter and the PA gives a linear output signal. Each input signal sample in the digital domain is multiplied with a complex coefficient from LUT according to an addressing function using again the input signal sample. Since the coefficients are complex, it is possible to correct not only AM-AM but also AM-PM distortion of the PA. The AM-AM and AM-PM distortion of the PA depend on the input signal power [3] but not on the phase, so the magnitude or the power of the input can be used for the LUT addressing. Calculating the square of a complex signal is easier and faster than calculating the magnitude of it. Therefore the square of the complex baseband signal, which is proportional to its power, has been used in the simulation and measurements.

The signal predistortion is done in the DSP which results in an additional computational load and power consumption but it is less than the gained power in the investigated system solution. The proposed system requires that some of its components might be adjusted which is discussed in the following: The first component is the D/A converter. As can be seen from Fig.2a the predistorted signal can have a higher peak value (about 3dB) than the original signal. Since the average stays almost constant, the peak to average ratio will be accordingly higher. The predistorted signal has also a wider frequency band as can be seen in Fig.2b. The signal to the quantization noise power ratio of a sine wave in an ideal converter is [4],

$$S/N = n \times 6.02 + 1.76\ dB \qquad (1)$$

where n can be defined as the effective number of bits and 1.76 dB offset is due to peak to RMS value of the sine wave. This offset changes with modulation type. The effective number of bits of the D/A converter in the proposed system depends on the increase in the peak to average value of the signal after predistortion, and this increase depends on the maximum value of the real and imaginary LUT coefficients. If the maximum coefficient value is 2,4,8,…, then the increase in the signal peak to average ratio is appr. 3,6,9,…dB and the effective number of bits is n-1,n-2,n-3,… accordingly. If the

predistortion is applied and the number of bits of the D/A is held constant, then the effective number of bits will decrease and S/N will decrease w.r.t. the signal without predistortion. Equation (1) gives the signal to noise power ratio, which means that there is 6.02 dB less dynamic range (S/N) for each less effective bit. In the measurements presented here the actual number of bits is 12 and the effective one is 11 because the maximum LUT coefficient value is 2.

The second component to be discussed is the reconstruction filter. The predistorted signal must reach the PA without significant distortion. The simulations showed that, if the cut-off frequency of the filters is kept low, than the linearizer performance degrades significantly. The bandwidth of the available reconstruction filters must be increased in order to let the predistorted signal pass through but a sufficient image suppression needs to be obtained at the same time. These new filter requirements can be fulfilled in two different ways [5]; by either increasing the system oversampling ratio and using a low order filter, or by leaving the oversampling ratio as previous and using a higher order filter.

Moreover, the complete analog baseband circuit, the modulator and the preamplifier (VGA shown in Fig. 1) must be able to handle the new signal having a higher peak to average ratio. For an acceptable linearization, the distortion added in these building blocks must be acceptable, which is investigated in the next chapter.

III. Simulations And Measurements

Fig.3 shows the experimental implementation of the DP system. An FPGA from Xilinx is used for the digital processing of the I and Q signals. The LUT size is 256 and the word length of the digital signals is 10-bit. I and Q signals are sent to 12 bit D/A converters after predistortion. Compared to Fig.1 an SMIQ signal generator from Rohde&Schwarz is used instead of the quadrature modulator and VGA to develop a principal understanding of the system characteristics. The amplifier used is a TDMA PA operating at 850 MHz. The input signal is a WCDMA like signal with 3.84 MHz BW and peak to average ratio of 4.7 dB. Fig.4 shows the comparison of the first and the second adjacent channel power ratios with and without DP. There is considerable linearity improvement in the first channel but slight degradation in the second one. The amplifier gives about 2 dB more linear output power with the same DC supply voltage if the DP is implemented. If we assume –40 dBc ACPR for the first and –50 dBc for the second channel as the linearity condition, then DP is not required below 24.5 dBm output power as it can be seen from Fig.4. It is therefore suggested to use DP only if higher linear output power is required. The additional power consumption in digital circuitry has been estimated to be less than 100 mW. For a mobile phone using WCDMA the probability of transmitting these maximum output powers is low (in the order of 0.5-1 %). This means the DSP will be used for DP infrequently and hence the average digital power consumption is low. On the one hand we loose power in digital circuitry but on the other hand an amplifier having 2 dB less linear output power can be used which is more efficient. Fig.5 shows the estimated efficiency enhancement with a linearized PA. Solid lines are the measured output power and efficiency curves of the amplifier which delivers 26.5 dBm output power fulfilling the linearity condition (-40 dBc for the first and -50 dBc for the second ACPR) with DP and dashed lines are the output power and efficiency curves of an estimated amplifier delivering 26.5 dBm output power fulfilling the linearity condition without DP. Thus the amplifiers with and without DP are assumed to show similar power and linearity performance for the specified linearity condition. Comparison shows that there is an efficiency improvement from 32% to 39% at maximum linear output power of 26,5 dBm and from 2.4% to 3% at 10 dBm if the DP is used. The improvement at 26.5 dBm results in a power saving of 250 mW, which compensates more than the power consumption of the digital processor. Due to the smaller power stage usable in combination with the DP-concept considerably higher efficiencies can be obtained over typically used lower output power ranges. This is a very useful improvement for WCDMA systems, which have a big output power dynamic range [1]. For example in UMTS output powers from -50dBm to +27dBm are required, which depend on the position of the mobile station w.r.t. the base station and the number of users in the channel etc. The estimated probability function of the UMTS mobile station transmit power level is as shown in Fig.6. Therefore it is very important to improve the efficiency not only for high output powers but also for all other output powers, especially at power levels, which have high probabilities of occurrence (-10 to 22 dBm). Fig.6 shows also the improvement in the efficiency at different output powers. The average efficiency regarding the output power probability function with and without DP has been calculated and an increase from 6.23% to 7.6% has been observed, which means an improvement of more than 20%.

The performance of DP with changing DC supply voltage has also been measured. The DC voltage has been changed by +/-100mV from the nominal value. The performance of the DP is still good within these limits. The measured first and second ACPRs are close to the values in nominal case with a maximum degradation of 2dB as shown in Fig.7, so that the method is not much sensitive to the changes in supply voltage.

In the DP measurements the performance degradation due to the nonlinearities in the modulator and the preamplifier has not been considered (they have been assumed to be linear). Some simulations have been done to investigate the effects of these components on the predistortion. First a behavioral saturation model for these stages has been designed using some measurement data of the UMTS direct transceiver from Infineon Technologies. This model has been used for a system simulation with an input signal composed of the control channel and one data channel (DPCCH+DPDCH) having

a peak to average ratio of 3.7dB. It has been observed that the maximum ACPR degradation due to the nonlinearities in the modulator and the preamplifier at the PA output are 0.3 dB for the first and 0.9 dB for the second adjacent channels. This is an acceptable degradation. Therefore these components can be used without any change in their specifications.

IV. Conclusions

A digital predistortion system has been implemented, which is very simple and can be used in mobile phones with adjustment of the available components in the system. The improvement in the ACPR at the PA output has been verified. The implementation requires a low effort. It has been shown that the total system efficiency can be improved by 20% if the digital predistortion is used. The system is not much sensitive to the changes in DC supply voltage, which is very important for the proposed open-loop system. The saturation effects of the modulator and preamplifier have been simulated and observed that the amount of the degradation is acceptable, which makes it possible to use these stages without any change.

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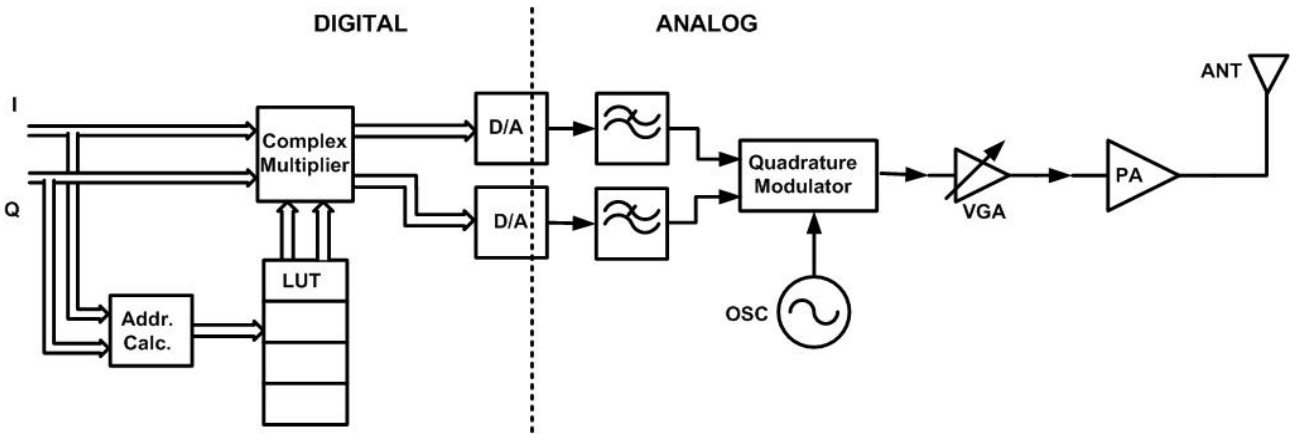

Fig. 1. The block diagram of digital predistortion.

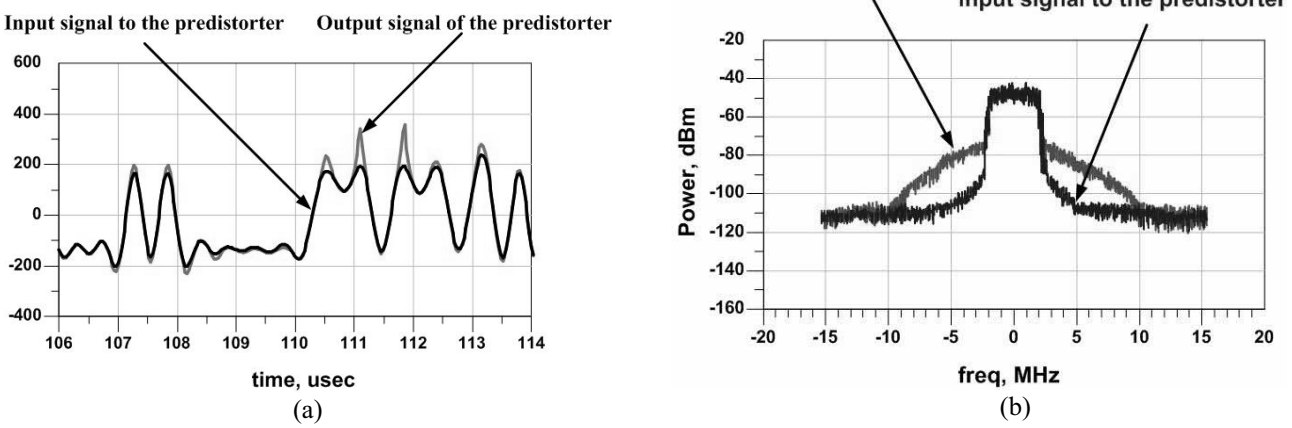

Fig. 2. (a) Time and (b) frequency domain input and output signals of the predistorter.

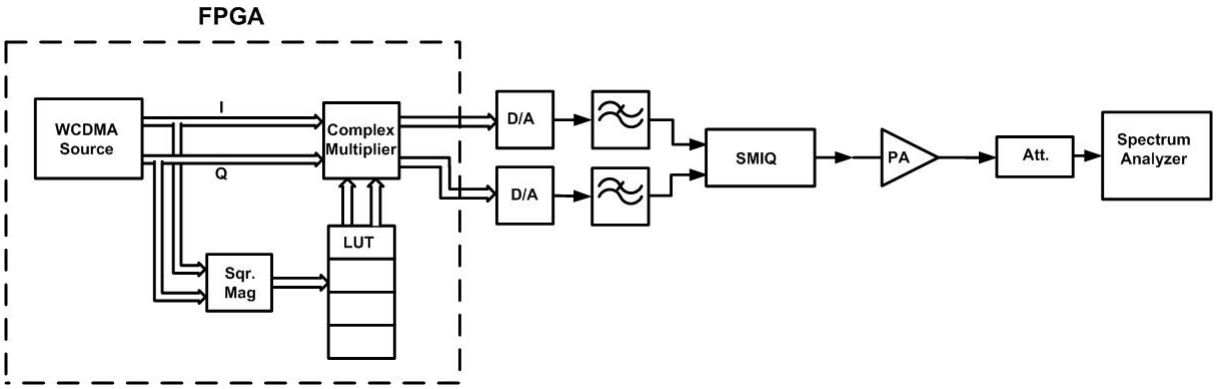

Fig. 3. Measurement setup.

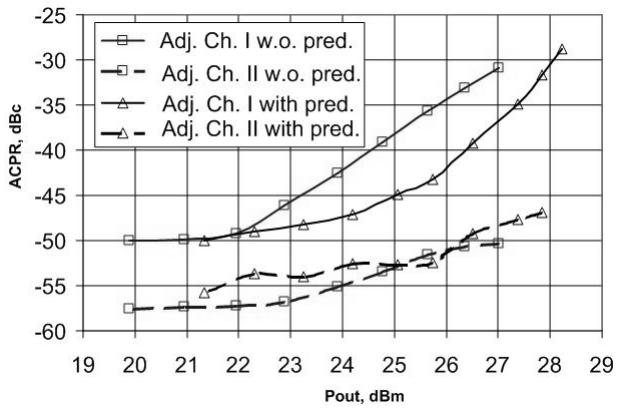

Fig. 4. ACPR measurements with and without DP.

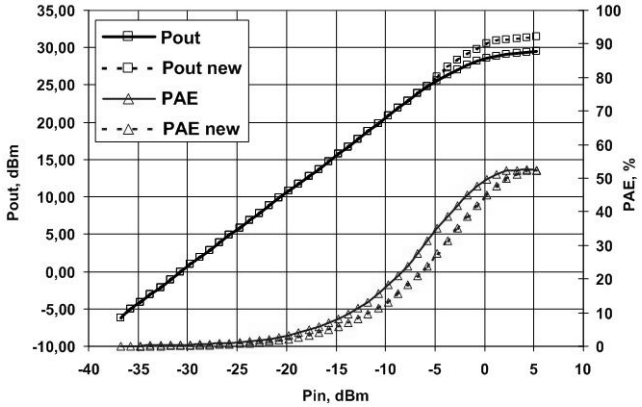

Fig .5. Output power and efficiency vs. input power curves.

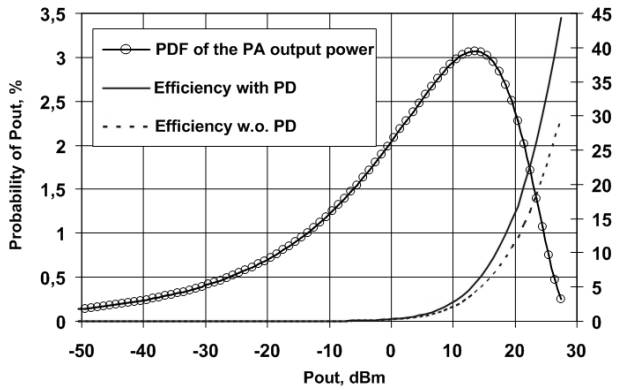

Fig. 6. Probability of PA output power occurrence in UMTS and the efficiency with and without PD at these output powers.

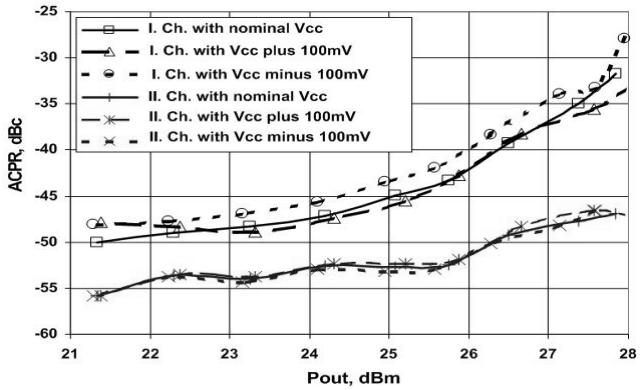

Fig. 7. ACPR measurements of the linearized PA with changing supply voltage.